REPORT CTSL– 17

A MULTIFOLD COINCIDENCE-VETO CIRCUIT USING TRANSISTORS

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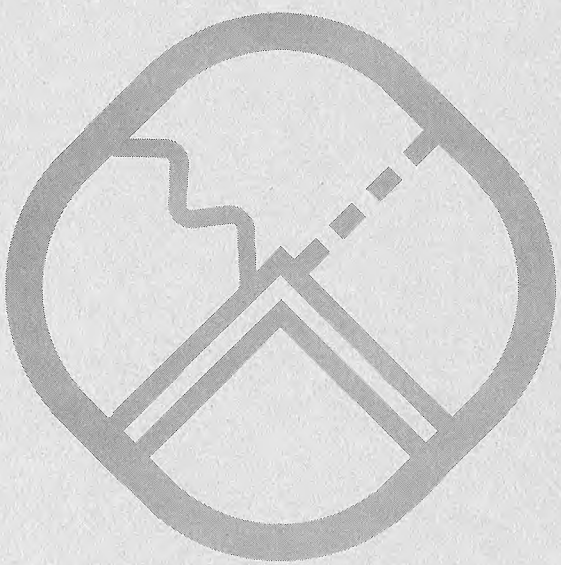

SYNCHROTRON LABORATORY

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Report CTSL-17

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Arpad Barna, J. Howard Marshall, and Matthew Sands

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Abstract

A versatile coincidence-anticoincidence circuit in the 50 nsec time range is described capable of being used with large number of counters. Basic considerations with detailed circuits, operation and performance are given.

1. INTRODUCTION

This paper describes a coincidence anticoincidence circuit designed primarily for use with counter telescopes at the Caltech 1.5 Gev electron synchrotron. It has been used successfully to set amplitude windows on pulses from counters in counter telescopes containing up to nine counters. In such counter telescopes, this circuit allows the precise determination of dE/dx, range, and particle type. The absolute stability of the circuit being better than 2 per cent, narrow windows and stringent requirements on pulse heights are possible. The resolving time of the fourfold coincidence circuit is 40 nsec, that of the four fold veto circuit is 75 nsec. Secondary operations are possible in the 0.5 μsec time range.

Because of its high complexity, the circuit is constructed using transistors. This reduces the size and power consumption and greatly increases the reliability and freedom from maintenance encountered in vacuum tube circuits.

The circuits are built on plug-in boards with a large degree of versatility in the wiring between boards. This allows the system to be programmed in many different ways.

The input can be driven from the output of a fast coincidence circuit or directly from a photomultiplier tube without the need for a preamplifier.

Fig. 1 shows the basic block diagram of the system.

The amplifier (Fig. 2) has a maximum gain of 250.

The triggering levels of the discriminators are adjustable from 1 to 10 volts. The outputs are 50 nsec wide negative pulses with 15 nsec risetime and 6 volt amplitude.

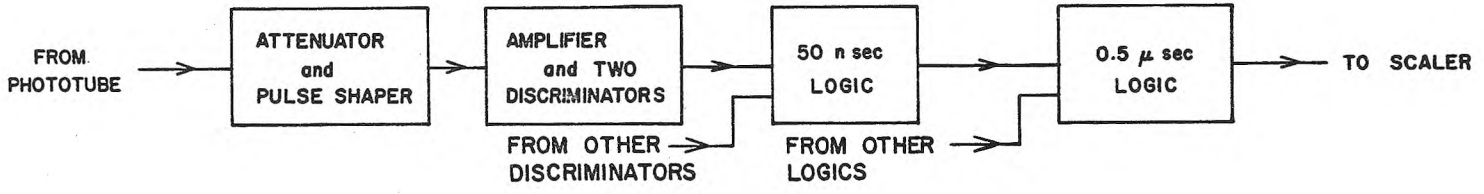


FIG. 1. SIMPLIFIED BLOCK DIAGRAM.

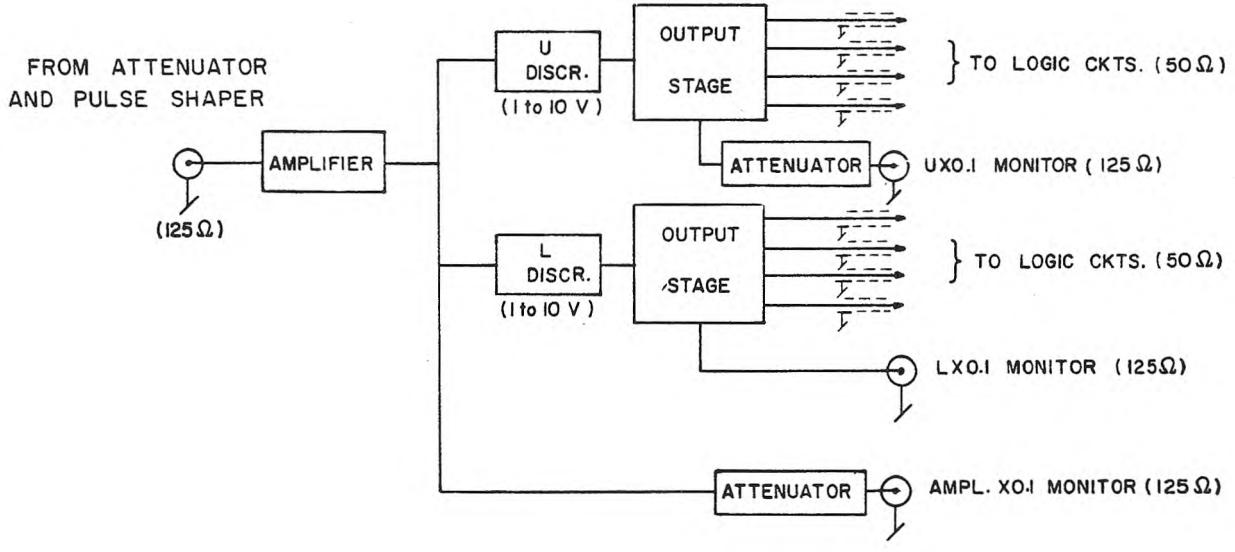


FIG. 2. AMPLIFIER and DISCRIMINATOR.

The 50 nsec logic (Fig. 3) has 4 pairs of inputs. Coincidence and veto can be selected between two of a pair, with a possibility for redundancy to check proper operation. Both vetoed and non-vetoed outputs are available. The pulse shape is critically damped to 0.5 μsec width with 2 volts negative amplitude.

The slow logic (Fig. 4) provides secondary coincidence and vetoes between outputs of 50 nsec logic or slow logic circuits.

2. CIRCUITS

2.1 Attenuator (Fig. 5)

The attenuator consists of 125 ohm π networks with a maximum attenuation of 100, attainable in 12 per cent (1 db) steps.

A coarse and a fine attenuator is provided. For attenuations larger than 10, double π networks are used for better transient response.

The values of the resistors are shown in Table I.

2.2 Pulse shaper and inverter (Fig. 6)

The pulse shaping circuit is an RLC combination.

When the output is loaded by 125 ohms, the input has a resistive impedance of 125 ohms, and the output current in response to an input $i_{IN} = Q\delta(t)$ is

$$i_{out} = (Q/_{2\tau})(t/\tau)e^{-t/\tau}$$

This response has $T_R = 0.56\tau$, $T_{1/2} = 2.4\tau$, and $T_{max} = \tau$. For this circuit $\tau = 20$ nsec. The curves of Fig. 7 give the response of the 50 nsec shaper to an input pulse with an exponential decay time constant of $k\tau$; similarly for a circuit with a δ function response of $e^{-t/k\tau}$, they give the output

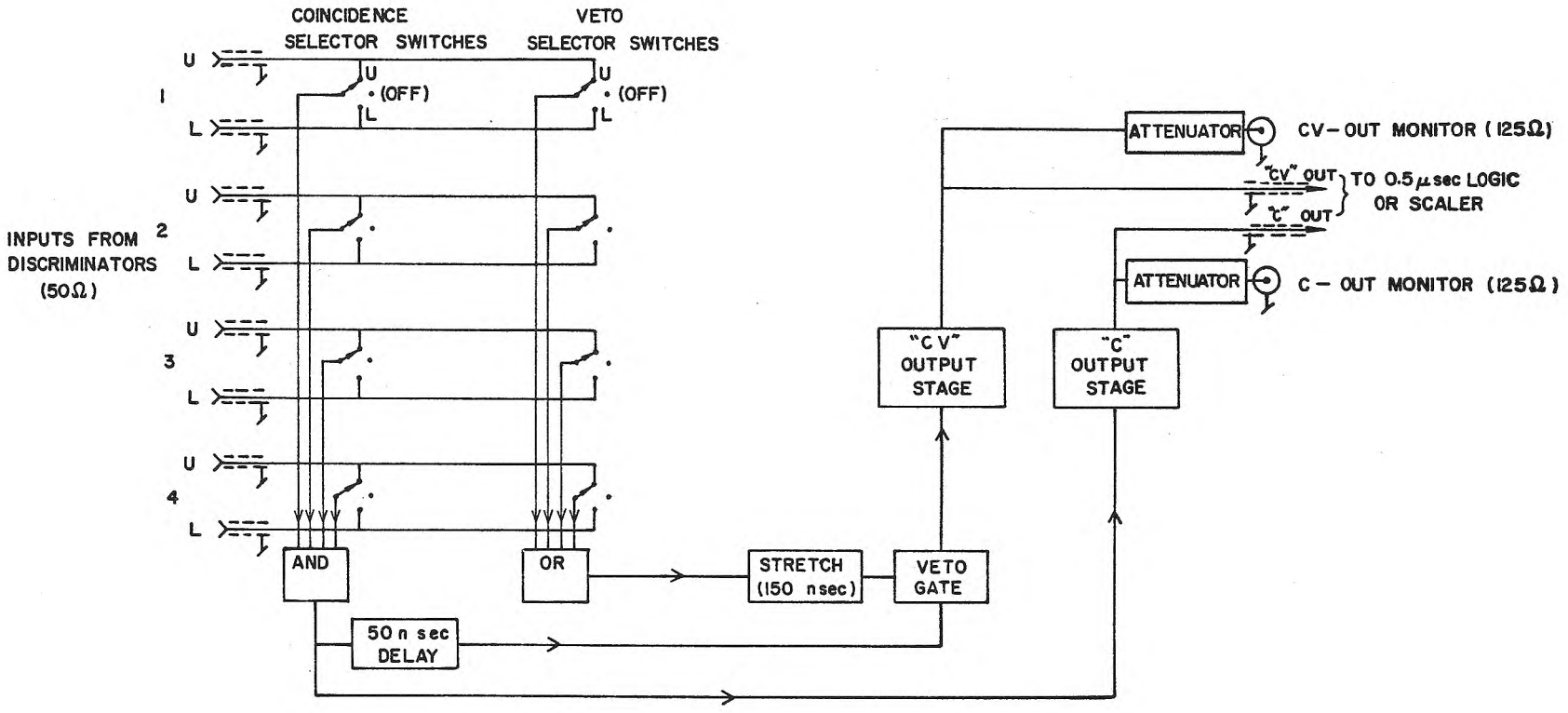


FIG. 3. 50 n sec LOGIC

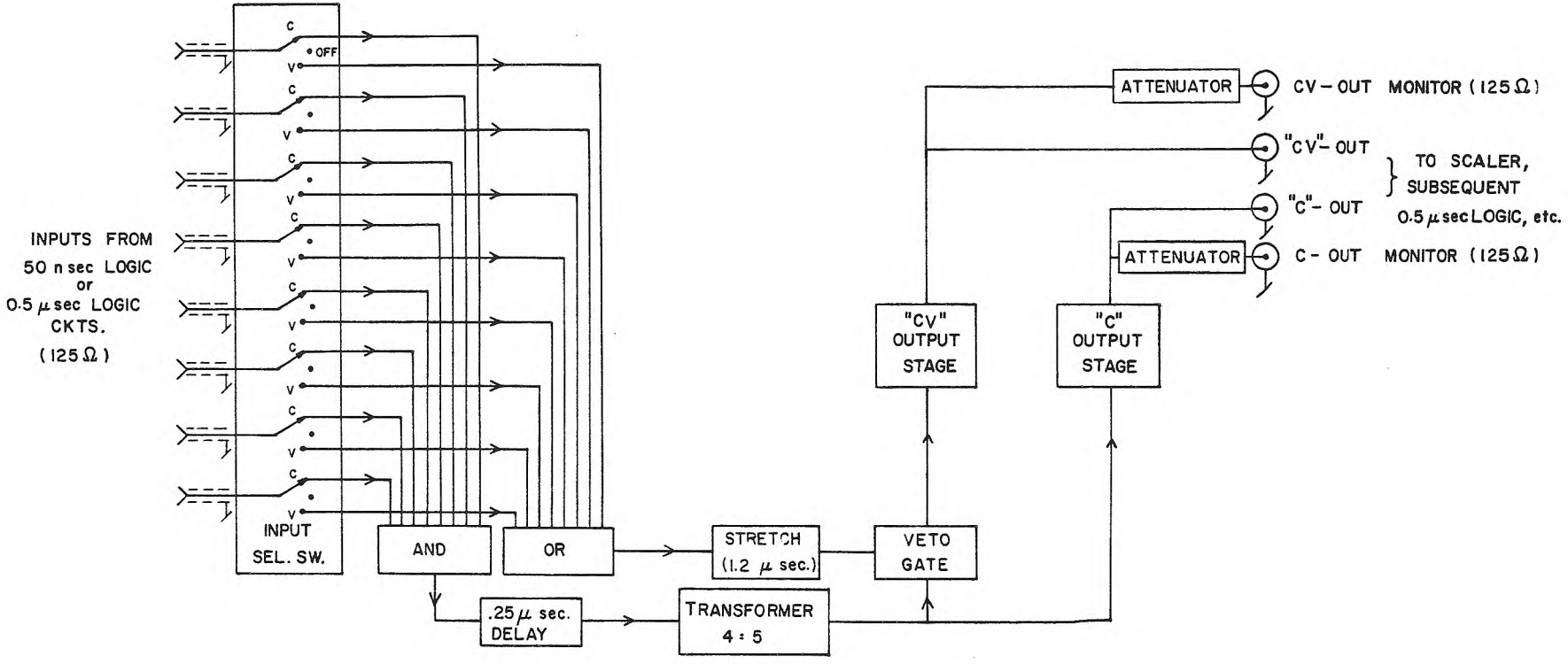


FIG. 4. 0.5 μ sec LOGIC.

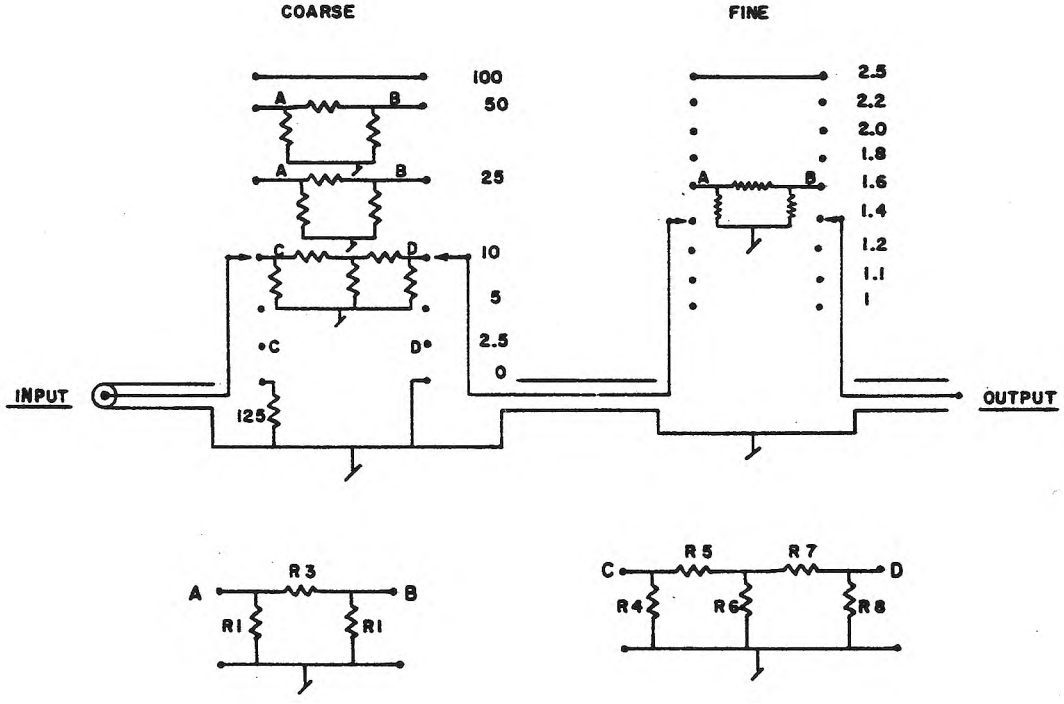


FIG. 5. ATTENUATOR.

TABLE I.

Switch Position	R_1	R_3	R_4	R_5	R_6	R_7	R_8
Coarse							
100	∞	0					
50	375-P	95-P					
25	210-P*	235-P					
10			300-P	125-P	120-P	250-P	200-P
5			190-P	300-P	100-P	235-P	200-P
2.5			172-P	385-P	85-P	385-P	172-P
Fine							
2.5	∞	0					
2.2	2.2k	15					
2.0	1.1k-5%	30-P					
1.8	750-5%	43-5%					
1.6	560-5%	62-5%					
1.4	440-P	77.5-P					
1.2	375-P	95-P					
1.1	330-P	110-P					
1	292-P	130-P					

* -P denotes one per cent resistor.

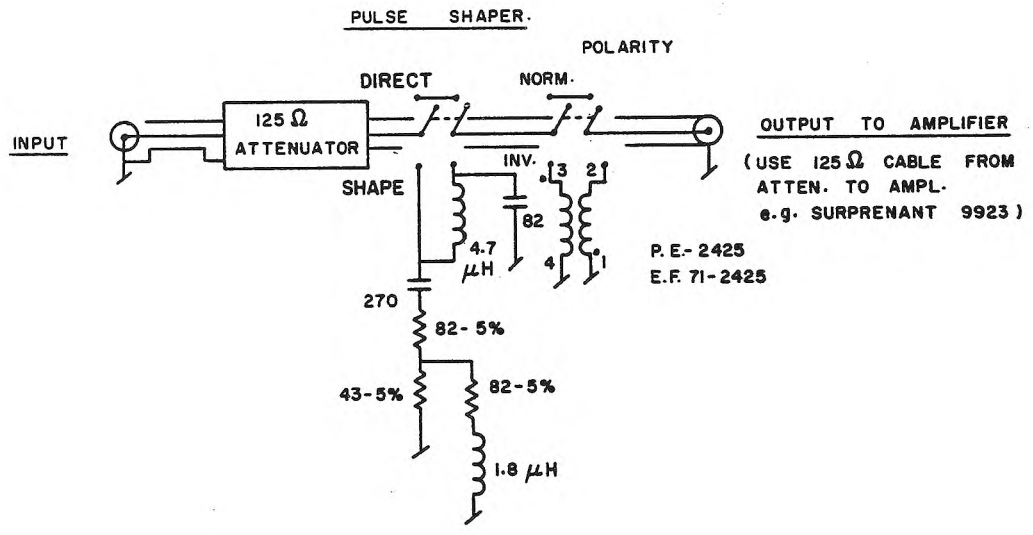


FIG. 6. INVERTER AND SHAPER.

for a 50 nsec shaper pulse.

The curves of Fig. 8 are derived from Fig. 7 and show the dependence of the delay, rise time and amplitude loss on the exponential time constant.

Since the amplifier rise time is not stabilized by feedback, it is not desirable for the output amplitude to be strongly dependent on the amplifier rise time. The curves in Figs. 7 and 8 with k = 0.25 ($k\tau$ = 5 nsec) approximately give the effect of the amplifier rise time (10 per cent to 90 per cent $\approx$ 11 nsec) on the pulse shape. For this use the amplitude loss at the peak is about 5 per cent, and thus $\pm$ 20 per cent variations in amplifier rise time will produce a $\pm$ 1 per cent effect on the peak amplitude.

The finite rise time also causes timing jitter for different input pulse heights. For $k\tau$ = 5 nsec (T_R = 11 nsec) the peak of the pulse occurs at 27 nsec, limiting the timing jitter to a maximum of 27 nsec. For the same reason wide input pulses should not be used with the shaper. Photomultiplier tube pulses with a half-width of about 10 nsec correspond to a k of approximately 0.3, and thus produce an acceptable response. For 10 nsec wide input pulses, maximum timing jitter on the output of the discriminator was found to be 30 nsec. This limits the coincidence resolving time to longer than 30 nsec.

The inverter consists of a 1:1 pulse transformer (PE-2425). The transformer can be switched in or out of the signal path. For a 125 ohm load, it has a 4 nsec rise time and 3 per cent droop at 50 nsec.

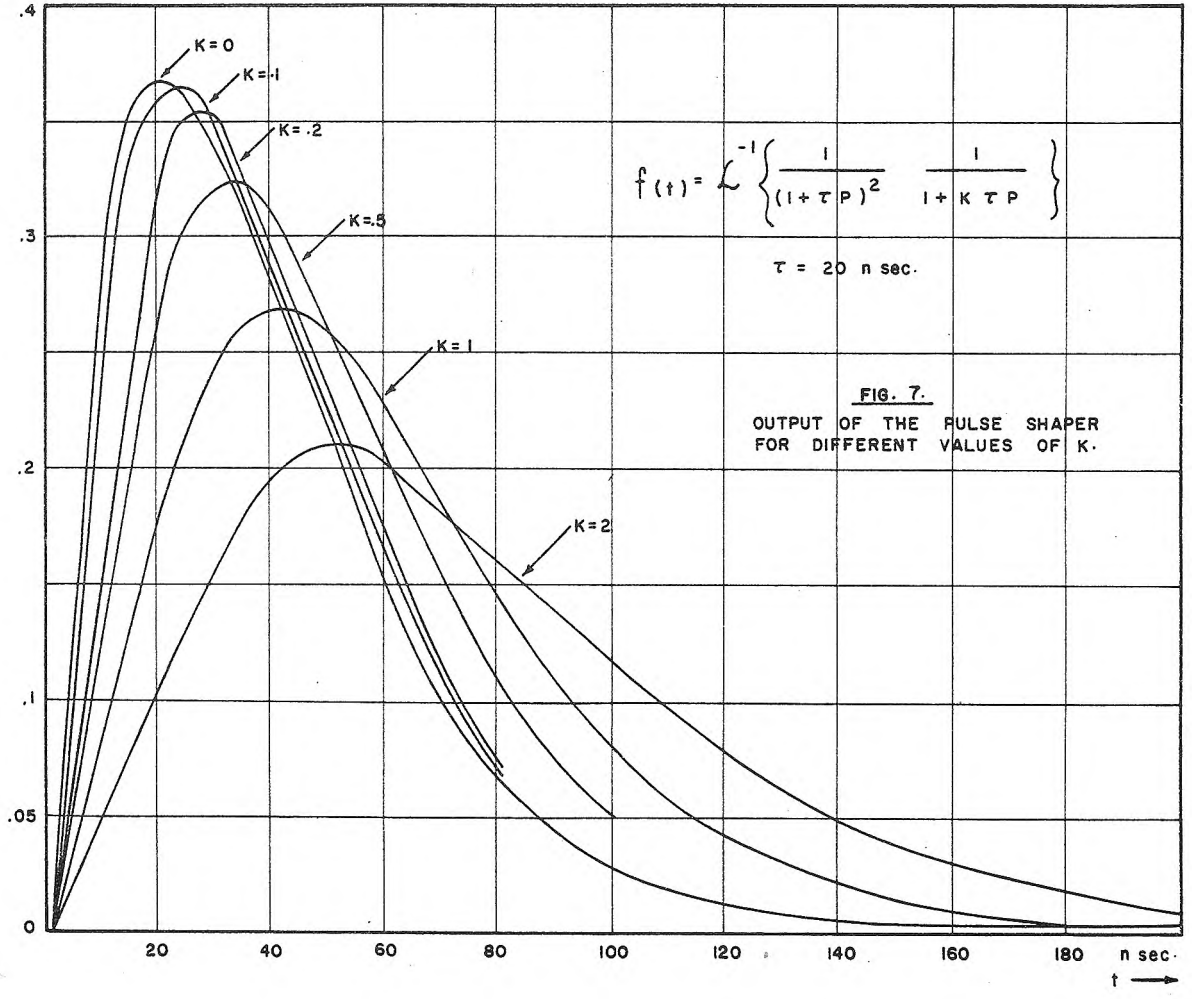
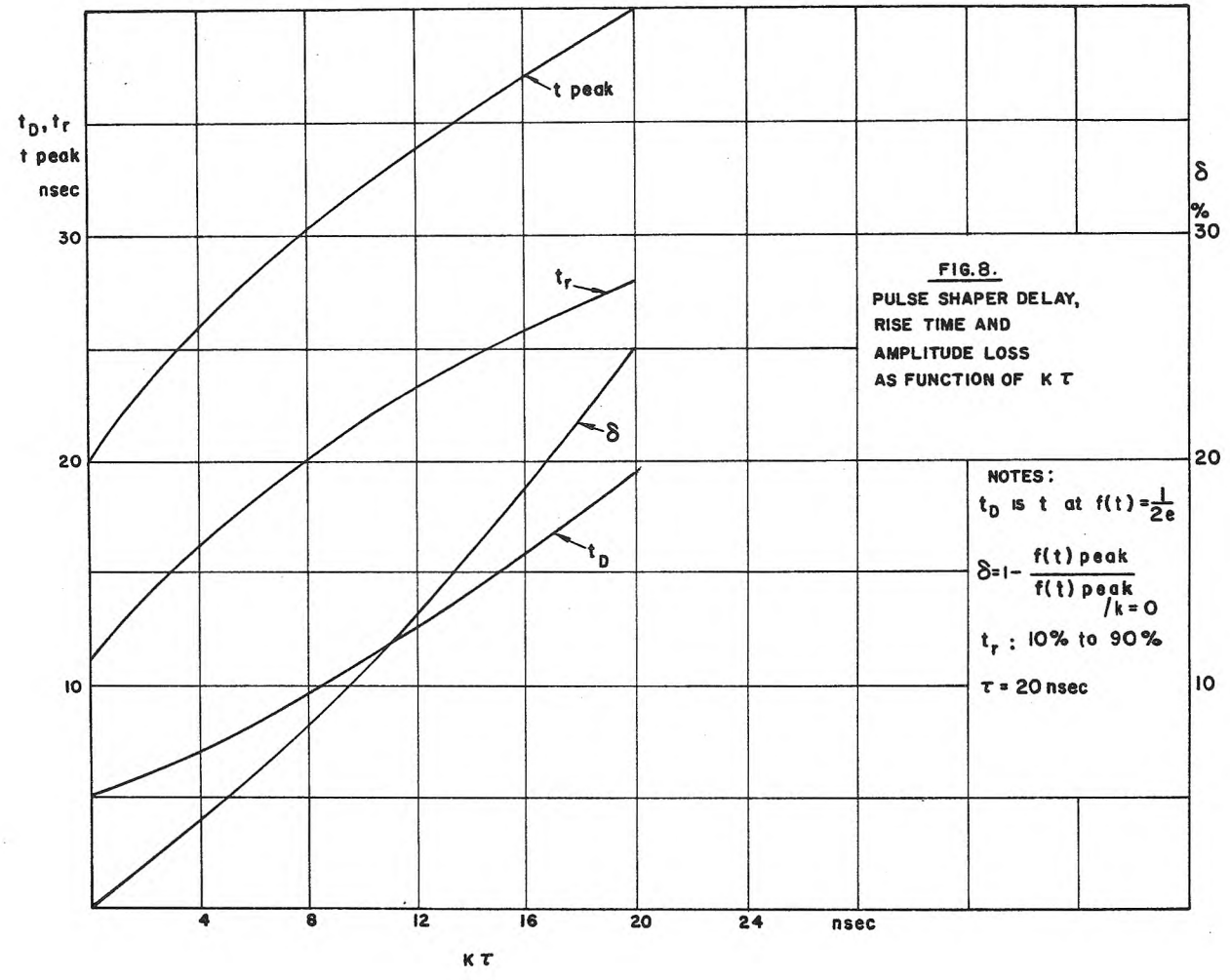


FIG. 7.
OUTPUT OF THE PULSE SHAPER FOR DIFFERENT VALUES OF K.


t_D, t_r
t peak
nsec
30
20
10
δ
%
30
20
10
t peak
t_r
δ
t_D
4
8
12
16
20
24
nsec
Kτ
FIG.8.
PULSE SHAPER DELAY,
RISE TIME AND
AMPLITUDE LOSS
AS FUNCTION OF Kτ
NOTES:
t_D is t at $f(t)=\frac{1}{2e}$
$\delta=1-\frac{f(t)\text{ peak}}{f(t)\text{ peak}/k=0}$
t_r : 10% to 90%
τ = 20 nsec

2.3 Amplifier (Fig. 9)

The amplifier consists of two stages, with a total gain of 250. For large input signals the first stage can be bypassed and the output stage, which has a gain of 5, can be used alone. The transient response is adjusted so that, with an input pulse with a 12 nsec rise time, the rise time of the output pulse is typically 17 nsec for a gain of 250, 15 nsec for a gain of 5; with overshoots and ringing less than 5 per cent.

The absolute value of the gain is within $\pm$ 5 per cent of the nominal value, the linearity better than $\pm$ 1 per cent, for output pulse heights $<$ 10v. The input impedance is 125 ohms $\pm$ 5 per cent. The output impedance $<$ 15 ohms; the maximum duty cycle is 10 per cent. The temperature drift of the amplification is less than $\pm$ 1 per cent for a temperature change of $\pm$ 10°C. The operation is as follows:

First stage:

With the amplification switch in the 250 position, T_1, T_2, and T_3 form a current feedback amplifier with a feedback current gain of 50. T_2 and T_3 each give a current gain of β[1]. T_1 isolates the output from the input, preventing back interaction and, since it is a grounded base stage, it has a current gain of α. The emitter of T_2 is capacitively grounded, making it a grounded emitter stage for signals. The coupling capacitor 0.01 μ from the collector of T_2 to the base of T_3 is chosen to

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1) Symbols and equivalent circuits are discussed in: A. Barna, J. H. Marshall, M. Sands: Nuclear Instruments and Methods 7 (1960) 124-134.

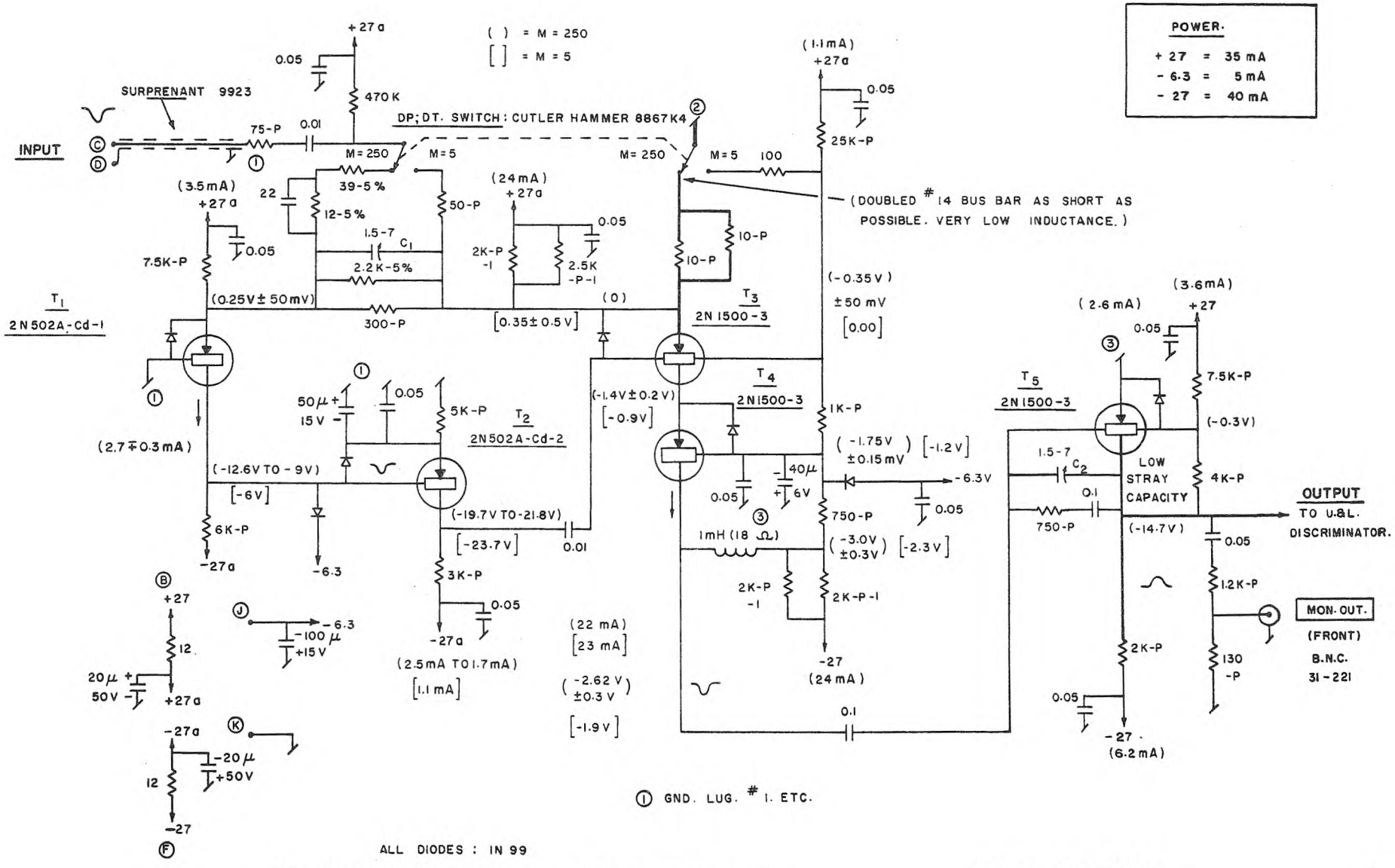


FIG. 9. AMPLIFIER.

give a closed loop decay time constant greater than 100 μsec. The signal emitter current of T_3 then divides between the 5 Ω to ground and the 264 Ω back to the emitter of T_1. Thus, the open loop gain is $M_o \cong \alpha_1\beta_2\beta_3 = 1200$ and the feedback gain:

$$M_f = \frac{R_F}{R_L} \frac{1}{1 + \frac{R_F}{R_L}\frac{1}{M_o}} = 50$$

where R_F = resistor from e_1 to e_3 = 264 Ω and R_L is the resistor from e_3 to ground (5 Ω). This gives a feedback factor $F = \frac{M_o}{M_f} = 24$ and an input impedance to the emitter of T_1 of $\frac{r_e}{F} \approx 0.2$ Ω for times longer than 20 nsec. Thus, for the total input impedance one has $R_{IN} = 120$ Ω, and the long time response is determined by the 0.01 capacitor at the input. Capacitor C_1 is set for optimum transient response. The rise time can be estimated:

$$T_{R_I} \cong \frac{2.2\tau_o\sqrt{\beta_2^2 + \beta_3^2}}{\sqrt{F_1}} = 11 \text{ nsec}$$

where $\tau_o = \frac{\tau\beta}{\beta} \cong 0.5$ nsec, τ_β is the β time constant.

With the amplification switch in the 5 position, the signal is fed into the emitter of T_3 whose base has now been grounded to eliminate T_1 and T_2 from the loop. The 5 Ω resistor is disconnected from ground to prevent its loading the input. T_3 then has a current gain of α_3 which is nearly 1(~ 98 per cent) and an input impedance of the order of 1 Ω.

Second stage:

T_4 acts as an isolation stage between the first stage and T_5, and it presents a low impedance to the collector of T_3 and a high impedance

to the base of T_5. It has a current gain of α_4 (~ 98 per cent).

T_5 is a single transistor feedback stage with an open loop current gain of β_5 and a feedback transfer impedance R_T given by:

$$R_T \approx R_F \left[\frac{1}{1 + \frac{R_F}{\beta_5 R_L}} \right]$$

R_F = feedback resistor from collector to base = 630Ω

R_L = load impedance from collector to ground ~ 500 Ω (includes two discriminators)

$$R_T \approx \frac{630}{1.017} = 625\ \Omega$$

The feedback factor F is given by:

$$F = \frac{\beta_5 R_L}{R_F} \cong 60$$

This gives an output impedance of:

$$R_{out} \approx \frac{R_F}{\beta_5} = 8.5\ \Omega$$

Capacitor C_2 has a similar function as C_1.

The output impedance of T_5 actually looks inductive with an inductance in series with $R_{F/\beta}$ of $R_F \tau_o$ where

$\tau_o \approx \tau_{\beta/\beta}$ and τ_β = β-rise time constant.

$\tau_o \approx 0.5$ nsec

This inductance will cause ringing if the stray capacity on the collector of T_5 is in excess of about 5 pf.

For signals small enough so that T_5 operates linearly, the rise time

of the second stage can be estimated as being:

$$T_{R_2} \sim 2.2\, R_F(C_c + C_2)$$

where C_c = collector to base capacity of the transistor T_5.

For $C_c + C_2 = 5$ pf:

$$T_{R_2} \sim 7 \text{ nsec.}$$

The DC currents through T_1 and T_2 are stabilized with emitter resistors; the emitter of T_2 is by-passed to ground capacitively so as to make it a grounded emitter stage for fast signals. The current through T_5 is stabilized by D.C. feedback from the collector to the base.

With the amplification switch in the 250 position, the current and dissipation of T_3 and T_4 are stabilized by D.C. feedback from the collector of T_4 to the base of T_3. The voltage of the base of T_4 is determined by a voltage dividing chain from the collector of T_4 to the base of T_3. The emitter of T_3 is essentially grounded through the 5 Ω resistor. In the amplification = 5 position, the current is stabilized by the 2K and 2.5K resistors in the emitter of T_3. The D.C. feedback is disconnected by grounding the base of T_3. The base voltage of T_4 is derived from a voltage divider chain as before.

All diodes (IN99) in the amplifier are protective.

2.4 Discriminator (Fig. 10)

The discriminator has a minimum useful input range of 1 to 10 volts with a linearity better than 0.1 v. The change in triggering level for constant amplitude pulses having widths of 20 ns and 200 ns is < 10mV;

for widths of 20 ns and 10 ns it is < 0.15 V. The change in triggering level, for a pulse arriving more than 150 nsec after the preceding one, is less than 0.1 V., for 100 nsec less than 0.75 V. The temperature dependence of the triggering level is < 5 mv/°C. The maximum continuous duty cycle is 10 per cent.

The output pulse height is -6.5 V ± 10 per cent with 50 nsec pulse width and less than 15 nsec rise and fall times. The discriminator consists of a window amplifier, whose output current is differentiated and used to trigger a univibrator, which drives the output stage.

The operation of the circuit is as follows:

Window Amplifier -

Transistors T_6 and T_7 form a long tail pair which, combined with the input diodes (D_1, D_2, D_3, D_4) form a window amplifier. A current of 3 mA is stabilized through D_3 by a resistor (8.2K) to -27 v. This current comes partly from D_4 and partly from resistors. D_2 is back biased by a voltage derived from an emitter follower (T_{13}). In case of high repetition rates, D_1 recovers the input capacitor (0.01), the discharge current flowing into the low impedance seen at the emitter of T_{13}. The 1 mA current through D_4 pulls the base of T_6 about 1/4 v negative, thus guaranteeing that the 10 mA current stabilized through the resistor (2.7K) to + 27 v all flows through T_6, leaving T_7 cut off.

The window amplifier starts to give an output when the input voltage becomes sufficiently positive, so that there is about 1 ma current flowing in D_2, causing D_4 to cut off. The maximum current of the window amplifier is 10 mA when the signal cuts off T_6. Larger positive inputs cause D_2 to

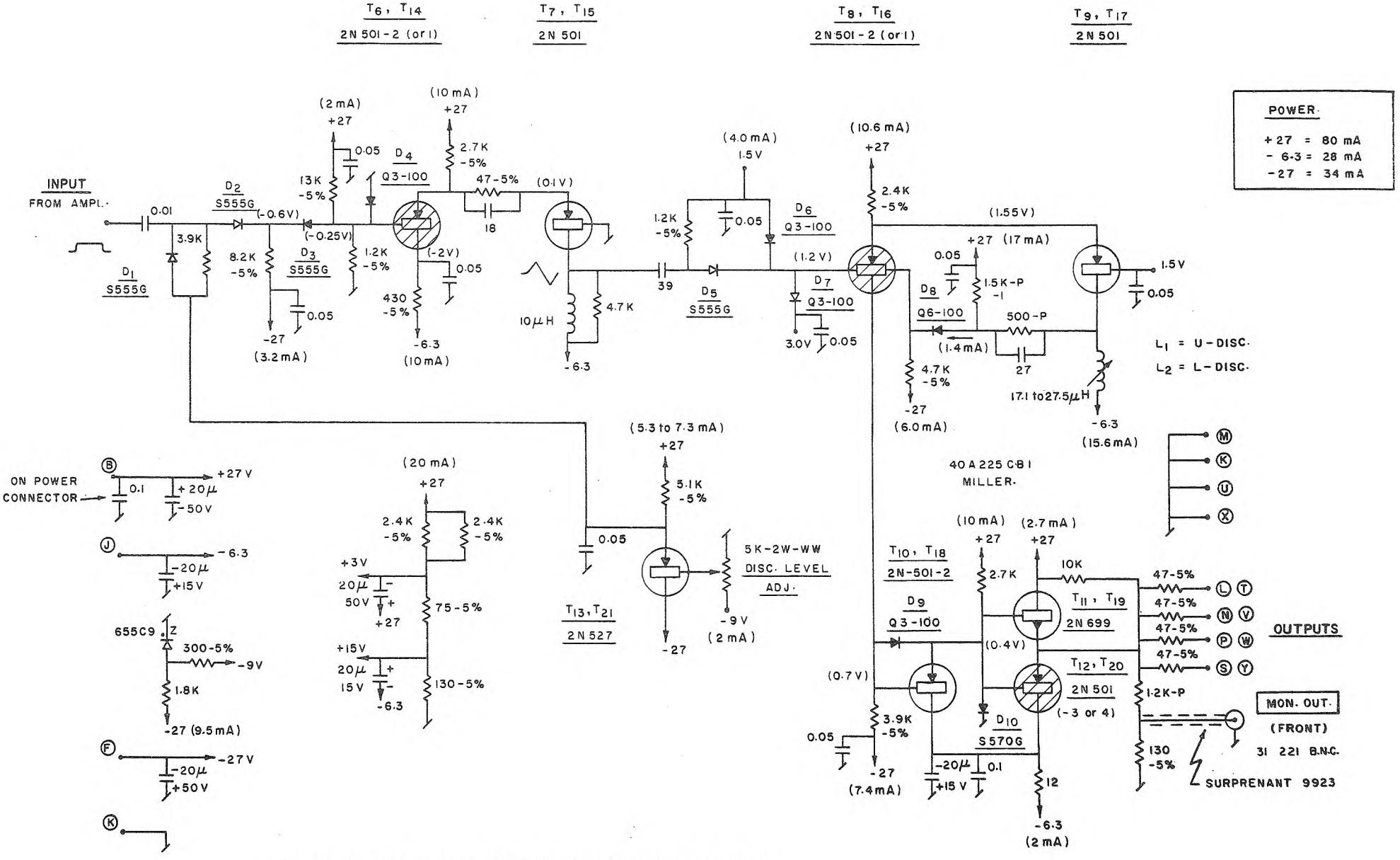


FIG. 10. DISCRIMINATOR.

draw the entire 3.2 mA of the 8.2K resistor, cutting off D_3 and disconnecting T_6 from the input. The base of T_6 goes to + 2.2 v and its emitter is at about + 0.7 v, safely cutting off T_6 without exceeding its maximum base-emitter back voltage of 2 v.

Temperature drifts in the emitter-base voltage of T_6 and T_7 tend to cancel each other, since the univibrator triggers at about 5 mA out of the 10 mA total current of window amplifier. This condition of equality is independent of the emitter-base voltage drop for identical transistors. Similarly, the voltage drifts of D_2 and D_3 tend to cancel each other, since they oppose each other. The principal temperature drift comes from T_{13} whose emitter base voltage drifts at about the rate of 2 mV/1°C. For a temperature swing of $\pm$ 10°C., this yields $\pm$ 20 mV.

The 47 Ω, 18 pf RC circuit between the emitters of T_6 and T_7 produces negative feedback, decreasing the rise time at the expense of transfer impedance according to the law:

$$T_R R_T = 2.2\tau_o(R_s + 2R_b)$$

$$R_T = \frac{V \text{ in}}{i \text{ out}} = \text{transfer impedance}$$

R_s = source impedance including forward resistance of D_2 and D_3.

R_b = base spreading resistance of the 2N501

T_R = 10 per cent to 90 per cent rise time

$\tau_o = \tau_{\beta/\beta} = 0.8$ nsec.

The circuit used has a transfer impedance of about 70 Ω and T_R ~ 10 nsec. The fast rise time is necessary to reduce the pulse width dependence of the triggering level.

Pulse Shaper -

The output of the window amplifier is shaped by the 10 μH choke and the 39 pF capacitor. Diode D_5 is normally slightly conducting and a low impedance path exists through D_5 and D_6 to A.C. ground. Under these conditions the LC circuit is undamped and has a sinusoidal response with a period of 70-80 nsec. When the signal current through the 39 pF condenser reverses sign, it cuts off D_5, leaving an impedance of 1.2K to ground, which is large enough to overdamp the response of the LC circuit, causing it to decay exponentially back to its D.C. level. Also, diode D_5 disconnects the trigger pulse from the univibrator after 35 nsec, allowing the univibrator's pulse width to be independent of the input pulse width even for long input pulses.

The damping of the pulse shaper response is critically dependent on stray capacity across the 10 μH choke. In order to reduce this effect, the choke is bypassed by 4.7K, providing additional damping.

Univibrator -

Transistors T_8 and T_9 form a long tail pair with positive feedback from the collector of T_9 to the base of T_8, making a univibrator. A current of 4.6 mA is drawn through D_6 causing T_8 to conduct all of the 10.6 mA with T_9 cut off. D_8 is conducting a current of about 1 mA.

The circuit triggers when a trigger pulse greater than 4.6 mA unhooks D_6 and causes current to flow in T_9. For short times the 20 μH

presents a large impedance, and all of T_9's current flows back to the base of T_8. This positive feedback continues to increase the current of T_9 until T_8 cuts off. The base of T_8 is clamped by D_7 and a low impedance path exists from the 500 Ω resistor to A.C. ground through D_7 and D_8. The 20 μH choke, 500 Ω resistor, and 27 pF condenser form a critically damped network causing the current through D_7 to decrease with time. After about 22 nsec, the current through D_7 reaches zero, causing it to unhook, leaving about 1.2K impedance to ground. The 20 μH choke continues discharging through this impedance for another 5 nsec, at the end of which time D_6 starts conducting and T_8 starts taking current from T_9. Thus, the circuit starts to trigger back in about 27 nsec. Since the circuit has a rise and fall time of about 10 nsec, this gives a total width at half maximum current (i.e., 5 mA) of:

$$T_{1/2} = 1/2\ (10 + 10) + 27 = 37 \text{ nsec}$$

After the circuit triggers back, D_8 unhooks the choke (20 μH), recovers through a 2K resistance and disconnects all but about 1 mA of its current from the biasing diode D_7. The higher impedance causes the choke to recover faster, and the fact that its current is no longer flowing in D_7 allows the circuit to be immediately retriggered. After 100 nsec, the choke is recovered and D_8 starts conducting again and the univibrator operates normally. For a trigger pulse less than 100 nsec after the first triggering pulse, the circuit will retrigger, but its pulse width is too short, due to residual current still flowing in the choke.

Output Stage -

Transistor T_{10} is normally cut off by the forward voltage drop of D_9 with its emitter clamped at 0.4 v by D_{10}. When the univibrator is triggered, the 10.6 mA from the collector of T_8 is turned off, causing the base of T_{10} to be pulled to -27 v through the 3.9k resistor. This unhooks D_{10} and the emitter follows the base toward -27 v and stops at -6.1 v when the transistor (T_{10}) saturates. The fact that T_{10} saturates causes its storage time to be added to the half width of the output pulse. The storage time is specified as 13 nsec for the 2N501, resulting in:

$$T_{1/2\ \text{output}} = 37 + 13 = 50 \text{ nsec}$$

The rise time can be estimated as follows, for times short compared to $\tau_\beta = 40$ nsec.

$$T_R \approx \tau_o \sqrt[3]{\frac{6CV}{I_o \tau_o}} = 11 \text{ nsec}$$

where C = load capacity (370 pF for four logic circuits and connecting cable).

V = output voltage (6.5 v)

I_o = input current (7 mA)

$\tau_o = \tau_{\beta/\beta} = 0.8$ nsec

If one includes a 10 nsec rise time for the input current:

$$T_R \approx \sqrt{(11)^2 + (10)^2} = 15 \text{ nsec}$$

2.5 50 nsec logic (Fig. 11)

The logic is a fourfold coincidence circuit with four veto inputs. There are two outputs, one for coincidence with veto and the other for coincidence without veto. The coincidence resolving time is 37 ± 5 nsec, the veto resolving time is 50 to 75 nsec, both defined as half width of the delay curve at half height.

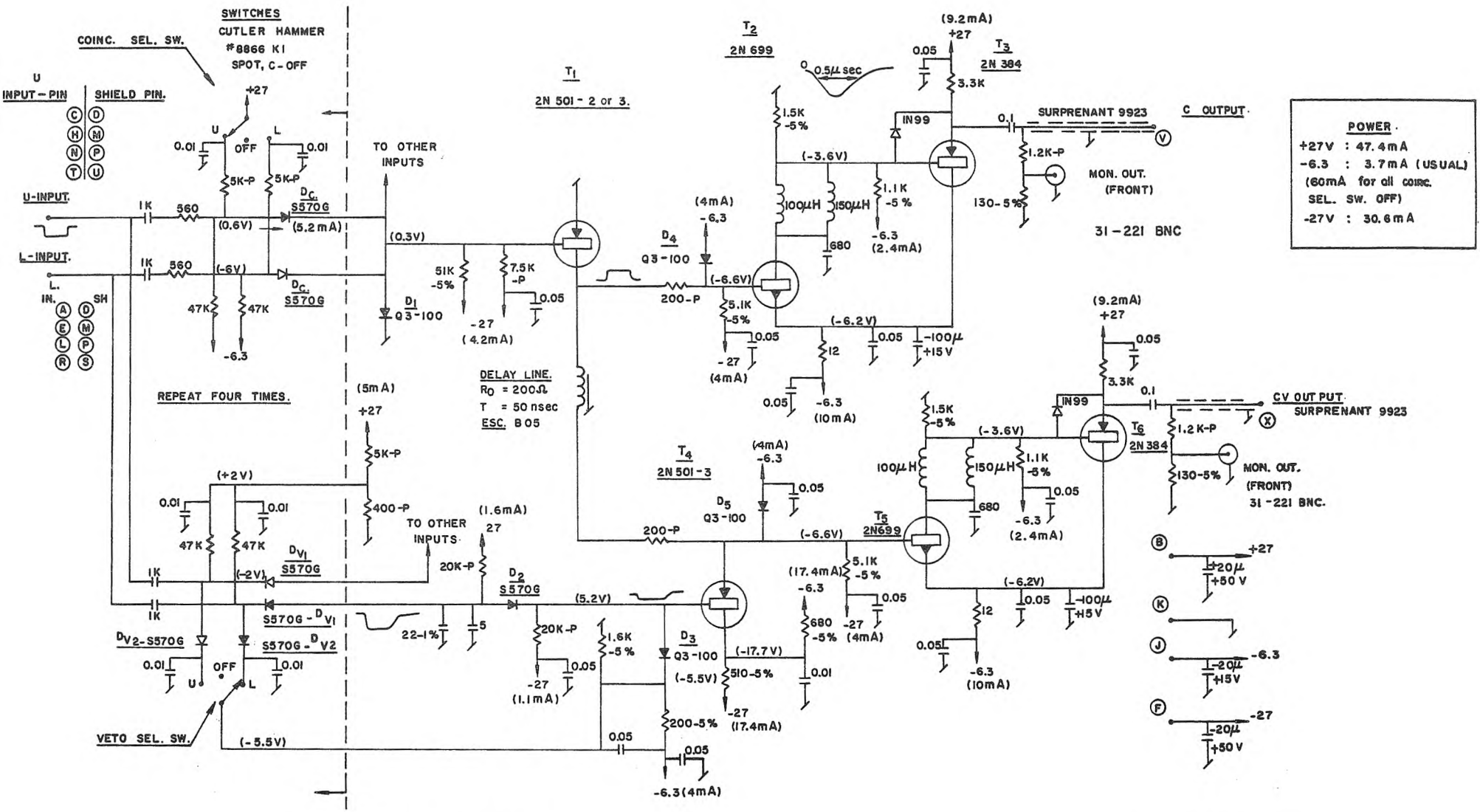
The output pulse is a critically damped -2.2 V ± 15 per cent pulse with a width of 0.4 to 0.5 μsec at half height and the peak at 0.2 μsec. The output for vetoed coincidence is typically ± 20 mv. The maximum continuous counting rate is 1 mc. The output impedance is < 20 ohms, and the output should not be loaded by more capacity than 300 pF.

The operation of the circuit is as follows:

Coincidence circuit -

The coincidence circuit is primarily an "And" circuit requiring the presence of certain pre-selected inputs in order to get an output.

The transistor T_1 is cut off by the forward voltage drop of D_1(Q 3-100). The D.C. current in D_1 is determined by the coincidence selector switch and the 4.2 mA drawn through resistors (7.5k-P, 51k-5 per cent) to -27 v. Whenever a coincidence selector switch is in either a "U" or an "L" position (i.e., not off), it causes 5.2 mA to flow from + 27 v through the coincidence control diode (D_c-S570G). Of the total current flowing through the eight D_c diodes, all but 4.2 mA normally flows through D_1. Thus, there can be from 1 mA (for only one coincidence selector switch not off) to 16.6 mA (for no switches off) flowing in this diode. In the case where all switches are off, the 4.2 mA pulls T_1 into



ALL RESISTORS ½ W 10% UNLESS OTHERWISE NOTED.

ALL CAPACITORS CERAMIC 50V DISK UNLESS OTHERWISE NOTED.

FIG. 11. 50n SEC. LOGIC.

saturation.

When a D_c diode is connected to + 27 v through 5k by the coincidence selector switch, thus conducting 5.2 mA, it can be cut off by a negative signal which will absorb its 5.2 mA. The cathode of the D_c diodes (i.e., base of T_1) shifts only about 0.6 v from D_1, conducting 17 mA to T_1 saturated. Thus, the required voltage at the input to cut off a D_c diode is approximately 560 Ω x 5.2 mA = 3 v. When a D_c diode is not connected to + 27 v through 5k by the coincidence selector switch, its anode is pulled to -6 v by a resistor (57k) to -6.3 v. Thus, any negative signals at its anode have little effect on the base of T_1. (It would take a positive stray signal of + 6 v to turn the diode on.)

To turn on T_1, D_1 must cut off and the 4.2 mA current then pulls T_1 into saturation. This can happen only if all the D_c diode currents are simultaneously zero. This means that one gets an output only if there are simultaneous signals of at least -3 v on all inputs which are connected to + 27 v through 5k by their coincidence selector switches. Thus, one has provision for making one to four-fold coincidence, depending on the setting of the coincidence selector switches.

When T_1 saturates, it sends a current of 30 mA toward the base of T_2, cutting off D_4 and saturating T_2. T_1 also sends a 30 mA current through the 50 nsec delay line toward the base of T_5, unhooking D_5 and saturating T_5 if there is no veto.

Veto Circuit (T_4) -

The veto circuit is primarily an "Or" circuit which vetoes one of the outputs of the coincidence circuit when any of certain preselected

inputs are present.

When no inputs are present, D_2 and D_3 are normally conducting, holding the base of T_4 at -5.2 v and thus cutting it off. If D_2 should become cut off, the 1.1 mA flowing through the resistor (20k) to -27 v then pulls T_4 into conduction, causing about 50 mA to flow through D_5 and its cathode to drop to about -6.9 v. If a coincidence current pulse of 30 mA arrives, it cannot unhook D_5 and thus T_5 does not turn on. The (low) impedance of the voltage divider in the collector of T_4 is chosen so that the D.C. saturation current of T_4 is greater than 30 mA, preventing a loss of veto from pile-up on the collector of T_4.

When the veto selector switch connects the cathode of one of the D_{v_2} diodes to -5.5 v, this pulls the cathode of the D_{v_1} diode connected to it to -5.2 v and turns this diode slightly on. If a negative pulse is applied to the cathode of such a conducting D_{v_1}, then the diode conducts harder, pulling the condenser (27 pF) on the anode of D_2 down to nearly the input voltage. This unhooks D_2 and starts the veto procedure. When the input signal returns to zero, the anode of D_{v_1} is held at about -11 v for a -6 v input signal, while the cathode goes back to -5.2 v. Thus, D_{v_1} cuts off and the 27 pF starts to decay exponentially to + 27 v with a time constant given by 20k x 27 pF = 540 nsec. When the anode voltage of D_2 has reached -6.9 v, D_2 starts conducting again, unclamping T_1 and ending the veto. The diode D_{v_2} presents a low impedance path for positive signals and thus recovers the input 1K condenser for pile-up at high counting rates.

When the cathode of a D_{v_2} diode is left open by the veto selector

switch, then its anode is pulled to + 2 v, thus cutting off the D_{v_1} connected to this input. This blocks input pulses up to -7 v from operating the veto circuit.

Output Circuit ($T_2T_3T_5T_6$) -

The purpose of the output circuit is to convert the short, fast rise pulse from the output of the coincidence circuit (collector of T_1) into a longer, slow rise output pulse useful for driving scalers or the Slow Logic.

The part of the circuit containing T_2 and T_3 is identical with the part of the circuit containing T_5 and T_6 except for the veto transistor T_4. If there is no veto, the outputs of the two parts are the same, and if a veto is present, T_3 gives the same output as if no veto were present, but T_6 gives no output.

Normally T_2 and T_5 are cut off by the forward voltages of D_4 and D_5 respectively. These diodes draw 4 mA determined by resistors (5.1k) to -27 v. In the collectors of T_2 and T_5 are pulse shaping networks which convert a short voltage pulse into an output of the form $V(t) = V_o\, t/\tau e^{-t/\tau}$ where τ = 200 nsec. T_3 and T_6 are emitter followers to prevent load impedances as low as 100 Ω from interfering with the pulse shaping network. The narrow voltage pulse to drive this network is manufactured by saturating T_2 and T_5 with the current coming from the saturation of T_1 at coincidence. As the width of the pulse at the collector of T_1 changes from 10 nsec to 20 nsec, the output pulse amplitude changes from 0.2 V to 2 V.

The pulse arriving at the vetoed coincidence output is delayed

50 nsec by a lumped constant 200 Ω delay line. This more nearly centers the coincidence pulse in the stretched veto pulse if both the coincidence and veto inputs occur simultaneously. (A 40 nsec delay line would have provided a more perfect centering, but none was commercially available.) The cable is nearly terminated on the base of T_5 by a 200 Ω series resistor. The voltage on the base of T_5 changes by about 0.5 v causing a 10 per cent reflection. By the time the reflection reaches the collector of T_1, the coincidence is over and the 200 Ω resistor to the base of T_2 prevents further reflections.

2.6 Slow logic (Fig. 12)

The coincidence resolving time is 0.25 to 0.5 μsec, veto resolving time is 0.5 to 1 μsec. The output pulse is the same within ± 10 per cent to the 50 nsec logic output pulse. The vetoed coincidence output is less than ± 0.1 v. The maximum continuous counting rate is 1 mc. The output impedance is < 20 ohms, the output should not be loaded by more capacity than 300 pF. The operation is the following:

Coincidence Circuit -

The coincidence circuit is a diode "And" circuit with Input Switches to determine which inputs are in coincidence.

When one of these switches is in the "C" position, it connects the particular input to the base of T_3 (2N501-4) through D_c and a 1/4 μsec delay cable. Unless all of the D_c diodes are unhooked, either by a negative input pulse or through the Input Selector Switch being in the "V" or "off" position, the base of T_3 is near ground. If all D_c diodes are unhooked, then the base of T_3 moves to the voltage of the least negative

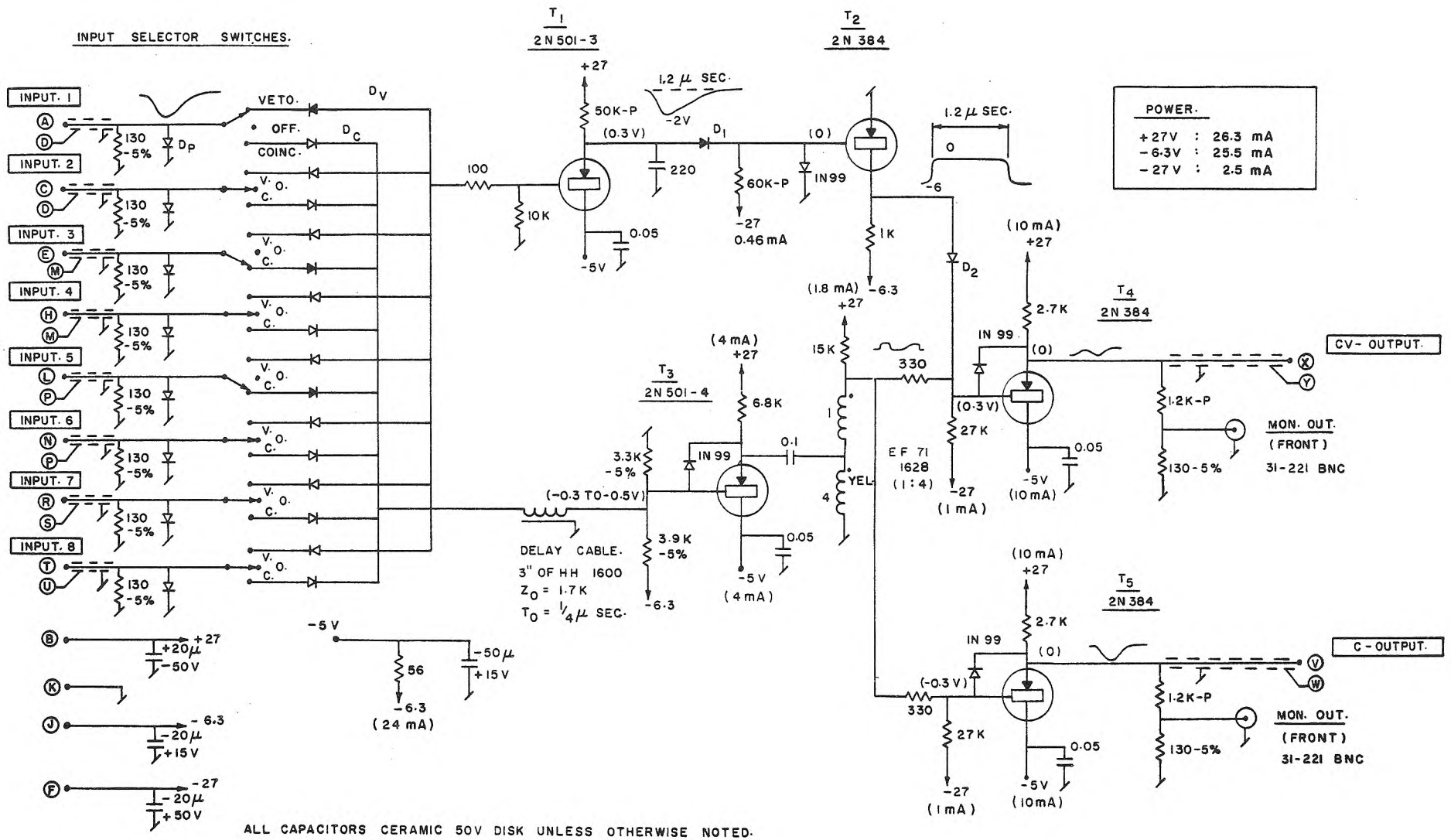


FIG. 12.0.5μsec LOGIC.

input to -3 v, whichever is less negative.

Transistor T_3 is an emitter follower and drives the 1:4 transformer (EF71-1628) which is connected as an auto transformer giving a 25 per cent voltage increase. The purpose of this transformer is to make up voltage losses in the emitter followers and thus give nearly unit gain from the input to the output at coincidence. This makes it possible to cascade slow logic circuits.

The 1/4 μsec delay cable (HH 1600) delays the coincidence inputs with respect to the veto inputs so that the veto pulse will overlap the coincidence pulse. The delay line is terminated in 1.7K at the base of T_3.

The diodes D_p on the input are to recover the capacitors coupling the outputs of the Logic Chassis. This prevents large D.C. drifts on the input at high counting rates. The IN99 diodes from emitter to base of the transistors are all protective.

Veto Circuit (T_1, T_2) -

The veto circuit is a diode "Or" circuit with the Input Switches determining which inputs can veto.

When one of these switches is in the "V" position, negative pulses on its input will pass through diode D_v (IN270) and reach the base of T_1. This charges the stretching capacitor (220 pF) which holds D_1 (IN270) unhooked for 1 μsec after charging. When D_1 is unhooked, the 1/2 mA flowing in the 60K resistor pulls T_2 (2N384) into saturation, raising its collector voltage from -6.3 v to zero. This makes D_2 (IN270) ready to conduct and prevent the passage of negative signals to the base of T_4

(2N384). Thus, the output of T_4 is vetoed by the low impedance of the saturated transistor T_2.

Output Stages (T_4, T_5) -

Both the coincidence output stage (T_5) and the vetoed coincidence output stage (T_4) are emitter followers. They are both connected to the transformer (EF71-1628) by 330 Ω resistors, and the bases are pulled negative by 1/3 v so as to give nearly zero output D.C. voltage.

The vetoed coincidence output stage is coupled by 330 Ω to the transformer so that the delay line termination will not be significantly changed by the low impedance seen at the base of T_4 when a veto is present. For the same reason, T_3 was chosen to be a high beta transistor ($\beta > 100$). The 300 Ω was used in the coincidence output stage so that the two output impedances would be the same when no veto was present.

The collectors of all the emitter followers are decoupled from the -6.3 v supply by 56 Ω and 20 μF to prevent pickup from pulse loading of the supply.

3. CONSTRUCTION

The circuits are built on 16 cm x 20 cm copper plates, having 4 cm x 17.5 cm front panels. Ten of these units plug into a 17.8 cm x 45 cm rack. Signals as well as power lines connect through the rear connector, the monitor coax connectors and the controls are mounted on the front panel. Components are mounted on ceramic terminal strips with coaxial cables and D.C. wires underneath. Care has been taken to keep grounds short. Interconnections between the discriminators and 50 μsec

logic circuits use 50 ohm cable with taper pins; other signal wires 125 ohm cable. It was found necessary to provide low inductance grounds to each chassis in a sliding contact built into the mounting channel.

Fig. 13 shows the unit of an amplifier and two discriminators. The first stage of the amplifier is located at the upper front part, the second stage under it, the two discriminators in the rear part.

Fig. 14 shows the 50 nsec logic. The coincidence and veto diodes are located in the rear and the 50 nsec lumped constant delay line at the upper front part. Six attenuators, pulse shapers and inverters are mounted on a 9 cm panel (Fig. 16).

4. PERFORMANCE

The circuit has been used successfully to identify protons and pions in a six counter telescope at the Caltech synchrotron (Fig. 16). At the present time, this telescope has been expanded to nine counters with dE/dx windows set by this circuit aiding in the detection of 150 Mev K^+ mesons. Plans are being made to make a further expansion of the telescope to 12 to 15 counters and detect higher energy K^+. Experience in the past has shown the circuit to have the high degree of stability and reliability required for such multi-counter experiments demanding narrow amplitude windows.

Extreme care has to be taken to provide reliable power lines (+ 27 V, -27 V, -6.3 V), since the absence of any of them may cause serious damage to the circuit. A safety interlock circuit has been used to ensure simultaneous shorting of all lines, if one fails.

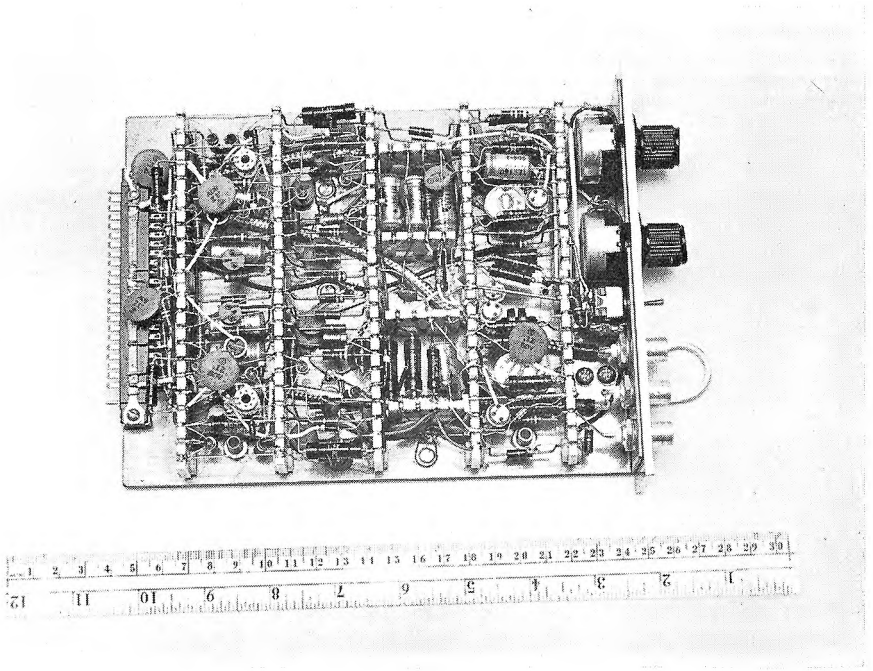


FIG. 13 Unit Consisting of an Amplifier and Two Discriminators

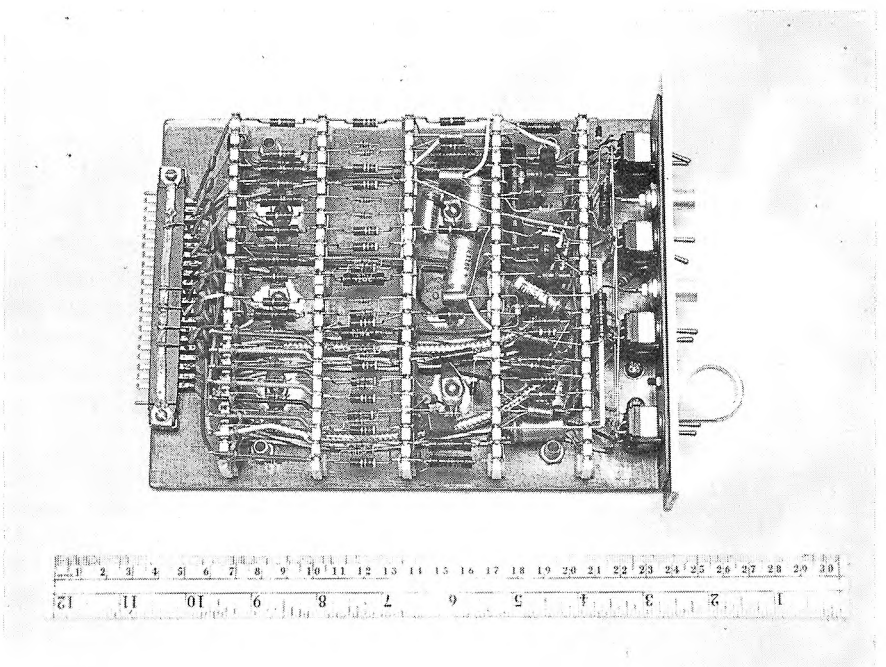


FIG. 14 The 50 nsec Logic (Shield Removed)

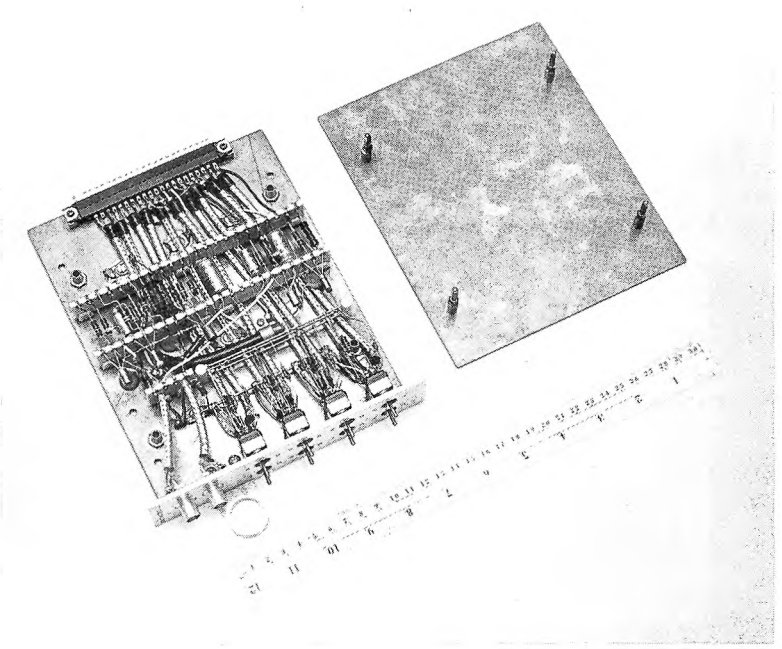


FIG. 15 The 0.5 μsec Logic and the Shield

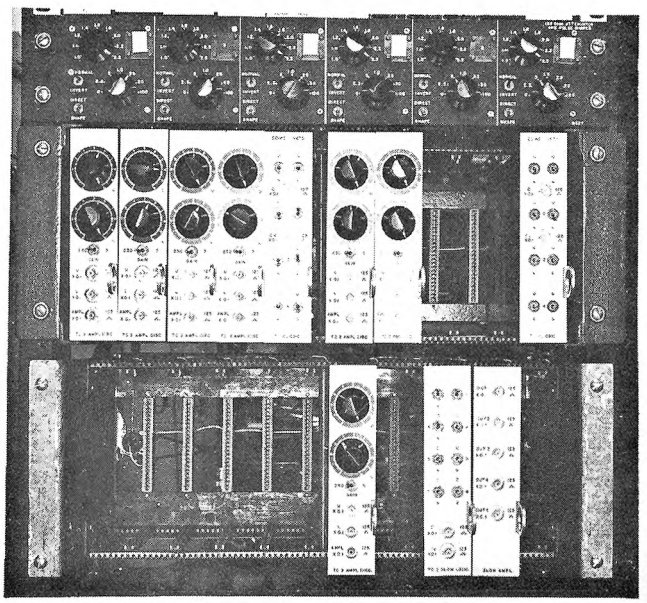


FIG. 16 An Instrument as Incorporated Into an Experiment