# Microprocessor-Controlled Digital Shunt Regulator

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**Abstract**

**A new approach to the design of power systems is presented in which a microprocessor is used as a controller for a digital shunt regulator (DSR). This approach meets the demands of future space and ground missions, i.e., high efficiency, high reliability, low weight, low volume, increased flexibility, and less development time. This approach responds to future demands by permitting real-time modification of system parameters for system optimization. This feature is especially important in the event of an anomaly. As the microprocessor need not be dedicated to the DSR, it can simultaneously be used for battery management and for charge regulator/discharge regulator control. This approach also reduces the component count, simplifies assembly and testing of the unit, results in significant time saving, and increases the reliability.**

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## I. Introduction

In recent years use of microprocessors for power processing systems has resulted in improved performance. To meet the predicted requirements of spacecraft, it is necessary that new and improved mehods of electrical power conditioning and control be developed. The power system should be modular and should not take any development time. Other constraints imposed are high reliability, minimum weight and volume, low cost, and flexibility. To meet these demands an attempt has been made to use a microprocessor to control the digital shunt regulator (DSR).

Since the advent of the space age, photovoltaic cell arrays have been used as the main energy source for spacecraft power generation. In addition, solar energy, which is abundant in space, may play an important role in meeting the world energy requirements by means of microwave transmission from space. Because the electrical output of photovoltaic cell arrays is unregulated, however, the power must be processed and regulated before it can be used by other equipment. Thus these solar power systems require bus regulators, of which the DSR is superior compared to other types of shunt regulators [1]. The main advantage of the DSR over other types of shunt regulators is that this can be employed for high-power systems as its weight, size and volume do not increase in proportion to the power requirements as others do. Although the circuitry is somewhat more complex than a simple analog shunt or sequential shunt, it does offer high reliability and is of low cost.

The power systems described above, whether used in space or on the earth must use batteries to meet the peak and eclipse/shadow requirements of the load. Hence, the storage batteries have to be charged during sunlit period/day time and have to be discharged during eclipse/nighttime or when there is a requirement for peak power. In addition, these batteries have to be protected from overcharge and undercharge. Attempts have already been made to use microprocessors for battery management [2,3]. Microprocessors can also be used to control charge and discharge regulators (CR/DR).

Thus the approach of using a microprocessor for the control of the DSR is a very useful one, especially since the same microprocessor may be used for controlling DSR, CR/DR, and battery management. This approach is expected to result in a single integrated system/unit for all the functions mentioned above with a bonus in system flexibility, high reliability, minimum weight and volume, and standardization. The processor can also be used to continuously monitor the status of its own system and the health of the overall power system as well.

The purpose of this paper is to present the hardware and software details of a microprocessor controlled digital shunt regulator.

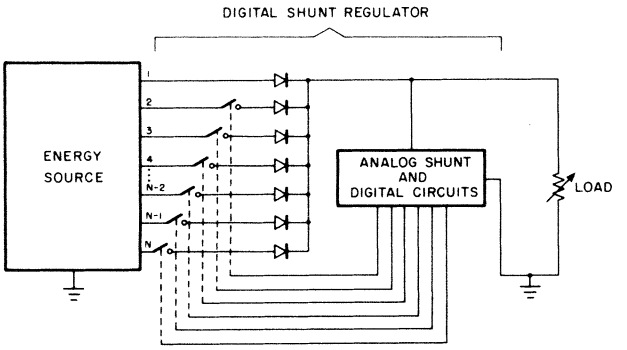


Fig. 1. Block schematic of power system using dsr.

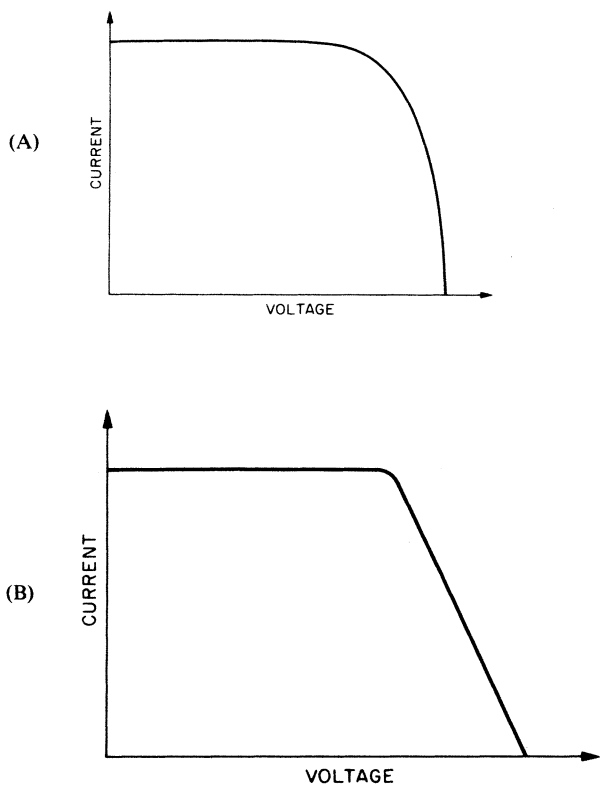


Fig. 2. I-V characteristic of (A) typical solar cell array, (B) solar array simulator.

Section II contains a brief description of the digital shunt regulator. Then follows the detailed description of solar array section simulators in Section III. The operation and design of the dissipative analog shunt is given in Section IV. Section V contains the description and design of shunt current comparators. The need for a special timing function and its design is discussed in Section VI. Section VII contains the description of the microprocessor controller, hardware implementation, software programs, and interfacing. The complete system is described in Section VIII. The experimental results of the model system constructed as described above is presented in Section IX. Some possible extensions are suggested in Section X.

## II. Digital Shunt Regulator

Fig. 1 shows the block diagram of a power system using a digital shunt regulator. As mentioned above, the energy source is a photovoltaic cell array. The digital shunt regulator regulates the output of the energy source to the needs of the load. The solar cell array is divided into $N$ sections, one section of which is permanently connected to the bus and all other sections are connected through switches. The DSR contains a small dissipative analog shunt which is designed to regulate one section of the array. The current through this dissipative shunt is monitored. Whenever this current exceeds approximately the current of a single section, $I_{max}$, the digital processing part of the DSR switches off one section. Whenever this current reduces to a minimum, $I_{min}$, then the digital part of the DSR switches on one section. Thus coarse regulation is achieved by the digital part of the DSR and fine regulation is achieved by the dissipative shunt. This DSR will be described in detail in the following sections.

Because the solar cell array is not available to test the DSR, solar cell array section simulators have been constructed and used instead. First various building blocks of the microprocessor controlled DSR will be explained and then the overall description of the complete system will be given.

The demonstration system has been designed to the following criteria: Regulated bus voltage 28 V, Maximum power to be handled 30 W, Number of solar cell array sections 4.

## III. Solar Cell Array Simulator

Fig. 2(A) shows the I-V characteristic of a typical solar cell array section. For the model system being used here, the simulator need not exhibit an I-V characteristic identical to that of a real solar array——it need only be similar. The nearest simulation with the least complexity is achieved by using a current source (as a solar cell is also a current source) whose I-V characteristic is shown in Fig. 2(B). This I-V characteristic is enough to simulate the solar cell array for testing of the DSR.

Each solar cell array section simulator has been designed to give about 300 mA at 28 V. Fig. 3 shows the circuit diagram of one simulator. Four units of this type have been constructed. The I-V characteristics of all four simulators are given in Fig. 4. The portion of the circuit within the dotted line in Fig. 3 is used to switch the simulator on and off. An light-emitting diode (LED) has been included in each circuit as shown to indicate visually whether the section is switched on or off.

## IV. Dissipative Analog Shunt Regulator

As mentioned above, the dissipative analog shunt is used to achieve fine regulation of the bus voltage. This type of shunt has been chosen over the alter-

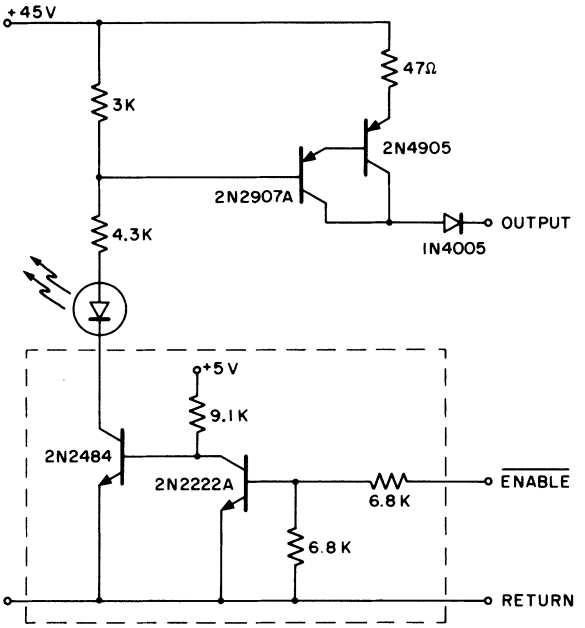


Fig. 3. One section of solar array simulator.

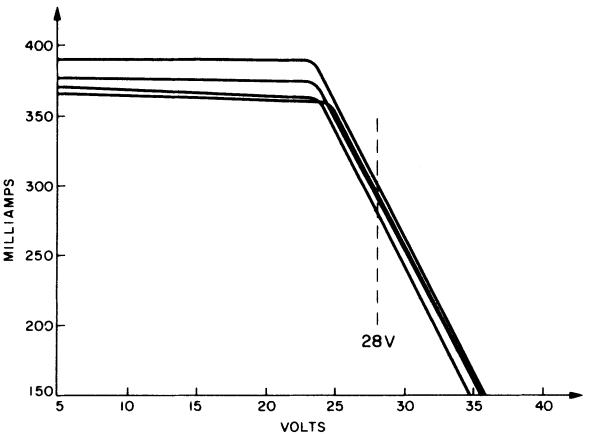


Fig. 4. I-V characteristics of all four solar array simulator sections.

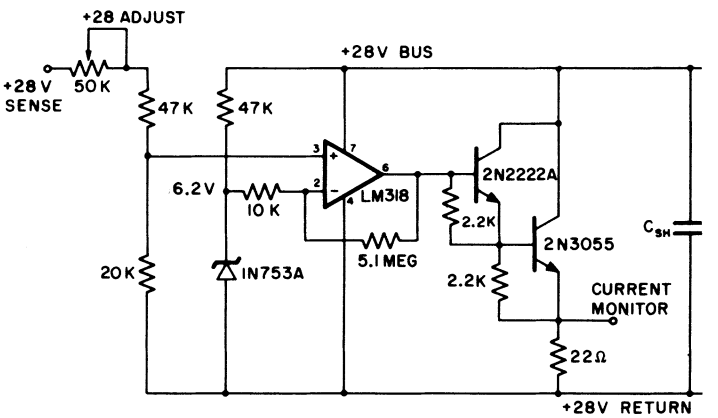


Fig. 5. Analog shunt regulator.

native pulsewidth modulated shunt because the analog circuit has a much higher bandwidth and therefore is more desirable for achieving finer regulation. Fig. 5 shows the circuit diagram of the dissipative analog shunt. Divided-down bus voltage is compared to the reference voltage and the amplified error voltage is used to control the current through the shunt. A resistor of suitable value (depending on the maximum design current of the shunt) is used in the shunt current path to monitor the current that is flowing through the shunt. This signal is used for further digital processing.

## V. $I_{max}$ and $I_{min}$ Comparators

The shunt current, measured automatically using a resistor in the shunt path (Fig. 5), is compared against two reference voltages to determine whether it is above $I_{max}$ or below $I_{min}$. Fig. 6(A) shows the circuit diagram of the $I_{max}$ and $I_{min}$ comparators. Fig. 6(B) shows the waveforms of the shunt current and the outputs of both the comparators.

The reference voltages for the $I_{max}$ and $I_{min}$ current comparators are derived from the bus voltage by using a zener diode and resistor dividers. It would also be possible to generate the references from digital-to-analog converters. In this way the reference voltages could be changed when necessary. Occasionally this must be done to compensate for degradations due to ageing. In a space system these changes can be telecommanded from ground. In ground-based systems, such maintenance commands can be given from remote locations.

An alternative approach to the one presented above is to use an analog-to-digital converter to put the shunt current signal into digital form. This digital information can then be compared with a digital reference within the microprocessor. This is illustrated in Fig. 7. In this case the digital-to-analog converter for the reference voltages mentioned above is not required.

## VI. Switch Timing

The two outputs from the $I_{max}$ and $I_{min}$ comparators are used by the microprocessor to switch the solar array sections. For stability reasons this is done according to a timing signal from an external clock. This will be discussed in detail in Section VII A.

## VII. Microprocessor Controller

Fig. 8 is a general block diagram which shows the position of the microprocessor in the digital shunt regulator system. Since this paper is concerned primarily with the microprocessor's role in voltage regulation, other signals and interfaces pertaining to possible housekeeping duties are not included in the diagram.

The processor's job is simply to add or to remove solar array sections from the bus to keep the shunt

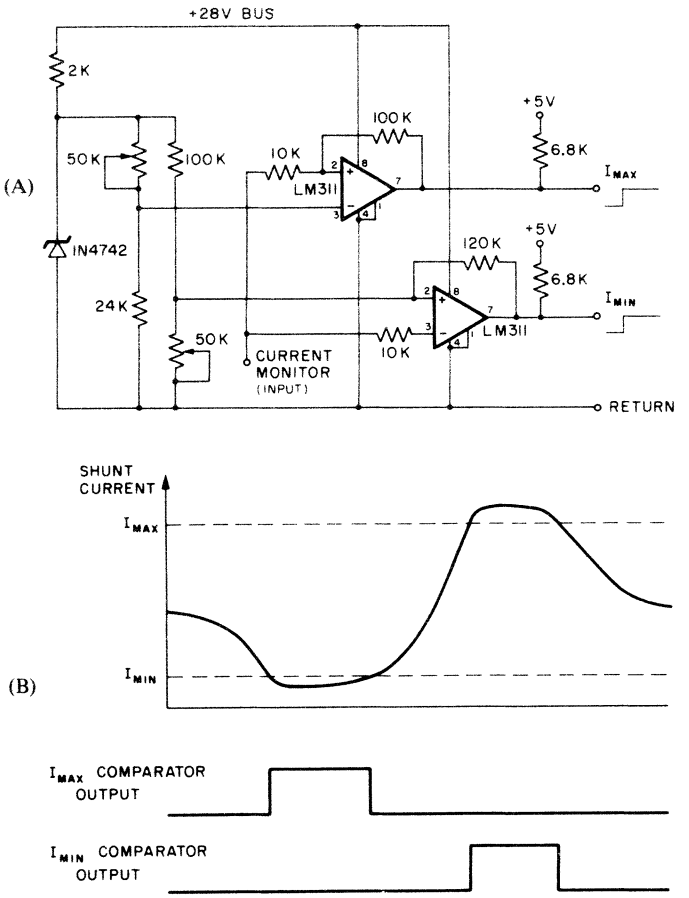


Fig. 6 Current Comparators. Relationships between $I_{min}$, $I_{max}$, and shunt current.

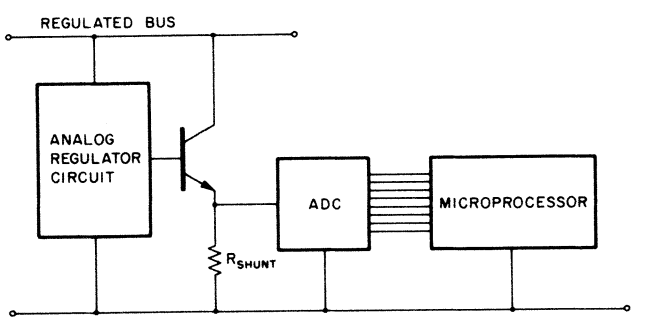


Fig. 7. Use of ADC for current monitoring.

current between its maximum and minimum limits.

Fig. 9 is a more detailed block diagram of the system's control loop. Many power systems have the inherent property that their loads don't change very often. A communications satellite, for example, might experience a load change only a few times per hour as transmitters are switched or antenna positions changed. The regulator's controller is configured to take full advantage of this system attribute.

While the load is constant and the solar array is under constant illumination, the bus voltage should remain in regulation, any small changes being compensated by the self-contained analog shunt regulator. Under these conditions the microprocessor is free to do housekeeping tasks and other routine management jobs.

When a change does occur, however, and the shunt current level trips either the $I_{max}$ or $I_{min}$ comparator, the microprocessor is interrupted from its background job. The interruption initiates software which reads the system status, determines whether array sections must be added or removed from the bus, changes the array control word to reflect the power demand, and then sends the new control word to the solar array switches. The processor then resumes its background job and waits for another interrupt.

For maximum speed and simplicity, only one section of the solar array is switched per interrupt. The microprocessor is so fast, however, that the power system may not completely respond to the addition or removal of a section by the time the software is ready to return to the background job. If it were permitted to return at its maximum speed, the background job could be interrupted again immediately because the system would not have time to fully respond to the initial correction——even if the single addition or removal was adequate to compensate for the initial load change. The controller would then overcorrect and the system could be unstable.

To eliminate this possibility, the switching of the array sections and the return of system control to the background job are synchronous with a slow clock. This term is used to distinguish it, running at kilohertz, from the processor's clock, which runs at megahertz. The state of the slow clock is a part of the

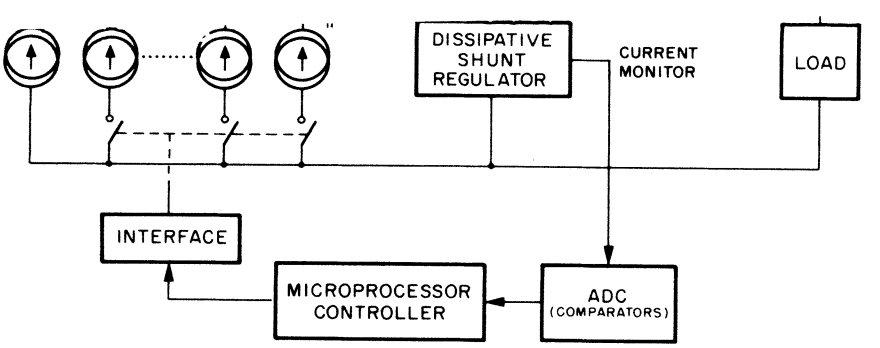


Fig. 8. Role of microprocessor in dsr system.

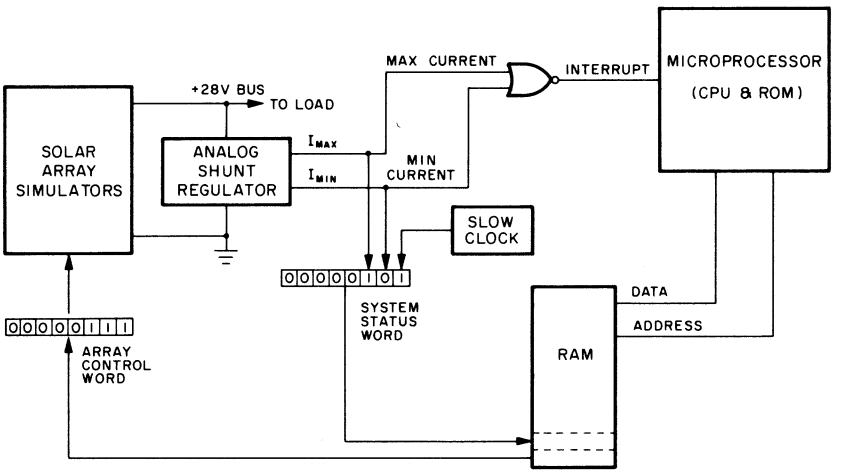


Fig. 9. System block diagram.

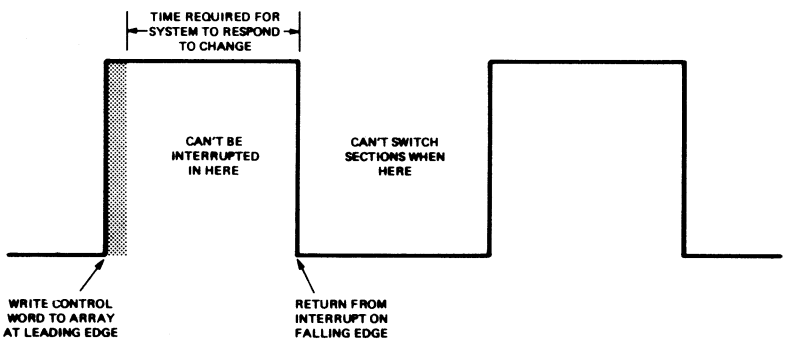


Fig. 10. Slow clock timing diagram assuring stability.

system status word that is read by the controller. Fig. 10 shows timing relations with respect to the slow clock. The degree of size reduction of power components realized by the adoption of a digital regulator is a function of the speed of the slow clock. The maximum frequency of the slow clock is related to the bandwidth and transient response characteristics of the analog regulator. This frequency may be further restricted by the microprocessor if the software is slow. In that case the microprocessor would limit the overall response and physical size reduction of the regulator. These considerations are discussed in greater detail in the next section.

## A. Frequency Limitations

There are several factors which determine the characteristics of the slow clock. It is desirable to have the clock run as fast as possible, since the amount of capacitance required at the output of the shunt regulator is inversely proportional to the rate at which solar array sections can be added to the bus. The capacitor is required for energy storage during transient loads.

Assume there is a step increase in load current. The shunt regulator responds by reducing its shunt current until $I_{min}$ is reached. Now no more current is available from the solar array and the capacitor must supply the balance of the load current until the microprocessor switches another array section onto the bus. The longer the processor takes to do this, the larger the capacitor must be to keep the bus voltage within specifications. A similar situation exists when there is a step reduction in load current. Then the capacitor must absorb the excess current until the processor removes a section from the bus.

The absolute maximum frequency which can be run is therefore determined by the time it takes for the microprocessor to respond to either an $I_{max}$ or $I_{min}$, whichever takes more time.

The absolute maximum frequency may not be suitable for the system, however. The transient limits specified for the bus voltage and the absolute maximum frequency will together determine the minimum capacitance required on the regulator output. The capacitance will in turn influence the transient response characteristics of the shunt regulator. The frequency of the slow clock may have to be decreased to give the regulator time to respond to changes caused by the switching of array sections. Transients in the response must be given time to decay sufficiently before the processor is permitted to evaluate system status. Also, such over all system considerations as electromagnetic inference (EMI) or special syn-

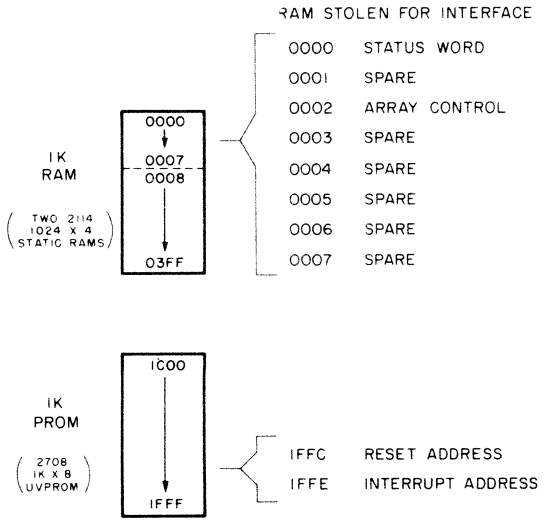


Fig. 11. Address allocation.

chronization requirements may influence the characteristics of the slow clock.

The software for the development system described in this paper requires 46 *processor clock cycles* to execute one switching action and return to a background job after an interrupt has occurred. At a 1 MHz rate this means that the slow clock can run at 21 KHz absolute maximum. A frequency of 10 KHz, however, was selected as a reasonable baseline for comparison with the performance of other system configurations.

For completeness it should be mentioned that the slow clock need not be operated at 50 percent duty factor as it is in this system, nor does it have to be periodic. A retriggerable single-shot could perform the same function by inhibiting the interrupt during the transient settling time.

In addition, the timing need not be derived from an independent source as it is done here. It may be more desirable in certain cases to derive a slow clock from the microprocessor's fast clock by means of a software-programmable frequency divider.

## B. Hardware Implementation

Selection of the hardware used in the model regulator was influenced not only by the immediate availability of the individual parts but also by the availability of the equipment and facilities required to support them. The design, therefore, is not the most desirable. It should be mentioned, however, that the Rockwell 6502 central processing unit (CPU) was the first choice for the heart of the controller since its advanced architecture permits instruction execution in a minimum number of clock cycles and its zero page addressing feature is extremely useful in high-speed data transfer. Both these features permitted maximum design flexibility and system performance.

Memory consisted of two 2114 1K × 4 static random-access memory (RAM) chips and one 2708 1K × 8 UVPROM. Decoding was done with 74138's and the slow clock was made with a 555 timer. Interfacing was accomplished with a 74367 tristate bus driver and a 74174 latch. Miscellaneous NAND/NOR/NOT functions called for a 7400, 7402, and a 7404.

Although the parts count is small, it is much larger than required for this system. The circuit was purposely overdesigned in anticipation of facilitating system expansion for future development work.

## C. Interfacing

The interfacing philosophy is very simple and straightforward. The address lines are decoded such that the lowest eight words of RAM are stolen for interfacing purposes. The addresses that were formerly in RAM are now external data ports. Fig. 11 shows the allocation of the addresses. Fig. 12 shows the decoding scheme and Fig. 13 gives the interface circuits.

Since this is only an elementary system only two of the eight available stolen addresses are utilized. If one wants to read the system status word, for instance, all that is required is to read the contents of address 0000. (Addresses here are written in hexadecimal). Writing to that location in inhibited by the decoding hardware and has no effect. To switch the array sections all one must do is store the array control word at address 0003. Attempts to read from that location are inhibited and have no meaning.

It is easy to see that it would be a simple matter to control or monitor many functions with just these eight locations, since each word contains eight bits of information. It is also a trivial matter to extend the interfacing addresses from eight to a higher power of 2 just by modifying the decoding circuit.

The interface to the processor's interrupt request line ($\overline{\text{IRQ}}$) is through a single NOR gate. Thus if the shunt regulator demands attention for either too much or too little current, the CPU is alerted.

## D. Software

Fig. 14 shows the entire program for the processor. The program as shown is written in 6500 mnemonics and coded for input to a cross-assembler. The flowchart for the operations is given in Fig. 15.

The program was written to execute the array switching operation in the fewest number of clock cycles to achieve a high value for the absolute maximum slow clock frequency discussed in Section VII A. Extensive use is made of the zero page addressing feature of the 6502.

The background job is just a dummy do-nothing routine which idles the processor when no demands are being made on the system.

# VIII. Complete System

This section summarizes the operation of the complete DSR system. When the power is first turned on,

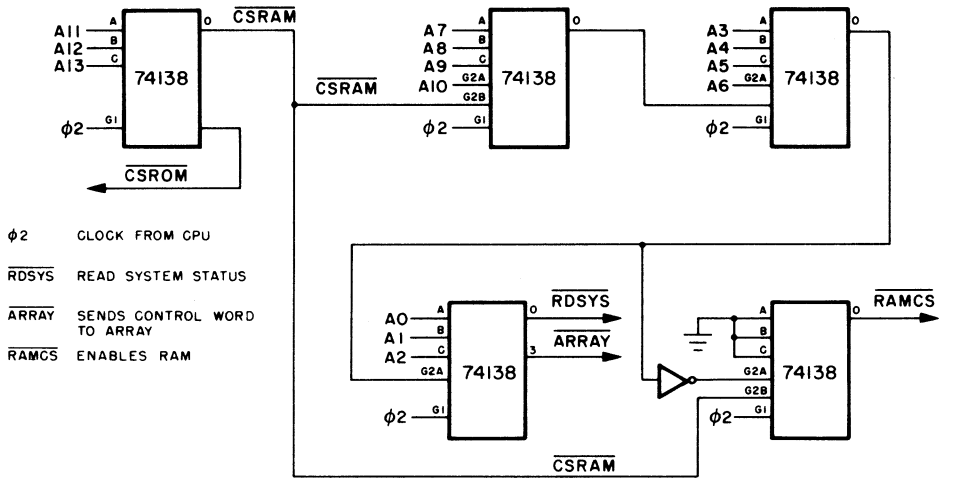


Fig. 12. Decoding scheme.

the dissipative analog shunt comes on immediately. As the bus voltage slowly builds up, no shunt current flows until the bus voltage crosses 28 V, after which the bus voltage is maintained by controlling the current in the shunt such that the sum of the load current and the shunt current is equal to the current of the solar cell array section at 28 V.

If the load current increases, the shunt current decreases and vice versa. If the load current continues to increase such that the shunt current reduces below the $I_{min}$ value, then the $I_{min}$ comparator output activates the microprocessor to switch one more section onto the bus. Now the shunt current rises to a level between $I_{max}$ and $I_{min}$. Again assume that the load current increases further such that the shunt current reduces below $I_{min}$. Then the processor will switch on one more section just as before. This process continues until all sections are switched on. Now the load current can increase no more as the system is designed only to this maximum value of load current.

Now say the load current decreases. Then the shunt current increases to maintain the bus voltage. But assume that the load current decreases such that the shunt current increases above the $I_{max}$ value. Then the $I_{max}$ comparator output is used by the microprocessor to remove one section from the system. The shunt current will then decrease. Assume now that the load current decreases again such that the shunt current increases to give an $I_{max}$ output. One more section will be switched off the bus. If the load current is decreased to zero this process continues until all sections are switched off and disconnected from the bus. As one section is connected permanently without a switch, one section will be on all the time. But as the shunt is designed for one section full power, the bus voltage is maintained even if the load is completely disconnected.

Thus the DSR maintains the bus voltage at fixed level from no load to full load.

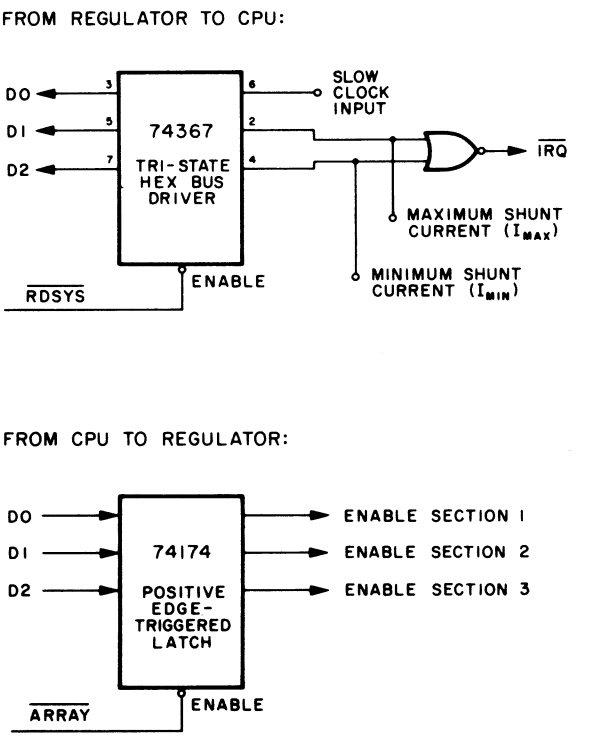


Fig. 13. Interface circuits.

## IX. Experimental Results

A model system of a microprocessor controlled digital shunt regulator was built as described earlier in this paper. Data taken from that setup is presented here to illustrate the system's performance under several interesting conditions.

```
                TITLE "DIGITAL SHUNT REGULATOR"

;  THIS SECTION DEFINES RAM LOCATIONS

       ASECT $0000
SYSTAT:         BLOCK 1          ;CLK, MIN, MAX

       ASECT $0003
ENABLE:         BLOCK 1          ;DSR5, DSR4, DSR3

       ASECT $0010
SETREG:         BLOCK 1          ;ARRAY CONTROL WORD

       ASECT $0050
STACKTOP:       BLOCK 20         ; RESERVED FOR STACK


;  THIS SECTION DEFINES ROM LOCATIONS

       ASECT $1FFC
              BKWORD RESET      ;PROGRAM GOES HERE ON RESET

       ASECT $1FFE
              BKWORD ATTN       ;PROGRAM GOES HERE ON INTERRUPT

       PSECT
;  INITIALIZATION ROUTINE

RESET:          LDA    #$07             :TURN OFF CURRENT SOURCES
                STA    ENABLE
                STA    SETREG           ;INITIALIZE CONTROL REGISTER
                CLD                     ;CLEAR DECIMAL MODE
                LDX    #$50             ;SET STACK POINTER
                TXS
                JMP    BACKGROUND       ;GO TO BACKGROUND JOB TASKS

ATTN:                                   ;PROGRAM GOES HERE ON INTERRUPT
                LDA    SYSTAT           ;LOAD ACCUMULATOR WITH SYSTEM STATUS
                AND    #$01             ;CHECK TO SEE IF MAX BIT IS SET
                BEQ    MIN              ;IF NOT GO TO MIN ROUTINE
                LDA    SETREG           ;REMOVE ONE SECTION OF ARRAY
                ASLA
                ORA    #$01             ;SHIFT IN A "1"
                JMP    CLKCHK           ;NOW WAIT FOR PROPER TIME TO WRITE
MIN:                                    NEED MORE CURRENT--ADD ONE SECTION
                LDA    SETREG
                LSRA                    ;SHIFT IN A ZERO

CLKCHK:                                 ;CHECKS FOR POSITIVE EDGE OF CLOCK
                LDX    SYSTAT           ;WAIT FOR CLOCK LOW
                CPX    #$03
                BPL    CLKCHK

WRITERDY:                               ;WRITE WHEN CLOCK GOES HIGH
                LDX    SYSTAT
                CPX    #$03
                BMI    WRITERDY         ;LOOP IF CLOCK STILL LOW
                AND    #$07             ;KEEP ONLY 3 LOWEST BITS
                STA    ENABLE           ;WRITE CONTROL WORD TO ARRAY
                STA    SETREG           ;STORE CONTROL WORD IN RAM

CLKFALL:                                ;CHECKS FOR NEGATIVE EDGE OF CLOCK
                LDX    SYSTAT
                CPX    #$03
                BPL    CLKFALL          ;LOOP IF STILL HIGH
                CLI                     ;IF NEGATIVE EDGE, CLEAR INTERRUPTS
                                        AND RETURN
               RTI


; BACKGROUND JOB

BACKGROUND:     CLI                     ;ENABLE THE INTERRUPTS
LOOP1:          LDY    #$20             ;ROUTINE PRINTS CHARACTERS
LOOP2:          CPY    #$5F             ;TO SIMULATE OTHER POWER
                BEQ    LOOP1            ;MANAGEMENT TASKS
                STY    $#411
                INY
                LDX    #$00
WAIT:           INX
                CPX    #$FF
                BNE    WAIT
                JMP    LOOP2
```

Fig. 14. Program.

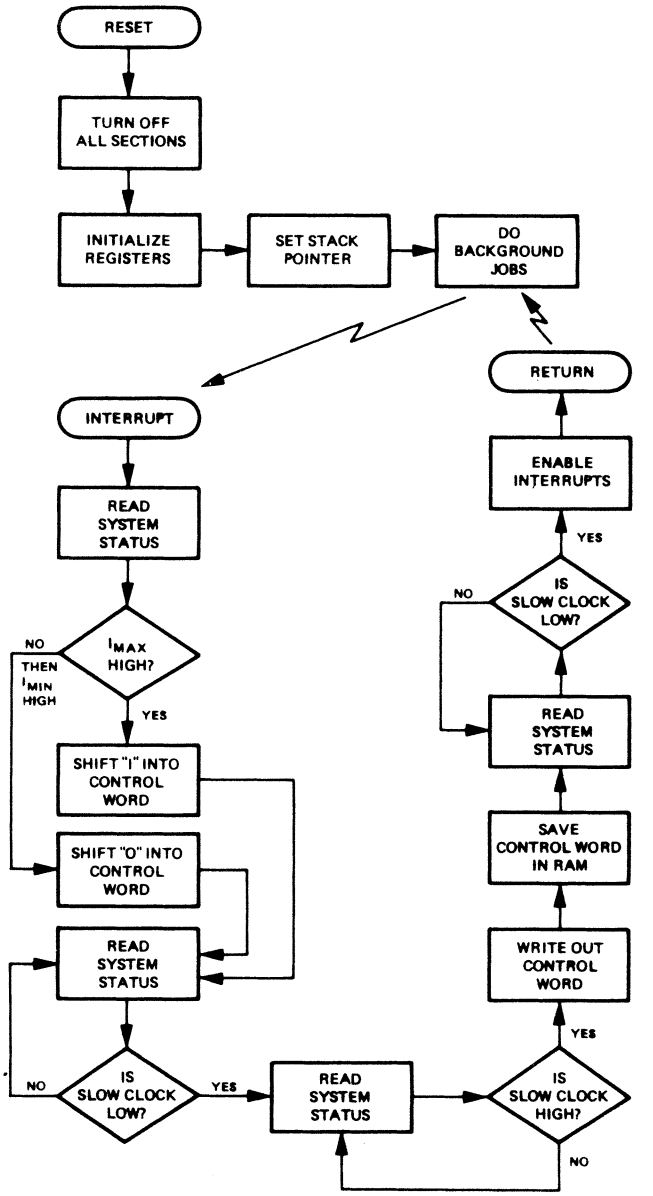


Fig. 15. Flowchart.

TABLE I
System Status at Various Loads

| Load Current | Shunt Current | Status of Switched Array Sections | | | Bus Voltage |
|---|---|---|---|---|---|
| (mA) | (mA) | S1 | S2 | S3 | (volts) |
| 0 | 290 | OFF | OFF | OFF | 28.02 |
| 200 | 90 | OFF | OFF | OFF | 27.98 |
| 300 | 310 | ON | OFF | OFF | 28.02 |
| 400 | 210 | ON | OFF | OFF | 28.00 |
| 500 | 110 | ON | OFF | OFF | 27.98 |
| 600 | 320 | ON | ON | OFF | 28.03 |
| 700 | 220 | ON | ON | OFF | 28.00 |
| 800 | 120 | ON | ON | OFF | 27.98 |
| 900 | 280 | ON | ON | ON | 28.03 |
| 1000 | 180 | ON | ON | ON | 28.01 |
| 1100 | 80 | ON | ON | ON | 27.98 |
| 1150 | 30 | ON | ON | ON | 27.97 |

Table I shows the dc steady-state values for system parameters under several different loads. The $I_{max}$ threshold was set for 400 mA and the $I_{min}$ value was set for 45 mA. These values were selected according to the measured I-V characteristics of the solar array simulators (Fig. 4). The levels must be chosen to be certain there is no possibility of overlap from $I_{min}$ to $I_{max}$ when a section is switched onto the bus. Some margin is included to allow for the presence of noise on the sense lines. The dc regulation is $\pm$ 30 mV from no load to full load. One can also see from the table that a section is switched when a change in load current causes the shunt current to cross either an $I_{max}$ or $I_{min}$ threshold. The limit of regulation is about 1.15 A, when the shunt current drops below the $I_{min}$ value and there are no more sections left to be switched onto the bus. A little more load current causes the output voltage to fall with increasing load.

The remaining data is for dynamic conditions. Fig. 16(A) shows the response of the regulator to a dynamic load under the condition that the load does not cause the shunt current to cross a threshold. The top trace is the ac portion of the bus voltage. The center trace is the load current at 200 mA/div and the bottom line marks zero load current. The load current experiences a 250 mA step at a dc load of 600 mA. The output voltage falls by about 60 mV. No switching of array sections has occurred. The bus voltage drop is just the dc regulation of the shunt regulator. The small slope in the voltage waveform is due to the ac coupling of the oscilloscope preamplifier being used at the low frequency (20 Hz pulse repetition frequency (PRF) of the dynamic load.

Fig. 16(B) is the same as above except that the dc load level is at 900 mA (current is 500 mA/div). The voltage waveform is virtually identical to that in the previous case since the shunt current is nearly the same. The extra load current is being supplied by one more array section which the processor has added to the bus.

Fig. 16(C) is the response to a dynamic load when the load change causes an extra section to be switched. Bus voltage is at 200 mV/div. The current is at 500 mA/div. The dc level is 700 mA and the step change is 400 mA. At the leading edge of the step the bus voltage falls until one section is added to the bus. Then the bus voltage rises to resume its proper regulated level. When the load transient is removed there is temporarily too much current being supplied (from the extra section) and this causes the bus voltage to rise. This excess current is soon detected by the processor, however, the section is switched off, and the regulated bus voltage is restored.

Fig. 16(D) is under conditions same as above but the leading edge is expanded in time and the slow clock is shown at the bottom to illustrate the timing relationships. Note that the array section is not switched (evidenced by the rising bus voltage) until the slow clock goes high as prescribed by the software.

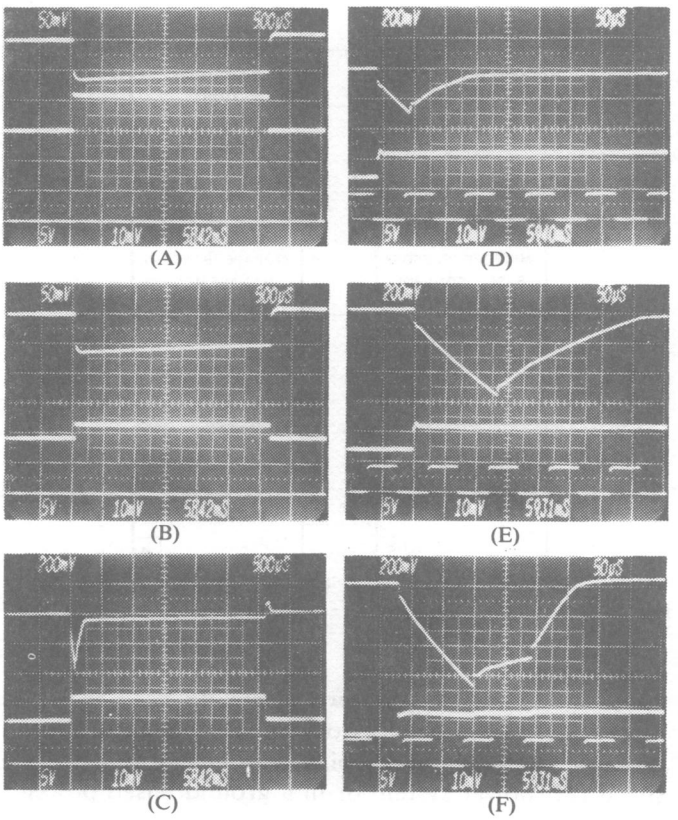


Fig. 16. Waveforms under dynamic loading.

Fig. 16(E) is identical to Fig. 16(D) except that the load transient has occurred at a different place in the period of the slow clock. The processor was interrupted almost immediately at the leading edge of the step, but recall that it takes 46 ms to execute a switching action. It hasn't enough time to switch the array in the present slow clock period and therefore has to wait until the next time the slow clock goes high. Thus the output voltage is allowed to fall much farther than in the previous case. The fact that the processor may have to wait one entire slow clock period *plus* the 46 ms execution time should be taken into account when computing worst case transient bus voltages.

Fig. 16(F) illustrates what happens when the load transient is enough to warrant two sections to be switched onto the bus. Current is at 500 mA/div, dc level is 500 mA and, the step is 400 mA. The slow clock is again at the bottom. One can clearly see the two array sections being added to the bus by noting the changes in slope of the bus voltage.

## X. Extensions

Fig. 17 shows the redundant systems of a microprocessor controlled DSR. Though two microprocessors are used, because of cross connection, the reliability has been further enhanced. In addition, this approach is expected to result in an integrated system for controlling DSR, battery management, and for

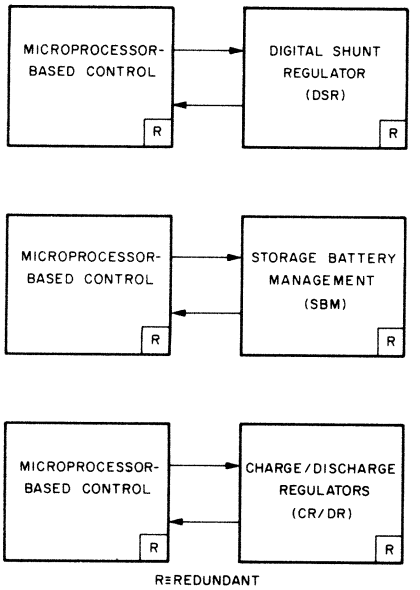


Fig. 17. Redundant Systems.

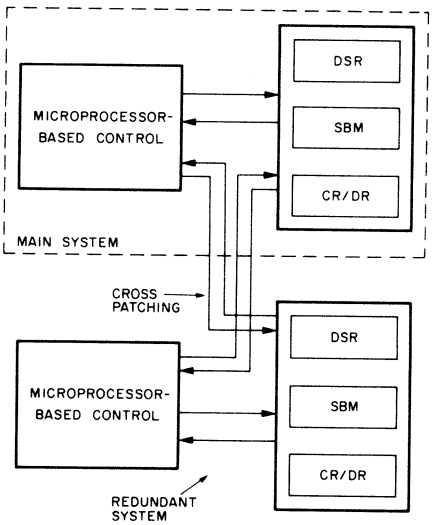


Fig. 18. An Integrated System for DSR, CR/DR, and Battery.

controlling CR/DR as shown in Fig. 18.

The same microprocessor can also be used to monitor various housekeeping parameters in a spacecraft power system or in a ground based power system.

## XI. Conclusions

For solar power systems a digital shunt regulator is superior to other types of shunt regulators, and the use of a microprocessor for the control of the digital shunt regulator results in improved system performance. System flexibility is the chief advantage of a microprocessor based system.

The advantages arise from the ability to replace hardware with software, permitting decisions related to design parameters to be made at a later stage in the project. For example, if the system requires a modification, the change can be implemented by changing the software only, or at worst, software and minimal hardware. Such modifications are simple and less time consuming to implement than previous solutions which involve major hardware design changes. Thus the system capability is enhanced, flexibility is increased, and the design is faster and less expensive than the conventional approach. Moreover, the system can be modified in real time in response to natural component degradations or to anomalies.

Since the microprocessor need not be dedicated to the regulator, it can simultaneously be used for battery management and for charge regulator/discharge regulator control. This feature reduces overall component count, simplifies assembly and testing of the unit, and results in significant time saving. Because the overall system component count can be reduced the reliability can be increased. Implementation of a redundant system is easily done to further enhance the high reliability of the power system.

#### Acknowledgments

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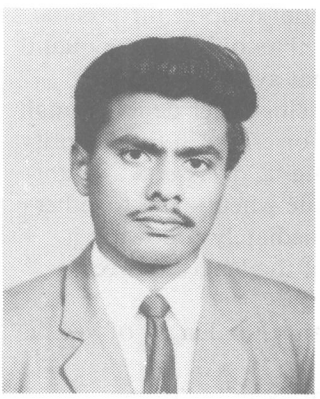

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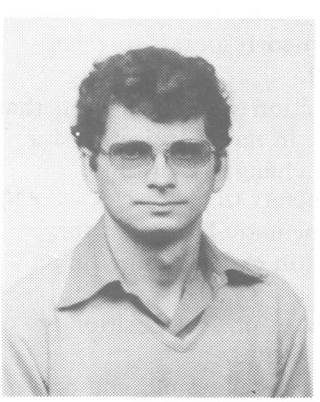

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