A High Resolution CMOS Imager with Active Pixel using Capacitively Coupled Bipolar Operation

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Abstract

The active pixel sensor technology promises high performance than conventional CCD imagers. This paper reports a new high resolution CMOS imager with one-transistor active pixel sensing based on capacitor-coupled bipolar action. The base capacitor is pulsed negatively for image integration and positively for image sensing. The pixel size is 5.9um x 5.9um (on 0.8um design rule). The prototype imager has an array of 480 x 640 and operating at 5v Vcc. This active pixel structure is promising for future high-performance and high-density imagers in the information high-way era.

Introduction

High quality graphics processing systems become one of the most important tasks in information high-way era. Recent progress in digital video and camera calls for high performance imagers which can not be achieved by conventional CCD imagers. The active pixel sensor (APS) technology [1-3] promises high performance imagers with fine resolution, fast random access, non-destructive read-out, and more importantly, integrable with CMOS circuits. This paper reports a new high resolution CMOS imager with one-transistor (1T) active pixel using base capacitor-coupled bipolar action. The pixel size is 5.9um x 5.9um based on 0.8um CMOS design rules. The active pixel operations of image integration, amplification, and read are described in this paper. The limitations and solutions of image blooming and image lag are also discussed. The prototype imager is organized to an array of 480 x 640 (VGA compatible) and is operating at 5v Vcc.

Base Capacitor-coupled Active Pixel

The cross-section of the one-transistor (1T) active npn bipolar pixel (in n-well) is sketched in Fig. 1a (not to scale), where the base is coupled to a capacitor [4]. The layout of the pixel is shown in Fig. 1b. The size of the capacitor-coupled bipolar active pixel is 5.9um by 5.9um, which is about 5X smaller than the three-transistor (3T) CMOS active pixel design [1-3] based on the same 0.8um CMOS design rule. The base capacitor is not sensitive to misalignment between poly and diffusion masks. The fabrication method [5] of the bipolar active pixel is CMOS compatible with one additional mask for p-base implant (inside n-well). The dielectric of poly to base capacitor is formed by the gate oxidation. The emitter n+ implant is self-aligned by the LDD structure and n+ S/D implant. The NLDD implant helps improving leakage current at the emitter-base junction and reducing bipolar action along the emitter edge. The entire pixel array is in n-well which is biased at Vcc. The parasitic pnp bipolar transistors (i.e. p+ n-well and p-substrate) can also be used as pnp active pixels. However, the npn pixel will be used for illustration in this paper.

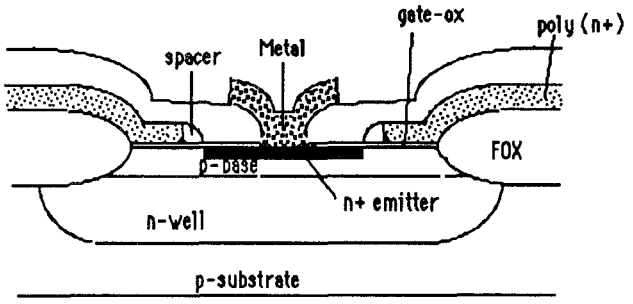

Fig.1a:A cross-section view of the new bipolar active pixel with capacitor coupled base. The fabrication process is CMOS compatible with one masking step for p-base implant (inside n-well).

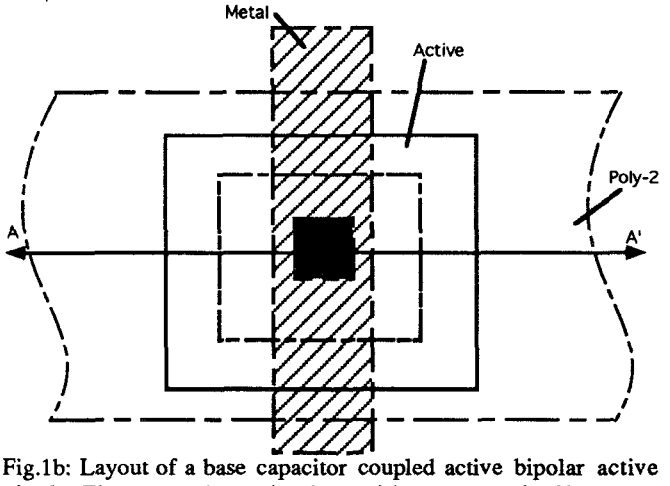

Fig.1b: Layout of a base capacitor coupled active bipolar active pixel. The capacitor is insensitive to misalignment among poly to diffusion masking steps.

Image Integration and Read Operations

When a pixel is exposed to image photons, as shown in Fig. 2a, electrons and holes are generated according to photon's intensity and energy. The pixel has two operation modes i.e. image integration (or storage) and image read (or sensing). The image integration starts when the strobe line (i.e. the poly line) of base coupling capacitor is pulsed toward negative so that the base-emitter junction is reverse biased as shown in Fig. 2b. The total amount of charge (Qb) removed from the p-base through the base capacitor coupling is simply the pulse height (ΔV) multiplied by the base capacitance (Cb), i.e. $Qb=\Delta V.Cb$. The photon-generated electrons (or image

electrons) are swept into the n-well (collector) and removed to Vcc; those photon-generated holes are accumulated in the floating p-base and result in the increase of p-base potential. This process continues until enough image holes (equal to Qb) are accumulated, the p-base to emitter junction then starts being forward-biased and there is "over-flow" current flowing into emitter as noise. More details of overflow (or blooming) mechanism and anti-blooming solutions will be discussed later.

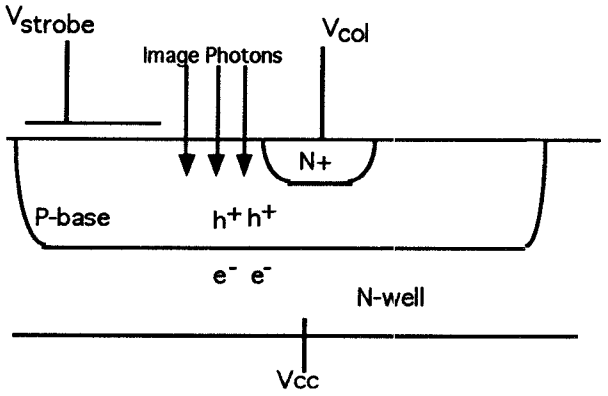

Fig.2a: A sketch of active pixel structure and generation of electrons and holes by image photons.

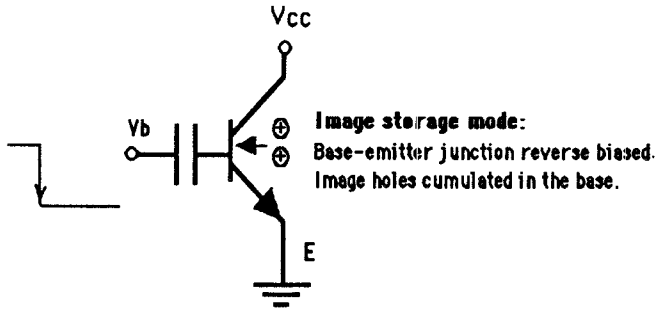

Fig.2b: The pixel enters into image storage mode when the row strobe (Vb) is pulsed down and the base is reverse-biased with respect to emitter.

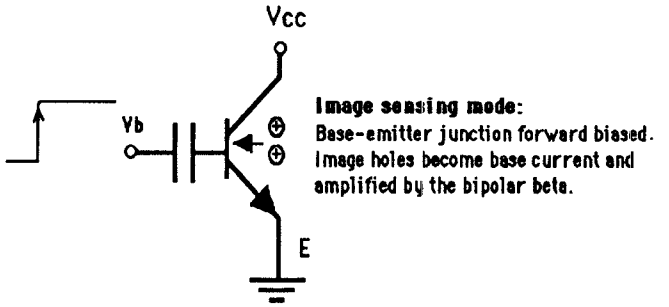

Fig.2c: The pixel enters into image read mode when the row strobe (Vb) is pulsed upward and the base is forward-biased with respect to emitter.

The image sensing (or read) operation starts when the strobe line (i.e. poly line) of base coupling capacitor is pulsed toward positive, the base-emitter junction is forward-biased as shown in Fig. 2c. The image charge is flowing into the emitter as high enough instantaneous base current so that the beta does not suffer low-current degradation. The total amount of charge detected by integrating emitter current during sensing period represents the amplified total image charge during storage mode. The 1T bipolar pixel's base potential during image integration and image sensing is sketched in Fig. 2d.

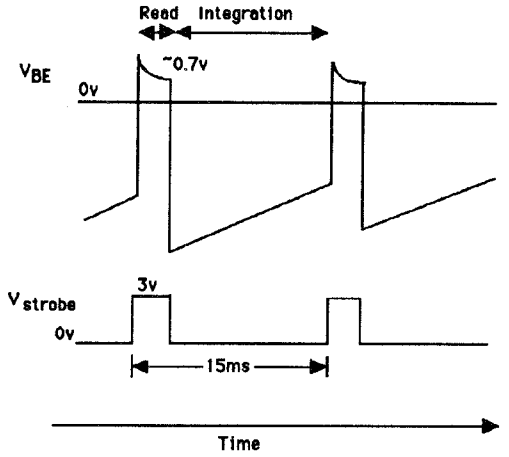

Fig.2d: The base-emitter voltage is reverse biased during image storage mode and forward biased during image read mode.

Sensing Circuits and Imager Performance

The prototype imager is organized into an array of 480 x 640 (VGA compatible) with column sensing amplifiers, vertical scanner (V-scanner), horizontal scanner (H-scanner) and other supporting circuits as shown in Fig. 3.

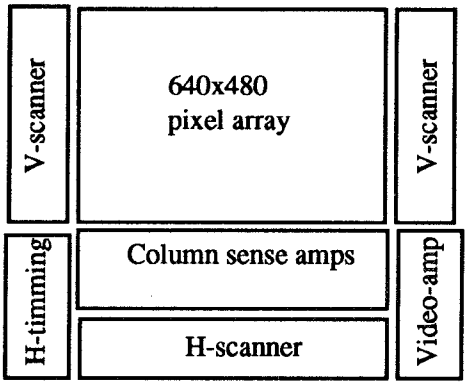

Fig.3: A floorplan of imager shows the arrangement of pixel array, sensing amplifiers, scanners, timing circuits and video amplifiers.

A simplified column charge sensing circuit [6,7] in Fig. 4 shows how the amplified image charge in one pixel (at ith row and jth column) is sensed. The first amplifier senses the charge. The second amplifier has unity gain and is used for correlated double sampling. The emitter current is first sensed and integrated by the charge amplifier (the first stage) and then feeds into the correlated double sampling (CDS) amplifier (the second amplifier). Finally, the output of the CDS amplifier is sample-and-hold and output to a serial video circuit to VGA monitor. Column circuit design is constrained by the narrow column pitch (i.e. one contact plus one metal line).

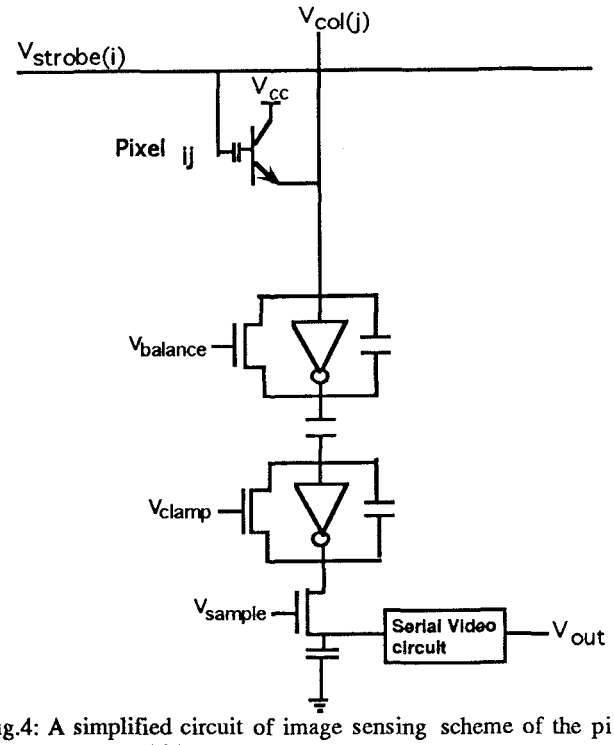

Fig.4: A simplified circuit of image sensing scheme of the pixel at jth column and ith row.

The reproduced image of resolution chart is shown in Fig. 5. For future 0.35um technology, the pixel size is further reduced to 4um x 4um, approaching the resolution limit of typical optics. The characteristics of imager sensitivity, dynamic range, noise performance, ...etc. will be published elsewhere [8].

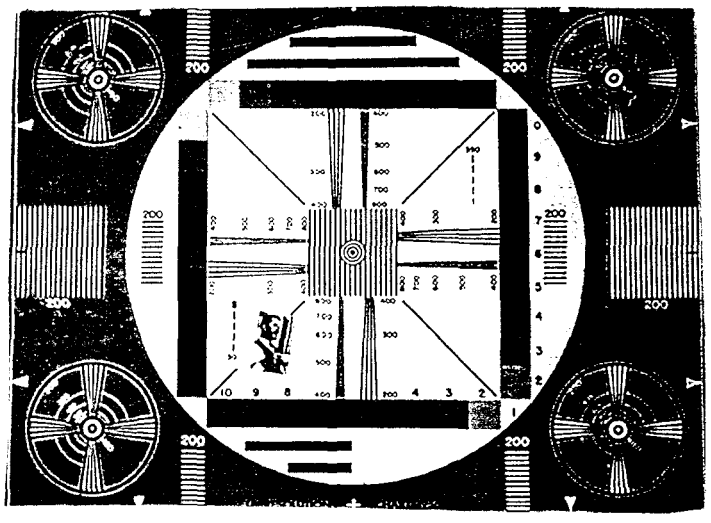

Fig.5:A reproduced resolution chart from VGA monitor.

Comparison of 1T and 3T pixels

The new capacitor-coupled 1T bipolar pixel has advantages of smaller pixel size (Fig. 6), wide dynamic range, and higher resolution than active pixels based on 3T CMOS transistors. The fabrication process of the new pixel is CMOS compatible with only one additional mask (for base implant). This 1T active bipolar pixel has advantages of lower fabrication cost and higher resolution than the 3T CMOS active pixel. As a result, the total imaging system cost may be reduced by using the 1T active pixel approach.

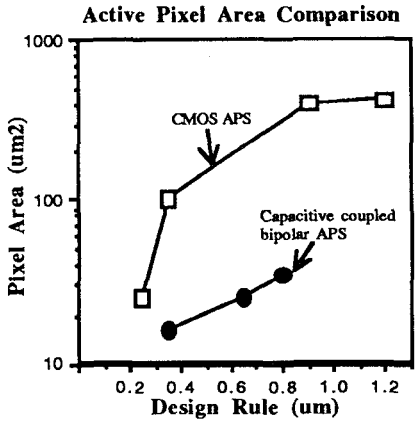

Fig.6: A comparison of pixel size between active pixel of CMOS transistors [1-3] and capacitor coupled bipolar pixel. The single-transistor base coupled bipolar active pixel has significantly smaller pixel size.

Another important feature of the 1T bipolar active pixel is its symmetrical layout, where image photons can enter into areas in between pixels. Those electrons and holes generated by photons in between pixels can be shared by adjacent pixels, in this manner the output of each pixel is not just a "point" sampling of the image but also contains image information around the sampling point. This feature provides a strong anti-aliasing capability than the 3T CMOS active pixel imager.

Blooming and Image-lag

The 1T bipolar pixel has two inherent problems of image over-flow (or blooming) and image-lag. The image over-flow problem comes from emitter current from pixels in integration with strong exposure of photons (i.e. bright image). The p-base potential of pixels under strong exposure increases so rapidly that the p-base to emitter junction is forward biased and the emitter current also flows into column sensing circuit. This "over-flow" current is added together with the real signal current from the pixel being read (in the same column) and causes brighter image than it should be. In this case, vertical streaks would appear around a bright spot. There is no mechanism in the 1T bipolar active pixel (Fig. 1) for preventing the base to emitter junction from being forward-biased during integration.

Another problem of the bipolar active pixel is image-lag, which is appearing as a tail following a moving bright spot or a blurred ghost image following moving objects until still. The image-lag of bipolar pixel is related to a residue charge, or "memory" from previous image. The residue charge comes from the minority charge storage in base during (forward-biased) sensing. The operation of integration by pulsing the base capacitor negatively with a fixed pulse height, can only remove a fixed amount of charge (i.e. Qb) from the base and is difficult to reset pixels back to the very same level of reverse-bias. Thus, a pixel with stronger previous exposure would left more electron charge in base after sensing and subsequent

removal through collector, so that more holes are left in p-base with higher base potential at the beginning of image integration. One way to improve the image-lag performance is to reduce the minority carrier life time for faster recombination of minority carriers.

Electronic Shutter and Anti-blooming

A second emitter junction (referred to as shutter) can be included in the 1T bipolar pixel and serves as an electronic shutter and overflow control [9]. The layout and cross-section of the modified 1T pixel with shutter (i.e. the 2nd emitter) is shown in Fig. 7 and Fig. 8. The shutter can be used as a switch to turn-off selective rows of pixels by applying shutter bias lower than emitter (by ~2v) during partial period of image integration. In this way, the effective image integration time is reduced and the shutter serves as a function similar to the mechanical shutter of a camera for reducing exposure time.

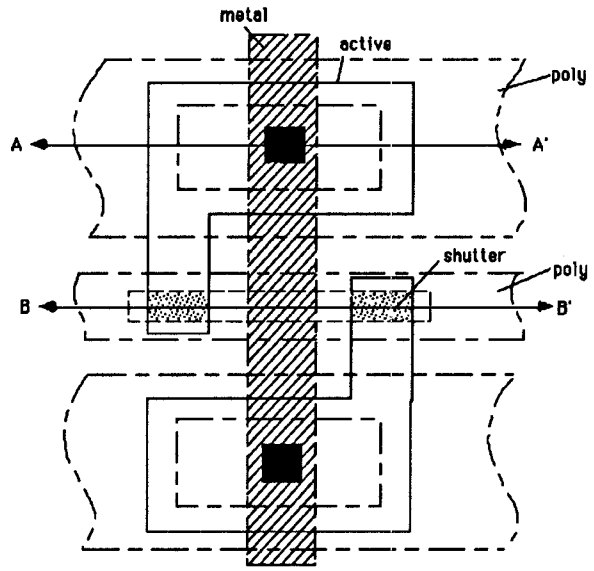

Fig.7: The 1T active pixel with a 2nd emitter used as electronic shutter and over-flow control.

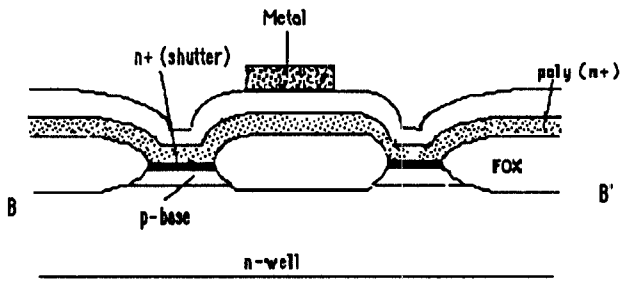

Fig.8: The cross-section view of the 1T pixel with a 2nd emitter for over-flow control along directions of BB'. The cross-section view along AA' is the same as that in Fig.1a.

The shutter can also be used as overflow control of pixels by biasing its potential slightly lower than the emitter potential (by ~0.1-0.5v) during integration period, so that the shutter junction will be forward-biased earlier than the emitter when pixels are under strong exposure; the overflow current is removed from the shutter instead of through the emitter. With electronic shutter and overflow control, the image-lag can also be reduced significantly but not totally eliminated. Thus the bipolar pixel imager is ideal for still photography with high resolution and high-performance.

The imager array of pixels with shutter and column sensing is shown in Fig.9. Each shutter line is shared by two rows (in this design) with proper biasing and timing. The shutter line can be fabricated by using poly or metal with one additional masking step for shutter area opening.

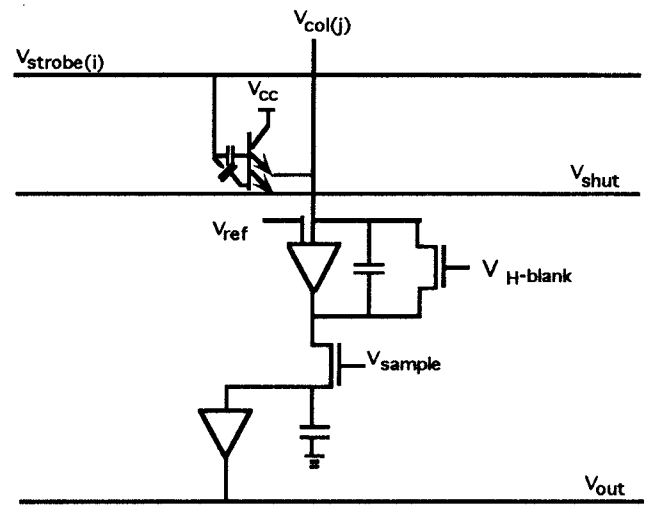

Fig.9: A simplified circuit of image sensing scheme of the 1T pixel (at jth column and ith row) with overflow control shutter.

Conclusion

The imager based on the new one-transistor capacitor coupled active bipolar pixel is promising for high resolution and high-performance still photography applications in digital camera, personal computer image capture, home security, and portable communication systems.

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