A νMOS Soft-Maximum Current Mirror

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ABSTRACT

In this paper, we describe a novel circuit consisting of $N + 1$ MOS transistors and a single floating gate which computes a soft maximum of N current inputs and reflects the result in the output transistor. An intuitive description of the operation of the circuit is given. Data from a working two-input version of the circuit is presented and discussed. The circuit features a high output voltage swing and an interesting feedback mechanism which causes its output impedance to be comparable to that of a normal MOS transistor despite the fact that the output device is a floating-gate transistor.

I. Introduction

Analog VLSI signal processing has come to be the subject of much interest and active research in recent times. [1] In particular, the current-mode approach in which quantities of interest are represented as currents and voltages play only an incidental role in the operation of the circuit has become the focus of much attention. [2] Among the plethora of nonlinear operations required to perform current-mode signal processing, the maximum function stands out as being particularly useful. A *soft-maximum* function is one which follows the largest input and changes over in a smooth manner when the magnitude of two or more inputs become comparable. The circuit presented in this paper computes a soft-maximum of N current inputs and reflects the result in its output.

Floating-gate MOS transistors have been used to great advantage in analog VLSI in the capacity of long-term non-volatile information storage devices. The quantity of charge stored on the gate of these transistors has been used as free parameters which are adapted so as to increase the precision of analog circuits [3, 4, 5] and as weights in various VLSI implementations of neural networks [6, 7, 8]. Recently, a marvelous way of using floating-gate MOS transistors was proposed [9] in which multiple "control gates" capacitively couple into the floating gate, establishing its voltage as a weighted sum of the input voltages via a capacitive divider. The channel of the floating-gate transistor then forms a current which is a nonlinear function of the voltage on the floating gate. In [9] these compound devices were dubbed neuron MOS (neuMOS or νMOS) transistors in view of a loose analogy between the function performed by these devices and by cells in the nervous system. A simple above threshold model is derived in [9] and a number of interesting applications are discussed. A corresponding subthreshold model is developed in [10]. The soft-maximum current mirror presented in this paper uses a single floating gate with N control gates and N channels beneath it to enforce a competition between the various input currents, the largest of which establishes the voltage on the floating gate. An additional channel beneath the floating gate computes the output current.

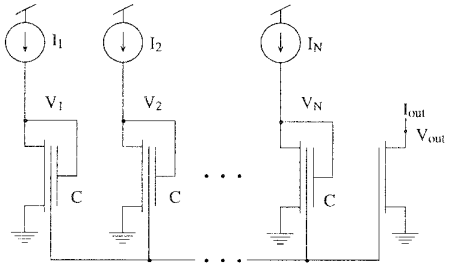

Figure 1: N-input soft-max current mirror.

II. Circuit Description and Operation

A schematic diagram of an N-input soft-maximum current mirror is depicted in Figure 1. The circuit consists of a

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single floating gate with $N+1$ channels beneath it forming N input transistors and a single output transistor. The drain voltage of each input transistor capacitively couples into the floating gate via capacitors of equal strength. The N input currents are sourced into the drains of the input transistors and the output current is sunk from the output node by the output transistor.

A qualitative understanding of the operation of the circuit can be obtained as follows. Each of the $N+1$ transistors in the circuit share a common floating gate and, hence, have the same gate voltage. Also, their sources are all at a common potential. Thus, the saturation current in each of the circuit's $N+1$ transistors will be nominally equal. If any particular input current is less than this saturation current, the drain voltage of the corresponding input transistor will begin to fall, at first reducing the saturation current of all of the transistors in the circuit via the capacitive coupling to the floating gate. Eventually, if that drain is unable to reduce the saturation current of the $N+1$ transistors enough, that particular input transistor will come out of saturation until its drain current just equals the input current. On the other hand, if any particular input current is larger than the saturation current of the transistors in the circuit, the drain voltage of the corresponding input transistor will rise, at first bringing the input transistor into saturation subsequently increasing the saturation current in all of the transistors until it just equals the input current. Taken together, these considerations imply that the saturation current in the $N+1$ transistors in the circuit will be set by the largest of the input currents with each of the other input transistors being out of saturation. So long as the output transistor remains saturated, the output current will reflect the largest of the input currents.

The above considerations rely only on the concepts of saturation and conservation of charge, hence the description is valid at current levels both above and below threshold. A mathematical analysis of the circuit is possible using either the above threshold νMOS model from [9] or the subthreshold model from [10]. However, no general closed-form solutions are available; only self-consistent approximate solutions have been obtained. The resulting analysis is somewhat unwieldy and does not offer any insight into the operation of the circuit beyond that obtained from the qualitative description given above.

There is a trade-off between dynamic range and the number of inputs in this circuit. The lower limit of operation is determined by the saturation current in the $N+1$ transistors in the circuit when the drains of all of the input transistors are at ground. This approximation is valid when none of the input currents is large enough to saturate its corresponding input transistor. This current level is determined by the quantity of charge stored on the floating gate. The upper limit of operation is effectively determined by the saturation current in the circuit's $N+1$ transistors when the drain voltage of one of the input transistors is at the positive supply rail. The more inputs there are, the less effective any one of them is at pulling up the floating gate voltage and, hence, the lower the upper limit of operation. The effective dynamic range of the circuit can be increased for the case of many inputs by adapting the charge on the floating gate as a function of the input current levels by means of a simple feedback loop. If the input current levels are too high, positive charge can be placed on the floating gate by means of Fowler-Nordheim tunneling [12] or UV photoinjection [11] thereby increasing the current levels supported by the circuit. If the input current levels are too low, negative charge can be placed on the floating gate by means of hot electron injection [13] or UV photoinjection.

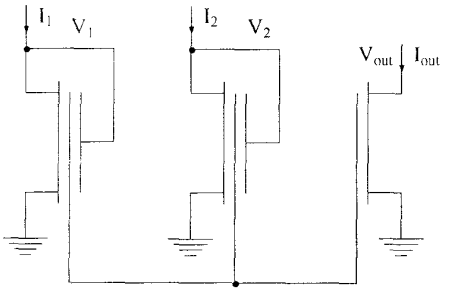

Figure 2: Two-input soft-max current mirror.

III. Experimental Results

The schematic of a two-input soft-maximum current mirror is depicted in Figure 2. Data from such a circuit fabricated in a standard $2.0\mu m$ CMOS process (ORBIT) through the MOSIS service is depicted in Figure 3. In each case, I_2 is held constant while I_1 is swept from below to above the level of I_2. The circles represent the measured output current. The horizontal solid lines represent the measured value of I_2 during each sweep. The diagonal solid line is the measured value of I_1 plotted against itself. As expected, in each case the output current remains constant at nearly the level of I_2 until I_1 exceeds I_2 at which point, the output begins to follow I_1. Data are shown for input current levels ranging over more than five orders of magnitude.

IV. Output Impedance and Voltage Swing

As pointed out in [10], in general care must be taken when using νMOS transistors as current sources because of the

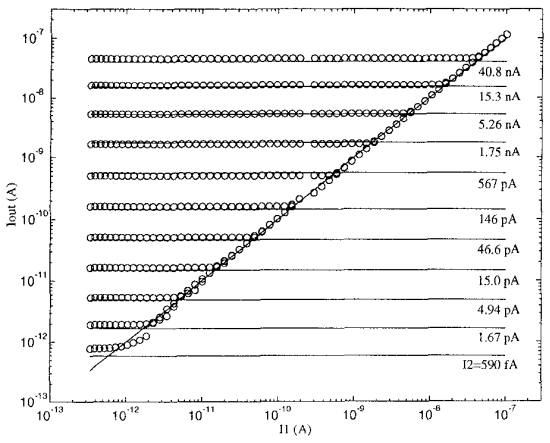

Figure 3: Measured data from a two-input soft-max current mirror. I_1 is swept for various values of I_2. The horizontal solid lines represent the various values of I_2. The diagonal solid line is the measured values of I_1 plotted against itself. The circles represent the measured values of I_{out}. As expected, I_{out} follows the maximum of I_1 and I_2.

parasitic capacitance between the gate and drain of any MOS transistor. Since the gate of a νMOS transistor is floating, the drain voltage is able to couple in via this parasitic capacitance and partially determine the voltage on the floating gate. Since the drain current is a sensitive function of the gate voltage, this small coupling can cause the drain voltage to have a large effect on the drain current through the device, resulting in a relatively low drain resistance. This phenomenon is especially troubling in subthreshold in which case the drain current is an *exponential* function of the drain voltage.

However, the circuit described in this paper has a curious feedback mechanism built into it which completely compensates for this parasitic coupling from the drain of the output transistor to the floating gate. Consider what happens in the circuit if the output voltage is increased slightly. The floating gate voltage will increase slightly, increasing the saturation current level in all of the $N+1$ transistors of the circuit. This, in turn, will cause the drain voltage of the input transistor(s) setting the current level to decrease until the saturation current in all $N+1$ transistors is restored to the original current level.

Data from the two-input circuit depicting this phenomenon is shown in Figure 4. The curve with '$\times$' point markers depicts the result of setting the input current level with a current source and measuring the output current as a function of the output voltage as the output voltage is swept from ground to the positive supply rail. The resulting curve looks very much like a standard MOS drain curve. When the output transistor is saturated, the output current is fairly insensitive to the output voltage. For comparison, the drain voltage of the input transistor setting the current level was measured and clamped at that value with a voltage source thereby disabling the feedback process. The output current was again measured as the output voltage was swept from ground to the positive supply rail. The resulting curve is shown with 'o' point markers. Note that without the feedback the current changes by about 300% as the output voltage changes from rail to rail. From these data, it is also clear that the output voltage swing is limited only by the need to maintain the output transistor in saturation.

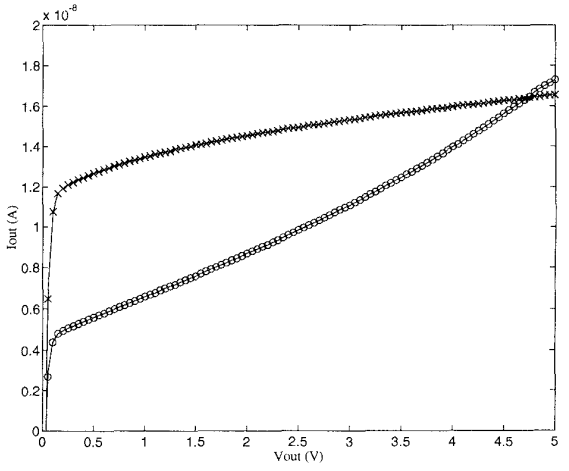

Figure 4: Measured output current as a function of output voltage of the two-input soft-max current mirror. The curve with the '$\times$' pointmarkers is the normal behavior of the circuit with the inputs driven by current sources. The curve with the 'o' pointmarkers represents the behavior of the circuit without the feedback mechanism; i.e., with voltage sources driving the drains of the input transistors instead of current sources.

V. Conclusion

A simple circuit which computes a soft-maximum of $N+1$ input currents has been presented. A qualitative description of the operation of the circuit which is valid at all current levels has been given. Data from a working two-input version of the circuit has been shown. The circuit

features a relatively high output impedance and a high output voltage swing.

VI. Acknowledgements

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