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Supporting Online Material for

Bridging Dimensions: Demultiplexing Ultrahigh-Density Nanowire Circuits

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Supplementary Online Materials

Materials and Methods

1. Demultiplexer Fabrication

This supplement describes our procedure for fabricating the field-effect transistor (FET)-based demultiplexers for addressing a high density array of semiconductor nanowires. All scanning electron microscopy and electron beam lithography were done with an FEI XL-30 scanning electron microscope (SEM) coupled to a computer that operates a Nanometer Pattern Generation System (Nabity Systems) version 6.0. Metal depositions were done using an electron beam evaporator (Semicore Corp, CHA-Mark 40; Freemont, CA) unless otherwise stated. Pictures of the process flow are shown in figure 4 of the text.

The nanowires were fabricated using the superlattice nanowire pattern transfer (SNAP) technique (S1) using a silicon-on-insulator (SOI) wafer (100 orientation; 30 nm thick silicon on 150 nm SiO_2). We have previously demonstrated that, through a combination of precision nanofabrication, diffusion-based doping methods (as opposed to ion-implantation methods), and high-frequency, low-sample bias reactive ion etching, SNAP Si nanowires can be prepared with bulk-like conductivity characteristics (S2). The SNAP process can produce nanowires up to several millimeters in length, although it is typical for sections of the array to have imperfections over that length scale. For the demultiplexer, the section of, for example, 150 SNAP nanowires should be at least 10 μm in length.

One aspect of the diffusion-based doping method that is utilized for increasing the response of the nanowires to field-effect addressing, is the capability for establishing a doping gradient through the thickness of the SOI film from which the nanowires are created. This is discussed in some detail in the Supporting Text, §2.

Ohmic contacts were patterned using standard electron-beam lithography (EBL) procedures, and writing through a polymethyl methacrylate resist that was spun coated onto the wafer. The following process was utilized to develop the EBL pattern: immersion in methyl isobutyl ketone (MIBK): isopropyl alcohol (IPA); 1:3, 60 sec, an IPA rinse for 10 sec, a water rinse ~5 sec, and dry with N_2 gas. Metal deposition is 50-70 Å Ti, 300-500 Å Al, and 200 Å Pt or Ni. The contacts are annealed in an inert Ar or N_2 atmosphere at 450°C for 5 minutes (S3). At this point the conductivity of the nanowires (and the cross-conductivity) is tested. In all circuits reported here cross-conductivity was greater than 1 TΩ, and the nanowires initially exhibited conductivity characteristics that were within a factor of 10 of what was expected from the resistivity measured (using a 4-point probe) for the bulk SOI wafer after diffusion doping.

Starting from good Ohmic contacts, the actual demux may then be constructed. A thick SiO_2 layer is deposited as the low gate capacitance dielectric material. SiO_2 may be deposited by either spin on glass (SOG; Emulsitone Co.) or plasma enhanced chemical vapor deposition (PECVD). The SOG is likely to have a slightly lower κ value than a PECVD oxide due to the lower quality of the film, which is useful for increasing the high- and low-gate contrast but also results in a less homogeneous film, making careful etching of the film difficult. The thickness of this film should be > 50 nm to ensure electrical isolation from top gate electrodes and to minimize the capacitance of the low gate junctions.

After deposition of the SiO_2 film, the film must be removed from the previously defined metal contact pads so that the demux defining etch step may be monitored. ZEP-520A (Zeon Corp.; Tokyo, Japan) is spin coated at 4000 rpm, 30 sec., baked at 200°C for 2 min. Windows slightly smaller than the contact pads are written on top of the contact pads. The oxide is then

etched using a CF_4 plasma reactive-ion etch (RIE). An additional layer of metal may then be re-deposited on the contact pads if necessary.

50% ZEP-520A in chlorobenzene is then used as an EBL resist and RIE etch mask to define the binary tree gated regions. The ZEP-520A is developed in a solution of 1:1 MIBK:IPA for 60 sec, 10 sec IPA, water rinse, N_2 dry. A brief O_2 plasma (15 sccm O_2, 20 mTorr, 40 W at 40 MHz, ~10 sec), cleans the developed areas before etching in an RIE etch gas mix of CF_4/He/H_2 at 20 sccm/30 sccm/2.5 sccm at a total pressure of 5 mTorr, and an RF power of 40 W. The endpoint is determined by an interferometer used on a blank Si wafer prepared with an oxide film identical to the sample.

Recalling the doping gradient along the z-axis of the nanowires (Fig. 2 and supporting text), the SiO_2 etch step can then be used to lower the doping concentration of the wires in precisely the regions where we would like to have a high gate response. As the endpoint of the etch is approached, the etch may be slightly prolonged to remove the highly-doped top layer of the SNAP wires. Special care must be taken to not over etch the wire, as the doping level drops significantly below ~ 10 nm. To monitor the over-etch step, iterations of etching, followed by conductance measurements of the SNAP wires are done to insure that the nanowires are not significantly damaged during the etch process. When the conductivity has been lowered to a satisfactory level, the remaining ZEP-520A residue is removed by liftoff and sonication in acetone.

Following the critical SiO_2 etch, HfO_2 is deposited as a high-κ dielectric for the high gate AND junctions. A window in a layer of 5.5% MMA and 3% PMMA layer is patterned over the entire binary decoder pattern. Hf metal is evaporated in an O_2 atmosphere (15 sccm O_2, 6.7×10^{-5} Torr) using a modified CHA evaporator identical to the one used to deposit the gate dielectric for

previous gating experiments. The thinnest possible HfO_2 film should be used to maximize the gate capacitance; a thickness of ~3 nm (determined by elipsometry) is typically sufficient.

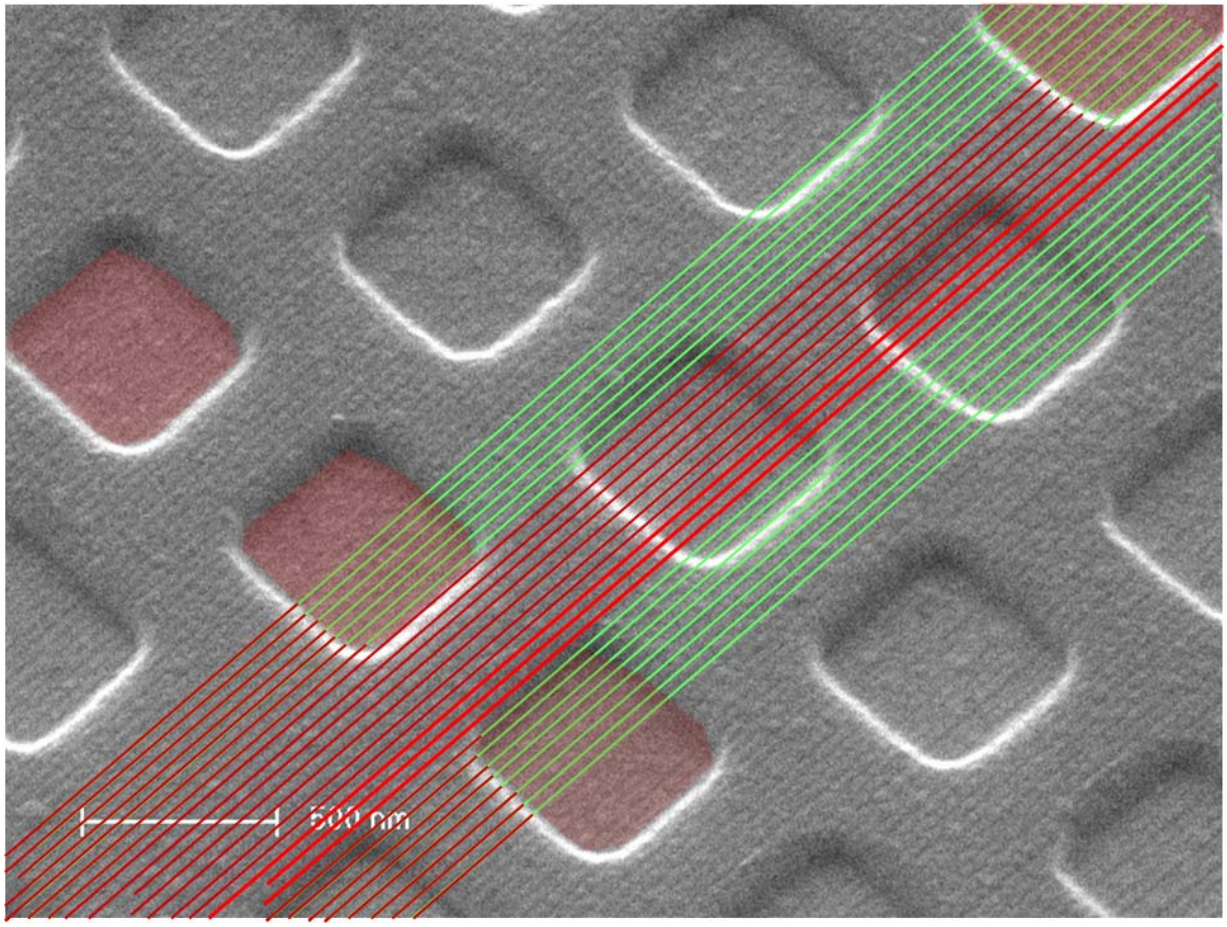

Figure S1. Detailed view illustrating the ability of the demultiplexer design to select out very few nanowires, and to thus enable the testing of the worst-case scenario for nanowire addressing. Note that the pattern of the SNAP nanowires is observed as ridges in the overlying dielectric thin films. All wires are initially red-colored, to indicate that they are in the conducting state. Once a nanowire is gated, it is switched to the green, or non-conducting state. Only nanowires, colored bright red, are selected in this address configuration.

The final step is the deposition of top gate electrodes (100 Å Ti/ ≥ 1000 Å Al/ 200 Å Pt or Ni). The total thickness of the metal layer should be greater than the depth of the holes in the SiO_2 to ensure that the gate electrodes are continuous. The final metal deposition is lifted off in acetone.

A final gentle cleaning may be done by heating the device in a high boiling-point organic solvent (like anisole) just below the boiling point of the liquid.

2. Detail on Testing and Validation of Nanowire Demultiplexer

One of the key aspects of the testing and validation of the multiplexer resides in the ability of this device to interrogate the worst case scenario – i.e. comparing nanowires that are just adjacent to a gate electrode, versus nanowires that lie underneath a gate electrode. This was accomplished here by fabricating the smallest binary tree gate electrodes in a specific way, and registering those electrodes with the 16 test contacts (Fig. 3A). The gated regions of the nanowires (regions in which the nanowires are separated from the metal gates by the HfO_2 high-κ dielectric) were significantly larger than the spacing between those gates. Under those spacings, the nanowires are isolated by the low-κ SiO_2 dielectric. This pattern is shown in Fig. S1. The electron micrograph utilized in this Figure was collected prior to fully fabricating the demultiplexer. At this point in fabrication, the binary tree has been patterned by etching through the low-κ SiO_2 dielectric film, and the thin, high-κ HfO_2 film has been deposited. Note that in this figure it is possible to see the underlying SNAP Si nanowire array manifest itself as a periodic structure of lines on top of the film. Thus, it is possible to identify which wires are isolated for a given gate address. Five rows of gates are shown in Fig. S1, running perpendicular to the direction of the nanowire array. The right four of those rows correspond to the rightmost gating electrodes shown in figure 4 of the Report, and so are the smallest gate electrodes that were patterned. In the image, we simulate an addressing experiment by coloring the regions through which a gate voltage is applied red. The 4 red pads that are drawn would correspond to an address of '10' on the narrowest pitch wire pairs. Approximately 25 wires, registered with the underlying SNAP nanowire array, are drawn in red or green. When a wire passes under an

active gate (and is deselected), it is switched from red to green color. Note that only the 3 bright red wires pass through the demultiplexer without being de-selected. At least 1 or 2 of these wires is contacted to one of the 16 test electrodes. This example is characteristic of how the demultiplexer was constructed and how the gates and test electrodes were registered to one another. Thus, to best of our ability to tell, this demultiplexer design allowed for a testing of the worst case, or at least near-worst case, scenario, such as is described in the text.

Supplementary Text

1. Defect Tolerance

Any demultiplexing architecture that can bridge the patterning densities that are possible using novel nanofabrication methods to those achievable through lithographic patterning must meet three requirements: 1) it must be tolerant of manufacturing defects; 2) it must take into account the limitations of both the nanofabrication method and the lithographic patterning approach; 3) it should utilize order $\log_2(\boldsymbol{N})$ lithographically patterned demultiplexer wires to address $\boldsymbol{N}$ nanowires. All three issues are interrelated. In this section, we discuss these issues within the context of the demultiplexer scheme presented within the Report.

There are a number of nanofabrication methods for preparing aligned arrays of semiconducting nanowires. Depending on how precisely the dimensions of the nanowire array (i.e. nanowire diameter, length, pitch, etc.) can be controlled, more or less may be required from the nanowires themselves, or from the demultiplexer fabrication process. Nanowire arrays have been assembled using various techniques. One approach is to utilize Langmuir-Blodgett techniques for both preparing and organizing the nanowires (S4), or to just organize nanowires that have been previously prepared using materials synthesis techniques (S5, S6). Another approach is to harness competing interactions (i.e. long range Coulombic repulsions and short-

range van der Waals attractions) to control the structure of the nanowire array (S7, S8). Finally, the method used in this Report, called superlattice nanowire pattern transfer, or SNAP, utilizes the edges of superlattices as templates for depositing and transferring metal nanowires onto a silicon-on-insulator substrate (S1). Those metal nanowires then serve as etch masks for preparing an array of aligned silicon nanowires. For most of these methods, nanowire diameter,

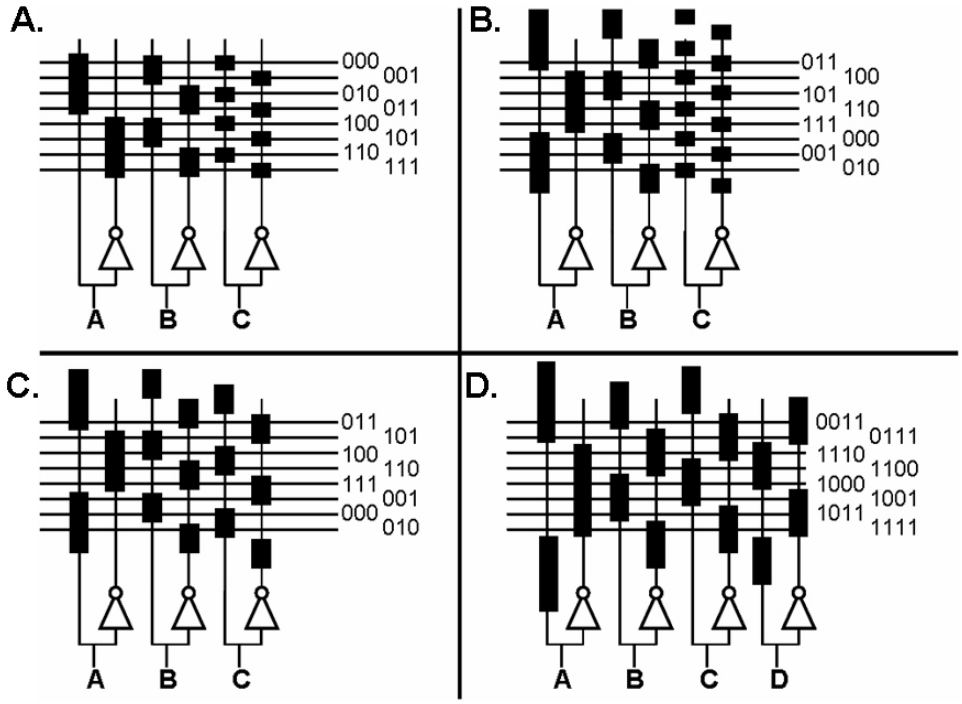

Figure S2. The operation of a binary tree demultiplexer, as the fabrication requirements for the demultiplexer are relaxed. The nanowires are represented by 8 horizontal wires, and the demultiplexer by 3 vertical complementary wire pairs. The operation of a complementary wire pair may be understood by considering an input address of '1' to wire pair A. The left wire is sent high by this address, and the right wire is sent low. For an input address of '0', the reverse is true. The gates are shown as bars. When a nanowire passes under a bar that is connected to a wire in the high state, that nanowire is deselected. The input address that selects each nanowire is indicated next to the nanowire. A. A standard binary tree demultiplexer; B. A binary tree demultiplexer in which the binary tree pattern is not registered with specific nanowires, and extends beyond the limits of the nanowire pattern. Note that the addresses are no longer sequential. C. The binary tree pattern of gate electrodes is shown at twice the pitch and twice the feature size of the nanowire array. Note that $2\log_2(\boldsymbol{N})$ address wires are still need to address $\boldsymbol{N}$ nanowires. D. The binary tree pattern of gate electrodes is shown at three times the pitch and three times the feature size of the nanowire. Note that an additional pair of address wires is needed, and so half of all address values are inactive.

pitch, alignment, etc., are only approximately controlled. The proposed demultiplexing concepts then require a combination of sophisticated nanowires (i.e. nanowires in which the dopants are controlled along the axial dimensions (S9, S10, S11)) and demultiplexers with several additional (redundant) address lines. This has consequences that extend beyond the need to build a larger demultiplexer, as described below. For the SNAP nanowires, all of the nanowire dimensions are controlled to a nearly atomic level of perfection, and this substantially eases the requirements on both the nanowires and on the demultiplexer. Rather than requiring the demultiplexer to bridge fabrication approaches and dimensions, it only has to bridge dimensions.

The binary decoder architecture used for the FET-based demultiplexer is a defect tolerant design that can allow for large margins of error in its implementation and still remain fully functional. This architecture provides at least partial solutions to two issues: 1) alignment of the submicrometer demultiplexer features with the nanoscale features of a nanowire array and, 2) the use of large demultiplexer feature sizes and feature pitches to address a nanowire array that is characterized by a substantially smaller (but tightly defined) nanowire width and pitch. Here we first discuss these issues within the context of the architecture, using Figure S2 to guide the discussion. We then we discuss these same issues within the context of the high-resolution lithographic patterning techniques utilized to define the demultiplexer. For the following discussion, we consider the x-direction to be along the axis of the nanowires to be demultiplexed, and the y-axis to be perpendicular to that axis.

Alignment Tolerance through Architecture

Alignment along the x-axis of the nanowires is relatively straightforward for SNAP nanowires, since those nanowires can be extremely long (typically millimeters). Thus, the key problem to solve involves alignment in the y-direction. A partial solution to this problem is to

fabricate the binary tree of the demultiplexer with a repeating pattern, the period of which is equal to the width of the nanowire array. In this fashion, the decoder pattern will extend beyond the boundaries of the array (Fig. S2B). If, for example, the decoder pattern misses its intended position on the nanowire array by 500 nm, causing the top 500 nm of addresses to miss their mark, the addresses are simply repeated at the bottom of the array. The decoder pattern can be fabricated to an arbitrary length, giving any amount of y-axis tolerance desired. The cost of giving up absolute demultiplexer alignment is that the knowledge of which nanowire corresponds to which demultiplexer address is lost. However, it is still possible to know that every nanowire has a unique address, and that is the key issue.

Feature Size Tolerance through Architecture

The second challenge towards bridging the dimensions from the nanometer features of a nanowire array to the sub-micrometer features of the demultiplexer revolves around the limits of the lithography used to define the demultiplexer binary tree features. For the binary decoder that is depicted in Fig. S2C, the narrowest pitch gate patterns on the address wires are at twice the pitch of the output wires, and there is no need for redundant address lines (i.e. the scaling is $2\log_2 \boldsymbol{N}$ address wires for $\boldsymbol{N}$ nanowires). In reality, addressing an array of 30 nm pitch Si nanowires, such as those utilized within the Report, with large repetitions of 60 nm pitch gate electrodes is difficult. However, the gate electrodes may be fabricated at a pitch that is **n** times the nanowire pitch, where **n** is an integer, and an example is given in Fig. S2D. for **n**=3. This requires an additional input wire pair and then offsetting the placement of the gates by a single nanowire pitch. Note that taking any three out of the four input addresses does not produce a set of unique addresses for the 8 nanowires shown – all four are needed. This type of alignment, in which the gates are aligned to one another with high precision but not aligned with the

underlying pattern, is practical to achieve (as discussed below). However, there are three 'penalties' associated with adding additional wire pairs. The first penalty is simply that a larger demultiplexer must be fabricated. The second and third penalties result from the fact that each additional address pair of demultiplexing wires reduces the number of good address by half. For example, for 2 additional address pairs, 75% of all addresses will be invalid. This is demonstrated in Fig. S2D, in which one additional pair of address lines is needed, and only 50% of all possible input addresses actually identify a wire. The second penalty, then, is that the 'good' addresses would have to be stored in memory. Since the number of good addresses is nominally the number of nanowires to be demultiplexed, this penalty is not particularly onerous. On the other hand, finding those good addresses requires significant testing of the circuit, and this penalty increases significantly as additional address wire pairs are needed. For the two other demultiplexer concepts referenced in the Report, the number of large wires need to address $\boldsymbol{N}$ nanowires scales as $5\times\log_2(\boldsymbol{N})$ (S12) or $[2.2\times\log_2(\boldsymbol{N})]+11$ (S13). For those cases, the vast majority of all possible addresses are invalid. The point at which these penalties outweigh the benefits of the circuit will vary from application to application. Nevertheless, by applying the scheme demonstrated in Fig S2.D., an arbitrary pitch for the address wire gates may be utilized with the addition of extra address wire pairs.

Alignment Tolerance through Patterning

One alignment issue that is not solved by having the periodically repeating gate structures shown in Fig S2B is illustrated by the drawings of Fig S3. Note that in Fig. S3A it is clear that D represents a deselected nanowire, and S represents a selected nanowire. For Fig. S3B, it is not clear whether the nanowire labeled S is deselected or selected. The implication is that it is necessary to control the placement of the gate electrodes to at least one-half of the pitch of the nanowires. This is true, but, as described below, that accuracy is only required for the relative placement of the gated with respect to each other, rather than with respect to the underlying nanowire array. We turn now to this describing this issue in some detail.

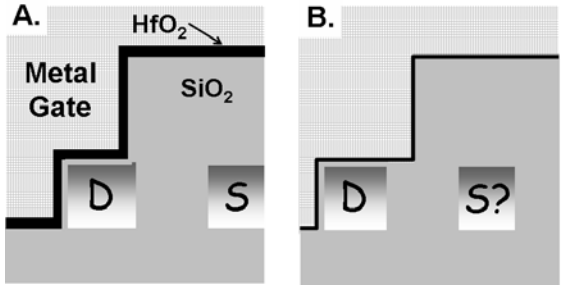

Figure S3. An illustration of the importance of alignment precision between the demultiplexer gate structure and the underlying nanowire array. **A.** A perfectly fabricated demultiplexer gate structure, with a deselected (D) and selected (S) nanowire. **B.** An imperfectly fabricated demultiplexer. The nanowire labeled D is clearly deselected, but it is not clear that S is selected.

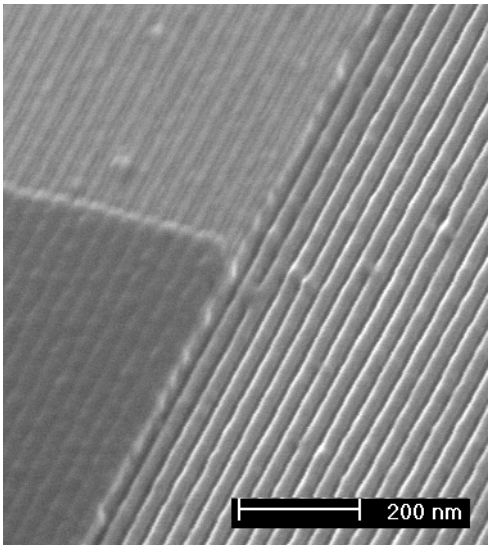

Figure S4. An illustration of the ability of lithographic patterning to define highly oriented and well-defined patterns with nanometer scale precision. The picture is an electron micrograph of an array of silicon nanowires (14 nm wide, 34 nm pitch). The nanowires at the top left are planarized with a thin SiO_2 film. The nanowires at the bottom left are coated with a dielectric plus a thin metal film. The nanowires at the right are coated with a thin dielectric.

Absolute alignment of the demultiplexer pattern with an underlying nanowire array to a few nanometers accuracy is difficult, but highly precise relative alignment of the demultiplexer features with each other is relatively straightforward. In other words, precisely defining the gated regions with respect to each other rather than with respect to the

underlying nanowires is readily achievable. In addition, angular alignment (i.e. orienting the demultiplexer pattern at 90^o to the nanowire array) can also be accomplished with high precision. These issues are demonstrated in the SEM micrograph of Figure S4. Given these constraints, the FET-based demultiplexer described in the Report can be made tolerant to large alignment errors in both the x and y directions, and it can be fabricated with features that are substantially larger than those that characterize the nanowire array. This can be done through the use of redundant demultiplexer address lines. However, unlike for the situation discussed in the preceding section, these redundant address lines do not lead to redundant addresses. Instead, redundant wire pairs are separately tested and then one of them is selected according to which address wire pair yields the best performance.

The concept is to take advantage of the precise relative alignment that can be achieved through methods such as electron-beam lithography (and can be replicated through nanoimprinting (S14,S15)), and yet still not require absolute alignment which can be difficult or impossible to achieve. Figure S5 illustrates this concept, which consists essentially of incorporating an additional set of gate electrodes with a slight phase shift with the following important qualifications. First, such redundancy in the demultiplexer is probably only required for those address wires with the smallest gate electrode

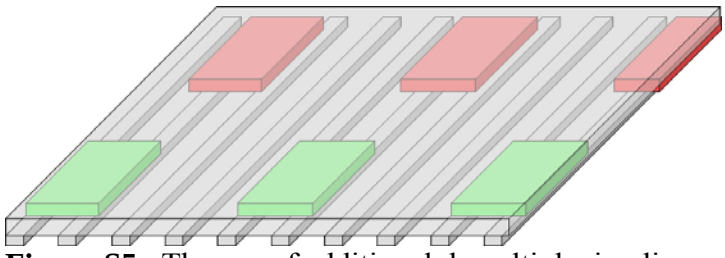

Figure S5. The use of additional demultiplexing lines (but not additional addresses) is illustrated in this drawing. An array of 10 nanowires is shown. Using the nanowire pitch (P) and width (W) as a reference, two gate electrode patterns (green and red) are drawn with a width = P + W and a pitch = 4P. The red gates are shifted by ½ a nanowire pitch relative to the green gates. Upon testing, the demultiplexer wire that utilizes the green gates would be expected to give superior selectivity compared to the one that utilizes the red gates. Only the demultiplexer wire with superior performance would be used to address the nanowire array.

regions. For address wires with large gate electrode regions, very few nanowires will have a poorly defined selection/deselection. Second, for a nanowire array that is not characterized by a well-defined nanowire width and pitch, the scheme illustrated in Fig. S5 will not work.

Even with the additional wires fabricated into the demultiplexer, as shown in Figure S5, the selectivity of the demultiplexer will still be limited by the resolution of the lithographic technique that it utilizes. Careful inspection of Figure S4 reveals that the lithographically defined regions are not perfectly straight, but instead fluctuate with an amplitude of about 3-4 nm. Without significant improvements in this technology, it is likely that such fluctuations will eventually prove limiting for this demultiplexer scheme when applied to nanowires patterned at a pitch of less than 10-15 nm or so.

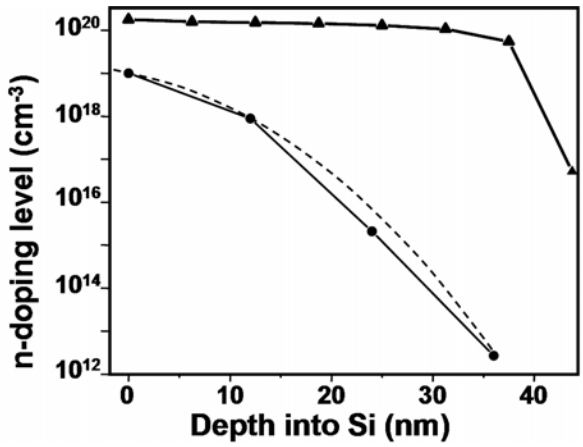

Figure S6. Measured doping profile through the 40 nm thick silicon film on the silicon-on-insulator wafers from which the nanowires were patterned. The top trace (triangles) represents a film that was uniformly doped throughout its thickness, and the bottom trace (circles) represents a doping gradient. Gradient doping was utilized for the preparing the wafers from which the SNAP silicon nanowires were patterned. The dashed line is a mathematical model of the doping profile that is based upon the one-dimensional diffusion equation.

2. Doping Gradients through Nanowires and Doping Calculations

Control over the vertical doping profile in a nanowire is of great assistance for translating this demultiplexer architecture into a working circuit. Data showing such control is presented in Figure S6. The standard method for achieving a high level of control over the doping of Si devices is ion-implantation doping. For nanowires, this method is not particularly useful, as it leads to defects in the silicon wafer which seriously damage the

conductivity characteristics of very thin nanowires. Thus, for the SNAP nanowires, we utilized diffusion based doping of the silicon-on-insulator wafer from which the nanowires were fabricated. In this section, we describe the mathematical calculation for the doping profile through the thickness of a silicon nanowire that was presented in Fig S6.

The diffusion of dopant atoms into Si is approximately governed by the 1-D diffusion equation

$$\frac{\partial C(x,t)}{\partial t} = D(T)\frac{\partial^2 C(x,t)}{\partial x^2},$$

where C is the dopant concentration, x is the depth into the Si epilayer, T is the anneal temperature, t is the anneal time, and $D(T)$ is the temperature dependent diffusivity for Si and is given by the empirical relation

$$D(T) = A\exp\left(-\frac{E}{8.6\times10^{-5}T/K}\right),$$

with A and E constants of order unity (which can be looked up in any semiconductor processing book) that depend on the diffusing dopant atom (S16). Our theoretical doping profile is calculated from the 1-D diffusion equation subject to the following boundary conditions:

1) A constant dopant concentration at the Si surface. Note that this boundary condition is completely physical for diffusion doping from a spin-on glass and is mathematically stated as $C(0,t) = C_o$, where C_o is the dopant concentration at the surface (which is known from the concentration of our spin-on glass)

2) The dopant concentration goes to zero at some depth relatively far from the surface. This boundary condition can be stated mathematically as $C(\infty,t) = 0$.

The solution of the above boundary value problem is given by

$$C(x,t,T) = C_o erfc\left(\frac{x}{2\sqrt{D(T)t}}\right),$$

where *erfc* is the complementary error function.

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