PHOTODEFINABLE SILICONE MEMS GASKETS AND O-RINGS FOR MICROFLUIDICS PACKAGING

Scott Miserendino^{*}, Yu-Chong Tai California Institute of Technology, Pasadena, CA, USA (*Corresponding Author. Email: scott@mems.caltech.edu)

ABSTRACT

Fully-integrated MEMS gaskets and O-rings made of SU8 and photosensitive silicone are described and tested under varying conditions of compressive stress. An analytical theory of microgasket sealing behavior is also presented. The theory shows the critical importance of device surface flatness. The microgasket is found to be capable of deforming approximately 25% of its initial thickness and forming leak-free fluidic seals at inlet pressures below 50 psi. The microgasket is incorporated into a modular microfluidic system that exhibits system leak rates lower than 2.3 nL/min for working pressures up to 250 psi. Fabricated chip-to-chip interconnects exhibit a low dead volume of approximately 9 nL while further optimization can reduce dead volume per interconnect to about 1 nL.

1. INTRODUCTION

Microfluidic packaging that exhibits low leak rates, high maximum sealing pressures, no clogging, good thermal stability, chemical inertness, high mechanical strength, low dead volume, integrated fabrication, and fundamental ease-of-use has been desired for almost ten years yet has proven elusive. Glues and epoxies naturally were the first techniques explored but exhibited many difficulties such as under/over dosing, contamination from the glue, easy clogging, and low operational pressure drops. Other interconnect techniques have been suggested to improve the sealing properties of a microfluidic device and a piece of tubing or silica capillary and can not easily be applied to modular microfluidic systems [1].

Here, we introduce and demonstrate a fully integrated micro gaskets and o-ring technology. These micro gaskets and o-rings can be directly fabricated on top of microfluidic device chips or on separate interconnect chips so both chip-to-chip and chip-to-package high-performance microfluidic connections can be simplified. This technology enables the construction of multi-chip systems with >200 psi pressure limit and a minimized dead volume of approximately one nanoliter per via.

2. DESIGN AND FABRICATION

The usefulness of the micro gaskets and o-rings is demonstrated in a two-chip microfluidic system. The interconnect chip is fabricated on a soda-lime glass substrate for optical transparency and incorporates a novel, integrated microgasket that seals the vias between the interconnect and device chips. Due to the precise CNC machining of the jig, the interconnect chip and device chips can typically be aligned to within 100 μ m. The entire system is compression sealed using four screws and an acrylic cover piece.

All microfluidic components are fabricated using surface micromachining Parvlene-based. techniques. Parylene microfluidics provides several advantages over other common microfluidic technologies such as PDMS, glass, and silicon. Parylene-C is highly biocompatible and is recognized for having the highest biocompatibility rating (USP Class VI) by the US Food and Drug Administration which qualifies it for use in chronic biomedical implants[2, This high biocompatibility comes from its highly 31. chemically inert structure. Parylene microfluidic techniques have been developed that can resist internal fluid pressures above 1000 psi which allows its use in high pressure applications that are inaccessible to PDMS with its top working pressure between 75 and 100 psi [4, 5].

Interconnect and Device Chip Microfabrication

The interconnect and device chip are microfabricated using embedded parylene microchannel technology. The fabrication processes for the two types of chips are nearly identical, although there is no requirement that the device chip be fabricated using the interconnect chip process. Cross-sectional diagrams of the fabrication process are shown in Fig. 1. Soda-lime glass substrates were used for both device and interconnect chips.

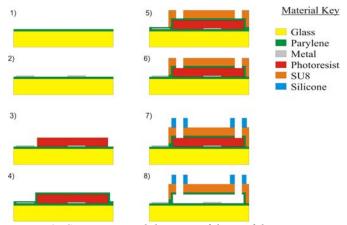


Figure 1: Cross-sectional diagram of device fabrication.

A 3 μ m layer of Parylene-C is deposited on both devices using silane A174 (Specialty Coating Systems) as an adhesion promoter. A metal layer is added to the device chip substrate by electron beam evaporation and patterned by lift off. Microchannels are formed by patterning thick photoresist (20 to 50 μ m). This sacrificial layer of

369

photoresist is then conformally coated with a second, 3 μ m layer of Parylene. The surface of the wafer is planarized using a 65 μ m thick layer of SU8. The SU8 is patterned to open the fluidic vias. The Parylene beneath the SU8 vias is then removed using oxygen plasma in a reactive ion etcher (RIE).

For interconnect chip fabrication a layer of photodefinable silicone (Dow Corning WL-5150) is spun on to a thickness of approximately 30 μ m. The silicone is then patterned. After development of the silicone it is necessary to remove all residual silicone scum from the vias. The scum layer is removed using an SF₆/O₂ plasma in a RIE. A dry etching rate for the silicone of approximately 0.15 μ m/min was achieved using 75 sccm O₂, 50 sccm SF₆ at 200 mtorr chamber pressure and 180 W of RF power. Finally, the wafer is diced and the sacrificial photoresist is released in isopropyl alcohol at 80°C. The SU8/silicone stack acts as a photodefinable microgasket (Fig. 2). When the chips are squeezed together by tightening the screws, the silicone compresses sealing the fluidic vias on the device chips.

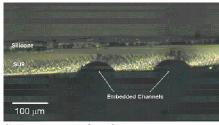


Figure 2: Cross-section of gasket structure.

3. MICROGASKET THEORY

For a proper seal, the gasket must form an enclosed contact with the device chip around the vias. The gasket must also have enough compressive force to both initially seat the gasket and to overcome any hydrostatic end force developed by the internal fluid. It is understandable that gasket contact is not a major concern for macro gaskets because they are typically thick and can compress a distance well in excess of the amplitude of flange surface irregularity. But for microgaskets the maximum compression is near or possibly smaller than the variation in surface flatness. In other words, the level of surface irregularities and the gasket compressibility become the critical factors for the use of microgaskets.

For any gasketed-flange system to be leak-free the compressive force on each gasket supplied by the screws must exceed the hydrostatic end force applied to the flange by the fluid in the system. This balance can be expressed mathematically for an annular gasket geometry made from a self-energizing gasket material (gasket factor, m = 0) as:

$$H_G = M\pi \left(\frac{G}{2}\right)^2 P \tag{1}$$

$$H_G \le \frac{NT}{KD_f} \tag{2}$$

where H_G is the hydrostatic end force, M is the number of identical gaskets under simultaneous compression, G is the diameter at location of gasket load reaction, P is the internal working pressure, N is the number of bolts, T is the torque on each bolt, K is the bolt friction factor (typically 0.20 for a dry bolt and 0.16 for a lubricated bolt), and D_f is the nominal bolt diameter [6]. The force balance and system geometry is depicted in Fig. 3 for a two-device, single interconnect system. According to the American Society of Mechanical Engineering (ASME) Code for Pressure Vessels Section VIII Division 1 for typical microgasket geometries, G is defined as the mean gasket diameter

$$G = D_{o} - W_{o} \tag{3}$$

where D_g is the outer gasket diameter and W_g is the width of the gasket.

Using the ASME definition of G and rearranging equations (1) and (2) to show the maximum working pressure sustainable

$$P \le \frac{4NT}{\pi MKD_{f} \left(D_{g} - W_{g}\right)^{2}} \tag{4}$$

For a typical two-chip modular fluidic system $D_g = 900 \ \mu m$, $W_g = 250 \ \mu m$, and M = 36.

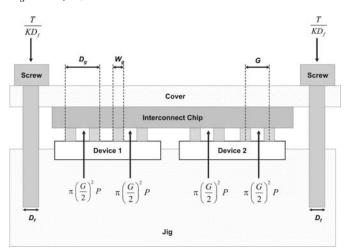


Figure 3: Force balance diagram of modular microfluidic system under compression.

Microgaskets verse Micro O-rings

The flange surface profile plays a critical role in microgasket sealing behavior. Consider two types of microgaskets both of thickness, t, having maximum compressibility percentage, C_{max} , and minimum compression percentage required for sealing, C_{seal} . The first type of gasket is a flat gasket that covers the entire surface of the interconnect chip except the vias. The flange surface must have a global height minimum, y_{min} , and maximum, y_{max} . The second type of gasket is a patterned gasket, or micro o-ring, that has a sealing radius, r, that must be in contact with the device chip surface to seal. For the micro o-rings we define a local minimum, y'_{min} , and local maximum, y'_{max} , on the flange surface within a radius *r* of the via. To guarantee the flat gasket seals across the surface

$$y_{\max} - y_{\min} \le (C_{\max} - C_{seal})t \tag{5}$$

For the micro o-rings to seal

$$y_{\max}^r - y_{\min}^r \le \left(C_{\max} - C_{seal}\right)t \tag{6}$$

To guarantee simultaneous sealing of M micro o-rings with sealing radius, r_i

$$\max_{\leq i \leq M} \left[y_{\max}^{r_i} \right] - \min_{1 \leq i \leq M} \left[y_{\min}^{r_i} \right] \leq \left(C_{\max} - C_{seal} \right) t \tag{7}$$

Note that for the M micro o-rings as M grows this case collapses into the flat gasket condition of equation (5). For a particular gasket thickness, maximum compressibility, and minimum sealing compression, equations (5) and (7) bound the allowable surface height variation of the flange. Even without exact parameters, using this worse-case analysis, we can conclude that patterned gaskets, specifically o-rings, do no worse then the flat gasket.

IV. EXPERIMENTAL

The functional characteristics of the microgasket were tested by measuring the gasket compression versus varying degrees of compressive stress. The leak rate of the entire system was measured under constant compressive stress but varying inlet pressures.

Gasket Compression Tests

As the four screws are tightened on the jig a compressive stress develops in the gasket causing it to deform and seal the fluidic vias. The amount of compressive stress achieved as a function of uniform screw torque can be calculated as

$$\overline{S}_g = \frac{NT}{A_g K D_f},\tag{8}$$

where A_g is the total gasket surface area and all other variables are defined as before. During the compression and leak rate tests, a flat gasket under uniform compression was used. A flat gasket, as opposed to a patterned gasket, was necessary to achieve a significant range of compressive stress given the resolution of the torque wrench. To achieve uniform compression each screw was tightened with a torque wrench in 2 in-lb increments in a crisscross pattern until the final desired torque was reached.

An indirect technique based on parallel plate capacitance was used to monitor the thickness changes. The first capacitor is formed by SU8 with a reported relative permittivity, ε_r , of 4 and is assumed to be fixed [7]. The second capacitor is formed by the silicone and is expected to vary as the silicone is compressed. The silicone manufacturer reports a relative permittivity of 3.2 at 1 MHz [8]. The ratio of the change in capacitance to the initial

capacitance is a function of the thicknesses and relative permittivities of the layered materials, and can be expressed as

$$\frac{\Delta C}{C_0} = \frac{\varepsilon_{r,SU8} \left(t_{silicone}^0 - t_{silicone}^c \right)}{t_{SU8} \varepsilon_{r,silicone} + t_{silicone}^c \varepsilon_{r,SU8}},\tag{9}$$

where θ indicate pre-compression conditions, c indicates conditions under compression, C is capacitance, t is thickness, and ε_r is relative permittivity. The surface area is assumed to be unchanged by the compression. Using this model, the compressibility of the microgasket can be measured as a function of compressive stress (Fig. 4). The silicone can compress to approximately 25% of its initial thickness and is fully compressed by a compressive stress of 750 psi.

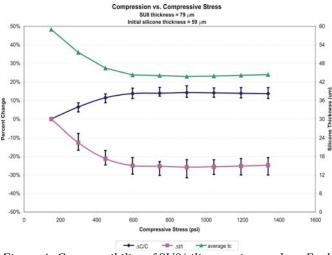


Figure 4: Compressibility of SU8/silicone microgasket. Each data point represents the average of five measurements at the indicated compressive stress and the error bars mark the minimum and maximum values obtained during all trials (only average data for compressed silicone thickness is shown).

Leak Rate Measurements

Experimental observations suggest that the relative shape of the vias on the device and interconnect chips is important in establishing a good seal. Three circular geometries were studied: smaller device vias, smaller interconnect vias, and All three geometries were capable of same-size vias. establishing a seal but when used in multiple device systems smaller interconnect vias proved to be the most robust (able to seal the most vias simultaneously). The smaller interconnect vias have a portion of the gasket material that overlaps the edge of the device via. It is at this point of overlap that the strongest seals are formed because the gasket material deforms into the device via instead of merely being compressed around it. This effect is similar to that of a raised-ridge design in a standard gasketed-flange system.

The leak rate of a complete modular system consisting of a single device chip and an interconnect chip

was measured. A constant volumetric flow rate test at 5 μ L/min showed the system sealed between 300 and 400 psi of compressive stress with no measurable leak rate for compressive stresses at or above 400 psi.

In a second test, a constant compressive stress of approximately 1100 psi was applied to fully compress the gasket. The system was then filled with food coloring to aid in visualization of fluid flow. The outlet port on the jig was sealed using a screw and Teflon tape. Varying amounts of pressure were applied using pressurized nitrogen gas. The change in position of the fluid front was monitored over time to determine the system leak rate. Leak rates below 2.3 nL/min were observed for all inlet pressures below 250 psi with no observable leak rate below 50 psi.

The leak rate reported here is that of the entire system. It is believed that the microgaskets did not leak but instead the observed leak was from the commercial fittings and plug screw. No leaking could be observed from the microgasket regions under the microscope. The system failed at inlet pressures above 250 psi. The failure occurred in the embedded Parylene channels when the two layers of Parylene delaminated under high pressure. This failure mode was observed in all trials at approximately 250 psi. No other failure mode was observed.

5. DISCUSSION

The failure of the embedded channel structure at 250 psi has precluded experimentally determining the maximum sustainable working pressure of the microgaskets. The microgasket theory predicts high working pressures but also shows that surface profile variations of the device chips can cause sealing problems. While it is possible to achieve sealing using the flat gaskets, that system geometry has been experimentally limited to a single device chip. To extend the usefulness of this design concept multiple device chips must be sealed simultaneously. The micro o-rings offer a superior gasket geometry proven to seal across multiple devices.

Another concern of any microfluidic system is the minimization of the dead volume. For purposes of quantitative assessment, we will define the dead volume in the via as that volume of liquid that achieves a fluid velocity less than 1% of the inlet flow velocity to the via. The threedimensional flow velocity profile for a 4 mm/sec inlet flow velocity of room-temperature water was numerically simulated using COMSOL Multiphysics Package with Matlab (The Mathworks, Inc.) based on the fabricated via geometry. Using the finite element simulation the dead volume in the via is estimated to be approximately 9 nL. The dead volume can be minimized by reducing the channel diameters and the inner gasket and flange diameters subject to the alignment constraints. Using optimal via geometry for 100 μ m x 25 μ m channels, the dead volume could be reduced to approximately 1 nL per via.

6. CONCLUSION

The introduction here of a robust, easy-to-use, fully integrated interconnect technology makes the possibility of widespread interchangeable microfluidic devices and complex microfluidic systems feasible. The microgasket sealing theory confirms the feasibility of surface micromachined gaskets for use in modular microfluidic systems. It is concluded that micro o-rings are superior over unpatterned gaskets. As the complexity of microfluidic systems increase, the need to independently design and fabricate system components will become greater for many applications. Modular microfluidics will be necessary to reduce system research and development time, improve system flexibility, and allow for system maintenance. By separating system component fabrication, individual parts can be more readily optimized and characterized. These advantages of modular microfluidics far outweigh the minimal increase in cost and complexity associated with the fabrication of an interconnect chip.

ACKNOWLEDGEMENT

This work was supported by the Center for Cell Mimetic Space Exploration (CMISE), a NASA University Research, Engineering and Technology Institute (URETI), under award number #NCC 2-1364.

REFERENCES

- C. K. Fredrickson and Z. H. Fan, "Macro-to-micro interfaces for microfluidic devices," *Lab Chip*, vol. 4, pp. 526-533, 2004.
- [2] D. C. Rodger, J. D. Weiland, M. S. Humayun, and Y. C. Tai, "Scalable high lead-count parylene package for retinal prostheses," *Sens. Actuators B: Chemical*, vol. 117, pp. 107-114, Sep 12 2006.
- [3] N. Stark, "Literature Review: Biological Safety of Parylene C", Medical Plastics and Biomaterials, 3(2), 1996.
- [4] A. M. Christensen, D. A. Chang-Yen, and B. K. Gale, "Characterization of interconnects used in PDMS microfluidic systems," *J. Micromech. Microeng.*, vol. 15, pp. 928-934, May 2005.
- [5] Q. He, C. Pang, Y.-C. Tai, and T. D. Lee, "Ion liquid chromatography on-a-chip with beads-packed parylene column," in *Proc. MEMS 2004*, Maastricht, the Netherlands, 2004, pp. 212-215.
- [6] D. E. Czernik, *Gaskets: Design, Selection, and Testing*. New York: McGraw-Hill, 1996.
- [7] J. R. Thorpe, D. P. Steenson, and R. E. Miles, "High frequency transmission line using micromachined polymer dielectric," *Electronics Letters*, vol. 34, pp. 1237-1238, 1998.
- [8] Dow Corning Corporation, MI. (2003). Information About Dow Corning Brand Low-Stress Patternable Silicone Materials. [Online]. Available: <u>http://www.dowcorning.com/contentapps/abstracts_index.asp?</u> <u>app=SelGuides&DCWS=Electronics&DCWSS=Patternable%2</u> <u>0Silicones%20for%20Electronics&Type=Selection%20Guide</u>