Statistical Analysis of Integrated Passive Delay Lines

Behnam Analui and Ali Hajimiri

California Institute of Technology, Pasadena, CA 91125

Email: behnam@caltech.edu

Abstract

Statistical properties of integrated passive LC delay lines are investigated. A new variation using spiral inductors and vertical parallel plate (VPP) capacitors is introduced whose delay is primarily determined by the lateral dimensions, resulting in very accurate and repeatable delays. An MIM-based version of this line is also fabricated for comparison. Additionally, LC delay-based oscillators are implemented to compare the variations in active and passive delay elements. Experimental data is obtained from measurement of 27 and 47 sites on two wafers from two different process runs, respectively. The measurements show 0.6% delay variations for VPP-based delay line compared to 1.0% for its MIM-based counterpart.

Introduction

Accurate timing is the underlying principal used in communication and computation systems. The timing accuracy directly affects the performance of these systems. Integrated delay elements are arguably one of the most critical building blocks whose accuracy and repeatability directly affect the timing accuracy of digital and mixed-mode systems. Various forms of active and passive delay elements have been used in different circuits and systems such as delay-based oscillators (*e.g.*, [1][3]), delay-locked loops (DLLs) (*e.g.*, [4]), digital-to-phase convertors (*e.g.*, [5]), and transversal filters and equalizers (*e.g.*, [6]).

As the frequency of these applications increases, the requirement on the absolute accuracy of the delay elements tightens. It is important to control the delay of these elements in the presence of variations in process parameters, supply voltage, and temperature to achieve higher yield and reliability for the specified performance. In systems using active non-linear (*e.g.*, digital) delay elements, this is usually done through a feedback system relating the delay accuracy to an external reference. While practical for many digital systems, applications such as transversal filters and equalizers (*e.g.*, [6]) require linear wideband delay elements not to introduce distortion on the signal. This can be achieved more readily by using integrated passive delay lines with practically no sensitivity to the supply voltage while maintaining a low sensitivity to process variations and temperature.

It has been shown [2] that using building blocks that depend only on the lateral dimensions, such as vertical parallel plate (VPP) capacitors, one can achieve a tighter tolerance and better matching across the chip, wafer, and process lots. This is primarily due to the inherently higher accuracy of the lithography and etching processes used to define the lateral dimensions of these components. Interestingly, the inductance of spiral inductors is primarily determined by its lateral dimensions, encouraging the design of passive LC delay lines using these lateral components. It eliminates the delay dependency on less accurate process steps such as deposition and planarization that control the vertical dimensions.

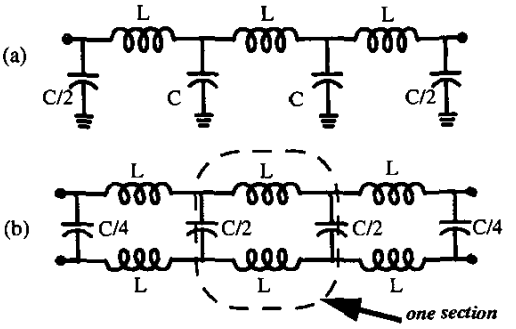

Fig. 1 Constant-k LC ladder structure with 3 stages: a) Single-ended b) Differential (termination is not shown)

This work presents the experimental results of a set of measurements and statistical analysis on fabricated passive delay lines and delay-based oscillators. It verifies low sensitivity of LC delay lines to process variations. In the rest of the paper, we review the theory of LC delay lines, and introduce our implementation of integrated LC delay lines. Then, we discuss the measurement setup and results.

LC Passive Delay Lines

There are several structures comprising inductors, L, and capacitors, C, that can be used as delay lines. Perhaps, the best known is Bessel-Thomson filter [7][8] that has maximally flat delay response. However, it is not suitable for integration since it results in delay values that are small for today's applications and also because its component values become unrealistic for integration, as the filter order increases.

Constant-k LC ladder structures on the other hand consist of identical interconnected inductors and capacitors in a ladder form, as shown in Fig. 1a. The ladder is a lumped approximation of transmission line and hence, can be used as a delay line. It can be shown that the delay of the structure is approximately:

$$T_D = n\sqrt{LC} \tag{1}$$

where n is the number of LC sections. Using spiral inductors and high density VPP [2] or MIM capacitors one can obtain large delay values. Using the image impedance techniques, one can easily calculate the impedance of the line to be:

$$Z(\omega) = \sqrt{\frac{L}{C}} \cdot \sqrt{1 - \frac{LC\omega^2}{4}} = Z_0 \cdot \sqrt{1 - \frac{LC\omega^2}{4}} \tag{2}$$

where $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the line [9]. As can be seen, the impedance becomes imaginary for frequencies above a critical frequency given by:

$$\omega_c = \frac{2}{\sqrt{LC}} \tag{3}$$

0-7803-7842-3/03/$17.00 © 2003 IEEE IEEE 2003 CUSTOM INTEGRATED CIRCUITS CONFERENCE

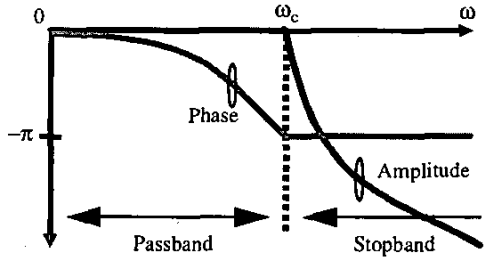

Fig. 2 Amplitude and phase characteristics of constant-k filter sections

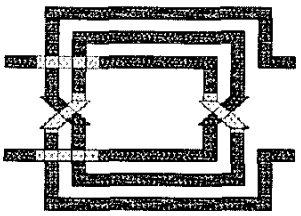

Fig. 3 Differential symmetric interwound inductors for one section of the delay line

The transmission characteristics of a line composed of ideal Ls and Cs is lossless upto the critical frequency defined in (3). Typical transmission amplitude and phase characteristics of a constant-k filter consisting of ideal Ls and Cs with proper termination is shown in Fig. 2. Notice that this *lossless* ladder structure is band limited.

While the attenuation is zero in the passband, at frequencies above ω_c the ladder will attenuate the input signal [9]. Moreover, in contrast to a continuous transmission line, the delay of an LC delay line is not constant over the entire passband [9]. Thus, the frequency dependent group delay over the desired range should be measured to fully characterize the line.

The LC delay line can be designed in a differential form as shown in Fig. 1b. In such circuits, the differential inductors can be interwound in order to benefit from mutual inductance of the two. Therefore, larger value inductances will be achievable with same (or even smaller) area/size. It can be shown that if two equal differential inductors with value L are interwound with mutual inductance of k (with proper sign), the effective inductance value for each will be $(1+k)L$. We have taken advantage of this fact in our implementation of the delay lines.

LC Delay Line Implementation

Two sets of LC delay lines are implemented in the form of differential constant-k filters in a 5-metal SiGe BiCMOS process in two different process runs. We will refer to these two process runs by PR1 and PR2. The differential inductors are implemented using coupled inductors and have 1.25 interwound turns in the top metal. Fig. 3 shows the symmetric layout of the inductors. Inductors are simulated using a 2.5D electromagnetic simulator over desired range of frequencies.

The first set of delay lines use MIM capacitors and consist of 24 LC sections in PR1. In the second set, the VPP capacitors are used instead of the MIMs. It has 19 LC

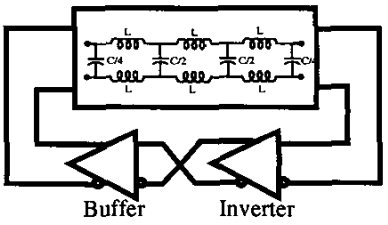

Fig. 4 Delay-based oscillator for testing passive delay lines

sections and was fabricated in PR2. Based on our earlier discussion, we expect this VPP-based delay line to show smaller delay variations compared to its MIM-based counterpart. In VPP capacitors, the distance of adjacent parallel plates of the capacitors are chosen to be larger than the minimum allowable spacing between adjacent metals to reduce the effect of lateral surface roughness on the capacitor value. The increased fringe capacitance is modelled accurately with electromagnetic simulations.

In addition to standalone passive delay structures, a delay-based oscillator is made in PR2 with 6 sections of similar LC delay lines (with MIM capacitors), as shown in Fig. 4. The buffer and the inverter are conventional ECL gates. Post-layout simulations taking various parasitic effects into account predict an oscillation frequency of 4.8 GHz. The oscillator core is isolated from the output by buffers desensitizing the frequency to the load and trace variations. TABLE 1 summarizes the parameters and simulation results of the delay lines.

TABLE 1 Summary of Delay Line Parameters

Delay Line Parameter	*Value*
Effective Inductance per section	0.58 nH
Total Capacitance per section	230 fF
Characteristic Impedance	50 Ω (100 Ω differential)
Total Simulated Passive Delay per section	11.5 ps
Ideal Critical Frequency ($\omega_c/2\pi$ from (3))	28 GHz

Experimental Results and Analysis

Standalone delay structures using MIMs and VPPs and the oscillators in PR2 are tested with direct on wafer probing. The results are summarized in the following sub-sections.

A. *Measurement Accuracy and Repeatability*

27 MIM-based delay lines in PR1 and 47 VPP-based delay lines in PR2 were characterized using an Agilent Technologies E8364A network analyzer. To ensure constant environmental conditions (including temperature and measurement setup variations) during the measurement of all 74 sites, a set of preliminary experiments were performed. Six random sites were selected as witness cases and were measured three times each at different times during the measurement. Then, the results for each site were compared. The observed variations were always less than 0.05% indicating the measurement error and the degree of its repeatability. This very high repeatability of results indicates minimum changes in the conditions of the experiments.

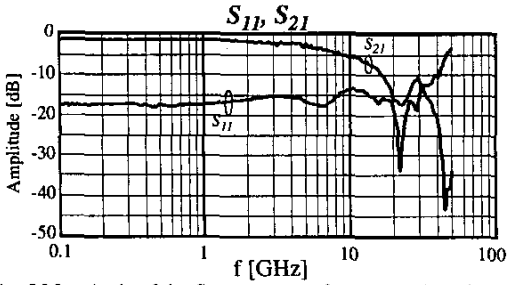

Fig. 5 Magnitude of the *S*-parameters of one MIM-based standalone delay line

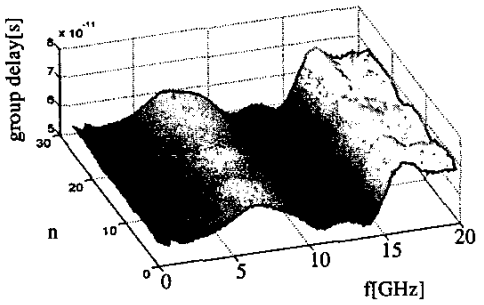

Fig. 6 Collective group delays of 27 standalone MIM-based delay lines

B. Standalone Delay Lines: S-parameters

Magnitude of S_{11} and S_{21} parameters of MIM-based and VPP-based delay lines were measured. A sample result for a MIM-based delay line, plotted in Fig. 5 shows S_{11} < -12dB (upto 30 GHz). Similar measurements for VPP-based delay lines show S_{11} < -16dB ($1.5GHz \leq f \leq 20GHz$). They indicate that the delay line characteristic impedances are very close to 50 Ω over that wide range of frequencies. The low frequency loss of MIM-based delay line is 1.2 dB and its 3-dB bandwidth is 7.5 GHz.

C. Standalone Delay Lines: Group Delay

The group delays of the whole ensemble for both MIM-based and VPP-based lines are plotted in Fig. 6 and Fig. 7, respectively. The dominant source of variations over different wafer sites for samples in MIM-based lines is the tolerance of MIM capacitors. The reported MIM tolerance in this process technology is $\pm 0.15fF/\mu m^2$. It translates to a total tolerance of ΔC=18.8 *fF* for the MIMs that we used. The time delay variations per section can be approximated from (1) as follows:

$$\Delta T_D = \frac{\partial T_D}{\partial C} \cdot \Delta C \tag{4}$$

$$\frac{\Delta T_D}{T_D} = \frac{1}{2} \cdot \frac{\Delta C}{C} = 0.04 \tag{5}$$

The normalized standard deviations of group delay (normalized to the mean group delay at corresponding frequency) for MIM-based and VPP-based lines are plotted in Fig. 8. The variations for MIM-based lines are within the tolerance of the MIM capacitors in (5). The delay lines with VPP capacitors are almost twice more accurate across most of the frequency range. This corresponds to a

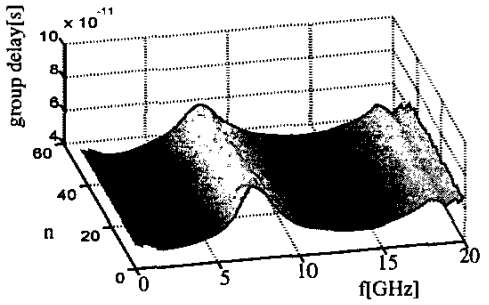

Fig. 7 Collective group delays of 47 standalone VPP-based delay lines

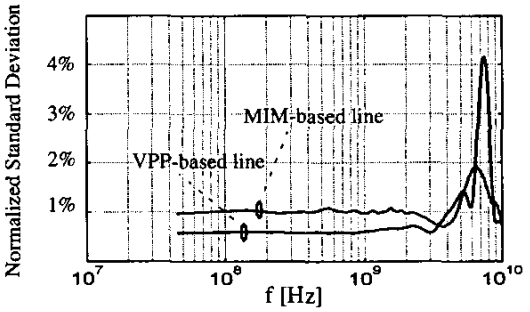

Fig. 8 Normalized standard deviations for group delays of standalone delay lines

factor of 3.3 improved tolerance for the VPPs in agreement with [2]. TABLE 2 compares the average low frequency group delays and the average normalized standard deviations of that in both cases. Again, it can be seen that the VPP-based delay lines are almost twice more accurate. Fig. 9 shows distribution of normalized delay at 1 GHz for both MIM- and VPP-based delay lines.

TABLE 2 Statistical comparison for MIM and VPP-based lines

Parameter	*Mean* (η)	*Standard Deviation* (σ)	σ/η
MIM *low freq. group delay*	56.7 ps	0.572 ps	1.01%
VPP *low freq. group delay*	52.14 ps	0.306 ps	0.59%

D. Delay-Based Oscillators

Adelay-based oscillator is fabricated similar to the one in Fig. 4. The measured frequency of the oscillator will be a direct indicative of the aggregate time delay of the passive delay line and cascaded active circuitry. An output buffer is added to drive 50 Ω load. Total of 47 sites are measured from two different wafers. The two wafers have received different emitter processes, one resulting in an improved emitter resistance. Therefore, the active elements in two sets are different.

The oscillation frequencies are measured with on wafer probing using HP 8563E spectrum analyzer and HP 53150A frequency counter. It is noteworthy that the frequency is recorded after each oscillator stabilizes. Stabilization time constant after start-up is measured to be around 30 secThe frequency mean and standard deviation

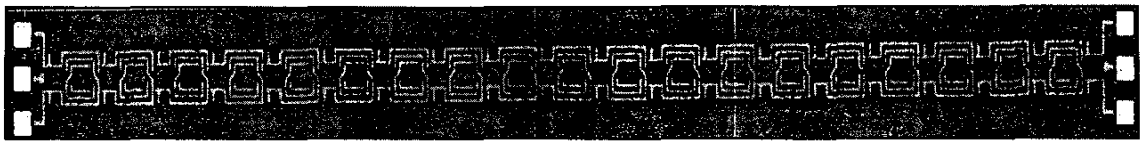

Fig. 10 Die photo of 19-section VPP-based LC delay line

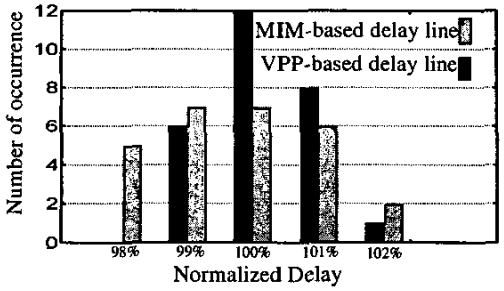

Fig. 9 Distributions of normalized delay at 1GHz for both MIM and VPP-based delay lines

are listed in TABLE 3. The measurement is in good agreement with the simulation results. Overall data shows 0.8% variability in center frequency with respect to mean. The mean time delay around the loop is 105.2 ps and its corresponding normalized standard deviation is 0.85%. The loop delay is calculated from half of the inverse of oscillation frequency for each oscillator.

TABLE 3 Statistical analysis of the oscillators

Parameter	*Mean (GHz)*	*Standard Deviation (MHz)*	*Normalized Standard Deviation*
Standard Process (23 chips)	4.762	44	0.924%
Enhanced Emitter Process (24 chips)	4.745	35.2	0.742%
Overall data (47 chips)	4.75	40	0.84%

.The die photo of the VPP-based line, MIM-based line and the oscillator are shown in Fig. 10-12, respectively. The passive delay lines are dominating the area. The spiral inductors are formed in a loop in the oscillator to avoid long interconnect lines. The capacitors are located in between the inductors. Inductor size is $150\mu m \times 150\mu m$ The total chip dimensions for the oscillator are $900\mu m \times 560\mu m$.

Conclusions

In this paper a set of experiments are performed to investigate the sensitivity of two different types of integrated LC delay lines to process variations. The component values of such integrated delay lines depends only on accuracy of lithography and etching processes in the case where VPP capacitors are used. Delay lines implemented using such LC structures are shown to be more accurate. The measurements based on 47 VPP-based delay line chips and 27 MIM-based delay line chips indicates twice as large variations in group delay for MIM-based delay lines. In summary, passive LC delay lines with VPP capacitors are best structures for implementing linear passive delay lines with low sensitivity to process variations and no sensitivity to supply variations.

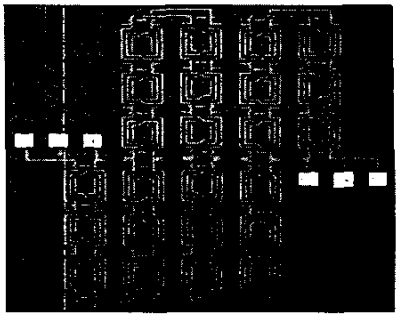

Fig. 11 Die photo of 24-section MIM-based LC delay line

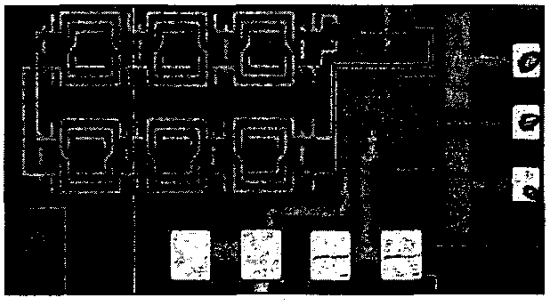

Fig. 12 Die Photo of the delay-based oscillator with 6-section differential LC delay line

Acknowledgments

The authors acknowledge M. Owrang for assistance in measurement and valuable feedbacks. They are also grateful to A. Komijani, S. Mandegaran, and J. Buckwalter from Caltech's CHIC group for useful discussions and helps. They thank Lee Center for Advanced Networking, IBM, and Agilent Technologies for supporting this project.

References

[1] H. Wu and A. Hajimiri, "Silicon-Based Distributed Voltage Controlled Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 493-502, March 2001.

[2] R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 384-393, March 2002.

[3] J. E. Rogers and J. R. Long, "A 10-GB/s CDR/DEMUX with LC Delay Line VCO in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 37, no.12, pp. 1781-1789, Dec. 2002.

[4] T. H. Lee and J. F. Bulzacchelli, "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1736-1746, Dec. 1992.

[5] J-M Chou, Y-T Hsieh, and J-T Wu, "A 125 MHz 8b Digital-to-Phase Converter," *Digest of Int'l Solid-State Circuits Conf. ISSCC'03*, vol. 46, pp. 436-437, Feb. 2003.

[6] H. Wu, et. al., "Differential 4-tap and 7-tap Transverse Filters in SiGe for 10Gb/s Multimode Fiber Optic Link Equalization," *Digest of Int'l Solid-State Circuits Conf. ISSCC'03*, vol. 46, pp. 180-181, Feb. 2003.

[7] W. E. Thomson, "Delay Networks having Maximally Flat Frequency Characteristics," *Proc. IEE*, pt. 3, vol. 96, pp.487-490, 1949.

[8] G. C. Temes and J. W. LaPatra, *Circuit Synthesis and Design*, New York: McGraw-Hill book company, 1977.

[9] D.M. Pozar, *Microwave Engineering*, 2nd ed., New York: John Wiley & Sons, 1998.