Electron-beam-induced current measurements in silicon-on-insulator films prepared by zone-melting recrystallization

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Enhanced diffusion of arsenic along grain boundaries and subboundaries in zone-recrystallized silicon-on-insulator films has been measured by electron-beam-induced current analysis of lateral *pn* junctions fabricated in the films. A four-hour diffusion at 1100 °C resulted in protrusions of arsenic at the junction edges which measured approximately 3–5 μm along the grain boundaries and only 1–2 μm along the subboundaries. The results suggest that under more ordinary thermal processing conditions, field-effect transistors with channel lengths greater than about 1.5 μm can be randomly positioned with respect to the more numerous subboundaries, but grain boundaries should be avoided.

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Zone-melting recrystallization by means of a movable-strip heat source can produce continuous device-worthy silicon films over thermally oxidized silicon when a suitable encapsulation layer is present to prevent silicon agglomeration.[1–5] The films consist of large grains, typically 1 mm wide and extending the length of the zone scan, which are seeded from a transition region where solidification begins.[2,5] Individual grains contain subboundaries, typically 25 μm apart, which are generally parallel to one another and to the direction of motion of the molten zone. The subboundaries consist of linear arrays of dislocations with angular deviations of the order of one degree or less; they originate at the interior corner of the solid-liquid interface during recrystallization.[5,6] Large-angle grain boundaries can be eliminated by seeding from the silicon substrate beneath the silicon dioxide layer[7,8] or by appropriate patterning of the silicon film prior to recrystallization.[9] The subboundaries are more difficult to control; however, entrainment techniques which force the subboundaries to be positioned at specific regular intervals have been reported.[6]

In a previous letter,[10] the electrical characteristics of both grain boundaries and subboundaries were examined by fabricating large (92×375 μm), phosphorus-doped (1×10^{17} cm^{-3}) resistors which were either parallel or perpendicular to the line defects. One or more transversely oriented grain boundaries provided significant ($\sim15\%$) bulk conductivity degradation; whereas, an average of 20 subboundaries provided only marginal ($\sim0.15\%$) bulk conductivity degradation. The surface conductivity at the interface between the silicon film which contained the resistors and the silicon dioxide below could be modulated by using the silicon substrate as a gate electrode. Transversely oriented grain boundaries induced peculiar "kinks" in the turn-on characteristics of these "upside-down" depletion-mode field-effect transistors. The influence of subboundaries on surface conductivity could not be detected. These results suggest that grain boundaries must be avoided when considering the placement of field-effect transistors on zone-recrystallized silicon-on-insulator films and that the degradation of electrical properties due to subboundaries can be ignored.

As the dimensions of field-effect transistors fabricated on zone-recrystallized silicon-on-insulator films are reduced, another potential problem arises, i.e., the enhanced diffusion of dopant impurities during high-temperature processing along line defects which form a connective path between source and drain. This phenomenon shortens the effective channel length of the transistor and ultimately leads to an abrupt increase in subthreshold leakage current. Enhanced diffusion of arsenic along grain boundaries in laser-recrystallized silicon-on-insulator films was shown to be significant when channel lengths are less than 3 μm, given a source-drain anneal at 900 °C for 90 min.[11]

In an earlier study,[12] enhanced diffusion of arsenic along grain boundaries in the vicinity of lateral *pn* junctions fabricated in laser-recrystallized silicon films was measured by electron-beam-induced current (EBIC) analysis, and the results were compared with scanning-electron-beam voltage-induced contrast as a check for measurement consistency. A five-hour arsenic diffusion at 1000 °C resulted in protrusions of arsenic at the junction edges extending up to 5 μm along the grain boundaries. The different lengths of the protrusions suggested significant variations in the microstructures or diffusivities of the grain boundaries.

This letter presents the results of EBIC analysis of lateral *pn* junctions fabricated in zone-recrystallized silicon-on-insulator films. In recognition of the electrical and crystallographic differences between grain boundaries and subboundaries, particular effort has been made to compare the enhanced diffusion along the two types of line defect. Earlier work suggested a difference in diffusion characteristics,[13] but the measurements were by a less accurate procedure in which the arsenic-rich regions of the lateral *pn* junctions were preferentially etched. If minimal diffusion along subboundaries could be demonstrated, it would further justify the random placement of devices with respect to the

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subboundaries, thereby simplifying the processing requirements associated with zone-recrystallized silicon-on-insulator films.

Prior to recrystallization, samples were prepared by oxidizing (100) n-type silicon wafers at 1100 °C to obtain a silicon dioxide thickness of 0.5 μm. The thermal oxide was sequentially coated with a 0.5-μm-thick layer of low pressure chemical vapor deposition (LPCVD) polycrystalline silicon, a 2.0-μm-thick layer of CVD silicon dioxide, and a 0.03-μm-thick layer of sputtered silicon nitride. The details of the zone-melting recrystallization procedure have been reported elsewhere.[1-5] Briefly, the sample was placed within an argon ambient on a graphite strip which was resistively heated to 1000 °C. A movable upper strip, approximately 1 mm above the sample and 1 mm wide, was resistively heated until the polycrystalline silicon film melted, and the molten zone was moved across the sample at a speed of approximately 1 mm/s. After recrystallization, the silicon dioxide and silicon nitride encapsulation layers were removed in concentrated hydrofluoric acid. The silicon film was implanted with a fluence of 2×10^{12} cm^{-2} boron at 70 keV. The boron was uniformly redistributed throughout the silicon film at a later point in the process sequence to yield a concentration of 4×10^{16} cm^{-3}.

In order to distinguish the subboundaries from the grain boundaries, the films were decorated by a regular matrix of anisotropically etched pits.[14] These were prepared by depositing a 0.4-μm-thick layer of CVD silicon dioxide over the silicon film and then etching 5-μm-diam holes on 50-μm center spacing. The exposed silicon was etched in a potassium hydroxide solution until square pits revealed the local crystallographic orientations throughout the film. As in other experiments,[1-5] the texture of the film was (100).

The fabrication of lateral pn diodes began with the opening of large (up to 2×2 mm) holes in the silicon dioxide which had been used to define the matrix of etch pits. The holes defined the diode emitter (n^+) regions and were implanted with a fluence of 1×10^{15} cm^{-2} arsenic at 150 keV. The implant was annealed at 1100 °C for 10 min in dry oxygen to form a thin silicon dioxide cap and then for 4 h in dry nitrogen to exacerbate the degree of enhanced diffusion which was expected along the grain boundaries. The silicon dioxide over the diode emitter regions was removed following the anneal. Aluminum was deposited over the sample and then defined to form contact pads which were slightly recessed from the junction edges. The fabrication process concluded by etching the silicon dioxide which remained over the silicon film.

After processing, the samples were mounted on headers and aluminum wires were bonded to the diode n^+ contact pads. There was no direct electrical contact available to the diode p regions (field); the diodes were connected back-to-back in pairs without an applied bias voltage. A JSM-50 (Japanese Electron Optics Limited) scanning electron microscope was used for the EBIC analysis. With a 5-keV electron beam, the EBIC resolution was presumed to be consistent with that established in Ref. 12, approximately 0.5 μm.

Many grain boundaries were located near the transition region of the zone-recrystallized film. A typical EBIC image

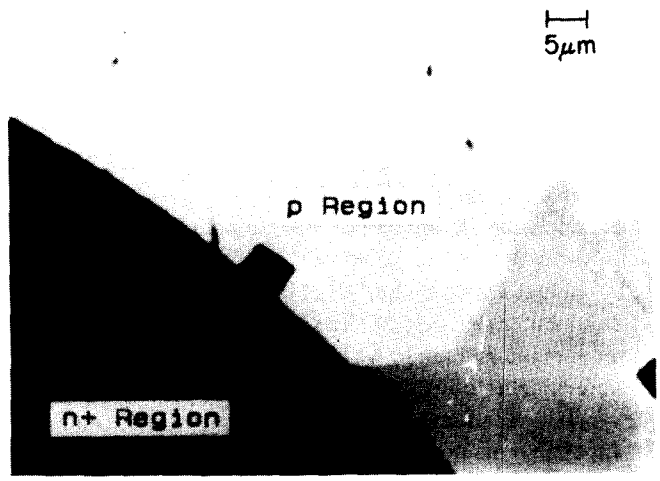

FIG. 1. EBIC image in the vicinity of a lateral pn junction which is intersected by grain boundaries. The large dark square which extends from the diode n^+ region is an anisotropically etched pit used to determine grain orientations in the recrystallized silicon film. A second dark square at the right indicates that a grain boundary is located between the two squares, and the misorientation of the squares indicates that the angle of the grain boundary is approximately 20°. Note the large protrusions where the grain boundaries intersect the junction edge.

from this region is shown in Fig. 1. The arsenic protrusions extend approximately 3–5 μm from the edge of the lateral pn junction. A protrusion length is assumed to be roughly equal to a diffusion length $(Dt)^{1/2}$, where D is the coefficient of line

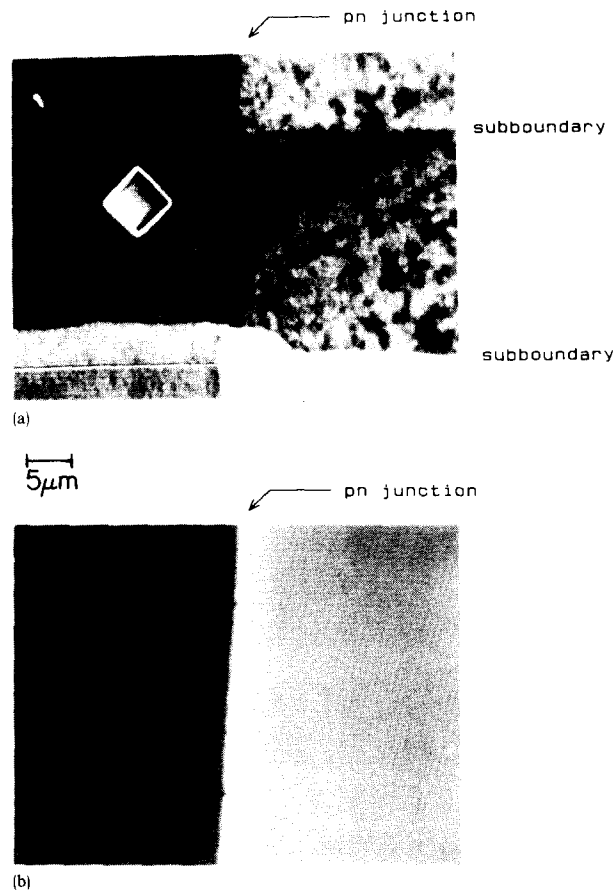

FIG. 2. (a) Secondary electron image in the vicintiy of a lateral pn junction which is intersected by subboundaries. The distinct contrast is due to preferential electron channeling. (b) Corresponding EBIC image. Note the small protrusions along the subboundaries.

defect diffusion and t is the diffusion time. From this relation, the coefficient for arsenic diffusion along a grain boundary at 1100 °C is about 1×10^{-11} cm^2/s. The value which was estimated in Ref. 12 for the case of arsenic diffusion at 1000 °C was also about 1×10^{-11} cm^2/s. If the enhanced diffusion which brings about the transistor failure mode of Ref. 11 is assumed to correspond to a diffusion length of 1.5 μm for an arsenic diffusion time of 90 min at 900 °C, the estimated coefficient of grain boundary diffusion for this case is approximately 4×10^{-12} cm^2/s. Since these particular estimates vary as the square of a diffusion length and yet are comparable to within a factor of 2, the degree of enhanced arsenic diffusion along grain boundaries appears to be weakly dependent upon temperature over the range of 900–1100 °C. This conclusion is not consistent with that of earlier work[15] in which the enhanced diffusion of arsenic along grain boundaries in laser-recrystallized silicon-on-insulator films suggested a thermal activation energy of about 2.3 eV.

The EBIC analysis in the vicinity of subboundaries suggests a lesser degree of enhanced arsenic diffusion. Figure 2(a) shows two subboundaries separating regions of distinctly different contrast. The contrast results from preferential electron channeling along certain crystalline orientations.[5] The corresponding EBIC image of Fig. 2(b) shows small protrusions at the subboundary locations which extend approximately 1 μm beyond the lateral *pn* junction edge. The protrusion lengths were sometimes greater along other subboundaries within the sample, but in no case did a protrusion extend more than about 2 μm. For a nominal protrusion length of 1.5 μm, the estimated coefficient of arsenic diffusion along subboundaries has the approximate value of 1×10^{-12} cm^2/s, roughly one order of magnitude less than for the grain boundaries. Under more ordinary processing conditions, the subboundary diffusion length scales downward by a factor of 2 as the diffusion time is reduced to one hour, and some degree of scaling can be expected as the diffusion temperature is reduced. These results suggest that field-effect transistors can be randomly positioned with respect to the subboundaries provided that channel lengths are greater than about 1.5 μm.

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