Microelectronic Packaging for Retinal Prostheses

A high-density, chip-level integrated interconnect packaging system

BY DAMIEN C. RODGER AND YU-CHONG TAI

The retinal prosthesis initiative at the Biomimetic Microelectronic Systems (BMES) center, an National Science Foundation (NSF) Engineering Research Center (ERC) at the University of Southern California (USC), the California Institute of Technology (Caltech), and the University of California, Santa Cruz, calls for a novel set of packaging technologies for bioimplant device construction. The testbed requires high-resolution electrical stimulation of the remaining functional neurons of the macula and a mechanically and electrically robust method for interconnecting application-specific integrated circuits (ASICs) with the interfacial electrodes. Our epiretinal prosthesis comprises a video-capture and data-encoding mechanism, a radio-frequency (RF) coil system for power and data transmission and recovery, an analog/digital ASIC with driving electronics, and a flexible retinotopic electrode array for neural stimulation, all in a chronically implantable, hermetically sealed package. Here, we discuss an innovative parylene-based high-density chip-level integrated interconnect (CL-I^2) packaging system for retinal implants.

Development of a new technology for packaging of the intraocular components of the electrical retinal prosthesis system is of paramount importance for the testbed's efforts. The need for such a technology stems from several underlying elements of the prosthetic device. First, as with any chronic implant, biocompatibility of the implanted materials, especially of those in direct contact with the patient's tissues and fluids, must be ensured. The long-term efficacy of the device must also be guaranteed because revision surgeries are not tolerable; moisture must not penetrate the package over a period of decades. To ease implantation, the entire packaged system must be flexible enough to be threaded through a small surgical incision.

Of particular importance for the retinal prosthesis is the high lead count necessary to achieve truly useful vision. The overall goal for the testbed by the end of the ERC's tenure is to complete a 1,000-electrode system, far more than the 16-electrode device currently in use [1]. Because of the complexity of the driver circuitry necessary for such high lead-count devices, these circuits, typically, must be fabricated at a foundry. The cost involved in obtaining an undiced wafer from the foundry is impractically high and, as a result, individual chips are ordered from the foundry. As yet, there is no cost-effective method for high-density and scalable interconnection of a foundry-fabricated driving integrated circuit (IC) with the RF coil and retinal stimulator.

Current flexible packaging paradigms described in the literature can accommodate center-to-center pad distances on the driving microchip on the scale of 80–100 μm or more. For a 32×32 array, this would limit the minimum size of the chip (assuming a square arrangement of pads) to approximately 3.2×3.2 mm^2. While this chip size is tolerable, it is clear that such an arrangement of output pads, while desirable, is all but impossible (output pads are typically grouped spatially and account for a small percentage of total chip area), and the width of the incision necessary to implant the chip increases as chip size increases. Furthermore, these kinds of interconnection and packaging schemes are usually carried out by a skilled technician who tediously creates interconnects one by one (as per wire-bonding), which, for a 1,000-electrode device, is impractical. The need exists for a simplified interconnection and packaging scheme that, while increasing the resolution of interconnection with the driving circuitry beyond current limits, is fully mass-producible and formed almost entirely of biocompatible, flexible materials. A packaging technology that enables fabrication and assembly of a monolithic intraocular system in a single process is also a highly desirable goal for a retinal prosthesis since it maximizes yield. A technology that promises to meet these requirements has been realized in the first year of the ERC.

It should be mentioned that several alternative approaches to retinal stimulation have been proposed. Most of these use the electrical stimulation paradigm [1]–[4]. Some recent work has been undertaken involving a microfluidic approach, where targeted neurotransmitter delivery to the neurons downstream from the nonfunctional photoreceptors is the end goal [5]. Such a microfluidic approach benefits from avoiding the use of a potentially harmful electrical stimulus that can damage the delicate retinal tissue, and it presents the possibility of enabling selective activation at target synapses through controlled release of different neurotransmitters. There are several drawbacks to these neurotransmitter-based prosthetics, however. Perhaps the most obvious drawback is the difficulty of renewing the neurotransmitter supply in a fully implanted system.

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Furthermore, the glutamate proposed as a likely neurotransmitter in these prostheses is both acutely and chronically neurotoxic [6], requiring a very tightly controlled delivery system. Moreover, the fabrication of such a high-density microfluidic delivery device in a biocompatible package is formidable, and the electrical circuitry required is more complicated than for an electrical stimulation device, while still calling for a flexible, high-density interconnection scheme. Indeed, our technology is not specific to electrical prostheses and can be tailored for use in microfluidic as well as other types of systems.

The CL-I^2 Packaging

In order to break the current resolution barrier, we have developed the new CL-I^2 technology for integrating individual prefabricated chips comprising driving electronics and discrete components into a flexible parylene substrate with high-density electrical interconnection. Parylene is a United States Pharmacopoeia (USP) Class VI biocompatible polymer that is deposited through a highly conformal vapor deposition process. Of the three most common parylenes (Figure 1), parylene C is the most widely used in industry. The advantages of the use of parylene include its proven biocompatibility [7], its strength and flexibility (Young's modulus $\approx$ 4 GPa), its conformal pinhole-free room-temperature deposition, its low dielectric constant ($\approx$ 3) and high volume resistivity ($> 10^{16}\Omega$-cm) [8], its transparency, and its ease of manipulation using standard microfabrication techniques such as reactive ion etching (RIE) [9]. Several research groups use parylene C deposition as a method of creating a biocompatible, water-blocking seal around electrode arrays, typically fabricated using a polyimide substrate [4], [10]. This is necessary because most polyimides have a moisture absorption that is more than an order of magnitude higher than that of parylene C [11], [12]. Some specialized polyimide films have lower moisture absorption, but they require high-temperature curing steps that are generally not post-IC compatible, and their use in permanent medical implants is not permitted [13].

Driven by the success of prior parylene skin and IC integration work in our group [14], [15], our effort focuses on using parylene as the main substrate for the entire prosthesis, minimizing the number of potential failure modes caused by the use of multiple materials, and taking full advantage of the biocompatible and mechanical properties of the material. This innovative use of parylene as the substrate rather than as a coating material also enables simultaneous fabrication of various system components, dramatically simplifying the packaging of the implant. For example, a 16×16 multielectrode array of parylene-embedded 125-μm-diameter planar platinum electrodes (Figure 2) has already been fabricated, and pulse testing and accelerated-lifetime saline soak testing have

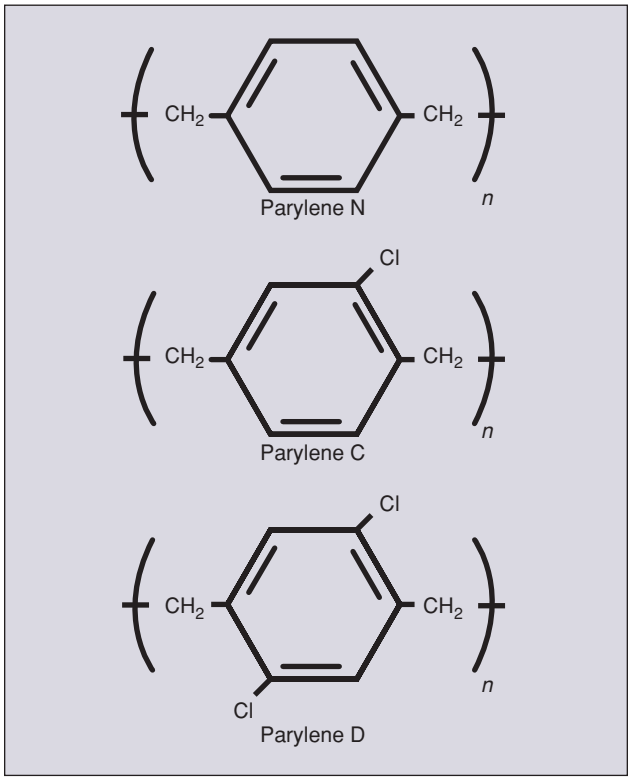

Fig. 1. Chemical structures of the three most commonly employed parylenes. Parylene C was selected for this application because of its mechanical strength, biocompatibility, and low moisture permeability.

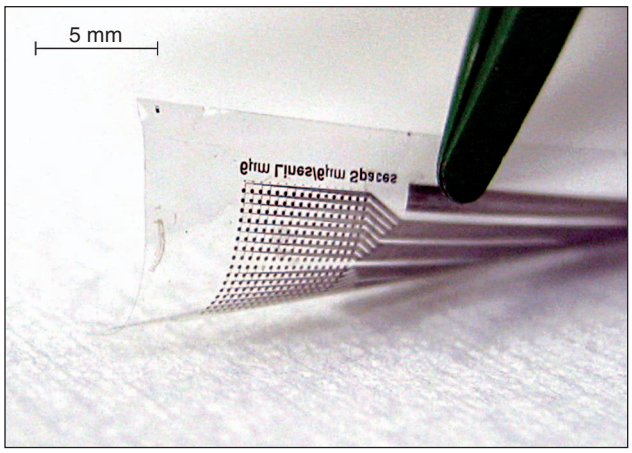

Fig. 2. Parylene-based multielectrode array consisting of 256 thin-film platinum electrodes. The electrodes are 125 μm in diameter, and the traces have a pitch of 12 μm.

The parylene skin with the simulated IC chip embedded is extremely flexible, a feature that facilitates implantation.

demonstrated its potential as a retinal stimulator. A multilayer RF coil using parylene as a substrate is under development, with fabrication alongside the electrode array being possible. For these components to be functional, however, they must be easily integrated with the driving circuitry.

Our method for packaging and interconnection involves inserting the foundry-fabricated ASIC directly into the fabrication process of the retinal stimulator and RF coil as though the circuitry had originally been manufactured in the host wafer on which these other parylene-based components are fabricated. It is a process superficially similar to one proposed during the development of multichip modules in the 1990s [16], [17], but it was conceived independently and is entirely tailored to the retinal testbed's needs of flexibility, biocompatibility, and scalable, photolithography-defined lead density. Figure 3 illustrates this concept, where the prefabricated standalone IC chip is shown directly integrated with the retinal stimulator, shown at the top-right of the figure (the pads to the bottom-left are used for testing, but in the final system would be replaced with the RF coil). A cutaway view of the same is shown in Figure 4, depicting the chip underlying the flexible parylene skin.

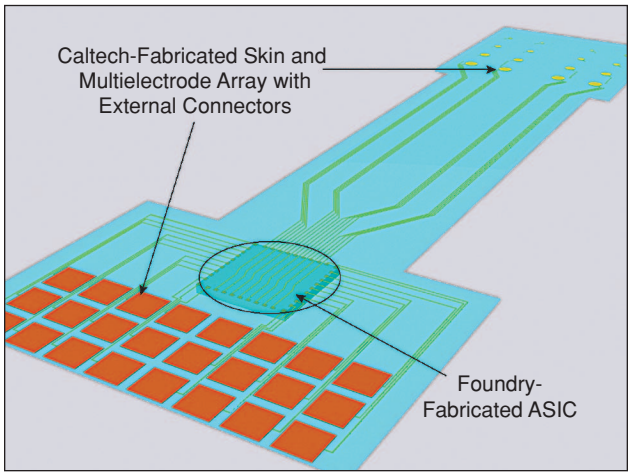

Fig. 3. An illustration of the CL-I^2 package concept. The prefabricated ASIC has been directly inserted into the fabrication process of the overlying parylene skin.

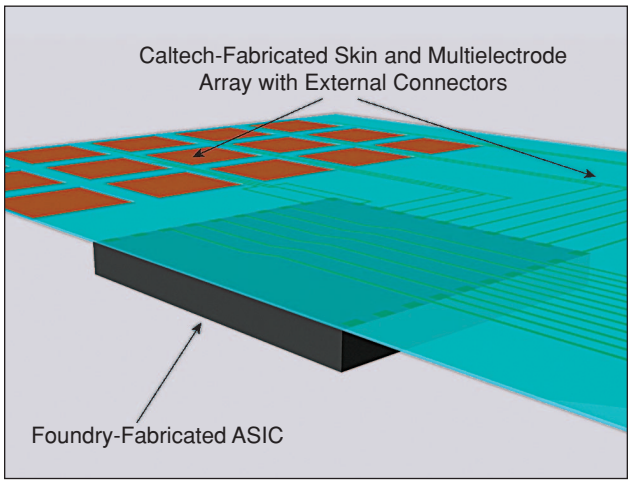

Fig. 4. A cutaway view of the CL-I^2 package concept. The chip can be coated with parylene a priori so that the entire system is protected by parylene.

Chips fabricated to simulate MOS Implementation System (MOSIS) IC chips were used to demonstrate our technology. The only properties of these prefabricated chips that had to be known a priori were the electrical pad dimensions and locations, as well as the overall length, width, and thickness of the chips. The simulated chips, consisting of simple electrical shorts and intrinsic through-die resistors, were embedded in a standard silicon wafer using backside mechanical anchoring with parylene. The entire wafer then underwent standard processing as though the circuitry had been prefabricated in the wafer itself, with electrical connections to remote pads far from the chips being demonstrated.

Fabrication

Figure 5 shows the chip integration and interconnection method in terms of an abridged process flow. Briefly, photoresist is spun on a standard 550-μm-thick silicon wafer. Then, $2.51 \times 2.63\,\text{mm}^2$ through-holes are patterned in the photoresist after alignment and etched using the Bosch process in a PlasmaTherm SLR-770B system (Unaxis Corporation, St. Petersburg, FL). The width of these holes ensures accurate chip alignment to within built-in tolerances. The 260-μm-thick chips (many different thicknesses can be accommodated) are inserted from the backside and planarized using Nitto tape on the front of the wafer. They are horizontally self-aligned in these holes to within 10 μm of lateral displacement. The chips are then sealed on the backside with photoresist and mechanically anchored with a parylene deposition using a PDS2010 system (Specialty Coating Systems, Indianapolis, Indiana). After removal of the tape, fabrication is then carried out on this wafer as though it were a whole wafer with integrated circuitry. A sacrificial photoresist layer is patterned, and parylene is deposited on the frontside and patterned using an oxygen RIE to open contact holes to the chip pads. An e-beam evaporation process (SE600 RAP, CHA Industries, Fremont, California) is used to deposit 200–500 nm of metal with optimized step coverage. The deposit is patterned using the liftoff technique or chemical etching and standard photolithography. A second layer of

The CL-I² technology for the retinal prosthesis packaging effort obviates the need for a technician to create electrical and mechanical connections one by one.

parylene is deposited to sandwich the metal contacts and traces and patterned as before to expose the contacts/electrodes. The total thickness of parylene in our prototype was approximately 13 μm, but it can be anywhere from 5 – 20 μm or more, depending on the specific implementation. The sacrificial photoresist layer is then removed, leaving a flexible skin with embedded circuitry. Because the IC chip can be conformally coated with parylene before the entire fabrication process is started and patterned, during the initial parylene etch step to open the chip contacts (Step 2 in Figure 5), the end result can be a stimulation system that is completely enclosed in parylene, where parylene's pinhole-free coating would protect it from the surrounding biofluids after implantation. If the need arises, other coatings, such as metals, can be deposited on or within the entire structure to increase hermeticity and device longevity.

Results

Figure 6 shows an overhead view of the parylene skin with the simulated IC chip embedded in this manner and demonstrates the system's size relative to a penny (seen through the transparent parylene). Figure 7 shows the underside of the same device. As can be clearly seen from this picture, the entire system is extremely flexible, a feature that facilitates implantation. Additionally, because parylene is the bulk substrate, the system is also mechanically robust. Figure 8 shows a magnified view of the interconnects (patterned using photolithography) from the remote pads to the perimeter pads on the chip. Electrical testing verified that electrical contact to the chip had been made and that the circuits on the chip were functioning as expected. For example, the circuit between Remote Pads 1 and 8 (seen in Figure 6), which are connected through the similarly labeled traces

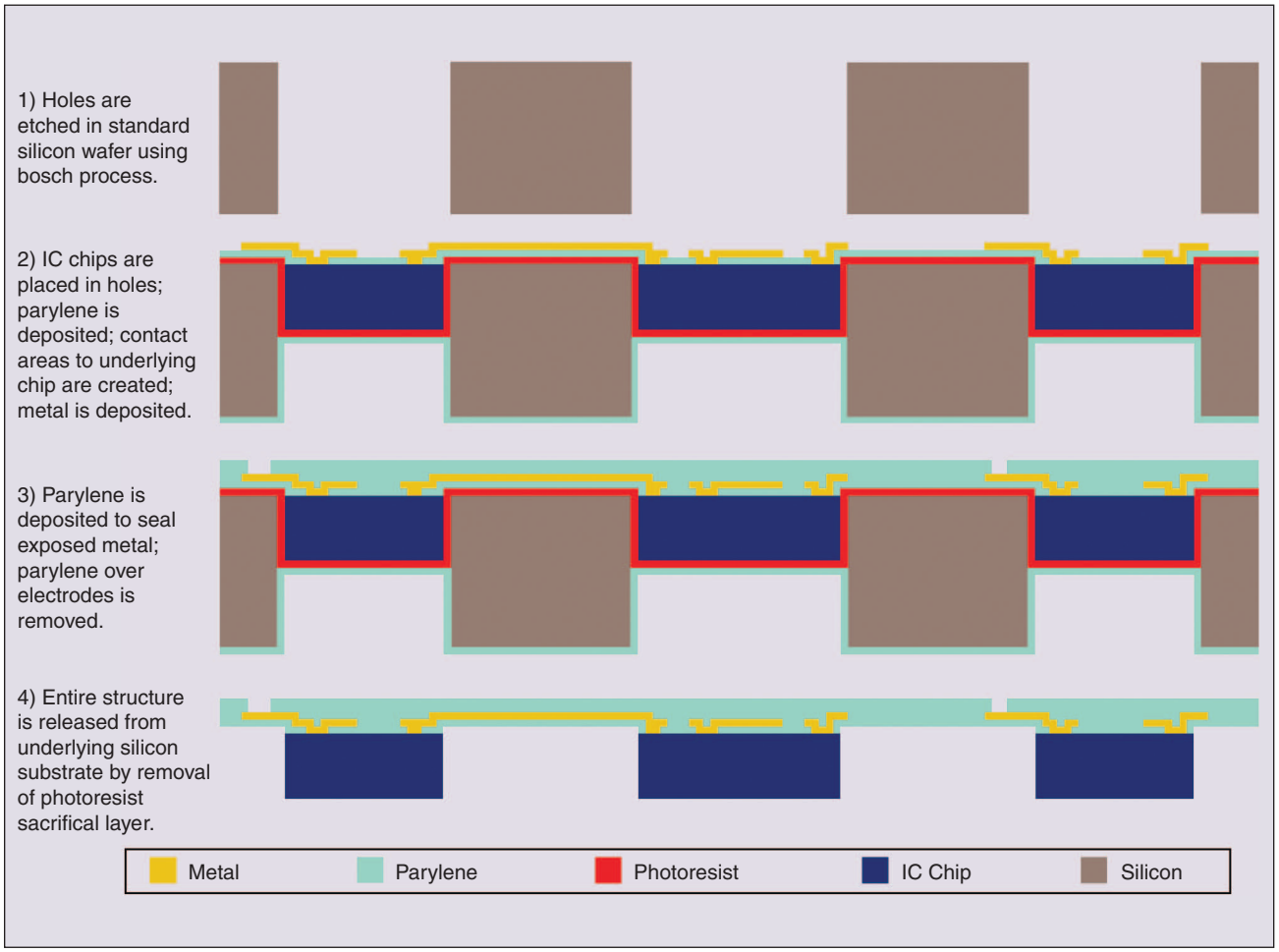

Fig. 5. An abridged process flow for the chip integration process.

to the corresponding pads on the chip (seen clearly in Figure 8), is ohmic with a resistance of 61.0 Ω. Between Remote Pads 1 or 8 and 2, the expected Schottky contact is observed, corresponding to the metallized lines connected through the doped intrinsic silicon of the die. These data indicate that this electrical interconnection and packaging scheme was successful. The contact pads in this demonstration were approximately $70-100 \times 100\,\mu m^2$, with a center-to-center pad spacing of 200 μm to simulate a real MOSIS chip, but these pads can now be scaled down in size by approximately an order of magnitude and placed in nonperimeter locations at a high density as a result of the successful demonstration of our technology.

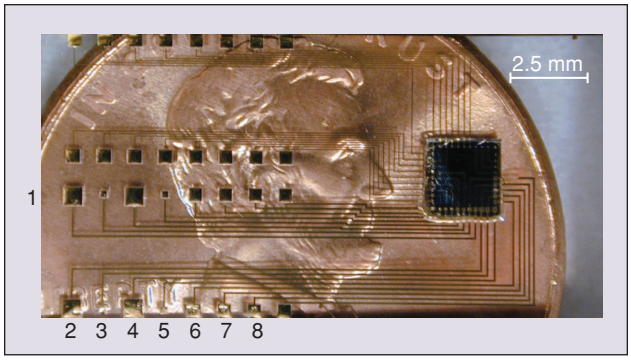

Fig. 6. An overhead view of a parylene skin with an embedded chip. Traces within the parylene connect the numbered remote contact pads on the left to the chip on the right.

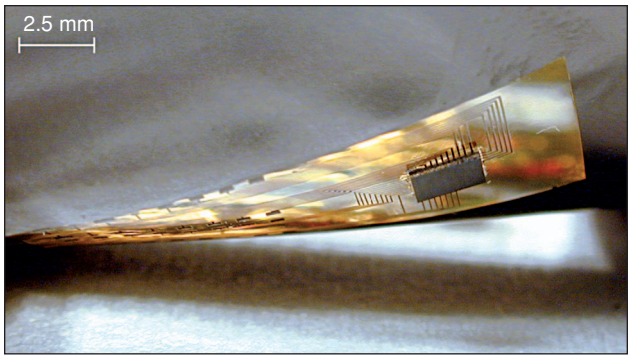

Fig. 7. An underside view of a parylene skin with an embedded chip. Because the entire system is parylene based, permeability to biofluids is minimal.

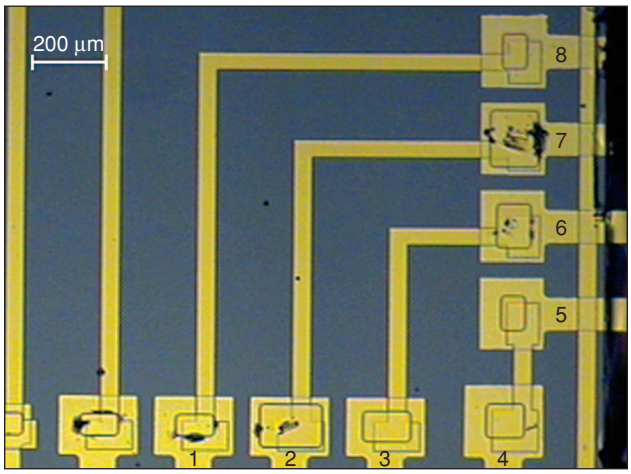

Fig. 8. A magnified view of the remote pad to chip interconnects. Numbered traces connect to the numbered remote pads shown in Figure 6.

This package has been designed to take full advantage of parylene's superior properties when compared with other polymeric materials. Accelerated-lifetime saline soak tests, pulse tests, and mechanical tests are underway to completely study the reliability of this packaging scheme. Although preliminary results are encouraging, because of the novelty of this technology, it is too early to determine exactly how well this package will function when chronically implanted.

Discussion

The implications of this CL-I^2 technology for the retinal prosthesis packaging effort are far-reaching. As opposed to current paradigms for flexible packaging, this technology obviates the need for a technician to create electrical and mechanical connections one by one. Instead, the technology is limited only by standard photolithography and standard microfabrication techniques, providing the capability for a reduction of an order of magnitude or more in the center-to-center pad distances that can be accommodated in the process. High-density electrode arrays are thereby feasible, because the fabrication process places no limit on the number of output pads that can reasonably be connected to the array.

In addition to being physically flexible, this package also adds flexibility to the development of circuit components, since individual chips can now be interconnected postfabrication and directly integrated with the stimulating electrode array. For example, one team can work on a 256-electrode driver chip, and another can work on the design of a multiplexer chip for driver chip addressing. In addition to the possible fabrication of a 256-electrode array for testing, the multiplexer can be interconnected with four of these driver chips to create a 1,024-electrode driver circuit without the need for a complete overhaul of the design and expensive fabrication of an entirely new chip. Discrete components such as chip capacitors can also be interconnected with the driver chip, electrode array, and RF coil in this manner. This may also prove useful because, as electrode density increases, so too does the size of the driver chip; if a large chip can be broken down into several individual component chips, these components can be integrated into a flexible skin, folded on top of each other for insertion into the eye through a small incision, and subsequently unfolded, thus facilitating surgery.

The cost-effectiveness of this packaging technology when compared with alternative methods should be stressed. For example, when a wafer is designated for IC processing with direct microelectromechanical systems (MEMS) integration, real estate on the wafer must be reserved for the MEMS device during IC fabrication. This is inherently a costly practice, since IC fabrication is most economical and high-yield when as many die as possible are fabricated simultaneously on a wafer. When certain areas on a wafer are earmarked for MEMS fabrication, valuable space is essentially wasted during the IC fabrication step. Using our technology, a full wafer can be used for IC fabrication. The wafer can then be diced and the individual functional chips

inserted into another standard wafer and directly integrated with the corresponding MEMS device in a photolithography-limited manner in such a way that, from a practical standpoint, it is as though the IC had been fabricated in this host wafer. Thus, when compared with full-wafer IC processing and MEMS integration [15], our process is more cost-effective, both for research purposes and for mass production.

This high lead-count package solves the problem of interconnection of the microelectronic components of high-resolution retinal prostheses. Its real strength lies in the pad sizes and line-widths it can accommodate, as all features are defined using standard photolithography and standard microfabrication techniques, making the technology fully scalable to the limits of the equipment used for fabrication. The resulting package is flexible, which facilitates implantation, and permeability to moisture is minimized through the use of parylene, a significant advantage over packages fabricated using other polymers. This cost-effective and biocompatible technology, when compared to other packaging techniques in other embodiments of retinal prostheses, promises to open the door to high-density biomimetic systems that are capable of transducing visual data with a resolution more akin to that provided by healthy photoreceptors.

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Damien C. Rodger received the B.S. degree in electrical engineering (magna cum laude) from Cornell University, Ithaca, New York, in 2000. His microelectromechanical systems (MEMS) research while at Cornell concentrated on SCREAM-fabricated microwave transmission lines and continuous phase shifters, conducted under Dr. Noel MacDonald, and on biomotor-driven microdevices as a W.M. Keck Foundation Fellow in Nanobiotechnology under Dr. Carlo Montemagno. He also worked in the MEMS group at the NASA Jet Propulsion Laboratory on the Coriolis force vibratory microgyroscope, under Dr. Tony Tang and Dr. William Tang. He is currently an M.D./Ph.D. candidate at the Keck School of Medicine of the University of Southern California, Los Angeles, California, and the California Institute of Technology (Caltech), Pasadena, California, conducting research in bioengineering under Dr. Yu-Chong Tai and Dr. Mark Humayun in the area of bioMEMS for ophthalmic use. He holds a Whitaker Foundation Graduate Fellowship in biomedical engineering, and is copresident of the Biomimetic Microelectronics Student Association (BMESA).

Yu-Chong Tai received his B.S. degree from National Taiwan University, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley. After Berkeley, he joined the faculty of electrical engineering at the California Institute of Technology (Caltech) and built the Caltech microelectromechanical systems (MEMS) lab. Not long ago, he joined the bioengineering department, and he is currently a professor of electrical engineering and bioengineering at Caltech. His current research interests include flexible MEMS, bioMEMS, MEMS for retinal implants, parylene-based integrated microfluidics, neuroprobes/neurochips, and high-performance liquid chromatography-based (HPLC-based) labs-on-a-chip. He has received several awards such as the IBM Fellowship, the Best Thesis Award, the Presidential Young Investigator (PYI) Award and the David and Lucile Packard Fellowship. He cochaired the 2002 IEEE MEMS Conference in Las Vegas. He is currently a subject editor of the *Journal of Microelectromechanical Systems.*

Address for Correspondence: Damien C. Rodger, California Institute of Technology, 1200 E. California Blvd., M/C 136-93, Pasadena, CA 91125 USA. Phone: +1 626 395 8477, Fax: +1 626 584 9104. E-mail: dcrodger@mems.caltech.edu.

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