Bandwidth Enhancement for Transimpedance Amplifiers

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***Abstract*—A technique for bandwidth enhancement of a given amplifier is presented. Adding several interstage passive matching networks enables the control of transfer function and frequency response behavior. Parasitic capacitances of cascaded gain stages are isolated from each other and absorbed into passive networks. A simplified design procedure, using well-known low-pass filter component values, is introduced. To demonstrate the feasibility of the method, a CMOS transimpedance amplifier (TIA) is implemented in a 0.18-μm BiCMOS technology. It achieves 3 dB bandwidth of 9.2 GHz in the presence of a 0.5-pF photodiode capacitance. This corresponds to a bandwidth enhancement ratio of 2.4 over the amplifier without the additional passive networks. The trans-resistance gain is 54 dBΩ, while drawing 55 mA from a 2.5-V supply. The input sensitivity of the TIA is -18 dBm for a bit error rate of 10^{-12}.**

***Index Terms*—Bandwidth enhancement, integrated circuits, low-pass filter, matching networks, passive networks, transimpedance amplifier (TIA), wide-band amplifiers.**

I. Introduction

THE ever-growing demand for higher data rates has resulted in a rapid emergence of highly integrated communication systems. Silicon integrated circuits are the only candidates that can achieve the required level of integration with reasonable speed, cost, and yield and have thus been pursued to a great degree in recent years. In particular, full integration of silicon-based optical-fiber communication systems at 10 and 40 GB/s is of great interest. However, silicon-based integrated circuits implementing such systems face serious challenges due to the inferior parasitic characteristics in silicon-based technologies, complicating the procedure for a wide-band design.

Wide-band amplifiers are one of the most critical building blocks at the electrooptical interface on the receiver side. Wide-band operation is an inseparable part of any baseband communication system such as nonreturn-to-zero (NRZ) amplitude shift keying (ASK) common to optical fiber communications due to the signal's low-frequency spectral content. Particularly, all amplifiers in the signal path should have enough bandwidth with minimum variations in the passband and near constant group delay to avoid distortion in the signal.

The inherent parasitic capacitors of devices are the main cause of bandwidth limitation in wide-band amplifiers. Several bandwidth enhancement methods have been proposed in the past. First-order shunt peaking has historically been used to introduce a resonant peaking at the output as the amplitude starts to roll off at high frequencies [1]–[3].[1] It improves the bandwidth by adding an inductor in series with the output load to increase the effective load impedance as the capacitive reactance drops at high frequencies. Neuhauser *et al.* study the effect of bondwire inductors and use an active peaking network to enhance the bandwidth [4], [5]. Capacitive peaking [6] uses an explicit capacitor to control the pole locations of a feedback amplifier and thus potentially improves the bandwidth.

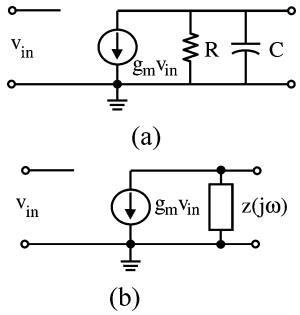

Fig. 1. Single-stage amplifier. (a) First-order load. (b) General passive impedance load.

A more exotic approach to solving the problem was proposed by Ginzton *et al.* using distributed amplification [7]. Here, the gain stages are separated with transmission lines. Although the gain contributions of several stages are added together, the artificial transmission line isolates the parasitic capacitors of several stages. In the absence of loss, we can improve the gain–bandwidth product without limit by increasing the number of stages. In practice, the improvement is limited by the loss of the transmission line. Hence, the design of distributed amplifiers requires careful electromagnetic simulations and very accurate modeling of transistor parasitics. For instance, a CMOS distributed amplifier was presented in [8] with a unity gain frequency of 8.5 GHz.

The study presented here applies a multipole bandwidth enhancement technique to wide-band amplifier design. It is based on turning the entire amplifier into a low-pass filter with a well-defined passband characteristic and cutoff frequency. The inevitable parasitic capacitances of the devices are absorbed as part of the low-pass filter and, hence, affect the bandwidth of the amplifier in a controlled fashion. Theoretical limits of gain–bandwidth product of lumped amplifiers have been known for over half a century [9]–[14]. Broad-band filter synthesis techniques for bandwidth enhancement has been used for wide-band amplifier [15], [16] and interconnect [17] design. Applying proper matching networks between amplifier stages to approach those limits is the key step in improving

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[1]For more references on traditional techniques for wide-band amplifier design, look at the bibliography of [9].

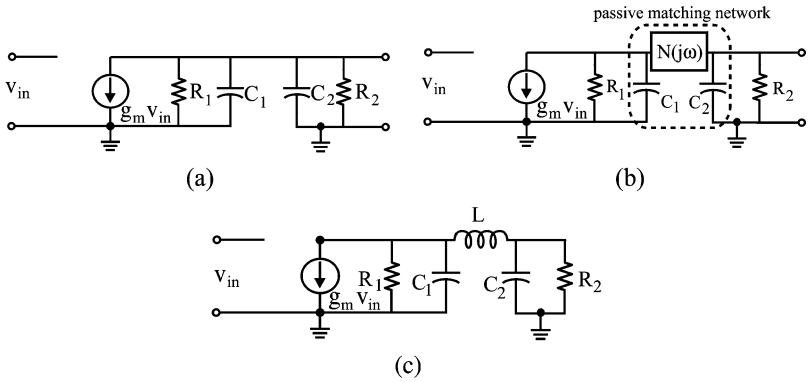


Fig. 2. (a) Small-signal model of an amplifier with the loading effect of the next stage amplifier. (b) The inserted passive network isolates the amplifier parasitics and the load. (c) Additional inductor forms a third-order passive network at the output.

wide-band amplifiers bandwidth with this method. Section II reviews these theoretical limitations. Section III presents a technique to improve the bandwidth of wide-band amplifiers. A design example using this technique follows in Section IV to demonstrate the practicality of the method, whose validity is shown with experimental results in Section V.

II. Wide-Band Amplifier Limits

A wide-band amplifier should retain near-constant gain and linear phase over its passband. The bandwidth requirements of such amplifiers continuously increase following the drive for higher speed systems. While device scaling continues to provide faster transistors with higher cutoff frequencies, it is still desirable to improve the bandwidth of amplifiers using circuit techniques that enable us to do so for a given process technology.

Over the last few decades, many techniques have been developed to improve the bandwidth of amplifiers [2]–[8], [18]. An improvement in the bandwidth of the amplifier is often accompanied by a corresponding drop in its low-frequency voltage gain. As such, the gain–bandwidth product (GBW) can serve as a first-order figure of merit for an amplifier topology in a given device technology [9], [10]. For the purposes of this discussion, the bandwidth is defined as the lowest frequency at which the voltage gain drops by $\sqrt{2}$ or 3 dB. Accordingly, this bandwidth is often called the 3-dB *bandwidth*. In Section II-A, we discuss the GBW limits of single-stage amplifiers for one- and two-port passive load networks. Section II-B is dedicated to GBW limits of multistage amplifiers.

A. Single-Stage Amplifiers

1) One-Port (Two-Terminal) Load Network: Fig. 1(a) shows the simplest model for a linear single-stage amplifier, where R and C are respectively the aggregate parasitic resistance and capacitance of the transistor and the input of the following stage. The GBW of this amplifier is given by

$$\text{GBW} = \frac{g_m}{2\pi \cdot C}. \tag{1}$$

As can be seen, the parasitic capacitance directly limits the bandwidth by reducing the output impedance of the amplifier as the frequency grows. Consequently, retaining a uniform output impedance over a wider frequency range will increase the GBW. In general, it is possible to introduce a more elaborate passive load network $Z(j\omega)$ to do so. Fig. 1(b) shows the generic load network, $Z(j\omega)$, that should look like a constant resistor over as wide a frequency range as possible. Wheeler [9] and Hansen [10] have derived an intuitive upper bound for such a range. Bode [11] has mathematically proven the existence of a bandwidth limit for a class of load impedances. Fano [12] and Youla [13] have further generalized the theory for a larger class. This theoretical limit (a.k.a. the Bode–Fano Limit) for the amplifier in Fig. 1(b) is [19]

$$\text{GBW}_{max} = \frac{g_m}{\pi \cdot \overline{C}} \tag{2}$$

where $\overline{C}$ is defined as

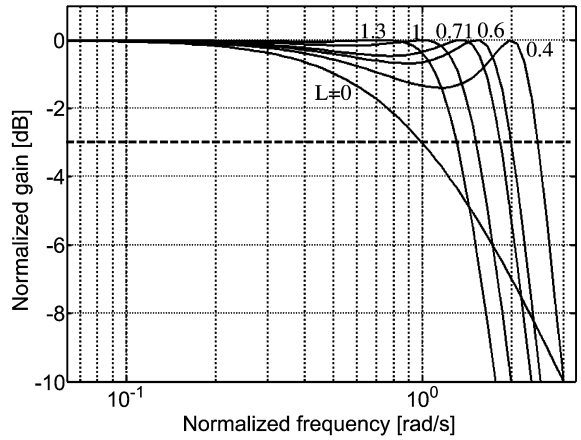
$$\overline{C} = \lim_{\omega \to \infty} \left(\frac{1}{j\omega Z} \right) \tag{3}$$

and $Z(j\omega)$ is an impedance function, as defined in the Appendix. $Z(j\omega)$ includes the aggregate output capacitance C, shown in Fig. 1(a). It is easy to show that, for a one-port load network, $\overline{C}$ is greater than or equal to C. Thus, according to (2), *any* one-port passive network added in parallel to C can improve the GBW by at most a factor of two over that of the amplifier in Fig. 1(a). As a result, the maximum achievable bandwidth enhancement ratio (BWER) for a one-port load is *two*. Shunt-peaking [1], [3], [9] is an example of this case. Shunt peaking results in BWERs of 1.6 and 1.72 when designed for optimum group delay or maximally flat responses, respectively [3].

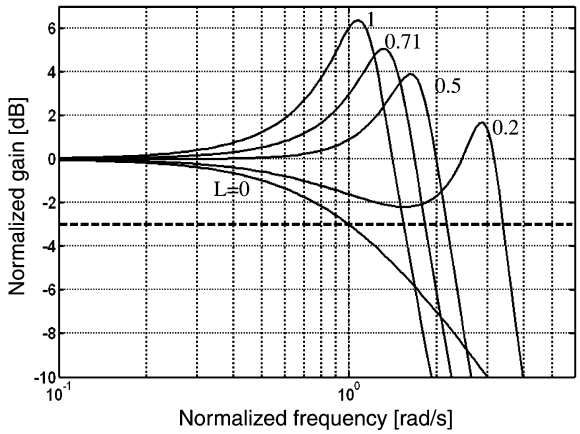
2) Two-Port (Four-Terminal) Matching Network: Fig. 2(a) shows a single-stage amplifier, where the intrinsic output resistance and capacitance of the transistor, i.e., R_1 and C_1, are separated from those of the load, namely, R_2 and C_2. The combination of capacitors C_1 and C_2 limits the bandwidth of the amplifier, i.e.,

$$\text{GBW} = \frac{g_m}{2\pi \cdot (C_1 + C_2)}. \tag{4}$$

In this case, a passive two-port network can be inserted between the transistor's intrinsic components (R_1 and C_1) and load (R_2 and C_2) to increase the bandwidth, as shown in Fig. 2(b). This two-port passive network can be designed to maintain the impedance constant over a wider frequency range, as it separates and isolates C_1 and C_2. Therefore, C_1 is the only



(a)



(b)

Fig. 3. Normalized gain of the amplifier with third-order network load and different inductor values. (a)$R_1 = R_2 = 1\ \Omega, C_1 = C_2 = 1\ F$. (b) $R_1 = 0.5\ \Omega, R_2 = \infty, C_1 = C_2 = 1\ F$.

capacitor that affects GBW at the input port of the network. Based on the argument in Section II-A1, the maximum GBW product at the input port of $N(j\omega)$ is

$$\text{GBW}_{max} = \frac{g_m}{\pi \cdot C_1}. \tag{5}$$

Bode [11] has shown that, for $C_1 = C_2 = C/2$,[2] it is possible to design $N(j\omega)$ in such a way that the GBW product at the output port is the same as that of the input. Thus, for a single-stage amplifier with a two-port passive load network, we have

$$\text{GBW}_{max} = \frac{2g_m}{\pi \cdot C}. \tag{6}$$

This can be done by using a constant-*k LC*-ladder filter [9], [11], [20] terminated to its image impedance. A constant-*k LC*-ladder filter that is terminated in its image impedance has a *constant* transfer function over the frequencies less than its cutoff frequency. Compared to (4) with $C_1 = C_2 = C/2$, (6) is four times larger than the GBW product of a single-stage amplifier

[2]If not equal, he proposes adding an ideal transformer at the output to match C_2 to C_1 with a proper ratio.

TABLE I
BWERs FOR THE TWO THIRD-ORDER PASSIVE NETWORKS IN FIG. 3

L value [H]	Case 1 (R_1=R_2=1Ω)	Case 2 (R_1=0.5Ω, R_2=∞)
0	1	1
0.2	1.44	3.4
0.4	2.46	2.42
0.5	2.2	2.17
0.6	2	1.99
0.707	1.83	1.83
1	1.52	1.55
1.3	1.31	1.36

without additional coupling network. As a result, for equal low-frequency gain, the maximum achievable BWER for a two-port load is *four*.

In general, it is computationally difficult to calculate the component values for the optimizing two-port network directly. Even in the case of a third-order system, with only an additional inductor between the device and the load as in Fig. 2(c), the equation for the value of the inductor that maximizes the bandwidth is quite complicated. Instead, graphical or numerical methods can be used. Fig. 3 shows normalized gain of a single-stage amplifier with a passive network load similar to Fig. 2(c), where a single inductor isolates C_1 and C_2. The component values are normalized to achieve 0 dB gain at low frequency and a 1-rad/s 3-dB bandwidth. Fig. 3(a) corresponds to when the output impedance of the amplifier is equal to the load ($R_1 = R_2 = 1\ \Omega$ and $C_1 = C_2 = 1$ F). Fig. 3(b) shows the case for $R_1 = 0.5\ \Omega$ and $R_2 = \infty$. This may occur when the output of the amplifier is connected to a next stage with capacitive input. Values for the BWER, defined as the ratio of the 3-dB bandwidth of the amplifier to the 3-dB bandwidth when $L = 0$, in both cases is summarized in Table I. It is noteworthy that even with a simple third-order passive network, BWER is significant compared to its theoretical limit. Bandwidth optimization assumes no gain peaking constraints.

An alternative method to design the passive network is to look up the component values in standard tables for low-pass filter design [21] or compute them from corresponding equations [9], [22], [23]. Essentially, the additional passive networks are low-pass structures that control the frequency response of the amplifier. After choosing the desired frequency response for the amplifier, such as maximally flat gain or maximally flat group delay, the component values can be chosen directly from standard tables. This will be discussed thoroughly in Section III.

B. Multistage Amplifiers

Often it is hard to achieve a desirable GBW product with a single-stage amplifier. Then, several stages can be cascaded. The total gain is the product of the gain of each stage. However, the overall bandwidth is less than the bandwidth of each stage, because the gain drop in the passband of each amplifier will accumulate. For instance, the overall 3-dB bandwidth and the GBW of an amplifier made by cascading N similar

single-pole amplifiers with gain A_v and bandwidth ω_o with no mutual loading is

$$\omega_{\text{overall}} = \omega_{\text{o}} \cdot \sqrt{\sqrt[N]{2} - 1} \tag{7}$$

$$\text{GBW} = A_v^N \cdot \omega_{\text{overall}}. \tag{8}$$

Comparing to the single-stage gain–bandwidth product, $A_v\omega_o$, there is a gain–bandwidth improvement of[3]

$$\frac{\text{GBW}_{\text{multistage}}}{\text{GBW}_{\text{one-stage}}} = A_v^{N-1} \cdot \sqrt{\sqrt[N]{2} - 1}. \tag{9}$$

For instance, $N = 2$ and $A_v = 10$ correspond to a factor of 6.4 improvement in GBW. For larger A_v, GBW will increase dramatically by introducing additional single stages at the price of increasing overall power consumption.

In practice, each stage has a loading effect on its previous stage, which reduces its bandwidth, hence reducing the overall bandwidth. The matching networks introduced in Section II-A2 can reduce the loading effect by separating the output of an amplifier from the input of its next stage. One disadvantage of multistage amplifiers, in general, and multistage amplifiers with two-port matching networks between each stage, in particular, is excessive phase shift that each amplifier stage or each network adds to the signal path [11], which can result in instability in *feedback* amplifiers.

III. Design Methodology

Based on the discussions in the previous section, for a given wide-band amplifier, one can add passive matching networks at the input and output, as well as between the gain stages of the amplifier to enhance the bandwidth. This method brings each stage of the amplifier closer to its theoretical limit discussed in Section II. The networks absorb the capacitive parasitic components of the gain stages (transistors) and/or the source and load into their structure. Each network can be designed as a *low-pass filter* structure with standard response [9], [23]. To achieve a particular response shape for each network (e.g., maximally flat group delay), the components in the passive network take the same values as their corresponding element in the filter.

In this approach, one can resort to passive networks with *low sensitivity* to component values such as ladder structure [24], [25]. Fig. 4 shows a general low-pass ladder structure inserted between two gain stages in an amplifier. The component values are generated using standard look-up tables [21] or network synthesis methods [22]. The network order N is an additional design parameter. Using higher order networks will provide wider bandwidth and sharper transition from passband to stopband. However, it may cause some practical issues, such as unreasonable components values, a large number of passive components (large die area), and additional signal loss due to passive components (primarily inductors). Typically these issues limit the order of the network to *five*, i.e., only three additional passive components.

[3]The overall GBW will actually improve if $A_v > (\sqrt[N]{2} - 1)^{(-1/(2N-2))}$.

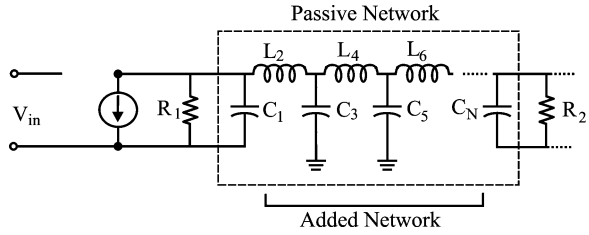


Fig. 4. Passive ladder structure of order N, inserted between the gain stages.

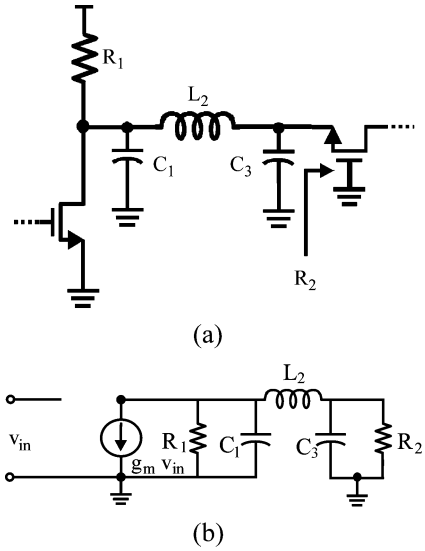


Fig. 5. (a) Inductor is inserted between two gain stages. (b) The small-signal model shows formation of a third-order ladder network.

Design Example: Here, we show the procedure for designing a maximally flat response third-order passive network as an example. Fig. 5(a) illustrates two stages of a given amplifier with an inductor inserted between them. Fig. 5(b) demonstrates that the inductor forms a third-order ladder structure with C_1 and C_3, which are transistor parasitic capacitances. The values for R_1, R_2, C_1, and C_3 are known for the amplifier. To achieve a maximally flat frequency response at the output of the ladder, components values should be equal to their corresponding third-order Butterworth filter elements as follows [22]:

$$C_1 = \frac{1}{R_1(1-\delta)\omega_c} \tag{10}$$

$$L_2 = \frac{2}{(1-\delta+\delta^2)\cdot\omega_c^2\cdot C_1} \tag{11}$$

$$C_3 = \frac{1}{R_2(1+\delta)\omega_c} \tag{12}$$

where δ is an indication of impedance transformation between R_1 and R_2 and is defined as

$$\delta = \sqrt[3]{\frac{R_1 - R_2}{R_1 + R_2}} \tag{13}$$

and ω_c is the 3-dB cutoff frequency of the network. From (10), the new amplifier bandwidth at the output of the ladder structure is

$$\omega_{c,\text{new}} = \frac{1}{(1-\delta)\cdot R_1 \cdot C_1}. \tag{14}$$

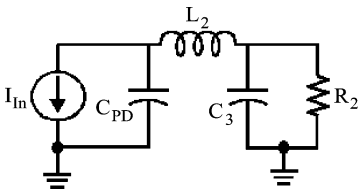


Fig. 6. Inductor at the input forms a third-order ladder network with the photodiode capacitance.

The inductor value can be calculated from (11) and (14). C_3 for the original amplifier may not be equal to the value with the new cutoff frequency, calculated from (12). Some explicit capacitance should be added to adjust for this. If we define the BWER as the ratio between the new 3-dB bandwidth and the old one (without adding the inductor) of the single-stage amplifier, we can show

$$\text{BWER} \equiv \frac{\omega_{c,\text{new}}}{\omega_{c,\text{cold}}} = \frac{1}{1-\delta} \cdot \frac{R_2}{R_1+R_2} \cdot \frac{C_1+C_3}{C_1}. \quad (15)$$

Equations (10), (12), and (13) simplify (15) to an expression based on the ratio of R_1 and R_2. BWER decreases monotonically when R_2/R_1 increases. For a given amplifier with $R_2 < R_1$, adding the inductor always enhances the bandwidth by BWER. When $R_2 = R_1$, BWER$= 1$ and there is no bandwidth enhancement with adding the inductor. However, a maximally flat passband and sharp cutoff response is still achieved.

The same analysis can be applied to the input stage of a transimpedance amplifier. The photodiode is modeled as a current input and R_1 is eliminated from the model, as shown in Fig. 6. Design calculations using (10)–(14) can use an arbitrary value for R_1. An optimum value for R_1 can be computed from (14) with fixed C_1 and R_2, to maximize the 3-dB bandwidth. It results in $R_1 = 2.05R_2$ with $\delta = 0.7$. After designing the inductor and adjusting for C_3, R_1 can be eliminated. Essentially, the transimpedance gain will increase as no portion of the input current is absorbed by R_1. The enhancement ratio should also be modified for the input passive structure as

$$\text{BWER} = \frac{1}{1-\delta} \cdot \frac{R_2}{R_1} \cdot \frac{C_{PD}+C_3}{C_{PD}} = 1.63 \cdot \left(1+\frac{C_3}{C_{PD}}\right). \quad (16)$$

The preceding example can be generalized to any response shape when (10)–(12) are replaced with their corresponding filter component equation. Equations (15) and (16) should also be modified to correspond to the new component values.

IV. Example Design

To demonstrate the effectiveness of the developed methodology, a CMOS transimpedance amplifier (TIA) is designed. It is a single-ended design consisting of three gain stages. The first stage is a shunt-shunt feedback transimpedance stage as shown in Fig. 7(a). The input resistance of the amplifier is approximated by $R_f/(A+1)$, where A is the inverting voltage gain. Thus, it can provide a low input impedance and reduce the dominant effect of the input pole due to the large photodiode junction capacitance C_{PD}. The input pole frequency can be written as

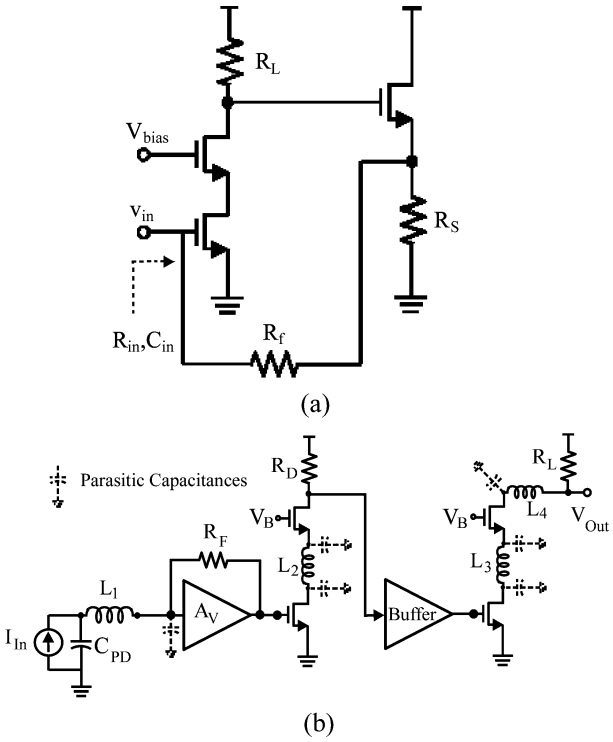


Fig. 7. (a) Schematic of the input stage of the TIA. (b) Schematic of the TIA with parasitic capacitances and additional inductors.

$$P_{\text{in}} \approx \frac{1}{R_{\text{in}} \cdot (C_{PD}+C_{\text{in}})} \approx \frac{A}{R_f \cdot (C_{PD}+C_{\text{in}})} \quad (17)$$

where R_{in} and C_{in} are the input resistance and input capacitance, respectively. For the circuit in Fig. 7(a), if the transistors are in the short channel region, both C_{in} and A are proportional to the input transistor width W_{in} as follows:

$$A \approx g_m \cdot R_L \approx v_{\text{sat}} C_{\text{ox}} W_{\text{in}} \cdot R_L \quad (18)$$

$$C_{\text{in}} \propto C_{\text{ox}} L_{\text{in}} W_{\text{in}} \quad (19)$$

where C_{ox} is the gate oxide capacitance, v_{sat} is the carrier saturation velocity, and L_{in} is the input transistor channel length. When the input width increases, there is a bound for the input pole dominated by C_{in}. However, additional constraints such as power consumption or input noise set an optimum width for the input transistor [26]. Adding the additional inductor to isolate C_{in} and C_{PD} enhances the bandwidth according to (16). In this design, we match the input resistance to our electrical measurement setup which had a 50-Ω input resistance. The next two stages of the amplifier are designed as a cascode configuration with intermediate inductors and are isolated using a source follower buffer. Adding the source follower avoids the large input capacitance of the third-stage amplifier to load the second stage as well as providing a low impedance node at its output and increasing its pole frequency. The simplified schematic of the circuit including the added passive components is shown in Fig. 7(b).

Four passive networks are inserted between the stages of the amplifier to enhance the bandwidth. The input network sepa-

TABLE II
COMPARISON OF THE INDIVIDUAL EFFECTS OF THE INDUCTORS ON BWER

additional inductors	BWER
no inductor	1
L_1 only	1.48
L_2 only	1.42
L_3 only	1.62
L_4 only	1.17
L_1, L_3	2
L_1, L_2, L_3	2.3
All	2.4

rates the photodiode capacitance and the parasitic capacitance of the input stage. Adding one inductor will transform it to a third-order ladder structure, which can be designed as explained in Section III. The next two networks are also third-order and are placed between the cascode transistors. The load capacitance in conjunction with the output capacitance (including bonding pad) and output bondwire inductor form the output third-order network.

The capacitors, as shown by the dotted line in Fig. 7(b), are the parasitics from the devices and only four inductors are added to the original circuit. The input and output inductors are bondwire inductors and the interstage ones are on-chip spiral inductors. A final optimization step in the simulation is performed to include the bilateral effects of the devices. Note that the output network is different from a conventional shunt-peaking approach. For a photodiode capacitance of 0.5 pF, the circuit achieves over 9 GHz 3 dB bandwidth. This is 2.4 times larger than the bandwidth achieved using same circuit without the inductors. The individual effect of each passive network and the effect of a combination of them is summarized in Table II from simulation results. L_3 causes the largest improvement in bandwidth because the device sizes of the second cascode amplifier are large to drive 50 Ω with a minimum loss of gain. L_1 is separating the two large capacitances that form the input pole frequency. In our design, this pole is the dominant bandwidth-limiting factor of the core TIA without a driver. L_4 is not remarkably enhancing the bandwidth because the output pole is not dominant. However, L_4 will exist in the circuit as the bondwire and should be modeled. All four passive networks have a ladder structure for lower sensitivity to process variations.

Both on-chip inductors were implemented as spiral inductors in the top metal layer. Accurate electromagnetic modeling of the inductors was done using ASITIC [27] and SONNET [28] E&M simulators and gave similar results. The parasitic capacitances of the inductors are not negligible and their impact is considered in addition to device parasitics.

V. EXPERIMENTAL RESULTS

The TIA was implemented in a 0.18-μm BiCMOS process technology using *only* CMOS transistors. It draws 55 mA from a 2.5-V power supply. The scattering parameters were measured

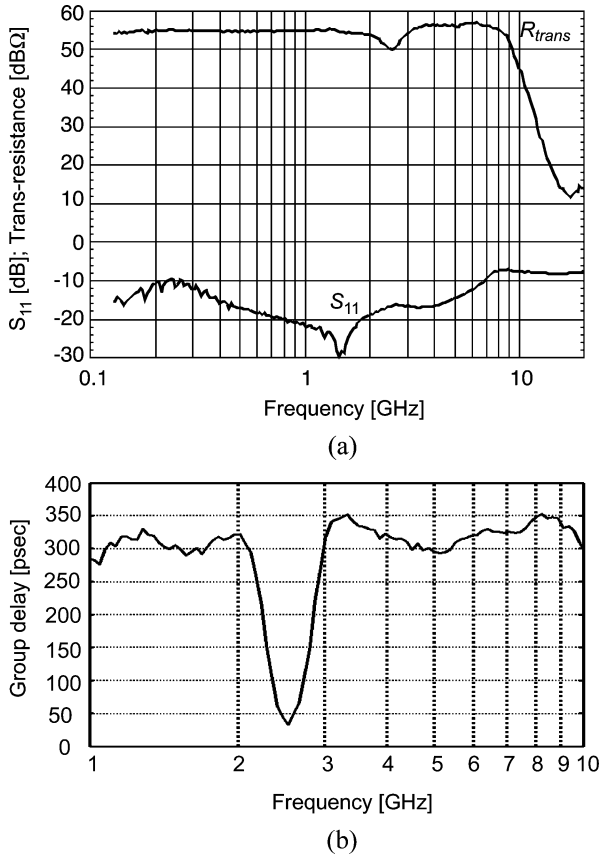


Fig. 8. (a) Transresistance gain of the TIA with 0.5 pF photodiode capacitance. (b) Group delay response of the TIA.

with a 20-GHz HP8720B network analyzer. The amplitude and group delay response of the implemented TIA, extracted from measurement data, are shown in Fig. 8(a) and (b), respectively. Here, the photodiode capacitance is $C_{\rm PD} = 0.5$ pF. Matched output will cause a 6-dB drop in the gain which is adjusted for in the reported result. Group delay is calculated from the phase response of the amplifier and logarithmic frequency steps of the network analyzer.

The 3-dB bandwidth is 9.2 GHz, in good agreement with the simulations, and the transimpedance gain is 54 dBΩ. To the best of our knowledge, this is the fastest 0.18-μm CMOS TIA to date. The input reflection coefficient S_{11} remains below -10 dB up to 7 GHz. Although we did not design for flat group delay, the group delay ripples are ± 25 ps. The dip in the frequency response of the transimpedance at 2.5 GHz can be correlated to a resonance mode between the on-chip supply bypass capacitor and bondwire and supply line inductances. Changing these parameters changes its depth and frequency during the measurement and can be removed by using a different supply bypassing technique in a revised version of the design. The design has low sensitivity to inductor values. L_1 and L_4 are 0.5–0.6 nH. L_2 and L_3 are 1-nH 100×100 μm^2 spiral inductors.

Fig. 9 shows the eye diagram when a $2^{31} - 1$ pseudorandom bit sequence (PRBS) is applied to the input at 10 GB/s. The ringing is partly due to the resonance mode at 2.5 GHz and partly due to the absence of the photodiode capacitance that will cause peaking in the overall transfer function. This peaking

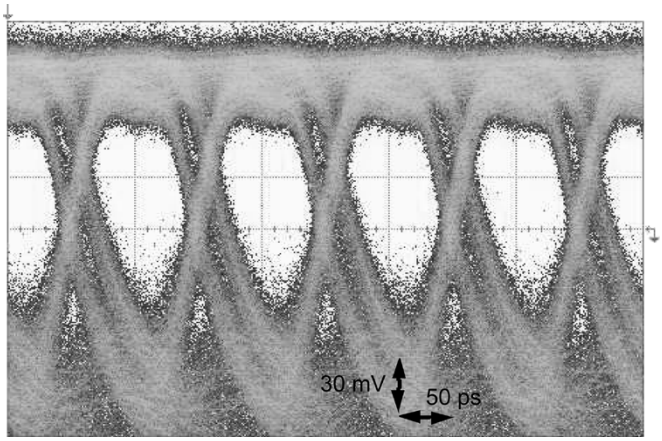


Fig. 9. Eye diagram of the TIA output with 10 GB/s $2^{31}-1$ PRBS at the input.

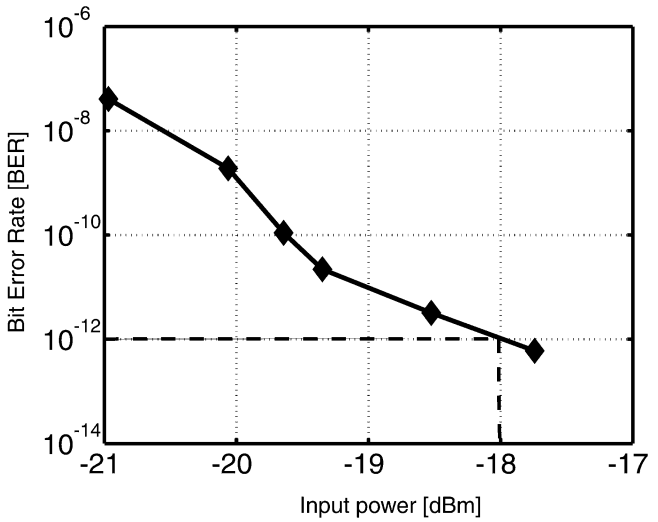


Fig. 10. BER of the TIA for different input powers at 10 GB/s.

translates to a ringing response in the time domain and will increase the intersymbol interference penalty and close the eye vertically. However, the TIA still achieves the overall sensitivity of -18 dBm for a bit error rate (BER) better than 10^{-12}, as we will discuss next.

The electrical sensitivity of the amplifier for different BERs is measured using Antrisu's MP1763C and MP1764C BERT system. A $2^{31}-1$ PRBS is applied to the input at 10 GB/s and the BER is measured for different electrical input powers at 500-s intervals. The results are depicted in Fig. 10. For a data communication link, the required BER is typically 10^{-12}. The TIA achieves a sensitivity of -18 dBm or 15.8 μW for this BER when photodiode capacitance is not present. At very low power inputs, we were limited to the sensitivity of the bit-error-rate test (BERT) system. The TIA output swing was not large enough to meet the minimum requirement of the BERT input. Simulated total input noise current, integrated over the bandwidth, equals 1.6 μA, which is comparable to TIAs with the same bandwidth [18].

The amplifier core occupies 0.8×0.8 mm^2 of area, as shown in Fig. 11. Table III summarizes the performance of the prototype TIA that has been demonstrated.

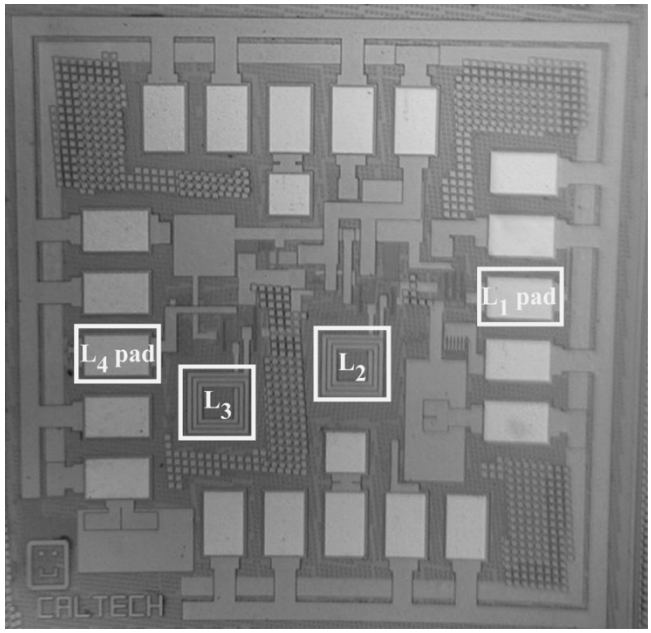


Fig. 11. Die photograph of the 9.2-GHz TIA.

TABLE III
TIA PERFORMANCE SUMMARY

TIA performance summary	
Bandwidth (3dB)	9.2 GHz
single-ended trans-impedance	54 dBW
sensitivity for BER=10^{-12}	-18 dBm
input reflection coefficient (S_{11})	$\leqslant$ -10 dB
dc current consumption	55 mA
power supply	2.5 V
core die area	0.64 mm^2
technology	0.18µm CMOS

VI. CONCLUSION

In this paper, we address the gain–bandwidth product limits of amplifiers and introduce a practical methodology that can be used to enhance the bandwidth of wide-band amplifiers with specified characteristics for their transfer function. In a simple design procedure, parasitic capacitances of transistors can be absorbed into passive networks, inserted between the gain stages. The component values can be calculated based on standard low-pass filter structures. A prototype CMOS TIA implemented using the developed technique achieves over 9-GHz bandwidth and 54-dBΩ transimpedance gain in the presence of a 0.5-pF photodiode capacitance.

APPENDIX

An impedance function is a rational function (ratio of two polynomials with real coefficients) of frequency with no right half-plane poles. Additionally, the numerator polynomial should be of at most one degree higher than the denominator one. The conditions for an impedance function can be found in [11], [19]. The upper bound in (2) is not valid if the load does not satisfy

the conditions of an impedance function. In other words, if the overall transfer function of an amplifier is of the form

$$A_v(j\omega) = g_m \cdot Z(j\omega) \tag{20}$$

and $Z(j\omega)$ is *not* an impedance function, then the Bode–Fano limit need not be satisfied. Distributing passive structures between gain stages can result in overall transfer functions that are *not* impedance functions per se [23]. Therefore, the GBW product can potentially be higher than the limit in (2). One design approach for such structure is stagger tuning of the frequency responses. An early amplitude roll-off due to a low-frequency pole in one stage can be compensated for with a peaking in the next stage. Similarly, the overall phase response of passive structures can be properly controlled.

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