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Design of a 5-bit algorithmic A/D converter for potential use in a wireless neural recorder application

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Thesis

DESIGN OF A 5-Bit ALGORITHMIC A/D CONVERTER FOR POTENTIAL USE IN A WIRELESS NEURAL RECORDER APPLICATION

by

NIKHIL RANJAN

B.Tech., Dr. B.R. Ambedkar National Institute of Technology, 2009

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Approved by

First Reader _____

Ronald W. Knepper, Ph.D.
Professor of Electrical and Computer Engineering

Second Reader _____

Min-Chang Lee, Ph.D.
Professor of Electrical and Computer Engineering

Third Reader _____

Rabia Yazicigil, Ph.D.
Assistant Professor of Electrical and Computer Engineering

I wonder what's going on in our brain,

and if only I could do something to find out.

DEDICATION

I would like to dedicate this work to my advisor, Professor Ronald W. Knepper (Ph.D., BU ECE), my parents and my younger brother and his wife. Without their unconditional and continuous support, I could not have made it so far.

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I am grateful to Professor Knepper, my erudite advisor, for providing this opportunity and be my anchor throughout my Master's program at BU. He is the reason for all the knowledge I have acquired in Analog Circuit Design. His course structure, innovative project ideas and round the clock availability to help out students has helped me with my preparation of this thesis and made me ready for the professional world out there.

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I thank my family and friends for their belief in my abilities and encouraging me with their love to move ahead in my life.

DESIGN OF A 5-Bit ALGORITHMIC A/D CONVERTER FOR POTENTIAL USE IN A WIRELESS NEURAL RECORDER APPLICATION

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ABSTRACT

The constant endeavor to measure and record neural signals from the human brain and anticipate the results to figure out the mechanism which governs the functionality of our brain and its true behavior is the major driving force behind this thesis. Neural recording integrated circuits (ICs) are often inserted directly into the brain, with a set of probes for sensing these action potentials (and local field potentials), and appropriate circuitry for amplifying the neural signals (Pre-Amp), sampling and converting the analog signals to digital (ADC) and transmitting the resulting digital signal (Transmitter) to a nearby reader instrument (Receiver). Action potentials are comprised of signals typically looking like spikes having a peak voltage of 1-2mV, whereas local field potentials are continuous signals generally having an amplitude of around 100-200μV often with a dc component of several mV. Fourier analysis of action potentials and local field potentials show frequency components in the range of 0.1 Hz up to 10kHz.

This thesis proposes a low-power 5-bit algorithmic A/D converter to feed a 5-stage serial shift register for use in sampling and converting a presumed neuron action potential signal at the rate of 20k samples/sec. In addition to that, a low-power preamp with at least 40dB gain and a low-pass type spectrum having

a unity-gain frequency of at least 20MHz is used to amplify the input signal. The algorithmic A/D converter includes a sample-and-hold circuit for sampling the analog action potential spike at a rate of 20kHz. The ADC utilizes an X2 gain circuit based on a capacitive redistribution technique. A less complex circuit in terms of dependency on Capacitor sizing and their non-ideal effects is the key factor for selecting this type of ADC which can be used for neural recording applications. All the circuits are designed based on the IBM/Global Foundries 8HP 130nm BiCMOS technology.

Keywords: Algorithmic ADC, low power design, multiply by 2(voltage) Circuit, neural recorder applications, Analogue Adder, Comparator, Pre-Amplifier

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LIST OF ABBREVIATIONS

ADC.....Analog to Digital Converter

BU .....Boston University

DNL.....Differential Nonlinearity Error

ENOB .....Effective Number of Bits

INL.....Integral Nonlinearity Error

MEMS .....Micro Electro Mechanical System

Op-Amp..... Operational Amplifier

RMS..... Root Mean Square

SAR ..... Successive Approximation Register

SFDR.....Spurious Free Dynamic Range

SNDR ..... Signal to Noise and Distortion Ratio

SNR .....Signal to Nosie Ratio

SPDT .....Single Pole Double Throw

SPST .....Single Pole Single Throw

THD..... Total Harmonic Distortion

CHAPTER 1: INTRODUCTION

1.1 Background

With the increasing development in the field of semiconductors and advent of new sensors and transducers, the curiosity and experimentation to measure bodily signals are also on the rise. One such example is to measure and record neural signals from the human brain and anticipate the results to figure out the mechanism which governs the various functionalities of our brain. The bio-electronic characteristic of our brain when monitored properly, can provide useful insights which can be very vital in treating a lot of diseases better, for example, Parkinson's and Alzheimer's disease.

1.2 Neural Sensor

Neural signals produced by Neurons due to their electrically active nature are generally weak in nature and need a very sensitive device to measure the signal. Ongoing developments in the field of MEMS have made it possible to measure these signals but they still need amplification. Another workaround is to collect signals using an array of electrodes as shown in Fig. 1.1.

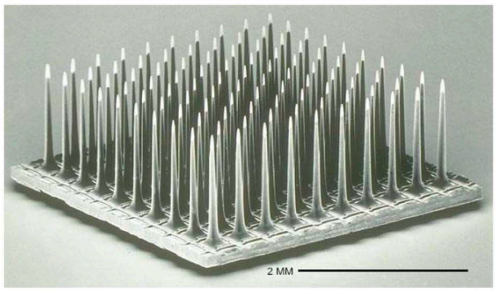

Fig. 1.1 Silicon based Electrode Array [Harrison, 2008]

1.3 Neural Recording Applications

Action potentials (signal from an individual neuron) and local field potentials (average signal from a group of neurons) are of particular interest to researchers for studying the brain. Neural recording integrated circuits (ICs) are often inserted directly into the brain, with a set of probes for sensing these action potentials (and local field potentials), and appropriate circuitry for amplifying the neural signals (Pre-Amp), sampling and converting the analog signals to digital (ADC) and transmitting the resulting digital signal (Transmitter) to a nearby reader instrument (Receiver). Action potentials are comprised of signals typically looking like spikes having a peak voltage of 1-2mV, whereas local field potentials are continuous signals generally having an amplitude of around 100-200μV often with a dc component of several mV. Fourier analysis of action potentials and local field potentials show frequency components in the range of 0.1 Hz up to 10kHz.

Several designs for Neural Recording applications have been published, [Biederman, 2013; Bagheri, 2013; & Wang, 2016]. There is a desire, however, in many applications to further reduce the complexity of the circuit design and the maximum stimulation current that could be achieved for a given supply voltage. In this process, the size of the neural interface device and available power also reduces significantly which is a constant challenge and therefore more research, for a better design and implementation is still ongoing.

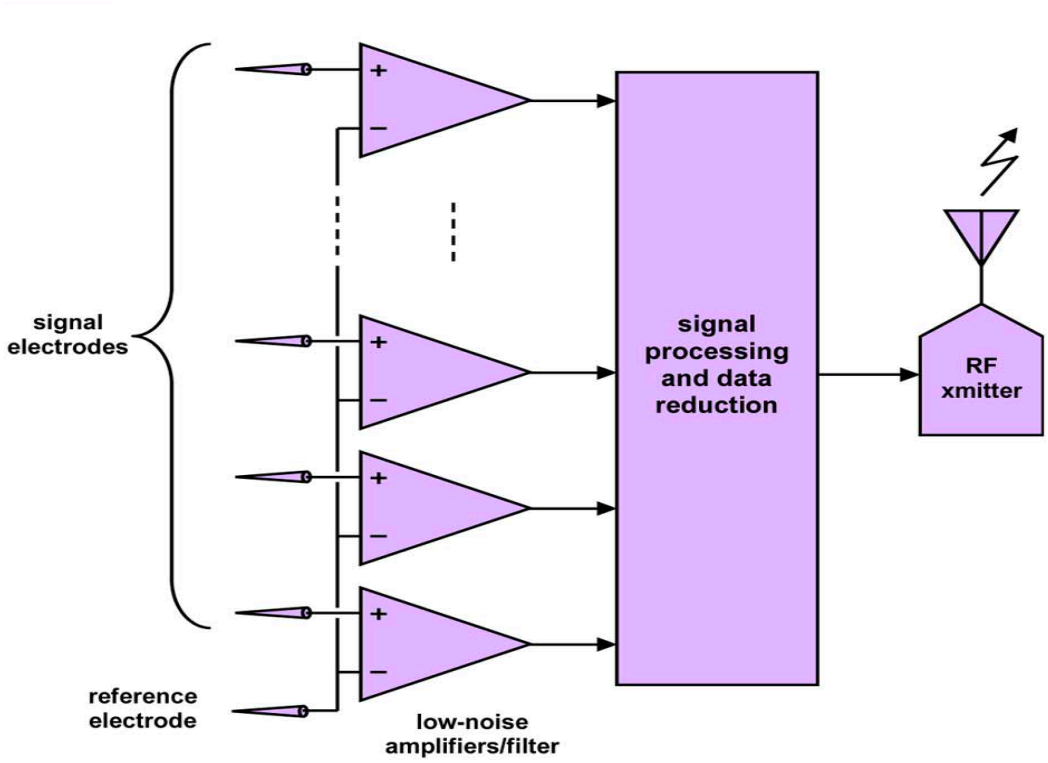

Fig. 1.2 Block Diagram for Neural Recorder [Harrison, 2008]

Fig. 1.2 shows a typical neural recording application block diagram.

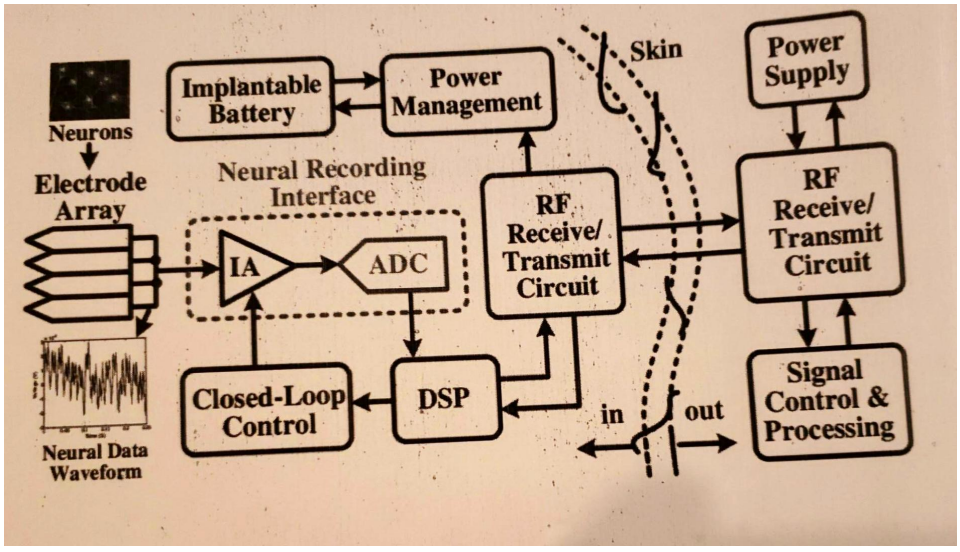

Fig. 1.3 Typical representation of Neural Recording Application

Fig. 1.3 shows another typical neural recording block diagram [Xu, 2015]

1.4 ADC's role in a Neural Recording Application

ADCs play an important role in the whole process as illustrated in previous sections. The sampling speed to match the output of neural sensor array, the accuracy of the output without missing bits in the process, the complexity of the ADC design, power consumption, and die area are some of the most important considerations. In this work, the primary focus is to reduce the complexity of ADC design and remove the dependency on Capacitor matching as is required in case of SAR based ADCs, while keeping the accuracy, speed and die area into check.

CHAPTER 2: General Overview of ADCs

2.1 Introduction

Most of the electrical signals we encounter in our daily life are analog in nature and the signal processing devices are digital in nature. ADCs bridge the gap between these two by acting as the interface and in turn become a very important component of most of the modern circuits.

The basic functionalities of an ADC are as following:

- Sample and Hold
- Quantization
- Assign a digital code

ADCs take an analog input, convert it into various samples, and assign a digital set of bits for each of these samples. Based on the bits collected, final output bit word is arrived at and is called the digital output. Time taken to convert one analog input to digital bit word output is called conversion time. The length of bit word, or the number of bits in the digital output is called the resolution of the ADC. Accuracy is defined as the output obtained without missing any bits for a particular range of inputs and to be able to correctly assign a digital set of bits for each of the smallest sample based on the resolution.

ADCs can be categorized based on their speed and accuracy as shown in Table 2.1[Carusone, 2012].

Low to Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low to Medium Accuracy
Integrating	Successive Approximation	Flash
Oversampling	Algorithmic	Two-Step
		Interpolating
		Folding
		Pipelined
		Time-Interleaved

Table 2.1 Different ADC Architectures [Carusone, 2012]

The performance of an ADC can be illustrated through their General, Static and Dynamic Characteristics.

2.2 General Characteristics

Fig. 2.1 shows the block diagram of an ADC. V_{in} represents the analog input and B_{out} is the digital output word. V_{ref} is the reference voltage to which the input signal is compared to calculate the output bits. V_{LSB} is defined as the signal change corresponding to a single LSB change [Carusone, 2012].

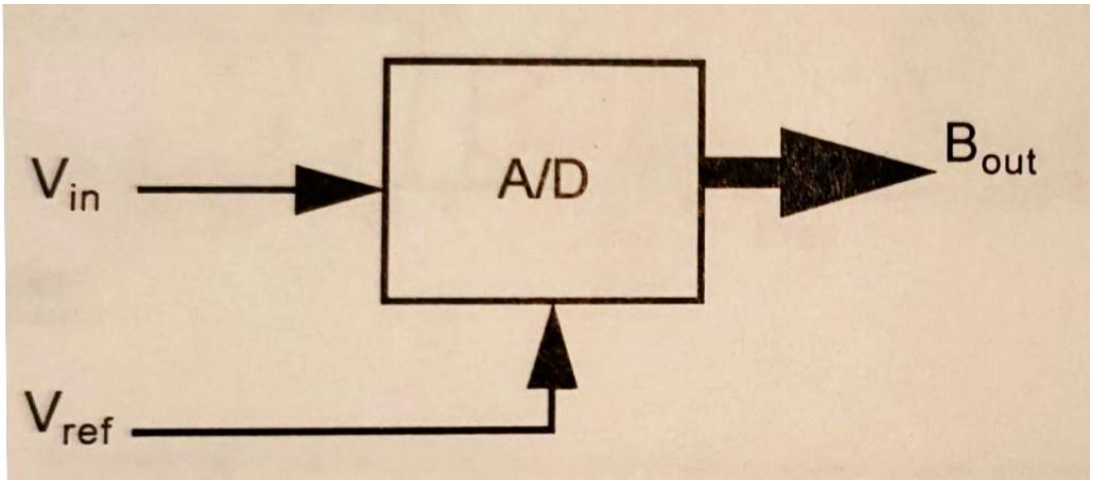

Fig. 2.1 ADC Block Diagram [Carusone, 2012]

For an ADC, the transfer characteristics represent the relation between input and output as shown in Fig. 2.2. In an Ideal ADC, it is similar to a staircase function.

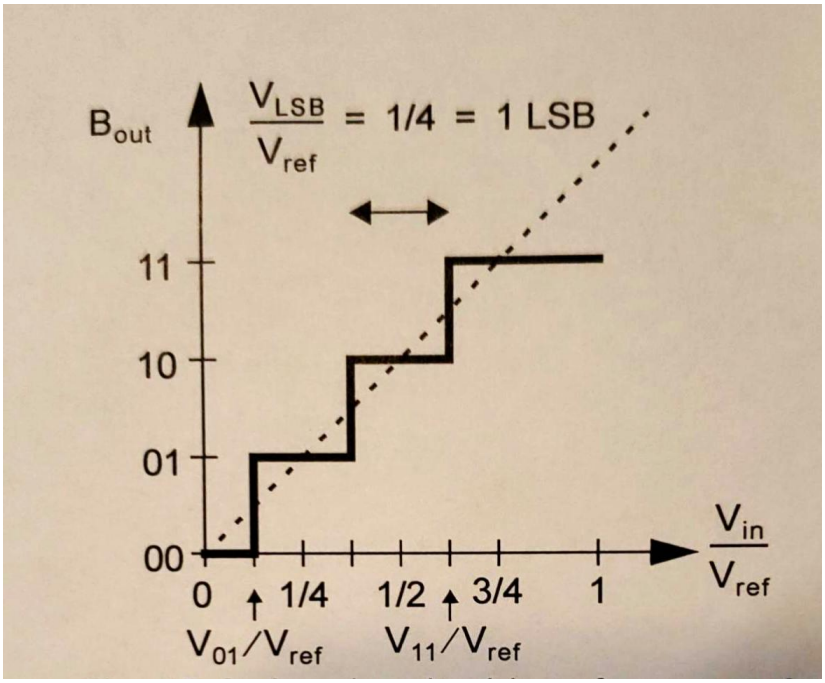

Fig. 2.2 Input Output Characteristic Curve for a 2-Bit ADC [Carusone, 2012]

We can clearly see from Fig 2.2 that the range of values for which digital output remains the same is $\frac{-1}{2}$ V_{LSB} to $\frac{1}{2}$ V_{LSB}. This ambiguity produces Quantization Error and leads to Quantization Noise which lies between -0.5 LSB to +0.5 LSB for an ideal ADC.

2.3. Static Characteristics

Static characteristics are those which are measured at very low input frequencies or DC [Carusone, 2012]. Offset and Gain errors, INL and DNL Errors are the major static characteristics of our interest.

Offset Error is the difference between Ideal and measured curve, whereas Gain Error is the difference between the ideal and measured curve after offset error has been corrected [Carusone, 2012]. Offset reduces the dynamic range of the ADC by its value.

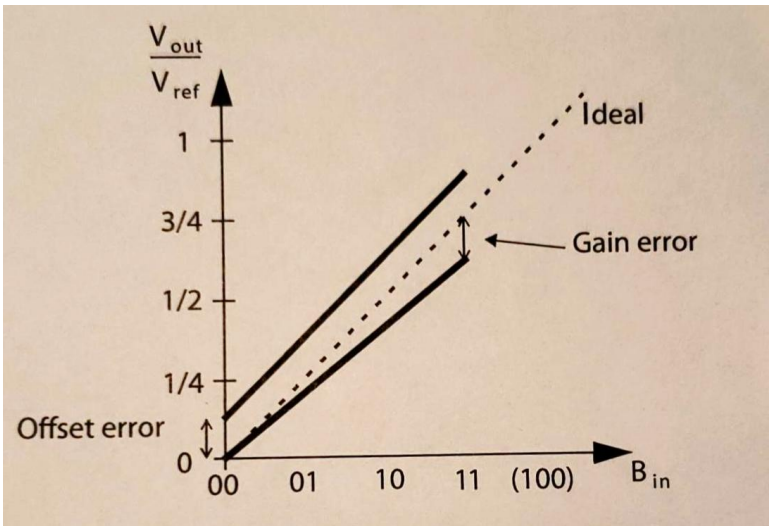

Fig. 2.3 Offset and Gain Error [Carusone, 2012]

INL is the deviation from the ideal curve after the offset and gain errors have been corrected. DNL is the variation in analog step sizes away from 1 LSB after correction of offset and gain errors [Carusone, 2012]. Normally, code transitions are 1 LSB apart. DNL should be always less than 1 LSB, else we can miss a code at output. The integral of DNL error is called the INL error. In other words, the accumulation of all DNL errors at a given point of time is INL error. There are various methods to measure INL error like End Point Method or Best Fit Method.

2.4 Dynamic Characteristics

These are measured at high input signal frequencies, hence the name Dynamic characteristics. SNR, SNDR, THD, ENOB, Dynamic Range and SFDR are the major characteristics of our interest.

SNR is the ratio of Signal power to Noise power.

SNDR is the ratio of signal power to Noise and Distortion Power.

THD is the ratio of amplitudes of the input signal to the sum of amplitudes of harmonics.

ENOB is given by the relation ENOB = $\frac{\text{SNDR}-1.76\text{dB}}{6.02\text{dB}}$ bits [Carusone, 2012].

Since for a given sinusoidal input, maximum signal to quantization noise ratio is 6.02N+1.76 dB. [Carusone, 2012].

Dynamic range is the range of values of inputs for which output is valid. Noise determines the minimum input and distortion determines the maximum input.

Spurious free Dynamic Range (SFDR) is the ratio of RMS value of the amplitude of input signal fundamental tone to the RMS value of the amplitude of the largest tone with distortion. SFDR is basically the measurement of fidelity of the circuit.

2.5 Summary

The various characteristics mentioned from section 2.2 to 2.4 form the basis of ADC design and the requirements can vary slightly for different applications. Some applications can focus more on static errors while for some, dynamic errors could play a vital role. Proper requirement analysis is the first step towards selecting the type of ADC which will be suitable for the particular application.

CHAPTER 3: Algorithmic ADC

3.1 Introduction

For neural recording applications, input signals are generally in the range of 0.1Hz to 10 kHz, so as per the Nyquist Criterion, Sampling rate would be around 20 KHz. As we can see speed is not a concern in our case, and the primary focus is on the complexity of the circuit design. From Table 2.1 we can see that medium speed ADCs will be a perfect fit for this sampling rate. I have considered Algorithmic type over SAR based ADC due to less complex circuit design of the former and a smaller number of capacitors, minimal dependency on the capacitor sizes and their non-ideal effects.

3.2 General Architecture

Algorithmic ADC works on the principle of switched capacitor charge transfer [Quinn, 2003]. Its operation is similar to SAR based ADC, with a major difference that instead of reducing the V_{ref} with every cycle as in case of SAR based ADC, an algorithmic ADC keeps the V_{ref} constant and rather multiplies the V_{err} by 2 using an X2 Gain Circuit [Carusone, 2012]. V_{err} is the voltage error value calculated by adding $-/+V_{ref}/4$ to the input voltage for every bit. In other words,

$$V_{err} = V_{in} + b_i * V_{ref}/4$$

where

V_{in} is the input to the ADC,

And b_i is decided as per the output of comparator.

When comparator output is 1 then b_i is -1, and

when comparator output is 0 then b_i is +1.

It is also similar in operation to pipelined ADC while having a simpler design which in turn saves die area and proves better in our case since speed is not a major concern.

Depending on the resolution of the ADC, i.e. based on the no of bits (N), it takes N cycles to produce the digital output word. The output of each cycle is taken back as input for the next cycle and after N cycles, a new sample input is taken in. The flow graph of an algorithmic ADC is shown in Fig. 3.1.

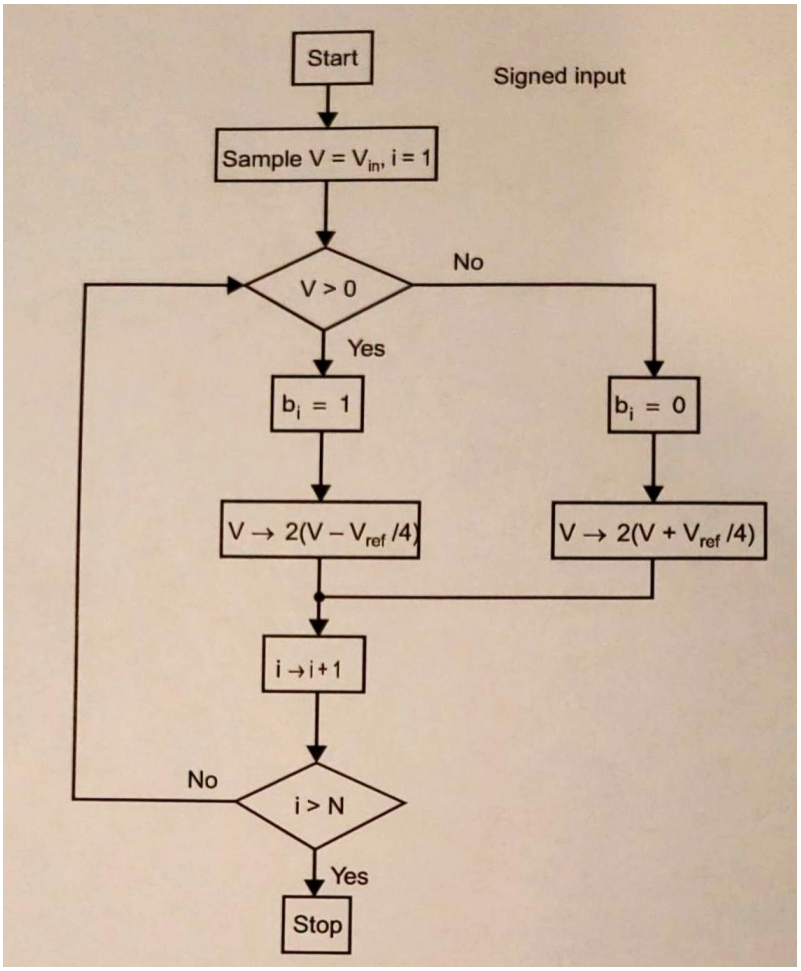

Fig. 3.1 Flow Graph of an algorithmic ADC [Carusone, 2012]

The analog input is compared with 0 volts, and it gives the output bit either 1 or 0 depending on it being positive or negative. Further $\frac{1}{4}$ V_{ref} is subtracted or added from or to it, respectively, and this value is passed to X2 gain circuit. The output is taken as input for the next cycle and this whole process is repeated for N times depending on the number of bits N, which is the resolution of the ADC. Fig. 3.2 shows the block diagram of an algorithmic ADC.

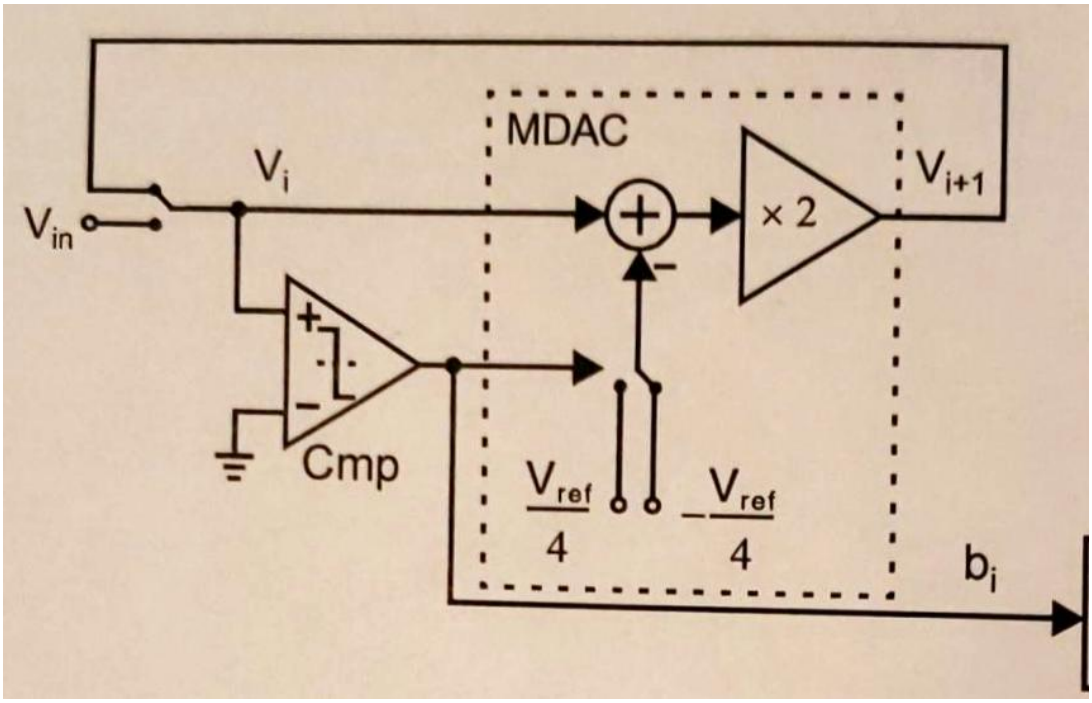

Fig. 3.2 Block Diagram of a Algorithmic ADC [Carusone, 2012]

As we can see, the same circuit is used for calculating all the bits spread in the time domain, the analog circuitry required is so far less as compared to SAR based ADC. Table 3.1 summarizes the reasons for selecting algorithmic ADC.

Advantages of Algorithmic ADC over SAR Based ADC		
S.No	**Algorithmic ADC**	**(SAR) Type ADC**
1	Independent of Capacitor's ratio and Op-Amp non-idealities	DAC and comparator need to be as accurate as the overall system
2	Low power consumption	Low sampling rates
3	High resolution and Accuracy	Accuracy dependent on Capacitors's ratio
4	Smaller form factor	Larger form factor

Table 3.1 Algorithmic ADC vs SAR based ADC

3.3 Major Challenges

The heart of this algorithmic ADC is the Multiply by two (X2) gain circuit since the precision of the ADC depends on the accuracy of the X2 gain circuit [Carusone, 2012].

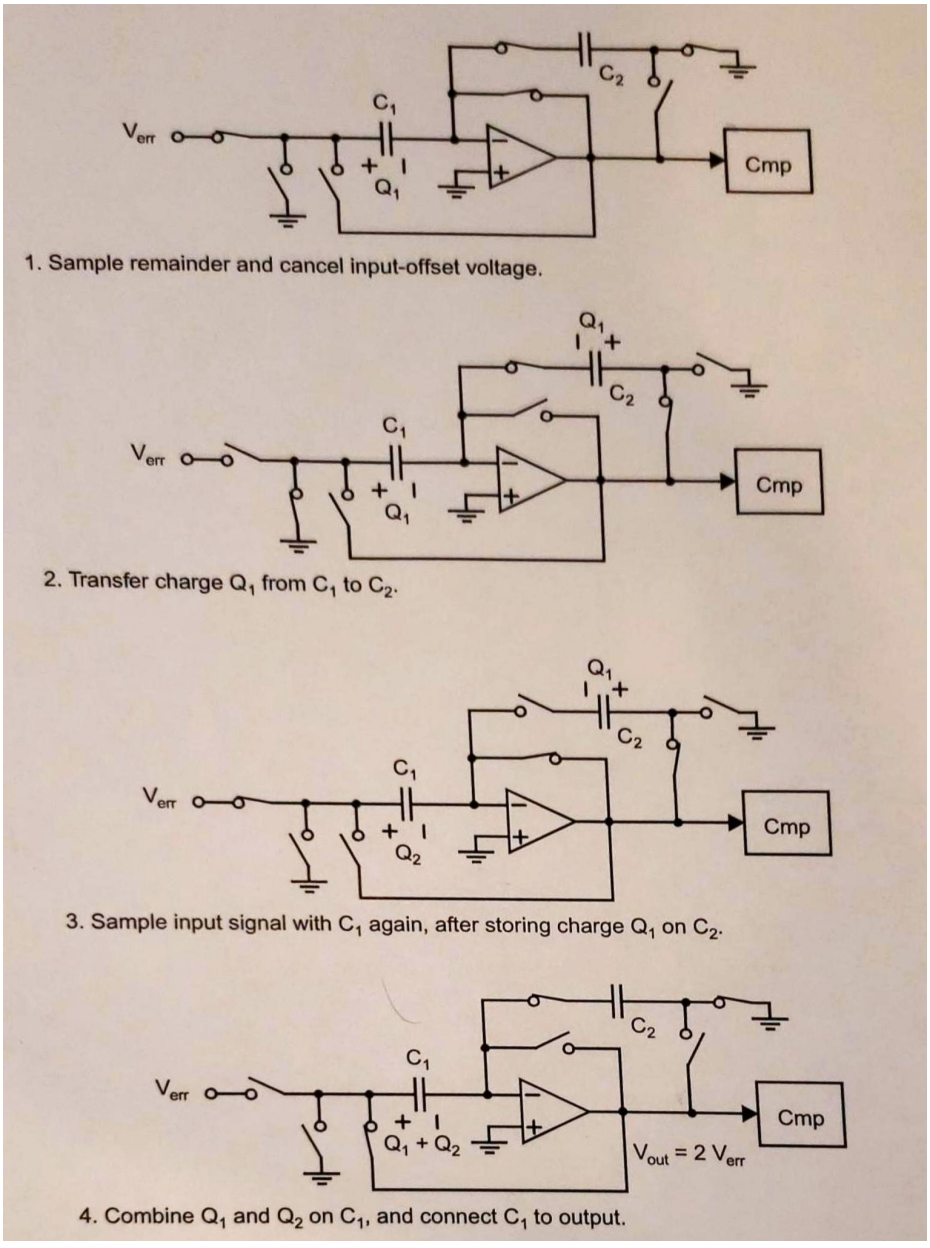

Fig. 3.3 X2 Gain Circuit [Carusone, 2012]

Fig. 3.2 shows the step wise approach of X2 gain circuit. As we can see, it consists of a high gain Op-Amp, a comparator which is basically an Op-Amp as well, two capacitors, and seven SPST switches. The goal of this circuit is to manipulate the charging/discharging of the capacitors and switching them accurately to make it independent of capacitor ratio and also accounting for the input offset errors of the Op-Amp [Zheng, 2000]. The Op-Amp with a high gain basically works continuously trying to keep both the inputs at the same level at all the time. This helps us to move the charges from C1 to C2 and vice versa. The non-inverting terminal of the Op-Amp is kept at ground, at all times. The first step is to take the V_{err} input and put it on the capacitor C1, allowing it enough time to completely charge C1, and since the SPST switch is in closed state, Op-Amp output is directly connected to inverting input terminal. Therefore, the two capacitors have different charges at this point. While capacitor C1 would have $C1(V_{err}-V_{off})$, where V_{off} is the input offset of the Op-Amp, C2 would have $C2(-V_{off})$. This is first clock cycle of the X2 Gain Circuit. Then, in second clock cycle this difference of charge is accumulated on capacitor C2. In third clock cycle, V_{err} is again taken in, and by the end of fourth clock cycle this charge is put back on C1 resulting in a voltage of $2V_{err} - V_{off}$. Hence, the output voltage is $2V_{err}$, thereby being independent of both capacitor values of C1 and C2 as well as Op-Amp input offset error, V_{off} [Carusone, 2012].

The Comparator Op-Amp ensures that we get rail to rail output for each of the input which is basically a digital 0 or 1 since the inverting input is always kept at ground.

As shown in Fig 3.2, First of all, Analog input is taken in, compared to 0 volts using a comparator, and $\frac{1}{4}$ V_{ref} is added or subtracted accordingly using an analog adder, which gives us V_{err}. This is the input to X2 gain circuit and the multiplication by 2 is performed in 4 clock cycles. It is important to note that this clock cycle is different from the one mentioned earlier for the generation of each output bit.

In the first step, capacitor C_1 is charged with Q_1 due to input V_{err} which is transferred to capacitor C_2 in step 2. Then, Capacitor C1 is again charged with Q_2 in step 3 and finally in step 4, Q_1 and Q_2 is combined on C_1 and it gives the output as $2V_{err}$.

7 SPST switches are used to implement this logic in 4 steps.

It can be mathematically derived that the output is independent of the size or ratio of the two capacitors. It is also independent of the input-offset voltage [Carusone, 2012]. Manipulating the charging and discharging of capacitors along with accurate switching is critical and something which requires numerous iterations in Cadence to arrive at the optimal accuracy of the design. It is important to note that getting the X2 gain circuit to work is quite challenging due to the oscillations encountered because of using the capacitors and is also indicated in the book [Carusone, 2012] and even IEEE Papers like [Quinn, 2003].

CHAPTER 4: Circuit Level Design

4.1 Algorithmic ADC

The circuit design is done on Cadence platform (Cadence EDA: IC 6.1.7 (Virtuoso) & Spectre simulation tool) using IBM/Global Foundries 8HP 130nm BiCMOS technology. Fig. 4.1 shows the overall block diagram for 5-bit algorithmic ADC.

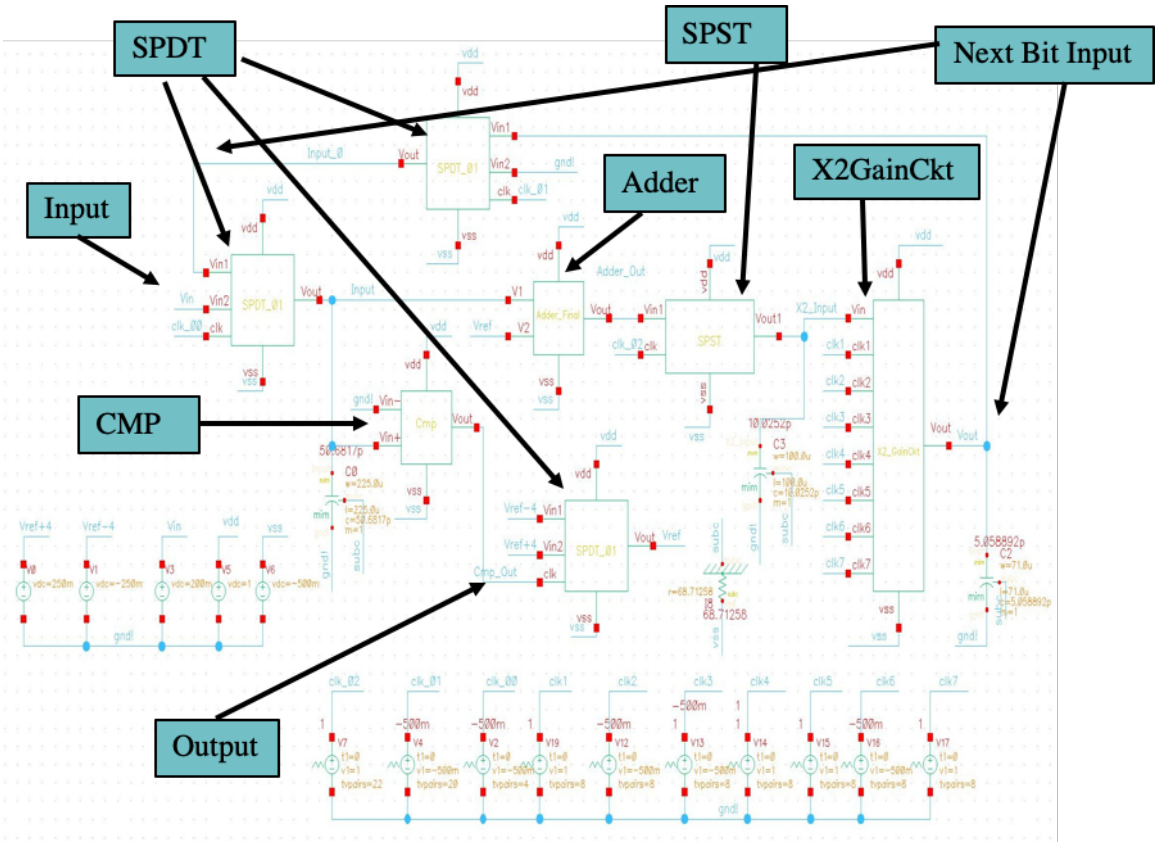

Fig. 4.1 Overall Circuit Diagram for an Algorithmic ADC

Its building blocks consists of

- a comparator,
- an analog adder,
- an X2 gain circuit and

- Switches (SPDT & SPST).

The neuro Signal measured from Electrode Array is a very weak signal ranging from 100μV to 1mV at max. Therefore, as a first step we need amplification of the signal for which it is passed through a Pre-Amplifier and the output is fed as an input to the ADC. The pre-amplifier gives an output in the range of 100mV and is suitable for the processing through algorithmic ADC designed. The comparator then gives the digital bit output and tells us whether to add or subtract $V_{ref}/4$ to the input signal. Analog adder then performs the arithmetic function and its output is fed as an input to the X2 gain circuit. The switches carry out the digital logic part of the circuit and based on the resolution, this ADC generates the final digital word output.

Each component of the circuit is covered in detail in the following sections.

4.2 Pre-Amplifier

The pre-amplifier circuit is the first building block of the circuit designed in this work. A very low power, high gain and minimum input offset Op-Amp is designed for this purpose [Johns, 1997]. Fig. 4.2 shows the cadence generated circuit diagram.

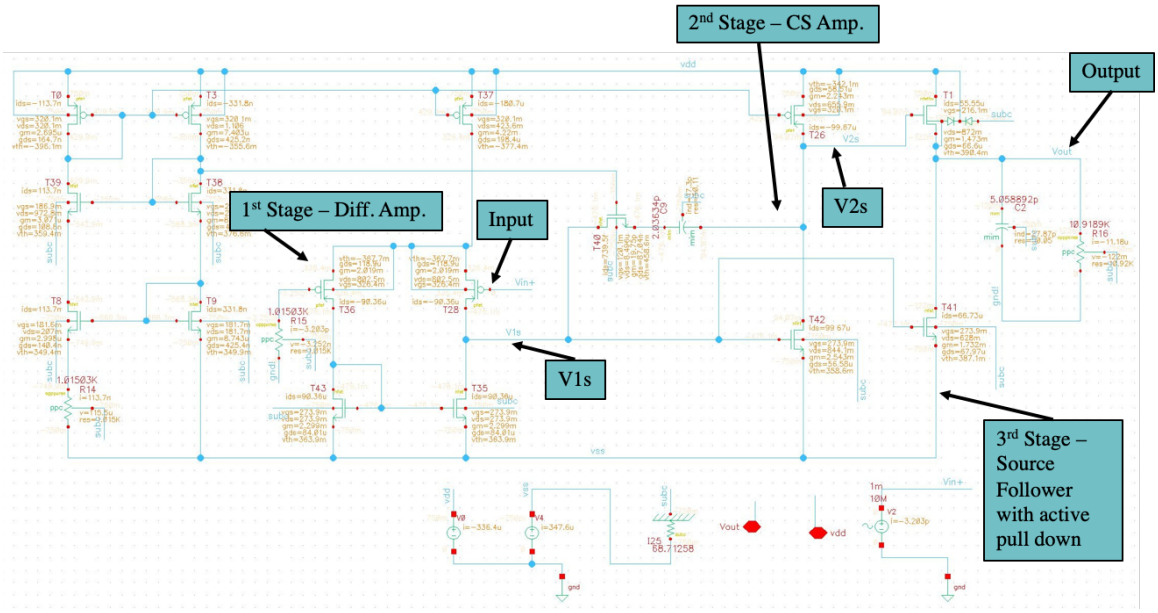

Fig. 4.2 Pre-Amplifier Circuit Diagram

It is a three stage Operational Amplifier with a dedicated bias circuit. PMOS transistors are used in Differential amplifier (1st Stage) with NMOS current mirror to maximize the slew rate. At the same power dissipation level and in turn bias current, PMOS has higher V_{eff} (V_{GS} - V_{th}) than NMOS [Johns, 1997]. Having a higher slew rate helps increase the range of incoming input signals and makes the circuit useful over a wider range of input signals. Next Stage (2nd Stage) is a common source amplifier stage with a PMOS active load to increase the overall gain of

the amplifier. Miller's capacitor along with an NMOS resistor is used between Input and Output of this stage to improve the stability of the circuit and reduce oscillations. The third stage is a source follower stage also known as unity gain buffer stage with active pull down. Vdd = 1V and Vss = -0.5 V is used for all the circuits in this work.

Fig.4.3 shows the transient simulation results for the Pre-Amplifier.

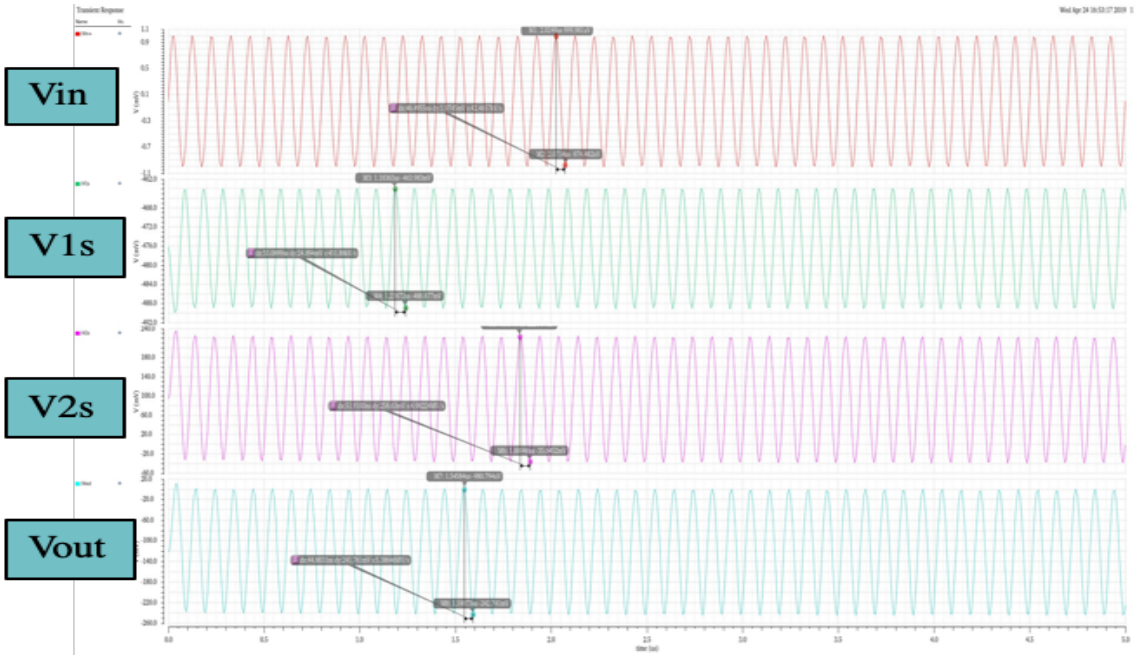

Fig. 4.3 Transient Simulation results for each stage of Pre-Amplifier

Vin+ is the input to the pre-amplifier. V1s is the output of the differential amplifier (first) stage has a gain of 22 dB. V2s represents the output of common source amplifier(second) stage and is around 20.33 dB. Vout is the final voltage output and the gain of third stage is -0.59 dB. The total simulated transient voltage gain achieved is 41.78 dB and is shown in Table 4.1 below.

Unit	mV	mV	mV	mV	dB	dB	dB	dB
Variable	Vin+	V1s	V2s	Vout	1st Stage Gain	2nd Stage Gain	3rd Stage Gain	Total Gain
Value	1.97	24.89	258.63	241.76	22.03	20.33	-0.59	41.78

Table 4.1 Voltage Gain Calculation for the Pre-Amplifier

The transistor widths considered vary but the length is kept constant at 120nm. Minimum number of fingers and multiplicity is used in the design. Sub-threshold operation techniques are utilized to bring down the total power consumption. Total power dissipated is 0.9 mW.

Fig. 4.4 AC Analysis of Pre-Amplifier Circuit

Further AC analysis of the circuit gives us an AC gain of 45.9 dB. Unity gain frequency comes out to be 223.6 MHz and -3dB frequency of the circuit is 8.29 MHz. Fig. 4.4 shows the AC gain, unity gain frequency and -3dB frequency of the Pre-Amplifier.

4.3 Comparator

An efficient comparator with very low input offset is important to get the correct output bit as well as to decide whether $\frac{1}{4}$ V_{ref} is to be added or subtracted.

$V(k+1) = 2*\{V(k) + b(k)*V_{ref}/4\}$ [Zheng, 2000]

Where V(k+1) = next voltage input, V(k) = previous voltage input, and

B(k) = previous digital bit

The inverting terminal of the comparator Op-Amp is always kept at ground and the input is applied to the non-inverting terminal. Rail to Rail swing design is implemented to get a perfect 0 or 1. Input offset is reduced to μV by running numerous simulations to avoid any additional loading of the input signal. MIM capacitors are used everywhere in this design. Substrate (subc) is configured at low resistance (68.7 Ω) to avoid leakage and feedback through substrate. Fig. 4.5 shows the circuit diagram of the comparator designed for this purpose.

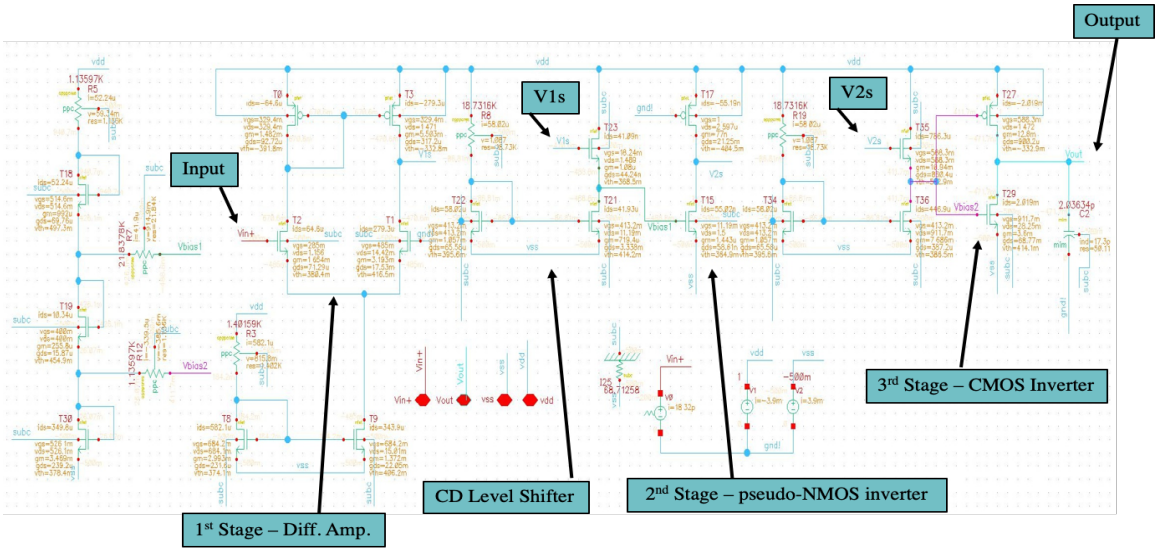

Fig. 4.5 Comparator Circuit Diagram

In this architecture, the first stage is an NMOS Differential amplifier with PMOS and NMOS current mirrors on top and bottom respectively along with single-ended output. Then, a common drain or source follower is used which acts as a level shifter to bring the signal dc level down for the next stage. The next stage is a pseudo-NMOS inverter to sharpen or improve the rise and fall time of transition followed by a level shifter and CMOS Inverter to provide a rail to rail output. Additional bias circuit is used to improve the biasing of inverters and in turn the accuracy of the comparator.

Fig. 4.6 shows the transient simulation results for the comparator.

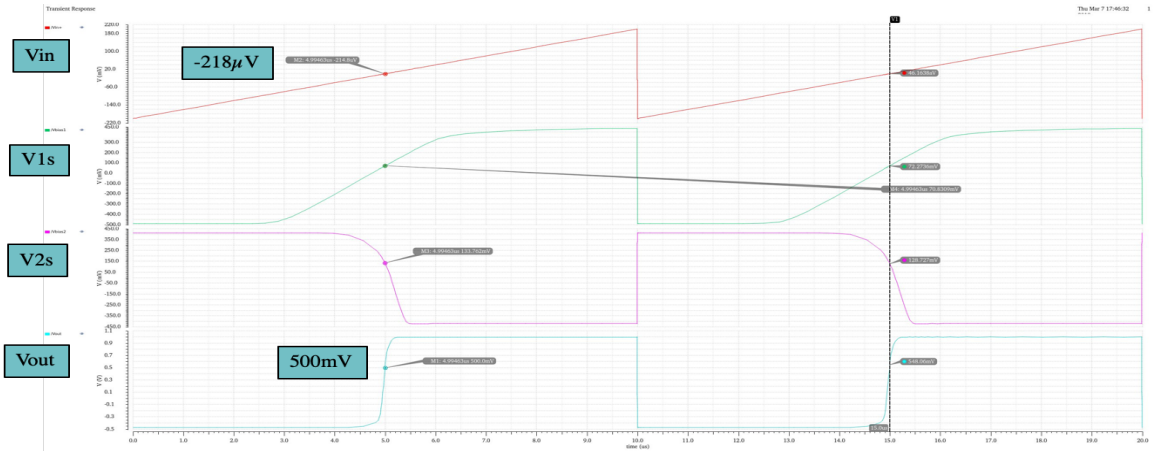

Fig. 4.6 Transient Simulation results for Comparator

A RAMP Input ranging from -200mV to +200mV is used to test the functionality of the designed comparator. For inputs from -200 mV up to 0V, the output is 0 and as soon as the input crosses 0V, the output quickly changes to 1. As we can see, the input offset is around -214.8 μV. Nodes V_{bias1} and V_{bias2} are the inputs to second and 3rd stage respectively and represent the intermediate behavior of the circuit.

4.4 Analog Adder

The analog adder is used to add or subtract $\frac{1}{4}$ V_{ref} to the input voltage as per the comparator output. Fig. 4.7 shows the circuit diagram of the analog adder.

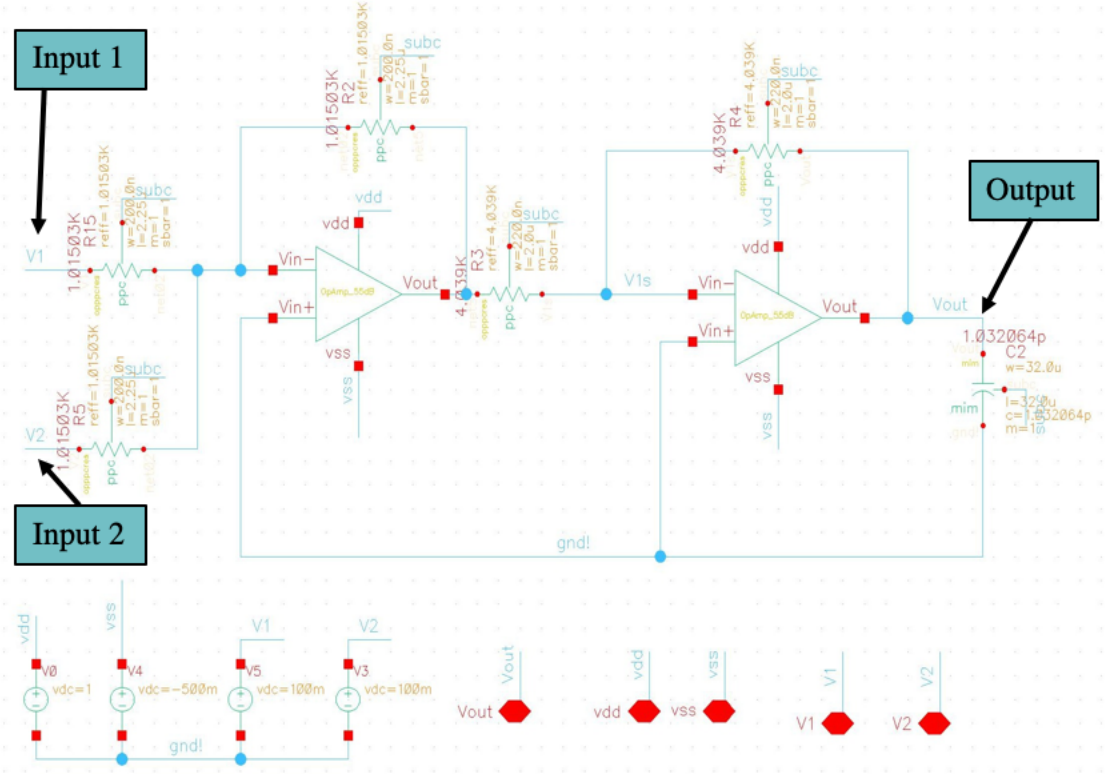

Fig. 4.7 Analog Adder Circuit Diagram

Two analog inputs are fed to the inverting terminal of the Op-Amp through resistors. The ratio of resistor (R5 and R15) sizes determines the addition. Since both resistors are of the same value, the actual values of input are added together. Since, this circuit inherently behaves as an adder and can't perform the operation of subtraction, two separate dc sources are required to provide positive and negative voltages equivalent to +/-V_{ref}/4. These two dc sources are

to be a part of power planning when fabricating the chip and proper attention will be needed to ensure the availability of the same on the chip for accurate functionality of this adder. Now, since the output is inverted, a unity gain buffer is used as an analog inverter to get the output with correct phase. The same high gain Op-Amp is used in unity gain buffer stage as well.

A very high voltage gain (around 55dB) Operational Amplifier (Op-Amp) is used as a building block for this analog adder. The Op-Amp is the same which is designed for the X2 gain circuit and is described in detail in the next section. The only difference is that the Miller capacitor has a value of 2pF. Fig. 4.8 shows the Op-Amp Circuit.

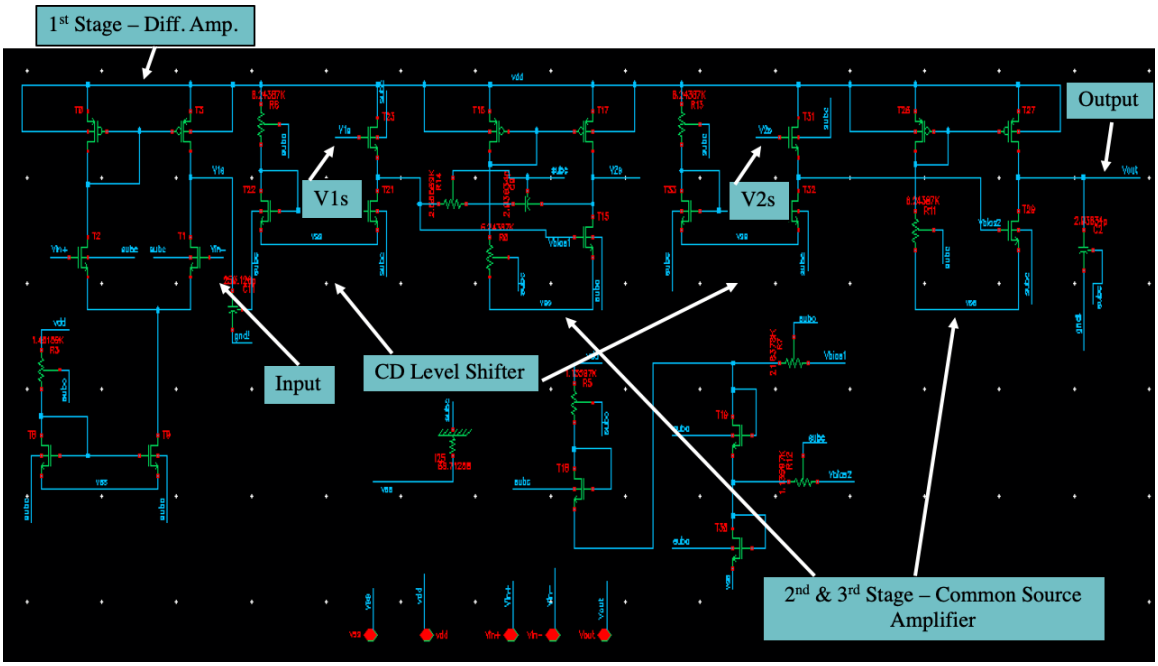

Fig. 4.8 OpAmp_55dB Circuit Diagram

Various simulations were performed to test and confirm the accurate operation of analog adder.

Fig. 4.9 shows the simulation result establishing the functionality of analog adder.

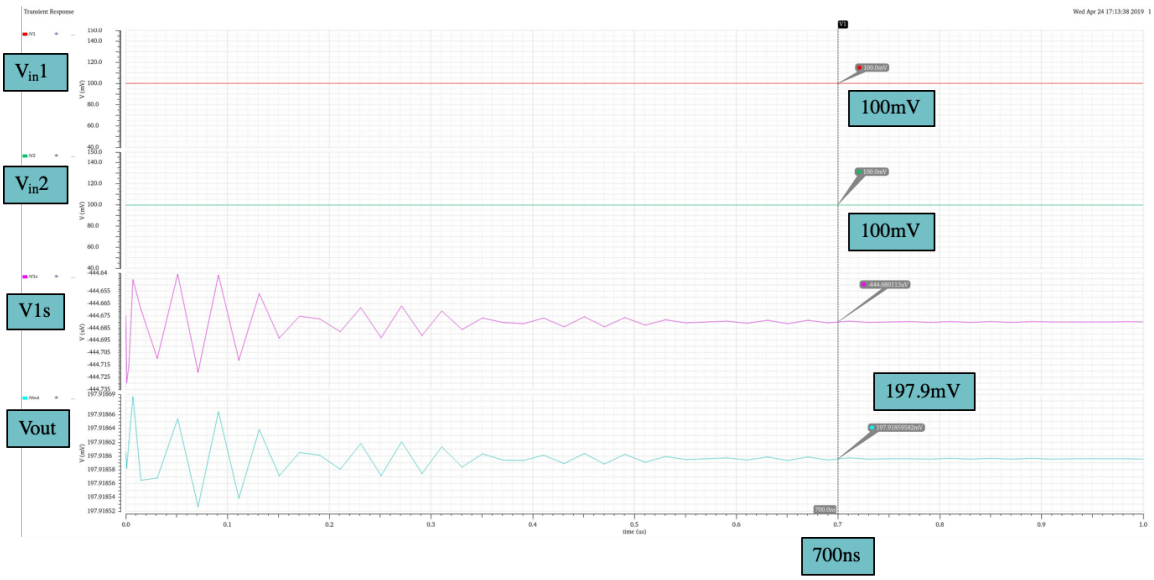

Fig. 4.9 Simulation results for Analog Adder.

For two inputs of 100 mV each, we get an output of 197.9 mV which is correct with only 1% error. As we can see from the above diagram the adder takes around 0.7μs to stabilize the final output, the clock cycle is chosen accordingly as we will see in Chapter 5.

4.5 X2 Gain Circuit

X2 Gain circuit is the most important element of the ADC design. Fig. 4.10 shows the circuit diagram.

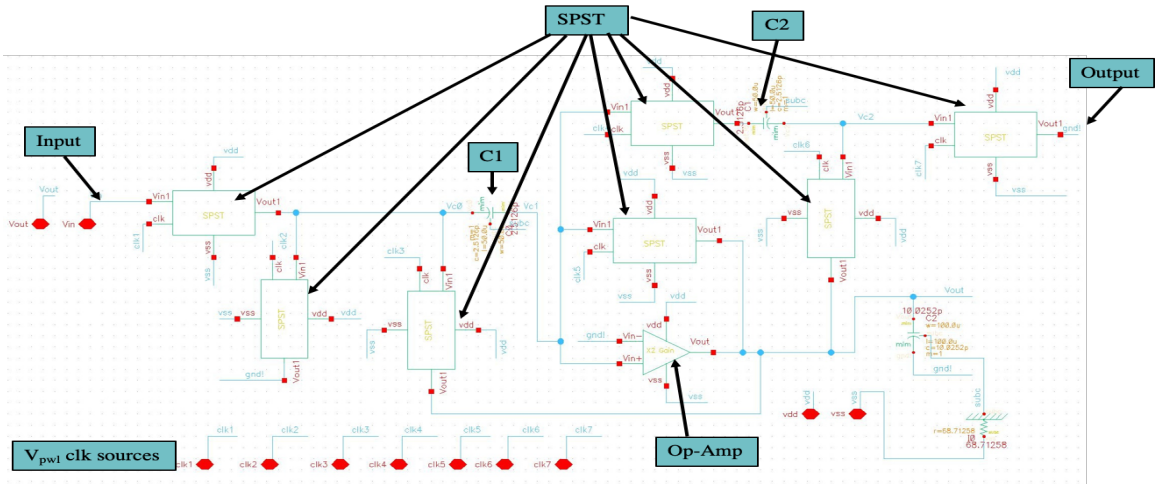

Fig. 4.10 X2 Gain Circuit Diagram

As we have seen in section 3.3, SPSTs divide the whole process in 4 cycles and the respective step goals are achieved by turning these switches on or off.

Fig. 4.11 shows the clock cycles pattern used to achieve the X2 gain.

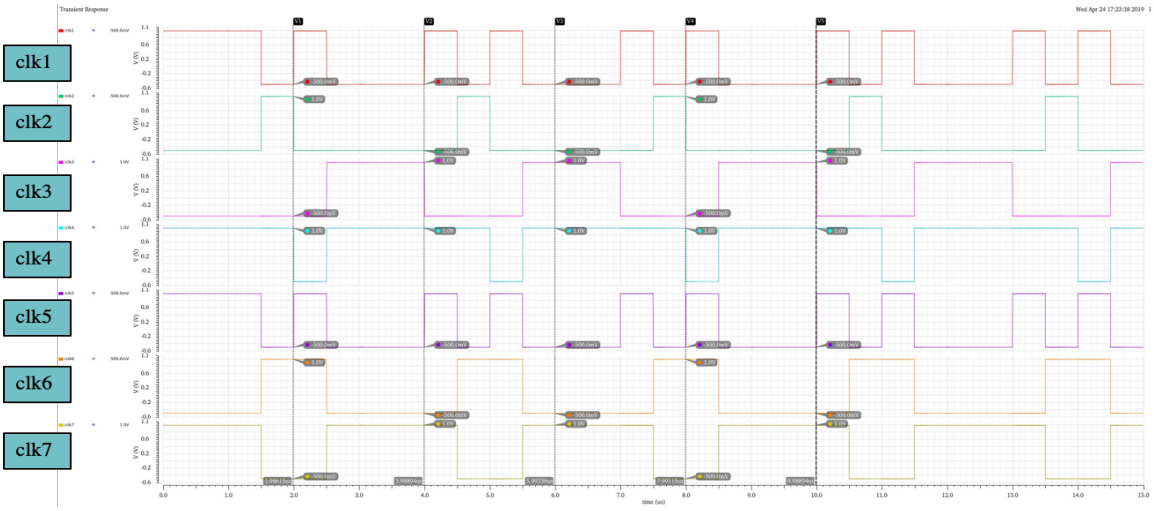

Fig. 4.11 Clock Cycles for X2 Gain Circuit

First and foremost, most important requirement of this design was a high gain Op-Amp to ensure that both inverting and non-inverting terminals are almost at the same potential or virtual ground in our case since the non-inverting terminal is always kept at ground potential.

Fig. 4.12 shows the Op-Amp circuit designed. As mentioned earlier vdd = 1V and vss = -0.5V is used everywhere, thereby providing a 1.5V as DC power supply. The first stage is an NMOS differential amplifier stage with PMOS current mirror at the top and NMOS current mirror at the bottom. The second and third stages are Common Source (CS) amplifier stages with active load and PMOS current mirror, to achieve high voltage gain.

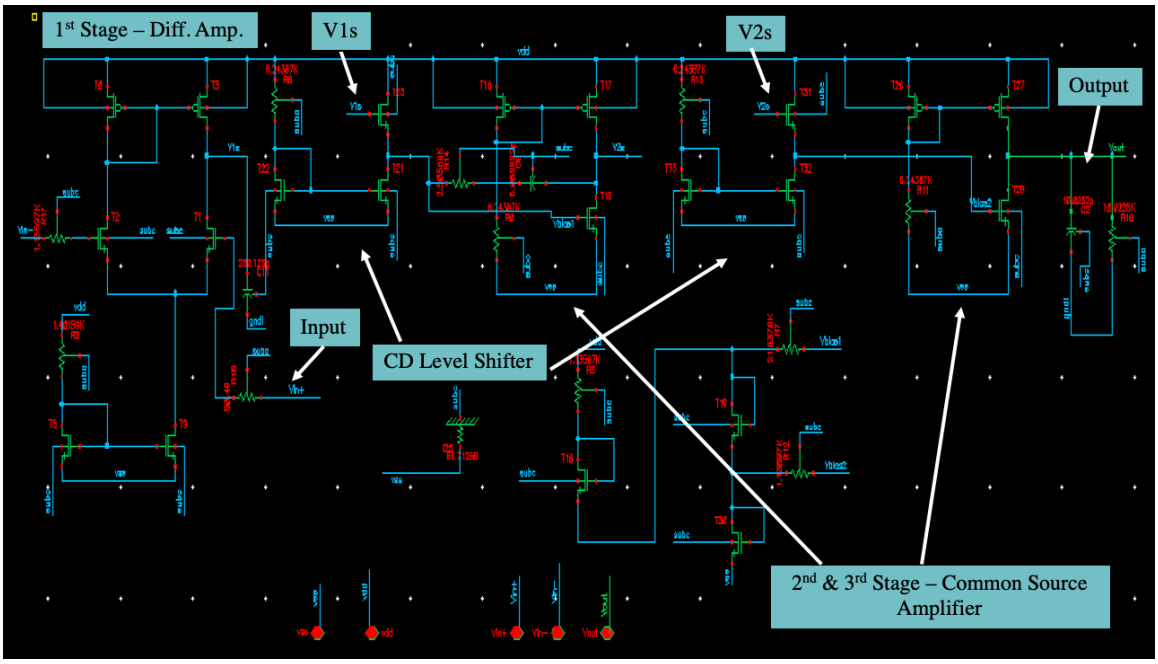

Fig. 4.12 X2 Gain Op-Amp Circuit Diagram

The second and third stages are Common Source (CS) amplifier stages with active load and PMOS current mirror, to achieve high voltage gain. The proper biasing

of common source amplifier NMOS transistor is critical for optimal performance of the amplifier stage at minimum dc power consumption. The output of first stage comes out to be very high at around 900mV and a voltage level shifter is used to bring down the voltage to a logical range for optimal operation and biasing of next stage amplifier. A voltage level shifter is nothing but a common drain amplifier or source follower with active load and NMOS current mirror and it immensely helps in biasing the circuit properly by bringing down the voltage level of first stage output from 900mV approx. to 400mV level. The final simulated transient voltage gain achieved was 49.62 dB and presented in the table 4.2 below.

Unit	mV	mV	mV	mV	dB	dB	dB	dB
Variable	Vin+	V1s	V2s	Vout	1st Stage Gain	2nd Stage Gain	3rd Stage Gain	Total Gain
Value	1.97	9.54	78.23	597.40	13.68	18.28	17.66	49.62

Table 4.2 DC Gain of X2 Gain Op-Amp Circuit

Fig. 4.13 shows the transient analysis results

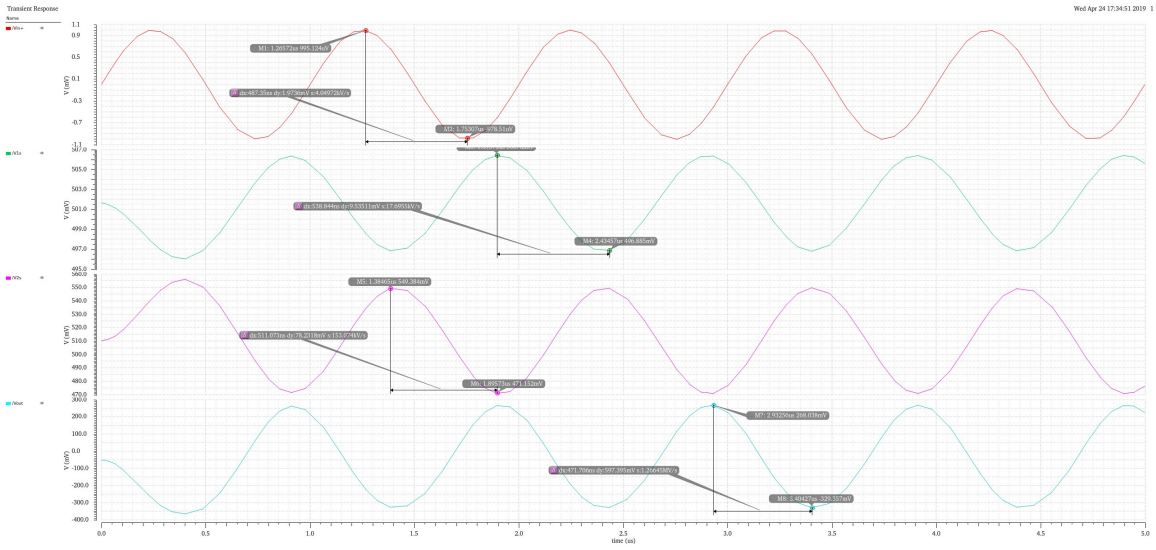

Fig. 4.13 Transient analysis result for X2 Gain Circuit Op-Amp

This Op-Amp when plugged in the X2 gain circuit, would not give an accurate multiplication by 2 output if the capacitor C1 is not given enough time to charge and transfer the charge to C2. Therefore, the clock cycles are designed in a way to provide enough time to capacitors to perform charging and discharging completely. Miller's capacitor and a resistor combination is hooked up between input and output of second stage [Johns, 1997], to improve the stability.

Miller's Theorem states that when a capacitor is added between input and output of a typical 2 or more poles system, it is equivalent to as if we add 2 capacitors, one at input and the other at output. It pushes the first pole or dominant pole of the system to a lower frequency and the other pole to a much higher frequency. This phenomenon is also referred as pole splitting. Further, adding an appropriate resistor in series with Miller's capacitor helps in moving the zero of the system to almost same frequency as 2^{nd} pole which nullifies the effect of 2^{nd} pole when gain is high as we can see in the Fig. 4.14 below. Therefore, the overall phase margin is improved thereby improving the overall stability. Although, the resistor along parasitic capacitances of directly connected transistors gives rise to a third pole, but normally if the resistor is not too big, and considering the fact that parasitic capacitors don't have a very large value, this doesn't hurt the phase margin of the system.

Further, a load capacitor is added at the output of first stage. This improves the phase margin of the Op-Amp Circuit and in turn the stability of the circuit. Fig. 4.14 shows the AC analysis results.

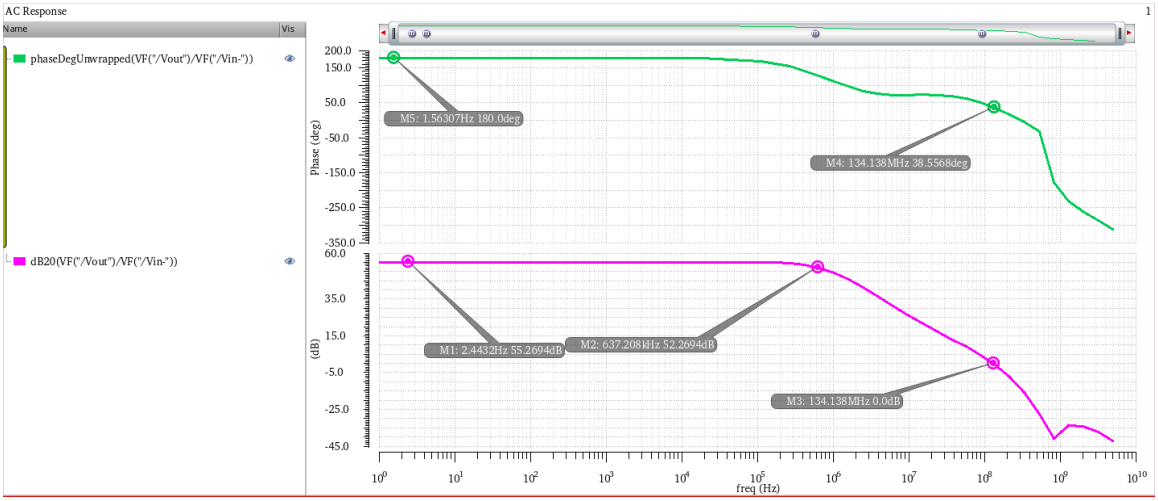

Fig. 4.14 AC analysis result for X2 Gain Circuit Op-Amp

As we can see, when gain reaches 0 dB at 132.664 MHz, called the Unity Gain Frequency of the OP-Amp, the phase angle is 38.6 degrees. It is to be noted that initial phase is 180 degrees. Therefore, the phase margin of the Op-Amp is 38.6 degrees. Phase margin is defined as the phase angle left at unity gain frequency before the phase changes it's value by 180 degrees and in turn becomes a positive feedback circuit from a negative feedback circuit, which gives rises to instability due to large oscillations in case of positive feedback.

Finally, after tweaking the values of components, X2 gain was achieved for various values of inputs with marginal errors. Fig. 4.15 shows the transient analysis outputs of X2 Gain Circuit for a RAMP Input.

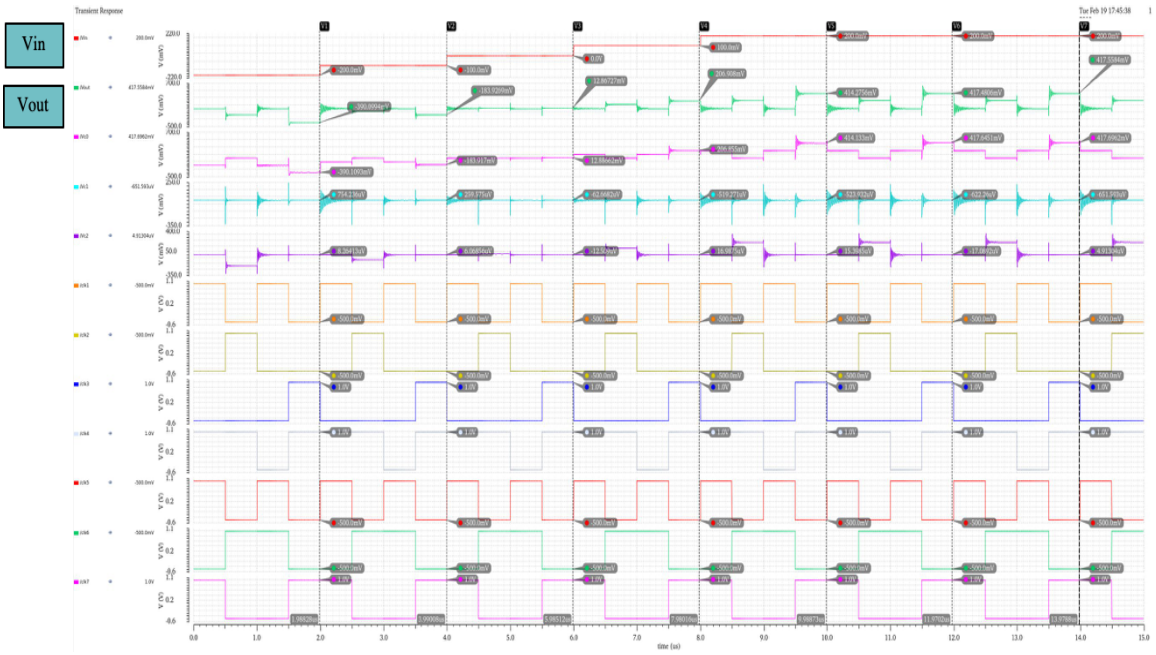

Fig. 4.15 Transient analysis results of X2 Gain Circuit

As we can see, for various inputs ranging from -200mV to +200mV the output is correct with an error less than 9%.

4.6 Transmission Gate Switches (SPST/SPDT)

Transmission gate switches play a vital role in the operation of the ADC circuit and their switching time with optimal accuracy is key to the overall design. In plain MOS switches bulk is generally connected to the source terminal. While NMOS switch passes a strong 0 and weak 1, PMOS switch passes a weak 0 and strong 1. Also, the gate to source voltage (V_{GS}) required in case of NMOS switch is supposed to be more than the threshold voltage (V_{th}) for it to work properly as a switch and just the reverse in case of PMOS switch i.e. $V_{GS} < V_{th}$.

However, a transmission gate utilizes both NMOS and PMOS transistor properties to provide a strong 0 and 1. The source and drain of both NMOS and PMOS are connected together. The gates of these transistors are connected together via an inverter to which the control voltage is applied to turn the switch ON or OFF. At a given point of time, both PMOS or NMOS transmitters are either turned ON or OFF. The substrate of PMOS is connected to vdd and the substrate of NMOS is connected to subc which is in turn connected to vss.

Therefore, for better accuracy, transmission gate switches are used in this work. Two types of switches have been incorporated in our design.

SPST – For usage in Single Input Single Output cases, this type of switches includes a transmission gate and an inverter. Fig. 4.16 shows the circuit diagram of a SPST.

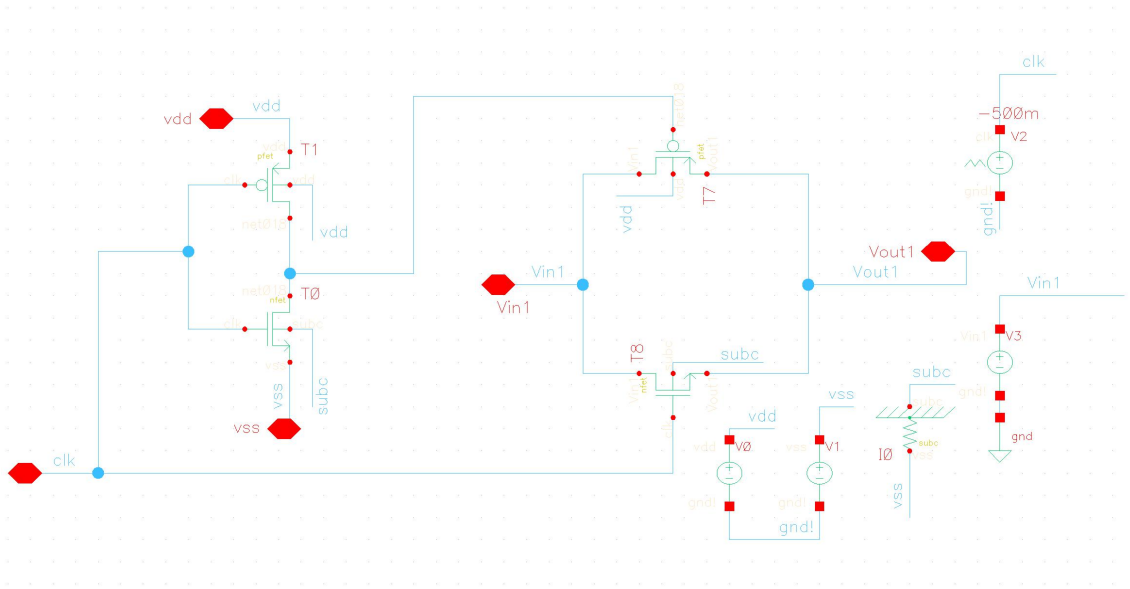

Fig. 4.16 Circuit Diagram of SPST

Transient simulations establish the proper functionality of the switch as illustrated in Fig. 4.17 below.

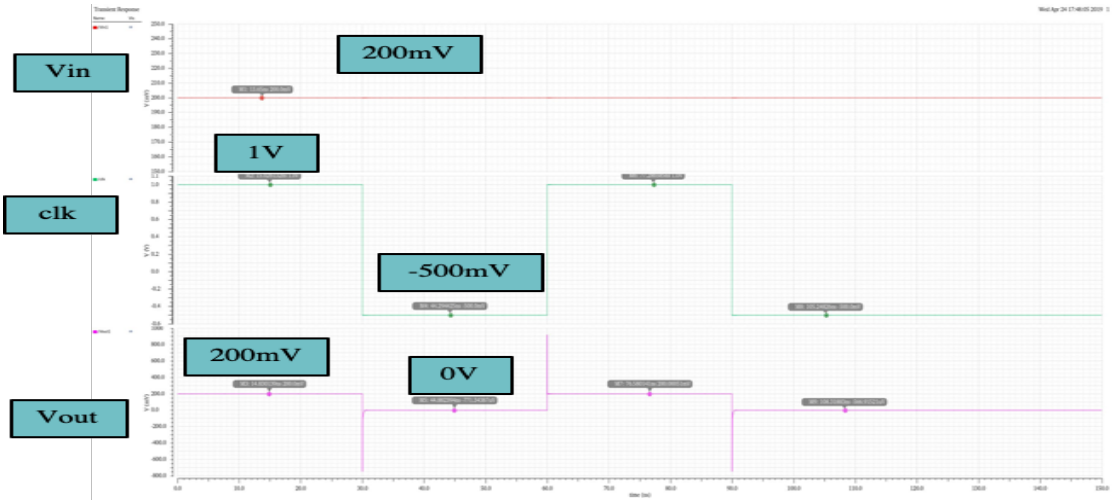

Fig. 4.17 Transient Simulation results of SPST

SPDT – For usage in 2 input and one output cases, this type of switches includes two transmission gates and one inverter. Fig. 4.18 shows the circuit diagram of a SPDT.

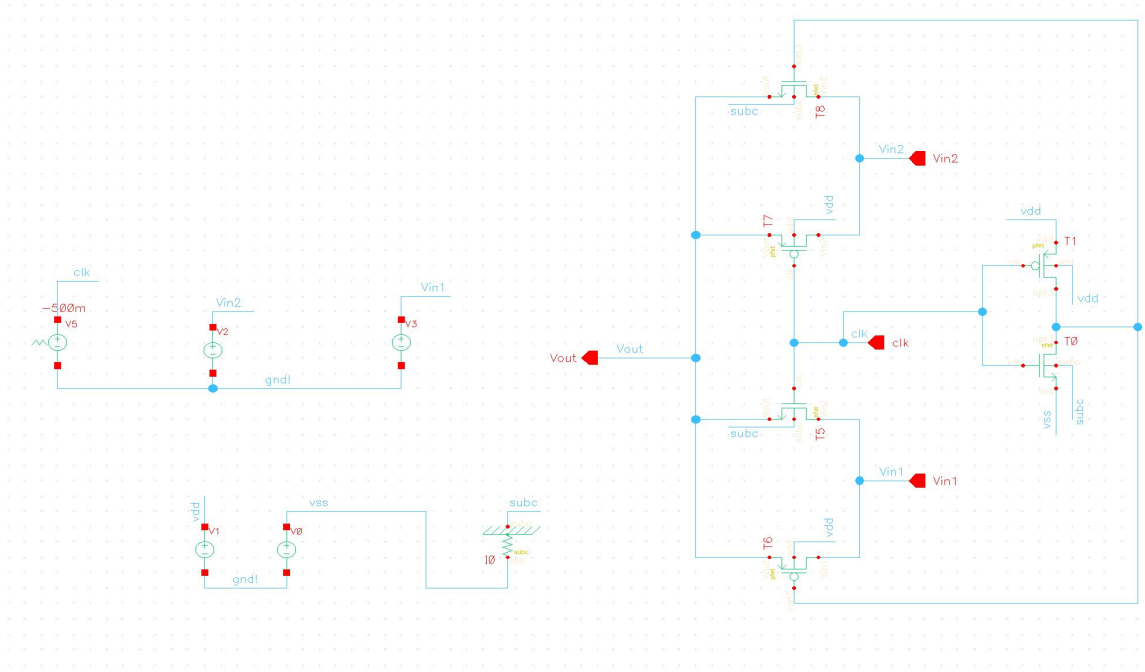

Fig. 4.18 Circuit Diagram of SPDT

Transient simulations establish the proper functionality of the switch as illustrated in Fig. 4.19 below.

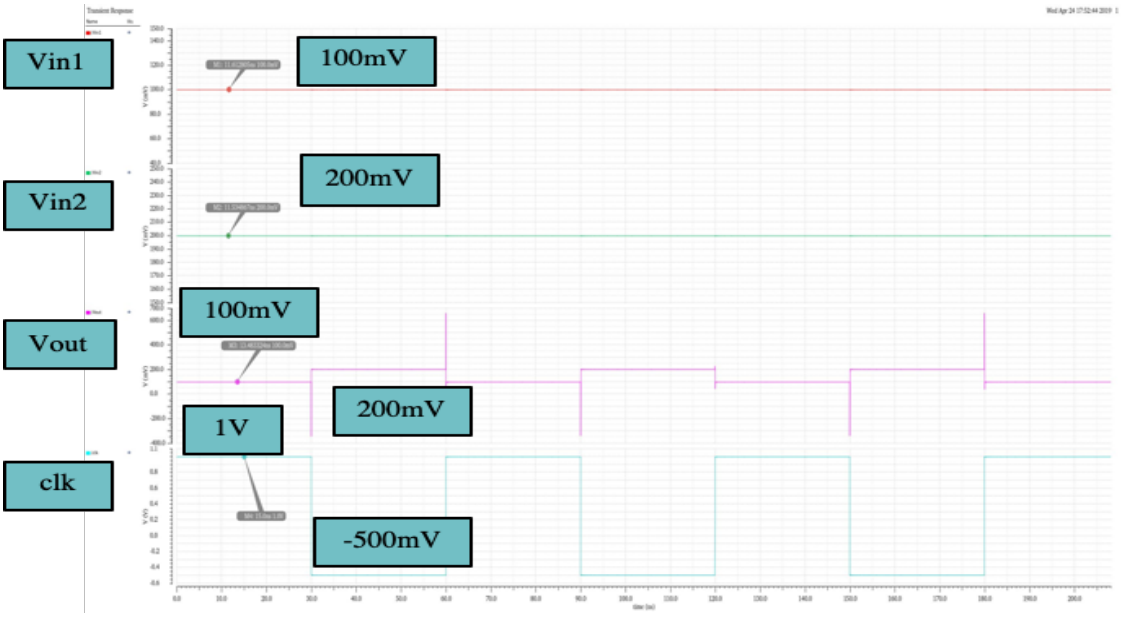

Fig. 4.19 Transient Simulation results of SPDT

CHAPTER 5. ADC Circuit Simulations & Results

5.1 Simulations

After designing and testing all the components of the algorithmic ADC individually, the whole circuit was assembled together for final simulations and optimization. Fig. 5.1 shows the overall ADC circuit.

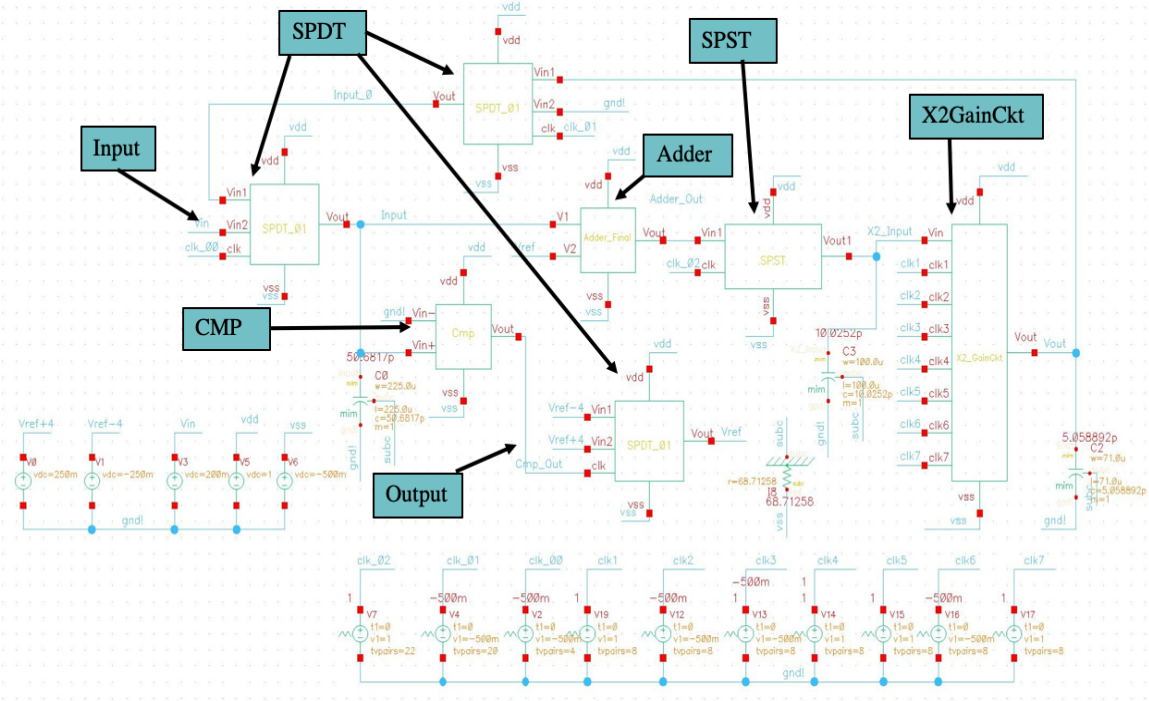

Fig. 5.1 Overall ADC Circuit

The input signal is taken through SPDT (clk_00) and stored on the capacitor to keep it stable. This signal is fed to the comparator and depending on the output of comparator $V_{ref}/4$ is accordingly added or subtracted to this input signal. This part of the process takes around 1µs. Therefore, 1st bit output requires only 1µs. Now the adder output is passed through a SPST (clk_02) switch and fed to X2 gain circuit. A capacitor is used here to keep the Adder output stable. X2 gain circuit

has 4 clock cycles of 500ns each, thereby requiring 2µs. The output of X2 gain circuit is then passed through a SPDT (clk_01) and fed back to the comparator again in a cyclic manner via SPDT (clk_00). Since our ADC has a resolution of 5 bits, for next 4 bits, 1 µs is required for the operation of comparator and analog adder and 2µs (500ns clock cycle for each stage) for the operation of X2 gain circuit. A total of 13µs is required for 5-bit digital output for each analog input. Therefore, the conversion time of the circuit is 13us. Fig 5.2 to 5.4 illustrate the 5 Bit output of the algorithmic ADC for various input signals.

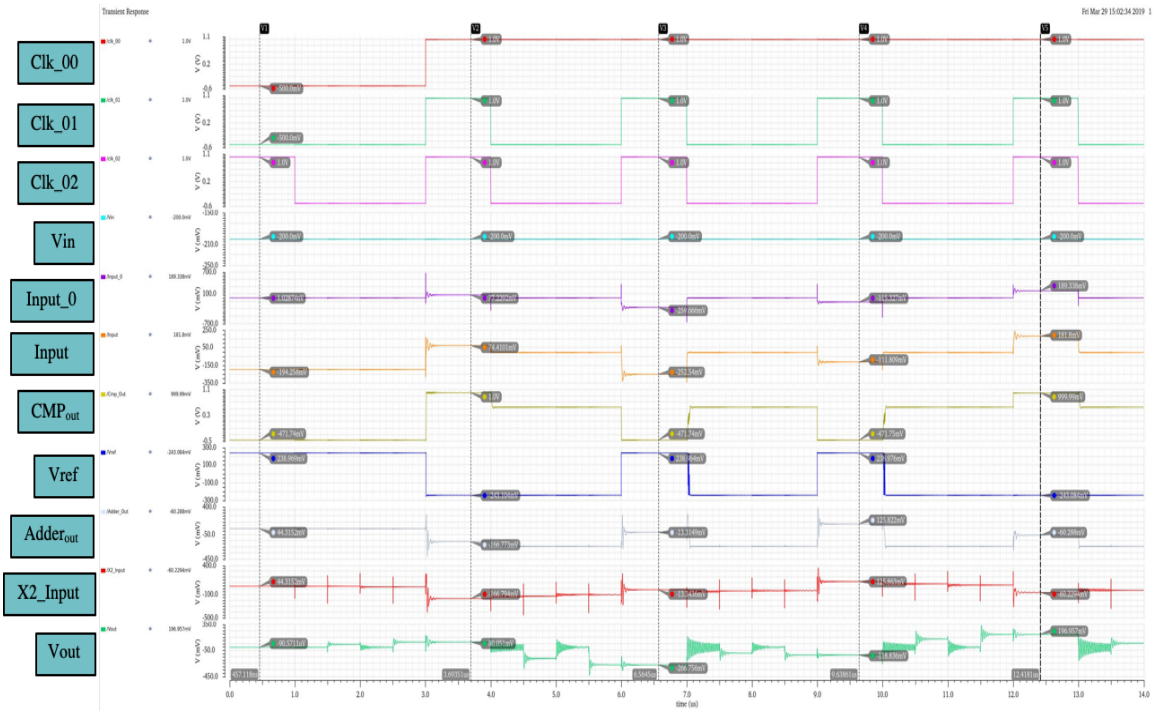

Fig. 5.2 Transient Plot for -200mV Input_01001 Output

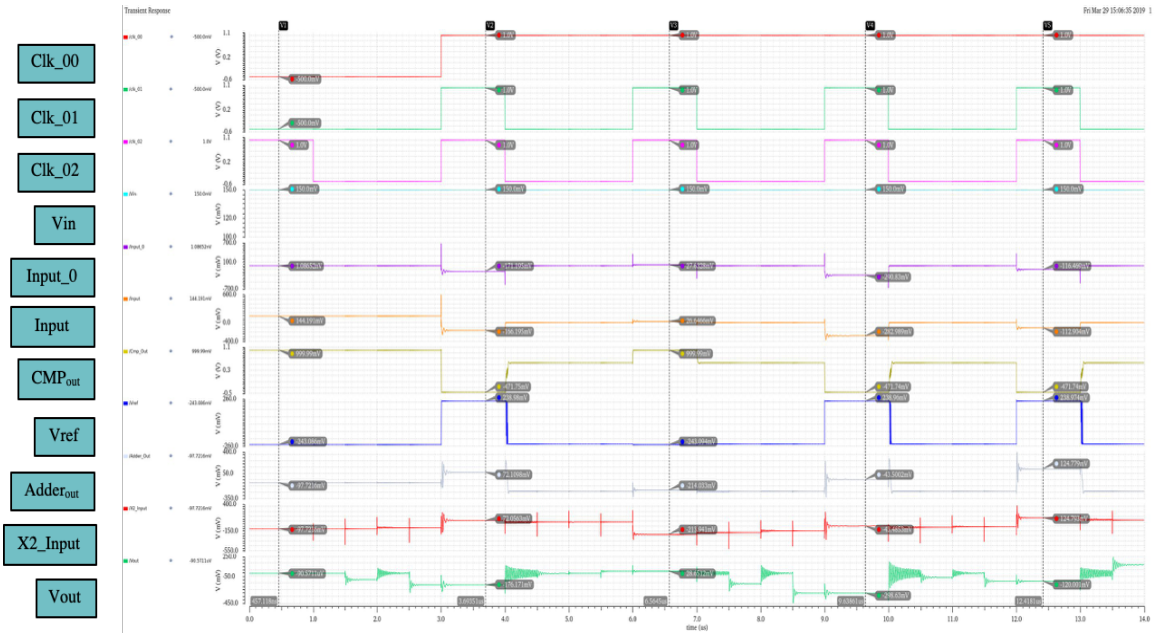

Fig. 5.3 Transient Plot for 150mV Input_10100 Output

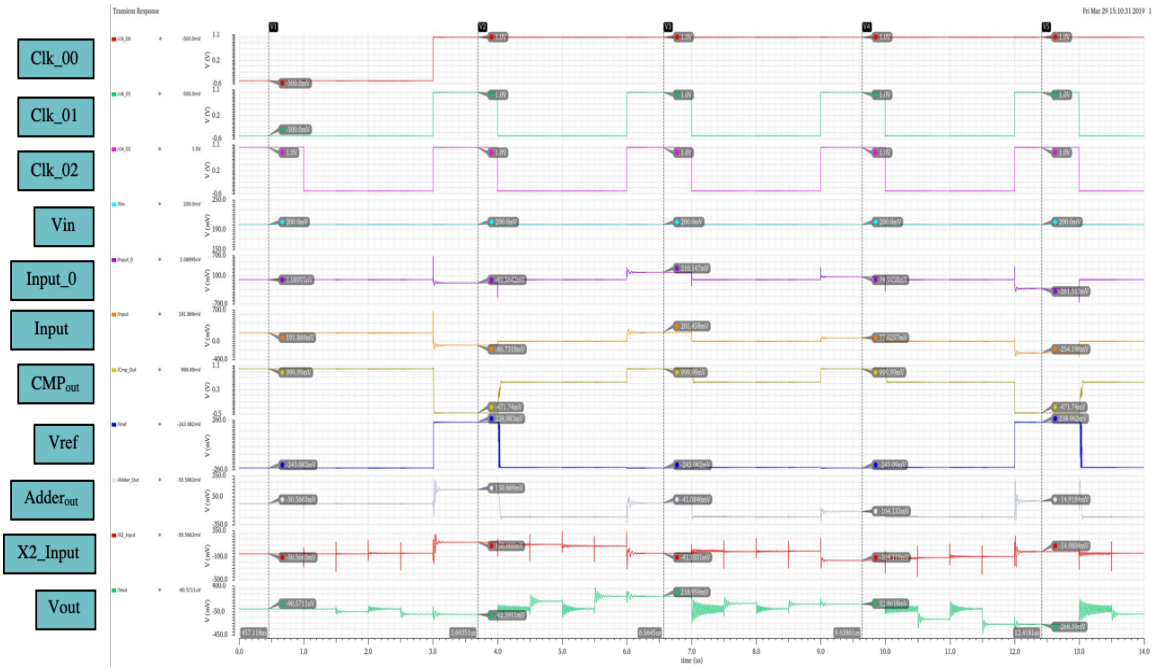

Fig. 5.4 Transient Plot for 200mV Input_10110 Output

5.2 Results

In the above simulations, bit output is depicted by comparator output as mentioned earlier. We can see that the output is correct for each input.

Table 5.1 summarizes the Input output behavior required and achieved.

S.No	Input	1st Bit	Vout1	2nd Bit	Vout2	3rd Bit	Vout3	4th Bit	Vout4	5th Bit	Output	Remarks
1	-200	0	100	1	-300	0	-100	0	300	1	01001	all bits correct
2	150	1	-200	0	100	1	-300	0	-100	0	10100	all bits correct
3	200	1	-100	0	300	1	100	1	-300	0	10110	all bits correct

Table 5.1 Analog Input and Digital 5Bit Output Log

The ADC was tested with DC input values ranging from -250mV to 250 mV. The overall dc power consumption is around 90mW. Table 5.2 provides a summary of performance parameters.

Performance Characteristics			
S. No	**Description**	**Values**	**Remarks**
1	Process Technology	130 nm	
2	Input Frequency	10 kHz	
3	Sampling Rate	20 Ksps	
3	Conversion Time	13us	
4	Input Range	"-250mV to +250mV"	
5	Resolution	5-bits	
6	Reference Voltage	1 V	
7	Power Supply	1.5 V	
8	Power Consumption	90 mW @ 20 Ksps	

Table 5.2 Performance Characteristics

CHAPTER 6. Conclusion

6.1 Conclusion

Wireless neural recording applications basically involve capturing the neuron potential using an electrode/array and then processing that signal to study the behavior. The neuron potentials are very weak so a pre-amplifier plays a vital role for the further processing of the incoming signal. An ADC is the most crucial component of the neural recorder system which also has an RF transmitter for sending the digital signal to a wireless recorder receiver. In this work, the pre-amplifier and algorithmic ADC is designed in Cadence using the IBM/Global Foundries 8HP 130nm BiCMOS technology.

The schematic level circuit design has been successfully completed and the performance parameters are illustrated. The pre-amplifier is working accurately as per the requirement with adequate gain of at least 40 dB at very low power (less than 1mW). The Comparator provides a rail to rail output with a very low offset value of -200μV. Analog Adder is working well with a marginal error of 1% in some cases but without affecting the digital bit output for all the tested cases. X2 gain circuit's functionality is tested exhaustively and the maximum error encountered is 9% in some of the cases which is within permissible limits since it is not affecting the digital bit output for all the tested cases.

The main goal of designing this algorithmic ADC was to simplify the design and remove the dependency on capacitor mismatching for medium speed requirement applications in contrast to SAR based ADCs where the number of

capacitor and dependency on the capacitor sizes is significant. Further, non-ideal effects of capacitors and Op-Amps is also nullified in this design. Die area reduction is achieved as well in this process due to very simple yet difficult to attain design. X2 gain circuit, the most critical element of this design is successfully working in turn ensuring the accuracy of the overall circuit. A 5 -Bit ADC is designed in this work. However, for industrial grade applications, a minimum of 8-10 Bit resolution is recommended.

CHAPTER 7. Future Work

7.1 Future Work

To make this ADC industrial grade, there are few areas where more work can be put in by analog design enthusiasts. A few suggestions are proposed for ready reference. While designing the X2 gain circuit, DC sources were used to provide the inputs for each bit output which are quite stable. On the other hand, when the whole circuit was put together, there was no dc source anymore to provide the input for each bit as the output of X2 gain circuit is fed as an input. To hold this charge, MIM Capacitors were used at comparator input as well as X2 gain circuit input. While the first capacitor holds the charge accurately and emulates an accurate dc source, the second capacitor at X2 gain circuit input does not. This capacitor needs to be bigger in size but doing so is resulting in oscillations and further analysis is needed to rectify this problem so that the resolution of the ADC could be increased to 8–10 bits.

Transient simulations still contain some oscillations which damp out with several hundred ns. Therefore, the ADC is giving 1-bit errors in some cases when we try to extend the input range. The oscillations need to eradicated by stopping the charge leakage between the capacitors. MIM capacitor's diode charge leakage could be the reason behind it. This is another area where more analysis can be done to improve the stability of the overall design for higher resolutions (8–10 bits).

Further, this algorithmic ADC can be hooked up with a low-power RF transmitter to provide 10mW output power into a 50Ω antenna at a frequency of 4GHz. On-off keying (OOK) can be used to modulate the RF transmitter, i.e. a "1" can be represented as full amplitude output RF signal while a "0" can be represented by a low amplitude RF output (or vice-versa). This will be a complete wireless neural recording transmitter solution except the neural electrode array.

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