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Methodology for Standby Leakage Power Reduction in Nanometer-Scale CMOS Circuits

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Abstract

In nanometer-scale CMOS technology, leakage power has become a major component of the total power dissipation due to the downscaling of threshold voltage and gate oxide thickness. The leakage power consumption has received even more attention by increasing demand for mobile devices. Since mobile devices spend a majority of their time in a standby mode, the leakage power savings in standby state is critical to extend battery lifetime. For this reason, low power has become a major factor in designing CMOS circuits.

In this dissertation, we propose a novel transistor reordering methodology for leakage reduction. Unlike previous technique, the proposed method provides exact reordering rules for minimum leakage formation by considering all leakage components. Thus, this method formulates an optimized structure for leakage reduction even in complex CMOS logic gate, and can be used in combination with other leakage reduction techniques to achieve further improvement.

We also propose a new standby leakage reduction methodology, leakage-aware body biasing, to overcome the shortcomings of a conventional Reverse Body Biasing (RBB) technique. The RBB technique has been used to reduce subthreshold leakage current. Therefore, this technique works well under subthreshold dominant region even though it has intrinsic structural drawbacks.

However, such drawbacks cannot be overlooked anymore since gate leakage has become comparable to subthreshold leakage in nanometer-scale region. In addition, BTBT leakage also increases with technology scaling due to the higher doping concentration applied in each process technology. In these circumstances, the objective of leakage minimization is not a single leakage source but the overall leakage sources. The proposed leakage-aware body biasing technique, unlike conventional RBB technique, considers all major leakage sources to minimize the negative effects of existing body biasing approach. This can be achieved by intelligently applying body bias to appropriate CMOS network based on its status (on-/off-state) with the aid of a pin/transistor reordering technique.

Methodology for Standby Leakage Power Reduction in Nanometer-Scale CMOS Circuits

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Chapter 1
Introduction

As CMOS technology and supply voltage (V_{DD}) are scaled down, gate oxide thickness and threshold voltage must also be reduced to maintain reasonable short channel effects and to achieve the desired performance improvement, respectively. Despite the use of a lower power supply voltage in each technology generation, the leakage power increases exponentially due to the reduced gate length, gate oxide thickness and threshold voltage [1].

With technology downscaling, subthreshold leakage current exponentially increases as threshold voltage reduces. Previously, subthreshold leakage was the dominant leakage component, and thereby conventional leakage reduction techniques focus primarily on subthreshold leakage alleviation, whereas the effect of gate leakage current was neglected. However, downscaling of gate oxide thickness (T_{OX}) produces significant gate tunneling leakage current, which has become a major leakage component in CMOS circuits [1], [2]. Furthermore, as the T_{OX} scales below 2nm, gate tunneling leakage current increases drastically, and thus gate leakage becomes a dominant leakage component [2]-[5] since the gate

tunneling leakage current strongly depends on T_{OX} [6], [7]. Thus, circuit-level techniques, which used to only suppress subthreshold leakage, need to reevaluate in nanometer-scale technologies since subthreshold leakage is not the only serious leakage source in nanometer-scale era.

In this thesis, we focus on leakage behavior of CMOS circuits, and propose general leakage reduction methods for standby leakage power reduction. In the following, proposed techniques are described in more details.

1.1 Analysis of Steady States in a CMOS Transistor

In this work, we provide an in-depth study and analysis of the possible steady states of both PMOS and NMOS transistors in a CMOS circuit. Based on this fundamental analysis, we point out problems related to previous steady state model, and provide an accurate steady state model in CMOS circuits. Further, we propose the five distinct types of steady states based on leakage components of a single transistor to better understanding of leakage behavior, and present the major leakage sources of each network (on- and off-state network) in CMOS circuits by analyzing the components of steady states in on- and off-state CMOS

network. Finally, we define the main steady states of CMOS transistors since main steady states are found in every CMOS logic gate unlike other steady states.

1.2 Analysis of the Effect of Pin/Transistor Reordering on Leakage Current

In this research, we first discuss how gate and subthreshold leakage varies with input vector of CMOS gate. And then we investigate the opportunities for reducing gate and subthreshold leakage simultaneously by using pin reordering, and point out the problems and limitations associated with existing pin reordering technique when applying this technique to pull-up network of CMOS circuits and complex CMOS logic gates. To solve these problems, we propose a novel pin and transistor reordering technique for leakage reduction. The proposed method provides an optimized formation for leakage reduction, and can be used in combination with other leakage reduction techniques to achieve further improvement.

1.3 Effective Body Bias for Standby Leakage Power Reduction in Nanometer-Scale CMOS Circuits

Reverse Body Biasing (RBB) technique [8]-[12] has become one of the most widely used circuit design technique for leakage power reduction. It utilizes the body effect of CMOS gates by manipulating the threshold voltage in standby mode. In this research, we analyze the RBB technique from a structural point of view, and address the problems associated with overall leakage savings due to the lack of awareness of other than subthreshold leakage. To solve these problems, we propose the leakage-aware body biasing methods which take into account not only the subthreshold leakage but also gate and BTBT leakage, resulting in enhanced the effectiveness of body biasing for leakage power reduction.

1.4 Dissertation Outline

The remainder of the thesis is organized as follows. Chapter 2 briefly reviews major leakage current components, and a number of commonly used leakage reduction techniques. Chapter 3 describes the possible bias conditions for CMOS transistors in a circuit. The analysis of the effect of pin reordering on leakage

reduction is presented in Chapter 4. Chapter 5 describes the proposed transistor reordering method for leakage power reduction. Chapter 6 describes the proposed leakage-aware body biasing methodologies in association with pin/transistor reordering technique. Finally, conclusion and future work are presented in Chapter 7.

Chapter 2
Background

In this chapter, we briefly review the leakage sources in CMOS transistors, and existing leakage power reduction techniques. This chapter is helpful for understanding the remainder of this thesis.

2.1 Standby Leakage Components

In nanometer-scale CMOS devices, the main components of leakage currents are subthreshold leakage (I_{SUB}), gate tunneling leakage (I_G), and reverse biased junction BTBT leakage (I_{BTBT}). We describe the effect of scaling trends on these three main leakage components in this subchapter.

2.1.1 Subthreshold Leakage

The subthreshold leakage is a current flowing between drain and source terminals of CMOS transistor when the gate voltage is below the subthreshold voltage. This subthreshold leakage increases exponentially with technology

scaling due to reduced threshold voltage. The subthreshold current of a MOSFET device can be expressed as [7], [19]:

$$I_{SUB} = \mu \frac{W_{eff}}{L_{eff}} \sqrt{\frac{q\varepsilon_{si}N_a}{2\Phi_s}} V_T{}^2 \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \quad (1)$$

where μ is the electron surface mobility q is the electronic charge, ε_{si} is the silicon permittivity, N_a is the doping concentration in the substrate, $V_T = kT/q$ is the thermal voltage; k is the Boltzman constant, T is the absolute temperature, and Φ_s is the surface potential, V_{DS} is the drain-source voltage, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage and n is the subthreshold swing parameter.

I_{SUB} depends on the transistor threshold voltage (V_{th}), gate-to-source (V_{GS}) and drain-to-source voltages (V_{DS}), and temperature (T). When the MOSFET is off-state ($V_{GS} = 0V$), reduction of the threshold voltage causes subthreshold current to increase exponentially as shown in (1). The threshold voltage equation considering the body effect is given by [19]:

$$V_{th} = V_{fb} + 2\Psi_B + \frac{\sqrt{2\varepsilon_{si}qN_a(2\Psi_B + V_b)}}{C_{ox}} \quad (2)$$

where V_{fb} is the flat band voltage, Ψ_B is the difference between Fermi potential and intrinsic potential in the substrate and equal to $(kT/q)ln(Na/ni)$, where ni is the intrinsic carrier concentration, V_b is the substrate (body) bias voltage and C_{ox} is the gate oxide capacitance. The RBB scheme has been used to reduce the subthreshold leakage by applying reverse body bias which increases the V_b – a phenomenon known as body effect. On the other hand, forward body bias decreases V_b, and thereby increases the subthreshold leakage by reducing the threshold voltage.

2.1.2 Gate Leakage

In nanometer-scale MOSFET device, gate-oxide thickness becomes thinner with technology scaling in order to control short channel effects and increase the transistor driving strength. The aggressive scaling in the gate-oxide thickness (T_{ox}) causes gate tunneling current to exponentially increase since the gate leakage is a strong exponential function of the oxide thickness as shown in (3). The gate tunneling current density (J_g) is given by [19], [20]:

$$J_g = A\left(\frac{V_{ox}}{T_{ox}}\right)^2 exp\left(\frac{-T_{ox}\, B\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)\right)^{\frac{3}{2}}}{V_{ox}}\right) \tag{3}$$

$$\text{where } A = \frac{q^3}{16\pi^2\,\hbar\phi_{ox}} \text{ and } B = \frac{4\sqrt{2m^*}\,{\phi_{ox}}^{\frac{3}{2}}}{3\hbar q}$$

where V_{ox} is the voltage drop across the gate oxide, T_{ox} is the gate oxide thickness, ϕ_{ox} is the barrier height for tunneling electron, $\hbar$ is the reduced Plank's constant, and m^* is the electron effective mass.

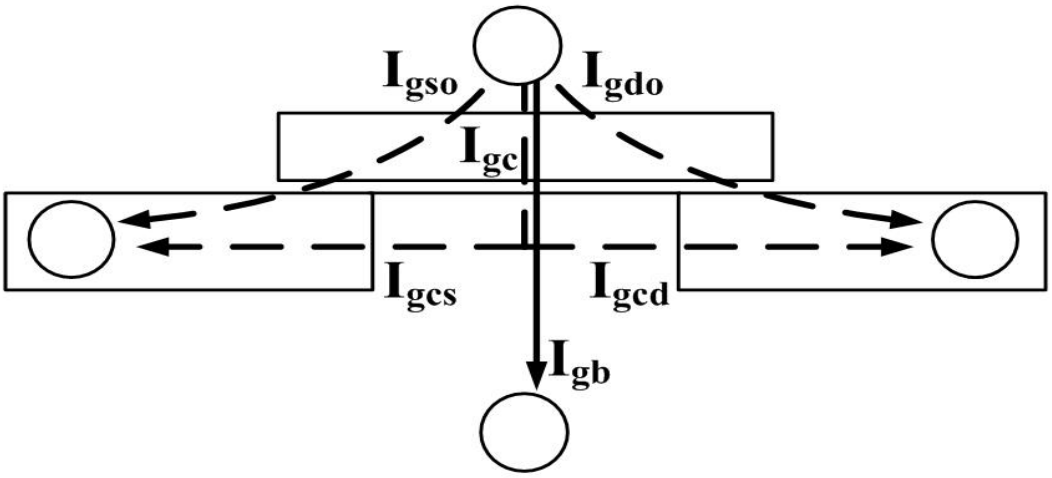

Figure 1: Gate tunneling current flows and components.

Figure 1 shows the components of I_G between gate and source/drain diffusion regions (I_{gso} and I_{gdo}), between gate and bulk (I_{gb}), and between gate and channel (I_{gc}), which is further partitioned between the source and drain terminals by I_{gc} = I_{gcs} + I_{gcd} [6]. Hence, the gate tunneling currents can be divided by the current flows; gate to source (I_{GS} = I_{gso} + I_{gcs}), gate to drain (I_{GD} = I_{gdo} + I_{gcd}) and gate to body (I_{GB} = I_{gb}). Hence, I_G is equal to the sum of the I_{GD} , I_{GB} and I_{GS} .

2.1.3 Band-to-Band Tunneling Leakage

As CMOS technology scales down, substrate doping concentration increases in order to reduce the short channel effects. Therefore, heavily doped n+ drain/source and p-type substrate yield high electric field across the reverse-biased p-n junction, which produces significant current flows through the junction, and the BTBT current density is expressed as [19], [20]:

$$J_{btbt} = \frac{\sqrt{2m^*}q^3\,\xi\,V_{app}}{4\pi^3\,\hbar^2\,E_g^{\frac{1}{2}}}\,exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3q\hbar\xi}\right) \qquad (4)$$

$$\text{where } \xi = \sqrt{\frac{2q\,N_aN_d\,(V_{app}+V_{bi})}{\varepsilon_{si}\,(N_a+N_d)}}$$

where ξ is the electric field at the junction, E_g is the energy bandgap, V_{app} is the applied reverse voltage across the junction, V_{bi} is the built-in voltage and N_a and N_d are the doping concentration of p and n side. As shown in (4), when substrate doping concentration increases, BTBT current exponentially increase with the increase of the electric field at junction.

2.2 Standby Leakage Reduction Techniques

In this subsection, we review previous circuit design techniques for leakage reduction in CMOS circuits.

2.2.1 Leakage Reduction by Stacking Effect

Stacking of series-connected transistors reduces the subthreshold leakage currents when more than one transistor in the stack is turned off, which is known as stacking effect [17]. It yields a positive potential at the intermediate node of off-transistors, which has three effects: 1) gate-to-source voltage (V_{GS}) of upper transistor becomes negative; 2) reverse biased body-to-source voltage (V_{BS}) of upper transistor induces larger body effect; 3) reduced drain-to-source voltage

(V_{DS}) of upper transistor causes less drain-induced barrier lowering (DIBL). Therefore, the subthreshold leakage current reduces exponentially under stacking effect. For instance, considering the two-input NAND gate (see Figure 2) with stacking effect case (AB="00"), the positive potential at the intermediate node (Vinter > 0) between off-transistors (Tr1 and Tr2) causes the negative V_{GS} and V_{BS} of upper transistor (Tr1), and reduction in V_{DS} of Tr1. Due to the stacking effect, leakage in a logic gate depends on the applied input vector during standby periods since it determines the number of off-transistors in the stack. In the following, existing techniques are described in more details.

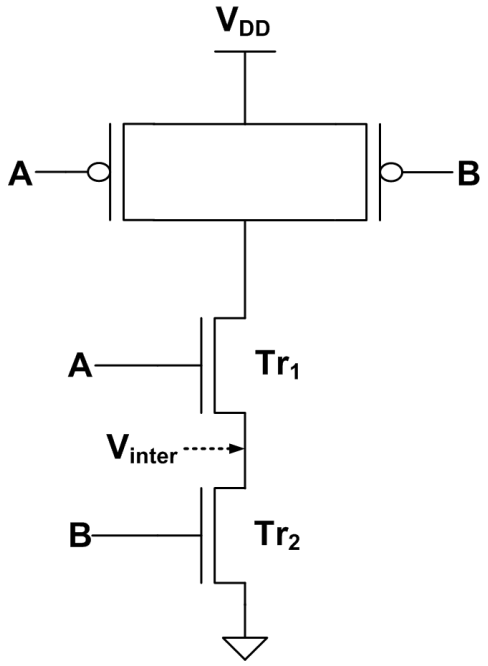

Figure 2: Two-Input NAND Gate.

The input vector control (IVC) technique [16]-[18] is presented to find minimum leakage vector (MLV) which finding the input pattern that maximizes the number of off-transistors in all stacks across the circuit during standby periods. Leakage reduction can be achieved up to 39% savings if input vector control is used [18]. Implementing the predetermined vector (MLV) during standby mode is done by adding static latches at the inputs of the circuit [17].

The IVC technique does not guarantee that all logic gates of a circuit block are working under stacking effects due to the inverter and logic correlation between gates. Inherently, an inverter does not present the stacking effects since both networks (pull-up and pull-down) consist of a single transistor, and some logic gates did not benefit from IVC as shown in Figure 3 (a) which shows the sample path of the circuit block. For this reason, stack forcing technique [21] was introduced. The main objective of this technique is to increase the number of logic gates in stacking effects; a non-stacked transistor is changed into a stack of two transistors by replacing a single transistor with two transistors of the same size. Hence, stack forcing technique guarantees two off-transistors for every off-input of the gate, which reduces leakage currents as shown in Figure 3 (b). This technique, however, reduces the drive current due to the iso-input load

requirement, resulting in increased delay. Therefore, stack forcing technique can be used only for paths that are non-critical.

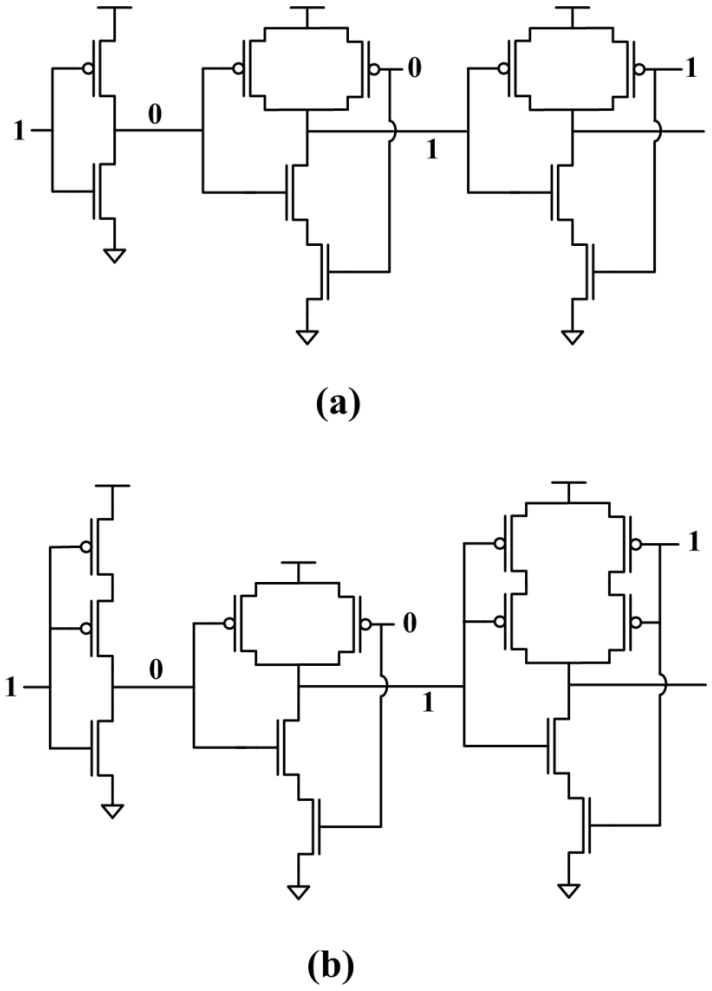

Figure 3: (a) logic gate parts of circuit block when predetermined input vector applied in standby mode (b) stack forcing applied to non-stacked logic gates.

Another technique to reduce leakage power through stacking effects is LECTOR [22], which uses two extra transistors called leakage control transistors (LCTs) inserted in series between pull-up network and pull- down network in

each CMOS gate as shown in Figure 4 (b). Leakage control transistors cause increase in resistance of the path from supply voltage (V_{DD}) to ground since one of the LCTs is always near its cutoff region, thereby decreasing leakage current. However, this technique suffers from signal quality with technology scaling down to deep submicron era due to the LCTs [23].

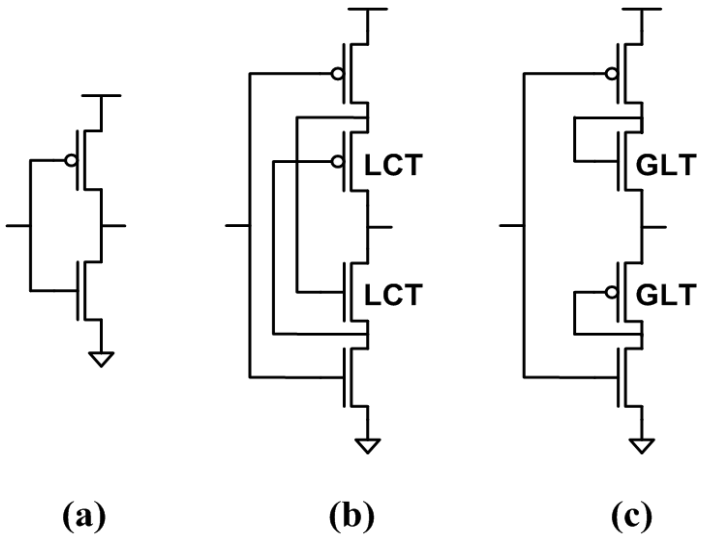

Figure 4: (a) Original Inverter (b) LECTOR Inverter (c) GALEOR Inverter.

GALEOR technique [24] has the same structure as LECTOR except that the locations of extra transistors (referred to as Gated Leakage Transistors (GLTs)) are switched as shown in Figure 4 (c). PMOS GLT is located between pull-down network and output and NMOS GLT is located between pull-up network and

output. The effectiveness of this technique, however, reduced as technology scaling because of the signal quality problems [23].

2.2.2 Leakage Reduction by Sleep Transistor

There are many ways to use a sleep transistor, but the basic idea is to increase the resistance by inserting the extra transistors (sleep transistors) in series between the power supply and ground, thereby reducing the standby leakage currents. The sleep transistors are turned on when circuits are in active mode and turned off when circuits are in standby mode. In the following, existing techniques are described in more details.

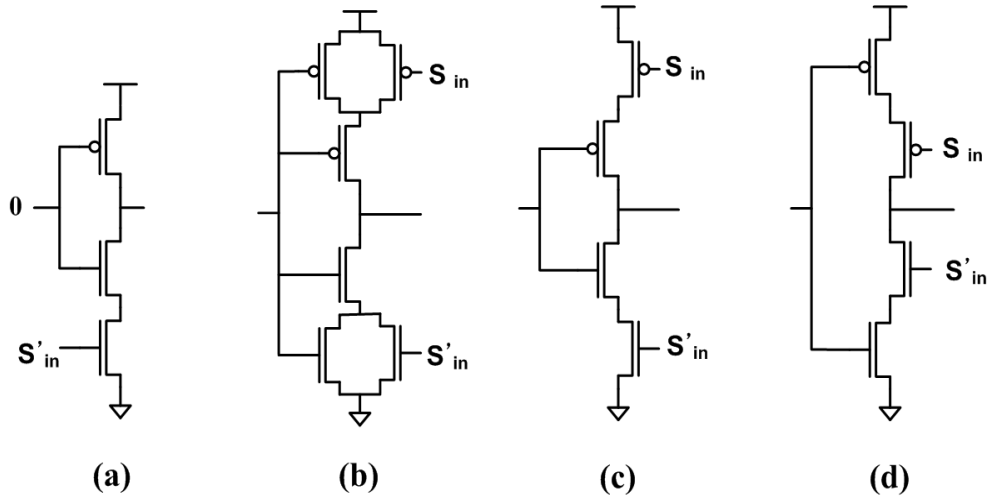

Figure 5: (a) single-V_{th} stacking (b) Sleepy stack (c) Power gating (d) Drain gating.

In [25], the circuit is evaluated based on predetermined minimum leakage input vector, and additional leakage control transistors are inserted in the non-critical paths where only one transistor is originally turned "OFF" as shown in Figure 5 (a), and thereby reduce the subthreshold leakage. The extra transistor is turned on during the regular mode of operation and turned off during the idle mode of operation.

Sleepy stack technique [26] is an upgraded version of the stack forcing technique, using additional sleep transistors inserted parallel to one of the transistors in each set of two stacked transistors (forced stack), which is shown in Figure 5 (b). The sleep transistors of the sleepy stack operate in a way similar to the sleep transistors used in the sleep transistor technique where sleep transistors are turned on during active mode and turned off during sleep mode. As compared to the stack forcing technique, parallel connected sleep transistors cause the decrease in resistance of the path, thereby decreasing the propagation delay during active mode while stacked transistors suppress leakage current during standby mode. Sleepy stack technique, however, comes with some delay and significant area overheads since every transistor is replaced by three transistors.

Power gating [27] technique uses additional transistors, called sleep transistors, which are inserted in series between the power supply and pull-up (PMOS) network and/or between pull-down (NMOS) network and ground to reduce the standby leakage currents as shown in Figure 5 (c). The sleep transistors are turned "ON" when circuits are in active mode and turned off when circuits are in standby mode. By disconnecting the logic networks from the power supply and/or ground using sleep transistors, this technique reduces the leakage power in standby mode.

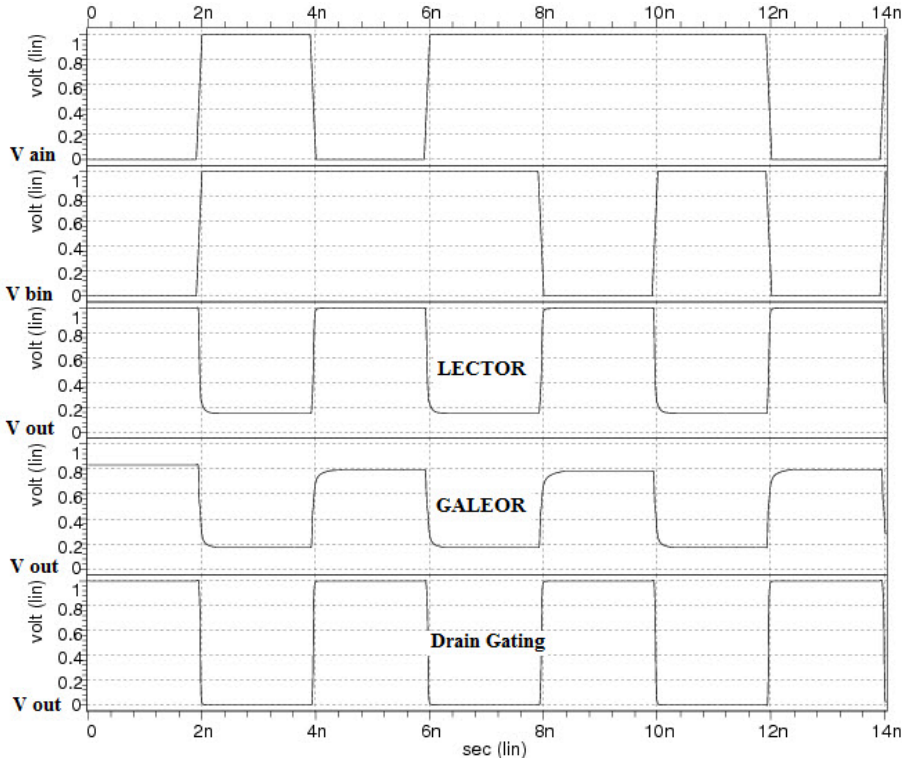

Figure 6: Transient characteristics of two-input NAND gate in LECTOR, GALEOR and Drain Gating simulated by HSPICE [23].

Another technique to reduce leakage power by using sleep transistor is the drain gating technique [23] reduces the leakage current by inserting extra sleep transistors between pull-up and pull-down networks. This technique introduced to overcome the limitations of LECTOR and GALEOR techniques. When applied to sub-45nm process technologies, both LECTOR and GALEOR techniques suffer a significant problem; that is, the low signal is very much higher than 0 volt. In addition, GALEOR causes high signal much lower than the V_{DD}. Such phenomena make the use of both techniques unfeasible. A typical case for a 2-input NAND gate using 45nm technology is shown in Figure 6, where the low signal is 0.2V for both LECTOR and GALEOR, and the high signal for GALEOR is 0.8V, rather than 0V and 1V, respectively. Similar troubling behaviors are consistently observed for all other gate types such as NOR, OR, AND, XOR. To make things worse, the problems become even more severe as process technology scales down such as in 32nm and 22nm process technologies [23]. As shown in Figure 5 (d), a PMOS sleep transistor(s) is placed between pull-up network and network output and an NMOS sleep transistor(s) is placed between network output and pull-down network. During active mode, both sleep transistors are turned on to reduce the resistance of conducting paths, thereby

reducing performance degradation. During standby mode, both sleep transistors are turned off to produce stacking effect which reduces leakage current by increasing resistance of the path from power supply to ground. By applying two turned-on sleep transistors in active mode, drain gating produces exact logic levels as shown in Figure 6 due to less resistance of the path from V_{DD} to ground than that of LECTOR and GALEOR which always have one turned-on LCT/GLT and the other near cutoff region LCT/GLT, thus preventing exact logic state. Furthermore, the drain gating technique has less leakage current than LECTOR and GALEOR techniques because, in standby mode, two turned-off sleep transistors (drain gating) yield more resistance to the path from V_{DD} to ground than the combined effect of a near cutoff region LCT/GLT and a turned-on LCT/GLT.

2.2.3 Leakage Reduction by Increasing the Threshold Voltages

Increasing the threshold voltage is one of the effective ways to reduce the leakage current. There are several ways to achieve this [28]: (1) increase a doping

concentration; (2) increase a gate oxide thickness; and (3) apply a reverse body bias voltage. In the following, existing techniques are described in more details.

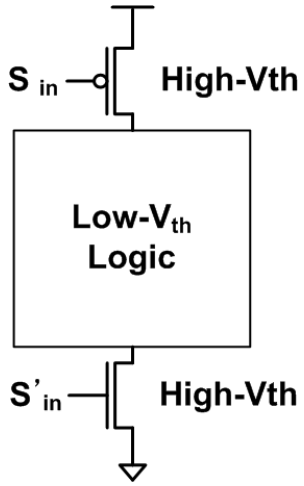

Figure 7: Multi-Threshold CMOS (MTCMOS).

Multi-threshold voltage CMOS (MTCMOS) [28]-[32] uses high-threshold devices as sleep transistors while low-threshold devices are used to implement the logic as shown in Figure 7. In practice, one sleep transistor per gate is used, but larger granularities are also used, which require fewer but larger sleep transistors. Typically, the NMOS sleep transistor is preferable because the on-resistance of NMOS is smaller than that of PMOS at the same width; hence, NMOS has size advantage over PMOS. This technique, however, comes with area and performance penalties.

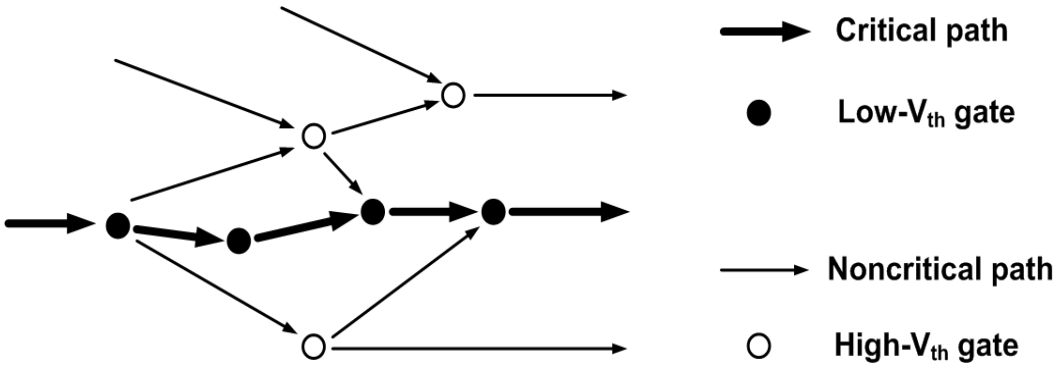

Figure 8: Dual threshold voltage technique.

Dual threshold voltage technique [33]-[35] assigned different threshold voltages depending on whether a gate is on critical or non-critical path as shown in Figure 8. Low threshold voltage on the critical path is used to maintain the performance, while high threshold voltage assigned along non-critical path reduces the leakage current.

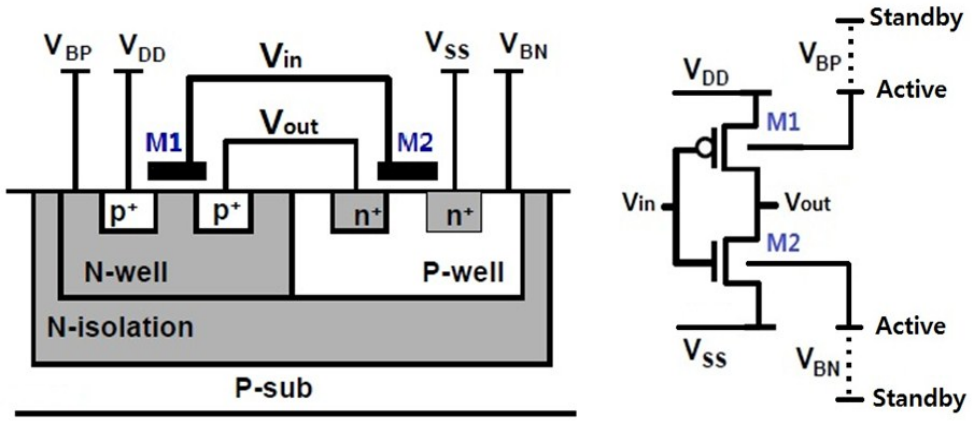

Figure 9: Reverse Body Biasing.

Reverse boy biasing (RBB) [8]-[12] is an effective way of reducing the leakage in standby mode by increasing the threshold voltages of MOS transistors (making the substrate (body) voltage higher than supply voltage for PMOS transistors and lower than ground for NMOS transistors); reverse biasing body-to-source junction of a MOS transistor widens the bulk depletion region and increases the threshold voltage. Reverse body bias is applied to suppress the leakage current when circuits are in standby mode, and is removed to restore the nominal performance of the transistors when circuits are in active mode as shown in Figure 9.

Adaptive body biasing (ABB) techniques have been introduced [36]-[40] in order to alleviate the impact of die-to-die and within-die parameter variations on microprocessor frequency and leakage. The aim of this technique is to meet the delay and power constraints in each die through post-silicon tuning; forward body bias is applied to the slow and less leaky devices to boost the performance while reverse body bias is applied to the fast and highly leaky devices to reduce the leakage. Therefore, effect of parameter variations is mitigated by post-silicon tuning, results in reducing the process variations impact as well as improving the total yield.

Chapter 3
Analysis of Steady States in a CMOS Transistor

3.1 Introduction

Rao *et al*. introduced six different steady states of MOS transistors for gate leakage estimation [41]. However, they made an overly simplified assumption that PMOS transistor has the same character as NMOS transistor. Such an assumption has led to a misleading conclusion that PMOS transistor has the counterpart of each steady state of NMOS transistor; that is, both NMOS and PMOS transistors have the same number (six) of steady states.

In this chapter, we first explore possible steady states of both PMOS and NMOS transistor in a CMOS circuit, and demonstrate that possible steady states of PMOS transistor is not six but five. And then we present the five distinct types of steady states based on leakage components of a single transistor, and analyze the components of steady state transistor in on- and off-state CMOS network. Finally, we define the main steady states of a CMOS transistor.

3.2 Possible Steady States for CMOS Transistors

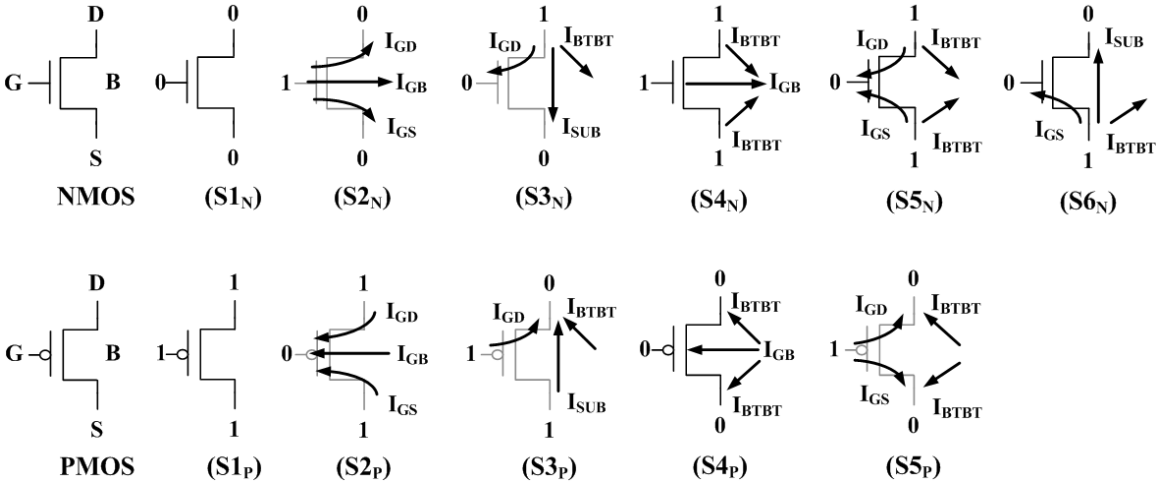

Figure 10: All possible bias conditions for CMOS transistors.

A single transistor has four terminal nodes: gate (G), drain (D), source (S) and body (B). The NMOS and PMOS body connected to ground (logic 0) and V_{DD} (logic 1) respectively. The body and gate nodes have full logic values (either V_{DD} or ground) in steady state conditions, while the other nodes (drain and source) have either at or close to full logic values depending on circuit structures.

Figure 10 shows the major leakage currents of eleven steady states in NMOS ($S1_N$-$S6_N$) and PMOS ($S1_P$-$S5_P$) transistors. The logic values "1" and "0" are represented by the high and low level of each terminal node. The direction of

current flows for MOS transistor is determined by voltage between gate and source (V_{GS}), gate and drain (V_{GD}), gate and body (V_{GB}), drain and body (V_{DB}), drain and source (V_{DS}), and source and body (V_{SB}).

Among four nodes in MOS transistor, drain and source nodes are dependent nodes since their logic values determined by either logic value of gate node or by circuit structure:

- In conducting (on) MOS transistor, gate node of NMOS (PMOS) transistor connected to V_{DD} (ground). In this condition, the dependent nodes (drain and source nodes) are only determined by gate node. Hence, a source node has the same logic value as a drain node ($S2_N$, $S4_N$, $S2_P$ and $S4_P$ in Figure 10)
- In non-conducting (off) MOS transistor, gate node of NMOS (PMOS) transistor connected to ground (V_{DD}). In this condition, dependent nodes are determined not only by gate node, but also by circuit structure. Intuitively, in a non-conducting transistor, it is clear that one of dependent nodes is 0 regardless of the other dependent node (either 1 or 0). This behavior works well under most circumstances of non-conducting transistor; this is shown as $S1_N$, $S3_N$, $S6_N$, $S3_P$ and $S5_P$ in Figure 10.

However, in certain cases ($S5_N$ and $S1_P$ in Figure 10), dependent nodes are not determined by gate node but by circuit structure, resulting in both drain and source nodes being 1 even though the transistor is in an off-state.

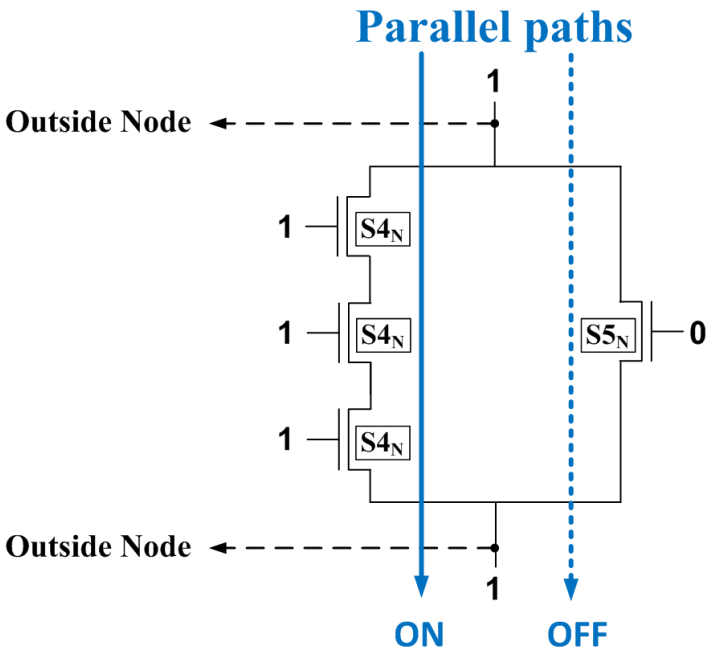

Figure 11: Pull-down network structure in the presence of $S5_N$.

Let us first consider an NMOS case. $S5_N$ will exist only if all of the following conditions are met: (1) logic value of outside nodes in parallel structure is 1 (high), which means that at least one of paths in parallel structure is "on"; (2) at least one of paths in parallel structure contains an off-transistor, and hence this path is "off"; this is shown in Figure 11.

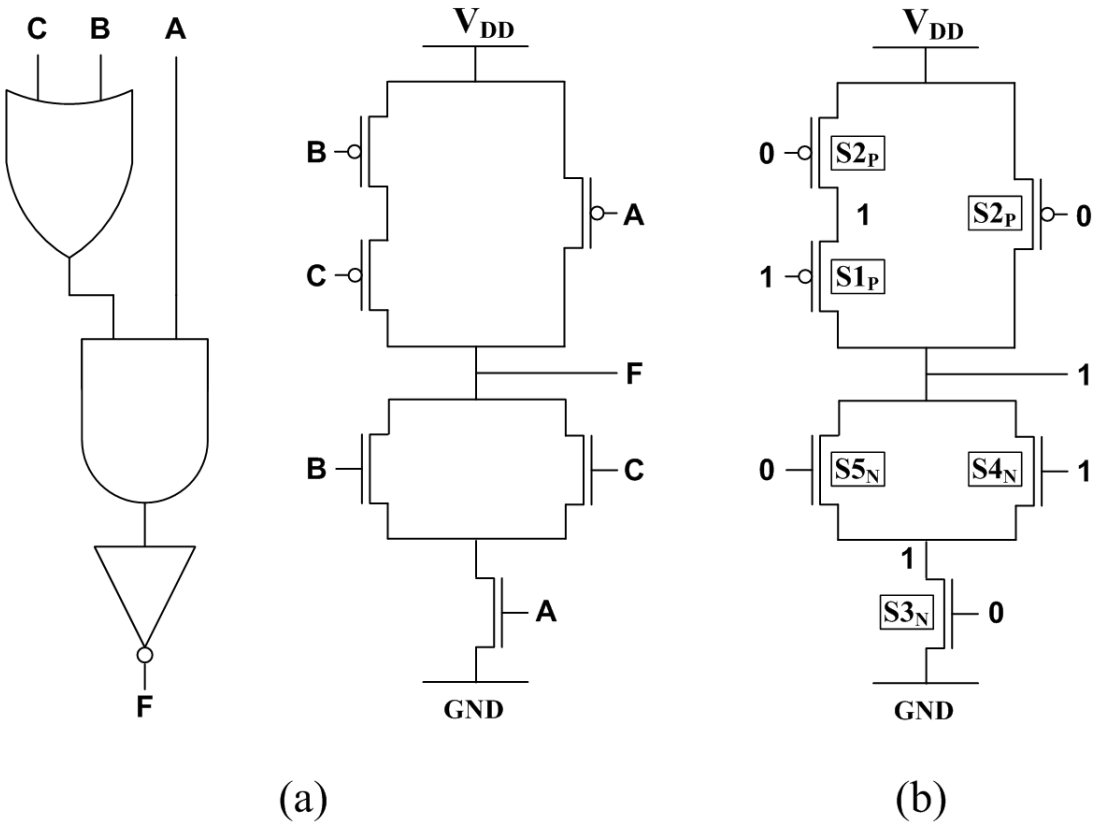

Figure 12: (a) 3-input OAI-21 gate ($F = \overline{A\,(B + C)}$) (b) Input: ABC = 001.

Table 1: Logic values and node voltages (V) of each transistor in 3-input OAI-21 gate with input (ABC) = "001".

Network	Input	State	Node Voltage			Logic value		
			V_D	V_G	V_S	D	G	S
PUN	A	$S2_P$	1.1	0	1.1	high	low	high
	B	$S2_P$	1.1	0	1.1	high	low	high
	C	$S1_P$	1.1	1.1	1.1	high	high	high
PDN	A	$S3_N$	0.846	0	0	high	low	low
	B	$S5_N$	1.1	0	0.846	high	low	high
	C	$S4_N$	1.1	1.1	0.846	high	high	high

Note that in the case described by condition (1), non-conducting transistors need to be located in the bottom of serial structure in order to have a high logic value at the bottom node of outside nodes. Hence, $S5_N$ exists only in a combination of serial and parallel MOS structures, which can be found in complex (compound) CMOS logic gates. For instance, Figure 12 (a) shows a 3-input OAI-21 gate ($F = \overline{A\,(B + C)}$) implemented with complex CMOS logic. Figure 12 (b) shows the particular input vector of OAI-21 gate which meets the conditions for the existence of $S5_N$ case. Table 1 lists the corresponding bias voltage and logic value of each node in Figure 12 (b); PUN and PDN stand for pull-up network and pull-down network, respectively.

In this chapter, all experimental data are conducted by HSPICE using the default 65nm PTM [42] at room temperature (standby mode).

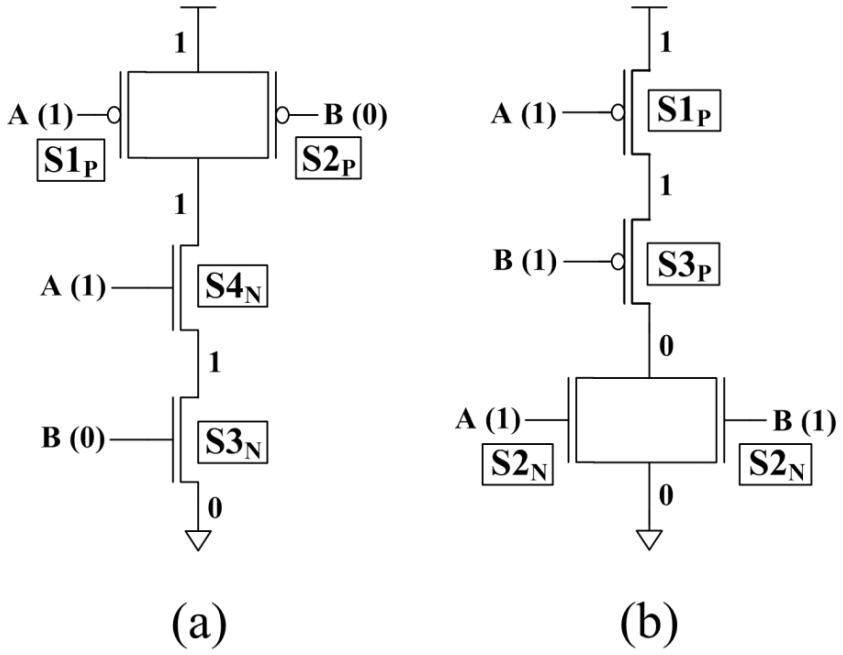

Figure 13: (a) 2-input NAND gate with input (AB) =10 (b) 2-input NOR gate with input (AB) =11.

Table 2: Logic values and node voltages (V) of each transistor in 2-input NAND gate with input (AB) = "10", and NOR gate with input (AB) = "11".

Gate type	Network	Input	State	Node Voltage			Logic value		
				V_D	V_G	V_S	D	G	S
NAND2	PUN	A	$S1_P$	1.1	1.1	1.1	high	high	high
		B	$S2_P$	1.1	0	1.1	high	low	high
	PDN	A	$S4_N$	1.1	1.1	0.847	high	high	high
		B	$S3_N$	0.847	0	0	high	low	low
NOR2	PUN	A	$S1_P$	0.990	1.1	1.1	high	high	high
		B	$S3_P$	2.13E-6	1.1	0.990	low	high	high
	PDN	A	$S2_N$	2.13E-6	1.1	0	low	high	low
		B	$S2_N$	2.13E-6	1.1	0	low	high	low

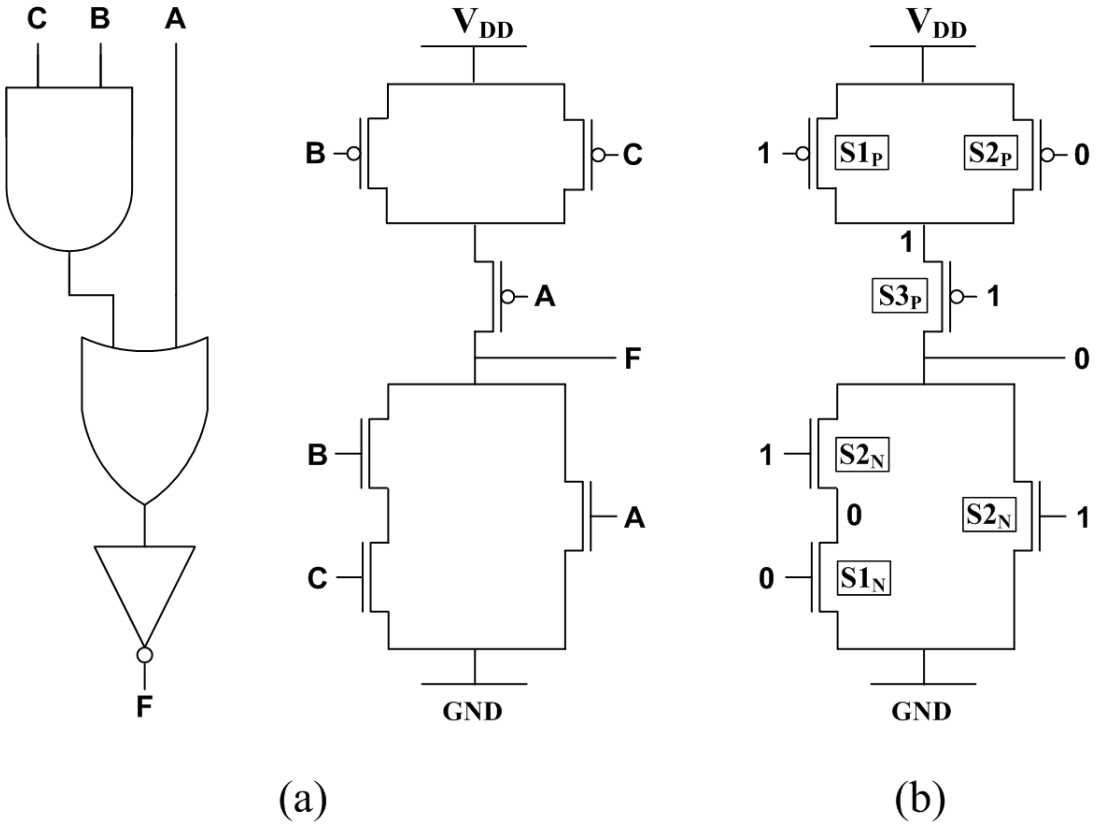

Figure 14: (a) 3-input AOI-21 gate (F = $\overline{A + BC}$) (b) Input: ABC = 110.

Table 3: Logic values and node voltages (V) of each transistor in 3-input AOI-21 gate with input (ABC) = "110".

Network	Input	State	Node Voltage			Logic value		
			V_D	V_G	V_S	D	G	S
PUN	A	$S3_P$	2.81E-5	1.1	1.1	low	high	high
	B	$S1_P$	1.1	1.1	1.1	high	high	high
	C	$S2_P$	1.1	0	1.1	high	low	high
PDN	A	$S2_N$	2.81E-5	1.1	0	low	high	low
	B	$S2_N$	2.81E-5	1.1	3.00E-5	low	high	low
	C	$S1_N$	3.00E-5	0	0	low	low	low

Now, let us consider the PMOS case. Unlike NMOS case ($S5_N$), $S1_P$ can exist in non-complex CMOS logic gate, and thus it also present complex CMOS logic gate. To elucidate this, we consider two-input NAND and NOR gates as illustrated in Figure 13. $S1_P$ can be existed not only parallel structure (Figure 13 (a)) but also serial structure (Figure 13 (b)). Table 2 lists the corresponding bias voltage and logic value of each transistor in Figure 13. Note that the first non-conducting transistor from output node presents the $S3_N$ and $S3_P$ in off-state pull-down and pull-up network, respectively. Figure 14 shows the presence of $S1_P$ in complex CMOS logic gate (3-input AOI-21). Table 3 lists the corresponding bias voltage and logic value of each transistor in Figure 14.

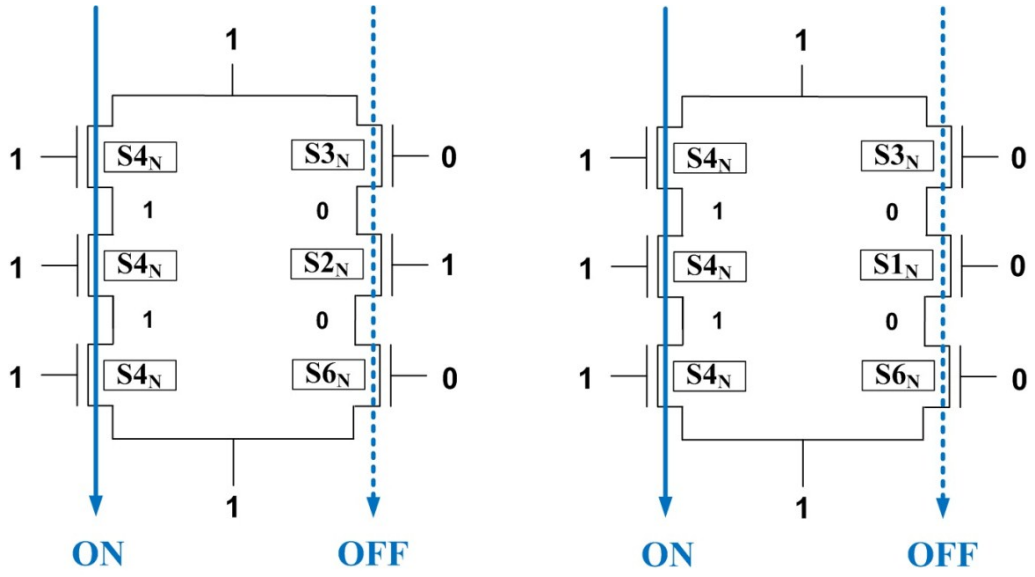

Figure 15: Pull-down network structures in the presence of $S6_N$.

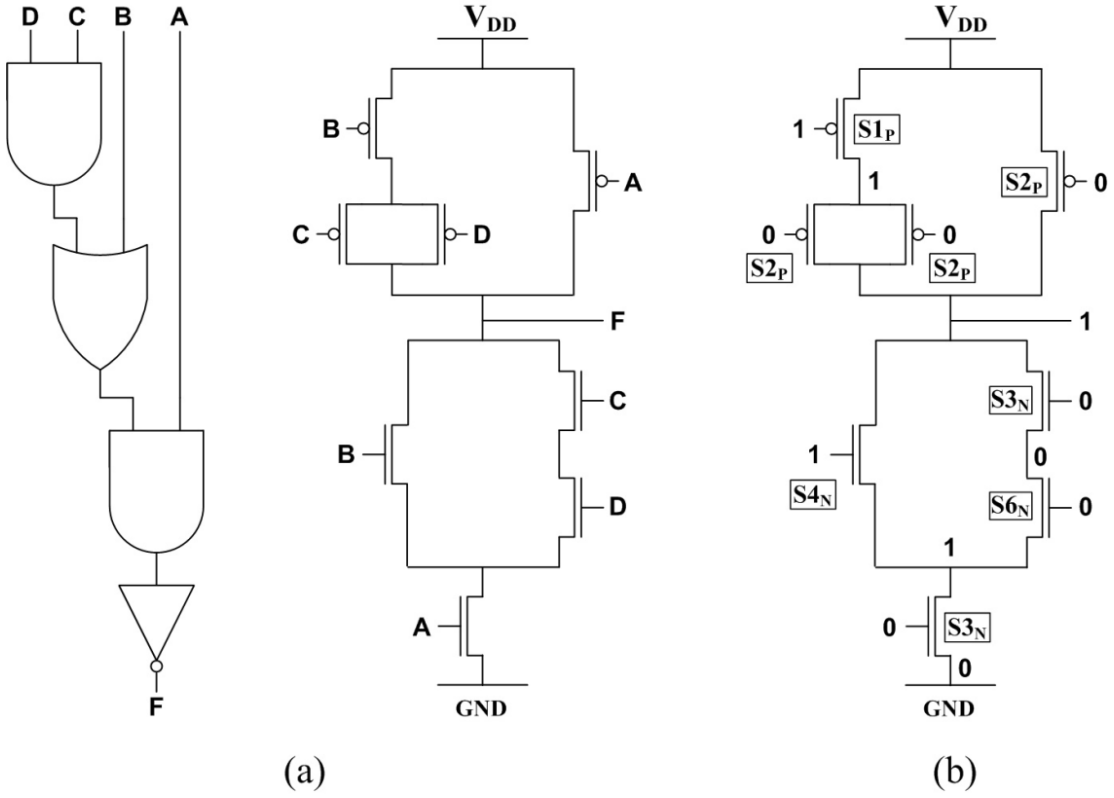

Figure 16: (a) 4-input AOAI-211 gate (F = $\overline{A(B + CD}$) (b) Input: ABCD = 0100.

Table 4: Logic values and node voltages (V) of each transistor in pull-down network of 4-input AOAI-211 gate with input (ABCD) = "0100".

Input	State	Node Voltage			Logic value		
		V_D	V_G	V_S	D	G	S
A	$S3_N$	0.846	0	0	high	low	low
B	$S4_N$	1.1	1.1	0.846	high	high	high
C	$S3_N$	1.1	0	0.237	high	low	low
D	$S6_N$	0.237	0	0.846	low	low	high

Additionally, $S6_N$ will exist under the same structural formation in the presence of $S5_N$ except for the number of off-transistors in off-path; $S6_N$ will exist only if the off-path has at least two off-transistors connected in series as shown in Figure 15. Note that $S6_N$ and $S3_N$ always coexist with each other. $S6_N$ and $S3_N$ exist only in complex logic gate just like the $S5_N$ case. For instance, Figure 16 (a) shows a 4-input AOAI-211 gate $F = \overline{A\,(B + CD)}$ implemented with complex CMOS logic. Figure 16 (b) shows the particular input vector of AOAI-211 gate which meets the conditions for the existence of $S6_N$ case. Table 4 lists the corresponding bias voltages and logic values of each node in Figure 16 (b).

An important point to note is that the counterpart of $S6_N$ does not exist in the PMOS transistor unlike other steady states; on-transistors of PMOS ($S2_P$ and $S4_P$) are the counterparts of on-transistors of NMOS ($S4_N$ and $S2_N$), and off-transistors of PMOS ($S1_P$, $S3_P$ and $S5_P$) are the counterparts of NMOS ($S5_N$, $S3_N$ and $S1_N$). To demonstrate this, we apply the same conditions for the existence of $S6_N$ to the PMOS case (Figure 17). It is shown that logic values of the all intermediate nodes are not 0 (low) but 1 (high), and thus, PMOS transistor has not six but five steady states unlike the assumption made in previous work [41]; experimental data is shown in Table 5.

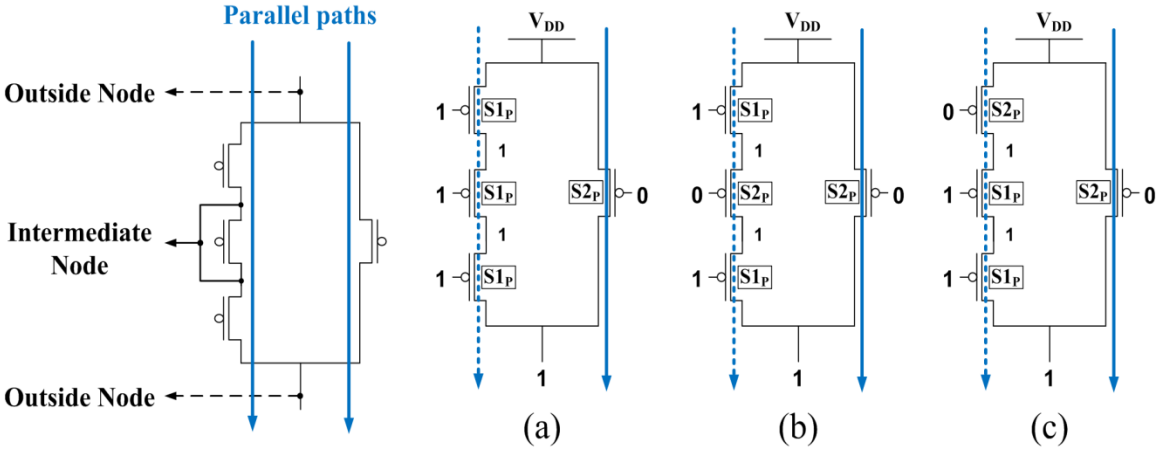

Figure 17: Pull-up network of OAI-31 gate ($F = \overline{A(B + C + D)}$) with different input vectors (a) ABCD=0111 (b) ABCD=0101 (c) ABCD= 0011.

Table 5: Logic values and node voltages (V) of each transistor in pull-up network of 4-input OAI-31 gate with different input vectors.

Input vector (ABCD)	Input	State	Node Voltage			Logic value		
			V_D	V_G	V_S	D	G	S
0111	A	$S2_P$	1.1	0	1.1	high	low	high
	B	$S1_P$	1.1	1.1	1.1	high	high	high
	C	$S1_P$	1.1	1.1	1.1	high	high	high
	D	$S1_P$	1.1	1.1	1.1	high	high	high
0101	A	$S2_P$	1.1	0	1.1	high	low	high
	B	$S1_P$	1.1	1.1	1.1	high	high	high
	C	$S2_P$	1.1	0	1.1	high	low	high
	D	$S1_P$	1.1	1.1	1.1	high	high	high
0011	A	$S2_P$	1.1	0	1.1	high	low	high
	B	$S1_P$	1.1	1.1	1.1	high	high	high
	C	$S1_P$	1.1	1.1	1.1	high	high	high
	D	$S1_P$	1.1	1.1	1.1	high	high	high

3.2.1 Sources of Leakage Currents in a CMOS Transistor under Different Bias Conditions

The leakage currents of a transistor are dependent on difference in voltage between any two nodes in a transistor:

- Subthreshold leakage exist only in non-conducting (off) transistor with $|V_{DS}| > 0$. There is no subthreshold leakage when drain and source nodes are same voltage ($V_D = V_S$).
- Gate leakage exists in both conducting and non-conducting transistors with $|V_{GS}| > 0$ or $|V_{GD}| > 0$ or $|V_{GB}| > 0$. Among steady states, gate leakage in $S2_N$ (NMOS) and $S2_P$ (PMOS) is the highest in each MOSFET. There is no gate leakage when all nodes are same voltage ($V_G = V_D = V_S = V_B$).
- BTBT leakage exists in both conducting and non-conducting transistors when reverse bias voltage applied between drain and body, or drain and source, or both; $V_{DB} > 0$ or $V_{SB} > 0$ or both in NMOS, and $V_{DB} < 0$ or $V_{SB} < 0$ or both in PMOS. If V_D (V_S) is close to 0, BTBT leakage in I_{DB} (I_{SB}) is negligible. There is no BTBT leakage when body, drain and source nodes are same voltage ($V_B = V_D = V_S$).

It is shown that each leakage component is highly dependent on the biasing conditions of the transistor. Therefore, steady states can be divided into five distinct types based on components of leakage sources: least leaky state (S_{LEAST} : $S1_N$ and $S1_P$), most gate leaky state (S_{GATE} : $S2_N$ and $S2_P$), subthreshold leaky state (S_{SUB} : $S3_N$, $S6_N$ and $S3_P$), least gate leaky state (S_{LG} : $S4_N$ and $S4_P$), and reverse gate leaky state (S_{RG}: $S5_N$ and $S5_P$).

3.3 Steady State Components in On- and Off-State network

3.3.1 Steady state components in on-state CMOS network.

The on-state network of CMOS logic gates is present in either the gate leaky state ($S2_N$/$S2_P$) alone, or gate leaky state along with least leaky state ($S1_N$/$S1_P$), but not in other steady states (i.e., subthreshold, least gate and reverse gate leaky); if pull-up (pull-down) network is ”on”, both source and drain nodes of every transistor in on-state network carry high (low) logic value regardless of its gate input state. Hence, when pull-up network is “on”, the number of gate leaky

states in on-state network is the same as the number of low (i.e., 0 volt) gate input states in input vector, whereas when pull-down network is "on", the number of gate leaky states in on-state network is same as the number of high (i.e., V_{DD}) gate input states in input vector. It is noteworthy to note that subthreshold leakage does not exist in on-state network since all internal nodes in on-state network exhibit almost equal to full logic values (V_{DD} (ground) in pull-up (pull-down) network). For instance, node voltages of on-state pull-up network are shown in Table 1 and Table 2 (NAND2) and Table 3).

The internal node of on-state CMOS network can be divided into two cases. The first case of the internal node in on-state pull-up (pull-down) network always has conducting path to the V_{DD} (ground) as shown in Figure 18 (a) and (c); the second case of the internal node surrounded by off-transistors, which is illustrated in Figure 18 (b) and (d). In both cases the internal node exhibits either at or very close to full logic value, and thus every gate leaky state ($S2_P$ and $S2_N$) in on-state network has almost identical gate leakage current in each network, while leakage current of least leaky state ($S1_P$ and $S1_N$) is negligible as tabulated in Table 6. Hence, the major leakage source of on-state network is the gate leakage current.

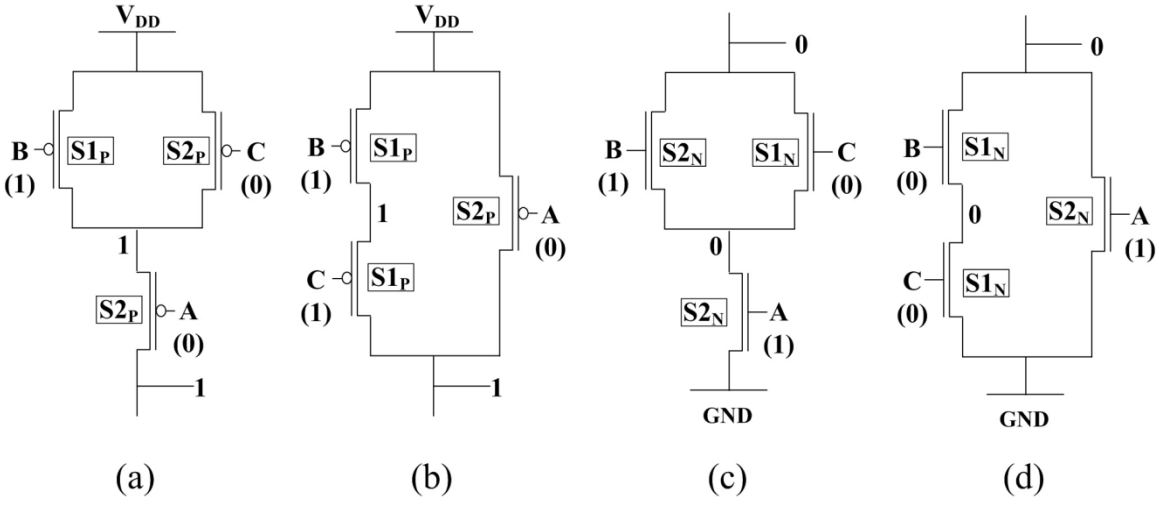

Figure 18: Steady state components in on-state pull-up/-down network: Case1 ((a) and (c)) and Case2 ((b) and (d)).

Table 6: Steady state components, node voltages (V) and gate leakage current (nA) in different ON-state CMOS networks of Figure 18.

Network	Input	State	Node Voltage (V)			I_G (nA)
			V_D	V_G	V_S	
PUN (a)	A	$S2_P$	1.1	0	1.1	3.034E-02
	B	$S1_P$	1.1	1.1	1.1	2.365E-10
	C	$S2_P$	1.1	0	1.1	3.034E-02
PUN (b)	A	$S2_P$	1.1	0	1.1	3.034E-02
	B	$S1_P$	1.1	1.1	1.1	8.538E-11
	C	$S1_P$	1.1	1.1	1.1	3.034E-02
PDN (c)	A	$S2_N$	3.67E-5	1.1	0	4.112
	B	$S2_N$	6.95E-5	1.1	3.67E-5	4.111
	C	$S1_N$	6.95E-5	0	3.67E-5	1.360E-08
PDN (d)	A	$S2_N$	2.43E-5	1.1	0	4.112
	B	$S1_N$	2.43E-5	0	1.21E-5	4.668E-09
	C	$S1_N$	1.21E-5	0	0	1.556E-09

3.3.2 Steady state components in off-state CMOS network.

The off-state network of CMOS logic gates exists in either the subthreshold leaky state ($S3_N/S3_P$) alone or in the subthreshold leaky state along with other types of steady state; thus, all types of steady state exist in off-state network:

- In case of off-state pull-down network, least leaky ($S1_N$) and gate leaky ($S2_N$) states are present when each of those transistors ($S1_N$ and $S2_N$) is located below the subthreshold leaky state ($S3_N$), while other steady states (least gate ($S4_N$) and reverse gate ($S5_N$) leaky state) are present when each of those transistors ($S4_N$ and $S5_N$) is located above the subthreshold leaky state ($S3_N$) as shown in Figure 12 (b).
- In case of off-state pull-up network, the least leaky ($S1_P$) and gate leaky ($S2_P$) states are present when each of those transistors is located above the subthreshold leaky state ($S3_P$) as shown in Figure 14 (b), whereas both least gate leaky state ($S4_P$) and reverse gate leaky state ($S5_P$) are present when each of those transistors is located below the subthreshold leaky state ($S3_P$).

Thus, the major leakage sources of off-state network are the subthreshold and gate leakage current. Note that, unlike the $S4_N$, $S1_P$ and $S2_P$, the $S5_N$ cannot exist along with the subthreshold leaky state without accompanying the $S4_N$ as described earlier in this chapter. Unlike on-state network, the number of subthreshold leaky states in off-state network is not always the same as the number of high (low) input states in pull-up (pull-down) network due to the presence of series-connected transistors in off-state network (see Figure 13 (b)). For this reason, each subthreshold leaky state is always accompanied by gate leaky state, whereas gate leaky state is not always accompanied by subthreshold leaky state (see Figure 12 (b), Figure 13 (a) and (b), and Figure 14 (b)). Hence, the number of gate leaky states is always greater than or equal to that of subthreshold leaky states in CMOS logic gates.

3.4 Main Steady States in a CMOS Circuit

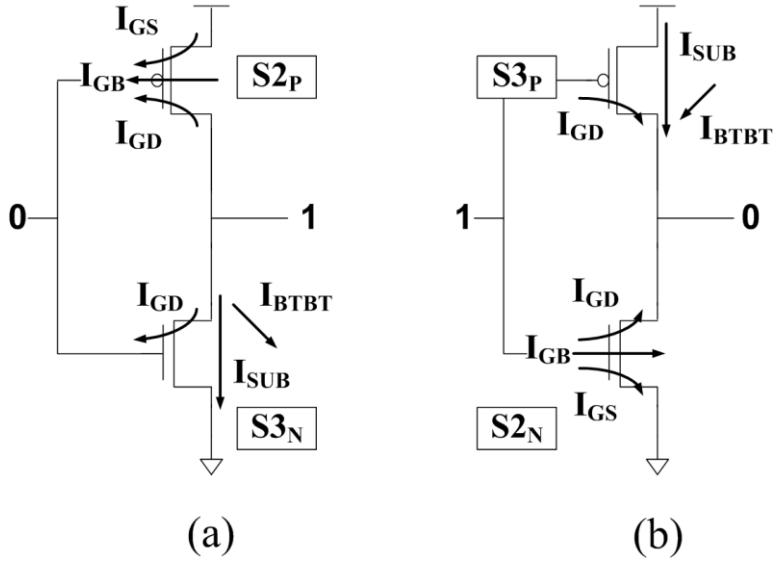

Figure 19: Steady state components of Inverter: (a) input=0 (b) input=V_{DD}.

The main steady states of CMOS circuit are gate leaky state and subthreshold leaky state because these steady states are found in every CMOS logic gate unlike other steady states; in standby mode of each CMOS logic gate, one network (either pull-up (PMOS) or pull-down (NMOS)) is always "on" and the other network is always "off", which means that the off-state in pull-down/pull-up network always has at least one subthreshold leaky state ($S3_N$/$S3_P$), and on-state in pull-down/pull-up network always has at least one gate leaky state ($S2_N$/$S2_P$). In other words, every CMOS logic gate has either a pair of $S3_N$ and $S2_P$, or a pair

of $S2_N$ and $S3_P$ depending on its input; $S3_N$ and $S2_P$ are present when input logic value is low, and $S2_N$ and $S3_P$ are present when input logic value is high. For instance, Figure 19 shows the steady states of each input vector in an Inverter. Therefore, $S2_N$ and $S3_N$ represent the basic NMOS transistors, and $S2_P$ and $S3_P$ represent the basic PMOS transistors.

3.5 Summary

In this chapter, an accurate steady state model was presented. Based on this model, the five distinct types of steady states were proposed to better understanding of leakage behavior in CMOS circuits. We then presented the major leakage sources of each network (on- and off-state network) in CMOS circuits by analyzing the proposed types of steady states in on- and off-state CMOS network. Finally, we defined the main steady states of CMOS transistors since main steady states are found in every CMOS logic gate unlike other steady states.

Chapter 4
Analysis of the Effect of Pin Reordering on Leakage Current

4.1 Introduction

The input vector control (IVC) technique [16]-[18] is presented to reduce subthreshold leakage current by using stacking effect. The idea of this technique is to find minimum leakage vector (MLV) that maximizes the off-transistors in all stacks across the circuit. Thus, the primary input vector switch to the MLV for leakage reduction with help of a sleep signal when a circuit is at standby mode. However, IVC technique does not guarantee that all logic gates in a circuit are benefited from stacking effects due to the logic correlation between the gates. For example, only two gates (G1 and G2) out of six gates in C17 circuit take advantage of stacking effect when MLV (00010) is applied as shown in Figure 20.

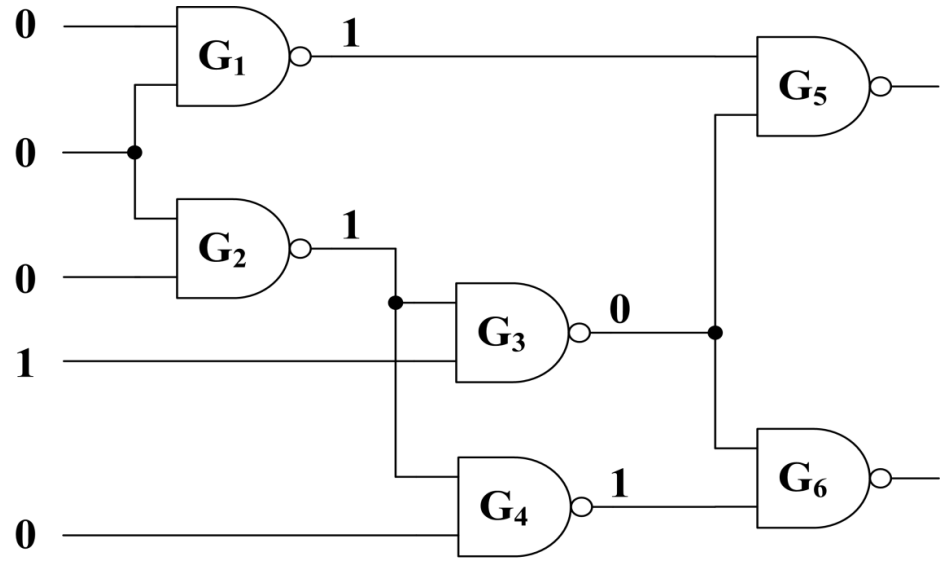

Figure 20: MCNC benchmark circuit C17 [43].

In CMOS logic gates, there are two kinds of input vectors: one of input vectors produces the same gate input state (either high or low in all gate nodes: G1, G2 and G3 in Figure 20), and the other one produces the different gate input states (high and low logic: G4, G5 and G6 in Figure 20).

Table 7 lists the leakage current of 2-input NAND gate for all possible input vectors to the gate. The leakage values are obtained from a HSPICE simulation using the 65nm PTM [42] models at V_{DD} (1.1V). Note that half of gates in C17 present different gate input states (both high (V_{DD}) and low (ground) exist in gate nodes: G4, G5 and G6)) when MLV is applied.

Table 7: Leakage current (nA) of two-input NAND gate.

Input	I_{SUB}	I_G	I_{TOTAL}
00	1.226	1.078	2.304
01	15.229	5.160	20.389
10	6.961	0.260	7.221
11	48.011	8.252	56.264

As can be seen from Table 7, the leakage currents corresponding to input vector (01) and to input vector (10) are different, and hence the leakage of C17 varies with the input vectors of G4, G5 and G6. The additional leakage reduction can be achieved by pin reordering (forcing those inputs to "10"). Therefore, it is critical to set the minimal leaky state in different gate input states under the same input combination (e.g., input (01) and (10) in NAND2 gate has same input combination: one high and one low).

Several research efforts [44]-[46] related to transistor reordering have been conducted and reported. The main goal of these techniques is to minimize the dynamic power consumption under delay constraints in active mode instead of reducing the leakage power in standby mode. Lee *et al*. [3] proposed the pin reordering technique combined with IVC to reduce the gate leakage in standby mode. In this approach, the effects of pin reordering on pull-up network of CMOS circuits are not considered. This leads to misleading results when the

concept of this approach is extended to a pull-up network. Since this approach focus on the gate leakage reduction in pull-down network, it did not provide any details or information regarding pin reordering rule for pull-up network, and pin reordering effects on subthreshold leakage. Furthermore, there are limitations of using the pin reordering in complex CMOS logic gates, which will be discussed in later in this chapter.

For this reason, better understanding and more accurate method of pin reordering is essential. In this chapter, we present complete pin reordering rules for CMOS circuits by including the pull-up network. For the first time, we comprehensively analyze the pin reordering effects on both gate and subthreshold leakage current in different conditions (stacking effect and non-stacking effect), and define the three effects of pin reordering on leakage reduction. In this wok, we provide a direct and accurate method for implementing a minimal leaky structure in CMOS logic gates by pin reordering, which leads to reducing the overall leakage dissipation of a CMOS circuit.

The rest of this chapter is organized as follows. First, we analyze the effect of pin reordering on gate and subthreshold leakage, and then provide the minimal leaky structure in different gate input states under the same input combination of

typical CMOS logic gates, such as NAND, NOR, XOR, XNOR, AOI and OAI, to enhance the leakage power reduction in CMOS circuits.

4.2 Leakage Reduction through Pin Reordering

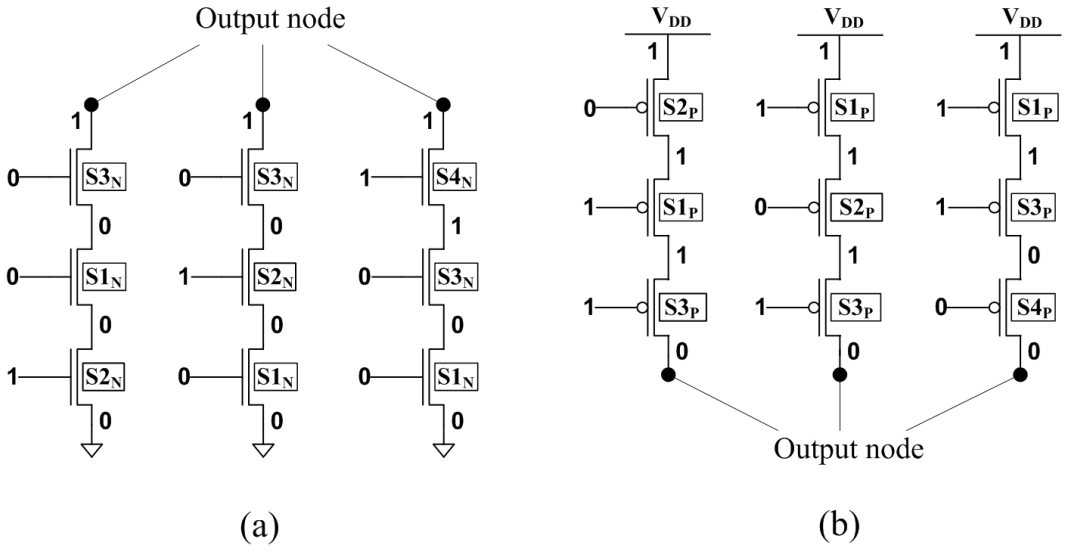

Figure 21: Steady states in off-state network: (a) NMOS (b) PMOS.

Both NAND and NOR gates consist of a parallel structure and a serial structure. For example, in a NAND gate, PMOS part has a parallel structure and NMOS part has a serial structure. When input vectors include both 1 and 0, then the only conducting network (i.e., the on-state network) in NAND or NOR gates will be in the parallel part of the gates. Transistors of off-state network are connected in series and thus only one transistor will be in the subthreshold leaky

state. To illustrate this, consider an NMOS/PMOS transistor stack in the pull-down/pull-up of a 3-input NAND/NOR gate, as illustrated in Figure 21. In this example, NMOS/PMOS transistors of off-state network are connected in series; the first nonconducting transistor from output node will be in the subthreshold leaky state (S_{SUB}: $S3_N$ and $S3_P$), and rest of nonconducting transistor will be in the least leaky state (S_{LEAST} : $S1_N$ and $S1_P$).

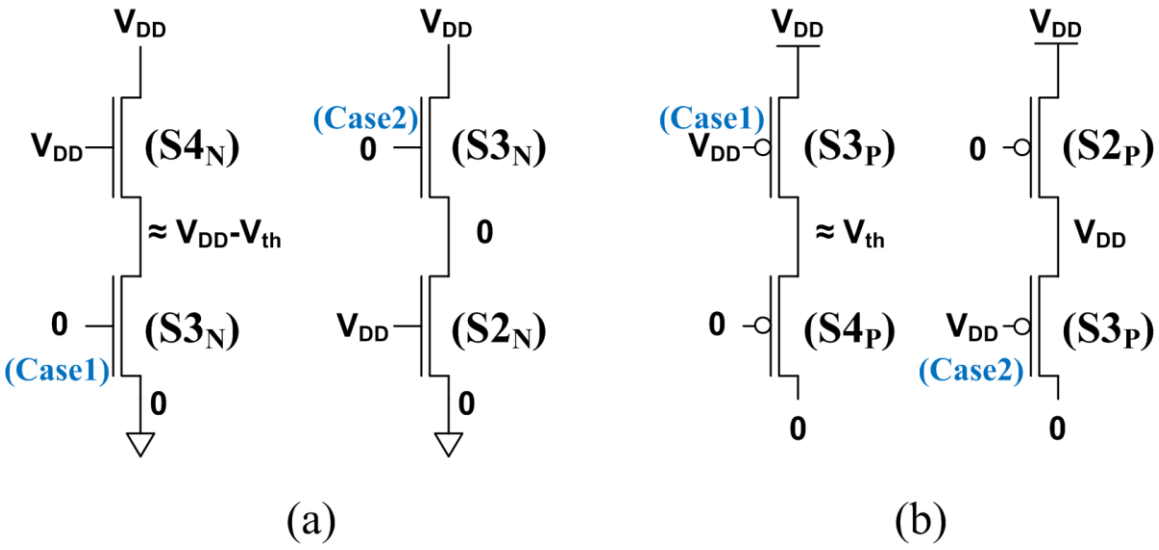

Figure 22: Comparison of Steady states in two transistor stacks with different input vectors: (a) Pull-down (b) Pull-up.

Under different gate input states in off-state network, S_{SUB} ($S3_N$ and $S3_P$) can be divided into two cases based on correlation with conducting transistor. To

demonstrate this, consider the series-connected parts of a NAND or NOR gates, which are in off-state when with input vector "10" and "01" as shown in Figure 22. The following is an elucidation of the two cases in S_{SUB} for an NAND gate and a NOR gate.

- For NAND gate:
  (1) Case 1 (when input vector = 10): For the transistor in state $S3_N$, when $S3_N$ is located other than top in transistor stacks of pull-down network, the drain voltage (V_D) of $S3_N$ is approximately V_{DD}-V_{th}.
  (2) Case 2 (when input vector = 01): For the transistor in state $S3_N$, when $S3_N$ is located on the top in transistor stacks of pull-down network, the drain voltage (V_D) of $S3_N$ is V_{DD}.

- For NOR gate:
  (1) Case 1 (when input vector = 10): For the transistor in state $S3_P$, when $S3_P$ is located other than bottom in transistor stacks of pull-up network, the drain voltage (V_D) of $S3_P$ is approximately V_{th}.
  (2) Case 2 (when input vector = 01): For the transistor in state $S3_P$, when $S3_P$ is located on the bottom in transistor stacks of pull-down network, the drain voltage (V_D) of $S3_P$ is 0.

When the source node voltage (V_S) of case1 and case2 has the same in $S3_N$/$S3_P$, leakage current of S_{SUB} in Case1 (S_{SUB1}) is less than that of S_{SUB} in Case2 (S_{SUB2}) since the V_{DS} and V_{GD} of S_{SUB2} are approximately V_{th} higher than S_{SUB1} as shown in Figure 23.

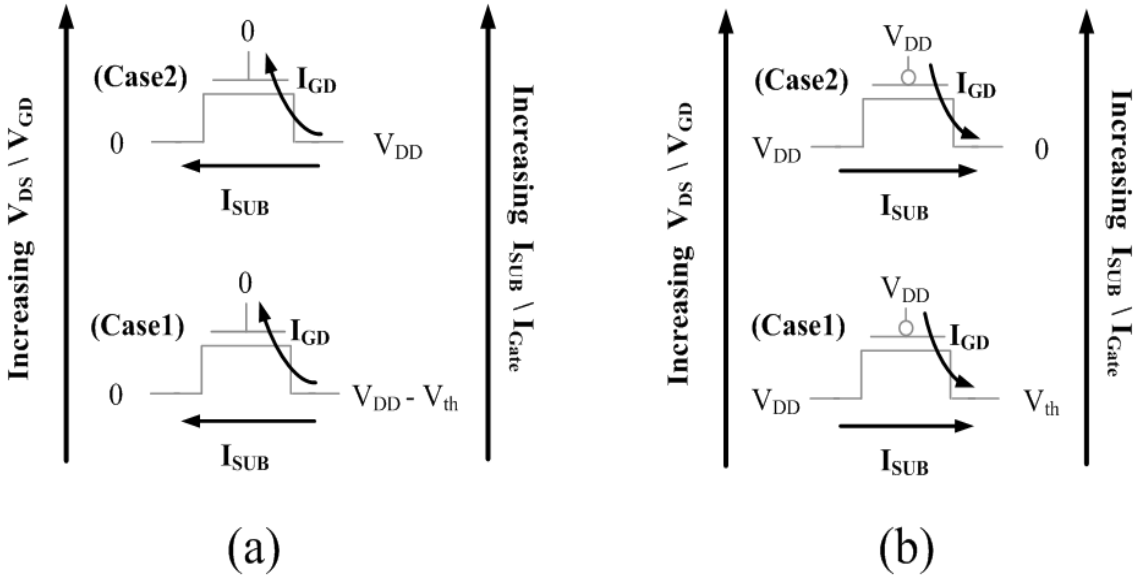

Figure 23: Leakage comparison of S_{SUB} in different bias voltage conditions: (a) NMOS ($S3_N$) (b) PMOS ($S3_P$).

In a similar way, under different gate input states in off-state network, there are two types of conducting transistors (S_{GATE} ($S2_P$/$S2_N$) and S_{LG} ($S4_P$/$S4_N$)); the state type (S_{GATE} /S_{LG}) depends on correlation with S_{SUB}. The S_{GATE} presents when conducting transistor is located below (above) the S_{SUB} in pull-down (pull-up)

network, whereas the S_{LG} presents when conducting transistor is located above (below) the S_{SUB} in pull-down (pull-up) network (see Figure 21 and Figure 22). Note that S_{LG} leak significantly less than S_{GATE}, typically 3 to 6 orders of magnitude less, since magnitude of the gate leakage is a strong function of the applied bias [6].

Figure 24 depicts the behavior of the gate leakage response for bias voltage between nodes (V_{GS}, V_{GD} and V_{GB}) in conducting transistors. Noted that in Figure 24, the second-smallest leaking state ($V_D=V_S \approx V_{DD}-V_{th}$ ($\approx V_{th}$) in $S4_N$ ($S4_P$)) presents when more than one conducting transistors located above (below) the S_{SUB} in stacks. In addition, second-highest leaking state ($V_D=V_S \approx 100mV$ ($\approx V_{DD}-100mV$) in $S2_N$ ($S2_P$)) presents when conducting transistor located between non-conducting transistors.

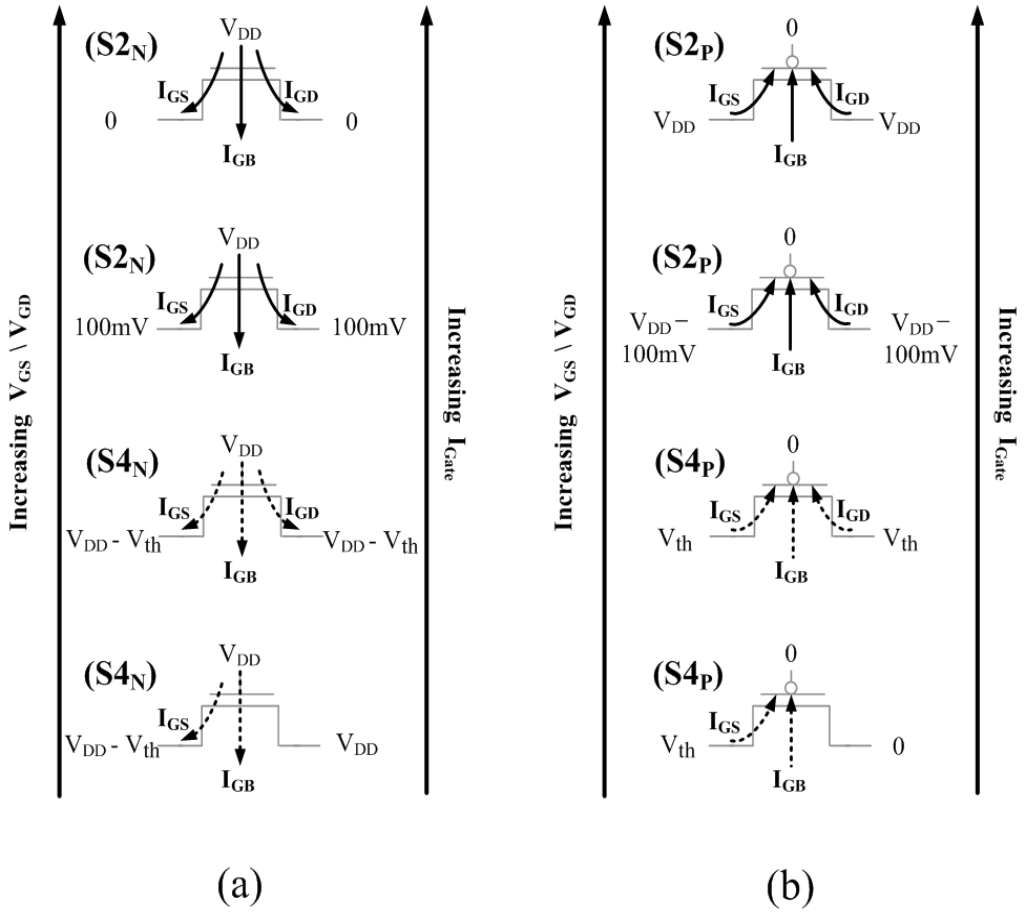

Figure 24: Leakage comparison of conducting transistors: (a) NMOS (b) PMOS.

Table 8: Leakage current (nA) of two transistor stacks with different input vectors.

Network	Input	State	Type	I_{SUB}	I_G	I_{TOTAL}	$\lvert V_{DS} \rvert$	$\lvert V_{GS} \rvert$	$\lvert V_{GD} \rvert$
PDN (a)	01	$S3_N$	S_{SUB2}	15.229	1.017	20.358	1.1	0	1.1
		$S2_N$	S_{GATE}	0	4.112		0	1.1	1.1
	10	$S4_N$	S_{LG}	0	0.002	7.191	0.253	0.253	0
		$S3_N$	S_{SUB1}	6.961	0.228		0.847	0	0.847
PUN (b)	01	$S2_P$	S_{GATE}	0	0.030	24.01	0	1.1	1.1
		$S3_P$	S_{SUB2}	23.965	0.015		1.1	0	1.1
	10	$S3_P$	S_{SUB1}	9.150	0.005	9.155	0.853	0	0.247
		$S4_P$	S_{LG}	0	0		0.247	0.247	0

Table 8 lists the corresponding leakage currents and bias voltage of Figure 22 (two transistor stacks with different gate input states). The data shown in Table 8 are conducted by Synopsys HSPICE simulator that invokes the default 65nm Predictive Technology Model (PTM) [42]. In this chapter, all simulation data are conducted by HSPICE using the default 65nm PTM at room temperature, and the W/L and P/N ratio are designed as 4 and 2, respectively. It is noteworthy to note that gate leakage of $S3_N$ is a reverse gate leakage (reverse gate tunneling current), which has the same order of magnitude in forward gate tunneling current ($S2_N$). It can be observed that the leakage currents corresponding to input vector "10" and to "01" are very different due to the following reasons:

- I_{SUB} in "10" far less leaky than that in "01" because the V_{DS} of $S3_N$/$S3_P$ with input "10" is approximately V_{th} less than that in "01"; When the input vector is "10" in pull-down (pull-up) network, the value of internal node voltage is V_{DD}-V_{th} (V_{th}), whereas, when the input vector is "01" in pull-down (pull-up) network, the value of internal node voltage is zero (V_{DD}) due to the conducting path to the ground (Power supply).

- I_G in "10" significantly less than that in "01"; V_{GD} of $S3_N/S3_P$ with input "10" is approximately V_{th} less than that in "01". Furthermore, I_G in $S4_N/S4_P$ with "10" is considerably (3 orders of magnitude) less than that in $S2_N/S2_P$ with "01".

For this reason, leakage reduction can be achieved by pin reordering; conducting (nonconducting) transistor(s) of series-connected transistors in off-state pull-down (pull-up) network located above the nonconducting (conducting) transistor(s), and thereby leakage current can be minimized by replacing S_{GATE} ($S2_N/S2_P$) and S_{SUB2} with S_{LG} ($S4_N/S4_P$) and S_{SUB1} , respectively.

In other words, pin reordering technique formulates the minimal leaky steady state in certain input combination by eliminating gate leaky state; replacing the S_{GATE} with S_{LG}, results in S_{SUB} change from S_{SUB2} to S_{SUB1} .

It should be note that the previous pin reordering approach [3] (place the all conducting transistors on above the non-conducting transistors) only valid in the pull-down network since this approach focus on gate leakage reduction of pull-down network. Thus, we propose a reordering rule for leakage reduction in pull-up network; that is, place the all non-conducting transistors on above the conducting transistors.

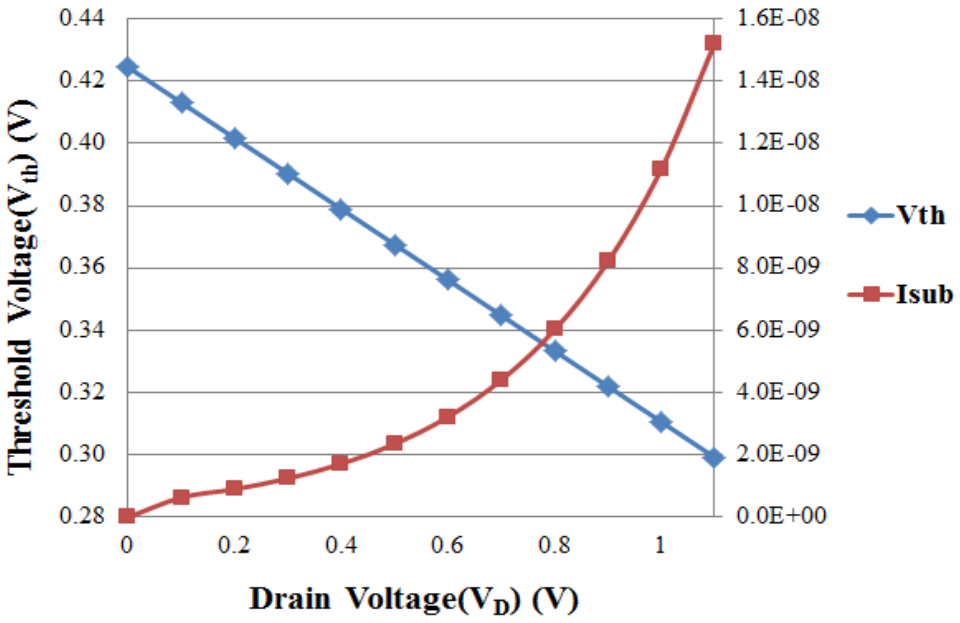

Figure 25: Leakage current and threshold voltage trends as a function of V_D in $S3_N$ with V_G= V_S=V_B=0, V_{DD}=1.1 and W/L=4 in 65nm technology. The unit of right side of Y-axis is Ampere (A).

Following is a summary of the effects of the pin reordering on leakage reduction:

(1) Reduced the drain-to-source voltage (V_{DS}) in S_{SUB} ($S3_N$/$S3_P$), which causes its threshold voltage to increase due to the less DIBL. Thus the subthreshold leakage reduced (see Figure 25).

(2) The gate-to-drain voltage (V_{GD}) in S_{SUB} ($S3_N$/$S3_P$) decreased, and thus the reverse gate tunneling leakage reduced.

(3) S_{GATE} replaced with S_{LG} , gate leakage reduced considerably; S_{LG} typically 3 to 6 orders of magnitude less than S_{GATE} .

4.2.1 A MOS Transistor Stacks in Off-state Network

Now, we use the three transistor stacks in pull-down/pull-up network as typical examples to analyze and compare the effects of pin reordering on stacking and non-stacking effect cases. There are two possible input combinations in three transistor stacks under different gate input states; the first one consists of two conducting and one nonconducting transistors (non-stacking effect case), and the second one consists of one conducting and two nonconducting transistors (stacking effect case).

4.2.1.1 Non-Stacking Effect Case

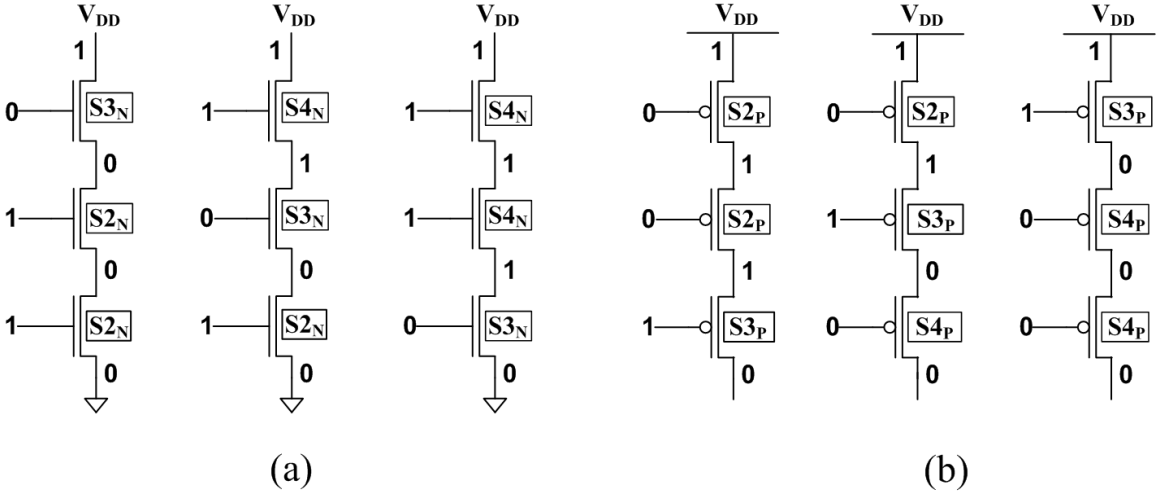

Figure 26: Possible input vectors of non-stacking effect case in three transistor stacks in different gate input states: (a) PDN (NMOS) (b) PUN (PMOS).

Let us consider the non-stacking input combination in three transistor stacks; only one off-transistor presents in transistor stacks. In this condition, source voltage (V_S) of $S3_N$ ($S3_P$) is zero (V_{DD}) even though $S3_N$ ($S3_P$) located other than bottom (top) of the transistor stacks since there is always conducting path to the ground (power supply) as shown in Figure 26.

Table 9: Leakage current (nA) and node voltage (V) for three transistor stacks with different input vectors in non-stacking effect case.

Network	Input	State	Type	I_{SUB}	I_G	I_{TOTAL}	V_D	V_G	V_S
PDN (a)	011	$S3_N$	S_{SUB2}	15.208	1.017	24.449	1.1	0	0
		$S2_N$	S_{GATE}	0	4.112		0	1.1	0
		$S2_N$	S_{GATE}	0	4.112		0	1.1	0
	101	$S4_N$	S_{LG}	0	0.002	11.299	1.1	1.1	0.847
		$S3_N$	S_{SUB1}	6.958	0.227		0.847	0	0
		$S2_N$	S_{GATE}	0	4.112		0	1.1	0
	110	$S4_N$	S_{LG}	0	0.002	6.552	1.1	1.1	0.849
		$S4_N$	S_{LG}	0	0.005		0.849	1.1	0.817
		$S3_N$	S_{SUB1}	6.356	0.189		0.817	0	0
PUN (b)	001	$S2_P$	S_{GATE}	0	0.030	24.009	1.1	0	1.1
		$S2_P$	S_{GATE}	0	0.030		1.1	0	1.1
		$S3_P$	S_{SUB2}	23.934	0.015		0	1.1	1.1
	010	$S2_P$	S_{GATE}	0	0.030	9.181	1.1	0	1.1
		$S3_P$	S_{SUB1}	9.146	0.005		0.247	1.1	1.1
		$S4_P$	S_{LG}	0	7.3E-5		0	0	0.247
	100	$S3_P$	S_{SUB1}	8.029	0.004	8.033	0.280	1.1	1.1
		$S4_P$	S_{LG}	0	1.7E-4		0.243	0	0.280
		$S4_P$	S_{LG}	0	7.1E-5		0	0	0.243

Table 10: Leakage current (nA) for $S3_{N/P}$ in different bias voltages (V).

Network	Input	Type	V_{DS}	$\lvert V_{GD} \rvert$	Vth	I_{TOTAL}
PDN	011	S_{SUB2}	1.1	1.1	0.299	16.225
	101	S_{SUB1}	0.847	0.847	0.328	7.185
	110	$\boldsymbol{S_{SUB1}}$	**0.817**	**0.817**	**0.331**	**6.545**
PUN	001	S_{SUB2}	1.1	1.1	0.212	23.949
	010	S_{SUB1}	0.853	0.853	0.246	9.151
	100	$\boldsymbol{S_{SUB1}}$	**0.820**	**0.820**	**0.251**	**8.033**

Table 9 lists the gate leakage current, subthreshold leakage current, total leakage current and node voltage for three transistor stacks in pull-down/pull-up network. As expected, the simulation shows that lowest leakage input vector of pull-down (pull-up) network is "110" ("100") which does not contain the S_{SUB2} and S_{GATE}, whereas input "011" ("001") is the worst case since each node (V_D, V_G and V_S) in steady states contains the full logic value (either V_{DD} or 0). Note that among S_{SUB1} cases, the input "110" ("100") in $S3_N$ ($S3_P$) exhibits least leakage because the V_{GD} and V_{DS} of this case has least value as shown in Table 10. In Table 10, the lowest leakage for each network is in bold.

4.2.1.2 Stacking Effect Case

Stacking effect occurs when more than one transistor in the stack is "OFF". In this formation, unlike in non-stacking effect case, V_S of $S3_N$ is not zero but

positive potential ($V_S > 0$), and V_S of $S3_P$ is not V_{DD} but less than supply voltage ($V_S < V_{DD}$); this phenomenon known as stacking effect. As aforementioned, this effect considerably reduces the subthreshold leakage. For example, when V_S of $S3_N$ has positive potential, the gate-to-source voltage (V_{GS}) becomes negative (reverse biased) and threshold voltage increase due to the larger body effect (body-to-source voltage (V_{BS}) becomes negative) and less DIBL effect (drain-to-source voltage (V_{DS}) reduced) than non-stacking case (V_S=0). As seen in Figure 27 and Table 11, the increase of V_S in $S3_N$ reduces the subthreshold leakage.

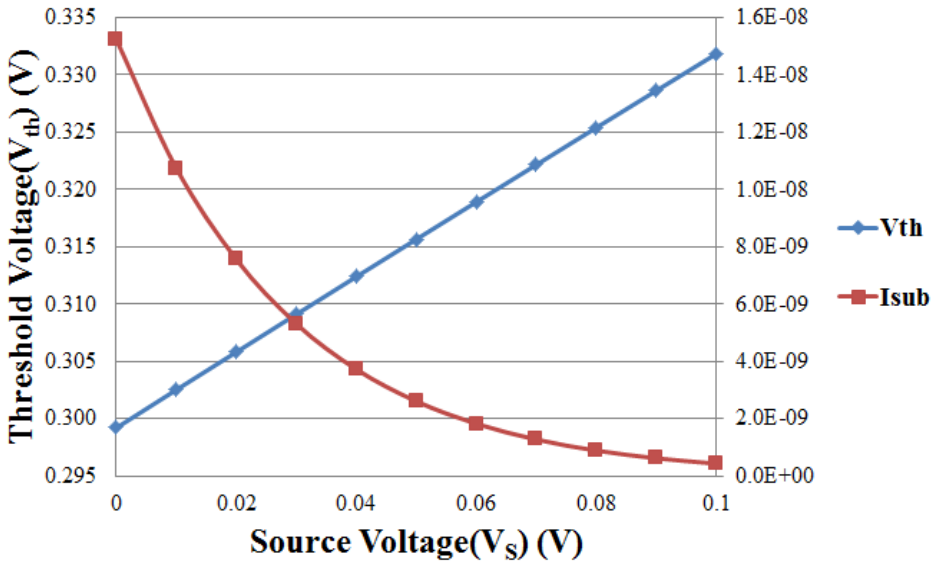

Figure 27: Leakage current and threshold voltage trends as a function of V_S in $S3_N$ with V_G=V_B=0, V_D= V_{DD}=1.1V and W/L=4 in 65nm technology. The unit of right side of Y-axis is Ampere (A).

Table 11: Variation of threshold voltage (V) and subthreshold leakage current (nA) with source voltage (V) in $S3_N$: V_G=V_B=0, V_D=V_{DD}=1.1V and W/L=4 in 65nm technology.

V_D	V_G	V_S	V_{DS}	V_{GS} / V_{BS}	Vth	I_{SUB}
1.1	0	0	1.1	0	0.299	15.229
1.1	0	0.01	1.09	-0.01	0.303	10.741
1.1	0	0.02	1.08	-0.02	0.306	7.559
1.1	0	0.03	1.07	-0.03	0.309	5.308
1.1	0	0.04	1.06	-0.04	0.312	3.720
1.1	0	0.05	1.05	-0.05	0.316	2.603
1.1	0	0.06	1.04	-0.06	0.319	1.818
1.1	0	0.07	1.03	-0.07	0.322	1.268
1.1	0	0.08	1.02	-0.08	0.325	0.883
1.1	0	0.09	1.01	-0.09	0.329	0.614
1.1	0	0.10	1.00	-0.10	0.332	0.427

To analyze pin reordering effect on stacking case, we use a three transistor stacks with certain input combinations which consist of two nonconducting (off) and one conducting(on) transistors as shown in Figure 21. Table 12 lists the gate leakage current, subthreshold leakage current and total leakage current in different input vectors along with node voltage in each transistor for NMOS/PMOS three transistors stacks in stacking case. Simulation verifies the prediction that "100" and "110" are the lowest leakage input vectors in pull-down network and pull-up network, respectively; those vectors do not have S_{GATE} and S_{SUB2}.

Table 12: Leakage current (nA) and node voltage (V) for three transistor stacks with different input vectors in stacking effect case.

Network	Input	State	Type	I_{SUB}	I_G	I_{TOTAL}	V_D	V_G	V_S
PDN (a)	001	S3	S_{SUB2}	0.613	1.017	6.355	1.1	0	0.09
		S1	S_{LEAST}	0.613	0		0.09	0	0
		S2	S_{GATE}	0	4.112		0	1.1	0
	010	S3	S_{SUB2}	0.613	1.017	5.407	1.1	0	0.09
		S2	S_{GATE}	0	3.162		0.09	1.1	0.09
		S1	S_{LEAST}	0.613	0.002		0.09	0	0
	100	S4	S_{LG}	0	0.001	1.467	1.1	1.1	0.903
		S3	S_{SUB1}	0.572	0.322		0.903	0	0.075
		S1	S_{LEAST}	0.572	9.2E-05		0.075	0	0
PUN (b)	011	S2	S_{GATE}	0	0.030	0.938	1.1	0	1.1
		S1	S_{LEAST}	0.444	1.0E-05		0.990	1.1	1.1
		S3	S_{SUB2}	0.449	0.015		0	1.1	0.990
	101	S1	S_{LEAST}	0.444	1.0E-05	0.926	0.990	1.1	1.1
		S2	S_{GATE}	0	0.018		0.990	0	0.990
		S3	S_{SUB2}	0.449	0.015		0	1.1	0.990
	110	S1	S_{LEAST}	0.410	7.0E-06	0.826	1.006	1.1	1.1
		S3	S_{SUB1}	0.410	0.006		0.164	1.1	1.006
		S4	S_{LG}	0	2.5E-05		0	0	0.164

It should be noted that the subthreshold leakage current of off-transistors ($S3_N$ and $S1_N$) in stacking case is almost identical. This is due to the fact that the same amount of subthreshold leakage current flows through all the transistors in the path. The subthreshold leakage equation (1) can be simplified to the following form,

$$I_{SUB} = \mu \frac{W_{eff}}{L_{eff}} \sqrt{\frac{q\varepsilon_{si}N_a}{2\Phi_s}} {V_T}^2 \; B \; C \tag{5}$$

$$\text{where} \quad B = \left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \text{ and } C = \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)$$

In equation (5), subthreshold leakage depends primarily on the V_{DS}, V_{th} and V_{GS}, when temperature is fixed at room temperature (standby mode); hence, the thermal voltage is 0.02585(V). Note that the effect of V_{DS} on V_{th} is involved with C term, while V_{DS} in B term is not an important factor in subthreshold lekage equation as shown in Table 13. Therefore, V_{GS} and V_{th} are the two dominant factors in subthreshold equation. In stacking effect case, subthreshold leakage current of S_{SUB} is about the same as S_{LEAST} because the V_{GS}-V_{th} of S_{SUB} is almost identical as S_{LEAST} as listed in Table 13.

Table 13: The main factors of the subthreshold leakage for PDN three transistor stacks with different gate input states in stacking effect case.

Input	Type	V_{DS}	V_{GS}	V_{th}	V_{GS} -V_{th}	B	C
001	S_{SUB2}	1.01	-0.09	0.329	-0.419	1	1.98E-04
	S_{LEAST}	0.090	0.000	0.414	-0.414	0.969	2.18E-04
010	S_{SUB2}	1.01	-0.09	0.329	-0.419	1	1.98E-04
	S_{LEAST}	0.090	0.000	0.414	-0.414	0.969	2.18E-04
100	S_{SUB1}	0.828	-0.075	0.346	-0.421	1	1.90E-04
	S_{LEAST}	0.075	0.000	0.416	-0.416	0.944	2.10E-04

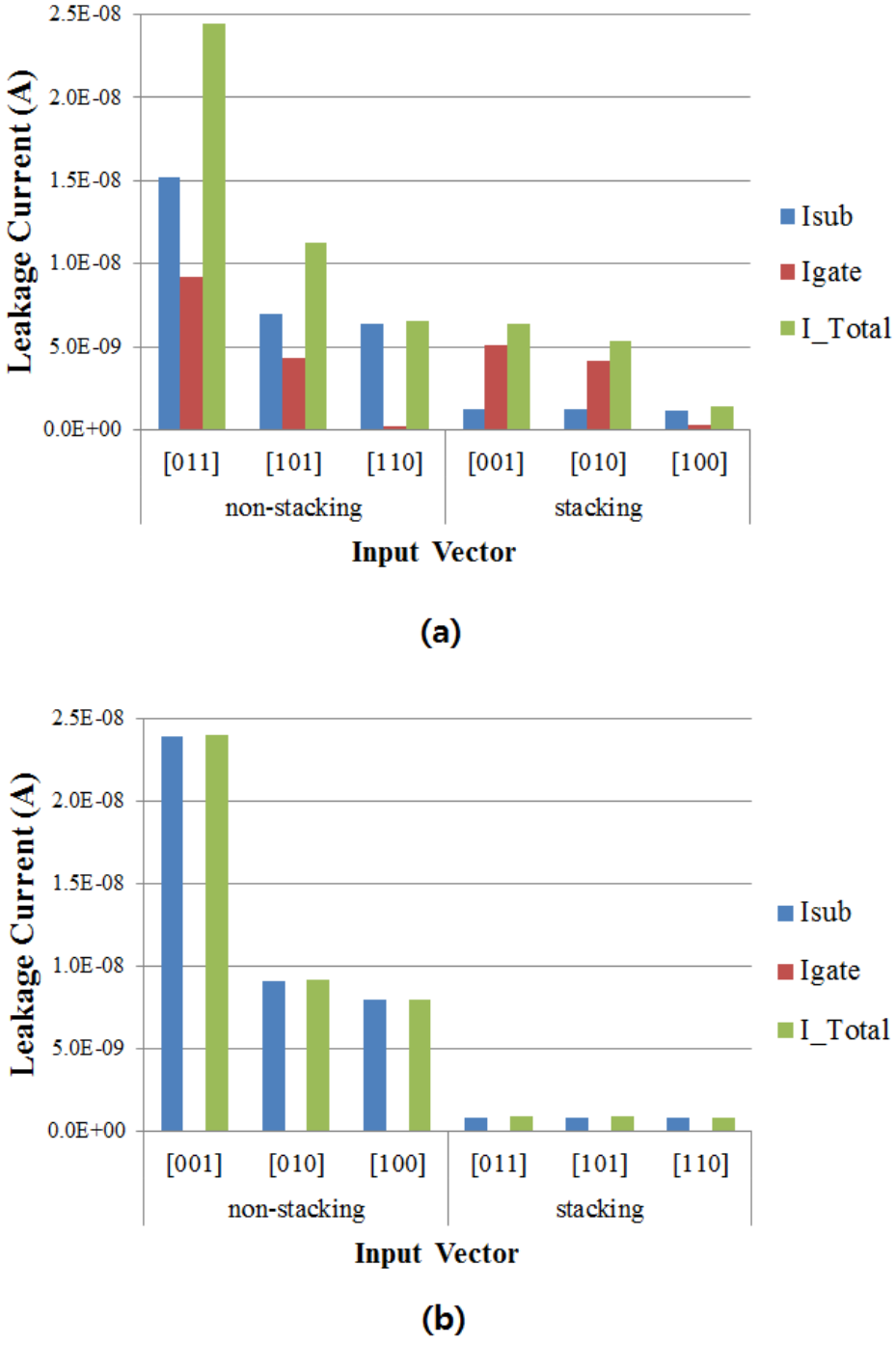

Figure 28: Variation of leakage current with different input vectors for a stack of three transistors. (a) Pull-down network. (b) Pull-up network.

Figure 28 shows the variation of leakage current with different input vectors for three transistors stack. Table 14 shows the leakage savings in subthreshold, gate and total leakage current with application of pin reordering for three transistors stacks. It can be observed that pull-down network (PDN) obtains more leakage savings than pull-up network (PUN) from pin reordering due to the ratio of gate leakage to total leakage as shown in Table 15. Typically, gate leakage for the PMOS transistor is an order of magnitude lower than for the NMOS transistor when using SiO2 [47] due to the higher tunneling barrier height for holes (4.5eV) than for electrons (3.1eV) [48]. In case of 65nm PTM, the gate leakage for the PMOS transistor is two orders of magnitude lower than for the NMOS transistor as shown in Table 9 and Table 12.

Table 14: Leakage savings and saving ratio with application of pin reordering for leakage reduction in three transistors stacks.

Network	Stacking effect	Pin reordering	Leakage Savings (%)			Saving Ratio (%)	
			I_{SUB}	I_G	I_{TOTAL}	I_{SUB}	I_G
PDN	Non-stacking	[011] → [110]	58.21	97.88	73.20	49.46	50.54
		[101] → [110]	8.65	95.48	42.01	12.68	87.32
	Stacking	[001] → [100]	6.69	93.70	76.92	1.68	98.32
		[010] → [100]	6.69	92.27	72.87	2.08	97.92
PUN	Non-stacking	[001] → [100]	66.45	94.67	66.54	99.56	0.44
		[010] → [100]	12.21	88.57	12.50	97.30	2.70
	Stacking	[011] → [110]	8.17	86.67	11.94	65.18	34.82
		[101] → [110]	8.17	81.82	10.80	73.00	27.00

Table 15: A comparison of leakage ratio between subthreshold and gate leakage in stacking and non-stacking cases with different gate input states in three transistors stacks.

Network	Stacking effect	Input	Leakage ratio (%)	
			I_{SUB}	I_G
PDN	Non-stacking	[011]	62.20	37.80
		[101]	61.58	38.42
	Stacking	[001]	19.29	80.71
		[010]	22.67	77.33
PUN	Non-stacking	[001]	99.69	0.31
		[010]	99.62	0.38
	Stacking	[011]	95.20	4.80
		[101]	96.44	3.56

For this reason, compared to PDN, PUN, where the contribution of gate leakage is much smaller than that of PDN, does not take full advantage of pin reordering effect on leakage reduction since the contribution of gate leakage reduction through pin reordering does not reflect the overall leakage savings. As seen in Figure 28, subthreshold leakage reduced considerably by stacking effect, and thus saving ratio of gate leakage in stacking case is higher than non-stacking case as listed in Table 14.

4.2.2 A Combination of Serial and parallel MOS Structures in Off-state Network

For the evaluation of the effect of pin reordering on leakage reduction in complex logic gates, we use an off-state network of typical complex CMOS logic gates such as exclusive-or (XOR), exclusive–nor (XNOR), and-or-inverter (AOI) and or-and-inverter (OAI).

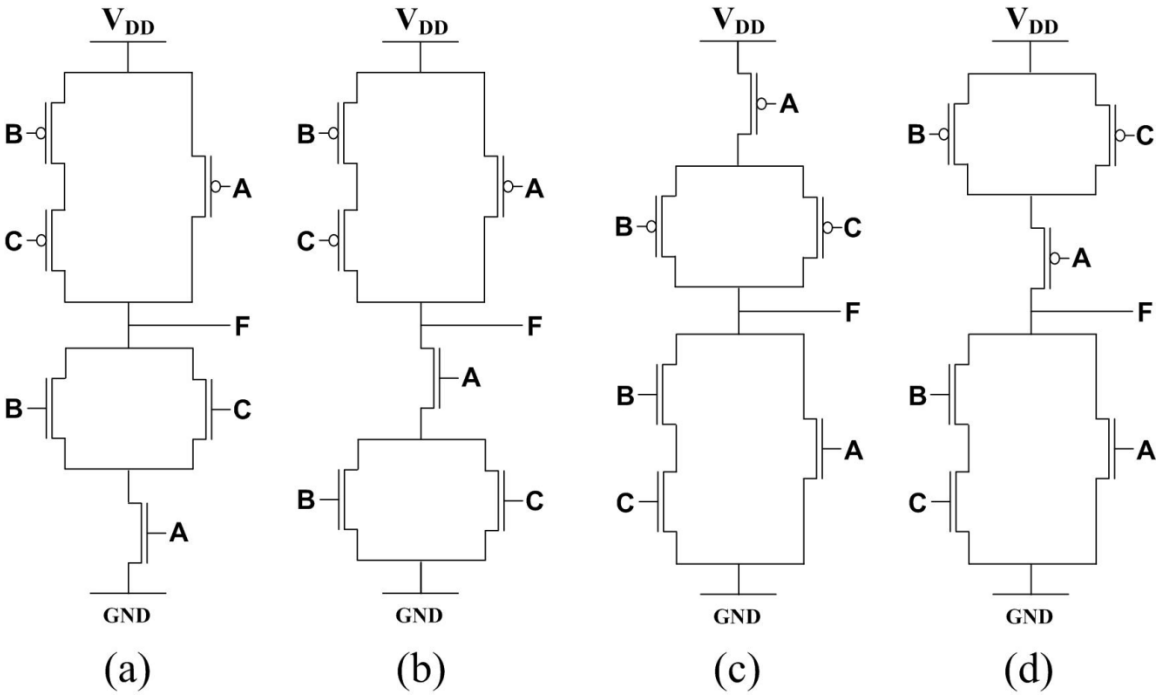

Figure 29: 3-input OAI-21 ($F = \overline{A\ (B + C)}$) gate with different pull-down structures ((a) Type1, (b) Type2), and 3-input AOI-21 ($F = \overline{A + BC}$) gate with different pull-up structures ((c) Type1, (d) Type2).

Table 16: Leakage current (nA) and steady state components for AOI-21 and OAI-21 logic gates in off-state network with different input vectors under different gate input states.

Gate type	Off-state network	Input (ABC)	Structure type	States (ABC)	State type (ABC)	I_{TOTAL}
OAI-21	PDN	001	**Type1**	**S3 S5 S4**	$\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{RG}}$ $\boldsymbol{S_{LG}}$	**8.413**
			Type2	S3 S1 S2	S_{SUB2} S_{LEAST} S_{GATE}	20.347
		010	**Type1**	**S3 S4 S5**	$\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{LG}}$ $\boldsymbol{S_{RG}}$	**8.413**
			Type2	S3 S2 S1	S_{SUB2} S_{GATE} S_{LEAST}	20.347
		011	**Type1**	**S3 S4 S4**	$\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{LG}}$ $\boldsymbol{S_{LG}}$	**7.604**
			Type2	S3 S2 S2	S_{SUB2} S_{GATE} S_{GATE}	24.459
		100	Type1	S2 S3 S3	S_{GATE} S_{SUB2} S_{SUB2}	36.558
			Type2	**S4 S3 S3**	$\boldsymbol{S_{LG}}$ $\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{SUB1}}$	**13.587**
	PUN	101	Both types	S3 S2 S3	S_{SUB2} S_{GATE} S_{SUB2}	48.008
		110		**S3 S3 S4**	$\boldsymbol{S_{SUB2}}$ $\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{LG}}$	**33.162**
AOI-21	PUN	011	Type1	S2 S3 S3	S_{GATE} S_{SUB2} S_{SUB2}	47.917
			Type2	**S4 S3 S3**	$\boldsymbol{S_{LG}}$ $\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{SUB1}}$	**17.088**
		100	**Type1**	**S3 S4 S4**	$\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{LG}}$ $\boldsymbol{S_{LG}}$	**9.796**
			Type2	S3 S2 S2	S_{SUB2} S_{GATE} S_{GATE}	24.056
		101	**Type1**	**S3 S4 S5**	$\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{LG}}$ $\boldsymbol{S_{RG}}$	**9.173**
			Type2	S3 S2 S1	S_{SUB2} S_{GATE} S_{LEAST}	24.010
		110	**Type1**	**S3 S5 S4**	$\boldsymbol{S_{SUB1}}$ $\boldsymbol{S_{RG}}$ $\boldsymbol{S_{LG}}$	**9.173**
			Type2	S3 S1 S2	S_{SUB2} S_{LEAST} S_{GATE}	24.010
	PDN	001	Both types	S3 S3 S2	S_{SUB2} S_{SUB2} S_{GATE}	36.605
		010		**S3 S4 S3**	$\boldsymbol{S_{SUB2}}$ $\boldsymbol{S_{LG}}$ $\boldsymbol{S_{SUB1}}$	**23.431**

Figure 29 shows the different implementations of OAI-21 ($F = \overline{A\ (B + C)}$) and AOI-21 ($F = \overline{A + (BC\ )}$) gate.

In OAI gate ($F = \overline{A \text{ and } (B \text{ or } C)}$), if the "or" components (input B and C in Figure 29(a) and (b)) consider as one single transistor, the logical function of OAI-21 gate is the same as NAND2 gate since the part of AND-Inverter in OAI gate is replaceable with NAND gate. Hence, pull-down network of OAI-21 gate is off-state under different gate input states, when either the "or" function or the other input (input A) is zero; under different gate input states, there is an one possible input existed for "or" function in zero case which input vector (ABC) is "100", while there are three possible inputs existed for the other case (A=0), those inputs (ABC) are "001", "010" and "011". In addition, pull-up network of OAI-21 gate is off-state under different gate input states when input A is high along with one of "or" function inputs is high, which inputs (ABC) are "101" and "110".

In a similar way, logical function of AOI-21 ($F = \overline{A \text{ or } (B \text{ and } C\ )}$) gate is the same as NOR2 gate when "and" function (input B and C in Figure 29(c) and (d)) in AOI gate consider as one single transistor since the part of OR-Inverter in AOI gate is replaceable with NOR gate. Hence, pull-up network of AOI-21 gate is off-state under different gate input states when either the "and" function or the

other input (input A) is high (V_{DD}); under different gate input states, there is an one possible input existed for "and" function in high case which input vector (ABC) is "011", while there are three possible inputs existed for the other case (A=V_{DD}), those inputs (ABC) are "100", "101" and "110". The pull-down network of AOI-21 gate is off-state under different gate input states when input A is low along with one of inputs in "or" function is low, which inputs (ABC) are "001" and "010". Table 16 lists the leakage current and steady state components for AOI-21 and OAI-21 logic gates in off-state network.

In off-state pull-down (pull-up) network of OAI-21 (AOI-21) gate, Type 1 structure do not present the S_{SUB2} and S_{GATE} other than input "100" ("011") case, and hence less leaky than Type 2 structure other than input 100 ("011") case, while Type 2 structure do not present the S_{SUB2} and S_{GATE} only when input "100" ("011") case, resulting in less leaky than Type 1 structure.

In off-state pull-up (pull-down) network of OAI-21 (AOI-21) gate, input "110"("010") is less leaky than input "101"("001") due to the steady states of input B and C; steady states of B and C in "110"("001") are S_{SUB1} and S_{LG} respectively, while steady states of B and C in "101"("001") are S_{SUB2} and S_{GATE} respectively.

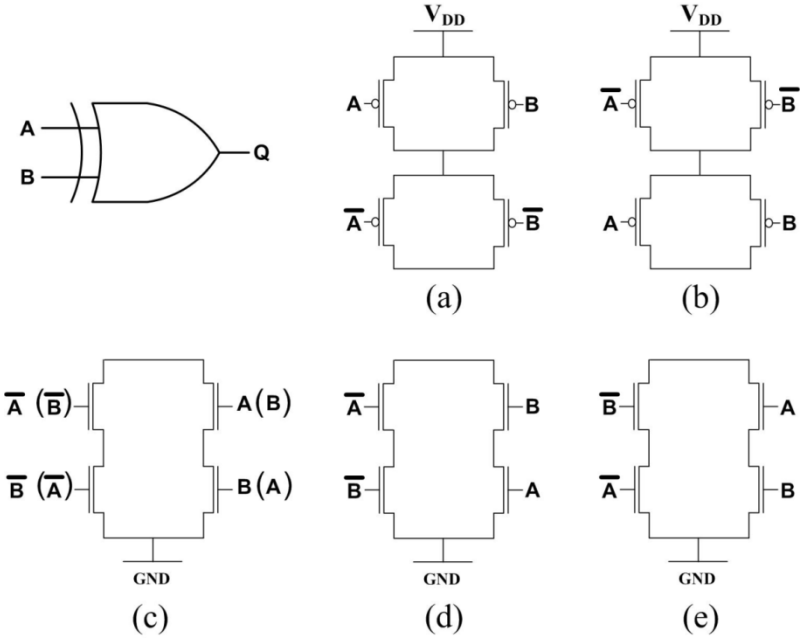

Figure 30: 2-input XOR gate ($Q = \overline{\overline{A}\overline{B} + AB}$) with different input positions in PUN ((a) Type1, (b) Type2) and PDN ((c) Type3, (d) Type4, (e) Type5).

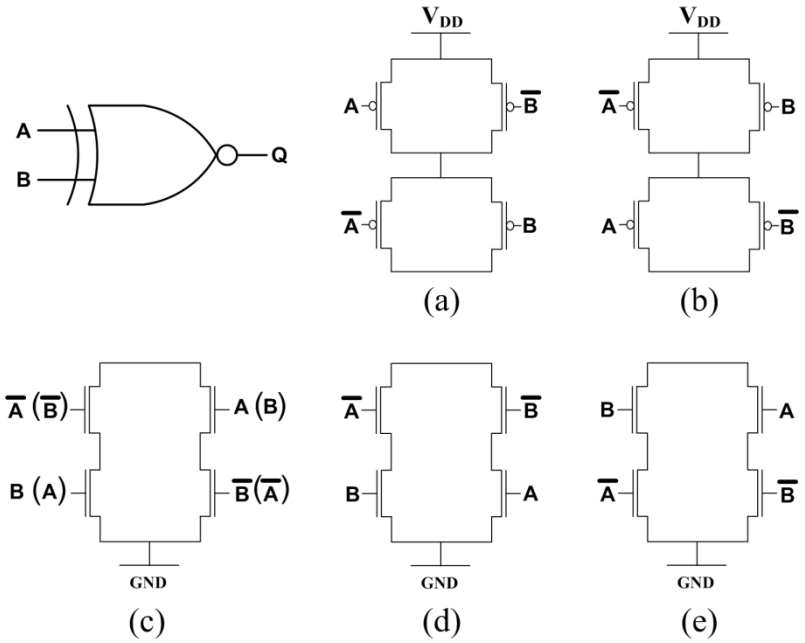

Figure 31: 2-input XNOR gate ($Q = \overline{\overline{A}B + A\overline{B}}$) with different input positions in PUN ((a) Type1, (b) Type2) and PDN ((c) Type3, (d) Type4, (e) Type5).

Table 17: Leakage current (nA) and steady state components for XOR (XNOR) logic gate in off-state network with different input vectors.

Off-state	Input: XOR (XNOR)	Structure type	Steady states (A B $\overline{A}$ $\overline{B}$)				Steady state type (A B $\overline{A}$ $\overline{B}$)				I_{TOTAL}
PUN	00 (01)	Type1	S2	S2	S3	S3	S_{GATE}	S_{GATE}	S_{SUB2}	S_{SUB2}	48.046
		Type2	**S4**	**S4**	**S3**	**S3**	$\boldsymbol{S_{LG}}$	$\boldsymbol{S_{LG}}$	$\boldsymbol{S_{SUB1}}$	$\boldsymbol{S_{SUB1}}$	**18.322**
	11 (10)	**Type1**	**S3**	**S3**	**S4**	**S4**	$\boldsymbol{S_{SUB1}}$	$\boldsymbol{S_{SUB1}}$	$\boldsymbol{S_{LG}}$	$\boldsymbol{S_{LG}}$	**18.322**
		Type2	S3	S3	S2	S2	S_{SUB2}	S_{SUB2}	S_{GATE}	S_{GATE}	48.046
PDN	01 (00)	Type3	S3	S2	S4	S3	S_{SUB2}	S_{GATE}	S_{LG}	S_{SUB1}	27.528
		Type4	**S3**	**S4**	**S4**	**S3**	$\boldsymbol{S_{SUB1}}$	$\boldsymbol{S_{LG}}$	$\boldsymbol{S_{LG}}$	$\boldsymbol{S_{SUB1}}$	**14.381**
		Type5	S3	S2	S2	S3	S_{SUB2}	S_{GATE}	S_{GATE}	S_{SUB2}	40.694
	10 (11)	Type3	S4	S3	S3	S2	S_{LG}	S_{SUB1}	S_{SUB2}	S_{GATE}	27.528
		Type4	S2	S3	S3	S2	S_{GATE}	S_{SUB2}	S_{SUB2}	S_{GATE}	40.694
		Type5	**S4**	**S3**	**S3**	**S4**	$\boldsymbol{S_{LG}}$	$\boldsymbol{S_{SUB1}}$	$\boldsymbol{S_{SUB1}}$	$\boldsymbol{S_{LG}}$	**14.381**

Figure 30 (Figure 31) shows the XOR2 (XNOR2) CMOS gate with two and three different input locations of pull-up and pull-down network, respectively. An important point to note is that if XOR2 and XNOR2 gates are implemented by complex CMOS gate realization, all input vectors of both XOR and XNOR gate never produce the same gate input state due to the presence of negated inputs. For example, if input components of XOR2 (XNOR2) gate are A and B, the logical expression of XOR2 (XNOR2) is $A \cdot \overline{B} + \overline{A} \cdot B$ $(A \cdot B + \overline{A} \cdot \overline{B})$, and thus both

original inputs (A and B) and negated inputs ($\overline{A}$ and $\overline{B}$) are presented in each CMOS network as illustrated in Figure 30 (Figure 31).

Consequently, unlike the other logic gates (such as NAND, NOR, AOI and OAI) which present the same gate input state when input vector consists of same logic value (either high or low), every input vector of XOR (XNOR) complex CMOS gate can be presented the most gate leaky state (S_{GATE}) in off-state network as shown in Table 17.

4.2.2.1 Limitation of Using Pin Reordering in a Complex CMOS Gate

As aforementioned, there is a limitation of using pin reordering technique in complex CMOS gate. To illustrate this, consider the different implementations of OAI-21 gate ($F = \overline{A \text{ and } (B \text{ or } C)}$) and AOI-21 ($F = \overline{A \text{ or } (B \text{ and } C)}$) gate, as shown in Figure 29. In this structure, only OR/AND components (B and C) of OAI-21/AOI-21 can be interchanged with each other, whereas inputs A and B, or A and C cannot be interchanged because this transformation affects the gate logic function. For this reason, only a pull-up (pull-down) network in OAI-21 (AOI-21) is benefited from pin reordering, whereas a pull-down (pull-up) network does

not. Similarly, pin reordering technique only effective in pull-down networks of XOR and XNOR gates. As a result, only one of CMOS networks (either pull-up or pull-down) benefit from pin reordering as shown in Table 18. In order to overcome this limitation of using pin reordering, transistor reordering is inevitable, which will be described on next chapter.

Table 18: Leakage current savings (%) obtained through pin reordering.

Gate type	Off-state Network	Pin reordering	Leakage Savings		
			I_{SUB}	I_G	I_{TOTAL}
OAI-21	PUN	101 → 110	30.88	67.67	30.92
AOI-21	PDN	001 → 010	27.16	79.72	35.99
XOR2 (XNOR2)	PDN	01 (00) : Type 3 → Type 4	37.20	91.43	47.76
		01 (00) : Type 5 → Type 4	54.26	95.52	64.66
		10 (11) : Type 3 → Type 5	37.20	91.43	47.76
		10 (11) : Type 4 → Type 5	54.26	95.52	64.66

4.3 Summary

In this chapter, we first discussed how gate and subthreshold leakage varies with input vector. And then we investigated the opportunities for reducing gate and subthreshold leakage simultaneously by using pin reordering, and pointed

out the problems and limitations in association with existing pin reordering technique when applying this technique to pull-up network of CMOS circuits. To solve these problems, we proposed the complete pin reordering rules for CMOS circuits by including the pull-up network. Experimental results show that pin reordering technique effectively reduced the both subthreshold and gate leakage.

Chapter 5

Leakage Reduction through Transistor Reordering for a Complex CMOS Gate

5.1 Introduction

Table 19: Leakage current savings (%) obtained through transistor reordering.

Gate type	Off-state Network	Transistor reordering	Leakage Savings		
			I_{SUB}	I_G	I_{TOTAL}
OAI-21	PDN	001 : Type 2 → Type 1	54.39	71.31	58.65
		010 : Type 2 → Type 1	54.39	71.31	58.65
		011 : Type 2 → Type 1	51.72	97.22	68.91
		100 : Type 1 → Type 2	56.67	93.33	62.84
AOI-21	PUN	011 : Type 1 → Type 2	64.31	86.01	64.34
		100 : Type 2 → Type 1	59.17	93.29	59.28
		101 : Type 2 → Type 1	61.82	47.05	61.80
		110 : Type 2 → Type 1	61.82	47.05	61.80
XOR2 (XNOR2)	PUN	00 (01) : Type 1 → Type 2	61.81	89.79	61.86
		11 (10) : Type 2 → Type 1	61.81	89.79	61.86

In a complex CMOS logic gate, which off-state network consists of combination of serial and parallel MOS structures, pin reordering is limited by a

gate logic function as discussed in previous chapter. To overcome this, transistor reordering is applied for leakage minimization. Therefore, all networks of complex CMOS logic gates are benefited from using pin and transistor reordering as listed in Table 18 and Table 19, respectively.

In this chapter, we proposed an optimized structure for leakage reduction in complex CMOS logic gate by transistor reordering. To accurate analysis of transistor reordering, we considering all components of gate leakage as well as subthreshold leakage.

The concept of previous pin reordering rule [3] for leakage reduction, placing all off transistors at the bottom of the stack for each gate, works well in simple complex CMOS logic gates such as 3-input OAI-21/AOI-21 gate as we explored previously. However, this approach is not fully optimized for every complex logic gate since it did not take into account the reverse gate leakage, and thus effect of reordering on reverse gate leakage is ignored. This can result in inaccurate analysis of the effect of transistor reordering on leakage reduction. To demonstrate this, consider OAI-4211 gate as shown in Figure 32 (a). This complex gate can transform into the simplified form as shown in Figure 32 (b), when we consider the parallel transistors as one single transistor.

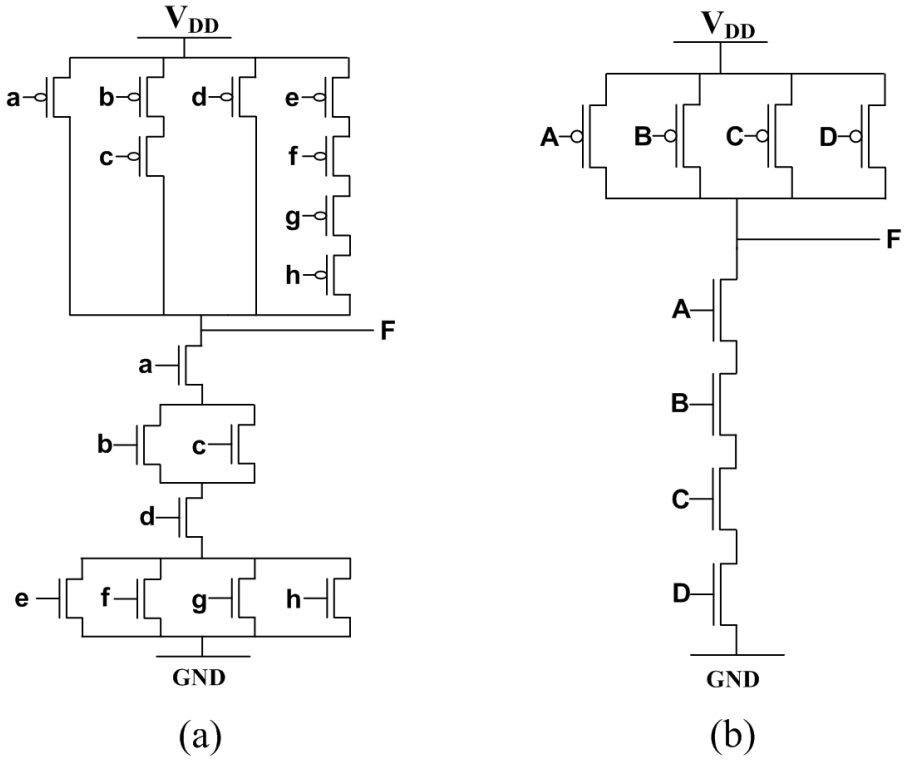

Figure 32: OAI-4211 gate (a) and its simplified formation (b).

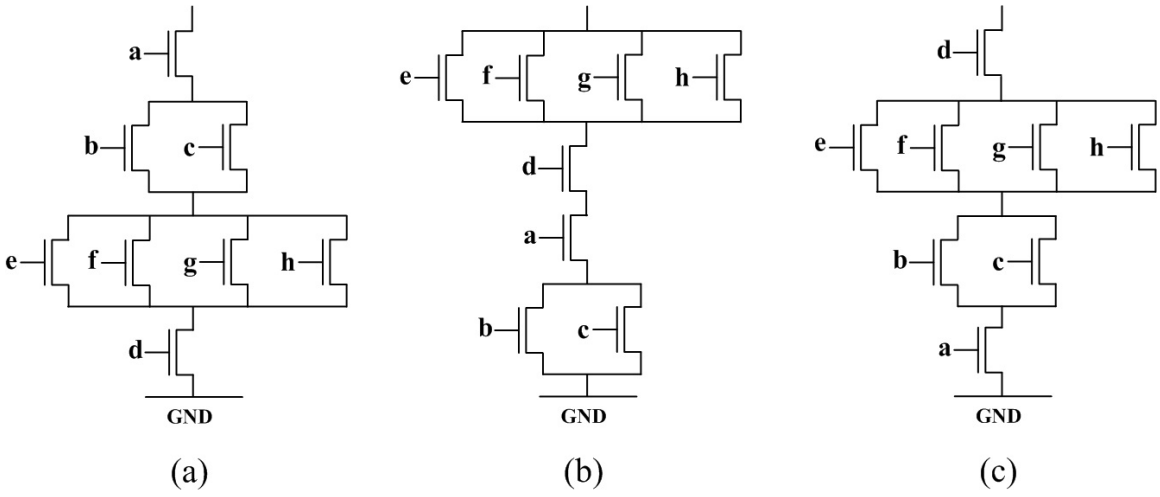

Figure 33: Various formations of pull-down network in OAI-4211 gate; simplified form input: (a) "ABDC" (b) "DCAB" (c) "CDBA".

Table 20: Comparison of leakage current (nA) considering without I_{RG} and with I_{RG} in off-state network of OAI-4211 gate with input: abcdefgh (ABCD) = 00011000 (0011).

Simplified formation in transistor order: Top → bottom (condition)	I_{SUB}	w/o I_{RG}		w I_{RG}	
		I_G	I_{TOTAL}	I_G	I_{TOTAL}
ABDC (off-off-on-on)	2.27	8.22	10.05	9.24	11.51

If the given input vector of this gate is abcdefgh (ABCD) = 00011000 (0011), the worst transistor order of simplified form (top-to-bottom order) is "off-off-on-on" (="0011"); possible input vectors are "ABCD", "ABDC", "BADC" and "BACD".

Among possible worst transistor orders, one ("ABDC") of worst orders is shown in Figure 33 (a), and Table 20 lists the leakage current with and without considering I_{RG}. The best transistor order of simplified form (top-to-bottom order) is "on-on-off-off" ="1100"); possible input vectors are "CDAB", "CDBA", "DCAB" and "DCBA"; two of best orders are shown in Figure 33 (b) "DCAB" and (c) "CDBA".

Figure 34 depicts the transistor reordering to minimize the leakage current. After this transformation is done, the off-state network can be divided into two block bindings: conducting block binding (CBB) and non-conducting block binding (NCBB).

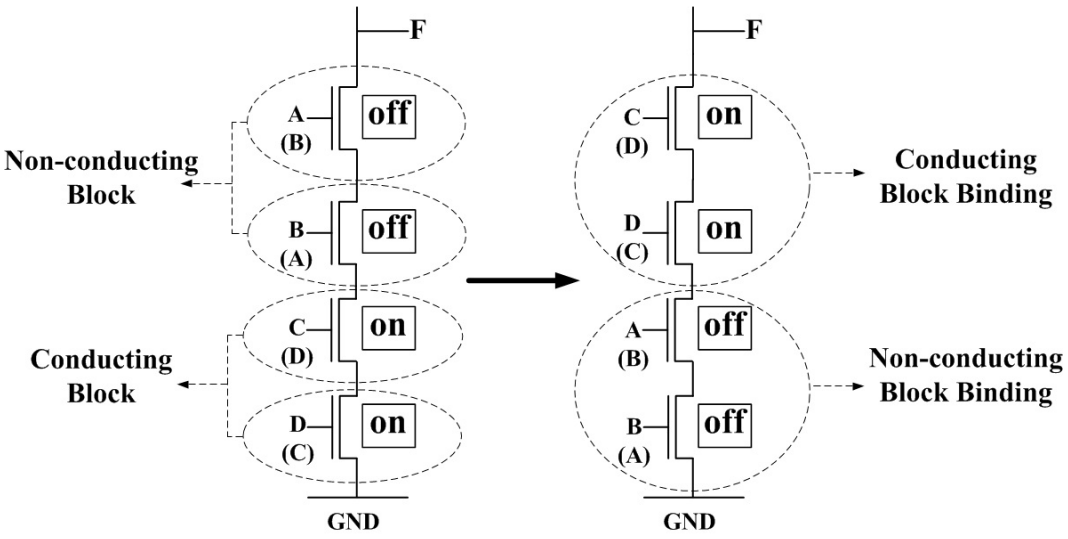

Figure 34: Transistor reordering for leakage reduction in off-state network when the simplified input (ABCD) of OAI-4211 gate is "0011".

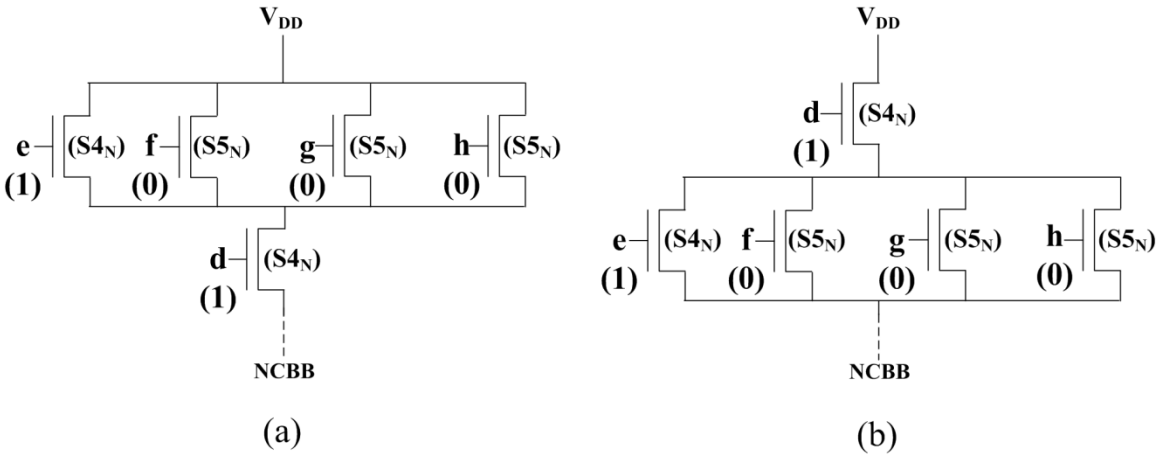

Figure 35: Different conducting block orders in CBB of OAI-4211 gate: (a) "DC" (b) "CD".

In this formation, the steady state(s) of each conducting block of OAI gate consists of either least gate leaky state ($S4_N$), or least gate leaky state along with

reverse gate leaky state ($S5_N$). For example, Figure 35 shows the two possible transistor (conducting block) orders ("CD" and "DC") in CBB of OAI-4211 gate under input: abcdefgh (ABCD) = 00011000 (0011).

If we ignored the reverse gate leakage ($S5_N$) in conducting block, the difference of the leakage current in two transistor orders is negligible. Thus, the impact of transistor reordering on reverse gate leakage is also negligible. However, when we take into account reverse gate leakage, there is a huge discrepancy between two transistor orders ("DCXX" and "CDXX", where XX stands for input vectors (AB, BA)) in leakage current as shown in Table 21.

Table 21: Comparison of leakage current (nA) considering without I_{RG} and with I_{RG} in different transistor orders in off-state network of OAI-4211 gate with input: abcdefgh (ABCD) = 00011000 (0011).

Transistor order in simplified form : Top → bottom (condition)	I_{SUB}	w/o I_{RG}		w I_{RG}	
		I_G	I_{TOTAL}	I_G	I_{TOTAL}
DCAB (on-on-off-off)	2.04	4.68E-3	2.05	4.15	6.19
CDAB (on-on-off-off)	2.04	5.17E-3	2.04	1.73	3.77
DCBA (on-on-off-off)	1.22	4.60E-3	1.22	4.41	5.62
CDBA (on-on-off-off)	1.22	5.10E-3	1.22	1.98	3.20

It can be observed that measuring leakage current is inaccurate without considering the reverse gate tunneling leakage, resulting in misleading the effect of transistor reordering on leakage savings as shown in Table 22.

Table 22: Comparisons of percentage leakage reduction obtained without I_{RG} and with I_{RG} in different transistor orders in off-state network of OAI-4211 gate with input: abcdefgh (ABCD) = 00011000 (0011).

Transistor Reordering [0011] → [1100]	Leakage Savings (%)					
	w/o I_{RG}			w I_{RG}		
	I_{SUB}	I_G	I_{TOTAL}	I_{SUB}	I_G	I_{TOTAL}
[ABDC] → [DCAB]	10.00	99.94	80.47	10.00	55.19	46.27
[ABDC] → [CDAB]	10.47	99.94	80.57	10.47	81.27	67.29
[ABDC] → [DCBA]	46.42	99.94	88.36	46.42	52.32	51.16
[ABDC] → [CDBA]	46.61	99.94	88.39	46.61	78.51	72.22

Experimental results indicate that the leakage current between two configurations ("DCXX" and "CDXX") is almost identical when the reverse gate leakage current is ignored. The inaccurate analysis of reordering effects causes to an overestimated its ability; existing reordering approach do not recognize the differences between "DCXX" and "CDXX". Furthermore, I_{SUB} also varies with transistor order; XXBA transistor order is less leaky than XXAB transistor order, where XX stands for input vectors (DC, CD).

Hence, just placing all off transistors at the bottom of the stack for each gate is not fully optimized strategy for every complex logic gate. Consequently, the impact of transistor reordering on reverse gate leakage and subthreshold leakage should be considered to achieve minimal leaky structure.

To overcome these problems, we proposed a novel transistor reordering method for leakage reduction. Unlike previous technique, proposed method provides exact reordering rules for minimum leaky formation by analyzing all leakage components such as reverse gate and subthreshold leakage.

As described in previous chapter, reordering rules for leakage reduction in pull-up network and pull-down network are different. Let us therefore consider these two networks separately.

5.2 Transistor Reordering in Pull-Down Network

In this subchapter, we assumed that the first step of transistor reordering has been conducted in pull-down network; that is, all conducting blocks are located above the all non-conducting blocks.

5.2.1 Transistor Reordering in Conducting Block Binding

To analyze the effect of transistor (conducting block) reordering on leakage current in CBB of pull-down network, we consider the different transistor orders ("CD" and "DC") in CBB of OAI-4211 gate with input: abcdefgh (ABCD) = 00011000 (0011), as shown in Figure 36. In CBB of off-state network, each conducting block contains at least one on-transistor; for instance, in case of OAI gate, each conducting block consists of either on-transistor (least gate leaky state ($S4_N$)), or on-transistor along with off-transistor (reverse gate leaky state ($S5_N$)).

Table 23 lists the leakage current of CBB in OAI-4211 gate. It can be observed that on-transistor ($S4_N$) and off-transistor ($S5_N$) exhibit different leakage behaviors based on the location in CBB

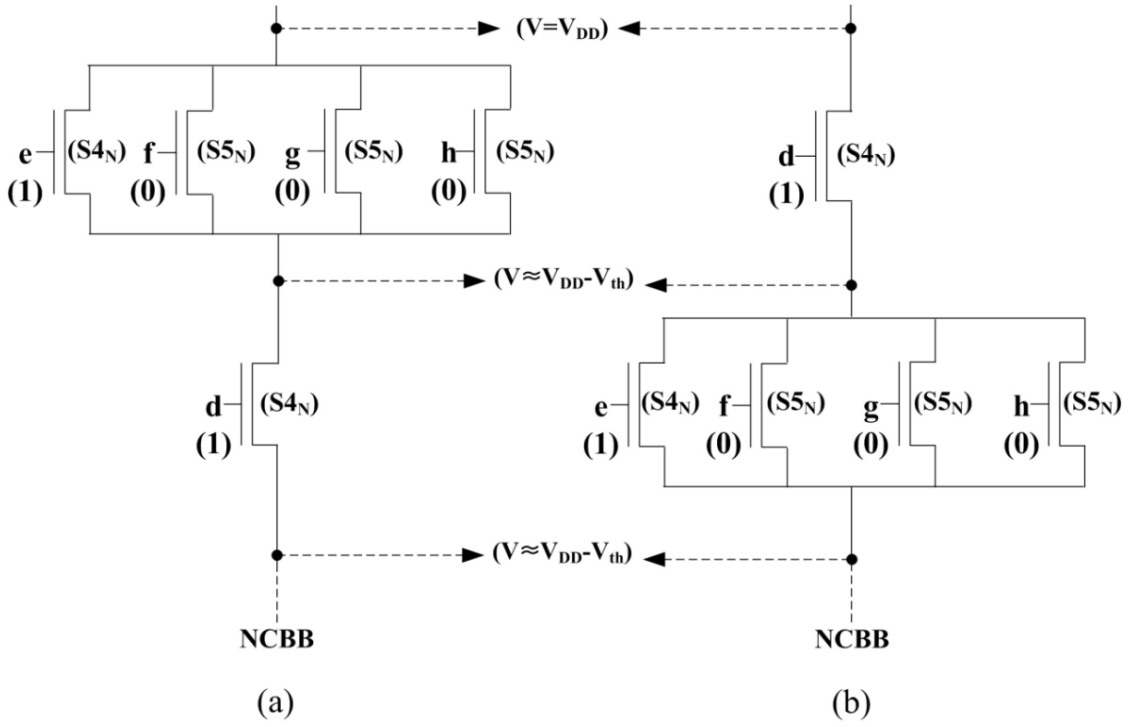

Figure 36: Different conducting-block orders in CBB of OAI-4211 gate: (a) "DC" (b) "CD".

Table 23: Leakage current (nA) in different conducting-block orders of CBB in OAI-4211 gate.

Transistor order (Top→bottom)	Conducting Block				
	C	D			C + D
	$S4_N$ (on)	$S4_N$ (on)	$S5_N$ (off)		$S4_N$+($S4_N$+3*$S5_N$)
	I_G	I_G	I_G	I_{SUB}	I_{TOTAL}
DC	3.095E-3	1.352E-3	1.300	3.510E-14	3.905
CD	1.490E-3	3.479E-3	0.504	3.046E-14	1.518

Table 24: Leakage current (nA) and the bias voltages between the nodes in on- and off-transistors under different locations of conducting block.

Conducting block	Steady state (status)	Conducting block location	$\|V_{GD}\|$	$\|V_{GS}\|$	$\|V_{GB}\|$	I_G
C	$S4_N$ (on)	**top**	**0**	**0.255**	**1.1**	**1.490E-3**
		bottom	0.218	0.238	1.1	3.095E-3
D	$S4_N$ (on)	**top**	**0**	**0.218**	**1.1**	**1.352E-3**
		bottom	0.225	0.249	1.1	3.479E-3
	$S5_N$ (off)	top	1.1	0.882	0	1.300
		bottom	**0.875**	**0.851**	**0**	**0.504**

As seen in Table 24, I_G in top-located on-transistor is less leaky than that in bottom-located on-transistor, whereas, I_G in off-transistor shows the opposite behavior; that is, I_G in top-located off-transistor is leakier than that in bottom-located off-transistor. In Table 24, the lowest leakage for each transistor is in bold. This is due to the fact that the drain voltage (V_D) of conducting block depends on the location in CBB. When the conducting block locates on the top of CBB, the drain voltage of conducting block contains full logic value (V_{DD}). Whereas, when the conducting block locates on the bottom of CBB, the drain voltage of conducting block contains approximately V_{th} less than full logic value as shown in Figure 36. For this reason, leakage in on-transistor reduces when conducting block moves from bottom to top in CBB, whereas leakage in off-transistor

reduces opposite way of transition (conducting block moves from top to bottom) in CBB. Note that the subthreshold leakage (I_{SUB}) of off-transistor ($S5_N$) in conducting block is negligible since the off-transistor ($S5_N$) of I_{SUB} is at least eleven orders of magnitude smaller than that of I_G as shown in Table 23. Thus, the effect of transistor reordering on I_{SUB} is also negligible in CBB. In other words, dominant leakage current of conducting block is the I_G. In addition, if conducting block contains the off-transistor, reverse gate tunneling current (I_{RG}), which exhibits only in off-transistor, is the dominant leakage among I_G components since this leakage is at least two orders of magnitude higher than forward gate tunneling current (which exists only in on-transistor) in CBB as listed in Table 24. Based on the above observations, we developed an algorithm for conducting block in CBB of pull-down network. The following is the transistor reordering procedure for leakage reduction in CBB of pull-down network.

1) Each conducting block calculates the delta leaky_CBB_PDN:

   Delta leaky_CBB_PDN= (off_gain_ttb) – (on_gain_btt):

   ⇨ Off_gain_ttb (calculate the off-transistors' leakage gain (reduction) when the block is moved from top to bottom in CBB): sum of all off-transistors' leakage current (I_G and I_{SUB}) when the conducting block is

located at the top of CBB – sum of all off-transistors' leakage current (I_G and I_{SUB}) when the conducting block is located at the bottom of CBB.

- ⇨ On_gain_btt (calculate the on-transistors' leakage gain (reduction) when the block is moved from bottom to top in CBB): sum of all on-transistors' leakage current (I_G) when the conducting block is located at the bottom of CBB – sum of all on-transistors' leakage current (I_G) when the conducting block is located at the top of CBB.

2) Conducting blocks are sorted by delta leaky_CBB_PDN in ascending order from top to bottom in CBB; the largest value of delta leaky_CBB_PDN is located at the bottom of CBB.

For example, Table 25 shows the delta leaky_CBB_PDN of each conducting block in CBB of OAI-4211 gate. Thus, the best transistor order of this CBB is "CD".

Table 25: Delta leaky of conducting blocks in CBB of OAI-4211 gate.

Conducting block	Off_gain_ttb	On_gain_btt	Δ leaky_CBB
C	0	1.605E-12	-1.605E-12
D	7.961E-10	2.127E-12	7.940E-10

5.2.2 Transistor Reordering in Non-Conducting Block Binding

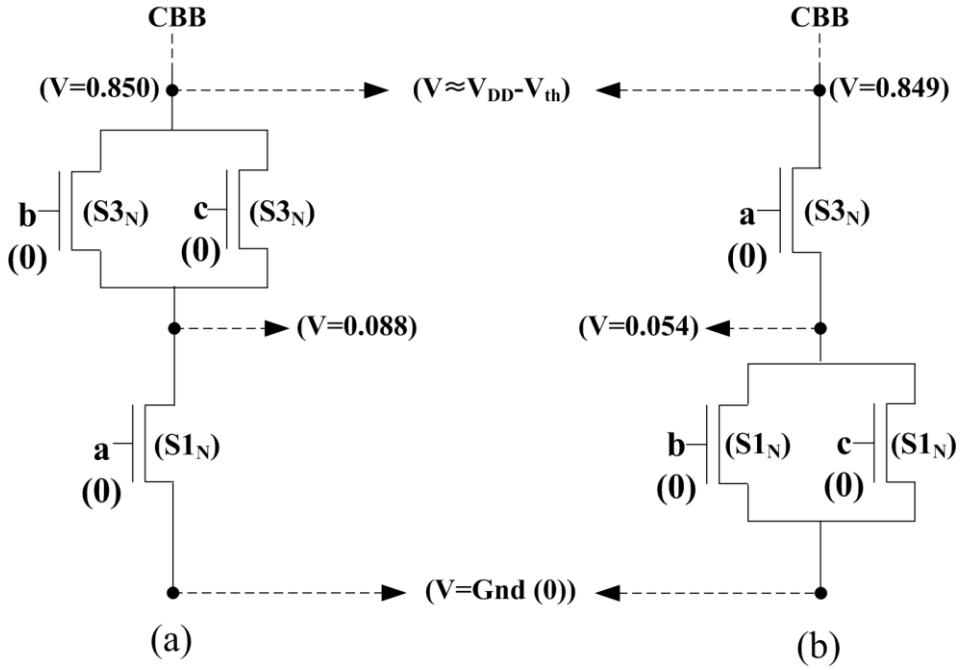

Figure 37: Different non-conducting block orders in NCBB of OAI-4211 gate: (a) "BA" (b) "AB".

Table 26: Leakage current (nA) in different non-conducting-block orders of NCBB in OAI-4211 gate.

Transistor order (Top→bottom)	Non-Conducting Block				
	A		B		A + B
	a		b + c		a + b + c
	I_G	I_{SUB}	I_G	I_{SUB}	I_{TOTAL}
BA	1.332E-4	0.606	0.468	0.606	1.681
AB	0.231	1.018	9.039E-5	1.018	2.267

Table 27: Gate leakage current (nA) and the bias voltages (V) between the nodes under different locations of non-conducting block (NCB).

NCB	NCB location	$\|V_{GD}\|$	$\|V_{GS}\|$	$\|V_{GB}\|$	$\sum$ W/L	I_G
A	top	0.849	0.054	0	4	0.231
	bottom	0.088	0	0		1.332E-4
B	top	0.850	0.088	0	8	0.468
	bottom	0.054	0	0		9.039E-5

To analyze the effect of transistor (non-conducting block) reordering on leakage current in NCBB of pull-down network, we consider the different transistor orders ("BA" and "AB") in NCBB of OAI-4211 gate with input: abcdefgh (ABCD) = 00011000 (0011), as shown in Figure 37. In NCBB of OAI off-state network, all non-conducting block contains the off-transistors. Table 26 lists the leakage current of NCBB in OAI-4211 gate.

In case of I_G in NCBB, for the same reason as off-transistors in CBB, NCB exhibit better leakage behavior when it located on bottom of NCBB due to the $V_{GD/GS}$ of the block as listed in Table 27. Note that, among gate leakage components, only reverse gate leakage is existed in the NCBB.

In case of I_{SUB} in NCBB, I_{SUB} in NCBB depends on the top block of NCBB as shown in Table 26; the same amount of subthreshold leakage current exhibits in the rest of blocks (other than top block), which discussed in the previous chapter.

Thus, total I_{SUB} in NCBB can be calculated by adding I_{SUB} of every transistor in top block of NCBB and multiplying it by the number of blocks in NCBB.

Table 28: Subthreshold leakage current (nA), V_{th} (V) and V_{DS} (V) in different widths of non-conducting block (NCB).

NCB	NCB location	V_{DS}	V_{th}	$\sum$ W/L	I_{SUB}
A	top	0.795	0.346	4	1.018
B	top	0.762	0.356	8	0.606

It should be noted that I_{SUB} in top block of NCBB varies with its width (sum of all off-transistors' W/L in block) as illustrated in Table 28; larger block width ($\sum$W/L) exhibits more stacking effect than smaller one since larger block width yields more positive potential in its source node than smaller one as illustrated in Figure 37. As can be seen from Table 27 and Table 28, I_G and I_{SUB} show different leakage behaviors in terms of block width; the I_G is proportional to the block width, whereas the I_{SUB} is inversely proportional to the block width.

Based on the above observations, we developed an algorithm for non-conducting block in NCBB of pull-down network. The following is the transistor reordering procedure for leakage reduction in NCBB of pull-down network.

1) Each non-conducting block calculates the delta leaky_NCBB_PDN:

Delta leaky_NCBB_PDN= (total_gate_top) + (total_sub_top) :

- ⇨ Total_gate_top (calculate the total gate leakage current in each block when the block is located at the top of NCBB): sum of all off-transistors' gate leakage current in the block when the block is located at the top of NCBB.
- ⇨ Total_sub_top (calculate the total subthreshold leakage current of NCBB based on the subthreshold leakage current in top block): sum of all off-transistors' subthreshold leakage current in the block when the block is located at the top of the NCBB * the number of the blocks in NCBB.

2) Non-conducting blocks are sorted by delta leaky_NCBB_PDN in ascending order from top to bottom in NCBB; largest value of the delta leaky_NCBB_PDN is located at the bottom of NCBB.

For example, Table 29 shows the delta leaky_NCBB_PDN of each block in NCBB of OAI-4211 gate. Thus, the best transistor order of this NCBB is "BA".

Table 29: Delta leaky of non-conducting blocks in NCBB of OAI-4211 gate.

Non-conducting block	Total_gate_top	Total_sub_top	Δ leaky_NCBB
A	2.309E-10	2.035E-9	2.266E-9
B	4.682E-10	1.212E-9	1.680E-9

5.3 Transistor Reordering in Pull-Up Network

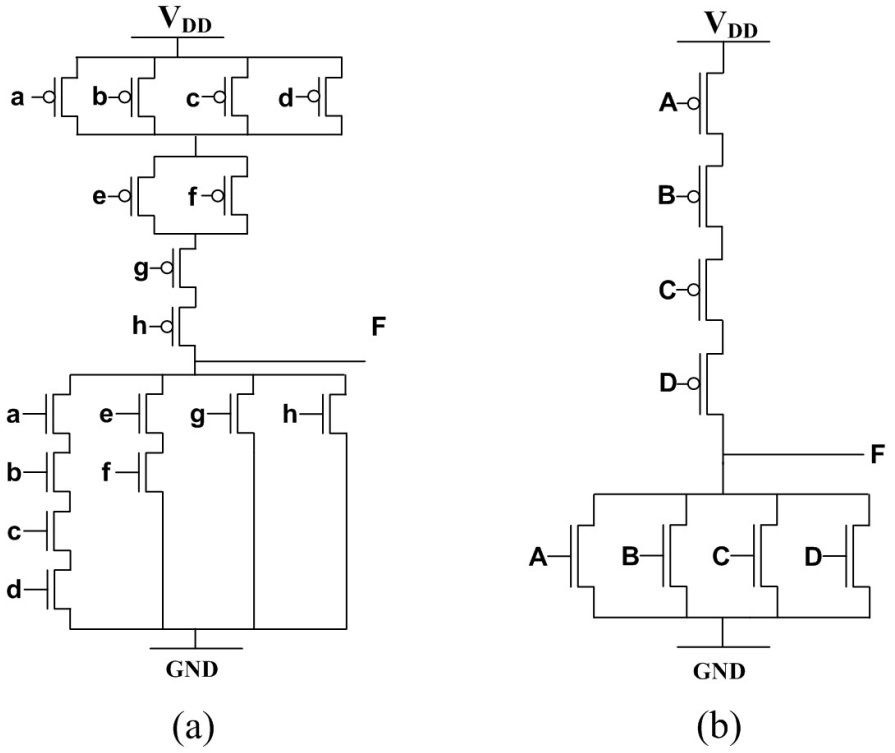

Figure 38: AOI-4211 gate (a) and its simplified formation (b).

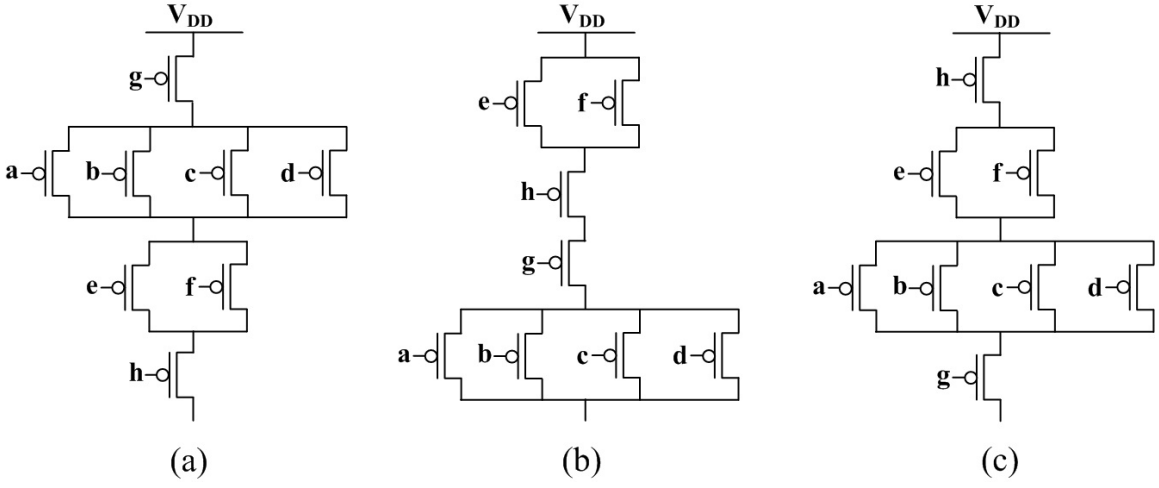

Figure 39: Various formations of pull-up network in AOI-4211 gate; simplified form input: (a) "CABD" (b) "BDCA" (c) "DBAC".

Table 30: Comparison of leakage current (nA) considering without I_{RG} and with I_{RG} in off-state network of AOI-4211 gate with input: abcdefgh (ABCD) = 01111101 (0101); abcd(A)=0111(0), ef(B)=11(1), g(C)=0(0), h(D)=1(1).

Simplified formation in transistor order: Top → bottom (condition)	I_{SUB}	w/o I_{RG}		w I_{RG}	
		I_G	I_{TOTAL}	I_G	I_{TOTAL}
CABD (on-on-off-off)	1.65	6.07E-2	1.71	7.54E-2	1.72

Now, let us consider the pull-up network in complex gate. To analyze the effect of transistor reordering on leakage sources of pull-up network, we use an AOI-4211 gate as shown in Figure 38 (a). This complex gate can transform into the simplified form as shown in Figure 38 (b). If the given input vector of this gate is abcdefgh (ABCD) = 01111101 (0101), the worst transistor order of simplified form (top-to-bottom order) is "on-on-off-off" (="0011"); possible input vectors are "ACBD", "ACDB", "CABD" and "CADB". Among possible worst transistor orders, one ("CABD") of worst orders is shown in Figure 39 (a). Table 30 tabulates the corresponding leakage sources of "CABD" with and without considering I_{RG}. The best transistor order of simplified form (top-to-bottom order) is "off-off-on-on" ="1100"); possible input vectors are "BDAC", "BDCA", "DBAC" and "DBCA"; two of best orders are shown in Figure 39 (b) "BDCA" and (c) "DBAC".

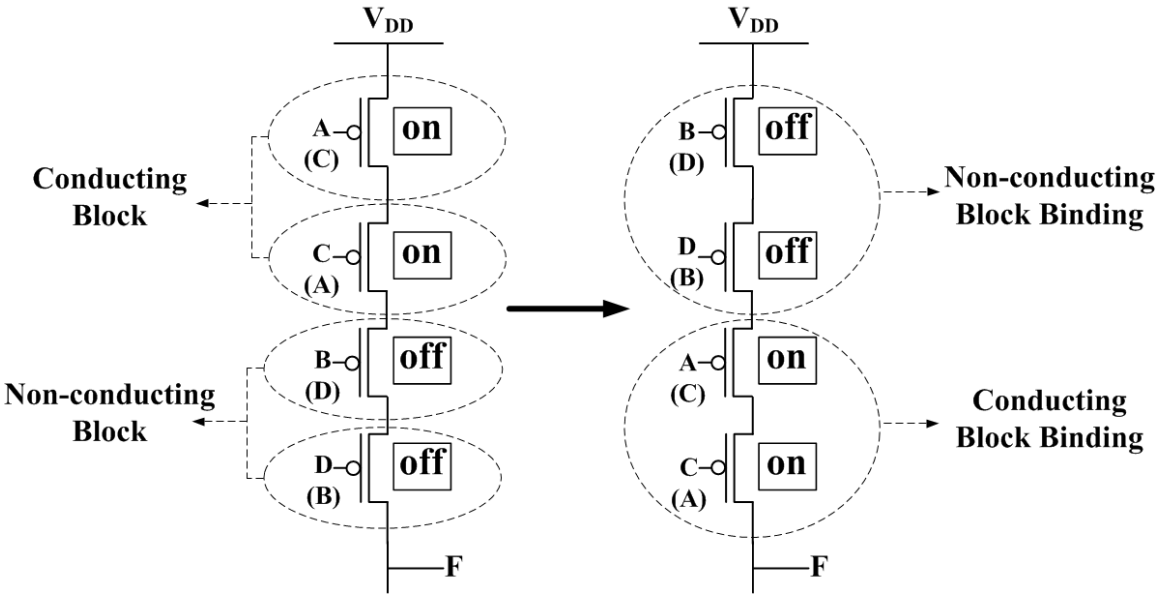

Figure 40: Transistor reordering for leakage reduction in off-state network when the simplified input (ABCD) of AOI-4211 gate is "0101".

Figure 40 depicts the transistor reordering to minimize the leakage current. After this transformation is done, the off-state network can be divided into two block bindings (CBB and NCBB).

As discussed in previous chapter, the gate leakage for the PMOS transistor is two orders of magnitude lower than for the NMOS transistor in 65nm PTM, and thus the contribution of the gate leakage to total leakage in pull-up network (4.07% in Table 30) is much smaller than that of pull-down network (80.28% in Table 20).

For this reason, as can be seen in Table 31 and Table 32, the impact of transistor reordering on CBB (XXAC and XXCA , where XX stands for input

vectors (BD, DB)) is much smaller than NCBB (BDXX and DBXX, where XX stands for input vectors (AC, CA)) because the dominant leakage current in CBB is the gate leakage.

Table 31: Comparison of leakage current (nA) considering without I_{RG} and with I_{RG} in different transistor orders in off-state network of AOI-4211 gate with input: abcdefgh (ABCD) = 01111101 (0101).

Transistor order in simplified form : Top → bottom (condition)	I_{SUB}	w/o I_{RG}		w I_{RG}	
		I_G	I_{TOTAL}	I_G	I_{TOTAL}
BDCA (off-off-on-on)	1.48	1.21E-4	1.48	6.88E-2	1.55
BDAC (off-off-on-on)	1.48	1.22E-4	1.48	4.08E-2	1.52
DBCA (off-off-on-on)	0.88	1.05E-4	0.88	7.62E-2	0.95
DBAC (off-off-on-on)	0.88	1.06E-4	0.88	4.91E-2	0.93

Table 32: Comparisons of percentage leakage reduction obtained without I_{RG} and with I_{RG} in different transistor orders in off-state network of AOI-4211 gate with input: abcdefgh (ABCD) = 01111101 (0101).

Transistor Reordering [0011] → [1100]	Leakage Savings (%)					
	w/o I_{RG}			w I_{RG}		
	I_{SUB}	I_G	I_{TOTAL}	I_{SUB}	I_G	I_{TOTAL}
[CABD] → [BDCA]	10.13	99.80	13.32	10.13	8.84	10.08
[CABD] → [BDAC]	10.18	99.80	13.37	10.18	45.98	11.75
[CABD] → [DBCA]	46.71	99.83	48.60	46.71	-0.94	44.62
[CABD] → [DBAC]	46.74	99.83	48.63	46.74	34.87	46.62

In the following subchapters, we assumed that the first step of transistor reordering has been conducted in pull-up network; that is, all non-conducting blocks are located above the all conducting blocks.

5.3.1 Transistor Reordering in Non-Conducting Block Binding

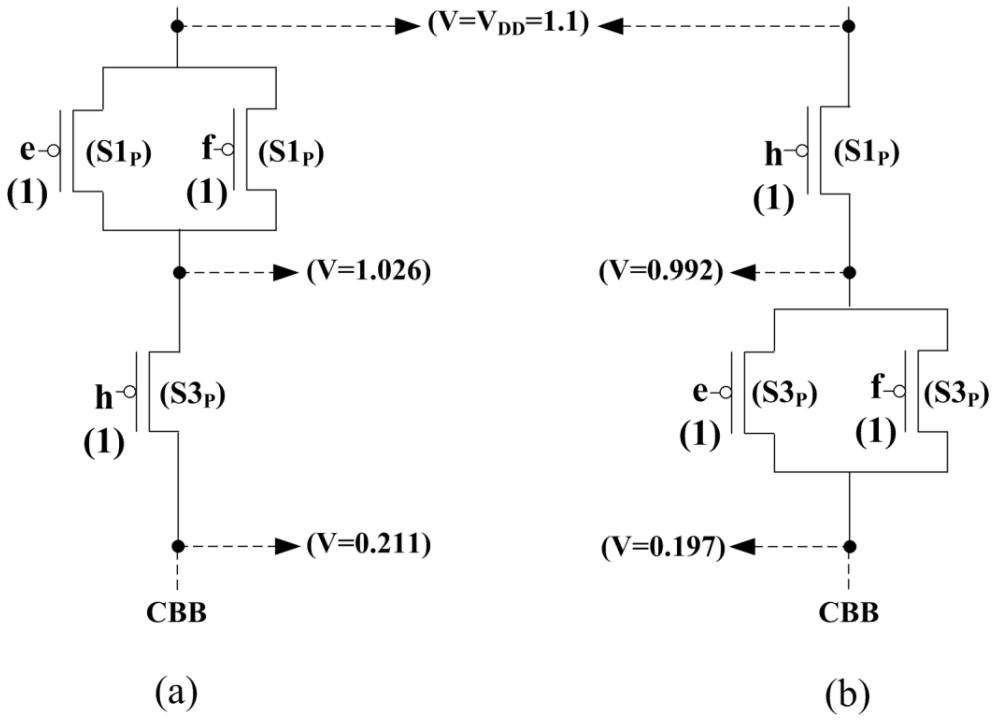

Figure 41: Different non-conducting block orders in NCBB of AOI-4211 gate: (a) "BD" (b) "DB".

Table 33: Leakage current (nA) in different non-conducting-block orders of NCBB in AOI-4211 gate.

Transistor Order (Top→bottom)	Non-Conducting Block				
	B		D		B + D
	e + f		h		e + f + h
	I_G	I_{SUB}	I_G	I_{SUB}	I_{TOTAL}
BD	8.095E-6	0.730	5.449E-3	0.749	1.485
DB	1.160E-2	0.438	9.551E-6	0.438	0.888

To analyze the effect of transistor (non-conducting block) reordering on leakage current in NCBB of pull-up network, we consider the different transistor orders ("BD" and "DB") in NCBB of AOI-4211 gate with input: abcdefgh (ABCD) = 01111101 (0101), as shown in Figure 41. In NCBB of AOI off-state network, all non-conducting block contains the off-transistors. Table 33 lists the leakage current of NCBB in AOI-4211 gate.

Table 34: Gate leakage current (nA) and the bias voltages (V) between the nodes under different locations of non-conducting block (NCB).

NCB	NCB location	$\|V_{GD}\|$	$\|V_{GS}\|$	$\|V_{GB}\|$	$\sum$ W/L	I_G
B	top	0.074	0	0	8	8.095E-6
	bottom	0.903	0.108	0		1.160E-2
D	top	0.108	0	0	4	9.551E-6
	bottom	0.889	0.074	0		5.449E-3

In case of I_G in NCBB, off-transistor exhibit better leakage behavior when it located on top of NCBB due to the $V_{GD/GS}$ of the NCB as listed in Table 34. Note that, among gate leakage components, only reverse gate leakage is existed in the NCBB.

In case of I_{SUB} in NCBB, I_{SUB} in NCBB depends on the bottom block of NCBB as shown in Table 33; almost the same amount of subthreshold leakage current exhibits in the rest of blocks (other than bottom block). Thus, total I_{SUB} in NCBB can be calculated by adding I_{SUB} of every transistor in bottom block of NCBB and multiplying it by the number of blocks in NCBB.

Table 35: Subthreshold leakage current (nA), V_{th} (V) and V_{DS} (V) in different widths of non-conducting block (NCB).

NCB	NCB location	V_{DS}	V_{th}	$\sum$ W/L	I_{SUB}
B	bottom	0.795	0.275	8	0.438
D	bottom	0.815	0.266	4	0.749

It should be noted that I_{SUB} in bottom block of NCBB varies with its width (sum of all off-transistors' W/L in block) as illustrated in Table 35; larger block width ($\sum$W/L) exhibits more stacking effect than smaller one. As can be seen from Table 34 and Table 35, I_G and I_{SUB} show different leakage behaviors in terms

of block width; the I_G is proportional to the block width, whereas the I_{SUB} is inversely proportional to the block width.

Based on the above observations, we developed an algorithm for non-conducting block in NCBB of pull-up network. The following is the transistor reordering procedure for leakage reduction in NCBB of pull-up network.

1) Each non-conducting block calculates the delta leaky_NCBB_PUN:

   Delta leaky_NCBB_PUN= (total_gate_bottom) + (total_sub_bottom):

   ⇨ Total_gate_bottom (calculate the total gate leakage current in each block when the block is located at the bottom of NCBB): sum of all off-transistors' gate leakage current in the block when the block is located at the bottom of NCBB.

   ⇨ Total_sub_bottom (calculate the total subthreshold leakage current of NCBB based on the subthreshold leakage current in bottom block): sum of all off-transistors' subthreshold leakage current in the block when the block is located at the bottom of the NCBB * the number of the blocks in NCBB.

2) Non-conducting blocks are sorted by delta leaky_NCBB_PUN in descending order from top to bottom in NCBB; largest value of the delta leaky_NCBB_PUN is located at the top of NCBB.

For example, Table 36 shows the delta leaky_NCBB_PUN of each block in NCBB of AOI-4211 gate. Thus, the best transistor order of this NCBB is "DB".

Table 36: Delta leaky of non-conducting blocks in NCBB of AOI-4211 gate.

Non-conducting block	Total_gate_bottom	Total_sub_bottom	Δ leaky_NCBB
B	11.603E-12	4.386E-10	4.502E-10
D	5.429E-12	7.487E-10	7.541E-10

5.3.2 Transistor Reordering in Conducting Block Binding

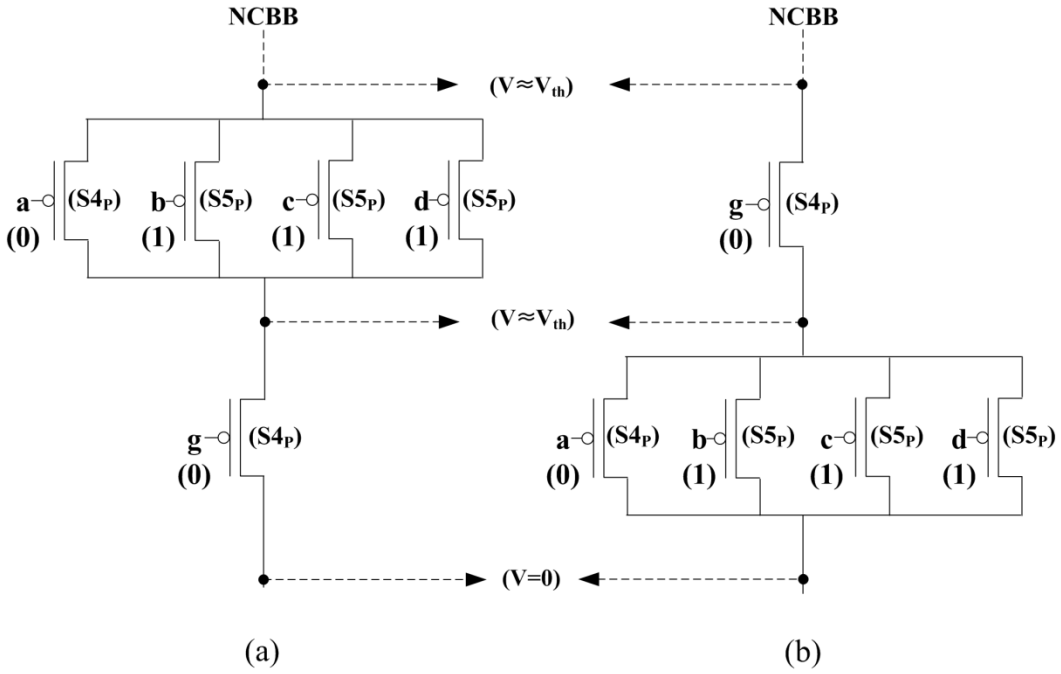

Figure 42: Different conducting-block orders in CBB of AOI-4211 gate: (a) "AC" (b) "CA".

Table 37: Leakage current (nA) in different conducting-block orders of CBB in AOI-4211 gate.

Transistor Order (Top→bottom)	Conducting Block				
	A			C	A + C
	$S4_P$ (on)	$S5_P$ (off)		$S4_P$ (on)	$(S4_P+3*S5_P)+S4_P$
	I_G	I_G	I_{SUB}	I_G	I_{TOTAL}
AC	6.884E-5	1.248E-2	3.719E-15	2.764E-5	3.753E-2
CA	2.722E-5	2.146E-2	3.486E-15	6.780E-5	6.448E-2

Table 38: Leakage current (nA) and the bias voltages between the nodes in on- and off-transistors under different locations of conducting block.

Conducting block	Steady state (status)	Conducting block location	$\|V_{GD}\|$	$\|V_{GS}\|$	$\|V_{GB}\|$	I_G
A	$S4_P$ (on)	top	0.169	0.198	1.1	6.884E-5
		bottom	**0**	**0.168**	**1.1**	**2.722E-5**
	$S5_P$ (off)	**top**	**0.931**	**0.902**	**0**	**1.248E-2**
		bottom	1.1	0.932	0	2.146E-2
C	$S4_P$ (on)	top	0.168	0.197	0	6.780E-5
		bottom	**0**	**0.169**	**0**	**2.764E-5**

To analyze the effect of transistor (conducting block) reordering on leakage current in CBB of pull-up network, we consider the different transistor orders ("CD" and "DC") in CBB of AOI-4211 gate with input: abcdefgh (ABCD) = 01111101 (0101), as shown in Figure 42. In CBB of off-state network, each conducting block contains at least one on-transistor; for instance, in case of AOI gate, each conducting block consists of either on-transistor (least gate leaky state ($S4_P$)), or on-transistor along with off-transistor (reverse gate leaky state ($S5_P$)). Table 37 lists the leakage current of CBB in AOI-4211 gate. It can be observed that on-transistor ($S4_P$) and off-transistor ($S5_P$) exhibit different leakage behaviors based on the location in CBB; as seen in Table 38, I_G in bottom-located on-transistor is less leaky than that in top-located on-transistor, whereas, I_G in off-

transistor shows the opposite behavior; that is, I_G in bottom-located off-transistor is leakier than that in top-located off-transistor. In Table 38, the lowest leakage for each transistor (steady state) is in bold. This is due to the fact that the drain voltage (V_D) of conducting block depends on the location in CBB. When the conducting block locates on the bottom of CBB, the drain voltage of conducting block contains full logic value (0). Whereas, when the conducting block locates on the top of CBB, the drain voltage of conducting block contains approximately V_{th} more than full logic value as shown in Figure 42.

For this reason, leakage in on-transistor reduces when conducting block moves from top to bottom in CBB, whereas leakage in off-transistor reduces opposite way of transition (conducting block moves from bottom to top) in CBB. Note that the subthreshold leakage (I_{SUB}) of off-transistor ($S5_P$) in conducting block is negligible since the off-transistor ($S5_P$) of I_{SUB} is at least ten orders of magnitude smaller than that of I_G as shown in Table 37. Thus, the effect of transistor reordering on I_{SUB} is also negligible in CBB. In other words, dominant leakage current of conducting block is the I_G. In addition, if conducting block contains the off-transistor, reverse gate tunneling current (I_{RG}), which exhibits only in off-transistor, is the dominant leakage among I_G components since this

leakage is at least three orders of magnitude higher than forward gate tunneling current (which exists only in on-transistor) in CBB as listed in Table 38. Based on the above observations, we developed an algorithm for conducting block in CBB of pull-up network. The following is the transistor reordering procedure for leakage reduction in CBB of pull-up network.

1) Each conducting block calculates the delta leaky_CBB_PUN:

   Delta leaky_CBB_PUN= (off_gain_btt) – (on_gain_ttb):

   ⇨ Off_gain_btt (calculate the off-transistors' leakage gain (reduction) when the block is moved from bottom to top in CBB): sum of all off-transistors' leakage current (I_G and I_{SUB}) when the conducting block is located at the bottom of CBB – sum of all off-transistors' leakage current (I_G and I_{SUB}) when the conducting block is located at the top of CBB.

   ⇨ On_gain_ttb (calculate the on-transistors' leakage gain (reduction) when the block is moved from top to bottom in CBB): sum of all on-transistors' leakage current (I_G) when the conducting block is located at the top of CBB – sum of all on-transistors' leakage current (I_G) when the conducting block is located at the bottom of CBB.

2) Conducting blocks are sorted by delta leaky_CBB_PUN in descending order from top to bottom in CBB; the largest value of delta leaky_CBB_PUN is located at the top of CBB.

For example, Table 39 shows the delta leaky_CBB_PUN of each conducting block in CBB of AOI-4211 gate. Thus, the best transistor order of this CBB is "AC".

Table 39: Delta leaky of conducting blocks in CBB of AOI-4211 gate.

Conducting block	Off_gain_btt	On_gain_ttb	Δ leaky_CBB
A	8.980E-12	4.162E-14	8.938E-12
C	0	4.016E-5	-4.016E-5

5.4 Procedure of Transistor Reordering for Leakage Reduction in Complex CMOS gates

With the understanding of the leakage behaviors of circuit structure, we propose a transistor reordering method for leakage reduction in complex CMOS gates. Following is the overall procedure for transistor reordering.

- For off-state pull-down network:
  (1) Blocks in off-state network divided into two categories: conducting and non-conducting blocks.
  (2) Place the all conducting blocks on above the non-conducting blocks.
  (3) Conducting blocks are sorted by delta leaky_CBB_PDN in ascending order from top to bottom in CBB.
  (4) Non-conducting blocks are sorted by delta leaky_NCBB_PDN in ascending order from top to bottom in NCBB.

- For off-state pull-up network:
  (1) Blocks in off-state network divided into two categories: conducting and non-conducting blocks.
  (2) Place the all non-conducting blocks on above the conducting blocks

(3) Non-conducting blocks are sorted by delta leaky_NCBB_PUN in descending order from top to bottom in NCBB.

(4) Conducting blocks are sorted by delta leaky_CBB_PUN in descending order from top to bottom in CBB.

5.5 Summary

In this chapter, we addressed the problems and limitations related to existing pin reordering approach when the concept of pin reordering for leakage reduction is extended to complex CMOS logic gates. To solve these problems, a novel transistor reordering technique for leakage reduction was proposed. The proposed method provides an optimized formation for leakage reduction, and can be used in combined with other leakage reduction techniques to achieve further improvement. For example, this method improves the leakage reduction attained from IVC as described in previous chapter. In addition, the proposed method can be easily integrated into existing CAD tools. Defining a lowest leaky state in each input combination of a logic gate is necessary in order to achieve minimum power dissipation in standby mode operation.

Chapter 6
Effective Body Bias for Standby Leakage Power Reduction in Nanometer-Scale CMOS Circuits

6.1 Introduction

Reverse Body Biasing (RBB) technique [8]-[12] has become one of the most widely used circuit design technique for leakage power reduction. It utilizes the body effect of CMOS gates by manipulating the threshold voltage in standby mode; leakage power reduced by raising the voltage of the PMOS substrate (N-well) with respect to the supply voltage, and by lowering the voltage of the NMOS substrate (P-well) respect to ground. This results in an increase the threshold voltage, thereby suppressing the subthreshold leakage. In active mode of RBB technique, threshold voltage decreased by removing the reverse body bias, thereby back to the normal performance of transistors as shown in Figure 43.

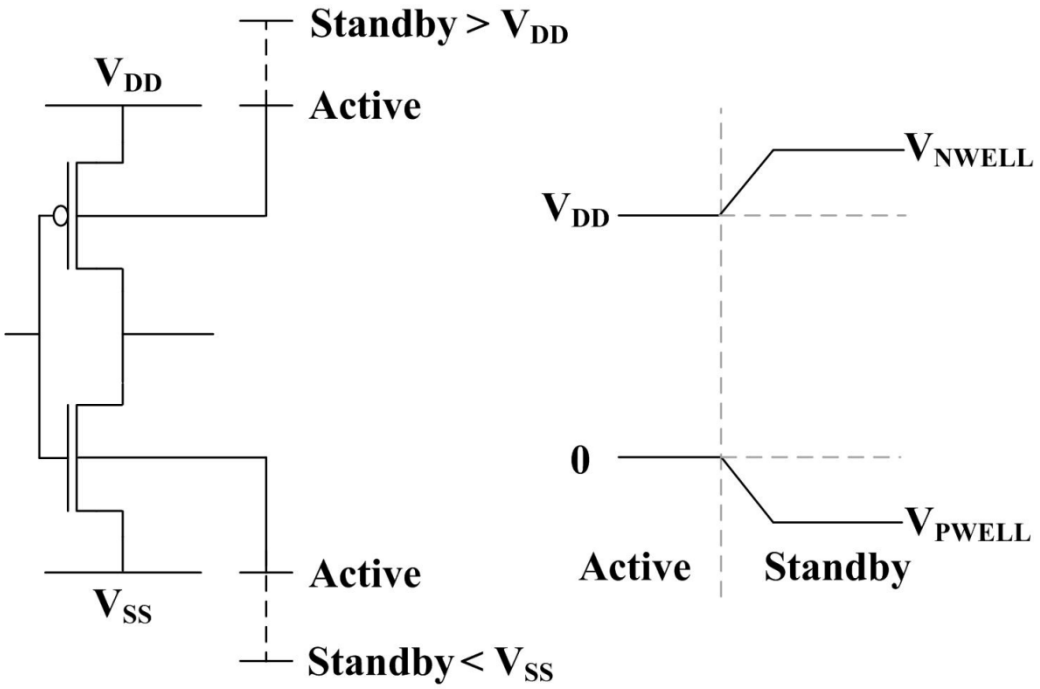

Figure 43: Reverse Body Biasing.

In addition, forward body biasing (FBB) technique [13]-[15] has been used in active mode to increase the circuit performance by decreasing the threshold voltages of CMOS transistors. The aim of body biasing technique is to manipulate the delay and leakage of the circuit by modulating the threshold voltage. The focus of our research is on the application of body biasing as the method for standby leakage reduction.

Traditionally, RBB scheme has not taken into account the impact of on-state networks of CMOS circuit since reverse body bias (V_R) applied to all substrates

regardless of state status (on- and off-state) of CMOS network; reverse body bias only reduces the subthreshold leakage in off-state networks of CMOS circuits by increasing threshold voltage (V_{th}), whereas, on-state networks in CMOS circuits do not present the subthreshold leakage because the drain and source terminal node of all transistors in on-state network have same voltage, thereby ineffective in on-state network. To make things worse, reverse body bias in on-state network increase the both gate and BTBT leakage by increasing the voltage between the gate and bulk node, and between the bulk to source/drain node, respectably. Thus, from a structural point of view, existing RBB technique has inherent drawbacks due to the redundant bias routing in on-state network. The RBB technique needs to take all of the above factors into consideration since subthreshold leakage is no longer the only serious leakage source in nanometer-scale technologies.

In this chapter, motivated by the above observations, we propose the novel leakage-aware body biasing methods called Reverse Body Biasing only in off-state CMOS network (RBB-off) and Hybrid Body Biasing (HBB) to increase the effectiveness of body biasing in leakage reduction.

The RBB-off technique combines the advantages of two well-known leakage reduction techniques, the Input Vector Control (IVC) technique [16]-[18] and the RBB technique. The IVC technique reduces the leakage power when the circuit is in standby mode by deploying the best input vector (minimum leakage vector) with the help of a sleep signal. Our work assumes that a triple-well process is supported for independent body biasing of both N-well and the P-well, and the minimum leakage vector of each circuit block is predetermined by IVC method, and hence information of on- and off-state network of each CMOS logic gate is given. Based on this information, RBB-off method applied V_R only to the off-state network in each CMOS logic gate in order to eliminate the adverse effects of existing RBB approach.

The HBB technique takes advantage of RBB-off technique and forward body bias (V_F) to maximize the overall leakage savings by body biasing. To control not only the subthreshold leakage but also gate leakage, the HBB technique applied V_F to on-state CMOS network and V_R to off-state CMOS network simultaneously. Therefore, compared with RBB-off, HBB method yields additional leakage savings by applying forward body bias (V_F) to on-state network in each logic gate; V_F in on-state network reduces the gate leakage by decreasing the gate to

bulk voltage. Hence, HBB technique can reduce the both gate and subthreshold leakage components.

The proposed leakage-aware body biasing methods (RBB-off and HBB techniques) do not have inherent problems related to RBB technique since proposed leakage reduction techniques do not applied V_R to on-state networks in CMOS circuits, and thus increase the effectiveness of body biasing for leakage power reduction. In addition, we combine the proposed methods with pin/transistor reordering technique for achieving further leakage power reduction. We investigate the characteristics of the proposed methods in terms of ability to reduce power consumption by examining the typical CMOS circuit cells such as an Inverter, NAND, NOR, XOR, XNOR, OR-AND-Inverter (OAI) and AND-OR-Inverter (AOI) gates.

The remainder of this chapter is organized as follows. To understand the impact of body bias on major leakage components, Chapter 6.2 analyzes the effect of reverse/forward body bias on a single transistor under various bias conditions. Based on this fundamental analysis, Chapter 6.3 demonstrate that a traditional way of using reverse body bias becomes ineffective in reducing overall leakage in nanometer-scale CMOS circuits, and then describes the

proposed leakage-aware body biasing methodologies. Chapter 6.4 draws conclusions.

6.2 Body Bias Effects on Leakage Components of CMOS Transistor

In this chapter, we use a modified Predictive Technology Model (PTM [49]) for 32nm HP bulk CMOS. This model based on a BSIM4 model [7] and the guidelines in the 2010 International Technology Roadmap for Semiconductors (ITRS) [4]. The leakage currents and powers are computed by HSPICE simulator excepted for BTBT leakage which is computed by using model presented in [20].

6.2.1 RBB Effects on Leakage Components

Reverse body bias effects on leakage components of transistor:

- I_{SUB} reduced as V_{th} increased by V_R.
- I_{GB} increased as V_{GB} increased by V_R.
- I_{BTBT} increased as V_{BD}/V_{BS} increased by V_R.

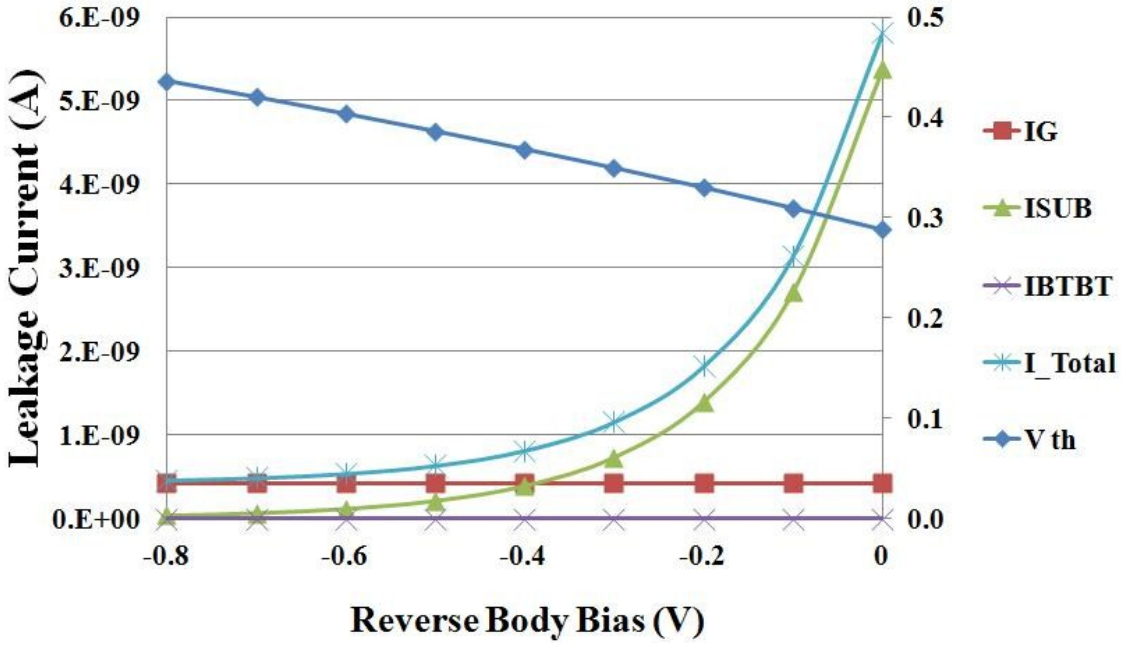

Figure 44: Standby leakage currents and threshold voltage of $S3_N$ (32nm with V_{DD}=0.9V and W/L=4) as a function of V_R, and the unit of right side of Y-axis is voltage (V).

Table 40: RBB effects on standby leakage current (nA) in $S3_N$ (32nm).

V_R	V_{th}	I_{GD}	I_{GB}	I_G	I_{SUB}	I_{BTBT}	I_{TOTAL}
-0.8	0.436	0.426	1.90E-4	0.426	0.038	6.57E-5	0.463
-0.6	0.403	0.426	8.16E-5	0.426	0.118	2.34E-5	0.543
-0.4	0.368	0.426	3.01E-5	0.426	0.393	7.44E-6	0.819
-0.2	0.330	0.426	8.01E-6	0.426	1.402	2.05E-6	1.827
0	0.289	0.426	0	0.426	5.383	4.72E-7	5.809

Figure 44 shows the reverse body bias (V_R) effects on leakage components of $S3_N$ transistor. When V_R applied to $S3_N$/ $S3_P$, I_{SUB} reduced as V_{th} increased by V_R, whereas increases of I_{GB} and I_{BTBT} are negligible as shown in Table 40.

In conducting transistor, such as $S2_N$ and $S4_N$, I_{SUB} did not exist since the I_{SUB} exist only in non-conducting (off) transistor with $|V_{DS}| > 0$. Therefore, when V_R applied to $S2_N$/$S4_N$, leakage current increased rather than decreased. For instance, the impact of V_R on leakage components of $S2_N$ transistor is shown in Figure 45 and Table 41. It can be observed that reverse body bias increase the gate leakage by increased the V_{GB}; this causes the I_{GB}, I_{gcs} and I_{gcd} to increase, whereas it does not affect the edge direct tunneling (EDT: I_{gdo} and I_{gso}) current which is the direct tunneling current between gate and drain/source.

In addition, leakage increases from I_{gcs}/I_{gcd} by applied V_R is negligible compared with that from I_{GB} by applied V_R. Note that leakage power is more sensitive than leakage currents due to the V_{GB} as shown in Figure 45. For example, V_{GB} is V_{DD} when V_R=0 (Zero Body Bias (ZBB)), and V_{GB}=2*V_{DD} when V_R=V_{DD}. Additionally, $S1_N$, $S4_N$, and $S5_N$ exhibit the same behavior (impact of V_R on leakage components) as $S2_N$ as listed in Table 42.

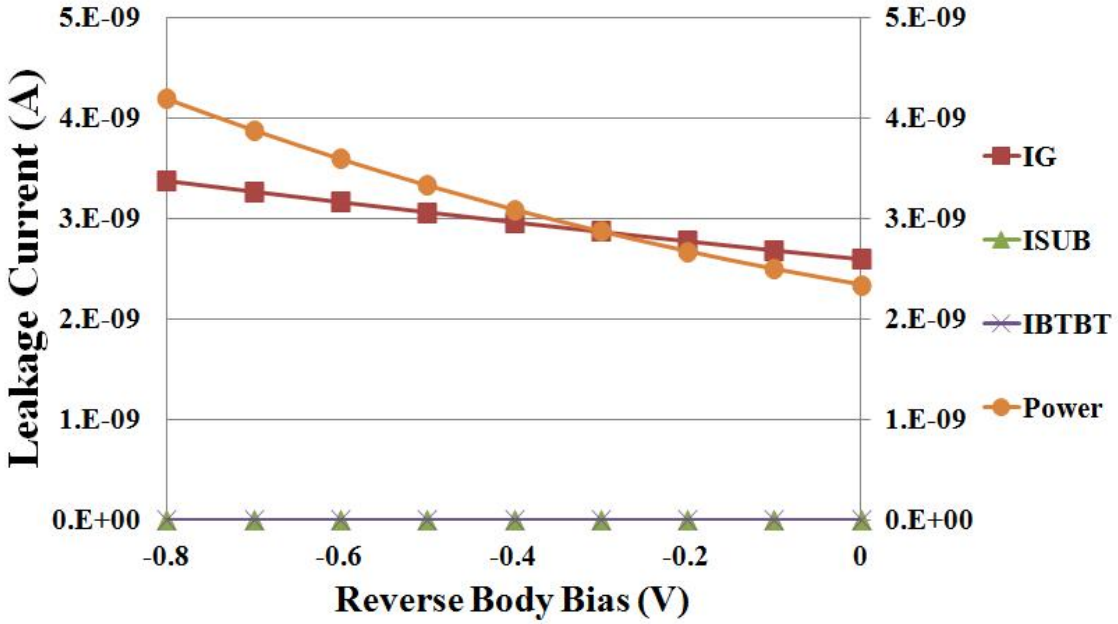

Figure 45: Standby leakage currents and power of $S2_N$ (32nm with V_{DD}=0.9V and W/L=4) as a function of V_R, and the unit of right side of Y-axis is power (W).

Table 41: RBB effects on standby leakage current (nA) in $S2_N$ (32nm).

V_R	$I_{gso/gdo}$	$I_{gcs/gcd}$	I_{GB}	I_G	I_{SUB}	I_{BTBT}	I_{TOTAL}
-0.8	0.155	0.808	1.444	3.369	0	1.74E-7	3.369
-0.6	0.155	0.805	1.241	3.160	0	2.39E-8	3.160
-0.4	0.155	0.802	1.048	2.962	0	2.15E-9	2.962
-0.2	0.155	0.800	0.866	2.775	0	9.80E-11	2.775
0	0.155	0.797	0.693	2.597	0	0	2.597

Table 42: Leakage power (nW) difference between ZBB and RBB at V_R=-V_{DD}.

Leakage	$S1_N$	$S2_N$	$S3_N$	$S4_N$	$S5_N$
P_G	2.51E-4	**2.19**	2.51E-4	8.46E-3	2.51E-4
P_{SUB}	0	0	**-4.83**	0	0
P_{BTBT}	1.93E-7	1.93E-7	1.12E-4	2.24E-4	2.24E-4
P_{TOTAL}	2.52E-4	**2.19**	**-4.83**	8.68E-3	4.75E-4

In Table 42, the negative and positive sign indicate a leakage reduction and growth by V_R, respectively. It is shown that gate leaky state ($S2_N$) and subthreshold leaky state ($S3_N$) are the most affected by V_R, whereas impact of the least leaky state ($S1_N$), least gate leaky state ($S4_N$) and reverse gate leaky state ($S5_N$) is negligible since four ($S1_N$ and $S5_N$) and three ($S4_N$) order of magnitude smaller than $S2_N$ and $S3_N$.

Therefore, the RBB technique is only effective in subthreshold leaky states ($S3_N$ and $S3_P$), whereas other steady states are ineffective due to the gate and BTBT leakage. In this chapter, the maximum V_R set to V_{DD}. Note that I_{BTBT} is strongly depends on N_a, and thus when applying dual-V_{th} technique [5] incorporating with high N_a, I_{BTBT} cannot be ignored and thereby the range of V_R limited by effect of I_{BTBT}.

6.2.2 FBB Effects on Leakage Components

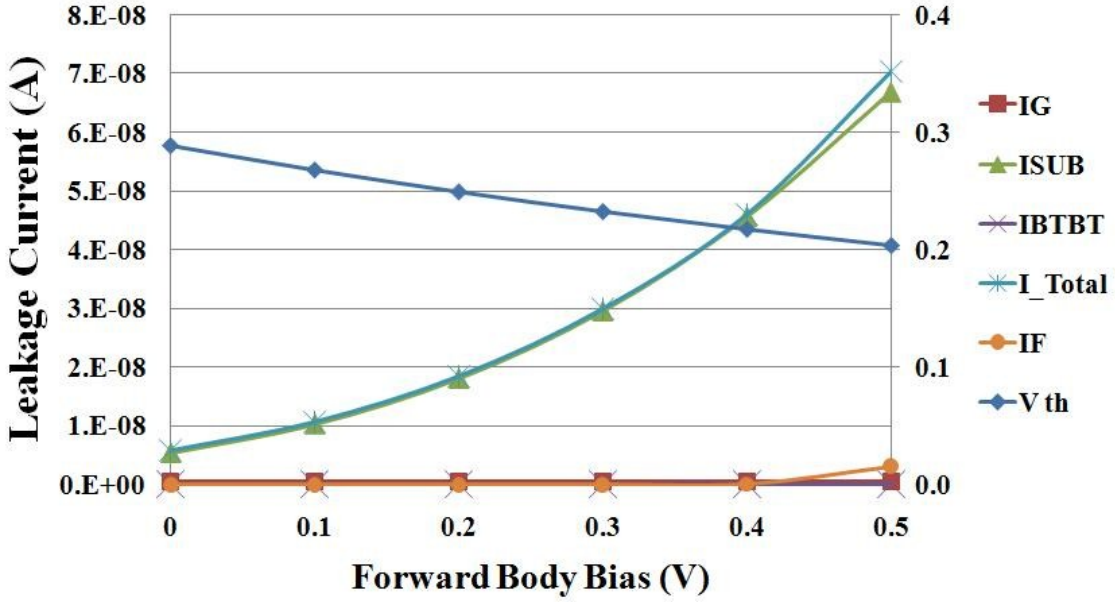

Figure 46: Standby leakage currents and threshold voltage of $S3_N$ (32nm with V_{DD}=0.9V and W/L=4) as a function of V_F, and the unit of right side of Y-axis is voltage (V).

Table 43: FBB effects on standby leakage current (nA) in $S3_N$ (32nm).

V_F	V_{th}	I_G	I_{SUB}	I_{BTBT}	I_F	I_{TOTAL}
0	0.289	0.426	5.383	4.72E-07	0	5.809
0.1	0.268	0.426	10.274	3.00E-07	9.01E-04	10.701
0.2	0.249	0.426	18.045	8.71E-08	9.27E-04	18.472
0.3	0.232	0.426	29.545	5.95E-08	2.21E-03	29.973
0.4	0.217	0.426	45.568	1.19E-08	6.49E-02	46.059
0.5	0.203	0.426	66.784	6.51E-09	3.140	70.350

Forward body bias (V_F) effects on leakage components of transistor:

- I_{SUB} increased as V_{th} decreased by V_F.
- I_{GB} decreased/increased as V_{GB} decreased/increased by V_F.
- I_{BTBT} decreased as V_{BD}/V_{BS} decreased by V_F.
- I_F increased as V_{BD}/V_{BS} increased by V_F.

In case of forward body bias, there is another factor that need to be taken into consideration in addition to three major leakage components (I_{SUB}, I_G and I_{BTBT}), which is the forward p-n junction leakage current (I_F). It should be noted that, the current between body to drain/source (I_{BD}/I_{BS}) can be either I_{BTBT} or I_F depends on the status of junction bias voltage between bulk and source/drain; reverse biased p-n junction leakage presents the I_{BTBT} , whereas forward biased p-n junction leakage presents the I_F. Hence, ZBB and RBB cases do not present the I_F.

Figure 47 shows the forward body bias (V_F) effects on leakage components of the $S3_N$ transistor. When applied V_F to $S3_N/S3_P$, I_{SUB} increased as V_{th} decreased by V_F, and I_F (I_{BS}) increased with V_F increased, while impact of V_F on I_G and I_{BTBT} (I_{BD}) is negligible as shown in Table 43.

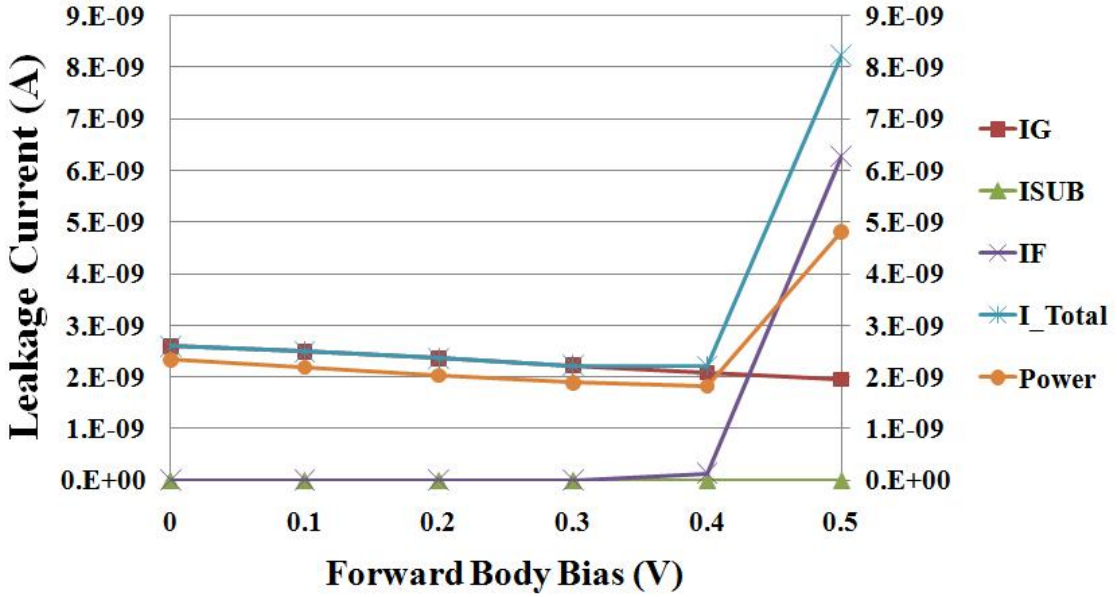

Figure 47: Standby leakage currents and power of $S2_N$ (32nm with V_{DD}=0.9V and W/L=4) as a function of V_F, and the unit of right side of Y-axis is power (W).

Table 44: FBB effects on standby leakage current (nA) in $S2_N$ (32nm).

V_F	$I_{gso/gdo}$	$I_{gcs/gcd}$	I_{GB}	I_G	I_{SUB}	I_F	I_{TOTAL}
0	0.155	0.797	0.693	2.597	0	0	2.597
0.1	0.155	0.794	0.595	2.493	0	2.01E-04	2.493
0.2	0.155	0.786	0.482	2.363	0	4.53E-04	2.363
0.3	0.155	0.774	0.366	2.223	0	3.21E-03	2.226
0.4	0.155	0.758	0.258	2.083	0	0.129	2.212
0.5	0.155	0.738	0.168	1.953	0	6.280	8.233

In steady states of $S2_N/S2_P$, V_F decrease I_G by decreasing V_{GB}, whereas I_F increased by increasing forward p-n junction of V_{BD} and V_{BS}.

The impact of V_F on leakage components of $S2_N$ transistor is shown in Figure 47 and Table 44. It can be observed that I_F limited the range of V_F. The maximum $|V_F|$ is conservatively assumed to be 0.6 V [50]. In this chapter, maximum $|V_F|$ set to the minimum point of overall leakage. In addition, I_{GB} can be either increase or decrease by V_F depends on its V_{GB}; in case of $V_{GB}=V_{DD}$ ($S2_N$ and $S4_N$), I_{GB} decrease as V_{GB} decreased by V_F, whereas, in case of $V_{GB}=0$ ($S1_N$ and $S3_N$), I_{GB} increase as V_{GB} increased by V_F.

Table 45: Leakage power (nW) difference between ZBB and FBB at V_F=0.4V.

Leakage	$S1_N$	$S2_N$	$S3_N$	$S4_N$	$S5_N$
P_G	6.83E-07	-0.566	7.00E-07	-2.54E-05	7.00E-07
P_{SUB}	0	0	36.167	0	
P_{BTBT}	0	0	-4.19E-07	-8.38E-07	-8.38E-07
P_F	5.16E-02	5.16E-02	2.60E-02	0	0
P_{TOTAL}	5.16E-02	-0.514	36.193	-2.63E-05	-1.38E-07

Table 45 shows that the forward body bias impact on leakage power of five different steady states of NMOS transistor; the negative and positive sign indicate a leakage reduction and growth by V_F, respectively. It can be observed

that other than gate leaky state ($S2_N$), impact of V_F on P_G (I_G) is negligible. The gate leaky state ($S2_N$) and subthreshold leaky state ($S3_N$) are the most affected by V_F, whereas the impact of V_F on the other steady states is negligible.

Table 46: Leakage power (nW) comparison under different steady states.

Leakage	$S1_N$	$S2_N$	$S3_N$	$S4_N$	$S5_N$
P_G	0	2.337	0.383	2.51E-04	0.766
P_{SUB}	0	0	4.845	0	0
P_{BTBT}	0	0	4.25E-07	8.50E-07	8.50E-07
P_{TOTAL}	**0**	**2.337**	**5.228**	**2.52E-04**	**0.766**

In summary of this section, gate and subthreshold leaky steady states are the most influenced by forward and reverse body biasing as shown in Table 42 and Table 45, and these steady states are the basic steady states of CMOS logic gate as described in chapter 3.4. Moreover, the highest order of magnitude in leakage power consumption among steady states is also the gate and subthreshold leaky steady states as listed in Table 46; the gate leaky state and subthreshold leaky state are at least an order of magnitude larger than other steady states. Therefore, the impact of body bias on leakage sources of on- and off-state network can be characterized by gate leaky state and subthreshold leaky state respectively.

An important point to note is that impact of V_F on subthreshold leaky state ($S3_N$ in Table 43) is not a factor since neither existing RBB technique nor our proposed leakage-aware body biasing techniques applies V_F to off-state network in standby mode.

6.3 Leakage-aware Body Biasing Technique

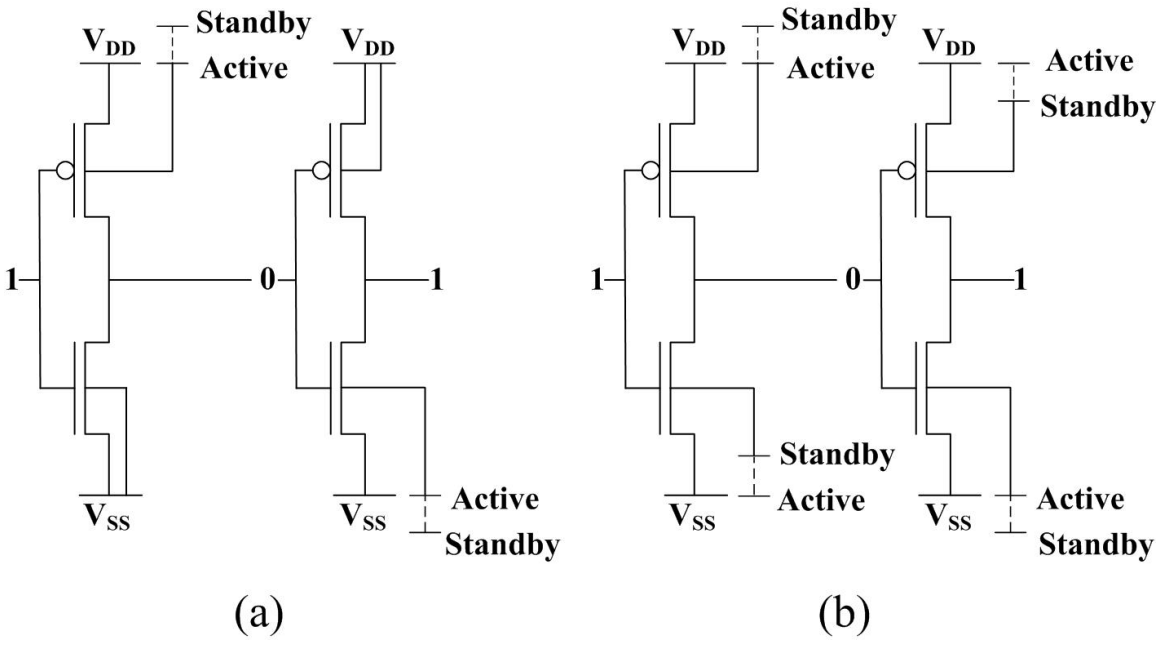

Figure 48: (a) RBB-off (b) Hybrid Body Biasing (HBB).

Table 47: Comparison of leakage power (nW) and savings (%) in different body biasing techniques in Inverter.

Input vector	Leakage Power (nW)				Leakage Savings (%)		
	ZBB	RBB	RBB-off	HBB	RBB	RBB-off	HBB
0	6.141	4.522	1.319	0.692	26.36	78.53	88.72
1	6.344	4.546	2.356	1.842	28.34	62.86	70.96
Average	6.242	4.534	1.838	1.267	27.37	70.56	79.70

RBB technique applied reverse body bias to each substrate regardless of status (on- or off-state) of network as shown in Figure 43. Unlike the RBB technique, proposed RBB-off and HBB methods depend on status of network (on- and off-state) when applying reverse/forward body bias to substrate.

The RBB-off scheme applied reverse body bias to only off-state network in CMOS logic gate, and HBB scheme applied forward body bias to on-state network and reverse body bias to off-state network of each CMOS logic gate as shown in Figure 48. Hence, both RBB-off and HBB methods eliminate the negative effects of existing RBB technique since proposed techniques never applied reverse body bias to on-state in CMOS network. Furthermore, HBB scheme yields additional leakage savings by applying forward body bias to on-state CMOS network, which reduces the gate leakage. Note that proposed HBB technique did not increase the subthreshold leakage since V_F always applied to

on-state network of CMOS logic gate. Comparison of the effect of body biasing techniques on leakage reduction in Inverter is tabulated in Table 47. It is shown that the HBB technique yields the best saving among body biasing techniques, whereas RBB technique yields the worst savings due to the V_R in on-state network. ZBB stands for Zero Body Bias applied to the circuit, which is an original circuit, and leakage savings computed from ZBB.

In the rest of this chapter, we narrow down our focus on the main steady states (gate and subthreshold leaky states) due to the following reasons:

- Main steady states are presented in every CMOS logic gate unlike the other steady states.
- The highest leaky state of both on- and off-state network is the main steady states.
- Main steady states are the most affected by body biasing.

As aforementioned, two cases of input vector are existed in CMOS logic gates; one produces the same gate input state (either high or low logic value), and the other one produces the different gate input states (high and low logic values). Let us therefore consider these two cases separately.

6.3.1 Same Gate Input State in CMOS Logic Gate

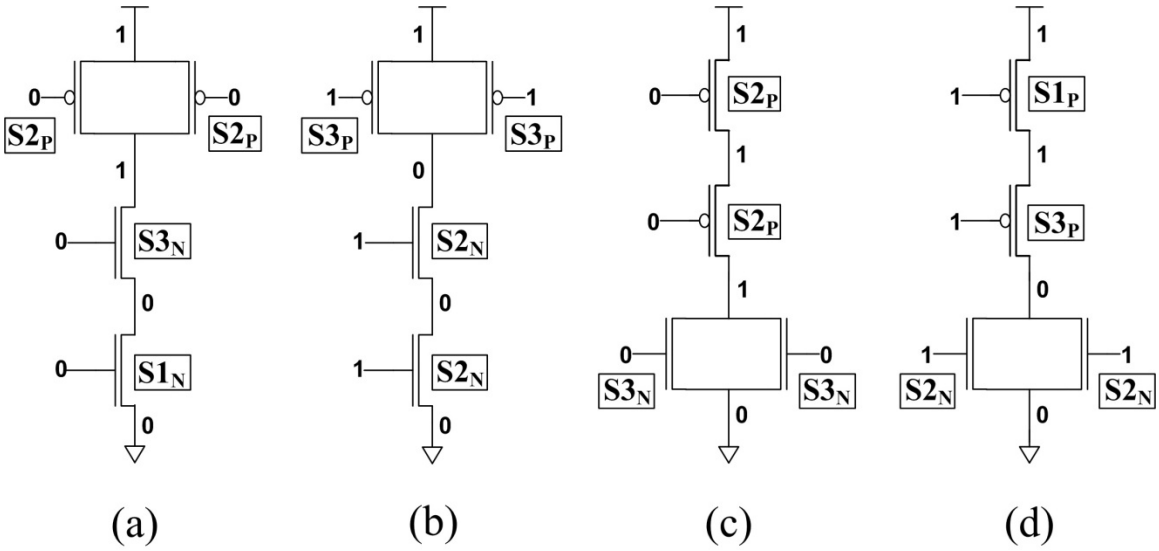

Figure 49: Steady states of a 2-input NAND ((a) and (b)) and NOR ((c) and (d)) gates in same gate input states: input=00 ((a) and (c)), input=11 ((b) and (d)).

In case of same gate input state in NAND/NOR gate, on-state network consists of gate leaky state ($S2_N/S2_P$), while off-state network consists of subthreshold leaky state ($S3_N/S3_P$) and least leaky state ($S1_N/S1_P$), thereby gate leaky state does not present on off-state network under the same gate input state. Hence, n-input vector of NAND/NOR gate always produces n gate leaky states in on-state network, while off-state network presents either one or n subthreshold leaky state depends on its structure; parallel structure in off-state

network yields at most number (n) of subthreshold leaky state while serial structure in off-state network yields at least number (1) of subthreshold leaky state. For instance, 2-input NAND and NOR gate have the 2 gate leaky states in on-state network regardless of its structure (both series (Figure 49 (b) and (c)) and parallel (Figure 49 (a) and (d)), while off-state network has one subthreshold leaky state in serial structure (Figure 49 (a) and (d)), and has two subthreshold leaky state in parallel structure (Figure 49 (b) and (c)).

In addition, same gate input state in n-input vector of complex-NAND (NOR) logic gate type (such as OAI (AOI)) also produces "n" gate leaky state(s) in on-state network, whereas at most number of subthreshold leaky states always less than "n" since the parallel structure of complex logic gate has series-connected transistor as shown in Figure 12 (Figure 14); when the input vector (ABC) of OAI-21 (AOI-21) gate is "111" ("000"), off-state network (parallel structure) presents "2" subthreshold leaky states while on-state network (serial structure) presents "3" gate leaky states.

Table 48 lists the comparison of the effect of body biasing techniques on leakage savings in 2- input NAND and NOR gates.

Table 48: Comparison of leakage power (nW) and savings (%) in different body biasing techniques in 2- input NAND and NOR gates under same input logic value.

Gate type	Input vector	Leakage Power (nW)				Leakage Savings (%)		
		ZBB	RBB	RBB-off	HBB	RBB	RBB-off	HBB
NAND2	00	3.331	8.626	2.219	0.967	-158.96	33.38	70.98
	11	12.689	9.090	4.713	3.684	28.36	62.86	70.97
NOR2	00	12.281	9.044	2.637	1.385	26.36	78.52	88.72
	11	5.227	9.062	4.684	3.656	-73.37	10.38	30.06

The difference between RBB and RBB-off indicates the increases of leakage power in on-state network by V_R. Further, when the off-state network has stacking effect, the increases of leakage power in on-state network even overwhelmed the leakage reduction from off-state network; existing RBB scheme increases the leakage rather than decrease when input vector is composed of the low (high) logic value in NAND (NOR) gates.

To make things worse, such phenomenon in RBB technique becomes even more severe as the number of input vectors increase; when the input vector of 5-input NAND gate is "00000", on-state network has 5 gate leaky state, and off-state network is in stacking effect. Whereas, the HBB technique is the most benefit from this situation. In the same gate input state of n-input CMOS logic

gates, proposed body biasing methods have not had any negative effects, whereas RBB technique suffer from the "n" gate leaky states in on-state network.

6.3.2 Different Gate Input States in CMOS Logic Gate

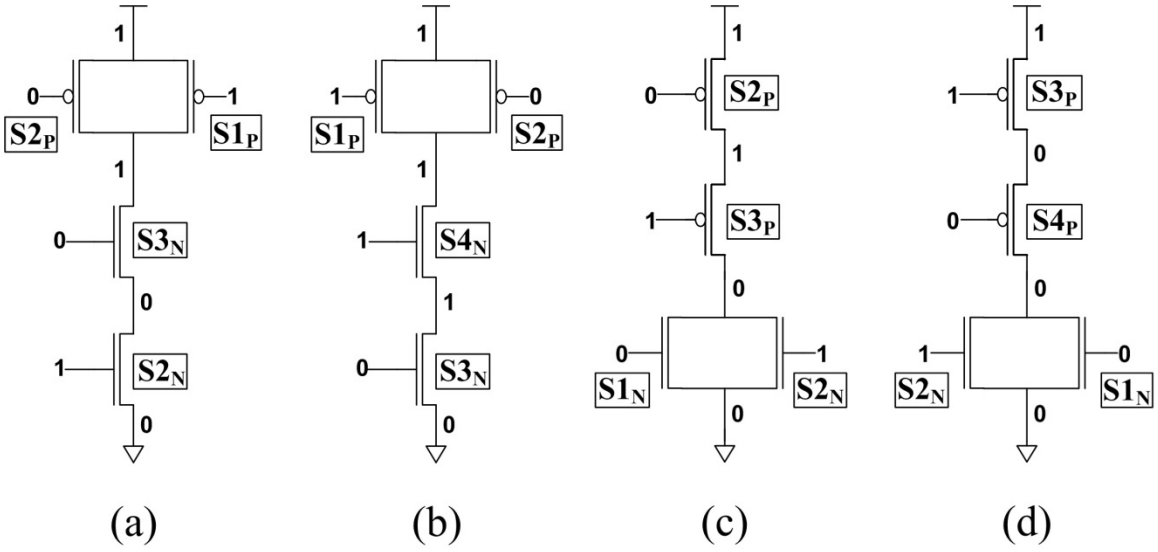

Figure 50: Steady states of a 2-input NAND ((a) and (b)) and NOR ((c) and (d)) gates in different gate input states: input=01 ((a) and (c)), input=10 ((b) and (d)).

In case of different gate input states in NAND/NOR gate, on-state network is the parallel part of gate since one of the different logic values make at least one transistor always "on" (gate leaky state), while off-state network is the serial part of gate, and thus only one transistor presents the subthreshold leaky state as

shown in Figure 50; if transistors of off-state network connected in series, the first off-transistor from output node presents the subthreshold leaky state, and rest of off-transistor(s) present the least leaky state.

It should be noted that, unlike same gate input state, gate leaky state ($S2_N/S2_P$) present not only on-state network but also off-state network; the presence of gate leaky state depends on the correlation with subthreshlod leaky state as discussed in the previous Chapter 4.2. Therefore, the efficiency of body biasing is reduced in the presence of most gate leaky state in off-state network; input "10" in NAND and NOR gates yield better leakage savings than input "01" as illustrated in Table 49.

Table 49: Comparison of leakage power (nW) and savings (%) in different body biasing techniques in 2- input NAND and NOR gates under different input logic values.

Gate type	Input vector	Leakage Power (nW)				Leakage Savings (%)		
		ZBB	RBB	RBB-off	HBB	RBB	RBB-off	HBB
NAND2	01	8.476	9.050	5.845	5.316	-6.77	31.04	37.28
	10	4.706	4.296	1.091	0.562	8.72	76.82	88.07
NOR2	01	7.255	8.662	6.475	6.009	-19.40	10.75	17.17
	10	4.773	4.557	2.366	1.904	4.53	50.43	60.12

In worst case, gate leaky state present at most n times in n-input NAND/NOR gate under different gate input states; if n-input vector (n=x + y) consists of "x" number of high input value and "y" number of low input value, on-state network presents "x" (pull-down)/"y" (pull-up) gate leaky state(s), while off-state network presents "y" (pull-up)/"x" (pull-down) gate leaky state(s) when all conducting transistor(s) of off-state pull-down (pull-up) network located in below (above) of the nonconducting transistor(s).

For instance, n-input NAND gate consists of different logic values (n=x + y), and all "x" number of high input transistors (conducting transistor) located under the "y" number of low input transistor (nonconducting transistor) in off-state pull-down network. In such formation of off-state pull-down network presents the "x" number of gate leaky states along with "y" number of gate leaky states in on-state pull-up network, resulting in "n" gate leaky states are presented as shown in Figure 50 (a). Additionally, n-input NOR gate case (off-state pull-up network) is shown in Figure 50 (c).

In order to fully take advantage of proposed leakage-aware body biasing techniques, gate leaky state should be eliminated in off-state network. To solve this problem, we use a pin/transistor reordering technique which excludes the

gate leaky state in off-state network as described in Chapter 4. For this reason, it is entirely possible to achieve the maximum leakage savings by reverse body biasing in off-state network.

Table 50: Leakage power savings (%) obtained through pin/transistor reordering in different body biasing techniques.

Gate type	Pin/Transistor reordering	Leakage Savings			
		ZBB	RBB	RBB-off	HBB
NAND2	01 → 10	44.48	52.54	81.34	89.43
NAND3	001 → 100	45.41	27.45	61.43	82.50
	010 → 100	17.38	3.68	13.86	32.26
	011 → 110	54.06	58.96	84.98	91.49
	101 → 110	34.50	40.84	73.16	83.81
NOR2	01 → 10	34.21	47.39	63.45	68.32
NOR3	001 → 100	43.04	64.21	77.51	80.64
	010 → 100	18.19	47.27	63.27	67.55
	011 → 110	15.53	31.11	46.59	52.41
	101 → 110	7.86	21.76	34.96	40.42
XOR2 (XNOR2)	00 (01) : Type 1 → Type 2	34.22	47.4	63.44	68.34
	01 (00) : Type 3 → Type 4	28.58	35.62	68.55	80.89
	01 (00) : Type 5 → Type 4	44.44	52.53	81.34	89.44
	10 (11) : Type 3 → Type 5	28.58	35.62	68.55	80.89
	10 (11) : Type 4 → Type 5	44.44	52.53	81.34	89.44
	11 (10) : Type 2 → Type 1	34.22	47.4	63.44	68.34
OAI-21	001 : Type 2 → Type 1	34.30	32.22	62.76	75.70
	010 : Type 2 → Type 1	34.30	32.22	62.76	75.70
	011 : Type 2 → Type 1	55.33	68.15	89.22	93.11
	100 : Type 1 → Type 2	37.19	36.99	70.09	83.56
	101 → 110	18.25	31.08	46.5	52.29
AOI-21	001 → 010	25.81	35.24	66.37	79.13
	011 : Type 1 → Type 2	31.19	31.13	46.58	52.37
	100 : Type 2 → Type 1	40.31	64.2	77.50	80.63
	101 : Type 2 → Type 1	25.85	31.09	46.54	52.34
	110 : Type 2 → Type 1	25.85	31.09	46.54	52.34

Table 50 shows the leakage power savings by removing the most gate leaky state in off-state network of original gate (ZBB) and body biasing techniques. The structure types of complex gates (XOR, XNOR, OAI-21 and AOI-21) in Table 50 are shown in Figure 29, Figure 30 and Figure 31. An important point to note is that pin/transistor reordering technique for effective body biasing is not only increasing the efficiency of body biasing but also reducing the leakage power of original gate by implementing the lowest leakage state in each input vector of logic gates.

Table 51: Comparisons of average leakage power savings (%) in different body biasing techniques.

Gate type	ZBB	RBB		RBB-off		HBB	
	w pin/tr	w/o pin/tr	w pin/tr	w/o pin/tr	w pin/tr	w/o pin/tr	w pin/tr
NAND2	12.91	-6.37	9.91	52.51	68.79	63.95	80.23
NOR2	8.40	-6.06	7.84	45.28	59.19	56.14	70.04
NAND3	22.46	-44.42	-3.55	33.57	68.32	47.74	82.90
NOR3	9.72	-42.28	-11.34	16.39	47.33	28.79	59.73
XOR2 (XNOR2)	24.79	-5.34	29.79	37.45	72.59	45.32	80.46
OAI-21 (Type1)	10.87	-16.44	-3.38	48.61	61.67	61.34	74.40
OAI-21 (Type2)	18.87	-21.4	5.90	37.81	65.11	49.40	76.70
AOI-21 (Type1)	10.18	-13.14	-1.30	45.82	57.61	57.88	69.66
AOI-21 (Type2)	15.10	-22.38	4.25	33.35	59.93	44.75	71.32

Table 51 shows the comparisons of average percentage leakage reduction obtained through all possible inputs using without pin/transistor reordering and with pin/transistor reordering under different body biasing techniques. It can be observed that effectiveness of body biasing increases as the most gate leaky state eliminated by pin/transistor reordering. Thus, proposed body biasing techniques along with pin/transistor reordering yields considerable leakage power savings compared to conventional RBB technique.

6.3.3 Summary

The efficiency of body biasing for standby leakage savings is reduced in the presence of most gate leaky state in on- and off-state network. It is observed that the n-input CMOS logic gates can be presented the "n" most gate leaky state in both same and different gate input states. Furthermore, unlike the same gate input state, the different gate input states of CMOS logic gate present the most gate leaky state not only on-state network but also off-state network depends on its input vector. For this reason, conventional RBB technique is not sufficient to reduce the overall leakage under these circumstances.

To overcome these problems, we first eliminate the negative effect from on-state CMOS network by proposed leakage-aware body biasing techniques, then remove the negative effect from off-state CMOS network by applying pin/transistor reordering technique, thereby enhancing the effectiveness of body biasing by eliminating the adverse effects of most gate leaky state in both on- and off-state CMOS network.

6.4 Summary

In this chapter, reverse/forward body bias effects on standby leakage components in nanometer-scale CMOS transistors and logic gates are studied. We analyzed the RBB technique from a structural point of view, and addressed the problems associated with overall leakage savings due to the lack of awareness of other than subthreshold leakage. To solve this problem, we proposed the leakage-aware body biasing methods which take into account not only the subthreshold leakage but also gate and BTBT leakage, resulting in enhanced the effectiveness of body biasing for leakage power reduction. Therefore, proposed methodologies are promising circuit techniques for future

CMOS technologies by increasing the effectiveness of existing body biasing technique, thereby alternative methods for RBB technique.

Chapter 7
Conclusion and Future work

7.1 Summary and Conclusion

In this dissertation, we have presented a novel transistor reordering method for leakage reduction. In previous approach, the effects of pin reordering on reverse gate tunneling current and pull-up network of a CMOS gate are not considered, and thus it is not sufficiently accurate to analyze the leakage reduction through pin reordering. This leads to misleading results when the concept of pin reordering for leakage reduction is extended to pull-up network of CMOS circuits and complex CMOS logic gates. Furthermore, there are limitations of using the pin reordering in complex CMOS logic gates. To overcome these problems, we proposed a novel transistor reordering method for leakage reduction. Unlike previous approach, the proposed method provides exact reordering rules for minimum leaky formation by analyzing all leakage components.

We also proposed a leakage-aware body biasing methodology to maximize the efficiency of body biasing technique for leakage reduction. In this work, we first investigated the effect of reverse body bias on all possible conditions for a single transistor in CMOS circuits. Then, we demonstrated that a conventional RBB technique can result in higher leakage power than original circuit in deep submicron region due to the lack of awareness of other than subthreshold leakage. In order to overcome the shortcomings of the conventional RBB technique, we presented the leakage-aware body biasing methodology which takes into account not only the subthreshold leakage but also gate and BTBT leakage, resulting in better leakage savings than existing RBB technique. In order to maximize the leakage reduction and efficiency, we combined the proposed method with pin/transistor reordering technique.

7.2 Future work

- **Investigating the effect of pin/transistor reordering on circuit delay:** In our research, we focus on reducing leakage power consumption, and did not consider the effect of pin/transistor reordering on circuit

delay. So, this should be analyzed and designed in order to meet the circuit performance value.

- **Analyzing the impact of loading effect on leakage current:** The impact of the loading effect on leakage current is considered to further enhance the accuracy of leakage current analysis in standby leakage reduction methods.

- **Combining the leakage-aware body biasing method with other leakage reduction techniques:** Usually, many low power techniques are combined to augment the leakage savings. Hence, it is possible to combine with other techniques, such as MTCMOS, to achieve better leakage savings.

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