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BROADBAND MATCHING FOR CIRCUITS WITH RESISTIVE TERMINATIONS

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BROADBAND MATCHING FOR CIRCUITS WITH RESISTIVE TERMINATIONS

BY

MICHAEL KLEMPA

B.S. in Electrical Engineering , University of New Hampshire, 2013

THESIS

Submitted to the University of New Hampshire

in Partial Fulfillment of

the Requirements for the Degree of

Master of Science

in

Electrical and Computer Engineering

May, 2017

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ABSTRACT

BROADBAND MATCHING FOR CIRCUITS WITH RESISTIVE TERMINATIONS

by

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University of New Hampshire, May, 2017

The work presented here explores the broadband matching characteristics for representative circuits with resistive terminations for frequencies up to 40 GHz, the typical band of interest for 100 Gigabit Ethernet (100GbE) applications. A simple test circuit comprised of high-frequency connectors, microstrip transmission lines and resistive terminations was designed and fabricated to better understand the mechanisms affecting broadband matching.

High fidelity measurements were performed using both a vector network analyzer (VNA) and a time-domain reflectometer (TDR). The data provided by these two devices were used to isolate the broadband behavior of the individual circuit components through the time-gating process, and that process showed the microstrip transmission line on FR-4 to be the greatest contributor to high-frequency mismatch. One facet of the work presented here was to explore the accuracy of a state-of-the-art electromagnetics model in estimating the broadband behavior of the test circuit. Comparisons of measured and modeled data are provided here, and those comparisons show reasonable agreement.

CHAPTER 1

INTRODUCTION

The objective of this thesis is to provide a thorough study of broadband matching, specifically for circuits with a resistive termination, using contemporary equipment and modeling methods. Guidelines currently exist [1] for broadband matching (IEEE 802.3bj), and these guidelines are used to serve as a reference for much of the data provided in this thesis. The guidelines relate to 100G Ethernet channel specifications which recommend data collection to frequencies up to 40 GHz [2]. Broadband matching with resistive terminations will be a common test fixture solution for the new QSFP-DD specification [3], which stacks a second port onto the typical QSFP receptacle to increase the density of ports found on a typical 100GbE switch. Resistive terminations are required because the typical SMA load termination is physically impossible due to the tight spacing of the pads on a QSFP-DD port.

The test circuit board used in this study consisted of seven, nearly-identical circuits comprised of an SMA connector, microstrip transmission line and resistive termination. Having duplicate circuits on the test board allowed for the assessment of measurement repeatability. Measurements were performed using a VNA to be consistent with the IEEE return-loss specification, and a TDR was used to isolate the components of the circuit using time gating. Similar results were observed in both the time- and frequency-domain measurements for the circuit after transformation into a common domain, thus providing validation in measurement accuracy. To gain a further perspective into the broadband match and the individual circuit elements themselves, the windowing process in the time domain known as time gating was used to remove the measurement artifacts caused by

discontinuities of circuit elements that were not under analysis. The time windows used were extracted from the TDR measurement using a series of open-circuit measurements to define the location of test circuit components.

In addition to performing broadband measurements for the resistive termination, two different modeling approaches were implemented with the objective of validating the measured data and assessing the suitability of these models to estimate broadband performance at high frequencies. Both modeling approaches were carried out using the industry-standard electromagnetics modeling code HFSS (High-Frequency Structure Simulator) by Ansoft [4]. In one of these approaches, a detailed layout of all of the circuit components (connector, microstrip and resistor) were used as inputs to the model. In the other approach, only the connector and microstrip were modeled from an electromagnetic perspective, and the resistor was replaced in HFSS by the lumped-circuit model provided by the resistor manufacturer [5]. Comparisons of data generated by the different modeling approaches with measured data are presented in Section 4 – Measurements of Test Circuit.

CHAPTER 2

TEST CIRCUIT DESCRIPTION

The test circuit used for this work was designed with the objective of determining broadband performance and measurement repeatability for a circuit that was built using standard, best-practice design techniques and components. The test circuit board contained seven, nearly-identical sub-circuits (lanes, or test circuits) which were comprised of an SMA connector connected to a microstrip transmission line terminated in a surface-mount resistor. The inclusion of multiple sub-circuits facilitated the determination of measurement repeatability. As is described below, the components chosen for the design were typical of what is used in standard, high-quality designs, which enabled a representative circuit to be evaluated.

A standard, 50Ω edge-mount SMA connector was used to bridge the coaxial medium from the test equipment to the 50Ω microstrip trace on the circuit board. SMA connectors are commonly used in 100GbE applications during the evaluation phase where electrical conformance measurements need to be performed. The typical SMA connector bandwidth is rated to 26 GHz [6], so the SMA was not expected to be a major contributor to impedance mismatch in this research, and that proved to be the case.

FR4 was used as the circuit-board material in this study because it is the most commonly used material for PCB manufacturing. The properties of FR4 are well documented [7], making it straightforward to model. It is recognized that FR4 may not be suitable for applications with long trace lengths that may exist in some 100GbE designs. Rogers Material is commonly used for high-speed, long-trace lengths that require minimal loss. Studies have shown FR4 to be suitable for trace lengths

under 10” at 20GHz [8], with an insertion loss of -9dB. The loss from the trace is not considered to be an issue in this study.

The selection of resistors was fairly straightforward, for at the time of the study there was only one resistor advertised with a data sheet detailing expected behavior at the high frequencies (50 GHz) at which it would be tested. Thin-film, chip surface mount resistors (model CH0603-50RJNT) were chosen to terminate the microstrip. These resistors were chosen to investigate the broadband performance of the test circuit in a typical scenario, intended to provide an adequate match broadband, even though that was not the result found. DC measurements of the resistors ranged from 48 Ω to 52 Ω , or $\pm 4\%$, but subsequent tests at higher frequencies show these terminations with an impedance well beyond this measured range.

The test circuit as described was meant to give a fundamental understanding of broadband performance with commonly used components. The test circuit board was designed in Altium Designer version 6.9 and the fabrication files were sent to Sunstone for fabrication. The microstrip transmission line on the printed circuit board was designed and fabricated using commonly-used design techniques [9] so as to achieve a characteristic impedance of 50 Ω . The simplicity of the design allowed for a single layer board, but a four-layer board was used to accommodate the 50 Ω SMA connector and to be representative of typical network equipment designs. The layout for each layer can be seen in Appendix A. The test circuit includes a mounting pad for the SMA and a pad for the termination tied to a via with a return path on the layer below. The bare boards were then populated with the resistors and SMA connectors. An image of the populated board can be seen in Figure 2.1. The finalized test circuits were then measured as described in the subsequent section.

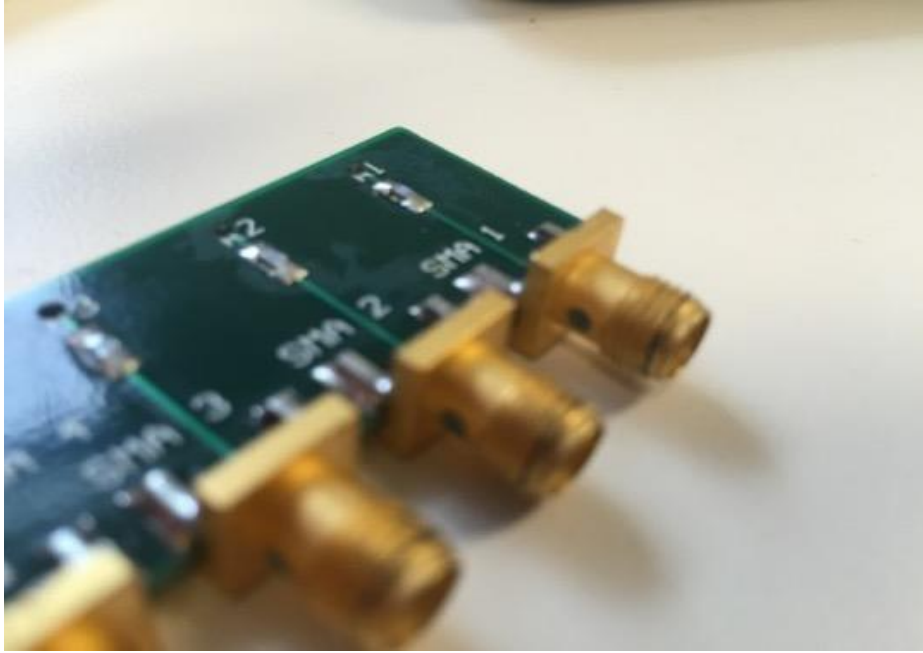


Figure 2.1 - Fully Populated Fabricated Test Circuit Board Used In Research

CHAPTER 3

MEASUREMENTS OF TEST CIRCUIT

Broadband measurements on the test circuit were performed in both the time and frequency domains using a VNA and a TDR. This dual-domain approach to data collection facilitated the evaluation of the broadband performance of each of the three components of the circuit (i.e., the SMA connector, the microstrip transmission line and the resistive termination) through the use of time gating, and it provided a means for validating the measured results.

A TDR measures broadband performance by sending a short-time-duration pulse into the system being evaluated and then analyzing the signals that are reflected back. Those reflections are caused by discontinuities in the impedance in the circuit, and they can be used to identify where one component ends and another one begins. If the circuit under test is perfectly matched for all of the frequencies contained in the pulse, there will be no discontinuities in impedance and hence there will be no reflections. For the measurements described here, the discontinuities evident in the TDR data were used to pinpoint the location in time for the components, and that information was used to evaluate individual circuit components with the process of time gating, which is detailed in Appendix C.

In contrast to the broadband pulse sent by the TDR, the VNA sends a sinusoidal signal to the device under test, and then measures the reflected signal received. By sweeping the input sinusoid over a range of frequencies, the broadband performance of the device under test can be determined. The ratio of the reflected signal to the sent signal is the return loss (denoted S_{11}) of the device and it will equal zero dB broadband for a perfectly-matched system. If the device has multiple ports,

the signals received at those ports, referenced to the transmitted signal, provide an indication of coupling between the ports. For example, S_{21} indicates the amount of signal received at port 2 referenced to an input on port 1.

In this study described here, a four-port network analyzer was available, allowing not only for return loss on the circuit under test but the coupling effects of adjacent lanes from the test circuit board. In a single port network on a multiport piece of test equipment such as this, the S-Parameters S_{21} , S_{31} and S_{41} typically associated with insertion loss provided insight to the coupling effects of adjacent lanes known as crosstalk for additional signal integrity validation. The data acquired from the VNA provided a means for test circuit validation against the expectations set by the IEEE 802.3bj return loss limits defined in the frequency domain. The limits were also imposed on the isolated and transformed time domain data.

A 40GHz Keysight N5245A VNA was used to collect return loss data as a function of frequency. VNA measurements can be extremely stable and precise because they typically do not contain errors caused by fluctuations of the input signal. Since the measurement is a vector ratio of the input and output signals, the results ignore any fluctuations in the measurement [10]. The measurement uncertainty of the VNA is an order of magnitude below that of the TDR due to its higher dynamic range [11]. The VNA was calibrated using an electronic calibration kit, which covered frequencies from 10 MHz to 40 GHz in 10 MHz steps. A picture of the test setup can be found in Figure 3.1. An insertion loss plot of the VNA test setup can be found in Appendix D, showing at most 0.2 dB of return loss out to 40 GHz on the cables used to make the return loss measurements on the test circuit.

Noise caused by reflections from other circuits degrading the signal of the circuit under test, known as crosstalk, was also analyzed in the frequency domain. Crosstalk measurements were performed to see the magnitude of the coupling effects adjacent test circuits had broadband. Achieved by sending a stimulus down all other lanes and capturing the energy being received by the circuit under test, crosstalk was measured as detailed in [12]. Figure 3.2 shows the crosstalk results from the three closest test circuits on the first test circuit. The coupling from test circuit 2 onto test circuit 1 was 10dB greater than test circuits 3 and 4 on test circuit 1 but at -70dB across most frequencies and peaks up around -20dB at 20 GHz. This low level of crosstalk means the additional losses from these adjacent test circuits was not a factor on the performance of a specific test circuit.

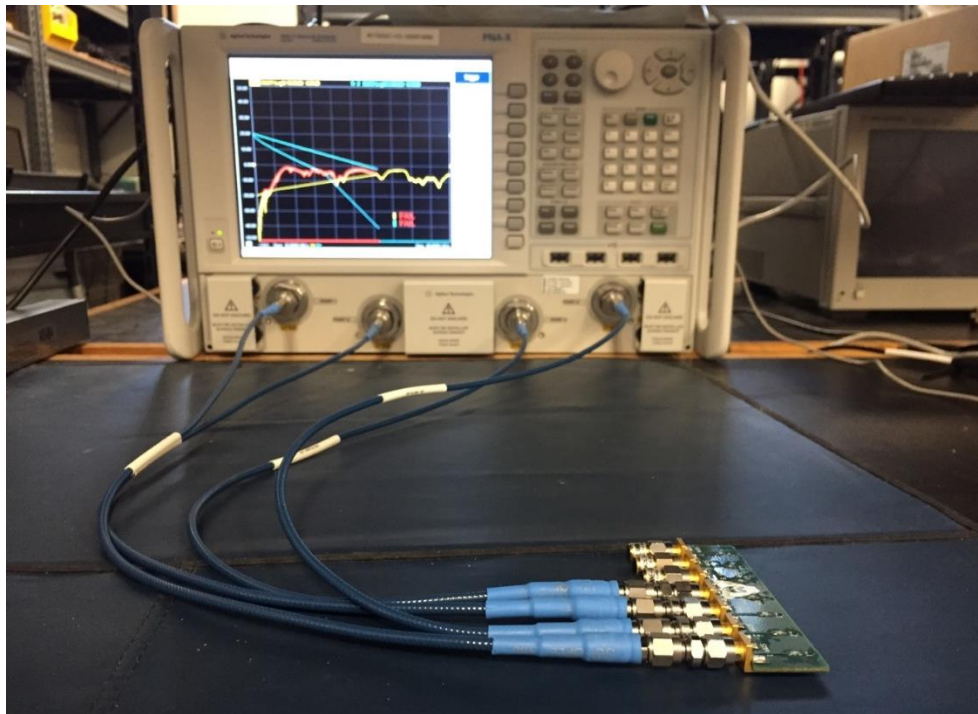


Figure 3.1 - VNA Setup For Frequency Domain Measurements On Test Circuit In Lab

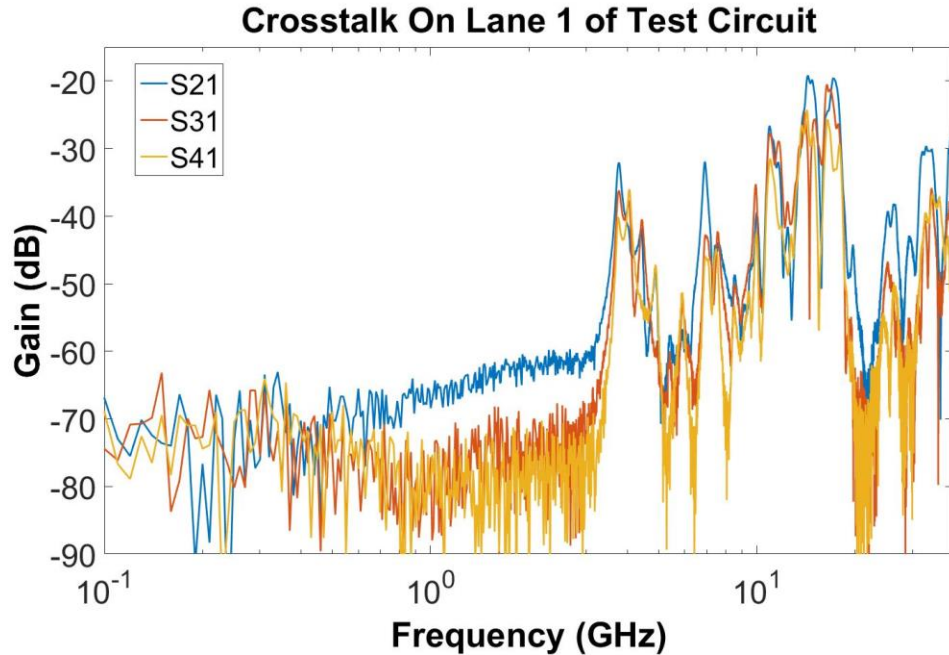


Figure 3.2 – The Effects of Crosstalk On Test Circuit 1 From the Closest Adjacent Test Circuits (2 Through 4)

The difference between the mean and the 95% confidence interval was at maximum 3dB. This was achieved through typical measurement best practices such as calibration, proper torquing and termination technique. The small measurement variation can be seen in Figure 3.3. The test circuit data was found to not meet the IEEE limit imposed on the circuit. The IEEE 802.3 limit for 100GbE Test Fixture Return Loss [1] was used as a definition of quality of a match, shown in black in Figure 3.3. This limit represents the estimated typical channel budget that will support an operational 100Gb Ethernet link. While not specifically a limit for a resistor, test fixtures terminate transceivers to perform conformance testing and untested lanes need to be terminated. The return loss limit is the requirement for the device under test on the near end. The IEEE 802.3 10 Gbps Backplane Return Loss channel definition limit [13] was used as a performance expectation for the FR4 portion

of the test circuit. There are no limits in the time domain that could be referenced in a similar manner. The largest deviation in test circuit return loss was 6dB. The very small deviation in the data indicates the measurements were reasonable and repeatable when analyzing the test circuit. The high return loss at 8 GHz is attributed to the effects of FR4, shown later in Figure 3.10.

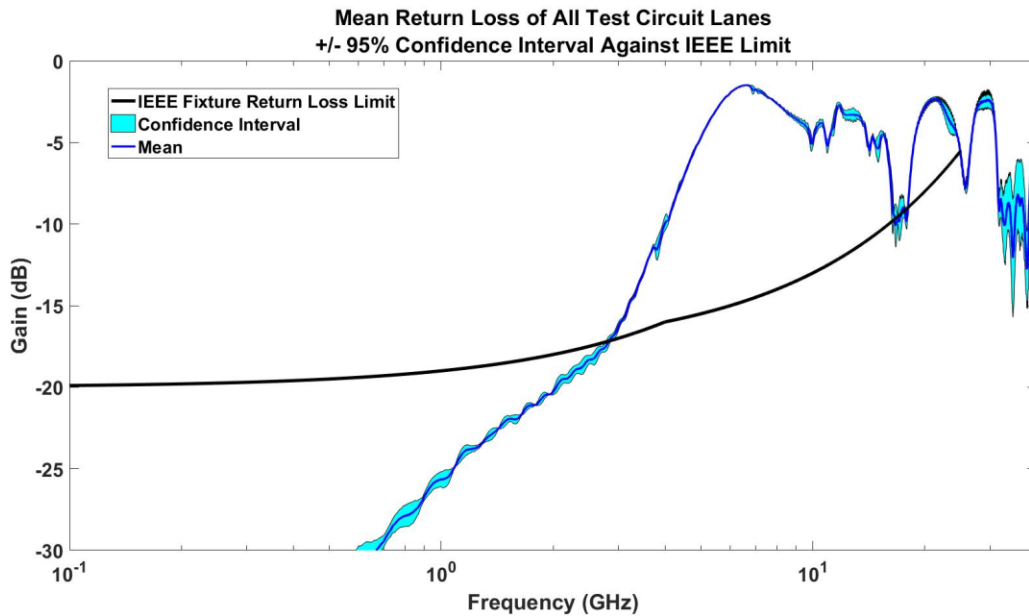


Figure 3.3 - Mean Return Loss of All Test Circuit Lanes on Test Board With Confidence Interval Against IEEE Limit

A 30 GHz Tektronix DSA8300 with a 80E08 TDR Module Option was used to collect impedance data as a function of time. A picture of the test setup can be found in Figure 3.4. The TDR response of a broadband 50 Ohm load can be seen in Annex D showing the ideal response of a TDR measurement on a termination. This removed any uncertainty that the data was showing incorrect data due to measurement setup issues. The TDR sampling module was removed from the measurement by calibration, revealing just the initial step response and the propagation down the test circuit to the termination.

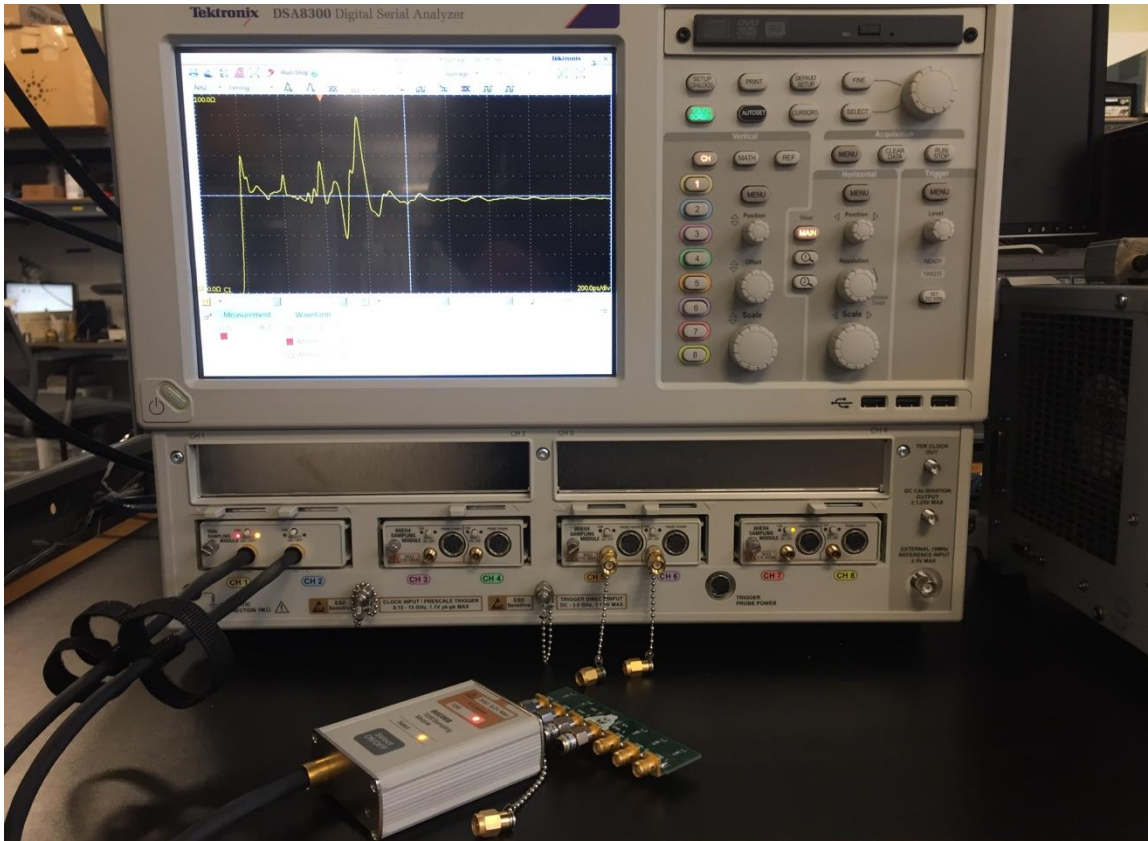


Figure 3.4 - TDR Setup For Time Domain Measurements On Test Circuit In Lab

Data obtained from the TDR was consistent. The maximum impedance in the test circuit was 90 Ohms and the largest deviation between lanes was 5 Ohms. The 95% confidence interval was within an Ohm of the mean. The high return loss at frequencies above 8 GHz on the VNA appears in the time domain in the form of ringing spikes on the TDR measurement. The high impedance and high return loss show correlation in performance on both the VNA and TDR. The TDR data in Figure 3.5 shows that there is a poor match at some point in the test circuit, but not necessarily the whole circuit is poorly matched. The VNA data details the performance at all frequencies, and at lower frequencies the match is good, which tracks with the initial DC measurements made with a multi-meter being within 2 Ohms of the nominal 50 Ohms.

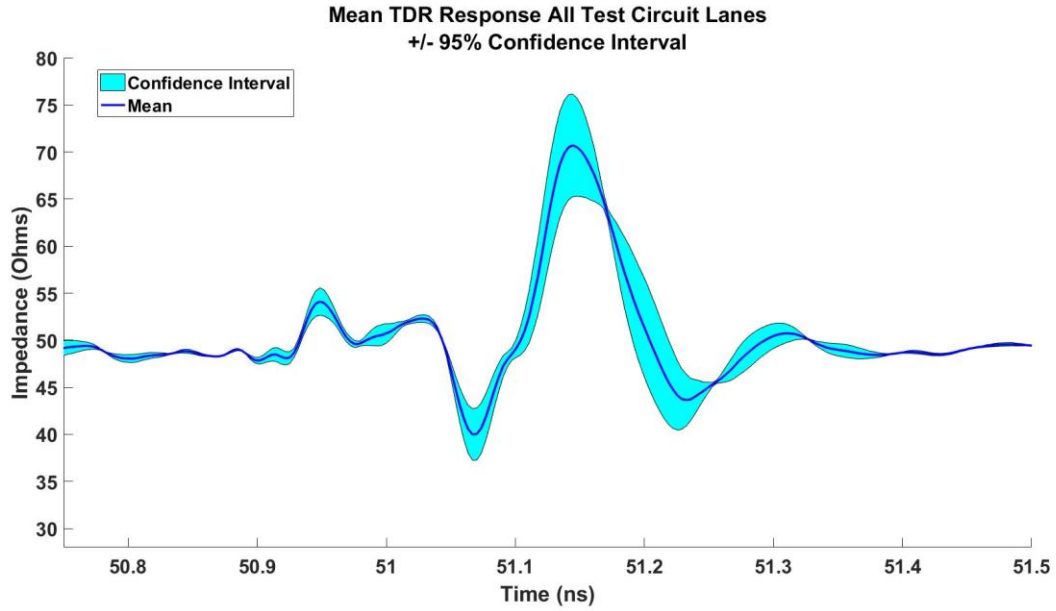


Figure 3.5 - Mean Impedance of All Test Circuit Lanes on Test Board With Confidence Interval

To explain the differences between the multimeter impedance measurement and the TDR impedance measurement, the bandwidth was limited by increasing the rise time of the TDR impulse. Rise time and bandwidth are inversely related as seen in Equation 1.1 [9]:

$$\text{Bandwidth (GHz)} = \frac{0.35}{\text{Risetime (ns)}} \quad \text{Eq. 1.1}$$

The term bandwidth is used for the highest sine-wave frequency needed to be included to adequately approximate the important features of the time-domain. The higher the bandwidth, the shorter the rise time and the more closely the waveform approximates an ideal square wave. Eq.1 is a rule of thumb to get the highest frequency component that is just barely above 70% of the same harmonic of an equivalent ideal square wave [9]. Slowing down the rise time of the TDR pulse effectively reduces the bandwidth that is being tested within the measurement, making it possible

to analyze the performance of the test circuit operating at a specific set of bandwidths. The measured maximum impedance of the test circuit increases from almost exactly 50 Ohms at a rise time of 2 ns to 64 Ohms as the rise time sped up to 20ps, equivalent to a bandwidth difference of 175 MHz to 17.5 GHz. This can be seen in Figure 3.6.

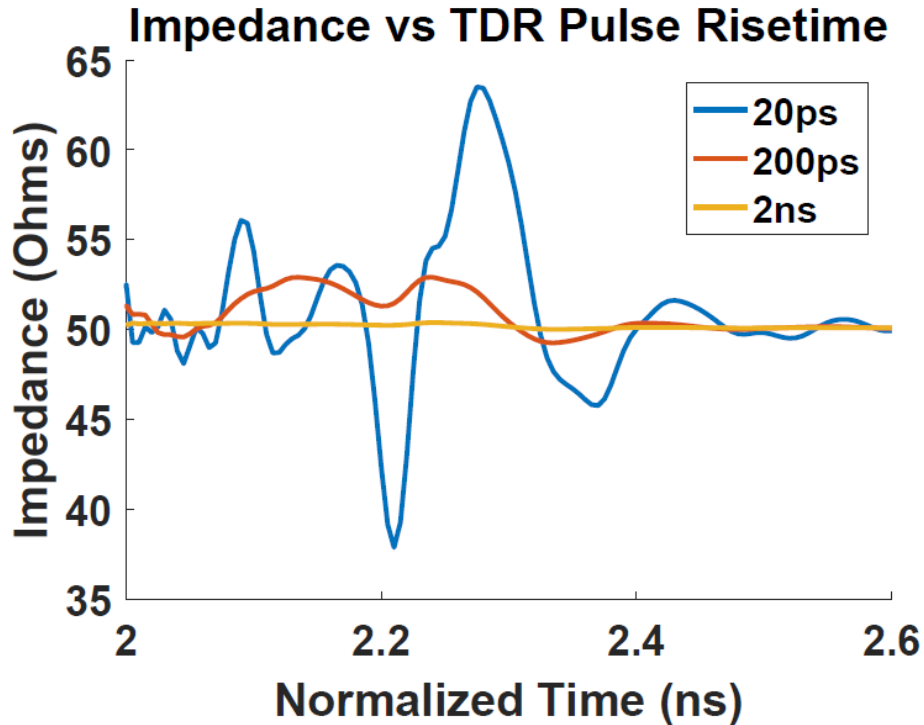


Figure 3.6 - The Effect Of Bandwidth On Test Circuit Impedance

The Fourier Transform was used to convert the time domain data discussed above into the frequency domain and the Inverse Fourier Transform was used to convert the frequency domain data into the time domain. To convert the data between domains, Keysight's Physical Layer Test System (PLTS) 2013 Build 20130118.1 implementation of the Fourier Transform function was used [14]. In this process, return-loss data from the VNA was transformed into the time domain,

and plotted against the TDR capture. The differences in magnitudes can be explained by the fact that the bandwidths of the equipment used were not the same. The discontinuities caused by the elements of the circuit occurred at the same times on both data sets. The window used to make the captures is also most likely different between equipment manufacturers, providing some deviation in similarities. These results show that the same answer can be arrived at whether a time-domain or frequency-domain analysis was used. With the reassurance that the collected data was valid, the next step was fully exploring the broadband matched circuit with the resistive termination.

At this point in the research, it was clear there was a poor match, but from what component in the matched circuit was unknown. The easiest way known to isolate the problem was determined to be using the TDR to make measurements through an open analysis. The largest mismatch seen on the TDR measurements was at 46 ns. TDR measurements were performed progressively, adding a component of the test circuit to the measurement. The first measurement was an open TDR measurement to get a sense of where in time the measurement starts. Then, a measurement was made only on an SMA connector, followed by an unterminated test circuit consisting of the SMA connector populated on the unterminated test circuit. Finally, a measurement was made on the complete test circuit. The measurement setup and result can be found in Figure 3.7:

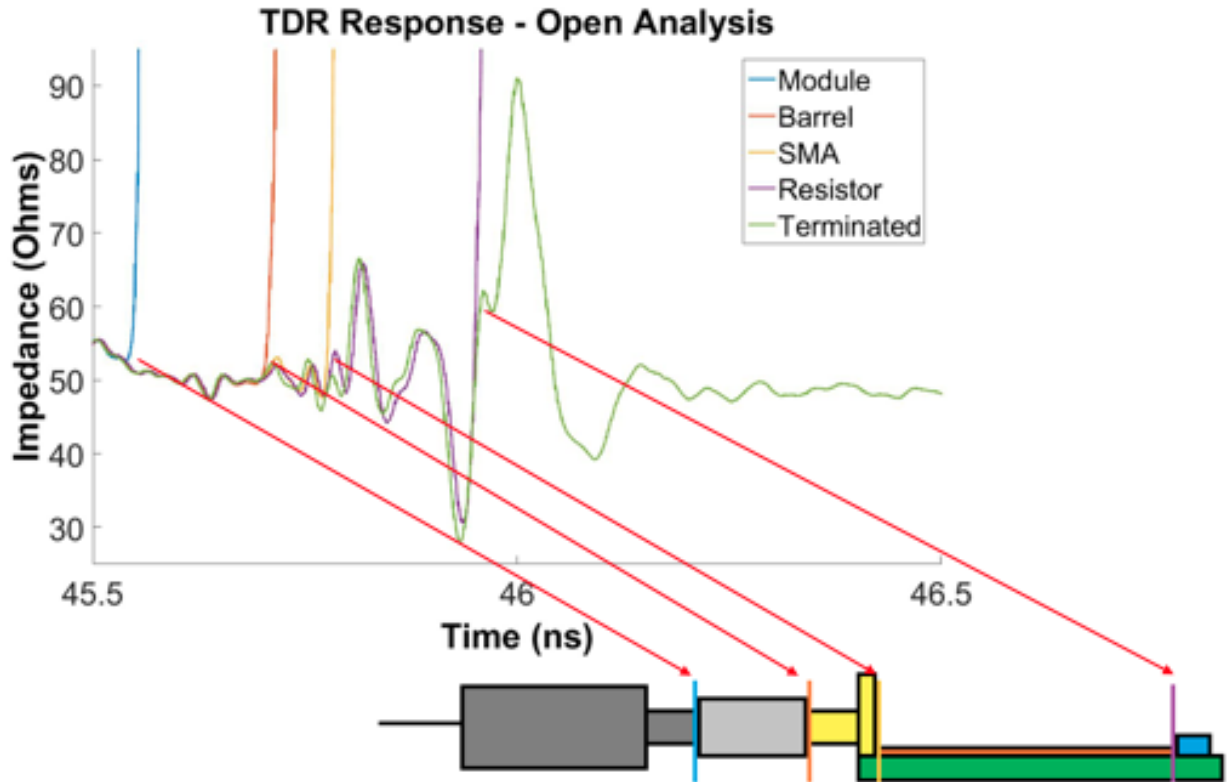


Figure 3.7 - Open Analysis on TDR Measurement Setup To Isolate Circuit Elements

The open analysis showed the point in time at which the microstrip meets the resistor was where the large impedance spike occurred. It is typical for impedance spikes at junctions where mediums are changing at frequencies in the range under test. The time at which the resistor ends was found using the provided dimensions of the resistor. The start and stop time of the resistor in the test circuit are represented with black bars in Figure 3.8. The dips that occur right after the initial time and right before the end time represent the end leads of the resistor. The effect of the losses from each element were explicitly identified using post-measurement time gating [15] which revealed the broadband performance characteristics of the three components in the test circuit. Each element of the test circuit was time gated with the timing windows acquired with this open analysis,

beginning with the SMA connector and systematically working to the termination. The time gating process is further detailed in [16] and Appendix C.

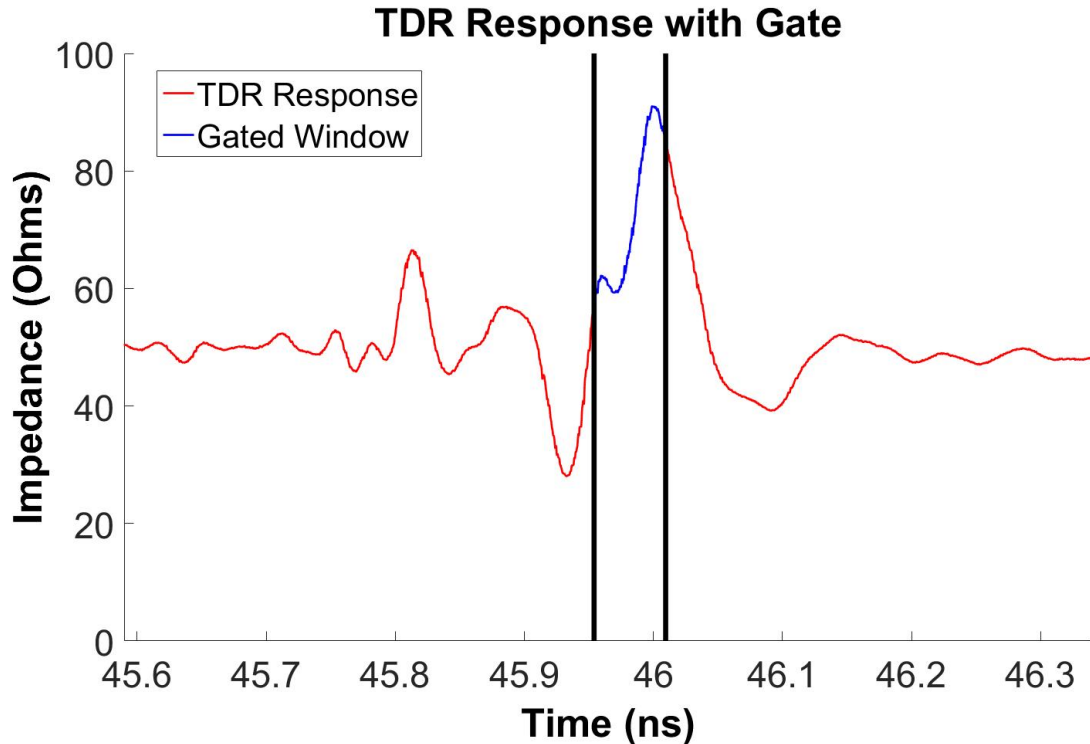


Figure 3.8 - TDR Response With Gate/Window Around Resistive Termination In Test Circuit

Beginning with the SMA Connector, the VNA data was imported into PLTS and the Fourier Transform was used to convert to the time domain. The start and stop times acquired from the open analysis were marked, and the Inverse Fourier Transform was performed on the data between the markers. Using the manufacturer's electrical data specification for the connector as a reference [5], the SMA frequency response was found to be as advertised. The connector had -30 dB of return loss from DC to 18 GHz, and had a maximum return loss of -20dB at 40 GHz. This easily meets the IEEE reference limit, and also clearly was not the test circuit component causing the high frequency mismatch as seen in Figure 3.9.

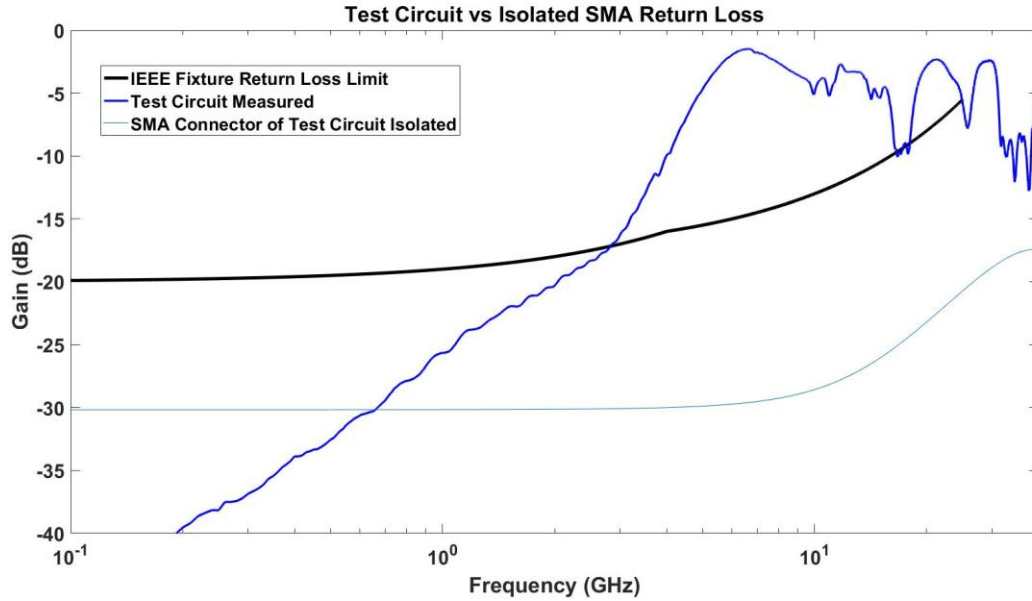


Figure 3.9 - Isolated SMA Return Loss versus Test Circuit Return Loss Performance Against IEEE Cable Assembly Limit

Using time gated return loss data and open TDR measurements to view the isolated microstrip component, the FR4 could be viewed as the worst performing component in the test circuit. The large spike in the test circuit return loss is also seen in the isolated microstrip return loss measurement. The short test circuit length likely amplified any reflections caused from the SMA junction and resistor pad or losses associated with FR4. To compare the measured data against a realistic expectation, the IEEE 10Gbps over backplane 10GBASE-KR channel specification [13] was used for a definition of a quality match over FR4. The limit imposed on the FR4 microstrip ensures with high confidence that a link can be established if the return loss stays within the allowed region. The isolated data collected meets this limit up to 10 GHz at which the return loss peaks above -5dB. With the entire test circuit overlaid with the isolated data, it is clear that the high frequency loss is attributed to the FR4 seen in Figure 3.10. The modal nulls seen in the test circuit data also appear here, showing the dominance of FR4 relative to the broadband circuit match at higher frequencies.

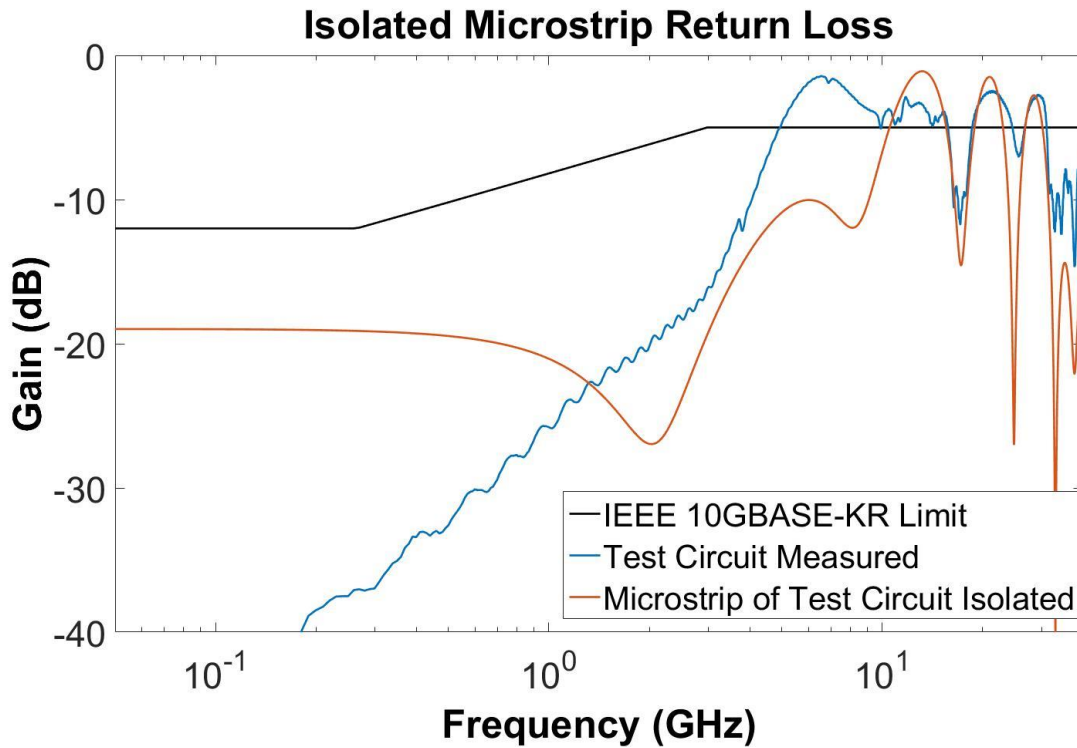


Figure 3.10 - Isolated FR4 Return Loss Versus Test Circuit Return Loss Against IEEE Backplane Limit

The Fourier Transform of the termination only, denoted by the blue impedance versus time plot in Figure 3.8, can be seen in blue in the resultant return loss plot in Figure 3.11 versus the return loss of the entire test circuit seen in red.

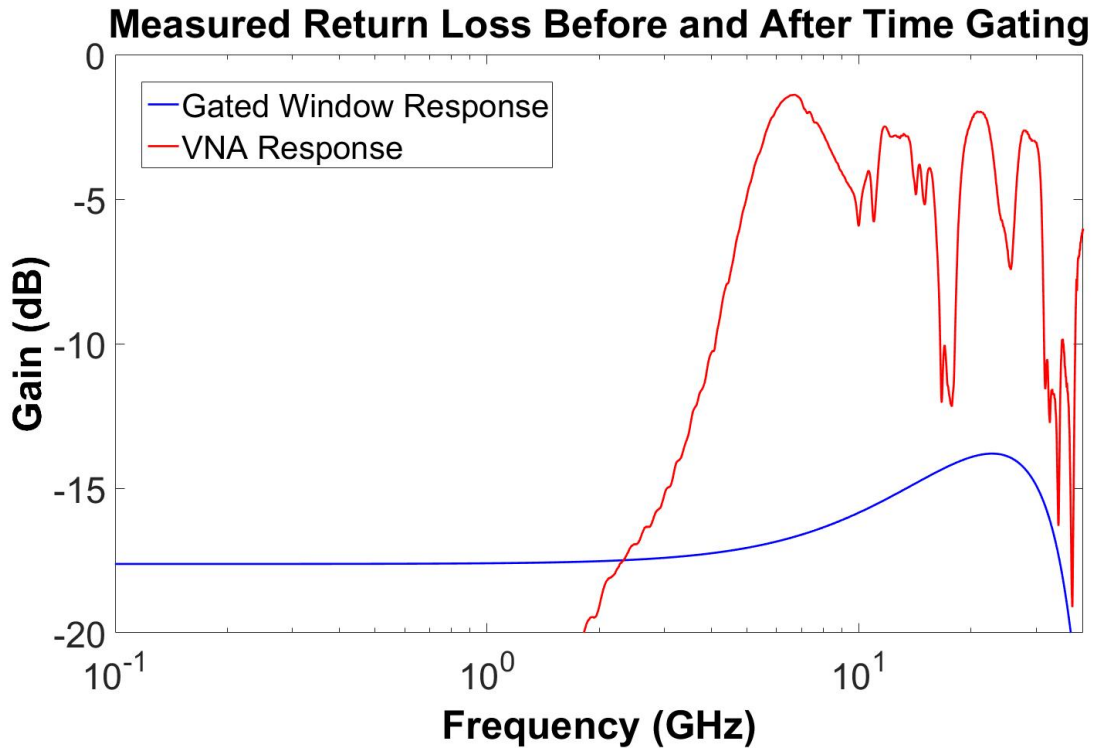


Figure 3.11 - Test Circuit vs. Isolated Microstrip Return Loss From Open Analysis

The isolated resistor has a relatively flat frequency response broadband, without the high frequency return loss seen in the test circuit measurement or the FR4 time gated data. After performing time gating at the point in time of the resistor across all lanes on the test board, all but three of the resistors met the IEEE test fixture specification across the full frequency range. Out of the three failing resistors, the worst failure point was 0.5dB out of specification at 10 MHz. This was likely due to the gating window, and not the actual performance of the termination. The gating process is heavily dominated by the start and stop times of the selected window due to the impedance discontinuities observed over the course of the entire channel. The TDR allowed for precise resolution in the time domain to choose an accurate start and stop time for the different elements in the circuit.

Using the collected start and stop time for the termination, the mean and the confidence interval of all collected data passes the specification as seen in Figure 3.12:

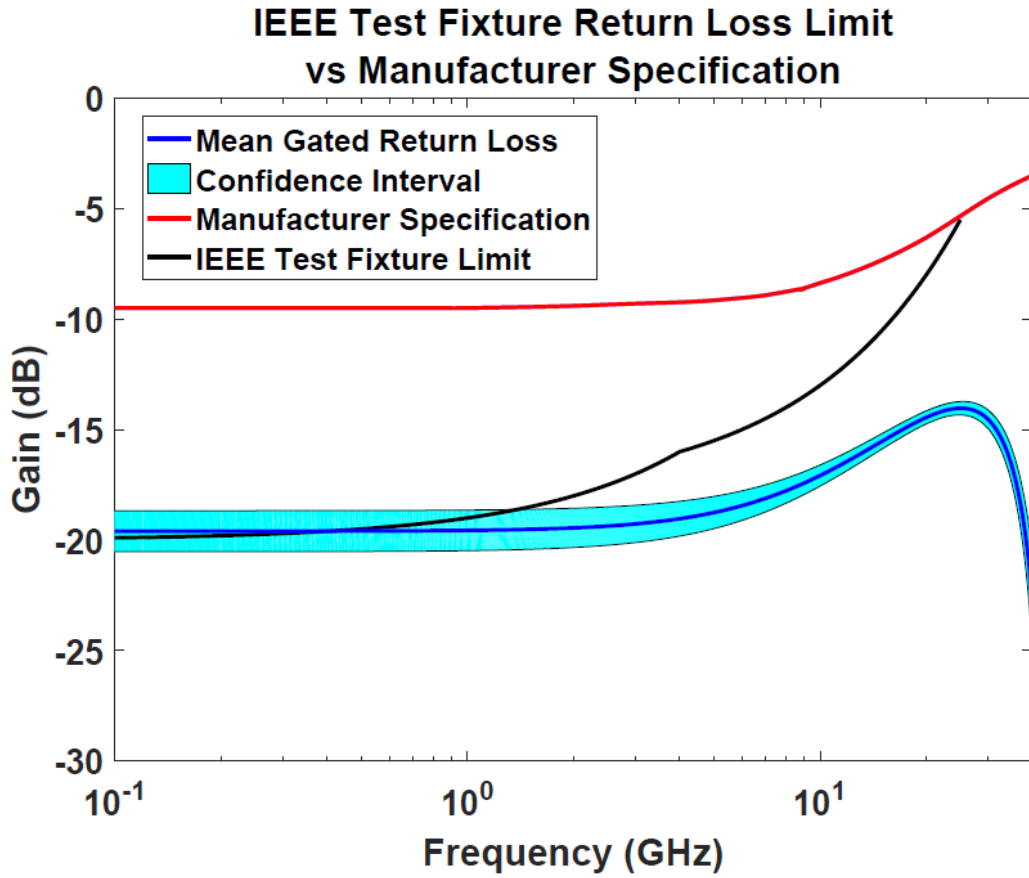


Figure 3.12 - Mean Return Loss of Isolated Termination From All Test Circuit Lanes +/- 95% Confidence Interval

Each board consisted of multiple test circuits meant to be as similar to each other as possible to increase sample size. Across seven identical measurements over two identical boards, the mean and standard deviation difference was under 1 dB. The mean of the collected data was roughly 6dB less than the manufacturer specification broadband, suggesting the resistor performs better than advertised. The significant difference between the manufacturer specification and mean of the collected

data can be seen in Figure 3.12. In an effort to correctly predict this behavior, models based on the manufacturer dimensions and electrical characteristics were created and later adjusted to better represent the measured data.

CHAPTER 4

MODELS OF TEST CIRCUIT

Models using manufacturer supplied dimensions and electrical parameters were created to validate the measured data. The files used to fabricate the board were imported and used for the models. These models were also assessed in their suitability of estimating the broadband performance of typical circuit elements like FR4. Precise agreement was not possible due to the uncertainty of the supplied dimensions, however the measured and modeled data converged on the same conclusion that FR4 contributes most to the broadband mismatch.

The test circuit was modeled in the industry standard modeling software HFSS. The SMA connector model was an HFSS SMA model from the HFSS Library [4]. The microstrip and board were modeled to match the top layers from the files used to fabricate the board. The resistive termination modeling theories were based on the two sets of data made available from the manufacturer. One theory was using HFSS to model the termination using the manufacturer supplied mechanical dimensions and materials. The other method was a lumped parameter model using the manufacturer supplied electrical properties and behavior of the resistor. Both models could be used as terminations in the test circuit, giving the ability to compare performance to the measured test circuit data as seen in Figure 4.1. An excitation was simulated using a wave port at the SMA connector input. The excitation propagated through the connector, the microstrip and into the termination. A single lane of the test circuit was modeled to minimize computation time.

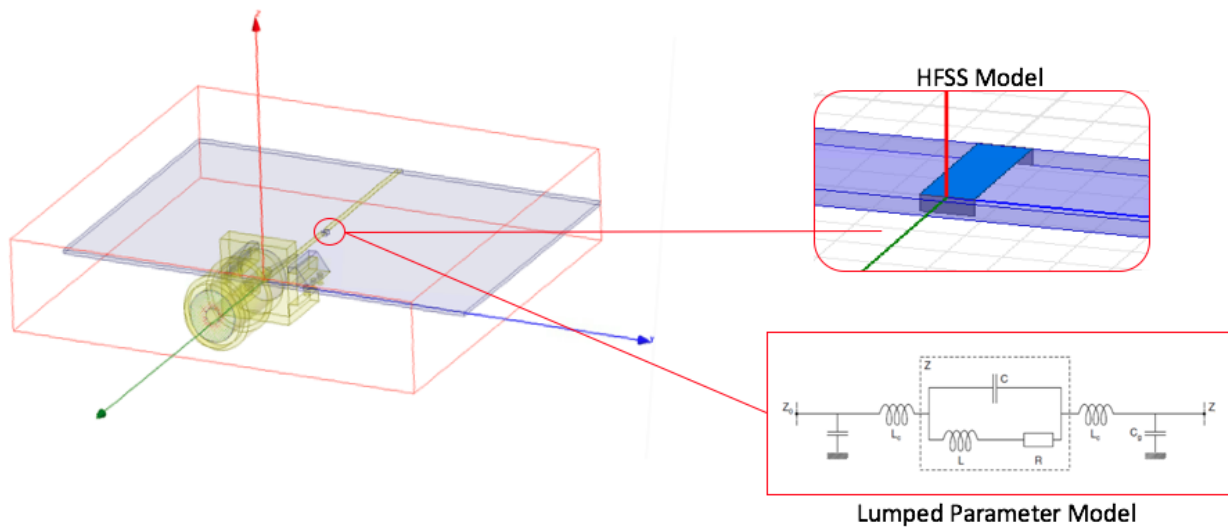


Figure 4.1 - Test Circuit HFSS Model with Both Termination Models

Other studies have shown their models of transmission lines for high speed design systems out to 30 GHz to be within 5% of the manufactured boards [17]. The supplied dimensions ranged in length from 1.51mm to 1.53mm, width from 0.74mm to 0.76mm and height from 0.373mm to 0.627mm specified by the manufacturer's datasheet [5]. These ranges did not allow for the kind of accuracy shown in [17]. In this study, all dimensions provided were approximations, so an exact match comparing the modeled and measured data was not expected. The models showed an approximation of the measurements, the deviation can be attributed to a difference between HFSS's default FR4 parameters and the actual parameters of the FR4 used, such as loss tangent and skin effect. The return loss of the modeled test circuit using both termination modeling methods can be seen in Figure 4.2, also showing the relative measured return loss of the test circuit and the IEEE limit.

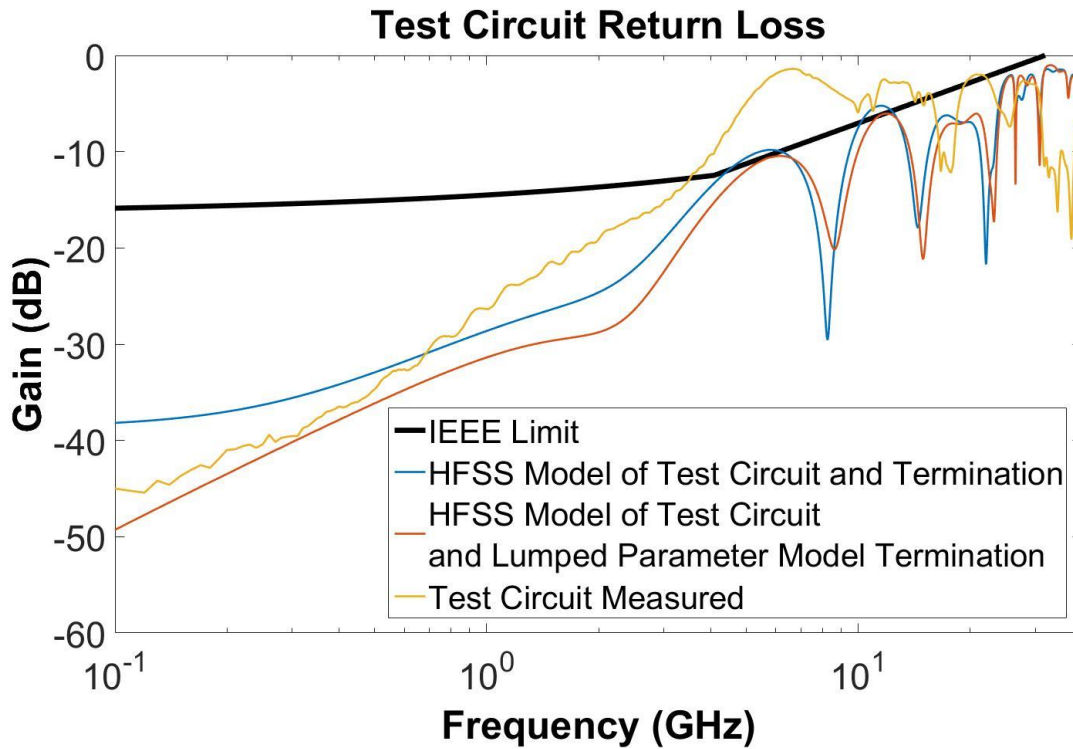


Figure 4.2 - Return Loss of Modeled Test Circuits vs. IEEE Limit

The lumped parameter model was created following the manufacturer’s typical high frequency performance electrical model as seen in Figure 4.3. It was their basis for their given return loss and insertion loss data. When calculating the equivalent resistance of the network at 40 GHz, the 50 Ohm resistor has a calculated impedance of 75 Ohms. The Fourier Transform of the 40GHz VNA data showed an impedance of 75 Ohms at the resistor in the time domain. The impedance of the resistor increased with frequency in the model analysis as well, right around 75 Ohms.

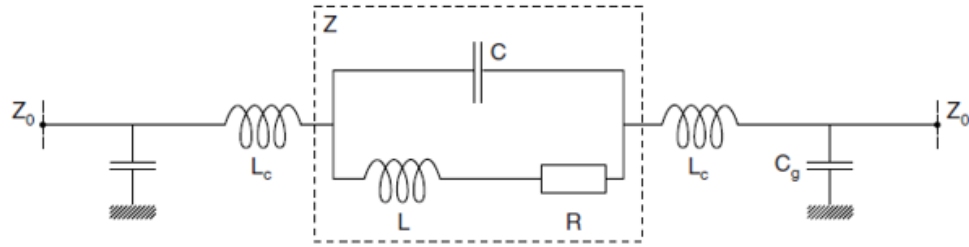


Figure 4.3 - Lumped Parameter Model of Termination

Table 4.1 - Lumped Parameter Model Values from Manufacturer

Internal shunt capacitance	C (pF)	0.05
Internal inductance	L (nH)	0.15
External connection inductance	L _c (nH)	0.3
External capacitance to ground	C _g (pF)	0.05
Resistance	R (Ω)	50
Internal Impedance (R, L, C)	Z (Ω)	50

The HFSS model of the termination was created with the supplied construction dimensions and materials as seen in Figure 4.4. The approximations were in micrometers as typical values. The calculated resistance of the resistor using the relationship of resistivity, cross sectional area and length was 80 Ohms. This impedance mismatch due to construction would also explain the high return loss at frequencies above 20 GHz. The HFSS model also agrees fairly close to the lumped parameter model given the constraints of the approximate dimensions, as seen in Figure 4.5. There was a noticeable dip in return loss beginning at 20 GHz in the HFSS model but not in the lumped parameter model. This looked to be structure related as it was also present in the measurements but not in the electrical equivalent model.

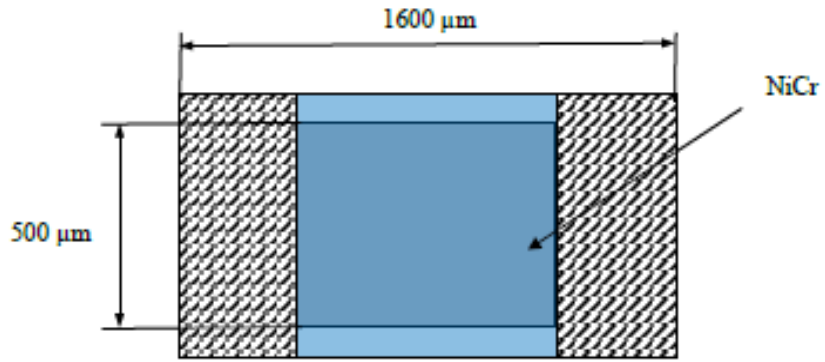


Figure 4.4 – Top Down View of Resistive Termination Dimensions Used In HFSS Model

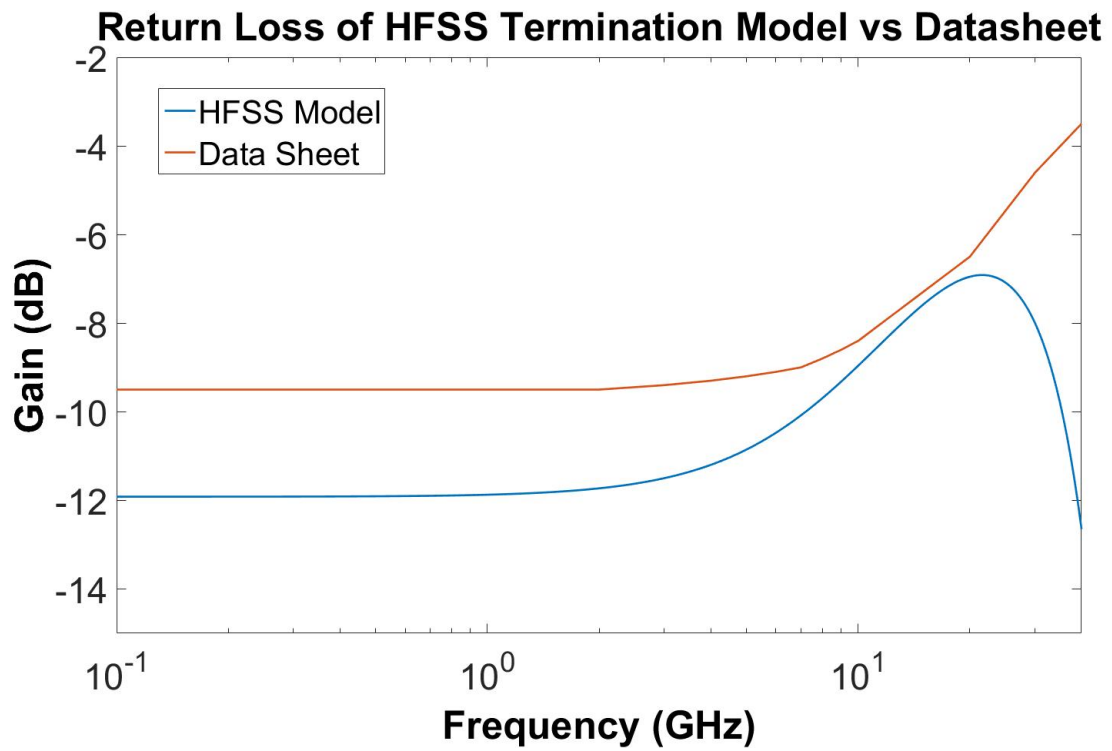


Figure 4.5 - Return Loss of HFSS Termination Model vs. Lumped Parameter Model (Datasheet)

After modeling to the manufacturer's specifications, slight changes to each model were made to improve the match to the measured broadband performance of the termination. The resistor dimensions were modified to still fit the correct pad size, so height was the only dimension adjusted. By increasing the height from 0.10um to 0.115um, the return loss below 8GHz matches the measured return loss within 1 dB. The width and length were not changed because pad size is static and needs to be consistent. While making the lumped parameter model calculations, it was noticed that inductance likely from the leads of the termination was the dominating factor for the impedance of the lumped parameter model, aside from changing the nominal resistance outright. Decreasing the inductance from 150pH to 70pH improves the return loss match to the measured data to within 2 dB broadband. These slight modifications seem more than reasonable, compared to the possibility of dimension range given. The modifications result in models which match the measurements and perform better than advertised from the manufacturer. This can be seen in Figure 4.6.

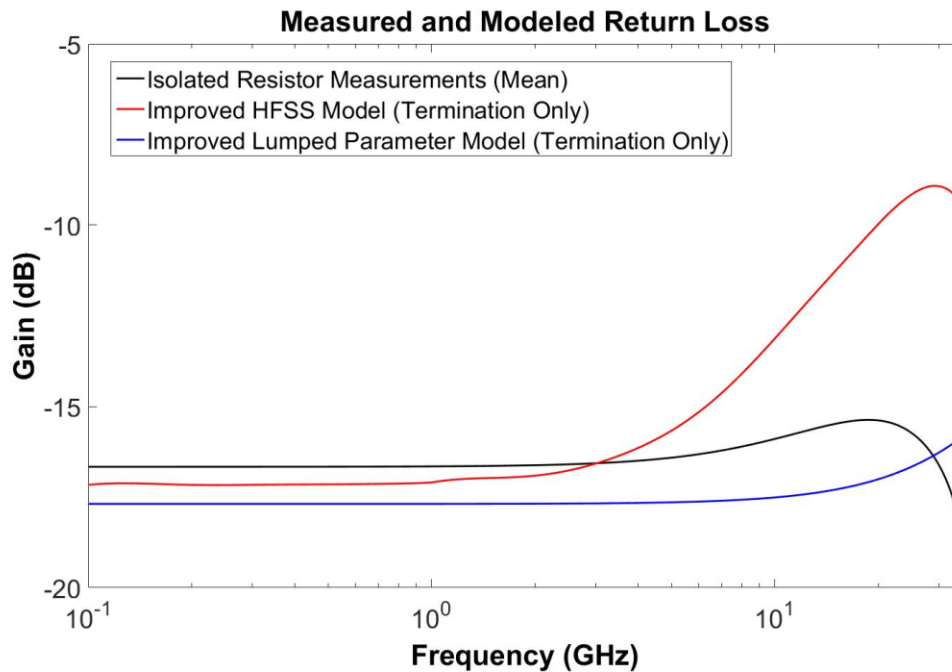


Figure 4.6 - Measured vs Modeled Return Loss of Isolated Termination

The models were shown to match the measured data within reason. Dimension approximation prevented an ideal perfect match. With slight adjustments to the manufacturer supplied dimensions, measured and modeled return loss were within 1 dB of each other at most frequencies. The correlation between measured and modeled results was present in both the complete test circuit results and the isolated termination results.

CHAPTER 8

CONCLUSION

In this case of a simple test circuit, the microstrip on FR4 contributed most to the mismatch when compared to the other circuit components in the time and frequency domains. Microstrip on FR4 may not be suitable for serial applications operating above 10Gbps. The SMA connectors were measured to behave according to manufacturer expectations and not a major contributor to the mismatch observed. The termination does contribute to mismatch at higher frequencies, particularly when populating a circuit on FR4. A more accurate model of the termination was solved.

Electromagnetic modeling software such as HFSS underestimates mismatch when using the standard library properties of FR4 in simulations at frequencies up to 40 GHz. A perfectly accurate model in this case was not possible due to the approximate nature of the dimensions of the solid that was to be modeled. In this study, the mean difference between the HFSS test circuit and termination model and lab measurements across all frequencies was 5.6dB. In this study, the mean differences between the HFSS test circuit model with the lumped parameter termination and lab measurements across all frequencies was 6.0 dB. Both the lumped parameter and the HFSS model were close to meeting the IEEE conformance limit. Due to the vague construction dimensions of the resistor, parameters could be changed within both the HFSS model and the lumped parameter model to achieve a better match to the measured isolated data.

Time gating was performed on the Fourier Transform of the measured VNA data using the start and stop times found on the TDR. This measurement method allowed for the isolation and analysis

of specific elements in the test circuit. The time gated impedance measurements were then transformed back into the frequency domain, showing only the performance of the resistor. Most terminations passed the IEEE specification, proving they would be a suitable termination for QSFP-DD test fixtures. The mean difference between the frequency domain measurements was under 2.0dB. The mean difference between the time domain measurements was 2.16 Ω .

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APPENDIX A -TEST CIRCUIT BOARD LAYOUT

The overall design of the board was based on typical design practices [9]. This can be seen in Figure Appendix A.1. Figures Appendix A.2 and Appendix A.3 show the specific designs of each layer of the board. Figure Appendix A.4 shows the top down view of all lanes together. Layer 1 as seen in Figure Appendix A.2 has pads for the SMA and termination as well as the microstrip and a via for each test circuit. Layers 2 and 3 can be seen in Figure Appendix A.3, which have connections from the SMA and ground vias to complete the return loop for the circuit. Layer 4 is empty except for the via, because there was no need to add extra circuitry due to the simplicity of the test circuit design. Figure Appendix A.4 shows the board populated with SMA connectors, before populating the terminations.

	Thickness (inches)	Tolerance (+/-)	
Layer 1	0.0017	0.0004	0.5 oz foil plated to approximate*
Bonding ply (1 x 7628, 2 x 1080)	0.0119	0.0010	Dielectric Constant 4.5 (+/- 0.10)
Layer 2	0.0014	0.0004	1 oz. foil
Laminate Core	0.0280	0.0025	Dielectric Constant 4.5 (+/- 0.10)
Layer 3	0.0014	0.0004	1 oz. foil
Bonding ply (1 x 7628, 2 x 1080)	0.0119	0.0010	Dielectric Constant 4.5 (+/- 0.10)
Layer 4	0.0017	0.0004	0.5 oz foil plated to approximate*
Overall:	0.0580	0.0061	

Figure Appendix A.1 - Layer Information for Test Circuit Board Fabrication

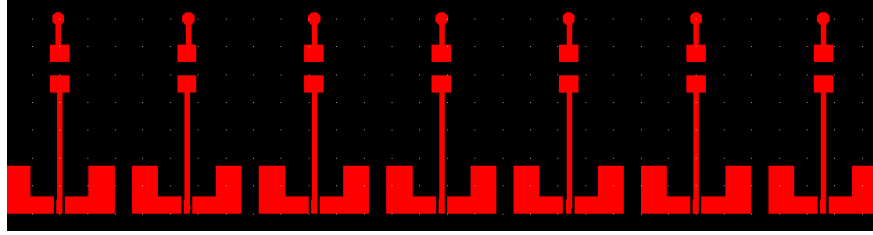


Figure Appendix A.2 - Layer 1 of Test Circuit Board

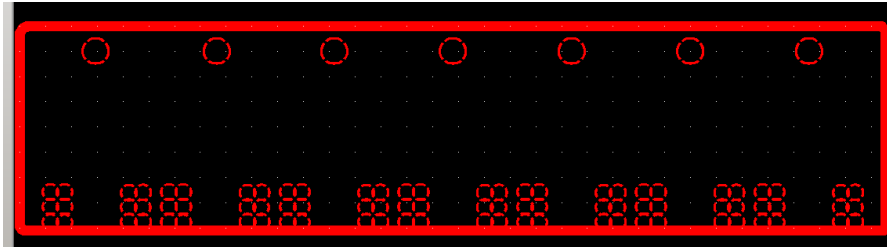


Figure Appendix A.3 - Layers 2 and 3 of Test Circuit Board, Detailing the Grounding of the Via off of the Termination and SMA Pad

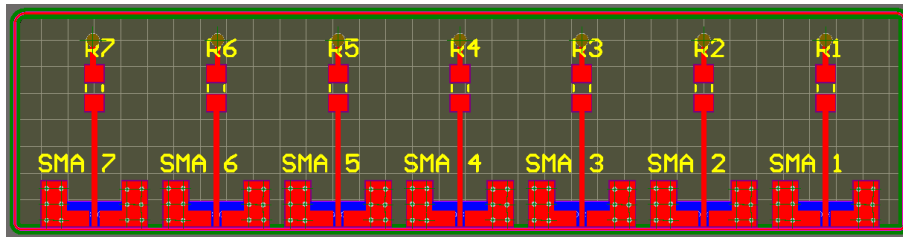


Figure Appendix A.4 - All Layers of Fabrication Board Stacked On Top of One Another

APPENDIX B - CALCULATIONS

Figure 4.3 shows the manufacturer specified typical high frequency performance electrical model, and Table 4.1 details the lumped parameter model values used to calculate the equivalent impedance of the model. At 40 GHz, the expected impedance of the 50 Ohm termination based off the electrical properties using Equation Appendix B.1 ends up being roughly 76 Ω . Figure 4.4 shows the manufacturer specified termination model dimensions, Figure Appendix B.1 shows further detail and Table Appendix B.1 details the material properties found in the model. Using the calculated cross sectional area of the resistor, length of the resistor, and the permittivity of the resistive material seen in Equation Appendix B.2, the expected impedance based off the termination physical properties ends up being roughly 76 Ω .

FR4 was used as the substrate for this research mainly due to the breadth of knowledge of the material in research, and the general cost of it versus another commonly used substrate, Rogers Material. The PCB manufacturer's specifications for the four layer board can be found in Fig. A.1 with the resultant microstrip line impedance found using Eq. Appendix B.3.

Once the layout was complete in the PCB designer software, the board was printed at a remote facility. While not the best substrate for high frequency operation, it is very common for PCB and the modeling software has a well-defined model of it making it a good candidate for proof of concept for this research. FR4 typically has a relative permittivity of 4.5 at lower frequencies.

$$Z = C_g \parallel \left(2L_C + \frac{R + j\omega(L - R^2C - L^2C\omega^2)}{1 + C((R^2C - 2L)\omega^2 + L^2C\omega^4)} \right) + C_g \parallel Z_L$$

Eq. Appendix B1.1

$$Z \approx 76 \Omega$$

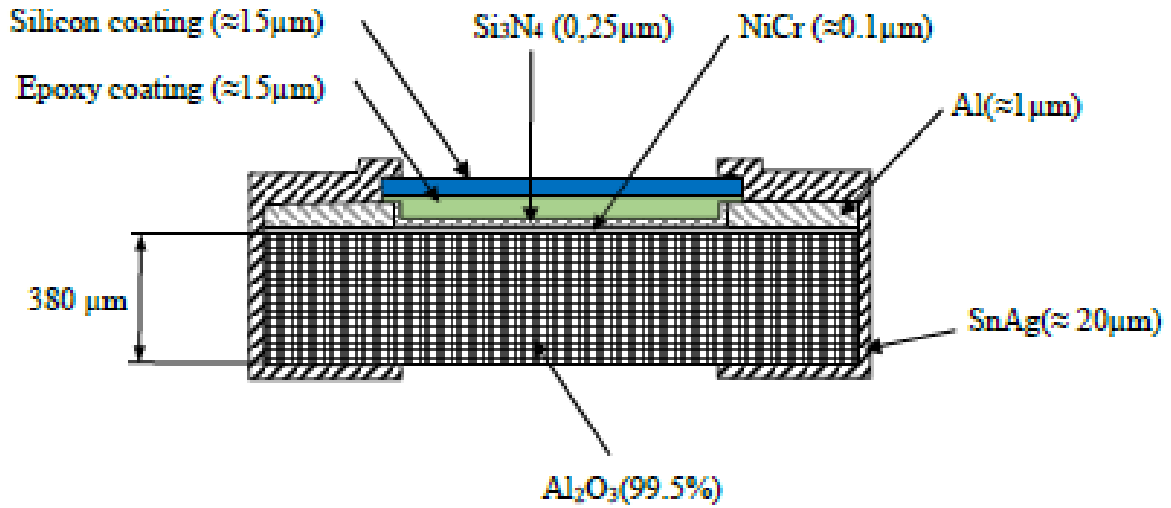


Figure Appendix B.1 - Manufacturer Supplied Resistor Dimensions

Table Appendix B.1 - Manufacturer Supplied Material Properties

Material	Resistivity
Al_2O_3	$>1\text{E}14$
NiCr	$25\text{E}-5$
Al	$2\text{E}-6$
Si_3N_4	$5.2\text{E}13$
Epoxy Coating	$1\text{E}13$
Silicon Coating	$1\text{E}13$
SnAg	$1\text{E}-5$

Table Appendix B.2 - Manufacturer Supplied Resistor Dimensions Used to Calculate Resistance

Permittivity of Resistor Material (ρ)	Length of Resistor (l)	Cross Sectional Area of Resistor (A)
25E-5 $\Omega \cdot \text{cm}$	1600 μm	500 $\mu\text{m} * 0.1 \mu\text{m}$

$$R = \rho * \frac{l}{A} \quad \text{Eq. Appendix B.2}$$

$$R = 80 \Omega$$

Expected Impedance Based Off Resistor Physical Properties

These microstrip properties resulted in the desired characteristic impedance of precisely 50 Ω :

Table Appendix B.3 - Microstrip Properties

Relative Permittivity (ϵ_r)	Trace Width (W)	Trace Thickness (T)	Substrate Height (H)
4.5	19.873 mils	1.7 mils	11.9 mils

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} * \ln\left(\frac{5.98 * H}{0.8 * W + T}\right) \Omega \quad \text{Eq. Appendix B.3}$$

$$Z_0 = \frac{87}{\sqrt{4.5 + 1.41}} * \ln\left(\frac{5.98 * 0.0119}{0.8 * 0.019873 + 0.0017}\right) \Omega$$

$$Z_0 = 49.999 \Omega \approx 50 \Omega$$

APPENDIX C - TIME GATING PROCESS

Time gating was introduced to isolate the resistor through an estimate of a transfer function applied to the measurement. A window is applied to a channel that either passes or stops a signal at a certain time. The window used will affect the magnitude and phase of the system in the frequency domain. Window size and shape is important to time gating because both properties will affect the trace spectrally. Two different shapes are rectangular and Hamming windows. Each window has different characteristics and affects the trace in different ways. The rectangular window was found to keep more of the energy of the transfer function, but also results in unnatural frequency weighting and adds much unwanted sideband noise. The Hamming window on the other hand results in less power saved from the transfer function, but gives more of a desirable Fourier Transform shape. In this instance, a Hamming window was used with a start point of right before the resistor as seen in the open analysis. The ending point is also easily calculated because we know the length of the resistor, and can calculate its electrical time via the relationship of the speed of light to wavelength to distance. Using this technique, we were able to achieve a pretty close approximation of the resistor alone. It is also possible to turn the bandpass filter into a notch filter, and see the effects of the rest of the system. The resistor behaves as expected and advertised, around -15dB flat of return loss. It has a little less loss than modeled, which could be more attributed to the frequency dependent loss of the FR4 material more than the actual resistor. However, you do see the same roll off as frequency increases in the time gated system like you do in the HFSS model.

The following graph shows a VNA capture with it's TDR transform using the Physical Layer Test System (PLTS) software. It allows for time gating in the time domain, and seeing in

real time the effects in the frequency domain. Marker 1 was set using the open analysis, and Marker 2 is 1600um further down the test circuit (the electrical length of the termination).

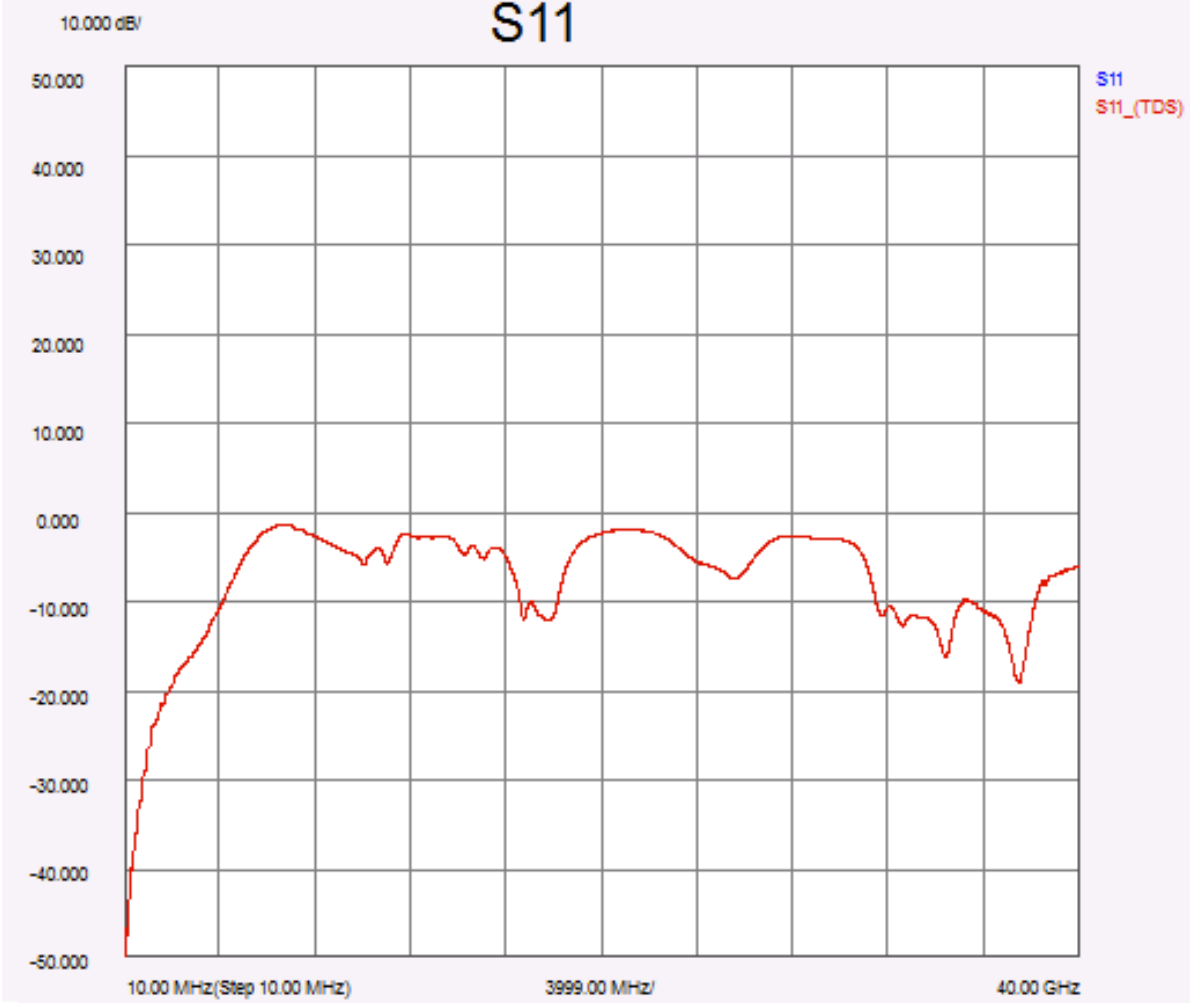


Figure Appendix C.1 - VNA Measurement of Test Circuit Return Loss (from PLTS)

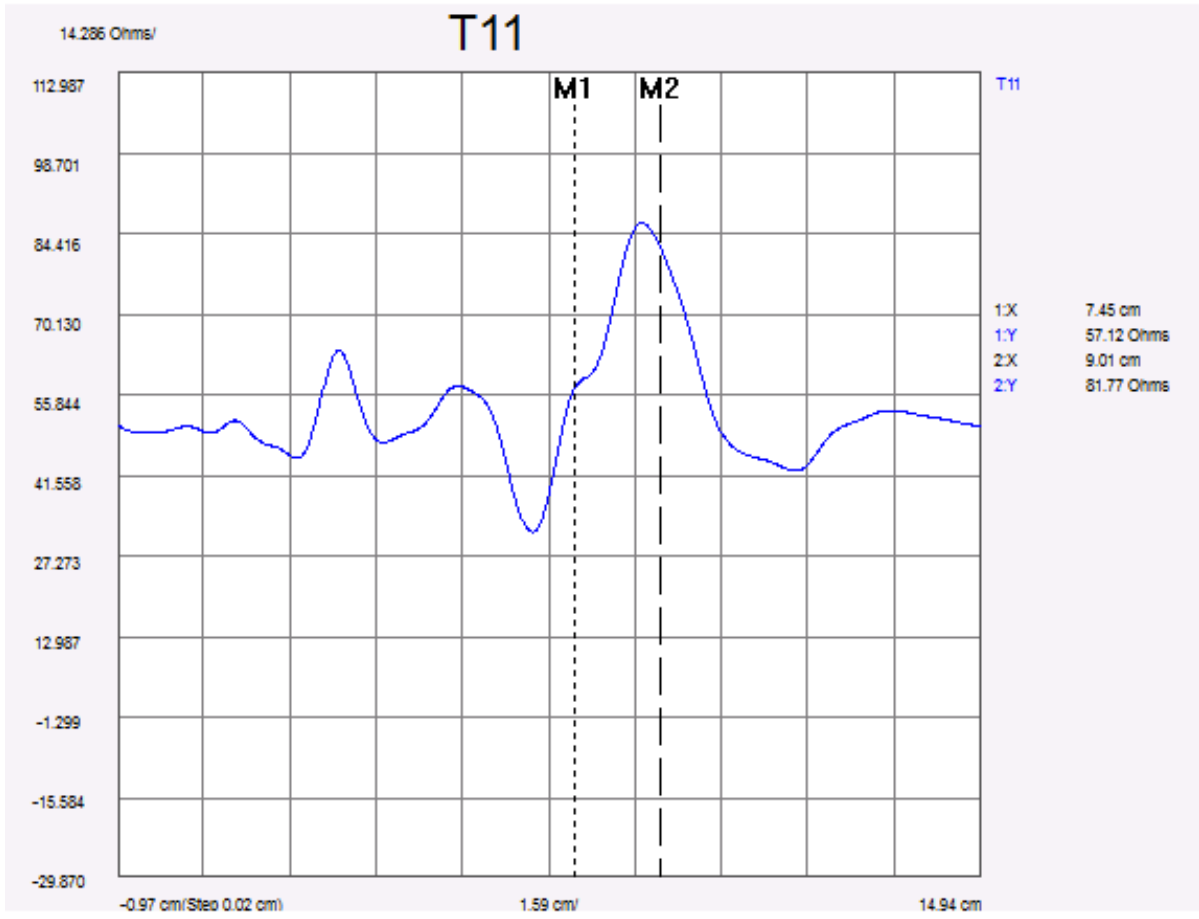


Figure Appendix C.2 – VNA Measurement Transformed into Time Domain (from PLTS)

When applying the filter to isolate the resistor, there is a significantly flatter response than before:

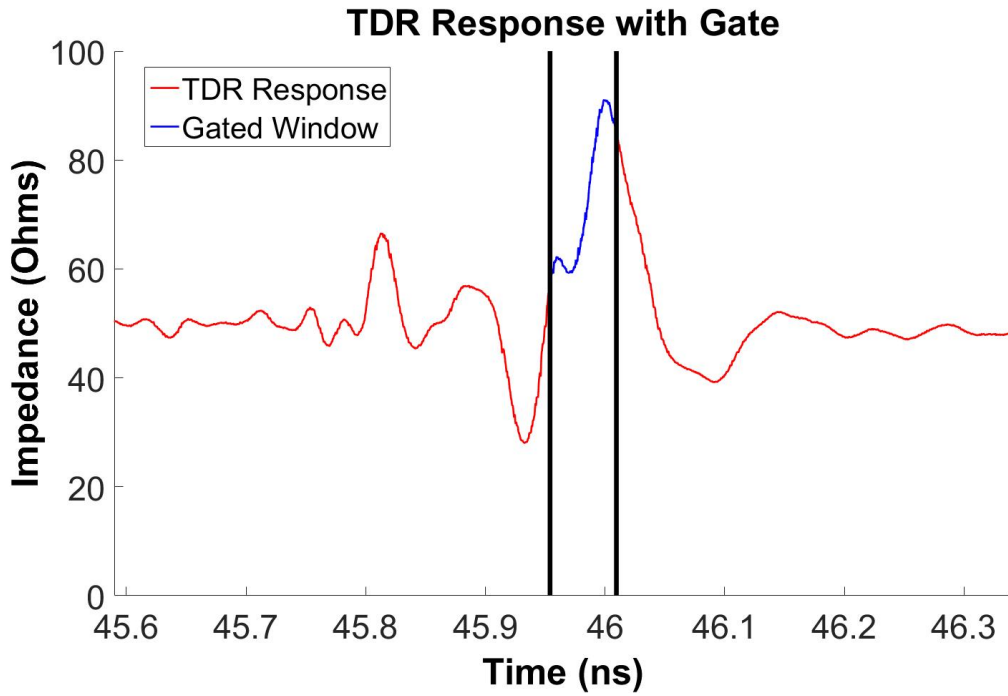


Figure Appendix C.3 - Window in Time Analyzed as Time Gated Data ("Isolated Termination")

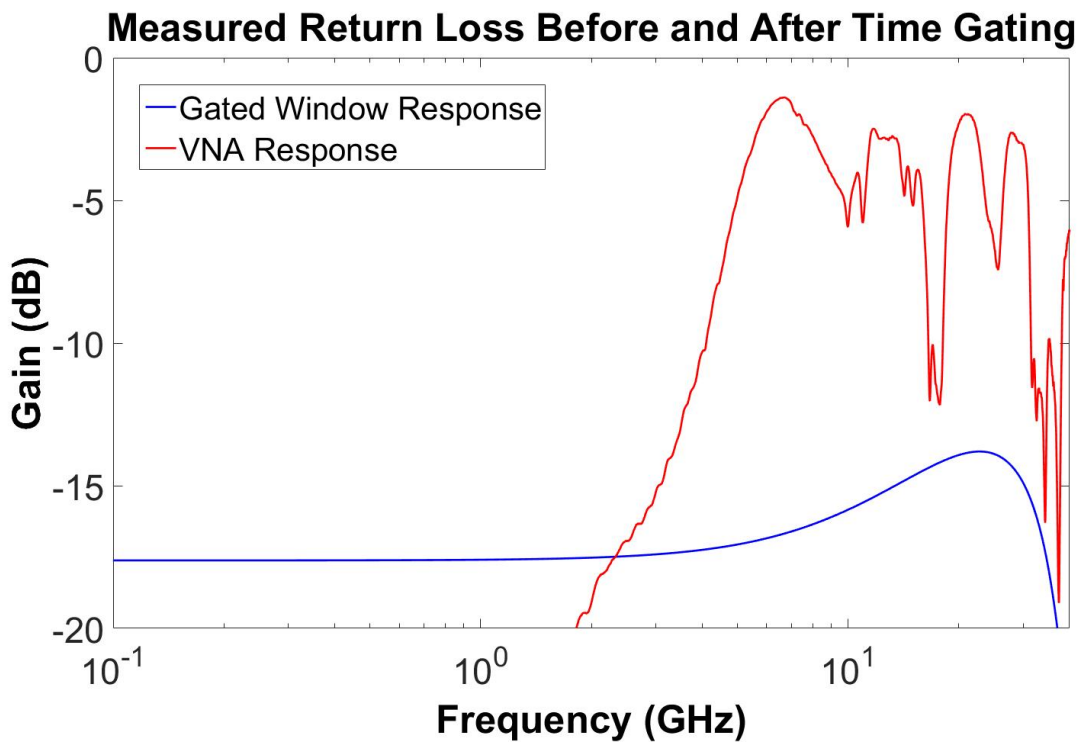


Figure Appendix C.4 - Results of Time Gating Shown In The Frequency Domain

APPENDIX D - MEASUREMENTS

To connect the test circuit to the VNA, high bandwidth Hubert and Suhner cables were used for all four ports. To connect the test circuit to the TDR, a barrel was needed to couple the connectors together. To check for any harmonic ringing, a thru measurement was performed from port to port of the VNA cables seen in Figure Appendix D.1.

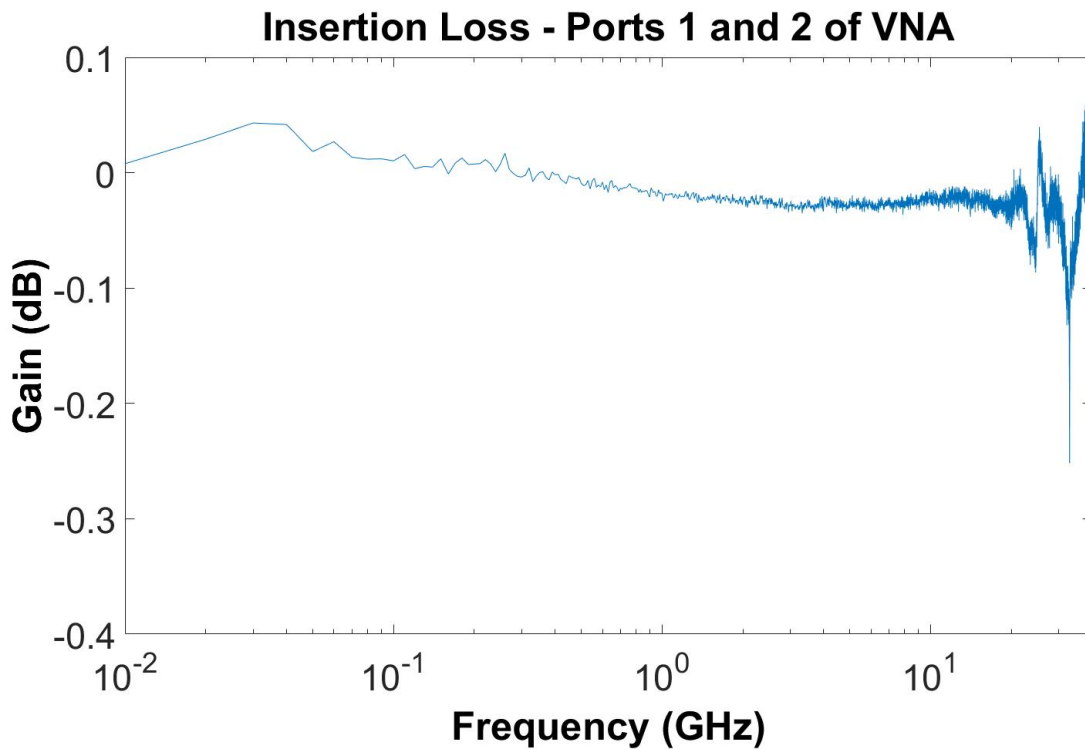


Figure Appendix D.1 - Insertion Loss of Ports Used To Make Measurements on VNA After Calibration

A TDR measurement was also made on a 50 Ohm load to check the validity of the calibration seen in Figure Appendix D.2.

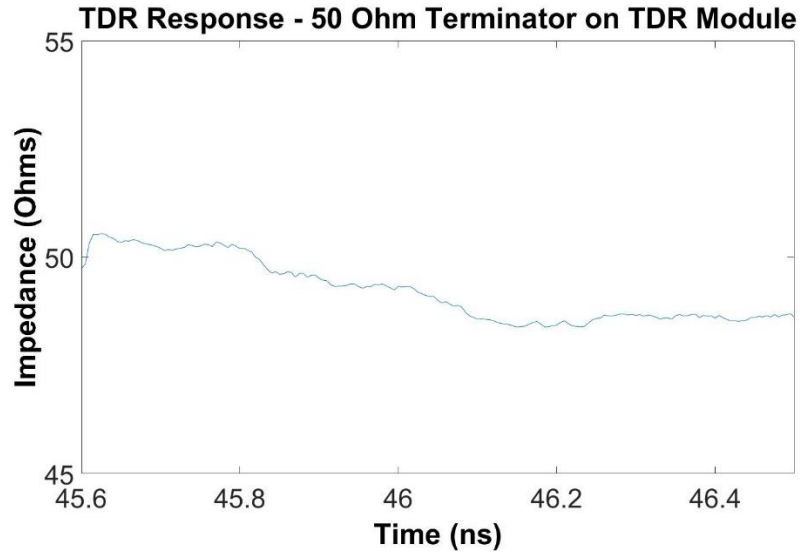


Figure Appendix D.2 - Response of Loaded Module Used To Make Measurements On TDR After Calibration

To prove the data captured on different pieces of test equipment produced the same results, the data was transformed into the opposite domain and compared as seen in Figures Appendix D.3

and Appendix D.4.

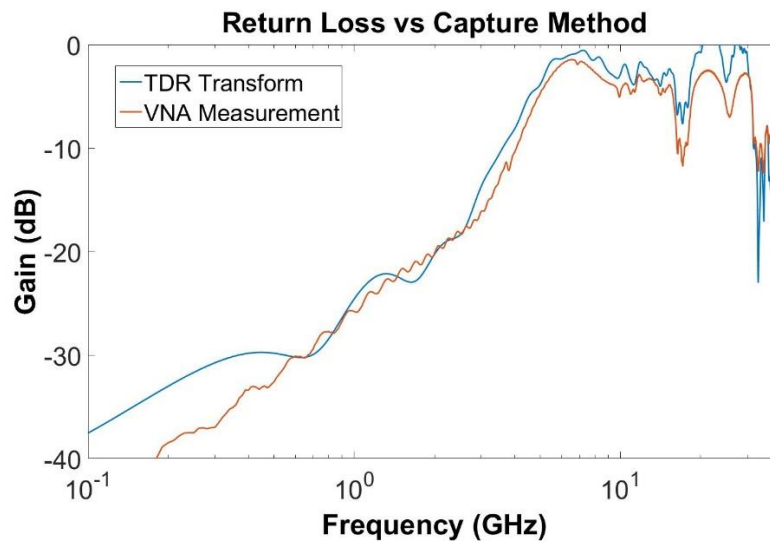


Figure Appendix D.3 - Transformed TDR Response of Time Gated Test Circuit Versus Time Gated VNA Data

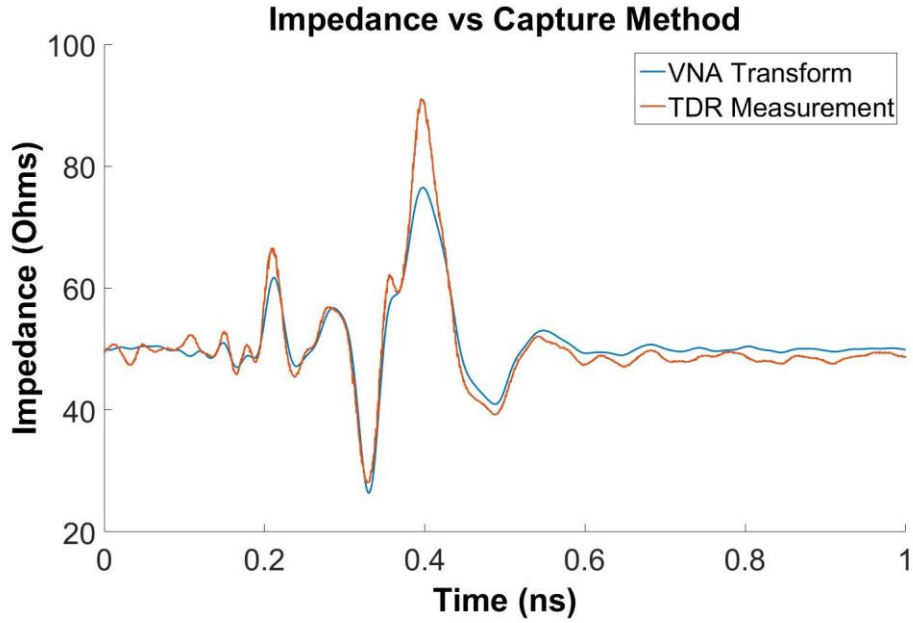


Figure Appendix D.4 - Comparison of Transformed VNA Data with TDR Data

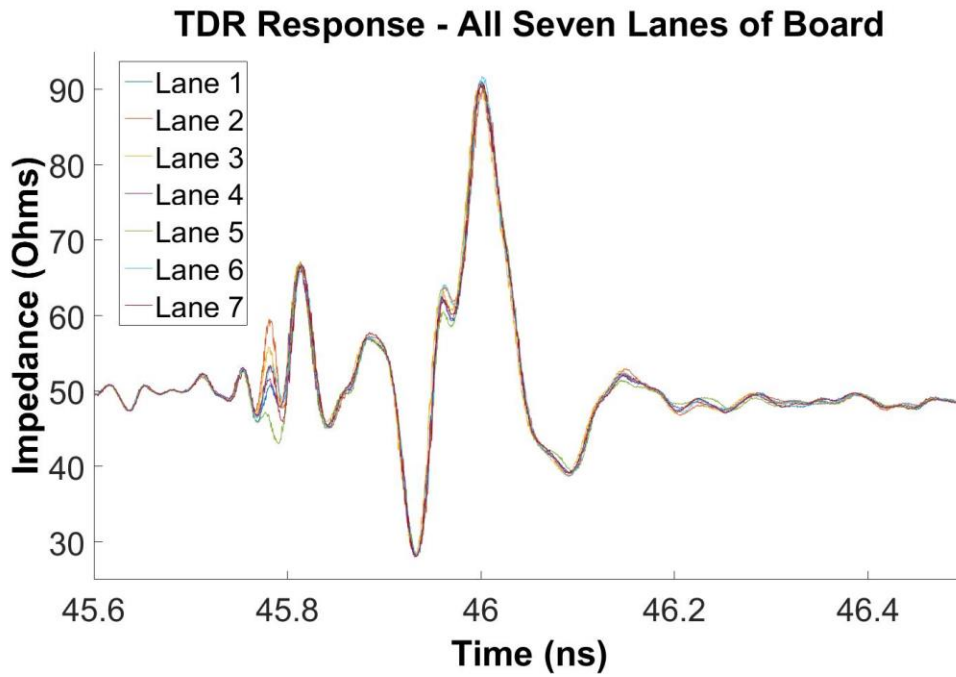


Figure Appendix D.5 - TDR On All Lanes

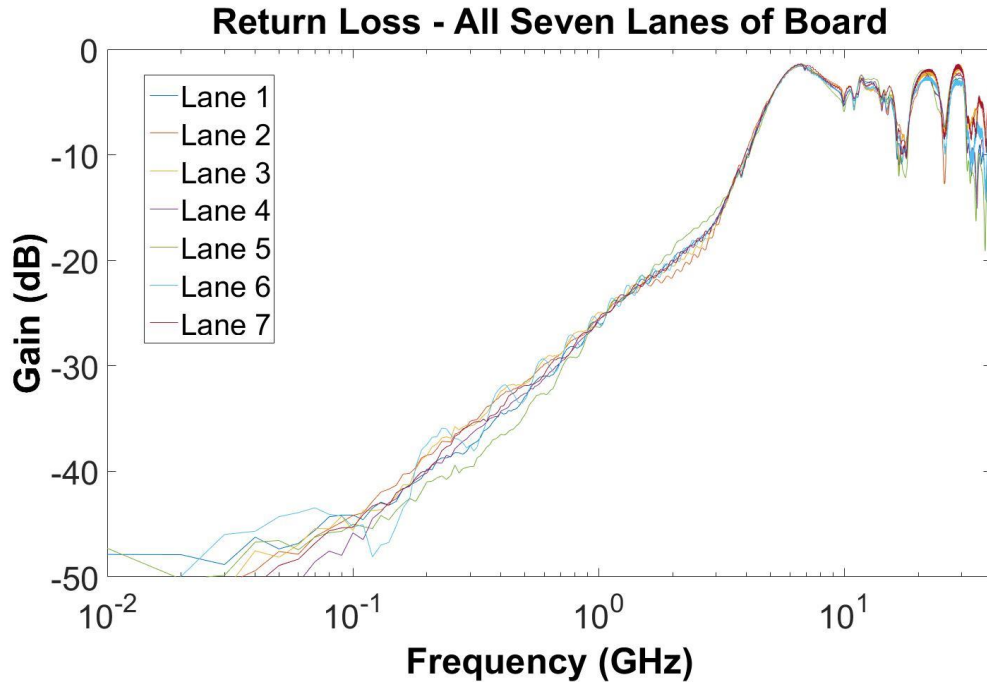


Figure Appendix D.6 - VNA On All Lanes

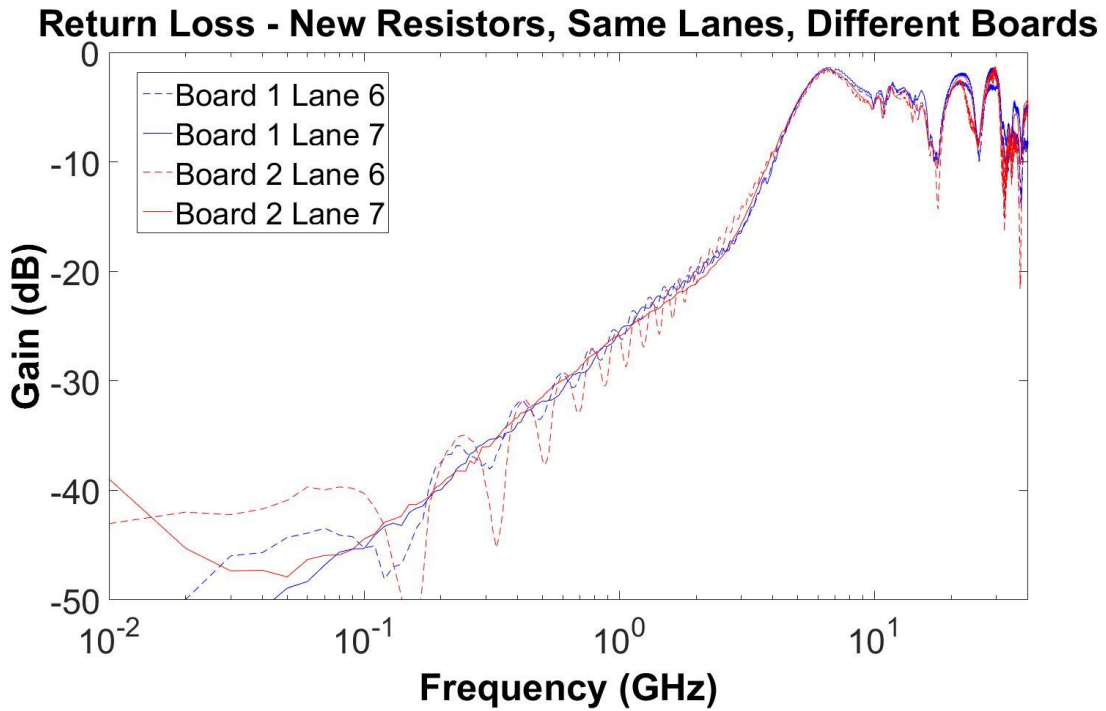


Figure Appendix D.7 - Return Loss: Same Lanes Different Fabricated Test Boards (Showing Repeatability)

APPENDIX E - MODELS

The following data shows the various HFSS models of the termination alone with the lumped parameter models of the termination alone. All models were performed to the manufacturer specified values. There was some approximations in the supplied dimensions, so the models were not expected to reflect the measurements exactly. The test circuit was also modeled (SMA connector, microstrip) with a wave port excitation as a stimulus and a variable lumped port termination so that the HFSS model or the lumped parameter model could be dropped in to compare against the entire test circuit measurements made on the VNA or TDR.

The models were also modified to provide a better representation of the measured termination. The HFSS model's height was changed from 0.10um to 0.115um and the model matched closely. The lumped parameter model's inductance was changed to 70pH and resistance needed to be increased to 60 Ohms, and the model matched closely.

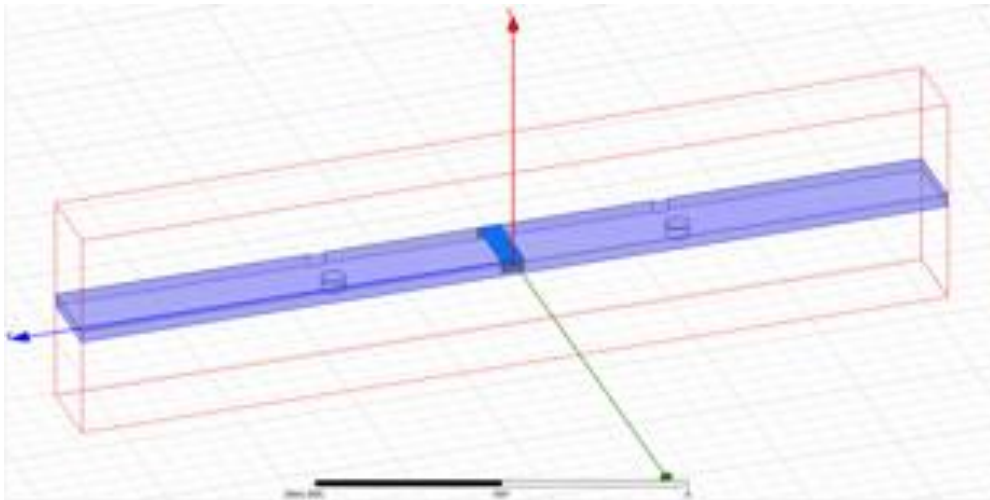


Figure Appendix E.1 - HFSS Model of Resistor

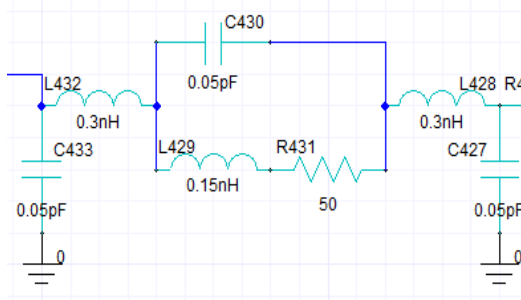


Figure Appendix E.2 - Lumped Parameter Model Used in HFSS for Termination

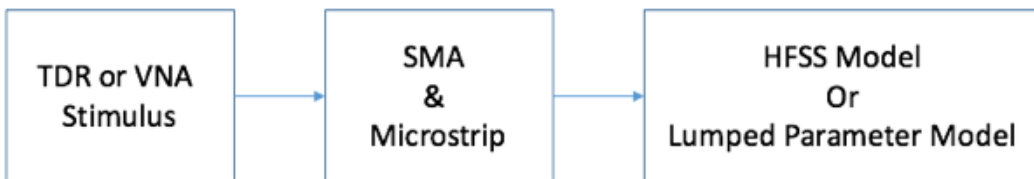


Figure Appendix E.3 - Measurements Performed in Model Environment Block Diagram

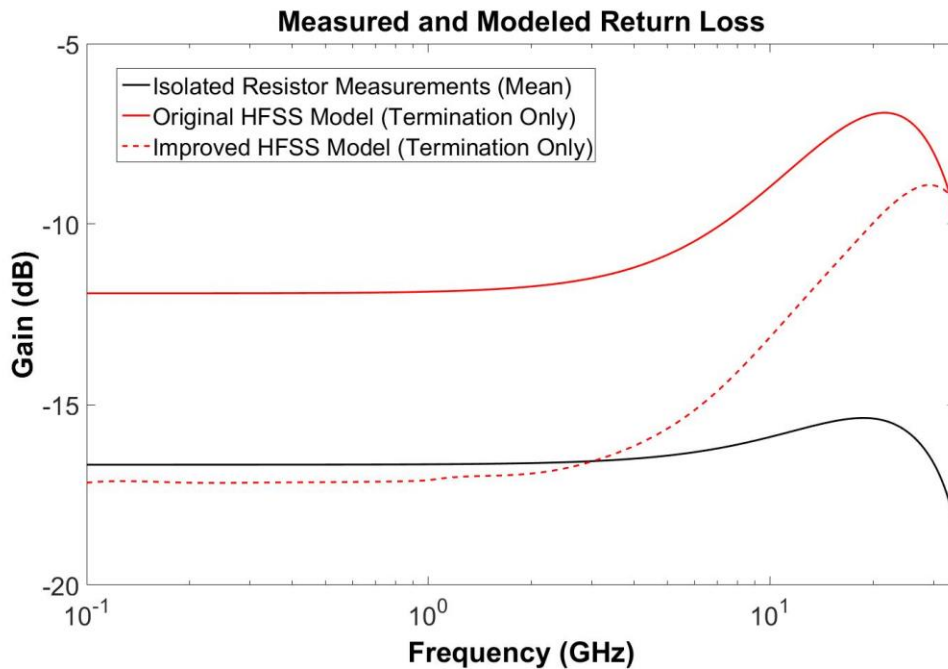


Figure Appendix E.4 – Improved HFSS Model of Modified Resistor versus Original HFSS Model of Resistor

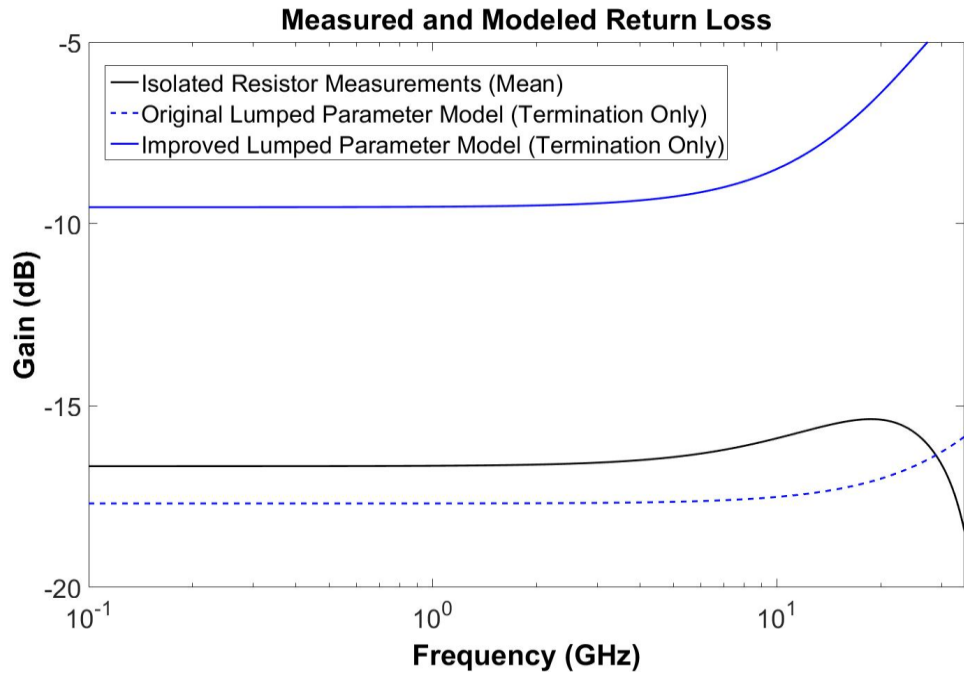
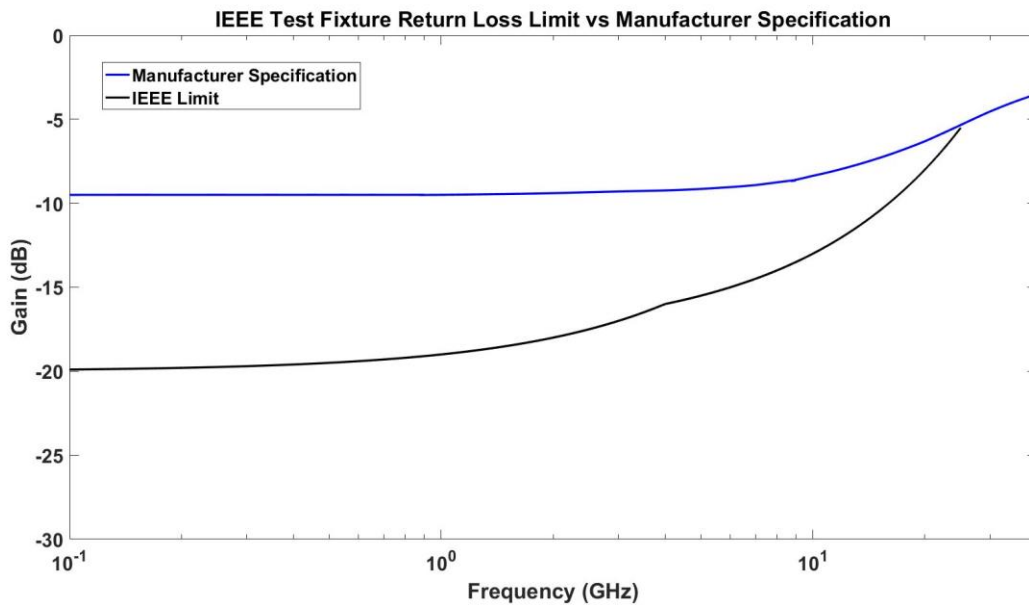


Figure Appendix E.5 - Manufacturer Specified Lumped Parameter Model Impedance versus Frequency

APPENDIX F – SPECIFICATIONS

The following figure shows the Manufacturer Specification, or how the manufacturer has reported the expected behavior of the termination, versus the chosen application specification, or the 100 Gigabit Ethernet (100GbE) Test Fixture Return Loss specification. Because these terminations are rated out to 50 GHz, 100 GbE is a relevant and widely accepted specification to choose as a reference point to evaluate the performance of these terminations.



Appendix Figure F.1 - Manufacturer and IEE Return Loss Specifications

$$Return\ Loss(f) \geq \left\{ \begin{array}{ll} 20 - f & 0.01 \leq f < 4 \\ 18 - 0.5f & 4 \leq f < 26 \end{array} \right\} (dB) \quad \text{Eq. Appendix F.1}$$

Where f is frequency in GHz