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INVESTIGATING THE EFFECTS OF SINGLE-EVENT UPSETS IN STATIC AND DYNAMIC REGISTERS

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BY

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LIST OF ACRONYMS

ASIC	Application Specific IC
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
DFF	D Flip-Flop
DICE	Dual Interlocked Cell
EHP	Electron-Hole Pair
FIT	Failure in Time
FPGA	Field-Programmable Gate Array
HCI	Hot Carrier Injection
HD-DFF	Hardened Dynamic D Flip Flop
IC	Integrated Circuit
$\mathbf{I_{NS}}$	Negative SEU current using the switch
$\mathbf{I_{PS}}$	Positive SEU current using the switch
LET	Linear Energy Transfer
MC	Monte-Carlo
NBTI	Negative Bias Temperature Instability
NGT-SDFF	Negative-Edge Triggered Static D Flip-Flop
NHD-DFF	Non-hardened Dynamic D Flip Flop
NMOS	n-type Metal-Oxide Semiconductor
PMOS	p-type Metal-Oxide Semiconductor
$\mathbf{Q_{coll}}$	Collection charge
$\mathbf{Q_{crit}}$	Critical Charge
RHBD	Radiation-Hardened-By-Design

SEE	Single-Event Effect
SER	Soft Error Rate
SEU	Single-Event Upset
SN	Sensitive Node
SNH	Selective Node Hardening
SPICE	Simulation Program with Integrated Circuit Emphasis
TDDB	Time-Dependent Dielectric Breakdown
TMR	Triple Modular Redundancy

ABSTRACT

INVESTIGATING THE EFFECTS OF SINGLE-EVENT UPSETS IN STATIC AND DYNAMIC REGISTERS

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Radiation-induced single-event upsets (SEUs) pose a serious threat to the reliability of registers. The existing SEU analyses for static CMOS registers focus on the circuit-level impact and may underestimate the pertinent SEU information provided through node analysis. This thesis proposes SEU node analysis to evaluate the sensitivity of static registers and apply the obtained node information to improve the robustness of the register through selective node hardening (SNH) technique. Unlike previous hardening techniques such as the Triple Modular Redundancy (TMR) and the Dual Interlocked Cell (DICE) latch, the SNH method does not introduce larger area overhead. Moreover, this thesis also explores the impact of SEUs in dynamic flip-flops, which are appealing for the design of high-performance microprocessors. Previous work either uses the approaches for static flip-flops to evaluate SEU effects in dynamic flip-flops or overlook the SEU injected during the precharge phase. In this thesis, possible SEU sensitive nodes in dynamic flip-flops are re-examined and their window of vulnerability (WOV) is extended. Simulation results for SEU analysis in non-hardened dynamic flip-flops reveal that the last 55.3 % of the precharge time and a 100% evaluation time are affected by SEUs.

CHAPTER 1

INTRODUCTION

1.1 Background

As technology continues to scale down, there is an increasing integration of more and more devices on a single die. However, the reliability of the integrated circuit (IC) designs becomes severely challenged. Previously negligible noise effects are becoming more prominent, leading to significant reliability and performance degradations of IC circuits. Failures in deep submicron circuit designs are also collectively known as single event effects (SEEs) and can lead to permanent (hard) or temporary (soft or transient) faults, respectively [1]. A permanent error leads to an irreversible damage and malfunction of the digital circuit. Examples of noise sources that cause permanent failures include the hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI) in transistors and electro-migration in interconnects [2]. The impact of hard error on an integrated circuit is illustrated in the following paragraph using the example of electromigration.

Electromigration (EM) is the transport of material caused by the gradual movement of the ions in a conductor. It eventually results in highly resistive interconnect or contacts and leads to open circuits [73]. Due to the need for low interconnect resistivity and high electromigration reliability, the semiconductor industry has recently shifted to using copper interconnects as opposed to using copper doped with aluminum [72]. In copper interconnects, the top surface of the copper damascene line is covered with a dielectric film, while the bottom surface and two sidewalls are sealed with a tantalum (Ta) liner [72, 73]. The tantalum liner prevents

electromigration along the surfaces it covers. However, the top surface of the line is not covered with tantalum. As a result, electromigration in copper interconnect is dominant at the top interface layer between the interconnect and the dielectric [73] as shown in Figure 1-1.

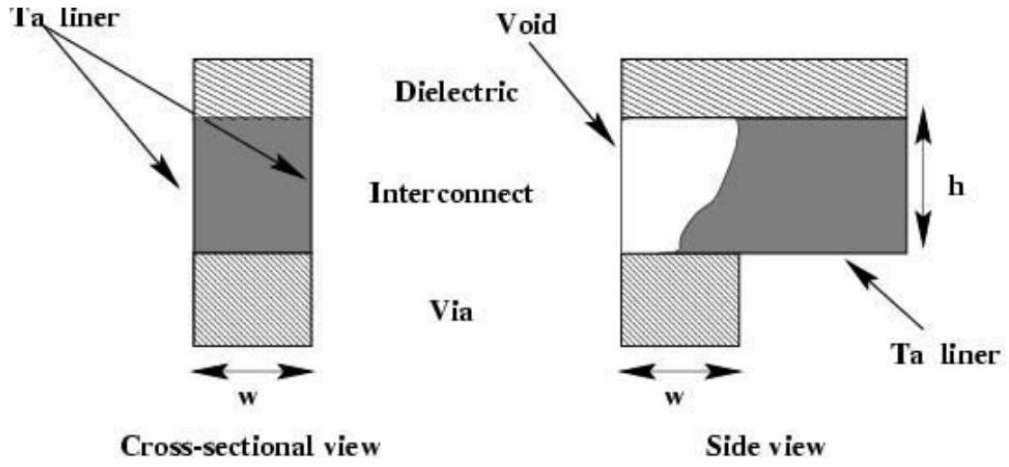


Figure 1-1. Electromigration in copper interconnects [73]

It is important to note that electrons may collide with the metal atoms as they move through the metal lines [74]. If these collisions transfer sufficient momentum to the metal atoms, then these atoms may get displaced in the direction of the electron flow. The depleted region becomes the void, and the region accumulating theses atoms creates an extrusion as shown in Figure 1-2. At the site of metal atom pile up, the resulting extrusions can cause shorts between adjacent metal lines [73].

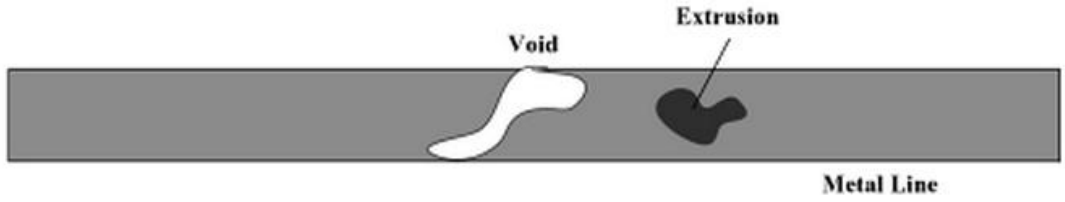


Figure 1-2. Void and extrusion in a metal line due to EM [74]

Unlike permanent errors, transient failures occur occasionally because of temporary environment conditions and last only for a short period of time. Examples of transient failure sources include power supply and interconnect noise, electromagnetic interference, electrostatic discharge and radiation-induced soft errors. Among transient errors, the radiation-induced soft error has become one of the most serious soft errors in deep submicron circuits. The radiation-induced soft errors caused by the interaction of highly energetic particles striking the sensitive regions in semiconductor devices are classified as single-event transient (SET) and single-event upset (SEU). The SET occurs in combinational circuits whereas the SEU happens in memory circuits as shown in Figure 1-3.

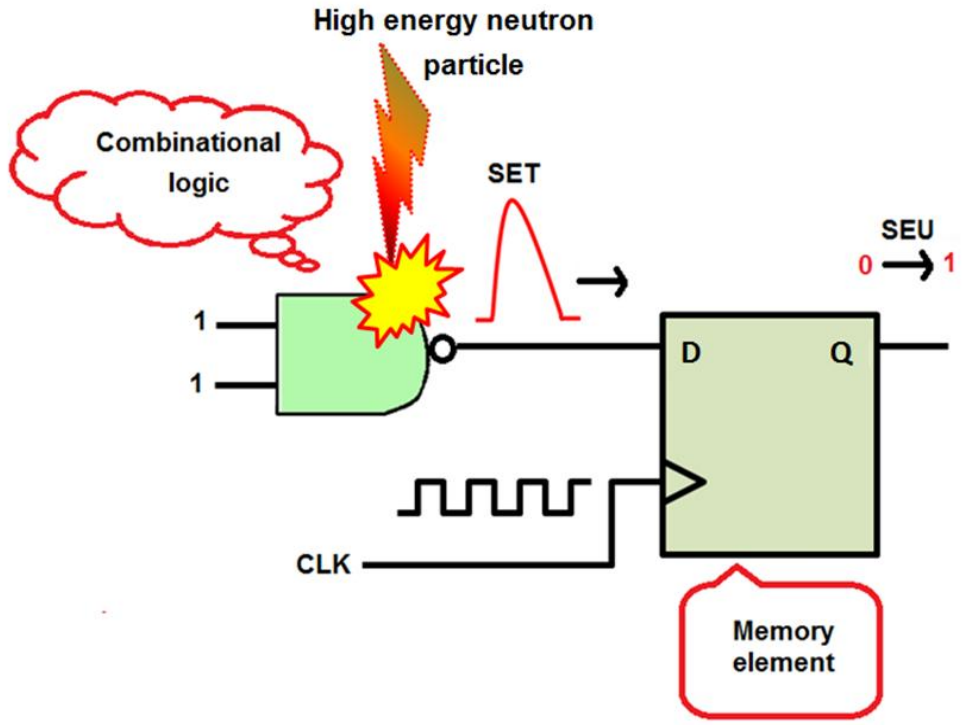


Figure 1-3. SEU in a D flip-flop due to a latched SET.

SEUs are the focus of this thesis. A SEU occurrence transfers the energy from the particle to bound electrons, promoting them to the conduction band and leaving a track of electron-hole

pairs (EHPs) in the semiconductor device. Linear energy transfer (LET) is defined as the rate of this energy loss per unit path length, dE/dx, divided by the density of the target material, resulting in units of MeV-cm^2/mg. If the charge is generated near a reverse-biased p-n junction, then the charge can be collected by the junction. If the collected charge is sufficient enough, it will create a single-event upset. However, charge generation deep in the bulk semiconductor region may recombine before it is collected by the junction [3] and no SEU event will occur due masking effects of the logic gates.

Radiation-induced single-event upsets (SEUs) constitute a major reliability concern for modern registers. As transistor feature sizes continue to decrease (as shown in Figure 1-4), the existing SEU analysis methods and hardening techniques become obsolete.

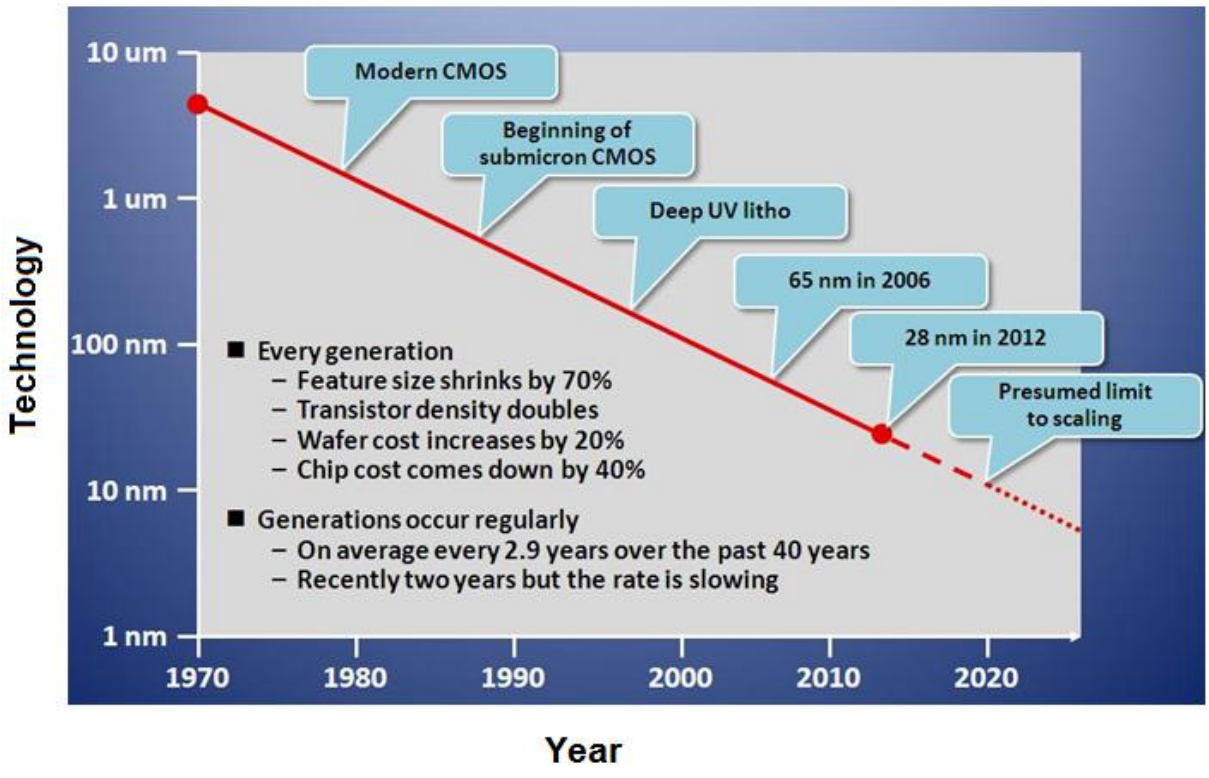


Figure 1-4. Technology scaling [75]

In addition, it is important to note that the noise margin is often used as a measure of device stability [67]. The continued shrinking of transistor feature sizes is coupled with a reduction of the transistor overdrive voltage and noise margin as indicated in Figure 1-5(a) and Figure 1-5 (b), respectively. In this thesis, a 180 nm process was used in all simulation analyses. As it can be seen in the shaded area of the noise margin chart in Figure 1-5 (b), the noise margin associated with 180 nm technology is smaller comparing with the noise margin of older technologies. Thus, the degradation of the noise margin due to technology scaling makes the transistor more vulnerable to SEUs since only a small induced voltage transient may upset the IC sensitive node.

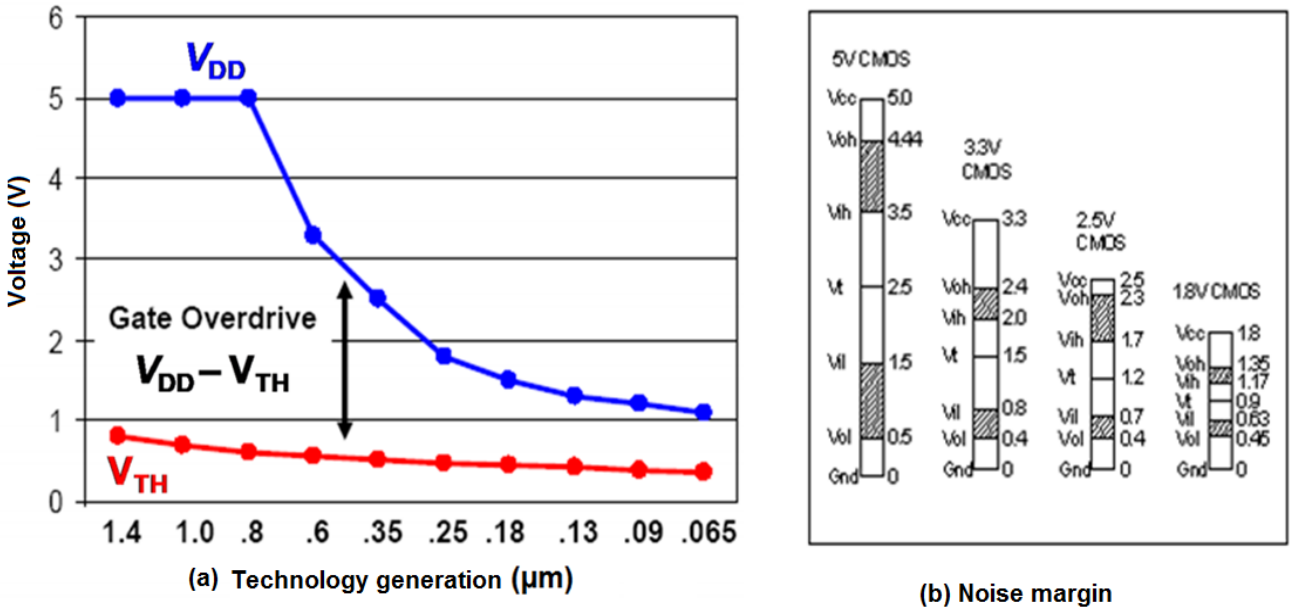


Figure 1-5. Impact of technology scaling on (a) voltage and (b) noise margin [75].

This thesis proposes a novel approach to re-examine the sensitivity of both static and dynamic registers in order to mitigate the impact of SEUs as technology keeps shrinking. Since

the D flip-flop (DFF) represents the fundamental building block of registers and microprocessors, static D flip-flops and dynamic logic based flip-flops are used for simulation test purposes.

The D flip-flop (DFF) acts as a sequencing element while designing any pipelined system. However, unlike latches flip-flops operate either at the rising edge or at the falling edge of the clock. The DFFs latch the input state to output state triggered by the rising or falling edge of the clock. A generic flip-flop is made of two back-to-back latches and this flip-flop configuration is called the master-slave flip-flop as shown in Figure 1-6.

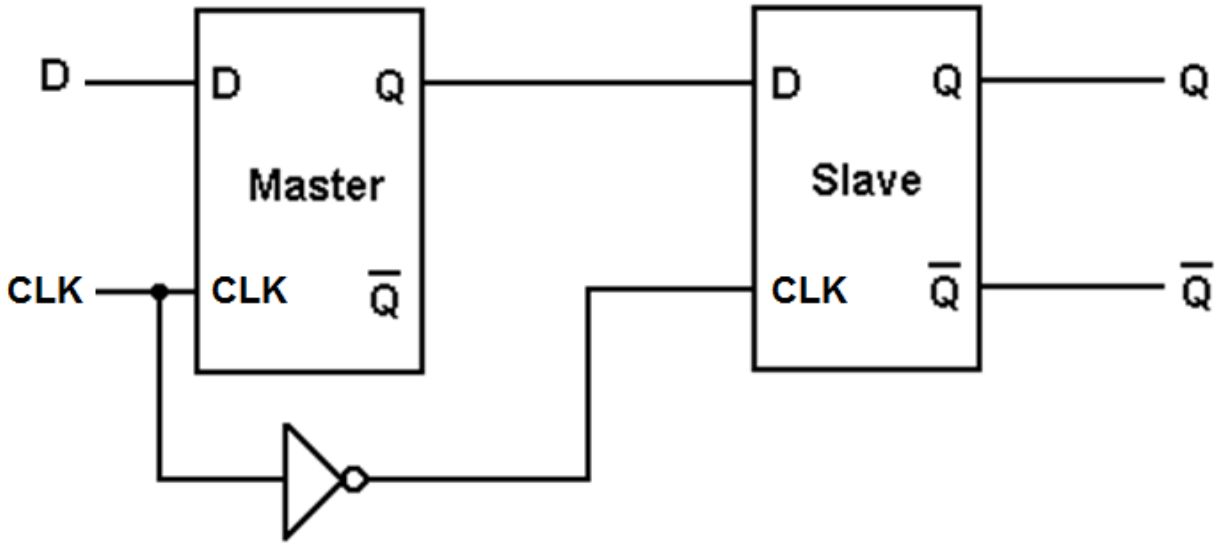


Figure 1-6. Circuit configuration of a negative edge-triggered master-slave flip-flop.

The SEU analysis of the static CMOS master-slave flip-flop circuit used in this thesis is presented in Chapter 3. In the following sections, a brief discussion of SEUs as a reliability concern is provided in section 1.2 and the thesis summary as well as its contributions are given in section 1.3.

1. 2 SEUs in deep submicron registers

1.2.1 A brief history of SEUs

The history of SEUs started in the 1960s. The first paper to ever explore the problem of SEUs was published in 1962 [4] and it anticipated the eventual occurrence of SEU in microelectronics due to terrestrial cosmic rays. The authors of this paper also predicted that the minimum volume of semiconductor devices would be limited to about 10μm on a side due to these upsets. However, the presentation of the first validated report of radiation-induced SEUs in space was given at the NSREC in 1975 [5] and stated four observed upsets in 17 years of operation in a communications satellite. Due to the small number of observed errors, it had been several years before the importance of SEU was fully recognized. In the late 1970s, evidence continued to mount that cosmic-ray-induced upsets were indeed responsible for errors observed in satellite memory subsystems, and the first models for predicting system error rates were formulated [6].

1.2.2 SEU modeling

SEU modeling approaches at the device level include either system or accelerated test methods. In the case of system method, the SEU sensitivity of a memory circuit is analyzed under nominal conditions [77]. This method consists of testing a large number of devices for a sufficiently large period of time, i.e., for weeks or months [78]. The number of recorded SEUs has to be large enough in order to accurately determine the SEU rate of a particular memory

element. Although this method is a direct and an accurate measurement of the circuit's sensitivity to SEUs, it is only feasible in a production environment, not for research purposes since it requires thousands of devices to be tested in parallel for long periods of time [77].

The accelerated SEU testing method is a more practical approach to determine the SEU sensitivity of a memory circuit. This method requires the presence of an ionization source with a relatively high activity, for instance, an alpha emitting source or a neutron (or proton) beam. In this method, devices are exposed to an extra radiation source. The energy spectrum of the emitted radiation is well-known and the intensity is both well-defined and typically several orders of magnitude higher than the intensity of background radiation. In addition, only a few devices are needed and measurement can be performed within days or hours [79].

Device simulation offers the possibility to study the phenomena that are at the origin of the single-event upset, which is not possible with experimental methods. Device simulations focus on the collection dynamics of the charge generated by ionizing particles and can be used to study the details of the SEU creation mechanisms and device response to induced charges, such as funneling and ion track structure [80] as shown in Figure 1-7.

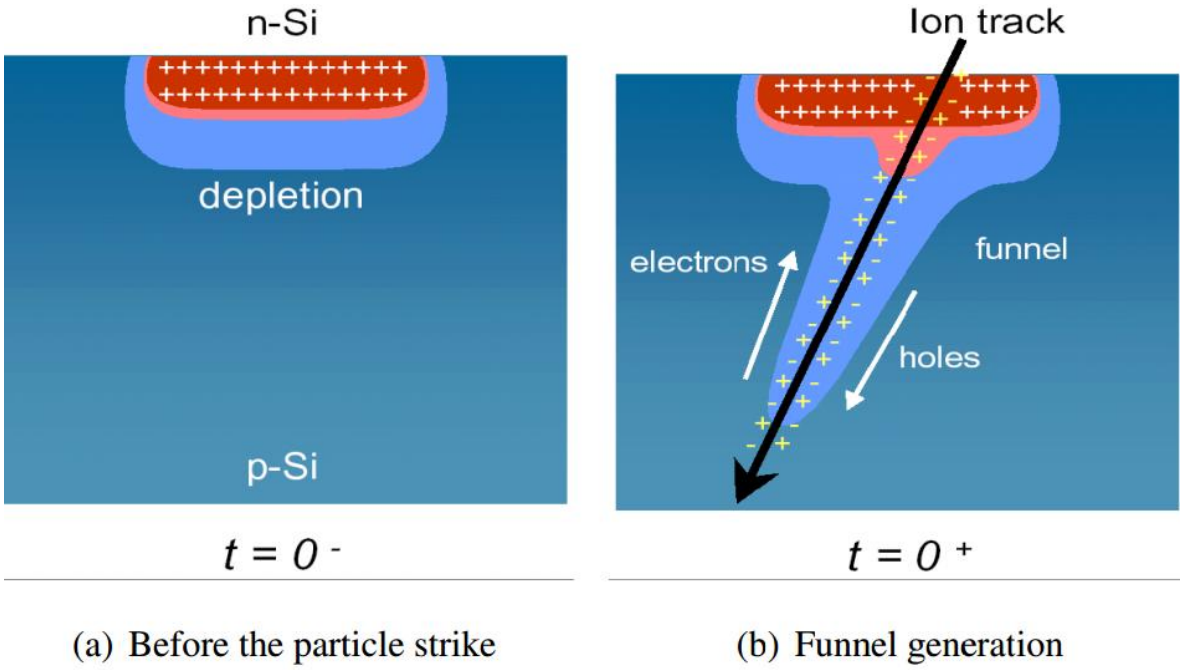


Figure 1-7. Charge generation and collection after a radiation-induced particle strike [77].

It is important to note that the analysis and modeling of SEUs in memory elements is an inherently complex problem. Various simulators and tools have been developed for SEU modeling and analysis over the past few decades [7-9]. These models provide insight into the effects of SEUs on registers. The tools for predicting and analyzing SEU effects include: circuit simulators for modeling the circuit response to a single event, device simulators for predicting the physical interaction between the charge generation and device reaction, and codes that can help predict error rates for a particular circuit. Since this thesis uses circuit simulation and device simulators, the importance of the two simulators are discussed below.

Device simulators

Device simulators use the information such as the doping prolife to determine the interaction of the device with the ion strike. Funneling shown in Figure 1-7 (b) strongly depends on the substrate doping. Substrate with a lower doping concentration shows a slower field distortion, but greater charge collection [77]. Lower doping means that the substrate has higher resistivity and requires more time for the holes to be pushed out of the depletion region. Hence the depletion region can collect more charge in the process. If the particle strike happens between the two n+ regions, then resulting funneling action can collect enough charge to turn the transistor on, resulting in the change of state, thus leading to a bit flip or a SEU.

Device simulators provide a cost effective means for analyzing different effects of device irradiation. The generated currents at the device terminals can be used in circuit simulators to determine the effects of the irradiation on circuit functionality. Examples of device simulators include: Athena [10, 11], SUPREM [12-15], Stanford's PISCES [16, 17], Silvaco's Atlas [18], PADRE [19], MEDICI [20], and Synopsis [21].

Circuit simulators

Circuit simulators can be used for simulating complex circuit designs from a macro-model view of the device. As the physical models are typically generated by extensive measurements of a given technology, circuit level simulations tend to represent realistic circuit performance which is approximately similar to physical device modeling. In addition, circuit

level simulations provide a cost effective way for analyzing the radiation performance of a circuit design. While it is true that circuit simulators sacrifice accuracy in device modeling, they make up for it with vastly increased computational throughput. Examples of circuit simulators include: Berkeley's SPICE [22], Silvaco's SmartSpice [18], Mentor's AccuSim [23], Synopsis HSPICE [21], and Cadence Virtuoso Spectre [24].

Tools such as the soft-error Monte-Carlo modeling (SEMM) program [25] used in industry provide the best level of accuracy that can be achieved by simulations, but are quite expensive because of the time-consuming Monte-Carlo (MC) simulations. The soft error simulation algorithm developed by Kaul et al. [26] uses parameterized closed form expressions to represent the responses of each gate. The generation, propagation, and capture of the SEU are modeled without running time-consuming circuit-level simulations, and hence the speed of the tool is greatly improved. However, this algorithm does require a database of parameters to fit the analytical expressions. The complexity of such equations is expected to increase dramatically for newer fabrication processes as a result of increasing complexity of the device models.

In this thesis, the double-exponential current source of the form

$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta} \left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \quad (1)$$

is used to model the SEU current at the transistor level or circuit level [27]. In equation (1), Q_{coll} is the charge deposited from heavy-ion strike; τ_α is the collection time constant or falling time and τ_β is the ion-track establishment time constant or rising time constant of the junction. In this work, it was opted to use the SEU current source described in equation (1) because it realistically

represents the behavior of a naturally occurring photocurrent from a real ion-strike photocurrent [27].

The reverse-biased junction is the most charge-sensitive part of circuits, particularly if the junction is floating or weakly driven (with only a small drive transistor or high resistance load sourcing the current required to keep the node in its state). The most sensitive node is usually the drain node of the transistor as shown in the cross-section view of the NMOS transistor (Figure 1-8). The high energy particle strike at a sensitive node causes a series of mechanisms, which result in the creation of the SEU current shown in Figure 1-9 (d). The development of photocurrent from initial ion strike to SEU current source is shown in Figure 1-9.

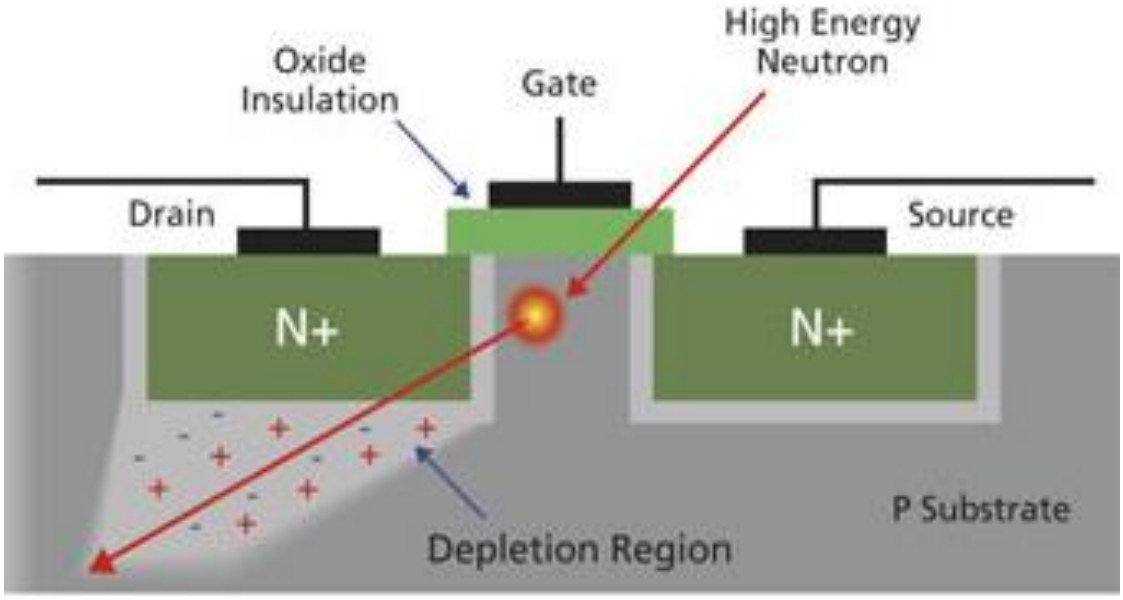


Figure 1-8. Sensitive node (drain) of the NMOS.

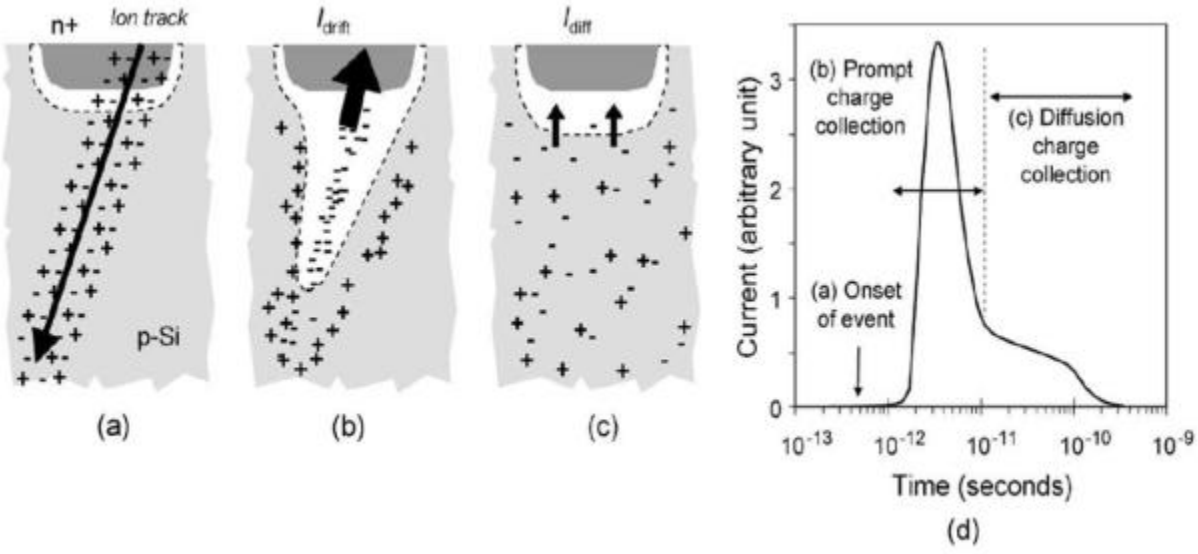


Figure 1-9. Development of photocurrent from initial ion strike to creation of SEU current [27].

A cylindrical track of electron hole pairs with a submicron radius and a very high carrier concentration are created at the beginning of an ionizing radiation event (a). When the resultant ionization track traverses or comes close to the depletion region, carriers are rapidly collected by the electric field creating a large current/voltage transient at that node. A remarkable feature of the event is the concurrent distortion of the potential into a funnel shape [7]. This funnel greatly enhances the efficiency of the drift collection by extending the high field depletion region deeper into the substrate (b). The size of the funnel is a function of substrate doping—the funnel distortion increasing for decreased substrate doping. This "prompt" collection phase is completed within a nanosecond and followed by a phase where diffusion begins to dominate the collection process (c).

Extra charge is collected as electrons diffuse into the depletion region on a longer time scale (hundreds of nanoseconds) until all excess carriers have been collected, recombined, or

diffused away from the junction area. The corresponding current pulse resulting from these three phases is also shown in Figure 1-9 (d) [27]. Overall, the farther away from the junction that the event occurs, the smaller the amount of charge that will be collected and the less likely it is that the event will cause a SEU. The amplitude of the induced transient has to be greater or less than the threshold voltage in order to erroneously change the state of the impacted circuit from logic "0" to logic "1" or logic "1" to logic "0", respectively.

1. 2.3 SEUs as a reliability concern

SEUs have become a major challenge for the design of microprocessors. In a digital circuit, information is encoded and processed as signals in the form of logic "1" and logic "0". Disturbances in the form of current or voltage variations may potentially damage the original signal, thereby causing a distorted or an erroneous data in the digital circuit as shown in Figure 1-10. SEUs occur when the passage of an ionizing particle in the semiconductor deposits a charge track which is then collected at the sensitive node. Radiation-induced upset errors have quickly evolved to a serious limiting factor in the circuit reliability [27]. In this thesis, "reliability" is a term used to describe the tendency of a digital circuit to restore the distorted signals and its ability to operate properly with the presence of noise interferences.

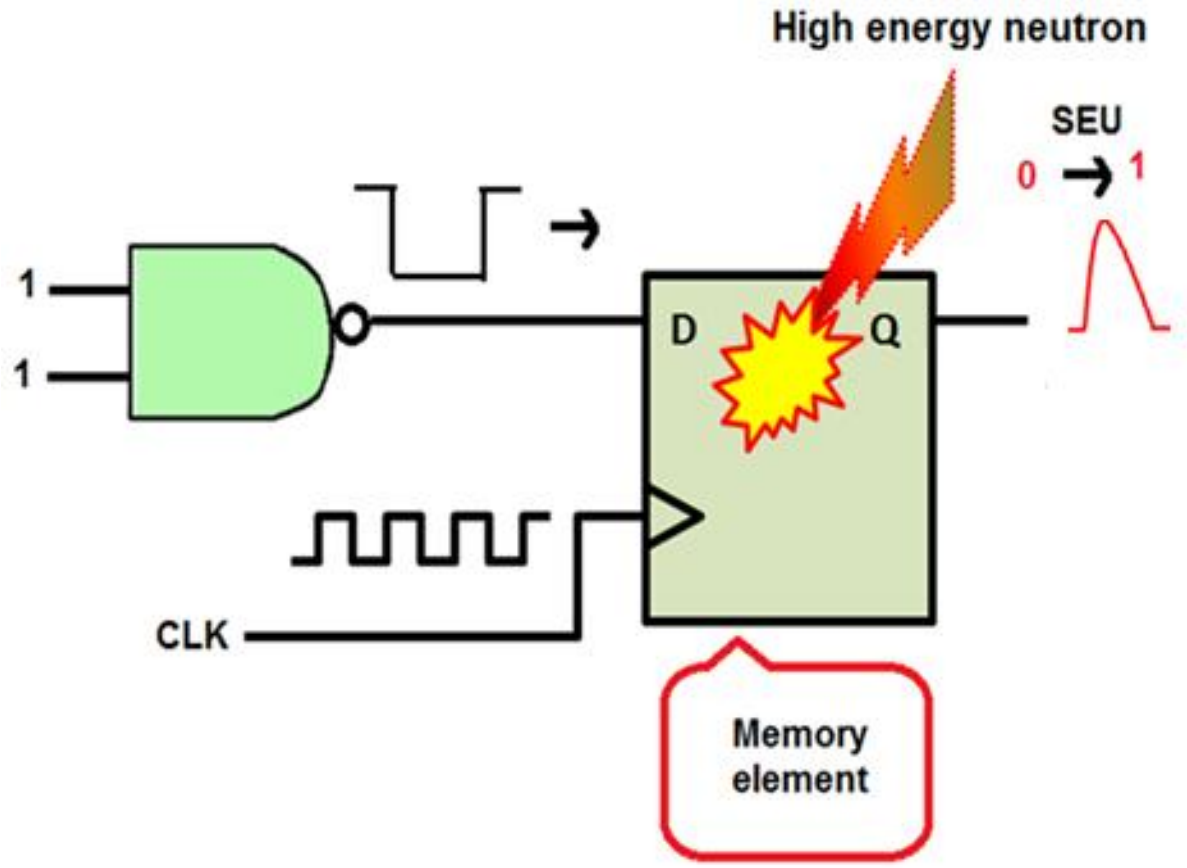


Figure 1-10. SEU due to a high energy particle strike in a D flip-flop.

Moreover, the shrinking feature sizes of transistors causes a reliability degradation and design concern and needs to be properly addressed. Several factors collectively contribute to the reliability issue of modern registers. First, as device dimension continues to downscale, noise sources become significantly more prominent than ever. Second, as the supply voltage reaches sub-volt range, noise margin of the semiconductor devices is significantly reduced, thus making the required noise level to cause irreversible distortion much lower. Third, the number of devices on a single die has increased. Although the increased integration capability makes sequential circuits to operate at a much faster rate, stronger and more frequent interactions among adjacent devices can lead to more disastrous error effects and higher failure rates.

This thesis uses both static D flip-flops and dynamic logic based D flip-flops as simulation test structures. There is a significant difference in the SEU sensitivity between the two flip-flop architectures. The schematics and the SEU analysis of the two flip-flop cells are largely discussed in Chapter 3 and Chapter 4 of this thesis, respectively. The choice of the D flip-flop as a test circuit in this thesis was driven both by its simplicity and its extensive use in modern digital circuits. The flip-flop is the basic building element of a register and it is widely used in digital and mixed-signal ASICs for microprocessors, both in synchronous operation and in control registers [28]. For example, flip-flops are extensively used in the SRAM cell, which commonly acts as the configuration memory for FPGAs. FPGAs are semiconductor devices that can be user-programmed with a logic function. The function can range from common structures such as arithmetic logic units or microprocessors to custom application-specific logic. The FPGA architecture consists of two key functional blocks – the configurable logic block (CLB) and a switch matrix that forms the interconnections between them.

FPGAs have gained popularity in recent years particularly in aerospace applications. One of the major reasons being the prospect of performing post-launch design optimizations or changes in spacecraft objectives. Present line of commercial FPGAs are capable of integrating powerful embedded processors and several common intellectual property cores that provide a complete system-on-chip solution [29]. However, the SRAM cell which is a basic component of the FPGA is known to be very vulnerable to SEUs [28], and its higher sensitivity to SEU may lead to a compromised functionality of the FPGA. SRAM cell is based on the 6-transistor storage cell. Figure 1-11 shows a possibility of how a SEU might affect the SRAM cell.

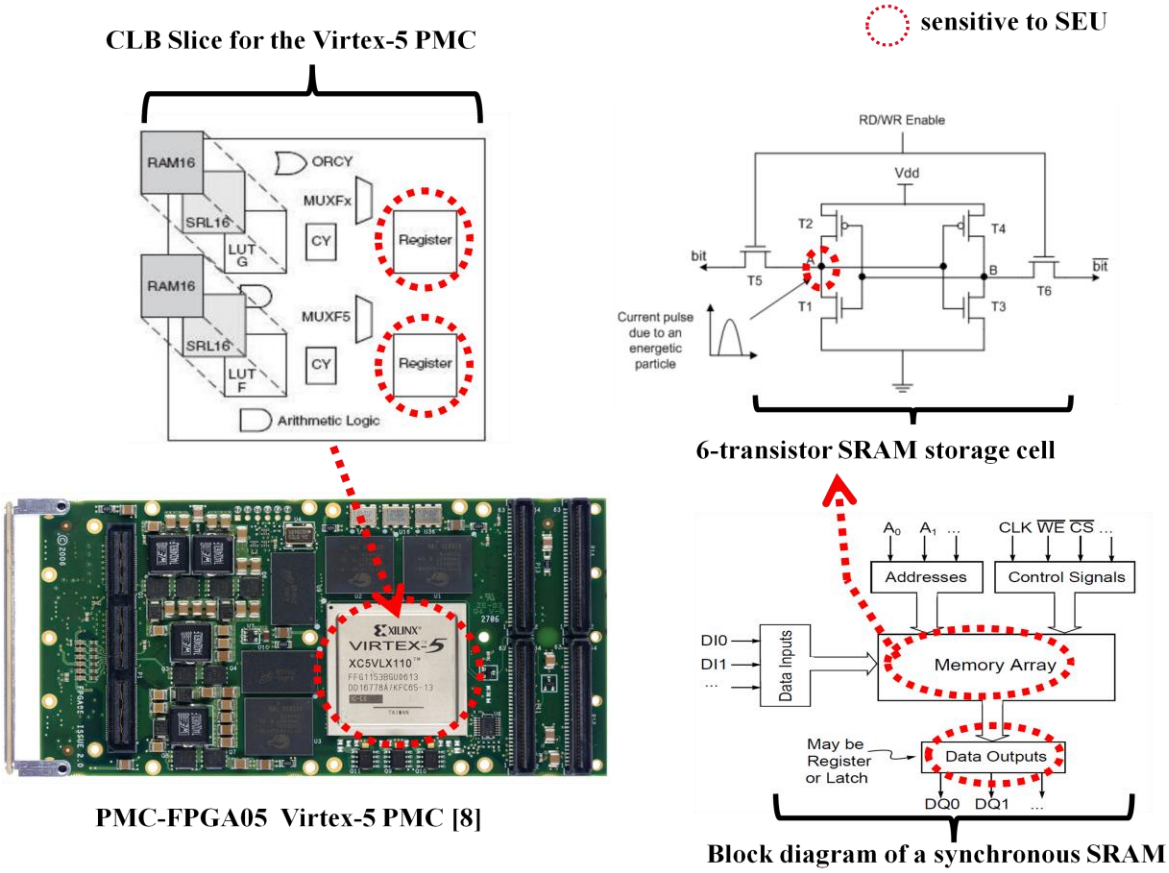


Figure 1-11. Illustration of SEU sensitivity of the PCM-FPGA05 Virtex-5

In Figure 1-11, various components of the FPGA that are vulnerable to SEUs are highlighted. The key message in Figure 1-11 is to show that the reliability of IC designs matters since even one microprocessor can have multiple areas that are vulnerable to radiation-induced SEUs as highlighted in Figure 1-11.

1. 3 Masking effects – Inherent SEU immunity of digital circuits

Masking effects are usually evaluated in studies of single-event transients (SETs), which are soft errors occurring in combinational circuits. In a combinational circuit, a voltage glitch due

to a radiation particle strike can propagate to the primary input of the flip-flop circuit and may be latched by the flip-flop as shown before in Figure 1-3. Whether or not a voltage glitch induced by a radiation particle strike at any gate node of a combinational circuit propagates to the primary output of the flip-flop (and results in a failure) depends upon the following three masking factors [31, 64-66]:

Electrical masking

Electrical masking occurs when a voltage glitch induced at a circuit node by a highly energetic particle strike attenuates as it propagates through the circuit to the primary output of a memory circuit such as the flip-flop. Electrical masking can decrease the magnitude of the induced voltage glitch to a value which does not cause any soft errors in the flip-flop circuits as shown in Figure 1-12. The effect of electrical masking cascades from one gate to the next because the slope at each gate decreases and hence the amplitude also decreases [82]

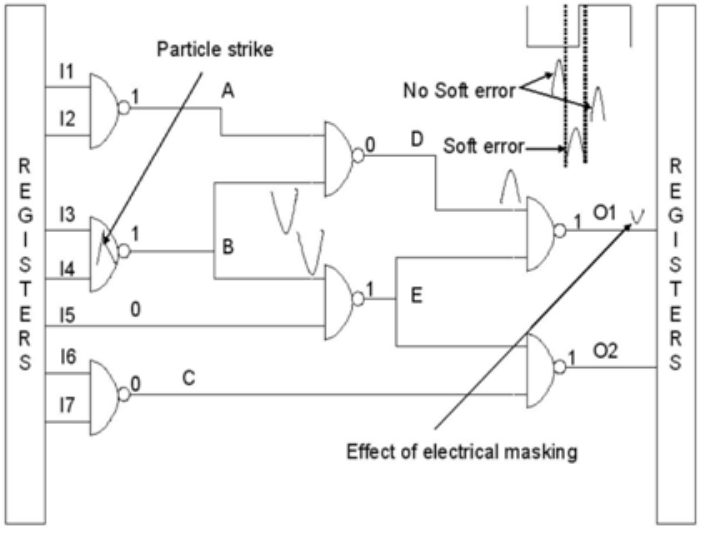


Figure 1-12. Electrical masking in a pipelined register stage [83].

Assuming that a particle strike causes a negative pulse at node B, the inherent delay in the gates before the next set of registers results in the progressive attenuation of the pulses, as shown in the Figure 1-12. This represents electrical masking, where the pulse is much smaller when it reaches the output O1.

Logical masking

Logical masking occurs when there are no functionally sensitized paths from the circuit node where a high energy particle strike has taken place to a primary output or memory element. As an example, Figure 1-13 is used to illustrate the mechanism of logical masking. In Figure 1-13, the controlling input A (where A = 0) makes that there is no path from the input node B where a high energy particle has stricken to the output node Y of the NAND gate. As a result, the SET at node B is considered to be logically masked.

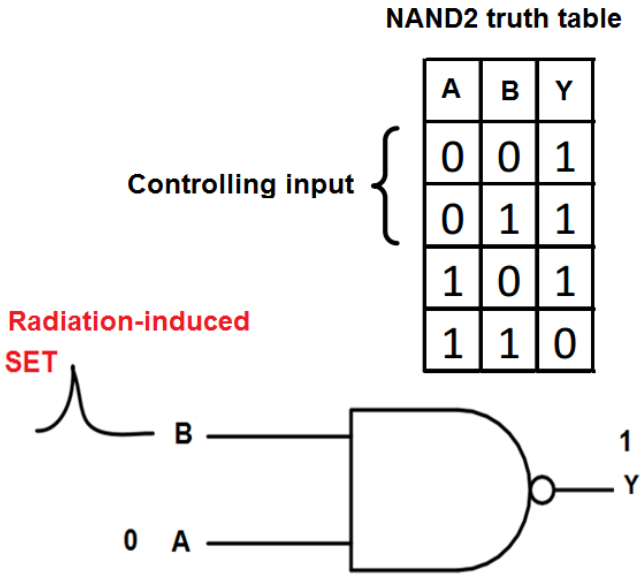


Figure 1-13. Logical masking in a NAND2 gate.

As it can be seen in Figure 1-13, if the input A of the NAND gate is logical “0”, the output of the NAND gate will always be valid as shown in the NAND2 truth table (logical “1”) regardless of the induced transient at the input B.

Temporal masking or latch-window masking

Temporal masking takes place if a voltage glitch due to a radiation particle strike reaches the sequential circuit at an instant other than the latching window of the sequential the circuit as illustrated in Figure 1-12 and Figure 1-14. The SET pulse should arrive within the setup and hold time of the latching element in order for the SET to be latched within the memory element. SET pulses that occur outside this latching window, as shown in two cases of Figure 1-14, do not result in a SEU. Thus, temporal masking depends on the frequency of operation of the sequential circuit and the pulse width of the propagated SET. Temporal masking provides the flip-flop circuit with certain degree of radiation tolerance against SEUs.

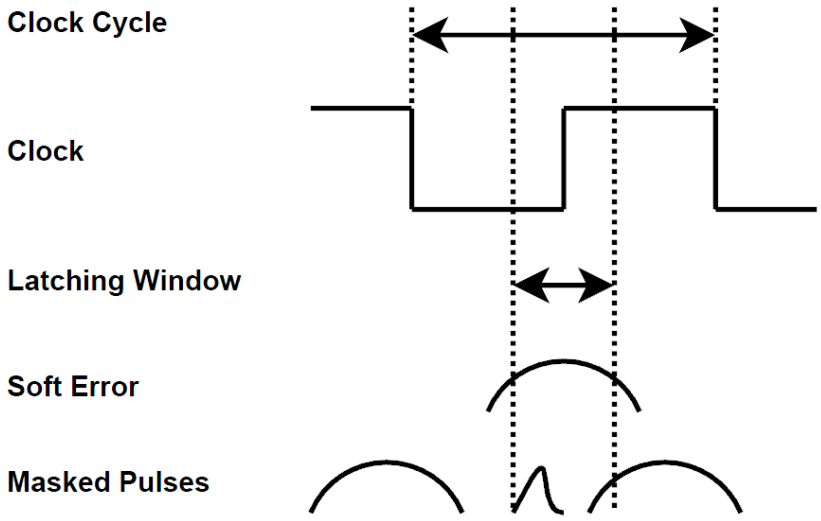


Figure 1-14. Example of latch-window masking [64]

The strengths of the three masking effects are purely determined by the electrical, logic and timing characteristics of the digital circuit and are independent of the external high energy particle activities. Thus, digital circuits are believed to have inherent tolerance to single event effects.

1. 4 Radiation hardening techniques

In addition to the IC circuit's soft error mitigation through masking effects, circuit designers oftentimes opt to design radiation-hardened (rad-hard) circuits which are more robust to the effects of highly particle strikes. Radiation hardening techniques used in circuit design can be classified into two main categories: radiation hardening by process (RHBP) and radiation hardening by design (RHBD). The RHBP focuses on modifying the IC fabrication process to make it structurally resilient to the effects of highly energetic particles strikes [84]. However, the existing hardened processes are substantially larger than current industry standard processes, while RHBD techniques allow current designs to scale with future process sizes [57]. For this reason, RHBD implementations are necessary for modern processes and are utilized in radiation hardened (rad-hard) circuits.

It is worth noting that all radiation hardening techniques have their individual advantages and disadvantages and should be selected depending on the application. In this section, various radiation hardening techniques will be reviewed, focusing specifically on two techniques called temporal hardening and node interlocking. Radiation hardening can be applied at any level of abstraction. It can be used at the device level, circuit level or at the architectural level. In

addition, hardening techniques are generally chosen to meet the application requirements.

1.4.1 Examples of radiation hardening by design (RHBD) techniques

As IC transistor feature sizes decrease, the critical charge Q_{crit} that is required to upset a sensitive node reduces as well. The RHBD techniques using commercially viable processes with no changes in process steps have attracted the attention of nowadays' IC designers [58]. Generally, the RHBD uses circuit design measures in order to achieve radiation hardness using standard foundry processes [59]. The resulting design using RHBD techniques have lower cost per chip, making the RHBD technique more cost effective when compared to RHBP techniques. The RHBD technique also provides the designers with flexibility to harden the circuit depending upon the IC circuit functionality.

Triple modular redundancy

The RHBD technique that is widely used the current rad-hard community is the logic-based hardware redundancy and it utilizes a majority voter. One of the known forms of this technique is called the triple modular redundancy (TMR) [60]. Figure 1-15 shows the block diagram of the TMR design.

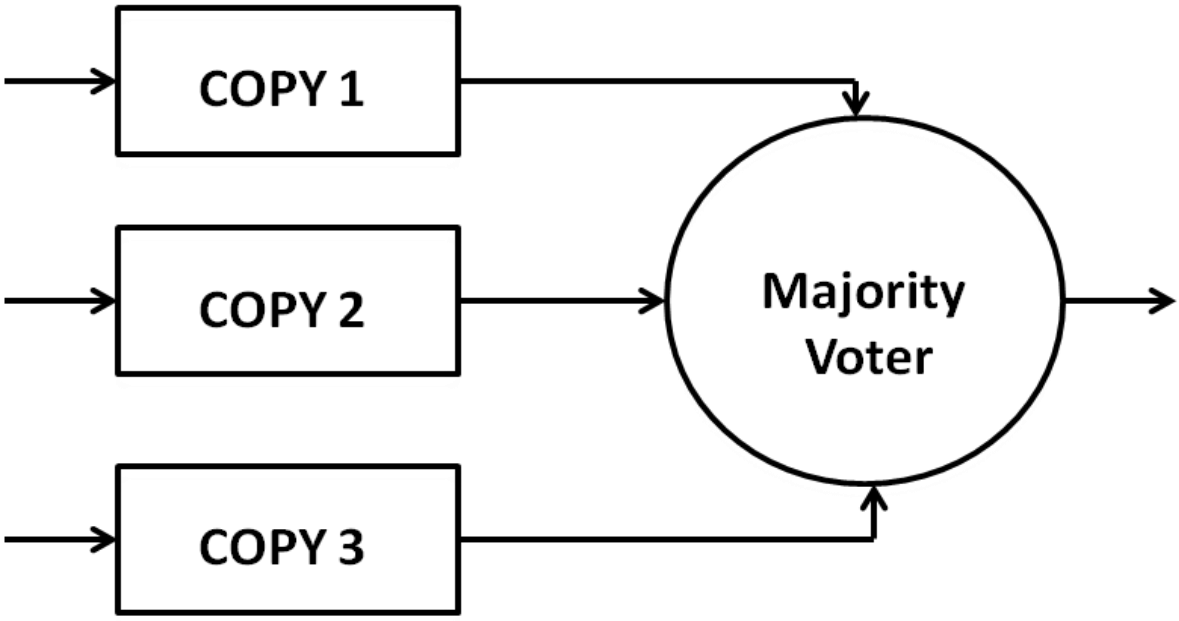


Figure 1-15. The basic structure of the TMR hardening scheme

The TMR technique replicates the designed flip-flop circuit node thrice and then passes the three copies through a majority voter as shown in Figure 1-15. If even one copy of the node is corrupted by SEU, two copies of the logic will be correct and the final signal observed at the overall output will be correct.

Moreover, although this thesis focuses on single upsets only, it is worth mentioning that multi-bit-upsets (MBU) due to highly energetic particles can cause the TMR technique to fail as two out of three copies may be corrupted and evaluated as an erroneous output. Thus, the redundant copies have to be spatially separated in layout. If two blocks are spatially separated by large distances, it is less likely to upset multiple copies of the same logic and the output will be correct. In order to utilize area efficiently, most designers prefer interleaving multiple cells in layout while designing TMR circuits [61].

Temporal hardening

Temporal hardening is another radiation hardening technique used to mitigate radiation-induced SEUs [62]. As its name implies it, this hardening scheme is time based. For temporal hardening approach, the output of a sensitive node is delayed using delay elements and sampled at different clock time intervals for performance consistency. The propagation delay of the delayed element must be greater than measured SEU so that the observed delay time surpasses the induced SEU lifetime. Figure 1-16 shows a circuit diagram of the aforementioned temporal hardening technique.

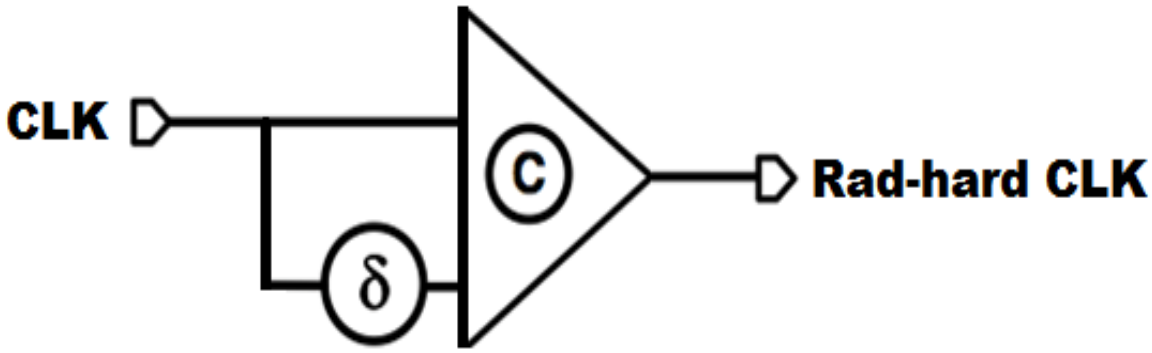


Figure 1-16. Temporal hardening using the delay element and Muller-C

Figure 1-16 shows the clock input CLK and its delayed version being fed to the Muller-C element (non-inverting). The Muller-C element inverts the output of the hardened node if both the inputs to the temporal hardening circuitry are the same. However, if one of the inputs does not match the other, the output node goes into a tri-state mode. If a SEU due to a highly energetic particle strike makes both inputs of the Muller-C mismatch, the IC circuit keeps its previous output value. This Muller-C element serves as a hardening structure, since the output cannot be

incorrect unless both the input nodes to the Muller-C circuit get hit simultaneously. If the Muller-C element is present at the CLK input of the flip-flop, then data has to be hold stable for at least δ time. Unfortunately, this temporal hardening element limits the maximum frequency of the circuit by increasing the delay time. Thus, the temporal hardening is not the best technique to mitigate SEUs in high-speed IC designs.

Dual Interlocked Cell (DICE) latch

With this type of hardening technique, the designer embeds the RHBD latch into the building blocks of the IC circuit that needs to be radiation-hardened. The dual interlocked storage cell (DICE) latch is the most widely used technique of this kind. An example of how the DICE technique can reinforce the SEU immunity of memory circuits is found in [63].

Using the DICE circuit from Calin et al.'s paper [63] as shown in Figure 1-17, one can notice that the DICE latch has four storage nodes labeled X0-X3 and four cross-coupled networks identified as P1 and N0, P2 and N1, P3 and N2, P0 and N3. The storage nodes store two pairs of complementary value (i.e. 1010 and 0101).

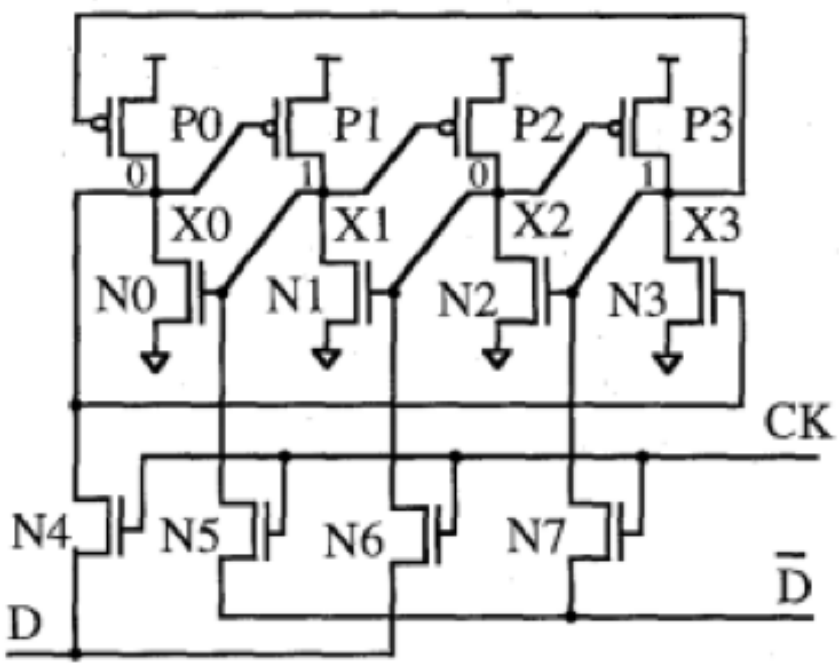


Figure 1-17. The basic DICE latch circuit [63]

It is also worth noting that all the four storage nodes can be accessed through four separate access transistors, with pairs connected to the same input D and $\overline{D}$. The DICE structure relies on "dual node feedback control" to achieve SEU immunity. As a result, each of the four storage nodes is controlled by the two adjacent nodes located in the diagonal. For example, a highly energetic particle strike on a single node cannot disturb the latched value in a flip-flop circuit using the DICE-based hardening technique since the DICE has quadruple storage nodes connected in a cross-coupled configuration. This is realized with four cross-coupled inverters as shown in Figure 1-17. In addition, the feedback to each of the dual redundant storage nodes is from a previous node. However, the NMOS and PMOS gate driving successive storage nodes do not form the same nodes, thus two of the storage nodes must have their logical states reversed to upset the cell.

1.4.2 Selective node hardening technique

Since prior hardening techniques introduce higher circuit area overhead (i.e., TMR and DICE latch) and longer propagation delay (temporal hardening technique), selective node hardening (SNH) is proposed in this thesis and will be largely discussed in Chapter 3. The proposed SNH technique can also be categorized as a RHBD technique. The SNH uses devise resizing approach to increase the channel width of certain PMOS transistors which are closer to any identified sensitive node. The increased PMOS width W_p is coupled with an increase in node capacitance and drive strength. Thus, the SNH method makes the Qcrit required to upset the node higher than it is in non-hardened circuit, thereby making the IC circuit less vulnerable to radiation-induced SEUs.

1.5 Summary of this thesis

With the continuing technology downscaling, it is imperative that new SEU analysis techniques be developed in order to increase the resilience of storage elements against potential SEU effects. The design and optimization of highly reliable deep submicron microprocessors depend on the accurate SEU analysis approaches. The analysis of the impact of SEUs on ASICs for memory applications is an extremely widespread field so it is impractical to cover its entire space. The research work presented in this thesis will focus on SEU analysis methods for sensitive nodes within both static and dynamic logic registers; more specifically this thesis will explore SEU effects in D flip-flops, which are the basic building blocks of registers.

1.5.1 Motivation and contributions

As CMOS technology continues to scale down, the semiconductor industry is benefitting the ever-increasing capability of integrating more and more devices on a single die. Meanwhile, single-event upset (SEU) effects are becoming more prominent, causing significant performance and reliability degradations of registers at deep submicron or even nanoscale technology node. It is imperative to improve SEU analysis techniques in order to better mitigate the expected SEU effects as transistor feature sizes continue to shrink.

The existing SEU analyses for static CMOS flip-flops focus on the circuit-level impact [36-38] and may underestimate the pertinent SEU information provided through node analysis. This thesis proposes a node analysis approach to evaluate the SEU sensitivity of static flip-flops and apply the obtained node sensitivity information to improve the resilience of the flip-flop circuits through selective node hardening (SNH) technique. Unlike previous hardening techniques such as the Triple Modular Redundancy (TMR) and the Dual Interlocked Cell (DICE), the SNH does not introduce a larger area overhead.

The proposed SEU analysis approach provides the ability to (1) properly identify critical SEU sensitive nodes of the flip-flop circuit, (2) characterize their sensitivity levels, (3) predict and characterize the overall circuit SEU reliability, and (4) increase the robustness of the flip-flop circuit through selective node hardening. The proposed node sensitivity analysis will unveil the flip-flop vulnerability to SEUs and provide ample information on the whereabouts of critical locations that need urgent hardening solutions.

Moreover, this thesis also explores the impact of SEUs in dynamic flip-flops, which are more appealing for the design of high-performance microprocessors because of their short latency, small area and high clock frequency. Previous work either uses the approaches for static flip-flops to evaluate SEU effects in dynamic flip-flops or overlook the SEU injected during the precharge phase. In this thesis, possible SEU sensitive nodes in dynamic flip-flops are re-examined and their window of vulnerability (WOV) is extended.

1.5.2 Thesis Outline

The rest of this thesis is organized as follows:

Chapter 2 presents the design description of the SEU current source and the Verilog-A approach to model it. In addition, a systematic method to select sensitive nodes within a flip-flop is described and validate through case-study tests. Moreover, the Cadence AnalogLib switch is used to stabilize the SEU current source and avoid potential convergence problems during the simulation runs. Chapter 3 analyzes the impact of SEUs in static CMOS flip-flop circuits and largely explores node sensitive analysis in order to efficiently mitigate SEU effects through selective node hardening. Chapter 4 uses a slightly different SEU analysis approach to investigate the impact of SEU in dynamic flip-flops. Finally, Chapter 5 summarizes the major contributions of the research works presented in this thesis.

CHAPTER 2

SEU MODELING

In this chapter, the modeling of the SEU current source using Verilog-A is presented and the possibility to instance the SEU current (Verilog-A based current source) into Cadence Virtuoso simulated circuits is discussed. Using the static CMOS D flip-flop (SDFF), an identification method for selecting sensitive storage nodes of the flip-flop is provided. The last part of this chapter addresses issues encountered while using the SEU model in Cadence Virtuoso and solutions undertaken to overcome those issues.

2.1 SEU current source modeling

The SEU current symbol is created using Verilog-A and incorporated into Cadence Virtuoso IC 6.1.5 for later node-level and circuit-level simulation purposes. The double-exponential current source of the form

$$I_{seu}(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \quad (2)$$

is used to model the SEU current at the transistor level or circuit level. In equation (2), Q_{coll} is the charge deposited from a heavy-ion strike; τ_α is the collection time constant or falling time constant because it is responsible for the falling time profile of the SEU current pulse created using the equation (2). In addition, τ_β is the ion-track establishment time constant or rising time constant of the junction and it is associated with the rising time feature of the SEU current pulse. Q_{coll} is proportional to both the particle LET and the effective collection depth L. According to

Mavis and Eaton [9], the deposited charge in silicon is roughly 10 femto-Coulombs (fC) per μm of track length for a particle having an LET of 1 MeV-cm^2/mg. Q_{coll}, τ_α and τ_β depend on several process related properties of the device such as the size of the device, biasing of various circuit nodes, substrate structure, device doping, the type of ion, its energy, its trajectory, the initial position of the event within the device, and the state of the device [27]. However, τ_α and τ_β are usually assumed to have values of 10 ps for the rise time constant (τ_β) and 100ps to 200 ps for the fall time constant (τ_α).

It is worth noting that Verilog-A was used to model the SEU current source since Cadence Virtuoso Analog Design Environment (ADE) does not have a direct way of modeling such a parametric equation (2). Parametric analysis is possible in Cadence Virtuoso, but the unsolved issue is that the Cadence simulation time cannot be linked with the variable time t in the parametric equation (2). Therefore, the SEU current is separately modeled using Verilog-A and later instanced into the test schematic built in Cadence Virtuoso ADE.

Traditionally, electrical circuit designs were all analog. However, with the advent of mixed-signal languages such as Verilog-AMS, a variety of modern IC designs and simulation analyses integrating both digital and analog behaviors have been made possible. The combined mixed-signal description language (Verilog-A or Verilog-AMS) addresses the cross domain issues and provides the designer with a new dimension in modeling, design and simulation capabilities for analog and mixed signal electronic systems such as the SEU effects as described in the parametric equation (2). Step-by-step instructions to generate the SEU current source using Verilog-A and create its symbol in Cadence Virtuoso IC6.1.6 are provided in the Appendix A of

this thesis.

The SEU current symbol created using Cadence Virtuoso is shown in Figure 2-1. The current through the terminal P is referred to as the current source (I_{P0}) of the SEU model and the current through the terminal N is the current sink (I_{NO}) of the same SEU current model. The current source and the current sink of the SEU model have equal magnitudes, but opposite signs.

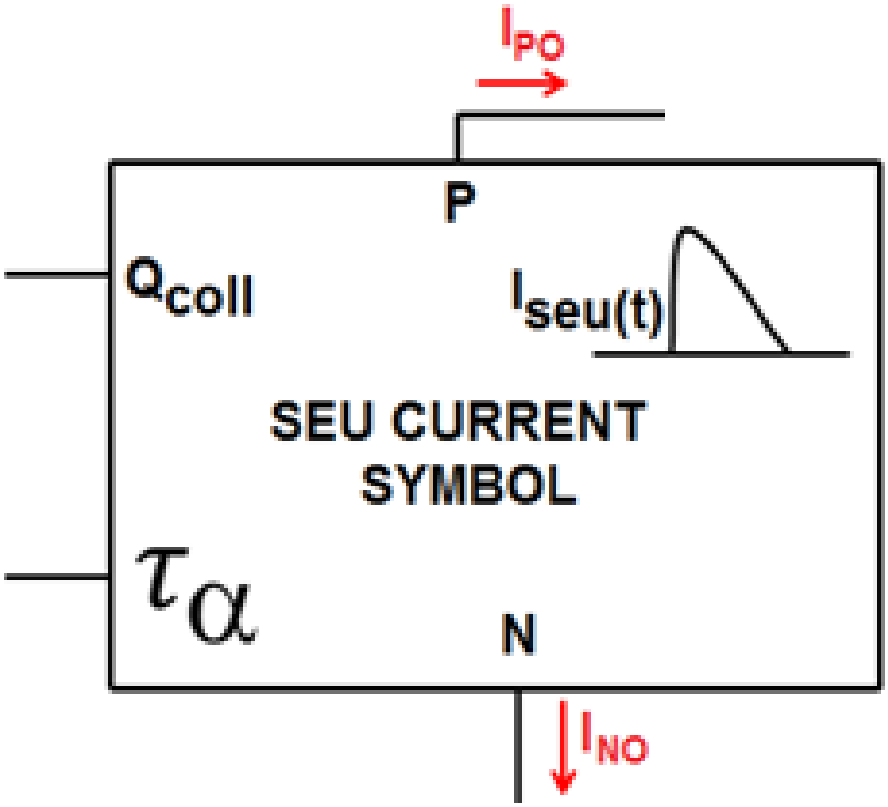


Figure 2-1. SEU current symbol created using Cadence Virtuoso

Figure 2-2 shows an example of the generated SEU current source simulated using the symbol provided in Figure 2-1.

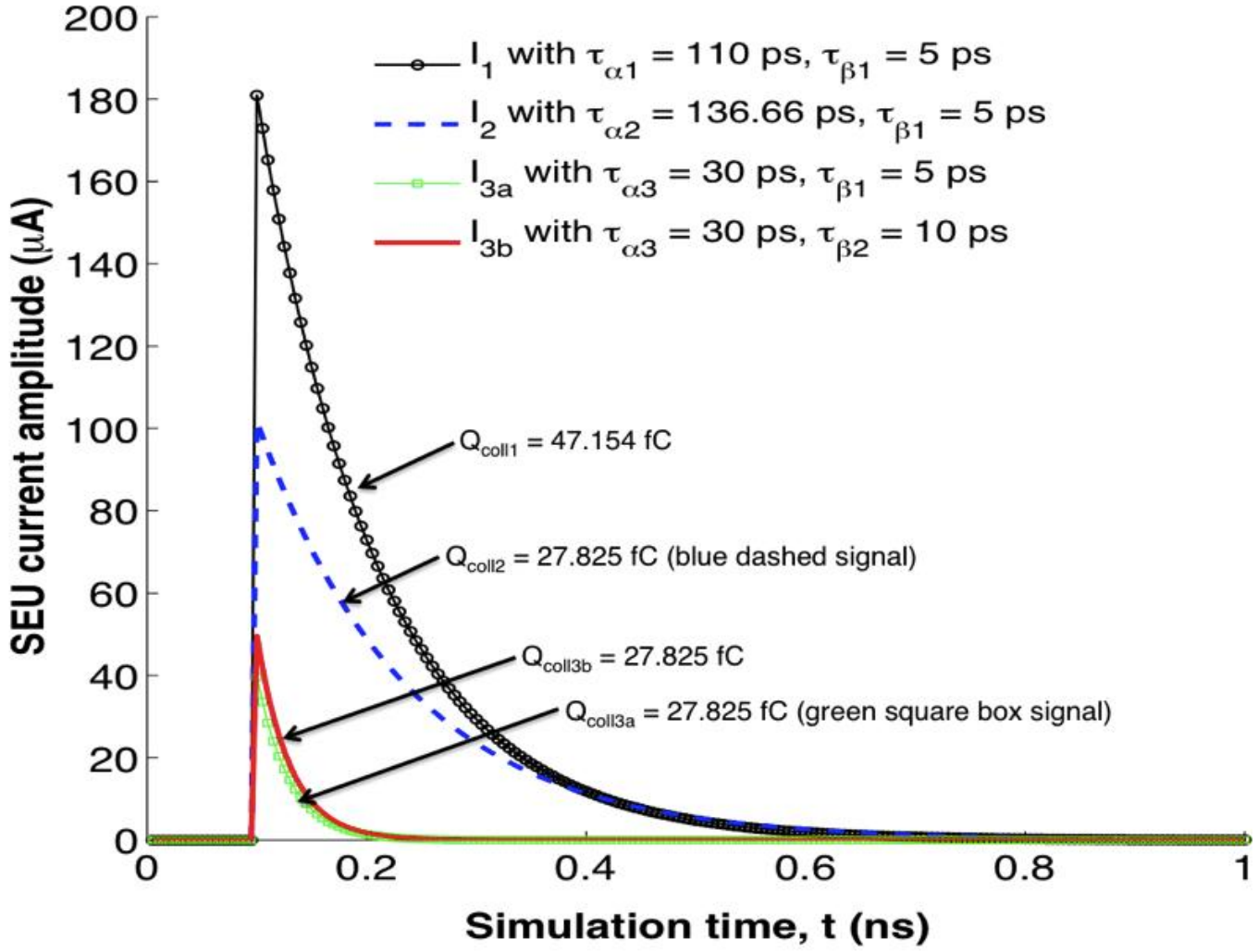


Figure 2-2. Example of a SEU current source

In Figure 2-2, the impact of the variation of τ_{β}, τ_{α} and Q_{coll} on the generated SEU current pulse is illustrated by varying those three parameter. As Q_{coll} increases, the SEU current amplitude increases as well. Also, the SEU current has a steep rising edge due to τ_{β}. In addition, τ_{α} can also be increased (or reduced) in order to widen (or narrow) the SEU current pulse, respectively as shown in Figure 2-2.

2.2 Signal distortion and convergence issues during first simulation tests of $I_{seu}(t)$

The SEU current symbol in Figure 2-1 was tested by injecting it at node N3 of the negative edge-triggered static CMOS D flip-flop (SDFF) shown in Figure 2-3. The reason why the SEU current was applied at N3 is because N3 is sensitive to SEUs. As it will be clearly explained in Chapter 3, storage nodes with feedback loop are the most sensitive regions of a static CMOS D flip-flop. The SEU current injected at N3 was generated using the equation (2) where τ_{β}, τ_{α} and Q_{coll} were set to 5ps, 105.5ps and 30 fC, respectively.

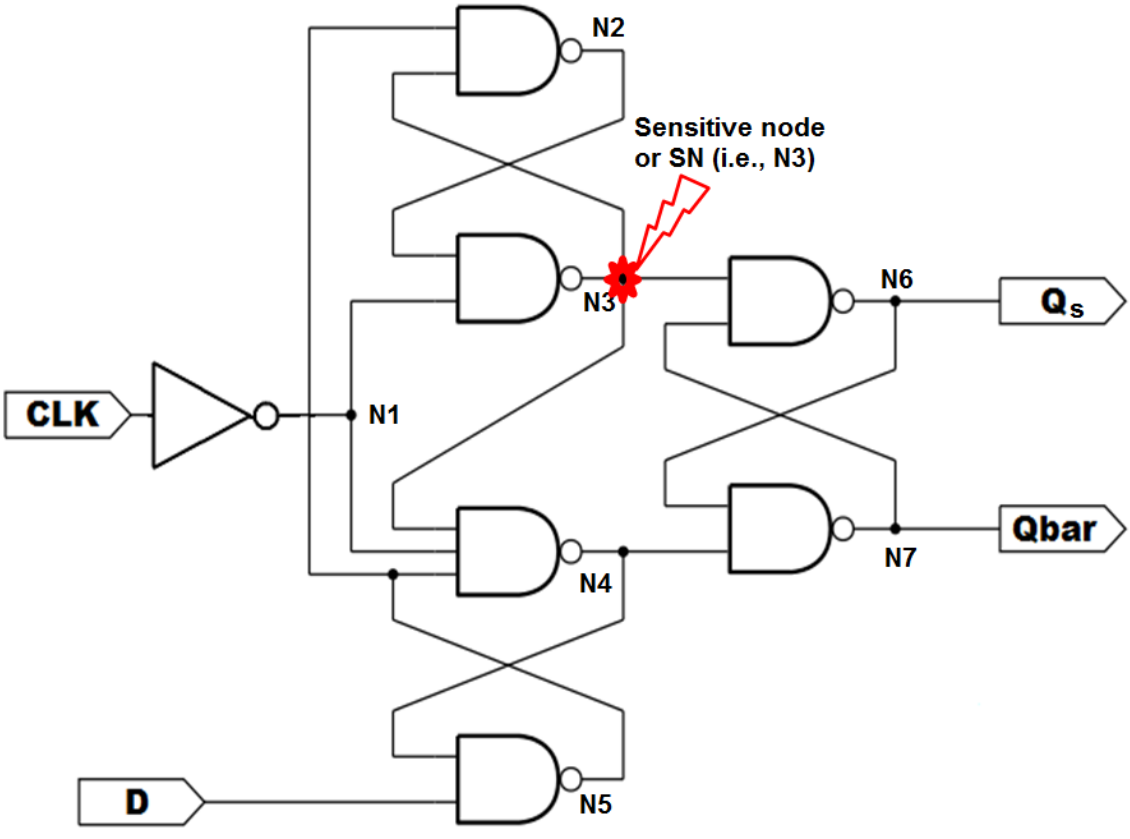


Figure 2-3. SDFF circuit used to test the SEU current source

Figure 2-4 shows the observed simulation results of the SEU current testing using the SDFF circuit. The observed error in the Q_s of Figure 2-4 is caused by the induced instability of the non-ideal SEU current source. For a negative edge-triggered D flip-flop, a new data value is stored at the output only at the falling edge of the clock.

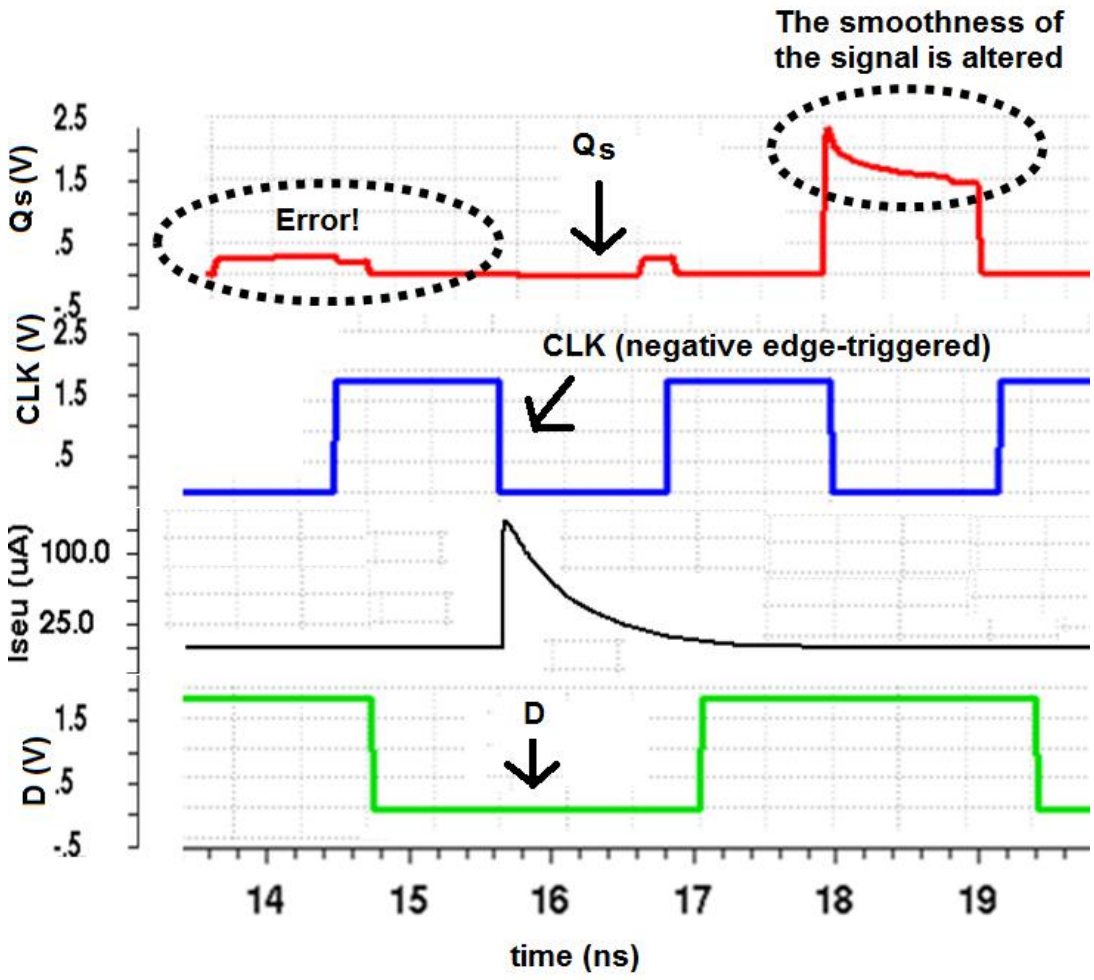


Figure 2-4. Simulation issues due to the non-ideal Verilog-A based SEU current source

The output error (bit flip: 1→ 0) one clock cycle before the injection of the SEU current is unusual. In addition, the smoothness of the flip-flop output signal Q_s appears distorted as opposed to the smooth input signal D as shown in Figure 2-4. The distorted Q_s pulse is due to the

instability of the applied SEU current on the sensitive node N3 (Figure 2-3) since it occurred one clock cycle after the injection of the SEU current. Moreover, the injection of the SEU current during the first simulation tests of the SEU current model also resulted in some random simulation crashes and simulation convergence issues. The unexpected simulation crashes were also believed to be due to the load sensitivity and instability of the SEU current model.

It is also worth mentioning that an ideal current source normally has infinite internal resistance so that changes in load resistance will not affect the current supplied. With an infinite output impedance of an ideal current source, the load's impedance is negligible and the ideal current source stays the same regardless of the type of the load connected to it. Unfortunately, the Verilog-A SEU current source is not ideal and is not immune to external changes of the circuit it is connected to.

2.3 The use of the analogLib switch

Since the use of the Verilog-A based SEU current into Cadence Virtuoso initially resulted in convergence issues and output signal distortion, a solution was needed in order to make the modeled SEU current more reliable and efficient regardless of the load connected to it.

2.3.1 Proposed SEU current model using Verilog-A/analogLib switch symbol

To fix the instability issue and convergence problems of the Verilog-A based SEU current source, the use of Cadence analogLib switch before injecting the SEU current to a

sensitive node is proposed as shown in Figure 2-5. A very large open switch resistance of 1 MΩ was set for the analogLib switch in order to limit the current variation before and after the switch to a very significantly small number.

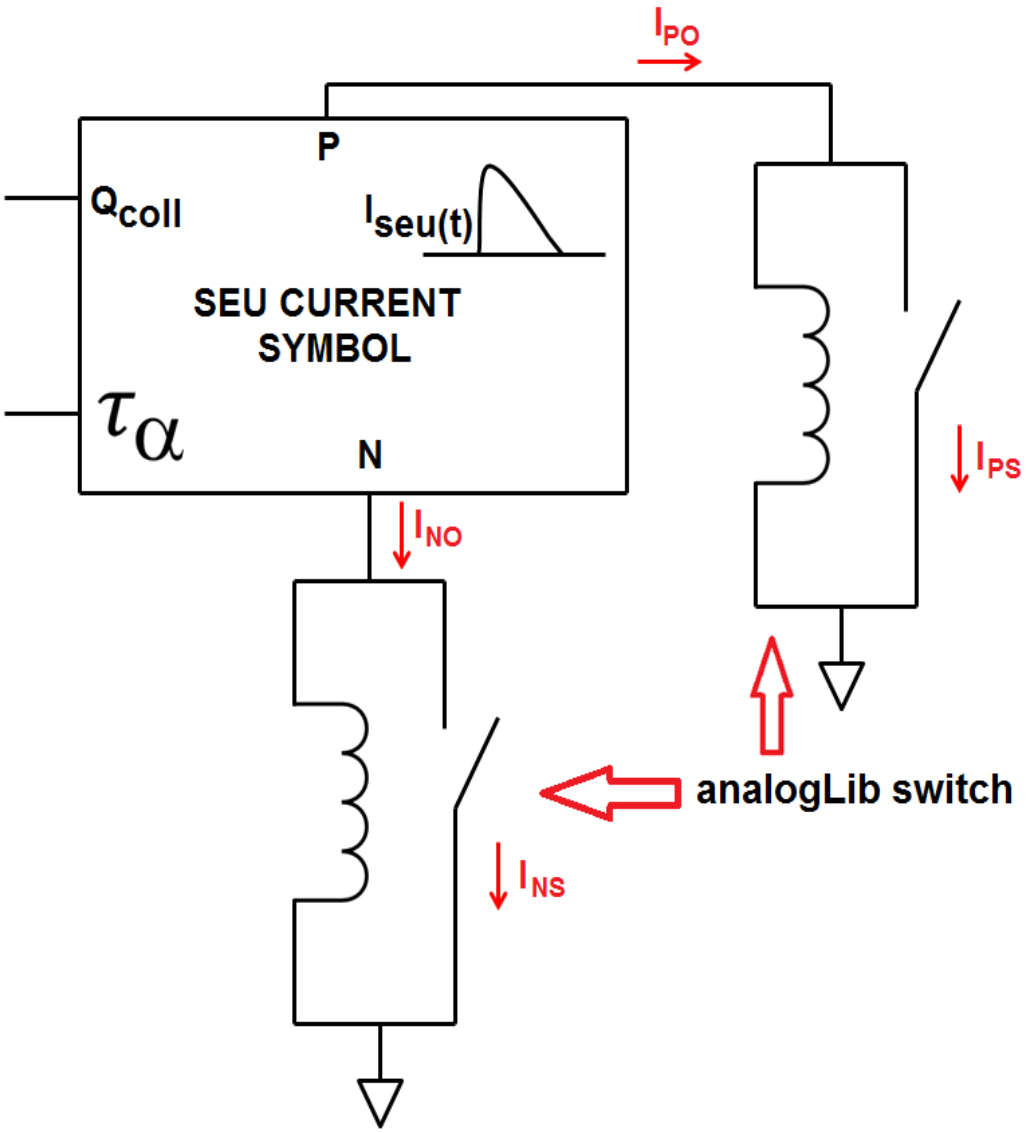


Figure 2-5. The proposed Verilog-A/analogLib switch symbol for SEU current.

The parameters of the analogLib switch in Figure 2-5 are set as follows: open voltage = 0 V; close voltage = 1.8 V; open switch resistance = 1 MΩ; and close switch resistance = 1 Ω. The

analogLib switch has only open and close characteristics of a switch and does not have any inductive property even though it appears to have a misleading coil-like shape on the left side of the switch.

To test the efficiency and consistency of the proposed Verilog-A/analogLib switch SEU symbol, a series of transient simulations on different types of load was performed. The variation in SEU current amplitude due to the augmented SEU current symbol was analyzed. The original SEU currents from the initial Verilog-A SEU model measured before the use of the analogLib switch are denoted as I_{P0} or I_{N0} as shown in Figure 2-5. However, SEU currents measured after using the analogLib switch are referred to as I_{PS} (SEU current source) and I_{NS} (SEU current sink), respectively. Simulation results from the sensitivity analysis of N3 of the SDFF in Figure 2-3) using the injection of I_{PS} (SEU current from the augmented Verilog-A/analogLib switch SEU symbol) are shown in Figure 2-6.

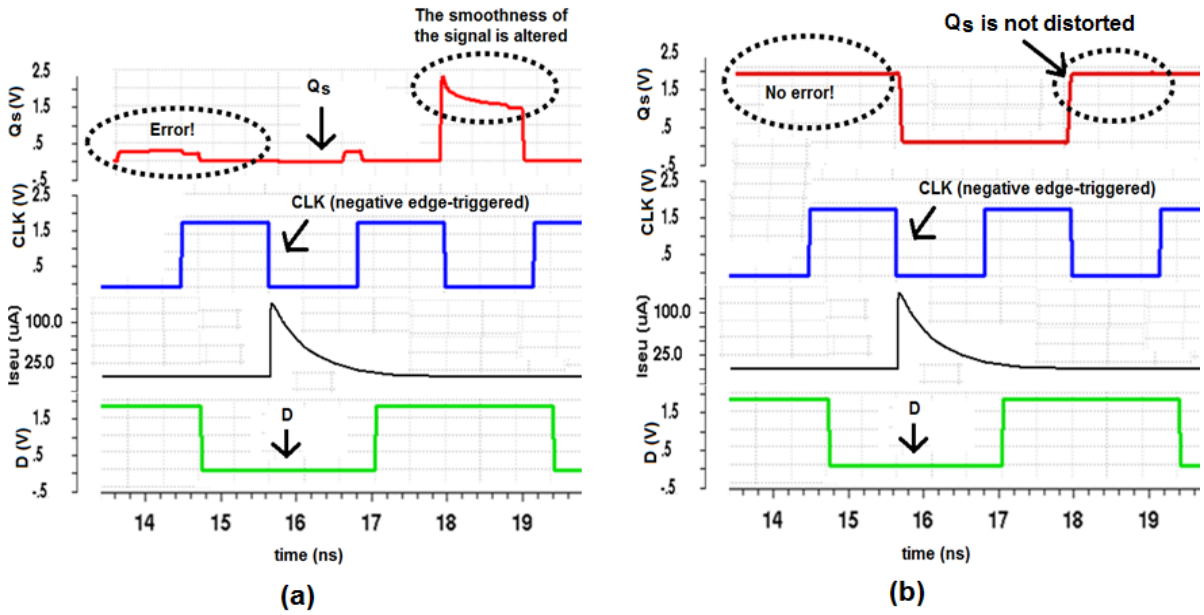


Figure 2-6: Comparison of simulation tests (a) before and (b) after the use of the analogLib switch.

Comparing the output signal Q_s of the SDFF in Figure 2-4 or Figure 2-6 (a) against the output signal Q_s of Figure 2-6 (b), one can see that the simulation issues due to the injection of the non-ideal SEU current on the sensitive node N3 have been resolved by the use of the augmented Verilog-A/analogLib switch SEU current symbol.

2.3.2 Validation test of the Verilog-A/analogLib switch SEU current symbol

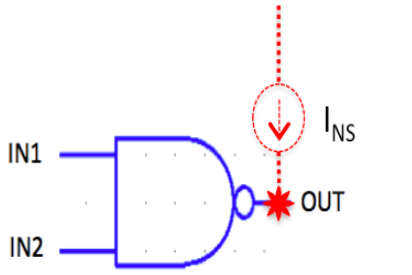
To check whether the SEU current using the Verilog-A/analogLib switch symbol can be reliable and consistent regardless of the load type connected to it, a series of transient simulations with different circuit configurations was performed. Due to the reduced noise margin of the 180nm technology, the average of the difference of the SEU current measured before the use of the analogLib switch and the SEU current measured after the use of the analogLib switch must be less than 1% in order to maintain distinctive logic switch levels from logic "0" to logic "1" and vice-versa. In this thesis, the averaged SEU difference is denoted as Avg (ΔI_{seu}) and must always remain below 1% regardless of the sensitive node and the load circuit configuration. Otherwise, the injection of the SEU current on sensitive nodes of flip-flops can result in an unexpected errors and logic ambiguity as shown in the previous Section 2.2.

In order to validate the reliability and consistency of the Verilog-A/analogLib switch SEU symbol, either I_{PS} or I_{NS} was connected to different logic gates and resistors as shown in Figure 2-7 and Figure 2-8, and the measured peak values of I_{P0}, I_{N0}, I_{PS} and I_{NS} were recorded in Table 2-1 through Table 2-5, respectively.

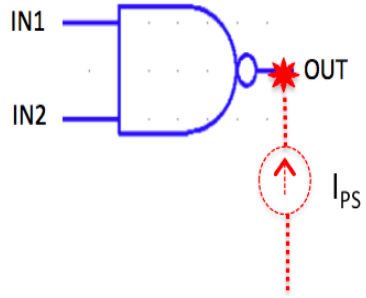
Table 2-1. Nominal (baseline) peak values of the SEU current source with no load connection

	SEU current peaks with no load connection			
	I_{P0} (µA)	**I_{PS} (µA)**	**I_{N0} (µA)**	**I_{NS} (µA)**
Without connection to analogLib switch	244.2	N/A	-244.2	N/A
With connection to analogLib switch	N/A	244.2	N/A	-244.2

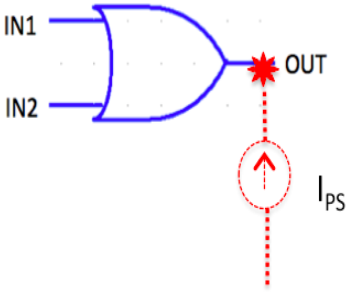
As shown by the tabulated data, the observed magnitude variation in SEU current using the augmented Verilog-A-analogLib switch is significantly smaller and can be neglected. The Avg (ΔI_{seu}) is less than 1% compared with the nominal SEU current peak values in Table 2-1.



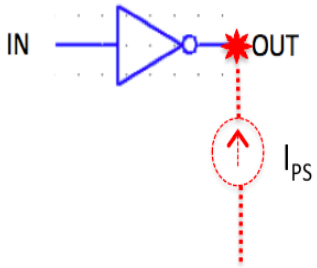
a) I_{NS} injected at output of a two-input NAND gate



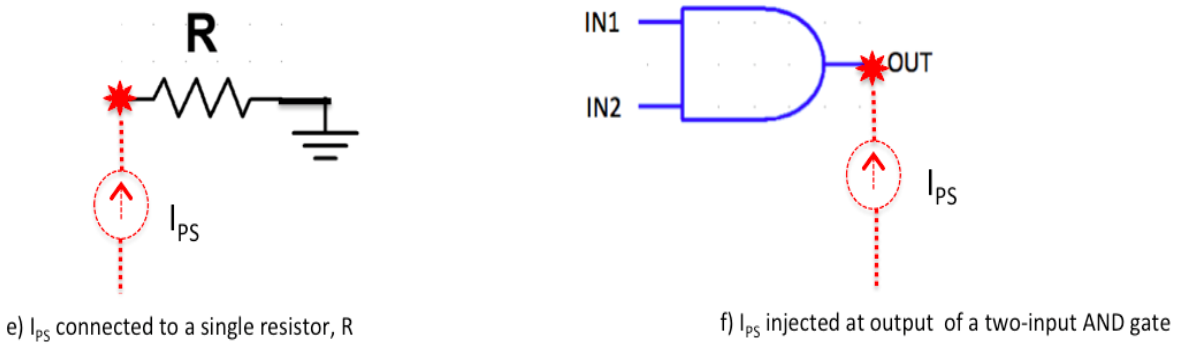
b) I_{PS} injected at output of a two-input NAND gate



C) I_{PS} injected at output of a two-input OR gate



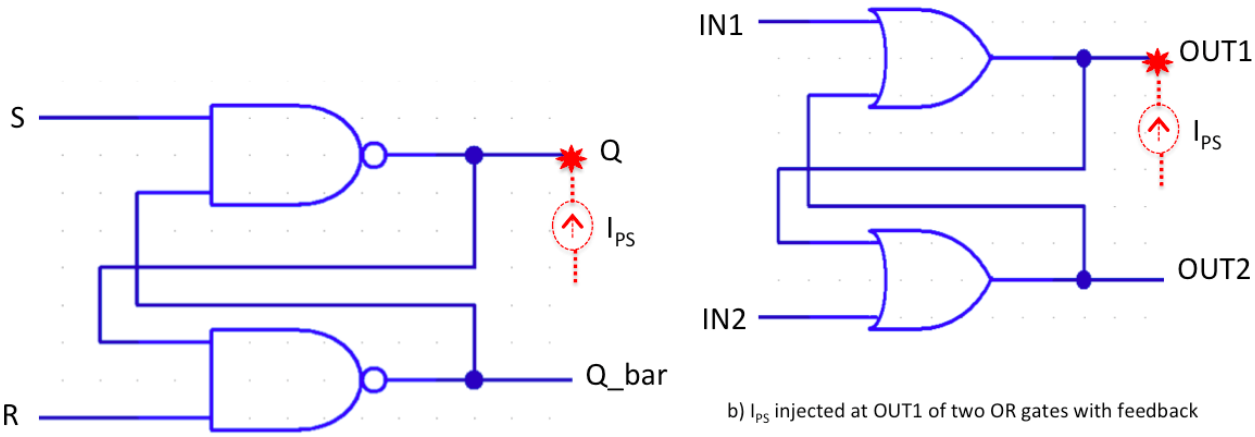
d) I_{PS} injected at output of an inverter



e) I_{PS} connected to a single resistor, R

f) I_{PS} injected at output of a two-input AND gate

Figure 2-7. Simulation setup of the proposed SEU current model with different load circuits



a) I_{PS} injected at Q of an S-R latch

b) I_{PS} injected at OUT1 of two OR gates with feedback

Figure 2-8. Simulation setup of the proposed SEU current model in circuits with feedback loop.

Table 2-2. Comparison of SEU current peak values for single logic gates.

W = same transistor width for NMOS and PMOS and I_{PO} = 244.2 μA.

	I_P (μA	**I_{PS} (μA)**	**Diff = I_{PS} - I_{PO}**	**Diff / I_{PO}**
NAND2 (W = 300nm)	244.3	244.3	0.1	0.00041
NAND2 (W = 400nm)	244.3	244.3	0.1	0.00041
NAND2 (W = 500nm)	244.3	244.3	0.1	0.00041
AND2 (W = 400nm)	244.9	244.9	-0.3	-0.00123
OR2 (W = 400nm)	244.3	244.3	0.1	0.00041
Inverter (W = 400nm)	244.3	244.3	0.1	0.00041
Average	**244.23**	**244.23**	**0.03**	**0.00014**

Table 2-3. Comparison of SEU current peak values for a resistor R with I_{PO} = 244.2 μA

	I_P (μA	**I_{PS} (μA)**	**Diff = I_{PS} - I_{PO}**	**Diff / I_{PO}**
R = 1 Ω	242.6	242.6	-1.6	-0.00655
R = 1KΩ	244.2	244.2	0	0
R = 1 MΩ	244.2	244.2	0	0
Average	**243.7**	**243.7**	**-0.53**	**-0.00218**

Table 2-4. Comparison of SEU current peak values for S-R latch and two OR2-gate circuit with feedback loop when I_{PO} = 244.2 μA is applied

	I_P (μA	**I_{PS} (μA)**	**Diff = I_{PS} - I_{PO}**	**Diff / I_{PO}**
S-R latch (W = 400nm)	241.5	241.5	-2.7	-0.01106
Two OR2-gate circuit (W = 400nm)	244.3	244.3	0.1	0.00041
Average	**242.9**	**242.9**	**-1.3**	**-0.00532**

Table 2-5. Comparison of SEU current peak values for the SDFF with I_{PO} = 244.2 μA

	I_P (μA	**I_{PS} (μA)**	**Diff = I_{PS} - I_{PO}**	**Diff / I_{PO}**
I_{PS} injected at SN1, D = 1 at the falling clock edge	244.3	244.3	0.1	0.00041
I_{PS} injected at SN2, D = 1 at the falling clock edge	244.2	244.2	0	0
I_{PS} injected at SN1 and I_{NS} at SN2 when D = 1 at the falling clock edge	244.3	244.3	0.1	0.00041
I_{PS} injected at SN1, D = 0 at the falling clock edge	244.3	244.5	0.3	0.00123
I_{PS} injected at SN2, D = 0 at the falling clock edge	244.3	244.5	0.3	0.00123
I_{PS} injected at SN1 and I_{NS} at SN2 when D = 0 at the falling clock edge	242.3	242.3	-1.9	-0.00778
Average	**243.90**	**244.02**	**-0.18**	**-0.00075**

Overall, the validation test results of the augmented Verilog-A/analogLib switch SEU symbol indicate that the Avg (ΔI_{seu}) is less than 1% regardless of the type of the load connected to it. Therefore, the variation of the modeled non-ideal SEU current is minimal and can be neglected in subsequent simulation analyses of this thesis.

CHAPTER 3

NODE SENSITIVITY ANALYSIS IN STATIC CMOS FLIP-FLOPS

3.1 Introduction

Single-event upsets (SEUs) in modern VLSI registers pose a major reliability concern. These upsets originate from two primary sources: highly-energetic cosmic ray particles occurring in the space environment and alpha particles emitted from the radioactive decay of uranium and thorium impurities located within the chip itself such as the silicon die, interconnects and ceramic packaging. Soft errors due to SEUs have been a known problem affecting semiconductor memories for quite some time and continue to be serious reliability threat for digital circuits [31].

Although the increasing integration density in modern digital ICs has permitted fast and complex computational capabilities of registers, the shrinking transistor sizes make storage elements more vulnerable SEUs [31-35]. Since the SEU sensitivity of flip-flop circuits is expected to increase as technology scaling continues, it is important to revisit current SEU analysis approaches in order to efficiently design better flip-flop circuits that are more resilient to SEUs. Current SEU analysis methods for static CMOS flip-flops mainly focus on the circuit-level SEU impact [36-41] and may underestimate the pertinent information of the SEU effect on the individual sensitive nodes. This thesis provides a node sensitivity analysis for static CMOS flip-flops. Since the D flip-flop constitutes the basic building block of any sequential circuits including registers, the CMOS D flip-flop (SDFF) shown in Figure 3-1 can used for SEU simulation tests. The SDFF circuit comprises two S-R latches and the S-R latch structure whose

storage nodes have a feedback loop is more vulnerable to SEUs.

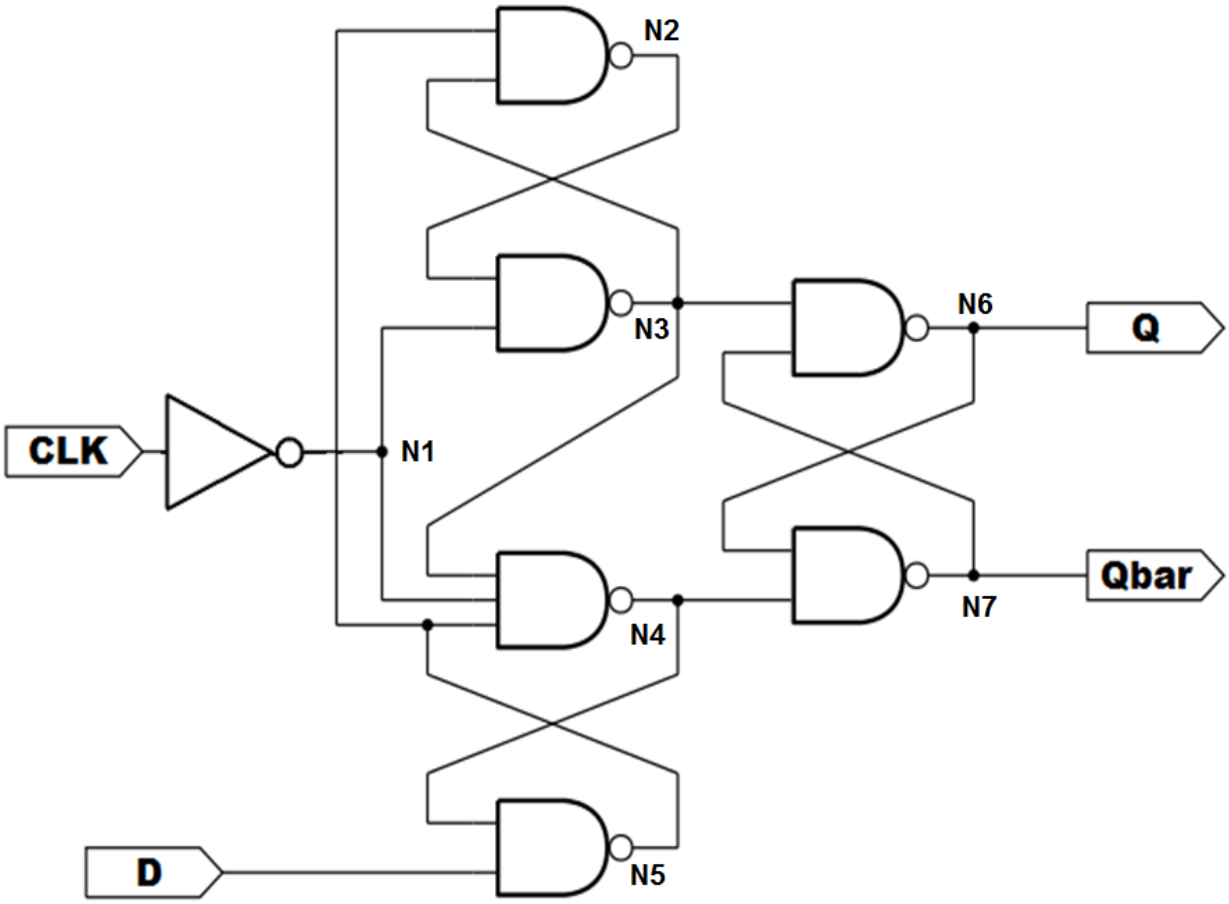


Figure 3-1. SDFF circuit.

The main contributions of this Chapter 3 include (1) the proposed systematic approach for identifying sensitive nodes of the SDFF, (2) SEU sensitivity node analysis approach and (3) the application of node analysis information for selective node hardening (SNH) technique which is cost-efficient without sacrificing the performance of the circuit under test. The SEU rate of a static CMOS flip-flop can be decreased by reducing the sensitivity of highly sensitive nodes in the SDFF circuit. One of the proposed techniques to reduce the node sensitivity to SEU is the selective node hardening (SNH). The SNH technique is based on the transistor scaling of the

logic gates associated with the sensitive nodes. Unlike other hardening techniques (i.e., TMR, DICE, etc.) which are coupled with large area overhead and more propagation delays, the proposed selective node hardening does not result in a large area overhead because it only targets the PMOS channel widths W_p of the logic gates closely connected to the more vulnerable node.

3.2 Sensitive node selection method

SEU current modeling at the circuit-level is usually done via the injection of a current source at a sensitive node. The amount of the SEU impact on a sensitive node also depends on the charge collection dynamics. SEU effects are caused by the interaction of ionizing particles with a semiconductor device. The passing of highly energetic particles (neutrons or alpha particles) through a semiconductor device deposits charge per unit length, which can be expressed as a linear-energy-transfer (LET) on the ion. LET is the average energy needed to create an electron-hole pair for a material. For example, 1 pC of charge per micron length is needed for the creation of an ion track and localized ionization along the track of the ion can result in the generation of sufficient charge to change the state of an internal node [30].

The sensitivity of any node to SEUs is usually determined by measuring the critical charge Q_{crit}, which is the minimal collection charge Q_{coll} needed to erroneously flip the output signal of a sensitive node. The SDFF circuit shown in Figure 3-2 is utilized to illustrate node sensitivity analysis procedure. In Figure 3-2, the sensitivity of the SDFF is determined by injecting the SEU current at the storage nodes with feedback loop.

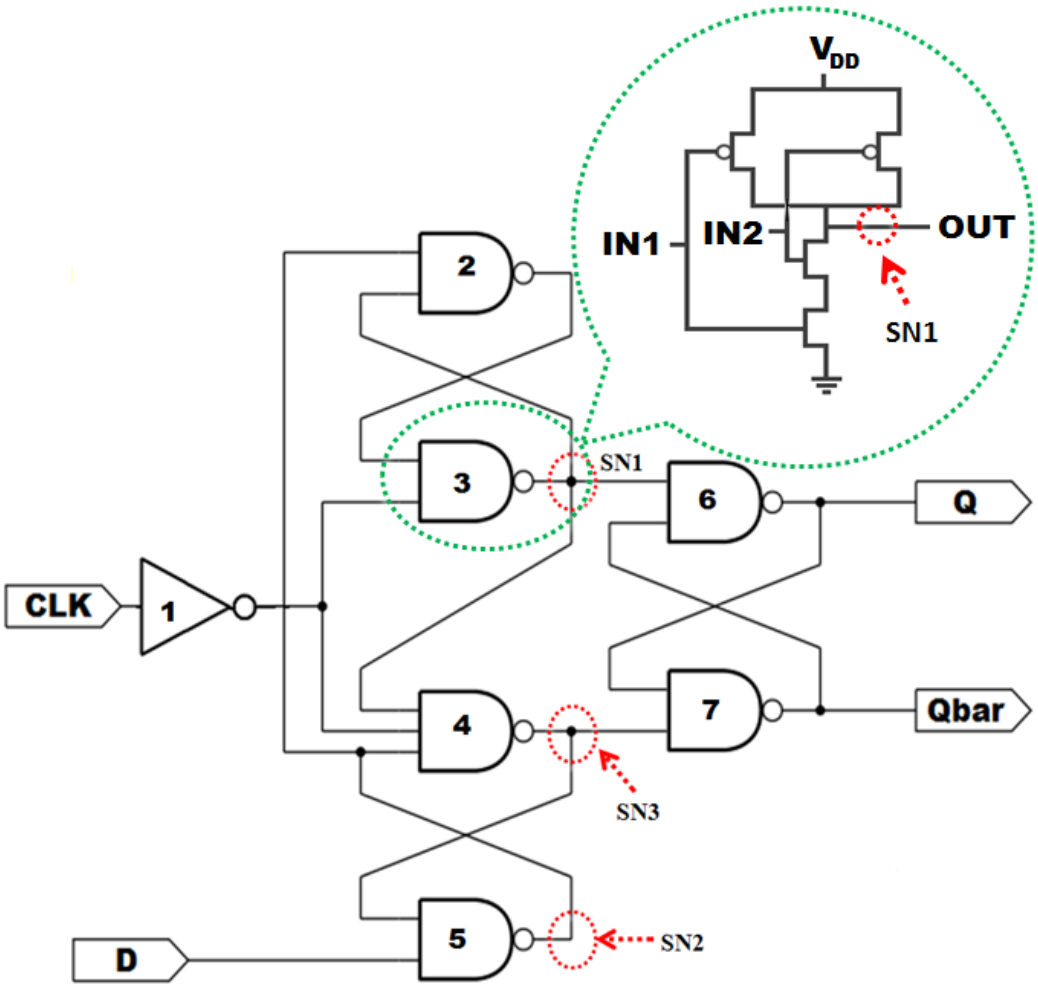


Figure 3-2. SDFF circuit and its sensitive nodes (SNs)

Parametric transient analysis on each storage node is done by varying Q_{coll} and τ_{α} values with 10,000 simulation sweeping steps as shown in Figure 3-3. Since the rising time of the SEU current due to τ_{β} is very steep and does not seem to change very often, τ_{β} is fixed to a constant value of 5 ps in all simulation analyses.

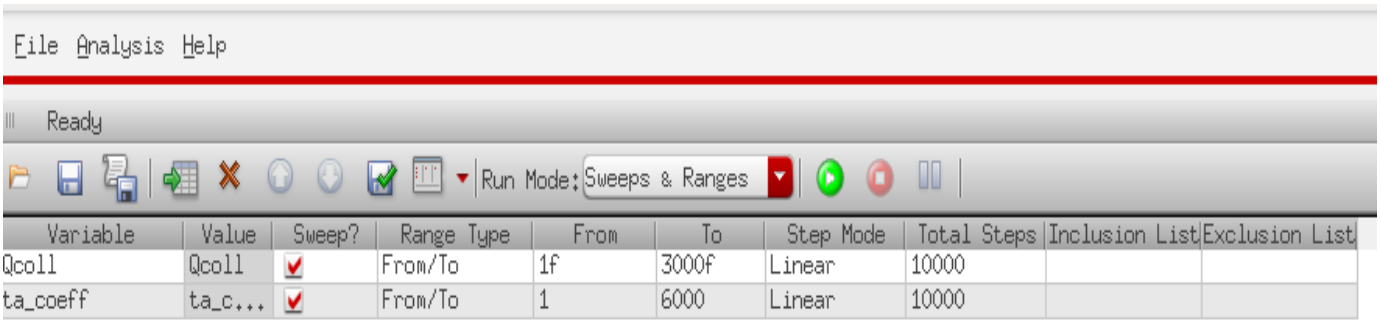


Figure 3-3. Simulation setup for parametric transient analysis

The node sensitivity analysis through parametric transient analysis shows that the minimum SEU current needed to flip a valid output Q from Low-to-High is 244.3 μA for the sensitive node (SN) labeled # 1 or SN1. Similarly, parametric simulations on the remaining storage nodes of the SDFF indicate that two more sensitive storage nodes exist within the SDFF circuit. Overall, three storage nodes were found sensitive to SEUs. The three nodes are denoted as sensitive node 1 or "SN1", sensitive node 2 or "SN2" and "sensitive node 3 or "SN3" as shown in Figure 3-2. Throughout this thesis, the acronyms SN1, SN2 and SN3 will be used for the sensitive node 1, 2, and 3, respectively. The order of their sensitivity to SEU injection is SN1 > SN2 > SN3

In addition, it is important to note that the last two NAND logic gates of the SDFF in Figure 3-2 form an S-R Latch. Inputs to this S-R latch are SN1 and SN3 and they are symmetric to each other. The symmetry between SN1 and SN3 plays an important role in their sensitivity to SEU. This symmetry also explains why the amount of SEU current needed to flip a valid output into an erroneous signal is different for each of the SN1 and SN2.

3.3 Node sensitivity analysis

When a highly-energetic particle strikes a sensitive node of a sequential circuit, it can potentially generate a charge sufficiently enough to create electron-hole pairs which can diffuse towards the device contacts. The collected charge can result in a transient voltage glitch at the node of impact. If the resulting transient causes a bit flip at both the sensitive node and the overall output of the sequential circuit, a single-event upset (SEU) has occurred within the sequential circuit. The impact of SEU on the circuit whose sensitive node has been stricken by the highly-energetic particle depends on many factors including the voltage supply and the total capacitance at the struck node. The minimum charge required to upset a sensitive node is called its critical charge Q_{crit} and has been approximated as the product of the supply voltage, V_{DD} and the total capacitance, C_i of the given sensitive node as described in equation (3).

$$Q_{crit} \approx C_i \times V_{DD} \qquad (3)$$

The approximation of the critical charge in equation (3) has been used in other studies [9, 42-44]. As the capacitance at a given storage node increases for a given supply voltage, the critical charge will also increase. The understanding of the implication of the equation (3) on the SEU node and hardening techniques is very important. In this 3rd chapter, transistor width up-sizing concept is exploited for selective node hardening purposes. For example, the drive strength of the logic gate close to a sensitive node is increased in order to reinforce the resilience of the sensitive node to SEUs. Increasing the drive strength is equivalent to sizing the transistor for SEU immunity.

To determine whether a SEU has occurred, the sensitive node voltage and the overall output voltage Q of both the circuit under test and the golden circuit are compared. If the output voltages Q's and voltage levels of the sensitive node are equal, no SEU has occurred.

3.4 Impact of selective node hardening on the SEU occurrence

Over the past few decades, designers and researchers of high-speed microprocessors have been using technology scaling as a way to increase computation capability and minimize the propagation delay, power consumption and chip area. More recently, however, transistor sizing has started to be re-examined as an option for enhancing reliability [45]. In this section, the channel widths of the PMOS transistors (W_p) in logic gates close to sensitive nodes were upsized as a means to increase the SEU resilience of the circuit. In this work, the transistor length for all NMOS and PMOS is fixed to 180nm ($L=L_{min}$). Setting the channel length of the NMOS and PMOS transistors to the minimum (i.e., $L_{MOS}=L_{PMOS} = L_{min}$) has been routinely adopted by rad-hard designers [34].

Moreover, the channel width W_p is varied parametrically and the critical channel width for PMOS transistor is recorded. The critical PMOS width $W_{p,\ min}$ is defined as the minimum PMOS channel width associated with the occurrence of an upset at the overall output of the flip-flop circuit. As the channel width W_p increases, the node capacitance and the drive strength of the corresponding logic gate increase as well. The total capacitance of any transistor network is larger with a parallel connection (CMOS PMOS configuration) than in a series connection (CMOS NMOS configuration). Thus, the up-scaling of PMOS W_p in the logic gate connected to

a sensitive node is a reasonable option for reinforcing the drive strength of the gate, thereby increasing its robustness to SEUs. A higher capacitance translates to a higher critical charge.

Figure 3-4 is used to further illustrate this scenario. In this case, the SEU current is injected at SN1 (t_inj =15ns, D =0, τ_α = 600 ps, Q_{coll} = 84.69fC). The parameter W_p represents the up-scaled width of the PMOS transistors of logic gate # 3 (NAND2) in tested SDFF circuit. As depicted in Figure 3-4, the structure of the logic gate influences the performance and reliability of a circuit. With transistor width W_{p1}=500nm, the SDFF's reliability through SN1 is threatened and the overall output Q becomes erroneous. However, through selective node hardening by increasing W_p to 520.4nm, the SEU effect is completely mitigated without having a larger area overhead.

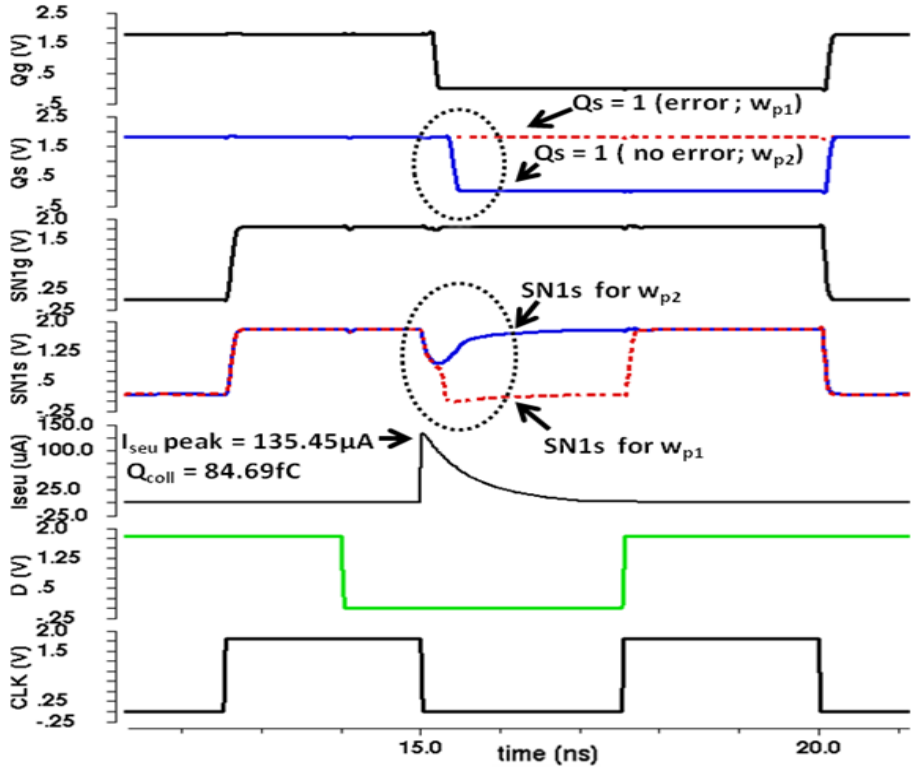


Figure 3-4. The impact of transistor sizing on SEU occurrence. W_{p1} = 500nm and W_{p2}=520.4 nm.

In addition, the impact of the critical charge Q_{crit} on the minimum PMOS width W_P required for selective node hardening was analyzed as shown in Figure 3-5.

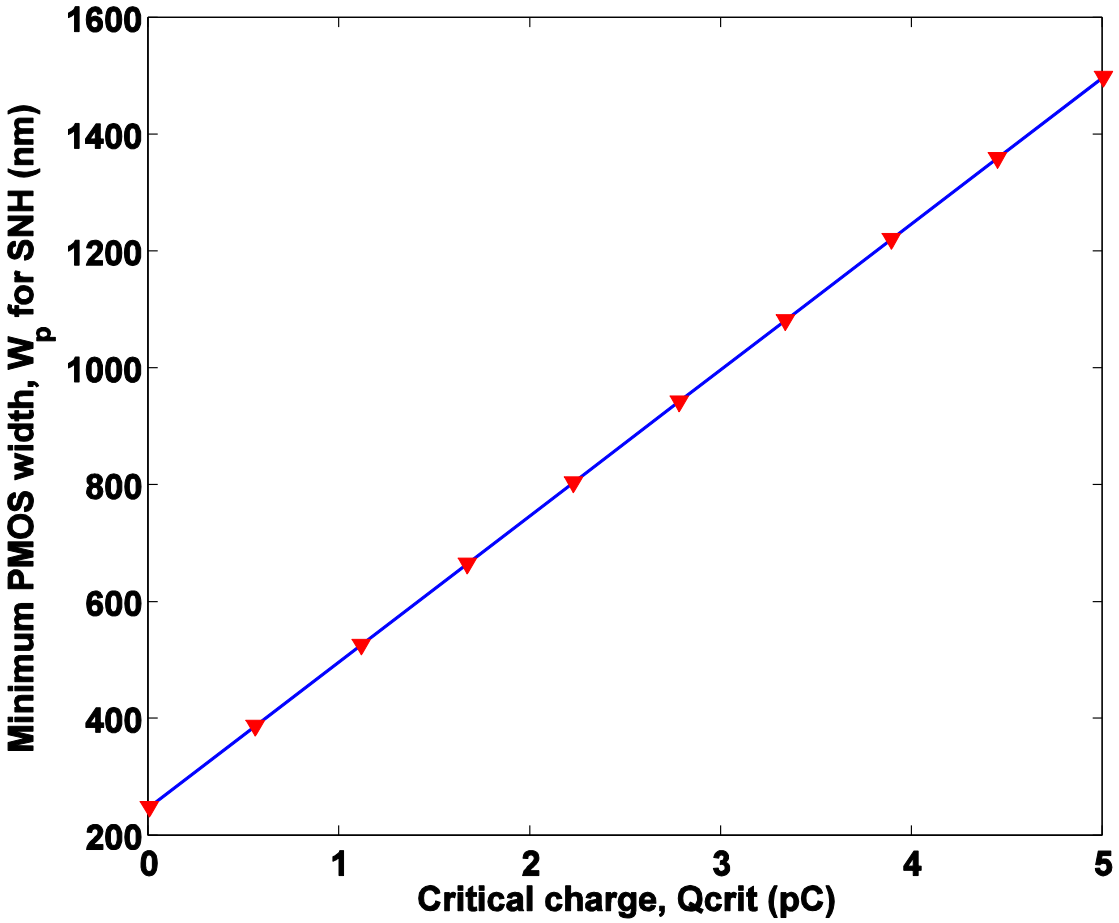


Figure 3-5. The impact of PMOS sizing on critical charge, Q_{crit} (for selective node hardening of SN1 when D = 0).

As shown in Figure 3-5, there is a linear dependency of the Qcrit on the upsized W_p for selective node hardening. A similar linear trend of transistor sizing on critical charges was

obtained in [85-87]. In order to easily compare the simulation results of this thesis against the results obtained by Zhou and Mohanram [85, 86], the relationship between the minimum SNH PMOS ration W_p/L and the critical charges Q_{crit} was plotted in Figure 3-6. It is important to note that the technology used in this thesis analysis was fixed to 180 nm as opposed to the varied technology in the compared previous studies [85-87].

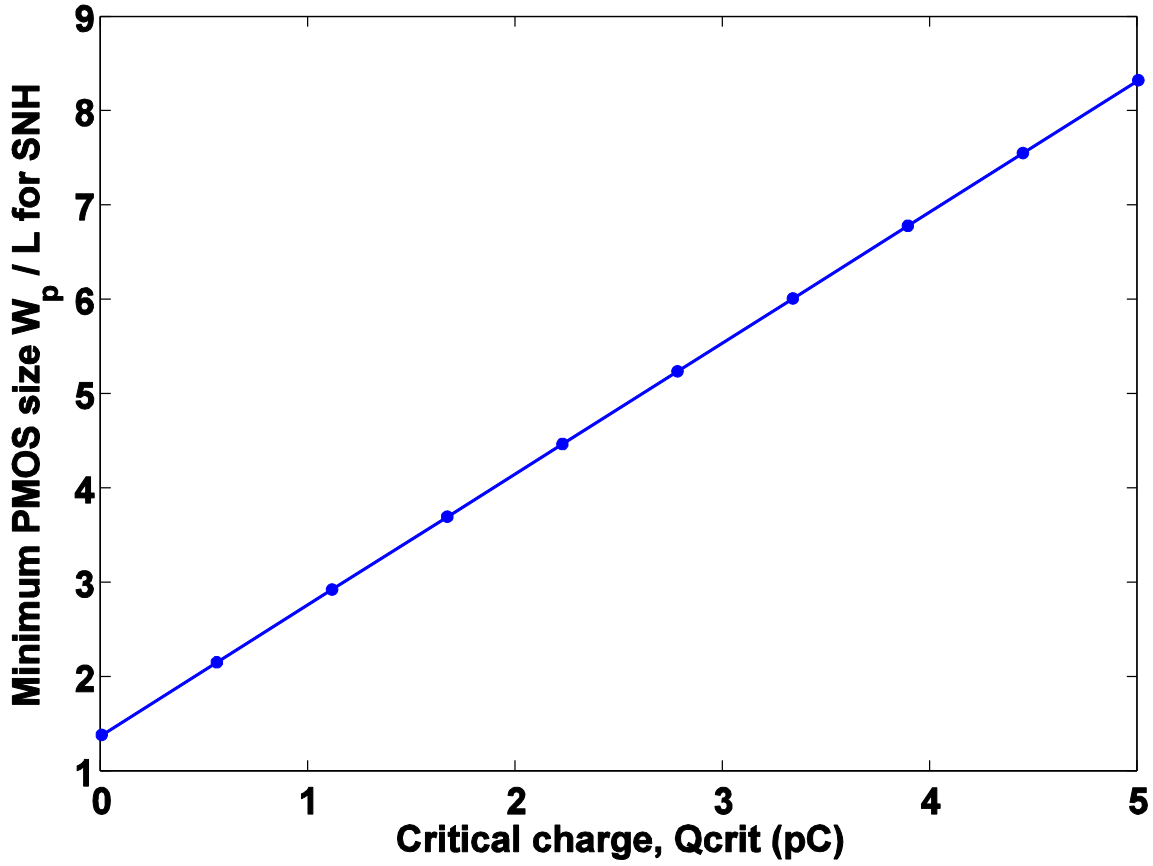


Figure 3-6. The effect of PMOS ratio W_p/L on critical charge, Q_{crit} (for selective node hardening of SN1 when D = 0).

Similarly to previous studies in [85-86], the impact of critical charge on the scaled transistor ration W_p/L has a linear relationship. The implications of this trend indicate that the critical charge Q_{crit} depends much more on the strength of the gate driving the sensitive node of a

memory circuit and should be accounted for in order to reinforce the SEU resilience of the analyzed memory element. However, further physical chip measurements are proposed as part of the future work in order to investigate whether the linear dependency observed using circuit-level simulations holds true when real high energy particles induce single-event upsets in a memory element.

3.5 Simulation results

A. Simulation setup

In this section, the simulation setup is briefly described. The clock period T_{CLK} of 5ns with 50% pulse duration was used in all SEU simulation analyses for the static CMOS D flip-flop. The tested SDFF was built using a 180 nm CMOS process from IBM. The transistor channel length L = 180nm was kept constant in all simulation analyses of this thesis. Initially, the same transistor width of 500nm was used for both PMOS (W_p) and NMOS (W_n) transistors. Then, the PMOS width W_p of certain logic gates (logic gate #3, 4 and 5) was varied from W_p = 250 nm to W_p = 1500nm in order to study how technology scaling reinforce or decreases the SEU impact on the flip-flop circuit.

C. Impact of critical charges on SEU occurrence

Critical charges play an important role in assessing whether a SEU event has occurred. Figure 3-7 and Figure 3-8 show how the critical charge determines the sensitivity of storage

nodes as well as the overall circuit-sensitivity. Simulation results in Figure 3-7 and Figure 3-8 show the alarming effect of SEU on sensitive storage nodes of the SDFF.

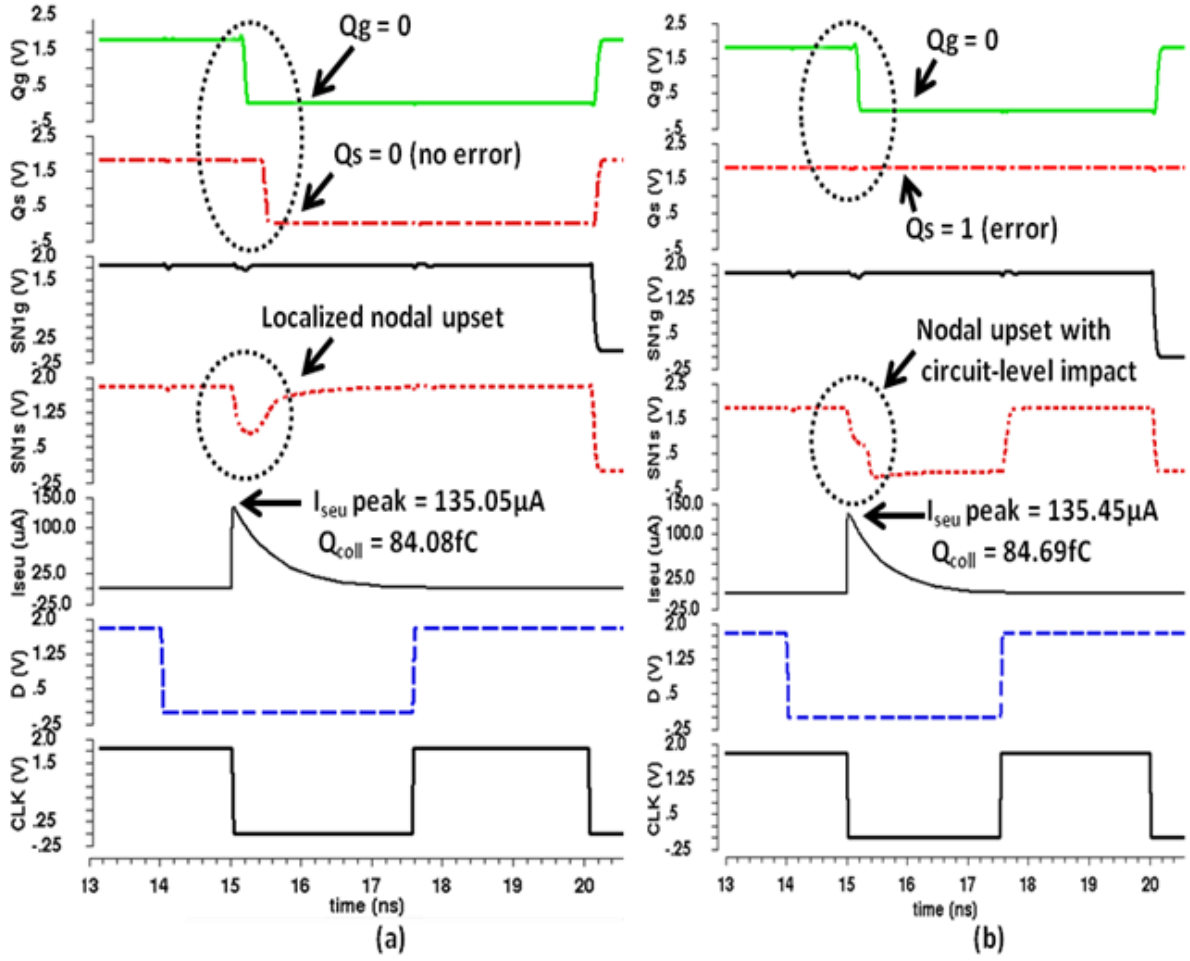


Figure 3-7. The Impact of SEU on SN1 (t_inj =15ns, D =0, τ_α = 600 ps). The collection charge difference of Q_{coll} = 0.61fC (84.69fC – 84.08fC) leads to a circuit-level error. (a)The injected SEU causes a localized transient glitch at the SN1, but does not affect the overall flip-flop output Q. (b)The injected SEU greatly affects both the struck node SN1 and the overall flip-flop output Q (erroneous flip-flop output, Qs).

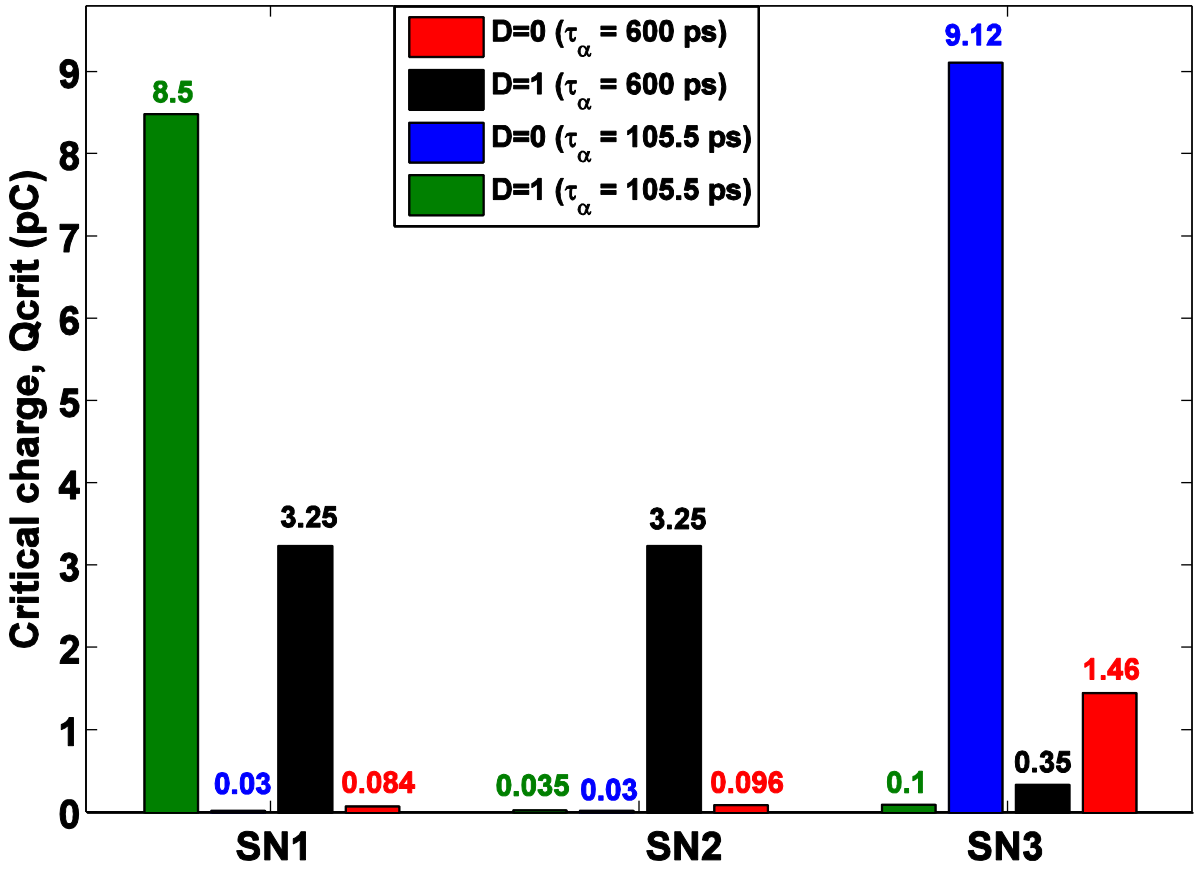


Figure 3-8. Comparison of critical charges, Q_{crit} among sensitive nodes (SN) of the SDFF circuit (The SEU current peak time, t_inj = 15ns for all the three sensitive node test cases).

The understanding of the impact of critical charges on the circuit is very important to the reliability analysis of the circuit. As shown in Figure 3-5, the collection charge difference of only 0.61fC changes the circuit response to SEUs from being resilient state to being more vulnerable to SEUs. In addition, Figure 3-6 shows that sensitive nodes which are upset by lower critical charge are more vulnerable to SEUs than others. The sensitivity level of the SDFF nodes also depends on the input condition of the flip-flop circuit as shown in Figure 3-6.

3.6 Conclusion

Memory devices are ubiquitous in modern consumer electronics and they are prone to soft errors due to the spectacular decrease of device feature sizes. With transistor size shrinking, SEUs in flip-flops pose a challenging threat to IC designers and manufacturers. This 3rd chapter illustrated the vulnerability of static flip-flops to SEUs. Three identified sensitive nodes 1, 2 and 3 of the SDFF displayed different levels of sensitivity to SEU current injection. The simulation results of the SDFF suggest that existing SEU analysis methods in the radiation-induced community be revised and should account for the node analysis information for implementing efficient hardening techniques. The SEU rate of a flip-flop can be reduced by reducing the sensitivity of highly sensitive nodes. One of the proposed techniques to reduce the node sensitivity is selective node hardening which increasing transistor widths of only PMOS devices of the logic gates in proximity with the sensitive node.

CHAPTER 4

EXPLORATION OF SEUs IN DYNAMIC FLIP-FLOP CIRCUITS

4.1 Introduction

The continued reduction of device feature sizes has resulted in significant increase in memory density and also makes nanoscale memory circuits more susceptible to single event upsets (SEUs) [30-31, 46]. However, the analysis of SEU effects in dynamic flip-flops has not been fully explored. Current SEU analysis on dynamic flip-flops either uses methods for static flip-flops or only considers storage nodes with feedback as sensitive to SEUs [47-48]. Unfortunately, the feedback structure is not the only vulnerable portion of dynamic flip-flops. It is imperative to develop a systematic method to promptly identify SEU sensitive nodes in dynamic flip-flops for designers who are interested in high-speed dynamic circuits.

In addition, current hardening techniques mainly reinforce the robustness of the dynamic flip-flop for the evaluation phase, rather than the precharge phase. This tendency to overlook the precharge phase presumably comes from the designer's prior awareness of the error-free precharge region in non-hardened dynamic flip-flops. However, we hypothesize that the effect of high-energy particle strikes happening in the precharge phase may also be propagated to the evaluation phase and thus contributing to the soft errors observed in the evaluation phase. Although current hardening methods are effective for preventing output failure during the evaluation phase, they overlook the effect of particle strikes on the clocked transistor failure. Thus, it is vital to properly re-examine the existing SEU analysis approaches and revisit current

hardening techniques in order to efficiently mitigate SEUs in dynamic flip-flops.

In this paper, a new SEU analysis approach is proposed and complements the existing SEU approaches. The rest of this fourth chapter is organized as follows. Section 4.2 highlights the mechanisms of SEU modeling in dynamic logic flip-flops and the proposed systematic analysis approach. Section 4.3 presents and discusses the simulation results. Finally, the analysis of SEU effects in dynamic logic based flip-flops is concluded in Section 4.4.

4.2 Proposed SEU analysis approach

In this Section 4.2 basic mechanisms of SEU modeling in dynamic logic flip-flops are briefly discussed and the proposed systematic analysis approach is presented. A window of vulnerability (WOV) for both dynamic non-hardened and hardened flip-flops is explained. The response of sensitive nodes, and in general, the response of the overall circuit to SEU injection is described using a test case-study of dynamic flip-flops.

4.2.1 Proposed analysis flowchart

Current SEU methods for either static or dynamic flip-flops only consider storage nodes with feedback structure as sensitive to SEUs [47-51] and overlook the impact of particle strikes on the clocked transistors. This thesis's approach (outlined in Figure 4-1 flowchart) also explores the SEU effects on the drain nodes of clocked transistors in dynamic flip-flops. Throughout this fourth chapter, the non-hardened dynamic D flip-flop is frequently referred to as NHD-DDFF

and the hardened dynamic D flip-flop is abbreviated to HD-DDFF. In addition, P-SN stands for the sensitive drain node of a clocked PMOS transistor while N-SN represents the sensitive drain node of the clocked NMOS transistors. For NHD-DDFF, both P-SN and N-SN of the NHD-DDFF are analyzed because radiation-induced charges on these nodes affect the overall output of the flip-flop. Particle strikes on P-SN or N-SN result in charge losses and charge gains on the two nodes, respectively. For HD-DDFFs, however, a greater focus is given on N-SN nodes because particle strikes on N-SN induce charge losses which may ultimately affect the output of the HD-DDFF. To determine whether a SEU has occurred, the output voltage Q and the sensitive node voltage of both the circuit under test and the golden circuit are compared. If the output voltages Q's and voltage levels of the sensitive node are equal, no SEU has occurred.

The SEU current source I_{seu} (t) is time-dependent and varies exponentially with simulation time. SEU current modeling at either transistor-level or circuit level is usually done via the injection of a current source at a sensitive node. The SEU current source Iseu is modeled in the form of double exponential waveform, as shown in equation (4).

$$I_{seu}(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \qquad (4)$$

where Q_{coll} is the charge deposited from heavy-ion strike, τ_α is the collection time constant or falling time and τ_β is the ion-track establishment time constant or rising time constant of the junction. In all simulation analyses of this thesis, only Q_{coll} and τ_α are varied parametrically. Since the rising time of Iseu (t) is very steep and does not seem to change significantly, τ_β is typically fixed to a constant value [9, 27, and 43] for different technologies. The minimal Q_{coll} capable of causing a bit flip at the output Qs is referred to as the critical charge, Q_{crit} and it is

found by varying Q_{coll} and τ_{α} parametrically.

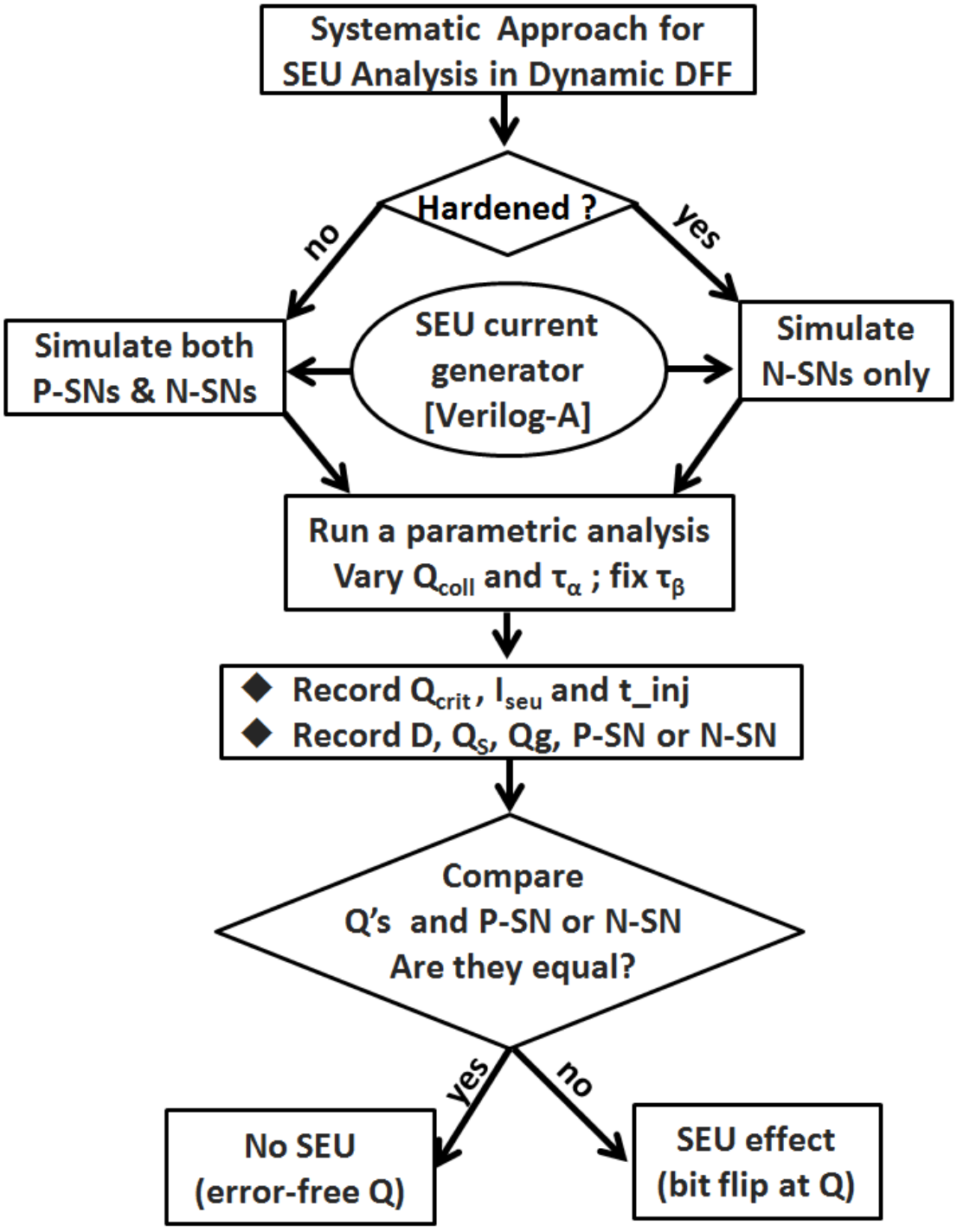


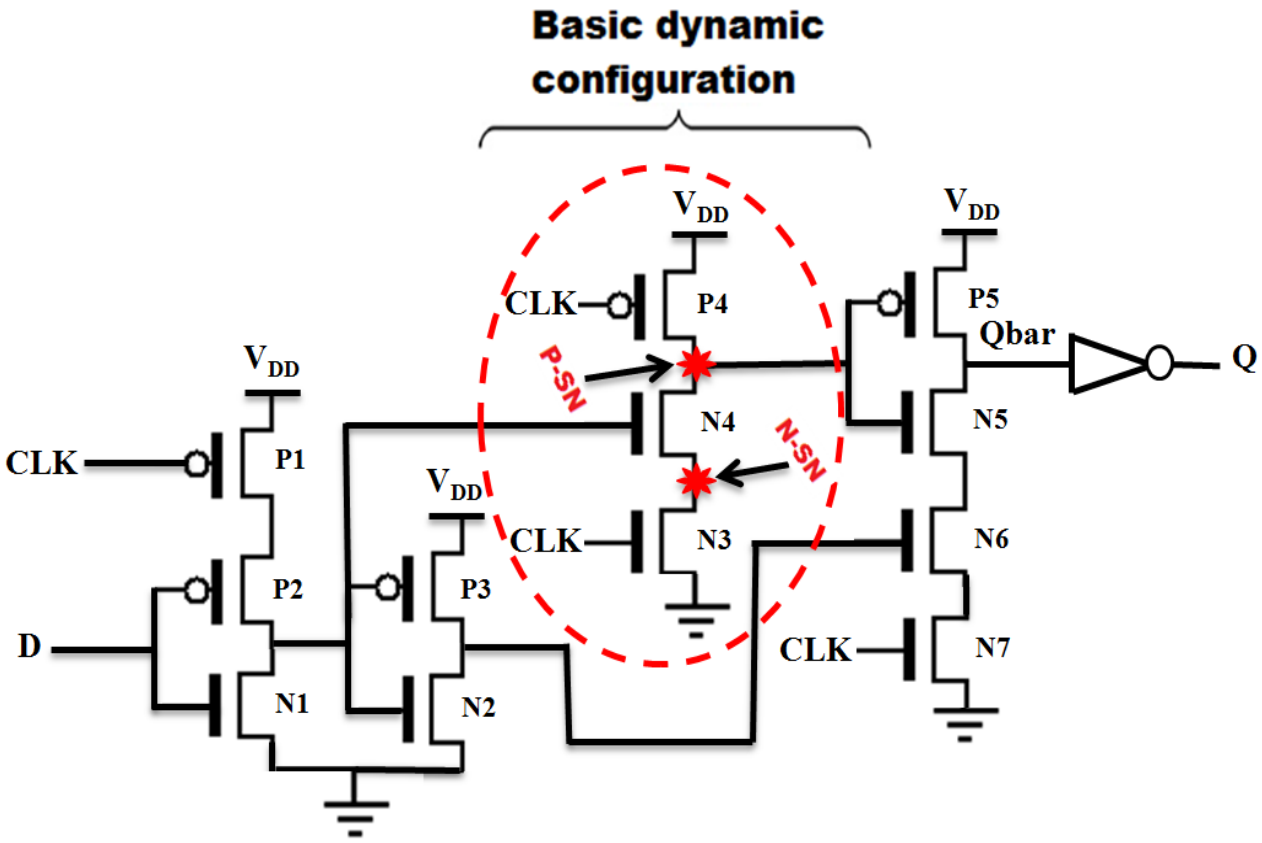
Figure 4-1. Proposed SEU analysis flowchart for dynamic logic flip-flops.

4.2.2 Window of Vulnerability (WOV)

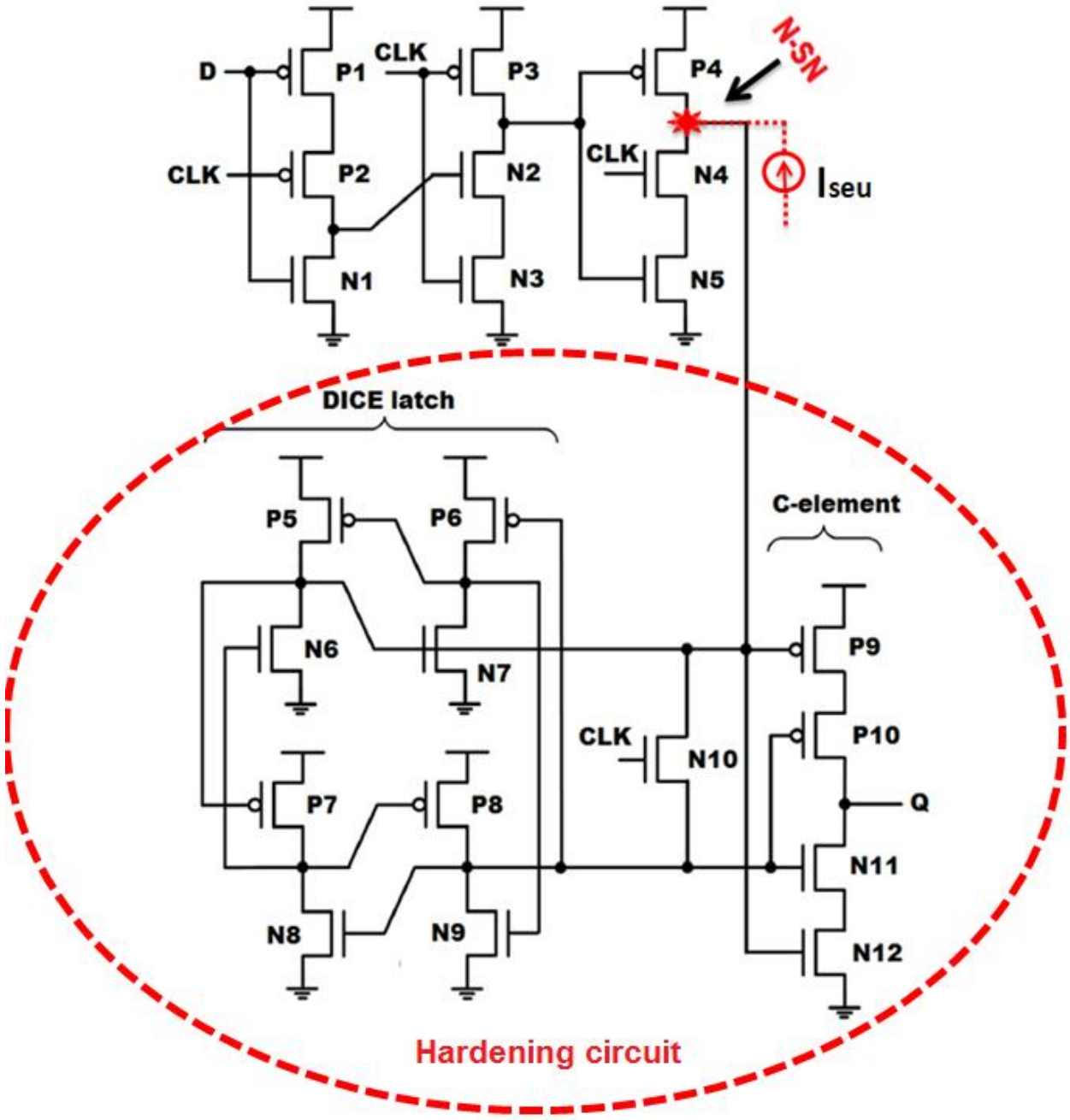
As a key feature of dynamic logic flip-flops, the flip-flop has two operation phases: precharge and evaluation. Different with previous work [47-48, 51, 53-55], this thesis investigates the SEU injected in NHD-DDFs not only at the evaluation phase, but also at the precharge phase. In this section, the analysis on NHD-DDF of Figure 4-2 (a) is used as a case study to zoom in the impact of particle strike timing on the output failure.

Drain nodes of a dynamic logic circuit configuration are normally charged to supply voltage V_{DD} during the precharge phase. However, a particle strike at the P-SN node gives rise to a transient current which affects the overall performance of the dynamic flip-flop. As shown in Figure 4-3(a), if a SEU reaches its peak time (t_inj) at 12.25ns, the P-SN node voltage is pulled up to V_{DD} before the end of the precharge phase. As a result, no SEU effect is observed in the evaluation phase. However, if the SEU current peak is shifted to 12.31ns, the P-SN node results in a SEU because it cannot charge back to V_{DD} before the evaluation phase starts, as shown in Figure 4-3(b). Let us denote tps1 as t_inj of the first SEU event recorded in the precharge phase and TP0 as the starting time of the precharge phase. In equation (5), a SafeTimeRatio is defined as the percentage of the error-free precharge during which P-SN can recover from SEU effect by charging back to V_{DD} through the PMOS device. It is worth noting that 50% clock duty cycle was used in SafeTimeRatio equation (5).

$$SafeTimeRatio = \frac{(tps1 - TP0)}{\left(\frac{1}{2}\right) T_{CLK}} \tag{5}$$


Basic dynamic configuration
V_DD
V_DD
V_DD
V_DD
CLK
P4
P5
Qbar
Q
P-SN
N4
N5
N-SN
CLK
P1
CLK
N3
N6
P2
P3
D
CLK
N7
N1
N2

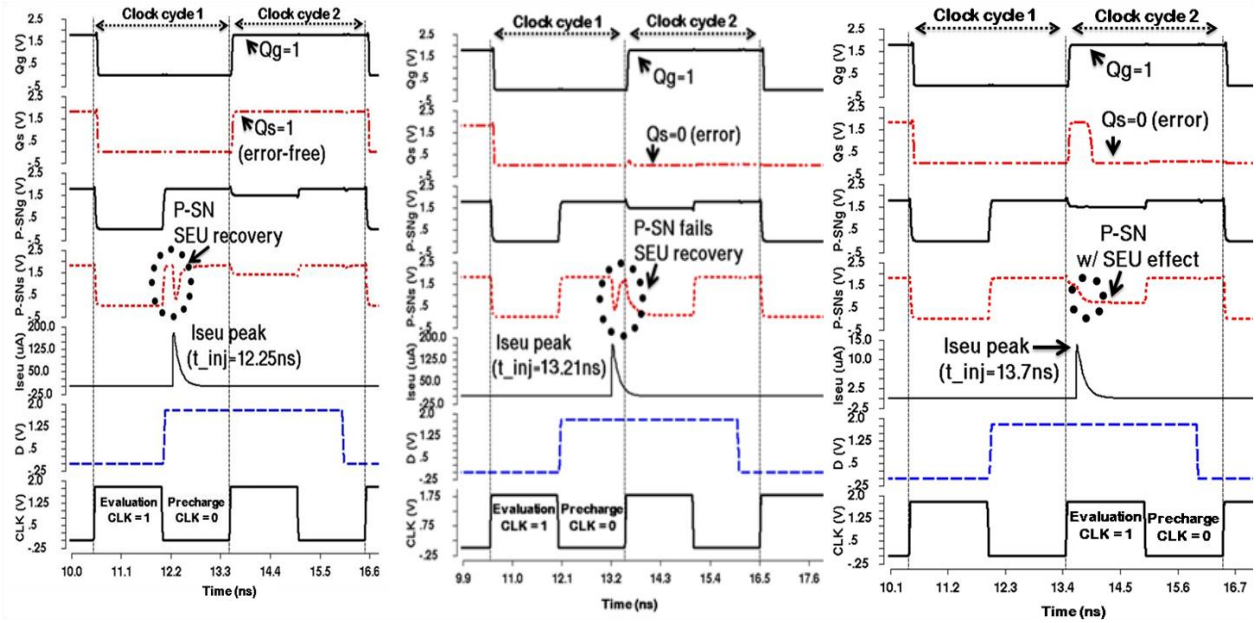
(a)



(b)

Figure 4-2. Analyzed dynamic flip-flops. (a) NHD-DDFF [47] and (b) HD-DDFF [56]. Sensitive drain nodes P-SN and N-SN for NHD-DDFF and only N-SN are highlighted in red.

If a SEU is injected within the range of [TP0, TP0 + (1/2)*T_{CLK}*SafeTimeRatio], no SEU effect will be propagated to the evaluation phase. A SEU occurring in the time window of [TP0 + (1/2)*T_{CLK}*SafeTimeRatio, (1/2)*T_{CLK} + tps1] causes the P-SN node voltage to drop below V_{DD}/2, thus spreading the SEU effect over the precharge-evaluation boundary to cause a sustained bit flip at the output of the flip-flop as shown in Figure 4-3(b). The affected P-SN and the overall output Qs of the NHD-DDFF are not able to fully recover from the SEU impact, thereby leading to an incorrect stored value of logic "0" instead of logic "1".



(a) (b) (c)

Figure 4-3. Simulation analyses for NHD-DDFF (D = 1 and TCLK = 3 ns). (a) P-SN affected by SEU strike recovers from SEU effect during precharge. (b) P-SN unable to recover from SEU during precharge. (c) SEU effect during evaluation.

During the evaluation phase, the drain node of the clocked PMOS in its off-state is more vulnerable to SEUs because there is no active path to V_{DD}. Figure 4-3 (c) shows the charge loss

due to SEU injection at the P-SN node resulting in an overall output error. Thus, the window of vulnerability (WOV) is defined as the simulation time window during which the SEU effect on the sensitive node can potentially result in an output error. This WOV depends on the clock period T_{CLK}, the injection time and the SEU current peak time, t_inj.

4.3. Simulation results

In this section, the simulation procedure for analyzing SEU effects in dynamic flip-flops is briefly described. Simulation results of the fourth chapter are also provided and discussed. In addition, the impact of clock frequency on critical charges is addressed. Since the SEU injection time affects the WOV in dynamic flip-flops, the impact of SEU injection time on upset probability is also presented.

4.3.1 Simulation setup

The SEU analysis on the NHD-DDFF in Figure 4-2 (a) and HD-DDFF of Figure 4-2 (b) is conducted using a 180 nm CMOS technology from IBM. Both flip-flop circuits were built using the same PMOS transistor width, W_n = 500nm and the NMOS transistor width, W_n = 400nm. The clock frequency, f_{CLK} = 333.33 MHz was used in all simulation analyses. The clock frequency was varied only in Section 4.3.2 in order to study the frequency impact on the output failure. Clock frequencies below 180 MHz and those above 1GHz seemed to cause unstable circuit outputs and were not included in the analyses of dynamic flip-flops.

4.3.2 Impact of clock frequency on critical charges.

In this section, τ_α was fixed (τ_α = 25 ps for NHD-DDFF and τ_α = 100 ps for the HD-DDFF) and both Q_{coll} and the clock frequency f_{CLK} were parametrically varied using at least 1,000 simulation sweeping steps. Then, each critical charge and the corresponding frequency associated with every observed SEU event were recorded. This study shows that the SEU sensitivity of non-hardened dynamic flip-flops is independent of the clock frequency as shown in Figure 4-4. However, critical charges for the HD-DDFF alternated between 200fC and 1200fC for 180 MHz $\leq f_{CLK} \leq$ 400 MHz. A constant critical charge of 200fC were recorded for f_{CLK} > 400 MHz, as shown in Figure 4-4.

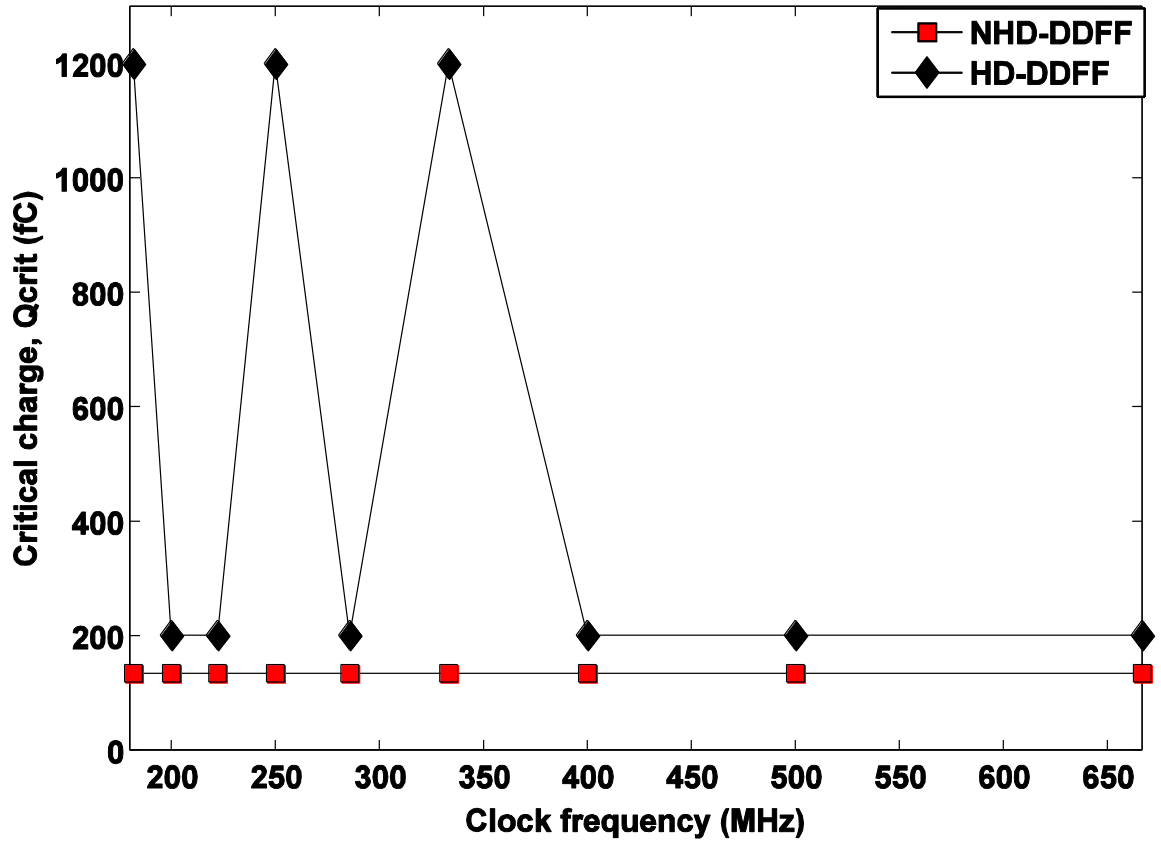


Figure 4-4. Impact of frequency on upset occurrence (D = 0). Diamond-shaped and squared

points represent both SEU events and their corresponding SEU current values.

The higher critical charge of 1200fC in the HD-DDFF for lower frequencies might be due to longer paths that the SEU effect needs to travel in order to reach the output of the flip-flop.

4.3.3 Impact of SEU injection time on upset probability

Using simulation results of the NHD-DDFF, the impact of SEU injection time on the output failure is illustrated in Figure 4-5. Three distinct scenarios characterize the performance of the NHD-DDFF in the presence of particle strikes. Transient faults due to SEUs are harmless to the overall performance of the flip-flop if they occur during the first 44.7 % of the precharge time (calculated by using Equation (5)) of the NHD-DDFF. During this clock time window, the affected drain node has enough time to precharge back to logic “1”. However, the affected P-SN and Q during either the last 55.3% of the precharge time or the entire evaluation phase are not able to recover from SEU because the SEU effect carries over to the evaluation phase, which is a very critical time for the data storage operation of the flip-flop circuit. Furthermore, as shown in Figure 4-6, the HD-DDFF is affected by SEUs only during the precharge time when particle strikes occur at the sensitive node N-SN.

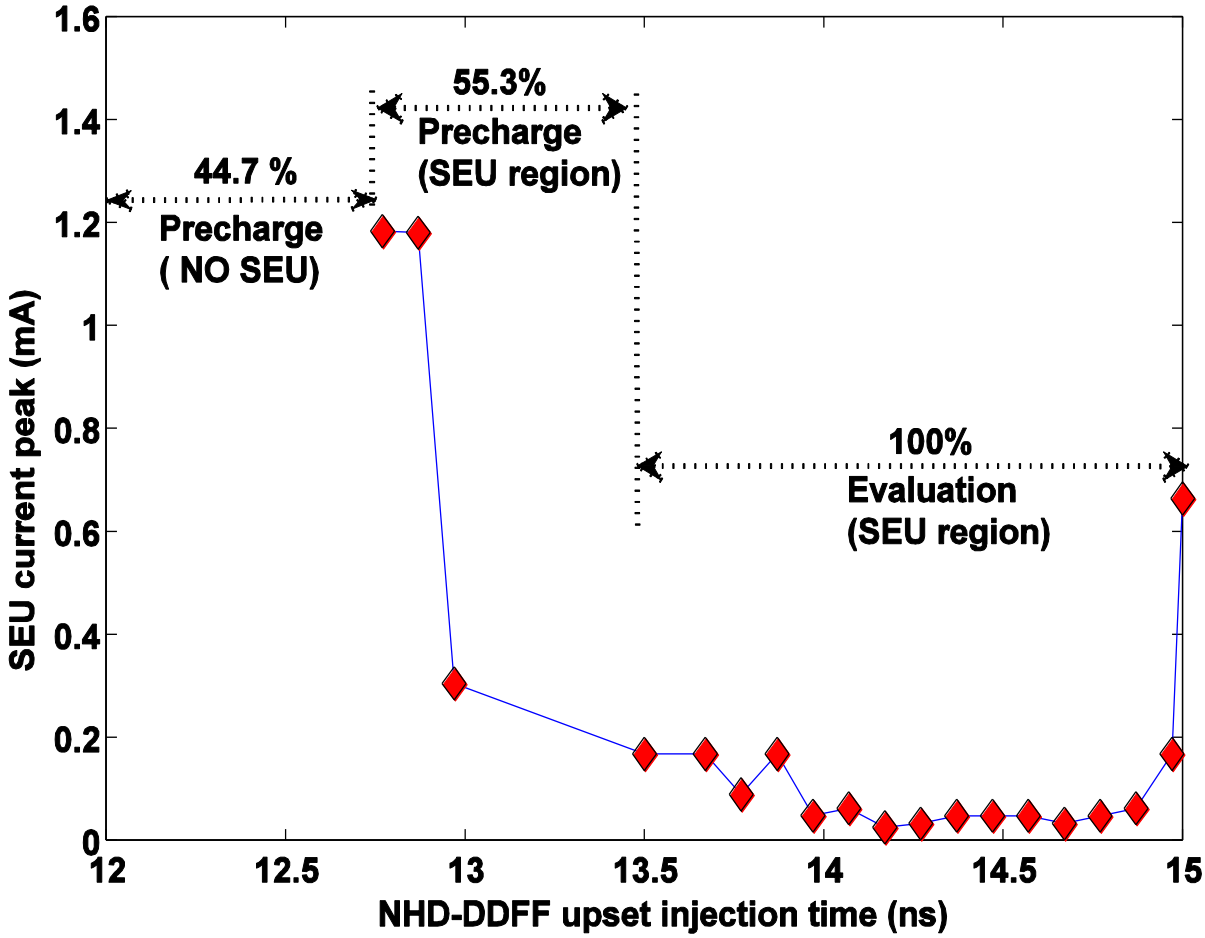


Figure 4-5. Impact of injection time on upset occurrence rate in the NHD-DDFF (SEU injection at P-SN when D=0). Diamond-shaped points represent both SEU events and their corresponding SEU current values.

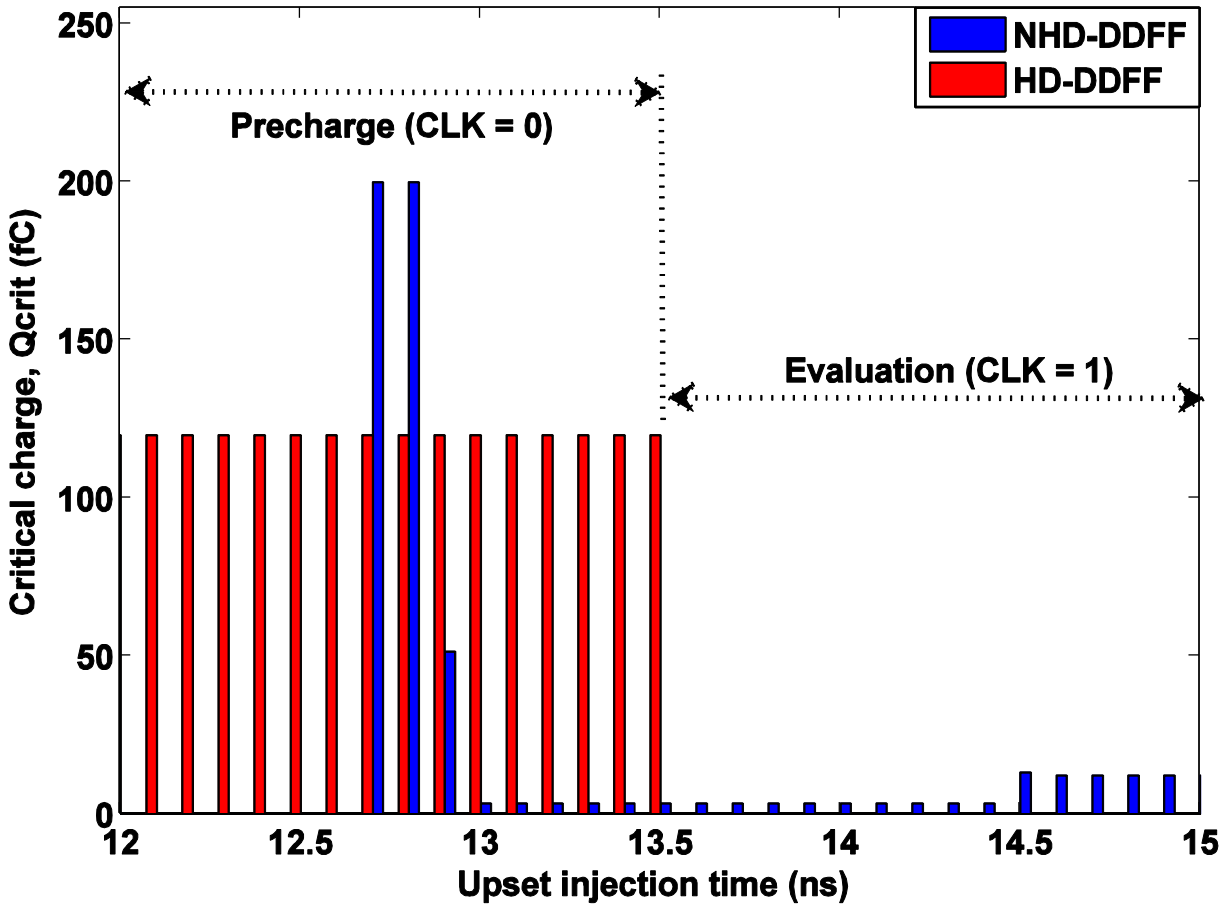


Figure 4-6. Impact of upset injection time on critical charges (D=0 in both NHD-DFF and HD-DFF).

4.4 Conclusion

The aggressive scaling of modern transistors keeps threatening the reliability of dynamic flip-flop circuits due to reduced critical charges to upset a transistor node. In order to guarantee robust dynamic flip-flops, their resilience against SEUs must be investigated. However, SEU effects in dynamic logic flip-flops have not been widely investigated. Previous methods focus on the feedback structure and overlook the analysis of the SEUs occurring in the precharge phase. A new method to analyze SEU effects is proposed in the fourth chapter of this thesis and a window of vulnerability that includes a portion of the precharge phase, in addition to the evaluation phase is also defined. Simulation results show that 55.3 % of the precharge time and a 100% evaluation time of the not-hardened dynamic flip-flops are affected by SEUs. The proposed method targets drain nodes of both clocked PMOS and NMOS devices as vulnerable paths to particle strikes in non-hardened dynamic flip-flops. This method was also applied to hardened dynamic flip-flops and the weakness of the previous hardening techniques for dynamic flip-flops was discussed. For example, the DICE hardening approach seems to protect the sensitive drain node of the clocked PMOS transistor (P-SN), but fails to mitigate SEU effects due to the SEU current injected on N-SN nodes at the precharge phase. Therefore, the findings of this fourth chapter can be used by researchers and designers alike to effectively improve future dynamic flip-flop designs and the existing hardening techniques.

CHAPTER 5

CONCLUSION AND FUTURE WORK

Radiation-induced single-event upsets (SEUs) have become a major reliability concern for modern registers. As transistor feature sizes continue to decrease, the existing SEU analysis methods and hardening techniques are enable to mitigate the SEUs. In this thesis, a systematic approach to re-examine the SEU sensitivity of static and dynamic registers in order to mitigate the impact of SEUs was presented. As the D flip-flop (DFF) constitutes the basic building element of registers and microprocessors, static D flip-flops and dynamic logic based flip-flops are used as simulation test circuits.

In order to perform SEU analysis for circuit-level simulation, a SEU model using Verilog-A and Cadence Virtuoso was designed and later utilized to analyze the SEU sensitivity of both static and dynamic flip-flops. However, the Verilog-A based SEU current model initially exhibited stability issues and led to simulation convergence problems. Using a pair of the analogLib switch along with the Verilog-A based SEU symbol, the observed simulations issues to the non-ideal SEU current were resolved. Moreover, an error boundary of less than 1% was set for validation purposes of the augmented Verilog-A/analogLib switch SEU symbol. The choice of the 1% percent error margin was required in order to maintain the noise margin of the used 180nm technology.

Using the critical charge (Q_{crit}) analysis, sensitive nodes of the static D flip-flops were identified as storage nodes with feedback loop and were categorized according to their level of

SEU sensitivity. Simulation results also revealed that the minimum collection charge needed to upset a node of a static D flip-flop (also known as the critical charge, Q_{crit}) depends on the input data value of the flip-flop. Moreover, a new hardening technique called "selective node hardening" or SNH was proposed in order to mitigate the SEU effects. Unlike previous hardening techniques which introduce a large area overhead and longer propagation delays, the SNH methodology only up-sizes the transistor width of the PMOS transistors closer to a sensitive node. As a result, the proposed SNH technique proved to be a promising and can be used to complement the existing hardening techniques.

In this thesis, it was also found that the SEU sensitivity analysis methods for dynamic flip-flops should be different from the SEU analysis approaches used for static CMOS flip-flops. Current methods for SEU analysis in dynamic flip-flops use the same SEU methods for static flip-flops which focus on storage nodes with feedback structure as the most and overlook the analysis of the SEU injected during the precharge phase. The proposed method in thesis only targets drain nodes of clocked PMOS and NMOS devices as vulnerable regions of dynamic flip-flops. In addition, a window of vulnerability (WOV) based on temporal characteristics of the dynamic logic based flip-flops was presented. This WOV was also extended to the precharge phase in order to account for all possible SEU vulnerable instances of dynamic flip-flops. Using the proposed analytical WOV, it was found that the first 44.7 % of the precharge phase in a non-hardened dynamic flip-flop are likely to recover from a SEU impact at both the local sensitive node and at the flip-flop circuit output. However, the same simulation analyses for non-hardened dynamic flip-flops show that the last 55.3 % of the precharge time and a 100% evaluation time are affected by SEUs. Therefore, the findings of this thesis can be adopted by researchers and

designers alike to effectively improve future memory circuit designs during the early design flow.

Based on the promising outcomes of this thesis, six future work steps are proposed below in order to fully investigate the effects of SEUs in registers and other memory elements.

1. The proposed boundary margin of 1% used to validate the effectiveness and consistency of the proposed Verilog-A/analogLib switch SEU model may be further explored using technology scaling. It can be hypothesized that the error margin due to the technology downscaling will be lower than the proposed 1% since the continued shrinking of transistor feature sizes is coupled with the reduction of the device noise margin.
2. The proposed window of vulnerability (WOV) of this thesis depends on the clock period T_{CLK} of the flip-flop circuit under test. However, all WOV simulation analyses in this thesis assumed 50% clock duty cycle. As part of the future work, it would be worth exploring how the change in clock duty cycle would affect the SEU sensitivity and critical charges of a flip-flop circuit.
3. Explore the effectiveness of the proposed SEU analysis method and selective node hardening technique in other logic technologies (i.e., ratioed logic, Differential Cascade Voltage Switch Logic or DCVSL, pass-transistor, and transmission gate).
4. Apply the proposed SEU analysis method to investigate the SEU sensitivity and reliability of memory elements built using emerging technologies such as memristors. The Memristor which presents a memory prospect is identified as the

fourth fundamental circuit element, the complement to resistor, capacitor and inductor.

5. Since there is a possibility of having multiple sensitive nodes within one flip-flop circuit, charge sharing and multiple bit upsets (MBUs) issues should also be explored. In addition, the concept called "SET-SEU cancellation" is proposed for future work.
6. Finally, the soundness and the efficiency of the proposed SEU analysis method and the selective node hardening (SNH) technique should be verified through physical device modeling in order to fully understand the impact of SEUs in registers. The observed linear dependency between the critical charge Q_{crit} and transistor sizing using the SNH technique should also be investigated using physical measurements of the memory circuit under test.

APPENDIX A

TUTORIAL OF SEU CURRENT MODELING

In this appendix, step-by-step instructions to generate the SEU current source using Verilog-A and create its symbol in Cadence Virtuoso IC6.1.6 are provided as follows:

Step 1: Create a new Cadence Virtuoso library for the SEU model and generate the SEU current as shown in Figure A-1.

- Click on ***File → New → Cell View***
- Then, the ***New File*** window should open as shown in Figure 1. Select Type = ***VerilogA;*** ***View*** = ***veriloga;*** Cell = ***SEU_Current*** (or name it differently). Then, click "***OK***".

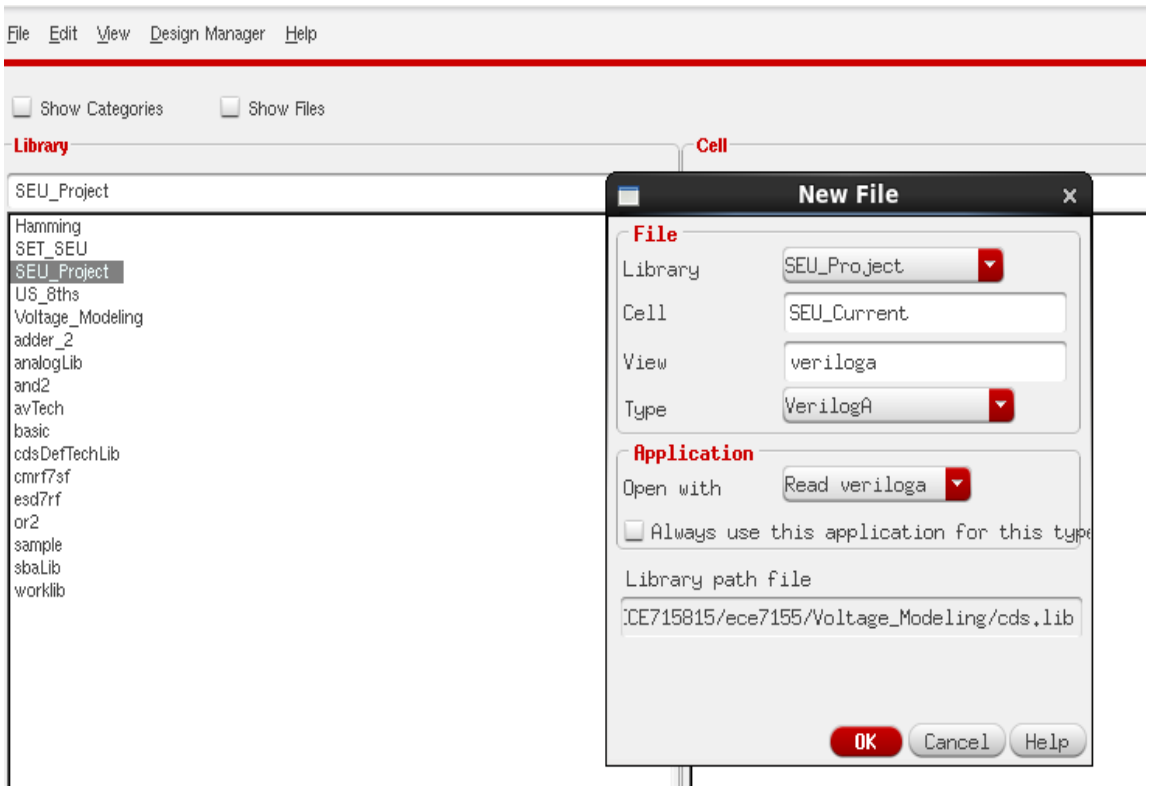


Figure A-1. Creating a new file for SEU symbol generation

***Step 2*:** A vi editor window should open. Modify or fill in the following SEU code as shown in Figure A-2.

```
`include "constants.vams"
`include "disciplines.vams"
module SEU_Current(P, N, Qcoll, ta_coeff);
input Qcoll, ta_coeff; // variable parameters
output P, N;
electrical Qcoll, ta_coeff,  P, N;
//Defining real parameters
parameter real TA= 1.0E-12; // tau alpha or falling time (ps)
parameter real TB= 5.0E-12; // tau beta or rise time (ps)
parameter real DELAYTIME = 16.5E-9; // delay constant (ns)
analog
  if($abstime < DELAYTIME)
    I(P,N) <+ 0;
  else
   I(P,N) <+ (V(Qcoll)/((TA*V(ta_coeff)) - TB)) * (exp(-1*($abstime -
DELAYTIME)/(TA*V(ta_coeff))) - exp(-1*($abstime - DELAYTIME)/TB));
endmodule
```

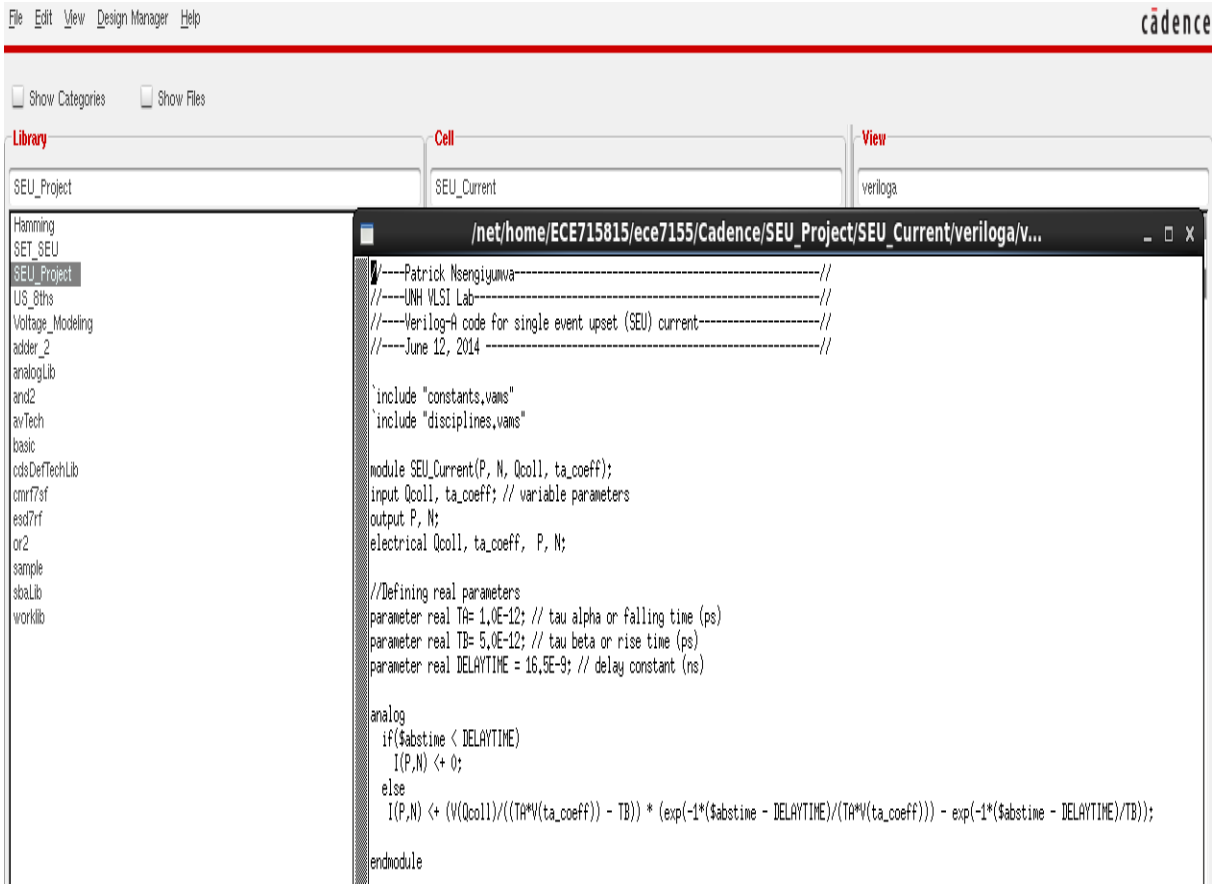


Figure A-2. Example of the SEU current code using Verilog-A

Step 3: Click the "***Esc"*** key on the keyboard. Then save and exit the SEU code using vi syntax "***:wq***". In case of a syntax error, follow the help message to correct the error. If there is no error, you will then be prompted to create a symbol as shown Figure A-3 and Figure A-4 and the CDF will be created.

Then, Click "***Yes"*** and "***OK.***"

Figure A-3. Prompted window for SEU symbol creation

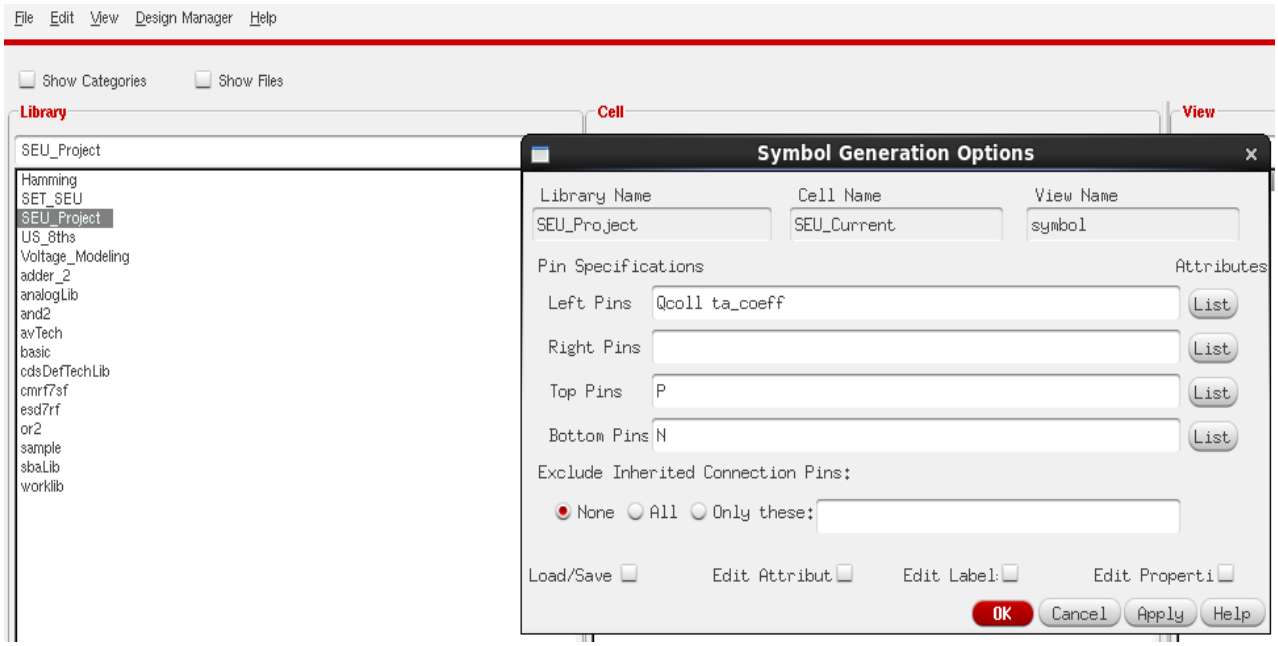


Figure A-4. SEU Symbol Generation Options window

Step 4: Then, a new window will pop up. Make sure ***xterm*** is installed on your machine. If not, use root to run this command "***yum install xterm***". Edit the SEU symbol as in Figure A-5 and save it by checking the top green check mark called "**Save and Check.**"

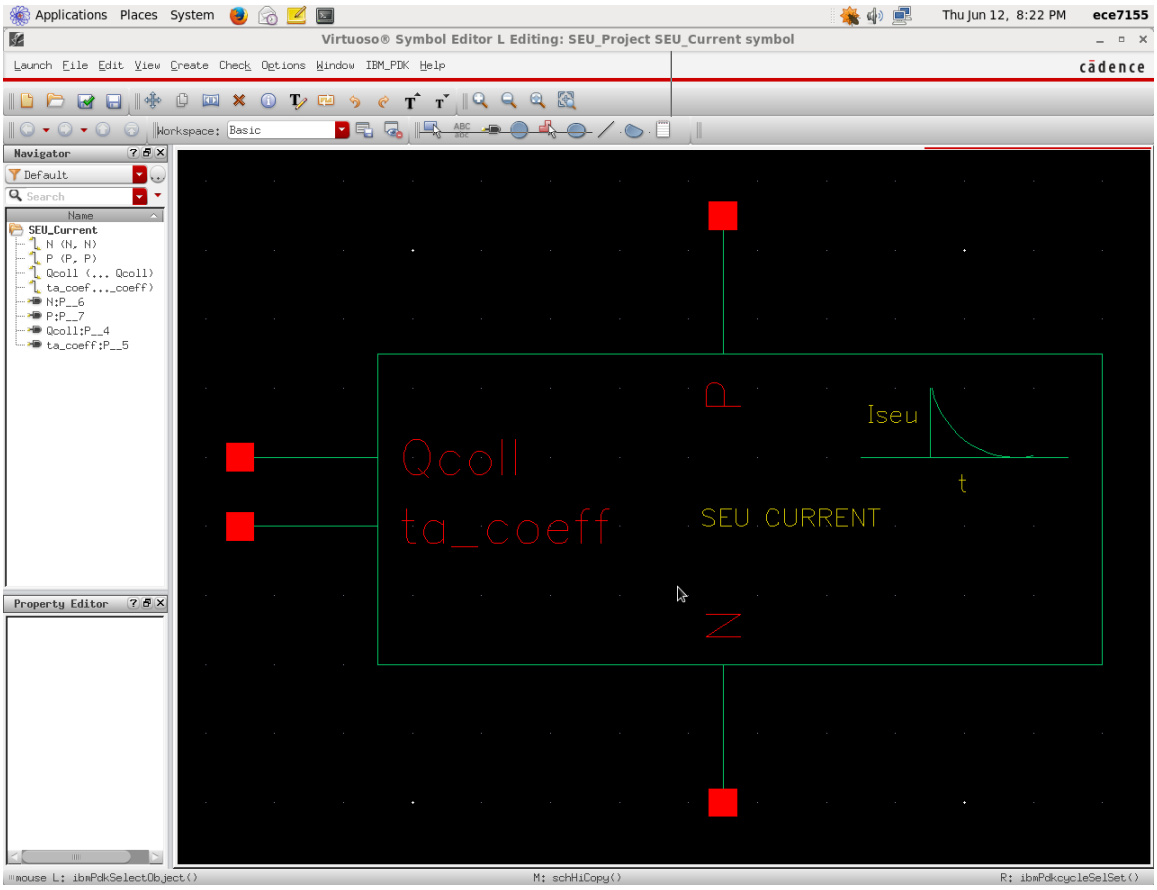


Figure A-5. Final SEU symbol in Cadence Virtuoso

Step 5: Then create a test bench schematic and instance the newly created SEU symbol in your design to test the SEU current model. The SEU current source has two terminals P and N, where P and N represent the positive current terminal and negative current terminal, respectively.

Due to convergence issues and instability of the SEU current, a pair of two analogLib switches was used in order to make the SEU current model more reliable and consistent regardless of the type of the load connected to it. Figure A-6 shows the augmented Verilog-A/Cadence SEU symbol that was used in all simulation analyses.

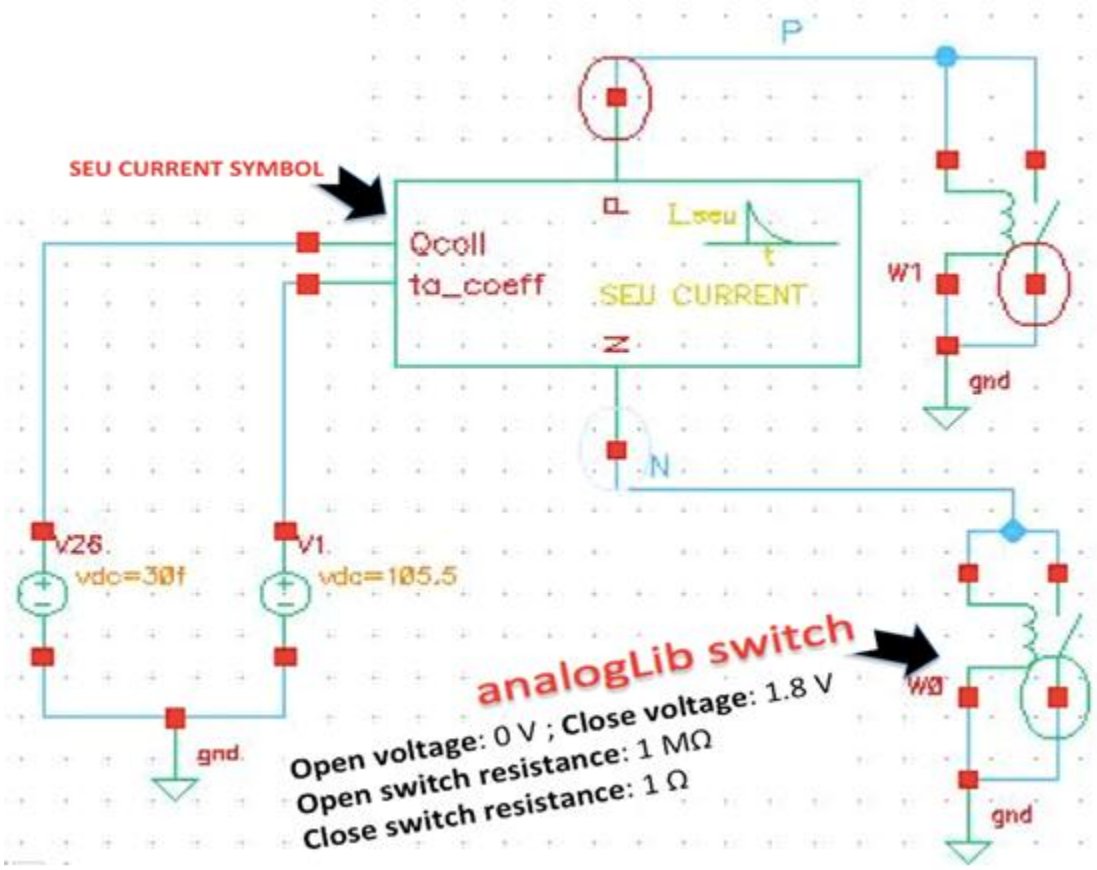


Figure A-6. The augmented SEU current symbol using Verilog-A/analogLib switch

Figure A-7 shows simulation-based SEU currents measured before the use of the analogLib switch (SEU current source I_{P0} and SEU current sink I_{NO}) and the SEU currents measured after the use of the analogLib switch (SEU current source I_{PS} and SEU current sink I_{NS}). The simulated SEU currents of Figure A-7 illustrate that the measured SEU current before

the use of the analogLib switch is approximately equal to the SEU current measured after the use of the analogLib switch.

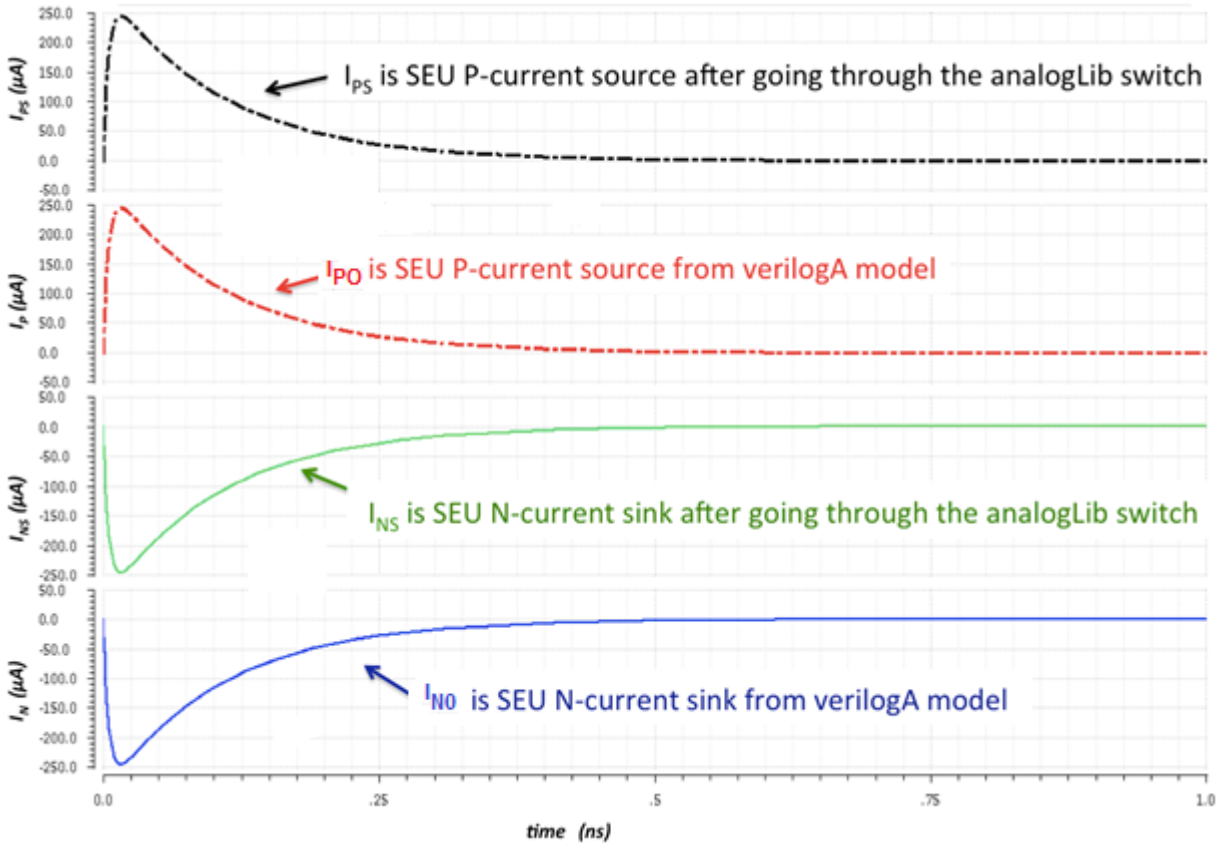


Figure A-7. SEU current source and sink. Q_{coll} = 30 fC and τ_{α} = 105.5 ps

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