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In-Memory Computing by Using Nano-ionic Memristive Devices

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by

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In-Memory Computing by Using Nano-ionic Memristive Devices

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Thesis Chapter	**Publication Title**	**Publication status**
Chapter 2	*Accurate Charge Transport Model for Nanoionic Memristive Devices*, in Microelectronics Journal	Published
Chapter 3	*Brain-inspired Pattern Classification with Memristive Neural Network Using the Hodgkin-Huxley Neuron*, in Proceedings of the 23rd IEEE International Conference on Circuits and Systems (ICECS)	Published
Chapter 4	*STDP-based Unsupervised Learning of Memristive Spiking Neural Network by Morris-Lecar Model*, in 2017 International Joint Conference on Neural Network (IJCNN) (***Best Poster Honorable Mention Award***)	Published
Chapter 5	*A Memristive CVNS Analog Adder*, in 2017 IEEE European Conference on Circuit Theory and Design (ECCTD)	Published
Chapter 6	*4:2 compressor cells design with nanoionic memristive devices*, in 2016 IEEE International Symposium on Circuits and Systems (ISCAS)	Published
Chapter 7	*Logic design on mirrored memristive crossbars*, in IEEE Transactions on Circuits and Systems II: Express briefs	Published

Chapter 2 of this thesis was co-authored with Jafar Shamsi, Majid Ahmadi, Arash Ahmadi, Karim Mohammadi, Mohammad Azim Karami, Shahpour Alirezaee, Chris Yakop-

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Abstract

By reaching to the CMOS scaling limitation based on the Moore's law and due to the increasing disparity between the processing units and memory performance, the quest is continued to find a suitable alternative to replace the conventional technology. The recently discovered two terminal element, memristor, is believed to be one of the most promising candidates for future very large scale integrated systems.

This thesis is comprised of two main parts, (**Part I**) modeling the memristor devices, and (**Part II**) memristive computing. The first part is presented in one chapter and the second part of the thesis contains five chapters. The basics and fundamentals regarding the memristor functionality and memristive computing are presented in the introduction chapter. A brief detail of these two main parts is as follows:

- **Part I: Modeling-** This part presents an accurate model based on the charge transport mechanisms for nanoionic memristor devices. The main current mechanism in metal/insulator/metal (MIM) structures are assessed, a physic-based model is proposed and a SPICE model is presented and tested for four different fabricated devices. An accuracy comparison is done for various models for Ag/TiO_2/ITO fabricated device. Also, the functionality of the model is tested for various input signals.

- **Part II: Memristive computing-** Memristive computing is about utilizing memristor to perform computational tasks. This part of the thesis is divided into neuromorphic, analog and digital computing schemes with memristor devices.

- **Neuromorphic computing-** Two chapters of this thesis are about biological-inspired memristive neural networks using STDP-based learning mechanism. The memristive implementation of two well-known spiking neuron models, Hudgkin-Huxley and Morris-Lecar, are assessed and utilized in the proposed memristive network. The synaptic connections are also memristor devices in this design. Unsupervised pattern classification tasks are done to ensure the right functionality of the system.
- **Analog computing-** Memristor has analog memory property as it can be programmed to different memristance values. A novel memristive analog adder is designed by Continuous Valued Number System (CVNS) scheme and its circuit is comprised of addition and modulo blocks. The proposed analog adder design is explained and its functionality is tested for various numbers. It is shown that the CVNS scheme is compatible with memristive design and the environment resolution can be adjusted by the memristance ratio of the memristor devices.
- **Digital computing-** Two chapters are dedicated for digital computing. In the first one, a development over IMPLY-based logic with memristor is provided to implement a 4:2 compressor circuit. In the following chapter, A novel resistive-type, single-step and multiple fanin and fanout memristive logic is designed over a novel mirrored memristive crossbar platform. Different logic gates are designed with the proposed memristive logic method and the simulations are provided with Cadence to prove the functionality of the logic. The logic implementation over a mirrored memristive crossbars is also assessed.

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This thesis is the outcome of the 3 years research in department of electrical and computer engineering, University of Windsor. To the best of my knowledge, this is the first Ph.D. thesis on emerging topic of memristive systems in Canada and it has been a great privilege to be the first Ph.D. student on this topic in the region. I gratefully acknowledge the people who assisted me along this path.

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Contents

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List of Abbreviations

ANN	Artificial Neural Network.
CAD	Computer Aided Design.
CBRAM	Conductive Bridge Random Access Memory.
CMOS	Complementary Metal-Oxide-Semiconductor.
CVNS	Continuous Valued Number System.
DRAM	Dynamic Random Access Memory.
FA	Full Adder.
HH	Hudgkin Huxley.
HRS	High Resistance State.
IC	Integrated Circuit.
IF	Integrate and Fire.
IMPLY	Material Implication Logic.
LIF	Leaky Integrate and Fire.
LTP	Long Term Potentiation.
LTD	Long Term Depression.
LRS	Low Resistance State.
MAGIC	Memristor Aided Logic.
MIM	Metal Insulator Metal.
ML	Morris Lecar.
MSIM	Metal Semiconductor Insulator Metal.
MUX	Multiplexer.
NMOS	n-Channel MOSFET.
PCRAM	Phase Change Random Access Memory.
PMOS	p-Channel MOSFET.

RMS	Root Mean Square.
RRAM	Resistive Random Access Memory.
SNN	Spiking Neural Network.
SRAM	Static Random Access Memory.
STDP	Spike Timing Dependent Plasticity.
STT-MRAM	Spin Transfer Torque Random Access Memory.
TEAM	Threshold Adaptive Memristor Model.
TSMC	Taiwan Semiconductor Manufacturing Company.
VCM	Valence Change Mechanism.
VLSI	Very-Large-Scale Integration.
XNOR	Exclusive-NOR.
XOR	Exclusive-OR.

Chapter 1

Introduction

MEMRISTOR (*memory-resistor*) is a two-terminal device which attracts significant amount of interest by the researchers recently due to its unique characteristics. Its unique $i - v$ curve shows a device with memory and variable resistance that makes it an interesting element for future computing and memory systems. Its non-volatility, low power and high switching speed promise an alternative solution for conventional high speed Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). It does not have a leakage power due to its non-volatile behavior, which makes it a suitable candidate for Flash memories. Also, this device can implement logic in addition to its memory features and this can provide an architectural solution for future computing systems. Memristive computing systems can provide logic within the memory in the same platform, which has the potential to change the current Von-Neumann computing paradigm. In addition to these features, memristor devices are believed to be able to mimic biological synaptic behavior and reproduce Long Term Potentiation (LTP) and Long Term Depression (LTD) phenomenon. Utilization of memristive systems have been intensified in neuro-science research by the experts who are in the quest of building brain-like computers. Therefore, with these features memristors can be applied for wide ranges of applications. This introductory chapter reviews the memristor device definition, functionality, modeling,

applications and the thesis outline.

1.1 Definition of Memristor

Until 2008, it was believed that there are only three fundamental passive circuit elements, capacitor (1745), resistor (1827) and inductor (1831). Although by 1960 Widrow [1] proposed the first concept of memory resistor device which was named *Memistor*, the three-terminal device with the ability to control its memristance by the time integral of current passes through the device, this device was not considered as fundamental element in circuit theory. Later in 1971, Leon Chua theorized that the fourth fundamental element named *Memristor* should exist based on the symmetrical relationship between voltage (v), current (i), charge (q) and flux (Φ) [2]. As it can be seen in Fig. 1.1, this device would complete the circle where the resistor holds relation between voltage and current ($f(v, i) = 0$), the inductor holds relation between current and flux ($f(i, \Phi) = 0$ where $v = \frac{d\Phi}{dt}$ and $\Phi = Li$), the capacitor holds relation between voltage and charge ($f(v, q) = 0$) and the memristor holds relation between charge and flux ($f(q, \Phi) = 0$). Chua, based on the mathematical analysis, predicted that a solid-state device (memristor) should exist to make a connection between charge and flux. Later, he developed the idea of memristor to broader class which is called memristive devices and systems while a memristor is only a special case in this family [3]. In 2008, the first physical realization of a memristor device was realized in HP lab by Dr. Strukov [4]. The device structure was composed of a doped titanium dioxide (TiO_{2-x}) thin film which was sandwiched by two platinum (Pt) electrodes. The doping is performed by creating positively charged oxygen vacancies over the length of TiO_2 film by removing the negatively charged oxygen atoms from their position in crystallization stage. By applying an electric field over the device, oxygen vacancies tend to move along the length of the film and it results the alteration in the conductivity of TiO_2 film. Therefore, resistance of the device can be changed based on the time integral of current passes through

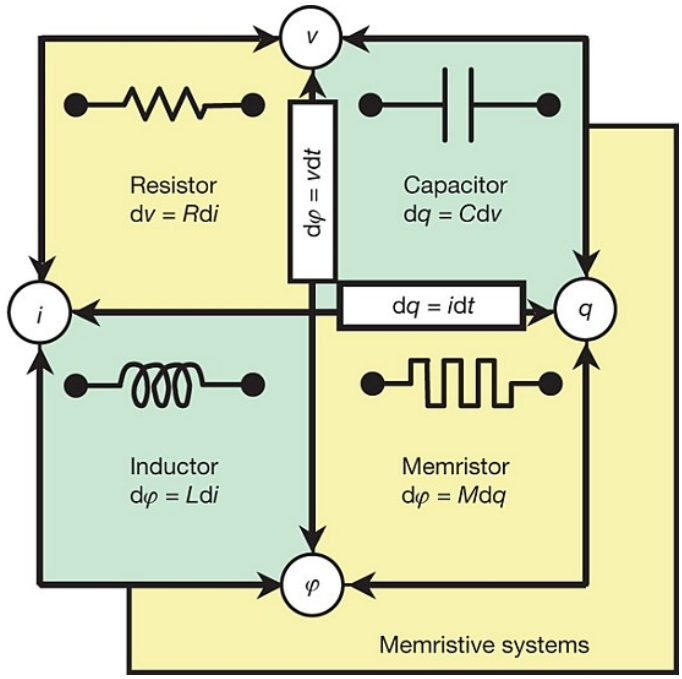


Figure 1.1: The fourth missing fundamental circuit elements [4].

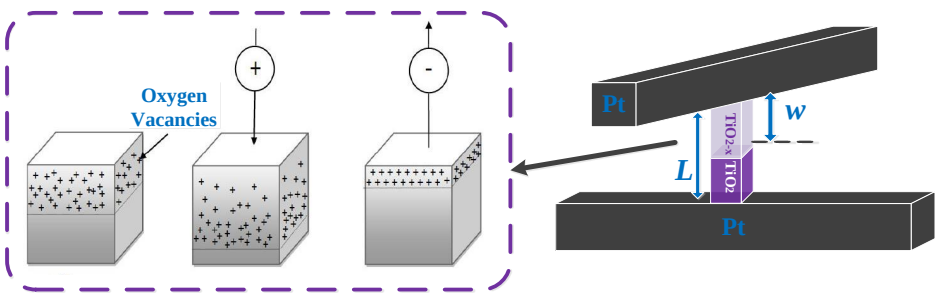


Figure 1.2: The TiO_2-based device and its doping profile behavior is displayed.

the device [4]. Also, the oxygen vacancies will remain in their position as the electric field is removed from the device which shows non-volatility behavior of it. The TiO_2-based device is presented in Fig. 1.2. In 2009, Di Ventra extended the definition of memristor and memristive systems to capacitor and inductor by defining the terms, *meminductor* and *memcapacitor* which are history dependent elements [5]. Memristor device's i-v curve is a hysthersis loop which shows variable resistance between High Resistance State (R_{HRS}) and Low Resistance State (R_{LRS}). The device is in high resistance state when the doping

profile is not spread along the film length and the un-doped region covers the whole length of the device. On the other hand, the high resistance state is when the oxygen vacancies are migrated through the length of the device and cover the whole length of the film. The memristor symbol used in this thesis is displayed in Fig. 1.3(a). The polarity of the device is recognized by a thick black bar. As it can be seen in this figure, the resistance of the device decreases when the current goes through the bar side and it is increasing when current enters the device from non-bar side. HP proposed a model [4] for memristor and considers the variable length of the doped region along the device as the internal state variable (w). The device is in high resistance state when $w = 0$ and it is in low resistance state when $w = L$ (L is the total length of thin film). Memristor device characteristic can be defined by the following equations:

$$i = g(w, v) \cdot v, \tag{1.1}$$

$$\frac{dw}{dt} = f_v(w, v). \tag{1.2}$$

These equations refer to the voltage-controlled memristor devices. i and v are the current and voltage over the memristor device, respectively. Parameters w is the internal state variable of the device and based on the HP model, it is in the domain of $0 \leq w \leq L$. Also, function $g(\cdot)$ is the memristor's conductance which is named *memductance*. Current-controlled memristor devices characteristics can be defined by,

$$v = R(w, i) \cdot i, \tag{1.3}$$

$$\frac{dw}{dt} = f_i(w, i). \tag{1.4}$$

Function $R(\cdot)$ refers to the resistance of the memristor which is named *memristance*. Memristor is any two terminal black box that follows these equations and have hystheresis i-v curve which alters in shape by changing the excitation frequency over the device. Hystheresis loop of the device is displayed in Fig. 1.3(b) for lower frequencies. Also, it is

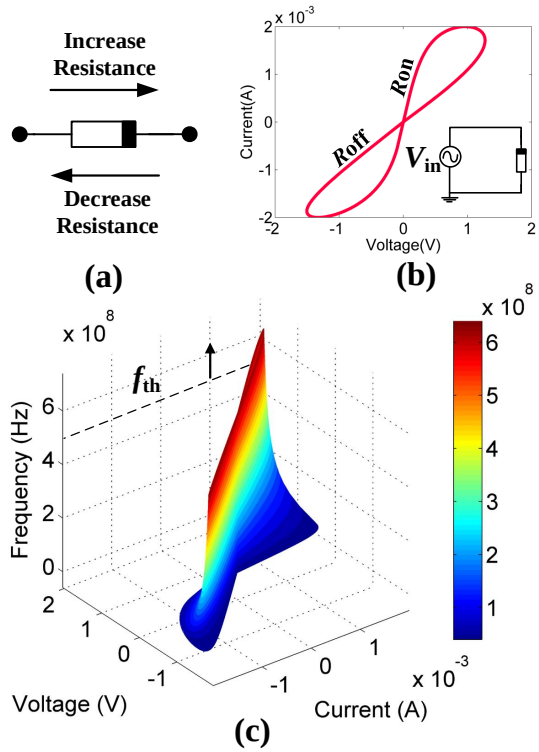


Figure 1.3: (a) The memristor symbol and its behavior toward different current directions enter the device. (b) Hystheresis loop in low frequencies. (c) The frequency behavior of i-v curve of the device.

shown that by increasing the excitation frequency the hystheresis loop begins to shrink and it becomes a single line as the frequency goes beyond specific threshold (f_{th}). Memristor's i-v curve behavior by altering frequency is displayed in Fig. 1.3(c). This speed limit feature can be applied in READ operation of the memristor devices to avoid unwanted state changes in the device.

1.2 Memristor Modeling

Since 2008 due to exciting discovery of memristor device, significant amount of research has been devoted in the search for novel materials and structures to manufacture these non-volatile devices [6–13]. Also, there is a vital need to a reliable models which can reproduce

the behavior of the device for simulation and development of memristive circuits and systems. In addition to acceptable accuracy and computational efficiency, the proposed model should be compatible with commonly accepted design modeling packages like SPICE. Following the recent advancements in the memristor and memristive systems and applications, several models have been developed for implementation in SPICE-like simulators for designing and simulating the future analog and digital systems based on memristor [14–30]. The very first efforts for modeling memristor [4] presented a linear ion drift model of memristor which is a physical model derived from mathematical equation of HP 2008 fabricated memristor. HP memristor was consisted of $\mathrm{TiO_2}$ thin film sandwiched between two platinum electrodes. Deficiency in oxygen atoms in one side of $\mathrm{TiO_2}$ makes a doped region of the film ($\mathrm{TiO_{2-x}}$). This kind of doping makes two regions with different resistance in series (doped region: low resistance, undoped region: high resistance). Since the oxygen vacancies have low mobility by removing the bias over the titanium oxide film they have the tendency to remain at their current place. Memristors saving information capability by means of its resistance makes it a non-volatile memory. Effective resistance of the thin film is related to the boundary position of the regions. The boundary position between the doped and un-doped regions is proportional to the place of the dopants which is determined through dopants velocity. Position of the boundary region can be determined through its velocity (v_{D}).

$$v_{\mathrm{D}} = \lim_{\Delta t \to 0} \frac{\Delta w}{\Delta t} = \frac{dw}{dt} \tag{1.5}$$

Linear form of the velocity of dopants (v_{D}) equation is the reason for calling this model, linear boundary drift model. It is determined by,

$$v_{\mathrm{D}} = \frac{\eta \mu_{\mathrm{D}} R_{\mathrm{LRS}}}{L} \cdot i(t) \tag{1.6}$$

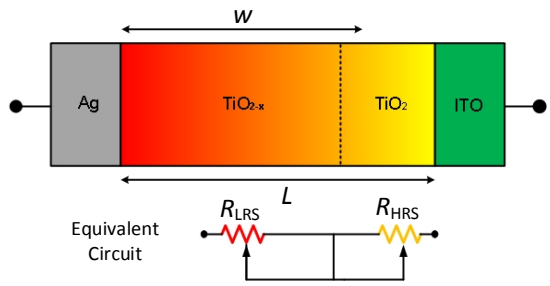


Figure 1.4: The linear ion drift model equivalent circuit for TiO_2-based device.

where L is the length of the film, η shows the memristors polarity and μ_{D} indicates the mobility of dopants and as mentioned before, the memristor is considered as two series resistors which have high and low resistances. The doped region has low resistance (R_{LRS}) while the undoped region shows high resistance (R_{HRS}). Boundary region is moved along the TiO_2 film. Therefore, the memristance for a TiO_2 memristor with boundary position of w less than its films thickness L can be determined through:

$$R_{\mathrm{w}} = R_{\mathrm{LRS}}\frac{w}{L} + R_{\mathrm{HRS}}\left(1 - \frac{w}{L}\right). \tag{1.7}$$

Schematic illustration of the linear boundary drift model for Ag/TiO_2/ITO memristor is depicted in Fig. 1.4. Consequently, the i-v relationship is determined by,

$$i(t) = \frac{v(t)}{R_{init}\left(\sqrt{1 - \frac{2\eta\mu_D R_{\mathrm{LRS}}\Delta R\phi(t)}{D^2 R_{init}^2}}\right)}. \tag{1.8}$$

where the parameters R_{init} and ΔR are given by,

$$\Delta R = R_{\mathrm{HRS}} - R_{\mathrm{LRS}} \tag{1.9}$$

$$R_{\mathrm{init}} = R_{\mathrm{LRS}}\frac{w_0}{L} + R_{\mathrm{HRS}}\left(1 - \frac{w_0}{L}\right). \tag{1.10}$$

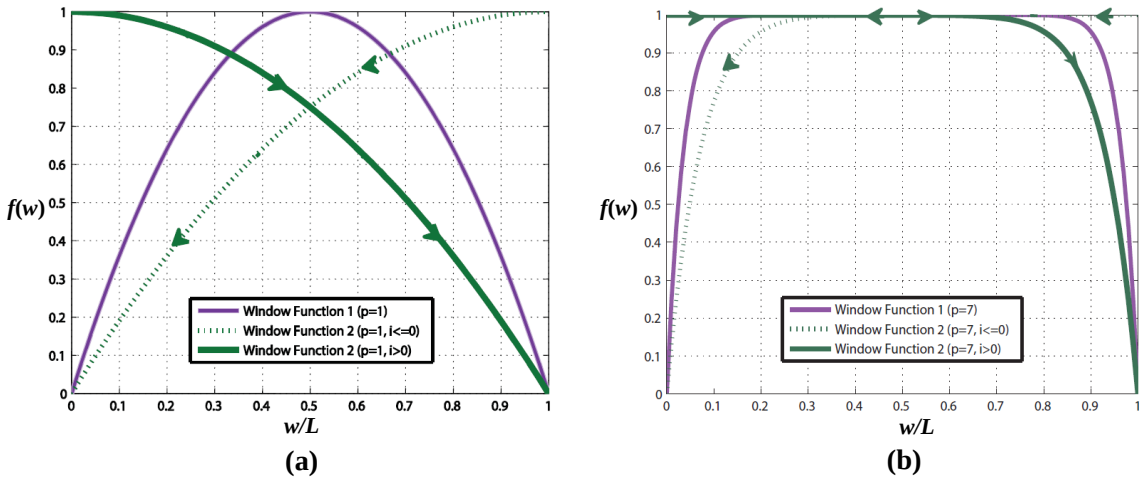


Figure 1.5: The behavior of window function 1 and 2 which are defined in [19] and [18] are considered for two different p values. (a) The $p = 1$ is set for the window function 1 and 2. (b) The $p = 7$ is set for the window function 1 and 2.

Position of the boundary region varies along the length of $\mathrm{TiO_2}$ film. In linear ion drift model, Eqn. 1.6 shows that the velocity along the whole film thickness has linear behavior, while the maximum pace of the dopants occurs at the middle point of the film. Due to the non-linear characteristic of the dopants movement, different window functions ($f(\cdot)$) were proposed to insert non-linearity into velocity,

$$v_{\mathrm{D}} = \frac{\eta \mu_{\mathrm{D}} R_{\mathrm{LRS}}}{L} \cdot \times f(w) \times i(t) \tag{1.11}$$

For the purpose of decreasing the dopants velocity at the edge of the film and having the maximum speed at the middle in [19], the non-linear phenomenon takes into account.

$$f_w = 1 - \left(\frac{2w}{L} - 1\right)^{2p} \tag{1.12}$$

where, p has a positive value. Power of the above equation adjusts non-linearity in the velocity of dopants. By increasing p, the linearity rate is soared and this is demonstrated in Fig. 1.5. The above window function has some problems for incorporating with memristors

model. After setting memristor to its terminal states R_{LRS} or R_{HRS} where window function 1 has zero value [19], changing its state to another value becomes impossible [17]. The second problem with using this window function is, its weakness for showing the asymmetric switching behavior. It uses the same behavior pattern for both zero to one and one to zero transitions ,which may not be the case based on experimental results for ON and OFF switching [20]. While these mentioned obstacles do not satisfy with window function in Eqn. 1.12, the following function was proposed which meets the above requirements [18],

$$f_w = 1 - \left(\frac{w}{L} - \mathrm{stp}(-i)\right)^{2p} \tag{1.13}$$

In the above equation, i is the memristors current. The maximum value of this window function is limited to one and cannot be adjusted to the values less or more than one. Therefore, in this window function the scale factor has been added for the purpose of having adjustable maximum value for the state variable [23],

$$f_w = j\left(1 - \left(\left(\frac{w}{L} - 1\right)^2 - 0.75\right)^p\right) \tag{1.14}$$

where j is scale factor. It controls the maximum value of the window function. This window function [23] as is depicted in Fig. 1.6, has different maximums which are lower or upper than one. In addition, the hyperbolic sine behavior has been noticed between the changing rate of the differential conductance and the applied voltage at low electric field relative to the tunneling barrier width [31]. While those window functions satisfy the boundary problems the linear ion drift model cannot fully reproduce the non-linear behavior of the device. Additionally, the common problem in former models is that there was no threshold consideration. To fulfill these issues, in [23] the following equations are

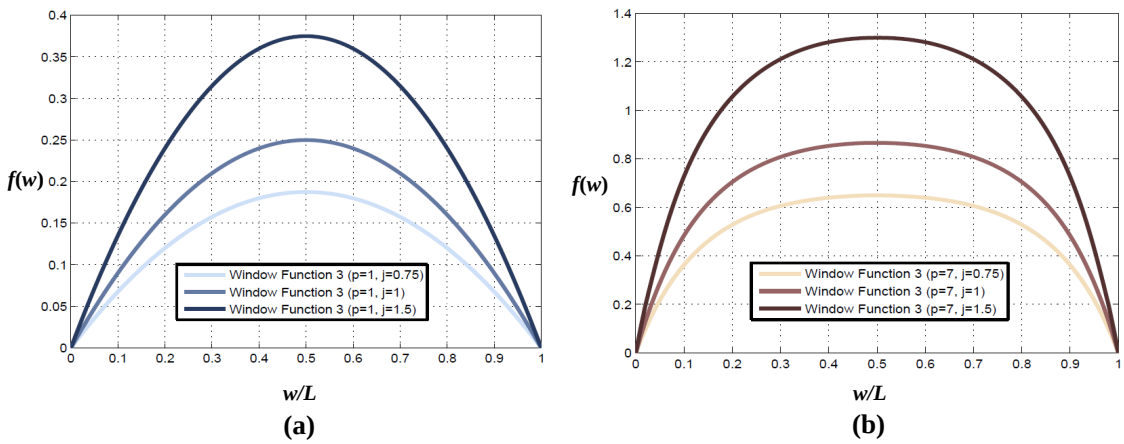


Figure 1.6: The window function 3 [23] can adjust its amplitude through the scale factor j. (a) Three figures of window function 3 [23] with the same $p = 1$, and three different scale factor values ($j = 0.75, j = 1, j = 1.5$). (b) Three figures of window function 3 with the same $p = 7$, and three different scale factor values ($j = 0.75, j = 1, j = 1.5$).

presented,

$$\frac{dw}{dt} = a \times f(w) \times g(v) \tag{1.15}$$

$$i(t) = w(t)^n \beta \sinh(\alpha v(t)) + \chi \left(\exp(\gamma v(t)) - 1\right). \tag{1.16}$$

where $g(v) = v(t)^m$ and m is an odd integer. Also, a is a constant parameter. The velocity equation shows nonlinear relation to voltage. The differential parameters are α, β, γ and χ which can be determined through experimental data. In the above equation, n is a parameter which demonstrates the impact of the state variable over the memristor's current. w parameter is the normalized state variable which has a value between 0 and 1. This state variable is approximately equal to one in ON state. When the memristor has the lowest memristance the second expression, $\chi \left(\exp(\gamma v(t)) - 1\right)$, has a negligible value in comparison with the first part, $\beta \sinh(\alpha v(t))$, which defines the tunneling phenomenon. When the opposite state occurs the dominant value is the second expression which behaves like an

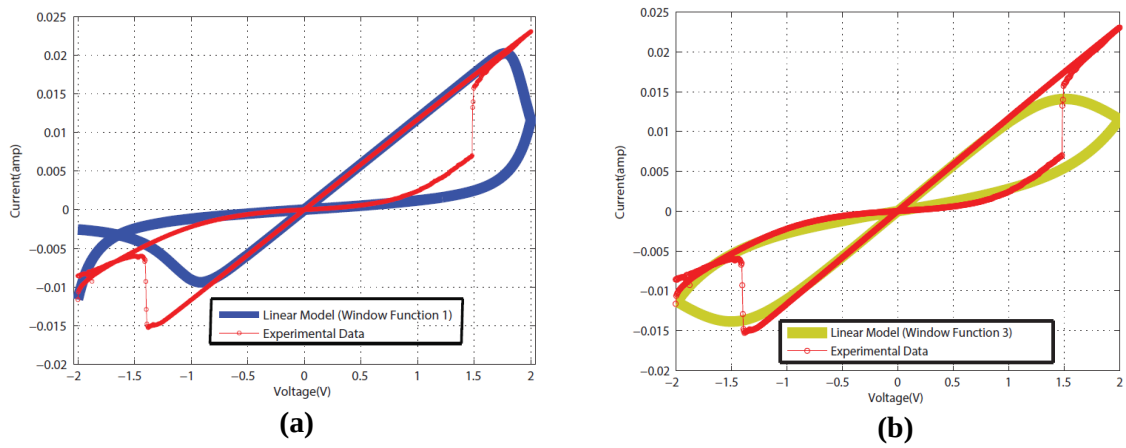


Figure 1.7: (a) It depicts Ag/TiO_2/ITO memristors linear ion drift model hysteresis plot with an input voltage source by 2 V triangular wave with 1 Hz frequency in comparison with the memristors measured experimental data [20].(b) This shows linear ion drift model of Ag/TiO_2/ITO memristor by proposing window function 3.

ideal diode. Another model can be defined by [32],

$$\begin{cases} A\text{sign}(v(m)\left(\exp(\frac{|v_M|}{v_0} - \exp(\frac{v_{TH}}{v_0}\right) & |v_M| > v_{TH} \\ 0 & \text{otherwise} \end{cases} \tag{1.17}$$

where v_{TH} and v_{M} are the threshold and the applied voltage, respectively. This equation consists of signum function, and v_0 may depend on the velocity of dopant or be independent. In the high resistance state of memristor the velocity of the dopants is assumed 0 which is an ideal value as the applied voltage is less than the threshold voltage. The Ag/TiO_2/ITO memristors nonlinear model is shown in Fig. 1.8 in comparison with the real measured data in laboratory. In the non-linear ion drift modeling of memristor like the linear ion drift modeling, the memristor doped and undoped region considered as two series resistor. In [14], a new assumption of memristor for modeling is presented. In this model, memristor is considered as a resistor in series with an electron tunnel barrier. As it is shown in Fig. 1.9, the state variable x is the Simmons tunnel barrier width. So the dopants drift

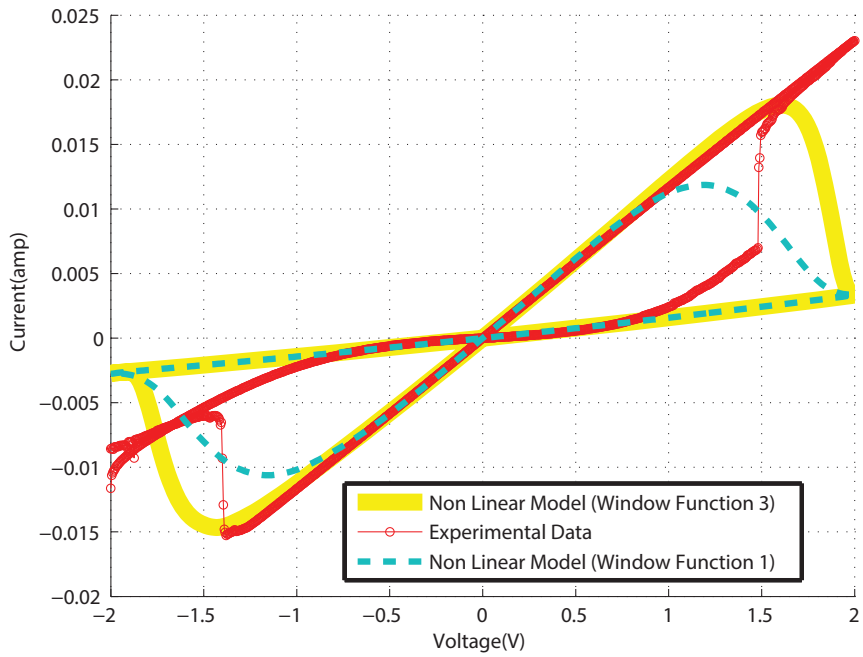


Figure 1.8: This shows nonlinear ion drift model of Ag/TiO2/ITO memristor by proposing window function 1 and 3.

velocity can be determined by [14],

$$\frac{dx}{dt} = \begin{cases} c_{off}\sinh(\frac{i}{i_{off}}\exp\left(-\exp\left(\frac{x-a_{off}}{w_c}-\frac{|i|}{b}\right)-\frac{x}{w_c}\right) & i>0 \\ c_{on}\sinh(\frac{i}{i_{on}}\exp\left(-\exp\left(\frac{x-a_{on}}{w_c}-\frac{|i|}{b}\right)-\frac{x}{w_c}\right) & i<0 \end{cases} \tag{1.18}$$

Fitting parameters are c_{off}, c_{on}, a_{off}, a_{on}, i_{off}, i_{on}, w_c and b. c_{off}, c_{on} adjust the magnitude of x derivative change while c_{on} is larger about an order of magnitude than c_{off}. Since this model provides a programming threshold, i_{off} and i_{on} are the quantities for limiting the threshold current. Changing in state variable derivative is desired for higher current than the threshold current. The a_{off} and a_{on} defines the upper and lower bound interval for state variable x. Therefore, the $x-a_{off}$ and $(x-a_{on})$ are negative quantities. Subsequently, since the exponential function is used in this equation and the negative value of its variable, a small value is allocated to the derivative of the state variable x. This equation demonstrates

the different ON and OFF switching pace which fits the experimental results as well. The current voltage relationship in this model defined as follow [14],

$$v_g = v - i(t)R_s, \tag{1.19}$$

where v_g is the voltage of un-doped region and v is the internal voltage on the memristor which is differed from the applied voltage on memristor. A SPICE model of simmons tunneling barrier model is proposed in [15]. Although it has complexity and high computational time, it brings the highest accuracy in comparison with the other models. This model is shown in Fig. 1.9, for Ag/$\mathrm{TiO_2}$/ITO memristor in comparison with the experimental data. The other good model is [33] which is based on a piece wise modeling approach which is the subtle function of the rate of change in memristance. In [33], the window function is eliminated whereas the $g(.)$ function is imposed the tunneling phenomenon and asymmetric switching behavior to the model,

$$\frac{dx}{dt} = v_x.g(v, \rho(w), \phi_0), \tag{1.20}$$

where v_x is a constant which is determined switching pace in x normalized distance (0,1) based on experimental data and ϕ_0 is the equilibrium barrier height. ρ_w is the shape factor parameter which has a linear dependent to the tunneling junction width. This makes a high non-linearity in one boundary of memristor and low non-linearity at opposite side which results dinormalization of the function. The voltage current relationship which is the modification of the $i - v$ relation [33],

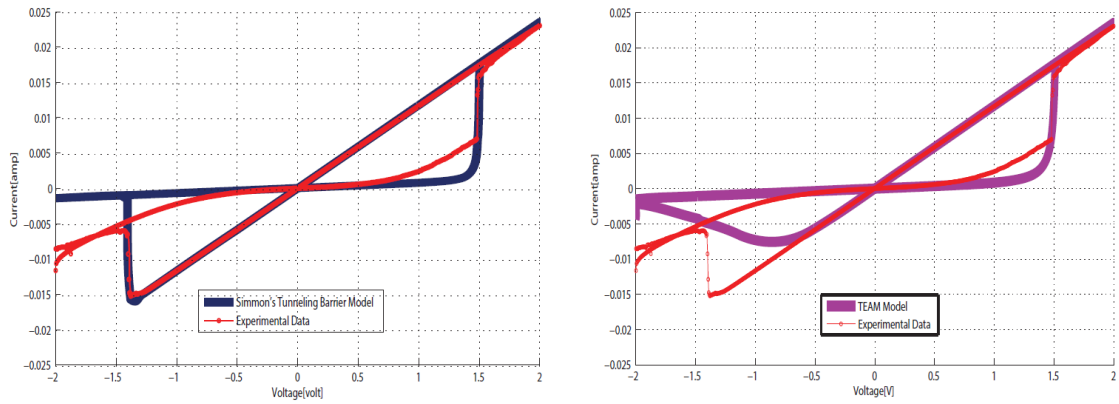
$$i(t) = w^n \sinh(v_M \vartheta) + \chi \left(\exp(\gamma v_M) - 1\right), \tag{1.21}$$

where w and ϑ are fitting parameters for defining ON state of the device. χ and γ are the fitting parameters for characterizing OFF state as well [34]. The non-linearity is inserted

through the first term of this equation. Parameter n is defined the rate of non-linearity between the drift velocity of dopants and the ON switching current. The higher value parameter n has the non-linearity rate is increased. Like the model in [15], this model is showed acceptable accuracy and a good adaptation with tunneling phenomena. A more simplified model [21] with acceptable accuracy in comparison with its former peers was presented later. In addition of its generality in comparison with Simmons tunneling barrier model, it uses simpler mathematical functions to achieve the same physical memristive behavior. Since this model is using polynomial dependence rather than exponential one which was used in Simmons tunneling barrier model, the TEAM model is becoming more computationally efficient. The TEAM models derivative state variable is,

$$\frac{dx}{dt} = \begin{cases} k_{off}\left(\frac{i(t)}{i_{off}} - 1\right)^{\alpha_{off}} \cdot f_{off}(x) & 0 < i_{off} < i \\ 0 & i_{on} < i < i_{off} \\ k_{on}\left(\frac{i(t)}{i_{on}} - 1\right)^{\alpha_{on}} \cdot f_{on}(x) & i < i_{on} < 0 \end{cases} \tag{1.22}$$

The i_{on} and i_{off} are the current thresholds and k_{off}, k_{on}, α_{off} and α_{on} are constants. The effective electric tunnel width which is considered as an internal state variable is represented by x. The window functions are f_{on} and f_{off} which limit the internal state variable to $[x_{on}\ ,\ x_{off}]$ interval. Like Simmons tunnel barrier asymmetric behavior, f_{on} and f_{off} may have different values. This model shows an acceptable accuracy but lower than Simmons tunneling barrier model. In Fig. 1.9, the Ag/TiO_2/ITO memristors experimental data has compared with the TEAM models simulation data. Later on, a voltage-based model is also presented with the same method [27]. Beside the mentioned predictive models in the literature, model in [26] was proposed based on fitting to an experimentally measured $i - v$ curve from a fabricated memristive device. The compact model [26] based on experimental observations were developed to account for irregular $i - v$ characteristics. In this work, a simple compact model that describes behavior of chalcogenide based memristor devices



(a) **(b)**

Figure 1.9: (a) It depicts Ag/TiO_2/ITO memristors simmons tunnel barrier model which has the highest accuracy in comparison with the other predictive models. (b) It depicts Ag/TiO_2/ITO memristors TEAM barrier model.

is presented. Although this model has demonstrated better accuracy in comparison with the predictive models, it does not present a comprehensive template for modeling various memristive devices and it also needs mathematical computations to find the model parameters for every memristive device. One of the other model is presented in [24], is known as generalized memristive device model. In this work, by utilizing several mathematical functions, behaviors of the memristor devices are simulated based on their physical properties. Although the model in [24] is a general model which is simple and it can be used in large-scale computations, it cannot reproduce the non-linear device behavior in high resistance state. Also, this model in not fully established based on the physical charge transport mechanism of the memristor devices. The simulation of generalized model is displayed in Fig. 1.10

1.3 Memristor Crossbar

One of the most promising structure developed by memristor devices is crossbar architecture [35]. This structure is highly scalable and it can be used for future ultra-dense memory

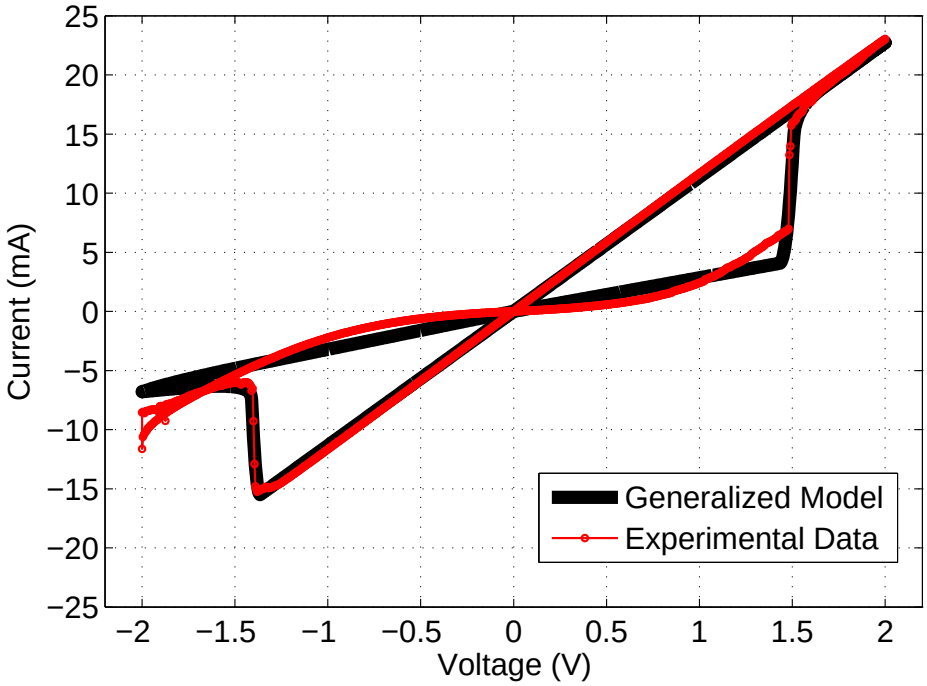


Figure 1.10: This plot displays how the generalized memristor model [24] is able to match the Ag/TiO_2/ITO-based memristor data.

systems. As it can be seen in Fig. 1.11, a memristor crossbar is a connected structure that comprises of a matrix of memristors connected with metal wires. Each device is connected to a top horizontal metal wire and a vertical bottom wire. The crossbar structure provides the highest possible integration density of memristor devices within a single layer, in which each memristor uses $4F^2$ circuit area where F is the minimum feature size.

One of the most important issue in memristor crossbar array is the problem of sneak path currents [36]. This can affect the functionality and performance of the system. As an example in READ operation, due to several alternate current paths in a regular crossbar array an exact value of stored value in cell cannot be READ properly. To avoid these issues, several approaches were proposed by the researchers [37, 38]. These solutions are in device and architectural level. In the device level, a complementary resistive switch (CRS) was proposed with specific $i - v$ characteristic [37]. This device comprised of two series memristor devices with different polarity and it provides high net resistance close to

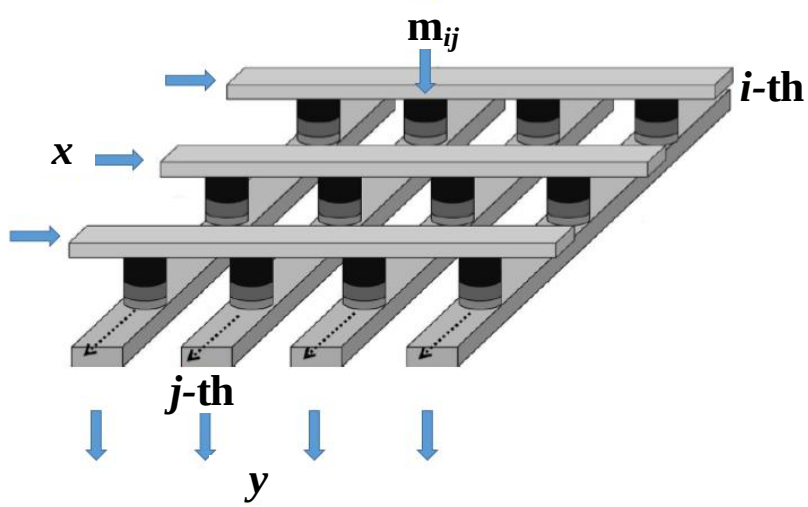


Figure 1.11: READ operation in memristor crossbar architecture.

high resistance state which considerably reduces the alternate current paths in crossbar.

Beside the device level solution, modification in the architecture of the memristive crossbar systems can provide lower sneak path effect. In [39], an access transistor was added over each memristor device which isolates other unwanted devices and mitigate alternate current paths. This crossbar architecture is called 1T1R architecture and its main drawback is its low density due to the large area needed for access devices. The other architecture is 1TNR [40] architecture which is utilized only one access transistor for all devices in each row. This architecture has higher density in comparison with 1T1R and provides acceptable sneak path current mitigation rate.

The READ operation in crossbar for each device can be done individually. For example, when reading the resistance of memristor m_{ij} connecting to i-th top metal wire and j-th bottom metal wire, a sensing voltage v will be applied on i-th top wire and all of the other wires are grounded. The current c_j can be sensed from j-th metal wire and resistance of $\mathrm{m}_{ij} = v/\mathrm{c}_j$. The programming (WRITE) procedure in the crossbar is displayed in Fig.

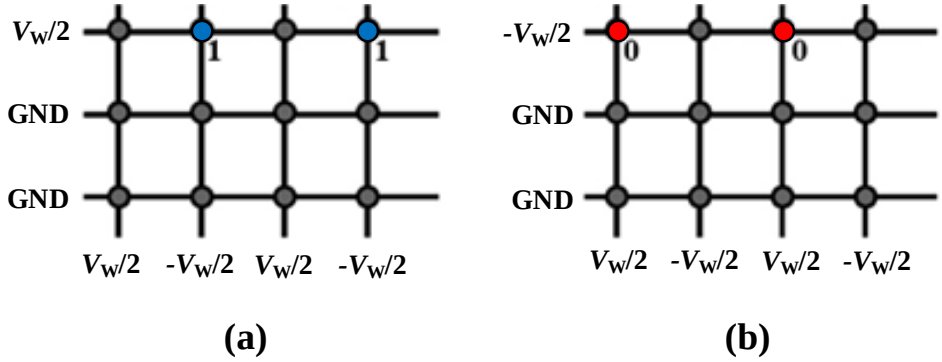


Figure 1.12: WRITE operation in memristor crossbar (a) Write 1. (b) Write 0.

1.12. This method is a two step process. It writes desired values on entire row of selected crossbar array. In the first step for writing logic 1 (R_{LRS}) on target devices, a voltage of $V_{\mathrm{W}}/2$ and GND (0 V) are applied to a selected row and all unwanted rows, respectively. The voltage V_{W} is greater than threshold of the device ($> V_{\mathrm{TH}}$). Also, the columns on which logic 1 should be connected to $-V_{\mathrm{W}}/2$ and a voltage $V_{\mathrm{W}}/2$ is applied to the other columns. The logic 1 will be written over the target devices in this step. In the second step, the selected row is connected to $-V_{\mathrm{W}}/2$ and the voltage of GND is applied to all unwanted rows. Furthermore, a voltage of $V_{\mathrm{W}}/2$ and $-V_{\mathrm{W}}/2$ are applied to the columns which logic 0 should be written on and other columns, respectively. This step will write logic 0 on all target devices in the selected row.

1.4 Applications of Memristor

Due to the unique features of nanoscale memristor devices, these devices attract researchers attention to be applied in wide ranges of applications. Memristor can be utilized in several applications like memory, logic, analog circuits, cryptography, neuromorphic, filter design, computer arithmetic, neuro-fuzzy systems and chaotic circuits. Here, we review memory,

logic and neuromorphic applications to get a better insight about the following chapters of the thesis.

1.4.1 Memory

One of the important application of memristor device is memory [41]. The non-volatility, low power, scalability and CMOS compatibility features of memristor device makes it a promising alternative for conventional SRAM and DRAM memories. Several types of memories are fabricated based on the memristive behavior. Spintronic memristor (STT-MRAM) is one of the most promising candidate for future ultra high density and high speed memories [42]. Spintronic memristor alters its resistance by changing the direction of the spin of the electrons. Due to the low memristance ratio ($R_{\mathrm{HRS}}/R_{\mathrm{LRS}}$) of these devices, an access transistor should be utilized in crossbar array for each individual memristors. This limits the maximum size of array's areal density by the size of access transistor devices.

Phase Change Random Access Memory (PCRAM) is another promising memory technology. In comparison with STT-MRAM and Resistive Random Access Memory (RRAM) it has a longer switching time (50 to 100 ns) and it has the lowest endurance in terms of switching cycles before failure [43]. Therefore, these devices are not considered for SRAM because of their low switching speed and they can be considered as a replacement for DRAM cells. The unipolar switching characteristic [44] in PCRAM makes these devices a good candidate for high density design which limiting the sneak path currents can be provided by using a diode. RRAM [45] is one of the important memory technologies and its functionality is based on the resistive switching. Unlike PCRAM devices which uses heat to change resistance state, the resistance of the RRAM device is changed by applying a voltage across the device. These devices provides high density, low manufacturing costs, high switching speed and relatively acceptable endurance. Conductive Bridge Random Access Memory (CBRAM) [46] is another memory with low current, high resistance ratio but it has a longer write time in comparison with other technologies.

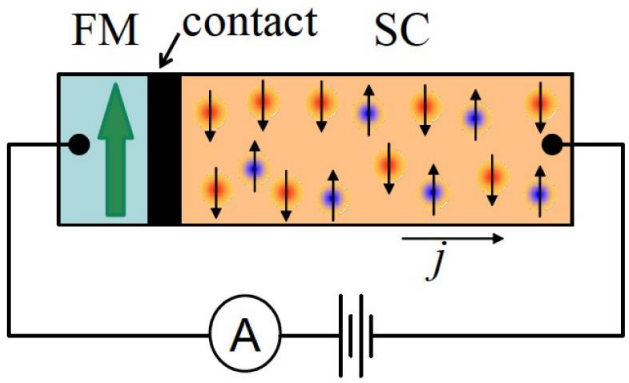


Figure 1.13: Spintronic memristor device schematic. [47].

1.4.2 Logic

Memristor is not only a memory but it has the capability to implement logic which makes it a unique device for use in future memory and computing systems [48]. These devices can implement logic within the memory which can be applied for in-memory computing scheme. Unlike Von-Neumann architecture where the memory and processing units are separate and there is a constant need for huge amount of interconnections between these units for constant communication, in-memory computing systems not only requires only one platform to implement logic and memory but also it does not need the interconnections. Thus, logic implementation with memristor has been intensified in research and there are several logic methods [48–50, 50–55] have been designed recently.

Memristor logic implementation methods can be divided based on the digital and analog property of the device. Memristor can be used as analog memory [53, 55] since it can be programmed to different memristance values. This opens a new path to explore analog arithmetic circuits by using the analog memory property of the memristor. Also, logic implementation of memristor can be applied in digital domain and there are several logic methods proposed [48–52]. Digital logic implementation with memristor devices can be categorized into the resistance-based and voltage-based logic methods. In resistance-based logic, the logical state can be determined by the memristance of the output device while in

voltage-based logic method the logical state is determined by the voltage level. Therefore, the resistance-based logic can be applied for in-memory computing scheme while there is no memory feature in voltage-based logic [51, 52]. In the resistance-based logic the logic 0 corresponds to high resistance state and the logic 1 corresponds to low resistance state. There are several resistance-based logic method proposed by memristor devices.

IMPLY logic is one of the famous logic implementation method with memristor [48]. This logic is based on IMPLY function which comprises of two input memristor devices and one resistor. The inputs should be programmed by memristance over the input devices. This logic is a sequential logic and it requires some steps to finish its computation procedure. Two voltage levels are required for this logic (V_{COND} and V_{SET}). IMPLY logic is a pure memristive logic and it can be implemented on memristor crossbar. The main drawback for this logic is, its sequential nature which requires several computational steps to implement large-scale computations. Also, the output is written over one of the input devices and this results in loosing one of the inputs. Another resistance-based logic is MAGIC [51] and this logic is a pure memristive logic. Only one voltage level is required to be applied in this logic. The inputs are the memristance of the input devices. The input and output devices in this technique are separate. In this method, for some input combinations, input devices' states are changed during the logic operation and this results in missing the input for next operation.

Hybrid CMOS/Memristor-based method is another technique to implement logic. MRL [49] is one of hybrid CMOS/memristor approach which is a voltage-based logic. This logic suffers from a signal degradation and therefore CMOS buffer is needed to amplify the output signal level. Also, for creating some logic gates like AND and OR, a CMOS inverter should be added to the output of NAND and NOR MRL gates. In this logic method, memristors are worked only as computational element and do not store any value. In this logic, the inputs are applied as voltage levels to the circuit and the initial memristance of the devices does not affect the logic computation. This logic requires only one computational

step to perform the logic operation.

1.4.3 Neuromorphic

Neuromorphic engineering is a field for designing neural architectures and circuits based on biological nervous system. Over the past few years, interest in neuromorphic computing has been increasing significantly [31]. There is a growing need for efficient smaller hardware with powerful data processing capability to implement large scale neural network for recognition, mining, and synthesis applications. The memristor is attracted significant attention as a potential element for building the neural systems. As it can be seen in Fig. 1.14, it has a similar behavior to a real synaptic connections in brain [56]. Since like brain synapses which need only electrochemical pulses to alter their weights, memristors require a voltage pulse for changing its conductivity. Memristor device can mimic a real biological synapse behaviors and can reproduce Spike Time Dependent Plasticity Mechanism (STDP) [57]. STDP consists of two main phenomenon Long Term Potentiation (LTP) and Long Term Depression (LTD) which generate based on timing difference of the pre- and post-synaptic spikes.

1.5 Outline of Thesis

This thesis encompasses two main parts **Part I** and **Part II**. **Part I** is related to the memristor device modeling and **Part II** is focusing on memristive computing circuits and applications. **Part II** is divided into different computing schemes (neuromorphic, analog and digital). This part contains five independent chapters. A background about memristor definition, its applications and a brief review of the selected previous models are presented in Chapter 1 (introduction). The modeling and its analysis is presented in Chapter 2. The neuromorphic computing task with memristor is studied in Chapter 3 and 4. Also, an analog domain application is presented in Chapter 5. Chapter 6 presents a development over

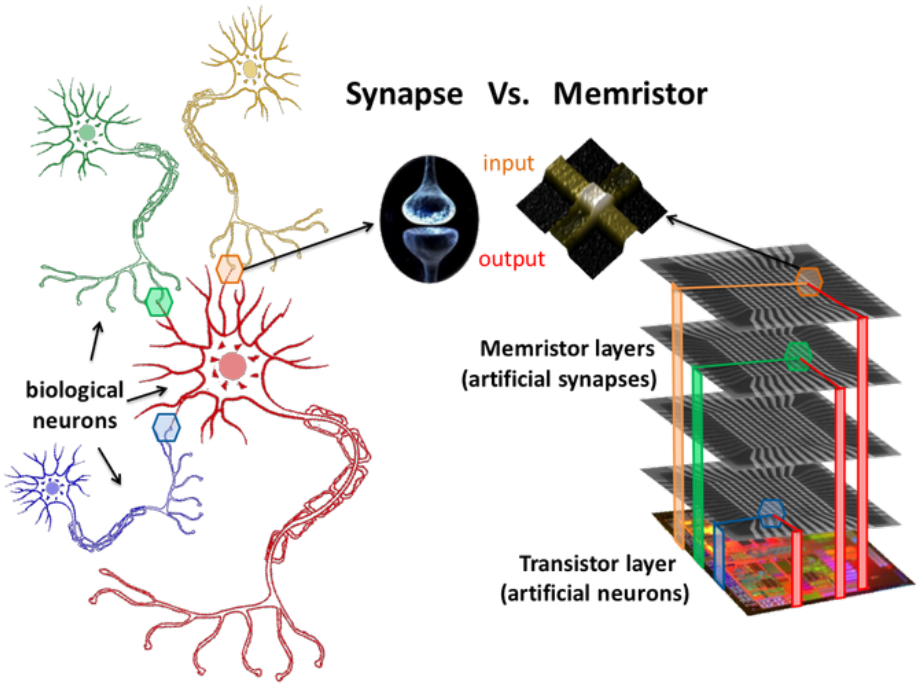


Figure 1.14: Memristor versus biological synapse [58].

existing memristive digital logic (IMPLY logic). In Chapter 7, a novel memristive logic is presented along with its novel architecture, summary, conclusion and future works are presented in Chapter 8.

- **Introduction,** in Chapter 1, the background information and memristor definition and its functionality is presented. Also, the memristor crossbar architecture is explained along with READ and WRITE operation methods within the crossbar on each device. In the next section, some relevant previous models, window functions and the modeling evolution are discussed. Then, the significant potential applications of memristor are explained (memory, logic and neuromorphic).

- **Part I- Modeling,** in Chapter 2, an accurate model for nanoionic memristive device is presented. The proposed model is based on the charge transport mechanisms in memristor devices. The main charge transport mechanism in metal-insulator-metal

structures are discussed. A physic-based model is presented based on charge transport mechanisms existed in schottky barrier region. Also, a SPICE code is developed for the proposed model and it is tested for various devices to ensure its functionality.

- **Part II- Memristive Computing,** This part is comprised of 5 chapters. In Chapter 3 and 4, pattern classification tasks are performed by a memristive bio-inspired Spiking Neural Network (SNN). In Chapter 5, an analog memristive adder is presented with a Continuous Value Number System (CVNS). This adder is designed based on the analog property of memristor devices. In Chapter 6, a 4:2 compressor circuit is designed with IMPLY logic and this implementation is completely optimized. In Chapter 7, a novel memristive logic paradigm is presented and a mirrored crossbar architecture has been developed to implement this novel logic. Different logic gates are also designed and tested with the proposed logic scheme. Also, the mirrored architecture has been tested by Cadence simulation for a larger combinational logic function.

1.6 Summary of Contributions

This thesis consists of several contributions which are defined briefly in this section.

Memristor modeling is an important topic in memristive systems research due to the growing need of circuit designers for an accurate and reliable model which is capable of reproducing the behavior of a real device. For this purpose a review of the memristor models is presented in **Chapter 1** and different models were analyzed. In **Chapter 2**, a physic-based accurate model is presented based on the charge transport mechanisms in schottky barrier region of the memristor devices. This is one of the novel contributions in this thesis. The proposed model was tested in Matlab to prove its functionality and it showed an acceptable error in comparison with experimental data extracted from a real fabricated device (Ag/TiO_2/ITO). Also, a SPICE code is developed based on the equivalent

circuit model of the proposed memristor model. The functionality of the SPICE code is tested by simulating four different devices. Also, based on the error analysis the proposed model showed the most accurate behavior toward experimental data in comparison with its previous relevant peers.

Implementing a bio-inspired system that functions based on the brain's learning mechanisms attracts so much attention in recent years. Memristor device mimics the behavior of real synaptic connections in the mammalian brain and its nanoscale feature makes it a promising candidate for ultra dense neuro-inspired integrated chips. In **Chapter 3**, the memristive implementation of a noble prize winner Hudgkin-Huxley (HH) neuron model is discussed and a bio-inspired spiking neural network based on memristor synapses and HH neurons is presented. The STDP learning mechanism is successfully implemented with this network. Some pattern classification tasks are done with this network by an unsupervised learning scheme.

In **Chapter 4**, a memristive implementation of Morris-Lecar (ML) neuron model is defined. Then, a biological spiking neural network is implemented using the defined ML neurons and memristor synapses. The STDP learning mechanism is successfully tested with the proposed network. Also, pattern classification tasks are performed by applying different patterns as the input to the network and the results proved the functionality of the design.

Multi-state memory would allow an increased information storage on a single element. Then, output of arithmetic operations on these multiple states could be stored directly in memory itself and this will results in omitting the data transfer between computing unit and memory which is the bottleneck of the current digital computers. Memristor has the analog memory feature and it can be programmed to different levels. In **Chapter 5**, a novel analog adder is designed with memristor devices based on a recently proposed continuous value number system. A programmer circuit is designed to map part of the adder circuit to provide modulo operation. Also, CVNS scheme is interpreted for memristive systems

and it has been shown that the environment resolution is dependent on memristance ratio of memristor devices. The functionality of the proposed adder is tested for different numbers.

Memristor as an emerging history dependent nanoscaled element will play an important role in future nanoelectronic computing technologies. Some pure and hybrid memristor-based implementation techniques have been proposed in recent years. Material implication logic is one of the significant areas for memristor-based logic implementation. In **Chapter 6**, a memristor-based 4:2 compressor cell is implemented based on IMPLY logic. 4:2 compressor cells are commonly utilized in high performance arithmetic systems and they are basic blocks in multipliers architecture. Two XOR/MUX and full adder-based representation of 4:2 compressors are implemented by using the IMPLY logic gates. The proposed parallel design showed good speed performance with considerably less area than conventional CMOS designs.

Chapter 7 presents another novel contribution of this thesis where a new memristor-based logic is presented. This logic needs only one computational step and it is a resistance-based logic. This logic can be applied for in-memory computing systems. This logic has the capability to provide multiple fanins and fanouts. AND, OR, NAND, NOR, NOT and COPY logic gates are designed with this logic and CADENCE simulation have been carried out to ensure their functionality. A mirrored crossbar architecture is developed to implement the proposed logic. This architecture reduces alternate current paths since during the logic whole operation time one plane of the crossbars is isolated by switches.

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Chapter 2

Accurate Charge Transport Model for Nanoionic Memristive Devices

MEMRISTORS have the potential to significantly impact the memory market, and have demonstrated the potential for analog computing within a sub-class of neuro-inspired information processing. In order to enable circuit designers to use and test memristor/CMOS hybrid circuits, it is necessary to have an accurate and reliable memristor model. Here, a new memristor model based on Charge Transport Mechanism (CTM) is presented. This chapter analyzes different current mechanisms that exist in Schottky barrier region of memristors: direct tunneling, thermionic emission, and Ohmic currents. The proposed memristor model is based on direct tunneling and Ohmic conduction, and it accounts for physical phenomena within memristive devices. The proposed model is implemented in SPICE and a sub-circuit for the model is provided.

2.1 Introduction

The memristor (memory-resistor) was first theorized as the fourth fundamental circuit element by Leon Chua in 1971 [1]. In 2008, Hewlett-Packard laboratories (HP Labs) an-

nounced fabrication of a physical memristor device [2]. The resistive switching effects in memristive devices promise an emerging alternative for flash memory, which has limitations in the sub 20 nm range. The Valence Change Memory (VCM) effect is a special type of resistive switching in redox-based devices [3]. VCM memristors offer bipolar switching behavior due to valency change within specific transition oxides like TiO_x, HfO_x, TaO_x and $SrTiO_3$. Following the recent advancements in the memristor-based applications, several models have been developed for implementation in SPICE-like simulators. These models can be the base for designing and simulating future memristive-based analog and digital systems. Due to either the complexity or inaccuracy of previous models, it is necessary to develop an accurate model that can be used in SPICE-like circuit simulators and closely matches experimental data.

In this chapter, we present a new physics based memristor model that incorporates ionic transport and tunneling mechanisms. The proposed model is based on data extracted from a fabricated memristor with a Ag/TiO_2/ITO structure [4]. The developed model can be easily utilized as a macro model in SPICE-like circuit simulators such as HSPICE and SPECTRE. The noise aspect of charge/trap hopping and effects of process variation within memristor devices are beyond the scope of the presented work.

The chapter is organized as follows: Section 2.2 defines memristor device functionality. The most important models of memristor devices are discussed in Section 2.3. In Section 2.4 different memristor charge transport mechanisms are discussed. In Section 2.5, the proposed model is presented with its SPICE code. The applicability of the model is tested for various input stimuli with different shapes, amplitudes, and frequencies in this section. In Section 2.6 the behavior of the proposed model is discussed and its accuracy is compared with state of art models. A conclusion of the presented work is provided in Section 2.7.

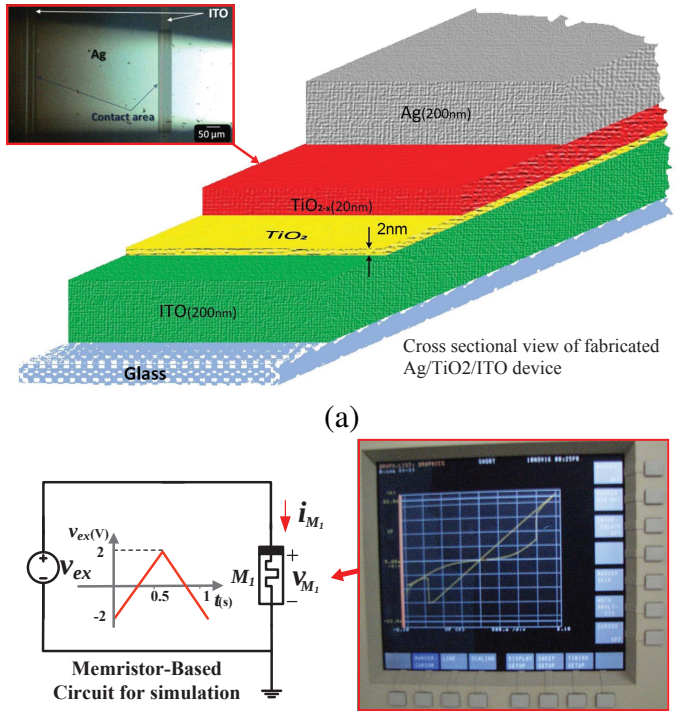

Figure 2.1: (a) A cross-sectional view of the Ag/TiO_2/ITO memristor with a fabricated memristor micrograph [4] is illustrated. The Ag and ITO top and bottom electrodes have a 200 nm width each while the thickness of the TiO_2 is about 22 nm. In this case, the doped and un-doped regions have thickness of 20 nm and 2 nm, respectively. The whole structure is placed on top of a glass layer because of the transparent nature of Indium Tin Oxide (ITO) electrodes [4]. (b) The i-v characteristic of the physical Ag/TiO_2/ITO memristor device that was obtained using a Keithley 4200-SCS semiconductor parameter analyzer [4]. The proposed circuit and the triangular excitation input voltage are also displayed.

2.2 Memristor Device Functionality

The memristor is a special class in a more general family of memristive systems and can be either a voltage-controlled or current-controlled. From this point on, it is assumed that the term memristor refers to the physical memristive device developed for the work in this chapter. The behavior of the Nth order current-controlled memristor is defined through,

$$V_M(t) = M\left(u, i, t\right) i(t) \tag{2.1}$$

$$\dot{u} = f(u, i, t), \tag{2.2}$$

where u is a vector and it represents N internal state variables. The parameters $V_M(t)$ and $i(t)$ are the voltage and current across the memristor device, respectively and M is called memristance (memory resistance). The charge-controlled ideal memristor is a particular case of equations (1) and (2), where memristance becomes a function of charge,

$$V_M = M\left(q\left(t\right)\right) i, \tag{2.3}$$

and current is defined by: $i = dq/dt$. The pinched hysteresis loop in the i-v characteristic is a unique feature of memristors. It demonstrates the passive nature of these devices as M is always positive. By increasing the excitation frequency, the hysteresis loop shrinks, and it will approach a single line as the input frequency approaches infinity. A schematic illustration and i-v curve of Ag/TiO_2/ITO memristor [4] are depicted in Fig. 2.1. The initial resistance of the device is 172 Ω. The memristor-based circuit for simulation is comprised of a serially connected input voltage source with a Ag/TiO_2/ITO memristor where the positive side of the voltage source is connected to the doped side of the memristor. The common node between the negative side of the voltage source and the undoped terminal of the device is grounded. The input voltage is one period of a 1 Hz triangular wave with a range of -2 V to 2 V.

2.3 Review of Memristor Models

The first memristor modeling effort [2] considered it to be two resistors in series. In this model, the memristance of device is dependent on the ratio between the thickness of doped region within the dielectric layer and the total dielectric thickness (D). The dopants velocity decreases at the edge of the thin film, and this non-linear effect is modeled using a window-

ing function. A number of efforts to model the non-linearity aspect of these devices using windowing functions have been demonstrated [5], [6], [7], however the accuracy of these models is limited. Subsequently in [8], changing modeling approach and using non-linear functions for simulating memristor device behavior have resulted in a non-linear boundary drift model. The non-linear ion drift model of memristors, like the linear ion drift model, is divided into doped and undoped regions that are represented by two separate series resistors. Due to the non-linear dependency between the derivative of the state variable, the thickness of the doped region along insulator film, and voltage, this model is considered non-linear. However, this modeling approach is unable to accurately model the switching behavior of the device.

In [9], a new assumption for memristor modeling considered memristor as a resistor in series with an electron tunnel barrier. The state variable in this model is Simmons tunnel barrier width [10]. This model provides a programming threshold, so change in the state variable is only occurs for current values higher than the threshold current. Due to the impact of the exponential function, there is no need for defining a window function. A SPICE based model that utilizes the Simmons tunnel barrier was proposed in [11]. Although it is complex and has a high computation time, the model is more accurate when compared to the previous models. In [12], the electron tunnel barrier model [9] is modified to avoid non-convergence, numerical errors, and non-physical solutions during time-domain simulation. Also, two physics-based models have been proposed recently for $\mathrm{TaO_x}$-based devices [13] [14]. The model in [13] considers $\mathrm{TaO_x}$-based devices with a circuit model that consists of a Schottky barrier diode in low resistance state, a variable resistor, and a base-layer resistor. In [14], modeling is based on incorporating the tunneling probability factor between the metal layers and the semiconductor layer, and demonstrating its effect on the conduction mechanism.

Another popular model is described in [15] that uses a piecewise modeling approach [16] when determining the rate of change in memristance. In [15] the window function is elim-

inated and another function is implemented to model the tunneling phenomena and asymmetric switching behaviors of the memristor. This causes a high non-linearity in one of the memristance boundaries and a low non-linearity at the opposite side. This model shows a high accuracy and good adaptation of tunneling phenomena like [11].

A more simplified model with lower accuracy, when compared with [17], was presented in [18]. In this model, unlike the other predictive memristor models, the i-v relationship can be adapted according to data from every i-v characteristic of memristor devices based on setting their related threshold voltage. In addition to its generality in comparison with Simmons tunnel barrier model [9], it uses simpler mathematical functions to achieve the same physical memristive behavior. The effective electric tunnel width is an internal state variable in this model. It has two window functions that limit the internal state variable. This model shows an acceptable accuracy, but it is still lower than that of the Simmons tunneling barrier model.

As an alternative the mentioned predictive models in the literature, [19] and [4] are applied to measured data and evaluated by fitting an experimentally measured i-v curve from a fabricated memristor. The compact model [19] based on experimental observations was developed to account for irregular i-v characteristics. In this case a simple compact model that describes the behavior of chalcogenide based memristor devices is presented. Although this model shows better accuracy in comparison with the predictive models, it does not present a comprehensive template for modeling various memristors, and would require additional mathematical computations to find new model parameters for different memristor devices.

One of the latest models presented in [20] is known as the generalized memristor model, which utilizes a set of mathematical functions to model the behavior of several different memristor devices. This model has been used to match the characterization data of 6 different device structures with less than 7 percent relative Root Mean Square (RMS) error [20] and is capable of successfully simulating several thousand memristors within a single cir-

cuit. Other than the model proposed in the following sections, this model was able to match the Ag/TiO_2/ITO memristor with the least amount of error.

Although this model is accurate for a broad range of memristors, it is not fully established based on the physical charge transport mechanisms present in memristor devices. This model is slightly less accurate when modeling the memristors OFF state in contrast to modeling the ON state. This is because the device i-v characteristic has a curvature present in the OFF state due to more complex charge transport effects. In the following sections we present a SPICE-like physical model that is based on the charge transport mechanisms in memristor devices and we present an accurate physical model of the memristor.

2.4 Memristor Charge Transport Mechanisms

Since the memristor is fabricated using a transition oxide (TiO_2) its special behaviors mainly originate from the conduction properties of titanium dioxide. The transition oxides can also act as semiconductor materials. The doped titanium dioxide thin film of a memristor is divided into two regions. One side of the TiO_2 film which contains oxygen vacancies that shows semiconductor properties, and the other side is behaving as an insulator. Therefore a typical memristor has a Metal-Semiconductor-Insulator-Metal (MSIM) like structure. Unlike typical semiconductor-based devices, the ionized atoms can drift in the direction of the current in transition oxide while an electric field is applied [21] across the memristor. Movement of this mobile ions via the phenomenon of electro-migration causes a change in ion concentration along the film. Subsequently it results in changing the conductivity of the device. Therefore, for assessing the memristors charge transport, analyzing the oxygen vacancy drift is primary. Two metallic contacts at both sides of the doped TiO_2 and undoped TiO_2 region are different from each other. The electrode in contact with the doped TiO_2 region (Ag with TiO_{2-x}) is the ohmic contact, and the electrode in connection with undoped region (ITO with TiO_2) is considered the Schottky contact [17]. In this

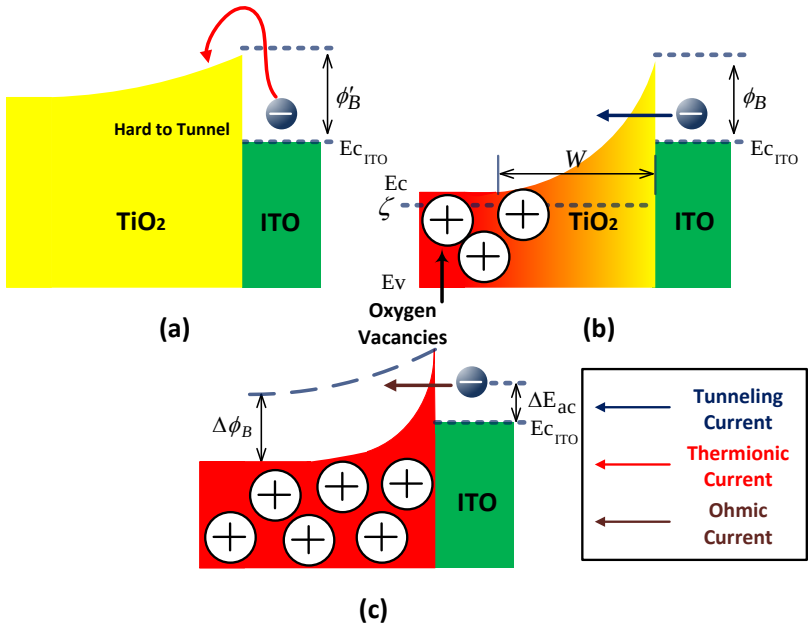

Figure 2.2: The Schottky Barrier Region is demonstrated as one of the main charge transport mechanisms. As it can be seen E_C and E_V are energy levels of conduction and valence bands of the insulator region respectively. The parameter ζ is the Fermi level. Also $\Delta\phi_B$ is the difference insulator barrier height before and after the doped region (TiO_{2-x}) extension over the insulator film length near the Schottky barrier region. The ΔE_{ac}, W, ϕ_B and $\phi_B^{'}$ are the activation energy required for an electron to leave the valence band, width of the Schottky barrier, the Schottky barrier height, and the maximum barrier height. (a) The TiO_2 near Schottky barrier region is fully undoped and tunneling current is limited. Therefore the dominant transport mechanism is thermionic. (b) The oxygen deficiencies are reaching the Schottky barrier region and the potential barrier is decreased significantly. Thus, the dominant conduction mechanism is becoming tunneling. (c) In this state the number of oxygen deficiencies has reached its maximum value near the Schottky barrier so the main conduction mechanism is ohmic.

structure, the oxygen vacancies drift from the doped region to the undoped zone when the appropriate electric field is applied. The number of oxygen vacancies migrating through the undoped region in the Schottky barrier zone of titanium dioxide film can demonstrate the ionic drift behavior of the memristor device. The quantity of the oxygen vacancies as a rate can be expressed as [22],

$$\frac{dN_{\text{Schottky}}}{dt} = \frac{1}{\tau}\left[-\text{stp}(V)N_{\text{Schottky}} + \text{stp}(-V)N_{\text{Rest}}\right] \tag{2.4}$$

N_{Schottky} and N_{Rest} are the number of mobile oxygen vacancies in the Schottky barrier region and rest of titanium dioxide thin film areas, respectively. The total quantity of oxygen vacancies along the thin film is the sum of N_{Schottky} and N_{Rest}. The high resistance and low resistance cases occur when $N_{\text{Schottky}} = 0$ and $N_{\text{Rest}} = 0$, respectively. τ is the time required for oxygen vacancies to move from one region to another and it can be found using an activation-type expression for the drift velocity as proposed in [23]

$$\tau \approx \frac{L/2}{\nu} \approx \frac{L}{2\mu E_0 \sinh\left(\frac{|E|}{E_0}\right)} \approx \frac{L}{2\mu E_0 \sinh\left(\frac{|V|}{LE_0}\right)} \tag{2.5}$$

$$\text{where} \qquad E_0 = \frac{2K_B T}{e\, t_V}, \tag{2.6}$$

and ν is the vacancies drift velocity along the insulator film during the electro-migration. K_B and L are the Boltzmann constant, and the length of titanium dioxide film, respectively. T, e, μ and t_V are the temperature, the electron charge, the dopant mobility, and the potential period, respectively. The oxygen vacancies are confined by the periodic potential due to all other atoms along the film. The quantity of oxygen vacancies near Schottky barrier region can determined by [22],

$$n_L = N_{\text{Schottky}}/(N_{\text{Schottky}} + N_{\text{Rest}}) \tag{2.7}$$

After analyzing ion migration in memristor the charge transport in Schottky barrier region should be discussed. The charge transport in transition oxides is comprised of three main mechanisms: quantum mechanical tunneling, thermionic emission, and ohmic conduction [24–28]. The previous efforts in modeling the memristor are based on a current equation derived from the Simmons current equation extracted from [10] for MIM structures.

2.4.1 Tunneling Current

The main limitation for electron movement is the Schottky barrier, the contact zone between the metallic electrode and the undoped zone of the TiO_2 side along the memristor. When a negative bias is applied across the device, width of the Schottky barrier expands and results in less electrons tunneling through as can be seen from Fig. 2.2. On the other hand, by applying a positive bias the oxygen vacancies will move toward the Schottky barrier side of the TiO_2. This results in narrowing the width of the Schottky barrier and more carriers movement, therefore the tunneling current density is increased dramatically and it is determined by [10],

$$J_{\text{Tunn}} = \frac{\alpha\, e^{(-\beta)}}{(\gamma K_B T)^2} \frac{\pi\gamma K_B T}{\sin(\pi\gamma K_B T)} \left[1 - e^{(-\gamma e V)}\right], \tag{2.8}$$

where α and K_B are the Richardson and Boltzmann constants respectively. The β and γ parameters that are a function of V show different behaviors toward forward and negative bias, while the Richardson constant has the same behavior in the different bias conditions. In the forward bias they can be determined by

$$\alpha = \frac{4\pi\, m\, e\, (K_B T)^2}{h^3} \tag{2.9}$$

$$\beta = \frac{\phi_B - eV}{E_M} \tag{2.10}$$

$$\gamma = \frac{1}{2E_M} \ln\left[\frac{4(\phi_B - eV)}{\zeta}\right], \tag{2.11}$$

where m is the effective electron mass. ϕ_B is the barrier height which is the difference between the affinity of the semiconductor and work function of the metal. For the sake of simplicity a constant barrier height is considered in the proposed model calculations. ζ is the Fermi level of the semiconductor. The energy E_M is the material dependent parameter

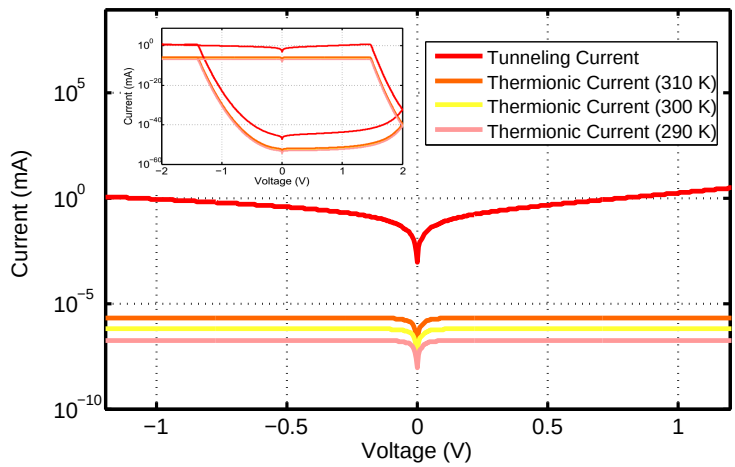

Figure 2.3: The plot displays the Ag/TiO_2/ITO memristor's tunneling current in comparison with the thermionic current at different temperatures for a -1.2 V to 1.2 V voltage domain and a ± 2 V, 1 Hz triangular wave input voltage.

that is inversely related to the width of the Schottky barrier [10] and given by [29]

$$E_M = \frac{E_{0M}}{(1 - a_M\, n_L)}, \tag{2.12}$$

where E_{0M} is the value of E_M at $n_L = 0$. a_M is constant with a value between 0 and 1. The width of the Schottky barrier, W, will change linearly as function of the quantity of oxygen vacancies that have drifted through this region given by

$$W = W_0(1 - a_M\, n_L). \tag{2.13}$$

The maximum width of the Schottky barrier is W_0. The minimum width happens when the quantity of oxygen vacancies is increased to its highest value when n_L is considered as 1. Therefore the minimum width of the Schottky barrier is $W_0(1 - a_M)$.

2.4.2 Thermionic Current

In addition to the tunneling current, the thermionic current is another electron transport mechanism in the Schottky barrier region. Based on Fig. 2.2 this mechanism is more considerable when the doped region is not spread around the Schottky barrier region. Usually in memristor models this mechanism is ignored due to its negligible value in comparison with the tunneling current. The thermionic current density in metal insulator metal structures is determined through [30],

$$J_{\text{Therm}} = A_{th}\, T^2 e^{\left(\frac{-\phi_B^{'}}{K_B T}\right)} \left[1 - e^{\left(\frac{-eV}{K_B T}\right)}\right] \tag{2.14}$$

$$\text{where} \qquad A_{th} = \frac{4\pi\, m\, e\, K_B^2}{h^3}, \tag{2.15}$$

where $\phi_B^{'}$ is the maximum barrier height and h is Planck's constant. Based on Fig. 2.3 this mechanism has a negligible value in comparison with the other mechanisms in Schottky barrier region.

2.4.3 Ohmic Current

The charge transport mechanism in the memristor becomes an ohmic process when oxygen vacancies move forward to the Schottky barrier and cover the whole length of the TiO_2 thin film. Therefore the doped and undoped regions will contain oxygen vacancies and both of them will behave as semiconductor materials. The TiO_{2-x}/ITO interface is considered an ohmic contact as shown in Fig. 2.2. The ohmic current density can be determined by [31]

$$J_{\text{Ohmic}} = \frac{e\, n(T) \mu_\nu\, V}{D} \tag{2.16}$$

$$\text{where} \qquad n(T) \cong \sqrt{\frac{N_D N_C}{2}} e^{\left(-\frac{\Delta E_{ac}}{2K_B T}\right)}, \tag{2.17}$$

and ΔE_{ac} is the activation energy of electrons. $n(T)$ is the temperature dependent charge carrier concentration. N_D and N_C are the effective density of states in the valence band and the effective density of states in the conduction band, respectively. The density of states in a semiconductor equals the density per unit volume and energy of the number of solutions to Schrodinger's equation.

2.5 An Accurate SPICE-Based Memristor Model

The idea of this model is based on the electron transport mechanisms in the Schottky barrier region. The current in the memristor may be due to either tunneling, thermionic emission, ohmic contact, or a combination of the three depending on the state and applied voltage in the model. The thermionic current is too small in comparison with the tunneling mechanism. Therefore, to decrease the complexity of the model, thermionic current is ignored due to its negligible effect on improving accuracy. Although in the proposed model thermionic current is not considered, its effect on memristor device behavior can be assessed in future works for a wide temperature spectrum. The movement of oxygen deficiencies and the electron traveling mechanisms should be considered to determine the memristor current. The proposed model is simulated in Fig. 2.4 for the Ag/TiO_2/ITO memristor fabricated in [4]. As described in Table 5.2, the i-v curve has been divided into six regions based on the voltage domain and the memristor's Schottky barrier currents in each region for the Ag/TiO_2/ITO device. . To implement the dominant memristor current mechanisms for different regions in Table 1, the state variable n_L is determined by,

$$\frac{dn_L}{dt} = g(V, n_L). \tag{2.18}$$

By substituting (5) into (4) the oxygen vacancy dynamics determined in (4) can be rewritten as [22]

$$g(V, n_L) = \frac{2\mu E_0}{L} \text{sinh}\left(\frac{|V|}{LE_0}\right)\left[-\text{stp}(V)n_L + \text{stp}(-V)(1 - n_L)\right], \tag{2.19}$$

also $n_L = N_{\text{Schottky}}/(N_{\text{Schottky}} + N_{\text{Rest}})$. The state variable n_L describes the quantity of the oxygen vacancies near the Schottky barrier region of the memristor. It is worth noting that the proposed model successfully reproduced the i-v curve of different devices with different excitation voltages. However, the behavior of the Ag/TiO_2/ITO device has been analyzed and accuracy comparison with other memristor models has been made for the triangular-voltage excitation because of data availability for this type of excitation. The equivalent circuit for the proposed SPICE model is displayed in Fig. 2.5. To implement the derivation presented by (2.19) in SPICE tools, a capacitor `Cn` with capacitance of 1 F is used. Also, the initial quantity of oxygen deficiencies near the Schottky barrier region, `n1`, is defined as the initial voltage stored across the capacitor, `Cn`, `VCn(0)=n1`. The equivalent circuit for state variable n_{L} is shown in Fig. 2.5. Therefore, the initial voltage stored in the capacitor of the equivalent circuit is considered as `n1`. This value shows the initial quantity of oxygen deficiencies in the first moment before applying a voltage across the memristor. The dependent current source `Gn` is used for extracting (2.19) from the voltage of the node n_L in Fig. 2.5. Also the mobility of the oxygen deficiencies is defined using two different parameters. The `uvp` is defined as the mobility of the oxygen deficiencies as the forward bias is applied to memristor. In this case, the vacancies drift toward the ITO electrode. In addition, the `uvn` is the mobility of the oxygen deficiencies when the memristor is reverse biased. Since the electron mobility in the forward bias is higher than in the reverse bias mode, these two parameters are used for fitting purposes based on the physical prop-

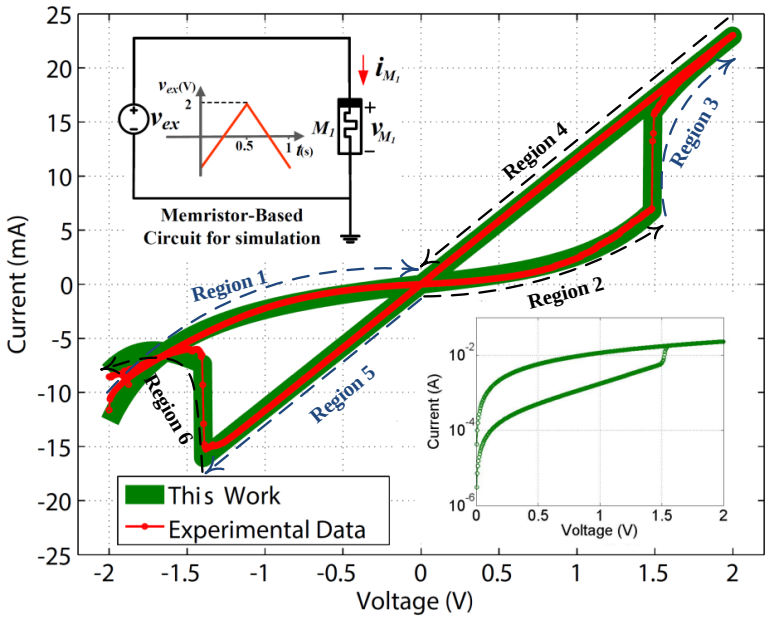

Figure 2.4: This plot displays the Ag/TiO_2/ITO memristor's CTM model i-v curve which has the highest accuracy in comparison with the previous works. The memristor i-v curve is divided into six regions with different voltage domains. The CTM model parameters are the same as parameters applied in Table 2.2. This i-v curve is for a ± 2 V, 1 Hz triangular wave input voltage. The bottom right corner inset displayed logarithmic scale i-v curve for positive voltages.

Table 2.1: The memristor i-v curve is divided into six regions with different voltage domains and limited current mechanisms for a ± 2 V triangular input voltage with 1 Hz frequency.

Region	Voltage Domain	Limited Current Mechanism
1	$-2 \leq V < 0$	Tunneling & Thermionic
2	$0 \leq V < 1.5$	Tunneling & Thermionic
3	$1.5 \leq V < 2$	Ohmic - Tunneling & Thermionic
4	$0 < V \leq 2$	Ohmic
5	$-1.4 < V \leq 0$	Ohmic
6	$-2 < V \leq -1.4$	Ohmic - Tunneling & Thermionic

erties of the insulator and electrodes of the memristor devices [32]. For memristor current, the `Gtunn` and `Gohmic` current sources are used. The switching of the the `Tran_func` function is defined based on the logistic function given in [20]. Since the change in state from LRS to HRS (or the inverse case) occurs gradually, the dominant current mechanism is changed with a non-linear behavior. For instance when switching from the LRS to the

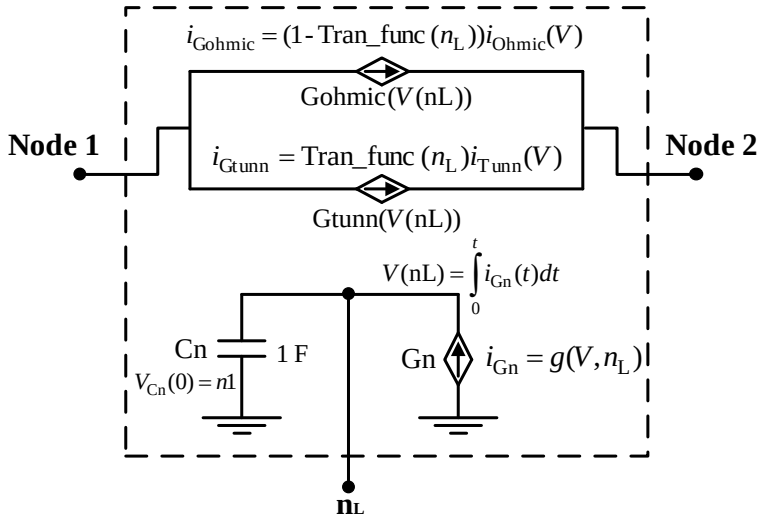

Figure 2.5: Memristor SPICE model schematic diagram. The memristor SPICE model has three nodes. Node 1 and 2 represent the positive and negative nodes of the memristor device, The node n_L is for visualizing the number of oxygen deficiencies near the Schottky barrier region.

HRS, the ohmic current is dominant at first, then the tunneling mechanism gradually starts to dominate. The changing coefficient to model this behavior is applied using a logistic function. The proposed equation is

$$\texttt{Tran\_func} = \frac{1}{1 + e^{(S\,\texttt{Dec})}}, \tag{2.20}$$

where S is the setting parameter to control the state shifting of the device. This parameter can have different values according to the physical properties of the various memristors. The `Dec` parameter is given by

$$\texttt{Dec} = n_{th} - n_L, \tag{2.21}$$

where n_L is the quantity of the oxygen deficiencies near the Schottky barrier region at each point in time. n_{th} is the threshold value for the quantity of oxygen deficiencies near the Schottky barrier region. Since the transition oxides behave like semiconductor materials as the number of the oxygen deficiencies is exceeded, the specific value of this parameter is

Table 2.2: Accurate memristor model spice code with charge transport mechanism analysis. The code is written in HSPICE software.

```
.title SPICE Model For Memristor based on CTM
*CTM= Charge Transport Mechanisms
**********************************************
* Connections:
* 2 - Positive Electrode
* 1 - Negative Electrode
* nl - initial state
**********************************************
.Subckt Acc_CTM_Mem 2 1 nl
*
*Constants
.param
+Area=1e-17      * Effective area
+L=22e-09        * Length of insulator film
+m0=9.109e-31    * Electron weight
+h=6.626e-34     * Plank constant(j.s)
+k1=1.38e-23     * Boltzmann constant(j.s)
+K=8.617e-05     * Boltzmann constant(eV.s)
+e=1             * Electron charge (e)
+q=1.6e-19       * Electron charge (c)
+pi=3.14
*
*Physical Parameters
+T=300           * Temperature
+uve=0.1e-10     * Electron mobility
+uvo=0.14e-14    * Ion mobilty
+E0=9e07         * E0=2kT/(qa1),
* T:Temprature
* q:Electorn charge
* a1:Potential period
* E_0M Related to Schottky barrier width at nL=0
+E_0M=1.7
+Eb=3.5          * Barrier height
+n_th=0.8        * Threshold of nL
+n1=0.79         * Initial value of node nL
+deltaE=0.11     * E is activation energy
+ND=1e19         * Density of states in valence band
+NC=9e19         * Density of states in conduction band
*
*Setting Parameters
+aM=0.99
+zeta=0.2
+S=550
+bn=0.27
*
*Simplifying Parameters
.param uvp='1*uvo'
.param uvn='bn*uvo'
.param m = '0.85*m0'
** A=Area*4*Pi*m*q*(K1*T)**2/(h**3)
.param A = '0.0875e11*Area*4*PI'
.param N = '0.707*sqrt(ND*NC)*Area*exp(-deltaE/(2*K*T))'
.param C1 ='log((4*Eb-4*e*V(2,1))/Zeta)*
+ (1-aM*V(nL,0))/(2*E_0M)'
.param b1='(Eb-e*V(2,1))*(1-aM*V(nL,0))/E_0M'
.param Tran_func = '1/(1+exp(S*(V(nL,0)-n_th)))'
.param sn='(sgn(V(2,1))+1)/2'
*****************************************************
* nL: Oxygen Deficiency Quantity around Schottky Barrier
.ic nL = n1
Gn 0 nL value='sinh(abs(V(2,1))/(L*E0))*
+  (sn*2*uvp*(E0/L)*(1-V(nL,0))+(1-sn)*2*
+   uvn*(E0/L)*(-V(nL,0)))'
Cn nL 0 1
*****************************************************
* Tunneling and Ohmic Currents*
Gtunn 1 2 value = 'Tran_func*A*pi*exp(-b1)*
+        (1-exp(-C1*V(2,1)))/(C1*K*T*sin(pi*C1*K*T))'
Gohmic 1 2 value = '(1-Tran_func)*e*N*(uve/L)*V(2,1)'
.ends Acc_CTM_Mem
```

called n_{th}. This threshold quantity is different for each of the transition oxide materials. It is also related to the electrode position at both sides of the insulator in the memristor device. Therefore, two different memristors such as the Pt/TiO_2/Pt device and the Ag/TiO_2/ITO device, have the same transition oxide but different electrode designs, so the value for n_{th} will be different in each case.

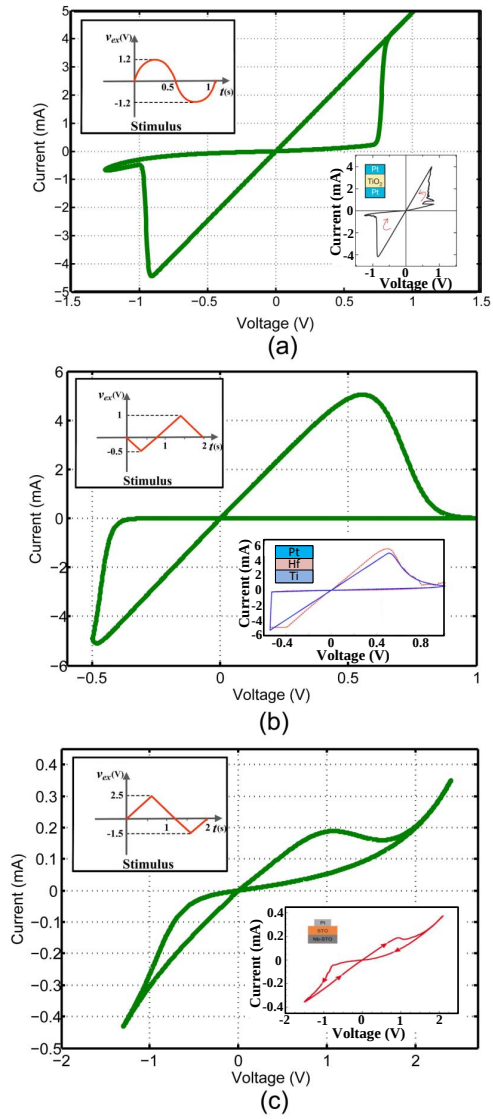

Figure 2.6: Proposed CTM model simulations in comparison with fabricated devices experimental data. In (a) the proposed CTM model fits the experimental data of the Pt/TiO_2/Pt memristor [2] and the model parameters are L = 50 nm, T = 300 K, $n_{\rm th} = 0.9, n_1 = 0.83, \Delta E_{ac} = 1.48, E_b = 3.7, E_0 = 2 \times 10^{-7}, E_{0\rm M} = 0.49, N_D = 3.16 \times 10^{17}, N_C = 3.6 \times 10^{17}, a_M = 0.2, \zeta = 0.2, b_n = 0.17, S = 450$. The input voltage applied to the device is displayed in the sub-window. In (b) the proposed CTM model fits the experimental data of the Pt/Hf/Ti memristor [33] and the model parameters are L = 10 nm, T = 300 K, $n_{\rm th} = 0.91, n_1 = 0.88, \Delta E_{ac} = 1.2, E_b = 2.5, E_0 = 2 \times 10^{-7}, E_{0\rm M} = 3.3, N_D = 1 \times 10^{18}, N_C = 5 \times 10^{17}, a_M = 0.03, \zeta = 0.1, b_n = 0.6, S = 100$. The input voltage applied to the device is displayed in the sub-window. In (c) the proposed CTM model fits the experimental data of the $SrTiO_3$ based memristor [34] and the model parameters are L = 500 nm, T = 300 K, $n_{\rm th} = 0.97, n_1 = 0.95, \Delta E_{ac} = 1.15, E_0 = 1 \times 10^{-6}, E_{0\rm M} = 1.2, N_D = 7 \times 10^{18}, N_C = 5 \times 10^{18}, a_M = 0.01, \zeta = 0.3, b_n = 0.06, S = 60$. The input voltage applied to the device is displayed in the sub-window.

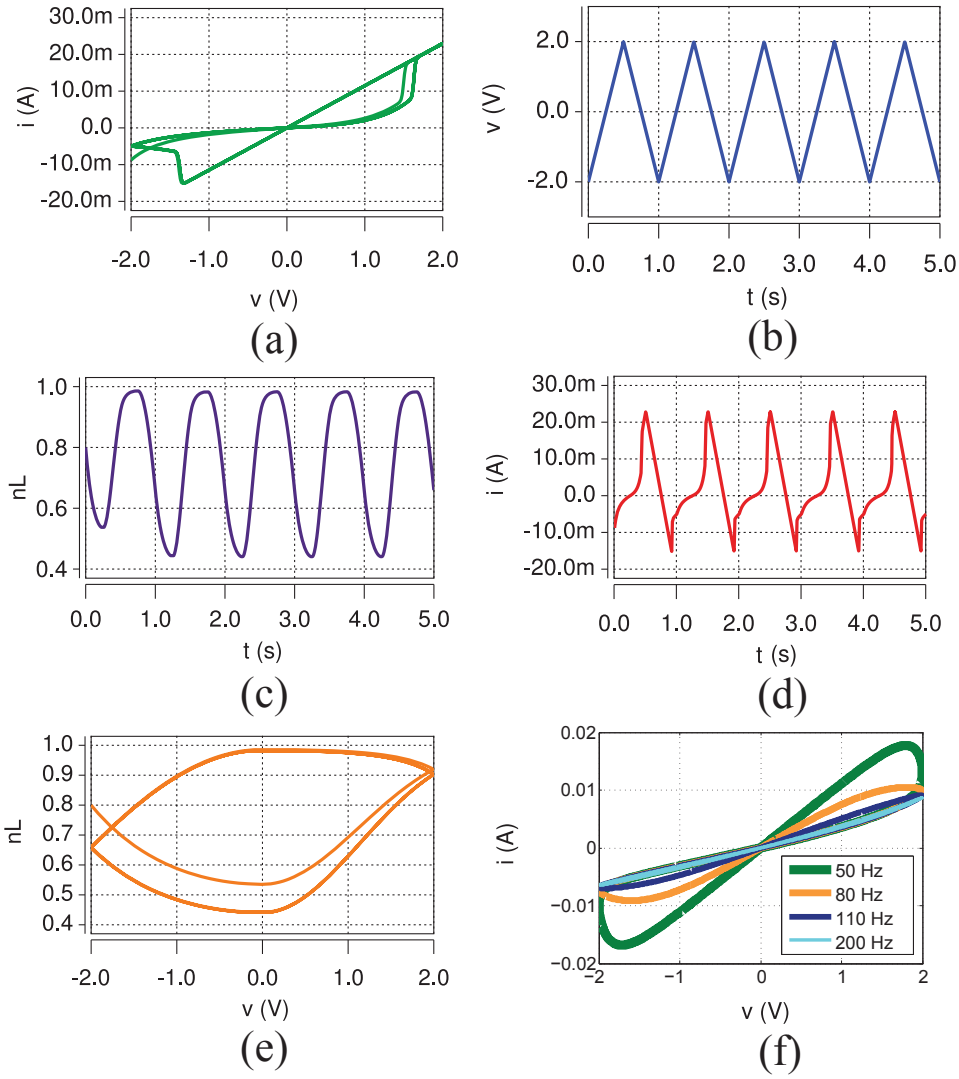

Figure 2.7: These plots illustrate the fabricated Ag/TiO_2/ITO memristor's accurate modeling and SPICE simulation. The plot in (a) shows that the i-v curve demonstrates a close match to the experimental data and (b) the triangular input voltage. The plot in (c) displays the behavior of the n_L parameter versus time and (d) shows the memristor current. The plot (e) shows the behavior of the n_L parameter versus voltage. Lastly (f) plot displays the Ag/TiO_2/ITO memristor model behavior for a ± 1 V sinusoidal input voltage of different frequencies.

The memristor current is determined through,

$$i_{\text{mem}} = \text{Tran\_func}(n_L) i_{\text{Tunn}}(V) + (1 - \text{Tran\_func}(n_L))\, i_{\text{Ohmic}}(V). \tag{2.22}$$

To implement first and second part of (2.22) two corresponding voltage controlled current sources, `Gtunn` and `Gohmic` are used. The node n_L is used to view the quantity of oxygen deficiency near Schottky barrier. The SPICE model code is written for an HSPICE as shown in Table 2.2. It is worth noting that simulator internal limits can affect the simulation results of the model, so careful attention to these limits should be taken into consideration when implementing the model with a specific simulator. If this appears to be an issue with a specific simulator, a lower capacitance value (e.g. 1 mF, 1 μF or 1 nF) can be utilized. Subsequently, there is a need to multiply the scaled coefficient (e.g. scaled coefficient for 1 mF is 0.001) with dependent current source `Gn` in the SPICE code and it does not affect the functionality of the coded models. Also this model can be used for other VCM memristors such as Pt/TiO_2/Pt device [2], Pt/Hf/Ti memristor [33], or this $SrTiO_3$-based device [34] by changing the aforementioned parameter values according to the physical properties of each of these devices. The results for modeling these devices are displayed in Fig. 2.6. In the SPICE code, the parameters are categorized into three groups: constants, physical parameters, and setting parameters. The constants are independent of memristor construction e.g. Boltzmann constant, electron charge, and others. The physical parameters vary for each memristor design, and these parameters can be obtained through the physical properties of each memristor e.g. thickness, mobility and others. The third category is the setting parameters. These parameters should be adjusted based on the experimental data for the fabricated memristors. The setting parameters are `bn`, `S`, `Zeta` and `aM` and last two parameters definition is given by (11) and (12), respectively. Also `bn` and `S` are parameters to control switching speed between the HRS and the LRS. The SPICE simulation for a triangular 2 V input pulse with a frequency of 1 Hz shows the same behavior as the

experimental data for Ag/TiO_2/ITO memristor. This simulation for a single triangular input pulse is demonstrated in Fig. 2.7. The simulation shows about 0.25 RMS error compared to experimental data. The proposed model also showed an appropriate behavior toward the alteration in frequency as seen in Fig. 2.7(f). By increasing the frequency, the hysteresis loop shrinks. Four sinusoidal shaped ± 1 V input voltages with different frequencies were applied to the model. When the 200 Hz frequency input voltage is used, the i-v curve diminishes to a single-valued curve. Also this model is tested for several input voltages with various amplitudes and shapes. In Fig. 2.8 the proposed SPICE model is simulated for three different input voltage waveforms, sinusoidal, triangular, and pulsed.

2.6 Memristor Model With Charge Transport Mechanisms (CTM) Analysis

For analyzing the CTM model, charge transport mechanism for different regions of i-v curve in Fig. 2.4 should be assessed. In region 1, the bias voltage imposed on the memristor is negative. As a result, the oxygen deficiencies remain in the TiO_{2-x} region. At this point, the length of the undoped region is at its largest value and the voltage barrier is high. The only way for electrons to migrate through the Schottky barrier is by tunneling and thermionic emission. This state is called the High Resistance State (HRS). Although the tunneling distance is high, some electrons can tunnel through the TiO_2 interface and migrate from the ITO electrode to the doped region. Also electrons can go through the barrier by gaining sufficient thermal energy from the ambient and pass the Schottky barrier. The newly arrived electrons start to move through the doped region according to the Poole-Frenkel current mechanism [35]. The oxygen deficiencies behave like traps for the electrons. So the electrons start their short hopping in this region until they reach to the other end of the doped region. Moreover, since $\mathrm{Ag/TiO_{2-x}}$ is the ohmic contact, these electrons can travel to the Ag electrode by an ohmic mechanism. By increasing the bias

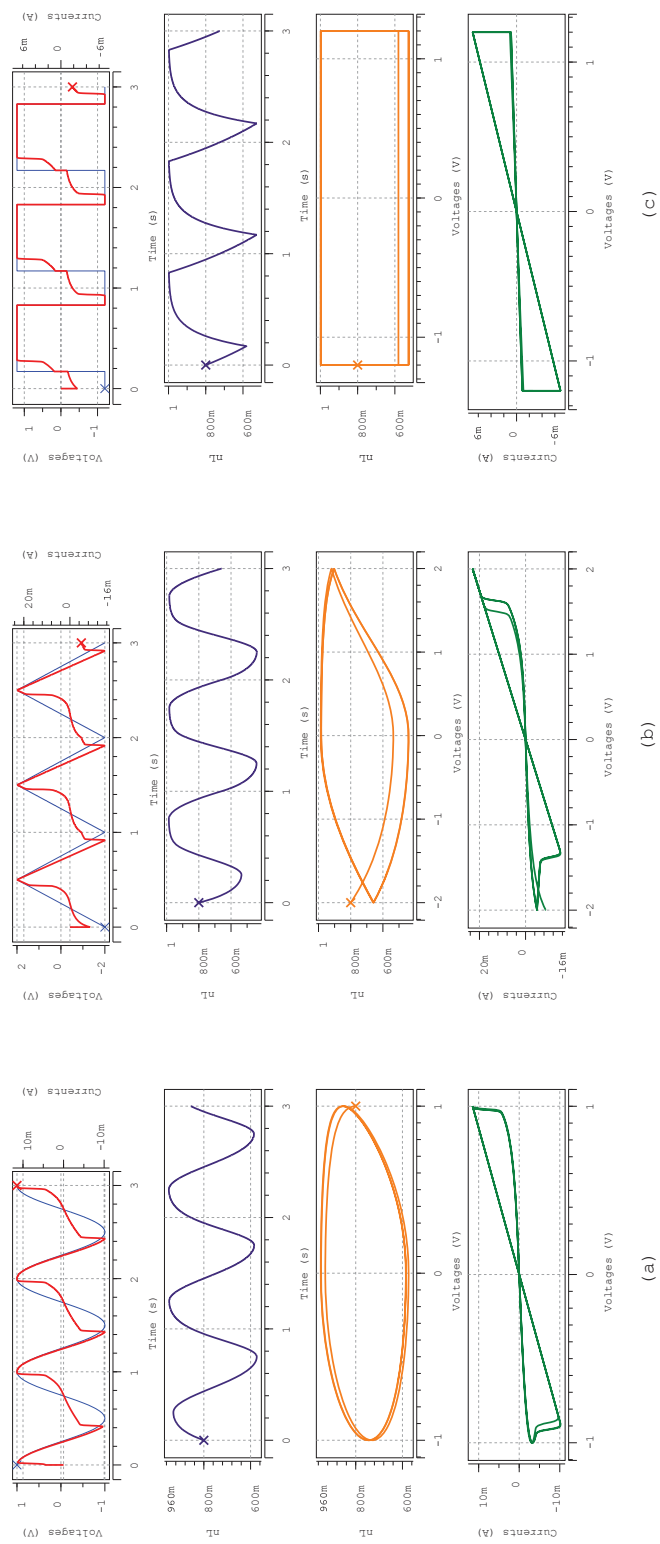

Figure 2.8: The Ag/TiO_2/ITO memristor's accurate model is simulated for three input waveforms. The first row shows subplot for different input voltages and currents of the memristor. The second and third rows of subplot shows the number of oxygen deficiencies near the Schottky barrier versus time and voltage, respectively. The lowest shape illustrates the $i - v$ curve. In (a) a 1 Hz frequency sinusoidal input pulse with 2 V peak to peak amplitude and 0 V DC offset voltage is used, in (b) a ± 2 V triangular input pulse with a 1 Hz frequency is used, and in (c) a ± 1.2 V square input pulse with a 1 Hz frequency is used.

voltage, the induced electric field forces the oxygen deficiencies to migrate further through the undoped region of TiO_2. Therefore, the width of the voltage barrier in the Schottky region is diminished. This phenomenon results in easier tunneling of the electrons from the ITO electrode through the undoped TiO_2 interface to the doped region of $\mathrm{TiO_2}$. Subsequently, surpassing the threshold voltage of the device places the memristor in its lowest resistance (R_{ON}). After reaching $+1.5$ V, the dopants are gradually spread all over the undoped region. In region 3, the quantity of the oxygen deficiencies near the Schottky barrier region reaches its maximum level and the ohmic contact is going to be shaped between the TiO_{2-x} and ITO electrode. Therefore, the ohmic current mechanism gradually becomes dominant over tunneling in this region. The memristor's state switches from the HRS to the Low Resistance State (LRS) and the ohmic current mechanism becomes dominant at the end of region 3 by reaching $+2$ V voltage over the device. In region 4, the voltage is decreased from $+2$ V to 0 V. In this domain, since the voltage is still positive the oxygen deficiencies are placed near the ITO electrode and remain immobile. Therefore, the whole dielectric length is still doped and ohmic current is the main charge transport mechanism. By entering region 5, the voltage across the memristor becomes negative. Thus, by reversing electric field, the oxygen deficiencies are forced to get back to the left side of the $\mathrm{TiO_2}$ thin film. Shaping a new Schottky barrier is time consuming. Although the oxygen deficiencies commence their movement to the left side of the TiO_2 thin film, the current mechanism remains ohmic until the undoped region is shaped. As the voltage is decreased to -1.4 V, a voltage barrier is going to be created at the Schottky region and the current mechanism is gradually altered to tunneling and thermionic emission. In region 6, the undoped region is shaped progressively. As ohmic current is reduced and the undoped zone is shaped little by little, the majority of the traveling electrons are tending to move from the ITO electrode to the doped region of $\mathrm{TiO_2}$ through tunneling or by passing the barrier by gaining enough thermal energy. As these electrons are enter the $\mathrm{TiO_{2-x}}$ region, the oxygen deficiencies act like the traps for the newly arrived electrons in the doped region. Subse-

quently, the electrons migrate through the remaining length of the doped $\mathrm{TiO_2}$ through the Poole-Frenkel mechanism. As can be seen in Fig. 2.4, this model shows high accuracy in comparison with the experimental data for the Ag/TiO_2/ITO memristor fabricated in [4]. To compare simulated and experimental data, relative Root Mean Square (RMS) error is utilized. This error can be determined by,

$$e_{v,i} = \sqrt{\frac{1}{N}\left(\frac{\sum_{n=1}^{N}(v_{s,n}-v_{r,n})^2}{\bar{v}_r^2} + \frac{\sum_{n=1}^{N}(i_{s,n}-i_{r,n})^2}{\bar{i}_r^2}\right)}, \tag{2.23}$$

where $\bar{v}_r$ and $\bar{i}_r$ are the mean values of the reference (experimental) data for voltage and current, respectively. Also v_s and i_s are the voltage and current extracted from the model simulation data. By comparing the proposed model with the experimental data, a relative RMS error was obtained that is considerably less than that of the other models. The relative RMS errors of some previous models (when modeling the experimental data from the $\mathrm{Ag/TiO_2/ITO}$ memristor) are calculated and presented in Table 2.3. The memristor-based circuit configuration in Fig. 2.4 is utilized to determine the relative RMS errors. The fitting parameters for the Simmons and TEAM models were selected for the best fitting accuracy while considering simulation convergence issues. A detailed study of several previous models' performance and optimization was completed in [36]. The semi-physical model [4] is used to simulate the $\mathrm{Ag/TiO_2/ITO}$ memristor device i-v characteristic by simplifying mathematical the equations extracted from the physical assumptions of memristor behavior when only considering tunneling current. Therefore, the memristor behavior in regions 3, 4 and 5 are not simulated accurately. This makes, this model vulnerable to error when simulating memristor device behavior. While the proposed model considered an ohmic current mechanism for those regions of the i-v curve. This results in accurate modeling for all regions based on the charge transport mechanisms in memristor devices. Also, the proposed CTM model shows good behavior when modeling the curvature of the OFF state in the i-v curve and it has a slightly smaller RMS error in comparison with the

generalized model.

2.7 Conclusion

In this chapter, a SPICE-based model that utilizes a charge transport mechanisms of memristor devices is proposed. Various modeling techniques are discussed. The proposed model considers the memristor as a special MIM device that uses transition oxides for its insulator. This memristor model is based on two main current mechanisms in the Schottky barrier region namely: tunneling and ohmic currents. These currents are selected as the dominant currents within the device based on the quantity of oxygen vacancies that exist near the Schottky barrier region. The SPICE code was defined for the proposed model. The applicability of the code was tested with various input voltages with different amplitudes and frequencies. The proposed model shows about 0.25 relative RMS error in comparison with the experimental data when simulated in MATLAB for the fabricated Ag/TiO_2/ITO memristor. Existing models in the literature were also used to simulate the Ag/TiO_2/ITO memristor and their accuracies were determined. The proposed model fit other VCM devices as well.

Table 2.3: The relative root mean square errors of various memristor models with the experimental data collected for Ag/TiO_2/ITO memristor as ± 2 V, 1 Hz triangular wave input voltage applied to the device.

Model	**Parameters**	**RMS error**
Linear Ion Drift [2] + Window Function [5]	D = 22 nm, R_{init} = 172 Ω, R_{ON} = 85 Ω, R_{OFF} = 1300 Ω, $\mu_{\text{v}} = 10^{-14}$ m^{2}s^{-1}V^{-1}, $p = 1$	2.53
Linear Ion Drift [2] + Window Function [6]	D = 22 nm, R_{init} = 172 Ω, R_{ON} = 85 Ω, R_{OFF} = 1300 Ω, $\mu_{\text{v}} = 10^{-14}$ m^{2}s^{-1}V^{-1}, $p = 1$	2.95
Linear Ion Drift [2] + Window Function [7]	D = 22 nm, R_{init} = 172 Ω, R_{ON} = 85 Ω, R_{OFF} = 1300 Ω, $\mu_{\text{v}} = 10^{-14}$ m^{2}s^{-1}V^{-1}, $p = 1, j = 2$	2.36
Nonlinear Ion Drift [8] + Window Function [5]	D = 22 nm, R_{init} = 172 Ω, R_{ON} = 85 Ω, R_{OFF} = 1300 Ω, $\mu_{\text{v}} = 10^{-14}$ m^{2}s^{-1}V^{-1}, $p = 1$, $\vartheta = 0.015$, $\beta = 0.75$, $y = 0.002$, $\chi = 0.001, n = 2$	1.53
Nonlinear Ion Drift [8] + Window Function [6]	D = 22 nm, R_{init} = 172 Ω, R_{ON} = 85 Ω, R_{OFF} = 1300 Ω, $\mu_{\text{v}} = 10^{-14}$ m^{2}s^{-1}V^{-1}, $p = 1$, $\vartheta = 0.015$, $\beta = 0.75$, $y = 0.002$, $\chi = 0.001, n = 2$	1.71
Nonlinear Ion Drift [8] + Window Function [7]	D = 22 nm, R_{init} = 172 Ω, R_{ON} = 85 Ω, R_{OFF} = 1300 Ω, $\mu_{\text{v}} = 10^{-14}$ m^{2}s^{-1}V^{-1}, $p = 1$, $j = 2$, $\vartheta = 0.015$, $\beta = 0.75$, $y = 0.002$, $\chi = 0.001, n = 2$	1.49
TEAM [18]	$a_{\text{ON}} = 20$ nm, $a_{\text{OFF}} = 15$ nm, $\alpha_{\text{ON}} = 3, \alpha_{\text{OFF}} = 3, k_{\text{ON}} = -1 \times 10^{-13}$ nm/s, $k_{\text{OFF}} = -26 \times 10^{-12}$ nm/s, $i_{\text{ON}} = 70\ \mu$A, $i_{\text{OFF}} = 480\ \mu$A, $x_{\text{OFF}} = 22$ nm, $x_{\text{ON}} = 0$ nm	1.28
Simmons Tunnel Barrier [9]	$a_{\text{ON}} = 20$ nm, $a_{\text{OFF}} = 15$ nm, $f_{\text{ON}} = -0.1$ nm/s, $f_{\text{OFF}} = -0.3$nm/s, $i_{\text{ON}} = 70\mu$A, $i_{\text{OFF}} = 480\mu$A, $w_{\text{c}} = 530$pm, $b = 500\mu$A	0.95
Semi-Physical Model [4]	$\eta_{\text{ON}} = 22, \eta_{\text{OFF}} = 28, p = 5, a = 1.2 \times 10^{-2}, b = 4.3 \times 10^{-6}, c_1 = 3.3 \times 10^{-4}, c_2 = 4.8 \times 10^{-4}, d_1 = 2.1, d_2 = 1.6, v = 4 \times 10^{-3}$	0.53
Generalized Memristor Model [20]	$V_p = 1.5$ V, $V_n = 0.5$ V, $A_p = 0.005, A_n = 0.08, x_p = 0.8, x_n = 0.5, a_p = 10, a_n = 40, a_1 = 0.227, a_2 = 0.227, b = 0.05, x_0 = 0.25, \eta = 1$	0.46
This Work	L = 22 nm, T = 300 K, n_{th} = 0.82, n_1 = 0.8, ΔE = 0.11, $E_0 = 9 \times 10^{-7}$, E_{000} = 2.4, N_D = 100, N_C = 900, α = 0.95, ζ = 0.06, S = 350	0.25

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Chapter 3

Brain-inspired Memristive Neural Network Using Hodgkin-Huxley Neuron

RECENT findings on utilizing memristor devices that mimic biological synapses in neuromorphic systems opens a new vision in neuroscience. Ultra-dense learning architectures can be implemented through Spike-Timing-Dependent-Plasticity (STDP) learning mechanism by exploiting these nanoscale nonvolatile devices. In this chapter, Spiking Neural Network (SNN) which uses biological plausible mechanisms is implemented. The proposed SNN is utilized Hudgkin Huxley neuron and memristive synapse as two perfect biological plausible candidates for implementation of a bio-inspired neuromorphic platform similar to brain. The behavior of the proposed SNN and its learning mechanism is discussed. Finally, the proposed design is successfully tested for pattern classification application.

3.1 Introduction

Spiking Neural Networks (SNNs) have demonstrated good potential for the wide range of applications like pattern recognition, clustering and computations. The SNN promises a

perfect generation of Artificial Neural Network (ANN) that can be comparable in terms of efficiency in processing information to its biological counterparts. Today, this may be a lost part of the hardware puzzle due to the growing needs for high volume data processing in the coming era of bioinformatics. Emerging memristor devices due to their analog memory property mimics biological synapses. These two terminal resistive switching devices attracted intensified research on several applications like memory [1], logic implementation[2][3][4], neural network [5] and neuromorphic computing [6][7]. It was shown in [8] memristor devices due to their adaptive behavior can reproduce Spike-Timing-Dependent-Plasticity (STDP) feature which is the main learning scheme in the brain.

There are several works that have been published on implementation of SNN using STDP learning scheme in most of these works they utilized simple Leaky Integrate and Fire (LIF) neuron for their structure [6][7]. Using a biological neuron model can give better insight of real brain-inspired SNN. Hudgkin Huxley neuron model [9] as one of the pioneer models in the literature defines the ionic mechanisms underlying the initiation and propagation of action potentials in the squid giant axon.

In this chapter, a memristor-based SNN is implemented by using Hudgkin Huxley neuron and STDP learning scheme is applied for its learning. The proposed SNN contains Hudgkin Huxley neurons as its neuron block and it also utilizes current controlled memristor device as synapse. Basic pattern recognition application is also applied to the proposed SNN to test its functionality.

Rest of this chapter is organized as follows. In section II Hudgkin Huxley neuron is defined. The STDP learning with memristor synapse is explained in section III. The proposed SNN structure and its behavior are described in Section IV. In section V the pattern classification results are presented. Finally in section VI conclusion and remarks are provided.

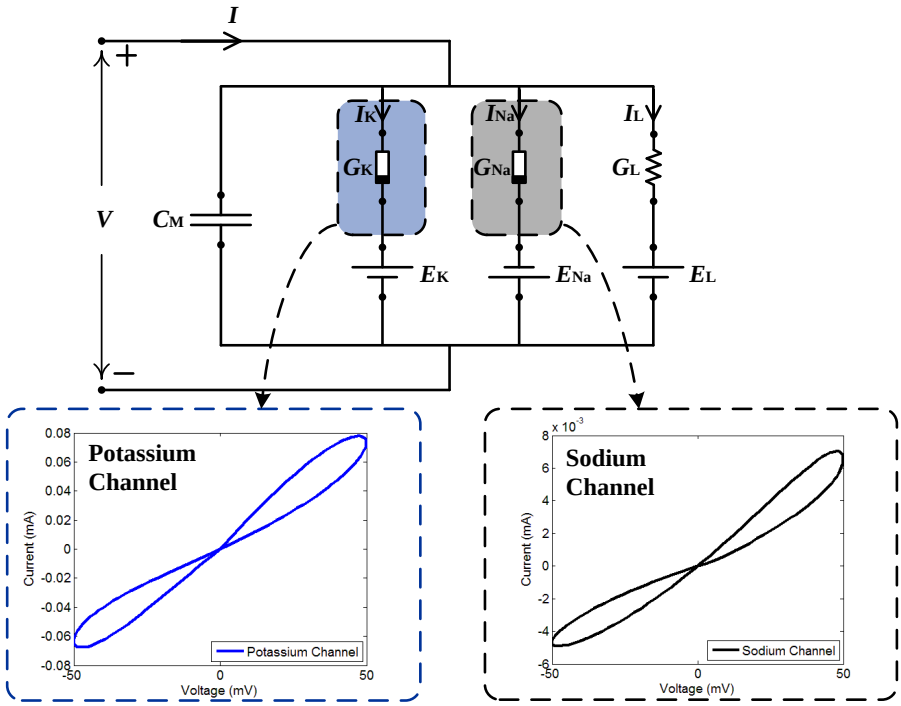

Figure 3.1: Equivalent memristive circuit schematic for Hudgkin Huxley neuron model. The I-V curves for memristor devices that model sodium and potassium channels are displayed.

3.2 Hudgkin Huxley Neuron

Understanding brain function as one of the most attractive topics in neuroscience can lead to finding new treatment for brain disease. Therefore it is crucial to model biological mechanism in brain specifically for the neurons and synapses. In recent years, several different neuron models have been presented. These models can be categorized into conductance-based models with biological precision and spiking-based models, that describe temporal behavior of cortical spike train. Hudgkin Huxley model [9] is one of the first conductance-based accurate neuron models that can explain biological mechanisms of neuronal behavior better than its other counterparts. In 1952 Hudgkin and Huxley by series of experiments demonstrated that the ionic currents in squid giant axon can be determined by considering change of the conductances of Sodium and Potassium ions in the axon membrane [12]. Their understanding lead to development of a coupled set of differential equations that be-

came known as Hudgkin Huxley neuron model. This model can accurately reproduce all the key biophysical properties of action potential. The electrical properties of this neuron can be presented in terms of an electrical equivalent circuit. The current across the membrane consist of the two major parts. One is associated with membrane capacitance and the other one is the current generated by flow of ions in the resistive channels. The equation of Hudgkin Huxley neuron model [9] can be written as,

$$I = C_{\mathrm{M}}\frac{dV}{dt} + I_{\mathrm{ionic}}. \tag{3.1}$$

Where I, V and C_{M} are the total membrane current, membrane potential and membrane capacitance respectively. $I\mathrm{ionic}$ is the total ionic current. This current includes currents of Sodium, Potassium and leakage channels. The ionic current can be determined by,

$$I_{\mathrm{ionic}} = I_{\mathrm{Na}} + I_{\mathrm{K}} + I_{\mathrm{L}}, \tag{3.2}$$

$$I_{\mathrm{Na}} = g_{\mathrm{Na}}(V - E_{\mathrm{Na}}), \tag{3.3}$$

$$\text{where} \qquad g_{\mathrm{Na}} = \bar{g}_{\mathrm{Na}} m^3 h, \tag{3.4}$$

$$I_{\mathrm{K}} = g_{\mathrm{K}}(V - E_{\mathrm{K}}), \tag{3.5}$$

$$\text{where} \qquad g_{\mathrm{K}} = \bar{g}_{\mathrm{K}} n^4, \tag{3.6}$$

$$I_{\mathrm{L}} = g_{\mathrm{L}}(V - E_{\mathrm{L}}), \tag{3.7}$$

where I_{Na}, I_{K} and I_{L} are related to currents in Sodium, Potassium and Leakage channels respectively. These currents passes Sodium, Potassium and leakage channels with g_{Na}, g_{K} and g_{L} conductances respectively. E_{Na}, E_{K} and E_{L} are the equilibrium potential for each

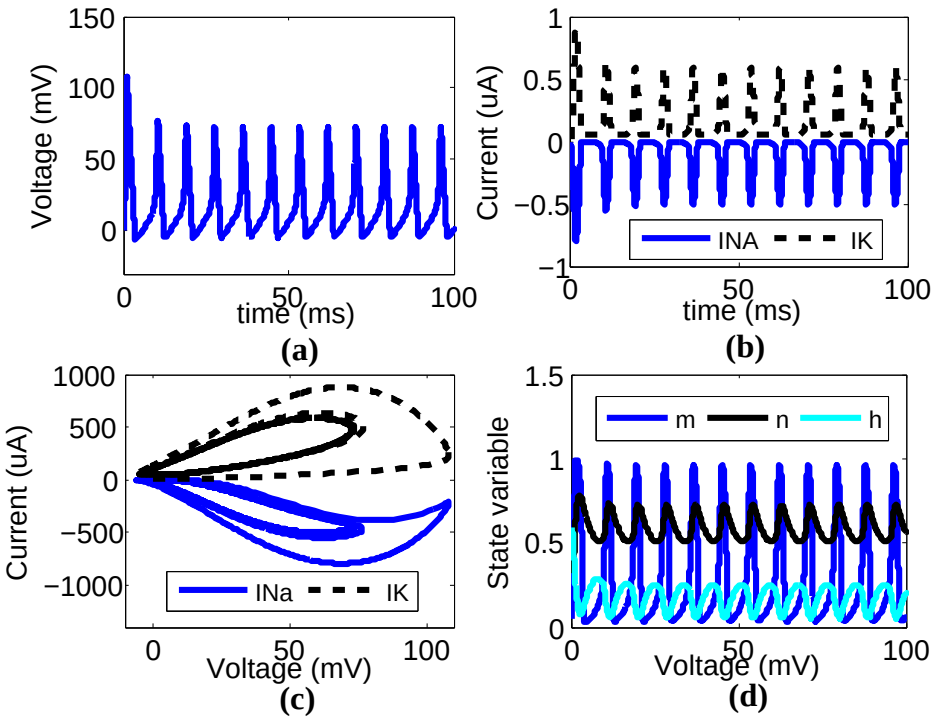

Figure 3.2: (a) Hudgkin Huxley membrane voltage for 15 $\mu\mathrm{A}/\mathrm{cm}^2$ stimulus current. (b) Sodium and potassium channel currents. The parameters were taken from original paper [9]. (c) Sodium and potassium channel currents versus membrane voltage. (d) Hudgkin Huxley neuron state variables behavior.

channels. The $\bar{g}_{\mathrm{Na}}$ and $\bar{g}_{\mathrm{K}}$ parameters are constants which are determined experimentally to fit biophysical properties of neuron action potential. m, n and h are state variables to control conductance of Sodium and Potassium channels. The state variables value altered between 0 to 1. The state variables can be determined by,

$$\frac{dn}{dt} = a_{\mathrm{n}}(1-n) - b_{\mathrm{n}}n, \tag{3.8}$$

$$a_{\mathrm{n}} = 0.01\frac{V+10}{e^{(\frac{V+10}{10}-1)}}, \tag{3.9}$$

$$b_{\mathrm{n}} = 0.125e^{(\frac{V}{80})}, \tag{3.10}$$

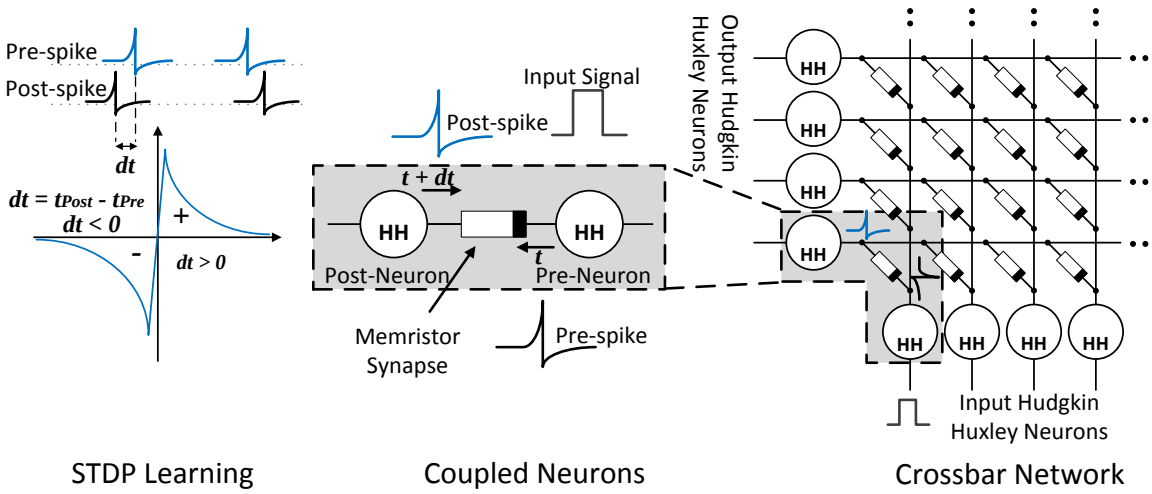

Figure 3.3: STDP learning mechanism is illustrated for two coupled neurons with a memristive synapse in proposed SNN architecture. The memristive crossbar array of synapses are connected to Hudgkin Huxley neurons.

$$\frac{dm}{dt} = a_{\mathrm{m}}(1-m) - b_{\mathrm{m}}m, \tag{3.11}$$

$$a_{\mathrm{m}} = 0.1\frac{V+25}{e^{(\frac{V+25}{10}-1)}}, \tag{3.12}$$

$$b_{\mathrm{m}} = 4e^{(\frac{V}{18})}, \tag{3.13}$$

$$\frac{dh}{dt} = a_{\mathrm{h}}(1-h) - b_{\mathrm{h}}h, \tag{3.14}$$

$$a_{\mathrm{h}} = 0.07e^{(\frac{V}{20})}, \tag{3.15}$$

$$b_{\mathrm{h}} = (e^{(\frac{V+30}{10})}+1)^{-1}, \tag{3.16}$$

The memristive circuit equivalent with Hudgkin Huxley neuron model has been defined by professor Leon Chua recently [10]. He showed the currents in sodium and potassium channels are similar to currents pass through specific memristor devices. The sodium and potassium channels current-voltage curves are displayed in Fig. 3.1 for 50 mV sinusoidal membrane voltage with 500 Hz frequency. The memristive equivalent electrical circuit is depicted in Fig. 3.1. Fig. 3.2 displays an example waveform of Hudgkin Huxley neuron for

Table 3.1: Scaled Hudgkin Huxley neuron parameters.

Parameters	Value	Parameters	Value	Parameters	Value
$\bar{g}_{\mathrm{Na}}(\mathrm{mScm}^{-2})$	6	E_{NA}(V)	2.3	C_{M}(nF)	50
$\bar{g}_{\mathrm{K}}(\mathrm{mScm}^{-2})$	1.8	E_{K}(mV)	-240		
$\bar{g}_{\mathrm{L}}(\mathrm{mScm}^{-2})$	0.015	E_{L}(mV)	212		

Table 3.2: Memristor device parameters for simulation.

Parameters	R_{LRS}	R_{HRS}	L	μ_v	V_{tp}	V_{tn}
Units	Ω	KΩ	nm	m^2/Vs	V	V
Values	100	40	3	9×10^{-13}	1.5	-1.5

$15\ \mu\mathrm{A/cm}^2$ stimulus current.

3.3 STDP Learning Mechanism with Memristor Synapses

STDP is a learning mechanism that is discovered in live neurons and elucidates cortical phenomena better than Hebbian correlation-based plasticity. This mechanism is based on time difference of arrival spikes from pre-synaptic and post-synaptic neurons. Unlike Hebbian learning mechanism STDP is capable of generating both Long Term Potentiation (LTP) and Long Term Depression (LTD) phenomenons. LTP results in increasing the synaptic strength or weight of the synapse W and it happens when post-synaptic neuron spikes after pre-synaptic neuron ($t_{\mathrm{post}} - t_{\mathrm{pre}} \geq 0$). On the other hand, in LTD the synaptic strength is decreased and it happens when pre-synaptic spike comes after post ($t_{\mathrm{post}} - t_{\mathrm{pre}} < 0$).

Memristive nanodevices have variable resistance and they can transmit spikes with variable conductance (or weight). When a positive voltage higher than device positive threshold (V_{tp}) is applied to memristive synapse, there will be an increase in its conductance. When a negative voltage smaller than device negative threshold (V_{tn}) is applied to memristive synapse, its conductance will be decreased. Memristor synapses can implement STDP bet-

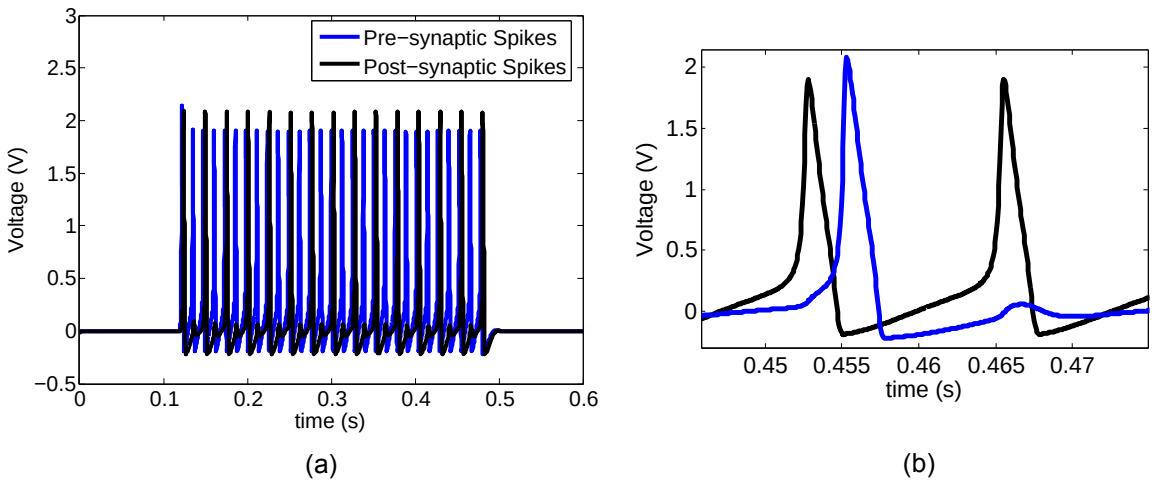

Figure 3.4: The membrane voltage of pre and post synaptic Hudgkin Huxley neurons connected with memristive synapse for 15 $\mu\mathrm{A}/\mathrm{cm}^2$ stimulus current.

ter than the other elements. In Fig. 3.3 STDP learning mechanism is illustrated for proposed SNN with memristive synapses.

3.4 Proposed SNN Architecture and Behaviour

The proposed SNN is utilizing voltage controlled memristors (VCM) as synapses and Hudgkin Huxley neurons as neuron blocks. The Hudgkin Huxley neuron parameters were scaled around 2 V to have biological plausible shape of spike for proposed SNN. The applied parameters for proposed Hudgkin Huxley neuron are defined in Table 1. For analyzing the behavior of the proposed SNN architecture, at first dynamic behavior of two coupled Hudgkin Huxley neurons connected with memristive synapse should be assessed. A voltage of memristive synapse's input terminal which is connected to pre-synaptic Hudgkin Huxley neuron is determined by,

$$C_{\mathrm{M}}\frac{dV_{\mathrm{pre}}}{dt} = \bar{g}_{\mathrm{Na}}m^3h(V_{\mathrm{pre}} - E_{\mathrm{Na}}) + \bar{g}_{\mathrm{K}}n^4(V_{\mathrm{pre}} - E_{\mathrm{K}}) + \bar{g}_{\mathrm{L}}(V_{\mathrm{pre}} - E_{\mathrm{L}}) - I_{\mathrm{applied}}. \tag{3.17}$$

The parameter V_{pre} is pre-synaptic neuron's membrane voltage. The I_{applied} is the input current to pre-synaptic neuron. The amplitude of input current for proposed Hudgkin Huxley neuron is 15 $\mu\mathrm{A/cm}^2$. On the other hand, the post-synaptic neuron input current is the current which passes memristive synapse. The membrane voltage of the post-synaptic neuron in two coupled Hudgkin Huxley neurons network can be determined by,

$$C_{\mathrm{M}}\frac{dV_{\mathrm{post}}}{dt} = \bar{g}_{\mathrm{Na}}m^3h(V_{\mathrm{post}} - E_{\mathrm{Na}}) + \bar{g}_{\mathrm{K}}n^4(V_{\mathrm{post}} - E_{\mathrm{K}}) + \bar{g}_{\mathrm{L}}(V_{\mathrm{post}} - E_{\mathrm{L}}) - I_{\mathrm{syn}}. \tag{3.18}$$

The parameter V_{post} is membrane voltage of the post-synaptic neuron. The I_{syn} is the current in memristive synapse. The memristive synapse is changing its conductance continuously as the applied voltage over the device (V_{post} - V_{pre}) exceeds the device threshold. The synaptic current is determined based on the memristive device model properties. Here linear boundary ion drift model is applied for simulation. The parameters of the utilized memristor is defined in Table 2. The synaptic current I_{syn} can be determined through,

$$I_{\mathrm{syn}}(t) = \frac{V_{\mathrm{post}}(t) - V_{\mathrm{pre}}(t)}{R_{syn}(w)}, \tag{3.19}$$

$$R_{syn}(w) = R_{LRS}\frac{w(t)}{L} + R_{HRS}(1 - \frac{w(t)}{L}), \tag{3.20}$$

$$\frac{dw}{dt} = \frac{\mu_v R_{LRS}}{L^2} \times I_{syn}(t) \times f(w), \tag{3.21}$$

$$f(w) = \left(1 - 2\left(\frac{w(t)}{L}\right)\right)^{2p}. \tag{3.22}$$

The parameter $f(w)$ is the window function [11] and p is a constant. The behavior of two coupled Hudgkin Huxley neurons with memristive synapse is illustrated in Fig. 3.4 for 15 $\mu\mathrm{A}$ input current. The proposed SNN can be utilized for pattern classification application. The proposed learning scheme is unsupervised as classification occurs based on the patterns given to input neurons. The output neurons represents a cluster and the center of each cluster is targeted by weights of connected synapses to each output neuron. When an input

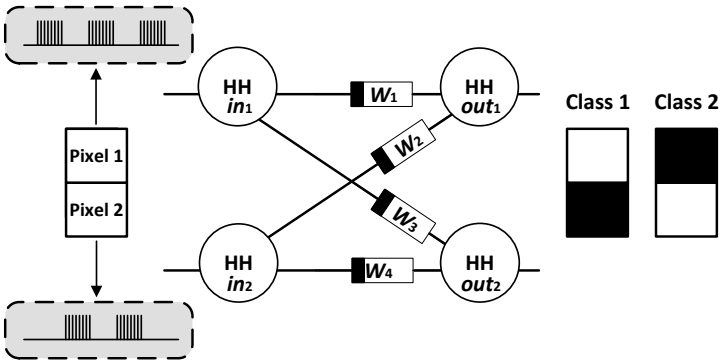

Figure 3.5: 2×2 network architecture of the proposed SNN. The input patterns for the proposed network are defined.

patterns applied to the input neuron one of the output neurons becomes a winner due to the combination of connected synaptic weights. The weight vector of the winner output neuron is the closest one to the input pattern vector.

3.5 Pattern Classification Results

3.5.1 2×2 Proposed SNN

The 2×2 network is implemented with two input and two output Hudgkin Huxley neurons. These neurons are connected with four memristive synapses. This network is utilized to classify between two patterns. These patterns are two pixel images with class 1 and 2. Pixel 1 and pixel 2 are applied as inputs to pre-synaptic neuron 1 and pre-synaptic neuron 2 respectively. The proposed network is illustrated in Fig. 3.5.

As it can be seen in Fig. 3.6 the post-synaptic neurons are spiking at first without any specific pattern. It takes some times for post-synaptic neurons to follow the input patterns. The learning is unsupervised and the winner neuron follows one of the patterns due to its initial weight vector. When the image with class 2 assigned to post-synaptic neuron 1, the weight of the memristive synapse 1 increases due to STDP mechanism. Since post-

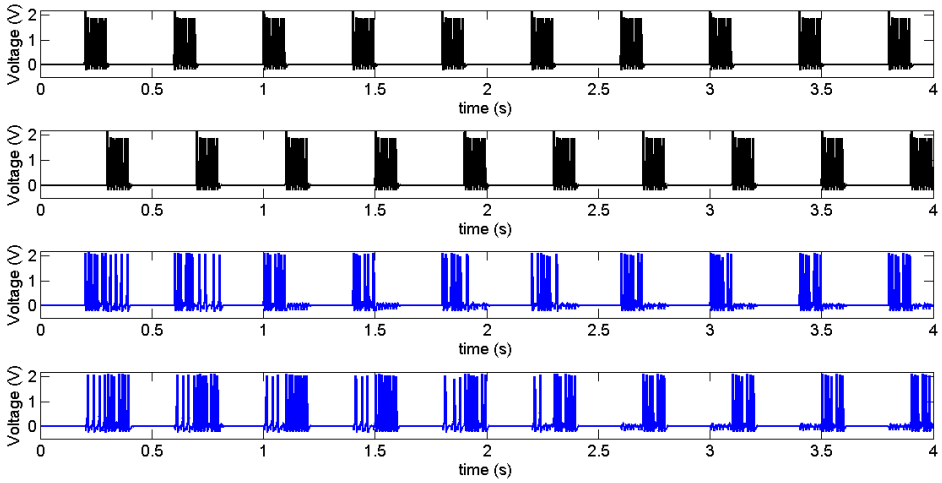

Figure 3.6: The membrane voltage of the pre synaptic (black curve) and post synaptic (blue curve) neurons for 2×2 network. The proposed network classifies the patterns successfully.

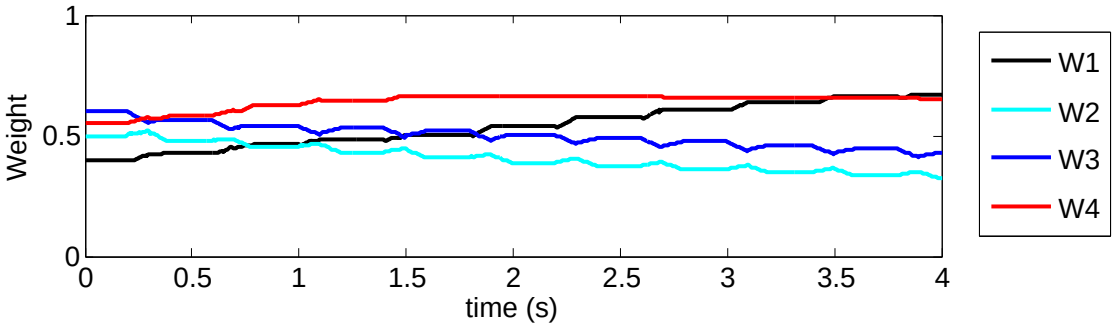

Figure 3.7: The weight evolution of the memristive synapse for 2×2 network.

synaptic neuron 1 spikes after pre-synaptic neuron 1 (black pixel has been applied to input neuron and make it spiking), the weight of the memristive synapse 1 increases. Also the memristive synapse 2 weight decreases since post-synaptic neuron 2 is inactive while the pre-synaptic neuron 1 spikes. The similar procedure is occurred for image with class 1. The input and output waves for proposed 2×2 SNN is displayed in Fig. 3.6. As it can be seen in Fig. 3.7 the memristive synapse weights W_1 and W_4 are increased and W_2 and W_3 are decreased for the proposed input patterns.

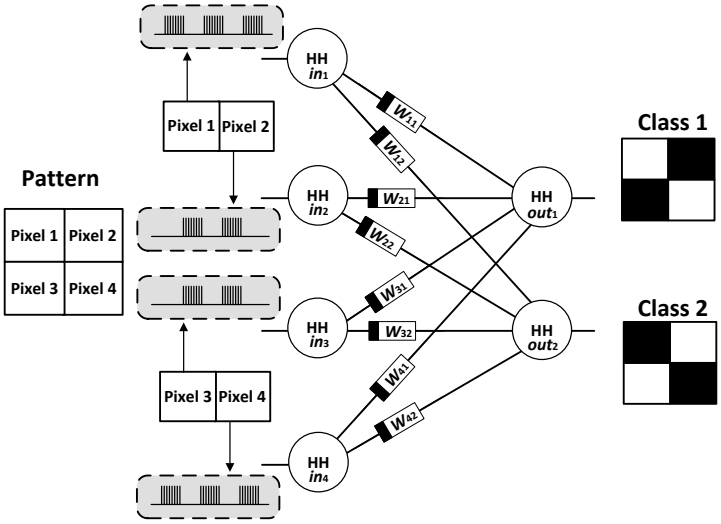

Figure 3.8: 4×2 network architecture of the proposed SNN. The input patterns for the proposed network are defined.

3.5.2 4×2 Proposed SNN

The 4×2 network of the proposed SNN is also implemented to classify between two four pixel images and it is illustrated in Fig. 3.8. The proposed network has been successfully tested as four pixels are applied as input to pre-synaptic neurons of the SNN. The input signals are displayed in Fig. 3.9. The proposed SNN output results with memristive synapses weight evolution are displayed in Fig. 3.10. The memristive synapses initial weights were randomly assigned. In the proposed network, image class 1 and class 2 are assigned to post-synaptic neuron 1 and post-synaptic neuron 2 respectively.

3.6 Conclusion

This chapter described a bio-inspired spiking neural network by utilizing Hudgkin Huxley neuron as one of the most accurate biological model. The proposed SNN uses memristive synapses and STDP online learning which provide closer match to biology for learning mechanism. The proposed SNN architecture and its learning mechanism explained in de-

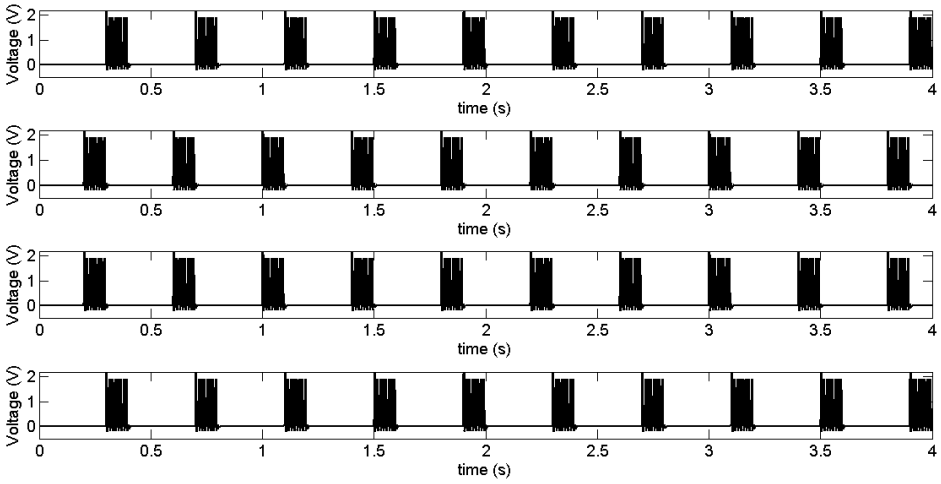

Figure 3.9: The membrane voltage of the pre-synaptic Hudgkin Huxley neurons.

tails. The proposed SNN small networks were successfully tested for pattern classification applications. The results showed close behavior to biology.

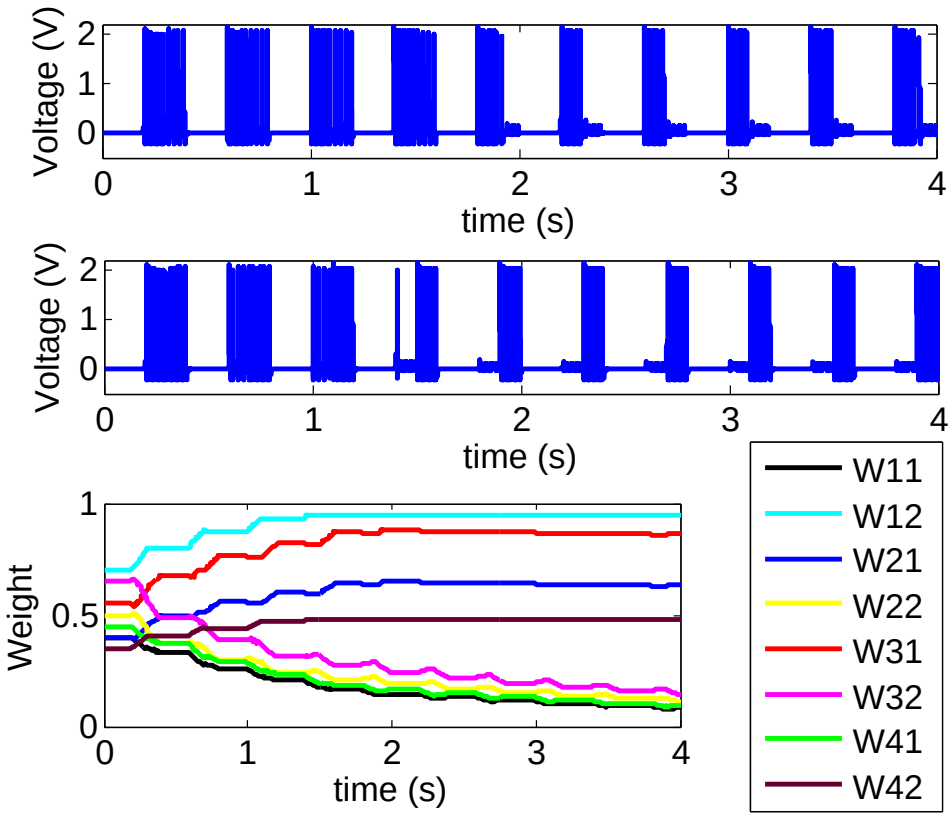

Figure 3.10: The membrane voltage of the post-synaptic Hudgkin Huxley neurons. The weights evolution of the memristive synapses are displayed in bottom graph.

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Chapter 4

STDP-based Memristive Spiking Neural Network Using Morris-Lecar Model

THESE days, there is an increasing interest in implementation of spiking neural systems that can be used to perform complex computations or solve pattern recognition tasks like mammalian neocortex. In this Chapter, Morris-Lecar neuron is utilized to implement bio-inspired memristive spiking neural network for unsupervised learning applications. The spike-Timing-Dependent-Plasticity (STDP) learning mechanism has been applied as the learning scheme in the system. The memristive implementation of the Morris-Lecar neuron has been analyzed. Also the memristors are utilized as the synapses for the proposed system. The proposed platform is tested for pattern classification applications and the results are successfully confirmed the functionality of it.

4.1 Introduction

Spiking Neural Network (SNN) is a promising generation of Artificial Neural Network (ANN) that can be comparable in terms of efficiency in processing information to its biological counterparts [1]. Today, this may be a lost part of the hardware puzzle due to the

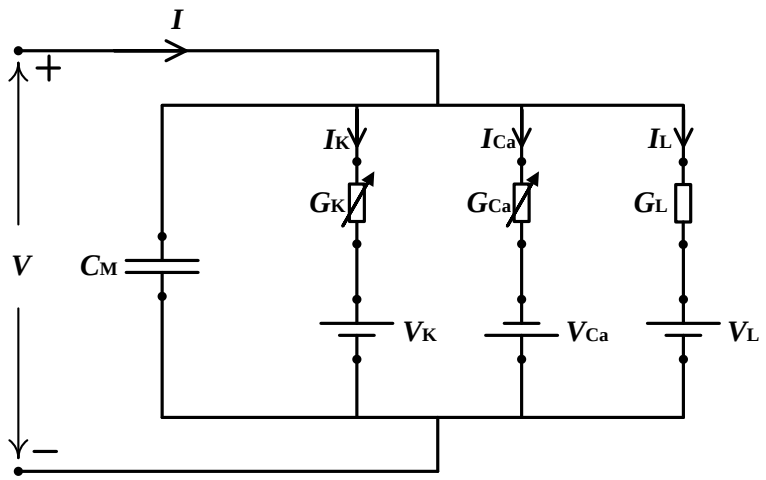

Figure 4.1: Equivalent circuit schematic for ML neuron model.

growing needs for high volume data processing in the coming era of bioinformatics [2]. In SNN, the presence and timing of individual spikes are considered as the main scheme for communication and neural computation [3]. Pulse-coupled neural networks with spike-timing are considered as a vital component in biological information processing systems, such as the brain. Understanding brain function, as one of the most attractive topics in neuroscience, can lead to discovery of new bio-inspired computing systems. Hence, it is crucial to model biological mechanism in brain specifically for the neurons and synapse to have a deeper understanding of brain information processing mechanisms.

In recent years, several different neuron models have been presented [4-9]. These models can be categorized into conductance-based models [4-7] with biological precision and spiking-based models [8-9], that describe temporal behavior of cortical spike train. Hudgkin-Huxley [4] is the pioneer of conductance-based model to describe the physiological mechanisms of neuronal behavior in central nervous system. Despite its high accuracy in defining a biological behavior of the neuron, it has a high computational cost for implementation due to its complexity. Thus, selecting a simpler model, which has a lower complexity and acceptable accuracy, is a viable alternative for low cost hardware implementation of bio-inspired neural systems.

Morris-Lecar (ML) model [7] is one of the computationally efficient conductance-based neuron models that offers a reasonable accuracy to produce biophysical behavior of neuronal activities. This model was developed to define the dynamics of the barnacle muscle fiber. The ML model includes a set of first order differential equations that reproduce the evolution of the membrane potential, calcium current and potassium current. Interestingly, ML neuron potassium and calcium current equations show memristive behavior [10]. Thus, ML neurons can be implemented by utilizing the nanoscale memristors which reduces the area overhead for hardware implementation ML-based neural systems significantly.

Memristor is an analog memory device, which can be fabricated in high density nanoscale fabrics. Unique characteristics of this new emerging technology has shown a great potential to be used as biological synaptic connection in bio-mimic hardware [11]. In addition, it can reproduce Spike-Timing-Dependent-Plasticity (STDP). Memristor crossbar architecture opens the opportunity to have ultra size scaling of very large scale neural networks. Recently, several studies have been done on neuromorphic computing with memristor devices but most of them employed spiking-based neuron model like Integrate and Fire (IF) and Leaky Integrate and Fire (LIF) [12]. Memristive neuromorphic computing using biological plausible model of neuron [19] is worth to be implemented as it leads to understanding of real neuronal interactions in brain.

In this chapter, unsupervised STDP-based learning is tested for memristive SNN by utilizing ML neuron. The memristive implementation of the ML neuron is analyzed by showing the potassium and the calcium channels memristive behavior. The coupled ML neurons behavior by using a memristive synapse are assessed for STDP learning rule. For testing the functionality of proposed SNN, two pattern classification applications are implemented by this scheme. The results of the simulations for pattern classifications are presented.

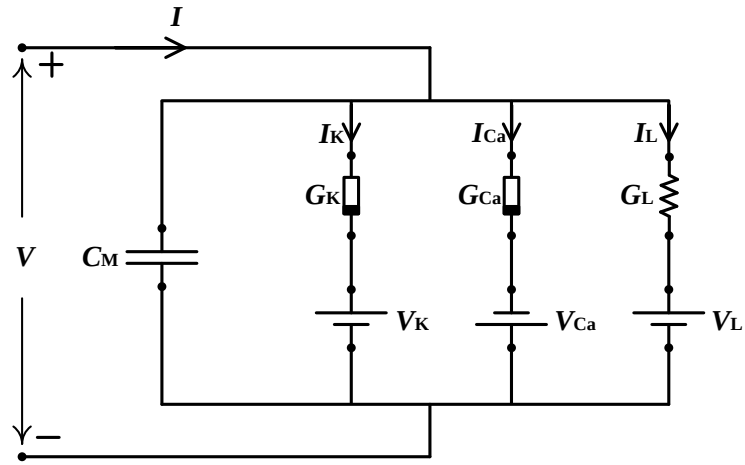

Figure 4.2: Equivalent memristive circuit schematic for ML neuron model.

4.2 Memristor Device and Its Functionality

A nanoscaled passive two-terminal resistive device with non-volatile characteristics was discovered in 2008 by researchers in HP lab [13]. This device had been envisioned earlier in 1971 by Leon Chua [14]. The pinched hysteresis $i - v$ curve of memristor represents its unique memory-dependent feature. These devices have been utilized in various applications such as, nanoelectronic memories [15], logic implementation [16-17] and neuromorphic [18-19]. Memristor comprises of an electrically switchable thin film sandwiched between two metal contacts with a total length of L. The thin film consists of doped and undoped regions. The instantaneous voltage and current of memristor device obey a state-dependent Ohm's law. The voltage-controlled device can be defined by,

$$i = G(v, w, t)v, \tag{4.1}$$

$$\frac{dw}{dt} = f(v, w, t)v. \tag{4.2}$$

The length of doped region, w, is considered as the internal state variable of the device. By applying a voltage higher than positive (V_{tp}) and negative (V_{tn}) threshold of the device, the internal state variable is altered and the device resistance is changed between low resistance

state (R_{LRS}) and high resistance state (R_{HRS}).

4.3 Morris-Lecar Neuron

The ML model [7] was developed to generate the biological behavior of calcium Ca^{++} and potassium K^{++} conductances in giant barnacle muscle fiber. This model has three ionic currents: a membrane leakage current, a potassium current and a calcium current. The electrical equivalent circuit for this model is defined in Fig. 4.1. The simplest form of the ML model is defined by,

$$I = C_{\mathrm{M}} \frac{dV}{dt} + I_{\mathrm{ionic}}. \tag{4.3}$$

$$I_{\mathrm{ionic}} = I_{\mathrm{Ca}} + I_{\mathrm{K}} + I_{\mathrm{L}}, \tag{4.4}$$

where I, V and C_{M} are the total membrane current, voltage and capacitance, respectively. The ionic current, I_{ionic}, consists of calcium (I_{Ca}), potassium (I_{K}) and leakage (I_{L}) currents. These three currents are determined by,

$$I_{\mathrm{Ca}} = g_{\mathrm{Ca}} M\left(V\right)\left(V - V_{\mathrm{Ca}}\right), \tag{4.5}$$

$$I_{\mathrm{K}} = g_{\mathrm{K}} N(V - V_{\mathrm{K}}), \tag{4.6}$$

$$I_{\mathrm{L}} = g_{\mathrm{L}}(V - V_{\mathrm{L}}), \tag{4.7}$$

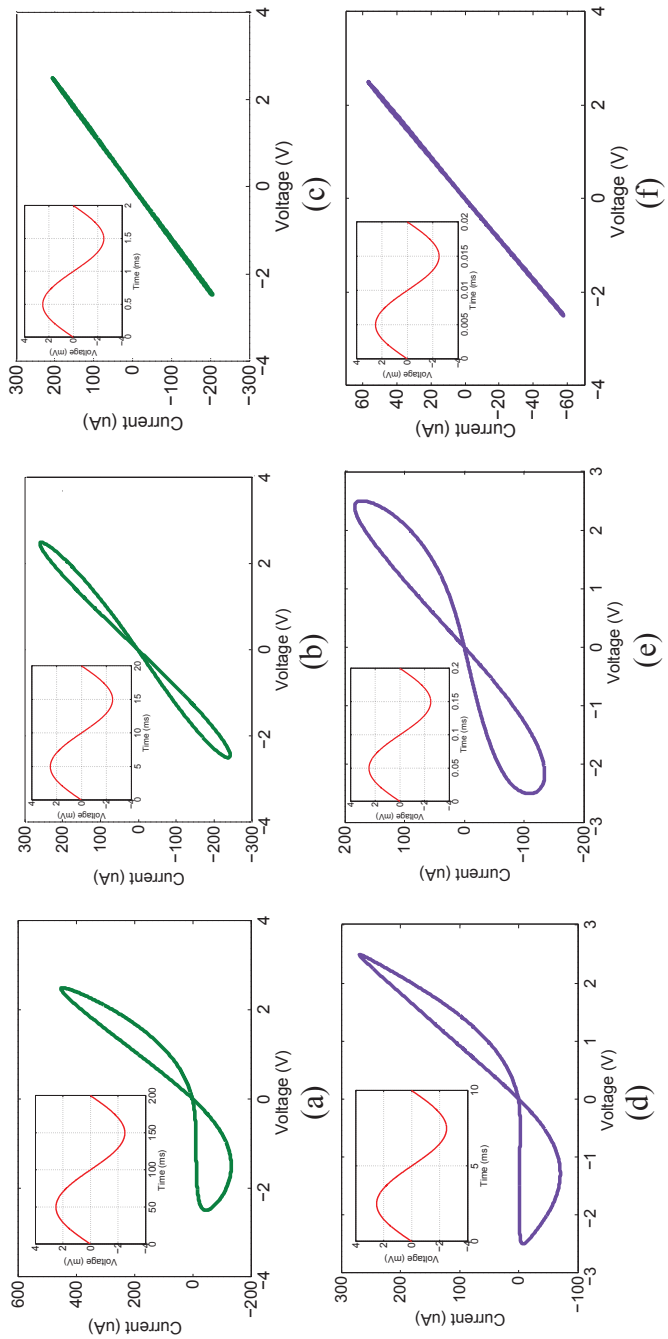

Figure 4.3: Memristive behavior of potassium and calcium channels for ML model is displayed for $2.5V$ sinusoidal voltage input wave in different frequencies. (a) Potassium channel memristor $i - v$ for 5 Hz. (b) Potassium channel memristor $i - v$ for 50 Hz. (c) Potassium channel memristor $i - v$ for 5 KHz. (d) Calcium channel memristor $i - v$ for 100 Hz. (e) Calcium channel memristor $i - v$ for 500 Hz. (f) Calcium channel memristor $i - v$ for 50 KHz.

where g_{Ca}, g_{K} and g_{L} are maximum or instantaneous conductance for calcium, potassium and leakage channels, respectively. The parameters V_{Ca}, V_{K} and V_{L} are equilibrium potentials corresponding to calcium, potassium and leakage channels, respectively. M and N denote the fraction of open calcium and potassium channels, respectively. These parameters can be determined by,

$$\frac{dM}{dt} = \lambda_{\mathrm{M}}(V)\left[M_{\infty}(V) - M\right], \tag{4.8}$$

$$M_{\infty}(V) = 0.5\left\{1 + \tanh\left(\frac{V - V_1}{V_2}\right)\right\}, \tag{4.9}$$

$$\lambda_{\mathrm{M}}(V) = \bar{\lambda}_{\mathrm{M}}(V)\cosh\left[\frac{V - V_1}{2V_2}\right], \tag{4.10}$$

$$\frac{dN}{dt} = \lambda_{\mathrm{N}}(V)\left[N_{\infty}(V) - N\right], \tag{4.11}$$

$$N_{\infty}(V) = 0.5\left\{1 + \tanh\left(\frac{V - V_3}{V_4}\right)\right\}, \tag{4.12}$$

$$\lambda_{\mathrm{N}}(V) = \bar{\lambda}_{\mathrm{N}}(V)\cosh\left[\frac{V - V_3}{2V_4}\right], \tag{4.13}$$

where M_{∞} and N_{∞} denote the fraction of open calcium and potassium channels at steady state, respectively. The parameter V_1 and V_3 are the membrane potential value at $M_{\infty} = 0.5\mathrm{mV}$ and $N_{\infty} = 0.5\mathrm{mV}$, respectively. V_2 and V_4 are reciprocal of slope of voltage dependent M_{∞} and N_{∞}, respectively. The parameters $\lambda_{\mathrm{M}}(\mathrm{V})$ and $\lambda_{\mathrm{N}}(\mathrm{V})$ are rate constants for opening of calcium and potassium channels, respectively. In addition, the maximum rate constants for opening of calcium and potassium channels are $\bar{\lambda}_{\mathrm{M}}(V)$ and $\bar{\lambda}_{\mathrm{N}}(V)$, respectively. By assuming that the response of the calcium ion is considerably faster than the response of the potassium ion and the state equation of calcium is in the steady state, $\frac{dM}{dt} = 0$ $(M = M_{\infty}(V))$, the differential equation in (1) is simplified to second-order form

Table 4.1: Scaled Morris-Lecar neuron parameters.

Parameters	Value	Parameters	Value	Parameters	Value
$g_{\mathrm{Ca}}(\mu\mathrm{Scm}^{-2})$	0.11	V_{CA}(V)	4.8	$C_{\mathrm{M}}(\mu\mathrm{Fcm}^{-2})$	0.5
$g_{\mathrm{K}}(\mu\mathrm{Scm}^{-2})$	0.2	V_{K}(V)	-3.36	$\bar{\lambda}_{\mathrm{N}}(\mathrm{ms}^{-1})$	40
$g_{\mathrm{L}}(\mu\mathrm{Scm}^{-2})$	0.05	V_{L}(V)	-2.4	$\bar{\lambda}_{\mathrm{M}}(\mathrm{ms}^{-1})$	800

as follows,

$$C_{\mathrm{M}}\frac{dV}{dt} = -g_{Ca}M_{\infty}(V)\left[V - V_{Ca}\right] - g_K N(V)\left[V - V_K\right] \\ -g_L\left[V - V_L\right] + I \tag{4.14}$$

By analyzing the general form of the ML model, it can be deduced that the calcium and potassium channels are showing memristive behavior [10]. The time-varying conductance in potassium and calcium channels can be defined by two memristors as it is displayed in Fig. 4.2. The parameters N and M are similar to the state variable of memristor devices. By simulating the current in potassium and calcium channels a pinched hysteresis loop under bipolar periodic signal is extracted. This feature is similar to the unique characteristic of memristor devices. In addition, by increasing the frequency of the applied bipolar periodic signal, the hysteresis loops are shrunk and by reaching to a specific frequency it becomes to a single-value function through the origin. Hence, these properties prove the memristive nature of calcium and potassium channels in ML model. The memristive equivalent model for ML is depicted in Fig. 4.2. For utilizing the ML model in the proposed SNN, the ML model is scaled to around $2\mathrm{V}$. The parameters for scaled ML model are defined in Table 1. The $i-v$ curve of the potassium and calcium channels are displayed in Fig. 4.3 for different frequencies. In addition, the bifurcation and parameters behavior in the proposed scaled ML neuron are illustrated in Fig. 4.4 for three different applied currents to the neuron.

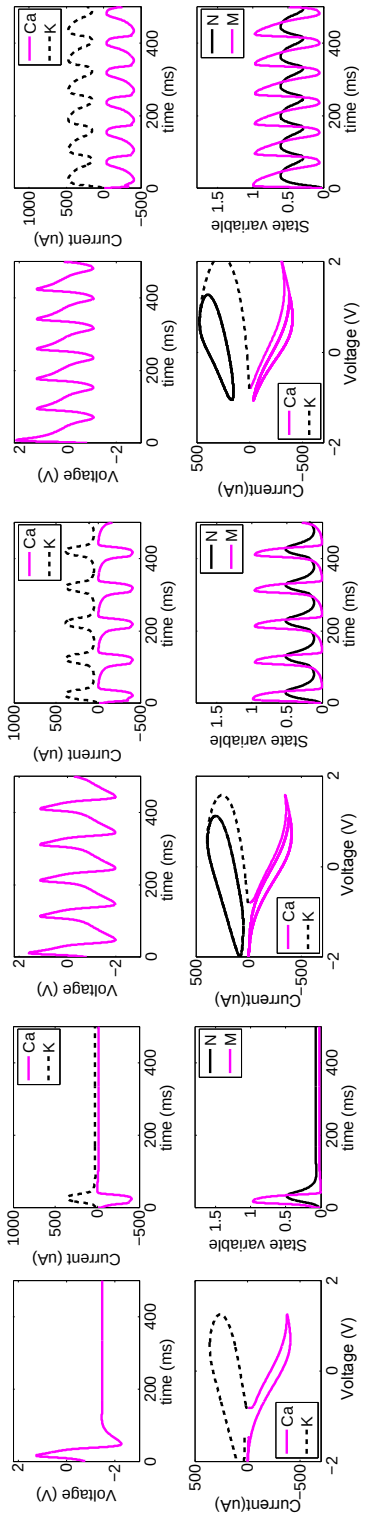

Figure 4.4: The scaled ML neuron bifurcation behavior for different current stimulus. The membrane voltage, calcium channel's current, potassium channel's current and state variables (M, N) are analyzed in each case. (a) The stimulus current of 60 μA. (b) The stimulus current of 100 μA. (c) The stimulus current of 200 μA.

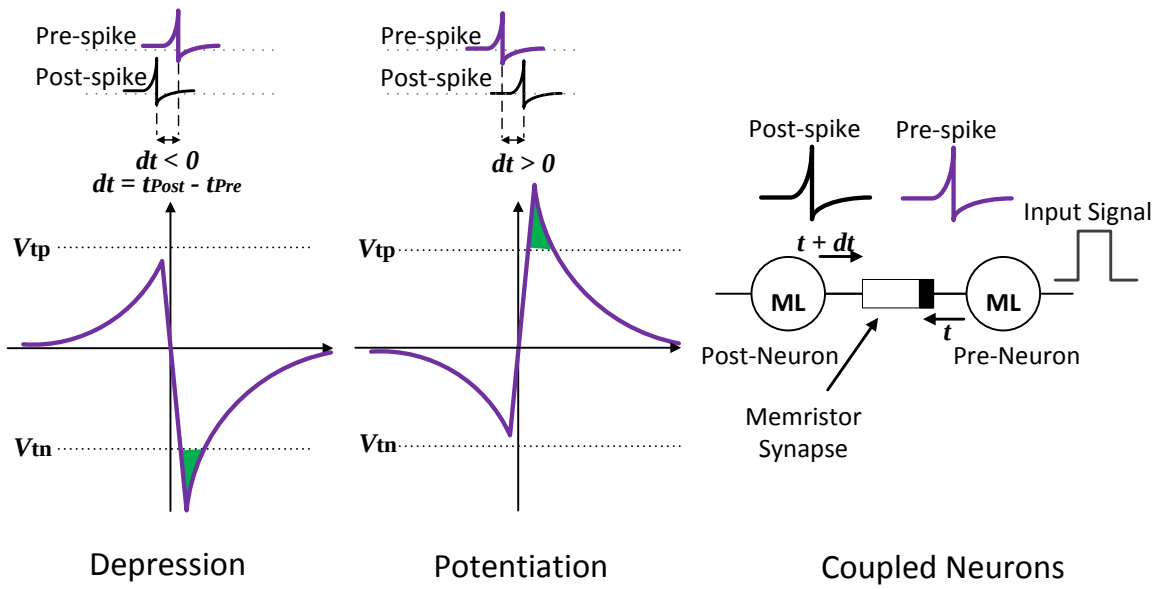

Figure 4.5: STDP learning mechanism is illustrated for two coupled ML neurons with a memristive synapse. LTD and LTP phenomenons are displayed.

4.4 STDP Learning Mechanism with Memristor Synapses

STDP is a timing-based learning mechanism postulated to exist in biological neurons of mammalian neocortex [18]. The functionality of this mechanism is based on the relative timing of spikes arrival from pre-synaptic and post-synaptic neurons. Long term potentiation (LTP) and long term depression (LTD) phenomenons can be generated by STDP mechanism and they cause alteration in synaptic efficacy (weight). LTP happens when pre-synaptic neuron spike proceeds the post-synaptic neuron ($t_{\text{post}} - t_{\text{pre}} \geq 0$) and it increases the synaptic weight (W). LTD takes place when post-synaptic synaptic neuron spikes before pre-synaptic neuron ($t_{\text{post}} - t_{\text{pre}} < 0$) and this results in reduction of synaptic weight. The degree of change in synaptic weight is a function of the time interval between post- and pre-synaptic spikes. The larger changes are induced by shorter time interval. Interestingly, the memristor device behavior mimics biological synapse in the brain as its conductance can be modulated by applying a stimuli with an ability to store the information [11]. These devices are capable of reproducing STDP mechanism similar to biology. In

LTP phenomenon, the voltage over the memristor synapse becomes greater than positive threshold of the device ($V_{\mathrm{post}} - V_{\mathrm{pre}} \geq V_{\mathrm{tp}}$) and the conductance (weight) of the memristor increases. On the other hand, in LTD phenomenon the voltage over the memristor synapse becomes less than negative threshold of the device ($V_{\mathrm{post}} - V_{\mathrm{pre}} < V_{\mathrm{tn}}$) and it results a reduction in conductance (weight) of the memristor. The STDP learning mechanism is displayed for proposed SNN with memristive synapse in Fig. 4.5.

4.5 The Memristive SNN with ML Neuron

The architecture of the proposed SNN comprises of ML neurons and voltage-controlled memristor synapses. The scaled ML model, with parameters presented in Table 1, generates biological plausible shape of spike. The memristor model [20] is applied for memristor synapse and its parameters are defined in Table 2. The proposed SNN has a pre-synaptic neurons layer that is connected with memristive synapses to post-synaptic neurons layer. To analyze the behavior of the SNN, at first two coupled ML neurons with one memristive synapse is assessed. The pre-synaptic neuron's membrane voltage can be determined by,

$$\begin{aligned} C_{\mathrm{M}} \frac{dV_{\mathrm{pre}}}{dt} &= -g_{\mathrm{Ca}} M_{\infty}(V_{\mathrm{pre}}) \left[V_{\mathrm{pre}} - V_{Ca}\right] \\ &\quad -g_K N(V_{\mathrm{pre}}) \left[V_{\mathrm{pre}} - V_K\right] - g_L \left[V_{\mathrm{pre}} - V_L\right] + I. \end{aligned} \tag{4.15}$$

The parameter V_{pre} is pre-synaptic neuron's membrane voltage. The parameter I is the applied input current to pre-synaptic neuron. The applied current to pre-synaptic neurons for proposed SNN is considered $100\ \mu\mathrm{A}$ which produces hopf bifurcation in ML neuron model. The membrane voltage of the post-synaptic neuron can be determined by,

$$\begin{aligned} C_{\mathrm{M}} \frac{dV_{\mathrm{post}}}{dt} &= -g_{\mathrm{Ca}} M_{\infty}(V_{\mathrm{post}}) \left[V_{\mathrm{post}} - V_{Ca}\right] \\ &\quad -g_K N(V_{\mathrm{post}}) \left[V_{\mathrm{post}} - V_K\right] - g_L \left[V_{\mathrm{post}} - V_L\right] + I_{\mathrm{syn}}. \end{aligned} \tag{4.16}$$

Table 4.2: Memristor device parameters for simulation.

Parameters	R_{LRS}	R_{HRS}	L	μ_v	V_{tp}	V_{tn}
Units	Ω	KΩ	nm	m^2/Vs	V	V
Values	100	10	3	1×10^{-15}	1.5	-1.2

The parameter V_{post} is membrane voltage of the post-synaptic neuron. The I_{syn} is the total

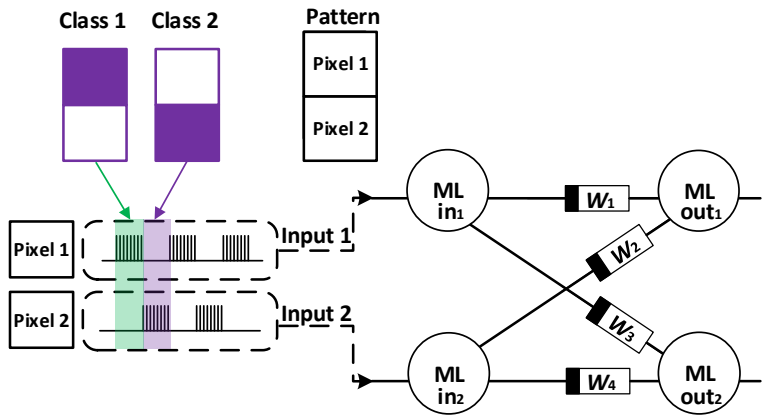

Figure 4.6: 2×2 network architecture of the proposed SNN. The input patterns for the proposed network are defined.

current enters the post-synaptic neuron by memristive synapses and in this case it is equal to the current passes memristor synapse. In larger SNN, as post-synaptic neuron is connected to k pre-synaptic neurons with memristive synapses that have currents (I_{syn1},I_{syn2},...,$I_{\mathrm{syn}k}$), the pre-synaptic neuron current is equivalent to,

$$I_{\mathrm{syn}} = \sum_{j=1}^{k} I_{\mathrm{syn}j}. \tag{4.17}$$

The synaptic current in each synapse varying due to the conductance change happens in each synapse during neuronal activities. As the voltage over each synapse exceeds the positive and negative threshold of the device, the LTP and LTD phenomenons occur and the conductance of the synapses alter. The current of each synapse $I_{\mathrm{syn}j}$ can be determined

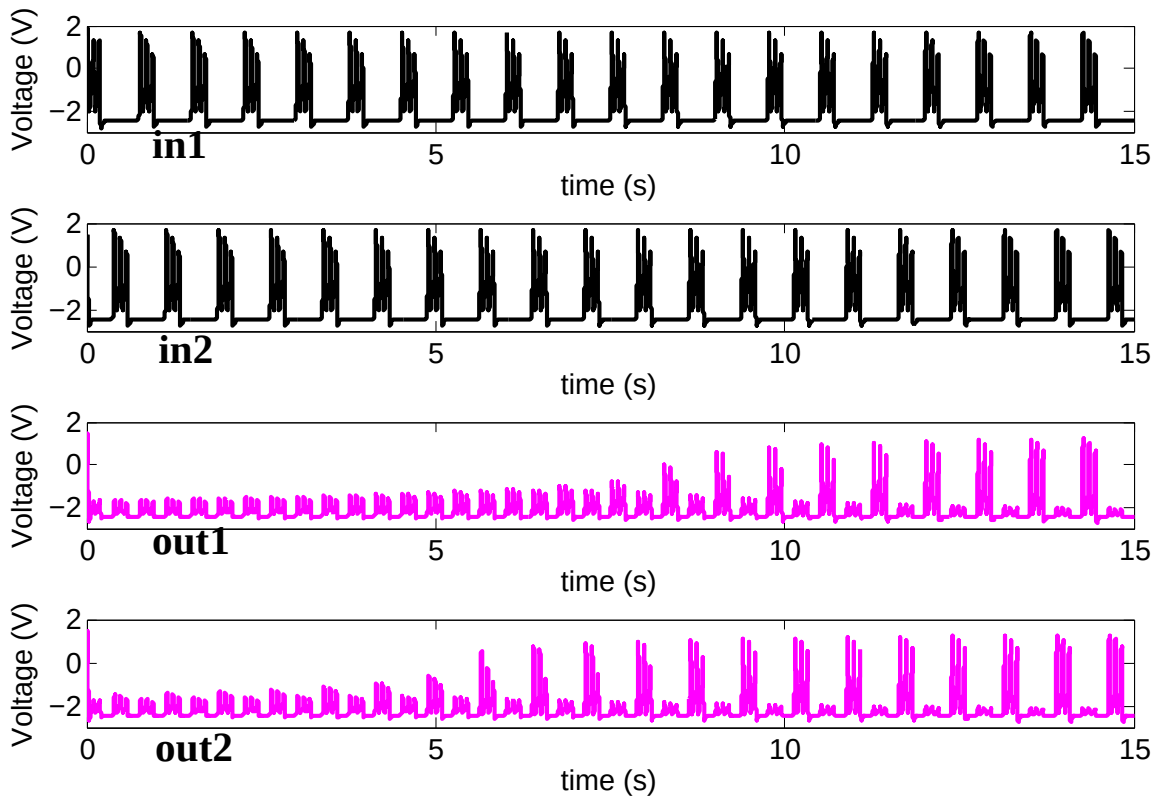

Figure 4.7: The membrane voltage of the pre-synaptic (black curve) and post synaptic (purple curve) neurons for 2×2 network. The proposed network classifies the patterns successfully.

as,

$$I_{\text{syn}j}(t) = \frac{V_{\text{post}}(t) - V_{\text{pre}j}(t)}{R_{\text{syn}j}(wj)}, \tag{4.18}$$

$$R_{\text{syn}j}(w_j) = R_{\text{LRS}}\frac{w_j(t)}{L} + R_{\text{HRS}}(1 - \frac{w_j(t)}{L}), \tag{4.19}$$

$$\frac{dw_j}{dt} = \frac{\mu_v R_{\text{LRS}}}{L^2} \times I_{\text{syn}j}(t) \times f(w_j), \tag{4.20}$$

$$f(w_j) = \left(1 - 2\left(\frac{w_j(t)}{L}\right)\right)^{2p}. \tag{4.21}$$

The parameter $f(w_j)$ is the window function [20] for each synapse and p is a constant. The p value is considered 2 in simulations. The pattern classification application has been tested for the proposed SNN.

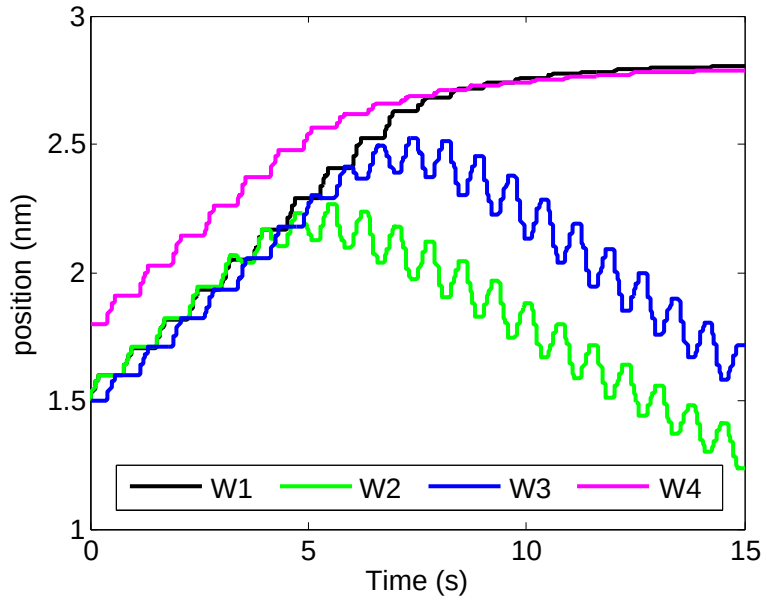

Figure 4.8: The weight evolution of the memristive synapse for 2×2 network.

4.6 Pattern Classification Results

The proposed SNN is utilized to perform unsupervised classification by STDP learning scheme. By applying different patterns to input neurons, the output neurons generate patterns based on the weight update of connected synapses to them. One of the output neurons becomes a winner and reproduce one of the patterns in input due to the combination of connected synaptic weights. This happens when the weight vector of the winner output neuron is closer to one of the input pattern vector. For testing the functionality of the proposed ML-based SNN two simple pattern classification tasks have been done. The first one is the 2×2 network that comprises of two input ML neurons $(\mathrm{in}_1, \mathrm{in}_2)$ and two output ML neurons $(\mathrm{out}_1, \mathrm{out}_2)$. These two layers are connected to each other by memristor synapses with random initial weights $(\mathrm{W}_1, \mathrm{W}_2, \mathrm{W}_3, \mathrm{W}_4)$. Each input neuron is connected to all output neuron with one memristive synapse. This network is applied to classify between two pixel images with class 1 and 2. As it can be seen from the Fig. 4.6, two different input waves are applied to the input neurons. The input wave can be divided into several time

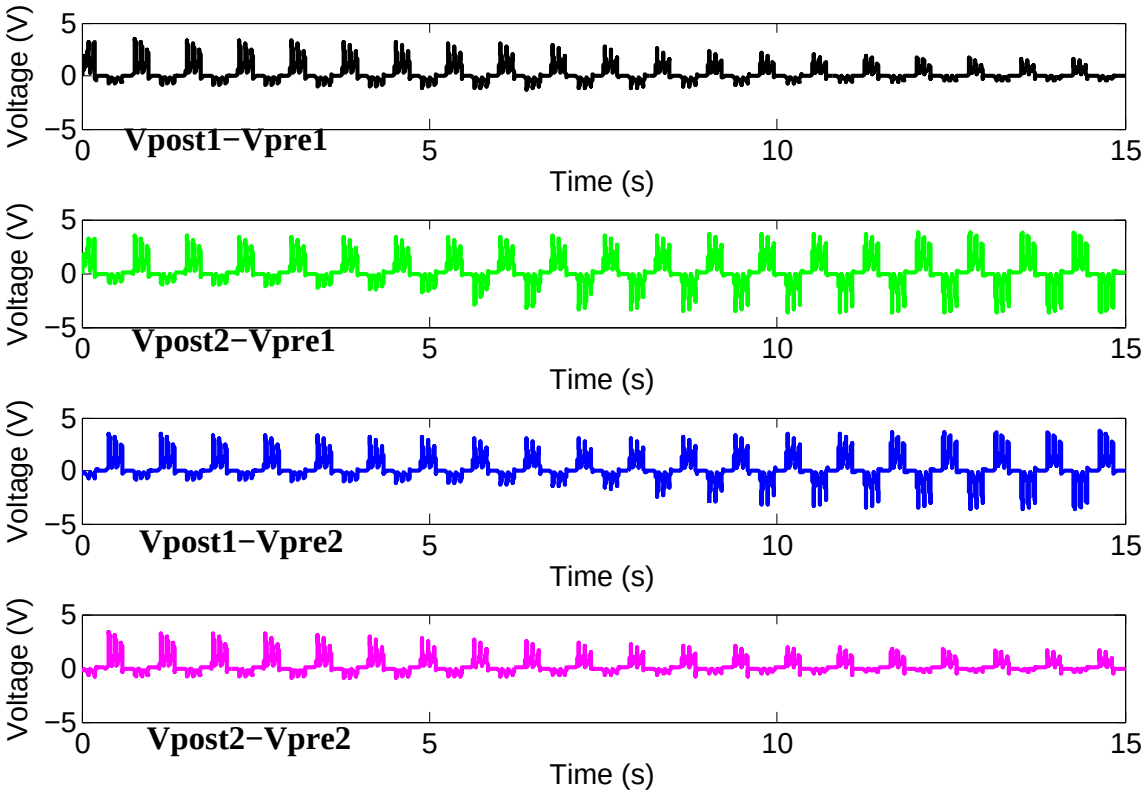

Figure 4.9: The voltage over each memristive synapse that produce LTP or LTD phenomenons for 2×2 network.

frames and in each time frame one of the classes are applied. The input 1 and 2 are corresponding to the pixel 1 and 2 of the pattern, respectively. In the first time slot which is corresponding to class 1, the input 1 is spiking because pixel 1 is black and there is no spike for input 2 since the pixel 2 is white in this class. Subsequently, in the next time slot, class 2 of the two pixel image is applied as the input 1 is not spiking and input 2 is spiking.

The output for the proposed network with applied input waves are displayed in Fig. 4.7. It takes some times for post-synaptic ML neurons to follow one of the input patterns. The initial weight vector of each output neuron specifies the consumed time to follow the pattern and the pattern class to display due to its closeness to input patterns vector. Assuming the class 1 is assigned to the post-synaptic neuron 1, the weight of W_1 increases by LTP phenomenon as pre-synaptic neuron in_1 spikes before the post-synaptic neuron out_1. On

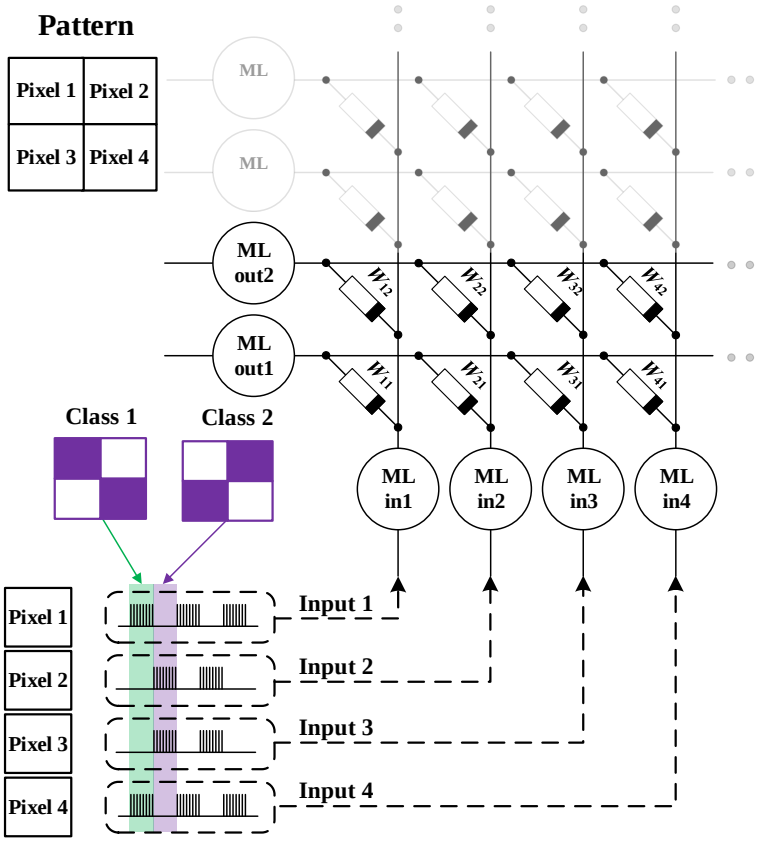

Figure 4.10: 4×2 network architecture in memristive crossbar array for the proposed SNN. The input patterns for the proposed network are defined.

the other hand, the weight of W_2 decreases due to the inactivity of out_2. The similar procedure is repeated for class 2 image. The memristive synapse weights and their behavior during STDP learning is displayed in Fig. 4.8. As it can be seen, W_1 and W_4 weights are increased and W_2 and W_3 are decreased. Also the voltage over each memristive synapse during STDP learning procedure and weight evolution is displayed in Fig. 4.9. The larger network, 4×2, is also tested with the proposed SNN. This network is displayed on memristive crossbar array in Fig. 4.10. The proposed network classifies 2 classes of the four pixel image. Two input patterns based on the classes are assigned to four input waves and applied to pre-synaptic neurons. These inputs are displayed in Fig. 4.11. The network is successfully performed the classification task and the output results are illustrated in Fig. 4.12

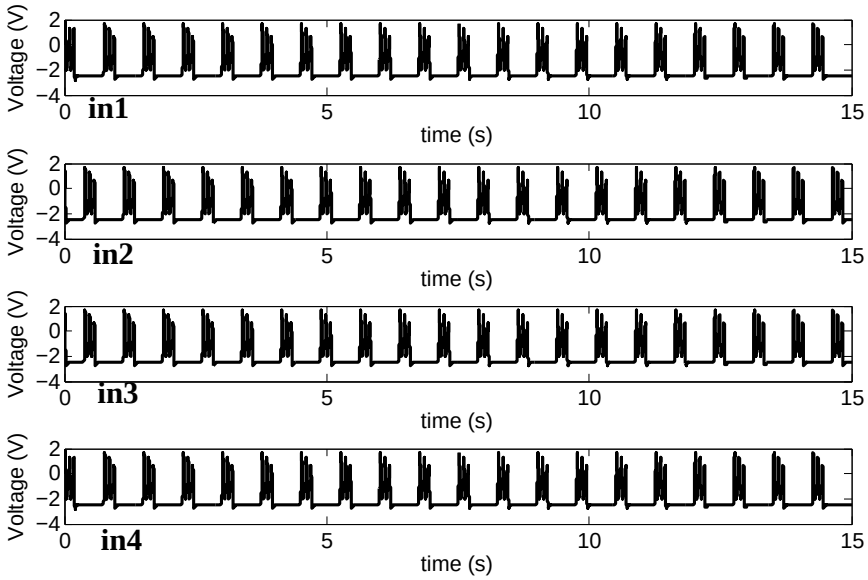

Figure 4.11: The membrane voltages of the pre-synaptic neurons for 4×2 network.

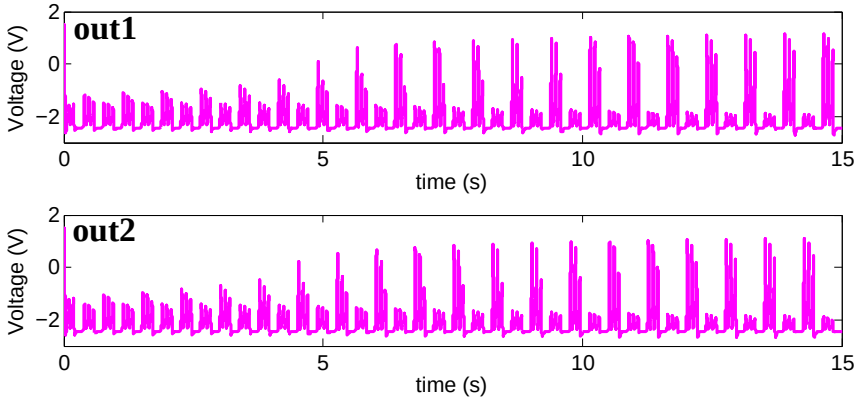

Figure 4.12: The membrane voltage of the post-synaptic neurons for 4×2 network.

for both post-synaptic neurons. The weight evolution and behavior for each synapses are depicted in Fig. 4.13.

4.7 Conclusion

This Chapter presented a memristive biological plausible spiking neural network with Morris-Lecar neuron model for pattern classification. The memristive implementation of

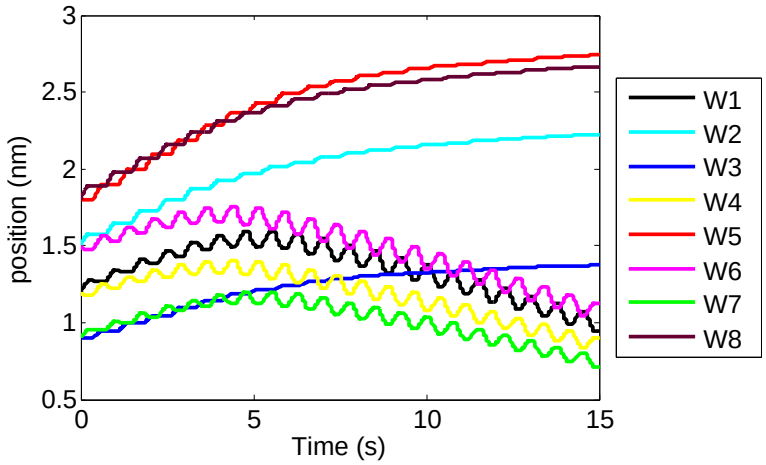

Figure 4.13: The weights evolution of the memristive synapses for 4×2 network.

ML neuron was explained and the potassium and calcium memristive channels behavior was investigated. The scaled model of the ML neuron was applied in a memristive SNN architecture and the STDP learning scheme was applied for pattern classification. Finally, two pattern classification examples was tested successfully with the proposed network as a proof of concept.

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Chapter 5

A Novel CVNS Adder with Memristive Analog Memory

CONTINUOUS Valued Number System (CVNS) is a new approach in computer arithmetic to develop high performance and efficient arithmetic units. In this chapter, CVNS-based computation scheme is applied to design a memristive analog adder and it has been demonstrated that this technique is a viable alternative approach to implement multi-digit arithmetic system with multilevel memory devices. The proposed CVNS adder has addition and modulo configurations to perform CVNS addition. A mapping circuit has been designed for modulo operation. The proposed memristive CVNS-based adder has been tested and analyzed for different CVNS values with radix-10 and 2-digit analog environment resolution. The simulations are shown acceptable accuracy and the presented system performance that promises an analog memristive computation method for future in-memory computation systems.

Table 5.1: radix-10 CVNS digits of an arbitrary value $x = 73.421$.

i	1	0	-1	-2	-3
$((x))_i$	7.3421	3.421	4.21	2.1	1
$\lfloor((x))_i\rfloor$	7	3	4	2	1

5.1 Introduction

Memristive logic circuit design [1]-[5] has been intensified in research, due to the nanoscaled features of memristor and its capability of performing logic and memory operations simultaneously. Von-Neumann based architectures requires a constant communication between the memory and computation unit. Thus, implementation of memristor-based computing system is attractive for future in-memory computing architectures which is beyond classical Von-Neumann theory.

The Continuous Valued Number System (CVNS) [6] is a continuous number system with non-integer digits. This novel number system has the potential in development of new types of arithmetic blocks. Due to its digit-wise nature to perform arithmetic operations, CVNS-based design reduces the wiring complexity and area consumption of the arithmetic circuits. Several arithmetic units such as adders and multipliers have been designed by CVNS scheme [7][8].

In this chapter, a memristive CVNS-based adder is implemented which is employed CVNS scheme to perform a digit-wise summation operation. A new scheme is presented to display a CVNS value by memristor devices. The proposed adder is required addition and modulo configurations for CVNS addition operation and it needs fewer number of interconnections to perform the operation as CVNS offers a summation operation with no carry. The functionality of proposed adder is evaluated and its relative error is extracted.

Table 5.2: radix-10 CVNS digits for addition two arbitrary value $x = 58.34$ and $y = 72.89$.

i	2	1	0	-1	-2
$((x))_i$	0.5834	5.834	8.34	3.4	4
$((y))_i$	0.7289	7.289	2.89	8.9	9
$((x))_i + ((y))_i$	1.3123	3.123	1.23	2.3	3

5.2 Continuous Valued Number System (CVNS)

The CVNS digits, $((x))_i$, in radix-β are designated as CVNS representation of any real value, x, within a boundary $|x| \leq M$ in a positional number system with radix-B [6]. The CVNS value $((x))$ can be written as a vector,

$$((x)) \Rightarrow \{((x))_L, ..., ((x))_0 \,|\, ((x))_{-1}, ..., ((x))_{-k}\} \tag{5.1}$$

where the bar $(|)$ shows the radix point and $(-k \leq i \leq L)$ represents the indices of CVNS digits. In the CVNS paradigm, the digits with higher indices contains higher information density in comparison with lower indices and the CVNS digit with the highest index has the whole information with a degree of uncertainty regarding the original value. The CVNS digits can be determined by applying a basic modular reduction operation as follows,

$$((x))_i = \left(\frac{x}{M}.\beta^{L-i+1}\right) mod\beta \tag{5.2}$$

where mod is the modulo operation on any real value such that $(a)\, mod\beta = a - N \times \beta$ by assuming $0 \leq (a)\, mod\beta \leq \beta$ and N is an integer. Each CVNS digit comprises of an integer part and non-integer part. The non-integer part overlaps with the lower index digits. The relationship between two adjacent CVNS digit is determined by,

$$((x))_i = \lfloor ((x))_i \rfloor + \frac{((x))_{i-1}}{\beta} \tag{5.3}$$

where $\lfloor . \rfloor$ denotes floor function. For better insight a radix-10 CVNS digits of an arbitrary

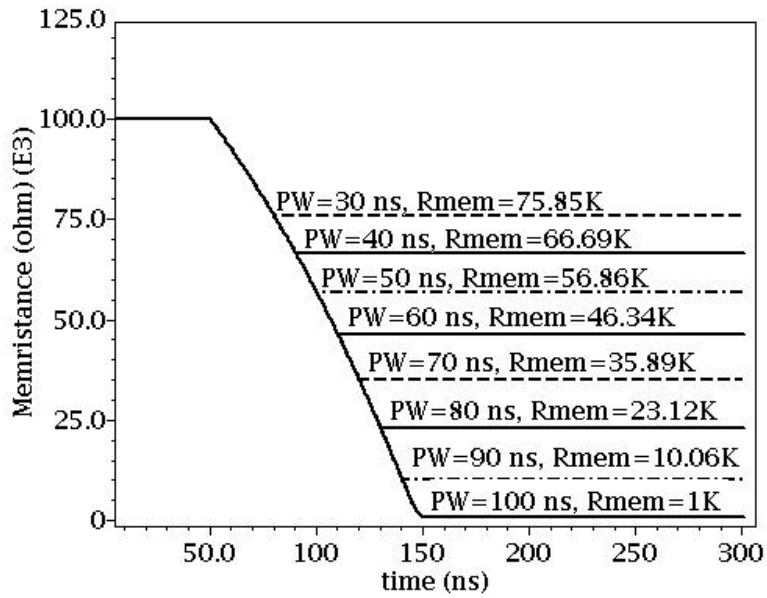


Figure 5.1: Programming memristor device by applying a 0.8 V square pulse with different pulse widths.

Table 5.3: Memristor device parameters for simulation.

Parameters	R_{LRS}	R_{HRS}	L	μ_v	V_{tp}	V_{tn}
Units	kΩ	kΩ	nm	m^2/Vs	V	V
Values	1	100	3	8×10^{-7}	0.4	-0.4

value $x = 73.421$ is defined in Table 1.

The addition is performed independently on each of the CVNS digits. Hence, it means there is no need for carry during addition operation in CVNS scheme. The CVNS digits of $((z)) = ((x))\,((+))\,((y))$, by considering $x, y \leq M$, can be determined by digit-wise addition,

$$((z)) = (((x))_i + ((y))_i)\, mod\beta. \tag{5.4}$$

The modular reduction operation after the addition prevents the overflow since it limits the digit within the radix value. Therefore the summation is done for each digit columns

without intercommunication. The radix-10 CVNS addition of two arbitrary values is shown in Table 2. The number of required CVNS digits is $L = 1$ and $k = 2$.

5.3 Memristor Device and Its Programming

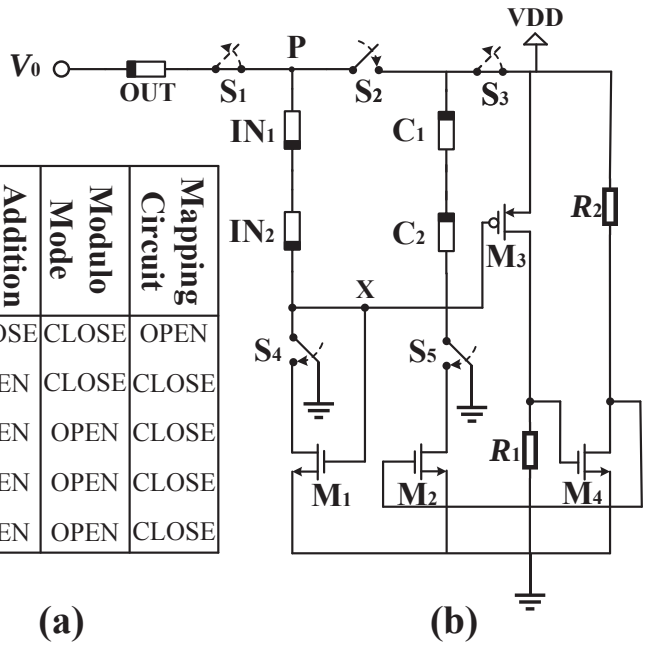
Memristor device is a promising candidate for analog computation and analog memory [5]. In these devices, by applying a voltage higher than a specific threshold the doping profile of transition oxide filament can be altered between two main states: High Resistance State (HRS) and Low Resistance State (LRS). The V_{tp} and V_{tn} are positive and negative threshold voltages in memristor devices. On the other hand, by applying a voltage less than $|V_{\mathrm{tp}}|$ and $|V_{\mathrm{tn}}|$ the change in device state is negligible. The voltage-controlled memristor device can be defined by [9],

$$i = G(v, w, t)v \tag{5.5}$$

$$\frac{dw}{dt} = f(v, w, t)v \tag{5.6}$$

where w is state variable that represents structural property of the device. The linear ion drift model [9] is described memristor behavior based on the movement of boundary region along the device. In this model a device with length of L, has doped region with length of w and un-doped region with length of $L - w$. The boundary region moves along the length of the transition oxide filament as the sufficient amount of charge has flown through the device. The memristor is considered as two variable resistors in series. The memristance of the device is defined by,

$$R_{mem}(w) = R_{\mathrm{LRS}}\frac{w}{L} + R_{\mathrm{HRS}}(1 - \frac{w}{L}). \tag{5.7}$$



	Addition Mode	Modulo Mode	Mapping Circuit
S_1	CLOSE	CLOSE	OPEN
S_2	OPEN	CLOSE	CLOSE
S_3	OPEN	OPEN	CLOSE
S_4	OPEN	OPEN	CLOSE
S_5	OPEN	OPEN	CLOSE

Figure 5.2: The schematic of CVNS adder circuit and configuration table for the switches. (a) Configuration table. (b) MCVNS adder.

The parameters R_{LRS} and R_{HRS} are the resistances of the device when doped and un-doped region covers the whole length of the memristor respectively. The parameters of memristor device, which is applied for simulation, are defined in Table 3. The memristor can be programmed by applying a square voltage over it. The amount of programming over the device is controlled by the duration of the pulse. As it can be seen in Fig. 5.1, the memristor device is programmed to the desired memristances by applying 0.8 V square pulse with different pulse widths. The write time for changing the device state from R_{HRS} to R_{LRS} is 100 ns. As an example, for writing 75.58 KΩ the square pulse with 0.8 V amplitude and 30 ns pulse width has been applied over the device.

5.4 Memristive Continuous Valued Number System (MCVNS) Adder

The memristive circuit performing CVNS-based addition is designed based on the addition and modulo operation in CVNS scheme. The proposed circuit stores values as the memristance of the memristor devices and the numbers are inserted to the circuit by adjusting input memristors to the corresponding state variables. The radix of the CVNS scheme is considered as R_{HRS} when the state variable $w = 0\mathrm{nm}$. The proposed circuit is displayed in Fig. 5.2. As it can be seen from the circuit schematic, the memristor IN_1 and IN_2 are the input devices. The memristor OUT is the output memristor that stores the CVNS addition results by the end of the operation.

This circuit is configured by monitoring of the node P to work in the addition or modulo modes. The switches $S_{1,2,\ldots,5}$ are applied to change the configuration of the circuit. Also, for modulo operation mode a mapping circuit has been designed to adjust C_1 and C_2 memristors to the desired values.

5.4.1 Memristive Addition Configuration

This mode is taken place when the addition result, $((z))_i$ of the inputs, $((x))_i$ and $((y))_i$, becomes less than the radix value (β). For this mode, the switches S_1 and S_2 are in CLOSE and OPEN state, respectively. This circuit mode comprises of three series connected memristors as it is illustrated in Fig. 5.3(a). Let $|V_{\mathrm{t}}| = |V_{\mathrm{tn}}| = |V_{\mathrm{tp}}|$ be the threshold voltage of memristor devices. In initialization step, the memristances of input devices, IN_1 and IN_2 should be set to the corresponding input values and the output device should be initialized to high resistance state (R_{HRS}). This circuit adds to CVNS digits with corresponding memristances R_{IN_1} and R_{IN_2} while $R_{\mathrm{IN}_1} + R_{\mathrm{IN}_2} \leq R_{\mathrm{HRS}}$ and stores the result, R_{OUT}, in the output device. By setting V_0 voltage to $2V_{\mathrm{t}}$ the functionality of the circuit is ensured for the

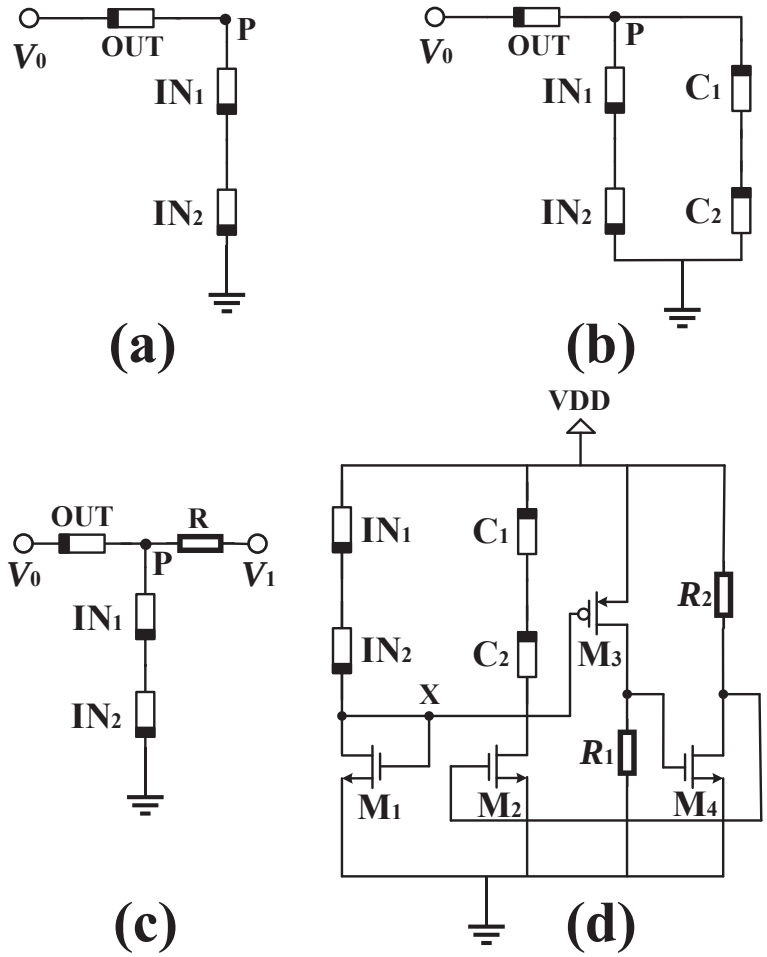


Figure 5.3: Different MCVNS adder configurations equivalent circuits. (a) Addition configuration. (b) Modulo configuration. (c) Modulo circuit for analysis. (d) Mapping circuit.

desired addition operation. The voltage over the output device is determined by,

$$V_{\mathrm{OUT}} = V_0 \left(\frac{R_{\mathrm{OUT}}}{R_{\mathrm{OUT}} + R_{\mathrm{Tot}}} \right), \tag{5.8}$$

$$R_{\mathrm{Tot}} = R_{\mathrm{IN}_1} + R_{\mathrm{IN}_2}. \tag{5.9}$$

The output device, OUT, voltage is depicted in Fig. 5.4 for $2R_{\mathrm{LRS}} < R_{\mathrm{Tot}} < 2R_{\mathrm{HRS}}$ domain. The maximum V_{OUT} voltage is around $2V_{\mathrm{t}}$ when two input devices are in low resistance state. The output device state has been changed until the voltage over it reaches

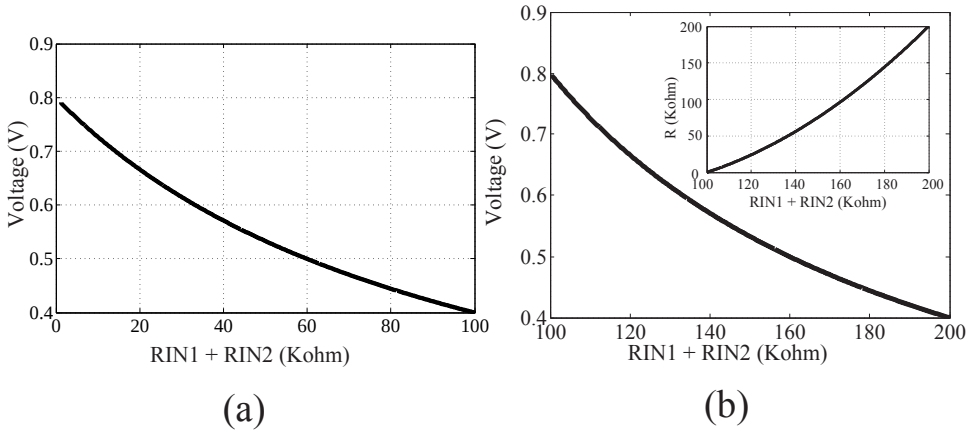


Figure 5.4: The voltage over the OUT device. (a) The voltage of the output device in $[2R_{\mathrm{LRS}}, R_{\mathrm{HRS}}]$ interval for addition configuration. (b) The voltage of the output device in $(R_{\mathrm{HRS}}, 2R_{\mathrm{HRS}}]$ interval for modulo configuration. Also, the resistance value for mapping is displayed.

to the threshold voltage of memristor (V_{t}) which is $V_0/2$. This means at the end of the operation R_{Tot} becomes equal with R_{OUT}. For the values greater than R_{HRS} the output memristor's state remains unchanged since the V_{OUT} is less than the threshold voltage.

5.4.2 Memristive Modulo Configuration

This configuration is applied when R_{Tot} is greater than R_{HRS}. The modulo configuration is displayed in Fig. 5.3(b). In this mode, the switches S_1 and S_2 are both closed and S_3 is OPEN. For designing a modulo operation a circuit schematic in Fig. 5.3(c) is analyzed. The only difference with addition circuit is the parallel branch with resistor R and the bias voltage V_1. In the modulo operation, the value of R_{OUT} should change from R_{HRS}, initial memristance, to $R_{\mathrm{Tot}} - R_{\mathrm{HRS}}$. By assuming $V_1 = 0\mathrm{V}$, the equivalent resistance which is in series with R_{OUT} is,

$$R_{\mathrm{Tot}}||R = \frac{R_{\mathrm{Tot}}R}{R_{\mathrm{Tot}} + R} = R_{\mathrm{Tot}} - R_{\mathrm{HRS}} \tag{5.10}$$

Table 5.4: Corresponding memristance for radix-10 CVNS digits with $\psi = 2$ resolution.

CMOS Devices	Width	Length	Resistors	Resistance
M_1	120 nm	60 nm	R_1	26 kΩ
M_2	500 nm	60 nm	R_2	6 kΩ
M_3	400 nm	60 nm		
M_4	500 nm	60 nm		

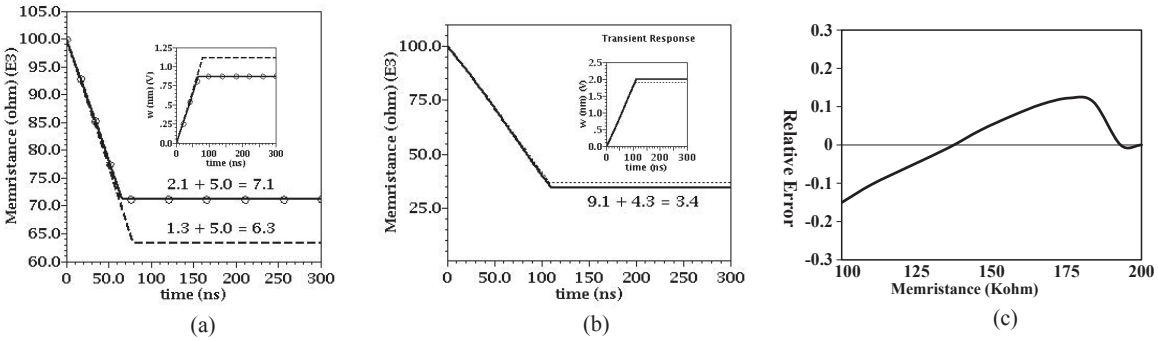
By simplifying this, the parallel branch resistor can be determined by,

$$R = R_{\mathrm{Tot}} \left(\frac{R_{\mathrm{Tot}}}{R_{\mathrm{HRS}}} - 1 \right) \tag{5.11}$$

To ensure the right functionality of the circuit, the grounded parallel resistance, R, maximum value should be R_{HRS} while $R_{\mathrm{Tot}} = 2R_{\mathrm{HRS}}$ and the minimum value occurs when $R_{\mathrm{Tot}} = R_{\mathrm{HRS}}$. Hence, in modulo configuration by considering $R_{\mathrm{Tot}} > R_{\mathrm{HRS}}$, the R_{Tot} interval of $(R_{\mathrm{HRS}}, 2R_{\mathrm{HRS}}]$ should be mapped to corresponding values in $(2R_{\mathrm{LRS}}, 2R_{\mathrm{HRS}}]$ interval on C_1 and C_2 devices. A mapping circuit is designed to map based on this scheme. The schematic of proposed circuit is depicted in Fig. 5.3(d). For activating the mapping circuit switches S_2, S_3, S_4 and S_5 should be in CLOSE state and the switch S_1 should be OPEN. The proposed mapping circuit architecture comprises of four CMOS devices, M_1, M_2, M_3 and M_4, and two resistors, R_1, R_2. The transistors aspect ratio and resistors resistance data are displayed in Table. 4.

5.5 Functionality Test and Simulation Results

The proposed CVNS-based adder is designed with $65\ \mathrm{nm}$ CMOS technology and all simulations are performed in Cadence Virtuoso. One of the important design issues for CVNS is the analog environment resolution (ψ). The CVNS digits are considered in radix-10 with the resolution of $\psi = 2$ to obtain a reliable value for CVNS addition result. Hence,



(a) (b) (c)

Figure 5.5: The simulation results for functionality of MCVNS adder and its relative error. (a) Two addition operations with the MCVNS adder for radix-10 digits. The circuit configured to addition configuration and behavior of state variable w is depicted for these additions. (b) Addition in modulo mode. The dotted and solid lines show the cases with programmed resistance with mapping circuit and theoretically extracted ideal resistance. (c) Relative error for modulo configuration.

Table 5.5: Corresponding memristance for radix-10 CVNS digits with $\psi = 2$ resolution.

Radix-10 CVNS digit	**Memristance**
0.1	R_{LRS}
0.2	$2R_{\mathrm{LRS}}$
. .	. .
9.9	$99R_{\mathrm{LRS}}$
A	$100R_{\mathrm{LRS}}$

the proposed CVNS adder analog environment can distinguish $10^{\psi}(= 100)$ different levels. This parameter is technology dependent and in memristive systems, it depends on the $R_{\mathrm{HRS}}/R_{\mathrm{LRS}}$ ratio. High ratio devices can produce high resolution environment. Table 5 displays the corresponding radix-10 CVNS values for different levels of memristance. The lowest value is R_{LRS} which corresponds to CVNS value 0.1. The highest value is considered as $100R_{\mathrm{LRS}}$ or R_{HRS} that corresponds to A. In fact, the A value is considered as 0 since it is the starting point of CVNS values when addition result exceeds R_{HRS}. This scheme is perfectly functional for applying CVNS on memristive analog memory due to the modulus nature of CVNS computation method and memristor device characteristics.

Radix-10 CVNS addition operation of the proposed MCVNS adder circuit is tested for different values and it is displayed in Fig. 5.5. As it can be seen in Fig. 5.5(a), for adding 2.1 with 5, in initialization step the input devices were programmed to corresponding memristance values for CVNS values 2.1 and 5 which are 21 kΩ and 50 kΩ, respectively. Then, addition configuration becomes activated since the total input memristance is less than the radix value R_{HRS}. The output device memristance is changed to 71 kΩ which is the correct addition result (7.1). In Fig. 5.5(b), CVNS addition of 9.1 and 4.3 is displayed. Initially, the input devices memristances were programmed to 91 kΩ and 43 kΩ for representing 9.1 and 4.3, respectively. The modulo configuration is configured for this case since the total input memristance exceeds R_{HRS}. At first, the mapping circuit writes 25.4 kΩ to C_1 and C_2 devices. Then, modulo circuit completes the addition operation and changes the output memristance to 35 kΩ. There is an error duo to the mapping circuit inaccuracy in writing the exact desired memristance value (25.4 kΩ). By writing the ideal memristance extracted from the theoretical analysis on C_1 and C_2 devices, the output memristance changes to 34 kΩ which is the corresponding memristance of correct value (3.4). This circuit has negligible error when it operates in addition configuration mode. The error analysis of the proposed CVNS adder for modulo configuration mode is displayed in Fig. 5.5(c).

5.6 Conclusion

In summary in this chapter, we have demonstrated a memristive analog adder that is able to perform addition operation by utilizing multiple levels of resistive memory devices. A CVNS computation scheme has been used for this memristive analog adder. The proposed CVNS-based adder circuit has two main configurations to perform CVNS addition and a mapping circuit was presented for its modulo configuration. The functionality of the designed system was tested by applying different CVNS values and their relative error has been extracted.

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Chapter 6

Improvement on IMPLY Logic design: Memristor-Based 4:2 Compressor Cells

MEMRISTOR-BASED arithmetic circuits promise new alternatives for their conventional CMOS-based peers due to memristors scalability and non-volatility features. In-memory memristor-based calculations become extensively attractive as it can be a solution to tackle memory bottleneck problems and also an ingredient for future beyond Von-Neumann computer architectures. In this chapter, material implication-based designs for 4:2 compressor cells using memristor devices are presented. A physical model is applied to determine real switching speed of memristive device. The proposed parallel design promises good speed performance with considerably less area than conventional CMOS designs. Finally, a comparison has been made between the proposed memristor-based and CMOS-based designs in terms of number of applied devices per cell and delay.

6.1 Introduction

CMOS technology scaling is reaching to its limits based on the Moores law beyond 2020. Recently discovered memristor devices [1] have attracted intensified research interests due

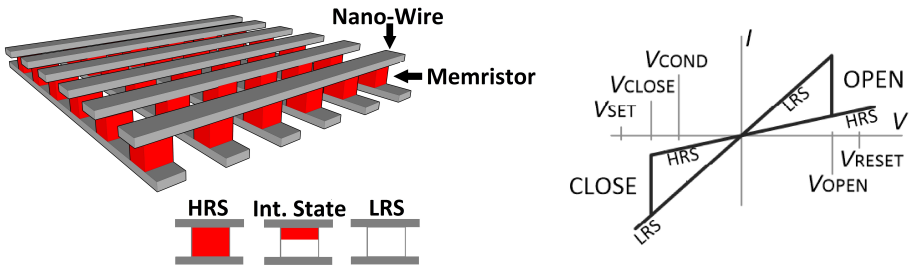
to their nanoscale features to replace conventional CMOS devices. One of the important application for these two terminal resistive switching devices is logic implementation and they are also used in arithmetic circuits [2]. Since memristor is capable of performing logic and memory operations it can be utilized for in-memory computation architectures which is beyond classical Von-Neumann architecture.

Various memristor-based logic implementation techniques are presented. Hybrid memristor/CMOS based logic in [3] is based on gaining the advantage of in silicon utilization. In this logic the voltage defines the logic value and it cannot store last logic state. Pure memristor-based logic implementations, e.g. Memristor Aided Logic (MAGIC) [4] and Material Implication Logic (IMPLY) [5], are merging memory and logic block in the same unit. In these logics unlike hybrid memristor/CMOS based logic, memristance of the output memristor shows output logic state. In memristive implication logic Boolean variables are considered by High Resistance State (HRS) and Low Resistance State (LRS) of binary memristor device where HRS and LRS states are considered for logic 0 and 1 respectively. The memristor-based IMPLY logic is a sequential process. Some memristor-based arithmetic circuits based on material implication logic were designed in [6], [8] and [11].

In this chapter, a memristor-based 4:2 compressor cell based on material implementation logic is implemented and compared with existing IMPLY-based designs. 4:2 compressor cells are key components in partial product reduction tree of parallel multipliers.

6.2 Memristor Device and Its Functionality

Transition oxide-based memristor devices are ion-migration-induced redox-based resistive switches. This kind of devices are belong to Valence Change Mechanism (VCM) class [7] and their functionality is based on anion migrations along the device. During SET process in VCM devices, oxygen ions or vacancies (O^{2-}) migrate toward anode and oxygen deficient region is generated along insulator film. Then the electrons emitted from cathode



(a) (b)

Figure 6.1: (a) Memristor-based crossbar structure. (b) Ideal VCM memristor I-V curve with different voltages for memristor switching between LRS and HRS.

are trapped by transition metal cations. The reduction in valence states of transition metal cations turns the oxide region conductive. At the anode, oxygen ions are oxidized and oxygen atoms are accumulated or released as oxygen gas. The VCM device changes its state to LRS at the end of the SET process.

The RESET procedure requires inverse voltage bias to device. The oxygen atoms gathered in anode are ionized and start to drift back as oxygen ions along the insulator film. At the end of the process of RESET the device is switched to HRS. Nano-crossbar layers of memristive devices can be placed over CMOS platform. Memristor logic states depends on amount and direction of charge passing through it. The crossbar memristor structure is displayed in Fig. 6.1. The voltages of V_{SET} and V_{RESET} should be greater than effective threshold voltage $|V_{\mathrm{OPEN}}|$ and $|V_{\mathrm{CLOSE}}|$ of VCM device respectively. Physical model [8] described TiO_2/TiO_{2-x} devices by dividing them into three regions: the conductive region, the transition region, and the insulating region. The switching time for SET procedure in TiO_2/TiO_{2-x} memristor to change device state from HRS to LRS is determined by [8],

$$t_{\mathrm{SET}} = \frac{{C_0}^2}{2\gamma_{\mathrm{t}}\beta V\lambda}. \tag{6.1}$$

The parameters γ_{t} and λ are the electron generating coefficient in the transition region and transition region length respectively. The parameter V is the voltage across device.

Other parameters, C_0 and β, can be determined by,

$$C_0 = \frac{\lambda}{2} + \left(\frac{n_\mathrm{c}}{n_\mathrm{i}}\right)\left(D - \frac{\lambda}{2}\right), \tag{6.2}$$

$$\beta = \frac{1}{4}\left(\frac{n_\mathrm{c}}{n_\mathrm{i}} - 1\right)^3 + \frac{2}{3}\left(\frac{n_\mathrm{c}}{n_\mathrm{i}} - 1\right)^2 + \frac{1}{2}\left(\frac{n_\mathrm{c}}{n_\mathrm{i}} - 1\right). \tag{6.3}$$

Here n_i and n_c are ions concentration in insulation and conduction regions respectively. Also D is thickness of device film. The RESET procedure switching time from LRS to HRS is [8],

$$t_\mathrm{RESET} = \frac{\left[\left(1 - \frac{n_\mathrm{c}}{n_\mathrm{i}}\right) D + 2C_0\right]\left(1 - \frac{n_\mathrm{c}}{n_\mathrm{i}}\right) D}{2\gamma_\mathrm{t}\beta V\lambda}. \tag{6.4}$$

6.3 Material Implication Logic with Memristor

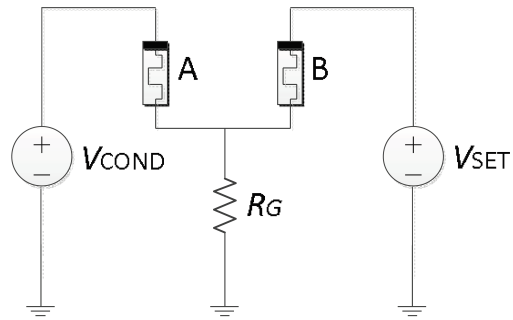
One of the specific realization of stateful logic with memristive device is material implication (IMP) [5]. Memristors can execute IMP logic as one of the fundamental Boolean logic operations. Memristor-based IMP gate is a simple circuit comprising of two electrically connected memristor devices and one grounded resistor. The IMP statement is defined as,

$$f = a \text{ IMP } b \cong a \rightarrow b \cong (a) \vee b \tag{6.5}$$

where f is only false if a is true and b is false. The IMP logic gate with memristor device is depicted in Fig. 6.2. Memristor A is considered as input memristor and memristor B is utilized as input/output device. The IMPLY logic with memristor has three main steps. Initializing the memristive devices based on the inputs is the first step. Then applying V_COND to memristor A and V_SET to memristor B simultaneously. The last step is reading out memristance of memristor B. In initialization of memristor devices each device based

Case	A	B	A IMP B
1	HRS (0)	HRS (0)	LRS (1)
2	HRS (0)	LRS (1)	LRS (1)
3	LRS (1)	HRS (0)	HRS (0)
4	LRS (1)	LRS (1)	LRS (1)

(a)



(b)

Figure 6.2: (a) IMPLY truth table. (b) Schematic of memristor-based IMPLY logic gate.

on the input value should be set to logic 0 (HRS) or logic 1 (LRS). The truth table of material implication logic and schematic of the IMP gate is shown in Fig. 6.2. The V_{COND} voltage magnitude is considered lower than V_{SET} ($|V_{\mathrm{COND}}| < |V_{\mathrm{SET}}|$). After this stage the output should be read by applying V_{READ} voltage pulse to the output memristor B. The resistance of R_{G} should be considered between R_{LRS} and R_{HRS} ($R_{\mathrm{LRS}} < R_{\mathrm{G}} < R_{\mathrm{HRS}}$). Also two V_{COND} and V_{SET} voltages are applied to the doped sides of A and B memristors respectively. The sequence of applying voltages to each memristive devices of the IMP gate in each stage for case 1 (a = 0, b = 0) is showed in Table. 1. In this case as it is stated in case 1 both devices should be adjusted to HRS initially. Therefore at first memristive device A should be switched with RESET pulse by duration of t_{RESET}. The same procedure is repeated again for device B in next step. At this point two devices are already switched to HRS state. Then V_{COND} and V_{SET} are imposed to A and B memristors. The voltage over the memristor B is determined by,

$$V_{\mathrm{B}} = \frac{R_{\mathrm{HRS}} + R_{\mathrm{G}}}{R_{\mathrm{HRS}} + 2R_{\mathrm{G}}} V_{\mathrm{SET}} + \frac{R_{\mathrm{G}}}{R_{\mathrm{HRS}} + 2R_{\mathrm{G}}} V_{\mathrm{COND}} \cong V_{\mathrm{SET}} \tag{6.6}$$

This voltage is enough to switch memristor B from HRS to LRS state. By considering the parameters in Table. 2 for device simulated in [8], -5.5 V for SET voltage and 5.5 V

Table 6.1: Material implication logic applied voltage sequence for case 1.

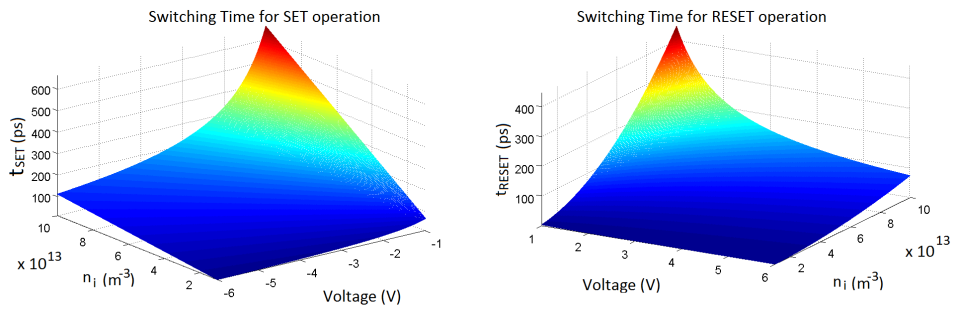
Memristors	**Init. A**	**Init. B**	**A IMP B**	**Read B**
A	V_{RESET}	0	V_{COND}	0
B	0	V_{RESET}	V_{SET}	V_{READ}

for RESET voltage over the device, minimum t_{SET} and t_{RESET} are about 70 ps and 25 ps respectively. The SET and RESET time behavior toward sweeping voltage over device and ions concentration in insulation region (n_{i}) parameters are displayed in Fig. 6.3. As it can be seen the worst speed performance is obtained in red region where n_{i} is about 10^{14} cm^{-3} and voltage is low ($|V| < 2$ V).

6.4 Memristor-based 4:2 Compressor Cell Designs

4:2 compressor cells are commonly utilized in high performance arithmetic systems and they are basic blocks in multipliers architecture. Parallel multipliers are consist of three main blocks: partial product generator, partial product reduction tree and final fast adder. Designing partial product tree is one of the key determining factors for improving speed, area and power consumption of multiplier. Several low power and high speed 4:2 compressor cell designs were presented by various digital logic style with conventional CMOS technology [9]. Memristor-based 4:2 compressor cell design can be applied in memristive crossbar architectures for signal processing application. The 4:2 compressor is a five-input/three-output device. It takes five equally weighted inputs $(X_1, X_2, X_3, X_4, C_{\mathrm{IN}})$ and produces a sum-bit (S), a carry-bit (C) and a carry-propagate-bit (C_{OUT}).
The Boolean expressions for outputs of 4:2 compressors are,

$$S = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{\mathrm{IN}}, \tag{6.7}$$



(a) (b)

Figure 6.3: (a) SET time behavior by sweeping voltage and n_{i}. (b) RESET time behavior by sweeping voltage and n_{i}.

Table 6.2: Material implication logic applied voltage sequence for case 1.

Parameters	**Value**	**Parameters**	**Value**	**Parameters**	**Value**
D(nm)	35	e(c)	1.602×10^{-19}	γ_{t}	2.3×10^{-6}
λ_0(nm)	$0.05D$	w_0(nm)	$0.15D$	γ_{i}	1×10^{-6}
$A(\mu\mathrm{m}^2)$	0.25	$n_{\mathrm{c}}(\mathrm{m}^{-3})$	8.75×10^{22}	$n_{\mathrm{i}}(\mathrm{m}^{-3})$	3×10^{13}

$$C = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{\mathrm{IN}} + \neg (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot X_4, \tag{6.8}$$

$$C = (X_1 \oplus X_2) \cdot X_3 + \neg (X_1 \oplus X_2) \cdot X_1, \tag{6.9}$$

Two primitive representations of 4:2 compressor cell are illustrated in Fig. 6.4. First design is comprised of two cascaded Full-Adder (FA). Further minimization of this design produces another representation comprising of four XOR gates and two multiplexers (MUX). Since with combination of FALSE and IMPLY logic, complete logic can be created, all basic logic gates can be implemented by applying IMPLY logic gate [3]. For implementing 4:2 compressor with two cascaded FA design two memristor-based full-adder implemented in [5] and [10] are utilized for two separate designs. The design with [5] full-adder requires 8 memristors and 58 computational cycles to complete its task. While by utilizing [10] full-adder with the same quantity of memristors, 44 computational steps are needed

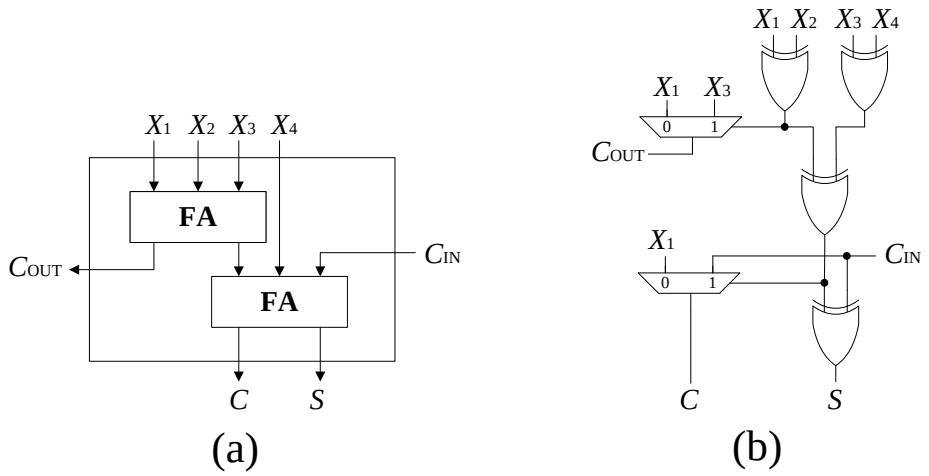


Figure 6.4: (a) FA design for 4:2 compressor. (b) XOR/MUX design.

to finish its operation. For designing 4:2 compressor with MUX/XOR design serial and parallel implementations can be applied. In the MUX/XOR design two blocks of XOR and MUX are required for implementation. The XOR block designed in [10] is utilized in two XOR/MUX designs of 4:2 compressor cells. The IMPLY-based implementation of applied XOR gate is [10],

$$A \oplus B = (A \text{ IMP } B) \text{ IMP } \neg (\neg A \text{ IMP } \neg B) . \tag{6.10}$$

This XOR design can be implemented by 4 memristors in 9 computational steps. For MUX circuit previously in [11] a 2 to 1 multiplexer with 13 computational steps (including initialization of devices) is designed with 6 memristors. Here a memristor-based MUX circuit with material implication logic is proposed by 4 memristors and 7 computational steps. By considering initialization of input memristors it needs 10 computational steps to complete its task. The proposed design utilizes memristors A and X as input devices. Also memristor B used as both input and output memristor. An additional memristor Y is applied for storing the values and performing FALSE operation during the procedure. The

Table 6.3: Memristor-based MUX computational steps.

Step	Logic	Value
1	False(Y)	Y = 0
2	X IMP Y	Y = $\neg X$
3	B IMP Y	Y = $\neg B$+$\neg X$
4	A IMP X	X = $\neg A$+X
5	FALSE(B)	B = 0
6	Y IMP B	B = $\neg$ Y=$B.X$
7	X IMP B	B = $\neg$ X+($B.X$)=$A.\neg X$+$A.X$

Table 6.4: Memristor logic states for proposed MUX in each step.

Memristors	**A**	**B**				**X**		**Y**		
Steps	$\mathrm{In_A}$	$\mathrm{In_B}$	5	6	7	$\mathrm{In_X}$	4	1	2	3
Case 1	0	0	0	0	**0**	0	1	0	1	1
Case 2	0	0	0	0	**0**	1	1	0	0	1
Case 3	0	1	0	0	**0**	0	1	0	1	1
Case 4	0	1	0	1	**1**	1	1	0	0	0
Case 5	1	0	0	0	**1**	0	0	0	1	1
Case 6	1	0	0	0	**0**	1	1	0	0	1
Case 7	1	1	0	0	**1**	0	0	0	1	1
Case 8	1	1	0	1	**1**	1	1	0	0	0
Value					**Output**					

computational steps and memristors logic states for proposed MUX are displayed in Table 3 and Table 4 respectively.

In first stage, logic statements of $\neg B$ + $\neg X$ and $\neg A + X$ should be generated. This can be done in three steps. First, FALSE operation should be applied on Y device to set it to HRS (logic 0). Then, $\neg X$ is stored in Y by utilizing IMPLY operation between X and Y device. Subsequently, by using IMPLY operation between B and Y the target logic statement of $\neg B + \neg X$ is stored in Y device. Finally, with IMPLY operation between A and X devices, $\neg A + X$ logic statement is stored in device X. Since an output of MUX device is $A.\neg X + B.X$, two stored logic statements in X and Y should be inverted first.

For this issue FALSE operation is applied to memristor B to change its state to HRS (logic 0). Then, inverse of the statement stored in Y is generated by IMPLY operation between Y and B and it is stored in B at the end of the step. The stored logic statement in B is $B.X$. In step 7 by IMPLY operation between X and B, the final logic statement stored in B becomes $A.\neg X + B.X$.

For serial implementation of 4:2 compressor XOR/MUX design, two different designs are proposed. First design has used the MUX circuit presented in [11] and the second design applied proposed MUX circuit. In XOR/MUX design with MUX circuit [11] 8 memristor devices are used and this design requires 64 computational steps. Second serial XOR/MUX design with proposed MUX circuit requires less devices and it has lower delay in comparison with first design. It needs 7 memristor devices for completing its task in 52 computational steps. Although these designs are efficient in terms of area and number of applied devices they are slower by considering current memristor technology and switching speed in comparison with conventional CMOS designs. For this purpose parallel implementation can be applied for increasing the speed of computations.

The parallel memristor-based XOR/MUX 4:2 compressor cell design requires 11 memristor devices and it requires 26 computational steps to finish its task as it is defined in Table 5. In this design, at first two XOR gates are implemented in parallel and it takes 9 steps for implementing them. The initialization of the input memristors is the first step for X_1, X_2, X_3 and X_4 devices. Also, all FALSE operations for 5 auxiliary memristors, $\mathrm{M}_{0,1,2,3,4,5}$, are completed in the first step in parallel. After that, XOR and MUX implementations are done in parallel. This stage requires 9 computational steps since XOR design last 9 steps with initialization which is 2 cycles more than proposed parallel MUX. The output of the MUX is stored in X_3 device in step 17 as $\mathrm{C}_{\mathrm{OUT}}$ of 4:2 compressor. In step 18, C_{IN} is applied to initialize C_1 and C_2 devices and FALSE operation is done for X_2, M_0, M_1, M_2, M_3 and M_4. In the last stage, XOR and MUX blocks are implemented in parallel to extract C and S. At the end of the procedure in step 26, device C_2 is stored C and M_0 is saved S.

By comparing proposed 4:2 compressor design in terms of delay with conventional CMOS designs with transmission gate and pass transistor logic in [9] the proposed parallel design showed acceptable speed performance. The delay of the circuits is determined by the time difference from when the inputs reach 10% of their swing until the output signal reaches 90% of its full potential measure. The worst case delay based on device parameter mentioned in Table 2 is 1.8 ns. Also in terms of area this model only applied 11 memristors while CMOS-based compressors with transmission gate and pass transistor logic are utilized 32 and 30 transistors respectively. The comparison for delay and device quantity per cell of the mentioned memristor-based designs with conventional CMOS designs are displayed in Fig. 6.5 and Fig. 6.6 respectively.

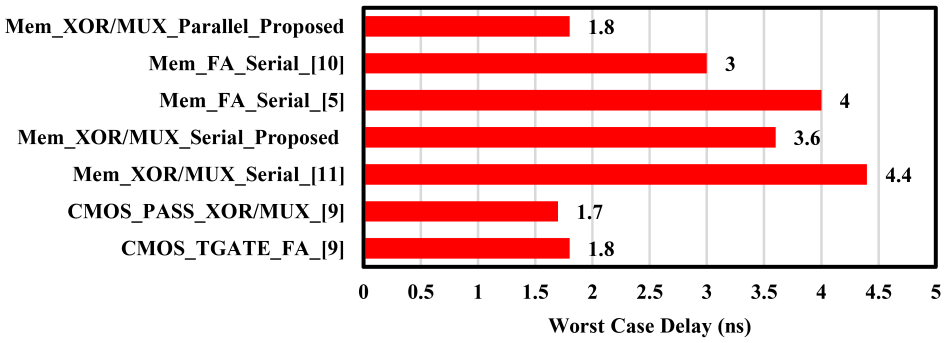


Figure 6.5: (a) FA design for 4:2 compressor. (b) XOR/MUX design.

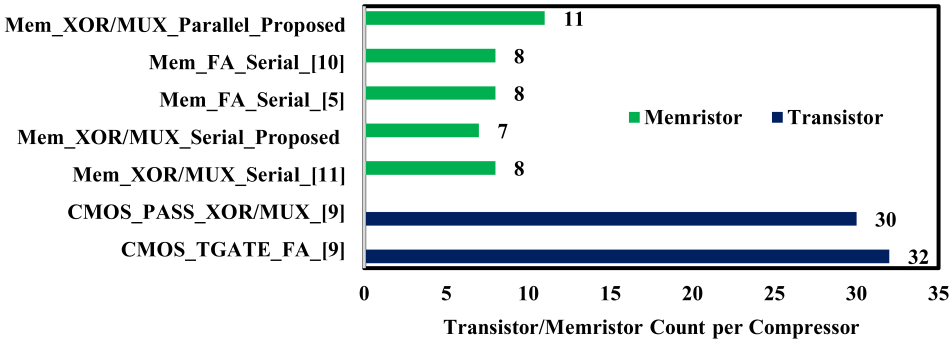


Figure 6.6: (a) FA design for 4:2 compressor. (b) XOR/MUX design.

Table 6.5: Computations are shown for each step of memristor-based 4:2 compressor operation.

Steps	**XOR1**	**XOR2**	**Steps**	**XOR3**	**MUX1**	**Steps**	**MUX2**	**XOR4**
1	$M_{0,1,2,3,4} = 0$		10	M_0 **IMP** M_1		19	X_4 **IMP** M_1	
2	X_1 IMP M_0	X_3 IMP M_2	**11**	M_0 IMP X_4	M_1 IMP X_2	**20**	M_1 IMP X_2	X_4 IMP M_0
3	X_2 IMP M_1	X_4 IMP M_3	**12**	M_2 IMP M_3	X_2 IMP M_4	**21**	X_2 IMP M_3	C_1 IMP M_4
4	X_1 IMP X_2	X_3 IMP X_4	**13**	M_0 IMP M_2	X_3 IMP M_4	**22**	C_2 IMP M_3	X_4 IMP C_1
5	M_0 IMP M_1	M_2 IMP M_3	**14**	X_4 IMP M_3	X_1 IMP X_2	**23**	X_1 IMP X_2	M_0 IMP M_4
6	$M_0 = 0$	$M_2 = 0$	**15**	$X_4 = 0$	$X_3 = 0$	**24**	$C_2 = 0$	$M_0 = 0$
7	M_1 IMP M_0	M_3 IMP M_2	**16**	M_3 IMP X_4	M_4 IMP X_3	**25**	M_3 IMP C_2	M_4 IMP M_0
8	X_2 IMP M_0	X_4 IMP M_2	**17**	M_2 IMP X_4	X_2 IMP X_3 = C_{OUT}	**26**	X_2 IMP $C_2 = C$	C_1 IMP $M_0 = S$
9	$M_{0,1,2,3,4} = 0, X_2 = 0, X_4 = 0$		**18**	$M_{0,1,2,3,4} = 0, X_2 = 0, C_{1,2} = C_{IN}$				

6.5 Conclusion

In this chapter, several memristor-based implementations by material implication logic for XOR/MUX and Full-adder based representation of 4:2 compressor are presented. The physical model of a VCM device is utilized to determine the SET and RESET time. The parallel implementation with memristor offers comparable speed with considerably less area in comparison with conventional CMOS-based peers that utilized pass transistor and transmission gate logic. Also all proposed memristor-based serial and parallel implementations of 4:2 compressor cells are compared with CMOS based design in terms of delay and number of device per cell.

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Chapter 7

Logic Design on Mirrored Memristive Crossbars

THIS chapter presents a hybrid CMOS-memristor logic design and implementation method on a novel mirrored crossbar architecture. The proposed structure supports in-memory computation and needs only one computational step to perform basic Boolean expressions. This logic can provide multiple fanins and/or fanouts, and does not have a destructive effect on input devices logical states. Various logic gates have been designed using the proposed structure. Simulation results and practical design constraints for different logic functions are presented, which confirms functionality of the method and its capability for large-scale memristive computations.

7.1 Introduction

Memristive crossbar array has been introduced as one of the promising candidates for future in-memory computation platforms due to the upcoming physical limitations on transistor scaling [1]. The non-volatility and high density in combination with logic implementation features make this device a viable alternative for the next generation of computers. Several

memristor-based logic designs have been presented during recent years [2-6]. In resistance based designs, the logical state 0 and logical state 1 are represented by device high resistance (R_{HRS}) and low resistance (R_{LRS}) states, respectively. This two terminal device has variable resistance, as the voltage greater than device threshold voltage, V_{TH}, has been applied to it. It can store the last resistance value after the voltage is dropped below its threshold or it is unpowered.

In Memristor Ratioed Logic (MRL) [3], memristor device is considered only as a computational element and its voltage is treated as the logical state. MRL logic suffers from signal degradation for implementation of AND and OR operations. This logic requires CMOS inverter block to perform NAND and NOR operations. Recently, several pure memristive techniques have been studied for logic in memory implementation [9-11]. Material implication logic (IMPLY) [2] is a resistance-based memristive logic. This logic can be implemented on memristive crossbar array, but suffers from high delay for implementation of Boolean expressions due to its sequential nature. Furthermore, another drawback for IMPLY logic is, storing the output over one of the inputs. MAGIC logic [11] performs any basic Boolean expression in one step (without considering the initialization step). In MAGIC, the input devices states can be altered after the operation is finished for some input combinations. Also this logic family cannot provide multiple fanouts.

In this chapter, a novel logic design is presented which requires only a single step to perform any basic Boolean function. The basic logic gates are implemented on two mirrored memristive crossbar arrays. This logic design is capable of providing multiple fanins and fanouts. Also, input and output memristor devices are separate and logic operation does not have a destructive effect on the input devices states.

7.2 Proposed Logic Design

The proposed logic design comprises of memristor devices and a switch within logic gates. The memristor device has variable resistance and by applying a voltage higher than a specific threshold (V_{TH}) over it, the doping profile of transition oxide filament is changed between two main states: High Resistance State (HRS) and Low Resistance State (LRS). The resistance of the memristor devices represents the logical states in this logic. In this logic, high resistance (R_{HRS}) and low resistance (R_{LRS}) are considered as logic 0 and logic 1, respectively. The polarity of memristor is represented by a thick black bar. The resistance of memristor decreases as current flows into the device from the bar side (negative side) and it increases when current enters the device from the non-bar side (positive side). Here, memristor model [12] with threshold has been utilized for simulations. The input and output memristors are separate in this logic and the input devices' logical states are not altered during the operation. The inputs of this logic should be set based on the input combination in initialization stage. The proposed logic gates require only one computational step to perform their operations without considering the initialization step.

7.2.1 NOR Gate

In the proposed NOR gate two memristors ($\mathrm{M_A}$, $\mathrm{M_B}$) are connected in parallel. The positive side of these input devices is connected to the negative side of the grounded memristor ($\mathrm{M_G}$). The common node of these three devices is connected to the gate terminal of the switch. The source terminal of the switch is connected to the positive side of grounded output device ($\mathrm{M_{OUT}}$). The voltage V_{COND} is applied to the negative side of input devices. The voltage V_{WR} is applied to drain terminal of the switch. The circuit schematic for NOR gate is illustrated in Fig.7.1(a). The inputs are resistances of memristors $\mathrm{M_A}$ and $\mathrm{M_B}$. The output is the final resistance of memristor $\mathrm{M_{OUT}}$. In the initialization stage, the input devices should be set to the desired states. Also, $\mathrm{M_G}$ and $\mathrm{M_{OUT}}$ devices should be set to low

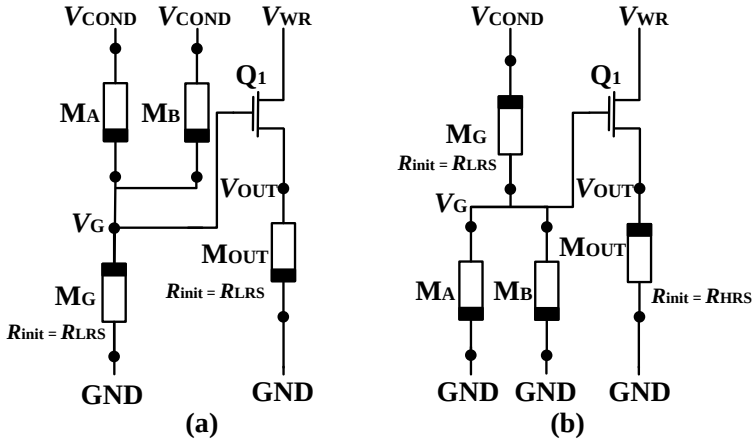

Figure 7.1: The schematic of logic circuits. (a) NOR gate. (b) NAND gate.

resistance. V_{COND} is applied to the sensing branch, where the inputs and $\mathrm{M_G}$ are placed. The value of V_{COND} should be selected in a range that the voltages over input memristors in the sensing branch become less than threshold voltage (V_{TH}) of each input devices. The voltage over $\mathrm{M_G}$ in the sensing branch, V_{G}, defines the switch ($\mathrm{Q_1}$) status. In the writing branch of the circuit, V_{WR} is applied to the drain of $\mathrm{Q_1}$. The voltage of V_{WR} should be sufficient to change the logical state of output device ($\mathrm{M_{OUT}}$). According to Kirchhoff's law, the V_{G} voltage can be determined by,

$$\frac{V_{\mathrm{G}}}{R_{\mathrm{G}}} + \frac{V_{\mathrm{G}} - V_{\mathrm{COND}}}{R_{\mathrm{A}}} + \frac{V_{\mathrm{G}} - V_{\mathrm{COND}}}{R_{\mathrm{B}}} = 0, \tag{7.1}$$

where R_{A}, R_{B} and R_{G} are the memristances of $\mathrm{M_A}$, $\mathrm{M_B}$ and $\mathrm{M_G}$, respectively. The V_{G} voltage is,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{R_{\mathrm{G}} \left(R_{\mathrm{A}} + R_{\mathrm{B}} \right)}{R_{\mathrm{G}} \left(R_{\mathrm{A}} + R_{\mathrm{B}} \right) + R_{\mathrm{A}} R_{\mathrm{B}}} \right). \tag{7.2}$$

Based on different input combinations the logic gate output can be concluded as follows:

$\mathrm{A} = 0, \mathrm{B} = 0$

In this case both input memristors, $\mathrm{M_A}$ and $\mathrm{M_B}$, are initialized to the high resistance state (R_{HRS}), which corresponds to logic 0. The $\mathrm{M_G}$ device memristance is set to R_{LRS}. By assuming $R_{\mathrm{HRS}} \gg R_{\mathrm{LRS}}$, in the operation mode, when V_{COND} is applied to sensing branch, the voltage of V_{G} becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{2R_{\mathrm{HRS}}R_{\mathrm{LRS}}}{2R_{\mathrm{HRS}}R_{\mathrm{LRS}} + R_{\mathrm{HRS}}^2} \right) \approx 0. \tag{7.3}$$

The voltage of V_{G} becomes smaller than the threshold of the switch (V_{Tsw}). Therefore $\mathrm{Q_1}$ remains OFF and there is no current in the output device $\mathrm{M_{OUT}}$. The $\mathrm{M_{OUT}}$ memristance remains on R_{LRS} which corresponds to logic 1.

$\mathrm{A} = 0, \mathrm{B} = 1$

First step is initialization of $\mathrm{M_A}$ and $\mathrm{M_B}$ to R_{HRS} and R_{LRS}, respectively. In operation step, the voltage V_{G} becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{R_{\mathrm{HRS}}R_{\mathrm{LRS}} + R_{\mathrm{LRS}}^2}{2R_{\mathrm{HRS}}R_{\mathrm{LRS}} + R_{\mathrm{LRS}}^2} \right) \approx \frac{V_{\mathrm{COND}}}{2}. \tag{7.4}$$

Since $\frac{V_{\mathrm{COND}}}{2}$ is greater than V_{Tsw}, $\mathrm{Q_1}$ turns ON. The current goes through $\mathrm{M_{OUT}}$ device and the voltage of V_{OUT} becomes greater than V_{TH} of memristor. Therefore the memristance starts to change from R_{LRS} (logic 1) to R_{HRS} (logic 0).

$\mathrm{A} = 1, \mathrm{B} = 0$

In the initialization step, $\mathrm{M_A}$ and $\mathrm{M_B}$ are set to R_{LRS} and R_{HRS}, respectively. This case is exactly the same as the case 2 after initialization stage.

$\mathrm{A} = 1, \mathrm{B} = 1$

In operation step, the voltage V_{G} becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{2R_{\mathrm{LRS}}^2}{3R_{\mathrm{LRS}}^2} \right) = \frac{2V_{\mathrm{COND}}}{3}. \tag{7.5}$$

Q_1 becomes ON, as voltage of $\frac{2V_{\mathrm{COND}}}{3}$ is greater than V_{Tsw}. Therefore, the current flows through the output device $\mathrm{M}_{\mathrm{OUT}}$ and the voltage over it becomes greater than memristor threshold voltage V_{TH}. This results in changing the state of $\mathrm{M}_{\mathrm{OUT}}$ from R_{LRS} (logic 1) to R_{HRS} (logic 0).

7.2.2 NAND Gate

The schematic of the proposed NAND gate circuit is shown in Fig.7.1(b). Two input memristors M_{A} and M_{B} are connected together in parallel similar to the NOR logic gate. The M_{G} memristor is placed on top of two parallel input devices and connected to the positive side of them. Two input devices are grounded from negative terminals. The V_{COND} is applied to negative side of M_{G}, where The memristances of M_{G} and $\mathrm{M}_{\mathrm{OUT}}$ devices are initialized to R_{LRS} and R_{HRS}, respectively. The voltage V_{G} is determined by,

$$\frac{V_{\mathrm{G}}}{R_{\mathrm{A}}} + \frac{V_{\mathrm{G}}}{R_{\mathrm{B}}} + \frac{V_{\mathrm{G}} - V_{\mathrm{COND}}}{R_{\mathrm{G}}} = 0, \tag{7.6}$$

By simplifying this equation, the voltage V_{G} becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{R_{\mathrm{A}} R_{\mathrm{B}}}{R_{\mathrm{G}} \left(R_{\mathrm{A}} + R_{\mathrm{B}} \right) + R_{\mathrm{A}} R_{\mathrm{B}}} \right). \tag{7.7}$$

The proposed NAND gate output for different input combinations can be determined as follows:

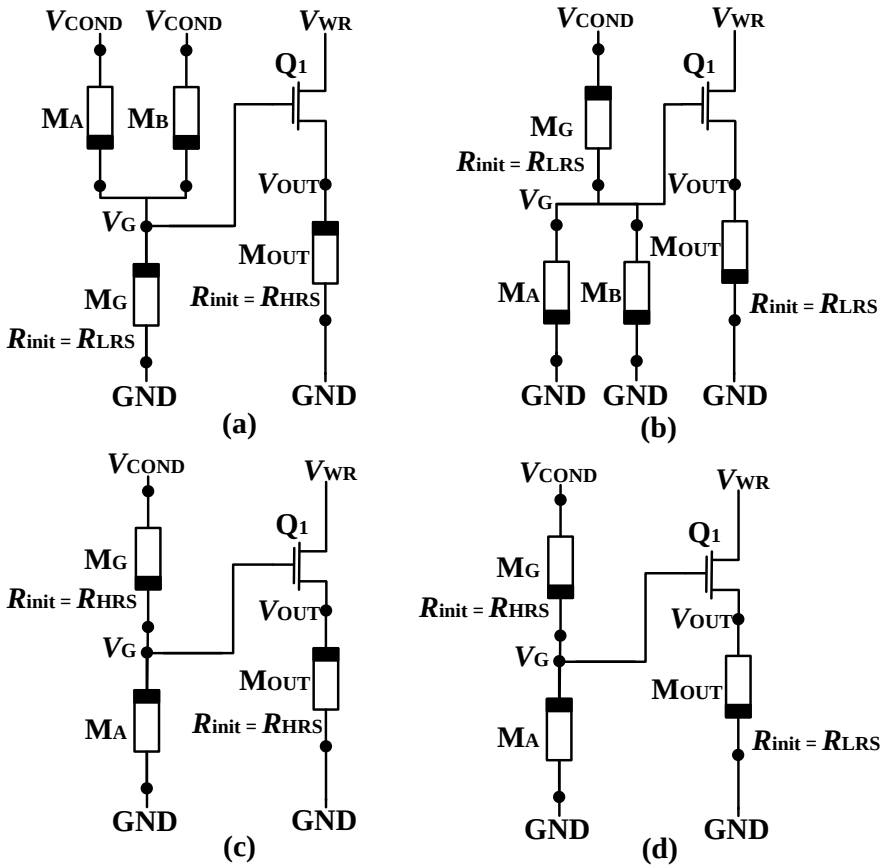

Figure 7.2: The Schematic of the proposed logic gates. (a) OR gate. (b)AND gate. (c) NOT gate. (d) COPY circuit.

$\mathrm{A} = 0, \mathrm{B} = 0$

After the initialization step, The voltage V_{G} in this case for operation mode becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{R_{\mathrm{HRS}}^2}{2R_{\mathrm{HRS}}^2 + R_{\mathrm{HRS}} R_{\mathrm{LRS}}} \right) \approx \frac{V_{\mathrm{COND}}}{2}. \tag{7.8}$$

This voltage is greater than V_{Tsw} and it turns Q_1 ON. The current goes from V_{WR} voltage source to the output device, $\mathrm{M}_{\mathrm{OUT}}$. The resistance of the $\mathrm{M}_{\mathrm{OUT}}$ starts to decrease from R_{HRS} (logic 0) to R_{LRS} (logic 1).

$\mathrm{A} = 0, \mathrm{B} = 1$

After initialization step, the voltage V_{G} in operation step becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{R_{\mathrm{HRS}} R_{\mathrm{LRS}}}{2R_{\mathrm{HRS}} R_{\mathrm{LRS}} + R_{\mathrm{LRS}}^2} \right) \approx \frac{V_{\mathrm{COND}}}{2}. \tag{7.9}$$

Q_1 turns ON, as its gate voltage is greater than the threshold voltage, V_{Tsw}. The voltage over the output device (V_{OUT}) becomes greater than the V_{TH} of memristor. The $\mathrm{M}_{\mathrm{OUT}}$ device changes state from logic 0 to logic 1.

$\mathrm{A} = 1, \mathrm{B} = 0$

This case is exactly the same as case (2) after initialization step.

$\mathrm{A} = 1, \mathrm{B} = 1$

In this case, after initializing the devices to desired states, the voltage of V_{G} in operation step becomes,

$$V_{\mathrm{G}} = V_{\mathrm{COND}} \left(\frac{R_{\mathrm{LRS}}^2}{3R_{\mathrm{LRS}}^2} \right) = \frac{V_{\mathrm{COND}}}{3}. \tag{7.10}$$

Since $\frac{V_{\mathrm{COND}}}{3}$ is lower than V_{Tsw}, Q_1 remains OFF. Therefore the output device remains on its last state (logic 0).

7.2.3 Other Logic Gates

The schematic of OR gate is illustrated in Fig. 7.2(a). The only difference with NOR gate is the $\mathrm{M}_{\mathrm{OUT}}$ memristor polarity and initial memristance. The memristance of $\mathrm{M}_{\mathrm{OUT}}$ is set to R_{HRS} (logic 0) initially. The proposed AND gate is illustrated in Fig. 7.2(b), which has a similar topology as the NAND gate but the polarity of $\mathrm{M}_{\mathrm{OUT}}$ device is opposite. The memristance of $\mathrm{M}_{\mathrm{OUT}}$ is set to R_{LRS} (logic 1) initially. In this design, NOT gate consists

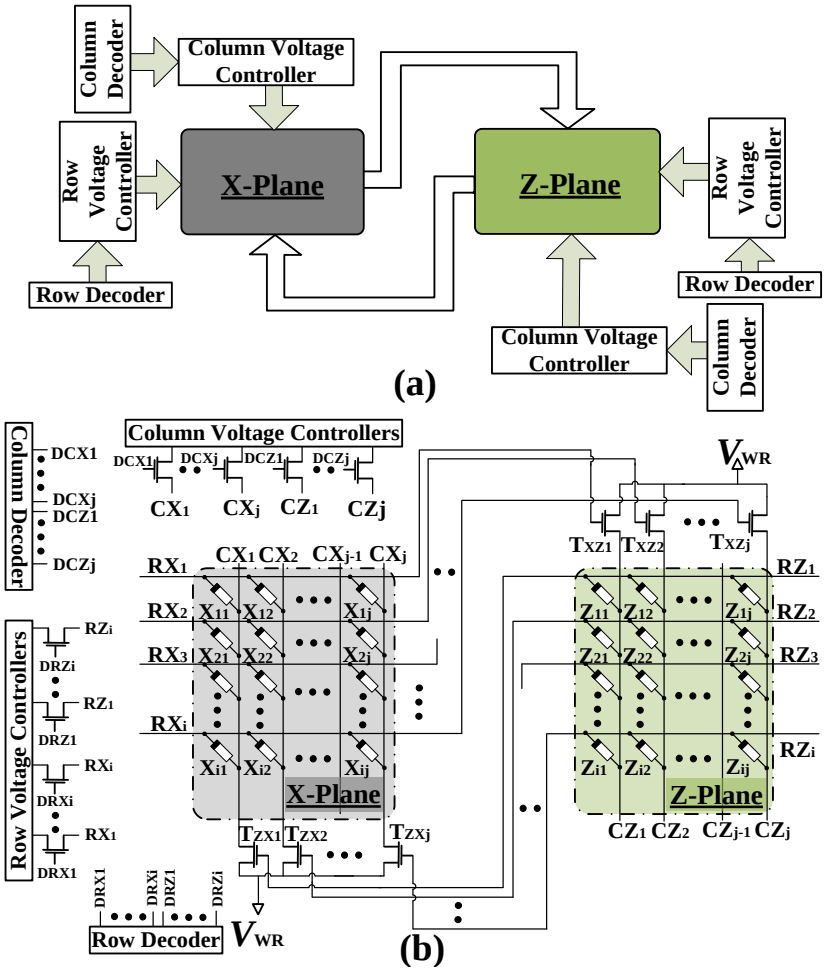

Figure 7.3: The proposed architecture. (a) Block diagram of the proposed architecture. (b) Mirrored memristive crossbar architecture.

of two memristors, $\mathrm{M_A}$ (input device) and $\mathrm{M_G}$, in sensing branch. As it is displayed in Fig. 2(c), the output device $\mathrm{M_{OUT}}$ is connected from its positive side to source terminal of $\mathrm{Q_1}$ and grounded from the other side. The schematic of NOT gate is displayed in Fig. 7.2(c). In initialization step, both of $\mathrm{M_G}$ and $\mathrm{M_{OUT}}$ devices are initialized to R_{HRS}. Here, COPY circuit is designed to store a value from one memristive cell to others. The proposed circuit schematic is displayed in Fig. 7.2(d). The polarity of $\mathrm{M_{OUT}}$ device and its initial memristance (R_{LRS}) is its only difference from the NOT gate. The operation principles of OR, AND, NOT and COPY gates are presented in Table 7.1

Table 7.1: The operation principles for OR, AND, NOT and COPY circuits for different input combinations.

Case	**OR**		**AND**		**Case**	**NOT**		**COPY**	
	V_{G}	R_{OUT}	V_{G}	R_{OUT}		V_{G}	R_{OUT}	V_{G}	R_{OUT}
A = 0, B = 0	$V_{\mathrm{COND}}\left(\frac{2R_{\mathrm{LRS}}}{R_{\mathrm{HRS}}}\right)$	R_{HRS}	$\approx \frac{V_{\mathrm{COND}}}{2}$	R_{HRS}	A = 0	$\frac{V_{\mathrm{COND}}}{2}$	R_{LRS}	$\frac{V_{\mathrm{COND}}}{2}$	R_{HRS}
A = 0, B = 1	$\approx \frac{V_{\mathrm{COND}}}{2}$	R_{LRS}	$\approx \frac{V_{\mathrm{COND}}}{2}$	R_{HRS}					
A = 1, B = 0	$\approx \frac{V_{\mathrm{COND}}}{2}$	R_{LRS}	$\approx \frac{V_{\mathrm{COND}}}{2}$	R_{HRS}	A = 1	$V_{\mathrm{COND}}\left(\frac{R_{\mathrm{LRS}}}{R_{\mathrm{HRS}}}\right)$	R_{HRS}	$V_{\mathrm{COND}}\left(\frac{R_{\mathrm{LRS}}}{R_{\mathrm{HRS}}}\right)$	R_{LRS}
A = 1, B = 1	$\frac{2V_{\mathrm{COND}}}{3}$	R_{LRS}	$\frac{V_{\mathrm{COND}}}{3}$	R_{LRS}					

7.3 Logic Synthesis on Mirrored Memristive Crossbars

The proposed logic design method can be realized on two mirrored memristive crossbar arrays (X and Z planes), which are connected to each other by switches. The proposed architecture is displayed in Fig. 7.3. This architecture is functional for implementation of other logic families, like MAGIC [11] and has a higher density in comparison with other hybrid CMOS-memristor architectures like 1T1M structure [9].

In each logic operation, one crossbar plane is used for implementation of sensing branch and the other one is used for writing branch. Hence, the inputs and outputs of each operation, are placed on different crossbar planes.

As can be seen in Fig. 7.3, multiple memristive devices (X_{11}, X_{12}, ..., X_{ij}) in each row of the X-plane crossbar is connected with one switch (T_{XZ1}, T_{XZ2}, ..., T_{XZj}) to the memristive devices (Z_{11}, Z_{12}, ..., Z_{ij}) in corresponding column of the Z-plane crossbar. Furthermore, a row decoder is required to provide signals (DRX_1, ..., DRX_i, DRZ_1, ..., DRZ_i) to select the rows on both crossbar planes. Also, a column decoder is considered to generate column select signals (DCX_1, ..., DCX_j, DCZ_1, ..., DCZ_j) for both planes.

Two voltage controllers apply desired voltages to rows and columns of the architecture. The row and column voltage controllers are responsible to provide the voltage for each row (RX_1, ..., RX_i, RZ_1, ..., RZ_i) and column (CX_1, ..., CX_j, CZ_1, ..., CZ_j), respectively. The voltages V_{COND} and V_{PRO} along with ground (0 V) and float status are provided by the voltage controllers.

The voltage V_{PRO} is applied to unselected lines to avoid unwanted changes in device states during the logic operation. This voltage should be chosen in a domain, which does not have an influence on the state of memristors in the unselected lines. The NOR-based architecture supports NOR and COPY operations in one step. Also, NAND-based architecture can be used to implement NAND logic in one step by reconfiguring the switches.

All logic operations can be implemented by these architectures. For implementation of single NOR gate on a NOR-based architecture with $i \times j$ crossbar arrays as sensing branch is placed on first row ($\mathrm{RX_1}$) of the X-plane crossbar, the voltage V_{COND} is applied to $\mathrm{CX_1}$ and $\mathrm{CX_2}$ columns. Column $\mathrm{CX_3}$ is grounded and V_{PRO} voltage is applied to the rest of unselected columns ($\mathrm{CX_4}$, ..., $\mathrm{CX_j}$) and rows ($\mathrm{RX_2}$, ..., $\mathrm{RX_i}$). Then V_{PRO} voltage can be determined by,

$$(V_{\mathrm{G}} - V_{\mathrm{COND}}) \left((R_{\mathrm{X_{11}}})^{-1} + (R_{\mathrm{X_{12}}})^{-1}\right) + V_{\mathrm{G}} R_{\mathrm{LRS}}^{-1} + (V_{\mathrm{G}} - V_{\mathrm{PRO}}) R_{\mathrm{LRS}}^{-1} \times (j-3) = 0. \tag{7.11}$$

The voltage V_{PRO} should be set at the same level of V_{G} (V_{RX1}) to avoid change in state of unselected devices on row $\mathrm{RX_1}$. By considering $V_{\mathrm{PRO}} = V_{\mathrm{G}}$, for $\mathrm{X_{11}}$ = 0, $\mathrm{X_{12}}$ = 0 input combination, the voltage V_{PRO} is $V_{\mathrm{COND}}/(\alpha + 2)$ where $\alpha = R_{\mathrm{HRS}}/R_{\mathrm{LRS}}$. For $\mathrm{X_{11}}$ = 1, $\mathrm{X_{12}}$ = 1 input combination, the voltage V_{PRO} is $2V_{\mathrm{COND}}/3$. By considering that α has a high value, $2V_{\mathrm{COND}}/3$ is bigger than $V_{\mathrm{COND}}/(\alpha+2)$. The voltage $|V_{\mathrm{PRO}} - V_{\mathrm{RX1}}|$ should be less than V_{TH}. By considering the appropriate configuration of applied voltages and lower number of alternate current paths within this structure in comparison with conventional crossbar, the sneak path effect is largely mitigated in the proposed design. In addition, logic implementation on two crossbar arrays which are isolated by transistor switches makes this design more resilient to form closed loops between logic input and output memristors.

The initialization procedure for this crossbar structure is a two-step process. It writes desired values on entire row of selected crossbar array. In the first step for writing logic 1 on target devices, a voltage of V_{COND} ($> V_{\mathrm{TH}}$) and V_{PRO} are applied to a selected row and all unwanted rows, respectively. Also, the columns on which logic 1 should be written, are grounded and a voltage V_{PRO} is applied to the other columns. In the second step, the selected row is grounded and the voltage of V_{PRO} is applied to all unwanted rows. Furthermore, a voltage of V_{COND} and V_{PRO} are applied to the columns which logic 0 should be written on and other columns, respectively. This step will write logic 0 on all target

devices in the selected row.

7.4 Simulation Results and Design Constraints

The proposed logic gates are simulated in Cadence Virtuoso and linear boundary drift memristor model with threshold and Biolek window function [12] are utilized for simulation. The 65nm CMOS technology has been utilized for the switch in logic gates. The circuits are designed by using the following parameters: $D = 3$ nm, $R_{\text{HRS}} = 10$ kΩ, $R_{\text{LRS}} = 1$ kΩ, $\mu_v = 8 \times 10^{-8}$ m^2 V^{-1}s^{-1}, $V_{\text{TH}} = 0.8$ V, p = 2, $V_{\text{Tsw}} \approx 450$ mV, $V_{\text{COND}} = 1.1$ V, $V_{\text{PRO}} = 0.4$ V, $V_{\text{WR}} = 2.5$ V. Parameters D and μ_v are device thickness and mobility of dopants, respectively. Parameter p is a positive integer in window function of the model and it adjusts the non-linearity of the model [12]. The behavior and speed of NOR, OR, NAND and AND gates are displayed in Fig. 7.4. The slowest input case is considered as delay for proposed logic gates. As it can be seen in Fig. 7.4(a), the proposed NOR gate has a delay around 1.356 ns for its slowest cases ($\text{A} = 0, \text{B} = 1$ and $\text{A} = 1, \text{B} = 0$). The parallel plate capacitance and line capacitance have been determined for each memristor in crossbar array. The parallel plate capacitance determined to be 205.32 aF by considering the plate area of device 2500 nm^2. The wire capacitance for each set of parallel wires in crossbar is determined to be 2.68×10^{-11} F/m, by considering half the spacing between wires and thickness of strips are 25 nm and 50 nm, respectively. This value is multiplied by 100 nm, the length of wire segments associated with each memristor in light of 25% packing density, and the wire capacitance per device has been obtained 2.68 aF. To determine the total capacitance for each device, the parallel plate capacitance of memristor is added to double the wire segment capacitance (for both horizontal and vertical wires). The total capacitance per each device is determined to be 216.51 aF. This capacitance has been added to the simulations in Cadence Virtuoso and it was determined that this was not enough capacitance to alter the operation in crossbar. The low R_{HRS} $(10\,\text{k}\Omega)$ of the device

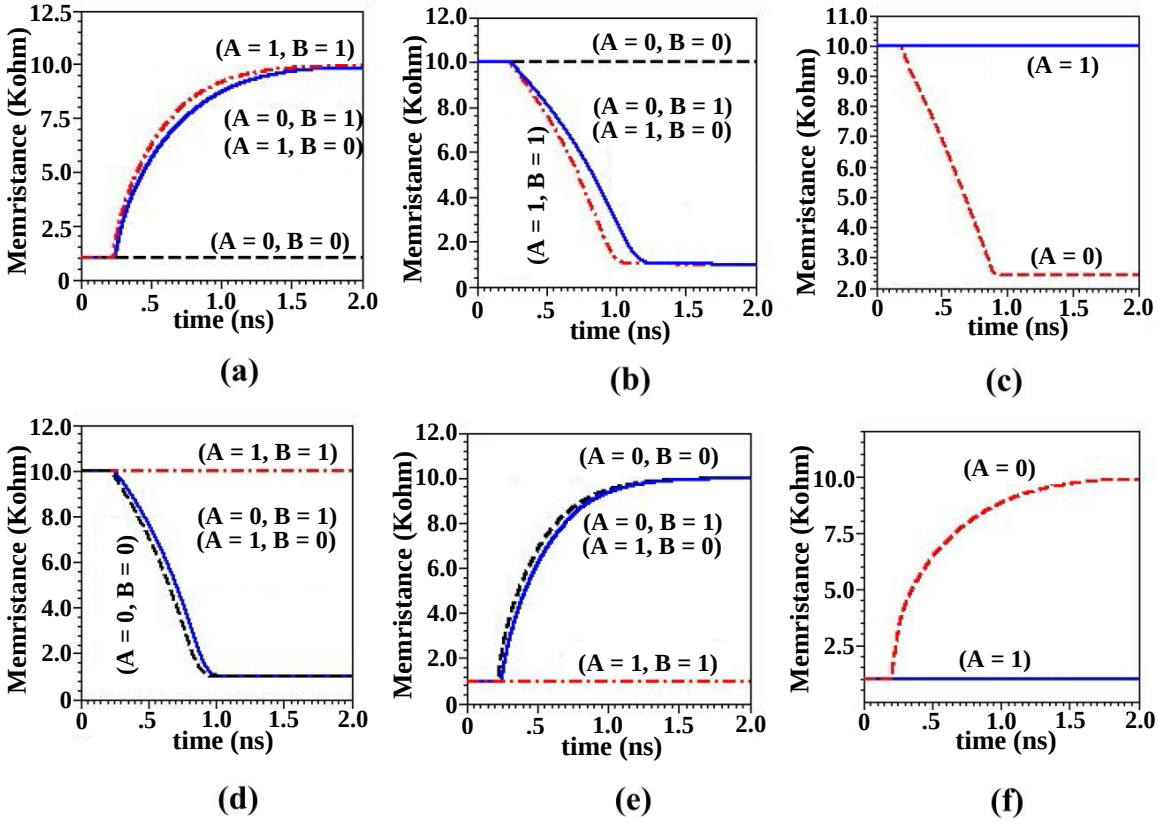

Figure 7.4: The simulation results are for following logic gates: (a) NOR gate. (b) OR gate. (c) NOT gate. (d) NAND gate. (e) AND gate. (f) COPY circuit.

leads to an RC time constant of 2.16 ps which is negligible in comparison with the average operation time of the gates (1 ns). The delay and output final state error of the proposed logic gates are displayed in Table 7.2. This error is the percentage error of the final state of $\mathrm{M_{OUT}}$ device from the ideal value. The main source for the error is due to the model and by changing parameter p error has been altered.

The voltage over inputs in sensing branch should not change the input devices states. For having a non-destructive voltage over the inputs and right functionality of the gates to have right outputs value, the V_{COND} voltage should be selected in a specific range. The proposed logic gates can be implemented with multiple inputs. Design constraints for selecting V_{COND} of n-input version of the proposed logic gates are displayed in Table 7.3. These are

Table 7.2: Delay and output final state absolute error for each gate.

Logic	NOR	OR	NAND	AND	NOT
Delay (ns)	1.356	1.112	0.853	1.245	0.801
Error (%)	0.085	0.003	0.001	0.033	0.005

Table 7.3: Design constraints for V_{COND} in proposed logic gates.

Logic	Design Constraints - Multiple Inputs
NOR-OR	$\left(V_{\mathrm{Tsw}}\left(\frac{2R_{\mathrm{HRS}}+(n-1)R_{\mathrm{LRS}}^{n-1}}{R_{\mathrm{HRS}}+(n-1)R_{\mathrm{LRS}}^{n-1}}\right), V_{\mathrm{TH}}\left(2+\frac{n-1}{\alpha}\right)\right)$
NAND-AND	$\left(V_{\mathrm{Tsw}}\left(2+\frac{n-1}{\alpha}\right), V_{\mathrm{TH}}\left(n+\frac{1}{\alpha}\right)\right)$
NOT-COPY	$(2V_{\mathrm{Tsw}}, 2V_{\mathrm{TH}})$

valid values for V_{COND} which ensures the right functionality and avoiding logic failure for each logic gates. The V_{COND} should be selected in a domain which does not change the input devices state and can produce appropriate voltage V_{G} for switching the CMOS during the operation. This design can provide right functionality even for input devices resistance states variation obtained after programming. NOR logic can tolerate variation in input devices resistance up to 40% and 20% for R_{HRS} and R_{LRS}, respectively. Also, the proposed design is feasible by considering a real device kinetics [7] and non-linear relationship of voltage and switching time with $50\ \mathrm{mV/dec}$ slope for voltage-switching time diagram [8]. In this design, each gate can have multiple fanouts. Multiple devices can be connected in parallel in the writing branch of the circuit as it is displayed in Fig. 7.5. With this feature, there will be no need for additional COPY operation in crossbar memory. Hence, it reduces the delay in large-scale computations considerably. In the proposed logic, the number of fanouts is limited and it is dependent to the drain source resistance of CMOS. The higher the number of the fanouts the lower the equivalent output devices resistance in the writing branch. This results in decreasing the voltage over the output devices. By reaching this voltage under threshold voltage of memristor (V_{TH}) the desired logic cannot be written over the output devices. The average total energy consumption per operation for proposed NOR gate is about $200\ \mathrm{fJ}$. Unlike CMOS logic, the proposed logic does not need static

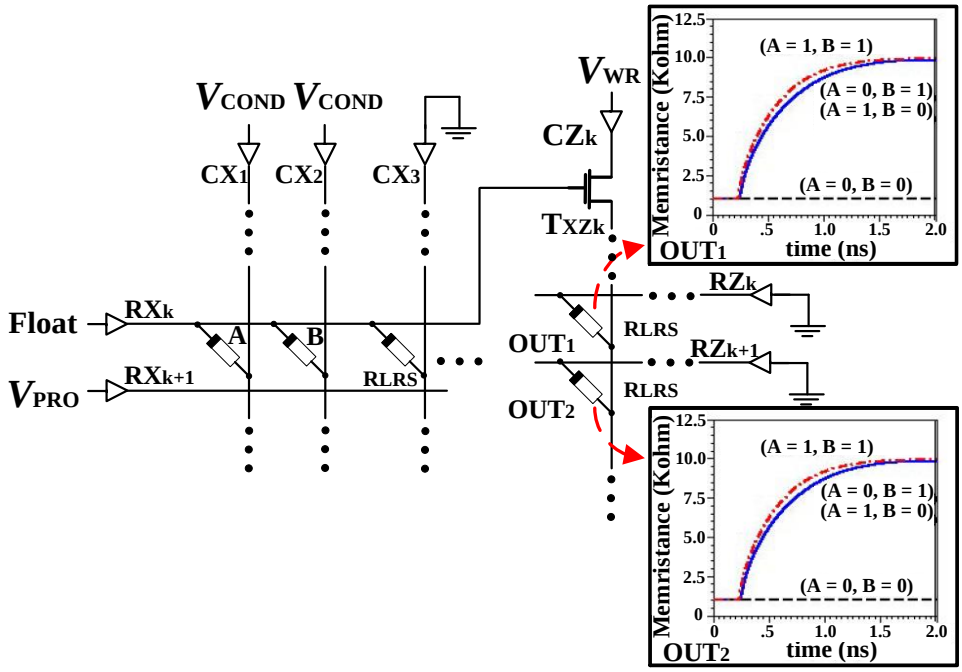

Figure 7.5: Multiple fanouts and simulation results for each output.

power and power for memory refresh in DRAM to keep the output. Also, SRAM has a leakage energy which does not exist in the memristor-based systems, because memristor does not require power to retain its memory state, and transistors in the crossbar arrays are only active during the logic operation or when read/write pulses are activated for memory operations. In addition, considering density and in memory computation capabilities of this approach, other implementation costs (i.e. area and speed) can be considerably lower in long term progress of this technology. As it can be seen in Fig. 7.6, XNOR logic is implemented with 3 computational steps on 4×4 mirrored memristive crossbar arrays. The sequence of applied voltage levels to the corresponding rows and columns of the architecture are defined in Table 7.4. As it can be seen, for each computational step the applied voltage is displayed by a 16-bits word. The V_{COND}, V_{PRO}, ground and float are displayed with $\mathrm{c}, \mathrm{p}, \mathrm{g}$ and f, respectively. The delay for implementation of XNOR function is 4.755 ns as it can be seen from simulation results in Fig. 7.7.

Table 7.4: The 16-bits words for voltage controller select signals in each step for XNOR implementation.

Step	RX_i	CX_j	RZ_i	CZ_j
	i = 1,2,3,4	j = 1,2,3,4	i = 1,2,3,4	j = 1,2,3,4
1	fppp	ccgp	ggff	ffff
2	fgff	ffff	ffpp	ccgp
3	pfpp	ccgp	ffgf	ffff

7.5 Conclusion

Hybrid CMOS-memristor based logic design is presented along with its implementation on crossbar arrays. The basic logic gates are implemented by proposed design. This logic requires only one computational step to perform any basic Boolean expression. The state of input devices remains unchanged during logic gates operation. An architecture presented by utilizing mirrored memristive crossbar arrays connected with CMOS switches for implementation of the proposed logic. Different logic functions are implemented with this architecture for testing the functionality of the design.

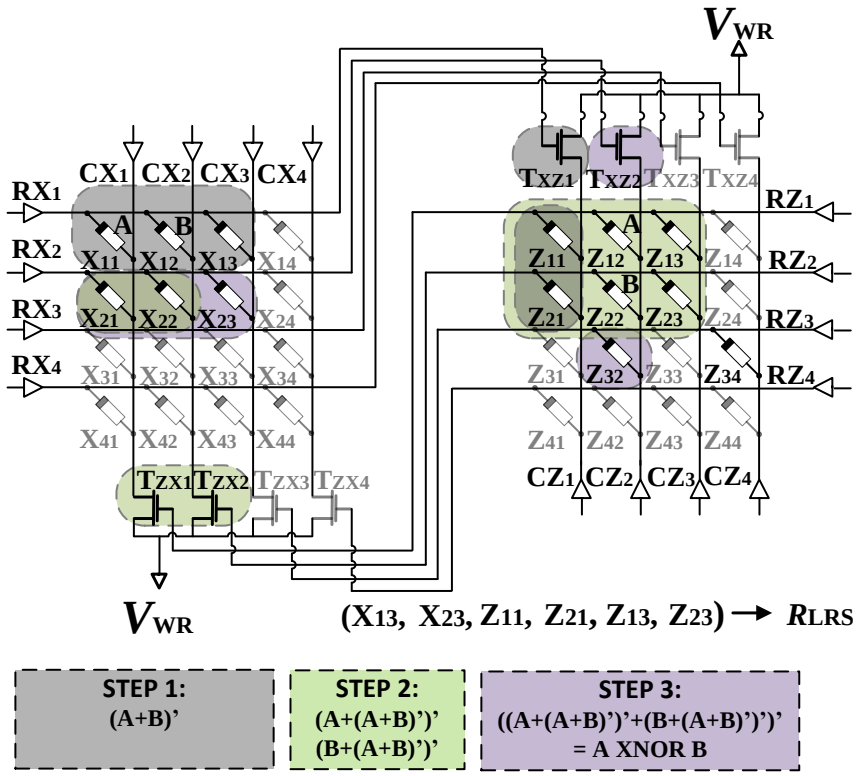

Figure 7.6: Implementation of XNOR function over two mirrored crossbar array.

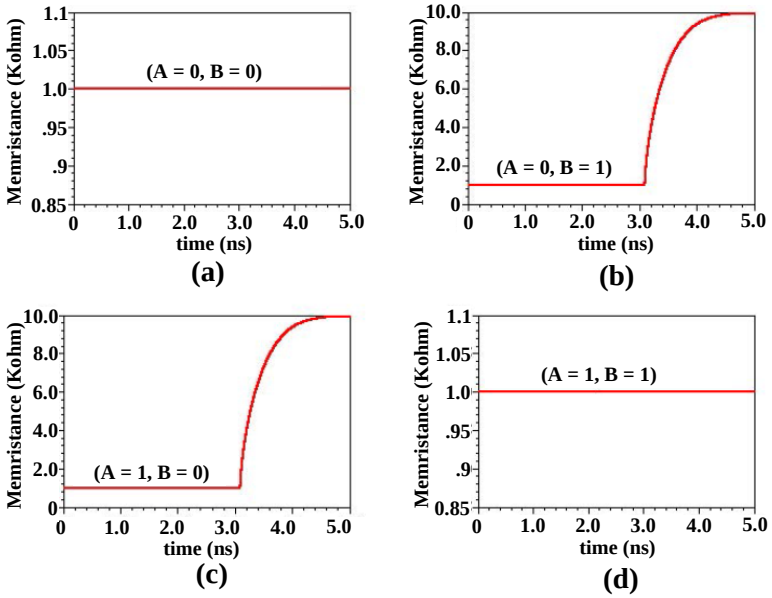

Figure 7.7: The simulation results for XNOR implementation on two mirrored memristive crossbars. This results are extracted from Z_{32} device.

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Chapter 8

Conclusion

RESEARCH reported in this dissertation mainly focused on memristor device modeling and memristive computing systems. At first, a brief overview of the memristor device, definition, historical background, functionality and structure was presented. Subsequently, modeling of the memristor device was discussed. Modeling evolution of the memristor was explained and each important model was briefly discussed and used to simulate an i-v behavior of the fabricated Ag/TiO_2/ITO device. Also, different state variables and window functions were discussed. Then, ultra-dense promising memristor crossbar architecture was introduced and READ and WRITE operations on each individual cells over this structure were defined. Also, the sneakpath problem over the crossbar was explained and some existing solutions to mitigate this problem were discussed. Memristor device potential applications are then defined. Different memory technologies were discussed and their important characteristics were highlighted. Also, a brief overview on the main memristive logic methods were presented, subsequently. Neuromorphic application of the memristor devices and their ability to reproduce STDP bio-inspired learning mechanism was discussed.

An accurate novel model was presented based on charge transport mechanisms in schottky barrier region. The state variable in this model was a quantity of oxygen vacancies

near schottky barrier zone. Also, the modeling was based on the dominant current mechanism existing in schottky barrier zone during the device operation. The proposed model was tested and it showed high accuracy in comparison with the experimental data of a real Ag/TiO_2/ITO fabricated device. Also, a SPICE code was developed and applied to simulate the device behavior in HSPICE software. The HSPICE simulation results for four different memristor devices confirmed the functionality of the proposed model. Also, the behavior of the proposed model was successfully tested toward different input waves with different frequencies. In addition, an error analysis was done by determining the RMS error of the simulation results and experimental data. The proposed model had 0.25 RMS error which is the lowest value in comparison with other models. This showed the proposed model has the highest accuracy to reproduce the non-linear behavior of the memristor devices.

Bio-inspired memristive neural networks were presented for pattern classification tasks by using unsupervised learning schemes. Understanding brain function as one of the most attractive topics in neuroscience can lead to finding new treatments for brain disease. Therefore, designing a bio-inspired system to model biological mechanism in brain is a crucial issue. A noble prize winner Hudgkin-Huxley neuron model which reproduces the most accurate biological behavior of the neurons in mammalian neocortex among its other peers is utilized in this bio-inspired network. Also, a memristor synapse as the closest electronic device which mimics real biological synaptic connection was utilized as the synapse in the proposed network. Therefore, this system is completely inspired by biology and due to the memristive implementation it represents a dense and nanoscale system. The memristive implementation of Hudgkin-Huxley neuron was discussed and a coupled HH neurons behavior was explained. The STDP learning mechanism was reproduced and pattern classification tasks were carried out which proved the functionality of the system. The same network was implemented by using a Morris-Lecar neuron model which is a more simplified model. A memristive implementation of Morris-Lecar neuron was explained and STDP learning mechanism was implemented by two coupled ML neurons. Also, a pattern

classification tasks were successfully carried out by the proposed network with unsupervised learning scheme.

A novel memristive analog adder was designed for Continuous Valued Number System (CVNS). Analog computation with memristor can be possible due to the analog memory property of this device. Also, CVNS scheme is a recently proposed numbering system which can provide design with less wiring complexity and it has an error correction property. The proposed analog CVNS adder was designed based on addition and modulo operations. The memristive addition circuit was developed by only three memristors and the inputs were programmed as the memristance of the input memristors in the circuit. Also, output is a memristance of the output device. This makes the proposed design an efficient computing scheme which can store the result in the same platform that perform the processing and computation. Also, since the analog computation is based on multiple levels of the memory in a single device, it can provide larger scale of computation in comparison with its digital peers. The modulo operation in this circuit was done by adding two memristor devices in parallel with the addition circuit. A mapping circuit was designed to program and map the additional memristors to the desired value which provide the right functionality for the modulo operation step. Therefore, the modulo step was comprised of two main steps: mapping and modulo operation. In addition to the adder design, this has led to development of CVNS computing scheme for memristive systems. It was explained that the environment resolution of the system is directly related to the memristance ratio of the memristor devices applied in the design. High environment resolution will result in more different levels and larger domain of numbers in the system. The proposed CVNS adder was tested for different scenarios and numbers. The addition and modulo operation was tested successfully and the modulo operation showed a negligible error which was due to the mapping circuit and non-linear behavior of memristor devices.

A memristive 4:2 compressor cell which is one of the important blocks in multipliers architecture was designed with material implication logic (IMPLY). This work presented

different IMPLY based implementations of 4:2 compressor cell. At first two XOR/MUX and full adder-based implmentations of 4:2 compressor were selected for memristive design. A memristive IMPLY-based multiplexer was designed by 4 memristors and 7 computational steps. Then, the existing optimized memristive IMPLY-based implementation of XOR and full adder was selected. Then, parallel and serial IMPLY-based scheduling for different implementations of 4:2 compressor circuit was assessed. The most efficient 4:2 compressor cell design was the parallel XOR/MUX design which requires 11 memristors and 1.8 ns delay. This implementation offers comparable speed with considerably less area in comparison with conventional CMOS-based circuits that utilized pass transistor and transmission gate logic.

A resistance-based novel memristive logic was presented. This logic is comprised of two sensing and writing circuit branches. The CMOS switch isolates two branches from each other. The sensing branch includes the input devices and based on the sensed voltage in sensing branch a CMOS switch status is defined and the writing branch is working correspondingly. Several logic gates like, OR, AND, NAND, NOR, NOT and COPY were designed with the proposed logic scheme. These gates were analyzed theoretically and simulated by Cadence to confirm their functionality. The proposed logic gates were tested successfully and provided desired output. This logic requires one computational step and it does not posses a destructive effect on the input devices during the logic operation. Also, it has a capability to provide multiple fanins and fanouts which omits the repetition in computations and reduces high volume of computations significantly. Also, a mirrored memristive corssbar array was proposed as a platform to implement this logic. This architecture was consisted of two memristor crossbar planes which is connected with CMOS switches based on the configuration in the proposed logic. The proposed platform can significantly reduces the alternate current paths as it isolates two crossbar planes from each other. Also, a larger combinational logic was implemented over the mirrored crossbar platform and it was successfully simulated by Cadence.

8.1 Future Work

In terms of future work, there are a number of areas worthy of further exploration.

Device Modeling

Although the model works properly and it can reproduce an accurate non-linear behavior of the device in high resistance state and low resistance state, the proposed model needs to be simplified for application in large-scale simulations. Also, thermionic current effect can be taken into the account for future work and the behavior of the device in different frequencies for the model should be considered in the future. Therefore, developing a new model which is a simplified version of the current model by considering the behavior of the device in different frequencies and temperature (thermionic effect) can be a potential future work.

Bio-inspired Neuromorphic Computing

The proposed biological spiking neural networks are just using the STDP learning mechanism to do the simple pattern classification tasks. Therefore, these SNNs are unable to do larger classification and image processing tasks since STDP alone is not enough to perform such tasks successfully. For this purpose a lateral inhibition should be considered as well as STDP learning mechanism to help these bio-inspired network perform larger tasks. As a future work applying a lateral inhibition to the proposed networks and testing them to do a larger image and video processing tasks can be interesting.

Memristive Analog Arithmetic

The other potential future work is to work on the memristive CVNS system. This system can have an error correction scheme because of CVNS behavior and it can be a game changer in arithmetic and computing hardware implementation. Also, memristive CVNS multiplier can be designed based on the proposed scheme. The mapping circuit can be developed to reduce the error in modulo operation of the memristive CVNS adder.

Mirrored Memristive In-Memory Computing Architecture

After presenting the mirrored memristive logic, proposing a novel mirrored crossbar com-

puting architecture is a potential future work. In this work, the memory speed, bit density and power consumption in the proposed architecture can be analyzed. Also, the READ and WRITE operation along with sneak path effects can be assessed. Then, logic functions should be implemented within the proposed architecture and the control signals of rows and columns could be defined along with the method to access individual devices within the architecture.

VITA AUCTORIS

Amirali Amirsoleimani was born in Babol, Mazandaran, Iran in 1988. He received the B.Sc. and M.Sc. degree from the Department of Electrical Engineering, Razi University, Kermanshah, Iran, in 2010 and 2013 respectively. He is currently pursuing the Ph.D.degree in Electronic Engineering with University of Windsor, Windsor, Ontario, Canada. He received IEEE Larry K. Wilson award for IEEE region 7 in 2016. He was the recipient of a best poster honorable mention award at International Joint Conference on Neural Network (IJCNN) 2017 in Alaska, USA. His research interests include Logic design, in-memory computing, RRAM, memristive circuits and VLSI circuit design.

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