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DESIGN OF A LOW POWER SWITCHED-CAPACITOR PIPELINE ANALOG-TO-DIGITAL CONVERTER

BY

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B.S., Qingdao University, China, 2003

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DISSERTATION

Submitted to the University of New Hampshire

In Partial Fulfillment of

the Requirements for the Degree of

Doctor of Philosophy

In

Electrical Engineering

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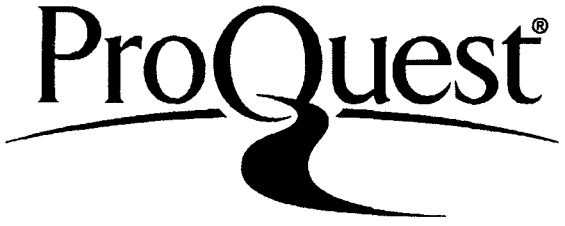

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ABSTRACT

DESIGN OF LOW POWER SWITCHED-CAPACITOR PIPELINE ANALOG-TO-DIGITAL CONVERTER

By

Gang Chen

University of New Hampshire, September, 2011

An Analog to Digital Converter (ADC) is a circuit which converts an analog signal into digital signal. Real world is analog, and the data processed by the computer or by other signal processing systems is digital. Therefore, the need for ADCs is obvious.

In this thesis, several novel designs used to improve ADCs operation speed and reduce ADC power consumption are proposed. First, a high speed switched source follower (SSF) sample and hold amplifier without feedthrough penalty is implemented and simulated. The SSF sample and hold amplifier can achieve 6 Bit resolution with sampling rate at 10Gs/s.

Second, a novel rail-to-rail time domain comparator used in successive approximation register ADC (SAR ADC) is implemented and simulated. The simulation results show that the proposed SAR ADC can only consume 1.3 μW with a 0.7 V power supply.

Finally, a prototype pipeline ADC is implemented and fabricated in an IBM 90nm CMOS process. The proposed design is validated using measurement on a fabricated silicon IC, and the proposed 10-bit ADC achieves a peak signal-to-noise-and-distortion-ratio (SNDR) of 47 dB. This SNDR translates to a figure of merit (FOM) of 2.6pJ/conversion-step with a 1.2 V power supply.

CHAPTER 1

INTRODUCTION

1.1 Background

Analog-to-digital converters (ADCs) are critical building blocks in modern signal processing and communication systems. Various kinds of ADC architectures have been implemented to meet different requirements in different applications, such as, flash ADCs, folding and interpolating ADCs, two-step ADCs, pipeline ADCs, successive- approximation-register (SAR) ADCs, delta-sigma ADCs, integrating ADCs, etc. Among all the ADC architectures, the pipelined ADC has the advantage of maintaining high accuracy at a high conversion rate with low complexity and power consumption. Therefore it is used extensively in high-quality video systems, high speed data acquisition systems, and high performance digital communication systems, where both precision and speed are critical. Some typical applications for ADCs are listed in Fig. 1.1.

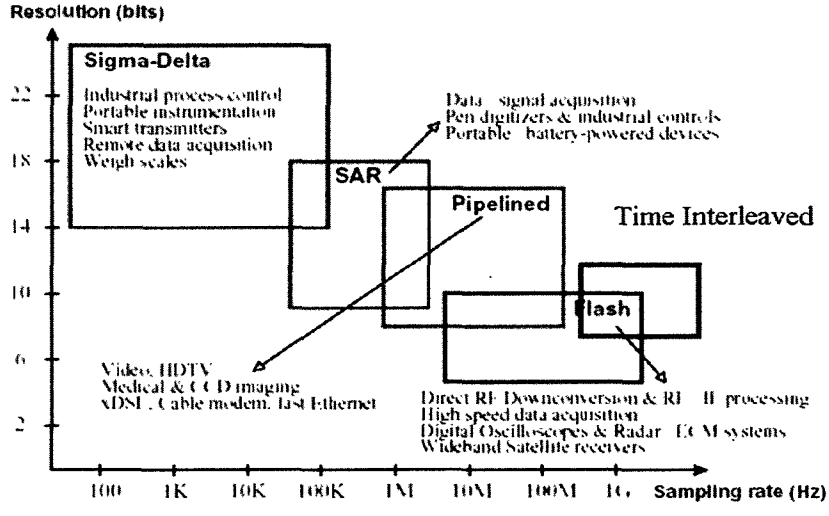

Figure 1-1 ADC Applications [1]

1.2 Motivation

The continued down-scaling of transistor dimensions in submicron CMOS technology brings much optimism to the current and future state-of-the-art digital IC systems because of the dramatically improved IC density and frequency response. As the supply voltage is also scaled down proportional to the transistor dimensions, the power dissipation of digital circuits is dramatically reduced. Pipeline ADC, however, are difficult to improve with down-scaling, because they rely on high gain operational-amplifiers (opamps) and well-matched components to produce high-precision converters. First, large open-loop opamp gain is difficult to realize without sacrificing bandwidth under the continuing trend of submicron CMOS scaling, which are coupled with lower power supply voltages. Second, there are physical limits on the component matching due to process variation, so conversion accuracy cannot be improved continually with CMOS technology scaling. Third, low-voltage analog design does not necessarily imply low power consumption. In order to compensate for the reduced signal swing and to achieve the same dynamic range, the power consumption of analog designs generally increases with reduced supply voltage.

Recently, with the demand for longer battery life in mobile systems, low power pipeline ADC is highly attractive. Therefore, in this project, our primary goal was to find a power-efficient pipeline ADC architecture to reduce the power consumption.

1.3 Existing Approaches

In this project, we will focus on the low power challenges of pipeline ADC. Proposed power-efficient pipeline ADCs techniques relevant to this thesis are:

(1) The elimination of the front-end S/H;

(2) Power scalability method;

(3) And the employment of non-opamp based amplifiers;

The front-end S/H was eliminated by relying on the redundancy of the first pipeline stage [13][14][15][16]. As a result, the impact of sampling skew appeared as an input-referred offset on the sub-ADC comparator is eliminated by the redundancy of the first pipeline stage. Therefore, high frequency inputs require a low sampling skew between the sub-ADC and multiplying digital to analog converter (MDAC), and increased conversion time (hence increased cost) must be taken into account.

Power scalability is a reconfigurable property, which allows for multiple design specifications to be met with only one low power design [17]-[20]. The reconfigurable solution enables an ADC's power to scale with different sampling rates and significantly reduces design time.

The most promising power-efficient topologies reported are those with no opamp, which is the most power hungry component in pipeline ADCs. Usually, in the pipeline ADC design, a capacitor feedback network around an opamp establishes a highly linear and precise gain but it comes at the cost of reduction of bandwidth in the closed-loop system. The unity gain frequency of the closed system is reduce $1/f$ times than that of the open loop. As a result, pipeline stages with large closed-loop gains come at the cost of reduced speed. To overcome this limitation, some researchers have investigated the method of open-loop amplifiers to reduce power consumption [21]-[23]. The penalty in an open-loop topology is reduced linearization and degraded process desensitization, of the closed loop system is sacrificed.

Therefore, open loop topology applied in pipelined ADCs requires complex nonlinear calibration [21] [22][23].

In this paper, a low-power pipeline ADC [24] is presented that has significantly lower power consumption than many previous 10 bit resolution ADCs in the mid-to-high speed. The ADC still requires power-hungry opamps, but the feedback factor f is greatly reduced. The power requirement of these opamps is much relaxed and consumes less power.

1.4 Novel Approaches

Although many techniques are already available to either improve the accuracy or reduce the power consumption, as we mentioned in Section 1.3, there is still some room for improvement in certain applications. In this work, several novel designs are proposed.

First, a high speed switched series source follower (SSF) sample and hold amplifier without feedthrough penalty is proposed. The feedthrough effect, which is a typical challenge for SSF sample and hold amplifiers, is cancelled in our new approach, and the proposed sample and hold amplifier obtains a 6dB better total harmonic distortion improvement over the traditional method.

Second, a novel rail-to-rail time domain comparator is proposed. The proposed time domain comparator does not only save power but also scales well in the deep submicron process.

Third, a novel multiplying digital to analog converter (MDAC) architecture is proposed. The proposed MDAC architecture eliminates the feedback penalty,

resulting in more than four times less power and two times less output noise than those of traditional architectures and it is used in 1.5 bits per stage pipeline ADC. Both methods are demonstrated in simulations as well as experiments in Chapter 5.

1.5 Thesis Organization

The thesis is organized as follows. The basic operations of various kinds of ADCs are described in Chapter 2. An overview of the sample and hold issues and advanced enhancement techniques is given in Chapter 3. In Chapter 4, advanced techniques for low power design are presented. In Chapter 5, a novel MDAC architecture, which can greatly reduce the power consumption as well as the output noise, is described. The conclusions and possible future work are presented in Chapter 6.

CHAPTER 2

ADC ARCHITECTURES

This chapter gives a brief introduction of the fundamentals of analog-to-digital converters (ADCs). Various ADC architectures are generally reviewed. The comparisons among different ADCs are summarized.

2.1 Analog-to-digital Conversion

An Analog-to-Digital Converter (ADC) can be described by two operations: sampling and quantization as shown in Fig.2-1.

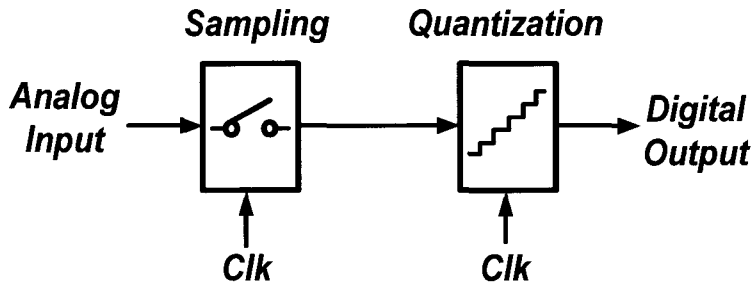

Figure 2-1 Principle of ADC Architecture

During the sampling stage, the analog input signal is converted into discrete time signals; while during the quantization stage, the discrete time signals are quantized into a set of discrete levels, which can be expressed in a digital format. Fig. 2-1 shows the transfer curve of an ideal 3-bit ADC. The X-axis and Y-axis represent the input signal V_{in} and D_{out} respectively. For a 3-bit ADC, eight levels of digital outputs are generated and each level is described by a 3-bit binary code. As shown in Fig. 2-2,

V_{FS} is the full scale analog input signal. Δ is the step size, expressed in units of LSB(least significant bit), and is calculated by:

$$1\ LSB = \Delta = \frac{V_{FS}}{2^m}, where\ m = number\ of\ bits \tag{2-1}$$

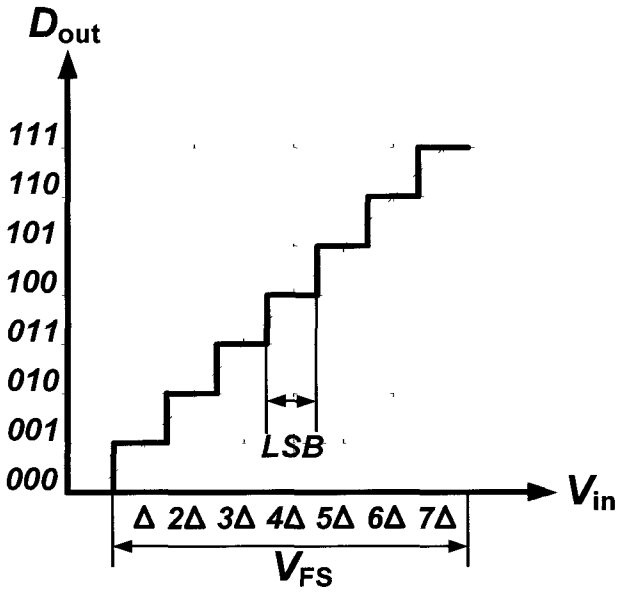

Figure 2-2 Ideal 3-bit ADC Transfer Curve

Even an ideal ADC introduces quantization errors. As shown in Fig.2-2, quantization error is defined as the difference between the discrete analog output level and the input value. Quantization error is bounded between -Δ/2 and+Δ/2 as shown in Fig.2-3. Those errors are usually modeled and studied as an additive noise source to the analog input signal; hence, the quantization error is also referred as quantization noise. Since the error is an intrinsic result of the quantization process and is independent of the particular method ADC operation, the quantization noise can be reduced only by increasing the resolution of the ADC.

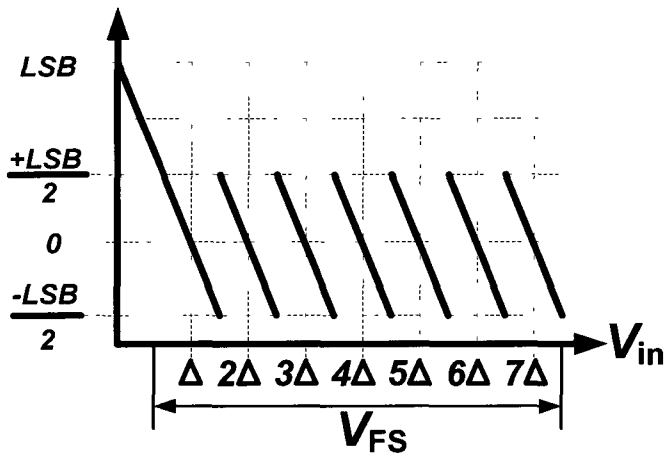

Figure 2-3 Ideal 3-bit ADC Quantization Errors

2.2 ADC Figure of Merit

ADC performance metrics, including both the static and dynamic sides of ADCs, is now presented. The specifications reviewed here are not complete, but cover most of the important performance characteristics discussed in this thesis [25] [26].

There are two sides of the ADC performance: static behavior and dynamic behavior [26]. The static behavior metrics are listed below:

- Sampling rate: how many samples the ADC can process within a given time;
- Effective Number of Bit (ENOB): the measurement of overall accuracy under real-world conditions;
- Latency: how many clock cycles between the sampling instant and the moment when the digital code is available at the ADC output;

• Differential nonlinearity (DNL): the maximum deviation of code width from Δ, i.e. 1 LSB as shown in Fig. 2-4;

• Integral nonlinearity (INL) is the maximum deviation of code transition from its ideal value as shown in Fig. 2-5;

• Offset: the amount by which the ADC transfer function is shifted from the ideal transfer function. It is often not a critical parameter, since it can be easily compensated by digital pre/post-processing.

Another group of parameters used to describe the dynamic performance of ADCs is shown below:

• Signal-to-noise ratio (SNR): the ratio of the output signal power to the total output noise power. This is usually measured with a sinusoidal input signal.

• Signal-to-noise and distortion ratio (SNDR): the ratio of the signal power to the total noise and harmonic power at the output. This is also usually measured with a sinusoidal input signal.

• Spur free dynamic range (SFDR): the ratio of the signal power to the largest harmonic noise component at the output. Also, this is usually measured with a sinusoidal input signal.

• Total harmonic distortion (THD): the ratio of the power of all the harmonics to the power of the fundamental signal component.

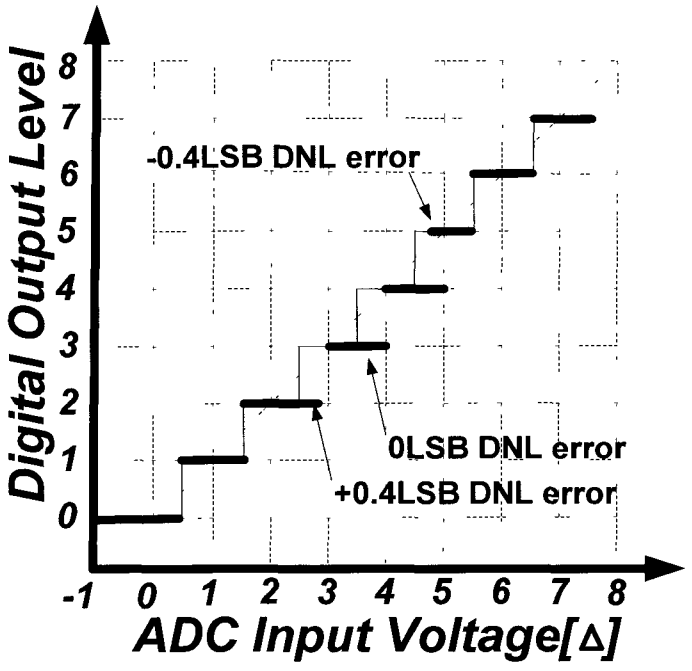

Figure 2-4 ADC Differential Nonlinearity

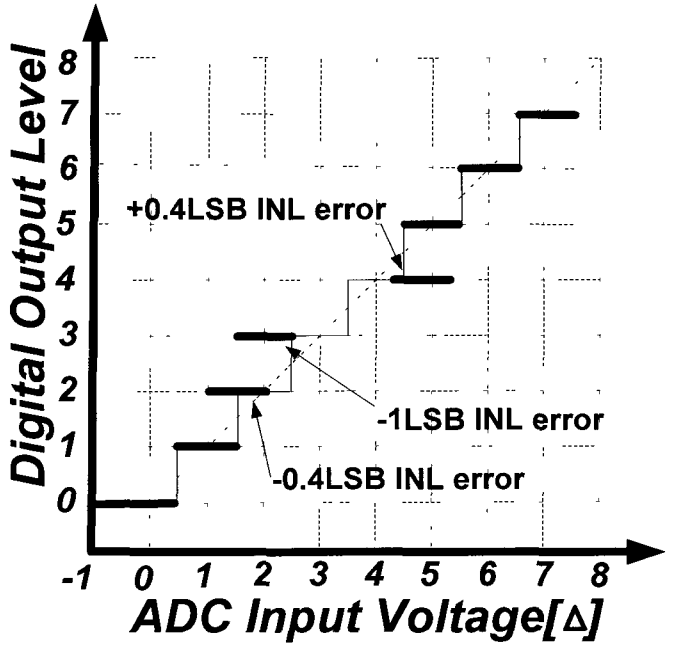

Figure 2-5 ADC Integral Nonlinearity

2.3 Converter Architectures

Based on the fundamental idea mentioned in the above section, different architectures have developed for implementing ADCs. Normally, Analog-to-Digital Converter (ADC) architectures can be separated into two main categories according to the sampling rate of the input analog signal [27]: 1) Nyquist-rate analog-to-digital converters; 2) Over-sampling analog-to-digital converters. A Nyquist-sampling ADC limits the input analog frequency range, which must be less than half of the Nyquist frequency. The sampling frequency of an over-sampling ADC can run many times higher than the input signal frequency. Within each category, there are many subsections. Table 2-1 shows the division of various types of ADC with their conversion rate and resolution.

Conversion Rate	**Nyquist-rate ADCs**	**Over-sampled ADCs**
Slow(1-100 Ks/sec)	Serial(ramp, dual-ramp) (<16 bits possible)	Very high resolution (<24 bits possible)
Medium(1-500 Ms/sec)	Successive approximation algorithm, Pipeline (<14 bit possible)	Moderate resolution (<16 bit possible)
Fast(1-10 Gs/sec)	Flash, Time- interleaved (<6 bits possible)	N/A

Table 2-1 Classification of ADC Architectures

Different ADC architectures can be adopted based on the application requirements. However, the challenges in all kinds of ADCs designs are to maximize the speed, accuracy and bandwidth while at the same time minimizing the power and chip area. In the following section, we will discuss the details of different ADCs topologies and their applications

2.3.1 Flash ADC

Flash ADCs are the fastest converters. Though flash converters are capable of very high sampling rates, the amount of associated hardware is very large when high resolution (>> 8 bits) is required. Therefore, flash ADCs are best candidate for very high speed but low resolution applications.

Full flash ADCs are the most straightforward way of flash ADC implementation as shown in Fig. 2-6 [28]-[29]. An N-bit flash ADC consists of a resistor string and 2^N-1 comparators, which evaluate the analog input and generate the digital output as a thermometer code. The codes are then converted to N-bit Binary or Gray codes. Since the converter requires only one clock cycle per conversion, the architecture is the fastest of all current structures. Because voltage references are generated through a resistor string, flash ADCs are inherently monotonic resulting in good differential linearity. However, there are several drawbacks for this architecture. Since 2^N-1 comparators are needed in an N-bit ADC, the hardware complexity increases exponentially with its resolution. This implies that power consumption and die area also increase exponentially with the resolution. The second drawback is that the ADC input needs to drive all the inputs of the front end comparators in parallel, which represents a significant nonlinear capacitance, thus increasing the total power and

aggravating the nonlinearity of the converter [30]. Third, the need for precision matching of the resistor string and the comparator's performance limits the linearity of the flash ADC.

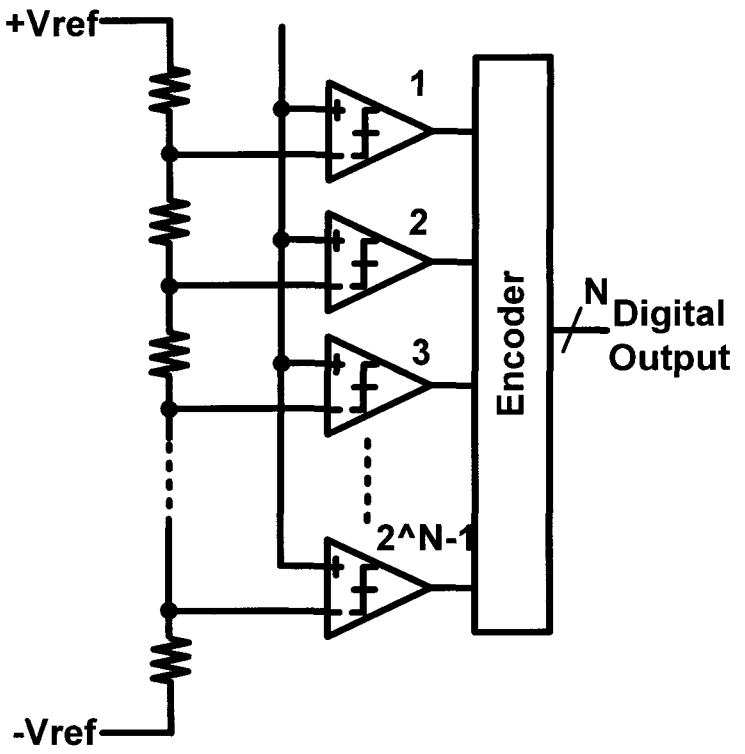

Figure 2-6 Flash ADC Architecture

Three properties of the string resistors affect their precision: (1) geometry (which is determined by shape), width, and length, resulting in local mismatch, (2) gradients of sheet resistance, and (3) variations in the polysilicon-metal contacts. Better matching can be obtained by using unit resistor elements with increased width and length. This is because most of the variation in resistance stems from perimeter irregularity due to lithography. The gradients of the sheet resistance can be cancelled to first order by cross-coupled layout [31]. Contact resistance also becomes an important factor to achieve good matching when the resistors have a low value.

There are three important degrading factors in comparator performance: (1) input offset, (2) kickback noise, and (3) sparkle (or bubble) error. The sparkle error results from the lack of a sample-and-hold amplifier with a fast-varying input signal. It can be resolved with digital correction logic [32]. Kickback noise generally corrupts sampling of the analog input signal. The general solution to suppress it is to add a preamplifier before the latched-comparator. Comparator input offsets can be reduced by numerous offset cancellation techniques [33].

2.3.2 Sigma-Delta ADC

Sigma-Delta analog-to-digital converters belong in the over-sampling converter category. Typically, the input signal is sampled many times faster than the digital output rate. Data conversion is first done at high speed with low resolution. Digital filtering is then applied to increase the overall resolution. This approach is very effective and can dramatically improve ADC performance [34] [35].

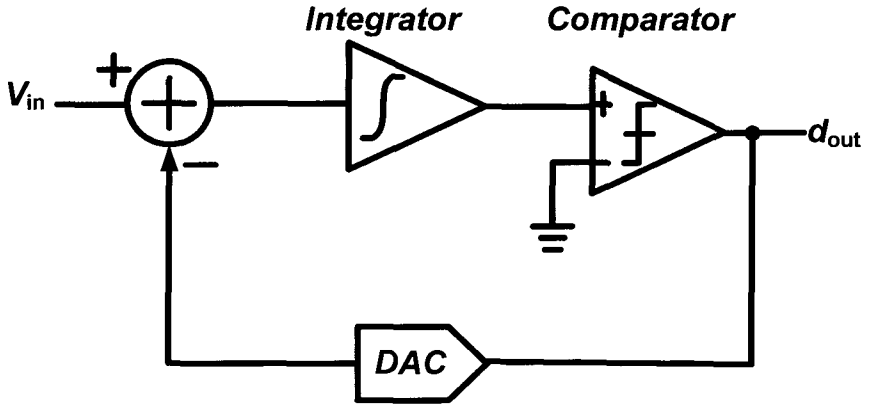

Figure 2-7 First-order Sigma-Delta Modulator

Fig. 2-7 shows the basic architecture of sigma-delta ADC. The input signal goes into the modulator through a summing node. It then goes through the integrator. The

comparator, acquiring on the output from the integrator, generates the digital output signal. The comparator output is fed back to the input summing node through a digital-to-analog converter (DAC). The feedback loop forces the average of the DACs output to be equal to the input signal. As a result, the average output of the modulator tracks the input voltage. A decimation filter is applied to the comparator's output to generate the final digital output. Since the sigma-delta ADC is an over-sampling ADC, it cannot run at very high speed. A sigma-delta ADC trades off speed for resolution. It has no stringent requirements imposed on its analog building blocks and doesn't demand strict band requirements for its analog anti-aliasing filters.

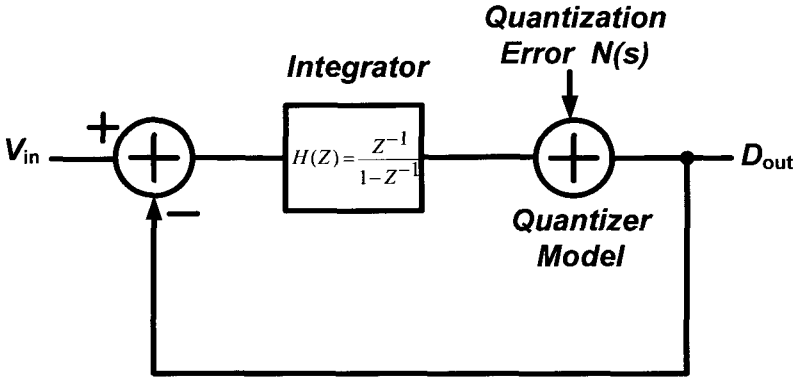

Figure 2-8 Noise shaping model of a sigma-delta modulator

The noise shaping of a sigma-delta modulator can be seen in the linear model shown in Fig.2-8. The comparator is modeled as an uncorrected additive quantization noise source, $N(s)$. The transfer function from input to output is given in equation (2-2):

$$\frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \tag{2-2}$$

which corresponds to a lowpass filter characteristic? However, the transfer function from the quantization noise to the output is given,

$$\frac{Y(z)}{N(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \tag{2-3}$$

which illustrates a highpass filter characteristic. Therefore, the sigma-delta modulator loop pushes the quantization noise into a higher frequency band, which is filtered out by the digital filter. As a result, the noise energy in the baseband decreases and the effective resolution of the converter is increased.

The higher the order of sigma-delta modulator one implements, the higher accuracy one obtains. For higher orders, however, system stability becomes an issue. Two or more cascaded stable sigma-delta modulator is possible to eliminate the stability issue [36].

2.3.3 Successive Approximation ADC (SAR ADC)

The successive approximation architecture [37] [38] has been the most popular architecture for ADC at moderate speed and resolution. It is the most power efficient ADC form and it uses the idea of the "binary search" algorithm.

Fig. 2-9 depicts the operation of a SAR ADC for an input signal V_{in}, which is sampled at the beginning of each conversion cycle. Conversion starts with the comparison between input signal V_{in} and the half-reference voltage $V_{ref}/2$, which determines the MSB of V_{in} and also determines the search region for the second MSB. In order to allow the binary search algorithm to approximate the actual V_{in}, the reference voltage used for the MSB will be divided by 2 and the result will be added

to or subtracted from the previous reference voltage, which delimits the following binary search regions. Each comparison between V_{in} and the updated reference voltage generates one bit of $V_{in}^{'}s$ digital representation. N bit SAR ADC will need N comparisons.

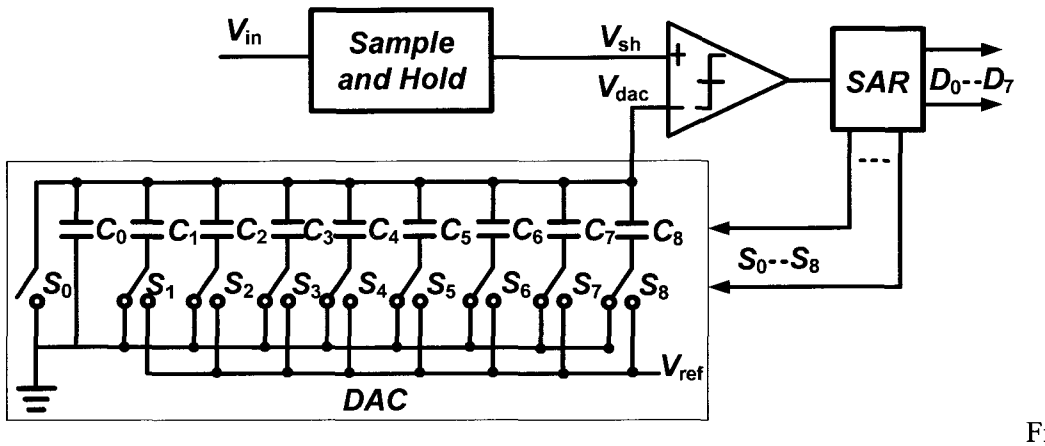

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Figure 2-9 General SAR ADC architecture

The detailed operation is described as follow.

S8 to S0 are the control signals generated by the SAR to control the switches of the DAC, and $C_i = 2^{i-1}C_0$, $i \in \{1,...,8\}$. The power consumption from the applied reference voltage source can be calculated according to equation (2-4)

$$PV_{REF}(V_{in}) = \frac{V_{REF}}{T}\sum_{i=1}^{9} Q_i \tag{2-4}$$

Where Q_i is the charge stored on the capacitor C_i. In the first cycle, all capacitors of the DAC are reset. There is no charge transferred from V_{REF} to the DAC; thus $Q_1 = 0$. During the second cycle, C_8 is connected to V_{REF} while the connections of the rest of the capacitors are not changed. As a result

$$V_{dac8} = V_{REF}\frac{C_8}{C_{DAC}}$$
$$Q_2 = C_2[(V_{REF} - V_{dac8})] \tag{2-5}$$

Where C_{DAC} is the total capacitance of the DAC array. In the third cycle, C_7 connects to V_{REF} and C_8 connects to V_{REF}. The output of the DAC at the end of this cycle is

$$V_{dac7} = V_{REF}\frac{C_7 + D_8 C_8}{C_{DAC}} \tag{2-6}$$

The total charge supplied by V_{REF} in the third cycle is written as

$$Q_3 = C_7[(V_{REF} - V_{dac7}) - (0 - V_{dac8})] + D_8 C_8[(V_{REF} - V_{dac7}) - (V_{REF} - V_{dac8})] \tag{2-7}$$

The general expression is:

$$V_{daci} = V_{REF}\frac{C_i + \sum_{j=i+1}^{8} D_j C_j}{C_{DAC}}$$
$$Q_i = C_{10-i}[(V_{REF} - V_{dac(10-i)} + V_{dac(11-i)}] + \sum_{j=11-i}^{8} D_j C_j (V_{dac(11-i)} - V_{dac(10-i)}),\ i \in \{3,...,9\} \tag{2-8}$$

As shown in Fig. 2-9, the largest power consumption component is the analog comparator, which makes the SAR ADC very power efficient. SAR ADCs cannot achieve high resolution (greater than 12 bits) because of capacitor mismatching. But with a digital calibration technique, SAR ADCs can achieve 16 bits resolution or higher [39]. Also SAR ADCs are suitable for ultra low power design with medium resolution [40]. With power supply voltage reduction, the time-domain comparator maybe designed to further decrease power consumption. Today, because of

improvement of fabrication process control, SAR ADC is made for high speed (up to GHz sampling rate) with medium resolution [41].

2.3.4 Pipeline ADC

A pipeline ADC architecture [42] [43], as shown in Fig. 2-10 is made of several stages working in conjunction with each other and in series with each other. Each stage has much fewer number of bits compared to the overall ADC resolution. When the first stage acquires the input signal, it digitalizes the input and also generates the residue. The second stage acquires the residue as its input signal to process it, and so forth. The various stages operate on the input signal as a shift register.

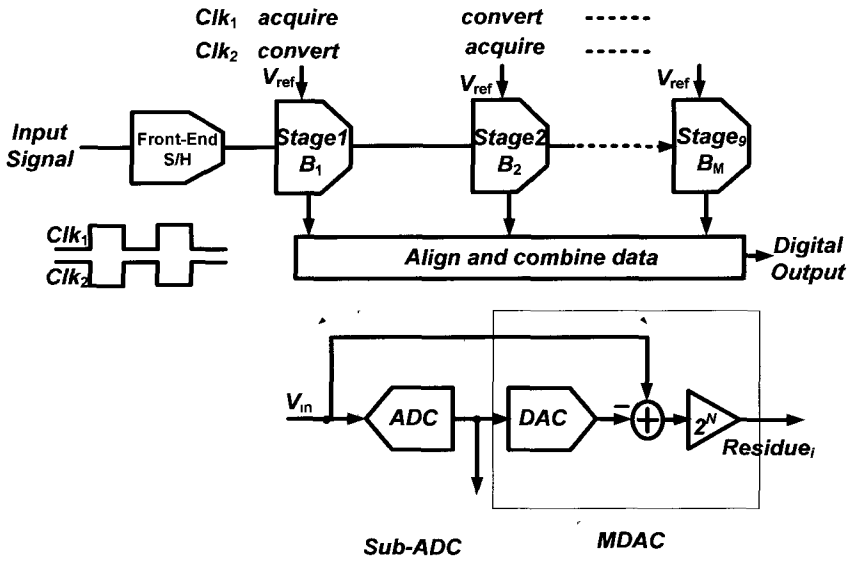


Figure 2-10 Pipeline ADC

Each stage has a resolution of $B_i + r_i$ bits, where B_i means the effective stage resolution and r_i stands for the stage redundancy which is used for a comparator offset correction. The resolution of each stage can be the same or can even differ from stage

to stage. Usually, the last stage consists only of a sub-quantizer that does not usually employ redundancy. Assume that k_j is the number that used for B_j bits, the total resolution N of a pipeline ADC with m different stage resolutions B_j is given by

$$N = \sum_{j=1}^{m} k_j B_j + B_k \tag{2-9}$$

where B_k is the resolution of the last stage. As shown in Fig. 2-10, each stage comprises a low-resolution sub-analog-to-digital converter (sub-ADC). The sub-DAC and gain stage are combined to implement the multiplying digital-to-analog converter (MDAC) that performs a sample and- hold (S/H) operation, coarse D/A conversion, subtraction, and amplification.

In operation, each stage performs an A/D conversion to generate B_i effective bits with r_i bit redundancy, converts the digital output back to analog and subtracts it from the sampled and held analog input. Finally, the output residue is amplified with a gain of

$$G_i = 2^{B_i+1-r_i} \tag{2-10}$$

The residue is the input signal of the next stage. The stages operate concurrently; that is, at any time, the first stage operates on the most sample while all other stages operate on residues from previous samples.

The digital outputs of each stage are delayed so that their values are synchronized. The resulting total C bits are forced to the correction circuitry

$$C = \sum_{i=1}^{k} (B_i + r_i) \tag{2-11}$$

The analog transfer function of the pipeline stage follows the equation

$$V_{out,i} = G_i V_{in,i} + D_i V_{ref} \tag{2-12}$$

where D_i is 2^i, whose value is dependent on the output of the sub-ADC.

As mentioned above, the redundancy is applied in each stage for a comparator offset correction algorithm. Adding a redundant bit means increasing the stage resolution by one bit minus one quantization level.

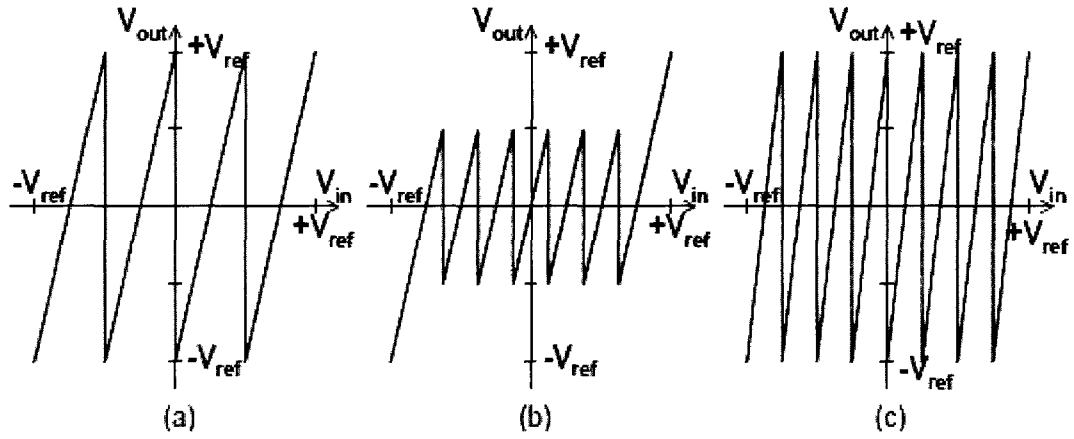


Figure 2-11 Transfer functions of (a) 2-bit ($B_i = 2,\ r = 0$), (b) 2.5-bit ($B_i = 2,\ r = 1$), and 3-bit ($B_i = 3,\ r = 0$)

In Fig. 2-11, a 2-bit (B_i = 2, r = 0) and a 3-bit (B_i = 3, r = 0) stage without redundancy are compared to that of a 2.5-bit (B_i = 2, r = 1) stage. Comparing Fig. 2-11(a) and Fig. 2-11(b), by introducing 1 bit redundancy, the number of quantization levels is increased from four to six while the gain is still kept at four. Moreover,

compared to the 3-bit stage in Fig. 2-11(c), there is one fewer quantization level in the 2.5-bit stage but the distance between two levels is equal. The locations of these levels are shifted by $V_{ref}/8$ and the gain is four instead of eight. As a result, the output of a 2.5-bit stage stays between $\pm V_{ref}/2$ for input voltages of $\pm 7V_{ref}/8$. As shown in Fig. 2-12, the transfer functions of 2-bit and 2.5-bit stages are plotted with the same quantization errors. The comparators with threshold voltages are applied to implement the coarse A/D conversion. The threshold voltage is equal to the quantization step locations in Fig. 2-11. Therefore, any offset V_{OS} is translated into a quantization error and appears as a shift in the location of the quantization step in Fig.2-12.

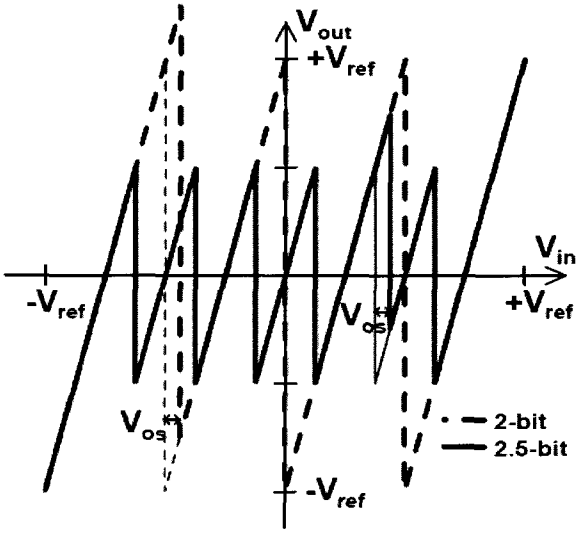


Figure 2-12 Effect of ADC offset voltages in 2-bit and 2.5-bit stages

In Fig. 2-12, as seen from the dashed line of the 2-bit stage, the comparator offset causes an overflow of the stage output voltage saturating the next stage and resulting in an erroneous quantization. However, in the 2.5-bit stage, marked with the solid line,

an equal comparator offset results in a stage output greater than $V_{ref}/2$ but smaller than V_{ref}. Thus, no information is lost and a correct quantization result can be reconstructed using the digital output of the next stage.

In general, the amount of offset voltage that can be tolerated for stage i is given by

$$V_{os,t} = \pm \frac{r_i}{2^{B_i+r_i}} V_{ref} \tag{2-13}$$

The primary advantage of the pipeline ADC architecture is its high throughput rate made possible by the concurrent operation of its stages. Its accuracy increases by cascading more stages, but without sacrificing the speed. However the front-end input sampling rate and accuracy of the interstage gain amplifier are the limitation factors of the ADC conversion rate. Compared with those of flash ADCs, chip area and power dissipation are dramatically reduced for a pipeline ADC. This is because the number of components increases linearly rather than exponentially with N. Chip area and power dissipation can be further reduced by stage downscaling [44]. However, interstage signal transfer and sub-DAC linearity decide the overall ADC performance. Recently, various correction and calibration techniques have been published to obtain high resolution and reduce the power consumption [43] [45]. A mutli-channel time-interleaved architecture is widely used to further increase the conversion speed [46] [47].

2.3.5 Time-interleaved ADC

Fig. 2-13 shows the block diagram of a time-interleaved architecture in which four ADCs are used in parallel to achieve four times the sampling rate of a single

converter. This is known as time-interleaved architecture [46] [47][48], since the operation of the ADC channels is interleaved in such a way that each channel processes every fourth sample. The digital outputs of the channels are combined with a multiplexer to a single full-speed bit stream. As shown in Fig. 2-11, the input is sampled by a front-end sample-and-hold amplifier running at full clock f_s. The sampled signal is fed into one of the sub-DACs in the correct order driven by four local clocks f_{s1} to f_{s4}. Since four channels are used in parallel, each of the ADCs runs at a lower frequency $f_s/4$, which give ADCs more time to finish the conversion.

With this approach, the conversion speed for each ADC can be lowered and sub-ADC design requirements are relaxed. However, at such a high conversion rate, the sample-and-hold amplifier must be carefully designed. Time-interleaved ADCs suffer from gain mismatch, offset and timing mismatch errors between the individual sub-ADCs, which need digital calibration [49][50][51].

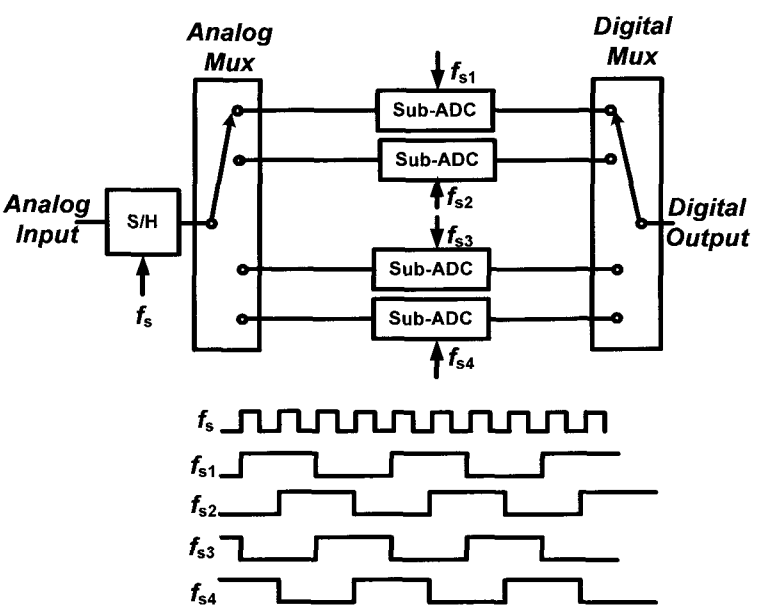


Figure 2-13 Four Channel Time-Interleaved ADC with Its Clock Signal

CHAPTER 3

SAMPLE AND HOLD PROCESS ANALYSIS

This chapter gives a brief description of the sample and hold (S/H) architectures. The closed loop and open loop S/H architectures are introduced. The differences between the closed loop and the open loop architectures are highlighted in the design of S/H circuits. This leads to very different architectural solutions in high-performance designs.

3.1 Introduction

Sample and hold amplifiers are an integral part of most high-performance ADCs. It is challenging to generate low jitter, low skew, and high voltage swing clock signals for high speed ADCs if the jitter is already comparable to the clock period. S/H amplifiers sample the input value and keep it constant for the next stage's operation where clock jitter effects can be removed. As shown in Fig. 3-1, a smaller S/H jitter will greatly improve the ADC performance [52].

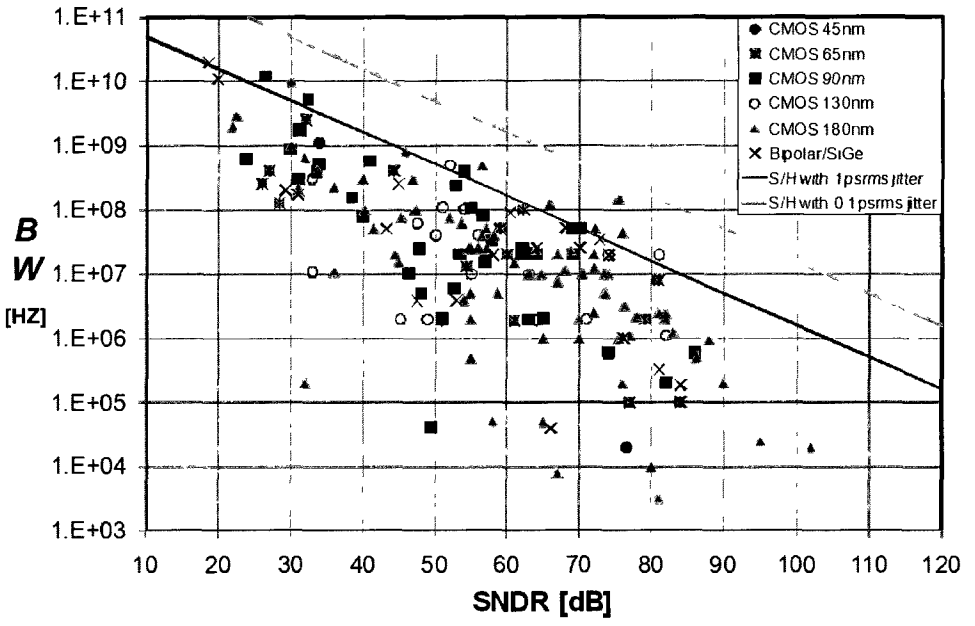


Figure 3-1 State of Art of ADCs [52]

As we mentioned above, a S/H amplifier can minimize the clock jitter's effect on the sampling signal. Hence, before we discuss how to design the sample and hold amplifier, we will take a look at how clock jitter affects the sampled signal.

3.2 Clock Jitter Effect

According to the Nyquist-Shannon sampling theory, the sampled signal can be flawlessly recovered if the original signal is sampled uniformly in time at a rate greater than twice the bandwidth of the signal. However, the sampling clock is not pure and is subject to timing errors. These timing errors affect the regularity of the clock pulse and correctness of the sample data. Fig. 3-2 shows the clock jitter effect on the sampling system.

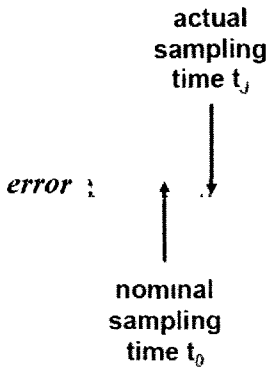


Figure 3-2 Jitter Error during Sampling

As show in Fig.3-2, sampling jitter adds an error voltage to the output. The error voltage is proportional to the product of $(t_J - t_0)$ as shown in Fig.3-2 and the derivative of the input signal at the sampling instant. The error voltage is defined in Equation (3-1).

$$e = x'(t_0)(t_J - t_0) \tag{3-1}$$

Note that jitter doesn't matter when sampling a DC signal ($x'(t_0)$ =0).

To analyze the consequences of jitter's effect on the sampled signal, we consider a continuous-time signal $x(t) = A\sin(2*\pi*f_x*t)$. The derivative of the signal is $x'(t) = A*2*\pi*f_x*\cos(2*\pi*f_x*t)$; therefore $\left|x'(t)\right|_{\max} <= A*2*\pi*f_x$. The error voltage should be defined by Equation (3-2):

$$e_t \le \left|x'(t_0)\right| d_t = \left|2\pi f_x A\right| d_t = 2\pi f_x d_t \left|A\right| \tag{3-2}$$

For the worst case, A equals $A_{FS}/2$ (A_{FS} is the full-scale input amplitude) and $f_x = f_s/2$ (f_s is the frequency of sampling clock).

To maintain ADC accuracy, the jitter-induced error voltage should be much smaller than half LSB

$$|e_t| << \Delta/2 = A_{FS}/2^{B+1} \tag{3-3}$$

where B is the number of bits and A_{FS} is the full input swing.

Taking all in consideration, we get the desired constraint on the peak jitter as,

$$d_t << \frac{1}{2^B * \pi * f_s} \tag{3-4}$$

Table.3-1 summarizes the jitter requirement according to ADC resolution and sampling rate.

N.O. of Bits	Sampling Rate	Jitter d_t upper band
16	10 MHz	0.5ps
12	100 MHz	0.8ps
10	200 MHz	1.6ps
8	1000 MHz	1.2ps

Table 3-1 Jitter Requirement According to ADC Resolution and Sampling Rate

From Table 3-1, we can see that the worst case jitter requirement looks rather stringent. Let's calculate the mean squared sampling error (variance), may be

estimated for a sinusoidal signal $x(t) = A\sin(2*\pi*f_x*t)$. As noted, $x'(t) = 2*\pi*f*A*\cos(2*\pi*f_x*t)$ and $E\left\{\left|x'(t)\right|^2\right\} = 2*\pi^2*f_x^2*A^2$. If the sample clock jitter has variance $E\left\{(t_i - t_0)^2\right\} = \tau^2$ and $x'(t)$ and the jitter are independent, we get,

$$E\left\{\left[x'(t)(t_j - t_0)\right]^2\right\} = E\left\{\left[x'(t)\right]^2\right\} E\left\{\left[(t_j - t_0)\right]^2\right\} \tag{3-5}$$

Therefore, the sampling jitter error power is given by equation (3-6),

$$E\left(e^2\right) = 2*\pi^2*f_x^2*A^2*\tau^2 \tag{3-6}$$

If the jitter is uncorrelated from sample to sample, the jitter noise is white. The relationship between sampling error power and SNR is given by equation (3-7)

$$\begin{aligned}\text{Dynamic Range}(DR)_{jitter} &= \frac{A^2/2}{2*\pi*f_x^2*A^2*\tau^2} \\ &= -20\log_{10}(1/(2*\pi*f_x*\tau))dB\end{aligned} \tag{3-7}$$

Fig.3-3. shows the SNR performance due to sampling clock jitter.

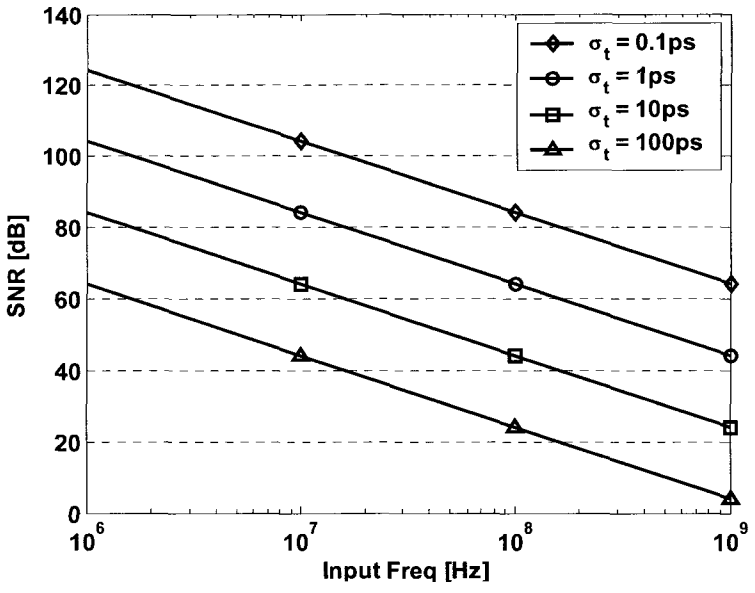


Figure 3-3 SNR Performance Due to Sampling Clock Jitter

3.3 Sample and Hold Amplifier Architecture

In general, an S/H amplifier can either adopt a closed loop or an open loop architecture. The closed loop architecture can achieve a higher resolution due to its bottom-plate sampling technique. However, it suffers from a relatively low sampling frequency limit because of the feedback loop. The open loop architecture is a better choice for high speed ADC designs although its resolution is limited. The performance comparisons between open loop architectures and closed loop architectures are shown in Table 3-2.

Category		Advantage	Disadvantage
Closed Loop Architecture		High resolution	Low bandwidth Low speed
Open Loop Architecture	Switched series Transistor approach	High speed Wide bandwidth	Non-linearity
	Switched source Follower approach	Very high speed Wide bandwidth Better linearity	Larger area Larger power

Table.3-2 Sample and Hold Amplifier Architecture

3.4 Open Loop S/H Architecture

The switched series transistor approach and the switched source follower approach are two main choices in the open loop architecture class.

3.4.1 Switched Series Transistor Architecture

The basic concept of a switched series transistor architecture [53] [54] [55] [56] is just a MOS switch with a capacitor as shown in Fig. 3-4

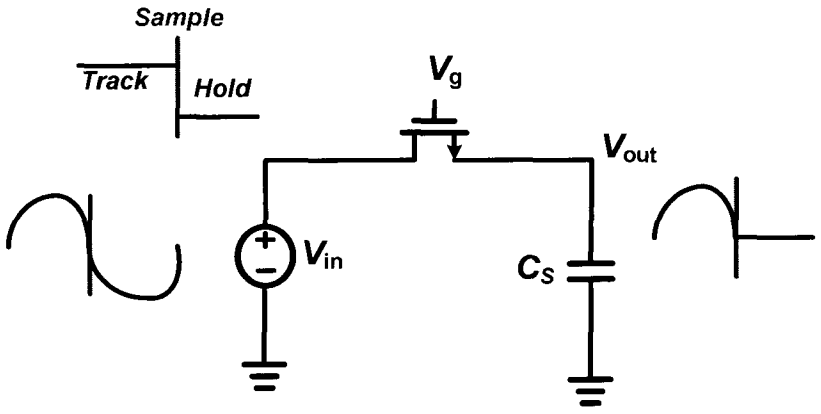


Figure 3-4 A simple Switched Series Transistor S/H Circuit

During the sampling phase of the clock, V_g is high and the voltage on the sampling capacitor C_S tracks the input voltage through the MOS transistor switch. Then, in the next clock phase when the clock V_g goes low, the transistor turns off and the input voltage is held on the capacitor C_S for further processing. The ideal sample and hold signal is shown in Fig. 3-5.

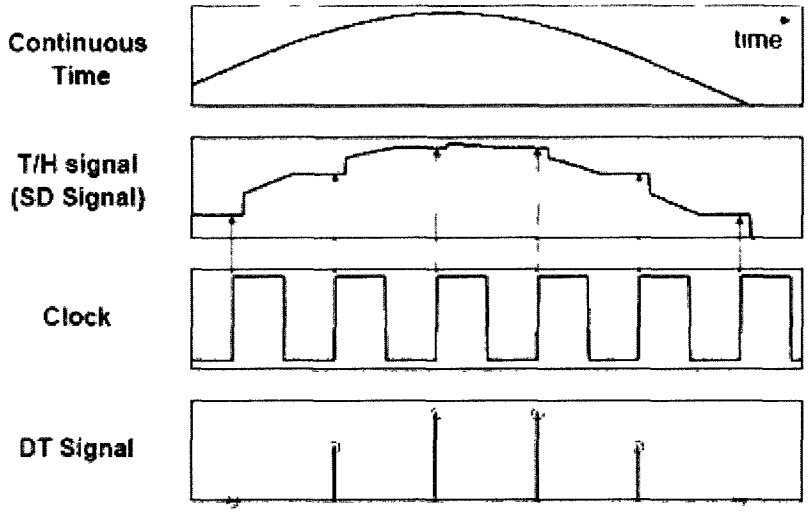


Figure 3-5 Ideal S/H Sampling

In this simple MOS S/H circuit, there are a number of non-idealities causing output errors, and the switched series transistor architecture is inherently slow due to the large series resistance of the switch [54]. The non-idealities include finite bandwidth in the sample mode, the signal dependent charge injection from the MOS transistor, clock feedthrough, etc.

3.4.1.1 Finite Bandwidth

When the MOS switch in Fig. 3-4 is closed, the switch on-resistance R of switch S1 turns the sampling network into a lowpass filter with the risetime = RC = τ. Assume V_{in} is constant during the sampling period and C is initially discharged. The output is given by Equation (3-8)

$$V_{out}(t) = V_{in}(1 - e^{-t/\tau}) \tag{3-8}$$

To get the value of time constant τ, we need to find the switch on-resistance. When the switch S1 is closed, the MOS transistor works in the triode region, and we get Equation (3-9).

$$I_{D(triode)} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS} \tag{3-9}$$

where V_{GS} is the gate-source voltage, μ is the electron mobility, C_{ox} is the oxide capacitance, W and L are the width and length of the transistor and V_{th} is the threshold voltage. This equation is only valid when V_{GS} is equal to or bigger than V_{th}. If the gate-source voltage decreases below V_{th}, the resistance increases abruptly as shown in Fig.3-6.

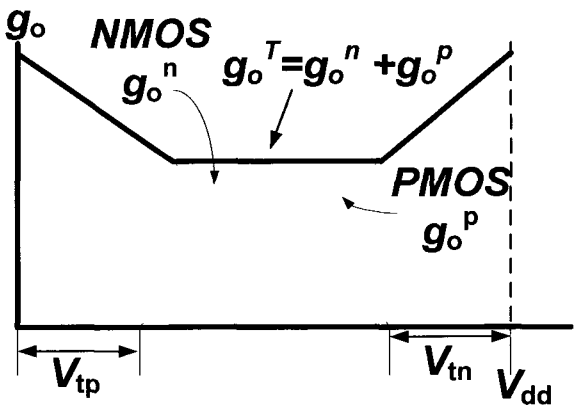


Figure 3-6 CMOS Transmission Gate Switch On-resistance

The switch on-resistance can be given by Equation (3-10)

$$R_{ON} \cong \left.\frac{dV_{DS}}{dI_{D(triode)}}\right|_{(V_{DS}\to 0)} \tag{3-10}$$

Combining Equations (3-9) and (3-10), we get the switch on-resistance:

$$R_{ON} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD}-V_{in}-V_{th})} \tag{3-11}$$

As we know from Equation (3-8), if there is an input signal V_{in}, the output signal V_{out} rises in an exponential way. Within finite time, V_{out} will not reach the value of V_{in}. If we can choose the R_{ON} and C to keep the voltage error between V_{in} and V_{out} much less than one LSB (1Δ), the sample and hold circuit can meet the system requirements. To make the voltage error between V_{in} and V_{out} is much less than one LSB (1Δ) In the worst case, $V_{in} = V_{FS}$. We must observe the constraint as follow.

$$V_{in} - V_{out}(t = \frac{1}{2f_s}) << \Delta \tag{3-12}$$

Combined Equation (3-8) and (3-12), we get,

$$V_{in} e^{-1/2f_s} << \Delta \tag{3-13}$$

To make sure the voltage error is much less than one LSB ($1\,\Delta$) in the worst case, $V_{in} = V_{FS}$, the constraints on the S/H time constant and switch on-resistance are described by Equation (3-14)

$$\begin{aligned} \tau &<< \frac{1}{2f_s} \frac{1}{\ln(2^B - 1)} \\ R &<< \frac{1}{2Cf_s} \frac{1}{\ln(2^B - 1)} \end{aligned} \tag{3-14}$$

If we assume $C = 1\,pF$, Table 3-3 summarizes the switch on-resistance based on ADC resolution and sampling rate.

N.O. of Bits	**Sampling Rate**	R_{on} **(ohm)**
16	10 MHz	4500
12	100 MHz	601
10	200 MHz	360
8	1000 MHz	90

Table.3-3 Switch On-Resistance Requirement

However, the above derivation is calculated based on a constant switch on-resistance. According to Equation (3-10), the switch on-resistance is voltage dependent as shown in Fig. 3-6, which causes nonlinear distortion.

To alleviate the problem with poor conduction and varying on-resistance, the gate-voltage bootstrapping technique has been proposed [57] [58] [59]. These switches are in principle realized with a single pass transistor and additional devices for generation of gate-source voltages for the pass transistor. As shown in Fig. 3-7 and Fig. 3-8, when clock phase phi2 is high, the gate is connected to V_{SS} and the transistor is cut off. The boost capacitor C_{boost} will be charged to V_{DD}. The big difference from regular analog switches is present when clock phase phi1 is high, and the gate to channel voltage is kept constant at V_{DD}. This is done by connecting a constant offset voltage between the gate and source terminals of the main switch. This voltage can be obtained by the use of a capacitor pre-charged in the phi2 phase. Since the absolute voltage at the gate terminal exceeds the supply voltage as shown in Fig.3-9, these switches have to be designed carefully so that they don't violate any reliability constraints [58][59].

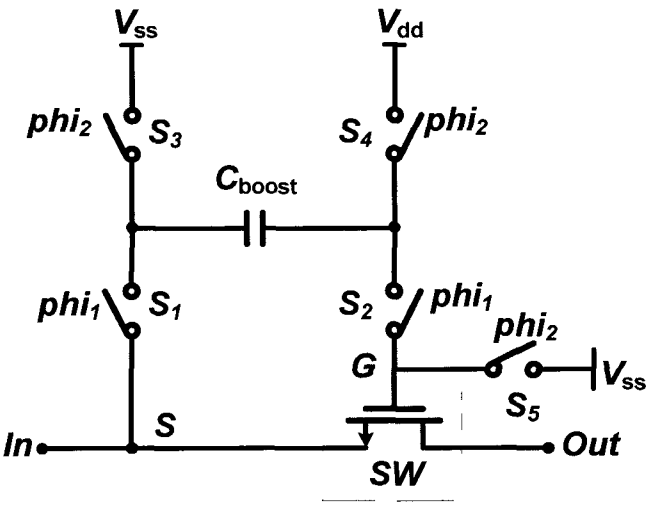


Figure 3-7 Booststrapped Switch Technique Implemented Topology

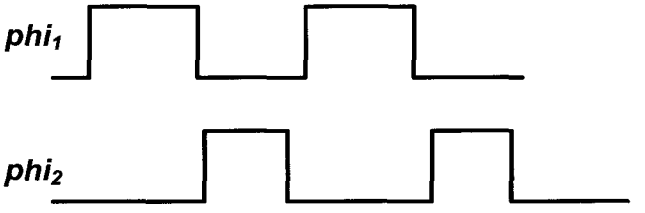


Figure 3-8 Control Signals for Booststrapped Switch

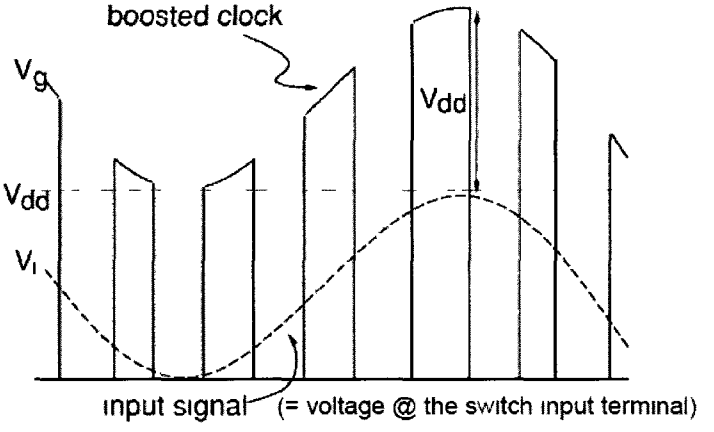


Figure 3-9 Constant V_{GS} Sampling

3.4.1.2 Charge Injection

Considering the sampling circuit of Fig. 3-4, when the switch is closed, a channel between drain and source of the MOSFET must exist at the oxide-silicon interface as shown in Fig. 3-10.

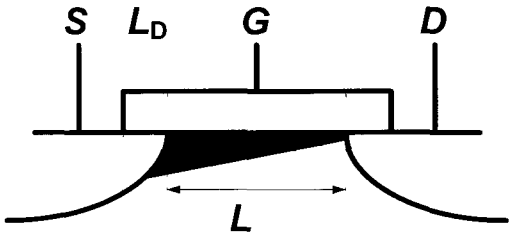


Figure 3-10 MOFET Operation in Triode Region Cross Section View

Assume that $V_{in} \approx V_{out}$. The total charge in the channel equals

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}) \tag{3-15}$$

where L denotes the effective channel length, W is the effective channel width and C_{ox} is the gate oxide capacitance per unit area. When the switch turns off, Q_{ch} exits through the source and drain terminals, a phenomenon called "channel charge injection" as shown in Fig.3-11.

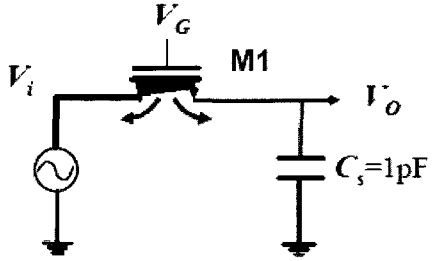


Figure 3-11 Charge Injection

Assume that the charge stored in the channel is ejected equally to both sides. The charge injected to the left side of Fig. 3-11 is absorbed by the input source, creating no error. On the other hand, the charge injected to the right side is deposited on sampling capacitor C_S, causing an error in the voltage stored on the capacitor as shown in Fig.3-12. For example, if half of Q_{ch} is injected onto C_S, the resulting error equals

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_S} \tag{3-16}$$

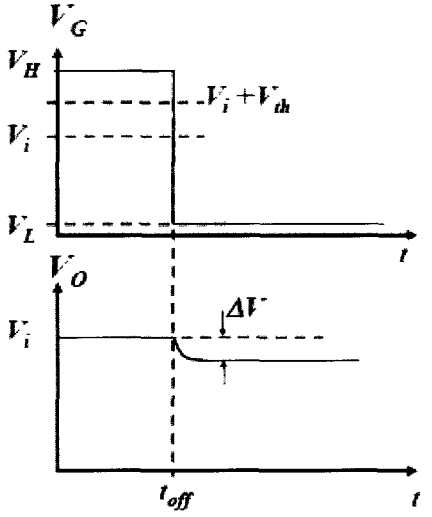


Figure 3-12 Error Voltage Caused by Charge Injection

In the previous analysis, we assumed that half of the channel charge is injected onto C_S. In reality, the percentage of charge that is injected into source and drain terminals is a relatively complex function of various parameters [60] [61]. In many cases, some parameters, such as the clock transition time etc., are poorly controlled. Also, most circuit simulation programs model charge injection quite well. As a worst-

case estimate, we can assume that the entire channel charge is deposited onto sampling capacitor C_S and the sampled output is given by

$$\begin{aligned} V_{out} &= V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_S} \\ &= V_{in}(1 + \frac{WLC_{ox}}{C_S}) - \frac{WLC_{ox}}{C_S}(V_{DD} - V_{TH}) \end{aligned} \tag{3-17}$$

According to Equation (3-17), the output signal suffers from two effects, a non-unity gain equal to $(1 + WLC_{ox} / C_S)$, and a constant DC offset voltage equals to $-WLC_{ox}(V_{DD} - V_{TH}) / C_S$. In other words, since we have assumed that channel charge is a linear function of the input voltage, the circuit suffers from only gain error and dc offset, as shown in Fig. 3-13

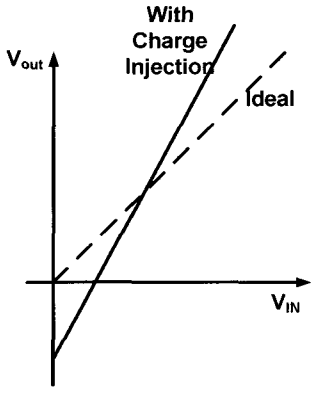


Figure 3-13 Input/output Characteristic Comparison

In the foregoing discussion, we assumed that V_{TH} is constant. However, because of the NMOS switch's body effect, the threshold voltage is varied with voltage V_{SB}.

$$V_{TH} = V_{TH0} + \gamma\sqrt{2\Phi_B + V_{in}} - \gamma\sqrt{2\Phi_B} \tag{3-18}$$

where V_{tho} is the gate voltage, γ is body effect coefficient and V_{SB} is source-bulk voltage.

Taking the body effect into account, we have,

$$V_{out} = V_{in} - \frac{WLC_{ox}}{C_S}(V_{DD} - V_{in} - V_{TH0} - \gamma\sqrt{2\Phi_B + V_{in}} + \gamma\sqrt{2\Phi_B}) \qquad (3\text{-}19)$$

We can see that the variation in V_{TH} introduces the nonlinearity for the circuit.

In summary, charge injection contributes three types of errors in MOS sampling circuits: gain error, dc offsets and nonlinearity. Actually, there is a tradeoff between sampling circuit speed and precision. Representing the speed by a simple time constant τ and precision by the error ΔV due to charge injection, we define a figure of merit as

$$\begin{aligned} F &= (\tau * \Delta V)^{-1}, \ where \\ \tau &= R_{ON} * C_S \\ &= \frac{1}{\mu_n C_{ox}(W/L)(V_{DD} - V_{in} - V_{TH})} \quad and \\ \Delta V &= \frac{WLC_{ox}}{2}(V_{DD} - V_{in} - V_{TH}) \quad and \\ F &= \frac{\mu}{L^2} \end{aligned} \qquad (3\text{-}20)$$

Therefore, reducing the switch size will increase the time constant τ, increasing the distortion, which is not a viable solution. To get a small τ and ΔV, we need to use a minimum channel length. For a given technology, $\tau * \Delta V$ is constant.

In the Equation (3-15), we can see that the charge injection is related to the input signal voltage, which will cause further distortion. Several methods, including

dummy switch architecture, bottom plate, and differential operation, are proposed to cancel the effect of charge injection [62].

The dummy switch architecture is depicted in Fig. 3-14. M_1 is the main switch and M_2 is the dummy switch. The dummy switch has the same length as the main switch but only half the width. Also, the source and drain are connected together to the output. When the main clock V_G goes low and the clock of dummy switch V_{GB} goes high, the dummy switch acquires same amount of channel charge that the main switch needs to lose. But the method only works if exactly half of the charge is transferred to M_2 and requires good matching between the clock in fall time and rise time.

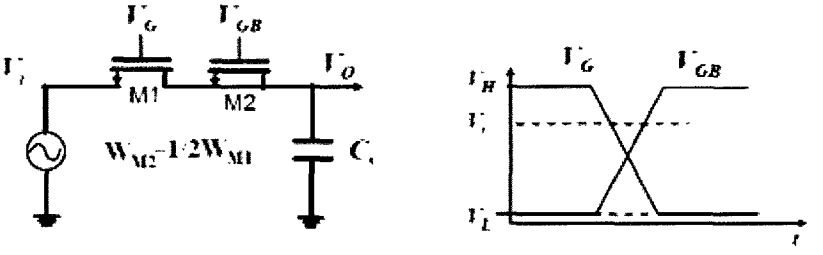


Figure 3-14 Dummy Switches [62]

To guarantee that half of the injected charge goes to each side, we need to create the same environment on both sides. As shown in Fig. 3-15, a capacitor in value equal to the sampling capacitor is added to the other side of the switch, and a fixed resistor which emulates resistance of next circuit is added. The two switches now face almost the same environment. However, the added capacitor and resistor will degrade the sampling bandwidth.

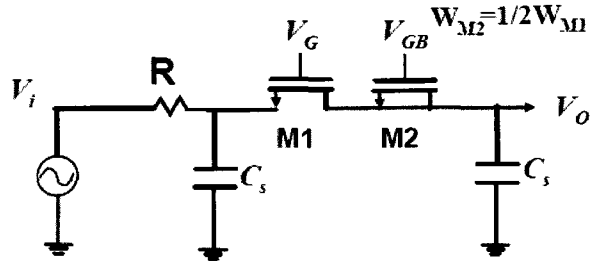


Figure 3-15 Dummy Switches with Matched Environment.

Another widely used technique to cancel the charge injection effect is called bottom-plate sampling, which is shown in Fig.3-16.

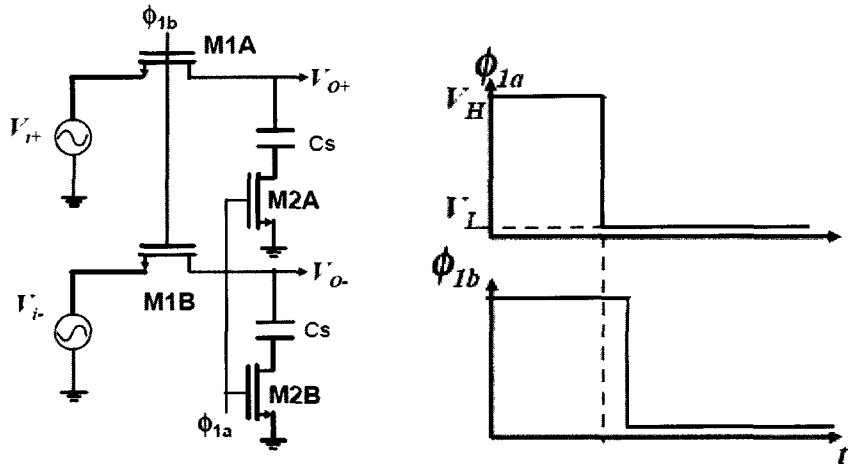


Figure 3-16 Bottom Plate Sampling

The bottom plate sampling circuit is controlled by the clocks ϕ_{1a} and ϕ_{1b}. ϕ_{1a} and ϕ_{1b} have the same frequency, but ϕ_{1a} switches to low earlier than ϕ_{1b}. When both ϕ_{1a} and ϕ_{1b} are high, the input signal is sampled on the sampling capacitor C_S. When ϕ_{1a} is low, switch M_{2A} is opened slightly earlier than M_{1A}. If switch M_{2A} is opened, injected charge caused by opening M_{2A} is dumped into the sampling capacitor C_S. But

the charge injection caused by M_{2A} is constant and independent of the input voltage, and it can be eliminated by differential operation. When ϕ_{1b} is low and switch M_{1A} is opened, but bottom plate of C_S is also opened, there is no path existing for charge injected onto C_S caused by opening switch M_{1A}. Moreover, switch M_{1A} can be further boost strapped. However, because there is one more switch serially connected in the signal path, the tracking bandwidth is reduced and the signal swing at the bottom of the sampling capacitor is not entirely zero. This circuit needs careful design and simulation to guarantee that the bottom plate sampling circuit meets the overall sampling circuit requirement.

3.4.1.3 Clock Feedthrough

In addition to channel charge injection, a MOS switch couples the clock transition signal to the sampling capacitor through its gate-source or gate-source overlap capacitance C_{OL}. As shown in Fig. 3-17, the clock feedthrough will introduce a voltage error in the sampled output voltage ΔV. If we assume the overlap capacitance is constant, the error voltage is given by

$$\Delta V = V_{CK} \frac{WC_{OV}}{WC_{OV} + C_S} \tag{3-21}$$

where C_{OV} is the overlap capacitance per unit channel width. The error ΔV is independent of the input signal, introducing a constant voltage offset on the sampled output signal V_0.

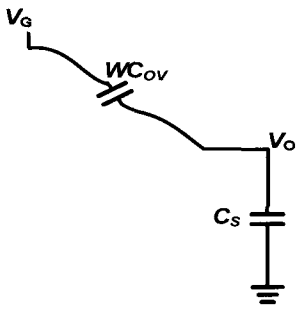


Figure 3-17 Clock Feedthrough

Clock feedthrough can be minimized by use of differential signal paths with symmetric clock signals. Various circuit techniques have been developed to cancel or suppress these effects and achieve high sampling accuracy. Table 3-4 summaries the error sources and possible solutions [63].

Error Sources	**Possible solution**
Finite bandwidth	Advanced technologies to lower the switch on-resistance Gate voltage bootstrapping
Charge injection	Bottom plate sampling Dummy switch
Clock Feedthrough	Differential signal paths

Table 3-4 Error Sources and Solution

These errors are consistent from sample to sample, called "deterministic components, and do not cause the fundamental limit for the input sampling to be equal to the converter resolution at least to the first order. Another error source which is unpredictable from sample to sample is noise. The dominant noise in the circuit of Fig.

3-4 is thermal noise, if we model the switch as a resistance when the switch is closed as shown in Fig. 3-18. Another noise source of the MOS transistor is called flicker noise or "1/f noise". Because of its low frequency characteristics, various techniques [64] [65] have been proposed to suppress flicker noise especially for high frequency sampling circuits. In the following analysis, we will focus on the thermal noise.

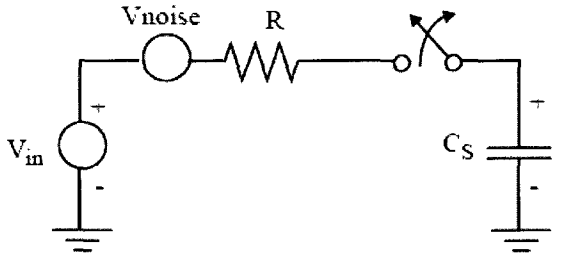


Figure 3-18 MOS S/H circuit equivalent models for noise calculation

In Fig. 3-18, the thermal noise of a resistor appears as additive noise to the signal, and its mean-square value within the bandwidth Δf (in Hz) is given by,

$$\overline{V}^2 = 4KTR * \Delta f \tag{3-22}$$

where K is Boltzmann's constant and T is the temperature in Kelvins. At room temperature $4KT = 1.66 * 10^{-20} V - C$.

During a sampling period, both the input signal voltage and the additive thermal noise appear across the sampling capacitor C_S. With single pole frequency response (R_{ON} and C_S), the total noise variance can be found by integrating the noise spectral density over frequency, and is given by

$$\delta^2 = \int_0^\infty \frac{\overline{V}^2}{\Delta f} \frac{1}{\left|1+\frac{jf}{f_{3dB}}\right|} d_f = \int_0^\infty 4KTR \frac{1}{\left(1+\left(\frac{f}{2\pi RC_S}\right)^2\right)} d_f = \frac{KT}{C_S} \quad (3\text{-}23)$$

where $f_{3dB} = \frac{1}{2\pi RC_S}$, R is the on-resistance of the MOS transistor, and C_S is the sampling capacitor value. This assumes that all the parasitic capacitance from the MOS switch is negligible compared to that of the sampling capacitor. Notice that the result is independent of R and is dependent only on temperature and the value of sampling capacitor C_S. This noise is usually called "KT/C" noise. The units of KT/C are V^2 and $\sqrt{KT/C}$ is the total rms noise voltage measured at the output. Table.3-5 shows RMS values for the noise for different sampling capacitor values at room temperature.

Capacitor value	$\sigma = \sqrt{KT/C}$
0.001 pF	640 μV
1 pF	64 μV
100 pF	6.4 μV

Table.3-5 RMS Values of Thermal Noise for Different Sampling Capacitance Values

To guarantee that the noise error doesn't degrade the ADC resolution accuracy, the KT/C noise power should be much less than the quantization noise power. In the worst case, the expression is given by

$$\frac{KT}{C_S} \leq \frac{\Delta^2}{12}$$
$$\Delta = \frac{V_{FS}}{2^B - 1} \qquad (3\text{-}24)$$
$$\Rightarrow$$
$$C_S \geq 12KT\left(\frac{2^B - 1}{V_{FS}}\right)^2$$

where B is the ADC resolution in bits, V_{FS} is the full-scale input range, Δ is the quantization step (magnitude of LSB) and $\Delta^2/12$ is the quantization noise power.

The minimal capacitor value for different resolutions is summarized in Table 3-6.

Resolution(bit)	C_{min} (V_{FS}=1 V)
8	0.003pF
12	0.8pF
14	13pF
16	206pF
20	52,800pF

Table.3-6 Minimal Capacitor Value C_S for Differential Resolutions

Due to the randomness of the samples, the error due to thermal noise cannot be perfectly predicted, and therefore the achievable signal-to-noise-ratio (SNR) for a given sampling capacitor value is limited. For given sampling capacitor C_S and input signal range V_{FS}, the SNR is given by

$$SNR = 10\log(\frac{V_{FS}^2/2}{\sigma^2}) \tag{3-25}$$

In reality, the ADC quantization noise dominates if the thermal noise is much less than the quantization step size. If we take the quantization noise into consideration, the SNR is given by

$$SNR = 10\log(\frac{V_{FS}^2/2}{\sigma^2 + \Delta^2/12}) \tag{3-26}$$

Combing Equations (3-24) and (3-26), for B=10 and C=1 pF, the SNR is 61.96dB for the noiseless ideal 10 bit ADC. In Fig. 3.19, the maximum achievable SNR is plotted for different sampling capacitor values at different resolutions levels. For a large sampling capacitor value, e.g. 10 pF, the curve is flattened out and the SNR is limited by the quantization noise.

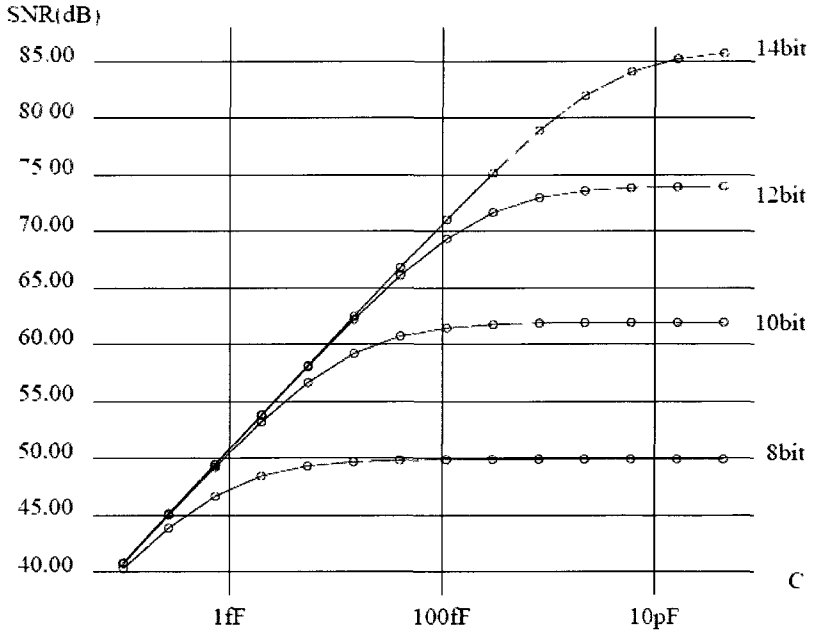


Figure.3-19 SNR for Different Sampling Capacitor Value and Resolution

3.4.2 Switched Source Follower Architecture

As mentioned before, the switched source follower can achieve a very high sampling speed but at the expense of power consumption. The schematic diagram of a traditional switched source follower sample and hold amplifier (SHA) is shown in Fig. 3-20 [66]. The SHA includes a differential input, two pairs of control switches, and an output follower. As shown in Fig.3-21, in the sample mode when the tracks signal is high. M_7 and M_{10} are turned on to pull the source voltage of M_{SF} on. The M_{SF} pairs are source followers and the output follows exactly the differential input signal. In Fig.3-22, in the hold mode when Hold signal is high, the tail current I_1 flows through the differential pair R to pull the gate voltage of M_{SF} low. The resistance of R is chosen so that the voltage drop across R can sufficiently turn off the transistor pair M_{SF}. Then the differential capacitors hold the sampled value until the next clock.

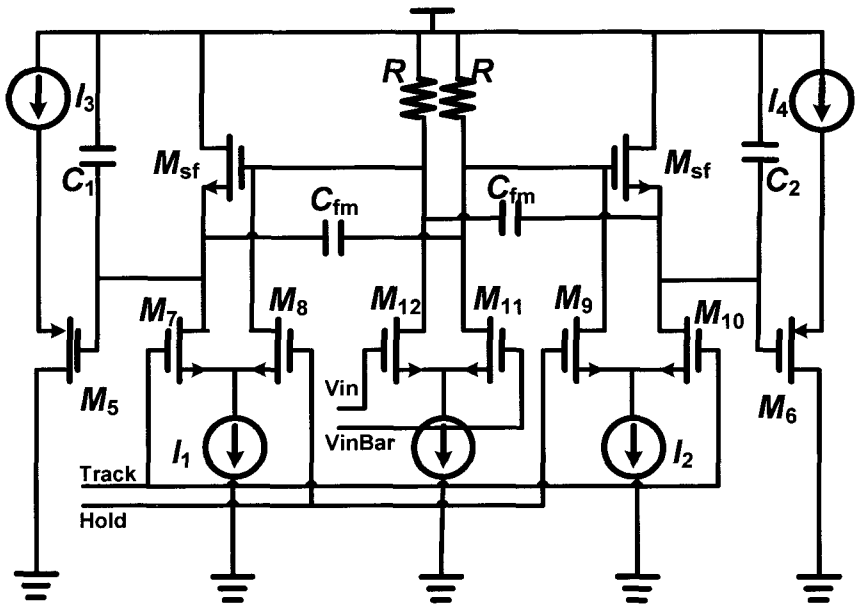


Figure 3-20 Traditional Switched Series Follower SHA

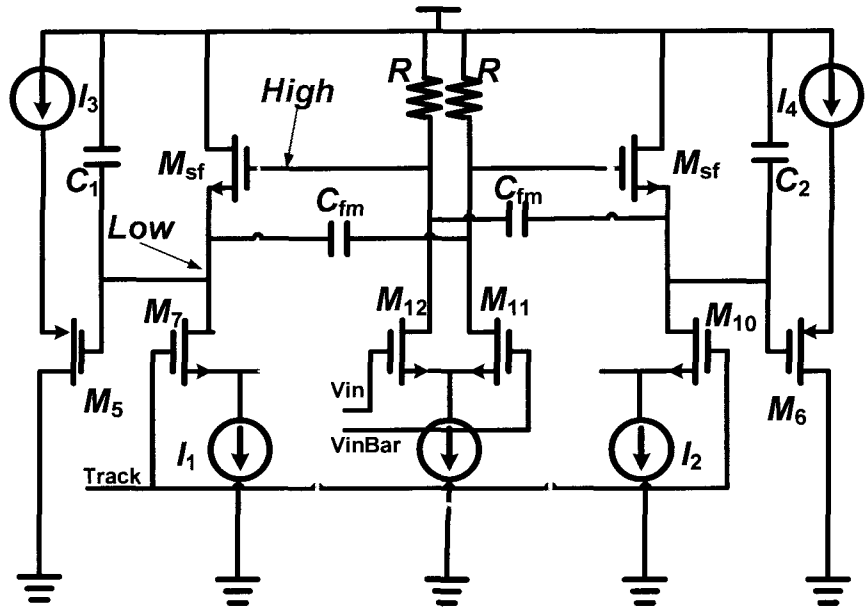


Figure 3-21 SSF SHA Operates on Sample Mode

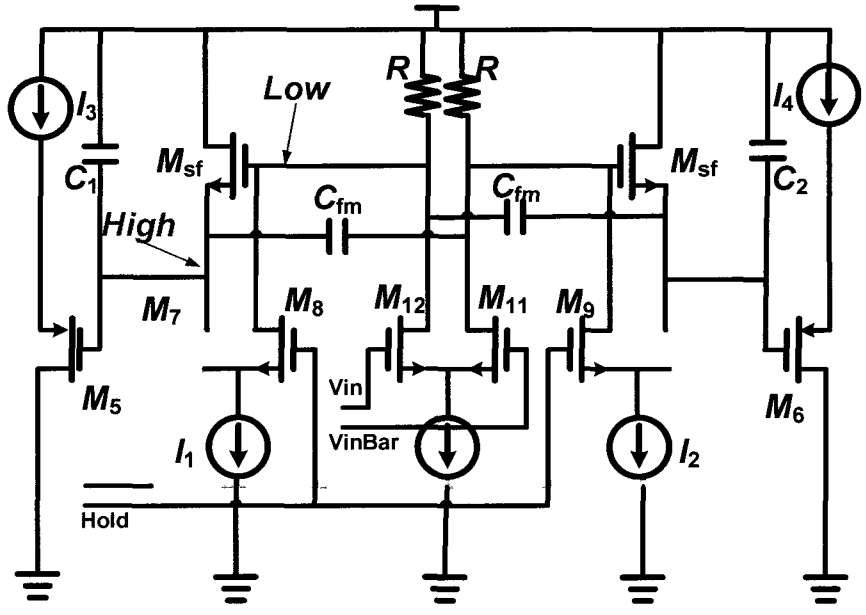


Figure 3-22 SSF SHA Operates on Hold Mode

However, this architecture suffers from two serious artifacts. The first one is the decay of the output signal as energy is lost from the storage element (usually a

capacitor) within the track and hold circuit. However, this droop problem is usually not a challenge for CMOS amplifiers since they have infinite DC input impedance. The second important artifact is the feedthrough in the hold mode. Input signals can still change the values at the output nodes during the Hold mode through the parasitic gate-source overlap capacitance C_{gso}. As a consequence, the output signals of the M_{SF} pair in Fig. 3-20, which are supposed to keep the sampled data constant, may have significant shift due to this feedthrough. In the past design [66], a fixed capacitance C_{fm} whose value is equal to C_{gso} of M_{SF} is used to match and thus cancel this feedthrough effect [67]. The capacitance C_{gso} of M_{SF} is voltage independent. During the sample mode, M_{SF} is on, and the gate-source capacitance C_{gs} of M_{SF} consists of the gate-channel source capacitance C_{gsc} plus the gate overlap capacitance C_{gso}. During the hold mode, the M_{SF} pair is off and C_{gs} is only the overlap capacitance C_{gso} in M_{SF}. Because C_{gso} is process dependent, a constant capacitor cannot perfectly match its value.

3.4.3 Novel MOSFET Switched Source Follower S/H Amplifier

Here, we propose a new technique to cancel the hold mode feedthrough effect as shown in Fig. 3-21. As mentioned earlier, when this SHA operates in the Hold mode, M_{SF} is off. The feedthrough capacitor becomes the gate-source overlap capacitance C_{gso}. The output still changes because the charge goes through the overlap capacitance C_{gso}. Thus, we can use an off- state transistor to perfectly match the feedthrough capacitor. As shown in Fig. 3-21, M_3 and M_4 are off-state transistors and their source voltages will follow their drain voltage through M_3 and M_4's

overlap capacitor C_{gso}. The noise signal travels through overlap capacitor of M_{SF} and is amplified by the source follower as in the red line and the noise signal also travels through the overlap capacitor of off-state transistor M_3. Therefore, we can subtract M_3 and M_4 's source voltage from the SHA output, the feedthrough impact can be theoretically removed from the SHA output.

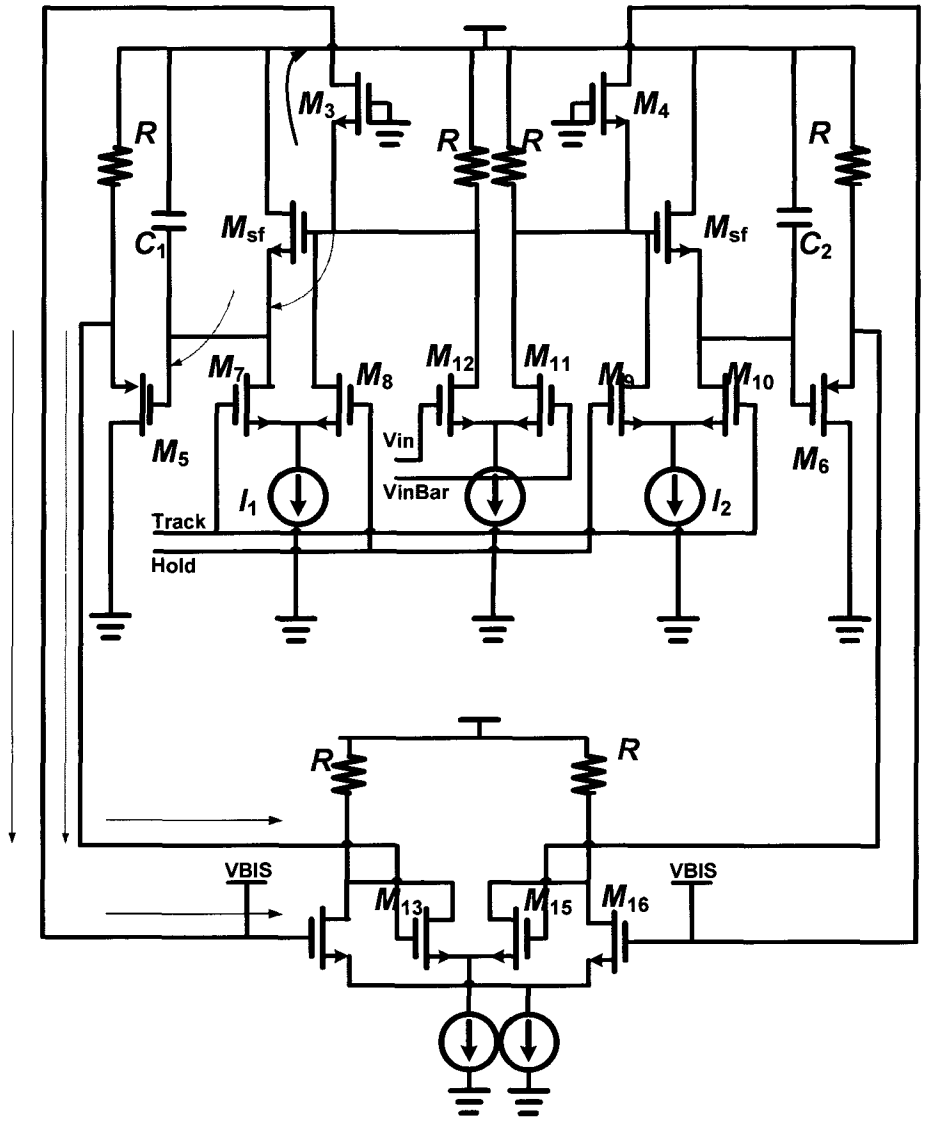
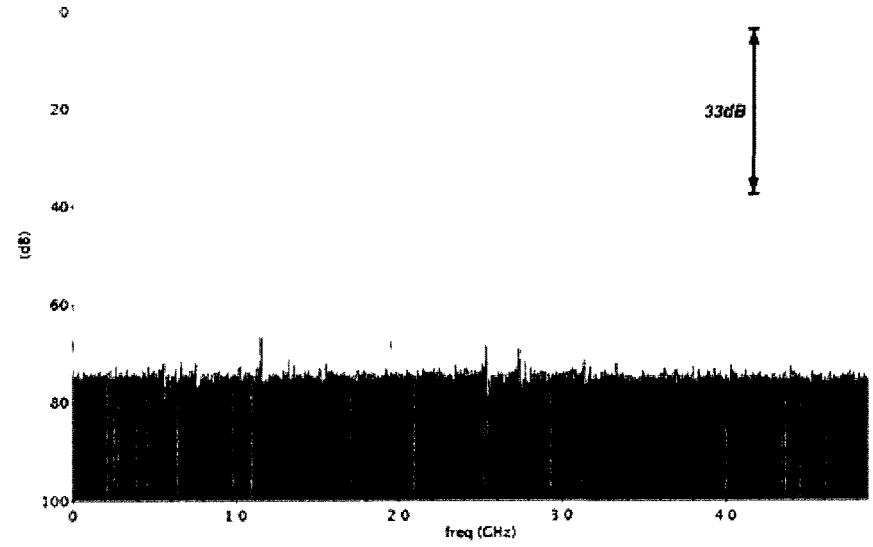


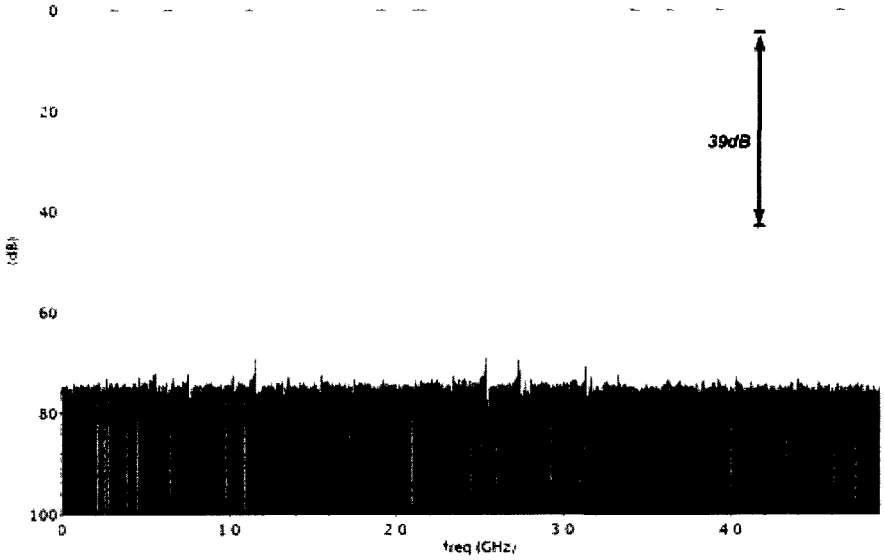
Fig.3-23 Proposed SHA with Feedthrough Cancellation

The simulated output of SHA without a feedthrough cancellation circuit is compared to the output of THA with the feedthrough cancellation circuit in Fig. 3-24. As shown in Fig. 3-24(a), when a traditional SSF SHA works in the Hold mode, the held voltage is not constant but is affected by the input signal through the parasitic capacitor between the input and output nodes.

The FFT (N=4096, sampling rate at 10 GHz) analysis comparison results are shown in Fig. 3-24. As shown in Fig.3-24, the proposed SHA achieves a 6 dB SFDR improvement over the traditional one.



(a) FFT of 1.95GHz and a Sample Clock@10GHz without Feedthrough Cancellation



(b) FFT of 1.95 GHz and a Sample Clock @ 10GHz with Feedthrough Cancellation

Fig.3-24 FFT Analysis Comparison

Fig. 3-25 shows the comparison of total harmonic distortion (THD) performance between traditional SSF SHA and that of the proposed feedthrough cancellation SSF SHA. The frequency of the analog sinusoidal input is varied from 500 MHz to 5 GHz.

The simulated results reveal that the SHA achieves 6-bit effective number of bits (ENOB) at 10 G samples/s and an input frequency of 4 GHz.

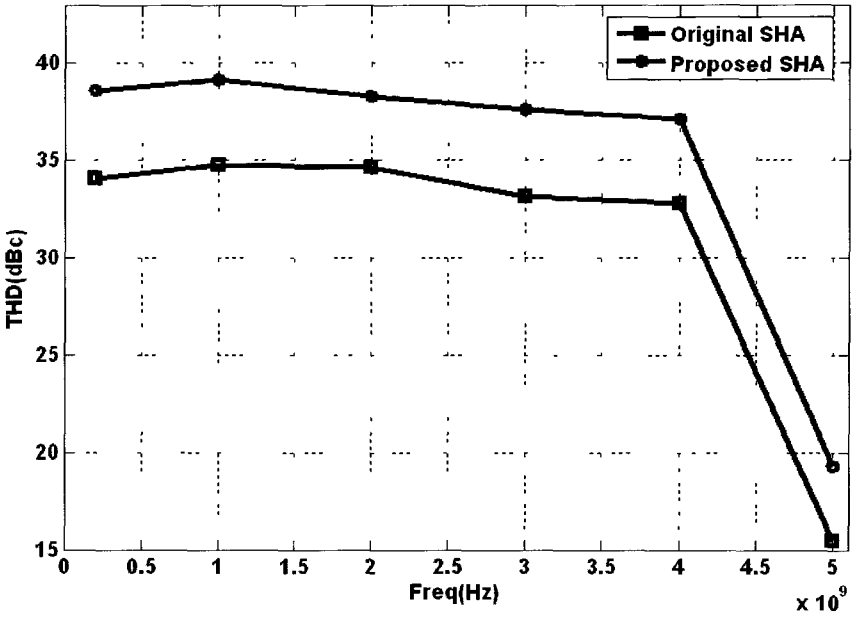


Fig.3-25 Total Harmonic Distortion (THD) Comparison

3.5 Closed loop S/H architecture

As discussed previously, the open loop architecture can achieve high speed but only limited resolution. When an S/H circuit with a precise gain (which is generally different from unity) and high linearity is needed, a switched capacitor circuit with its gain set by a capacitor ratio is the best solution. Negative feedback is a well-known technique used to linearize circuits. For example, enclosing the sampling capacitor in the feedback loop reduces the effects of nonlinear parasitic capacitances and signal-dependent charge injection in MOS switches. Unfortunately, an inevitable consequence of the use of feedback is reduced speed.

In this section three common switched-capacitor sample and hold (SC S/H) configurations are chosen and their basic operation and related key parameters are presented first for ideal op amps. A basic configuration is identified and discussions on its power dissipation are presented. The detailed analysis and practical design considerations will be discussed in next chapter.

Fig. 3-26, Fig. 3-27, and Fig. 3-28 show three common configurations for SC S/H circuits [68]-[77]. For simplicity, single-ended configurations are shown. Switch configurations shown in each figure are for the sampling phase, and the arrows indicate how the switches must be changed to establish the transfer (or hold) phase. In all cases, the basic operations include sampling the signal voltage on the sampling capacitor(s) and transferring its charge to the feedback capacitor by using an op amp in the feedback configuration. In the circuit in Fig.3-26, with an ideal opamp and switches, the opamp forces the

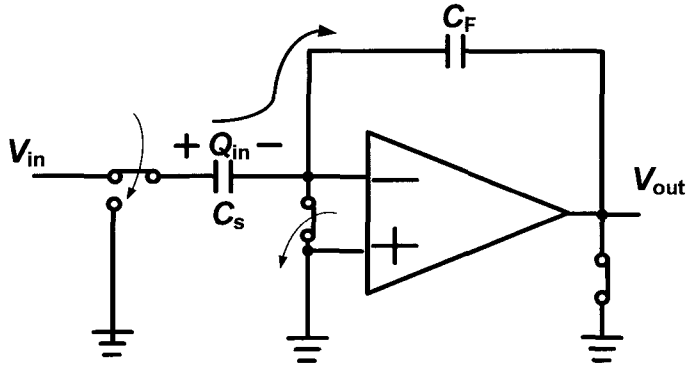


Figure 3-26 A SC Circuit with Separate Capacitor C_S and C_F

sampled signal charge on capacitor C_S to transfer to C_F, since the charge is conserved during the transfer stage. The voltage at the output of the opamp is given by

$$V_{out} = \frac{Q_{in}}{C_F} = \frac{C_S * V_{in}}{C_F} = \frac{C_S}{C_F} * V_{in} \tag{3-27}$$

In Fig. 3-27, only one capacitor is used as both sampling capacitor and feedback capacitor. This configuration cannot implement a gain other than unity, but it can achieve high speed because the feedback factor (the ratio of the feedback capacitor to the total capacitance at the summing node) can be much larger than that of the previous configuration, since it operates much closer to the unity gain frequency of the amplifier. This configuration is often used in the front-end of S/H circuits. According to the charge conservation rule, the voltage at the output of the opamp is given by

$$V_{out} = \frac{Q_{in}}{C_F} = \frac{C_F * V_{in}}{C_F} = 1 * V_{in} \tag{3-28}$$

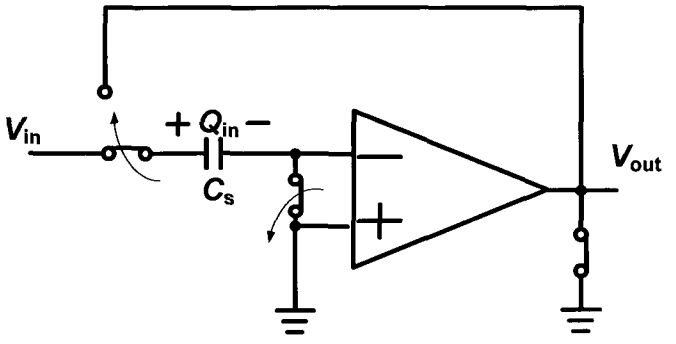


Figure 3-27 A SC Circuit with One Capacitor

Fig. 3-28 shows another configuration which is a combined version of the configurations in Fig. 3-27 and Fig. 3-28. In this configuration, the signal is sampled on both C_S and C_F, and the resulting transfer function is

$$V_{out} = \frac{Q_{in}}{C_F} = \frac{C_F * V_{in} + C_S * V_{in}}{C_F} = (1 + \frac{C_S}{C_F}) * V_{in} \tag{3-29}$$

In this configuration, C_F is also used as a sampling capacitor in order to improve the feedback factor. For example, if the closed loop gain is 2 and the op amp input capacitance (C_{opamp}) is negligible, the feedback factor F in this configuration is $C/2C = 0.5$, much larger than that of the configuration in Fig. 3-27($F = C/3C = 0.33$), which in turn results in 50% improvement in the SC circuit bandwidth. The detailed analysis of these results is discussed in Chapter 5.

Important parameters in determining the bandwidth of the SC circuit are Gm (transconductance of the op amp), feedback factor f , and output load capacitance C_{load}. In all of these three configurations, the bandwidth is given by:

$$BW = \frac{1}{\tau} = \frac{G_m}{C_{load}} * f \tag{3-30}$$

where C_{load} is the total capacitance seen at the op amp output.

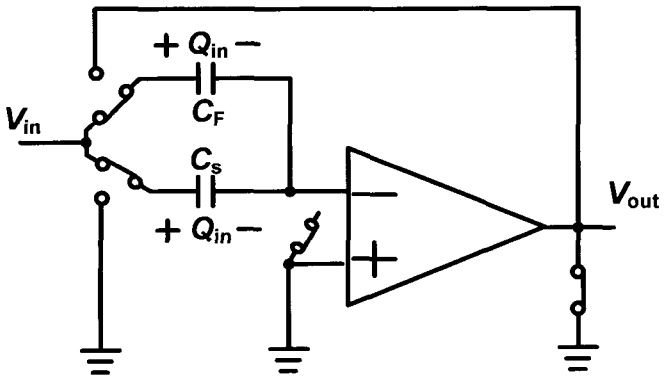


Figure 3-28 A SC Circuit with C_F and C_S as Sampling Capacitors

Table 3-7 summarizes the key parameters of the entire three configurations, where C_{opamp} is the opamp's input parasitic capacitance.

Configurations	Transfer Function (V_{out}/V_{in})	Feedback Factor (f)
Fig.3-26 (Conf I)	$\frac{C_S}{C_F}$	$\frac{C_F}{C_S + C_F + C_{opamp}}$
Fig.3-27 (Conf II)	1	$\frac{C_S}{C_S + C_{opamp}}$
Fig.3-28 (Conf III)	$1+\frac{C_S}{C_F}$	$\frac{C_F}{C_S + C_F + C_{opamp}}$

Table 3-7 Key Parameters Comparison among Three Configurations

As shown in Table 3-7, Conf II has a larger feedback factor, thus offering higher bandwidth, but it can't implement any gain greater than unity. Conf I and Conf III can achieve desired gain function with the proper choice of C_S and C_F. To achieve the same gain, Conf III has a higher bandwidth performance than Conf II.

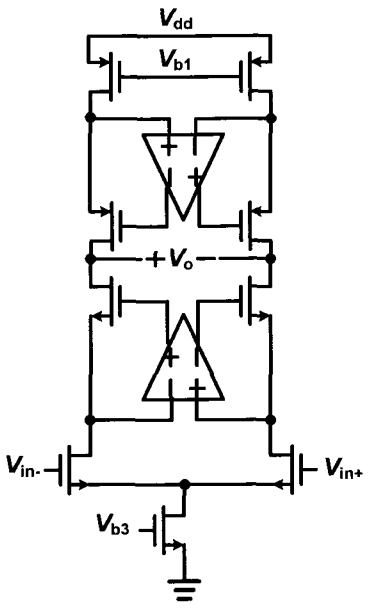
CHAPTER 4

LOW PWOWER CIRCUIT DESIGN

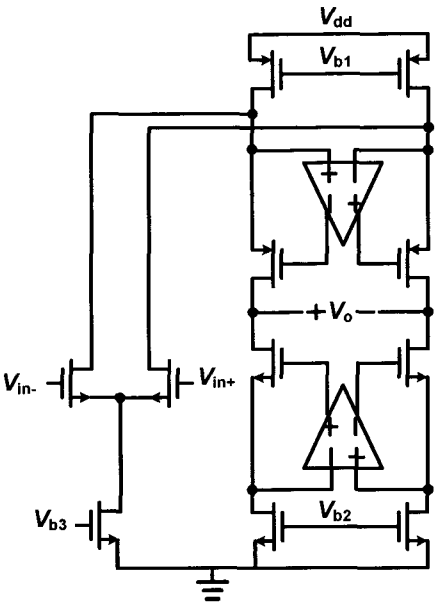
This chapter describes the analog building block used in analog-to-digital converter (ADC) design and focuses on various circuit imperfections that can degrade the analog-to-digital converter performance. The design trade-offs are presented and analyzed, and the requirements for different analog building blocks are derived.

4.1 Operational Transconductance Amplifier (OTA) Design

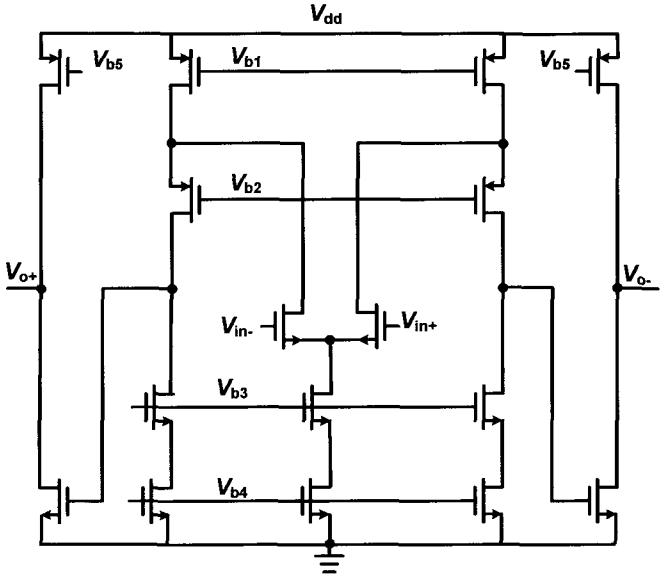
As CMOS design scales down for low power and low voltage, the operation of such analog circuits under limited voltage supply becomes more and more difficult. Amplifiers are widely used among all analog circuits. With technology shrinking down to the nanometer region, to get a high gain and large headroom amplifier is quite difficult. To increase the gain performance, several topologies are available, e.g. telescopic differential OTA with gain boosting [78], folded-cascode OTA with gain boosting [79], and 2-stage OTA. Those three OTAs are shown in Fig.4-1.



(a) Telescopic Differential OTA with Gainboosting



(b) Folded-Cascode OTA with Gainboosting



(c) Two Stage OTA

Figure 4-1 OTA Architectures

Among the three architectures, the telescopic amplifier has the lowest output swing range but minimum power consumption. Its output swing overhead is limited by five V_{dsat} (MOS overdrive voltage) and one V_{th} (MOS threshold voltage) if tail current is not considered, which will degrade the circuit dynamic range. However, since the minimum number of transistors is used, telescopic amplifiers can achieve a better noise performance.

The 2-stage OTA, on the other hand, can offer larger output swing with only two V_{dsat} (MOS overdrive voltage) limitations. The additional stage introduces another dominant pole, which has a negative impact on frequency response. Frequency compensation, such as Miller and cascode compensation techniques, has to be employed [80]. Therefore, there is a trade- off between power and bandwidth, which is not good for high speed ADC design.

The folded-cascode architecture with gain-boosting is the best fit for high speed and high dynamic range applications. It offers a relatively large output swing and only single-pole frequency response. Moreover, it can also achieve a much larger input common-mode voltage swing. With the assistance of the gain-boosting technique, it can achieve a voltage gain as high as $(g_m r_o)^4$ while still keeping the regular cascode structure frequency response characteristics. The OTA performance comparison is summarized in Table.4-1.

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	High
Two-Stage	High	Highest	Low	Medium	Low

Table.4-1 OTAs Comparisons

4.2 OTA Based Switched Capacitor Circuit

We have briefly introduced the basic switched capacitor (SC) circuit in the last chapter. In reality, there are a large number of non-idealities in a SC circuit influencing the performance of the ADC converters [80]. In this section, the influences of several non-idealities including finite OTA gain, finite OTA bandwidth, finite slew-rate and non-zero resistance of the switches on the transfer function of the SC circuit are studied. Other non-ideal effects include clock feed-through and charge injection of the switches, the influence of capacitor mismatch, and non-linear circuit non-idealities such as the non-linear resistance of the switches, the non-linear capacitors and the non-linear amplifier gain.

Due to the influence of non-idealities, the performance of a practical implementation of an ADC can be significantly worse than the values predicted by the simulation of an ideal ADC. To successfully design an ADC, the influence of various

circuit imperfections must be considered. Then specifications for different building blocks should be selected in order to minimize the performance degradation.

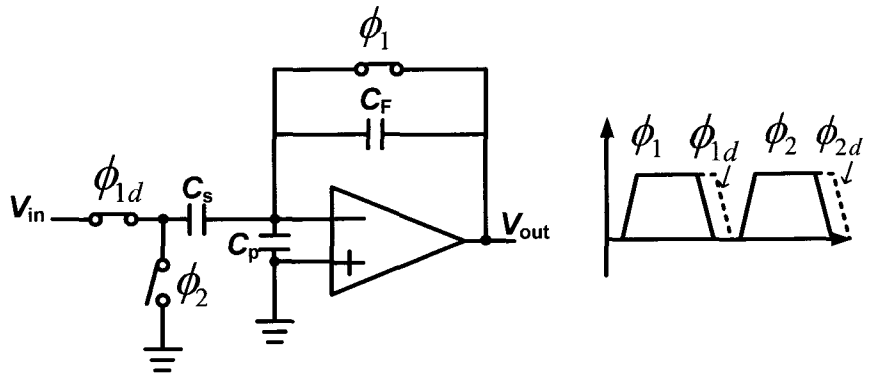


Figure 4-2 Switched Capacitor Amplifier

Fig.4-2 shows a well-known switched-capacitor amplifier model. A non-overlapping control signal is used in the following analysis. Two non-overlapping clock phases ϕ_1 and ϕ_2 in conjunction with their delayed versions ϕ_{1d} and ϕ_{2d} are used to avoid signal-dependent charge injection. C_S is the sampling capacitor. C_F is the integration capacitor. And C_P represents the total parasitic capacitance at the input of the OTA. C_L represents the sampling capacitance of the next integrator. For simplicity, only a single-ended model is shown here. In practice, all implementations are differential.

4.2.1 Finite OTA Gain

Ideally, the SC amplifier operation in its two phases is shown in Fig.4-3. Applying the principle of charge conservation and Kirchoff's laws and combining the equations for the sampling phase and the integration phase, the SC gain amplifier should have the following transfer function, as derived in Chapter 3.

$$V_o = \frac{C_S}{C_F} * V_i \tag{4-1}$$

If the OTA is ideal, the input/output transfer curve is a straight line with a slope of C_S / C_F. However, for practical purposes, we will say that the OTA is a voltage amplifier with a finite gain of A_v.

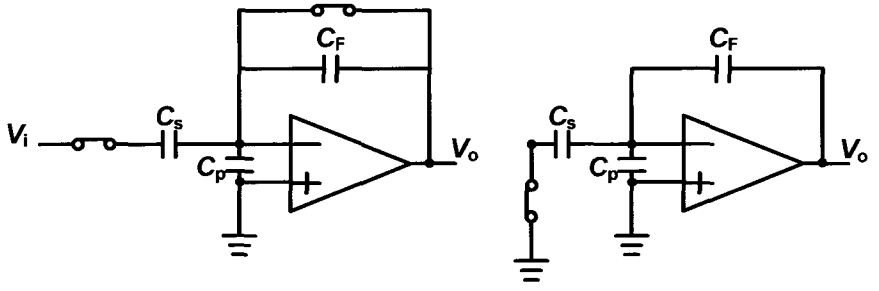


Figure 4-3 SC Amplifier Model with Finite OTA Gain

For simplicity, the transfer function is calculated without the input parasitic capacitance and without load capacitance. If the OTA has a finite DC gain, it will introduce a gain error in the actual input/output transfer curve. Fig. 4-4 shows the transfer curves with and without gain error. When we apply the principles of charge conservation and Kirchoff's laws and combine the equations for the sampling phase and the integration phase. The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{C_S}{C_F} * \frac{1}{1 + \frac{1}{A_v * f}} \tag{4-2}$$

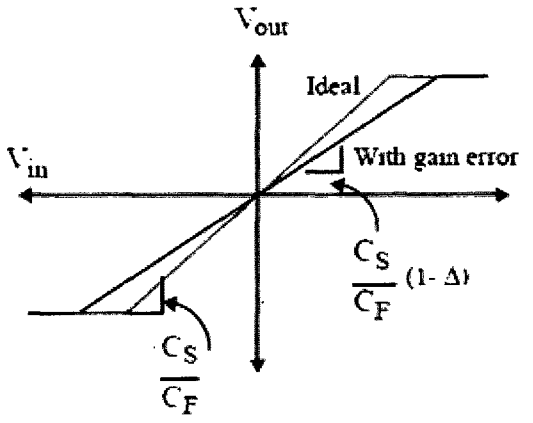


Figure 4-4 Transfer Curve with Gain Error for A SC OTA

f is the feedback factor and is defined by $f = C_F / (C_S + C_F)$ and A_v is the DC gain of the amplifier. Therefore, if the product $A_v f$, which is the loop gain of the feedback system is low, the gain will be less than the capacitor ratio C_S / C_F. The gain error is $1/A_v f$ as illustrated in Fig. 4-5. For the input S/H circuit, the gain error can be tolerated if the A/D conversion does not require an absolute scale. There is no error introduced if the gain is linear, but it will reduce the signal amplitude a little bit. For example, if we assume $C_S = C_F$ and A_v=300, the loop gain $A_v f$ equals 100. Therefore, the closed loop gain is 0.99 instead of 1. Usually, a 1% error of input scaling signal is tolerable for low resolution applications if the quantization does not depend on the absolute value. However, for the high resolution pipeline A/D converters (e.g. 10 bit), the OTA needs to have an exact high gain to get very high accuracy within +/- 0.1%. In this case, the DC gain of the OTA must be larger than 75 dB, so capacitors must be trimmed to compensate for the error because of the insufficient op amp DC gain. To increase the DC gain, the multi-stage op amp or gain-boosting technique is applied, which usually limit power dissipation. The latter solution, however, usually requires

an extra high precision circuit or method to measure the relative capacitor values [81] [82].

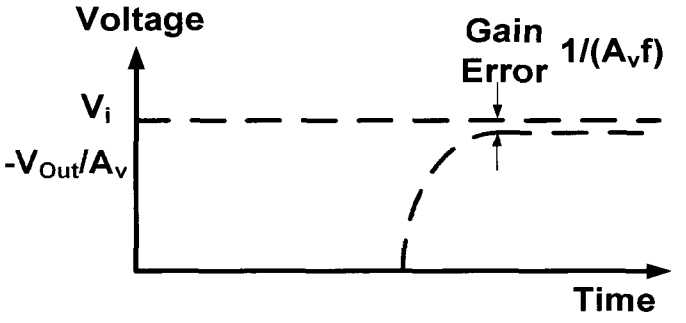


Figure 4-5 Gain Error

Distortion is another concern. In an actual OTA, the input/output transfer function curve is not a simple straight line but is instead a line with some curvature, which causes harmonic distortion. The negative feedback around the op amp can reduce its distortion by a factor of $A_v f$. Their distortion in an S/H circuit will result in large integral non-linearity error (INL) causing harmonic distortion and intermodulation distortion.

4.2.2 Non- linear of OTA Gain

In the previous section, the influence of a fixed finite gain of the OTA on the input/output transfer function was discussed. However, in reality, the gain varies for different input and output voltage of the OTA. The input voltage dependency can be neglected since the input voltage is sampled and stored in the capacitor at the end of the sampling interval and always settles to the same voltage. However, the output voltage of the OTA depends on the gain, and it varies significantly due to variations in the OTA finite gain.

By Taylor series expansion, neglecting the higher order nonlinear terms, we only consider the first and second order effects on the voltage gain, which is approximated by

$$A_v = A_o(1 + a_1 V_o + a_2 V_o^2) \tag{4-3}$$

To simplify the calculation, let's make $V_{o1} = V_o\left[(n-\frac{1}{2})T_S\right]$, $V_{o2} = V_o\left[(n+\frac{1}{2})T_S\right]$, $V_i = V_i[nT_S]$. Then, we get the signal transfer function as following.

$$V_{o2} - V_{o1} - \frac{V_{o2}}{A_o(1 + a_1 V_{o2} + a_2 V_{o2}^2)} + \frac{V_{o1}}{A_o(1 + a_1 V_{o1} + a_2 V_{o1}^2)} = \frac{C_S}{C_F} V_i \tag{4-4}$$

If we apply iterative recursive technique [83] to solve above equation with $a_1 V_{o1} + a_2 V_{o1}^2 << 1$, we get

$$V_{o2} - V_{o1} - \frac{V_{o2}}{A_o}(1 - a_1 V_{o2} - a_2 V_{o2}^2) + \frac{V_{o1}}{A_o}(1 - a_1 V_{o1} - a_2 V_{o1}^2) = \frac{C_S}{C_F} V_i \tag{4-5}$$

$$V_{o2} - V_{o1} = \frac{\frac{C_S}{C_F} V_i}{1 - \frac{a_1}{A_o}(V_{o1} + V_{o2}) - \frac{a_2}{A_o}(V_{o1}^2 + V_{o1}V_{o2} + V_{o2}^2)} \tag{4-6}$$

Assume $A_o >> 1$, we get

$$V_{o2} - V_{o1} \approx \frac{C_S}{C_F} V_i (1 - \frac{a_1}{A_o}(V_{o1} + V_{o2}) - \frac{a_2}{A_o}(V_{o1}^2 + V_{o1}V_{o2} + V_{o2}^2)) \tag{4-7}$$

If we apply an input sinusoid signal with amplitude V_i and frequency ω_i, the input and output are approximated as

$$
\begin{aligned}
&v_i = V_i \sin(n\omega_i T_s), \ and \\
&v_{o1} = V_o \cos[(n-\frac{1}{2})\omega_i T_s], \ and \\
&v_{o2} = V_o \cos[(n+\frac{1}{2})\omega_i T_s]
\end{aligned}
\tag{4-8}
$$

If we combine the above equations, the second harmonic distortion relative to the fundamental is approximated by

$$
HD_2 \approx \frac{a_1}{2A_o} V_o = \frac{a_1}{2A_o}(\frac{C_S}{C_F})V_i \tag{4-9}
$$

Similarly, the third harmonic is calculated by

$$
HD_3 \approx \frac{|a_2|}{4A_o} V_o^2 = \frac{|a_2|}{4A_o}(\frac{C_S}{C_F})V_i^2 \tag{4-10}
$$

The second and third harmonic distortions versus the coefficients a_1 and a_2 for different amplifier gains are plotted in Fig. 4-6. As shown, the second harmonic distortion is worse than that of the third harmonic. However, in the fully differential switched circuit implementation, the second harmonic distortion due to amplifier nonlinearity is eliminated except in case of circuit mismatch. Note that the larger the amplifier gain is, the less harmonic distortion it will have. However, if the coefficient a_1 and a_2 approach 0.1, the assumption of $a_1 V_{o1} + a_2 V_{o1}^2 << 1$ is not true any more. According to [84], the simulated second and third harmonic distortion is increased up to 12 dB and 6 dB when $a_1 = a_2 = 1$ comparing to when $a_1 = a_2 = 0$. Therefore, if we leave 6 dB margin for the requirement of harmonic distortion, the value of harmonic distortion can be roughly determined.

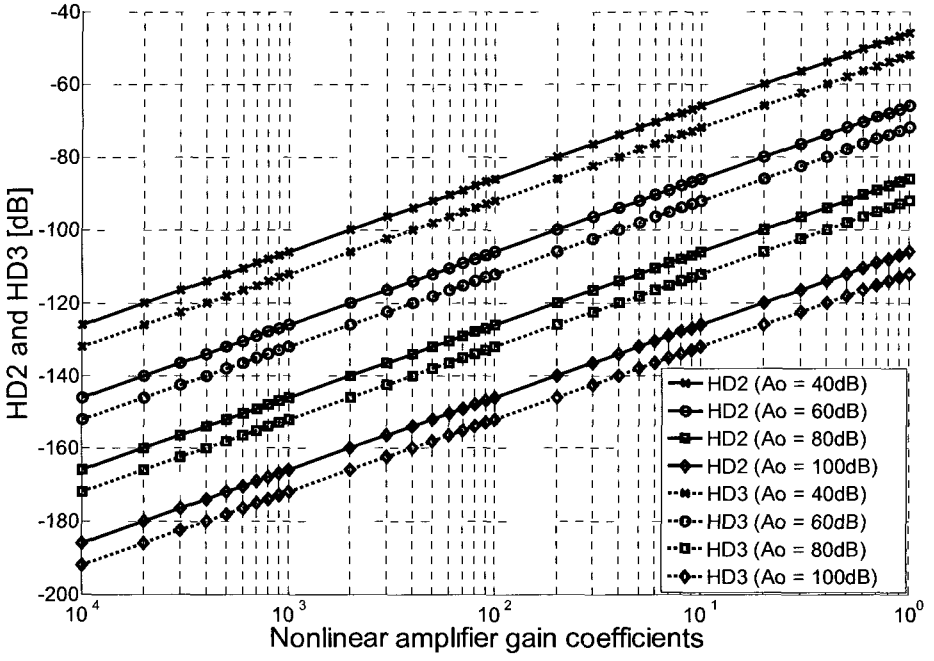


Figure 4-6 HD2/HD3 versus nonlinear gain coefficients a_1 and a_2 with different amplifier

4.2.3 Finite OTA Bandwidth

In practical implementations, during the transfer phase, the OTA can not settle at the final value instantaneously because of the finite bandwidth of the OTA. Instead, the settling occurs, and hence introduces settling error if the settling procedure is not fast enough.

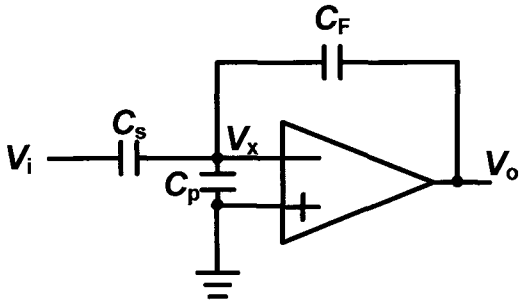


Figure 4-7 Switched Capacitor Bandwidth Calculation Model

As shown in Fig. 4-7, applying the principle of charge conservation and Kirchoff's laws and doing the Laplace transform of the input/output response, we get

$$\begin{cases} V_x*(C_S+C_F+C_P)=V_i*C_S+V_o*C_F \\ V_o*s*C_L+G_m*V_x+(V_o-V_x)=0 \end{cases}$$

$$\Rightarrow$$

$$\frac{V_o}{V_i}=\frac{\frac{C_S}{C_F}*f*(sC_F-G_m)}{fG_m+s(C_L+C_F(1-f))} \qquad (4\text{-}11)$$

$$\Rightarrow$$

$$\frac{V_o}{V_i}=\frac{-\frac{C_S}{C_F}*f*(1-sC_F/G_m)}{1+s\frac{C_L+C_F(1-f)}{fG_m}},$$

where f is the feedback factor, and $f=C_F/(C_S+C_F+C_P)$. Equation 4-11 tells that there is a major zero and a major pole in the transfer function. To calculate the feedback system's step response, a unit step is applied to the input terminal. Taking the inverse Laplace transform gives the time step response,

$$V_o(t) = \xi^{-1}\left\{H(s) * \frac{V_i}{s}\right\}$$
$$=> \tag{4-12}$$
$$V_o(t) = -V_i \frac{C_S}{C_F}\left\{1-(1-\frac{\rho}{z}) * e^{-t/\tau}\right\}$$

Where V_i is a non-unit amplitude step, $\tau = \rho = -fG_m / C_{Leff}$ and $C_{Leff} = C_L + C_F(1-f)$ and $z = G_m / C_F$. From Equation (4-12), we can see that the existing zero changes the initial behavior of the step response. There are two cases. Case I: If $|P/Z| << 1$, the step response can be reduced to

$$V_o(t) = -V_i * \frac{C_S}{C_F}\left\{1-e^{-t/\tau}\right\} \tag{4-13}$$

The relative settling error is given by

$$\varepsilon = \frac{V_o(t->\infty) - V_o(t=t_s)}{V_o(t->\infty)} = e^{-t/\tau} \tag{4-14}$$

where t_s is one clock cycle. For example, if the clock cycle t_s equals to 4.6 ns and the system requires 1% settling error, then, the time constant $\tau = -t_s / \ln\varepsilon = 1$ ns.

Case II: if $|P/Z|$ is not negligible, the relative settling error is given by,

$$\varepsilon = \frac{V_o(t->\infty) - V_o(t=t_s)}{V_o(t->\infty)} = (1-\frac{P}{Z})e^{-t/\tau} \tag{4-15}$$

Let's take an example to compare the two cases. If we assume C_S=250 fF, C_F=1 pF, $C_i = 250fF$ and $C_L = 1$ pF, the comparison is shown in Table. 1

	$\|P/Z\| \ll 1$	$\|P/Z\|$ *not negligible*
Settling error $\varepsilon = 0.1\%$	$t_s = 6.9\tau$	$t_s = 7.3\tau$

Table 4-2 Settling Error Comparison

Case II gives a more accurate estimate of the settling error due to the OTA's finite bandwidth and finite gain.

4.2.4 Finite slew-rate of OTA

In the previous section, we observed that the finite gain and bandwidth of the op amp can introduce settling error. Actually, the output signal does not exhibit simple linear settling behavior. The settling time consists of two time periods. One period is limited by the time constant, and the other period is determined by the slew rate, as illustrated in Fig. 4-8.

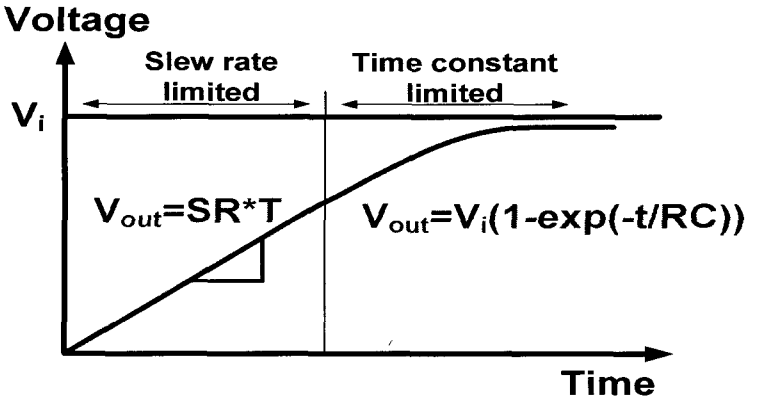


Figure 4-8 Voltage Waveforms at Output of a SC Circuit

As shown in Fig.4-8, slewing is followed by linear settling. If the output voltage achieves the desired value within the slewing time plus linear settling time, there will be no performance degradation.

To analyze the slewing and settling behavior, we apply the circuit model shown in Fig. 4-9.

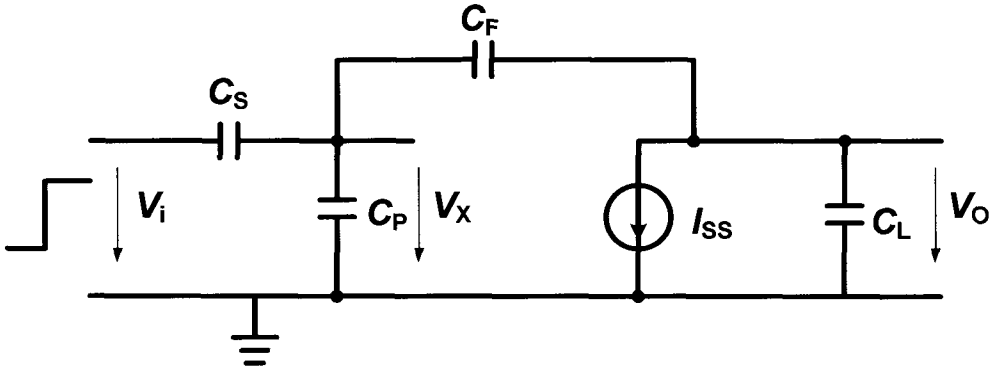


Figure 4-9 Circuit Model during Slewing

In Fig. 4-9, I_{SS} is the load current source. A step voltage is applied at the input terminal. At $t = 0$ ns, before I_{SS} is anything except zero, the voltage at V_x and V_o are determined by the capacitor divider and given by

$$V_x = V_i \frac{C_S}{C_S + C_2} \text{ with } C_2 = C_i + \frac{C_F C_L}{C_F + C_L} \tag{4-16}$$

$$V_o = V_x \frac{C_F}{C_L} \tag{4-17}$$

After $t > 0$ ns and before $V_x > V^*$ (V^* is MOSFET overdrive voltage), the MOSFET current is steered in one side and can be modeled as a constant current source I_{SS}. Then V_x and V_o are changed at a constant ramp rate as shown in Fig.4-10.

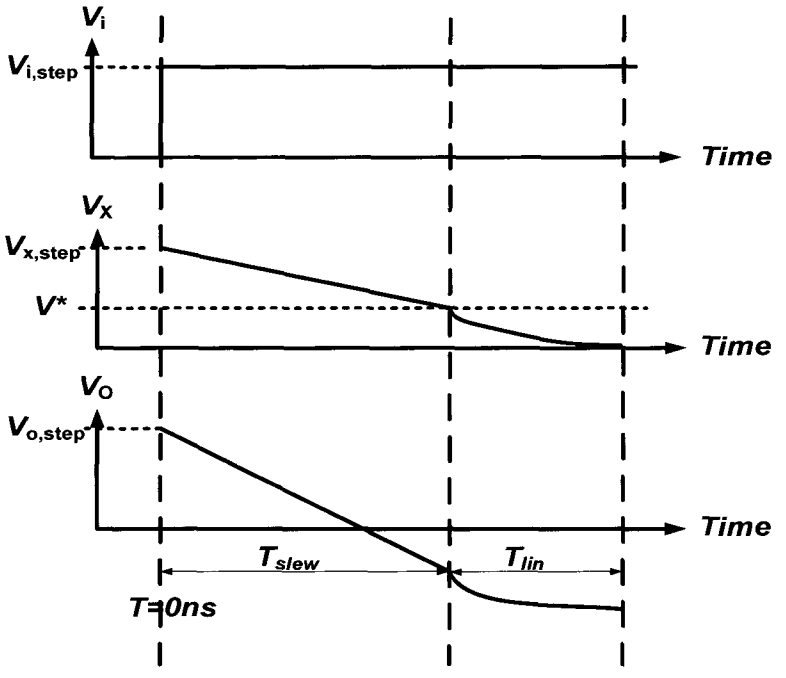


Figure 4-10 Slewing Analysis

After $V_x > V^*$, the opamp's linear settling behavior happens as analyzed in above section. The linear settling is illustrated in Fig.4-8. Therefore, the total settling time includes slewing time and linear settling time. The slewing time period starts from the beginning until $V_x = V^*$ and is calculated by

$$V_{x,step} = V_{i,step}\frac{C_S}{C_S + C_2} \quad with \; C_2 = C_i + \frac{C_F C_L}{C_L + C_F} \tag{4-18}$$

$$\Delta V_x = V_{x,step} - V^* \quad and \quad \Delta V_o = \frac{\Delta V_x}{f} \tag{4-19}$$

Combining Equations (4-18) and (4-19), the slewing time is given by

$$t_{slew} = \frac{\Delta V_o}{SR} = \frac{\Delta V_x C_{Leff}}{f I_{SS}} \tag{4-20}$$

The linear settling time period starts when $V_x < V^*$ and is given by

$$\frac{t_{s,lin}}{\tau} = -\ln(\varepsilon \frac{CV_{t,step}f}{V^*}) \tag{4-21}$$

4.2.5 Non-ideality of Switches

In SC circuits, switches are extensively utilized, which are not prefect in reality. The non-idealities originate from the switch have finite on-resistance, clock feedthrough and charge injection.

While in the previous section the resistance was assumed to have a fixed value, practically there are still signal-dependent events occurring even with the proper sizing ratio. Due to the body effect, the threshold voltage of the transistor shows nonlinear input voltage dependence, resulting in harmonic distortion [85]. This can be remedied by the boost-trapped switch as mentioned in Chapter 2.

In reality, high on-resistance in MOS switches can slow down the circuit speed and also make the feedback system unstable if the MOS switch is in the feedback loop, as shown in Fig. 4-11. The on-resistance from the switch will increase the delay and therefore increase the phase shift and cause a reduction in the phase margin. To avoid this, we have to reduce the value of the on-resistance of the switch. However if a switch of large cross-section is used to reduce the on-resistance, it will add a significant amount of drain/source junction parasitic capacitance at the output, reducing the overall bandwidth, which is a tradeoff as we mentioned in Chapter 2. A boot-strapped switch can be applied to lower the on-resistance of the switches while keeping the devices cross-section small.

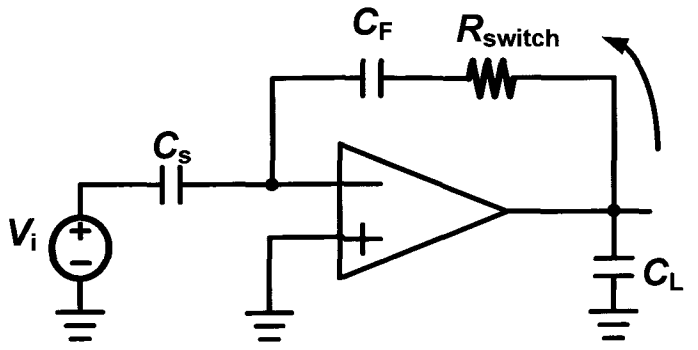


Figure 4-11 SC Circuit with On-Resistance Switches

4.2.6 Charge Injection

As mentioned in Chapter 2, when the switch turns on and off, the clock feedthrough and charge injection will greatly affect the switch's circuit performance. As with the SC circuit of Fig. 4-2, by proper timing control, the input-dependent charge injection can be eliminated. For simplicity, the parasitic capacitor C_P is neglected in this analysis. In Fig. 4-2, during the sampling phase, switches ϕ_1 and ϕ_{1d} are closed and the input is sampled and stored on C_S. After the sampling phase, switch ϕ_1 opens before switch ϕ_{1d}, and a constant charge injection Δq_2 is injected as shown in Fig. 4-12.

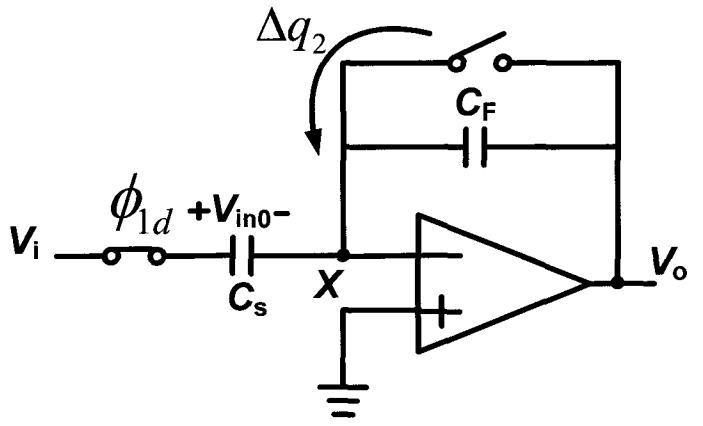


Figure 4-12 Effect of Charge Injection by switch ϕ_1

After switch ϕ_1 is open, the charge on the right plate of C_S is approximately equal to $-V_{in0}C_S$. Δq_2 is a constant charge and can be eliminated by differential operation. Switch ϕ_{1d} opens slightly later than switch ϕ_1 as shown in Fig.4-13.

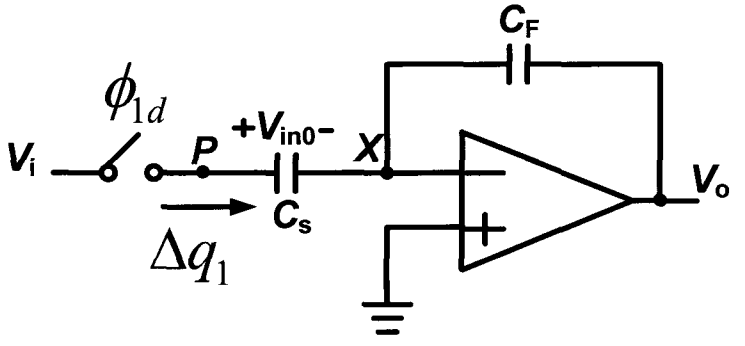


Figure 4-13 Effect of Charge Injection by ϕ_{1d}

As illustrated in Fig.4-13, the charge injected by switch ϕ_{1d}, Δq_1, causes a change in the voltage at node P by approximately $\Delta V_P = \Delta q_1 / C_S$, causing the output voltage to change by $-\Delta q_1 / C_F$. After switch ϕ_2 closes, node P is connected to the

ground as shown in Fig. 4-14, leading to the creation of the injected change Δq_3

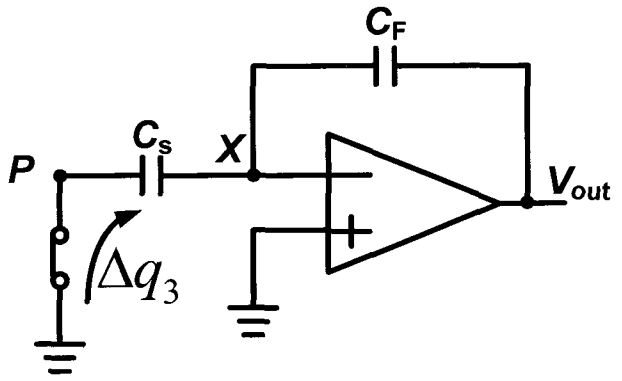


Figure 4-14 Effect of Charge Injection by ϕ_2

The charge Δq_3 is also a constant charge and can be cancelled by the differential operation. The total effect of charge injection on the output transition is shown in Fig. 4-15.

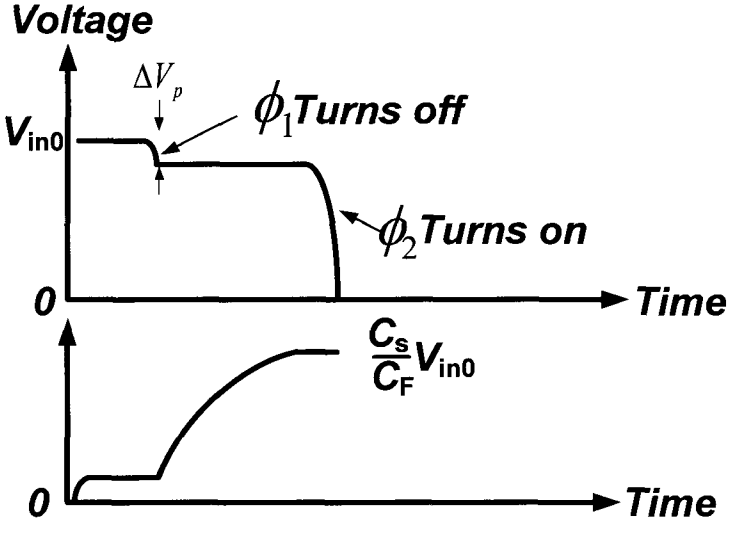


Figure 4-15 Total Charge Injection Effect at Output Transition

Since the output voltage of interest is captured after node P is connected to

ground, the voltage stored on C_S is nearly zero and the charge is transferred and stored on C_F. Therefore, the output voltage is approximately equal to $V_{in0}\frac{C_S}{C_F}$, and the charge injection by switch ϕ_1 does not affect the final output regardless of the intermediate voltage at node P. The charge injection analysis is more complex if the parasitic capacitor C_P is included [86].

4.3 Analog Comparator

A comparator compares the incoming input signal voltage to a reference voltage. The simplest way to implement a high speed comparator is to use simple regenerative cross-coupled MOSFET (strong arm) architecture to accomplish the comparison of two signals, as shown in Fig.4-16. Usually a pre-amp is implemented before the comparator to reduce the kick-back effect. The strong-arm comparator has an especially big kick-back , so that the eye diagram opening at the input of the comparator is large. The preamp stage is usually implemented by a differential pair with a source coupled current source as shown in Fig. 4-16. The preamp is usually in the open-loop configuration.

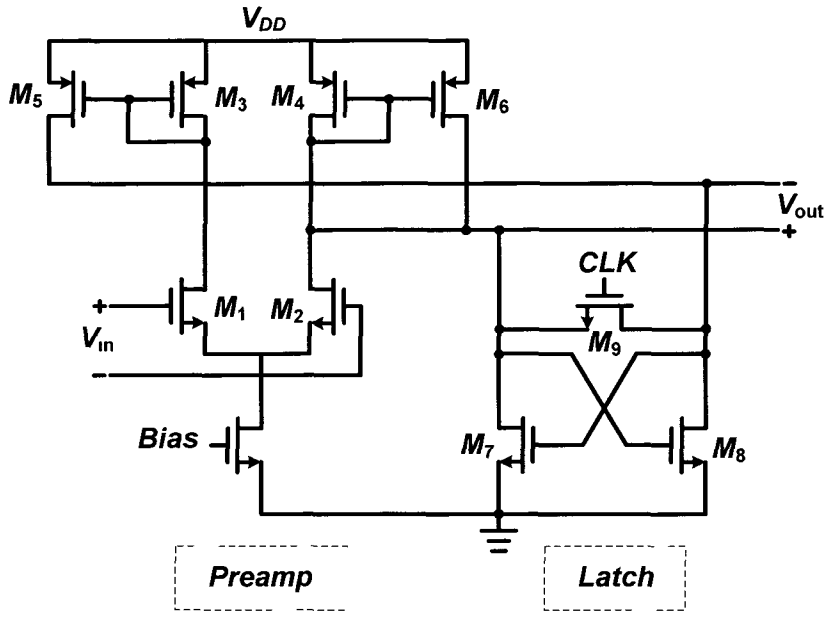


Figure 4-16 Analog Comparators

As shown in Fig. 4-16, the output nodes are equalized during comparator reset phase, and the output is regenerated and amplified to the digital logic level for subsequent processing as shown in Fig. 4-17.

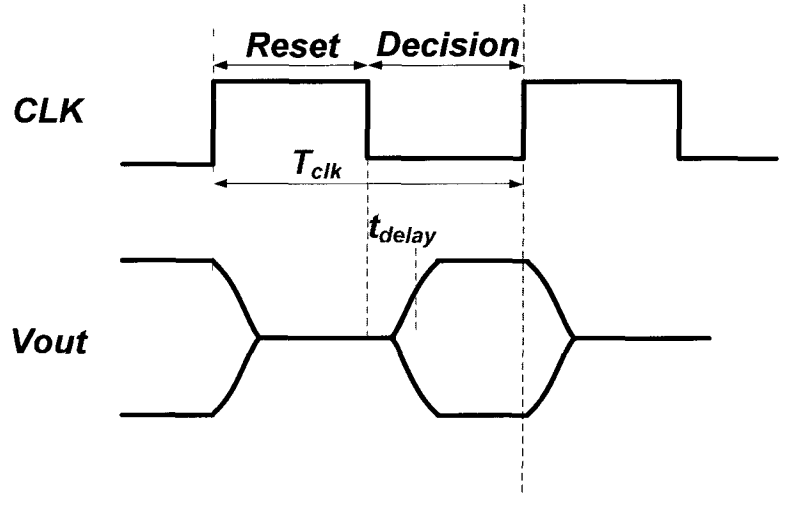


Figure 4-17 Analog Comparator Operation

The regenerative delay is given by [3]

$$\tau_{delay} \approx \frac{C}{g_m} \ln(A_v \frac{V_o}{V_{in}}) \tag{4-22}$$

where C is the parasitic capacitance at the output node, g_m is the transconductance of the MOSFET, A_v is the gain of the pre-amplifier, V_{in} is the input signal and V_o is the output signal. To reduce the τ_{delay}, we can (1) reduce the parasitic capacitance value, (2) increase the transconductance , or (3) reduce A_v. If the current source is fixed, C/g_m is approximately constant for various widths of the MOSFET. Applying (1) and (2) above are effective way to reduce τ_{delay}. Reducing A_v results in a large input referred noise. Therefore, the best way to reduce τ_{delay} is to use a large input voltage difference, as shown in Fig. 4-18.

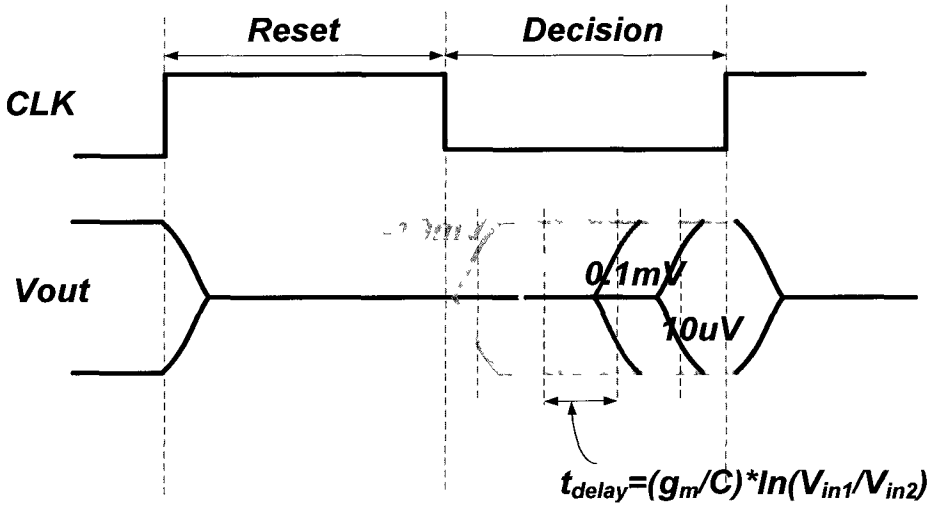


Figure 4-18 Comparator Output with Different Input Differences

Another major factor which affects the accuracy of the comparator is the offset voltage caused by mismatches resulting from process variations. For the circuit in Fig.

4-16, when the input signal is sampled on output nodes, any mismatch between the right and left half circuits will cause an offset voltage during its regenerative process. This includes charge injection mismatches from input switches, threshold and (W/L) mismatches between cross-coupled devices. The offset voltage can be easily as high as 100 mV. Due to the large offset present in this circuit, preamp stages are again required because the source coupled pair exhibits lower offset voltages. With careful layout (e.g. common-centroid) of the input stage, the preamp stage can have the offset down to ~ 1 – 10 mV, and about 10 bit resolution can be achieved without calibration [9]. For example, when the latch offset is 100mV and the preamp DC gain is 10, the preamp input-referred offset is 10 mv. The overall input-referred offset with preamp is $\sqrt{(10mV)^2 + (100mV/10)^2} = 14mV$, which is a factor of nine reduction compared with the case without the preamp. There is an extra 3 bits resolution.

For higher resolution, however, the use of a preamp must be combined with offset nulling techniques to reduce the offset below 1 mV. Fig. 4-19 shows a switched capacitor comparator widely used in ADC design.

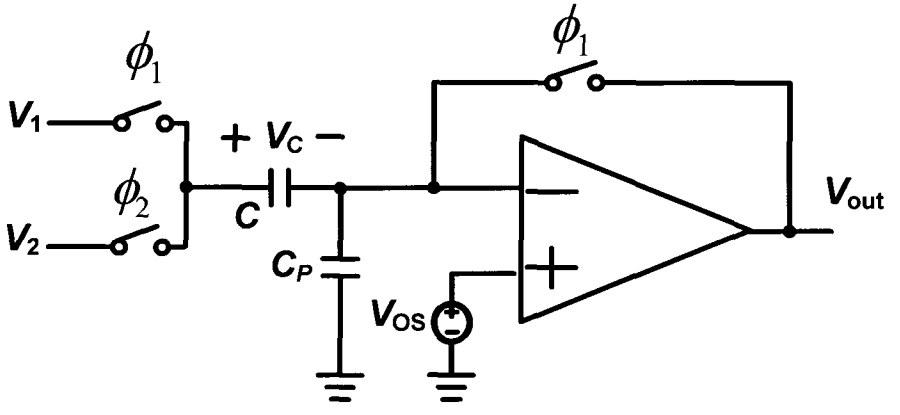


Figure 4-19 A Switched Capacitor Comparators

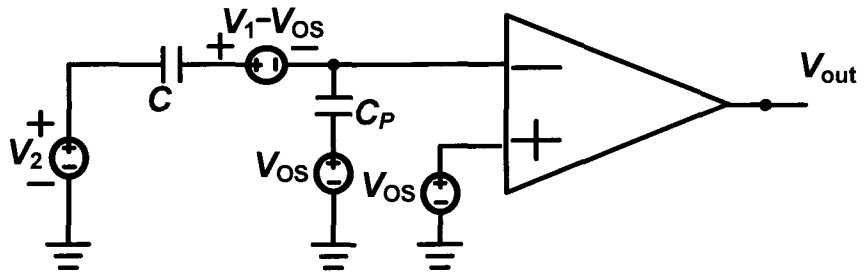


Figure 4-20 Equivalent Circuit When the ϕ_2 Switches are closed

As shown in Fig. 4-19 and Fig. 4-20, the offset cancellation is accomplished in two phases.

During the ϕ_1 phase, the V_1 input is sampled and the DC offset voltage is auto-zeroed.

$$\begin{aligned} V_C(\phi_1) &= V_1 - V_{OS}. \\ V_{CP}(\phi_1) &= V_{OS} \end{aligned} \tag{4-23}$$

During the ϕ_2 phase, the stored dc offset is cancelled.

$$\begin{aligned} V_{out}(\phi_2) &= -A\left[\frac{V_2 C}{C+C_P} - \frac{(V_1 - V_{OS})C}{C+C_P} + \frac{V_{OS}C_P}{C+C_P}\right] + AV_{OS} \\ &= -A\left[(V_2 - V_1)\frac{C}{C+C_P} - V_{OS}\left(\frac{C}{C+C_P} + \frac{C_P}{C+C_P}\right)\right] + AV_{OS} \\ &= -A(V_2 - V_1)\frac{C}{C+C_P} \\ &\approx A(V_1 - V_2) \ \textit{if } C_P \textit{ is smaller than } C \end{aligned} \tag{4-24}$$

However, a high precision quantization function requires larger power compared to the dynamic switching power of the cross-coupled latch, because amplification and offset error cancellation require extra complex circuits which usually consume static

power. As a result, ADC architectures which require many precision comparators for high resolution require large static power consumption.

4.4 Time-domain Comparator

With an ultra-low supply voltage, analog comparator design becomes challenging because analog design is sensitive to process variations. This situation becomes worse when the current varies exponentially in response to the V_{th} mismatch. In this dissertation a time-domain digital comparator is introduced to convert the input and reference voltage into pulses and to compare their phases. The time-domain comparator achieves low power consumption with excellent scalability. The design is no longer bounded by the poor analog properties of deep submicron devices. Traditional time-domain comparators often suffer from limited input signal amplitude [87]. The lower bound of the comparator input signal is limited by the MOSFET threshold voltage. The input signal swing is then constrained between V_{th} and V_{dd} [87]. Under low supply voltages, large input signal swings are essential to achieve high signal-to-noise ratios (SNRs). Our proposed rail-to-rail time domain comparator is shown in Fig. 4-21. The comparator consists of two voltage-to-time converters and a flip-flop. The voltage-to-time converters are used to translate the input and reference voltages into pulses with corresponding time durations. At the same time, the flip-flop is used as a phase detector to measure the timing difference between the clock and the data input. Compared with [10], our design has an auxiliary discharging path besides the main discharging path as labeled in Fig. 4-21. This auxiliary path ensures the rail-to-rail input signal swing.

As shown in Fig. 4-22, when the clock line ϕ is low, transistors M_3 and M_{23} are on, and capacitors C_1 and C_2 are charged to V_{dd}, while nodes A and B are discharged. At the same time, M_5 and M_{25} on the auxiliary path are off and there is no static power consumption. As shown in Fig. 4-23, when the clock line ϕ is high, both paths are starting to discharge the capacitors C_1 and C_2. The dual path architecture guarantees that at least one path is working no matter what the input value is. If V_{in} is less than V_{th}, transistors M_1 and M_{21} are off and transistors M_6 and M_{26} are on. The input signal will propagate through the auxiliary path to control the current mirrors to discharge the capacitors. When V_{in} is equal to V_{dd}, I_{M1} achieves its maximum value and also the gate voltage of M_4 goes to its higher extreme, leading to maximum discharge current. When V_{in} is equal to zero, I_{M1} is off, and the gate voltage of M_4 goes to its lower bound, which generates the lowest discharge current. Therefore the discharge current is approximately proportional to the input voltage. The discharging current follows the input voltage monotonically as shown in Fig. 4-24. The object here is achieving the minimal timing difference the comparator can detect, which sets the limit for the 1 LSB value. The timing resolution is mainly limited by the bandwidth of the flip-flop and the DAC. In this work, the resolution is determined by the set-up and hold time of the flip-flop.

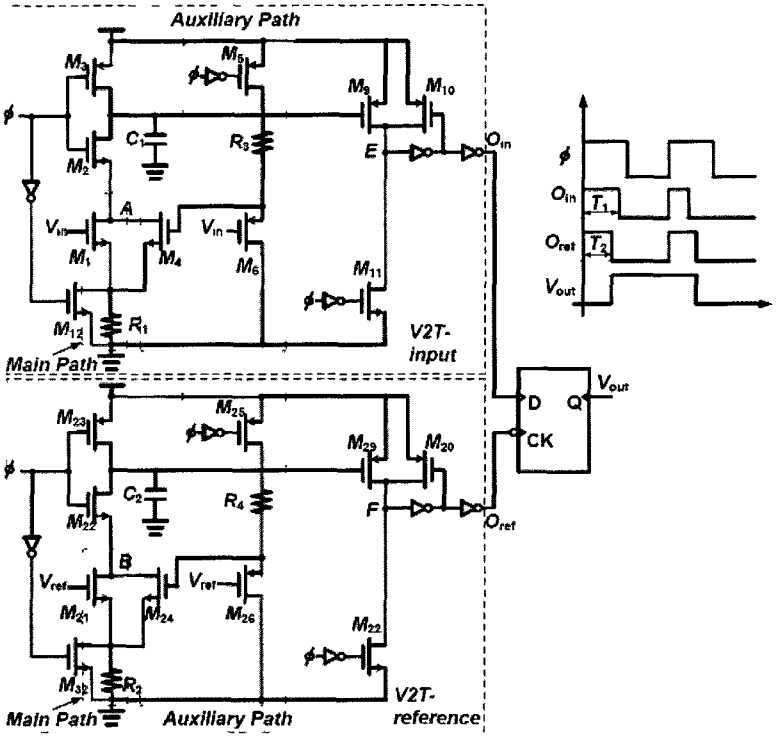


Figure 4-21 Proposed Time Domain Comparators

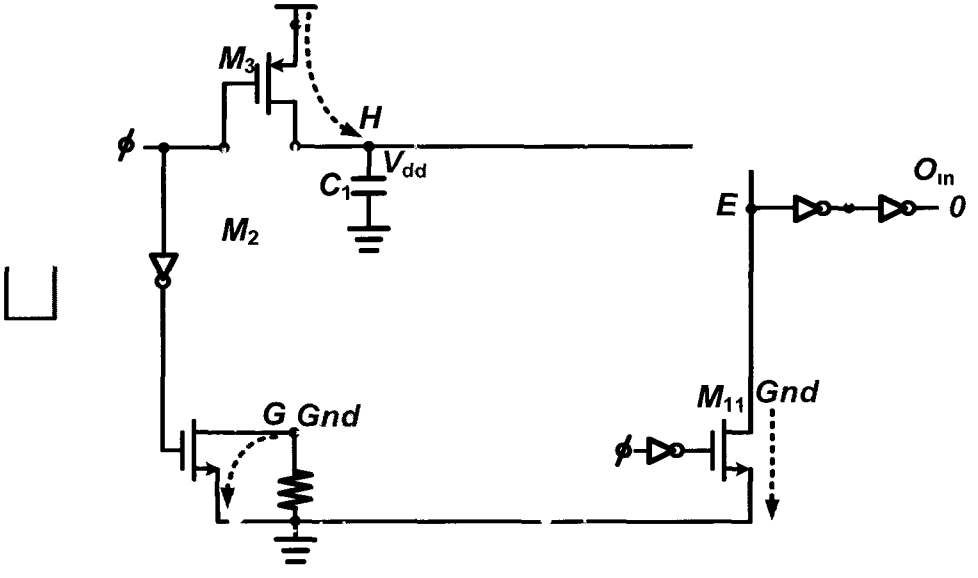


Figure 4-22 Voltage to Time Converter when Clock is Low

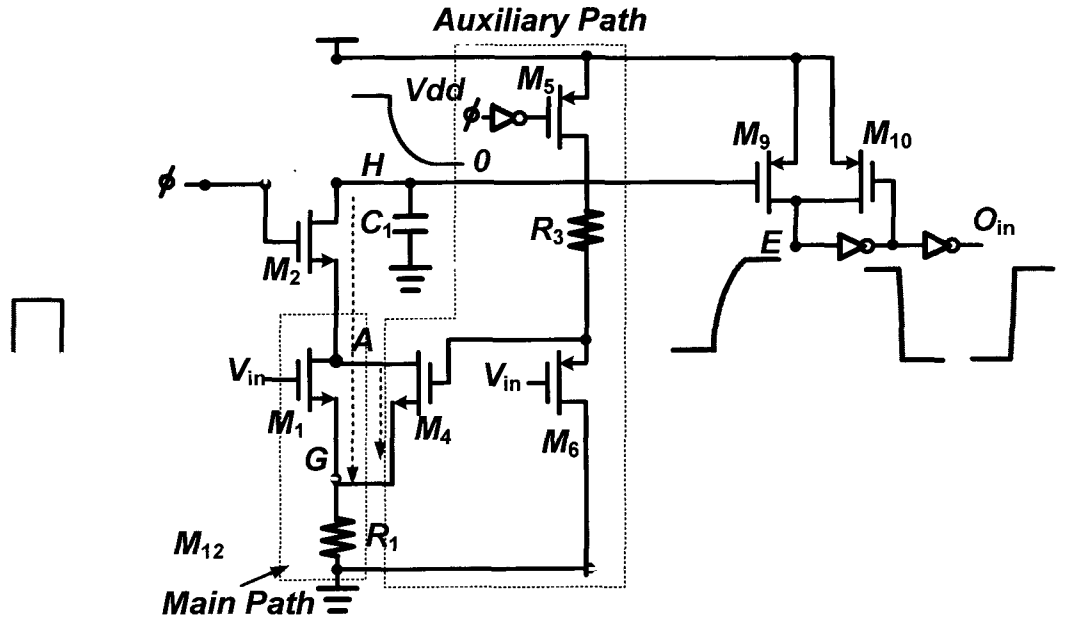


Figure 4-23 Voltage-to-Time Converter when Clock is High

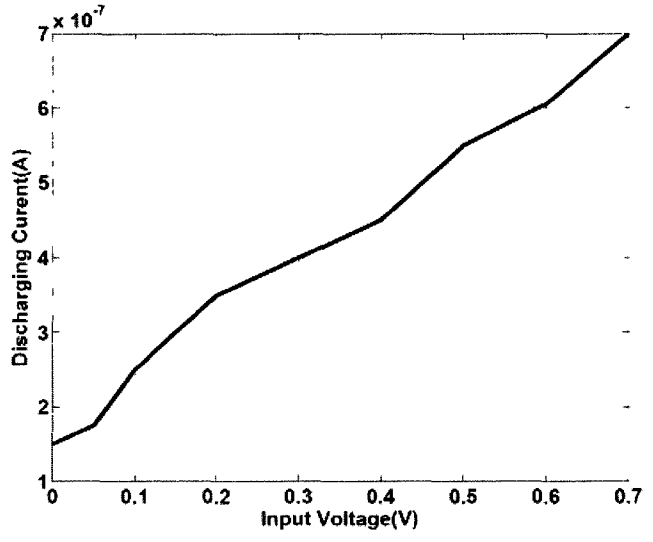


Figure 4-24 Discharging Current versus Input Voltage

In the design of Fig. 4-21 through Fig. 4-23, M_6 and M_{26} are the inputs to the PMOS source followers. MOS devices often suffer from the body effect but this can be alleviated in the FDSOI technology [88]. When the voltages across capacitors C_1 and C_2 are low enough to open transistors M_9 and M_{29}, the voltage of nodes E and

F start to rise. A pseudo-NMOS pull-up device is used here to speed up the low-to-high transition, generating two pulses with durations T_1 and T_2. The two pulses are then applied to the flip-flop inputs. The flip-flop setup time and hold time, the minimum allowed delay between the clock and the input, guarantee a reliable output value. The resolution of the comparator is determined by the *KT/C* noise where K is Boltzmann's constant, T is the absolute temperature and C is the load capacitor. ΔT (the maximum of T_{setup} and T_{hold}) is the flip-flop time margin, and the input referred noise. The error voltage due to the limited ΔT is given by:

$$\Delta V_{in} = \frac{\Delta T (V_{in} - V_{gs,m1})^2}{R_1 C_1 \Delta V_{out}} \tag{4-25}$$

where ΔV_{out} is the voltage drop across the capacitor. The input referred noise is given by:

$$V_{in,t}^2 = (\frac{\Delta V_{out}}{V_{in} - V_{gs,m1}})^2 V_{in,m3}^2 + V_{in,m1}^2 + V_{in,m6}^2 + (4KTR_3 + 4KT\frac{1}{g_{m4}}) / (g_{m6}R_3)^2 \tag{4-26}$$

CHAPTER 5

LOW POWER PIPELINE ADC DESIGN

In this chapter, a power efficient 1.5bit/stage multiplying digital to analog converter (MDAC) is presented. The proposed MDAC architecture, applicable to multi-stage pipelined analog-to-digital converters (ADCs), eliminates the feedback penalty resulting from operational transconductance amplifier (OTA) based feedback circuit. The proposed MDAC technique takes advantage of the low power architecture inherent in popular 1.5 bit per stage pipeline ADCs. In this chapter, the structure and operation of a typical pipelined ADC are first introduced. The details of the building block designs are described. The design issues critical to the function as well as performance are also discussed. The effectiveness of the proposed MDAC technique is demonstrated in simulation as well as experiment.

5.1 Design Specifications

In this project, the goal was to implement a 200 MHz sampling rate, 10 Bit pipeline ADC. The primary concern for this project was to find a new architecture which reduces the power consumption resulting from the use of the OTA.

The proposed 10-bit pipeline ADC consists of nine stages. Each stage has a resolution of 1.5 bits except that Stage 9 has a resolution of 2 bits. A front-end sample and hold stage is implemented as shown in Fig. 5-1. The supply voltage for this pipeline ADC is 1.2V and the differential input range is 1.2V.

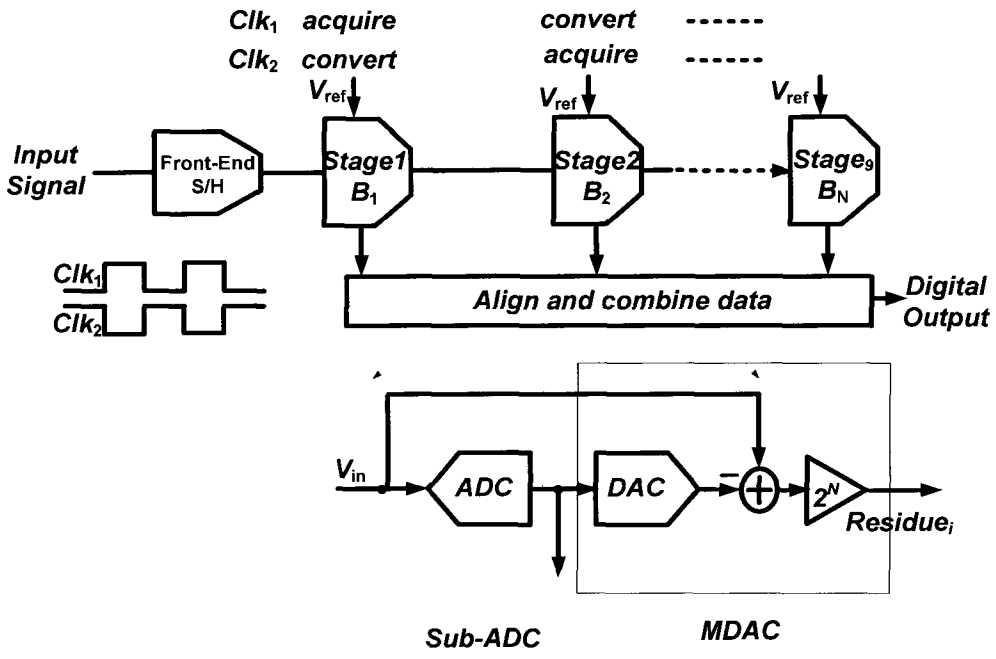


Figure 5-1 Pipeline Architecture

Before exploration of the practical design of a high-performance pipelined ADC, the specification for the desired pipeline ADC was developed here.

5.1.1 Sampling Capacitor

To guarantee that the noise error doesn't degrade the ADC resolution accuracy, the sampling capacitor in the sampling-and-hold amplifier was chosen to make sure that the KT/C noise power was much less than the quantization noise power. In the worst case, for a 10bit resolution, given the input range is full swing (1.2V), the minimum sample capacitance is given by,

$$C \geq 12K_B T\left(\frac{2^B - 1}{V_{FS}}\right)^2 \tag{5-1}$$

where $B = 10$ and $V_{FS} = 1.2V$. The value of sampling capacitor was chosen to be 1 pF.

5.1.2 Switch On-resistance

The non-zero on-resistance of the sampling switch will degrade the circuit bandwidth. To make sure that the bandwidth was large enough for a 200 MHz sampling rate ADC, the on-resistance of the switch needed to meet the requirement mentioned in Chapter 3. For the worst case, the on-resistance is given by

$$R << \frac{1}{2Cf_s} \frac{1}{\ln(2^B - 1)} \tag{5-2}$$

If we let $f_s = 200$ MHz, $C = 1$ pF and $B = 10$ bit, the resistance value is 178 Ω.

5.1.3 Clock Jitter Tolerance

As mentioned in Chapter 3, sampling jitter adds an error voltage to the output. If the error voltage exceeds the tolerance, it will degrade the ADC performance. To maintain ADC accuracy, this error voltage should be smaller than half of the least significant bit (LSB). The clock jitter should be smaller than the right side of Equation (5-3).

$$d_t << \frac{1}{2^B * \pi * f_s} \tag{5-3}$$

For the given speed (200 MHz) and resolution (10 bit), the clock jitter should be less than 1.6 ps.

5.1.4 OTA Gain Requirement

As mentioned in Chapter 4, in reality the OTA gain is finite – leading to an error into the charge balance equations when the OTA is employed in a feedback system.

The OTA gain must be made sufficiently large to minimize this finite gain error. The gain error ε is given by

$$\varepsilon < \frac{1}{A_v f} \tag{5-4}$$

where f is the feedback factor and A_V is the OTA's open loop voltage gain. In our case, for a 10 bit pipeline ADC, if the requirement for an error due to finite OTA gain is to be less than $1/4$ LSB, then 1/(4x1024)=1/(4096), and with $f = 1$, it follows that A_V > 4096, or A_V >72 dB. Fig. 5-2 illustrates the variation of relative error versus OTA gain.

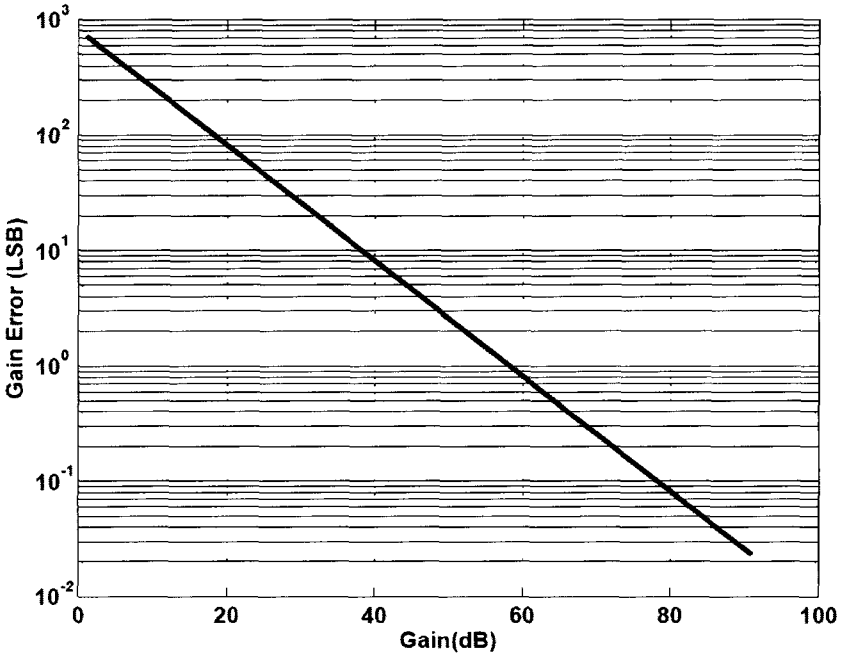


Figure 5-2 Gain Error Variation with OTA Gain with $f = 1$

Attaining 72 dB of DC gain while maintaining a reasonable bandwidth is nearly impossible with a simple single stage configuration (e.g, a differential pair) for sub-

micron technologies (for example, 90 nm CMOS technology in our design). Thus two-stage or gain-boosted configurations are applied to 10-bit pipeline ADCs.

5.1.5 OTA Bandwidth Requirement

Switched capacitor circuits suffer from the finite OTA bandwidth because of the finite time for the circuit to settle down to its final value. Thus to ensure a minimum settling accuracy, an certain OTA bandwidth must be considered. If the OTA is modeled as a first order system and is put into the feedback system as shown in Fig. 4-2. The OTA transfer function near the unity gain frequency is given by:

$$\begin{aligned} A(s) &= \frac{A_v}{1+s/\omega_{3dB}} \\ &\approx \frac{A_v\omega_{3dB}}{s} = \frac{\omega_{ta}}{s} \end{aligned} \tag{5-5}$$

where ω_{ta} is frequency near unity gain, A_V is OTA's DC gain, ω_{3dB} is OTA's bandwidth and ω_{ta} is OTA's unity gain frequency. If an OTA is employed in a feedback circuit as shown in Fig.4-2 and a unit step is applied to the input, the feedback circuit transfer function during the integration phase is calculated by

$$\begin{aligned} H_{CL}(s) &= \frac{1}{s}\frac{A(s)}{1+A(s)*f} \\ &\approx \frac{1}{s}\frac{\frac{\omega_{ta}}{s}}{1+\frac{\omega_{ta}}{s}*f} \\ &\approx \frac{1}{s}\frac{1}{f}\left[\frac{1}{1+\frac{s}{\omega_{ta}f}}\right] \end{aligned} \tag{5-6}$$

The time domain output is given by

$$h_{step}(t) = \frac{1}{f}(1 - e^{-\frac{\tau}{b}}) \tag{5-7}$$

where $\tau = \frac{1}{\omega_{ta} f}$, the slew rate is neglected, f is the feedback factor, and b is the settling accuracy in bits. The settling time for the circuit to settle is given by

$$t_{settling} = b(\frac{1}{\omega_{ta} f}) \ln 2 \tag{5-8}$$

Since the available time $t_{settling}$ to settle is half the clock period, $t = \frac{1}{2f_s}$, implying that the close loop bandwidth requirement is given by,

$$f_{ta} = b\frac{f_s \ln 2}{\pi f} \tag{5-9}$$

In our case, for a 200 MHz 10 bit pipeline ADC, the requirement for settling must to be less than $1/4$ LSB. If b is set at 12, then the required for the unity gain bandwidth for the OTA is around 500 MHz. The desired unity gain frequency is much larger than the sampling frequency needed to obtain high accuracy settling. Since the MDAC OTA must drive large capacitive loads (to minimize thermal noise), OTA consumes a large amount of power. As such, the power consumption of an OTA in a pipeline ADC often consumes 60-80% of the total ADC power.

5.1.6 Dynamic Range

The switched capacitor gain stage used in this project is illustrated in Fig. 5-18 and Fig. 5-19. The input dynamic range DR_{input} during the sampling phase is given by

$$DR_{input} = \frac{(1/2)(V_{signal}/2)^2}{V_{noise}^2} \tag{5-10}$$

In this project, the input is 600 mV, $V_{noise}^2 = KT/C_S$, and the desired dynamic range is 70 dB. Taking all the parameters into account, the value of C_S in gain stage is approximately 1 pF. Also the output dynamic range during the transfer phase is given by

$$\begin{aligned} DR_{Output} &= \frac{(1/2)(V_{OutSwing}/2)^2}{V_{noise,out}^2} \\ V_{noise,out}^2 &= \frac{KT}{C_{Leff}}\frac{NF}{f} \\ C_{Leff} &= C_L + (1-f)C_F \end{aligned} \tag{5-11}$$

where NF is the OTA input referred noise in Fig. 5-12 and f is the feedback factor. The output swing is 600 mV and f is 0.8 in our project. Taking all the parameters into account, the value of C_S in gain stage is approximately $1.5pF$. Since the value of C_S and C_F should be the same to get a gain by two function in our project, C_S and C_F was chose to be $1.5pF$.

Table 5-1 summarizes the component requirement for a 200 MHz 10bit pipeline ADC.

	Requirements
Front-end S/H sampling Capacitor	Large than 1 pF
Switch on-resistance	Less than178 Ohm
Clock jitter tolerance	Less than 1.6 ps
OTA gain	Larger than 72 dB
OTA bandwidth	Larger than 500 Mhz
C_S in gain stage	Larger than 1.5 pF
C_F in gain stage	Larger than 1.5 pF

Table 5-1 Component requirement for 200Mhz 10Bit Pipeline ADC

5.2 Input Sample and Hold Circuit

An on-chip sample-and-hold (S/H) circuit at the front of the pipeline stages is indicated in Fig.5-3. This front-end S/H circuit isolates the pipeline ADC with its driving circuit. As a result, the driver circuit suffers less kick-back noise from the comparators in the pipeline ADC. More importantly, the S/H circuit is used to keep the sampled input signal constant during the holding phase which can eliminate clock skew and jitter. The design of front-end S/H circuit is very critical to the overall performance of a pipeline ADC. The noise and linearity requirement should be the same or better than the overall noise and linearity requirement of the ADC. As a result, the S/H circuit usually takes a large die area and consumes quite amount of power. To achieve low power consumption, a pipeline ADC without S/H circuit is

proposed, as mentioned in Chapter 1. However, special effort has to be spent on the design to avoid the signal degradation issues mentioned above.

The sample and hold circuit used in this project was a capacitor flip-over S/H circuit as shown in Fig.5-3.

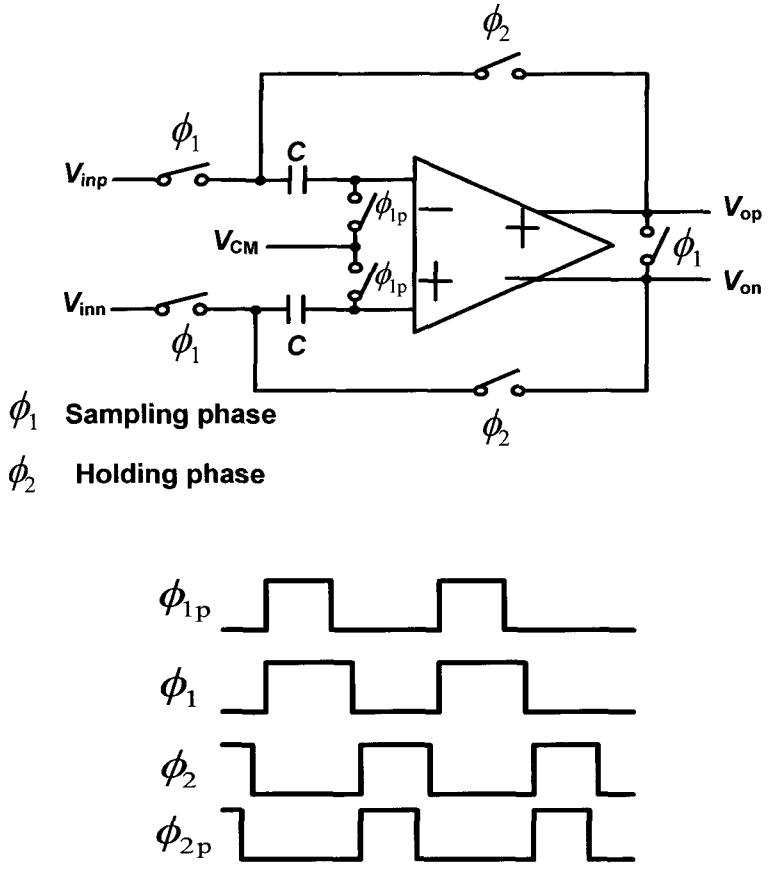


Figure 5-3 Capacitor Flip-over S/H Circuit

For the capacitor flip-over S/H architecture, there is no charge transferred, and only two differential capacitors are used. During the sampling phase, the differential input signal is sampled by the differential capacitors. During the holding phase, the input capacitors are "flipped over" by connecting their bottom plates to the output of the amplifier. The common mode and differential mode charges are both transferred

during this process. Although the amplifier's common mode feedback circuit will force the output's common mode back to the desired value, the amplifier's input common mode level will change because of the difference between the input signal's common mode level and the amplifier output's common mode level, which means the amplifier must be capable of handling large common-mode input variation. The flip-over S/H is still widely used in the state-of-the-art high-speed pipelined ADC designs because of its smaller size, lower noise, and lower power consumption. These advantages stem from the large feedback factor and lower number of capacitors. The detailed analysis can be found in [89].

The first stage's sampling linearity must therefore be better than the overall desired linearity. For a 10-bit ENOB pipeline ADC it is desirable that the linearity be at least 15 bits. This allows the noise component of the effective number of bit (ENOB) measurement to be dominant. Additionally, if the linearity requirement is met for the entire system, then the DNL and INL should also be at least 11 bits.

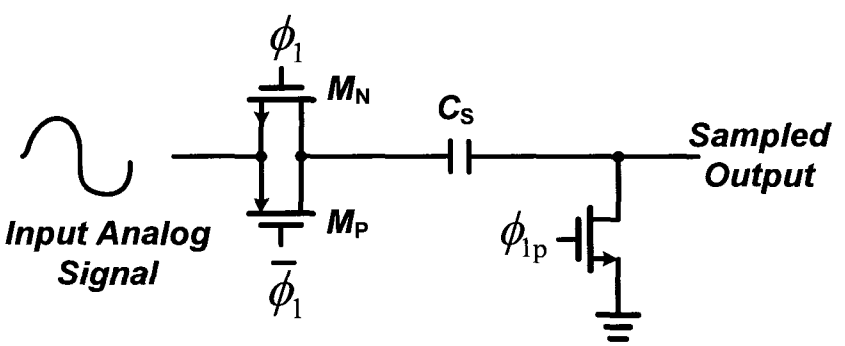


Figure 5-4 Input Sampling with MOS Switch

A common implementation of a switched-capacitor input sampling circuit is shown in Figure 5-4. The floating CMOS switch (or transmission gate) passes signals

anywhere in the range from the positive power supply to the negative power supply. This switch experiences a change in its source –to-drain resistance depended on gate-source voltage,

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{th})} \tag{5-12}$$

where $\mu_n C_{ox}$ is a device constant, W and L are the physical dimensions of the MOSFET channel, and (V_{GS} - V_{th}) is the MOSFET overdrive voltage. This signal-dependant resistance makes the sampled voltage on the input-sampling capacitor non-linear. The effect of this non-linearity can be greatly reduced if the resistance contribution from the PMOS and NMOS transistors is balanced. This improves the linearity because signals near the positive power supply experiences similar switch resistance from the CMOS switch as signals near the negative power supply. To accomplish this balance, usually the PMOS device needs to be 2 to 3 times larger than the NMOS device. Linearity achievable in the available 90 nm CMOS process with CMOS switches is on the order of 9 bits as shown in Fig. 5-5.

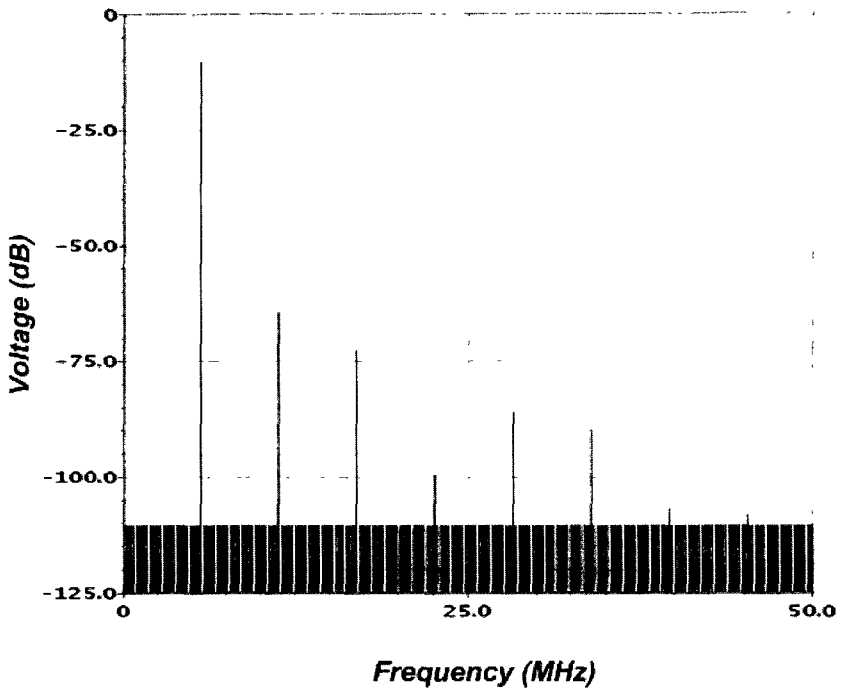


Figure 5-5 CMOS Switch Sampling Linearity

The sampling linearity can be greatly improved if the gate-source voltage is held constant for all input signals. A simple example of this would be to place a voltage source between the input (source) and gate of an NMOS switch. Ideal voltage sources are generally not within the scope of an IC design. Therefore capacitors are often used as a means to filter out the AC noise in the power supply. A sampling system incorporating a simplistic version of bootstrapping is shown in Fig.5-6.

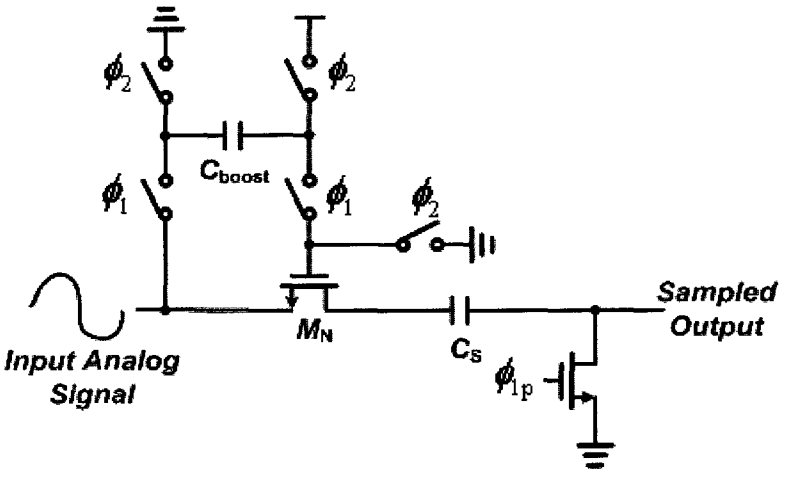


Figure 5-6 Bootstrapped NMOS Switch

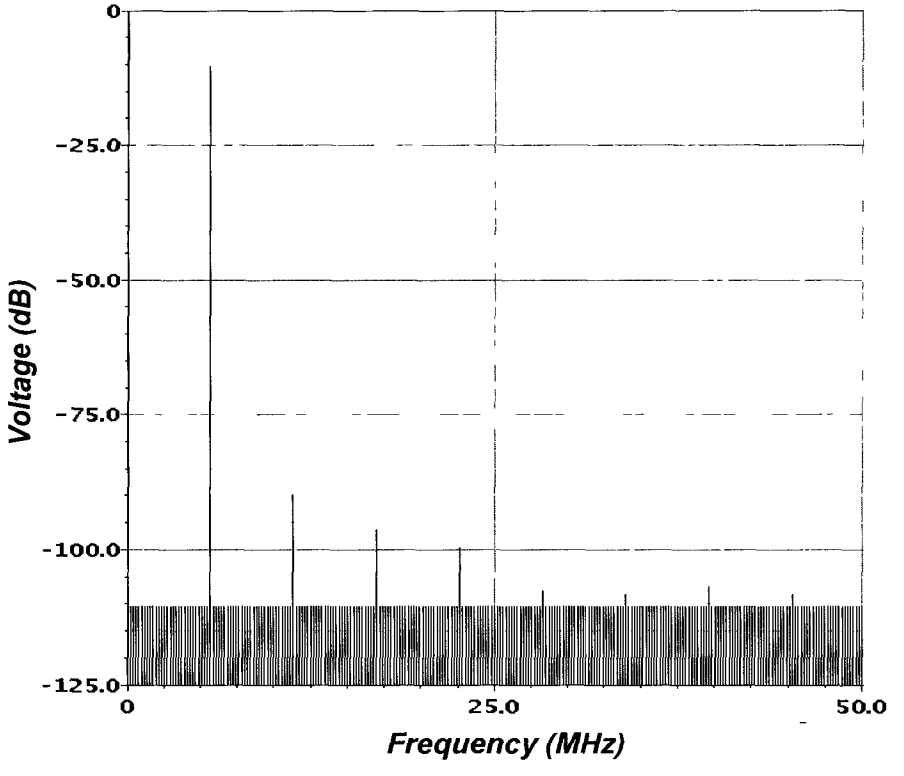


Figure 5-7 Bootstrapped NMOS switch sampling linearity

Linearity achievable with boostrapping in the available 90 nm CMOS process with CMOS switches is in the order of 11 bits (Fig. 5-7). One of the major drawbacks in bootstrapped switch circuits is that all transistors have to experience voltages greater than the power supply. For example, the switches on the gate of the NMOS switch (circled) in Fig.5-6 will experience source-bulk and drain-source voltages greater than the power supply. A popular circuit used to circumvent this problem was introduced in [90].

5.3 OTA Applied in MDAC

The first stage MDAC is the most critical circuit block to design in this system. Not only does it need to meet stringent system input and output linearity, settling, and noise requirements, but it also must deal with a rail-to-rail input and sample continuous-time signal.

The specifications that our desired OTA must meet are as follows:

1) Open Loop Gain > 10 bits (72 dB)

2) Unity gain bandwidth >500 MHz

3) Settling Time $\leq$ 2.5 ns

4) Linear Output Range =1.2 differential peak-to-peak volts.

The large output range (1.2Vp-p when using a 1.2V supply) and high-speed requirements of the system make the folded-cascode OTA a natural choice for the MDAC operational amplifier. The folded provides maximum output range while maintaining high-speed simplicity.

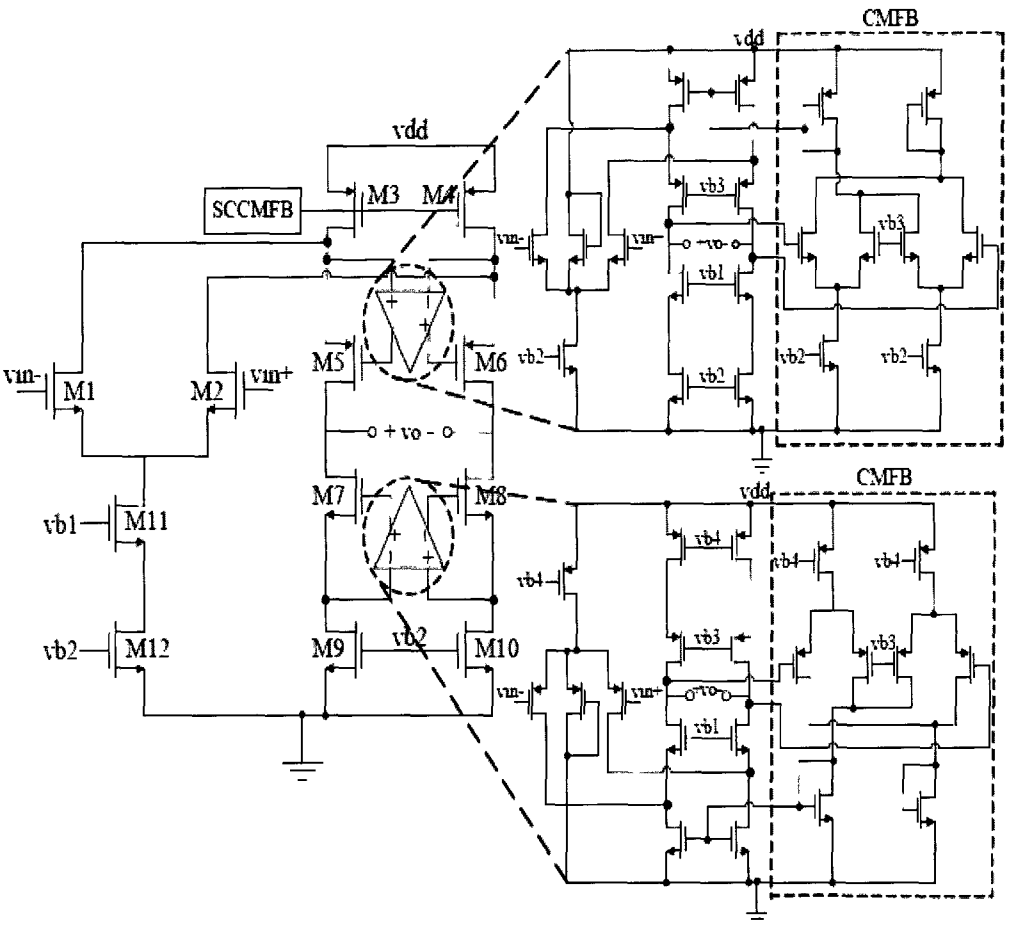


Figure 5-8 Folded-cascode with Gain Boosting

Achieving gains of greater than 70 dB in a single cascade ($(g_m r_o)^2$) stage in modern sub-micron processes is often not possible. For the output range desired, multiple stages are not an option either, because it would suffer from the speed penalties associated with compensating a two pole-system. One useful technique in a situation such as this is *gain boosting* (also known as *active cascode*) [91]. The concept behind this technique is quite simple. The idea of gain-boosting is to further increase the output impedance without adding more cascaded device as shown in Fig. 5-8.

The simple cascode circuit in Fig. 5-9 (a) has its output impedance is given by [91]

$$R_{out} = g_m * r_{o1} * r_{o2} \tag{5-11}$$

In Fig.5-9, M_1 is a source generation resistor, sensing the output current and converting it into voltage as shown in Fig. 5-9(b). As illustrated in Fig. 5-9(c), the gain-boosting idea is to drive the gate of M_2 by an amplifier to force V_x to be equal to V_b. Because V_x is regulated by an amplifier, voltage variations at the drain of M_2 affect V_x to a lesser content. With small variations at node X, the output current remains more constant, yielding higher output impedance [92], which is given by:

$$R_{out} = A_1 * g_m * r_{o1} * r_{o2} \tag{5-12}$$

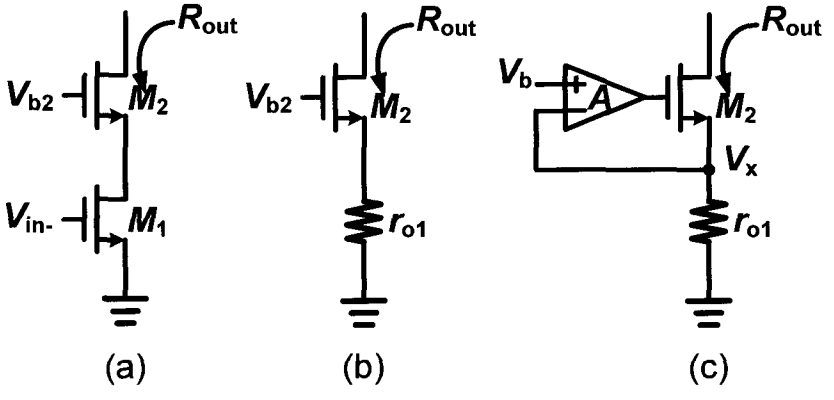


Figure 5-9 Gain-boosting Operation

Gain boosting can also be applied to a fully-differential OTA. In this case, the output common mode control of the OTA sets the bias voltage of the cascode transistor. The differential gain boosting technique shown in Fig. 5-8 was the approach taken in this work. The boost amplifiers were implemented as two opposite

polarity folded-cascode, double-cascode amplifiers (a NMOS input pair for the top amplifier (Fig. 5-8) and a PMOS input pair for the bottom amplifier). The additional cascade is possible because of the near-zero output swing required for the boost amplifiers. Moreover, minimal current was required for the boost amplifiers as the output load was only the gate capacitance of the main amplifier's cascode devices.

Returning to the folded-cascode with a gain-boosting OTA shown in Fig. 5-8, the voltage gain of the fully-differential gain-boosting amplifier is given by:

$$|A_v| \approx (g_m r_o)^4 \tag{5-13}$$

The Gain-boosting OTA voltage gain versus frequency is simulated in cadence and is shown in Fig. 5-8.

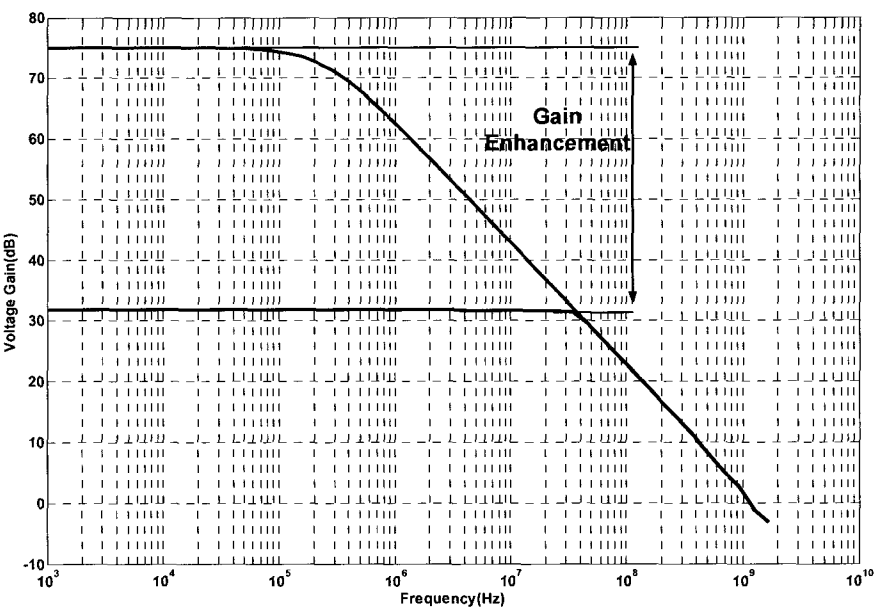
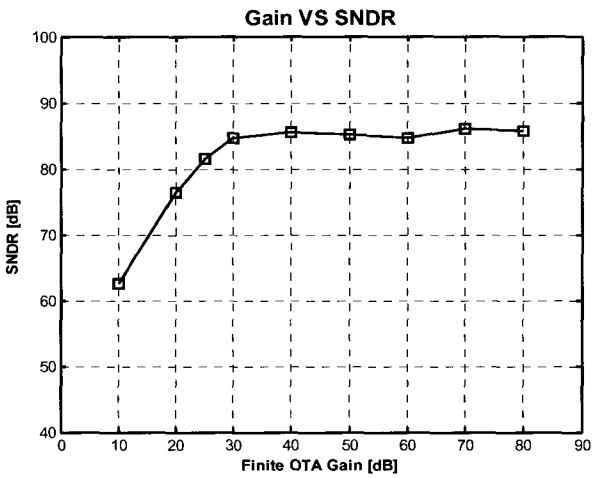


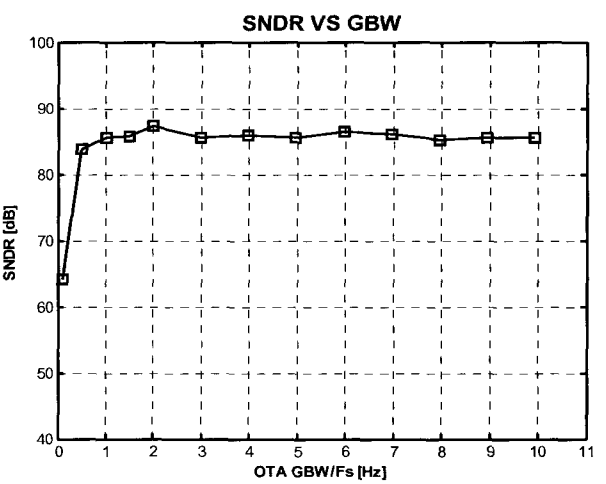
Figure 5-10 Gain-boosting OTA Voltage Gain

5.3.1 Amplifier non-ideality effect

As mentioned in Chapter 3, the non-idealities of the OTA will affect the performance of the actual implementation. As explained before, the first stage of an OTA is critical to the overall converter performance. The OTA's SNDR versus gain and The OTA's SNDR versus gain-bandwidth product are simulated in cadence and plot using Matlab as shown in Fig. 5-11.



(a) SNDR versus OTA Gain



(b) SNDR versus OTA Bandwidth/Fs

Figure 5-11 Non-idealities in SNDR versus OTA characteristics

5.3.2 Amplifier Noise

Since our ADC application was targeted to a frequency of MS/s, we ignored the flicker noise for the time being and only counted the thermal noise because of the large bandwidth requirement for faster settling. Flicker noise has an upper cut-off frequency of 100 kHz. For broadband systems it contributes only a negligible output noise power.

For a folded-cascode OTA, four current sources and two input differential pair transistors contributed most of the output noise, and the auxiliary amplifiers made small noise contributions to the output. The noise model is shown in Fig. 5-12. The cascode transistors contributed negligible noise to the output node. We also ignored the noise contribution from the gain booster OTA in the calculation below. Because the MOS transistor size and bias current in the gain booster OTA were much smaller than those in the main folded-cascode OTA. We concluded that the gain booster contributed only a small amount to the total output noise.

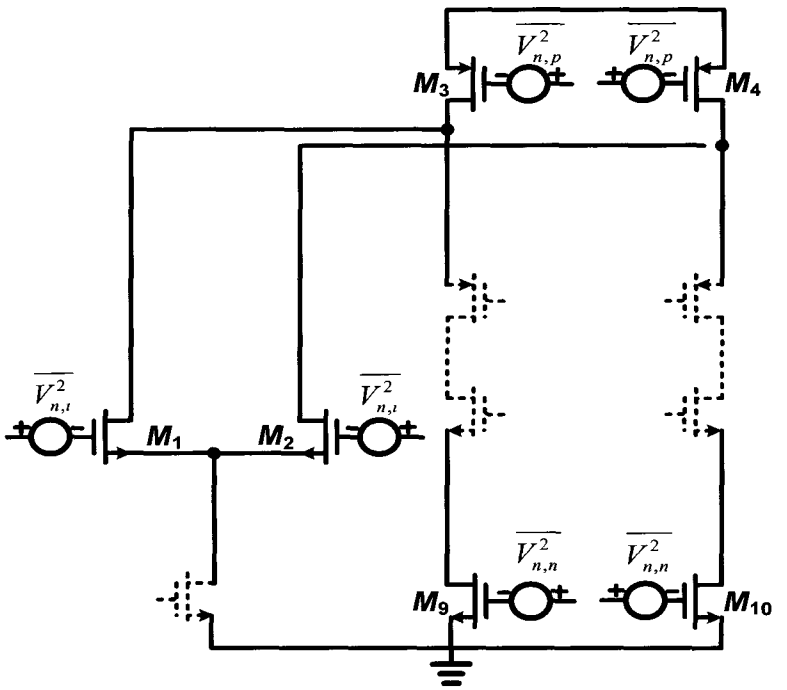


Figure 5-12 Folded-cascode Circuit for OTA Noise Calculation

To calculate the noise, we refer $\overline{V_{n,t}^2}$, $\overline{V_{n,n}^2}$, and $\overline{V_{n,p}^2}$, to the gates of the six transistors. Their values are given by:

$$\begin{aligned}\overline{V_{n,t}^2} &= 4kTr\frac{1}{g_{m1}} \\ \overline{V_{n,n}^2} &= 4kTr\frac{1}{g_{m9}} \\ \overline{V_{n,p}^2} &= 4kTr\frac{1}{g_{m3}}\end{aligned} \tag{5-14}$$

Where the coefficient r is derived to be equal to 2/3 for long-channel transistor and may need to be replaced by a larger value for submicron MOSFET. The total input referred noise is given by:

$$\overline{V_{tn,t}^2} = 2*(4kTr\frac{1}{g_{m1}} + 4kTr\frac{g_{m3}}{g_{m1}^2} + 4kTr\frac{g_{m9}}{g_{m1}^2}) \quad (5\text{-}15)$$

Since g_m is proportional to $\frac{I}{V_{dsat}}$, to reduce the input referred noise, it's good to have a small V_{dsat} for the input differential pair and a large V_{dsat} for the current source transistor. On the other hand, a small V_{dsat} for the input differential pair causes lower voltage gain, and a large V_{dsat} for the current source transistor will reduce the output swing. Therefore, there is a trade-off among noise, voltage gain and output swing.

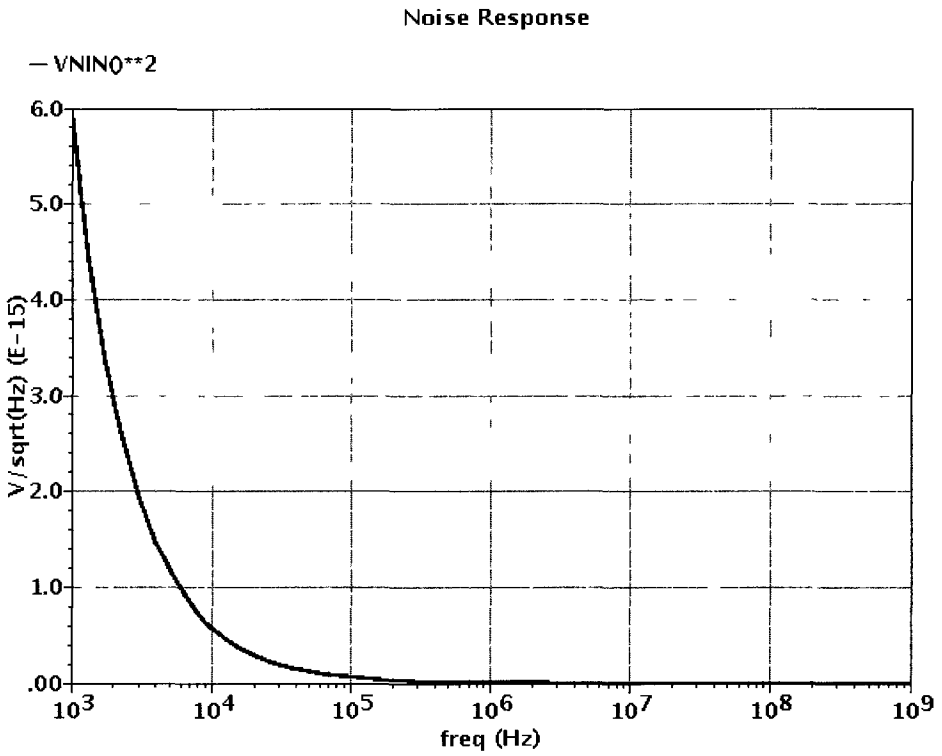


Figure 5-13 OTA Input Referred Noise

Noise simulation in SPECTRE gives 130 $\mu V - rms$ integrated noise over the entire noise band. This wide integration band is due to the sampling that will fold all noise frequencies into the $f_s/2$ frequency band.

5.4 Traditional 1.5Bit per stage MDAC

In the past 1.5 bit per stage MDAC architecture has been widely used in modern pipeline ADC design [42] [92]. Fig. 5-9 shows the details of the 1.5bit/stage circuit. It operates as follows.

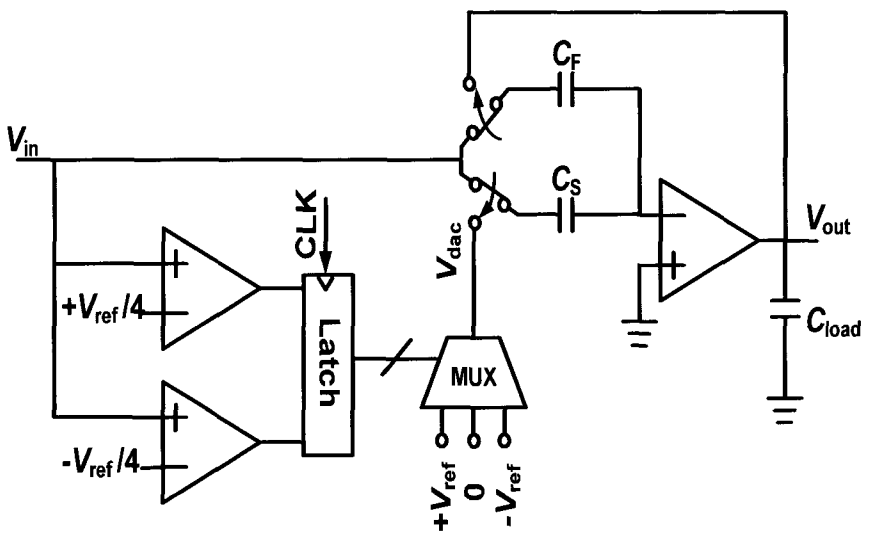


Fig.5-14 Conventional 1.5bits/stage MDAC [42]

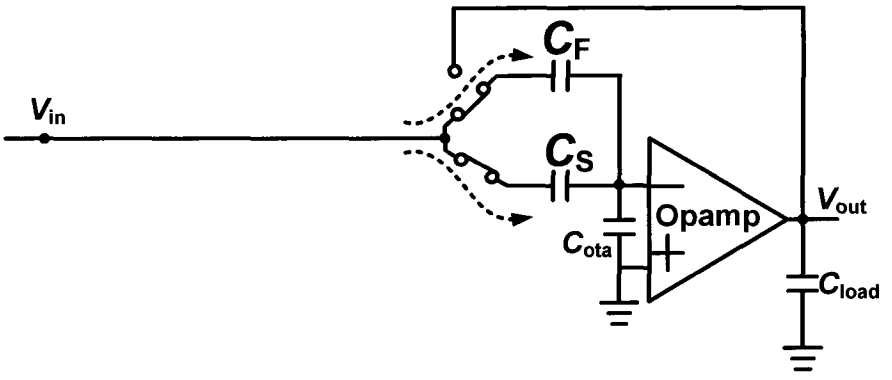


Fig.5-15 Traditional 1.5bits/stage in First Phase

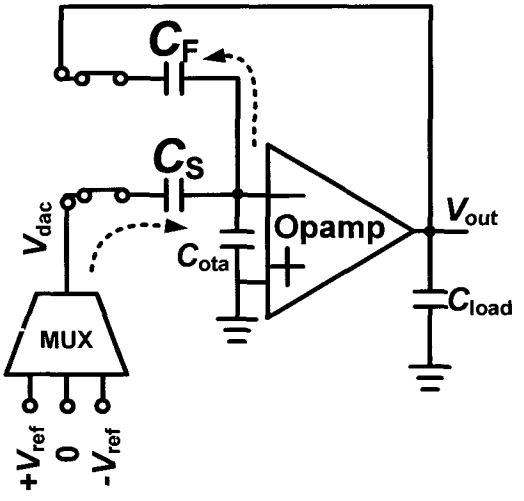


Fig.5-16 Traditional 1.5bits/stage in Second Phase

During the first phase in Fig. 5-15, the input signal V_{in} is applied to the input of the sub-ADC with thresholds at $+V_{ref}/4$ and $-V_{ref}/4$. The differential input signal can range from $+V_{ref}$ to $-V_{ref}$. Simultaneously, V_{in} is applied to the sampling capacitors

C_S and C_F. At the end of the first clock phase, V_{in} is sampled from C_S and C_F, and the output of the sub-ADC is latched.

During the second clock phase in Fig. 5-16, C_F closes a negative feedback loop around the OTA, while the top plate of C_S is switched to the DAC output. This configuration generates the stage residue at V_{out}. The output of the sub-ADC is used to select the DAC output voltage V_{dac} through an analog multiplexer, and V_{dac} is capacitively subtracted from the residue so that:

$$V_o = \begin{cases} (1+\frac{C_s}{C_f})V_{in} - \frac{C_s}{C_f}V_{ref} & if\ V_{in} > V_{ref}/4 \\ (1+\frac{C_s}{C_f})V_{in} & if\ -V_{ref}/4 \le V_{in} \le +V_{ref}/4 \\ (1+\frac{C_s}{C_f})V_{in} + \frac{C_s}{C_f}V_{ref} & if\ V_{in} < -V_{ref}/4 \end{cases} \quad (5\text{-}16)$$

The 1.5 bits/stage design with 0.5 bit redundancy can tolerate a sub-DAC error as large as Vref/8, as shown in Fig. 5-17, which will relax the pipeline ADC design. The challenge in this MDAC is the Gain-By-two design, which is used to amplify the first stage's residue by a factor of two.

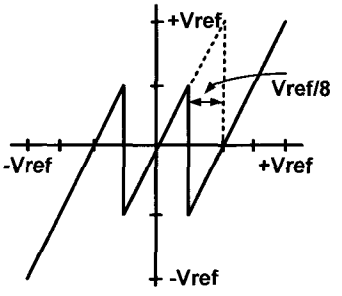


Fig.5-17 Error Tolerance in 1.5 bits Stage

The critical parameters in the MDAC design are the closed-loop bandwidth, the OTA gain, output noise, and nonlinearity. In this section, we focus on MDAC bandwidth improvement and output noise reduction. The MDAC bandwidth determines how fast the ADC can settle. In addition, it is proportional to power consumption. A significant amount of power can be saved by using higher closed-loop bandwidth. The details of the proposed MDAC will be discussed in the next section. The bandwidth of the conventional MDAC is given by:

$$BW = \frac{1}{\tau} = \frac{G_m}{(C_{load} + (1-f) * C_f)} * f \tag{5-17}$$

where $f = C_f / (C_f + C_s + C_{OTA})$, C_{OTA} is OTA input parasitic capacitance. Based on Equation (5-17), it is obvious that the feedback factor f (the ratio of the feedback capacitor to the total capacitance at the summing node) plays an important role. The output noise is given by Equation (5-18), if we neglect the OTA input-referred noise.

$$\overline{V_{on}^2} = \frac{KT}{(C_{load} + (1-f) * C_f)} * \frac{NF}{f} \tag{5-18}$$

where NF is the noise factor. This NF is calculated based on our gain-boost OTA.

5.5 Expanded Bandwidth, Reduced Noise 1.5-Bit per stage MDAC

As mentioned above, the switched capacitor circuit's bandwidth is affected by the feedback factor f. Also, the output accuracy highly depends on the matching between C_S and C_F. Equation (5-17) shows that bandwidth is proportional to G_m, where G_m is proportional to the power consumption. To achieve the desired bandwidth, the conventional MDAC will require more power consumption due to the

feedback factor penalty. To conquer these problems, we developed a novel pipeline MDAC architecture to minimize the impact of f. Our MDAC dramatically improves the settling behavior and operates much closer to the unity gain frequency of the amplifier. The novel MDAC Gain-By-Two architecture is shown in Fig.5- 18.

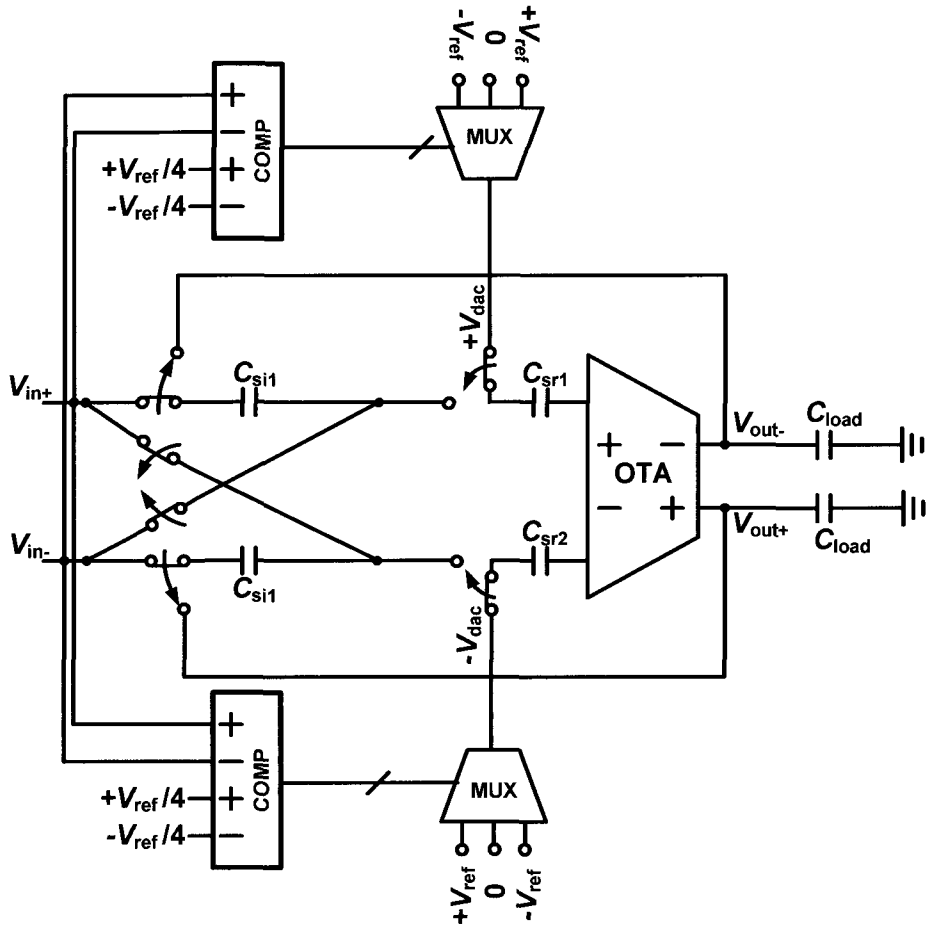


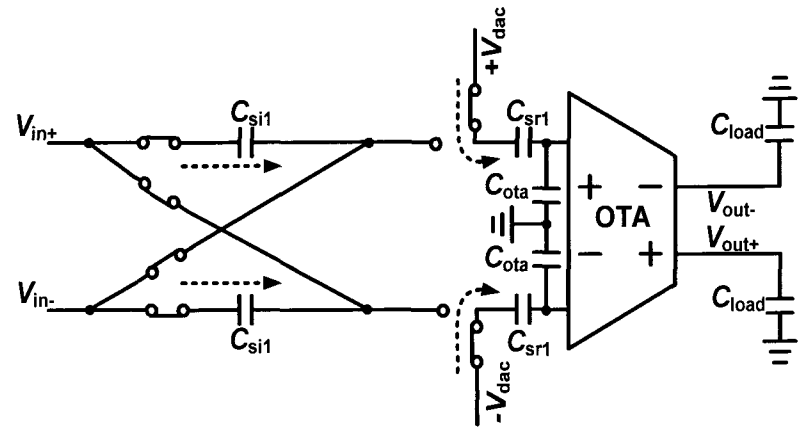
Fig.5-18 Novel MDAC Architecture

This architecture shares the comparator and analog MUX architecture with the conventional MDAC shown in Fig. 5-14. The novel architecture operates as follows. The MDAC operates in two phases as shown in Fig. 5-19: the sampling phase and the transfer phase. During the sampling phase, shown in Fig. 5-19 (a), the differential

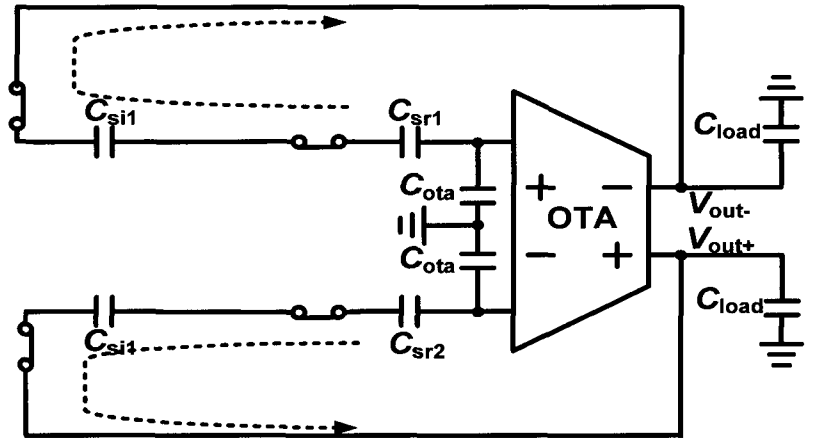
input signals V_{in+} and V_{in-} is applied to the cross-over sampling capacitors C_{s1} and C_{s2}. Then $(V_{in+} - V_{in-})$ is stored on C_{s1} and $-(V_{in+} - V_{in-})$ is stored on C_{s2}. At the same time, V_{in+} and V_{in-} will go through the comparators and MUXes to determine the corresponding $+V_{dac}$ and $-V_{dac}$ values. These two voltages will be stored on capacitors C_{sr1} and C_{sr2} separately. During the transfer phase, shown in Fig. 5-19 (b), C_{s1} and C_{s2} are serially connected together to transfer the stored voltage to the output. V_{dac} is capacitively subtracted from the residue so that,

$$V_{outd} = \begin{cases} 2V_{ind} - V_{refd} & if\ V_{ind} > V_{refd}/4 \\ 2V_{ind}\ if - V_{refd}/4 \le V_{ind} \le +V_{refd}/4 \\ 2V_{ind} + V_{refd} & if\ V_{ind} < -V_{refd}/4 \end{cases} \tag{5-19}$$

where V_{ind} equals to $(V_{in+} - V_{in-})$ and V_{refd} equals to $(V_{ref+} - V_{ref-})$.



(a) Sampling Stage



(b) Transfer Stage

Figure 5-19 Novel MDAC Operation

As shown in Fig. 5-19 (b), the switched capacitor circuit can achieve high speed because the feedback factor (the ratio of the feedback capacitor to the total capacitance at the summing node) approaches unity and is much larger than that of the traditional MDAC architecture. Such a unique feature makes the closed loop circuit

operate at approximately the unity gain frequency of the OTA. The bandwidth is give by

$$BW = \frac{1}{\tau} = \frac{G_m}{(C_{load} + C_{sr} // C_{si})} * f \tag{5-20}$$

where $f = (C_{si} // C_{sr}) / (C_{si} // C_{sr} + C_{OTA})$, and C_{OTA} is OTA input's parasitic capacitance. The output noise is given by,

$$\bar{V}_{on}^2 = \frac{KT}{(C_{load} + C_{sr} // C_{si})} * NF \tag{5-21}$$

The conventional MDAC and novel MDAC are compared in Table 5-1. To simplify the comparison, we normalize all the parameters. Assume both architectures use the same OTA, and they have the same G_m. Therefore, we assume C_{OTA} and C_{Load} (C_{Load} is the next stage input parasitic capacitor) are normalized to 0.5, and $C_{si} = C_{sr} = C_S = C_F$ are normalized to 1.

Ref.	f	BW	Noise	Power
MDAC[42]	0.4	$0.36G_m$	2.2KT*NF	1
Proposed MDAC	0.5	$0.5G_m$	KT*NF	1

Table.5-2 Comparison between Two MDACs

As shown in Table 5-2, the power consumption is normalized to the MDAC power consumption. Given the same power, we can calculate the MDAC performance metrics based on Equation (5-17), Equation (5-18), Equation (5-20) and Equation (5-21). Our novel MDAC can in practical achieve a better performance.

From the above analysis, we can see that the OTA's input parasitic capacitance C_{OTA} plays an important role in calculating the feedback factor f in both MDAC architectures. If C_{OTA} equals to zero, our proposed MDAC wins as much as twice the bandwidth than the traditional one, and if C_{OTA} equals to C_s, our proposed MDAC can only achieve the same bandwidth as the traditional one. Assume that $C_{si} = C_{sr} = C_S = C_F$ are normalized to 1. Fig. 5-20 shows the feedback factor versus input parasitic capacitance C_{OTA}.

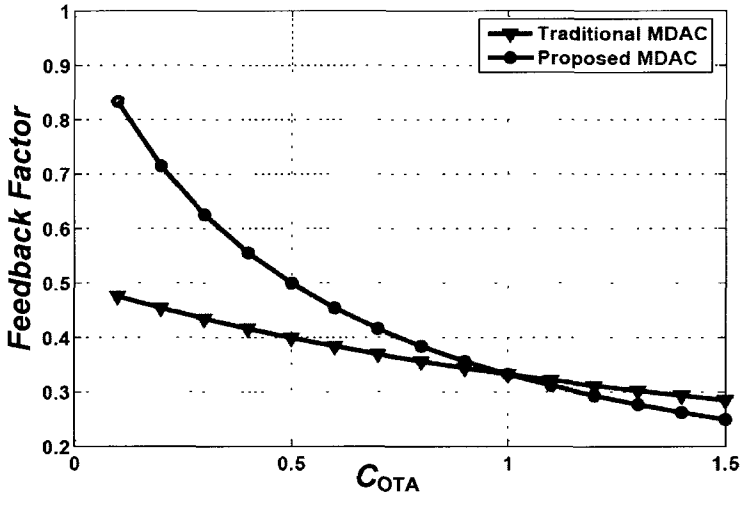
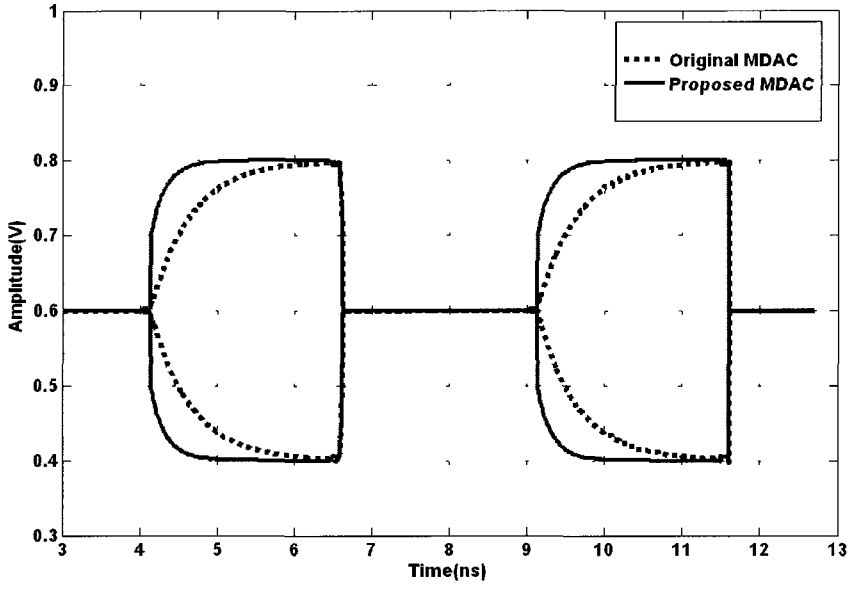


Figure 5-20 Feedback Factor Comparison

As shown in Fig. 5-20, our approach will get a higher feedback factor and have higher bandwidth as long as C_{OTA} is less than $C_{si} = C_{sr} = C_S = C_F$. In the real design, C_{OTA} is always less than $C_{si} = C_{sr} = C_S = C_F$.

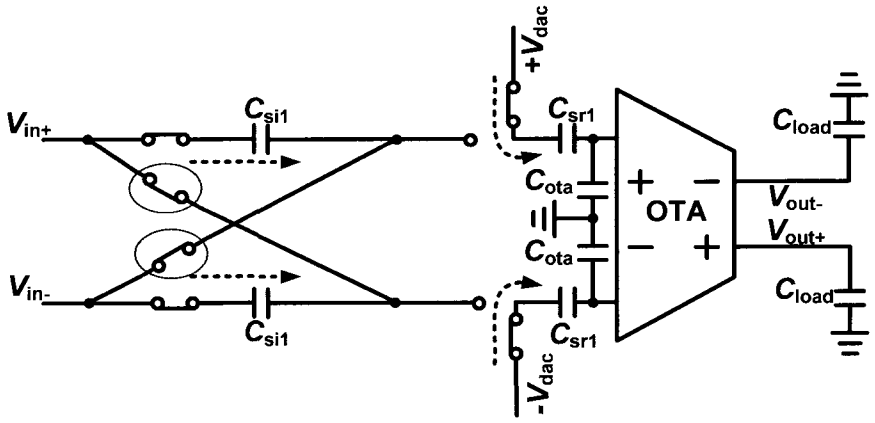
In the design implementation, we have boosted the closed loop bandwidth. The current in OTA can be reduced further as can the input parasitic capacitance. In our design, at the same speed performance, the proposed MDAC can consume four times

less power and produces one-half the noise of a conventional MDAC [5]. Moreover, bandwidth is related to settling behavior.

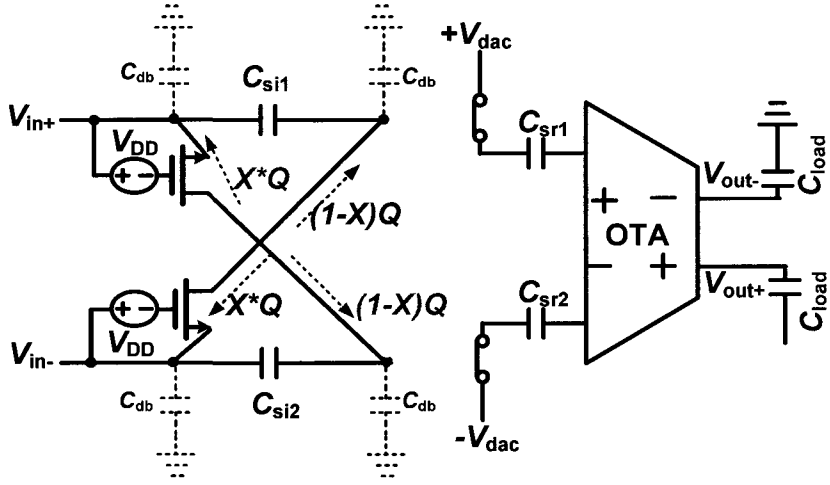


FFig.5-21 Step Response Comparisons between Two MDAC Architectures with Same Power Consumption.

Fig. 5-21 shows the settling behavior comparison between the two MDAC architectures working on differential mode with the same power consumption. The data need to be settled by the end of the clock cycle. Therefore, the novel MDAC has the opportunity for greater power reduction while allowing settling time compensate to the original MDAC. The novel technique still suffers from degraded switch linearity problem and exhibits a low SFDR (spur free dynamic range) performance. As shown in Fig. 5-22(a), the cycle switches cannot use bottom-plate architecture, because, when the cycle switches are switched on, the charges stored in the MOS channels will be rejected and accumulate on the sampling capacitors, which will cause sampling errors.



(a)



(b)

Figure 5-22 Switch Errors

To minimize the charge injection error, the bootstrapped switches will be used for the cycle switches as shown in Fig. 5-22(b). The bootstrapped switch has a smaller size and will cause a smaller error. Also, the charge injection is almost constant and given by

$$
\begin{aligned}
Q &= WLC_{ox}(V_{DD} - V_{th}) \\
&= WLC_{ox}(V_{DD} - V_{tho} - \gamma(\sqrt{2\Phi_F + V_{in}} - \sqrt{2\Phi_F})) \\
&-> taylor\ \ series \\
&= WLC_{ox}(V_{DD} - V_{tho} - \gamma\sqrt{2\Phi_F}(\frac{V_{in}}{4\Phi_F} - \frac{V_{in}^2}{8(2\Phi_F)^2})) \\
&\approx WLC_{ox}(V_{DD} - V_{tho} - \gamma\sqrt{2\Phi_F}(\frac{V_{in}}{4\Phi_F})) \\
&\text{where } \Phi_F = 0.9(V) \text{ and } \gamma = 0.45(V^2)
\end{aligned}
\tag{5-22}
$$

Moreover, there are a number of parasitic capacitors that impacts the MDAC's performance. Due to the differential operation, most common mode parasitic capacitor noise can be eliminated, but the parasitic capacitor between drain and substrate, C_{db}, is voltage dependent, as shown in Fig.5-23 and lack of settling causes C_{db} to change and that causes distortion at high clock rates. There were two more switches to generate more C_{db} in our design.

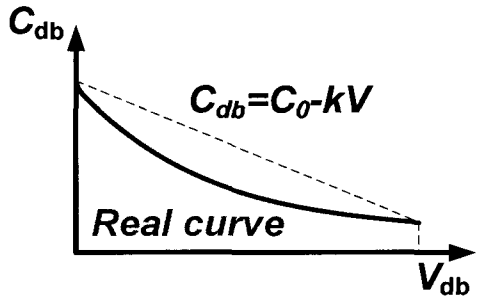


Figure 5-23 Voltage Dependent Parasitic Capacitance C_{db}

To calculate the voltage dependent parasitic capacitor effect on the MDAC performance, we apply charge conservation and KCL and get

$$\begin{cases} C_s(V_{out+} - V_{cm}) = C_s V_{in} + (C_o - kV_{in+}) \dfrac{WLC_{ox}(V_{DD} - V_{th} - \alpha V_{in-})}{2} \\ C_s(V_{out-} - V_{cm}) = -C_s V_{in} + (C_o - kV_{in-}) \dfrac{WLC_{ox}(V_{DD} - V_{th} - \alpha V_{in+})}{2} \end{cases} \quad (5\text{-}23)$$

The output reflecting parasitic capacitor C_{db} is given by

$$V_{out} = (2 + \frac{C_o WLC_{ox}}{2C_S}(\alpha - k(V_{DD} - V_{th})))V_{in} - \frac{C_o WLC_{ox}}{2C_S}\alpha k V_{in}^2$$

$$\Rightarrow$$

$$HD_2 = \frac{KC_o WLC_{ox}}{4C_s}\alpha V_{FS}$$

In our case,

$\alpha = 0.1$

$K = 0.06 fF / um / V$ (5-24)

$L = 90nm$

$Cox = 11 fF / um^2$

$R_o = 50ohm * um$

$C_o = 12 fF / um^2$

$Vcm = 0.6$

The SFDR performance versus sampling frequency due to parasitic capacitor effect is illustrated in Fig. 5-24.

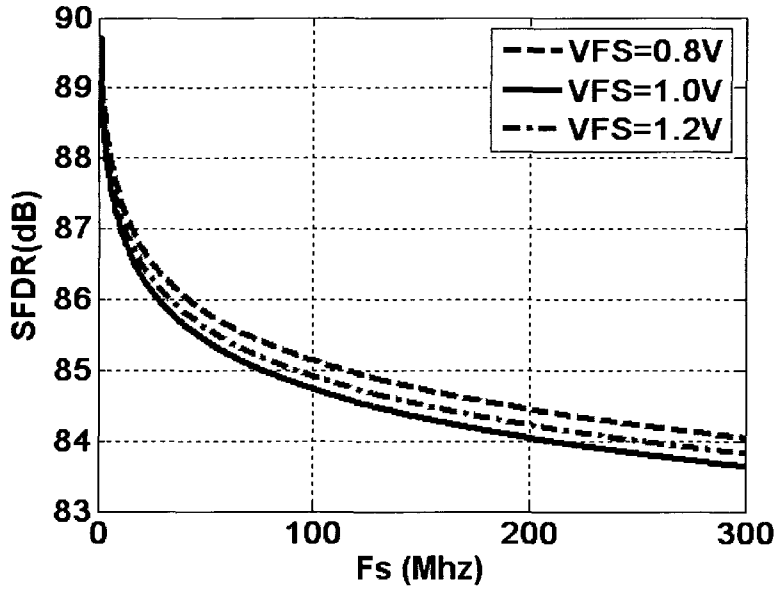


Figure 5-24 Simulated SFDR Performance versus Sampling Frequency with Parasitic Capacitance Effect

Form Fig.5-24, SFDR is approximately 84 dB with a 200 MHz sampling rate and 1.2 peak to peak differential input swings. Real-life situation is more complicated and will be measured in physical silicon.

5.6 Sub-ADC

A sub-ADC is employed to quantize the input signal and generate the intermediate digital bits for each stage. In our design, the 1.5 bits per stage sub-ADC architecture has three binary states for its output: 00, 01, and 10. To get the three binary states, two differential comparators with thresholds set at $+V_R / 4$ and $-V_R / 4$ are needed as shown in Fig. 5-25. Fig. 5-25 shows the locations of the sub-ADC thresholds and corresponding digital outputs.

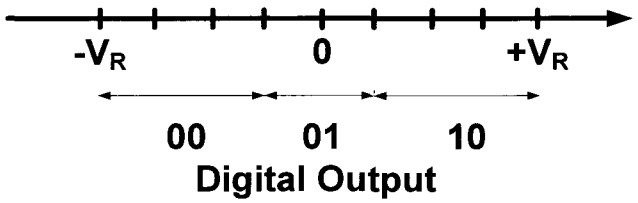


Figure 5-25 Sub-ADC Threshold Locations and Corresponding Digital Outputs

The comparators used in the sub-ADC are shown in Fig. 5-26. It consists of a capacitor network, clocking circuitry and voltage comparators. The outputs of the two differential comparators, which are part of the sub-ADC, are sent to the sub-DAC block. Logic within the sub-DAC block generates the three allowable binary states for a 1.5 bit per stage architecture.

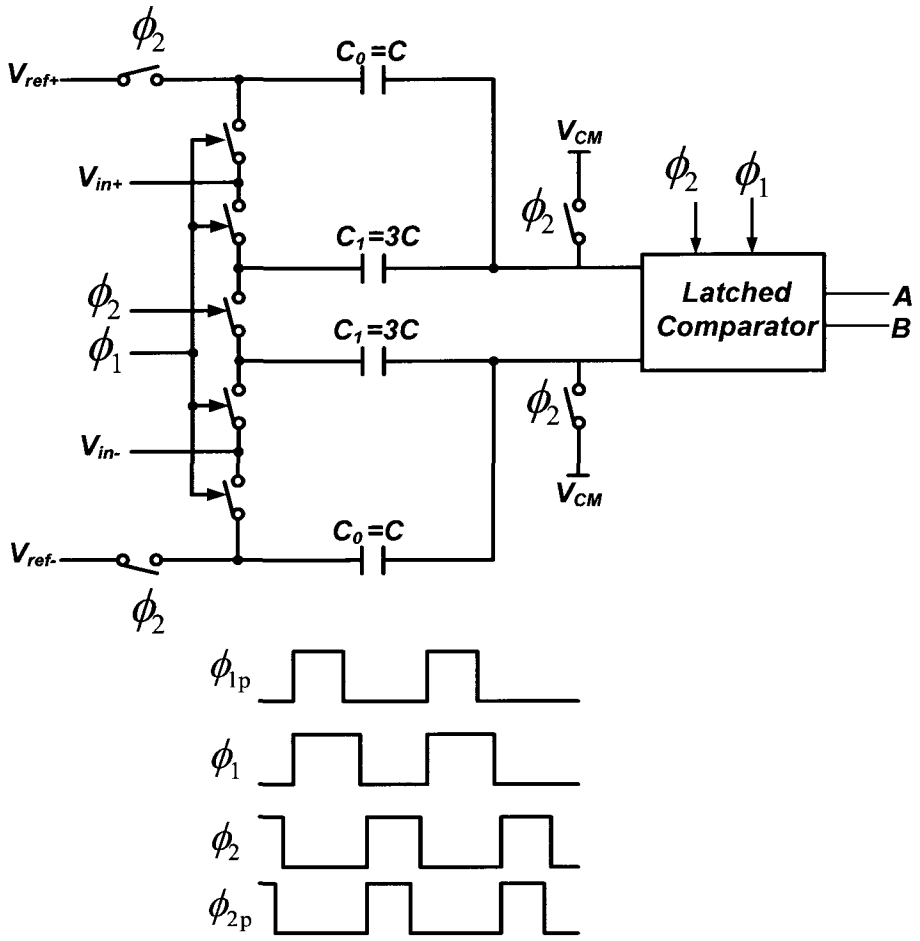


Figure 5-26 Differential Comparator in Sub-ADC

There are four clock phases (ϕ_1, ϕ_2, ϕ_{1p}, ϕ_{2p}) which are used to control the comparator operation. Capacitor C_0 and C_1 are sized with a ratio of 1:3 to divide the V_R by a factor of four. The four capacitors network is used to obtain thresholds $\pm\frac{V_R}{4}$ for the comparison operations. The value of V_R is different from $+V_{ref}$ and $-V_{ref}$ ($V_{ref+} = 900\ mV$, $V_{cm} = 600\ mV$ and $V_{ref-} = 300\ mV$) and can be calculated as follows:

$$V_R = \frac{V_{ref+} - V_{ref-}}{2} \tag{5-25}$$

The inputs of the voltage comparators are given by

$$+V_{inc} = +V_{in} + \frac{V_R}{4}$$
$$-V_{inc} = -V_{in} - \frac{V_R}{4} \qquad (5\text{-}26)$$

The switched circuit comparators are operated as follows. During phase ϕ_2, $\pm V_{ref}$ is sampled and stored on C_0 and $\pm V_{inc}$ is set as the common signal voltage V_{cm}. During phase ϕ_1, input signal $\pm V_{in}$ is applied and C_0 and C_1 are connected together. Since the ratio of C_0 and C_1 is 1:3, $\pm V_{ref}$ is redistributed between C_0 and C_1 to get the desired value in Equation (5-26).

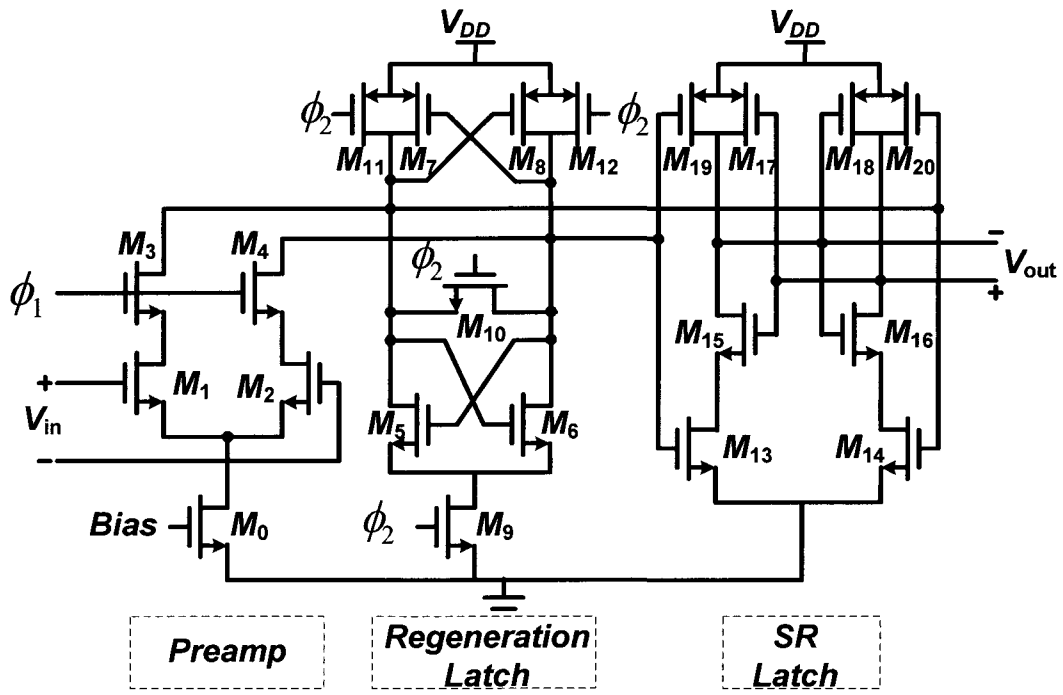


Figure 5-27 Latched Comparator

The critical part of this comparator module is the latched comparator shown in Fig.5- 27. It has three stages: input pre-amplifier, regeneration latches, and output S-R latch. The input pre-amplifier is just a simple NMOS differential pair, which not only provides some first stage gain but also reduces the kick-back noise from the regeneration latches. The NMOS switches (M_3 and M_4) will turn off the input differential pair during the regeneration interval to save power. Turning them off also helps to suppress kick-back noise from the following regeneration latch stages. The PMOS and NMOS complementary regeneration latches help to speed up the regeneration compared to only PMOS latches or only NMOS latches. The regeneration latches are reset to a voltage close to that of the power supply by M_{11} and M_{12} during the ϕ_2 phase. The reset switch M_{10} across the differential latching node reduces the offset due to the mismatch of M_{11} and M_{12}. The NMOS switch M_9 will disable the NMOS regeneration latch during the resetting phase to avoid any large DC current to ground. The output S-R latch will hold the comparison result during the whole clock period for the convenience of the encoding logic in the following stage.

5.7 Sub-DAC

The function of the sub-DAC is to supply the gain stage with the analog voltage level that represents the quantized portion of the input sample. The quantized portion is subtracted from the input signal to create a residue that will be sent to the next stage. The sub-DAC calculates the digital word for that stage according to the outputs from the sub-ADC. For the 1.5 bits per stage architecture, the sub-ADC can have one of the three binary outputs: 00, 01, and 10. These correspond to the sub-DAC outputs of $-V_R/2$, 0, and $+V_R/2$ respectively.

Fig. 5-28 shows the combination of logic and switches used to implement the sub-DAC. The inputs of the 3-input NAND gates are outputs of the sub-DAC and clock. The digital outputs are obtained after the NAND operation. They are forced into shift register array to synchronize all outputs of all stages. As shown in Table 5-3, for a given binary output, the corresponding V_{DAC+} and V_{DAC-} are selected and sent to the gain stage, where they are subtracted from the original input signal to generate the residue.

A_1 A_2	B_1 B_2	ϕ_2	MSB LSB	V_{DAC+} V_{DAC-}
0 1	0 1	1	0 0	V_{REF-} V_{REF+}
0 1	1 0	1	0 1	V_{CM} V_{CM}
1 0	1 0	1	1 0	V_{REF-} V_{REF+}

Table 5-3 Truth Table for Pipeline Stage and Corresponding sub-DAC Outputs

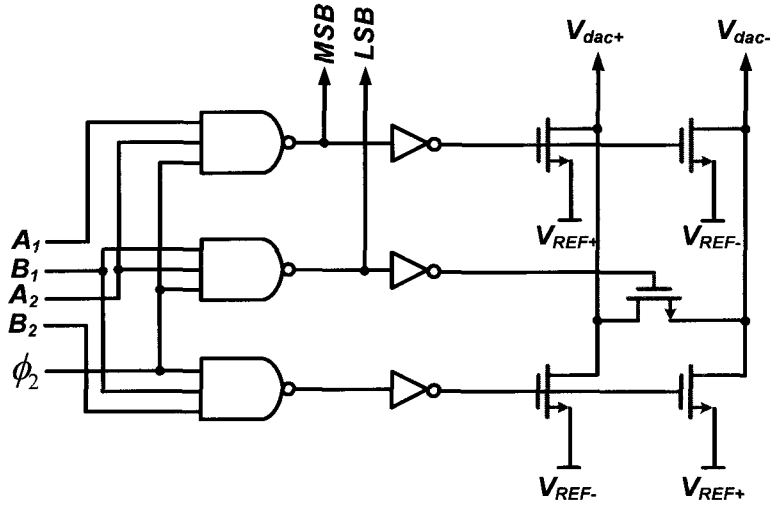


Figure 5-28 Sub-DAC Circuit

5.8 Digital circuit

Of primary importance in pipeline converters is the digital correction of digital output bits each stage. The outputs of every stage must be stored until the last stage gives the digital output. In our design, the shift register is used to implement the memory function. The design for the shift register was implemented in [91]. The basic structure of the shift register consists of inverters connected with switches, as shown in Fig. 5-29. The clocks are non-overlapped differential phases, and every other string of shift registers requires an additional stage of inverters. As shown in Fig. 5-29, digital data A and B will shift to the right side of the circuit when ϕ_2 is high. At the beginning, A is shifted through during ϕ_2 and B is shifted through during ϕ_1. Data from each stage are valid alternatively on opposite clock signals. Therefore, after N cycles, all the digital outputs are synchronized. The shift register is used to shift the eight stages of two bits/stage outputs before the data is sent to the correction logic block.

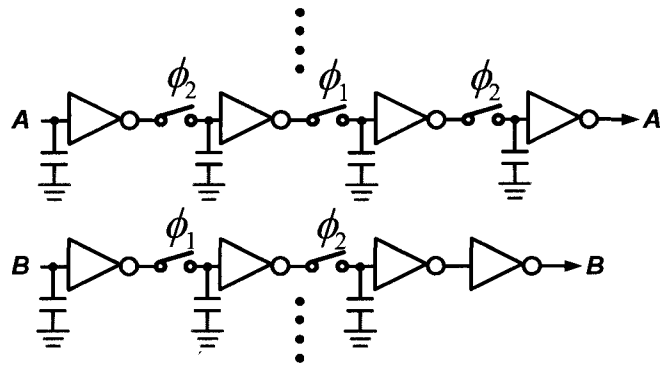


Figure 5-29 Shift Register

Before the outputs are sent out, the digital data were corrected by correction logic. In our pipeline converters, there were about twice as many bits generated through each

pipeline stage than actually required. These redundant bits needed to be digitally corrected to generate the correct ultimate output. There are many ways that can be applied to implement the logic calibration. But the concepts were similar. The outputs of the earlier stages were kept in the shift register until stage *N* provided its output. The collected data bits were then added to generate the required bits. In our design, the concept behind the correction logic is illustrated in Fig. 5-30.

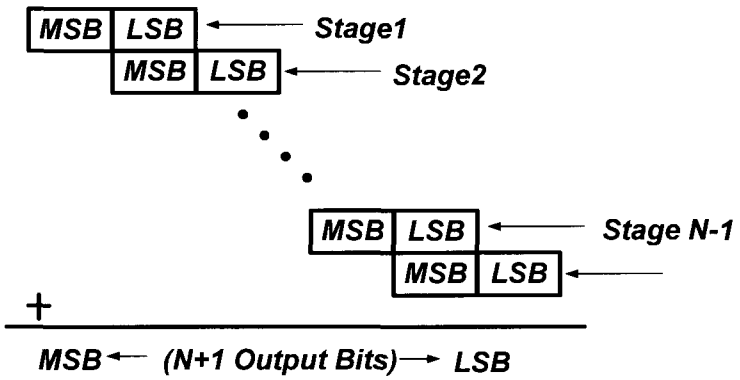


Figure 5-30 Digital Correction Concepts

In order to perform the mathematical operation shown in Fig. 5-30, a simple calculation for the operation is illustrated in Fig. 5-31.

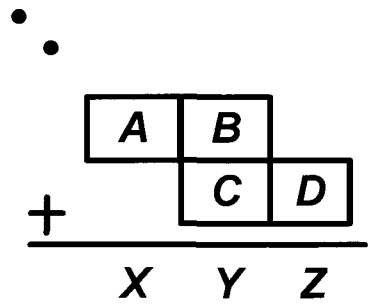


Figure 5-31 Mathematical Analysis of Digital Correction

As shown in Fig. 5-31, the binary operations are operated as follows:

$$
\begin{aligned}
Z &= D \\
Y &= B \oplus C \\
X &= A + BC
\end{aligned}
\tag{5-27}
$$

Y is calculated by a simple XOR. The CARRY-BIT block is applied to implement the AND/OR operation to generate X as stated in Equation (5-27).

5.9 Pipeline ADC Layout

The chip was fabricated in IBM 90 nm CMOS process technology. Because of the presence of the digital circuits in the sensitive analog circuits, special layout techniques are necessary. The layout floor-plan of a fully differential pipeline ADC is sketched in Fig.5-32. The first, second, third and fourth stages are located from the left to the right depicted in Fig.5-32. Also, to avoid capacitive coupling, all the switches were placed in the outer spaces so that the clock bus could be distributed surrounded with a ground-shielded guard ring, providing isolation and a low impedance return path for the injected substrate noise. The clock signal was fed through the bottom and was distributed according to H-tree architecture to allow for nearly equal delay to each stage.

In addition, a large p+ substrate contact tied to digital substrate bias was inserted between the sensitive analog and the noisy digital circuits, which provide a low impedance return path for switching noise injected into the substrate. Decoupling capacitors filled the empty area within the chip.

Capacitor matching is another critical issue to maintain accuracy. As a result, a uniform sized capacitor was chosen to implement all the sampling and integrating

capacitors. To further avoid mismatch due to over-etching, the dummy capacitors were placed on the boundaries of capacitor array.

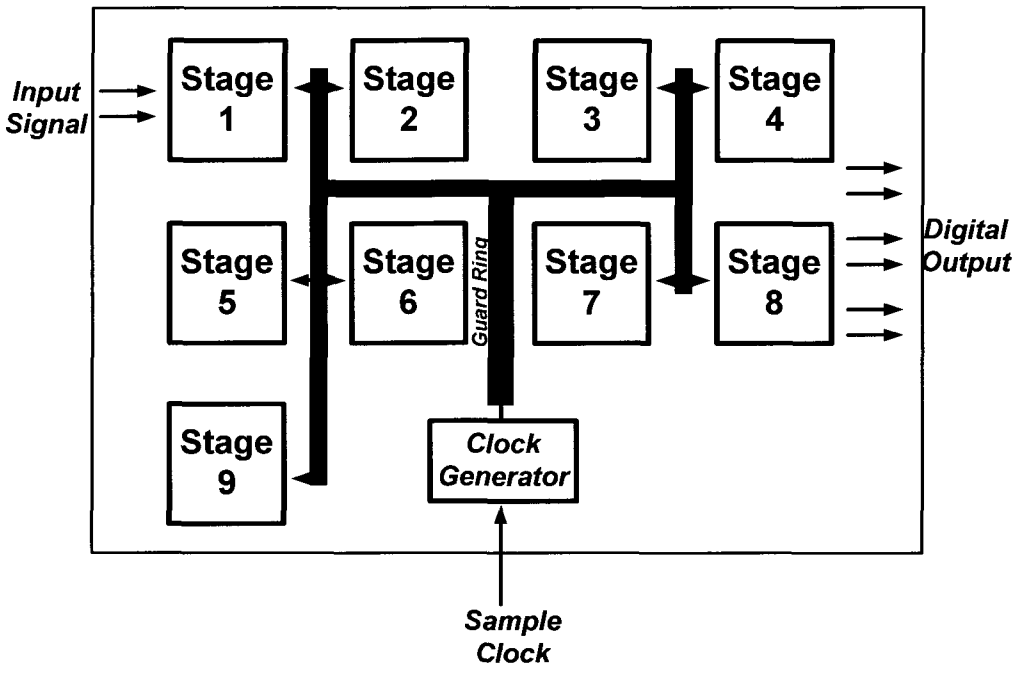


Figure 5-32. Layout Floor-Plan of a Fully Differential Pipeline ADC

5.10 Measurement result

The prototype circuit was fabricated using a 90nm IBM CMOS process. The total active area of the ADCs is $0.7\mu m * 0.6\mu m$ and the die photo is shown in Fig. 5-33. The chip was packaged by Quad Flat No lead (QFN) 72 pins package. The packaged Chip is installed into a socket for measurement. The total power consumption is 40mW at 1.2-V supply.

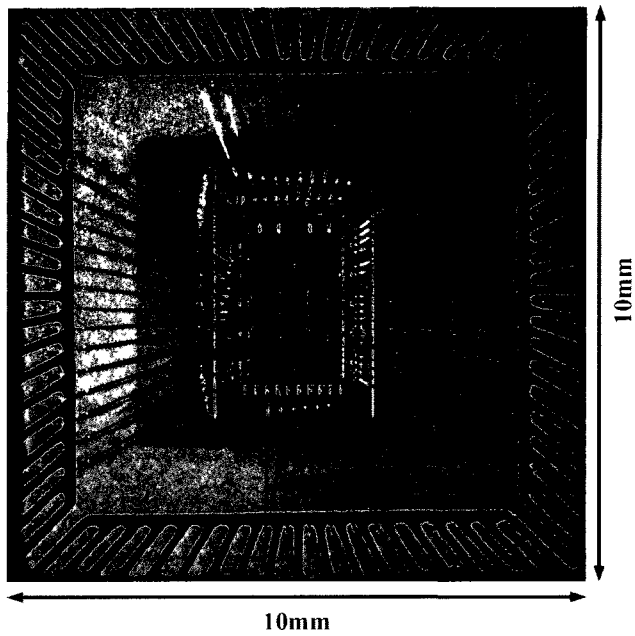


Figure 5-33. Chip Photo of the Pipeline ADC with QFN Package

Figure 5-34 shows the block diagram of the testing setup. The input and output impedance of all the terminals were matched to 50Ω for the matching from the external source to the ADC input and output. The signal-ended sinusoidal signal was first generated by the signal function generator and the differential signal was produced by using the Mini-Circuits ADT1-1WT (wideband 15 k – 300 MHz) balun with a 1:1 turns ratio for simplicity. The input common mode level of the ADC was applied at the center tap of the secondary turn. Moreover, in order to avoid the input current transient from the ADC input due to sampling switches, a 1 nF capacitor was added between input terminals to act as small charge reservoir. Additionally, the capacitor formed a lowpass filter to reduce the noise folding coming from the ADC due to sampling. All the power supplies, references, current and voltage bias were taken from the LDO regulator which is powered by the external power supply. The

regulated bias was applied to the dedicated IC pins via a multiple parallel decoupling networks.

The low jitter clock pattern generator was used to provide the clock signal for the on-chip clock generator of the ADC and to provide a clock trigger to sample the output data from the ADC's output at the logic analyzer. The captured data points form logic analyzer was finally exported to MATLAB for analysis.

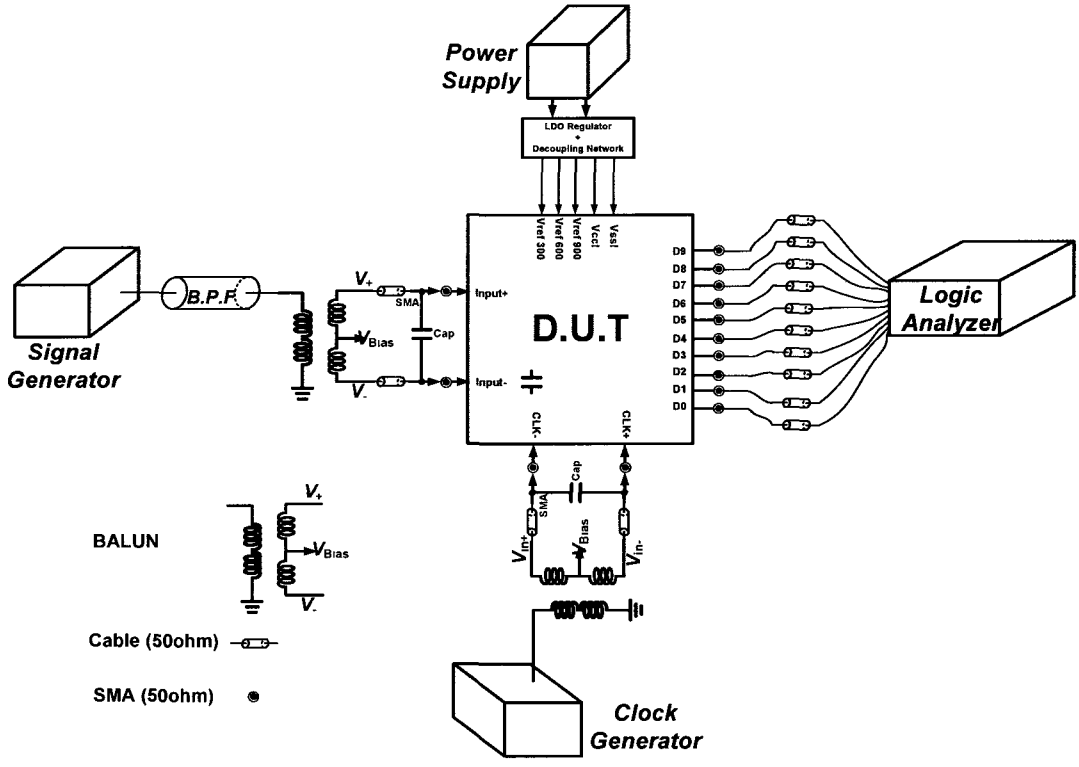


Figure 5-34. Block Diagram of the Chip Testing Setup

The equipments used in the chip testing are summarized in Table 5-4.

Test equipment	Model
Power Supply	HP 62058
Signal Generator	PMD AWG2041
Signal Generator	BK PRECISION 4084
Digital Analyzer	Agilent 1683A
Oscilloscope	Tektronix 2236

Table 5-4 Testing Equipments

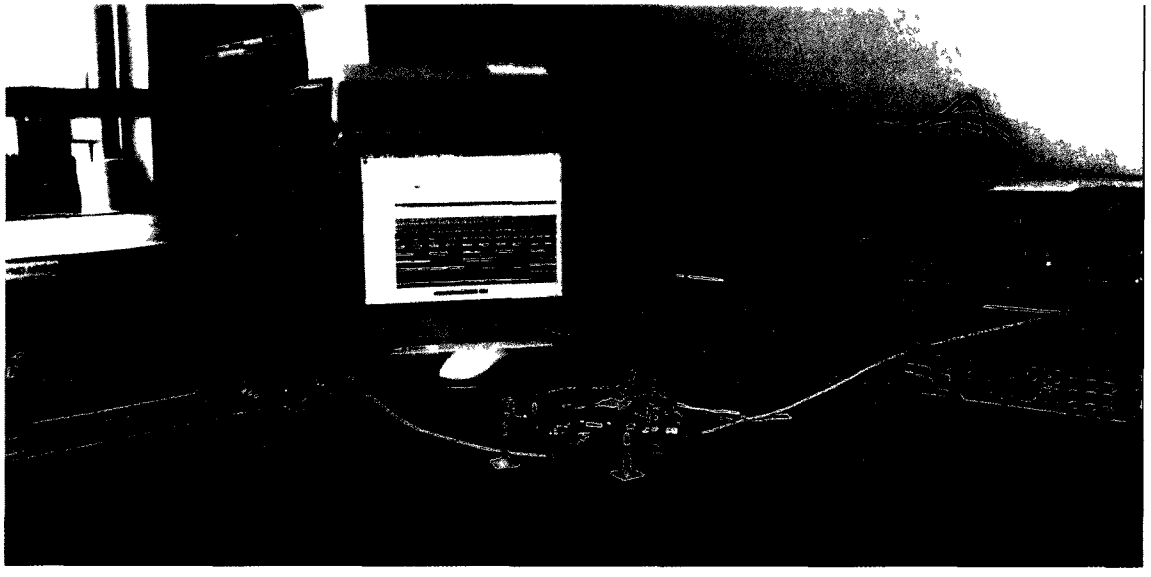


Figure 5-35 ADC Testing Setup

Fig. 5-35 shows the ADC testing lab setup. Fig. 5-36 show the ADC digital output from digital analyzer at sample rate at 400 KS/s.

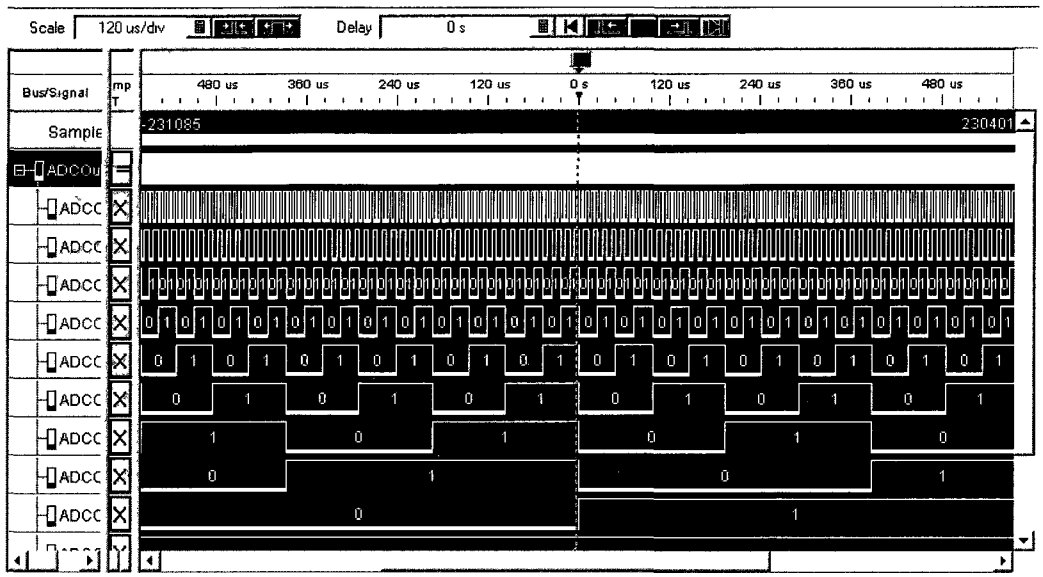


Figure 5-36 ADC output from digital analyzer sampled at 400KS/s

Fig. 5-37 shows the output spectrum of the novel ADC for a 3.89MHz input signal sampled at 95 MS/s. The SNDR was 46 dB and SFDR was 57 dB.

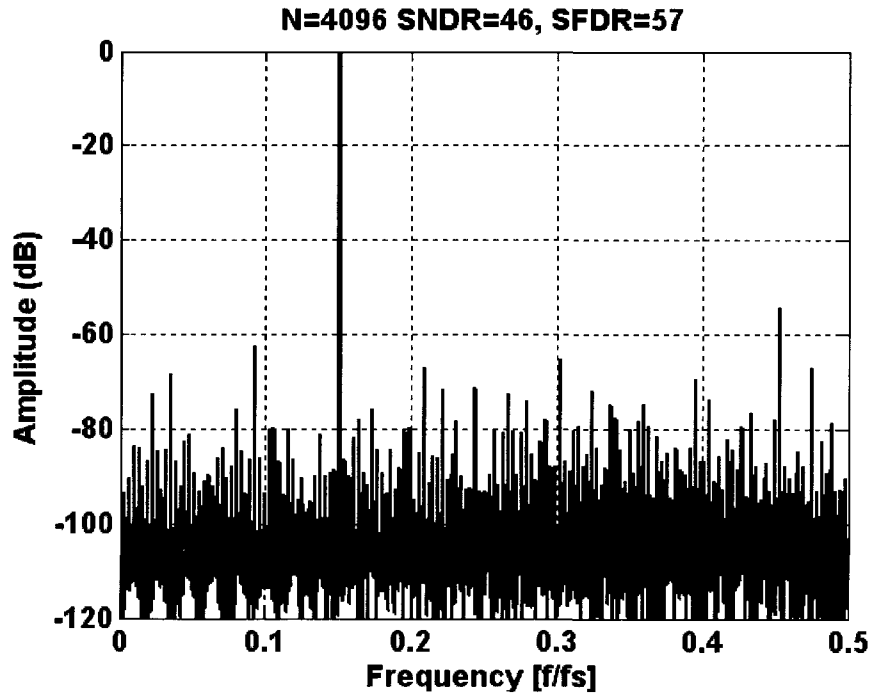


Figure 5-37 Output Spectrum for an Input Signal 3.8MHz sampled at 95 MS/s

Fig. 5-38 shows the SFDR and SNDR performance as a function of input frequency at the fixed sample rate of 95 MHz. The measure results are summarized in Table 5-4.

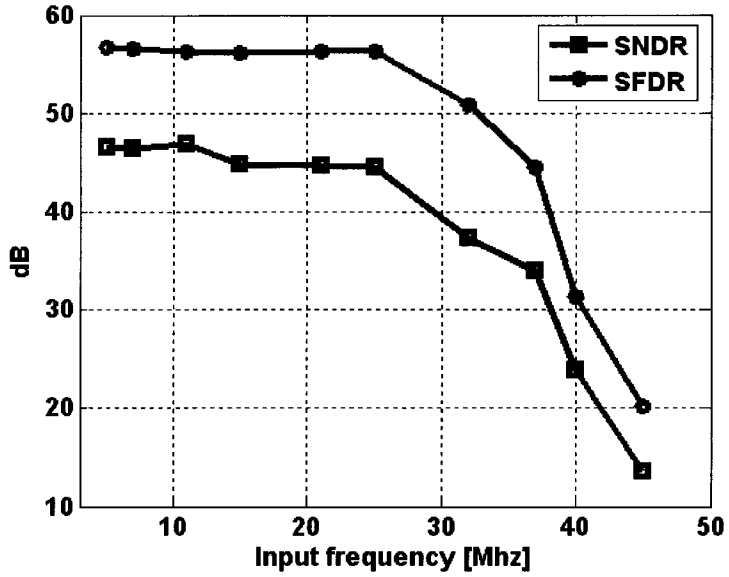


Figure 5-38 SFDR and SNDR as a Function of Input Frequency at a Sampling Rate 95 MHz

Architecture	Pipeline 8X1.5b,1X2b
Technology	IBM 90nm CMOS
Supply Voltage	1.2V
Input Range	1.2V P-P differential
Resolution	10b
ENOB	7.3bit
SNDR	46dB
SFDR	57dB
Fs	95Mhz
Power	40mW
FOM	2.6pJ/convstep

Table 5-4 Measured Results

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusions

Pipeline converters are widely used in communication systems as the analog-digital interface. Compared to other types of ADCs, the pipeline ADCs has the benefit of maintaining high accuracy at high conversion rates with low complexity and power consumption. In this thesis, the performance limiting factors and their effects on the performance of a converter were studied, especially the power consumption. Also several novel design technique applied to ADC were presented. A 95 MHz 10-bit low power pipeline ADC is fabricated and measured using our proposed low power technique.

The thesis started with the basic introduction of data conversion history and our motivations, Chapter 2 introduced the basic knowledge of the data conversion process and how the different converters work. In Chapter 3, the sample and hold process was discussed, and the effect of different limitation on sample and hold performance was addressed. A high speed switched source follower sample-and-hold circuit with feedthrough cancellation was presented and the proposed SSF realized a more than 6 dB improvement in total harmonic distortion performance. The low power switched capacitor circuit design techniques were present in Chapter 4. All of the non-ideal factors with their effects on the circuits were discussed in detail, including finite OTA gain, finite OTA bandwidth, charge injection and non-ideal switch. Those factors can greatly degrade the ADC performance without careful design. Moreover, a rail-to-rail

time domain comparator was proposed for ultra low power applications, which will not only save power but also will be better scalable with sub-micron technology.

In Chapter 5, the implementation of a 95 MHz 10-bit pipeline □converter was discussed. It started from the topology down to the circuit implementation of various building blocks. Pipeline ADC was applied to our novel multiply-digital-to-analog converter (MDAC) architecture. The proposed MDAC architecture which minimized the feedback factor effect in the switched capacitor circuit saved more than 50% power consumption and reduced noise effect more than 20%. The prototype circuit was fabricated in the IBM 90 nm CMOS process and measured. The novel 10-bit ADC achieved a peak signal-to-noise-and-distortion-ratio (SNDR) of 47 dB. This SNDR translated to a figure of merit (FOM) of 2.6 pJ/conversion-step with a 1.2V power supply.

6.2 Future work

There are still some existed low power techniques can be used in our pipeline ADC to further reduce our pipeline ADC's power consumption: Merged the SHA with the first stage[13][14][15], Stage scale-down[43] and digital calibration[43][50][81]

Merged the SHA with the first stage can be applied to reduce the power consumption of the front-end SHA. The front-end SHA needs highest accuracy in the pipeline ADC design, and it will take up almost 45% of the total power consumption, therefore, merged the SHA with the first stage will save large power.

Another technique is stage scale-down. In pipeline ADC design, the first stage requires higher accuracy than the following stages, and the following stages can be less accuracy. Then the following stages don't need as much power consumption as

the first stage. Stages scale-down techniques can save up to 70% of total stages power consumption.

Also, digital calibration can relax the analog blocks' requirement, and reduce the power consumption of the analog blocks. All the offset and errors can be corrected in digital domain.

If we can apply one or more the above technique in our design, we can save more power and achieve a better FOM performance.

LIST OF REFERENCE

[1]. William, C. Kun, "Introduction to D/A and A/D Converters," *Michigan State University,* OCT. 27th, 2004.

[2]. P. Li, M. Chin, and P. Gray, "A ratio independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 828-836, Dec1984.

[3]. C. Shih and P. Gray, "Reference refreshing cyclic analog-to-digital and digital-to- analog converters," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 544-554, Aug 1986.

[4]. B. Song, M. Tompsett, and K. Lakshmikumar, "A 12-b 1-Msample/s capacitor error-averaging pipelined A/D converter," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1324-1333, Dec 1988.

[5]. Y. Chiu, "Inherently linear capacitor error-averaging technique for pipelined A/D converter," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 229-232, March 2000.

[6]. Ali, A.M.A, Morgan, A, Dillon, C, Patterson, G, Puckett, S, Bhoraskar, P, Dinc, H, Hensley, M, Stop, R, Bardsley, S, Lattimore, D, Bray, J, Speir, C, Sneed, R.A, "16-bit 250-MS/s IF sampling pipelined ADC with background calibration," *IEEE J. Solid-State Circuits*, vol. 45, Issue.12, pp. 2602 - 2612, Oct 2010

[7]. A. Panigada, and I. Galton, "A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction, " *IEEE Solid State Circuits Conference*, pp. 84-85, Feb 2009.

[8]. Verma, A. Razavi, "A 10b 500MHz 55mW CMOS ADC, " *IEEE Solid State Circuits Conference*, pp. 162, Feb 2009.

[9]. L. Sumanen, M. Waltari, and K.A.I Halonen, "A 10-bit 200 MS/s CMOS Parallel Pipeline A/D Converter, " *IEEE J. Solid-State Circuits*, vol.36, no. 7, pp. 1048–1055, Jul 2001.

[10]. Kang-Wei Hsueh, Yu-Kai Chou *et al.*, "A 1V 11b 200MS/s pipelined ADC with digital background calibration in 65nm CMOS," *IEEE Solid State Circuits Conference,* pp.546-634, Feb 2008.

[11]. B. Hernes, J. Bjornsen, T. N. Andersen, "A 92.5mW 205MS/s 10b pipeline IF ADC implemented in 1.2V/3.3V 0.13μm CMOS," *IEEE Solid State Circuits Conference,* pp.462-615, Feb 2007.

[12]. H. Lee, D. Hodges, and P. Gray, "A self-calibrating 15-b CMOS A/D converter, " *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 813–819, Dec 1984.

[13]. B. Lee, B. Min, G. Manganaro, and J. W. Valvano, "A 14b 100MS/s pipelined ADC with merged active S/H and first MDAC, " *IEEE Solid State Circuits Conference*, Feb 2008.

[14]. Y.D. Jeon, S.-C. Lee, K.-D. Kim, J.-K. Kwon, and J. Kim, "A 4.7-mW 0.32mm 10b 30MS/s pipelined ADC without a front-end S/H in 90nm CMOS, " *IEEE Solid State Circuits Conference*, pp. 456-457, Feb 2007.

[15]. A.M.A. Ali, C. Dillon, "A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs Jitter," *IEEE Journal of Solid-State Circuits*, vol.41, no.8, pp. 1846-1855, Aug 2006

[16]. S. Devirajan *et al.*, "A 16b 125 MS/s 385 mW 78.7 dB SNR CMOS pipeline ADC, " *IEEE Solid State Circuits Conference*,, pp.86–87, Feb 2009.

[17]. N. Verma, A.P. Chandrakasan, "An utra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," *IEEE J. Solid-State Circuits,* vol.42, no.6, pp.1196-1205, June 2007.

[18]. M. Anderson, K. Norling, A. Dreyfert, and J.Yuan, "A reconfigurable pipelined ADC in 0.18 μm CMOS," *IEEE VLSI Circuits Symposium,* pp. 326-329, June 2005

[19]. W. Audoglio, E. Zuffetti, G. Cesura, R. Castello, "A 6-10 bits Reconfigurable 20MS/s Digitally Enhanced Pipelined ADC for Multi-Standard Wireless Terminals," *IEEE ESSCIRC Proceedings,* pp.496-499, Sep 2006

[20]. J. Craninckx, G. Van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7Mw 9b charge-sharing SAR ADC in 90nm digital CMOS," *IEEE Solid State Circuits Conference*,, pp.246-600, 11-15 Feb 2007

[21]. B. Murmann and B.E. Boser, "A 12 b 75 MS/s pipelined ADC using open-loop residue amplification, " *IEEE Solid State Circuits Conference*, pp. 328-329, Feb 2003

[22]. T. Sepke *et al.*, "Comparator-based Switched-capacitor Circuits for Scaled CMOS Technologies, " *IEEE Solid State Circuits Conference*, pp. 812-813, Feb 2006

[23]. J. Hu, N. Dolev, and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC using Dynamic Residue Amplification," *IEEE Symp. VLSI Circuits*, pp. 216-217, June 2008.

[24]. Gang Chen, K. Zhou, Y.F. Luo, "A 10B 200MHz Pipeline ADC with Minimal Feedback Penalty and 0.35pJ/conversion-step," *IEEE System on Chip Conference (SOCC)*, LV, USA, Sep 2010.

[25]. R. van de Plassche, "*Integrated Analog-to-Digital and Digital-to-Analog Converters*," Kluwer Academic Publishers, 1994.

[26]. B. Brannon and R. Reeder, "Understand high speed ADC testing and evaluation", *Analog Device Application Note AN-835*.

[27]. E. A. Phillip, R.H. Douglas, "*CMOS Analog Circuit Design*, Second Edition", *Oxford University Press*, 2003.

[28]. Y. Tambo and K. Yamakido, "A CMOS 6-b 500-Msample/s ADC for a hard disk drive read channel, " *IEEE Solid State Circuits Conference,.,* pp. 324–325, Feb 1999.

[29]. G. Geelen, "A 6-b 1.1-Gsample/s CMOS A/D converter, " *IEEE Solid State Circuits Conference,,* pp. 128– 129, Feb 2001.

[30]. B. Razavi, "*Principles of Data Conversion System Design*", *IEEE Press*, 1995.

[31]. R. Petschacher, B. Zojer, B. Astegher, H. Jessner, and A. Lechner, " A 10-b 75-MSPS subranging A/D converter with integrated sample and hold, " *IEEE J. Solid-State Circuits*, vol. 25, pp. 1339–1346, Dec 1990.

[32]. C. W. Mangelsdorf *et al.*, "A 400-MHz input flash converter with error correction," *IEEE J. Solid-State Circuits*, vol. SC-25, pp. 184–191, Feb 1990.

[33]. B. Razavi and B. A. Wooley, "Design techniques for high-speed high-resolutioncomparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1916-1926, Dec 1992.

[34]. J. C. Candy and G. C. Temes, "Oversampling methods for A/D and D/A conversion," *Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation*, pp. 1–25, *IEEE Press* ,1991.

[35]. B. Leung, " The oversampling technique for analog to digital conversion: a tutorial overview, " *Analog Integrate. Circuits Signal Processing*, vol. 1, pp. 65–74, 1991.

[36]. L.A.Williams and B.A.Wooley, "A third-order sigma-delta modulator with extended dynamic range, " *IEEE J. Solid-State Circuits*, vol.29, pp.193-202, March 1994.

[37]. I. Mehr and D. Dalton, "A 500-Msample/s, 6-bit Nyquist-rate ADC for disk-drive read-channel applications, " *IEEE J. Solid-State Circuits*, vol. 34, pp. 912–920, July 1999

[38]. S. Mortezapour and E. Lee, "A 1-V 8-bit successive approximation ADC in standard CMOS process, " *IEEE J. Solid-State Circuits*, vol. 35, pp. 642–646, April 2000.

[39]. H. Neubauer, T. Desel and H.Hauer, "A successive approximation A/D converter with 16 bit 200KS/s in 0.6um CMOS using self calibration and low power techniques", *IEEE International conference on Electronics, Circuits and System*,vol.2, pp. 859-862.

[40]. S. Lee, S. Park, Y. Suh, H. Park, and J. Sim, "A 1.3μW 0.6V 8.7-ENOB successive approximation ADC in a 0.18μm CMOS," *IEEE VLSI symposium* 2009, Jun. 2009.

[41]. Zhiheng Cao, Shouli Yan and Yunchu Li, "A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13um CMOS, " *IEEE Journal of Solid State Circuits*, vol.44, issue.3, pp.862-873, 2009.

[42]. A. M. Abo, P. R. Gray, " A 1.5V, 10bit, 14.3MS/s CMOS pipeline analog-to-digital converter, " *IEEE Journal of Solid State Circuits*, vol.34, issue.5, May 2009.

[43]. A.M.A, Ali, A. Morgan etc., "A 16b 250MS/s IF-sampling pipelined A/D converter with background calibration," *IEEE Solid State Circuits Conference*, pp.292-293, 7-11.Feb 2010

[44]. D.W.Cline, P.R.Gray, " A power optimized 13b 5MSamples/s pipelined analog-to-digital converter in 1.2um CMOS, ", *IEEE Journal of Solid State Circuits*, vol.31, no.3, pp.294-30, March 1996.

[45]. A.Verma, B.Razavi, "A 10b 500MHz 55mW CMOS ADC," *IEEE Solid State Circuits conference*, pp.84-85, Feb 2009

[46]. B.Verbruggen, J.Craninckx, M.Kuijk, P, P.Wambacq, G. Van der Plas, "A 2.6mW 6b 2.2GS/s 4-timesinterleaved fully dynamic pipelined ADC in 40nm digital CMOS, " *IEEE Solid-State Circuits Conference*, pp.296-297, Feb 2010.

[47]. K.Poulton, R.Neff, B.Setterberg, B.Wuppermann, T.Kopley, R.Jewett, J.Pernillo, C.Tan, A.Montijo, "A 20GS/s 8b ADC with a 1MB memory in 0.18um CMOS," *IEEE Solid-State Circuits Conference*, vol.1, pp.318-496, Feb 2010.

[48]. C. S. G. Conroy, D. W. Cline, P. R. Gray, "An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1-μm CMOS, " *IEEE J. Solid-State Circuits*, vol. 28, pp. 447– 454, April 1993.

[49]. S. Gupta, M. Choi, M. Inerfield, and J. Wang, "A 1-GS/s 11-bit ADC with 55-dB SNDR, 250mW power realized by a high bandwidth scalable time-interleaved architecture, " *IEEE Journal of solid-state circuits*, vol. 41, no. 12, pp-2650-2657, Dec 2006.

[50]. S. Jamal et al., "A 10-b 120-msample/s time-interleaved analog-to-digital converter with digital background calibration, " *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618-1627, Dec 2002.

[51]. K. Dyer et al., "An analog background calibration technique for time-interleaved analog-to-digital converters, " *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1904-1911, Dec 1998.

[52]. B.Murmann, "*ADC Performance Survey 1997-2011*," [online], Available: *http://www.standford.edu/~murmann/adcsurvey.html.*

[53]. S. Shahramian, S.P. Voinigescu and A.C. Carusone, "A 30GS/s Track and Hold Amplifier in 0.13um CMOS Technology," *IEEE Custom Integrated Circuits Conference,* pp. 493-496 Sept 2006.

[54]. T. Sato, S. Takagi, N. Fujii, Y. Hashimoto, K. Sakata, and H. Okada, "4-Gb/s Track and Hold Circuit using Parasitic Capacitance Canceller," *IEEE ESSCIRC*, pp. 347–350, Sept 2004.

[55]. B. Razavi, "Design of sample-and-hold amplifier for high-speed low-voltage A/D," *IEEE Custom Integrated Circuits Conference*, 1997.

[56]. B.Razavi, "Design of a 100-MHz 10-mW 3-V sample-and-hold amplifier in digital bipolar technology, " *IEEE Journal of Solid-State Circuits*, vol. 30, no. 7, pp. 724- 730, July 1995.

[57]. H.K.E. Sherif and B. Abdellafif, "A Bootstrapped Bipolar CMOS Gate for Low-Voltage Application," *IEEE Journal of Solid-State Circuits*, vol.30, no.1, 1995.

[58]. J. Steensgaard, "Bootstrapped Low-voltage Analog Switches, " *IEEE Journal of Solid-State Circuits*, vol.2, pp.29-32, July 1999.

[59]. M.Waltari and K.Halonen, "Bootstrapped switch without bulk effect in standard CMOS technology, " *IEEE Electronic letters*,vol.2,pp.29-32, 2002

[60]. G.Wegmann, E.A.Vittoz, and F.Rahali, "Charge injection in analog CMOS switches," *IEEE J.Solid-State Circuits*, Vol.SC-22, pp.1091-1097, Dec 1987.

[61]. B. J. Sheu and C.Hu, "Switch-induced error voltage on a switched capacitor, " *IEEE J. Solid-State Circuits*, vol.SC-19, pp.519-525, April 1984.

[62]. L. A. Bienstman *et al*, " An eight-channel 13 bit microprocessor compatible NMOS D/A converter with programmable scaling," *IEEE J. Solid-State Circuits*, vo.l5, no.6, Dec 1980.

[63]. K. L. Lee, "Low distortion switched capacitor filters," *Electron. Res. Lab. Memo M86/12*, University of California, Berkeley, 1986

[64]. R. C. Yen and P. R. Gray, "A MOS switched-capacitor instrumentation amplifier, "*IEEE J. Solid-State Circuits*, vol. 17, no. 6, pp. 1008-1013, Dec 1982.

[65]. K. C. Hsieh, et al., "A low-noise chopper-stabilized differential switched-capacitor filtering technique, " *IEEE J. Solid-State Circuits*, vol. 16, no. 6, pp.708-715,Dec. 1981.

[66]. J.C. Jensen and L.E. Larson, "A broadband 10-GHz track-and-hold in Si SiGe HBT technology, " *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 325-330, March 2001.

[67]. J. Lee, A. Leven, J.S. Weiner, Y. Baeyens, Y. Yang, W.J. Sung, J. Frackoviak, R.F. Kopf, and Y.K. Chen, "A 6-b 12- Gsamples/s track-and-hold amplifier in InP DHBT technology, " *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1533-1539, Sep 2003.

[68]. R. Gregorian, K.W. Martin, and G.C. Temes, "Switched-Capacitor Circuit Design," *Proceeding of the IEEE*, vol.71, issue.8, pp.941-966, Aug 1983.

[69]. A. N. Karanicolas, H. S. Lee, and K. L. Bacrania, "A 15b 1MS/s digitally self-calibrated pipeline ADC, " *IEEE Solid State Circuits Conference*,, pp. 60-61, Feb 1993.

[70]. T. B. Cho and P. R. Gray, "A 10bit, 20MS/s, 35mW pipeline A/D converter, " *IEEE Custom Integrated Circuits Conf.*, pp 2321-2324, May 1994.

[71]. S. H. Lewis, *et al.*, "10b 20Msample/s analog-to-digital converter, " *IEEE J. Solid-State Circuits*, vol. 27, pp. 351-358, March 1992.

[72]. Y. M. Lin, B. Kim, and P. R. Gray, "A 13b 2.5MHz self-calibrated pipelined A/D converter in 0.3 μm CMOS, " *IEEE J. Solid-State Circuits*, vol. 26, pp. 628-636, April 1991

[73]. T. Matsuura, *et al.*, "A 95mW, 10b, 15MHz low-power CMOS ADC using analog double-sampled pipelining scheme, " *IEEE Symposium on VLSI Circuits Dig. Tech. Papers*, pp. 98-99, Jun 1992.

[74]. C. S. G. Conroy, D. W. Cline, and P. R. Gray, "An 8-bit 85-MS/s parallel pipeline A/D converter in 1.5um CMOS, " *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 447-454, April 1993.

[75]. G.C. Temes, "High-accuracy Pipeline A/D Converter Configuration," *Electron. Letter.,* vol. 21, pp. 762-763, Aug. 1985

[76]. M. Yotsuyanagi, E. Etoh, and K. Hirata, "A 10-b 50-MHz pipelined CMOS A/D converter with S/H, " *IEEE J. Solid-State Circuits*, vol. 28, no. 3, pp. 292-300,March 1993.

[77]. C. W. Mangelsdorf, H. Malik, S. H. Lee, S. Hisao, and M. Martin, "A two-residue architecture for multistage ADCs," *IEEE Solid State Circuits Conference*, pp. 64-65, Feb 1993.

[78]. K. Bult and G. Geelen, "A fast-settling CMOS op amp with 90-dB DC gain and 116Mhz unity-gain frequency," *IEEE Solid State Circuits Conference*,, pp.108-109, Feb.1990.

[79]. K. Bult and G. Geelen, "The CMOS gain-boosting technique," *Analog Integrated Circuits and Signal Processing,* vol.1, no.2, pp.119-35, Oct 1989.

[80]. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed, New York, Wiley, pp. 644–652, 2001.

[81]. M. Taherzadeh-Sani, A. A. Hamoui, "Digital background calibration of capacitor-mismatch errors in pipelined ADCs," *IEEE Transactions on Circuits and Systems II, Express Briefs*, vol. 53 , no.9 , pp. 966 – 970, 2006

[82]. Xuan-Lun Huang, Yuan-Chi Yu and Jiun-Lang Huang, "Calibrating capacitor mismatch and comparator offset for 1-bit/stage pipelined ADCs," *IEEE 14th International Mixed-Signals, Sensors and Systems Test Workshop*, pp.1-6, 2008.

[83]. K. Abdelfattah and B. Razavi, "Modeling Op Amp Nonlinearity in Switched-Capacitor Sigma-Delta Modulators," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 197 – 200, Sept. 2006.

[84]. R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΣΔ A/D and D/A converters using data weighting averaging," *IEEE Transactions on Circuits and Systems II*, vol. 42, no. 12, pp. 753-762, Dec 1995.

[85]. H. Z. Hoseini and I. Kale, "Modeling of switched-capacitor delta-sigma modulators in SIMULINK," *IEEE Trans. on Instrumentation and Measurement*, vol. 54, no. 4, pp. 1646 – 1654, Aug 2005.

[86]. I. Ahmed, J. Mulder, D. A. Johns, "A 50MS/s 9.9mW pipelined ADC with 58dB SNDR in 0.18μm CMOS using capacitive charge-pumps, " I*EEE International Solid-State Circuits Conference,* pp.164 - 165, 2009.

[87]. A. Agnes *et. al.*, "A 9.4-ENOB 1V 3.8 μW 100kS/s SAR ADC with time domain comparator," *IEEE Solid State Circuits Conference*,, pp. 246-247, 2008.

[88]. MIT Lincoln Lab, "*Low power FDSOI CMOS process app notes 2006-1*,"2006.

[89]. W.Yang, D. Kelly, I. Mehr, M. Sayuk, and L.Signer, "A 3-V 340mW 14-b 75Msample/s CMOS ADC with 85-dB SFDR at nyquist input, " *IEEE J. Solid-State Circuits*, vol. 36, pp. 1931-1936, Dec 2001.

[90]. M. Dessouky and A. Kaiser, "Very low-voltage digital-audio modulator with 88dB dynamic range using local switch bootstrapping," *IEEE Journal of Solid-State circuits*, vol. 36, no. 3, pp. 349-355, March 2001.

[91]. D. Johns and K. Martin, "*Analog Integrated Circuit Design*," John Wiley and Sons, Inc., 1997.

[92]. K. Bult and G. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1379-1384, Dec 1990.