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AN EXPERIMENTAL AND ANALYTICAL STUDY OF THE MECHANISM OF MATERIAL MODIFICATION WHEN A BIAS IS APPLIED BETWEEN AFM TIP AND GOLD AND HIGHLY ORIENTED PYROLYTIC GRAPHITE

BY

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THESIS

Submitted to the University of New Hampshire

in Partial Fulfillment of

the Requirements for the Degree of

Master of Science

in

Mechanical Engineering

May, 2011

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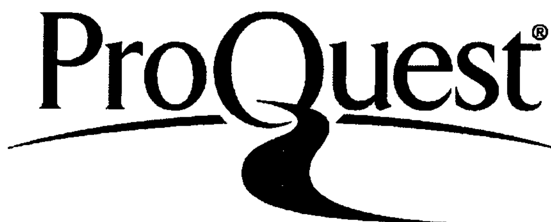

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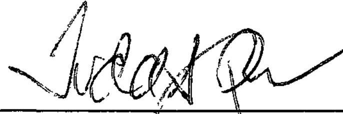

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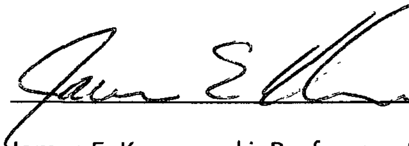

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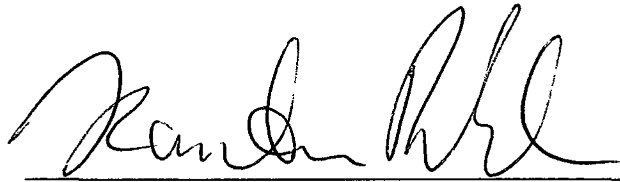

Karsten Pohl, Associate Professor of Physics

05/03/2011

Date

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ABSTRACT

AN EXPERIMENTAL AND ANALYTICAL STUDY OF THE MECHANISM OF MATERIAL MODIFICATION WHEN A BIAS IS APPLIED BETWEEN AFM TIP AND GOLD AND HIGHLY ORIENTED PYROLYTIC GRAPHITE

by

Anjali Parkhi

University of New Hampshire, May, 2011

The fabrication of nanostructures is of great importance for the continued development of nanodevices and molecular electronics. While field assisted tip based techniques are proposed to be versatile nanofabrication techniques that can be used for atomic-scale surface modification of wide variety of materials, the mechanism of material transport is not well understood. This research was performed to better understand the mechanisms of surface modification when the voltage bias is applied in ambient conditions; in particular, the conditions that Liu et al.[1,2] proposed will cause material transport.

We studied the evolution of the current voltage behavior of a doped silicon AFM tip on gold film on mica and highly ordered pyrolytic graphite (HOPG) to understand the impact of current on material modification for negative tip biases up to 10V. The SEM images of tips before and after use were compared to examine the physical changes caused to the tip and x-ray energy dispersive spectroscopy analysis was performed to study the chemical composition of used tips. We monitored modification on substrates and proposed possible mechanisms of material transport. We performed heat transfer analysis of the tip-substrate interface to show that the measured powers for negative tip biases in the range of 6 – 10 V are sufficient to raise

the temperature at the interface to as high as 100 – 1100 °C which in combination with very high electric field (> 10^8 Vm^{-1}) is sufficient to cause tip oxidation of bare silicon tip in an ambient environment and can cause diffusion, evaporation or melting of thin coatings from coated silicon tips used by Liu and Miller.[1,2]

CHAPTER 1

INTRODUCTION

Project Motivation

The synthesis or fabrication of precise nanostructures with at least one dimension in the 1 – 100 nm range continues to be an important problem in nanoscale science and engineering. As feature sizes shrink from the micron scale to the nanoscale, conventional fabrication technologies such as UV, EUV, and electron beam lithography reach their limits. Very sophisticated optical and charged beam systems are capable of delineating sub-100 nm patterns but they are not amenable to low cost, high-rate nanomanufacturing processes. Scanning probe or tip based lithography is a low cost alternative to expensive photon or e- beam techniques. A brief description of all these techniques is given in the following section.

Field assisted tip based techniques (like Field Assisted Nanopatterning[1,2]) are proposed to be versatile nanofabrication techniques that can be used for atomic-scale surface modification of wide variety of materials in vacuum or ambient conditions. A conventional atomic force microscope with no alterations can be used for patterning which is turned on or off by controlling tip bias, and the same tip is used for both patterning and imaging. Overall, the field assisted tip based techniques unique combination of abilities makes it well-suited as an inexpensive tool for nanofabrication. However, these techniques suffer from serious through-

put limitations and require development of multiple probe systems to cover large areas in manageable time. Also to meet the yield requirement, a nanofabrication technology has to be reliable, repeatable, and have the lowest defect level. Such scale up requires control of the deposition rate via an understanding of the mechanics of the tip substrate nanocontact during surface modification process. The correlation between the electrical properties, thermal properties and deformation behavior of the nanocontact is of paramount importance, yet not well understood.

This research was performed to better understand the physics of tip sample interface (or the mechanisms of surface modification) when the bias is applied in ambient conditions, in particular, the conditions that Liu & Miller proposed will cause material transport (6 – 10 V negative tip bias), so that the deposition process can be monitored and controlled.

We used experimental and analytical methods to study the correlation between the electrical, thermal, and deformation (or material modification) behavior of the nanocontact (when bias is applied) between the Si tip and HOPG and passivated Au substrates that were used in field assisted nanopatterning. We examined the physical and chemical changes to the tip at intermediate stages during our experiments to obtain a realistic understanding of the deposition process. We attempted to determine the factors influencing the rate and quality of field assisted material modification.

Conventional Lithography Methods (Top Down Processes)

Optical lithography (or Photolithography)

Principle of operation - The optical lithography uses photons for patterning. Figure 1 schematically illustrates this technique (using UV light). The laser shines ultraviolet light first

through an illuminator which homogenizes and conditions the beam and then through a photomask, which contains the pattern to be imaged onto the wafer. The projection lens reduces the photomask pattern by a factor of 4 or 5, and images in onto the photoresist (photosensitive coating on wafer). The desired pattern is transferred to wafer through an etch process. This sequence is repeated many times to complete the integrated circuit (IC).

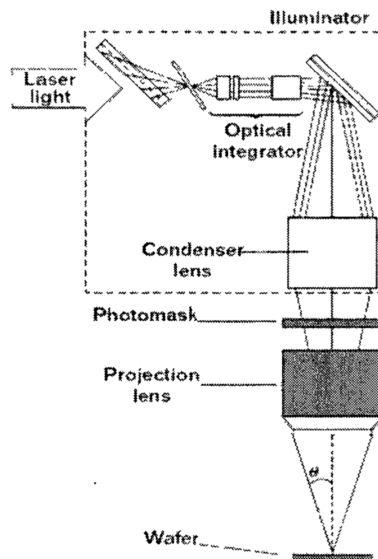

Figure 1: A schematic representation of optical lithography.

In optical lithography, feature resolution (minimal distinguishable feature size) depends on the wavelength of the photons. The light beam with shorter wavelength gives better resolution. So far, use of 157 nm wavelength is demonstrated using UV (feature size ~70-100 nm).

Capabilities and limitations - Optical lithography is the most widely used technique in the semiconductor industry for production of integrated circuits (ICs), because it has been the only technology which has the capacity of patterning over a hundred wafers per hour at desired circuit feature dimension.

As feature sizes shrink from the micron scale to the nanoscale, optical lithography reaches its limits. Though with the use of extreme UV (EUV), X-ray and resolution enhancement techniques (RETs), optical lithography was able to achieve ever-smaller dimensions; these solutions are too expensive and not easily accessible.

Electron Beam Lithography (EBL)

Principle of operation - In e-beam lithography, the pattern is written directly onto the electron-sensitive resist (called the e-beam resist) by scanning the focused beam of electron in a patterned fashion across a surface. The EBL system does not need a mask to project the pattern. The electron beam transfers the energy into a substrate material to perform structuring either by exposure of energy-sensitive polymer materials or by removing material directly. The technique is schematically illustrated in figure 2.

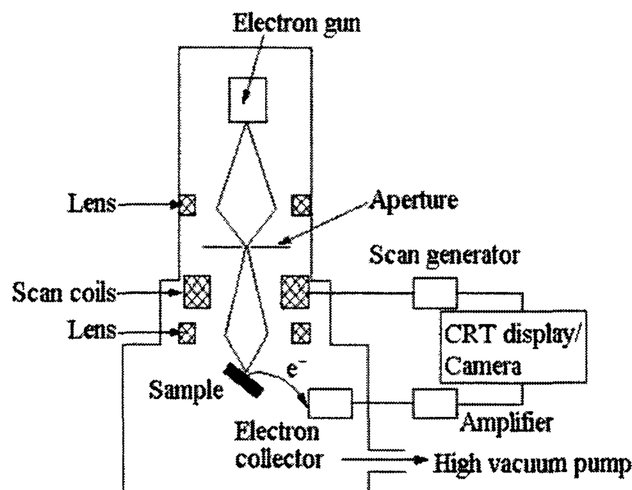

Figure 2: A schematic representation of E-beam lithography.

Capabilities and limitations - The EBL offers much higher resolution than optical lithography, based on the fact that they do not have the diffraction limitation associated with

the optical lithography. Very sophisticated e-beam systems can fabricate structures with less than 10 nm dimensions.

Although e-beam lithography is able to pattern sub-100 nm features easily, it is not practical for volume manufacturing of ICs because of its low throughput and high cost. EBL has found wide usage in photomask-making used in photolithography, low-volume production of semiconductor components, and research & development.

Tip-based Nanofabrication Methods

Tip-based techniques use scanning probes for various types of nanofabrication, either optically, chemically or mechanically. A scanning probe microscope (Scanning tunneling microscope (STM) or Atomic force microscope (AFM), figure 3) is used as a tool for surface modification.

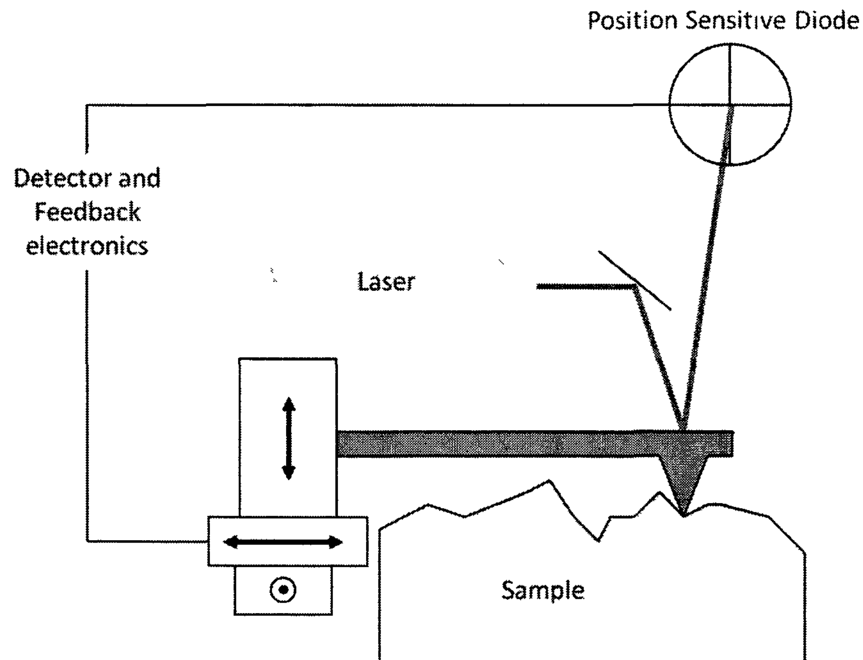

Figure 3: A schematic representation of AFM.

Principle of Operation of an AFM

AFM consists of a micro machined cantilever with sharp tip (typical tip radius is from a few to 10s of nm) on end which is brought into proximity of a sample surface by piezoelectric translators. The deflections of the cantilever due to tip-substrate interatomic forces (mechanical contact force, Vander Waals forces, capillary forces, chemical bonding, and electrostatic forces) are detected by reflecting a laser beam from the top surface of the cantilever on to a position sensitive photodiode. With the spring constant of the cantilever known, the tip-substrate force can then be obtained according to Hooke's law. While maintaining a constant tip-substrate force by feedback control of the piezoelectric translator, the tip is scanned over the substrate surface. The surface topography is determined from the voltage applied to translator to keep cantilever deflection (or force) constant. The principle of operation of AFM is schematically illustrated in figure 3.

Capabilities and limitations of Tip based Methods - Most low cost, high-rate nanomanufacturing processes will require bottom-up methodologies whereby molecules, polymers and other nanoelements self-assemble in predictable ways to form precise structures. The tip based methods have capability to develop nanotemplates, which can act as platforms to direct the self-assembly of nanoelements into controlled patterns.

These methods are not suitable for high-rate manufacturing in their current form of existence.

Dip-Pen Nanolithography (DPN)

Dip-Pen Nanolithography (DPN) is a scanning probe nanopatterning technique in which an AFM tip is used to deliver molecules to a surface via a water meniscus (which naturally forms in the ambient atmosphere). The inks (or molecules) are first coated on the tip via vapor coating or dip coating techniques, and then transferred to the substrate through diffusion process.

This direct-write technique offers high-resolution patterning capabilities but is largely confined to the transfer of liquid thiols[3] and electrochemical-DPN to the transfer of water soluble metallic salts[4] and polar monomers[5].

Mirkin's group at Northwestern University recently reported that they used 55,000 passive pen (or tip) array (Figure 4) where each pen occupies a 90 μm by 20 μm area[6]. They used this array to deposit ~80 nm dots of 1-octadecanethiol (ODT) as well as other patterns. Each cantilever is compliant enough to accommodate the small angular misalignment between the pen array and the substrate.

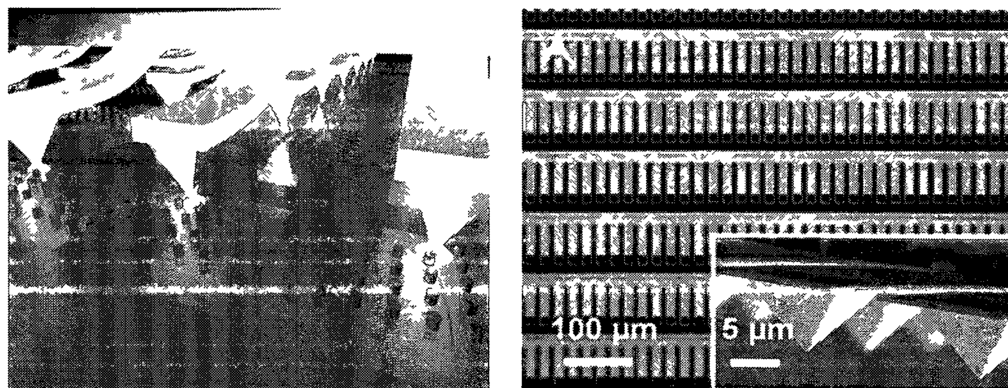

Figure 4 Massively parallel DPN with 55000- pen two dimensional arrays [6]

Field Assisted Nanopatterning (FAN)

Liu and Miller recently demonstrated the ability to selectively deposit 40-250 nm wide lines of several solid or liquid organic and inorganic molecules by applying a negative tip bias (6-10 V) at tip speeds of 100-500 nm/sec and tip force of ~2 nN in ambient conditions. They term their method, field assisted nanopatterning (FAN). Figure 5 shows the schematic representation of FAN. This technique while similar to dip pen lithography differs in that deposition only occurs when the bias is applied even though the tip is in contact with the substrate. They showed that the width and thickness of the lines increase monotonically with increasing negative tip bias or decreasing fabrication speed (Figure 6 and 7). They reported that no deposition was observed for positive tip bias.

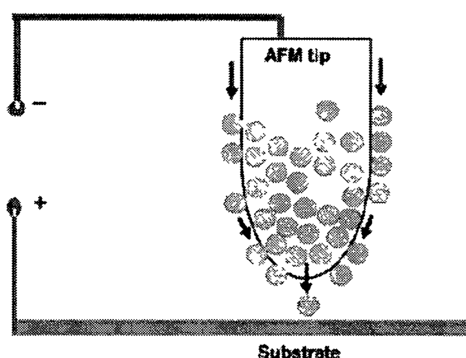

Figure 5: A schematic representation of field-assisted nanopatterning using an AFM tip.[1]

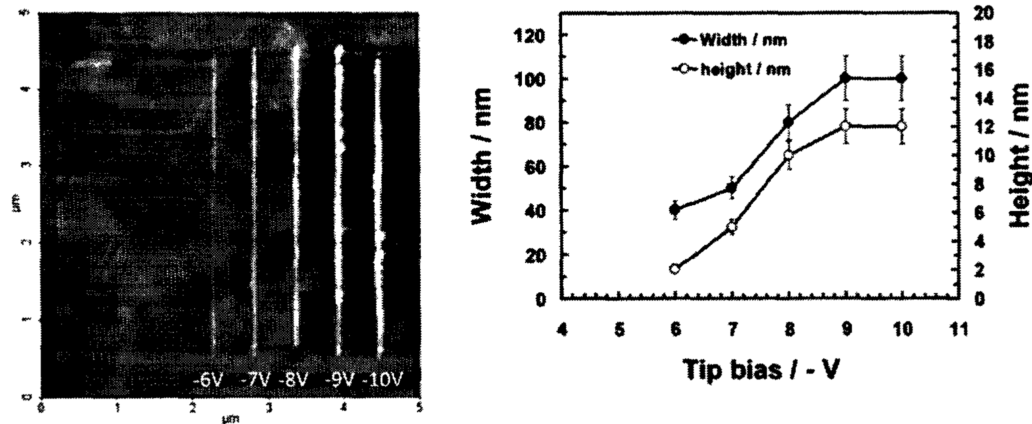

Figure 6: Field- assisted nanopatterning of [60]fullerene nanolines on octadecanethiol-coated Au[1]. The lines were fabricated using tip bias values of -6, -7, -8, and -10 V and a fabrication speed of 100 nm/s.

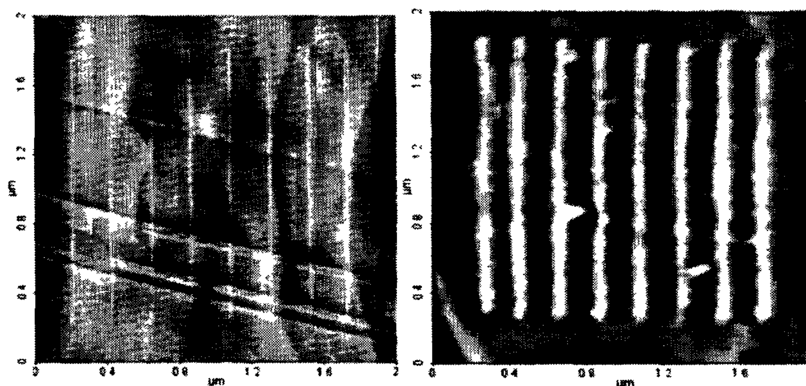

Figure 7: Field- assisted nanopatterning of Polyaniline on HOPG[1]. The lines were fabricated at a tip bias of -8 V and with fabrication speeds of 500 nm/s (left) and 100 nm/s (right).

The coatings (naphthalene, [60]fullerene, N-methylpyrrole, poly-3-octylthiophene, polyaniline, meso-tetraphenylporphyrin, MnO_2, ZnO, Fe, Fe_3O_4, and $MgCl_2$) were applied to soft (0.6 N/m) highly doped Si (0.01 – 0.05 Ω cm) AFM tips using solution or suspension evaporation methods after cleaning using UV light (3-4 Hr) followed by an ethanol rinse. All substrates were conductive (highly ordered pyrolytic graphite (HOPG), gold (Au), ODT-passivated Au, and indium-tin oxide (ITO)). A freshly exposed HOPG substrate was obtained by pulling a layer off

with tape. The Au substrates were flame-annealed in hydrogen and quickly coated with ODT to passivate the surface. The ITO surfaces were cleaned with ethanol prior to use.

Liu & Miller reported following advantages of FAN over other tip based lithography techniques like DPN:

1. The tip does not need to be lifted off the substrate to stop printing.
2. The same tip is used for both nanofabrication and imaging.
3. Pattern dimensions can be controlled by tuning tip bias and tip moving speed during fabrication.
4. A standard AFM with no alterations can be used.
5. The deposition rates and feature size are independent of humidity.

Summary of Important Observations Made by Liu & Miller (FAN)

1. There is no deposition in the absence of a tip bias.
2. There is no deposition when an uncoated tip is used.
3. FAN successfully nanopatterned on HOPG for relative humidities (RH) in the range of 0 to 80 %.
4. The dimensions of nanopatterned features are a function of either tip speed with feature heights ranging from less than one nm to greater than 20 nm.
5. The HOPG substrate produces the most uniform, continuous nanoscale features followed by ITO, passivated Au, and finally Au.
6. The semivolatile liquid N-methylpyrrole (bp 111-113 °C) was deposited onto HOPG using FAN and the resulting nanopatterns were observed to slowly disappear over a few hours

7. Nanopatterns created using nonvolatile organic and inorganic materials do not disappear.
8. Nanopatterned [60]fullerene is observed to slowly shrink and in some cases completely disappear upon addition of either toluene or diethylenetriamine, both of which dissolve [60]fullerene
9. [60]-fullerene monolayers created using FAN have measured heights of 0.9-1 nm, consistent with the diameter of [60]fullerene.
10. Monolayers of meso-tetraphenylporphyrin deposited on HOPG have measured heights of 3-4 Å, consistent with porphyrin molecules lying flat on the HOPG surface to achieve maximum π-π stacking interactions.
11. Monolayers of PANI deposited on HOPG also have measured heights of 3-4 Å, consistent with PANI molecules lying flat on the HOPG surface to achieve maximum π-π stacking interactions.
12. FAN is capable of creating multilayer nanostructures.

Literature Review of Tip-Substrate Interactions when a Bias Exists Between Tip and the Substrate

This section describes the observations made by other researchers when a bias is applied between different tip substrate combinations. Many researchers reported material transport from the uncoated tips which is in contrast to the claims of Liu et al.[1,2].

Multiple investigators have demonstrated that they can create lines and dots with nanoscale dimensions in ambient and vacuum conditions when a voltage bias is applied between a scanning probe microscope (SPM) tip and a substrate. The electrical behavior during

field induced surface modification using SPM tips in ambient conditions has also been reported by many investigators (described in subsequent paragraphs).

Song et al.[7] created gold nanostructures on graphite by applying negative voltage pulses of 0-20V for 0.2- 300 msec to gold coated silicon tips in air. The threshold voltage for mound formation was -5V and increased with repeated pulses. The contact resistance increased from 3 kΩ to 10^{11} Ω with repetitive cycling which gives currents in the range of 200 pA to ~7 mA. They attributed the resistance increase to the depletion of gold coating and attributed the mechanism of deposition to field evaporation of negative gold ions from the tip apex.

Schneegans et al.[8] obtained I-V curves for n-doped silicon tips and copper sample for negative tip bias of 0-3V in air. The resistance ranged from 5- 8 kΩ at different points on the sample and decreased to 2 kΩ after repetitive scanning of tip over the surface, giving currents on the order of 0.4- 1.5 mA. They did not propose a reason for the evolution of resistance.

Guo et al.[9] investigated the nanocontacts between a W_2C-coated tip and granular gold film under a small load (~5 nN) and found that the contact resistance changed between 400 MΩ and 10 GΩ (current range of 1-25 nA) for constant negative sample bias of 10 V at a fixed surface location for 45 min in air. No current was recorded after 45 min. They observed a reduction in current fluctuation for large forces (150 nN) and attributed it to improved electrical contact but the contact resistance was still very high.

Wolf et al.[10] obtained I-V data for high applied loads (50- 260 μN) using a diamond tip and n-type Si substrate. The current increased in the range of 5 nA to 60 μA (resistance range of 300 MΩ to 25 kΩ) with increase in the load for 1.5 V. These studies imply that very high loads (on the order of few μN) can substantially influence the resistance of the nanocontact and small

load (on the order of few nN) can influence the stability of the electrical contact without affecting the resistance.

Similar I-V measurements were performed by Lantz et al.[11] in vacuum. They observed significant decrease (135 GΩ to 35 GΩ) in resistance of the silicon tip and HOPG interface when the tip was reused after sputter cleaning, indicating the presence of insulating contamination layer on the Si tip initially. They also reported substantial decrease in resistance when the same tip was used with copper substrate (35 GΩ to 40 MΩ). The current for a Si tip with copper was on the order of 25 nA for 1 V positive sample bias for applied force of 10 nN.

Koyanagi et al.[12] deposited gold dots of 100 nm diameter and 10 nm height from a gold-coated SiO_2 tip on thin SiO_2 film by applying pulsed voltages of either polarity under 100 V for 0.001-10 ms in vacuum (figure 8). They found that the threshold field for negative tip bias (1.3 V/Å) is lower than that of positive bias (2.5 V/Å). These values are larger than those obtained in STM experiments by Mamin et al.[13] and is attributed to the presence of insulating film on the sample surface. They proposed that material transport occurred by field (electric) evaporation of Au atoms.

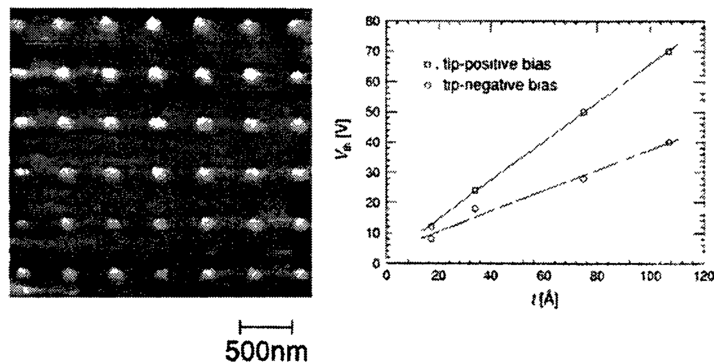

Figure 8: Field evaporation of Au atoms on SiO2 film by using an atomic force microscope.[13]

Park et al.[14] produced ~90 nm wide and ~15 nm high mounds on Au surface using a W_2C coated tip in vacuum (Figure 9). The tip bias in the range of 0 to -40 V was only applied when the

tip was above the surface. They were able to accomplish this by applying the bias in intermittent contact mode when the tip was above the surface. The current was ~ 65 pA for -40 V tip bias. They proposed that surface modification occurred by field emission induced local heating and concurrent field-induced diffusion. However, such a mechanism is very unlikely since the temperature rise caused by the field-emitted electrons in the experiment described by Park et al. estimated using linear heat flow equation[15] is less than 1K, which is not sufficient to modify the surface by diffusion.

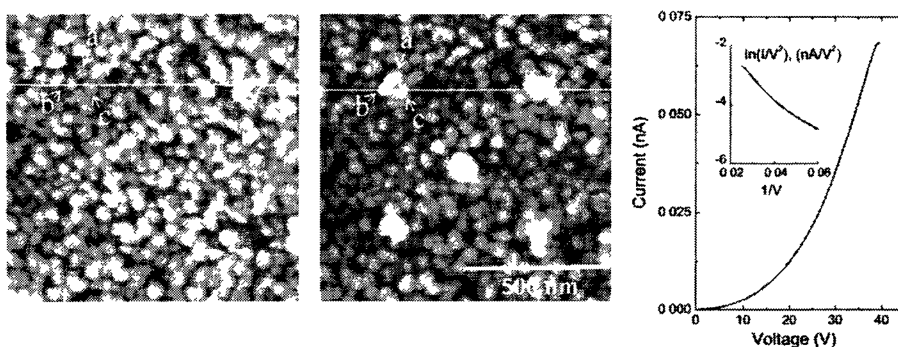

Figure 9: Field emission induced fabrication of nanostructures on Au thin films using a noncontact mode atomic force microscope.[14]

Most of the previous studies reported pit or groove formation on HOPG surface when a bias was applied between a SPM or STM tip and the substrate under ambient conditions. Jiao et al.[16] formed grooves on HOPG using a conductive Ti-Pt AFM probe for negative tip bias in the range of 6-10 V. The etch line depth increased exponentially with the increasing magnitude of tip bias. They attributed groove formation to the reaction of the carbon atoms with the H^+ and OH^- ions which are disassociated from H_2O molecules by the injection of electrons from the tip to the substrate. Kondo et al.[17] etched graphite at -2.3 V in air during their STM experiments using Pt and tungsten tips. They proposed surface modification occurred by oxidation of graphite with adsorbed water induced by tunneling electrons. Park et al.[18] produced holes of 10 nm diameter and 0.34 depth on HOPG using metal coated Si tip with negative pulse voltage of 10 V to the tip.

They measured currents on the order of several hundred μA for voltage range of 0 to 3V. The current decreased with repeated measurements.

Some investigators observed raised features on HOPG and attributed it to material transport from the tip when the bias was applied. Liu and Miller[1, 2] reported that they could create 50-250 nm wide, 2-15 nm thick lines onto HOPG by applying a negative bias to SPM tips dip-coated with a broad array of organic and inorganic molecules. They showed that the width and thickness of the lines increase monotonically with increasingly negative tip bias starting from a bias of approximately 6 V. No deposition was observed for a positive tip bias. They proposed material transport occurred by field evaporation where a threshold ionization and ejection potential exists for each molecule. Similarly, Song et al.[7] created gold nanostructures on HOPG by applying negative voltage pulses of 0-20V for 0.2- 300 msec to gold coated silicon tips in air. The threshold voltage for mound formation was -5V and increased with repeated pulses.

Jiang et al.[19] reported formation of both bumps and pits with Rh-coated AFM tip in the voltage range of 0 to 10V (negative tip bias) under ambient conditions. They concluded bump formation was due to straining of the topmost layer of HOPG. On increasing the amplitude or duration of the voltage, the bumps converted into pits. The features were observed only when the current was nearly zero even at high voltage. Zhang et al.[20] observed raised features on HOPG due to expansion of graphite lattice during anodic oxidation experiments performed using STM in dilute sulfuric acid.

Kondo et al.[17] etched graphite at -7.2 V tip bias in vacuum during their STM experiments using Pt and tungsten tips. They proposed the mechanism is sublimation of graphite induced by tunneling electrons. They indicated that the threshold voltage for surface modification is linearly dependent on the binding energy of the substrate.

CHAPTER 2

EXPERIMENTAL AND ANALYTICAL METHODS

The following sections will provide details about the heat transfer analysis methods, experimental methods, tips, substrates and instruments we used and our calculation methods.

Heat Transfer Modeling: Methods and Assumptions

A heat transfer study was performed to estimate the maximum temperature rise at the tip-substrate nanocontact as a function of power input. We hoped to:

1. Determine minimum power input to the nanocontact necessary to cause tip melting or thermal oxidation.
2. Predict the impact of temperature rise on tip coating material for conditions used in field assisted nanopatterning[1,2].

Two independent 2D axysymmetric models of Si AFM tip and substrate (gold film on mica and HOPG) were created using Marc Mentat finite element software. The power was applied to a small area on the apex of the tip to understand thermal response if heat transfer due to the substrate was neglected. Similarly, the power was applied to the substrate to understand thermal response if heat transfer due to the tip was neglected. Heat transfer to the environment was neglected for both cases. The thermal resistances for the tip and the substrate were

independently calculated using finite element models and the temperature rise at the nanocontact was estimated by assuming that the two thermal resistances acted in parallel. The following sections describe our heat transfer analysis method in detail.

Case I: Power Applied to the Tip Apex (Substrate is Neglected)

We performed a finite element analysis to estimate the maximum temperature rise associated when power was applied only to the tip. We assumed that the power from Joule heating was applied to a 10-50 nm radius on the apex of the tip and that there was no heat loss to the environment.

Model Construction of Si Tip and Meshing

An AFM probe consists of a micro machined cantilever with sharp tip on end. We constructed a 2D axysymmetric model (about X-axis) for tip. The advantage of 2D model over 3D models is that 2D models simplify the modeling and saves computing time. Modeling in 2D reduces the number of elements in the mesh, hence, avoids round-off error associated with large 3D models. We modelled the cuboidal cantilever as a cylinder with same cross sectional area (~ 50 μm^2). Since we assumed that there was no heat loss to the environment (heat transfer independent of surface area), our 2D cylindrical axisymmetric model closely represented the 3D tip but with much fewer elements. The tip was modeled as a truncated cone (full tip cone angle, $2\theta \sim 40^{\circ}$) with a hemisphere of ~ 50 nm radius (R) on end (Figure 10). The tip radius increases with usage (discussed later). Based on our observations of physical changes to tip, we chose the intermediate value of 50 nm, so that our model can be used for all conditions without changing the tip model dimension. Also, the resistance calculated using the Sharvin's formula for 50 nm radius is in the range of resistance observed by us during I-V measurements

(See Appendix G for contact resistance calculation). The total tip height (H) and cantilever length was taken as 20 µm and 130 µm respectively. Figure 11 shows the 2D axysymmetric model of the AFM tip.

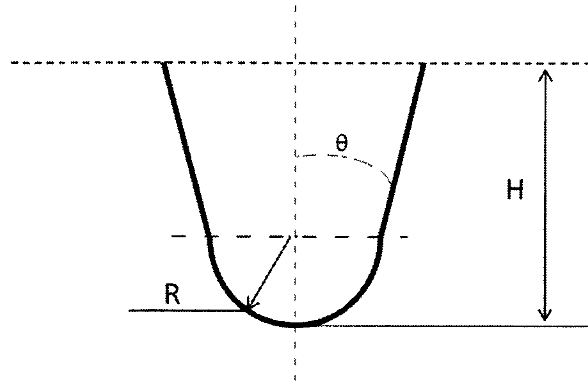

Figure 10: Schematic of FE axisymmetric model of an AFM tip. The tip is modeled as a truncated cone (full tip cone angle, 2θ~ 40°) with a hemisphere of ~ 50 nm radius (R) on end.

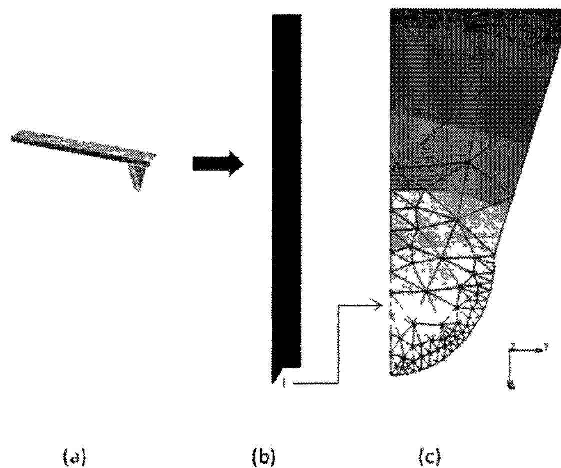

Figure 11: (a) AFM tip, (b) 2D axisymmetric finite element model of the tip. The model is axisymmetric about X-axis. All elements are three node triangular solid heat transfer type, and (c) Enlarged view of tip apex.

We meshed our 2D axisymmetric model with three node triangular elements (figure 11). The smaller the size of the elements, the more realistic the model simulation. We used small sized elements near the tip apex to get realistic results for temperature rise at the nanocontact.

Larger size elements were used for rest of the model to optimize the computing time and avoid round-off errors associated with large number of elements. The geometric properties of all the elements were defined as axisymmetric –solid-heat transfer type.

Material Properties

We assigned the thermal material properties of silicon to all elements in the mesh. The values of specific heat and mass density were taken as 0.707 $Jg^{-1}K^{-1}$ and $2.2X10^{6}$ gm^{-3} respectively. We included the temperature dependence of thermal conductivity of silicon[21] in the model. The relationship between the conductivity of silicon (K) and temperature rise (T) was established by using the conductivity versus temperature curve obtained by Grassbrenner et al.[21] (See Appendix A: Temperature dependence of thermal conductivity of Si). The conductivity was entered as a temperature dependent variable in our model and the relationship is given by:

$$K = \frac{301567}{(T)^{1.332}} \tag{1}$$

Another consideration is the nanoscale dimension of the contact. The dominant mechanism of heat transfer in Si is by phonons because of the low density of charge carriers. Since the mean free path of a phonon in Si is on the order of 20 nm (See Appendix B: Thermal conduction in Si), our continuum model is on the border of being a good estimate. However, the number of charge carriers increases dramatically at higher temperatures resulting in shorter mean free paths and the continuum assumption becomes more appropriate.

Initial and Boundary Conditions

We assumed that all nodes are initially at room temperature (T_i = 300 K). Since the model is axisymmetric about x-axis, all edges on x-axis were insulated (adiabatic boundary condition). The power flux was applied to a 10-50 nm radius on the tip apex. The top edge (cantilever end) was maintained at initial temperature ($T = T_i$ = 300 K, $\Delta T = 0$) because it is attached to massive conductive mass and acts as infinite sink. Also, it is distant from the heat source. We also assumed that no heat was transferred due to ambient air and therefore adiabatic boundary conditions were assigned to all remaining edges. The assumption of adiabatic boundary conditions will result in an overestimate of the temperature rise. A schematic diagram of the 2D axisymmetric model of the AFM tip with all boundary conditions is shown in figure below.

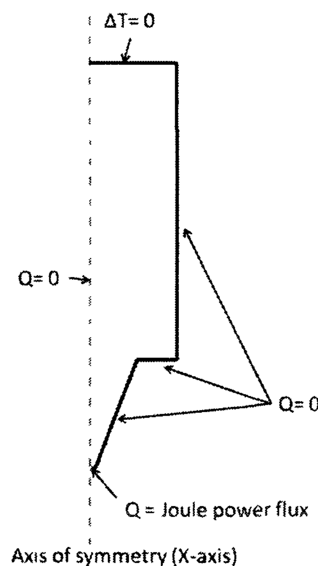

Figure 12: Schematic of the AFM tip showing all boundary conditions. The power flux was applied to a 50 nm radius on the tip apex. The top edge is maintained at initial temperature (ΔT=0). Adiabatic boundary conditions (heat transfer, Q=0) are applied to remaining edges.

Computation of the Temperature Rise and Thermal Resistance of the Tip

Steady state conduction is a form of conduction that happens when the temperature difference driving the conduction is constant, so that after an equilibration time, the spatial distribution of temperatures in the conducting object does not change any further. Since the

temperature in the tip change with time and it is important in this case to estimate how quickly the tip would heat up, we performed transient heat transfer analysis. The total loadcase time was taken as 1 μs with hundred constant time steps of 10 ns.

The power applied to the tip apex was varied from 0.5 mW to 3 mW to estimate the maximum temperature rise at the nanocontact as a function of power input. The plot of maximum temperature rise vs. power is included in this chapter because it is used as an intermediate step to calculate overall thermal resistance and hence the actual temperature rise. Figure 13 shows the steady state temperature rise at the tip apex as a function of power input. The time constant for the temperature rise is ~20-50 ns. The model is not valid beyond the point where temperature rise reaches melting point of silicon.

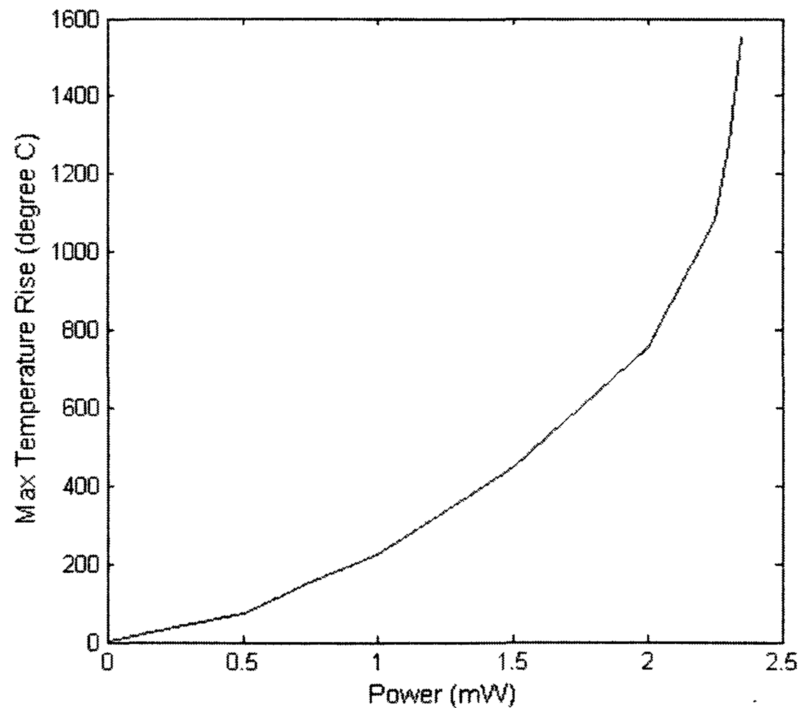

Figure 13: Steady state temperature rise at the tip apex as a function of power input when heat transfer due to substrate is neglected.

We used data from figure 13 to calculate the thermal resistance of the tip (R^{t}_{tip}) using the following formula:

$$R^{t}_{tip} = \frac{\Delta T_t}{Q} \quad (2)$$

where ΔT_t is the temperature rise at the tip apex (K) and Q is the applied power (W). The thermal resistance of Si varies with temperature (or power) because of the change in the thermal conductivity of silicon with temperature rise. To establish a relationship between the thermal resistance and the applied power, we plotted the values calculated from equation (2) against power (figure 14) and fitted the data by an exponential function as shown in the figure below.

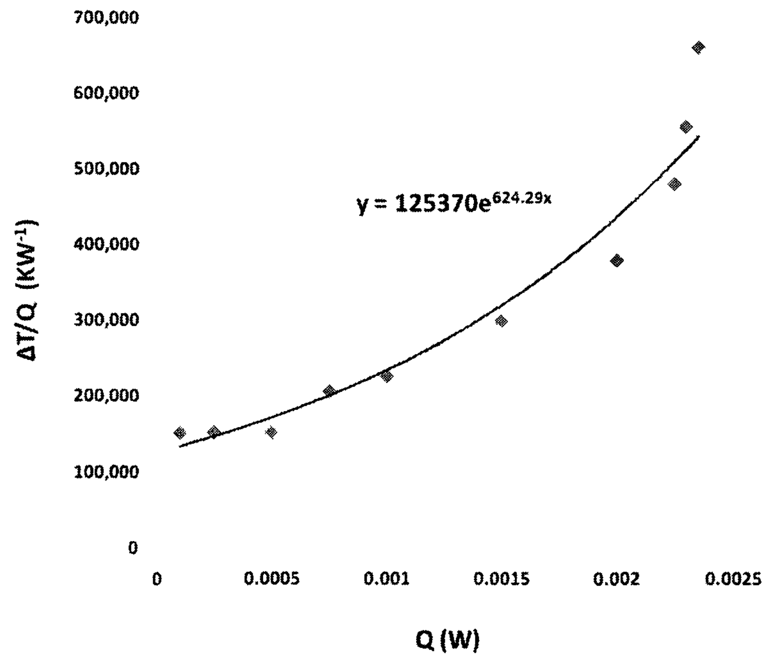

Figure 14: Thermal resistance of Si tip as a function of power input. The data is fitted by an exponential function.

The varying thermal resistance was then calculated as a function of power using the following equation:

$$R_{tip}^{t} = \frac{\Delta T_t}{Q} = 125370e^{624.29Q} \quad (3)$$

We realize that this is not a very good fit at the higher power. However, the thermal resistance of the tip is very high as compared to the substrate at powers greater than 2 mW and does not affect the overall thermal resistance at the higher power (because both resistances act in parallel).

Case II: Power Applied to the Substrate (Tip is Neglected)

We performed a finite element study to estimate the maximum temperature rise when power was applied only to the substrate. We assumed that the power from Joule heating was applied to a 10-50 nm radius at the center of the substrate and that there was no heat loss to the environment.

Model Construction of Gold and HOPG Substrates and Meshing

We constructed two independent finite element models for gold and HOPG substrates. We used axisymmetric models (about X-axis) for simplicity and, since we assumed that there was no heat loss to the environment, modelled the substrates as cylinder. The real dimensions of both the samples are infinitely large compared to the size of the nanocontact (~10-50 nm radius). It was not necessary to build a huge mesh with the real size of the sample since the elements far from the heat source have negligible influence on the temperature rise at the nanocontact. We constructed a mesh that consisted of a 1 µm thick gold film on 5 µm thick mica with a radius of 5 µm (fig. 15 (a)). Similarly, 6 µm thick model of HOPG substrate with a radius of 5 µm was constructed (fig 15 (b)).

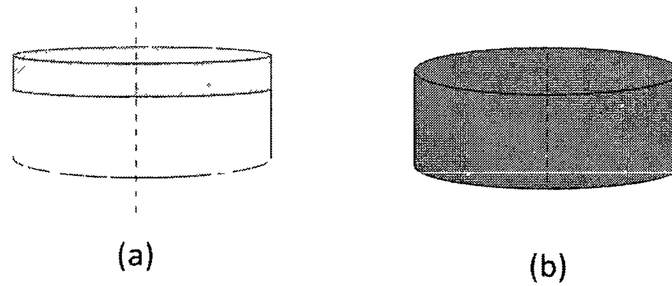

Figure 15: Schematic of (a) gold film on mica substrate (1 μm thick gold film on 5 μm thick mica with a radius of 5 μm), and (b) HOPG Substrate (6 μm thick model of HOPG substrate with a radius of 5 μm).

We meshed our 2D axisymmetric model with four node quadrilateral elements. We used small sized elements near the tip contact region to get realistic results for temperature rise at the nanocontact. Larger size elements were used for rest of the model. The geometric properties of all the elements were defined as axisymmetric –solid-heat transfer type.

Material Properties

Gold substrate - We assigned the thermal material properties of gold to the elements within 1 μm thick layer from top surface as shown in figure 16. The thermal properties of mica were assigned to the remaining elements. The values of specific heat and mass density were taken as 0.13 $Jg^{-1}K^{-1}$ and $19.3X10^6$ gm^{-3} for gold[22] and 0.5 $Jg^{-1}K^{-1}$ and $3 X 10^6$ gm^{-3} for mica[23,24] respectively. The thermal conductivity of thin gold films is slightly lower than the bulk values even if the thickness exceeds the electron mean free path.[25] Therefore we considered a range for the conductivity of gold (200 – 300 $Wm^{-1}K^{-1}$) in our model. The thermal conductivity of mica was taken as 0.71 $Wm^{-1}K^{-1}$. The thermal conductivity of gold and mica are assumed to be constant with temperature rise.

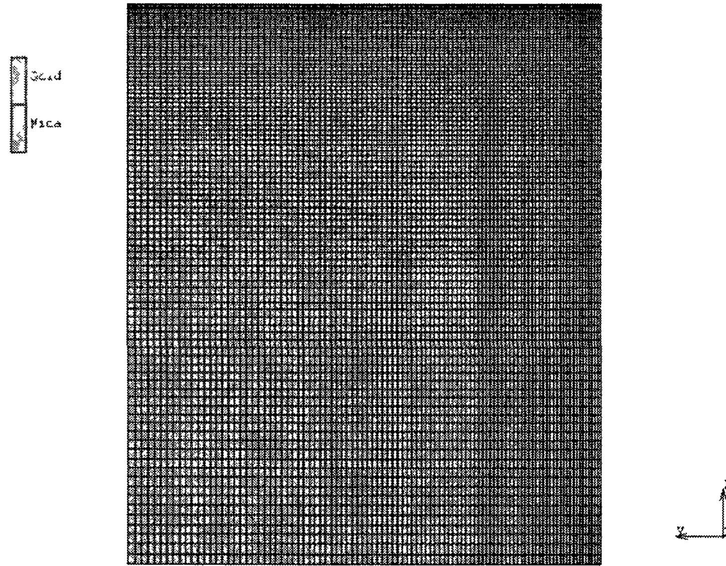

Figure 16: 2D FE model of Gold Substrate. The model is axisymmetric about X-axis. All elements are four node quadrilateral solid heat transfer type.

HOPG substrate - We assigned the thermal material properties of HOPG to all elements in the mesh (figure 17). The values of specific heat and mass density are taken as 0.710 $Jg^{-1}K^{-1}$ and $2.2X10^{6}$ gm^{-3} respectively[26,27]. Because of the anisotropic nature of HOPG, the thermal conductivity is different in different directions. The in-plane and perpendicular to plane thermal conductivities of HOPG are taken as 1800 $Wm^{-1}K^{-1}$ and 8 $Wm^{-1}K^{-1}$ respectively (manufacturer specified). The thermal conductivities for HOPG are assumed to be constant with temperature rise.

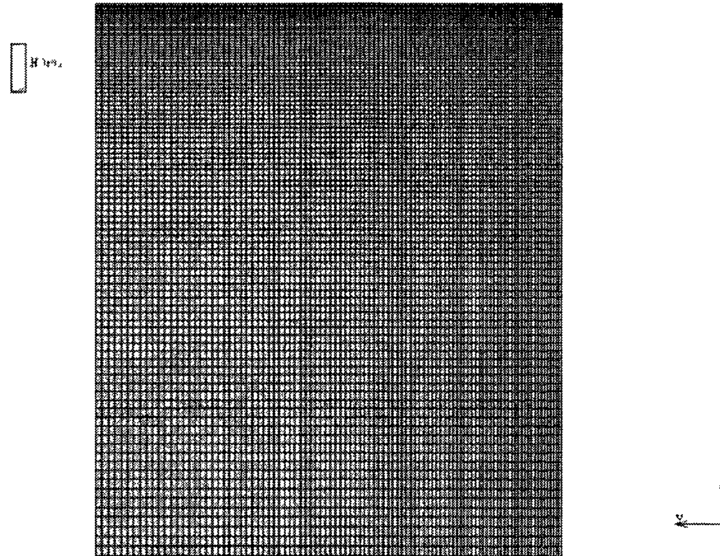

Figure 17: 2D FE model of HOPG substrate. The model is axisymmetric about X-axis. All elements are four node quadrilateral solid heat transfer type.

Initial and Boundary Conditions

We assumed that all nodes are initially at room temperature (T_i = 300 K). Since the model is axisymmetric about x-axis, all edges on x-axis were insulated (adiabatic boundary condition). The power flux from Joule heating was applied to a 10-50 nm radius at the center of the substrate (on top surface). We assumed that no heat was transferred due to ambient air and therefore adiabatic boundary conditions were assigned to the remaining edges on top surface. The assumption of adiabatic boundary conditions will result in an overestimate of the temperature rise. All remaining edges were maintained at initial temperature ($T = T_i$ = 300 K, $\Delta T = 0$) because they are distant from the heat source. Figure 18 shows a schematic representation of applied boundary conditions.

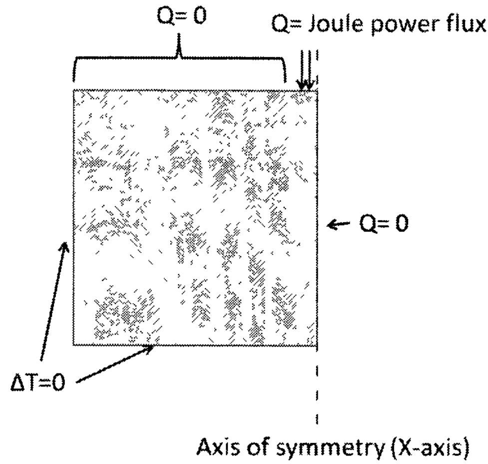

Figure 18: Schematic model of substrate showing boundary conditions. The power flux was applied to a 50 nm radius on the substrate. Adiabatic boundary conditions (heat transfer, Q=0) is applied to the top edge. The remaining edges are maintained at initial temperature (ΔT =0).

Computation of the Temperature Rise and Thermal Resistance of the Substrate

We performed transient heat transfer analysis for both substrates. The total loadcase time was taken as 1 μs with hundred constant time steps of 10 ns. The power applied to the substrate was varied from 0.5 mW to 20-25 mW to estimate the maximum temperature rise at the nanocontact as a function of power input.

The steady state temperature rise on the gold and HOPG substrates as a function of power is shown in figure 19 and 20. The thermal time constant for gold and HOPG substrates are on the order of 450-500 ns and 50-70 ns respectively. The thermal resistance of the gold and HOPG substrate remains constant with changing power and is calculated using the following formula (or slope of the curve):

$$R_{sub}^{t} = \frac{\Delta T_s}{Q} \qquad (4)$$

where Q is the power applied (W) and ΔT_s is the temperature rise at the substrate (K) associated with it.

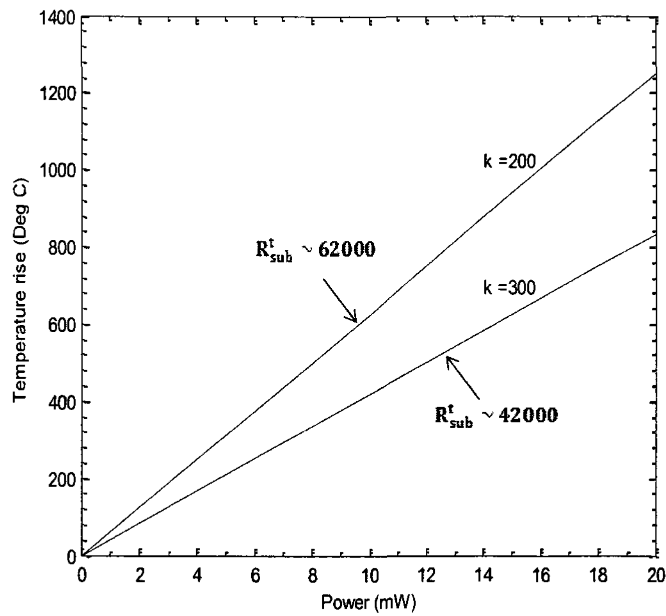

Figure 19: The steady state temperature rise on the gold substrate when heat transfer due to the tip is neglected. A range for thermal conductivity of gold (k = 200- 300 $Wm^{-1}K^{-1}$) is considered in the model. The slope of the curve gives the thermal resistance of gold substrate, R^{t}_{sub}.

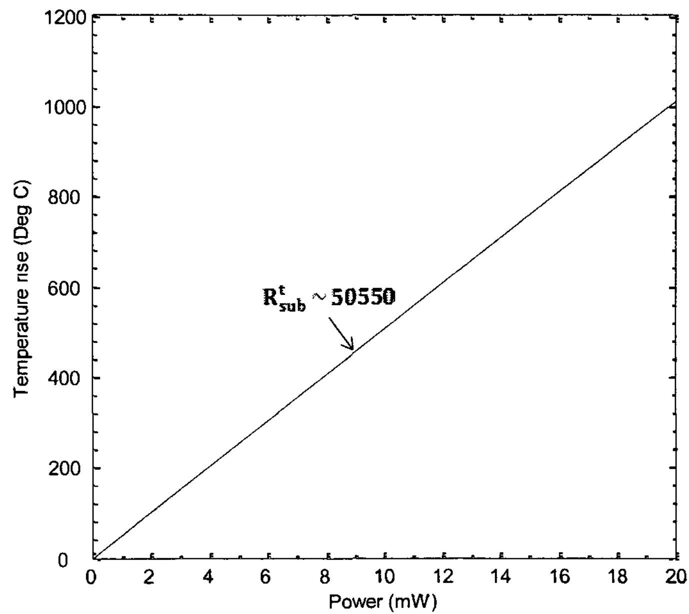

Figure 20: The steady state temperature rise on the HOPG substrate when heat transfer due to the tip is neglected. The slope of the curve gives the thermal resistance of HOPG substrate, R^{t}_{sub}.

Case III: Combined Effect of Tip and Substrate on the Temperature Rise

We estimated the actual temperature rise at the interface by using thermal-electrical analogy for the tip and substrate system. We assumed that the Joule heat was applied to a system consisting of two thermal resistances (tip and substrate) in parallel. We used the individual finite element models to calculate the thermal resistances of the tip and the substrate (described in previous sections).

We estimated the overall thermal resistance of the tip substrate system by using the thermal-electrical analogy of parallel resistors (equation 5).

$$R^t_{system} = \frac{R^t_{tip} R^t_{sub}}{R^t_{tip} + R^t_{sub}} \quad (5)$$

The temperature rise at the tip substrate interface was then calculated using the following formula:

$$\Delta T_{interface} = R^t_{system} Q \quad (6)$$

The power applied to the tip apex was varied from 0.5 mW to 20 mW to estimate the temperature rise at the nanocontact as a function of power input. The steady state temperature rise at the nanocontact as a function of power is shown in figure 34 and 35 in results and discussion chapter.

Experimental Methods

Tip and Substrate Preparation

Tip – We used the same probe used in Liu and Miller's experiments – highly doped Si (n-type) with a nominal spring constant of 0.6 N/m and specific resistance of 0.01-0.05 Ω cm

manufactured by Micromasch (See Appendix C: AFM tip used in our experiments (for dimensional details)). The probes were prepared by exposing them to ultraviolet light for 3-4 hours to help remove any adsorbed organic contaminants followed by rinsing with ethanol and air drying.

We also used the fullerene[60] coated tips for our experiments. The coating was applied to the same type of Si tip (Micromasch) using solution evaporation (solution used was C60 dissolved in toluene) methods after cleaning using UV light followed by an ethanol rinse.

Substrates - We used gold films on mica substrates supplied by Molecular Imaging. The Au surfaces were flame annealed in propane to form terraces. Self-assembled monolayers of 1-octadecanethiol (ODT) on the Au were deposited by immersing the freshly annealed gold thin films into 1 mM ODT solutions in ethanol for at least 24 h. Prior to use, the ODT- coated monolayers were rinsed with ethanol and blown dry with air.

We also used an HOPG substrate supplied by Micromasch. A freshly exposed HOPG surface was obtained by pulling a layer off with tape.

I-V Measurement: Conditions, Equipments and Methods

We performed I-V measurements for tip bias in the range of -10 to 10 V in ambient conditions for stationary as well as moving tips (100 -500 nm/sec). The I-V data was captured using two different methods (voltage ramp and static voltage) as described in the following section. The tip was in contact with the substrate and the tip force was in the range of 2- 50 nN.

I-V Ramp measurements

Current-voltage (I-V) curves were obtained using a Veeco Dimension 3000 atomic force microscope (AFM) with a conductive AFM module (CAFM) option while the tip was held stationary at a force of 20-50 nN based on deflection of the tip. The tip bias was ramped from

zero to -10V at a rate of 5V/s. The approximate current resolution for the CAFM module is on the order of several pA with a maximum range of 500 nA. The frequency response of the CAFM was on the order of 1 kHz.

The I-V curve for each tip-sample position was captured when the curve stabilized at a given position.

Static voltage (I-t) measurements

Current vs time (I-t) data at constant tip bias (-10 to 10 V) was obtained while the tip was traversed across the surface at velocity of 100-500 nm/sec (the same as used by Liu and Miller) at a force of 2-50 nN with a Veeco Multimode AFM. A 560 ohm resistor was inserted in series with the AFM probe for current measurements assuming it would not affect the voltage distribution across the tip substrate nanocontact, because resistance of the nanocontact is orders of magnitude higher (few kΩ to MΩ) than the inserted resistance. The current was determined using Ohm's law ($V = IR$) by measuring the voltage across the resistor using a Keithley Multimeter that sampled voltage at 10 Hz. The schematic of the setup is shown in figure 21. The current resolution for this setup was approximately 2 nA and the maximum current was on the order of 1 A. The current was plotted against constant negative tip bias to get the I-V characteristic of the nanocontact.

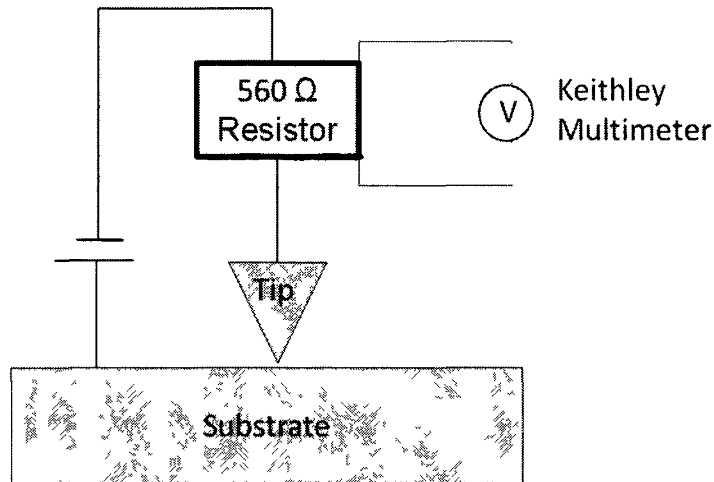

Figure 21: Schematic diagram of the setup for I-t measurements. A 560 ohm resistor inserted in series with the AFM probe. The voltage across the resistor is measured using a Keithley Multimeter.

Examination of Surface and Tip Modification

Surface modification - Topographical images of the substrate were captured after every negative tip bias (or voltage ramp during I-V measurements) application to observe the sample surface modification (nanopatterns) due to bias (in contact AFM mode, using same tip with same force).

To understand the mechanism and determine the factors influencing the HOPG and gold surface modification, we performed more controlled nanopatterning experiments in lithography mode on an XE-100 PSIA SPM in ambient conditions. The tip bias (-1 to -10 V tip bias), fabrication speed (50 – 3000 nm/sec) and contact force (2 – 2000 nN) were accurately controlled using standard lithography software (PSIA XEL software, version 1.2M2).

Tip modification - The used tips were mounted on a metallic stub (0.5'' diameter cylindrical mount) using a double coated conductive carbon tape (Figure 22) and examined under the Amray 3300FE field emission scanning electron microscope (SEM) to record the physical changes

to the tip due to bias. The chemical composition of used tips was also studied using the same SEM equipped with PGT Imix-PC energy-dispersive X-ray spectroscopy (EDS). See Appendix D: Instrument details for SEM- EDS evaluation.

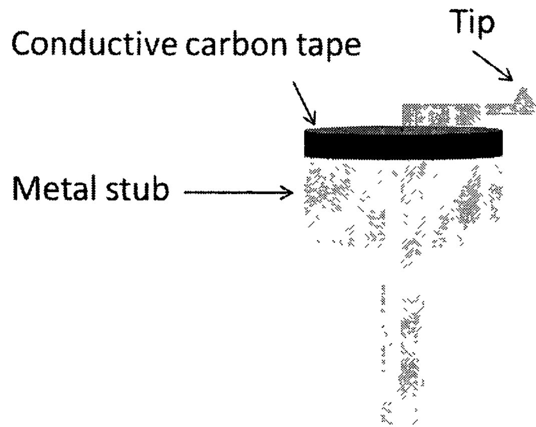

Figure 22: Schematic diagram of tip mounting for SEM-EDS evaluation.

Temperature Rise at the Nanocontact for FAN Conditions

We combined our heat transfer analysis and I-V measurement results to estimate the actual maximum temperature rise at the tip-substrate nanocontact associated with the measured current for the biases that Miller and Liu proposed will cause material transport of a coating on the tip to the surface. We also identified the voltages for which tip (or tip coating) modification due to temperature rise could occur.

CHAPTER 3

RESULTS AND DISCUSSION

We studied the evolution of the current voltage behavior of a doped Si tip on gold and HOPG to understand the impact of current on material modification for negative tip biases up to 10V. The maximum current measured for the bias range of -6 to -10 V on gold was 0.65 to 1.7 mA (~3.8 to 17 mW Joule power). The maximum current for HOPG was in the range of 0.45 to 1.96 mA (~2.7 to 20 mW Joule power). We performed heat transfer analysis of the tip-substrate interface to show that the measured powers are sufficient to raise the temperature at the interface to as high as 150 – 1100 °C (for gold and HOPG) which is sufficient to cause rapid tip oxidation of bare Si tip in an ambient environment (under very high electric fields on the order of 10^8 Vm^{-1}) and can cause diffusion or melting of organic or inorganic thin coatings from coated Si tips. The following sections describe our I-V measurements, SEM-EDS evaluation and heat transfer analysis results in detail.

I-V Behavior and Tip Modification

Highly Doped Si Tip with Gold Substrate

We performed I-V ramp as well as static voltage (I-t) measurements on the gold sample. The evolution of I-V behavior for an uncoated Si tip subjected to a 0-10 V negative bias sweep

(RH ~30-40 %) at a given point is shown in figure 23. The CAFM module saturates at 500 nA, so the curves in figure 23 and 24 only provide information regarding the low bias response of the tip-substrate interaction. This response should show the evolution of the interface independent of when it is evolving at higher biases. The current at higher, constant bias values was measured while tip was moving and is described in subsequent paragraphs. The initial resistance is high but decreases as the contact evolves. The number of sweeps for this to occur and the amount of resistance decrease varied from contact to contact but was on the order of 4-8 sweeps. Presumably, both the surface and the tip are evolving during the repetitive sweeps. Moving to a new location provides information regarding the evolution of the tip independent of the substrate.

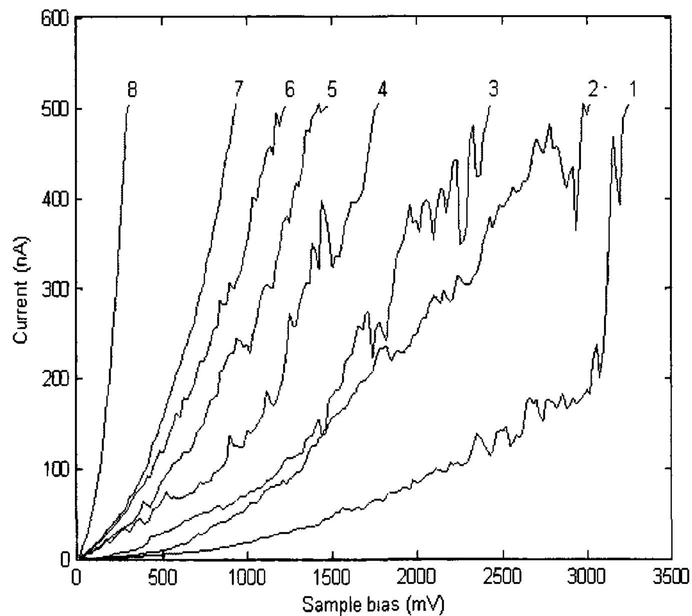

Figure 23: I-V curves acquired at a point for doped Si tip and gold substrate for negative tip bias (or positive sample bias). The number on each curve indicates the order in which the I-V sweep was applied.

Stabilized I-V curves at different locations using the uncoated doped Si tip on the gold sample are shown in figure 24. The tip-sample system offered very high resistance to current for

the first few locations. The resistance decreased up to the fifth location. Then, the resistance increased until the resistance was essentially infinite.

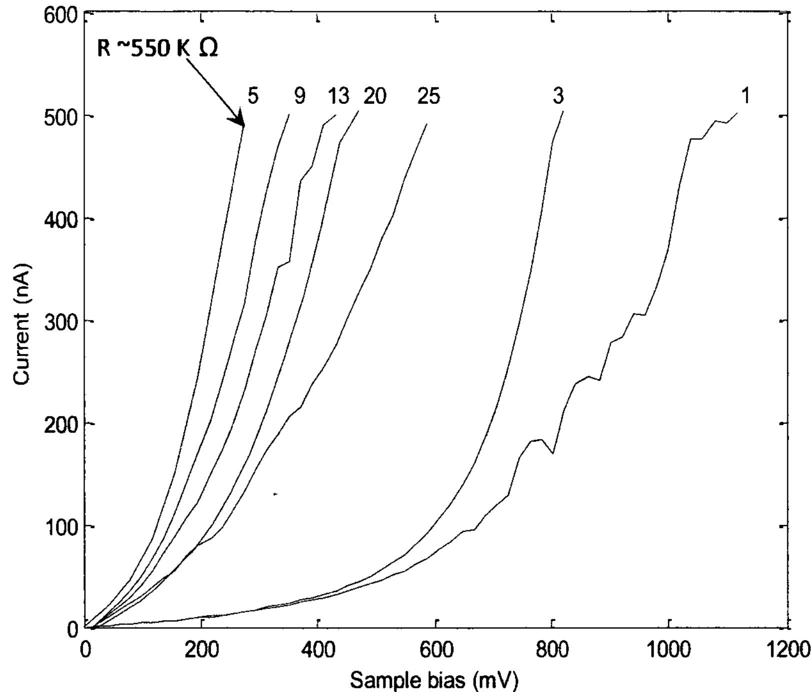

Figure 24: The IV characteristic of highly doped Si tip at different positions on gold substrate for negative tip bias. The number on each curve indicates the order in which the curve was captured on different locations on gold.

The high initial resistance of tips could be attributed to the presence of contamination from processing and storage or the native oxide layer on commercially available Si tips as observed by Arai et al.[28] and M. Tomitori.[29] We propose that application of repeated I-V ramps (0 to 10V) causes progressive degradation and subsequent breakdown of the insulating oxide or contamination layer present on the tip. The EDS analysis confirmed that oxygen content at apex of silicon tips decreased (from 8% to 4%) after two to three (0-10 V) I-V sweeps which supports the proposal that some sort of layer is removed from the tip. After the initial decrease, the resistance of tip substrate nanocontact increases until it is essentially infinite. We attribute this to oxidation of silicon tip at the elevated temperatures (presumably caused by Joule heating)

and high electric fields (oxidation kinetics of Si is explained in detail later in this chapter). The oxygen content increased (from 4% to 12%) as measured by EDS, which is consistent with our observation of increase in resistance.

EDS is an analytical capability which can provide elemental analysis on small volumes on the sample. The impact of the electron beam on the sample produces X-rays that are characteristic of the elements found on the sample. A detector is used to convert X-ray energy into voltage signals; this information is sent to a pulse processor, which measures the signals and passes them onto an analyzer for data display and analysis. The X-rays are generated in a region about 1 micron (and larger) in depth. We suspect that the oxide thickness in our case (described in the above paragraph) will not be this large and that EDS signal is a combination of the signal from the oxide layer on the tip and the Si below the oxide. Also, the EDS analysis is more accurate for flat, polished, and homogeneous samples. In all, we realize that the quantitative elemental data presented in this report is a coarse estimate of oxidation due to the limitations of the EDS, and the tip geometry. However, our EDS observations of increased/decreased volume-averaged oxygen concentration gives strong support to the idea that the oxide thickness varies with repeated voltage applications and do provide a good relative compositional estimate.

The other possible reason for initial decrease in resistance of the tip could be the change in radius of contact between the tip and the substrate. Kopycinska-Müller et al.[30] attribute the tip radius change to breaking of the sharp tip apex due to static contact loads. We believe that in addition to the high normal forces acting on the tip, the actual material transport during the voltage application is also responsible for change in the tip radius as discussed later in this chapter (figure 36). The before and after images in figure 25 shows a clear increases in tip

radius as well as removal of approximately 300 nm of tip material. The tip surface appears modified 100-200 nm from the apex, as well.

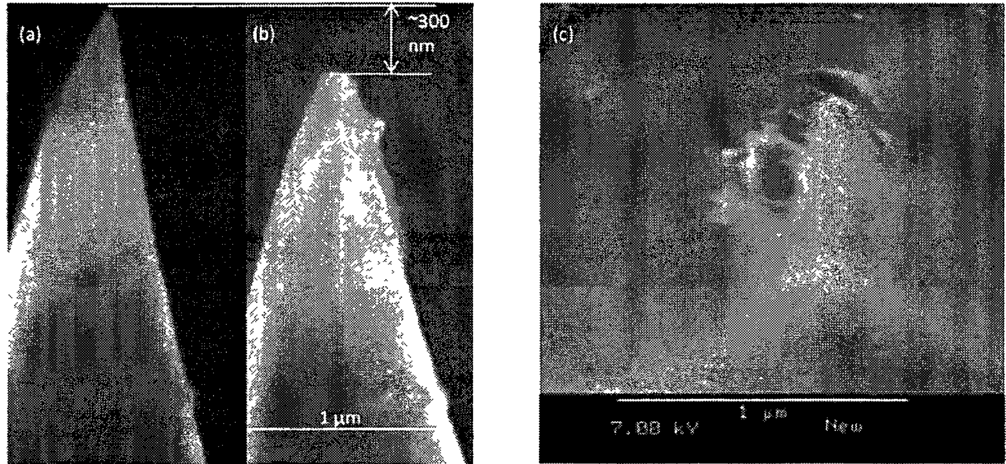

Figure 25: Tip shape evolution when negative tip bias is applied to Si tip and gold substrate system: (a) SEM image of new tip, (b) SEM image of used tip demonstrating removal of approximately 300 nm of tip material, and (c) Top view of the used tip demonstrating clear increase in tip radius (initial radius of curvature ~10 nm as specified by the manufacturer).

A rough calculation of the probe resistance was undertaken (See Appendix F: Mean free path of doped Si and estimation of probe resistance), in order to be compared with the resistance value measured during the experiment. It appears that measured resistance far exceeds the resistance of the tip or the substrate which are on the order of ohms (~1-2 kΩ total) and therefore represents the contact resistance. The contact resistance decreases significantly with increase in contact radius as per the Sharvin law[31] (See Appendix G: Contact resistance).

The I-V behavior of the Si tip with gold sample for the voltage range of -10 to 10 V tip bias is plotted in Figure 26. We measured currents of 1– 1.8 mA for constant negative tip bias of 10 V. The current (at -10 V tip bias) corresponds to much lower resistances (6-10 kΩ) than the minimum 550 kΩ determined by the I-V curves at low voltage (~250 mV, Figure 24). The

resistance decreases with an increase in bias as can be seen in figure 26. We attribute this to higher electron mobility in Si at high temperatures. We estimated temperatures in the range of 200 – 1100 °C for negative tip biases of 6-10 V (discussed in detail in the next section).

We observed very high resistance (20-500 MΩ) for positive tip biases in the range of 0-4 V. The resistance decreases with an increase in bias (~7 KΩ at 10V positive tip bias). The current was not stable for constant positive tip bias voltages, instead, current spikes were observed. Figure 26 shows peak current values for 0-10 V tip bias.

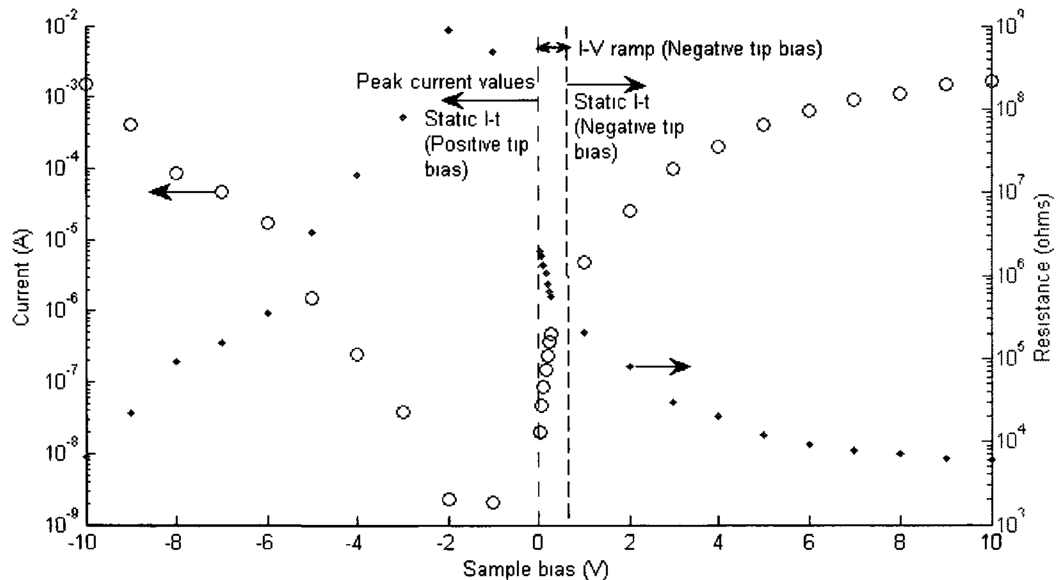

Figure 26: R/I-V data for doped silicon tip with gold substrate. The circles (o) represent the current data and the dots (·) represent the resistance data. The I-V ramp and static I-t data for negative tip bias (0-10 V) is marked on right hand side of zero bias reference. Only the static I-t data for positive tip bias (0-10 V) is marked on left hand side of zero bias reference.

The tip shape evolution and surface modification for positive tip bias is not discussed in this study because this research focuses on the conditions where the biased tip causes modification of the sample surface, in particular, the conditions that Liu & Miller[1,2] proposed will cause material transport of a coating on the tip to the surface (6 – 10 V negative tip bias). They

did not observe material transport for positive tip biases. Similar voltage polarity dependence for nanoscale surface modification has been reported by many investigators.[7,14]

Fullerene[60] Coated Highly Doped Si Tip with Gold Substrate

We only performed static voltage (I-t) measurements with [60] fullerene (or C60) coated Si tip with gold substrate. The I-V behavior for this tip substrate combination subjected to a static voltage in the range of 0 to -10 V is shown in figure 27 (at RH ~40 – 45 %). We also plotted the I-V behavior of uncoated Si tip with gold on the same graph for comparison.

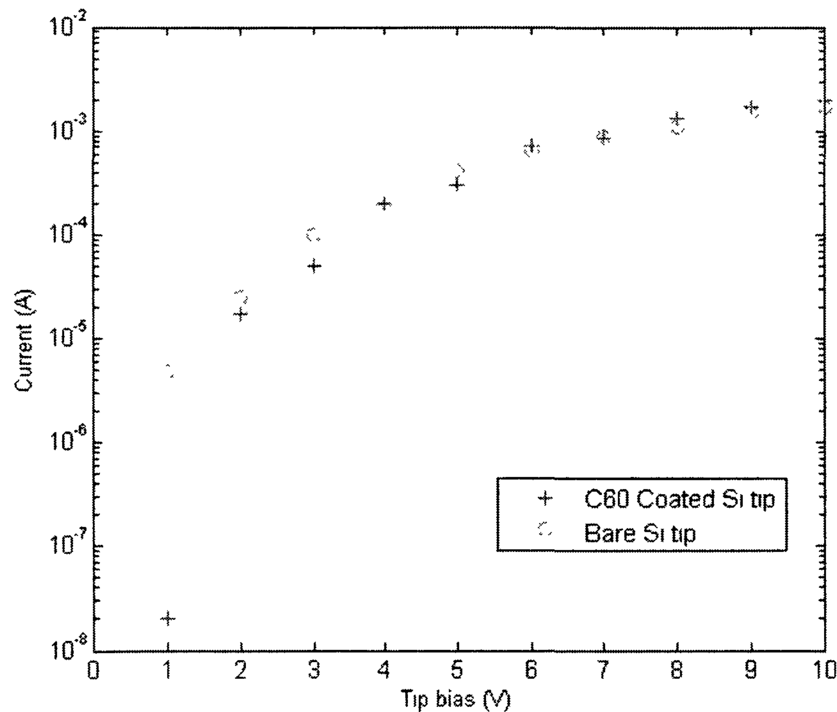

Figure 27: Comparative I-V behavior of C60 coated and bare Si tip for negative tip bias on gold (static I-t data for 0-10 V at RH ~40-45 %).

Figure 27 shows that the only difference between the current values of coated and uncoated tip is at 1 V. The current values for 5 to 10 V negative tip bias range (used by Liu & Miller during FAN) are almost identical.

Highly Doped Si Tip with HOPG Substrate

We performed only static voltage (I-t) measurements on HOPG. No voltage ramp measurements were performed because of the inability of the CAFM module to measure currents above 500 nA (the actual current recorded was on the order of few mA). The I-V behavior for several uncoated Si tips subjected to a static voltage in the range of 0 to -10 V on HOPG is shown in figure 28 (at RH ~60-65 %). We measured currents in the range of 10- 800 μA for constant negative tip bias of 1 – 7 V (A-B) applied for ~1-2 sec (per voltage). The current dropped significantly for negative tip bias of 8 V (C). This indicates that the resistance of the tip increased due to the application of -7 V (for ~1-2 sec). Curve D-E shows second I-V measurement for negative tip bias of 1 to 10 V indicating permanent change in the tip resistance. The resistance of the tip further increased with repeated measurements. Three new Si tips were used to measure current at constant negative tip bias of 8, 9 and 10 V each. Curve A-B-F shows the I-V response of a Si tip at static negative tip biases of 1 to 10 V. The resistance was dependent on bias (non linear) ranging from 100 kΩ at -1 V to 5-10 kΩ at -10 V tip bias (Figure 29) to values even larger than 10^9 Ω during the complete course of study (for negative tip biases of 1 – 10 V).

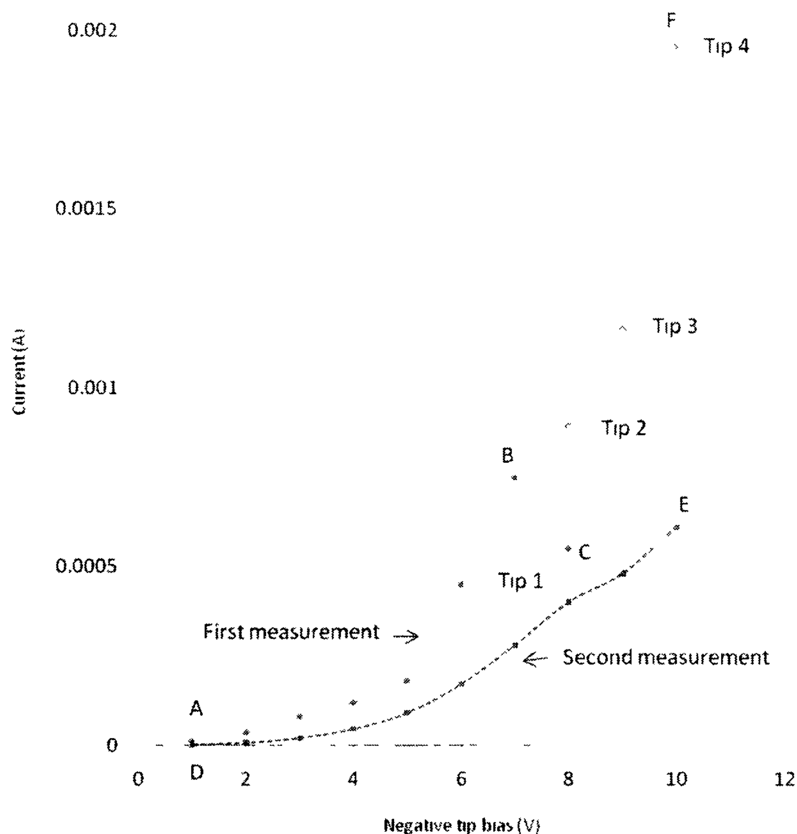

Figure 28: I-V measurements of the highly doped silicon tip on HOPG substrate for negative tip biases. The data is captured using four different tips (Tip 1, Tip 2, Tip 3, and Tip 4). Curve A-B represents the I-V behavior of Tip 1 for1-7 V negative tip bias. Point C shows the increase in resistance of Tip 1. Curve D-E shows second I-V measurement for Tip 1 indicating permanent change in the tip resistance. Tip 2, Tip 3, and Tip 4 are used to measure maximum current for -8, -9, and -10 V tip bias.

The increase in resistance of the tip could be attributed to the oxidation of silicon tip at the elevated temperatures presumably caused by Joule heating and very high electric fields (oxidation kinetics of silicon is described in detail later in this chapter). The oxygen content of tip 1 increased (from 4 % to 12.5 %) as measured by EDS. We realize that this is a coarse estimate of oxidation due to the limitations of the EDS and the tip geometry, however, gives strong support to the idea that the oxide thickness increases (as discussed in previous section).

Figure 29 shows I-V and R-V behavior for -10 to 10 V tip bias. The resistance for positive tip bias in the range of 0-10 V was higher than the corresponding resistance values for negative tip

biases. We also observed very high resistance (2-300 MΩ) for positive tip biases in the range of 0-5 V which decreased to ~40 KΩ at 10 V. The current was stable for constant positive tip bias voltages (unlike Si tip with gold in previous section).

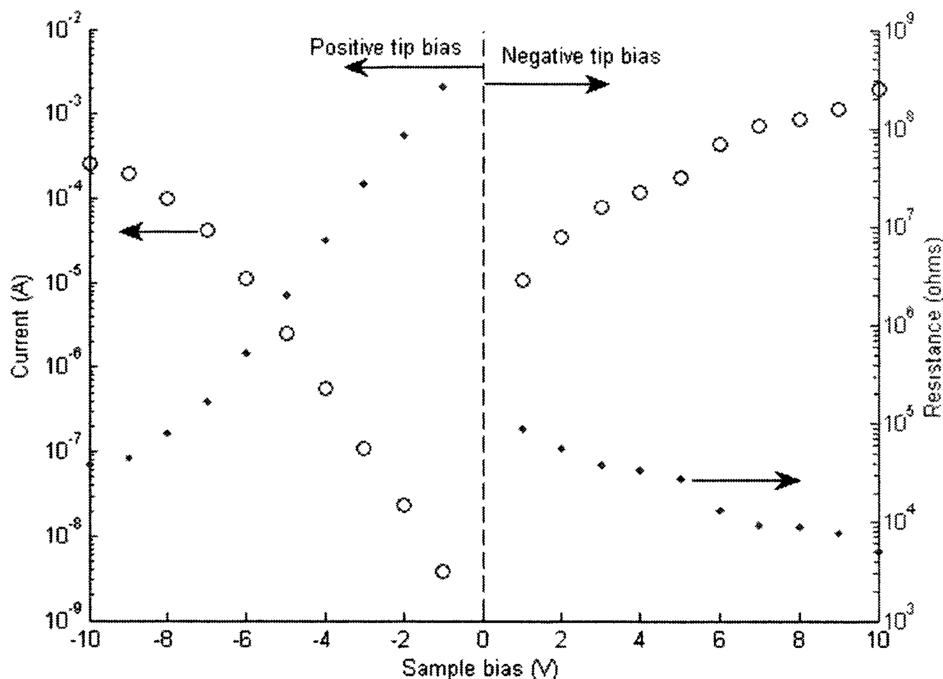

Figure 29: R/I-V data for doped silicon tip with HOPG substrate. The circles (o) represent the current data and the dots (·) represent the resistance data. The static I-t data for negative and positive tip bias (0-10 V) is marked on right and left hand sides of zero bias reference respectively.

The before and after images of tip in figure 30 shows a slight increase in tip radius as well as removal of approximately 50-80 nm of tip material. This can be attributed to blunting of the sharp tip apex with repeated usage due to static contact loads. Unlike Si tip on gold substrate, no significant change to the tip surface near the apex was observed.

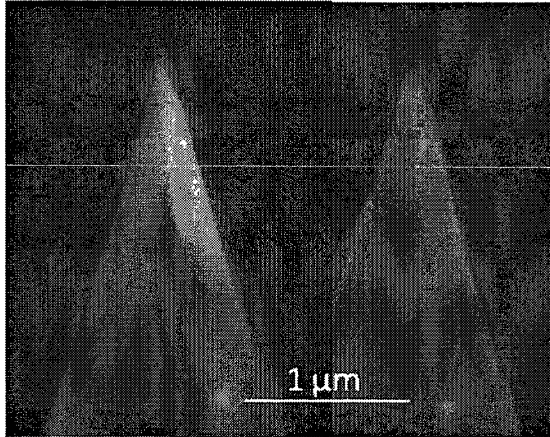

Figure 30: The tip shape evolution when negative tip bias is applied to Si tip and HOPG substrate system. The SEM images of new and used tip demonstrate a slight increase in tip radius as well as removal of approximately 50-80 nm of tip material.

Effect of humidity level on I-V behavior of Si tip and HOPG substrate

It is important to analyze the effect of humidity on I-V measurements on HOPG because of its hydrophilic nature. We made similar I-V measurements at lower humidity level (RH ~25 %). The I-V measurements obtained at low humidity are almost similar to the high humidity measurements.

The major difference was that the resistance of the tip gradually increased with number of repeated measurements (RH~25%) unlike in high humidity (RH~60-65%) case where it suddenly increased on single application of -1 to -7 V (each voltage applied for ~1-2 sec using static I-t measurement method) to the tip (figure 28). This shows that the presence of high moisture content in ambient air may not affect the current values but can significantly increase the rate of thermal oxidation of a Si tip. It is consistent with the higher oxide growth rate in wet oxidation (H_2O molecules act as oxidants, See Appendix E: Thermal oxidation of Si) as compared to the dry oxidation (O_2 molecules act as oxidants).

Oxidation Kinetics of Si

Initially, the growth of silicon dioxide is a surface reaction only. However, after the SiO_2 thickness begins to build up, the oxygen molecules must diffuse through the growing SiO_2 layer to get to the silicon surface in order to react and the reaction becomes diffusion-limited. Equation (7) mathematically describes the growth of an oxide layer on silicon (Deal-Grove Model).

$$t = \frac{X^2}{B} + \frac{X}{B/A} \tag{7}$$

where t is the time required to grow an oxide of thickness X at a constant temperature. B/A and B are the linear and parabolic rate constants respectively. These constants correspond to the oxidation conditions (temperature and wet or dry) and are thermally activated (equation 8).

$$k = k_0 \exp\left(-\frac{E_a}{k_B T}\right) \tag{8}$$

where k is either the linear or parabolic rate constant, k_0 is the pre-exponential factor, E_a is the activation energy (E_a is 1.24 and 0.79 eV for dry and wet oxidation respectively for parabolic rate constant, and ~2 eV for dry or wet oxidation for linear rate constant), and k_B is the Boltzmann's constant (8.6173×10^{-5} eV K^{-1}), and T is the temperature.

We realize that the model described above is a best fit for temperatures in the range of 700 – 1300 °C. All experiments were conducted in the humidity level of 25-65 % and therefore we assumed wet oxidation conditions. We used equation (7) to estimate the thickness of oxide that could form at several different temperatures for the times that the tip is in contact with the substrate. The linear and parabolic constants were taken from the curves (Linear rate constant vs. Temperature, and Parabolic rate constant vs. Temperature) obtained by Deal and Grove[32]. As

discussed in previous sections, we observed that the resistance of the tip increased with repeated voltage application (0-10 V) and the total effective time for this to happen varied from contact to contact. Therefore, we considered a range of time for oxide thickness calculation (10-150 s). The estimated thickness of oxide that could form at several different temperatures is plotted in the figure below.

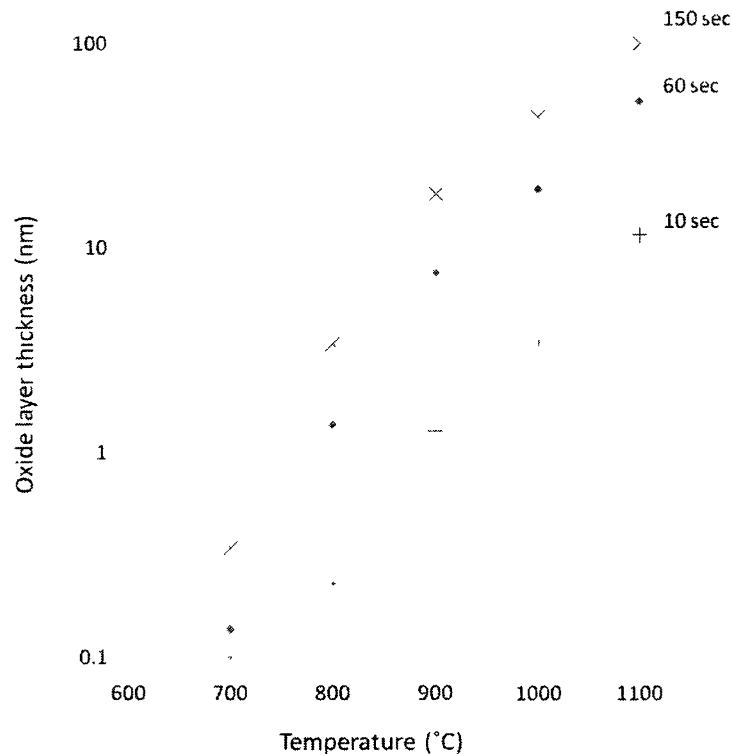

Figure 31: Estimated oxide layer thickness as a function of temperature for the tip substrate interaction time of 10 s (bottom curve), 60 s (middle curve), and 150 s (top curve).

Figure 31 shows that the oxide layer thickness increases with the temperature and becomes appreciable at very high temperatures (> 900-1000 °C). We observed increase in the oxygen content at tip apex at intermittent stages of voltage application (using EDS analysis as explained earlier in this chapter). We realize that the temperature was not always > 900 °C and

therefore oxidation of silicon tip at the elevated temperatures (traditional thermal oxidation) cannot be the single important factor for oxidation.

Kakiuchi et al.[33] reported that they obtained oxide layers on silicon at much higher rates (than conventional O_2 thermal oxidation process) using atmospheric plasma, even at very low temperatures (150 – 400 ˚C). Figure 32 shows the experimental setup and figure 33 shows oxidation time dependence of oxide layer thickness observed by Kakiuchi et al.

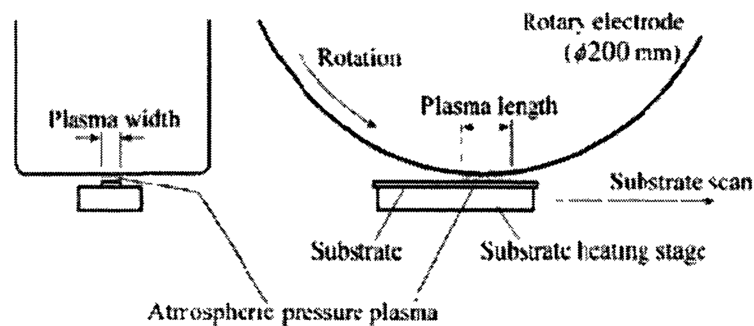

Figure 32: Schematic illustration of the front (left) and side view of experimental setup used by Kakiuchi et al.[33]

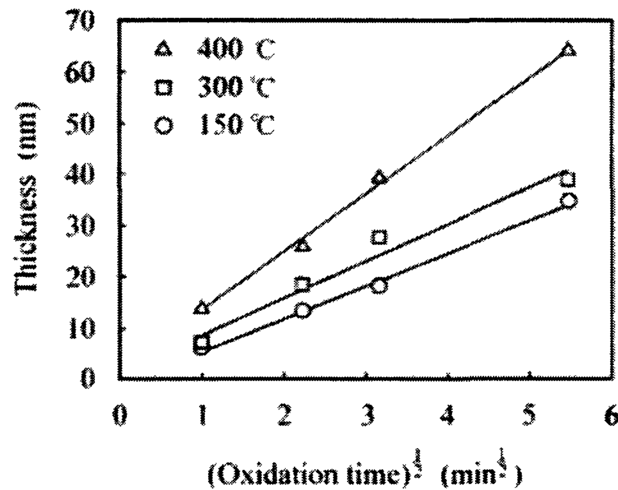

Figure 33: Thickness vs. oxidation time data for oxidation using atmospheric plasma.[33]

When a voltage bias is applied between a sharp tip and a substrate (close proximity), the electric field generated is extremely high (> 10^8 Vm^{-1}). The electrons emitting the tip at such high fields have enough energy to dissociate and/or ionize the O_2 molecules surrounding the tip-substrate interface into highly reactive oxygen atoms/radicals.[34] These reactive species can enhance the rate of oxidation (even at low temperatures, < 400 °C) of silicon similar to the atmospheric plasma effect on oxidation observed by Kakiuchi et al.[33] as explained above.

We suspect that the oxidation of Si tip observed during our experiments occurred by a combination of elevated temperatures (Joule heating) in the presence of highly reactive oxygen radicals produced due to extremely high electric field at the tip-substrate interface.

Estimation of Temperature Rise for Measured Current at the Nanocontacts

We measured currents for negative tip biases in the range of 1 to 10 V for Si tip with gold and HOPG substrates in the last section. The current (I) and applied voltage (V) generate Joule heating (Q=IV) that must be dissipated in the tip contact region. The heat transfer model described in the previous chapter estimates the temperature at the nanocontact due to Joule power. We combined our I-V measurements and heat transfer analysis results to determine voltages for which tip modification due to temperature rise occurs. We also estimated a range of temperature for the biases that Miller and Liu proposed will cause material transport (6 to 10 V negative tip bias).

Figure 34 shows temperature rise at the Si tip and gold substrate interface as a function of power input. The plot suggests that thermal oxidation of silicon by the mechanism described above could occur with tip biases > 6V (~4 mW of input at the junction). We have already shown that the I-V behavior for the C60 coated Si tip with gold is almost identical to that of uncoated Si

tip with gold (last section) and therefore the following figure estimates the temperature rise for coated tip as well.

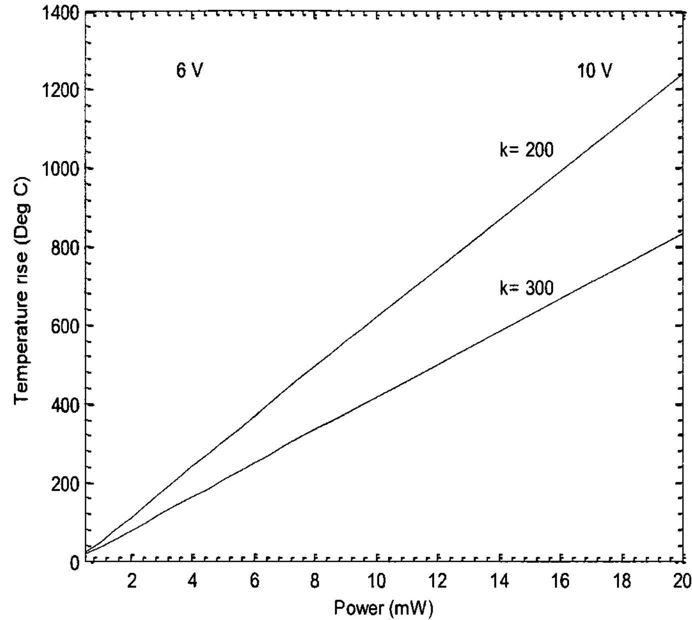

Figure 34: The temperature rise at the Si tip and gold substrate interface as a function of power input. A range for thermal conductivity of gold (k = 200- 300 $Wm^{-1}K^{-1}$) is considered in the model. The range marked with vertical lines displays the temperature rise during the deposition process demonstrated by Liu & Miller.[1,2]

Figure 35 shows temperature rise at the tip and HOPG substrate interface as a function of power input. The plot suggests that thermal oxidation of silicon in the presence of high electric fields could occur with negative tip biases > 6V (~2.8-3 mW of input at the junction). We observed oxidation growth at -7 V (sudden decrease in current was observed, EDS analysis confirmed increase in oxygen content at the tip apex as described in previous section) which corresponds to ~5.6 mW and ~300 ˚C temperature rise (shown by double dashed line). The melting of silicon tip should not occur for the tip bias range of -6 to -10 V.

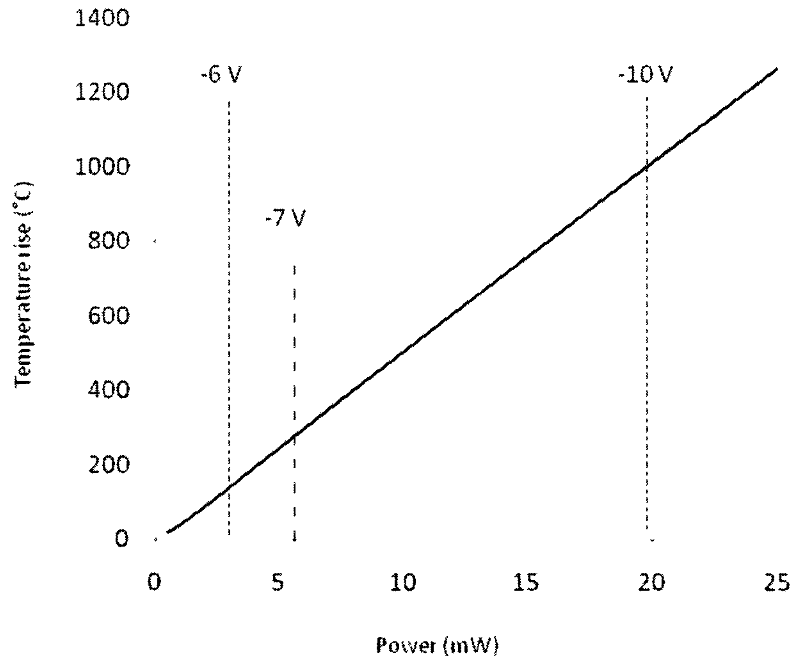

Figure 35: The temperature rise at the Si tip and HOPG substrate interface as a function of power input. The range marked with dashed lines displays the temperature rise during the deposition process demonstrated by Liu & Miller.[1,2]

The temperature rise in figures 34 and 35 (at powers above 2 mW) is nearly identical (1-3 % less) to the temperature rise when heat transfer only due to the gold and HOPG substrates are considered (figures 19 and 20) respectively indicating that the heat rise at the nanocontact depends primarily on the thermal resistance of the substrate for higher power.

Liu and Miller[1,2] deposited lines from Si tips coated with a broad array of organic and inorganic molecules (including C60) onto HOPG, and ODT-passivated Au by applying a negative bias to the tip in the range of 6 – 10 V. The range marked with vertical/dashed lines in figure 34 & 35 displays the temperature rise during the deposition process demonstrated by Liu & Miller. The temperature rise for uncoated/C60 coated Si tip with gold substrate is in the range of 160-250 °C at threshold bias of 6 V and 710-1060 °C for 10 V depending on the conductivity of the substrate film. The temperature rise for Si tip with HOPG substrate at threshold bias of 6 V is

~150°C and ~1000°C for voltage of 10 V. In all, the temperature at the junction for 6-10 V negative tip bias is well above the ambient and sufficient to cause modification of the tip coatings through diffusion, melting, or evaporation in both cases.

Substrate Modification during I-V Measurements

We observed a bump on the gold sample every time the 10 V negative tip bias ramp was applied irrespective of the nanocontact resistance at that point of time. The voltage threshold for obtaining bumps using doped Si tips on the gold substrate was determined to be -5 V at constant voltage. The height and width of the bump increased with increase in magnitude of tip bias and tip hold time on the substrate (typical height of 5-20 nm). One of the representative images is shown in figure 36. Repeated scanning in contact sometimes causes the bump to disappear leaving a pit behind. A typical sequence of images is shown in figure 37. It was observed that the bumps created in high humidity (> 60%) were more easily removed.

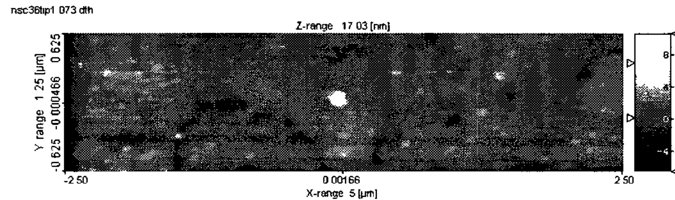

Figure 36: Effect of 0-10V (negatve tip bias) i-v sweep using doped Si tip in contact with the gold substrate (~ 10 nm high bump obserbed).

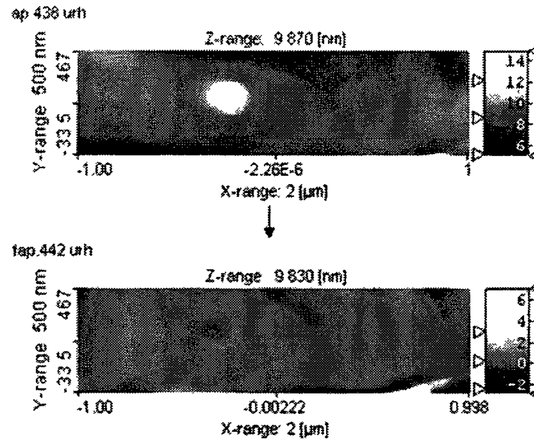

Figure 37: Example of conversion from a bump to pit as a result of repetitive scanning. The bump is the effect of 0-10V (negatve tip bias) i-v sweep using doped Si tip in contact with the gold substrate.

We observed a bump on the gold sample every time the negative tip bias greater than 5 V was applied using C60 coated Si tip. The surface modification obtained on gold with C60 coated Si tip and bare Si tip was similar.

We observed a pit or a bump on a HOPG substrate every time the negative tip bias of greater than 4-5 V was applied to a moving Si tip during the I-t measurements independent of the nanocontact resistance at that point of time (figure 38). The formation of the feature (bump or pit) depended on the tip speed, magnitude of tip bias, and dwelling time of tip at one location (or scan size for particular tip speed) during the voltage application.

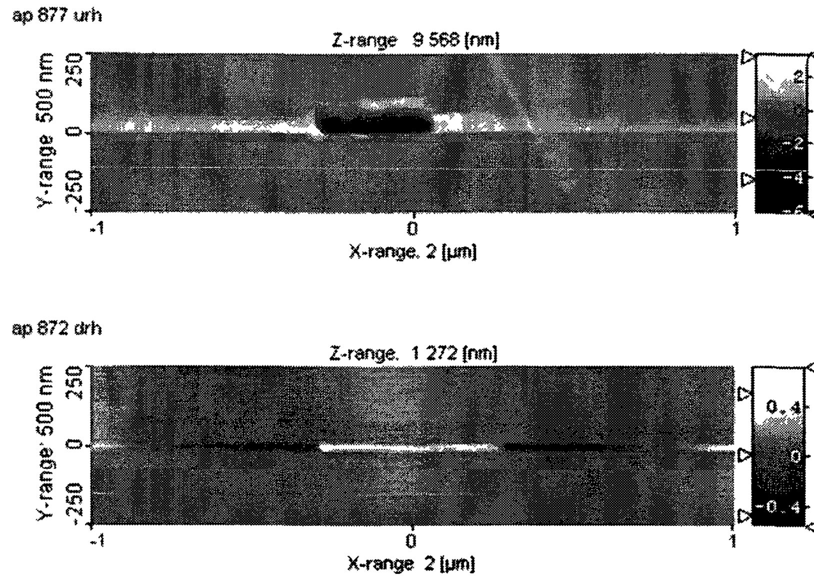

Figure 38: Pit and raised feature formation using doped Si tip in contact with the HOPG substrate.

We performed more controlled experiments in lithography mode on an XE-100 PSIA SPM to understand the mechanism and determine the factors influencing the gold (bump) and HOPG surface modification (pit or bump) for similar conditions. The results are discussed in detail in the following chapter.

CHAPTER 4

MECHANISM AND FACTORS INFLUENCING THE FIELD ASSISTED SURFACE MODIFICATION

Gold Surface Modification when Negative Tip Bias is Applied

As previously mentioned, we are able to produce bumps on gold surfaces when applying a negative tip bias (> 5 V). Repeated scanning in contact sometimes caused the bump to disappear leaving a pit behind. We varied tip bias, fabrication speed and contact force in lithography mode to understand the mechanism of gold surface modification. We used an XE-100 PSIA SPM and the lithography software (PSIA XEL software, version 1.2M2) to perform the measurements.

We observed bumps on the gold sample for 5-10 V negative tip bias in lithography mode (contact mode). The tip bias and tip fabrication speed have a strong influence on the formation of the bumps.

Figure 39 shows the formation of lines with varying tip speeds for tip bias in the range of -6 to -10V at constant tip force of 2 nN. All line patterns were generated on 5μm X 5μm area from top to bottom starting on the left and progressively moving to the right (Figure 39(b)).

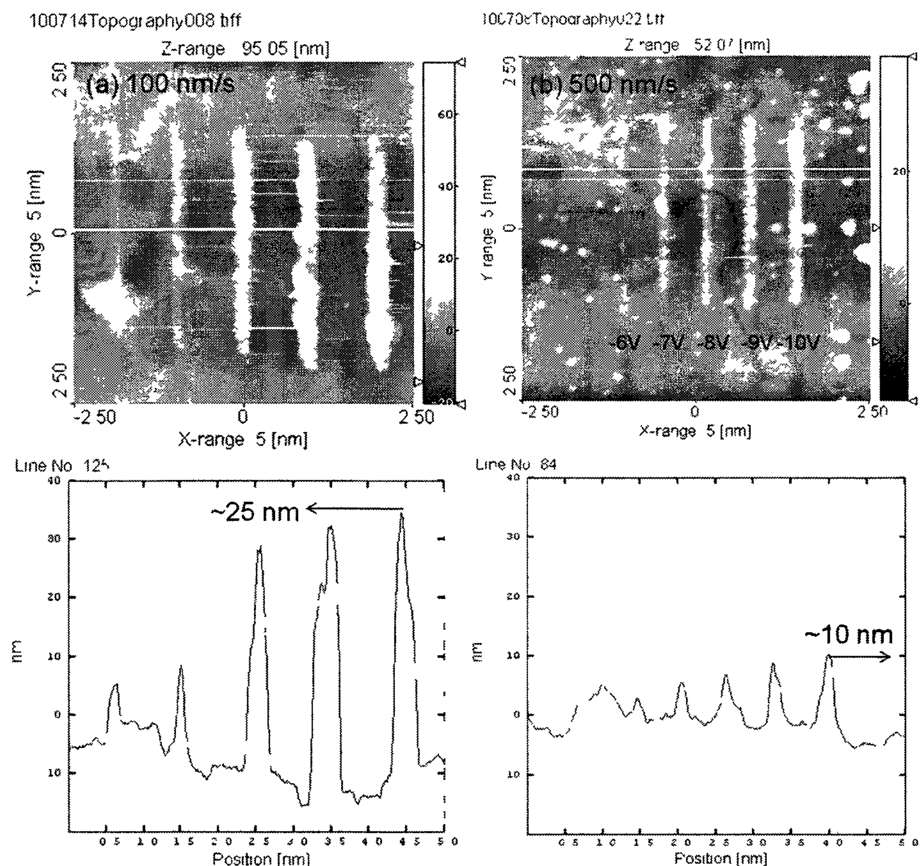

Figure 39: The formation of lines with varying tip speeds for tip bias in the range of -6 to -10V (from left to right). The lines were fabricated with tip speeds of 100 nm/s (left) and 500 nm/s (right).

The height of the lines increase with increasing negative tip bias or decreasing tip fabrication speed (figure 39). This set of results indicates that the tip substrate interaction time is one of the important factors in controlling the formation of bumps on gold.

We also fabricated lines at different set points for tip bias in the range of -6 to -10 V at constant tip speeds. No significant difference in bump size was observed for different set points in the range of 2-1000 nN. This clearly indicates that the mechanical effect does not contribute in the formation of bumps.

Several mechanisms for the surface modification of gold have been proposed. Liu and Miller[1,2] demonstrated that they could create 50-250 nm wide, 2-15 nm thick lines onto ODT-

passivated Au by applying a negative bias (> 5 V) to SPM tips dip-coated with a broad array of organic and inorganic molecules. They proposed material transport occurred due to electrostatic repulsions between molecules and the tip and the molecules at a threshold negative tip bias. However, the fact that all materials seem to be deposited in a narrow voltage range for such a broad spectrum of material suggests that this mechanism, however important, cannot be the cause of all deposition. Furthermore, this mechanism can be ruled out in case of uncoated tips.

Electromigration (proposed by Lo et al.[35]) occurs due to momentum transport from electrons to atoms at high current densities. However, the tip resistance and geometry continually evolves (Chapter 3) and therefore current or current density cannot be the single important factor for surface modification.

Field evaporation occurs when the atoms are ionized in the presence of extremely high electric field (on the order of a few V/nm) and directly pulled out of material surface. This mechanism was observed by Koyanagi et al.[12] and Mamin et al.[13] They found that the threshold field for negative tip bias is lower than that of positive bias.

Park et al.[14] produced ~90 nm wide and ~15 nm high mounds on Au surface using a W_2C coated tip and applying tip bias (0 to -40 V) in intermittent contact. They proposed that surface modification occurred by field emission induced local heating and concurrent field induced diffusion.

Based on our observations, we believe that material transport can occur by a combination of different mechanisms. It is conceivable that one of these mechanisms may be more important depending upon several factors including tip geometry, tip resistance and humidity level. The possible mechanisms of gold surface modification are discussed in the following section.

Formation Mechanism of the Nanostructures on Gold

We suspect that bumps are produced as a result of reaction of field evaporated silicon atoms with gold film under very high electric field to form inter-diffused region which in the presence of high temperature (>100 °C) forms gold silicon alloy[36]. The above effect is important at comparatively low current values (high tip resistance).

We also estimated very high temperatures (>500 °C) at the Si tip- gold substrate nanocontact for voltages above 7V (at low tip resistance) which can cause localized heating of gold film and cause it to flow by diffusion along the concentration gradient (similar to the mechanism proposed by Park et al.). It is conceivable that under high humidity level, heated gold also reacts with water molecules adsorbed on the surface to form gold hydroxide (gold hydroxide is a product of electrochemical reaction of gold subjected to moisture and positive electric potential) which is easily removed by repeated scanning. This is consistent with our results obtained in high humidity (bump disappears leaving a pit behind).

The surface modification obtained on gold with C60 coated Si tip and bare Si tip was similar. The figure below shows AFM images of nanostructures created on gold substrate using bare Si (a) and C60 coated Si tip (b).

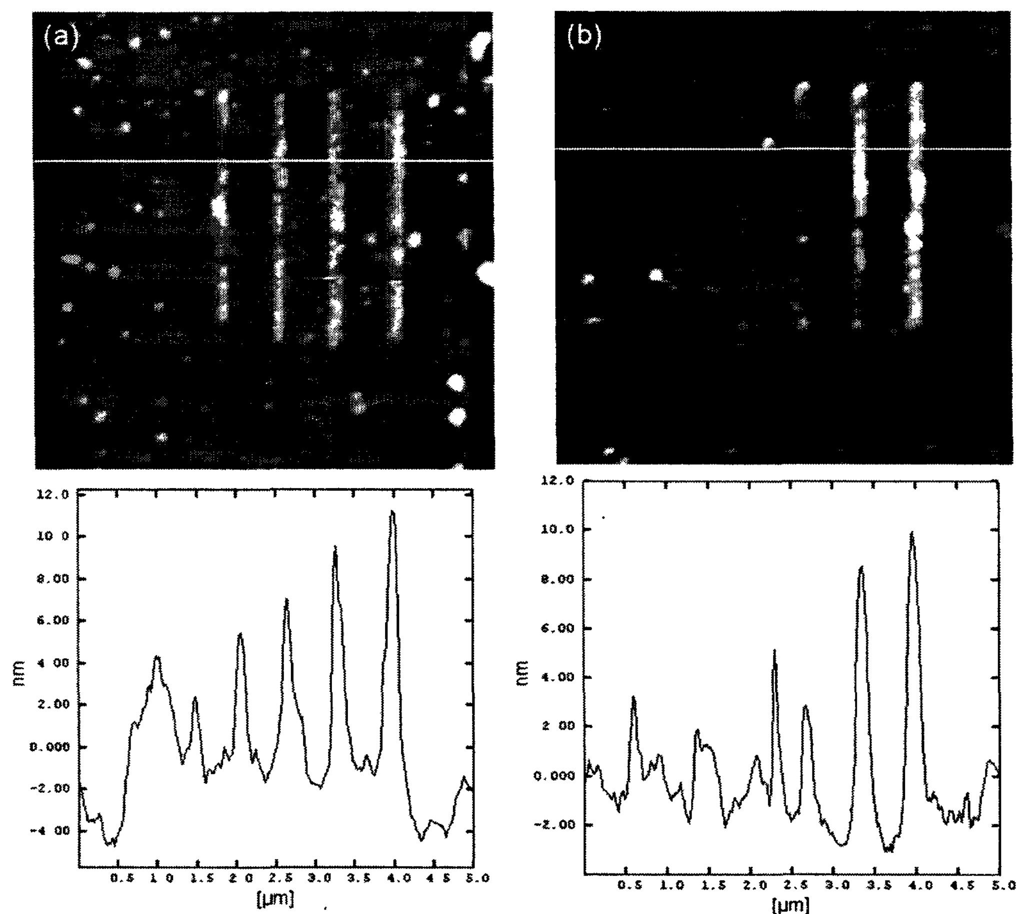

Figure 40: Lines drawn on gold using (a) bare Si tip, and (b) C60 coated tip for negative tip bias of 6 – 10 V (from left to right).

Further research is required to confirm the mechanism of bump formation at different tip and environmental conditions on gold.

HOPG Surface Modification when Negative Tip Bias is Applied

As previously mentioned, we are able to produce trenches and bumps on HOPG surfaces when applying a negative tip bias. We varied tip bias, fabrication speed and contact force in lithography mode to understand the mechanism of HOPG surface modification. We used an XE-

100 PSIA SPM and the lithography software (PSIA XEL software, version 1.2M2) to perform the measurements.

We observed bumps as well as trenches on the HOPG sample for 5-10 V negative tip bias in lithography mode (contact mode). The tip fabrication speed, tip force and humidity all have a strong influence on the formation of the bumps and trenches.

Figure 41 shows the formation of lines with varying tip speeds for tip bias in the range of -1 to -9V at constant tip force of 2 nN. All line patterns were generated on 5μm X 5μm area from top to bottom starting on the left and progressively moving to the right. Figure 41 (a) indicates the magnitude of bias and site to which it was applied on each area.

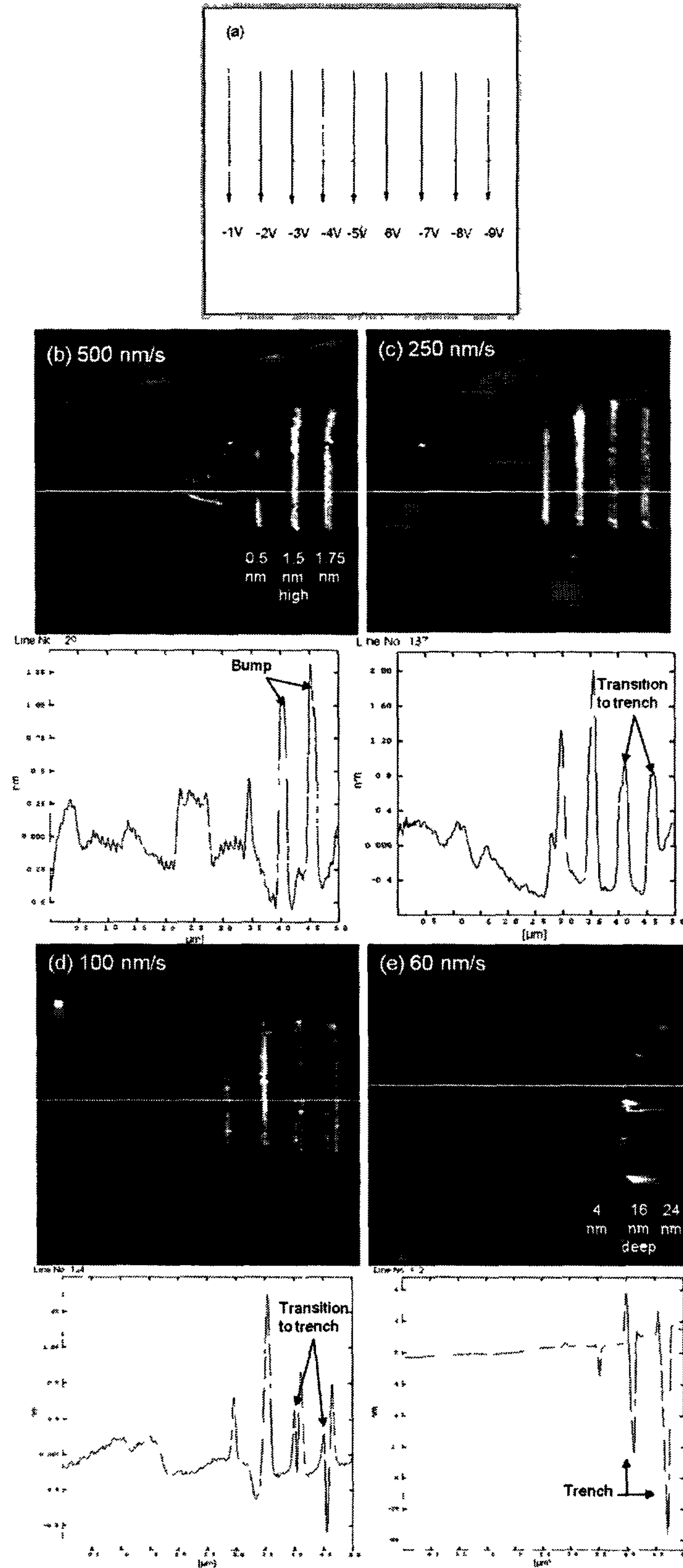

Figure 41: The formation of lines with varying tip speeds for tip bias in the range of -1 to -9V. The lines were fabricated at tip speeds of (b) 500 nm/s, (c) 250 nm/s, (d) 100 nm/s, and (e) 60 nm/s.

For a 9V tip bias, bumps turn into trenches as the speed is reduced. Neither bumps nor trenches were observed at any speed for tip biases below 6 V at this particular (high) humidity (55%) and tip speed range. When bumps are observed, the height decreases (within the height range of few angstroms to ~2 nm) with decreasing tip bias at a given tip speed until the bumps are no longer observed (figure 42). Trenches are observed at lower tip speeds and higher tip biases. The depth of the trenches also decreases with decreasing tip bias at a given tip speed (figure 43). No features were observed for very high speeds > 3000 nm/sec. This set of results indicates that the tip substrate interaction time is one of the important factors in controlling the formation of bumps and trenches on HOPG.

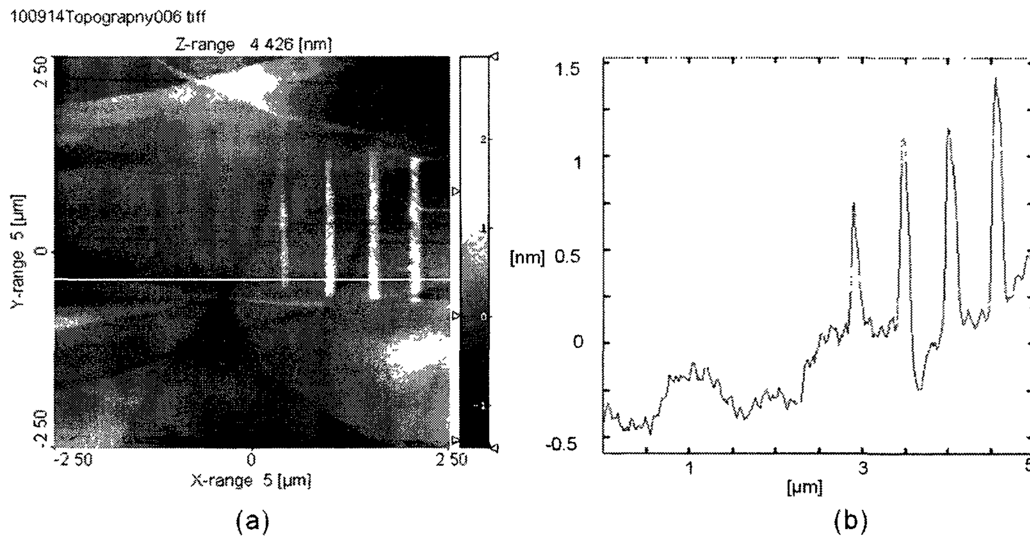

Figure 42: The formation of lines with varying tip bias at constant tip speed of 250 nm/s. The negative tip bias from 1 – 9 V was applied from left to right on 5 µm X 5 µm area.

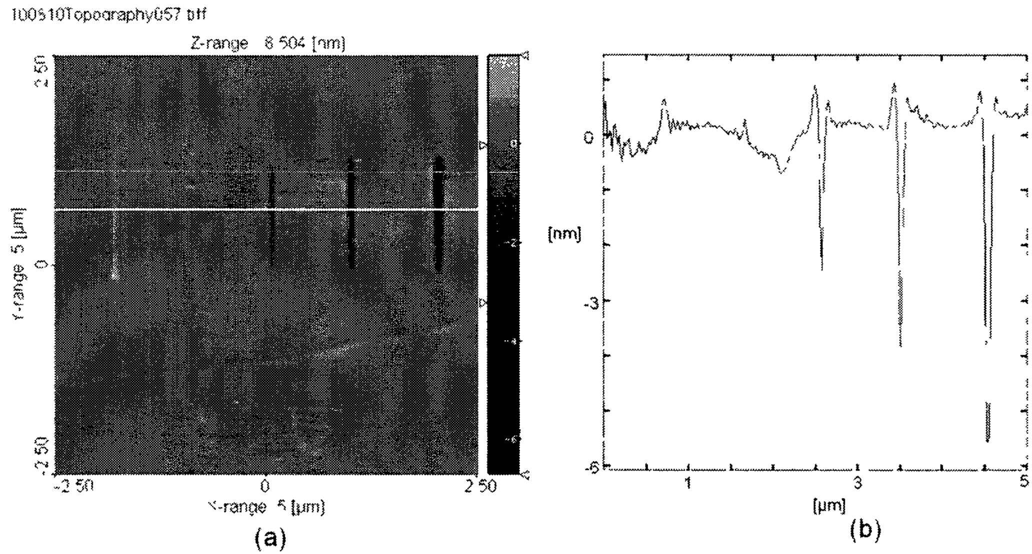

Figure 43: The formation of trenches with varying tip bias at constant tip speed. The negative tip bias from 6 – 10 V was applied from left to right on 5 μm X 5 μm area.

Figure 44 shows an array of parallel lines fabricated at different set points (tip force) for tip bias in the range of -6 to -10V at constant tip speed of 500 nm/s. All line patterns were generated on 5μm X 5μm area from top to bottom starting on the left and progressively moving to the right (Fig. 44(d)).

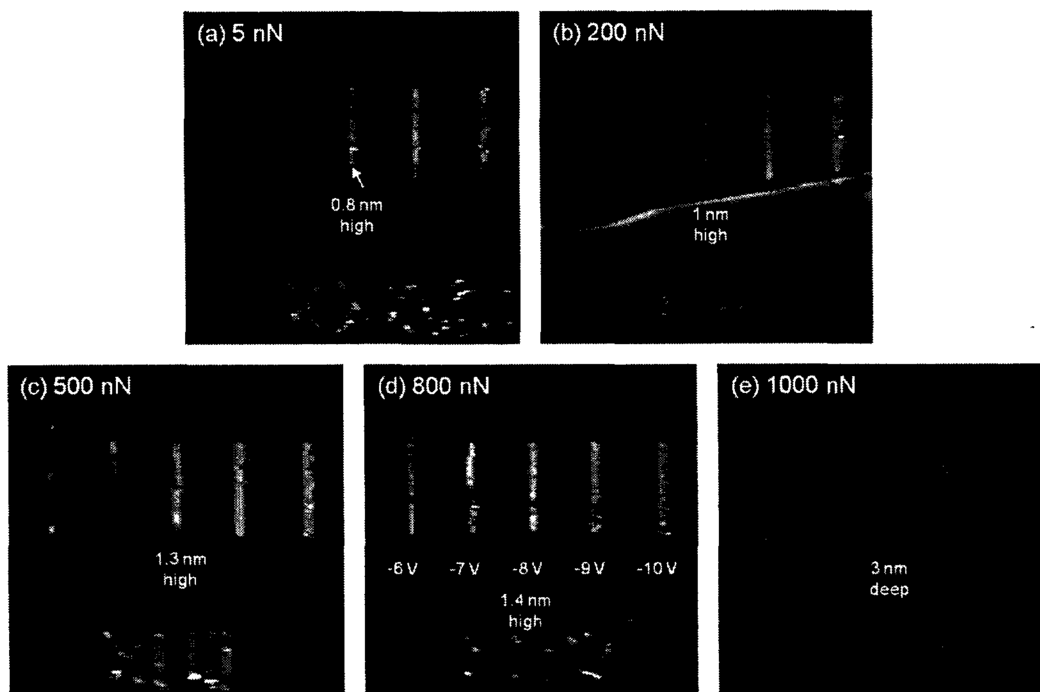

Figure 44: The lines fabricated at different set points (tip force) for tip bias in the range of -6 to -10V (from left to right) at constant tip speed of 500 nm/s. The lines were fabricated at tip forces of (a) 5 nN, (b) 200 nN, (c) 500 nN, (d) 800 nN, and (e) 1000 nN.

The height of the bumps increase (height range few Å to ~2 nm) with increasing force until, at high forces and bias, trenches are formed instead of bumps. The bump height increases with increasing bias until trenches form at the higher forces. This clearly indicates that the mechanical effect does contribute in the transition between a bump to a trench.

Trenches were more easily produced in high humidity. However, the general trend of transition from bump to trench with the varying tip speeds and set points for a particular humidity level remains the same as explained above. Figure 45 shows comparative images of patterning (-1 to -9V tip bias applied from left to right as shown in figure 41(a)) on the HOPG surface for different humidity levels at constant tip speed of 80 nm/s and set point of 5 nN.

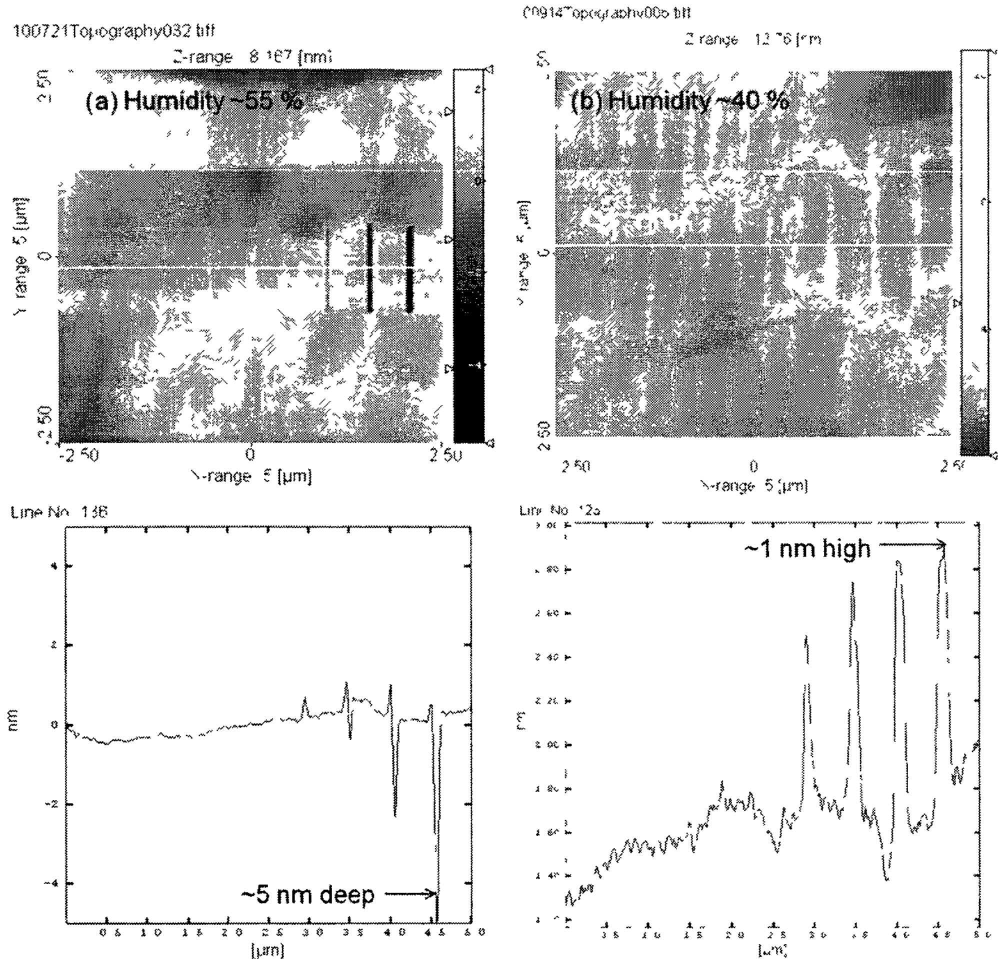

Figure 45: Nanopatterns on HOPG for different humidity levels at constant tip speed of 80 nm/s and tip force of 5 nN. The negative tip bias from 1 – 9 V was applied (from left to right) at relative humidity of (a) 55 %, and (b) 40 %.

According to the above experimental results, the bumps (few Å to ~ 2 nm height range) only occur for short tip substrate interaction time and therefore can be seen as intermediate stable structures for the formation of trenches. Very high contact forces (>800 nN) used during the lithography can fracture these bumps to create trenches. In all, the nanostructures on HOPG are affected by the tip bias, tip speed, tip force and humidity. For obtaining a desired pattern, three out of the above four parameters should be kept constant.

Several mechanisms for the surface modification of HOPG in air have been proposed. Kondo et al.[17] reported etching of HOPG in UHV at threshold tip bias of -7.2 V and attributed it to sublimation of carbon induced by tunneling electrons. However, Jiang et al.[37] reported that no features were observed for the voltage range of +/-10V in a vacuum. Many studies[37,16] attribute surface modification on HOPG to electrochemical oxidation in the presence of air and water. We also observed a clear effect of humidity on surface modification.

The tip resistance continually evolves (Chapter 3) and therefore current cannot be the single important factor for surface modification. We ruled out mechanical scratching because no features were created for very high contact forces without negative tip bias. We did not observe features on HOPG when positive tip bias was applied (0-12 V).

Zhang et al.[38] observed raised features on HOPG during anodic oxidation experiments performed using STM in dilute sulfuric acid. Jiang et al.[19] reported formation of both bumps and pits with metal-coated AFM tip in the voltage range of 0 to 10V (positive sample bias) under ambient conditions. They observed bumps at low voltage or short pulse duration and its transformation to pits when voltage or duration was increased which is consistent with our results. But the effect of contact forces and humidity during nanofabrication was not investigated which we believe are very important parameters in surface modification of HOPG.

Based on observations, chemical oxidation induced by electrons in the presence of air and water is the most probable mechanism which initiates with straining and buckling due to graphene oxide formation under very high electric fields. The feature formation mechanism is explained in detail in the following section.

Formation Mechanism of the Nanostructures on HOPG

Many researchers believe that water molecules (H_2O) are directly ionized at the high electric field[16]. Also dissociation of water to form OH^- and H^+ radicals by electron impact occurs with threshold electron energy of 5.1 eV [39] (equation 9). Our experimental conditions satisfy both ionization requirements.

$$e^- + H_2O \rightarrow H\cdot + OH\cdot + e^- \quad (9)$$

HOPG has a layered structure (Appendix H: Highly ordered pyrolitic graphite). It is well known that fluids such as air and water are present between the top layers of graphene, which are naturally adsorbed from the environment. We believe that the ionization of water molecules (at the threshold bias) initiates the oxidation of graphite to form graphene (or graphite) oxide on the surface. The formation of graphene oxide preserves the layer structure of the graphite, but the layers are buckled.[40,41] The extent of buckling depends on degree of oxidation. This is consistent with the height of bumps produced during our experiments ranging from few angstroms to ~2-3 nm. We believe that this is what happens at higher speeds and lower voltages. These buckled regions will be more susceptible to mechanical damage and can be fractured off leading to trenches as the tip force is increased. The above effect is greater at slow tip speeds and higher voltages and results in transition of bumps to trenches.

We also measured high currents in the range of ~0.8-2 mA (for 7 to 10 V negative tip bias range) for a Si tip with HOPG substrate (Chapter 3) which corresponds to 6-20 mW of power that must be dissipated in the tip contact region. The heat transfer model (described in Chapter 3) suggests that this can raise the temperature near the nanocontact by 300- 1050 °C due to Joule heating. It is known that graphite oxide exfoliates at moderately high temperatures[42] (~ 280-300 °C). This also explains transition of bumps to trenches at high voltage and low tip speeds.

We believe that trenches are produced as a result of oxidation of carbon with oxygen (from ambient air) and water molecules (humidity). It has also been identified that H_2O has high reactivity with carbon as compared to O_2 as an oxidizing agent[43], which is consistent with our results obtained in high humidity and relatively dry air (figure 45).

In all, the formation of nanostructures on HOPG can be attributed to the (different stages of) progressive oxidation that starts with the formation of graphene oxide on the surface and then progresses to oxidation to CO and CO_2.

CHAPTER 5

TECHNICAL ISSUES WITH FIELD ASSISTED NANOPATTERNING

Liu & Miller's[1,2] paper document that they can create raised features on HOPG and ODT-coated Au surfaces by applying negative tip bias in the range of 5 to 10 V. The height and width of the features increases with increasing tip bias or decreasing tip velocity. They have noted that lines produced using semi-volatile coatings (e.g. N-methylpyrrole), tend to disappear or diminish with time suggesting that the molecule transfers from the tip to the substrate without modification. However, they have not provided direct evidence that the raised features are the material that was on the tip. The scanning Auger microscope could be used to determine elemental composition of raised features on substrates.

We have obtained numerous experimental results showing similar raised features (same size range) using an uncoated, highly doped Si tip on HOPG and ODT-coated Au surfaces for negative tip bias range used in FAN. A representative image is shown in figure 46. We also have evidence that some features produced by uncoated tip are unstable and can be scanned off. We found that there is no significant difference in the features produced by coated or uncoated tips (figure 46 and 47).

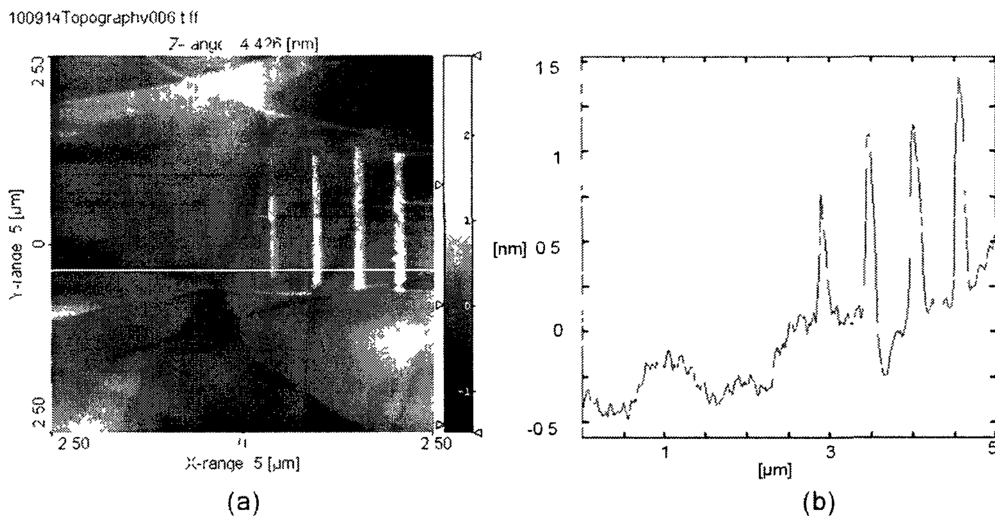

Figure 46: (a) Height image; and (b) cursor plot of raised features on HOPG with a tip that did not have a coating. The lines were fabricated using tip bias values of -6, -7, -8, and -9 V (from left to right).

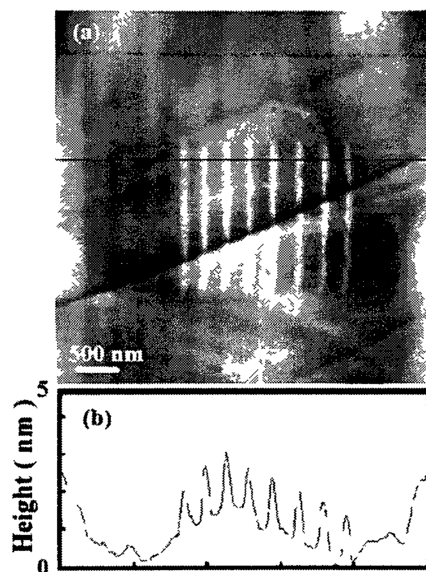

Figure 47: (a) Height image; and (b) cursor plot of Field–assisted nanopatterning of poly-3-octylthiophene-2,5-diyl lines on HOPG .The lines were fabricated at tip bias – 7 V.[1]

We coated the Si probes with C60 molecules by following the tip coating procedure described by Liu and Miller. One of the coated tips was randomly selected and examined under scanning electron microscope (SEM). Figure 48 shows non-uniform coating of C60 molecules on

cantilever and nearly no coating on Si tips. For reproducible deposition, availability of coating molecules on the sidewall of the tip is required. Since none of the tips were examined for the verification of proper coating prior to FAN and still raised features could be obtained for multiple experiments using same tips, it is doubtful that the raised features in FAN are always due to the material that was coated on the tip.

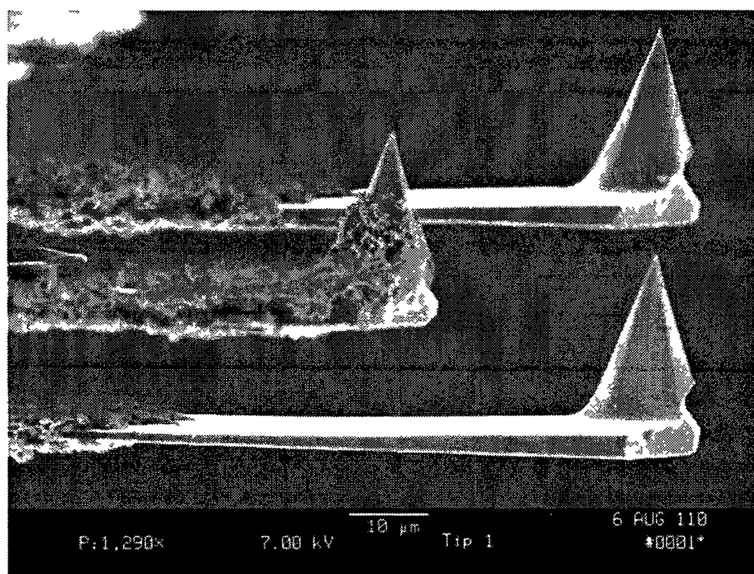

Figure 48: SEM image of AFM tip dip coated with C60 molecules. The tips were coated using the tip coating procedure described by Liu and Miller.[1,2]

Our heat transfer model shows that the temperature at the junction for 6-10 V negative tip bias is well above the ambient and sufficient to cause modification of the tip coatings like N-methylpyrrole (bp 111 – 113 ˚C), napthalene (bp 218 ˚C) etc through diffusion, melting, or evaporation. Since no attempt to limit the temperature rise (pulsed voltage or limiting the current) due to Joule heating was made during FAN, it seems unlikely that Liu et al.[1,2] could retain the coating for repeated deposition. This further raises the uncertainty that the raised features in FAN are due to the material that was coated on the tip.

We estimated the tip coating thickness necessary to produce lines in FAN papers (Appendix I: Estimation of tip coating). We assumed that the material transferred from coated Si tip to the substrate was not chemically modified. Therefore, the total volume of deposition that could be achieved from the tip is equal to the volume of coating material applied on tip as per the law of conservation of volume. For our calculations, we used dimensions of the features deposited by Liu and Miller and found that very thick coatings are required to draw few lines (~5-10) of these dimensions. For example, we estimated that ~ 30-200 nm thick coating (figure 49) is required for deposition of 1-10 lines at -10 V tip bias (deposited by Liu and Miller as shown in the figure below).

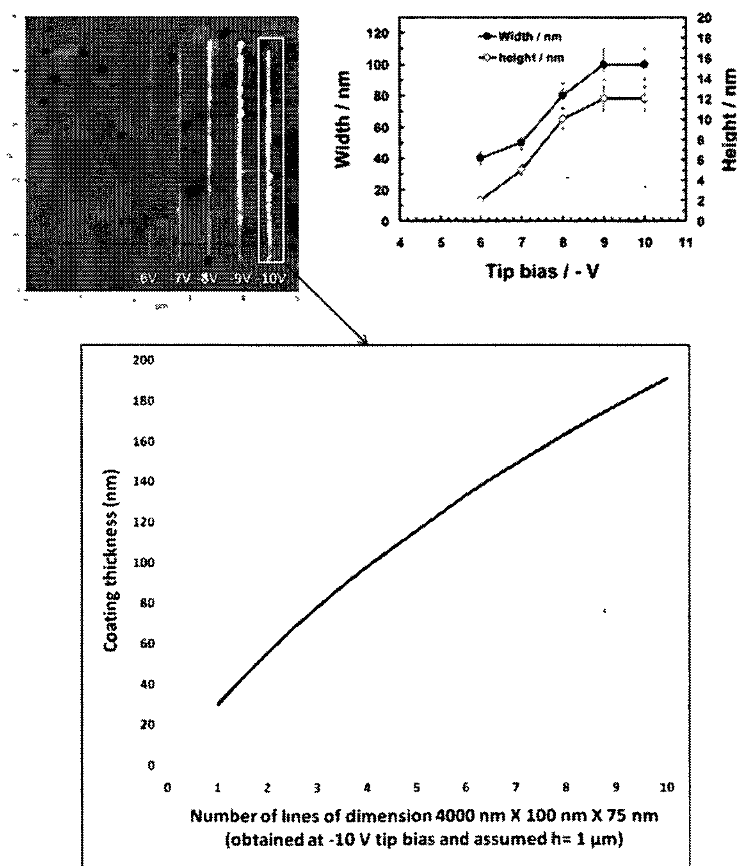

Figure 49: Estimated coating thickness for different number of lines fabricated using FAN at -10 V tip bias (bottom figure). The dimensions were taken from FAN paper[1] (top figure). The tip height (from apex) responsible for providing the molecules for deposition was taken as 1 μm.

Since no coating replenishment method was used, it seems unlikely that Liu et al. could have put enough coating material on the tip to make all lines and their SEM images show no evidence that this amount of material was removed. They also observed temporary loss of writing from the tip, which resumes again after some time. It is possible that the tip coating is consumed in first few applications of bias and the mounds produced after that are the result of surface modification due to the interaction of biased bare Si tip with gold or HOPG substrates by *mechanisms described in previous section.*

Further research is required targeting the fundamental uncertainties associated with FAN (described above). Once a reproducible and reliable single tip model of field assisted deposition is developed, scale up using multiple tips could be considered.

CHAPTER 6

FUTURE WORK

Suggestions for Future Work

In addition to the factors considered by Liu et al. (tip fabrication speed, tip bias and tip force), we found that the humidity and tip geometry also have a strong influence on the mechanics of surface modification during field assisted patterning. We suggest that further experiments should be performed in controlled environment to record the trend of tip damage (or oxidation) and feature sizes at different humidity settings. To control the tip damage for the bias range used in FAN, a more robust tip material or pulsed voltage should be used in future.

The solvent evaporation method for tip coating should be refined to produce uniform coatings. Some sort of tip surface modification to improve adhesion of coating molecules to the tip surface (such as silanization or surfactant) could be considered. The possibility of using different coating methods such as thermal evaporation should also be explored.

The scanning Auger microscope could be used to determine elemental composition of raised features on substrates. This will provide better understanding of the mechanism of surface modification.

CHAPTER 7

SUMMARY AND CONCLUSIONS

We studied the electrical nanocontact between a highly doped Si tip and ODT coated gold film on mica and HOPG substrates to understand the impact of current on material modification for negative tip biases up to 10V. The tip resistance evolves with time and eventually progresses to very high resistance (values even larger than 10^{11} Ω during the complete course of study). The I-V behavior is non linear for both tip-substrate combinations for a voltage range of 0 to -10V. The I-V behavior of coated tips (used by Liu & Miller) is same as uncoated tips. The tip radius increases with repeated exposure to negative tip bias. The oxide layer on the tip initially decreases but then increases with repeated exposure to negative tip bias (5-10V). The rate of oxidation is affected by humidity level.

The oxidation of silicon tip occurs by a combination of elevated temperatures (>150 °C) due to Joule heating and oxygen atoms/radicals formed due to extremely high electric field (> 10^8 Vm^{-1}). The heat transfer analysis showed that such oxidation of silicon could occur with negative tip biases > 6V at Si tip-gold/HOPG junction (~4 mW power for Si-gold and ~2.8 mW for Si-HOPG) in ambient conditions. It takes a significant power (> 20 mW) to heat a Si AFM tip to a high enough temperature to cause melting in both cases. We estimated high temperatures (~100-1100 °C) at the tip substrate interface due to Joule heating for bias conditions used by Liu et al.

(6 -10 V negative tip bias). This is well above the ambient and sufficient to cause modification of the tip coatings through diffusion, melting, or evaporation in both cases.

The nanostructures (only bumps, sub 20 nm to few hundred nm high) on gold substrate can be produced by applying negative tip bias (> 5 V) to coated or uncoated Si tips in contact with the substrate. The tip bias and tip fabrication speed have a strong influence on the formation of the bumps. The height and width of bumps increases with increase in magnitude of tip bias and tip hold time. For obtaining a desired pattern, one out of the two parameters should be kept constant. The bumps occasionally disappear with repetitive scanning leaving a pit behind and the bumps created in high humidity (> 60%) are more easily removed. The material modification occurs by a combination of mechanisms depending upon several factors including tip resistance (tip radius or/and oxide level at that time) and humidity level. The bumps are attributed to the formation of gold silicon alloy or gold hydroxide.

Both bumps and pits could be created on HOPG surfaces with coated or uncoated Si tips for negative tip bias > 4-5V. The tip fabrication speed, tip bias, tip force and humidity all have a strong influence on the formation of the bumps and trenches. We suspect that the bumps are produced by local modification of HOPG substrate, possibly formation of graphene oxide, under high electric field and there is no actual transfer of material from the tip. We have shown that there is no significant change in tip when used on HOPG unlike in the case of gold substrate. The slight blunting of the tip is attributed to the breaking of tip due to high static loads in contact mode AFM. The trenches are the result of oxidation of graphite to CO and CO_2 or the fracturing of graphene oxide by a combination of contact forces and buckling. The height of bumps produced on HOPG varies within the range of few angstroms to 2-3 nm.

Where most of the previous models of material transport assume that the tip is static and does not evolve during the application of the bias. We have clearly shown this not to be the case and this is one of our important findings.

At the same time, this work has identified some reliability and repeatability issues with the field assisted nanopatterning deposition method (using current protocol). Further research is required to address these issues in order to develop a reliable single tip model of FAN.

APPENDICES

APPENDIX A:

Temperature Dependence of Thermal Conductivity of Si

The conductivity of silicon varies with temperature[44]. From room temperature to the melting point of silicon, the conductivity decreases with increasing temperature as can be seen in figure below.

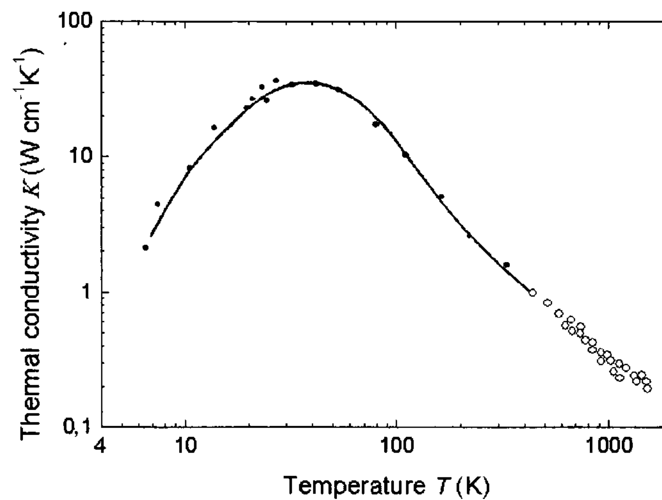

Figure 50: Thermal conductivity of Si with temperature.[44]

We plotted the conductivity versus temperature data for temperature range of 300 – 1000 K on a separate graph. We fitted the data by a power function: $Y = aX^b$ where Y is the conductivity of silicon, X is the temperature (K), and a and b are constants labeled in figure 51.

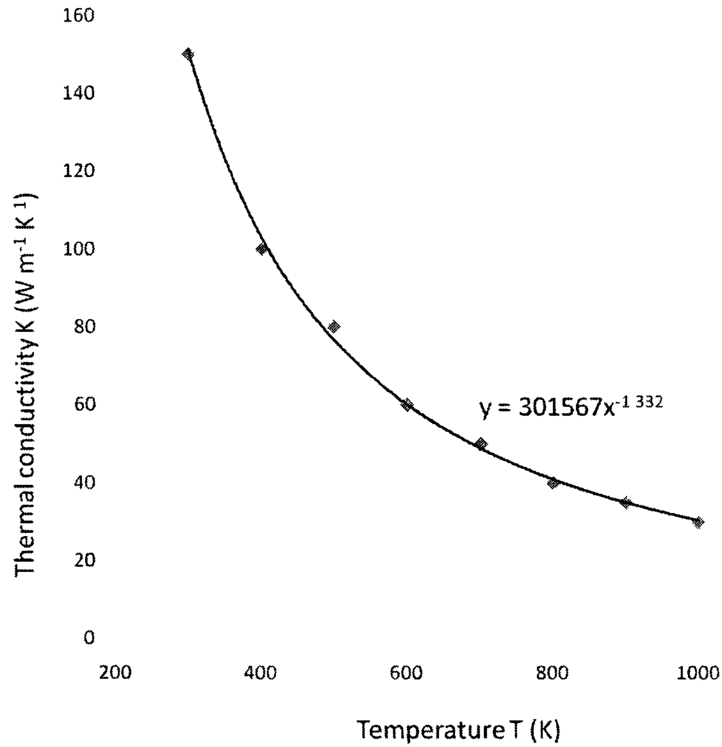

Figure 51: Thermal conductivity of Si with temperature in the range of 300- 1000 K. The data was fitted with power function of type $Y = aX^b$.

From figure 51, following relationship between the conductivity and temperature is established.

$$K = \frac{301567}{(T)^{1.332}} \qquad (10)$$

APPENDIX B:

<u>Thermal Conduction in Silicon</u>

In contrast to metals in which thermal conduction occurs by electronic transport, the dominant mechanism of thermal conduction in semiconductor materials is by lattice vibrations,

that is, phonons. A phonon is a quantum of energy associated with the vibrations of the atoms in the crystal. The heat absorbed in the hot region increases the amplitudes of the lattice vibrations.

Continuum models of heat transfer fail when the mean free path of heat carriers is greater than the characteristic dimensions of a system under consideration. Since the tip-substrate contact is of nanoscale dimension, it is important to compare it with the mean free path of phonon in silicon.

Calculation of Phonon Mean Free Path in Silicon (at 300K)

At room temperature, semiconductor data handbook[45] lists the following for Si:

K, Thermal conductivity = 130 $Wm^{-1}K^{-1}$

Y, Elastic modulus = 185 GPa

ρ, Density = 2.329 gcm^{-3}

c_s, Specific heat capacity = 0.7 $Jg^{-1}{}^{\circ}C^{-1}$

The phonon velocity (V_{ph}) is approximately equal to:

$$V_{ph} \approx \sqrt{\frac{Y}{\rho}} \sim 8912\ \mathrm{ms^{-1}} \tag{11}$$

Heat capacity per unit volume (C_v) is given by:

$$C_v = c_s\rho \sim 1.63\ \mathrm{X}\ 106\ \mathrm{JK^{-1}m^{-3}} \tag{12}$$

The phonon mean free path is therefore,

$$l_{ph} = \frac{3K}{C_v V_{ph}} \sim 25\ \mathrm{nm} \tag{13}$$

APPENDIX C:

AFM Tip Used in our Experiments

We used the conical shaped highly doped Si (n-type) tip manufactured by Micromasch (figure 52). The material and dimensional details are listed below (data taken from manufacturer's website).

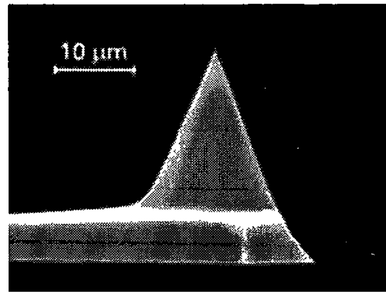

Figure 52: SEM image of uncoated highly doped silicon SPM probe tip (Image taken from MikroMasch website).

Typical probe tip radius of uncoated tip: ~10 nm

Full tip cone angle: 40°

Tip aspect ratio: more than 3:1 (4:1 typical)

Probe material: n-type silicon (phosphorus doped)

Probe bulk resistivity: 0.01-0.05 Ohm-cm

Total tip height: 20-25 μm

Cantilever width: 35 μm

Cantilever length: 130 μm

Cantilever thickness: 1 μm

APPENDIX D:

Instrument Details for SEM-EDS Evaluation

Scanning Electron Microscopy

The Amray 3300FE field emission SEM with PGT Imix-PC microanalysis system provides three-dimensional visual interpretation and elemental analysis of a specimen surface. The electron optics allow a depth of focus nearly 300X that of the light microscope, as well as a magnification range from 15X to 100kX at accelerating voltages from 1-25kV. The SEM resolution at 25kV is 1.5 nm. The 2048x2048 frame buffer allows high resolution (4.8 MB.tif) micrographs to be saved on the SEM computer.

Energy Dispersive Spectroscopy

The AMR 3300FE SEM is equipped with a PGT Imix-PC energy-dispersive X-ray microanalysis system, which allows the operator to control the microscope beam position while using the EDS software. The system uses an atmospheric thin-window detector capable of detecting carbon X-rays. X-ray maps of up to 8 elements can be obtained simultaneously. The digital images and X-ray maps can be stored for later viewing and analysis, and X-ray elemental maps can be color coded by element.

APPENDIX E:

Thermal Oxidation of Si

Thermal oxidation of silicon is the formation of a silicon dioxide (SiO_2) film on a silicon surface under very high temperatures. It is usually performed at a temperature between 500 and 1200°C.

Chemical Reactions

It may use either water vapor (steam) or molecular oxygen as the oxidant; it is consequently called either wet or dry oxidation. The oxidation reaction under ambient conditions is one of the following:

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad (14)$$

$$Si + O_2 \rightarrow SiO_2 \quad (15)$$

Wet oxidation has the higher oxide growth rate and therefore is preferred to dry oxidation for growing thick oxides.

APPENDIX F:

Mean Free Path of Doped Silicon and Estimation of Probe Resistance

Calculation of Mean Free Path of Electrons in Si (at 300 K)

Continuum model of conductivity fail when the mean free path of electrical carriers is greater than the characteristic dimensions of a system under consideration. Since the tip is of nanoscale dimension, it is important to compare it with the mean free path of electrons in Si tip.

We used highly doped n-type silicon tips for our experiments. The resistivity range of the material is provided by the manufacturer (0.01-0.05 Ω-cm). For the given resistivity, the

doping density can be estimated ($\sim 1.0\,X\,10^{18}\text{cm}^{-3}$) using the resistivity vs. doping density plot.[46] The electron mobility corresponding to this doping density is obtained using mobility vs. doping density plot.[46]

The electron mobility can also be given by equation below:

$$\mu_e = \frac{e\tau}{m_e^*} \tag{16}$$

where m_e^* is the effective mass of the electron in Si (the effective mass accounts for the internal forces experienced by the electron in a crystal), τ is the mean free time between scattering events and is given by:

$$\tau = \frac{l}{v} \tag{17}$$

where l is the mean free path of the electron and v is the mean speed of the electron. In the conduction band and in one dimension, the mean kinetic energy of electrons is $\frac{1}{2}KT$, so $\frac{1}{2}KT = \frac{1}{2}m_e^* v^2$. This gives:

$$v = \sqrt{\frac{kT}{m_e^*}} \tag{18}$$

The mean free path of electron in silicon is given by combining equations 16, 17 & 18:

$$\text{Mean free path, } l = \frac{\mu_e}{e}\sqrt{(m_e^* KT)} \tag{19}$$

By substituting values of electron mobility, effective mass of electron (~1.08 m_e), K (= 1.38 X 10^{-23} J/K) and T (= 300 K) in equation 19, we get l as 700-1000 nm.

Estimation of Probe Resistance

The probe resistance can be estimated by modeling it as two resistors in series, one coming exclusively from the cantilever and the other from the tip. The resistance of the cantilever can be calculated, using the following expression:

$$R_{cantilever} = \rho.\frac{l}{w.h} \tag{20}$$

where *l* is length, *w* is the width, and *h* is the thickness of the cantilever. Given the resistivity ρ (0.01-0.05 Ω-cm) of the material, the resistance of the cantilever ($R_{cantilever}$) is between 300 and 400 Ω.

The resistance of the tip (R_{tip}) can be calculated by using slices of the conical tip, and integrating over the entire length of the tip.

$$R_{tip} = \int_{l_1}^{l_2} \rho.\frac{l}{\pi.r^2}\ dl \tag{21}$$

where l_1 is mean free path of Si (the tip is supposed broken at the apex where the dimension is inferior to the electron mean-free path of doped silicon, ~700-1000 nm in this case), l_2 is the total length of the tip (~20 µm) and r is the radius of the cone at a length l from the tip apex, which is given by:

$$r = l\ \tan\theta \tag{22}$$

where θ is half included angle of tip (~15°). By solving for (21) and (22), we can get the resistance of the tip.

The estimated tip resistance (R_{tip}) lies between 300-1000 Ω. Therefore, the total resistance offered by the probe is on the order of 600-1400 Ω.

APPENDIX G:

Contact Resistance

When the contact dimension is very small (comparable to the electron mean free path of the material), the contact resistance is given by Sharvin law:

$$R = \frac{4\rho l}{3\pi a^2} \tag{23}$$

where a denotes the contact spot radius, ρ and l the resistivity and the electron mean path of the material respectively. If l is ~750 nm, a is ~50 nm and ρ is 0.01 Ω-cm, the Sharvin resistance is equal to ~13 kΩ.

APPENDIX H:

Highly Ordered Pyrolitic Graphite (HOPG)

Pyrolytic graphite is a graphite material with a high degree of preferred crystallographic orientation of the axes perpendicular to the surface of the substrate, obtained by graphitization heat treatment of pyrolytic carbon or by chemical vapor deposition at temperatures above 2500°K. Hot working of pyrolytic graphite by annealing under compressive stress at approximately 3300°K results in highly oriented pyrolytic graphite (HOPG). Thus HOPG is a highly-ordered form of high-purity pyrolytic graphite.

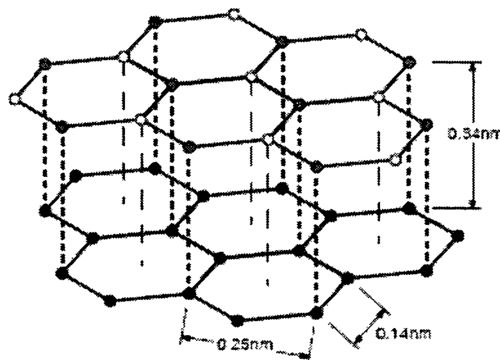

Figure 53: Schematic of atomic structure of HOPG.[47] The distance between layers is ~ 0.34 nm.

HOPG belongs to lamellar materials because its crystal structure is characterized by an arrangement of carbon atoms in stacked parallel layers – the two-dimensional and single-atom thick form of carbon that is called graphene. Graphite structure can be described as an alternate succession of these identical staked planes. Carbon atoms within a single plane interact much stronger than with those from adjacent planes. The distance between layers is ~ 0.34 nm.

Due to the anisotropic nature of HOPG such characteristics as thermal conductivity and electrical resistivity are different in different directions: along the basal plane and along the principal axis (perpendicular to the basal plane).

HOPG is an excellent tool for using in scanning probe microscopy as a substrate or calibration standard at atomic levels of resolution. It has an ideal atomically flat surface and provides results in a featureless background. This is vital for SPM measurements that require uniform, flat, and clean substrates, for samples where elemental analysis is to be done.

APPENDIX I:

Estimation of Tip Coating

The primary goal of this analysis is to estimate the tip coating thickness required for the transfer of different molecules from tip to the substrate by the field assisted deposition method. We assumed that the material transferred from tip to the substrate was not chemically modified. Therefore, the total volume of deposition that could be achieved from the tip is equal to the volume of coating material applied on the tip as per the law of conservation of volume.

Assumptions and Calculations

We assumed that (i) the coating thickness is uniform throughout the tip surface (ii) all the coating molecules available on the tip are transferred to the substrate when tip bias is applied (iii) the tip is modeled as a truncated cone with a hemisphere with radius equal to the radius of curvature of the Si tip as shown in figure 54. (iv) Although the real height of the tip is approximately 20-25 μm, we set the height of the tip to H (10 to 1000 nm) for our calculations since the probability of material transfer on the substrate is maximum from the coating available near the tip apex and decreases as we go higher.

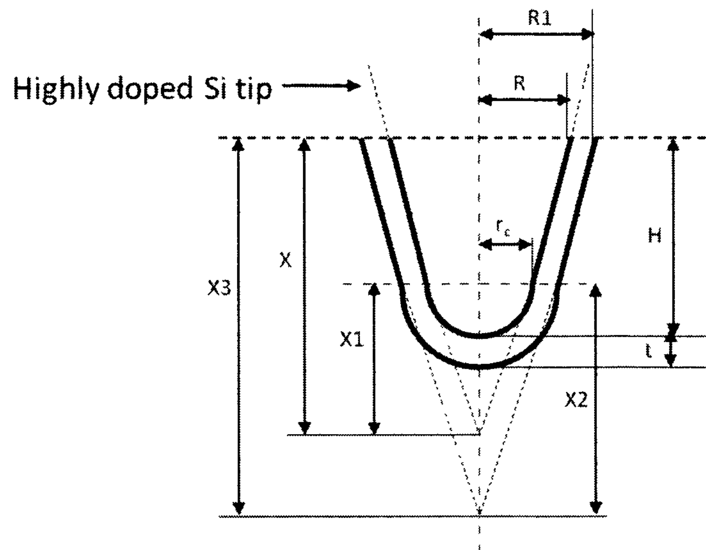

Figure 54: Schematic of the geometry of the coated tip. The tip is modeled as a truncated cone with a hemisphere at the end.

For our calculations, we used dimensions of the features deposited by Liu and Miller using field assisted nanopatterning. Figure 55 shows the patterning of [60]fullerene molecules on octadecanethiol-coated Au(111) at different tip bias values. The lines were fabricated using tip bias values of -6, -7, -8, -9, and -10 V (from left to right in the left image) and a fabrication speed of 100 nm/s.

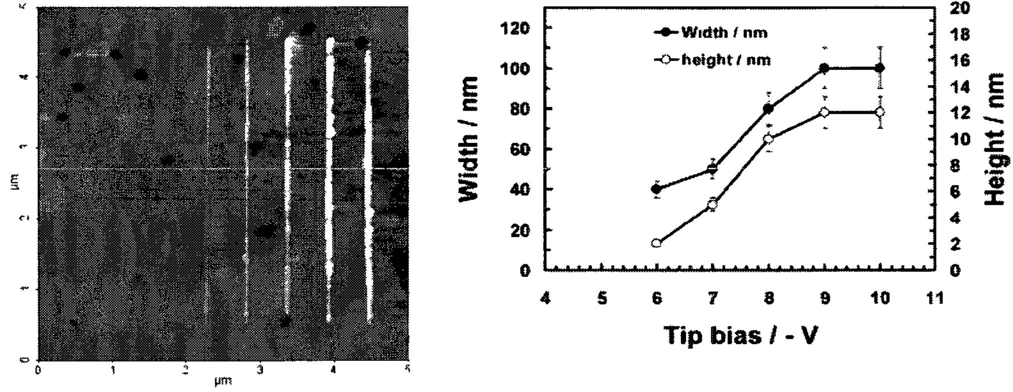

Figure 55: Nanofeatures deposited on gold using C60 coated Si tip. The lines were fabricated using tip bias values of -6, -7, -8, and -10 V and a fabrication speed of 100 nm/s.[1]

The total volume of the material deposited on the substrate in figure 55 can be calculated by:

$$V_s = V_{-6} + V_{-7} + V_{-8} + V_{-9} + V_{-10} \quad (24)$$

where V_{-6}, V_{-7}, V_{-8}, V_{-9} and V_{-10} is the volume of lines deposited at -6, -7, -8, -9 and -10 V tip bias respectively (calculated using the formula for volume of a cuboid $(l \times b \times h)$). The volume of tip coating required to produce these lines should be equal to V_s as explained above and can be calculated by:

$$V_c \; or \; V_s = V_{ct} - V_{bt} \quad (25)$$

where V_{ct} and V_{bt} is the volume of coated and bare tip respectively and can be calculated as follows (refer figure 54 for nomenclature):

$$V_{bt} = \frac{1}{3}\pi R^2 X - \frac{1}{3}\pi r_c^2 X1 + \frac{2}{3}\pi r_c^3 \quad (26)$$

$$V_{ct} = \frac{1}{3}\pi R_1^2 X_3 - \frac{1}{3}\pi (r_c + t)^2 X_2 + \frac{2}{3}\pi (r_c + t)^3 \quad (27)$$

where r_c is the radius of curvature of the tip (= 10 nm) and X, X_1, X_2, X_3, R and R_1 can be obtained as follows (15° is half included angle of the tip):

$$X_1 = {}^{r_c}/_{\tan(15^\circ)} \tag{28}$$

$$X = H - r_c + X_1 \tag{29}$$

$$X_2 = {}^{(r_c + t)}/_{\tan(15^\circ)} \tag{30}$$

$$X_3 = H - r_c + X_2 \tag{31}$$

$$R = X \tan(15^\circ) \tag{32}$$

$$R_1 = X_3 \tan(15^\circ) \tag{33}$$

By solving equations 24, 25, 26, 27, 28, 29, 30, 31, 32 and 33, we can obtain coating thickness (t) as a function of tip height (H).

The minimum coating thickness required for obtaining features in figure 55 as a function of tip height is plotted in figure 56.

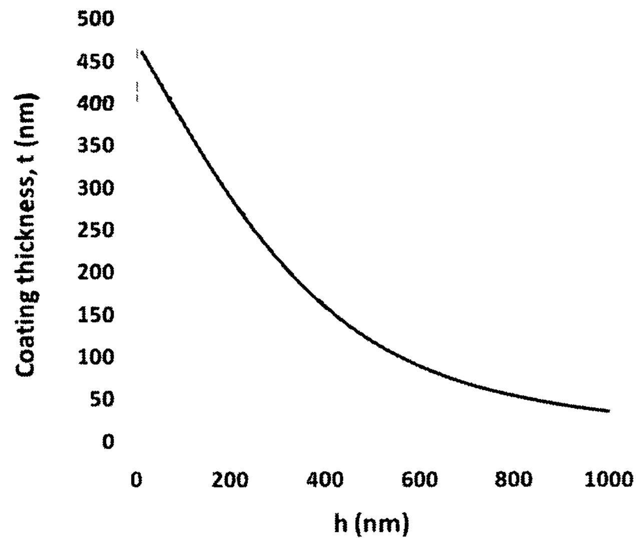

Figure 56: Estimated coating thickness as a function of functional tip height (h) for fabrication of lines drawn in FAN paper.[1]

The required thickness decreases with an increase in functional tip height. It can also be seen that about ~50 nm thick coating of C60 is required at tip height (H) of 1000 nm.

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