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# S.H.I.E.L.D Relays (Shadow-masked Hack-proof Ion Etched Latch Deterrence Relays)

Anh Dinh

*Virginia Commonwealth University*

Adrienne Ilustre

*Virginia Commonwealth University*

Thomas Nuckols

*Virginia Commonwealth University*

Sean Payne

*Virginia Commonwealth University*

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# SHIELD Relays \*Patent pending\*

(Shadow-masked Hack-proof Ion Etched Latch Deterrence Relays)

ECE 413 | Team members: Anh Dinh, Adrienne Ilustre, Thomas Nuckols & Sean Payne | Faculty adviser: Dr. Gary M. Atkinson

CAPSTONE DESIGN EXPO 2017

## Abstract

This project presents micro-scale logic devices using single cantilever relays fabricated in-plane from single crystal silicon. The devices will be a self-reliant entity that uses only a voltage source to operate. Thus allowing the relay to be free of any computer or internet based software that could potentially be hacked. This applied voltage will produce an electric field that will cause the actuator contacts to attract, closing the latch, allowing the ideal applied voltage to successfully control the relay. Because these devices are fabricated from silicon, they are extremely reliable, durable and adaptable. The logic devices are also rad-hard and chemically resilient. This allows the devices to remain durable in many types of environments, from satellites orbiting the earth, to submarines in the depths of our oceans. Industrial manufacturing plants with harsh chemicals and nuclear power plants could benefit from these devices as well. The patent pending shadow mask technique will be implemented to metalize sidewall trenches obtained through deep reactive ion etching.



Top view of design without supply voltage.

Top view of design with supply voltage

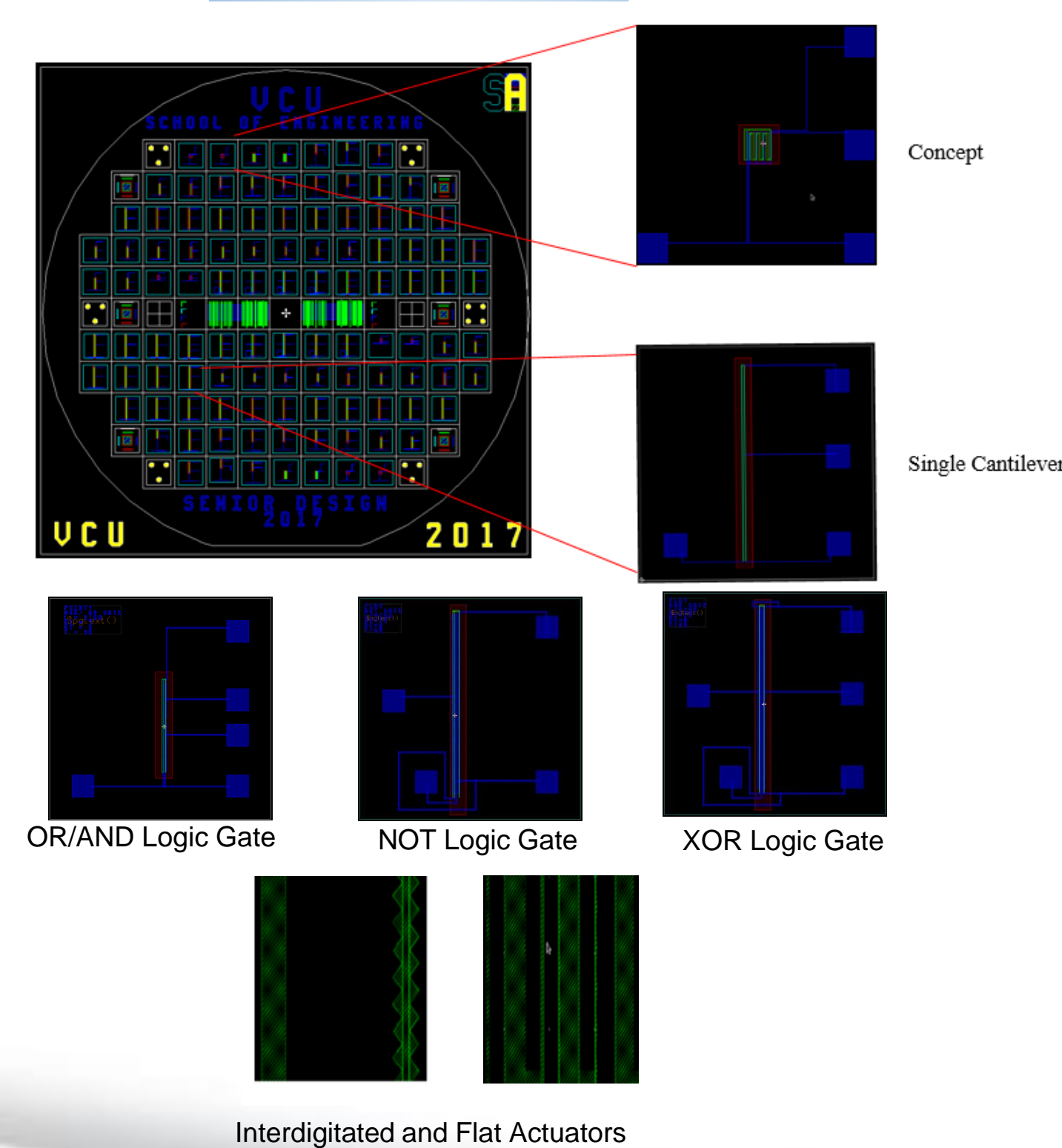
## Key Features

- Single Crystal Silicon
- In-plane
- Rad Hard
- System Voltage Adaptability
- Hack-Proof
- Shadow Masked Metallization

## Design

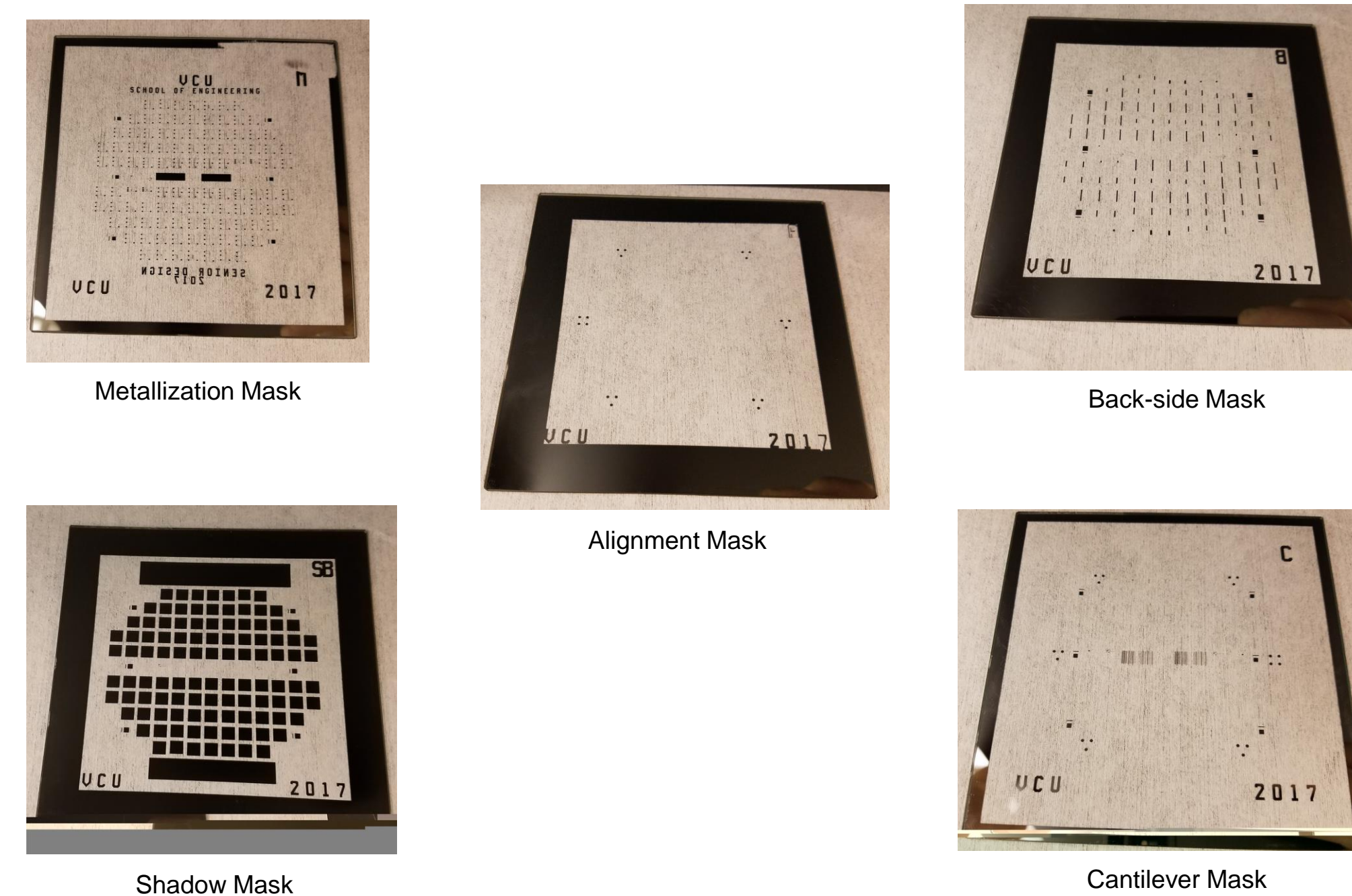
Device Type (um)	Length Cantilever	Length electrode	Width electrode	Gap electrode	Gap contact	Thickness	Operating Voltage [V]
<b>L = 1500</b>							
1500	1450	25	5	3	30	63.1	
1500	1450	25	5	3	50	135.7	
1500	1450	25	7	5	30	104.4	
1500	1450	25	7	5	50	224.7	
1500	1450	75	5	3	30	63.1	
1500	1450	75	5	3	50	135.7	
1500	1450	75	7	5	30	104.4	
1500	1450	75	7	5	50	224.7	
<b>L = 2100</b>							
2100	2050	25	5	3	30	31.5	
2100	2050	25	5	3	50	67.9	
2100	2050	25	7	5	30	52.3	
2100	2050	25	7	5	50	112.4	
2100	2050	75	5	3	30	31.5	
2100	2050	75	5	3	50	67.9	
2100	2050	75	7	5	30	52.3	
2100	2050	75	7	5	50	112.4	
<b>L = 4200</b>							
4200	4150	25	5	3	30	7.7	
4200	4150	25	5	3	50	16.6	
4200	4150	25	7	5	30	12.8	
4200	4150	25	7	5	50	27.4	
4200	4150	75	5	3	30	7.7	
4200	4150	75	5	3	50	16.6	
4200	4150	75	7	5	30	12.8	
4200	4150	75	7	5	50	27.4	
<b>Specialty</b>							
500	480	25	5	3	10	110.7v	

## Layout



## Fabrication Process

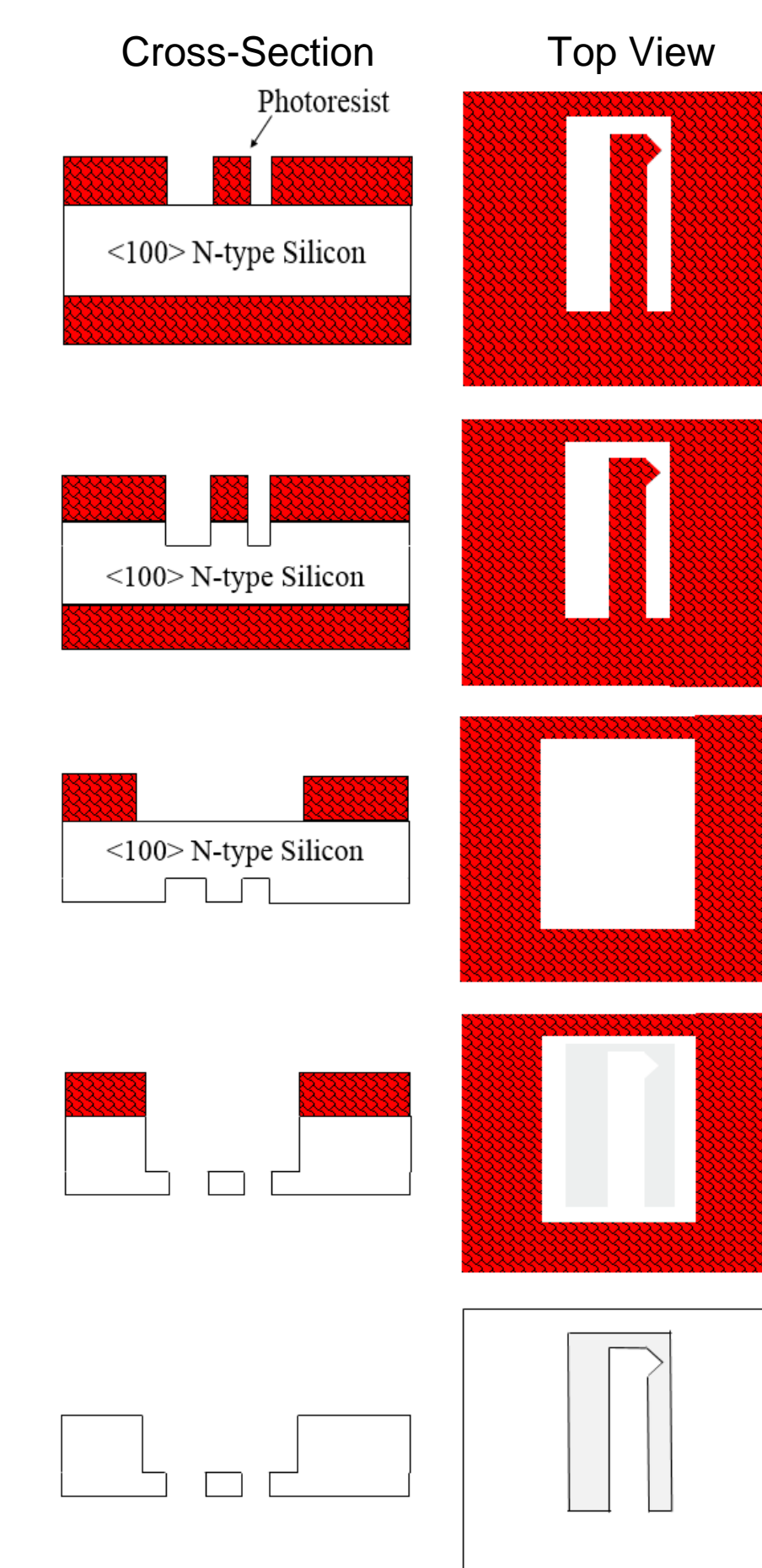
### Mask Fabrication



### Shadow Mask with Alignment Post

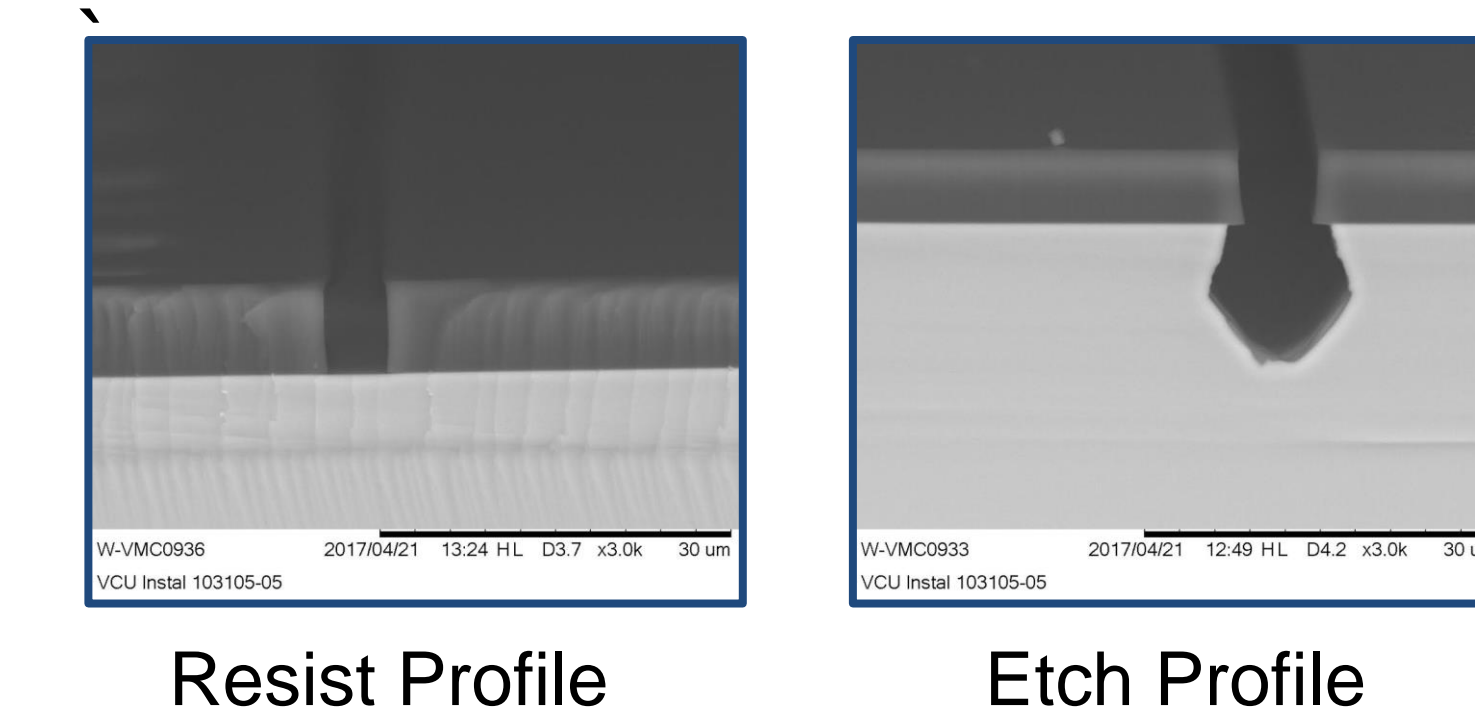
This project involves a new processing procedure using hi-resolution shadowing techniques that improves the fabrication of these devices. By using the hi-resolution shadow mask, we are able to reduce the number of steps required to fabricate the logic devices, shorten the processing time and reduce the chemical waste from fabrication. This allows the devices to be fabricated at a lower cost while also reducing the environmental impact from chemical waste.

### Relay Fabrication Process

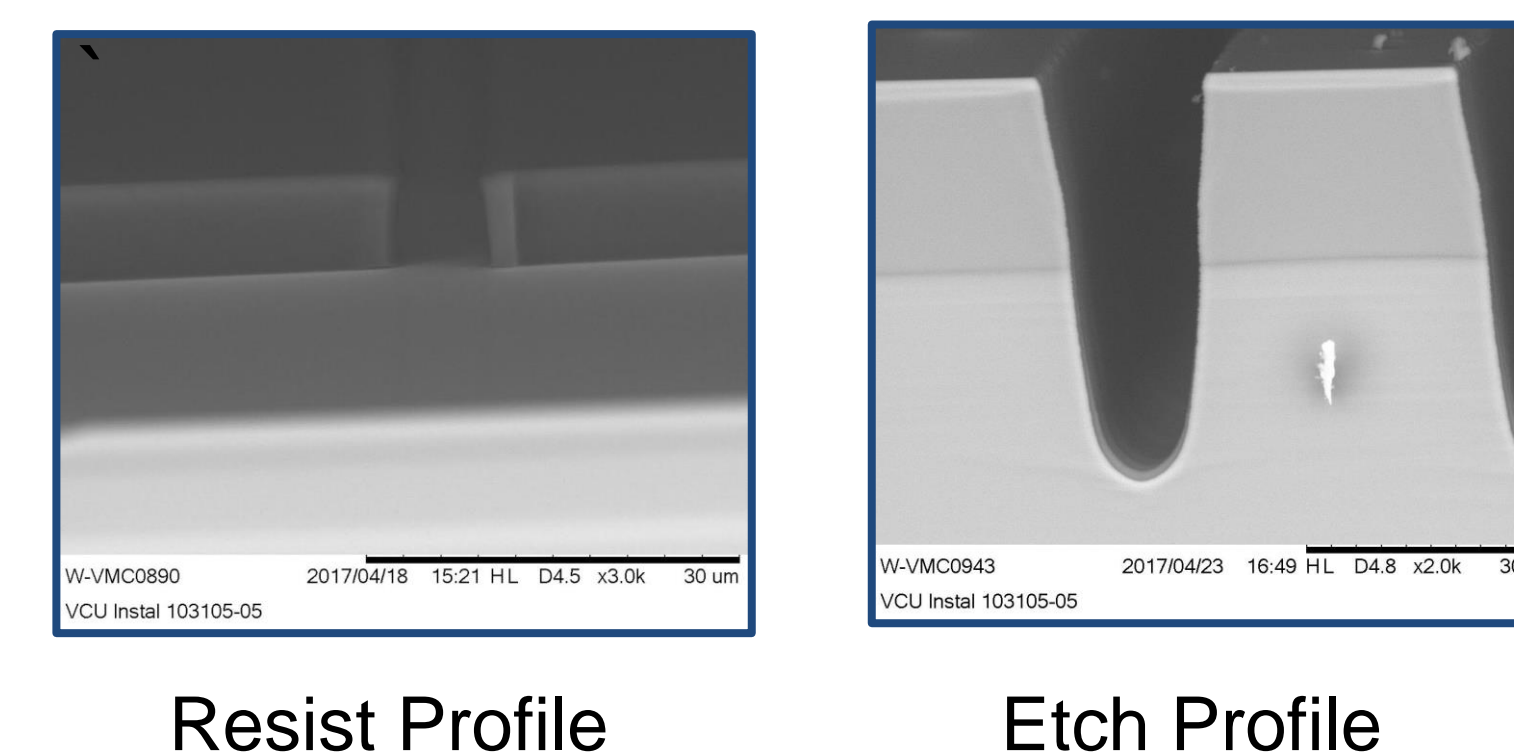


### DRIE Etch Characterization

### AZ P4620 Mask

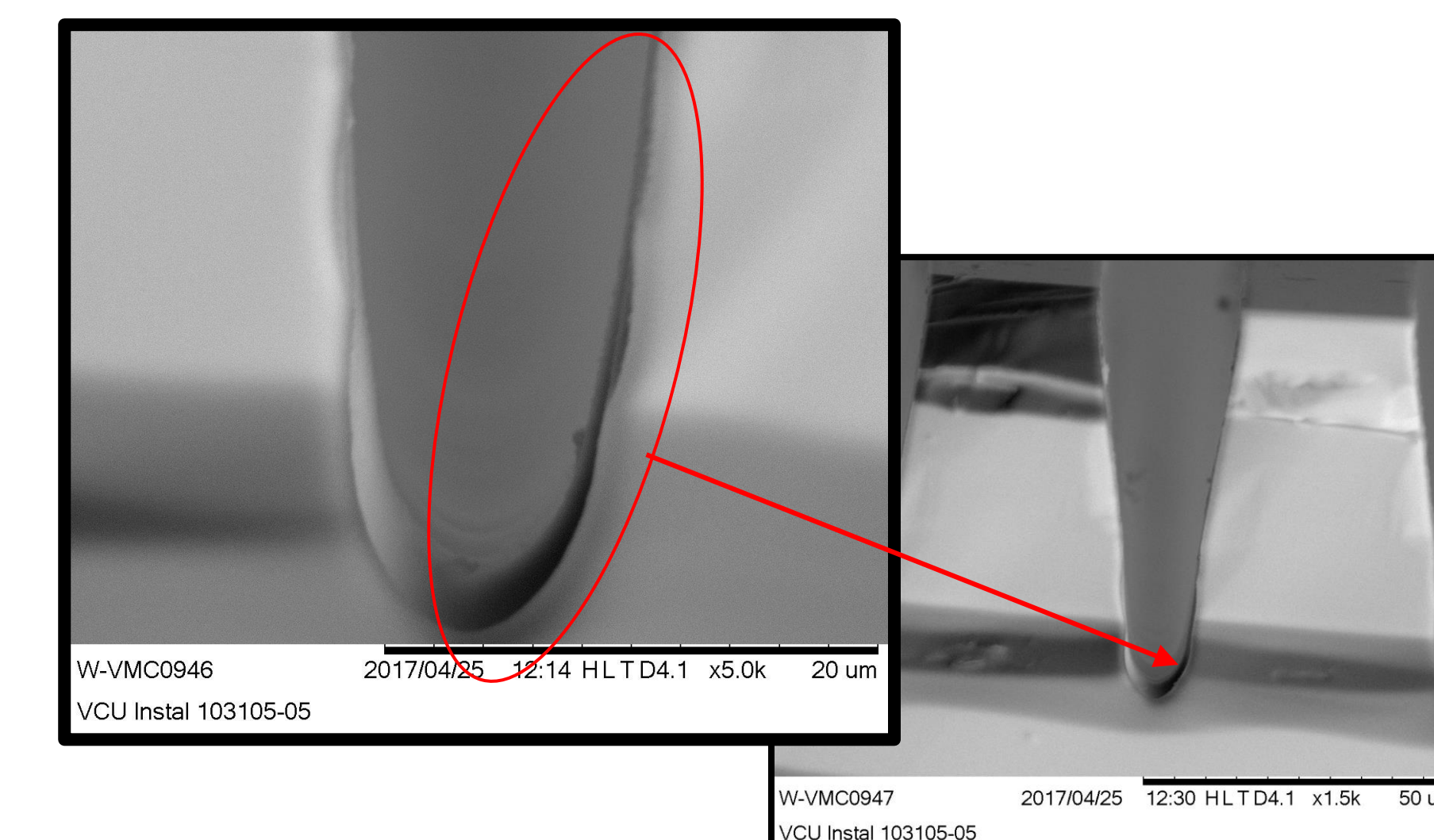


### SU-8 5

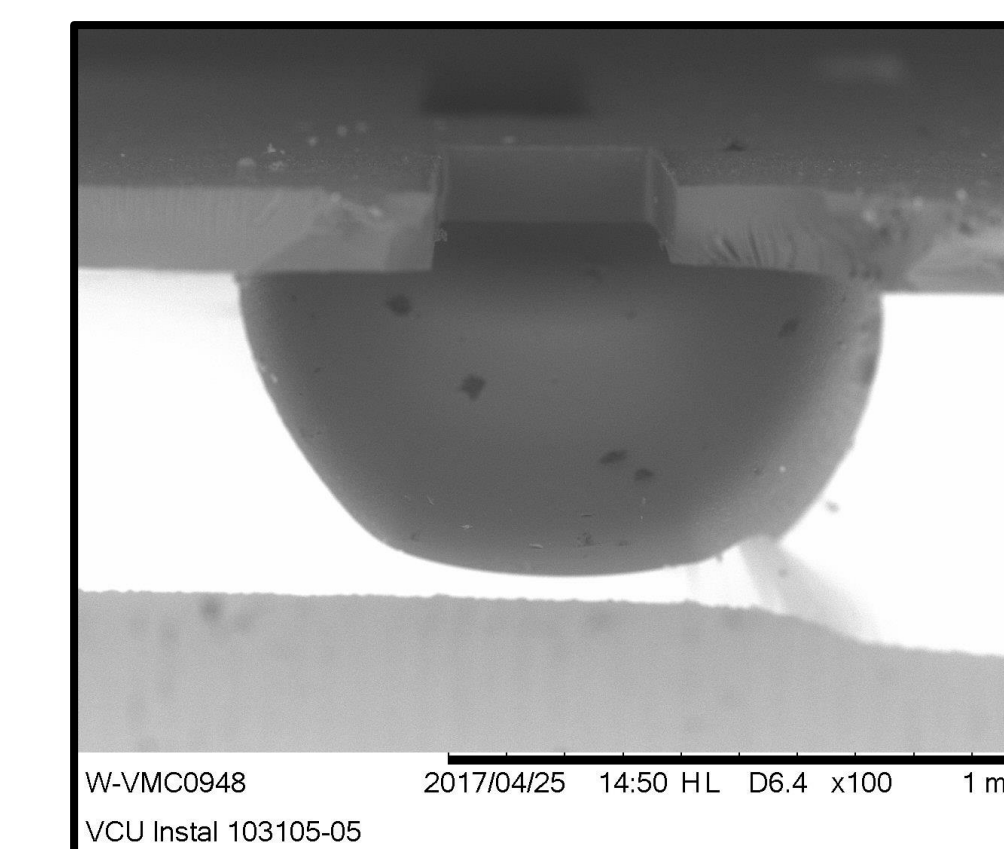


## Testing & Results

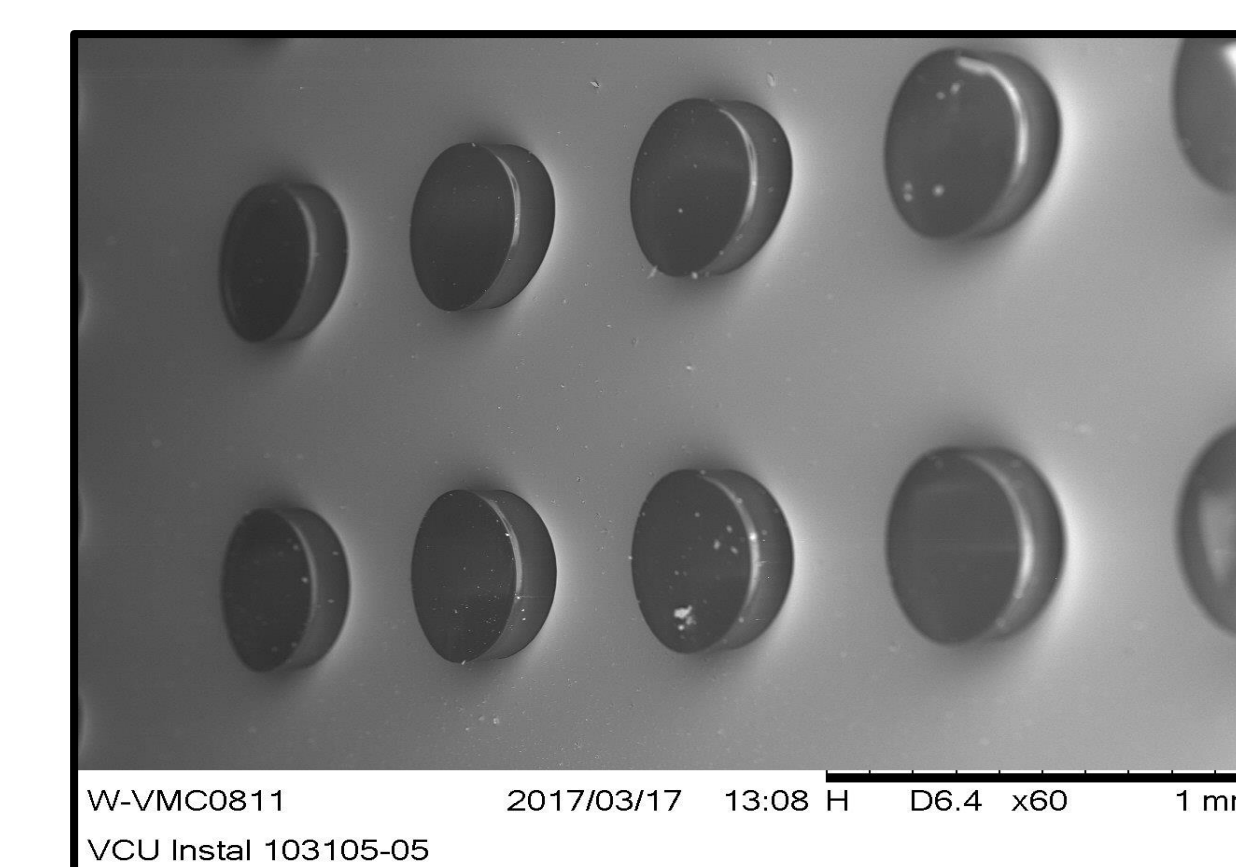
### Side-Wall Metallization



Side-Wall Metallization



Through Wafer Etch



SU-8 Post/Hole Alignment

## Conclusions

With the Shadow Mask and the DRIE process being a key element to this project, we were able to achieve feasible designs and completed mask designs. We were also able to have sidewall contacts through-wafer etching and alignments. This project still needs to be worked on to make this process perfect. This project has also applied for a VCU invention disclosure and also has patent pending.