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Model Development and Assessment of the Gate Network
in a High-Performance SiC Power Module

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

William Austin Curbow
University of Arkansas
Bachelor of Science in Electrical Engineering, 2014

May 2019
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This thesis is approved for recommendation to the Graduate Council.

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ABSTRACT

The main objective of this effort is to determine points of weakness in the gate network of a high-performance SiC power module and to offer remedies to these issues to increase the overall performance, robustness, and reliability of the technology. In order to accomplish this goal, a highly accurate model of the gate network is developed through three methods of parameter extraction: calculation, simulation, and measurement. A SPICE model of the gate network is developed to analyze four electrical issues in a high-speed, SiC-based power module including the necessary internal gate resistance for damping under-voltage and over-voltage transients, the disparity in switching loss between paralleled devices due to propagation delay, a high-frequency oscillatory behavior on gate voltage due to die-to-die interactions, and current equalization in the kelvin-source signal path. In addition, the analysis of parameter variance between paralleled MOSFETs and the effects of mismatched threshold voltage and on-state resistance on switching loss and junction temperature are investigated. Finally, three Miller Clamp topologies are simulated and assessed for effectiveness culminating in a solution for parasitic turn-on in high dv/dt systems such as those utilizing high-performance SiC power modules.

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CHAPTER 1

INTRODUCTION

1.1 Importance of Reliable Power Semiconductor Packaging

Electrical energy supplied roughly 40% of the world's power requirements in 2013 and has been increasing rapidly as countries migrate to renewable energy sources [1]. Global investment in clean energy has increased immensely in the past fifteen years from approximately $62 billion dollars spent on renewables in 2004 to a staggering $333 billion dollars in 2017. As of late, the world's leader in renewable investment, China, has increased its spending on alternative energies by 24% in the past year as shown in Figure 1. In addition, The United States now generates 18% of its electricity from renewable energies while its reliance on coal has decreased from 48% in 2008 to only 30% in 2017 [2]. This clear global trend marks an incredibly important shift in energy production and will have a massive impact on the surrounding industries.

Alternative energy sources such as solar, wind, and hydropower are made possible with the use of power electronics, which is the general term for the systems capable of converting and controlling

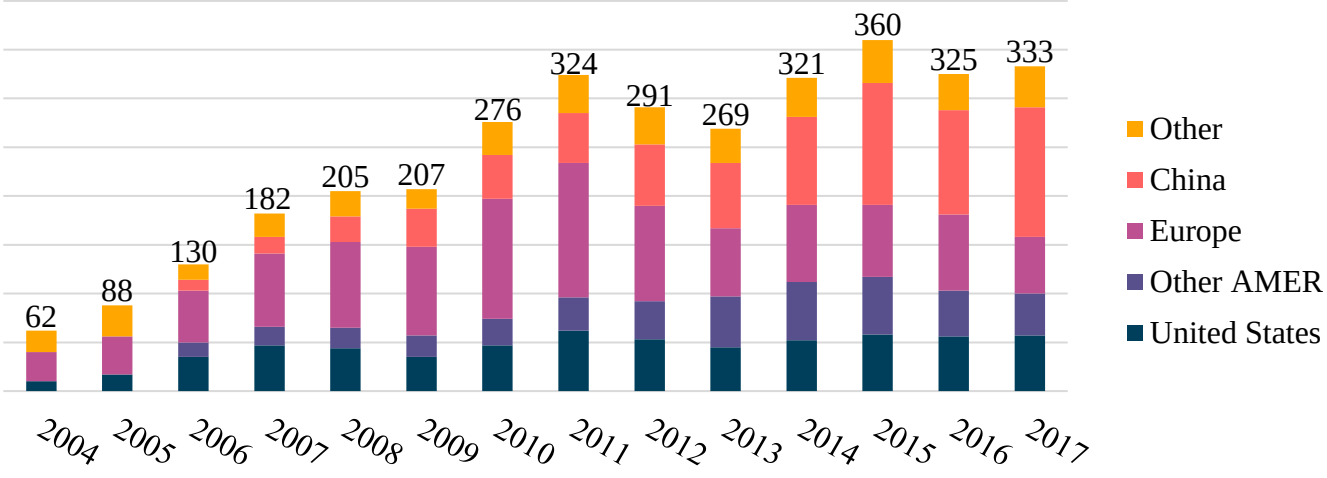

Figure 1. Total New Investment in Clean Energy by Country or Region

the flow of electrical energy [3]. At the core of these power electronics lies the power semiconductor, which is traditionally a silicon transistor capable of processing high magnitudes of voltage and current. Even with efficiency ratings of 96% to 99% for modern switch-mode power electronics systems [4], it is not feasible to use a single power semiconductor device per switch position in a system. To meet the requirements of the high-power systems responsible for converting energy obtained from renewables to consumable power on the grid, multiple power semiconductor devices must be operated in parallel inside an electronic package commonly referred to as a power module.

A power module is described as one or more power semiconductor devices in a package, in which the package and connection technology are just as important as the characteristics of the power semiconductor [3]. During construction and operation of a power module, there exist many mechanical, electrical, and thermal factors, which have a large impact on the performance and reliability of a system. According to Infineon, for this technology to be applied, the power modules

Figure 2. Common Power Modules Ranging from 10 A to 3600 A and 600 V to 6.5 kV [5]

must be robust and durable; moreover, in traction applications, lifetimes of 20 years or more are required with the need for a high-power cycling capability [3]. A few common silicon-based power modules from Infineon are displayed in Figure 2 [5].

Recently, power electronics are being utilized in applications such as motor drives for industry and HVAC, for traction drives in electric vehicles, and for data centers, which now consume over two percent of the United States and Europe's electricity consumption [1]. With these innovative utilizations of power electronics, it is crucial that the fundamental building blocks of these systems, the power modules, be durable, robust, and reliable for the countless energy conversion applications that the future will bring [4].

1.2 Next Generation Power Modules Using Wide Bandgap Power Semiconductors

The demands for high-performance power electronics are quickly surpassing the voltage rating, efficiency, and power density limitations governed by the intrinsic properties of silicon-based power semiconductors. Fortunately, a higher-performing alternative is growing in adoption and therefore becoming increasingly better understood, more reliable, and less expensive [6]. This next generation power semiconductor is Silicon Carbide (SiC), which is considered a wide bandgap semiconductor and exhibits an increase in bandgap energy of nearly three times that of silicon.

There are four main elements that differentiate SiC power semiconductors from silicon: bandgap, field strength, thermal conduction, and electron mobility [7]. The first, bandgap energy, allows the technology to operate at a higher junction temperature, which in turn allows the entire system to process more power in less space [8]. Next, SiC's much higher field strength enables high blocking voltages, low leakage currents, and a smaller drift region. This allows SiC to have a greatly reduced specific on-state resistance for an equivalent blocking voltage to Si; moreover, it

allows SiC to operate at voltages that were considered impossible in power electronics with Si technology. Third, the thermal conductivity of SiC is 3.7 W/cm·K while silicon exhibits roughly 1.6 W/cm·K [9]. This increase in thermal conductivity leads to higher current-carrying capability and more power-dense electronics. Finally, the higher electron mobility as well as the higher electron saturation velocity allows for higher frequency operation [7]. As commonly known, the increase in switching frequency of a power system directly influences the size of passive components and greatly increases power density.

As described in SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors, one of the most tangible advantages of SiC is the significantly reduced switching loss [11]. This is partially due to the lack of the current tail found in Si IGBT devices and the ability to eliminate reverse recovery through

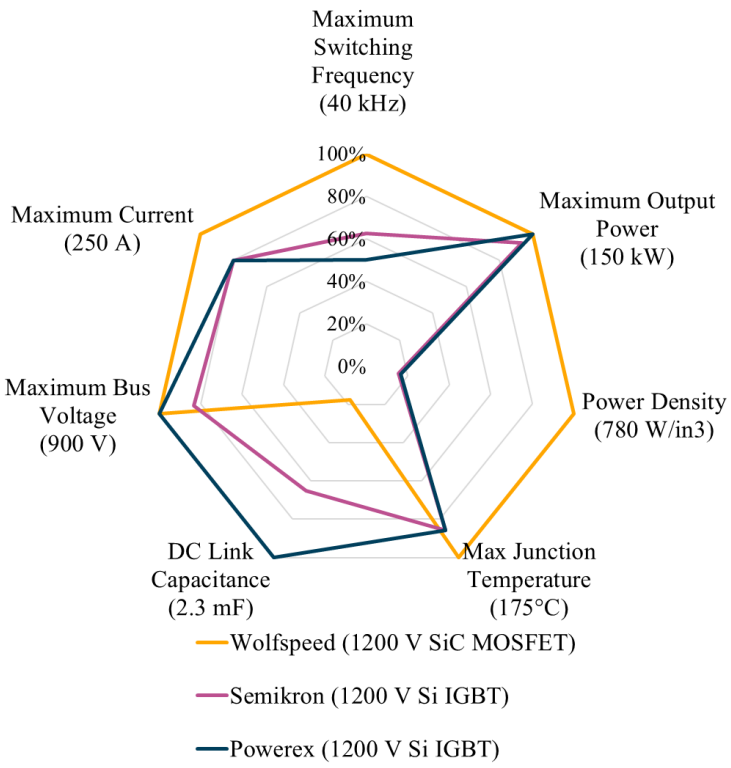

Figure 3. Performance Improvements of SiC over Si-based Inverters [10]

the use of an anti-parallel SiC Schottky diode [9]. Figure 3 portrays three technology demonstrating inverters: one using Wolfspeed's 1200 V SiC MOSFETs and the other two using silicon IGBT technology. As clearly illustrated in the figure, the SiC inverter exceeds the Si versions in switching frequency rating, maximum current rating, power density, maximum bus voltage, maximum junction temperature rating, and requries the lowest DC link capacitance [10]. The large improvements over silicon make SiC a perfect candidate for future power modules and power electronic technology. As stated by Joseph Carr, et al., "This is particularly true at medium-voltage levels where fast switching devices based on silicon are nonexistent and where new and ultra-efficient converter systems are required for future energy distribution networks." [12]. Considering the need for power electronics to unleash the full potential of alternative energy sources as discussed in the previous section, SiC is the suitable semiconductor technology to fill the current voids in power conversion systems.

1.3 Issues in Silicon Carbide Power Modules

Significant advancements in semiconductor technology do not come without inherent challenges. The same fast-switching behavior that permits power-dense and high-efficiency converters carries with it negative side-effects that need to be well understood when designing power modules and systems using wide bandgap technology [13]. One key side-effect under investigation in this effort is a high-frequency oscillatory behavior measured on the gate node of SiC power modules when operated at high-speeds (large dv/dt and di/dt). Under extreme circumstances this phenomenon can become unstable and destroy the switch position in the power module. An example of these high-frequency oscillations can be seen in Figure 4, which was obtained during double-pulse testing in a clamped inductive load simulation. The gate voltage waveform exhibits frequencies greater than 100 MHz that begin to grow rapidly during the turn-off of the module. This event

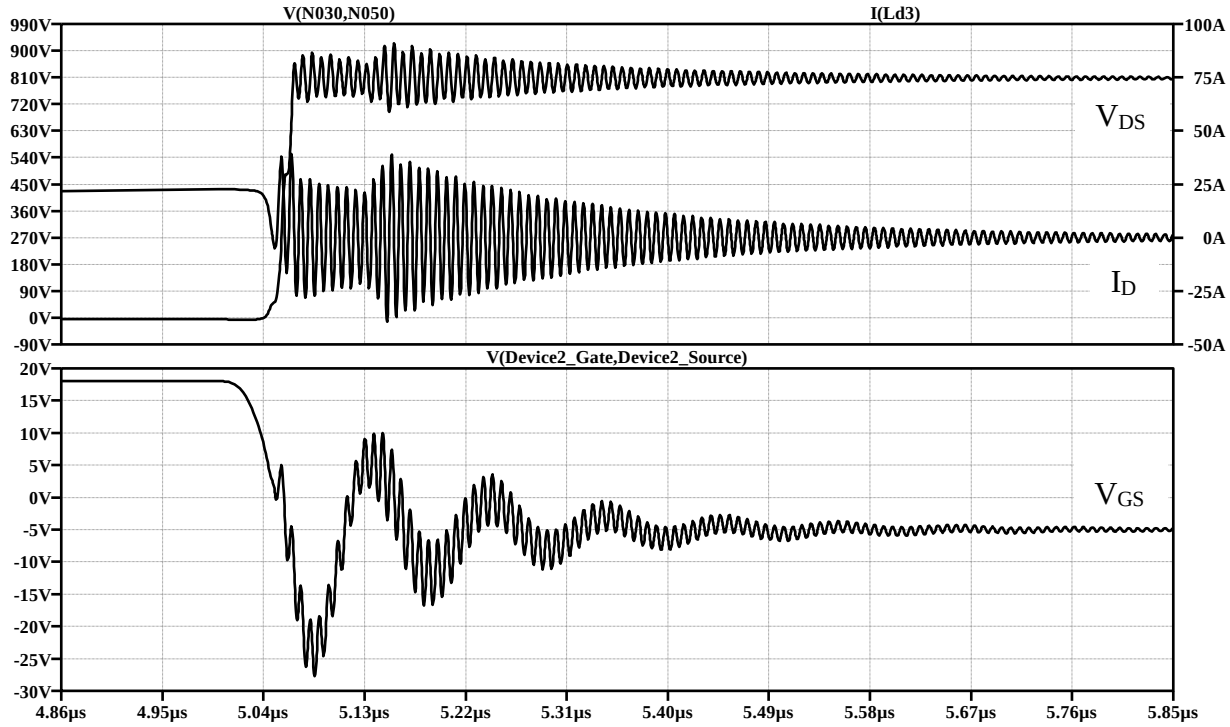

Figure 4. High-Frequency Oscillatory Gate Voltage during Turn-Off of SiC Power Module

would likely be destructive in a real-world test as the high-frequency oscillations cause parasitic turn-on and a brief shoot-through event. A greater understanding of the variables at play during this transition are necessary to reliably utilize the wide bandgap technology.

While manufacturers are currently able to produce SiC in six-inch-diameter wafers commercially with eight-inch-diameter wafers being demonstrated in development, it is still very difficult to obtain a silicon carbide wafer without defects [14]. To combat the defect density issues plaguing SiC materials, MOSFET manufacturers design relatively small chip areas when compared to silicon devices [11]. This process greatly increases the device yield from a SiC wafer and is extremely advantageous to decrease the high cost associated with SiC MOSFETs. Although a small chip area is beneficial to yield and to cost, it comes as a tradeoff for a higher on-state resistance and therefore a decreased current-carrying capability [14].

For the smaller area SiC MOSFETs to be used in high-power electronic systems, many devices must be operated in parallel to produce a single switch position. This practice is commonly carried out inside a power module where a single substrate and baseplate assembly can provide low-impedance connections between the MOSFETs. The downside of many paralleled devices in a single power package stems from the wafer variations of critical parameters such as transconductance and threshold voltage [15]. During a high-speed (large dv/dt or di/dt) event, any discrepancies in turn-on threshold can lead to one MOSFET turning on first and experiencing the full system current before its paralleled counterparts turn on [13] [16]. This can lead to premature device failure and negatively affect the reliability of the power module.

1.4 Proposed Solution

There are three planned components of the solution to the issues described in Section 1.3. The first includes the reduction of parasitic inductance on the gate and source connection PCB internal to the SiC power module. The second consists of transitioning from a single internal gate resistor per MOSFET in the power module to an impedance network comprised of a gate resistor, a source resistor and an optional gate-source capacitor per MOSFET. Finally, with the likely additional resistance necessary to combat the high-frequency oscillations, an active clamping circuit, also known as a Miller Clamp, will be added to each new impedance network of the MOSFETs' gate and source kelvin connections [13] [15] [17]. This theory is supported in literature as stated by Andrew Lemmon et al., "In the case that the reduction of switching speed is accomplished by increasing the value of the series gate resistance, this solution also increases the risk of Miller turn-on (and shoot-through in half-bridge circuits). Clearly, better techniques are needed to reduce the susceptibility of applications to self-sustained oscillation without

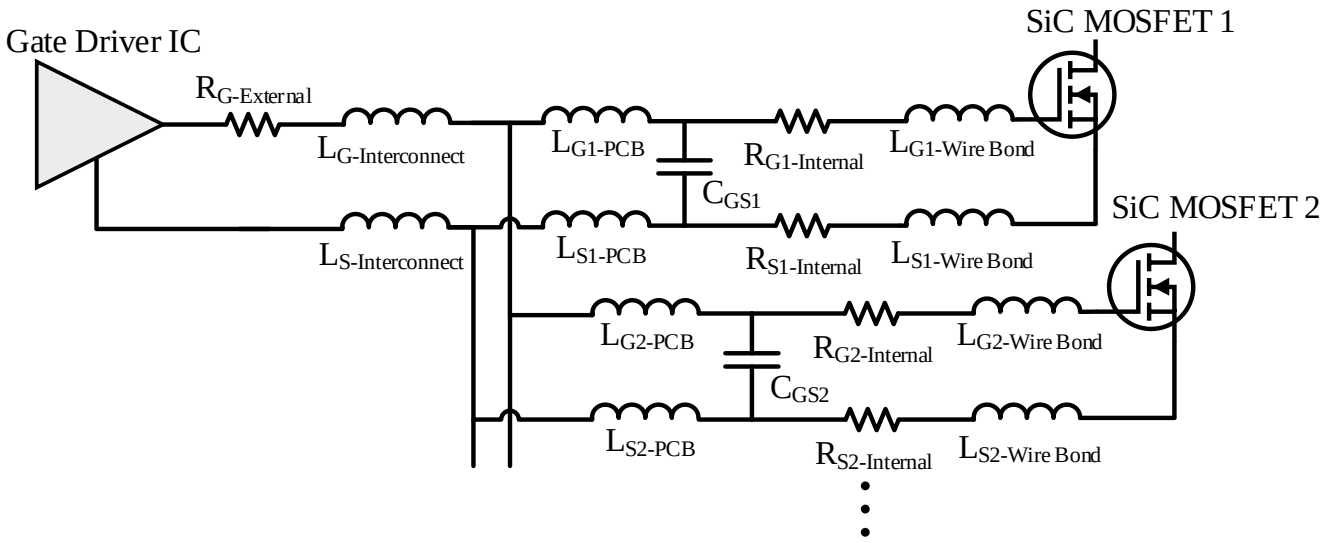

Figure 5. Gate Impedance Network Model with Parasitics and Tunable Components

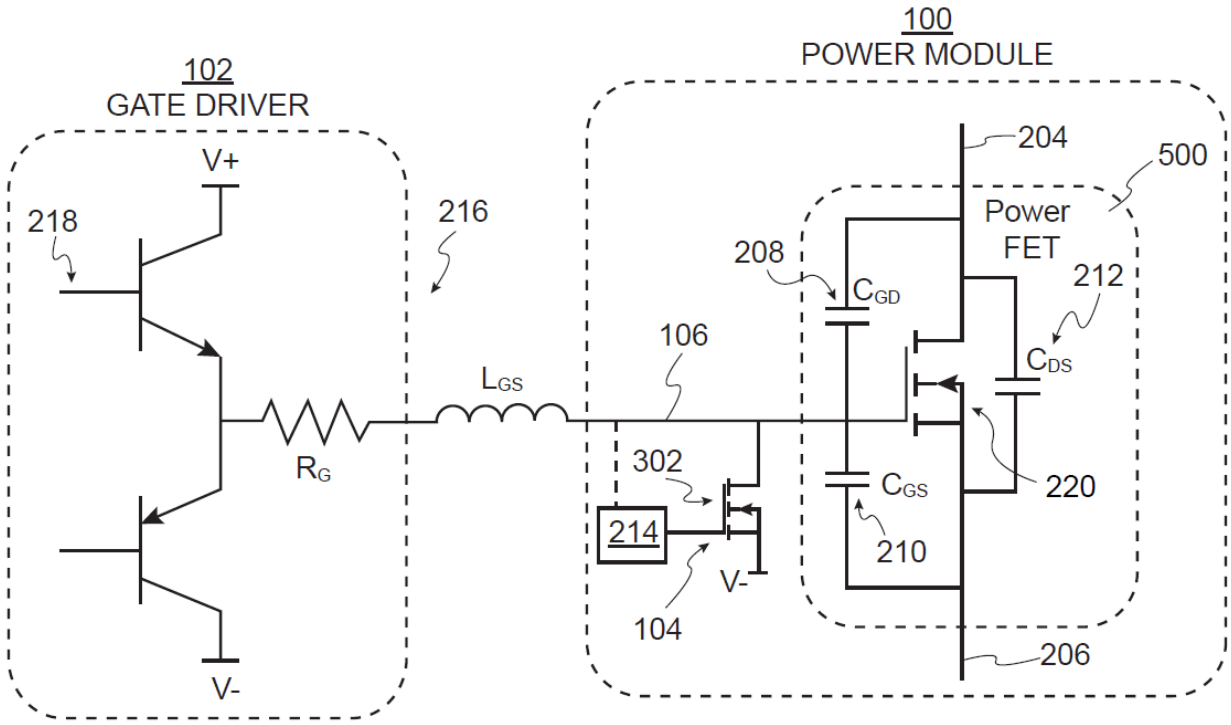

Figure 6. Simplified Circuit of Gate Driver and Power MOSFET with Clamping Device [18]

trading away the low-loss switching behavior that is one of the major attractions of WBG devices." [13] The proposed objectives for this thesis intend to provide solutions for these issues concerning the current state of wide bandgap technology.

The importance of a low inductance gate connection is well known in high-speed power electronics as stated by Sadik et al., "…when increasing the switching speeds, it was found that the gate oxide was exposed to voltages exceeding the recommended operation values. This could lead to reliability issues, particularly when high switching speeds are targeted. Moreover, a poorly designed gate-drive connection leading to high parasitic inductance in the gate loop can also be harmful for the device immunity." [15] It is critical to guarantee that all of the MOSFETs in a power package maintain a safe operating gate voltage. The lumped-element, parasitic model and associated simulations will provide clarity into this matter.

Figure 5 illustrates the proposed shift from a single gate resistor per MOSFET internal to the SiC power module to individual gate impedance networks optimized for high reliability, maximum switching speed, and simple drive requirements. Figure 6 displays the active clamping circuit that will be utilized as an integral part of the gate and source impedance network. The clamping circuit will directly connect the gate of the MOSFET to the kelvin source connection; therefore, any gate or source resistors used in the network are bypassed, and a very-low-impedance path is created [3] [18]. The clamping circuit also has the ability to hold the gate to a known negative potential again bypassing any gate or source resistors in the network [18]. Both revisions of the gate and source connection PCB are proposed to be investigated during this effort.

1.5 Objectives of Thesis

The chief objective of this thesis is to investigate the gate network parasitics of a silicon carbide power module, the CAS325M12HM2, featuring a large quantity of paralleled SiC MOSFETs in

order to increase performance, to eliminate instabilities, and to simplify the gate drive requirements. This objective will be achieved through the following process:

1) Accurately model the parasitics in the gate and source connection network of a high-performance SiC MOSFET power module.
2) Develop a method for acquiring properly sized gate resistor, source resistor, and gate-source capacitor values to compensate the network.
3) Advance the technology described in the author's patent filing, [18], by expanding the use of the Miller Clamping device to each MOSFET inside the SiC power module.
4) Validate the gate impedance network performance and reliability improvements via simulation results in a clamped inductive load test setup.

1.6 Organization of Thesis

This thesis will be comprised of six chapters starting with an introduction and theoretical background in Chapter 1. The lumped-element, parasitic model of the gate network in a state-of-the-art SiC power module will be obtained through theoretical calculations, physics simulations, and laboratory measurements in Chapter 2. In Chapter 3, the lumped-element model will be used to conduct circuit simulations to determine oscillation-eliminating gate resistance values in the power module. Chapter 4 will investigate the effects of parameter variances in SiC MOSFETs on switching performance. Three topologies of Miller Clamp circuits will be investigated and assessed in Chapter 5. Chapter 6 will contain the conclusions and discussions of future work.

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CHAPTER 2

PARASITIC ELEMENTS OF THE GATE NETWORK

This chapter presents the procurement of the parasitic elements in the gate-source network of a high-performance SiC power module. The three elements consist of finite material resistance, gate-source capacitance, as well as mutual and self-inductance. Each of the three parasitics are crucial for obtaining an accurate model of the gate-source network for the power module; therefore, three methods of obtaining the values are discussed in this chapter. The methods include theoretical calculations, simulations using the computer software COMSOL, and physical measurements of the circuit in a laboratory. Furthermore, the gate-source network is separated into three distinct sections: the first consists of the gate driver connector, the second is made up of the parallel planes inside the gate-source PCB, and the third comprises of the gate wirebond as well as the kelvin source wirebond. The values obtained in this chapter are used extensively in the simulations portrayed in the following chapter.

2.1 Gate Driver to PCB Interconnects

The first section is comprised of the gate driver to gate-source PCB interconnect. Cree's CAS325M12HM2 features two Samtec connectors, which deliver the gate signals down to the PCB inside the power module. These connectors are composed of ten, vertical, 10 μm flash-gold, aluminum pins. The square pins are 0.51 mm on each side with 2 mm spacing. Five of the pins are designated for the gate connection while the other five pins are designated for the kelvin source connection. Figure 7 indicates the area of interest for this section.

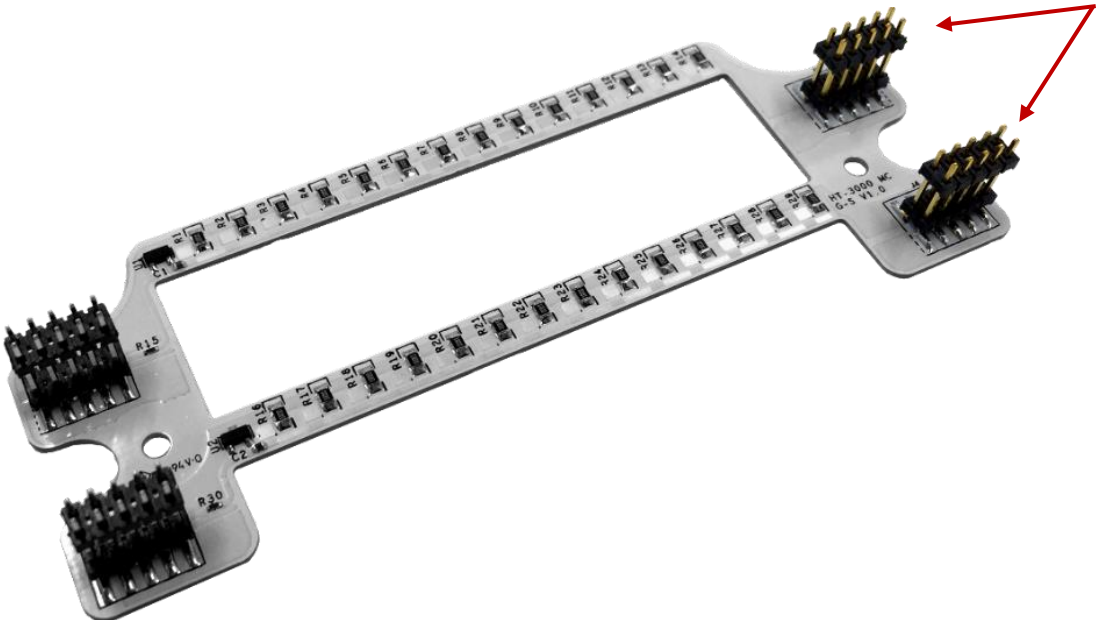

Figure 7. Gate Driver to PCB Interconnect

2.1.1 *Calculations*

To calculate the overall parasitic inductance of the gate-source connector, two phenomena must be considered: the self-inductance of each pin and the mutual-inductance between the adjacent pins. The first component of the inductance, the self-inductance is identical between the ten pins of the connector. The equation governing the self-inductance of a wire with length l and radius r is given by the equation below [1]. The length and radius are in millimeters while the resulting inductance is in nanohenries.

$$L_s = 0.2\left[l \ln \frac{l + \sqrt{l^2 + r^2}}{r} - \sqrt{l^2 + r^2} + \frac{l}{4} + r\right] \text{(nH)} \tag{2.1}$$

The length of each pin is approximately 11.86 mm. The pins have a square cross-section; therefore, a worst-case radius running from the center of the square to the center of one of the sides is used. This provides a radius of 0.255 mm. Using equation 2.1 to calculate the self-inductance

of a single pin, the value is found to be 9.02 nH. This result is assumed to be valid based on the common assumption of approximately 1 nH/mm for wires of this size [2].

The self-inductance of the connector is only a part of the actual inductance seen by the gate driver. The remaining piece, the mutual-inductance, commonly works in favor of the system impedance by providing a cancellation of a portion of the self-inductance. Two parallel conductors with currents flowing in opposite directions exhibit a negative mutual-inductance dependent on two parameters of the conductors: their length and their separation distance [2]. Conversely, if two parallel conductors have currents flowing in the same direction, they exhibit a positive mutual-inductance. These two effects are precisely what occurs in the gate driver connector. The polarity of the mutual-inductance determines if the overall inductance of the element will increase or decrease. This effect is easily visualized in Figure 8 where half of the conductors carry current from the gate driver to the power module (×) while the other five pins carry current from the power module back to the gate driver (·). Therefore, to determine the total mutual-inductance of a single pin, every other conductor's effect on the pin in question must be considered.

For example, consider the bottom-left (BL) pin of the gate-source connector shown in Figure 8. The other nine pins contribute a unique amount of either positive or negative mutual-inductance, which sum to attain the total mutual-inductance. The other four bottom-row pins contribute positive mutual-inductance while the five top pins contribute negative mutual-inductance. Equation 2.2 narrates this process.

$$M_{BL} = M(d_6) + M(d_7) + M(d_8) + M(d_9) - \left(M(d_1) + M(d_2) + M(d_3) + M(d_4) + M(d_5)\right) \tag{2.2}$$

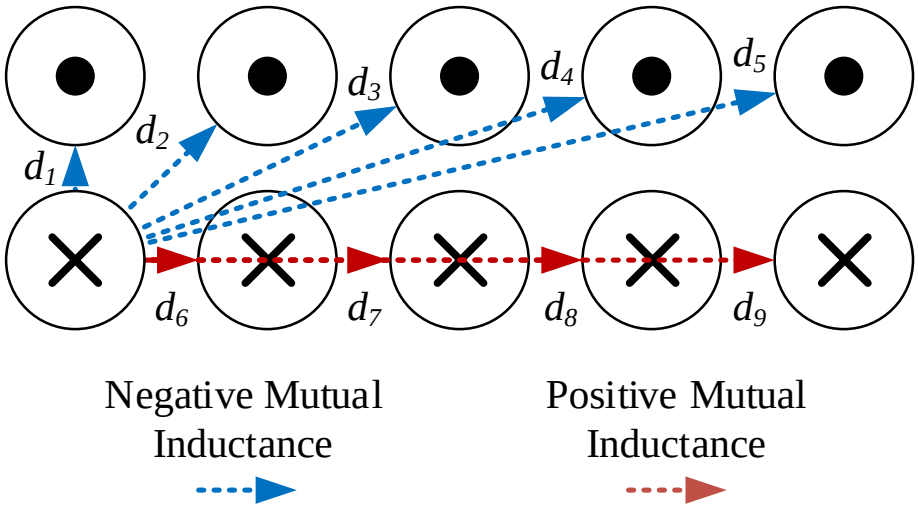

Figure 8. Cross-Section of Gate-Source Connector Portraying Mutual-Inductance

The mutual-inductance of each pin is modeled with Equation 2.3 where l is the length of a pin in millimeters and d is the distance between the two pins in question also in millimeters [1].

$$M(d_n) = 0.2\left[l \ln \frac{l + \sqrt{l^2 + {d_n}^2}}{d_n} - \sqrt{l^2 + {d_n}^2} + d_n\right] \text{(nH)} \tag{2.3}$$

The distance between each pin is calculated simply with the Pythagorean theorem as the pins are aligned in a 2 mm by 2 mm grid. Using the acquired distances shown in Table 2 as well as a pin length of 11.86 mm, each pin's mutual-inductance contribution is calculated and the results are displayed in Table 2 for the bottom-left conductor. Each of the components are summed to find the total mutual-inductance that the bottom-left pin experiences with Equation 2.2. As each pin is affected by five anti-parallel conductors and only four parallel conductors, the overall mutual-inductance of any pin is negative. This leads to a decrease in the total amount of inductance that the gate-source connector exhibits.

Table 1. Distance between Conductors with Corresponding Mutual-Inductance

Distance (mm)		Mutual-Inductance (nH)	
d_1	2	M_1 (-)	3.878
d_2	$2\sqrt{2}$	M_2 (-)	3.204
d_3	$2\sqrt{5}$	M_3 (-)	2.397
d_4	$2\sqrt{10}$	M_4 (-)	1.865
d_5	$2\sqrt{17}$	M_5 (-)	1.512
d_6	2	M_6 (+)	3.878
d_7	4	M_7 (+)	2.584
d_8	6	M_8 (+)	1.941
d_9	8	M_9 (+)	1.550

The final step for calculating the total inductance of the conductor consists of combining the mutual-inductance and the self-inductance of each pin, simplifying each side of the conductor into a single inductance by considering the five paralleled conductors, and ultimately summing the two inductances from each side of the connector. The first step is displayed in Table 2 where the self-inductance of each pin is summed with its mutual-inductance component to give way to the effective inductance of each pin. Pins in the same column exhibit an equal mutual-inductance component and have an equal effective inductance; therefore, the outcome for only the bottom row of pins is shown.

$$L_{Row} = \left[\sum_{x=1}^{5} \frac{1}{L_{eff}(x)} \right]^{-1} \tag{2.4}$$

The effective inductances of each pin are then paralleled with the simple calculation of paralleled inductors as shown in Equation 2.4. Using this equation, the inductance of one row of five pins is 1.301 nH. Considering the other row of five pins, the total calculated inductance of the gate-source connector is 2.602 nH.

2.1.2 *Measurement*

The inductance calculation obtained in the previous section must be validated through measurement to ensure that it is an acceptable value to create an accurate gate network model. In order to measure such a miniscule inductance value, extremely precise equipment must be utilized. The equipment chosen for this procedure is Agilent's E4980A 1 MHz precision LCR meter. Per the user manual, the absolute measurement accuracy in the 1 nH – 10 nH range is between 1% and 10% at a measurement frequency of 1 MHz. This is the highest operating frequency of this precision LCR meter, and it is the frequency at which all the measurements are obtained. When measuring inductances in the few-nanohenry range, it is impossible to obtain accurate results with the standard 4-wire alligator-clip probes. The small movements of the wires during open and short calibration nullify the corrections and generate nonsensical results. To attain meaningful results from this equipment, an inductance measurement fixture must be designed. This fixture keeps the coaxial wires and device under test (DUT) in the same position during each calibration as well as during the actual measurement, which ensures the most accurate results.

Table 2. Self-Inductance, Mutual-Inductance, and Total Pin Inductance

Pin Number *(x)*	L_s (nH)	M_x (nH)	$L_{eff\text{-}x}$ (nH)
1 (Bottom-Left)	7.4296	-2.9041	4.5255
2 (Bottom-LC)	7.4296	-2.2689	5.1606
3 (Bottom-Center)	7.4296	-2.1583	5.2713
4 (Bottom-RC)	7.4296	-2.2689	5.1606
5 (Bottom-Right)	7.4296	-2.9041	4.5255

The four measurement signals required by the LCR meter include two force connections and two kelvin connections. This is a common 4-wire technique designed to eliminate error from the measurement of the wires connecting the device under test. A relatively large current can flow through the force connections during the test; furthermore, this current induces a voltage drop across the finite resistance of the conductors. Using the 4-wire technique, this voltage drop is not included in the inductance measurement as the true measurement is performed at the terminals of the DUT through the other two conductors. This is commonly known as a kelvin connection.

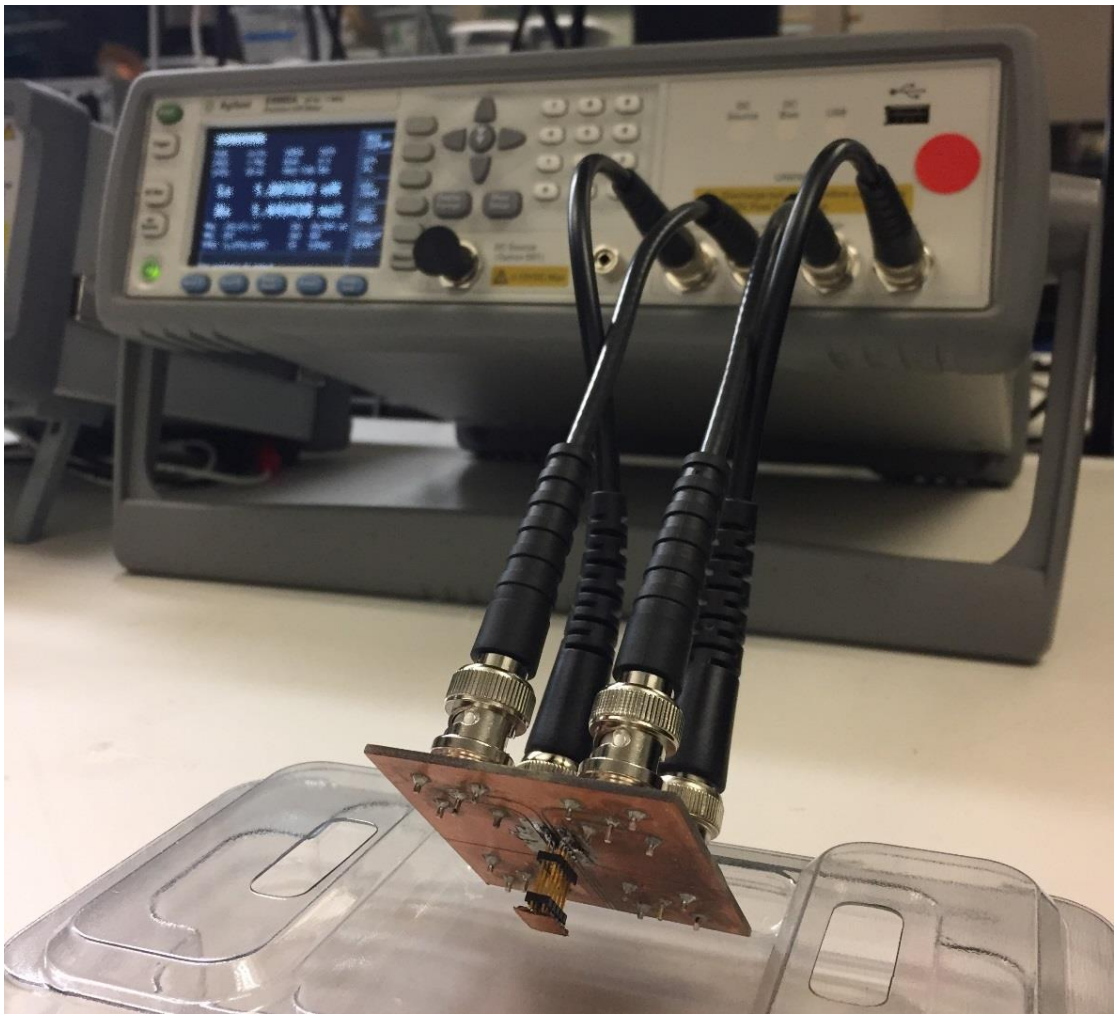

Figure 9. Inductance Measurement Fixture and Agilent's Precision LCR Meter

Another requirement of the inductance measurement test fixture is an easily accessible method to calibrate the LCR meter. Calibration is performed via an open measurement followed by a short measurement across the location of the DUT. Following the calibration procedure, the test fixture is prepared to accurately measure the gate-source connector. Finally, the feet of the connector are soldered onto the test fixture in the same area where the short measurement is conducted. The connector is open at the top and therefore must be linked to complete the current loop. As seen in Figure 9, a small piece of copper is used to connect the two rows of pins on the open end of the connector. As soon as the measurement loop is closed, the inductance and series resistance values are displayed for the test condition of 1 MHz and 20 mA of force current. The values obtained from this measurement are 2.097250 nH and 1.847527 mΩ. The percent error between the calculated value and the measured value is 19.4%, which is obtained using Equation 2.5.

$$Error\ \% = \left[\frac{L_{measured} - L_{calculated}}{L_{calculated}}\right] \times 100 \tag{2.5}$$

While the error percentage is rather high, the measured value is only 0.69 nH from the theoretical calculations. This level of accuracy is acceptable when considering the extremely low values of inductance provided by this piece of the system. When taking into account the larger parasitic inductances of the system, this small discrepancy between measured and calculated values is considered in the noise floor. In the next section, a physics-based simulation provides another take on the parasitic inductance of the gate-source connector.

2.1.3 *COMSOL Simulations*

To determine whether the calculation or the measured value of parasitic inductance is more accurate, a third method, COMSOL Multiphysics Simulator, is used. COMSOL is a powerful multi-physics solver capable of modeling electromagnetics, structural mechanics, fluid and heat transfer, as well as chemical reactions. For this investigation, an electromagnetic physics solver is utilized focusing on magnetic and electric fields, which allows for parasitic inductance, capacitance, and resistance extraction of a 3D CAD model.

The first step of the simulation procedure comprises generating a model optimized for use with COMSOL. A Solidworks model is provided by Samtec, the manufacturer of the gate source connector, but the model contains unnecessary information that greatly lengthens the time required to simulate the connector. Only the required information pertinent to the inductance measurement needs to be included in the model. For this reason, the plastic, structural pieces are removed from

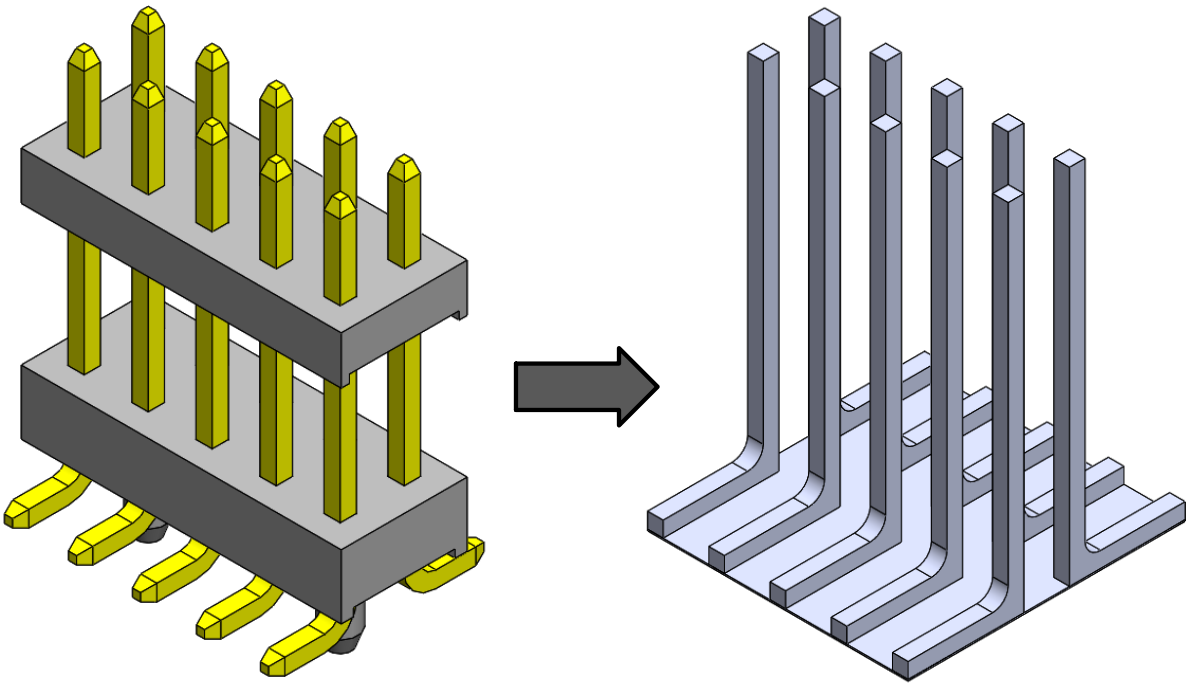

Figure 10. Manufacturer's 3D Model vs. 3D Model Optimized for COMSOL

the model as well as the chamfered ends of the pins. Figure 10 illustrates the manufacturer's model of the connector and the modified model that is simulated in COMSOL. Additionally, the simulation requires a closed path for the current to flow just as described during the measurement process. For this reason, a flat plane is added to the model to create a path for current to flow from the bottom of one side of the pins to the bottom of the other set of pins. The plane is displayed in Figure 10.

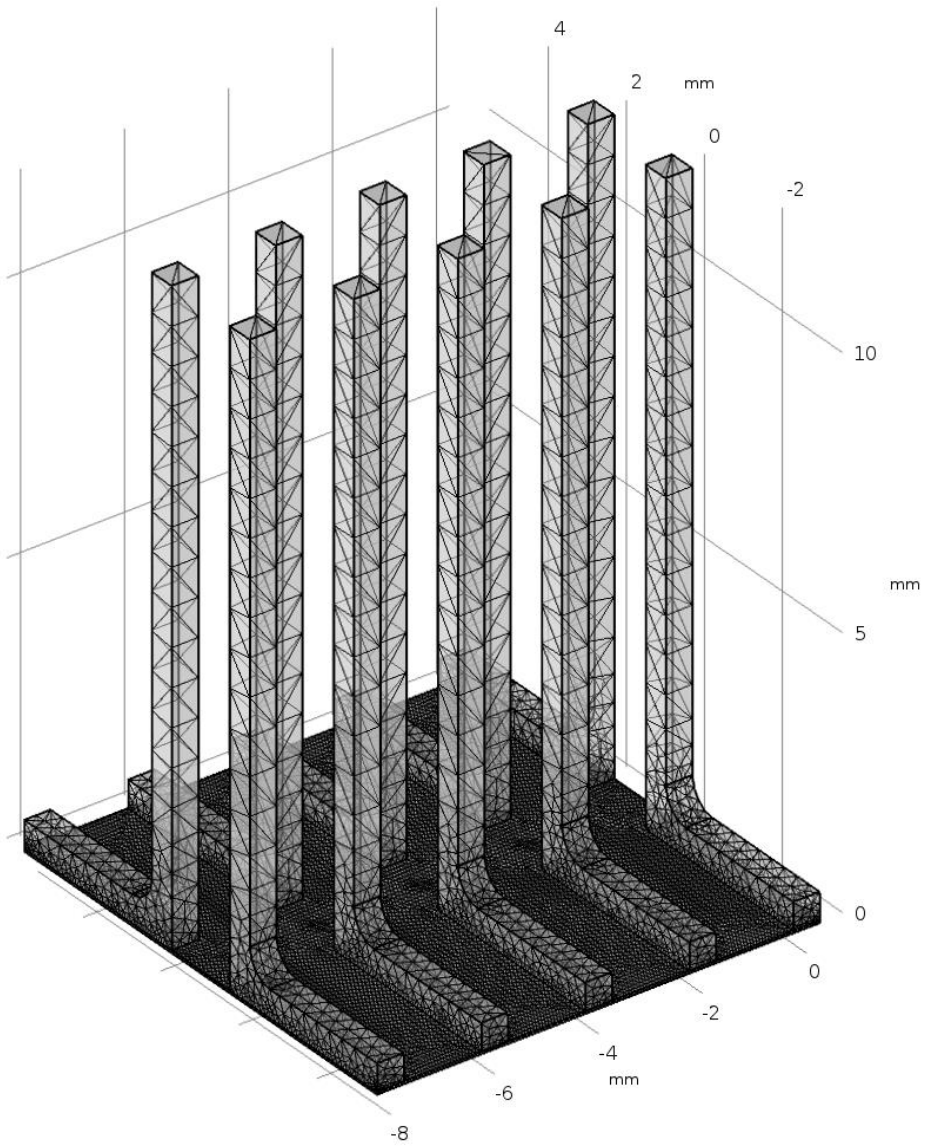

Figure 11. Constructed Mesh of Gate Source Connector

Next, the model must be meshed into an array of much smaller shapes, which are used by the physics solver to obtain a solution for the system. In COMSOL, meshing the 3D model is the most important step to creating an accurate and efficient model to simulate. If the mesh elements are too small, the solver will take an extremely long time to solve the system or the solver may never converge; however, if the mesh elements are too large, the result of the simulation may be inaccurate. The constructed mesh for the gate source connector is shown in Figure 11. Areas that are very thin such as the bottom copper plane have a very fine mesh while the larger pins have a coarser mesh. This mesh is created with COMSOL's automatic mesh settings set to fine, which yielded very good results. As this is a relatively simple model, the solver takes less than an hour to achieve a numerical solution with a 0.001 rated accuracy.

After the model has been meshed appropriately, the material of the domains must be selected, a ground and source boundary must be defined, and a stationary or frequency solver must be selected. The materials used for this simulation are copper for the rows of pins and the bottom plane while the remaining domains are set to air with both materials optimized for electromagnetic simulation. The ground boundary is defined as the top faces of five of the pins in one row while the source terminal is defined as the top faces of the other five pins. The source terminal is defined as a current source and is set to 1 A. Finally, a frequency domain solution is required to obtain the inductance; therefore, the solver is set to the frequency domain with a value of 1 MHz in order to match the point at which the measurements are obtained, and the simulation setup is complete.

After the solution converges and a result is obtained, COMSOL offers a myriad of visual aids to effectively portray the data. As seen in Figure 12, the surface of the connector contains the current density data in A/mm while the arrow-surface on a cut-plane in the air domain portrays the

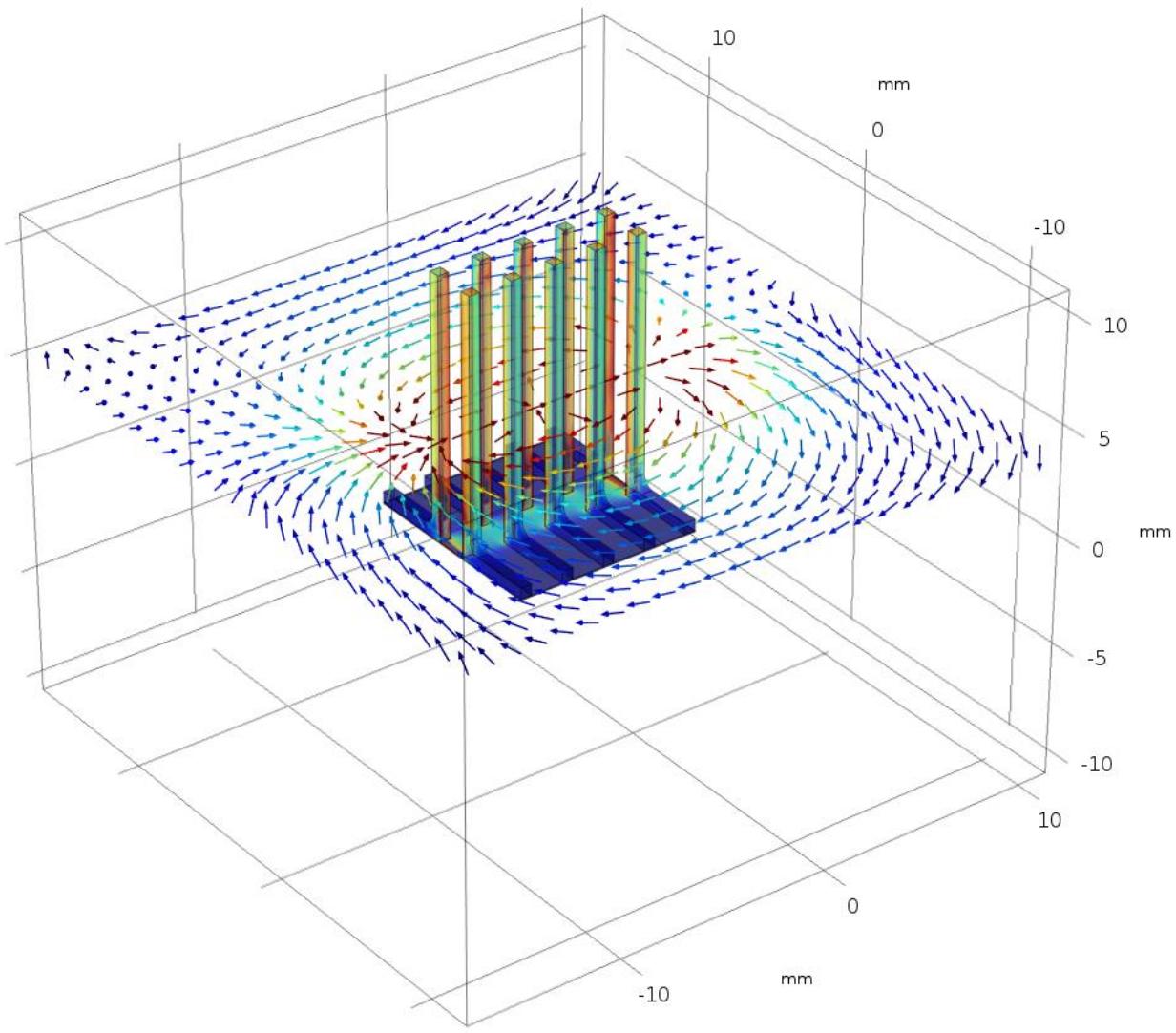

Figure 12. Magnetic Flux Density and Current Density of Gate Source Connector

magnetic flux density (μT). These results are helpful for visualizing the current flow and magnetic fields in the simulation. If the current or field does not appear as expected, the model should be re-meshed and solved again. Finally, a global expression is defined to find the parasitic inductance and resistance. The values obtained from this simulation are 2.6114 nH and 1.3840 mΩ, which match very closely to the calculated value. The percent error between the calculated value and the simulated value is 0.35% as per Equation 2.5.

2.2 Gate & Kelvin-Source PCB

The largest contributor to the parasitic inductance of the gate-source network is the printed circuit board (PCB). This section is the physically largest portion of the system and offers the most area for improvement between the existing design and one optimized for low-inductance routing. The current layout is composed of a single-layer containing multiple copper planes. One plane makes up the gate net, another creates the kelvin source net, and the remaining shapes create the wirebond locations for each MOSFET as displayed in Figure 13. As these planes are all on a single copper layer, they exhibit little benefit from flux cancelation in the form of mutual-inductance. As in the previous section, the three methods of parasitic extraction: calculation, measurement, and simulation are described in the following sections.

2.2.1 *Calculations*

To apply standard inductance calculations to the planes of the PCB, small modifications of the shapes must be made to allow the equations to apply. Instead of the 45° corners and angled sections of the planes, a rectangular approximation is created to allow Equation 2.6 to be applied. The rectangular approximations for the shapes are shown in Figure 13, and each rectangle is labeled as either G for gate net or S for source net with an A, B, or C identifier.

As with the gate-source connector, the first element to calculate is the self-inductance and is governed by the straight rectangular trace inductance approximation shown in Equation 2.6 [3].

$$L = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+h}\right) + \frac{w+h}{3l} + 0.50049\right] \text{(H)} \tag{2.6}$$

Assuming a fixed height or copper thickness of 0.017526 mm, the remaining width and length for each rectangle are measured in Allegro PCB and are displayed in Table 3. Using these measurements, the self-inductance of each rectangle can be calculated. These values are also

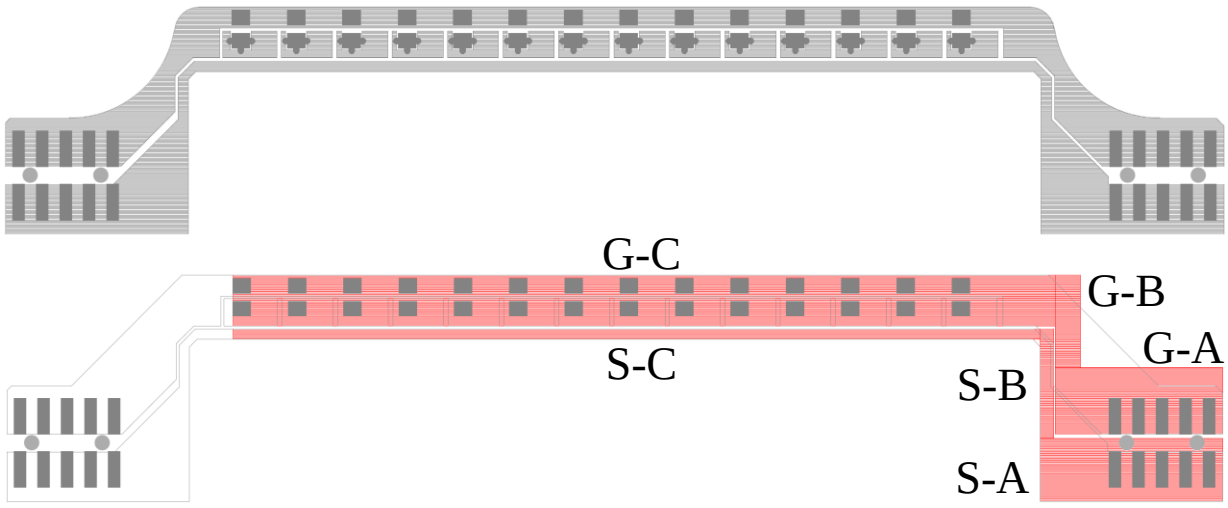

Figure 13. Gate Kelvin PCB Layout (Top) and Estimated Area for Calculations (Bottom)

included in Table 3. As expected, the planes create a large amount of parasitic inductance with the total self-inductance calculated as 155.519 nH. As the geometry of the copper was approximated for ease of calculation, there is likely to be a higher error percentage between the calculated and the measured or simulated values. Next, the mutual-inductance is calculated to close this section.

Table 3. Self-Inductance Calculation of Gate Kelvin PCB

Segment	Width (mm)	Length (mm)	Height (mm)	Inductance (nH)
G-A	5.594	14.224	0.017526	6.416
G-B	2.159	7.868	0.017526	4.046
G-C	4.318	69.850	0.017526	55.794
S-A	5.334	15.494	0.017526	7.350
S-B	1.143	9.271	0.017526	6.144
S-C	0.889	68.580	0.017526	75.770
Total				**155.519**

The mutual-inductance between two equal parallel conductors can be calculated with Equation 2.7 [3]. This calculation is appropriate for this application because the two shapes have an equal amount of separation for their entire length.

$$M = \pm\frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{s}+\sqrt{1+\frac{l^2}{s^2}}\right)-\sqrt{1+\frac{s^2}{l^2}}+\frac{s}{l}\right] \text{(H)} \tag{2.7}$$

There are only two variables necessary for the mutual-inductance calculation: conductor separation, *s*, and the length of the conductors, *l*. The separation is a constant 10 mils between the shapes, which is equal to 0.254 mm. The length is total sum of the G rectangles and is 93.218 mm. Applying Equation 2.7 produces a mutual-inductance value of -104.4 nH, which is a substantial portion of the self-inductance. Finally, summing the individual components of the total inductance, the self-inductance of 155.519 nH and the mutual-inductance of -104.427 nH, a value of 51.092 nH is obtained. When compared to the 2.6 nH provided by the input connector from the first section, the PCB delivers significantly more parasitic inductance to the system. The next subsection compares the theoretical calculations to the measured values.

2.2.2 *Measurements*

The DUT in this section is the printed circuit board, but to obtain the inductance measurement from the PCB, the connector from the first section is needed for connection to the fixture. After the measurement is complete, the inductance of the connector is subtracted from the measurement to compare directly with the theoretical calculation value. Like the procedure in the previous measurement section, the custom, inductance extraction fixture is used to calibrate the LCR meter with an open measurement and a short measurement. After fixture compensation, the DUT is prepared by soldering a piece of copper across the farthest wirebond pads in order to complete the

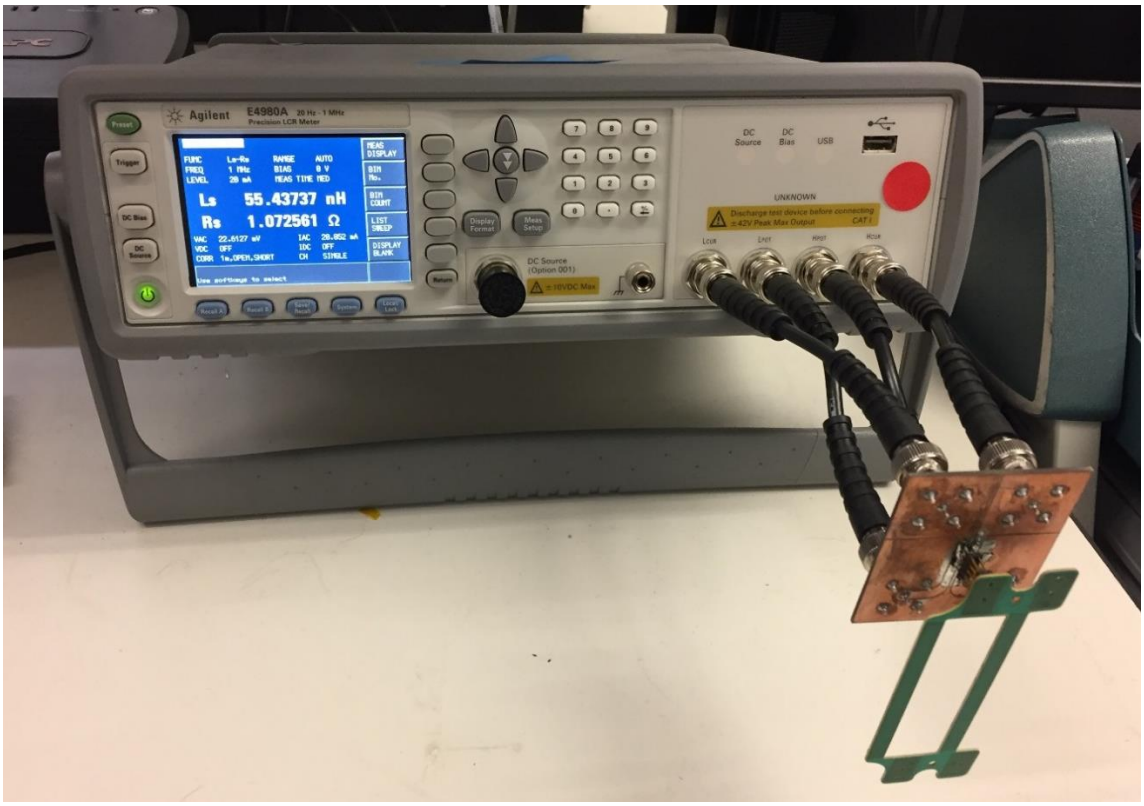

Figure 14. Gate Kelvin PCB Mounted on Substrate Assembly

loop. The PCB is soldered to the bottom of the gate-source connector and the fixture is connected to the LCR meter and can be seen in Figure 14. Also shown in Figure 14, the inductance measurement is 55.437 nH for the gate-source connector and the PCB. To ensure accurate results, an additional parasitic extraction tool is utilized to verify the results from the Agilent LCR meter. Keysight's E4990A impedance analyzer provided the second measurement, and at 1 MHz, the value of 54.161 nH is obtained. To directly compare the acquired measurement value to the calculations, the measured gate-source connector value must be subtracted from the total measurement value.

$$\frac{55.437\ \text{nH} + 54.161\ \text{nH}}{2} - 1.903\ \text{nH} = 52.896\ \text{nH} \tag{2.8}$$

As shown in Equation 2.8, the two measured values are averaged, and the gate connector inductance is subtracted to find the total inductance of 52.896 nH for the PCB. When compared to the calculated value, of 51.092 nH, the difference is only 1.80 nH and the error percentage is 3.4%. The small amount of error between the two methods of parasitic extraction reassure the methods in this investigation; moreover; in the next section, the COMSOL simulations provides another take on the parasitics of the gate-source PCB.

2.2.3 *COMSOL Simulations*

Following a similar procedure to the connector simulation, the first step of modeling the PCB in COMSOL is to create a 3D model optimized for simulation. The process includes removing any unnecessary information such as plastic mechanical features or floating conductive elements that

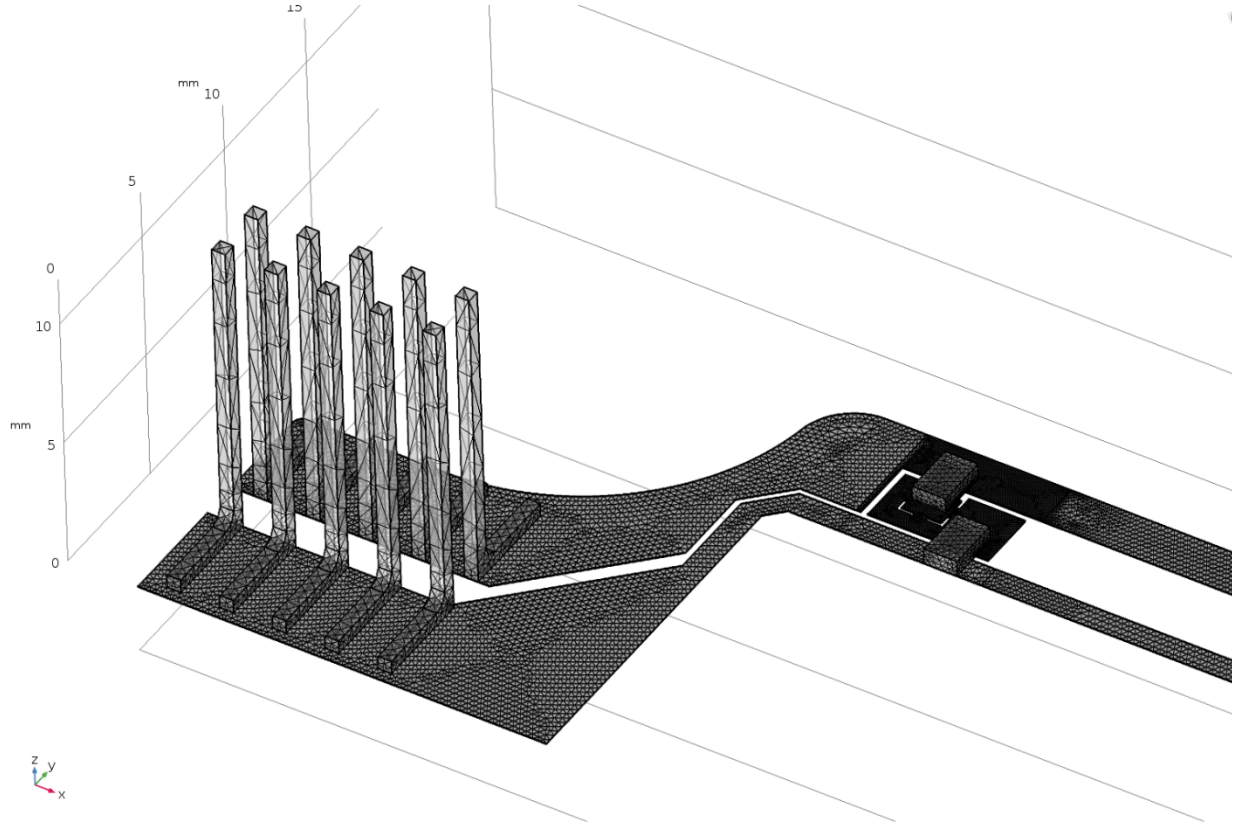

Figure 15. Mesh Construct for Solving COMSOL Electromagnetic Simulation of PCB

will render the system unsolvable. Using the layout software, Allegro PCB, a DXF file is generated, which contains the exact dimensions of the copper traces of the PCB. This file is easily imported into Solidworks as a sketch and is extruded to the correct copper thickness of 1 oz. or 0.0014 inches. A rectangle equivalent to the size of an 0805-resistor is drawn and extruded to the correct height and added to the model in place of the gate resistor. For this model, the gate source connector is added as well to complete the basic 3D CAD model.

There are as many as fourteen MOSFETs in parallel in the HT-3000 power module under investigation. It is necessary to determine the inductance to each position to create an accurate parasitic model for circuit simulation. For this reason, the simulation begins with the first position inside the module as shown in Figure 15. The 0805-resistor part created previously is re-used to close the current loop at the first MOSFET position, which is closest to the input connector. The last element necessary to simulate the model using COMSOL is an appropriately sized air domain. For this model, two air domains are used to increase the accuracy of the simulation while decreasing the required simulation time. A small air domain is created around the elements that exhibit fine features such as the resistor pad with thermal relief connections while a larger air domain surrounds the entire 3D model.

Next, the generated 3D model is meshed with a procedure enhanced for large, thin planes such as copper traces in a PCB. Each face of the model is meshed independently with a free-triangular mesh set to an appropriately selected element minimum and maximum dimension size; in particular, the domains with tight spacing require mesh element dimensions with a much smaller minimum size than the larger domains. After the top faces of the PCB have been completed, the meshes are copied to their equivalent bottom-side face. Finally, the two corresponding meshed faces of the PCB are swept together and distributed into three-dimensional shapes for simulation.

After the PCB has been successfully meshed, the small air domain is meshed with a free-tetrahedral mesh algorithm with dimension size set to extremely fine and the large air domain is meshed with dimension size set to normal. The meshed model, which is shown in Figure 15 is now ready for electromagnetic simulation.

The simulation takes several hours to converge to the set relative tolerance of 0.001. After the simulation is complete, the parasitic inductance is determined by adding a global evaluation expression comprising of the imaginary component of the impedance divided by the angular frequency. For the first position, an inductance of 19.696 nH was obtained. This procedure is repeated for the final MOSFET position to compare to the simulated inductance to the calculated and measured values to determine if the simulation method is accurate. Starting from the 3D CAD model in Solidworks, the small air domain, the resistors, and the wirebond pads are moved to the

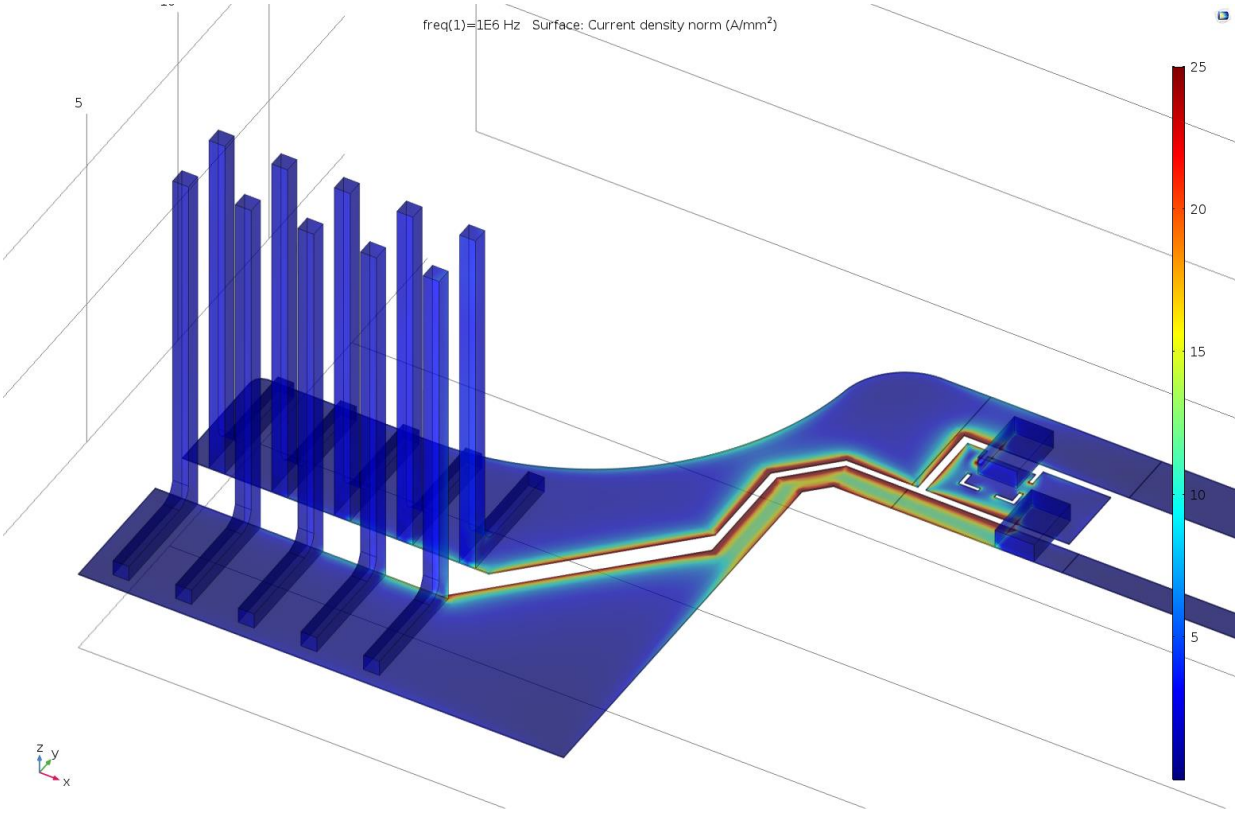

Figure 16. Current Density of First Position Shorted at Wirebond Pads

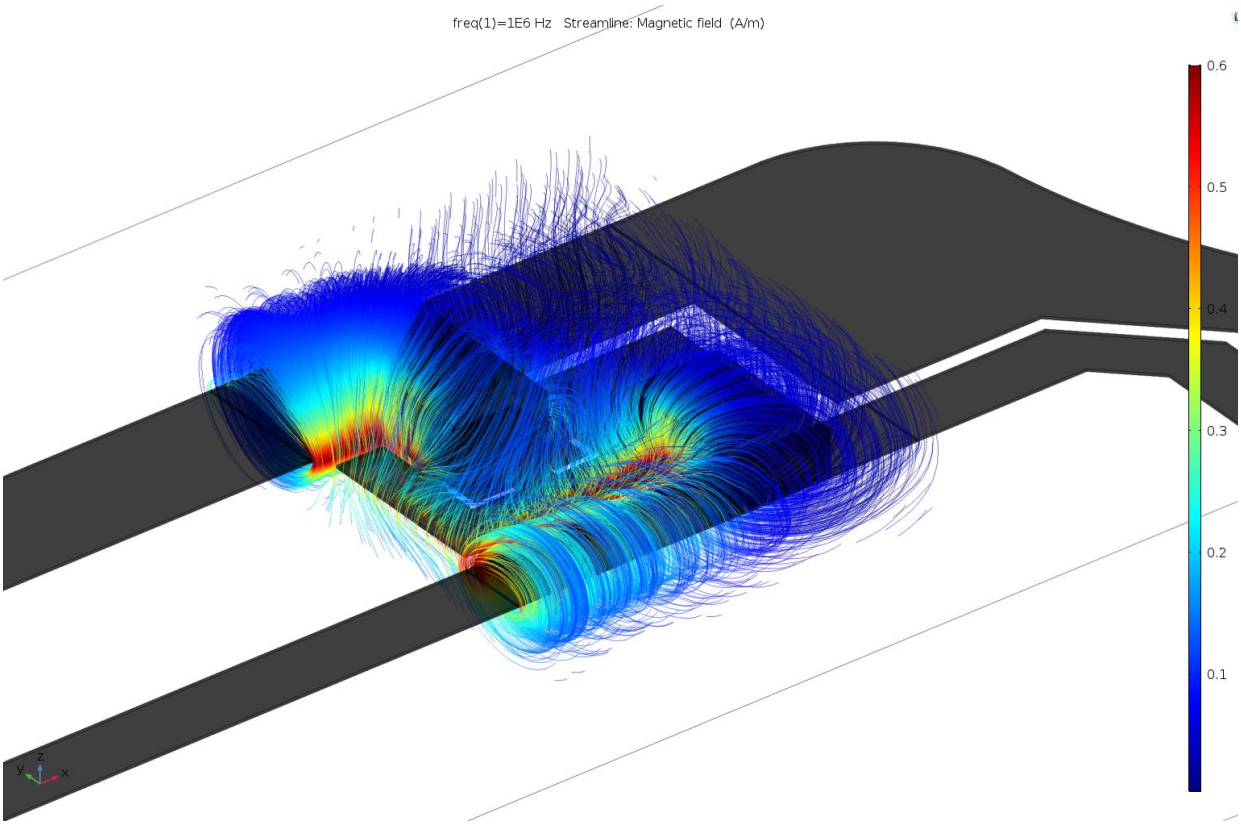

Figure 17. Magnetic Field (A/m) Surrounding Wirebond Pads and Shorting Resistor

last position on the gate-source PCB. The mesh parameters are updated with the correct boundaries and domains, and the simulation is conducted. The results of the simulation for the final position indicate that the inductance is 52.976 nH. These results match the measured values very well with an error percentage of 0.15%. The simulation method is verified as an effective parasitic extraction technique again through this experiment. Additionally, COMSOL is an extremely valuable visualization tool as illustrated in Figure 17, which portrays the magnetic field around the resistor and wirebond pads of the model. The streamline tool is used to visualize the field, and a rainbow color chart is applied to show the magnitude of the field.

2.3 Gate & Kelvin Source Wire Bonds

In stark contrast with the previous section, the wirebond is a much smaller contributor of parasitic inductance to the gate network. That being stated, due to the long and narrow geometry of the wirebond, and because there are two wirebonds per MOSFET, the parasitic inductance is non-negligible. The major variable governing the inductance of the wirebond is the length, which varies widely between the different switch positions. For this reason, it is difficult to achieve a low error percentage between the measured and calculated values while the simulated value matches the measured results closely. As in the previous two sections, the three methods of parasitic extraction: calculation, measurement, and simulation are described in the following sections.

2.3.1 *Calculations*

Two methods for calculating the inductance of a wirebond will be evaluated in this section. The first, the straight wire inductance approximation, is simply governed by the length and the radius of the wire. For this case, the wire is a 5 mil wirebond, which has a radius of 0.0635 mm. For both methods of calculating inductance, the length will be swept from 5 mm to 50 mm in 5 mm increments. The equation governing the straight wire inductance approximation is shown below in Equation 2.9 [3]. The results of this method are displayed in Table 5 on the next page.

$$L = \frac{\mu_0}{2\pi} \times l \left[\ln\left(\frac{l}{r} + \sqrt{1 + \frac{l^2}{r^2}} \right) - \sqrt{1 + \frac{r^2}{l^2}} + \frac{r}{l} + \frac{1}{4} \right] \text{(H)} \tag{2.9}$$

For the next method, Kazimierczuk in *High-Frequency Magnetic Components*, has approximated the inductance of a wirebond with Equation 2.10. Again, the equation's parameters are wirebond radius and length, but the equation is far simpler than the straight wire approximation. As

Table 4. Self-Inductance Calculation of Wirebonds of Varying Length

Length (mm)	Radius (mm)	Straight Wire Inductance (nH)	Wirebond Approximation Inductance (nH)	Error Percentage
1	0.0635	0.55	0.54	2.26
2	0.0635	1.37	1.36	0.92
3	0.0635	2.29	2.28	0.55
4	0.0635	3.28	3.27	0.39
5	0.0635	4.32	4.31	0.29
10	0.0635	10.02	10.00	0.13
15	0.0635	16.24	16.22	0.08
20	0.0635	22.80	22.78	0.06
25	0.0635	29.61	29.59	0.04

portrayed by the results in Table 5, both methods for calculating the inductance of a wirebond are extremely similar with the error percentage shrinking with increasing wirebond length.

$$L \approx \frac{\mu_0}{2\pi} \times l\left[\ln\left(\frac{2l}{r}\right) - \frac{3}{4}\right] \text{ (H)} \tag{2.10}$$

As there commonly exist multiple wirebonds leading to and from a semiconductor device, it is critical to examine the inductive effects shared by two parallel wirebonds [2]. For this study, the two wirebonds are used to connect the designated gate and source pads on the PCB to the corresponding gate and kelvin source locations on the MOSFETs. The mutual-inductance between two parallel wirebonds is given by Equation 2.11.

$$M = \pm\frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{s}\right) + \frac{s}{l} - 1\right] \text{ (H)} \tag{2.11}$$

The two parameters controlling the mutual-inductance are *s*, the separation between the two bonds, and *l*, the length of the bonds.

Table 5. Mutual-Inductance Calculation of Wirebonds of Varying Length

Length (mm)	Separation (mm)	Mutual-Inductance (nH)	Wirebond Self-Inductance (nH)	Total-Inductance (nH)
3	1	0.675	2.279	1.604
3	2	0.459	2.279	1.820
3	3	0.416	2.279	1.863
4	1	1.064	3.269	2.205
4	2	0.709	3.269	2.560
4	3	0.585	3.269	2.684
5	1	1.503	4.309	2.807
5	2	1.009	4.309	3.300
5	3	0.804	4.309	3.505

The mutual-inductance contributes about 1 nH for a 4 mm wirebond when the two bonds have 1 mm – 2 mm of separation. This value is not significant in regard to the total system inductance, but it is slightly over one-third of the self-inductance, which will greatly affect the die-to-die inductance for the circuit model in the next chapter. According to the wirebond profile for the HT-3000 module, the gate and source wirebonds are approximately 3800 μm and 4000 μm respectively. For this reason, 4 mm calculation values are used for comparing to the measured and simulated values in the next sections.

2.3.2 *Measurements*

As it is extremely difficult to accurately measure inductances in the few-nanohenry range, the wirebonds are placed in their intended locations in an empty module, and the entire gate-source loop is measured. This will ensure the wirebonds have accurate separation and length related to their actual operation. The inductance extraction fixture from the previous two measurement

sections is the appropriate tool to extract the full gate-source loop inductance. As there can be up to fourteen MOSFETs in parallel in one switch position in this module, the inductance to each position is measured independently. These results are used to generate the die-to-die parasitic values.

To begin, a clean gate-source PCB is populated with 0 Ω gate resistors and the gate-source connectors. A completed substrate and baseplate assembly provides a base for the PCB and creates a realistic air domain for the measurement. The LCR meter is compensated with an open measurement and a short measurement to ensure that the result does not include the inductance of the fixture. After fixture compensation, the first MOSFET position of the module is wirebonded

Table 6. Inductance Measurement of Gate Kelvin PCB

Position	Low-Side Inductance (nH)	Low-Side Resistance (mΩ)	High-Side Inductance (nH)	High-Side Resistance (mΩ)
1	22.55	63.78	20.67	65.42
2	25.95	72.89	24.11	71.88
3	28.47	74.68	25.95	76.34
4	32.43	87.64	29.09	82.58
5	34.70	87.79	33.28	90.73
6	38.87	97.23	35.98	95.21
7	41.17	103.69	38.50	101.08
8	44.20	107.03	41.66	107.43
9	46.69	112.26	45.69	116.60
10	50.50	122.98	48.16	120.82
11	53.16	126.05	50.58	122.64
12	56.78	136.32	55.26	133.73
13	60.33	141.48	58.28	140.87
14	61.93	140.83	60.29	143.57

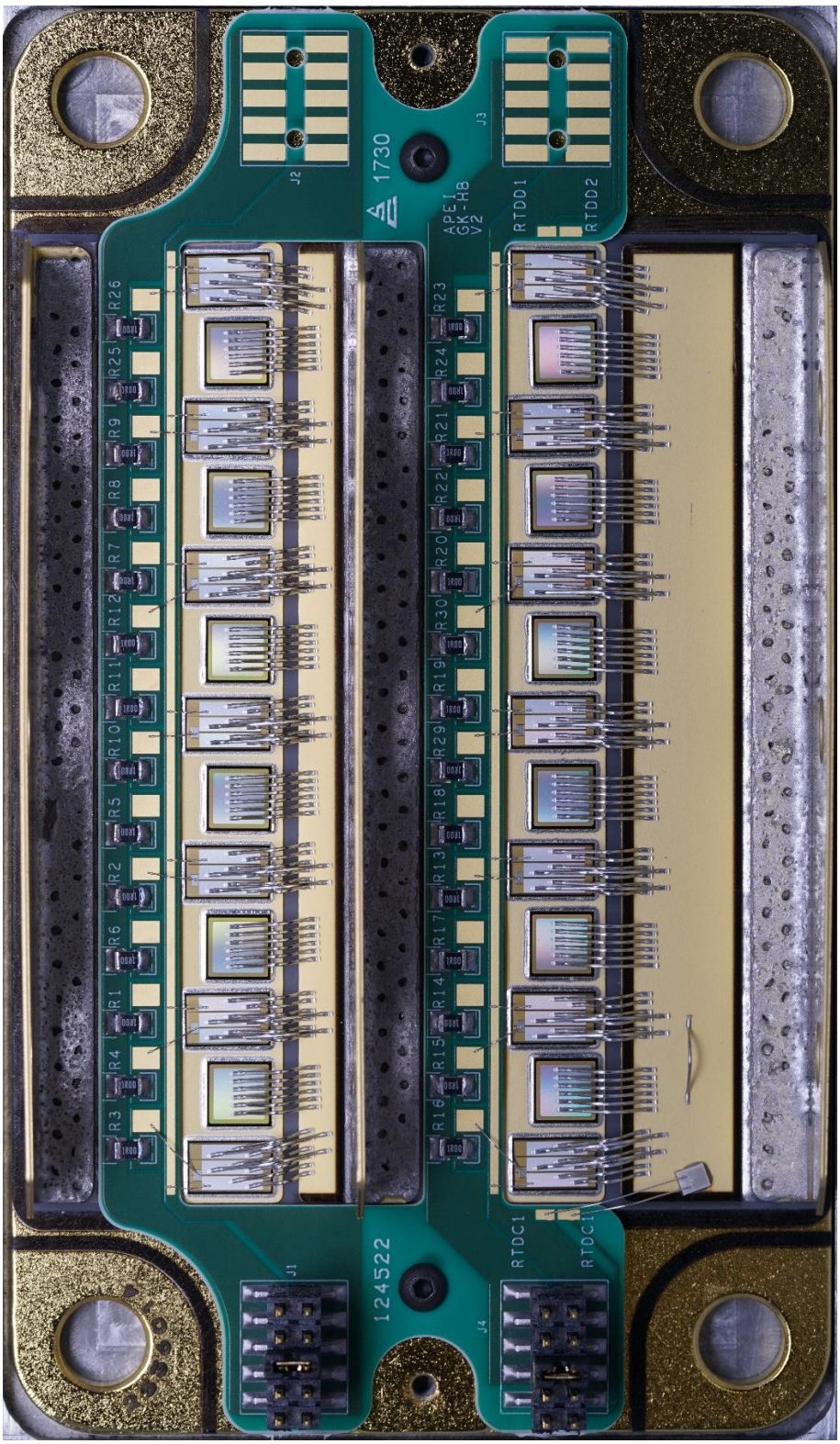

Figure 18. CAS325M12HM2 Gate Network PCB on Substrate Assembly with Wirebonds

from the designated pads on the PCB directly to the substrate rather a bare die. The gate network loop is completed through the short on the substrate. The wirebonded module subassembly is displayed in Figure 18. The measurement is taken at 1 MHz with the maximum source current available on the Agilent LCR meter, 20 mA. The process is repeated for each of the 14 MOSFET positions on the high-side and low-side of the module, and the results are displayed in Table 6.

Examining the last position's inductance value, the connector, PCB, and wirebonds measurement results in an inductance of 60.29 nH for the high-side as shown in Equation 2.12.

$$L_{Connector} + L_{PCB} + L_{G-Wirebond} + L_{S-Wirebond} = 60.29 \text{ nH} \tag{2.12}$$

The measurement of only the PCB and connector produce 55.437 nH as shown in Equation 2.13.

$$L_{Connector} + L_{PCB} = 55.437 \text{ nH} \tag{2.13}$$

This equates to a shared inductance of 4.853 nH for the gate and source wirebonds.

$$\begin{aligned} L_{G-Wirebond} + L_{S-Wirebond} &= 60.29 \text{ nH} - 55.437 \text{ nH} \\ &= 4.853 \text{ nH} \end{aligned} \tag{2.14}$$

Assuming that the inductance of the gate wirebond is equal to the source wirebond, the sum of the two bonds can be split into two equal parts as shown in Equation 2.15.

$$L_{G-Wirebond} = L_{S-Wirebond} = \frac{4.853 \text{ nH}}{2} = 2.427 \text{ nH} \tag{2.15}$$

Comparing to the calculated results for a 4 mm wirebond, this result places the spacing between 1 mm and 2 mm, which is exactly as expected; therefore, the measurement process is proven valid.

2.3.3 *COMSOL Simulations*

The verification of the measurements begins with the formation of a 3D CAD model optimized for accurate and fast simulations. As the measurements for this section were conducted on the entire gate loop, and the previous sections' measurements were subtracted away to obtain the wirebond's inductance contribution, the same procedure is repeated for the simulation. Therefore, starting with the 3D model from the connector and PCB, a wirebond and MOSFET must be added to complete the gate loop.

First, to create the wirebond, two lines are drawn to represent the feet of the bonds. They are placed 2 mm apart on the z-axis to simulate the difference in height of the MOSFET on the substrate and the wirebond pads on the top of the PCB. Next, with the help of a few construction lines, a spline is drawn in between the two feet to simulate the approximate shape of a wirebond. A plane is added to the drawing at the end of one of the feet, and a circle with a diameter of 5 mils

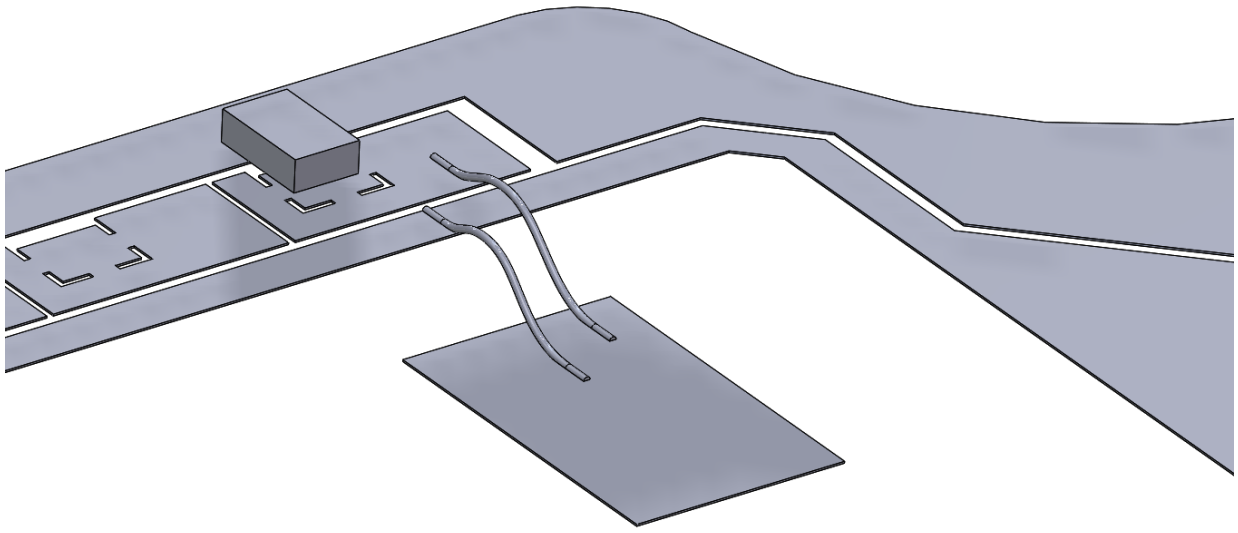

Figure 19. 0.005" Diameter Gate and Source Wirebonds Modeled in Solidworks

is added to represent the diameter of the bond. The circle is swept along the spline to give the bond its 3-dimensional form, and the two ends are sliced in create flat feet that will connect to the pads and the MOSFET.

To complete the gate loop, the gate and source bonds must have a conductive path between them. While the gate would be more accurately modeled with a capacitor, the simulation demands a short between the gate and source. To satisfy this requirement, the MOSFET bare die is modeled as a simple rectangle with a depth matching the copper thickness of the PCB and is defined as copper material in COMSOL. With the two additional parts modeled, the assembly is updated to include a wirebond from the gate wirebond pad on the PCB to the MOSFET model, which is placed 2 mm below the PCB, and a source wirebond is added from the MOSFET up to the PCB as shown in Figure 19. The gate loop and 3D model are now complete, and the model is ready to be imported into COMSOL for meshing.

The model is meshed with a technique enhanced for large, thin planes like those found in this model's PCB. Each face of the model is meshed independently with a free-triangular mesh, the face is then copied to its equivalent bottom-side face, and the two corresponding meshed faces are swept together and distributed into three-dimensional shapes for simulation. After the PCB trace meshes are defined, the wirebonds are meshed with an extremely fine free-tetrahedral mesh. This domain sets the minimum element size for the air domain around it; therefore, similar to the PCB simulation, a small air domain is place around the tightly spaced, last position of the model. This small air domain creates a transition from the small mesh elements of the wirebonds and thermal reliefs to a large element size for the majority of the air domain. This significantly decreases the time required to mesh the system and increases the accuracy in the tightly spaced area. The completed mesh for this model is illustrated in Figure 20.

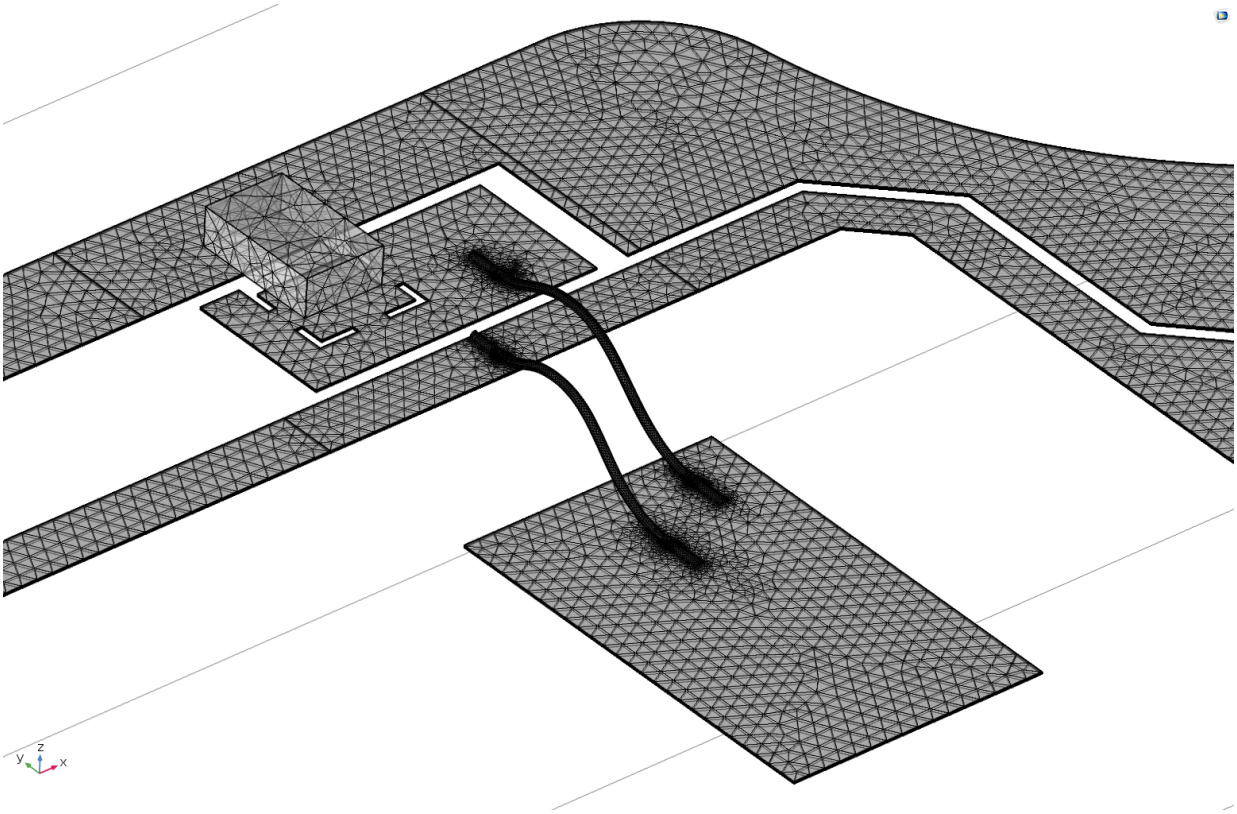

Figure 20. Last Position of Meshed 3D CAD Model in COMSOL

Finally, the simulation is conducted with 1 A of source current at 1 MHz. The simulation took approximately four days to converge due to the extremely fine size of the mesh elements as well as the high-frequency source, but the results proved to be worth the wait. Generating a global evaluation for the inductance of the gate loop resulted in a value of 60.292577 nH, which perfectly matches the high-side, last-position's inductance value of 60.29 nH. Again, the FEA simulation proves to be an effective method for extracting the parasitic inductance.

The simulation method uniquely has the ability to visualize the current density through every element of the 3D model. With this capability, a cross-section of the wirebonds illustrating the current density in A/mm^2 is displayed in Figure 22. An interesting aspect of this cross-section is the clear presence of the proximity effect as well as the skin effect. According to Kazimierczuk, "When two or more conductors are brought into close proximity, their magnetic fields may add or

subtract. The high-frequency current will concentrate within a conductor, where the magnetic fields are additive." [2]. This causes parallel conductors with currents flowing in the same direction to have current crowding on opposite sides, while parallel conductors with currents flowing in opposite directions have current crowding towards the middle of the two conductors. This phenomenon is known as the proximity effect and can be seen in the cross-sections of the wirebonds in Figure 22. Similarly, the skin effect is a high-frequency phenomenon, which is induced by eddy currents within the conductor causing non-uniform current densities [2]. In a circular conductor, the current flows uniformly on the outside or skin of the conductor at high-frequencies when under the influence of the skin effect. This phenomenon is also present in the wirebond and exhibited in Figure 22. The magnetic flux density is visualized in Figure 21 in the

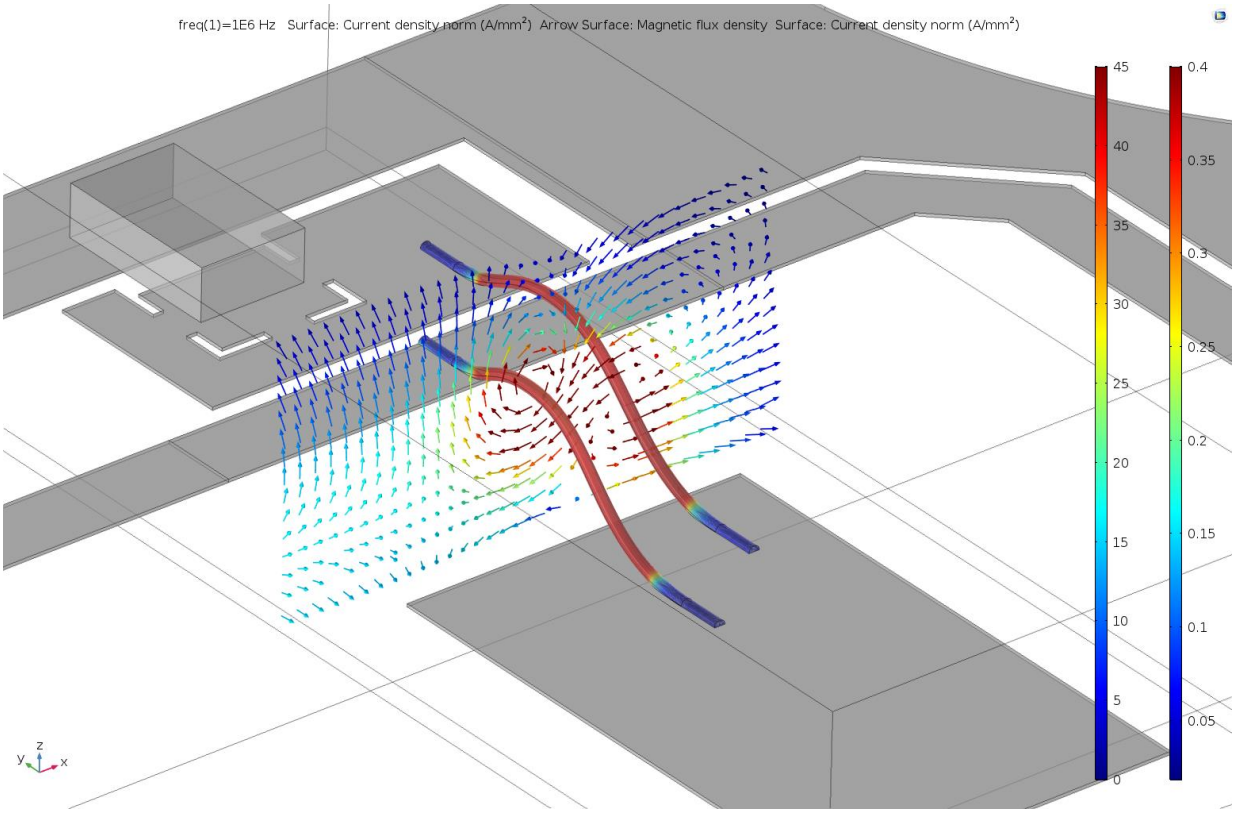

Figure 21. Current Density and Magnetic Flux Density of Wirebonds

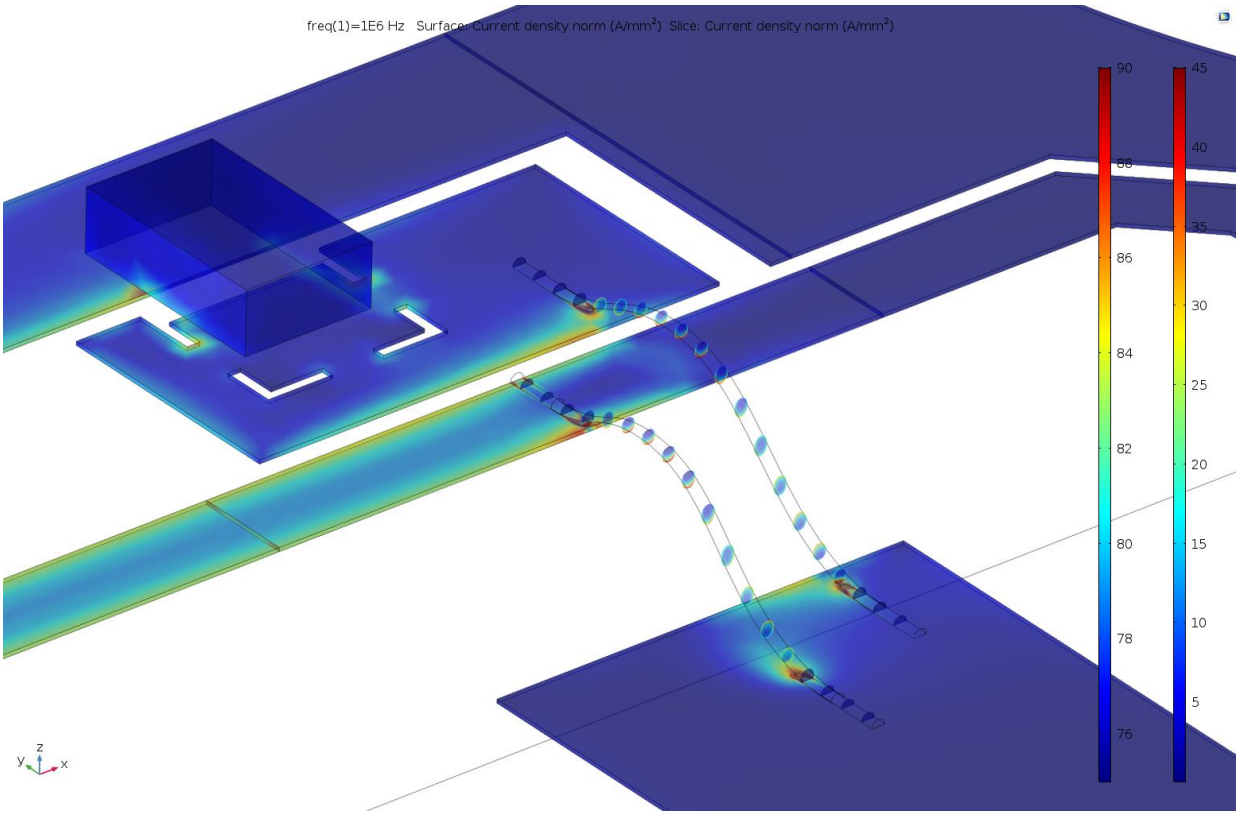

Figure 22. Current Density of Last Position and Proximity Effect of Wirebonds

small, finely meshed air domain around the wirebonds. The summation of the fields can be seen between the two bonds, which generates mutual-inductance and lowers the overall parasitic inductance of the bonds.

2.4 Conclusion

The internal gate-source network of a high-performance, SiC-based power module was divided into three sections: the input connector, the printed circuit board, and the wirebonds. Three parasitic extraction methods were utilized to obtain the inductance values for the three sections of the network with great success. The first, the input connector, contained the greatest error percentage between the measured value and the two other methods with a value of 19%, yet there was only approximately 0.5 nH difference between the three methods. The PCB showed extremely consistent results with a maximum error percentage of only 3.5% and a maximum difference of

Table 7. Comparison of Inductance Extraction Methods

Parameter	Calculated	Measured	Simulated	Units
Connector	2.602	2.097	2.611	nH
PCB (Last Position)	51.092	52.896	52.976	nH
Wirebond (One Bond from Pair)	2.430	2.427	2.353	nH
Last Position	58.553	60.290	60.293	nH

1.88 nH. The wirebond contained the lowest error percentage of 3.17% and a difference of only 0.074 nH. Table 7 displays the full list of results from each extraction method. These values will be used extensively in the next chapter to construct an accurate model of the gate-source network in SPICE.

2.5 References

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CHAPTER 3

GATE NETWORK MODELING AND ANALYSIS

This chapter presents the construction of the gate network SPICE model of a high-performance, SiC-based power module. The thoroughly investigated parasitic inductance values from the previous chapter will be utilized to calculate the lumped element, die-to-die inductances, and the acquisition of the parasitic resistances and capacitances will be discussed briefly. A SPICE model of the gate network will be created using these parasitic values, and the model will be exhaustively tuned to meet a list of stability and safe-operating-area (SOA) criteria. Finally, the gate network model will be combined with the power-loop model of the module, and the effects of parameter variation in SiC MOSFETs will be examined.

3.1 Parasitic Elements of the Gate Network

The model-ready parasitic elements of the gate network will be extracted from the values obtained in the previous chapter; additionally, the consideration of resistive and capacitive elements will be discussed. First, an overview of the lumped parameters in this study will be illustrated.

3.1.1 *Lumped-Element Parasitic Model Overview*

As there exist infinitesimal parasitic inductances, capacitances, and resistances in the physical power module, it is crucial to select only a meaningfully set of elements that significantly contribute to the performance in question. These lumped elements, while fewer than the actual number of parasitics in the system, provide an accurate model of the real-world circuit. They also make available a myriad of circuit analysis methods including series and parallel RLC circuit analysis and rapid simulations using SPICE. Figure 7 illustrates two of the fourteen MOSFET positions in the gate network, lumped-element model. Many of the parameters shown in

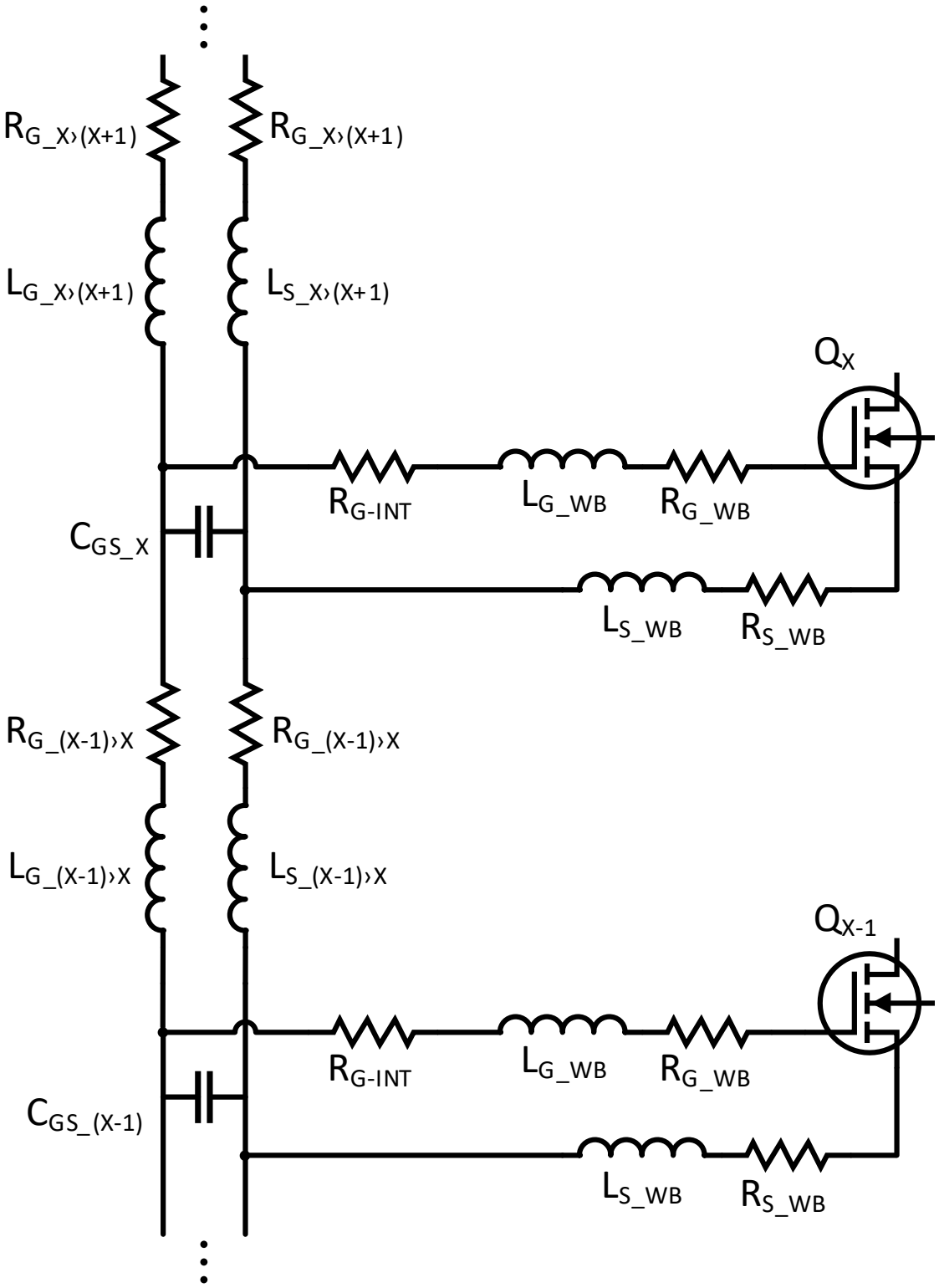

Figure 23. Lumped-Element Parasitic Model of Two MOSFET Positions

the figure were directly extracted in the previous chapter; however, some of the parameters will need to be derived from a system of equations of the measured values. After all of the parameters are defined, the values will be entered into a SPICE circuit simulation of the gate network mimicking the circuit in Figure 7.

3.1.2 *Die-to-die Parasitic Inductances*

One of the parameters that must be derived from the obtained measurements is the die-to-die inductance values. These values are represented by $L_{G\_(X-1)>X}$ and $L_{G\_X>(X+1)}$, $L_{S\_(X-1)>X}$, and $L_{S\_X>(X+1)}$ in the lumped parameter model in Figure 7. As each MOSFET position's inductance and resistance values were measured, a system of equations can be crafted to link the individual position's measured value to a combination of the individual inductances of interest in the path. For example, the inductance of the first MOSFET position in the module is the combination of the inductance of the connector and the inductance of the trace between the connector and MOSFET. For the next position, the inductance is the combination of the first position's value plus the additional inductance to the second position. To obtain the position-to-position inductance, the first position's inductance must be subtracted from the second position's value. This process is repeated until all of the MOSFET-to-MOSFET inductance values are known. This process is summarized by Equation 3.1 below.

$$\begin{gathered} L_{CONN} + L_{CONN-1} = L_1 \\ L_{CONN} + L_{CONN-1} + L_{1-2} = L_2 \\ L_{CONN} + L_{CONN-1} + L_{1-2} + L_{2-3} = L_3 \\ L_{CONN} + L_{CONN-1} + L_{1-2} + L_{2-3} + L_{3-4} = L_4 \\ L_{CONN} + L_{CONN-1} + L_{1-2} + L_{2-3} + L_{3-4} + L_{4-5} = L_5 \\ \bullet \\ \bullet \\ \bullet \end{gathered} \tag{3.16}$$

Table 8. Die-to-die Parasitic Inductance Values

Parameter	High-Side	Low-Side	Units
L_{CONN-1}	19.95	18.07	nH
L_{1-2}	3.40	3.44	nH
L_{2-3}	2.52	1.84	nH
L_{3-4}	3.96	3.14	nH
L_{4-5}	2.27	4.19	nH
L_{5-6}	4.17	2.70	nH
L_{6-7}	2.30	2.52	nH
L_{7-8}	3.03	3.16	nH
L_{8-9}	2.49	4.03	nH
L_{9-10}	3.81	2.47	nH
L_{10-11}	2.66	2.42	nH
L_{11-12}	3.62	4.68	nH
L_{12-13}	3.55	3.02	nH
L_{13-14}	1.60	2.01	nH
Average $L_{x-(x+1)}$	3.03	3.05	nH

After applying Equation 3.1 to all of the positions, all of the die-to-die parasitic inductance values are known. As the layout of the printed circuit board is symmetrical for each MOSFET position, the inductance between any two neighboring positions should be identical to any other two neighboring positions. For this reason, the average value of the die-to-die inductance is calculated as 3 nH and is used in the SPICE model. It is crucial to determine this value as the die-to-die interactions of the high-speed SiC MOSFET must be modeled correctly to simulate unwanted high-frequency oscillations caused by paralleling. If the measured values were simply inserted into the model, there would be an enormous amount of inductance between the MOSFETs even though the position's gate-source inductance loop would be correct.

3.1.3 *Parasitic Resistance and Capacitance Considerations*

Until this point, the parasitic element discussion has focused on inductance, which has the most significant influence over the factors examined in the upcoming sections. However, parasitic resistance and capacitance are present in the gate network and should be reviewed and included in the model where appropriate. This section will examine the resistance of the wirebonds using theoretical calculations as well as the capacitance of the PCB using measure techniques.

To determine the resistance of the wirebonds, the material properties and the size of the bond must be identified. Equation 3.2 illustrates this relationship where σ is the conductivity, *a* is the radius of the wirebond, *l* is the length of the wirebond, and δ is the skin depth of the material [1].

$$R = \frac{l}{2\pi a \delta \sigma} \tag{3.17}$$

The conductivity of aluminum is 3.77×10^7 S/m, the average length of the wirebonds in this study is 4 mm, and the radius of the bond wire is 5 mils or 0.0635 mm. The skin depth of aluminum must be calculated with Equation 3.3 where f_o is the desired frequency of operation, ρ is the resistivity of the material, μ_0 is the permeability in a vacuum, and μ_r is the relative permeability of the material.

$$\delta = \sqrt{\frac{\rho}{\pi f_o \mu_r \mu_0}} \tag{3.18}$$

An operating frequency of 1 MHz is chosen to match the other measurements and calculations from the previous sections. The resistivity of aluminum is 2.6548 μΩ·cm and the relative permeability is 1.00002. Solving Equation 3.3 for an operating frequency of 1 MHz results in a skin depth of 82.0 μm for an aluminum wirebond. The wirebond resistance equation's variables

are all known; therefore, the result is calculated below and will be included in the SPICE model of the gate network.

$$R = \frac{4\text{ mm}}{(2\pi)(0.0635\text{ mm})(0.082\text{ mm})(37700\text{ S/mm})} = 3.243\text{ m}\Omega \qquad (3.19)$$

The measurement method used in section 2.2.2 will be adjusted to obtain the capacitance between the gate and source traces in the printed circuit board. The custom parasitic extraction fixture for the PCB is attached to the Agilent LCR meter and a short calibration is performed on fixture. Next, an open compensation is performed on the fixture to account for the stray capacitance in the measurement hardware, which ensures that the measured capacitance will only include the connector and the printed circuit board. Setting the equipment to a C_S and R_S measurement with a 2 V output at 1 MHz, the capacitance value obtained for the connector and PCB was 9.6 pF. This capacitance is negligible will not appear in the model as the input capacitance for a single MOSFET is roughly an order of magnitude higher than the measured parasitic capacitance.

3.2 Safe-Operating-Area and Stability Criteria

Now that the gathering of parameters is complete, the complete model of the gate network can be analyzed. Four aspects of reliable operation are examined in this section including gate-to-source overvoltage avoidance, the effects of the network's propagation delay on switching performance, an inherent oscillatory behavior due to high switching speed, and an investigation of large source return current through the gate network. The SPICE model that was created in the previous sections will be extensively utilized to provide evidence for the issues presented and to assist in offering solutions to these problems.

3.2.1 *Gate-to-Source Over-Voltage Deterrence*

The first safe-operating-area parameter to be investigated is the MOSFET's rated gate-source voltage during transient operation of the power module. In order to guarantee the highest level of reliability of the module, an overvoltage must never be induced at the gate of any MOSFET in the module. As each position exhibits different parasitic values, there will be a gradient of transient peak voltage levels observed at each of the FET positions. In this section, series RLC circuit analysis is used to determine the passive components required to remove the module's ability of violating the gate-source voltage rating.

According to Wolfspeed's CPM3-0900-0010A datasheet, if the MOSFET's body diode is used, the transient V_{GS} maximum range is reduced to +19 V / -4 V [2]. As the recommended gate-voltage during the off-state is also -4 V, there is no room available for overshoot during transient operation. The body diode must be used during the deadtime of a half-bridge MOSFET configuration in order to freewheel the current in the load inductor while both switch positions are off. This fact forces the lack of V_{GS} overshoot on each MOSFET in the HT-3000, half-bridge power module under investigation in this effort.

Using the lumped-element parasitic model of the gate-source network obtained in the previous section, series RLC circuit analysis can be applied in order to determine the damping factor required to prevent overshoots of V_{GS} at the terminals of the MOSFETs. The damping of the overshoot is accomplished by the addition of extra resistance in the RLC series network. The extra resistance is realized with a surface-mount chip resistor placed in the gate path of each FET. The capacitance represents the input capacitance of the FET, C_{iss}, which is obtained from the device's datasheet and is highly voltage dependent. The inductance is realized as the parasitic inductance

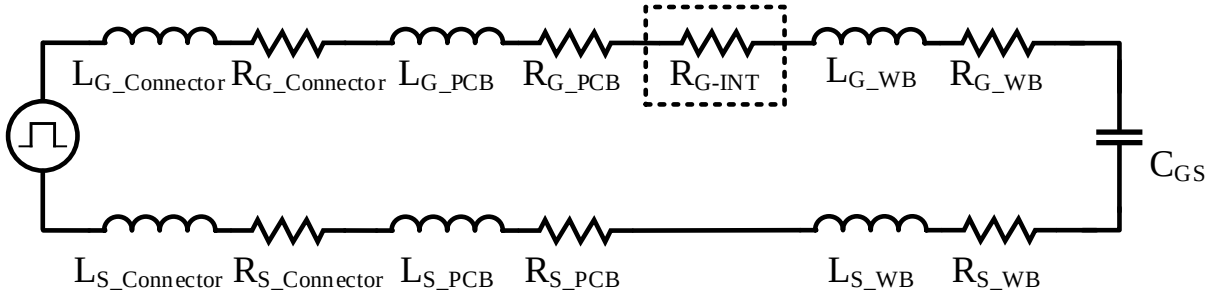

Figure 24. Series RLC Circuit of Last MOSFET Position

of the gate source network and is different for each position; therefore, only the worst-case inductance value must be considered as it sets the limiting factor.

When looking into the power module's gate and source connection points, the impedance seen by the gate driver is a series combination of resistors, inductors, and a capacitor. This series RLC circuit has many parameters as illustrated in Figure 24, yet the behavior of its response to a transient turn-on or turn-off event is identical to that of a standard, three-element RLC circuit. Using this connection, each of the resistances and inductances in Figure 24 are summed to create a single resistive and inductive component, and the equivalent circuit is displayed in Figure 25. The $R_{G\text{-}INT}$ component is left separate from the equivalent resistive component to demonstrate its importance as the independent variable in this study. $R_{G\text{-}INT}$ is the parameter that is tuned to achieve the desired response of the series RLC circuit.

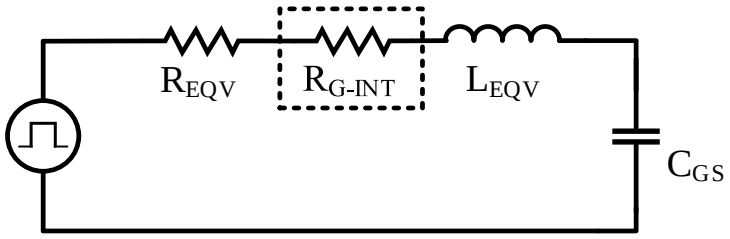

Figure 25. Equivalent Series RLC Circuit of Last MOSFET Position

In order to determine the optimal value for $R_{G\text{-}INT}$, series RLC circuit analysis must be performed. The characteristic equation for the series RLC circuit is displayed in Equation 3.5 below. This differential equation has two roots, which are shown in Equation 3.6.

$$s^2 + \frac{R}{L}s + \frac{1}{LC} = 0 \tag{3.20}$$

$$s_{1,2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{3.21}$$

Two important parameters of the series RLC circuit are the damping attenuation, which is the measure of how fast the transient response of the circuit will diminish after subjected to a step pulse [3]. The damping attenuation or neper frequency is show in Equation 3.7.

$$\alpha = \frac{R}{2L} \tag{3.22}$$

Next, the resonance frequency shown in Equation 3.8 is the frequency at which the RLC circuit will oscillate after subjected to a step pulse. This resonance occurs when the impedance of the circuit is at a minimum and is purely real or completely resistive [3].

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.23}$$

The damping factor is used to determine if the system will be overdamped, underdamped, or critically damped and is the ratio of the damping attenuation, α, to the resonance frequency, ω_0, as shown in Equation 3.9.

$$\zeta = \frac{\alpha}{\omega_0} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{3.24}$$

A system will be critically damped when the damping factor is equal to one. "The critically damped response represents the circuit response that decays in the fastest possible time without going into oscillation." [3].

Not every power module will encompass the same values for R and C due to the many different MOSFETs used in the several module variants; therefore, values for three common Wolfspeed MOSFETs are used to determine the required critically damping resistance. The on-chip gate resistance and the gate-to-source capacitance are unique for each MOSFET and are displayed in Table 9. Solving Equation 3.9 using the parasitic equivalent values of the last MOSFET position and the MOSFET datasheet parameters, the required lumped resistance necessary to achieve critical damping is shown in Table 9.

To verify that the circuit is sufficiently damped, the circuit parameters are inserted into a series RLC circuit simulation using SPICE. The result is displayed in Figure 26 and clearly demonstrations adequate damping during the transient turn-on and turn-off events as there is no positive or negative overshoot to violate the MOSFET SOA rating.

Table 9. Critical Damping for Three Common SiC MOSFETs

Parameter	CPM3-1200-0013	CPM2-1200-0025	CPM3-0900-0010	Units
C_{GS}	7658	2773	4488	pF
L_{EQV}	60.29	60.29	60.29	nH
$R_{ON\text{-}CHIP}$	5.9	1.1	1.6	Ω
R_{EQV}	0.1436	0.1436	0.1436	Ω
$R_{G\text{-}INT}$	-0.43	8.08	5.59	Ω

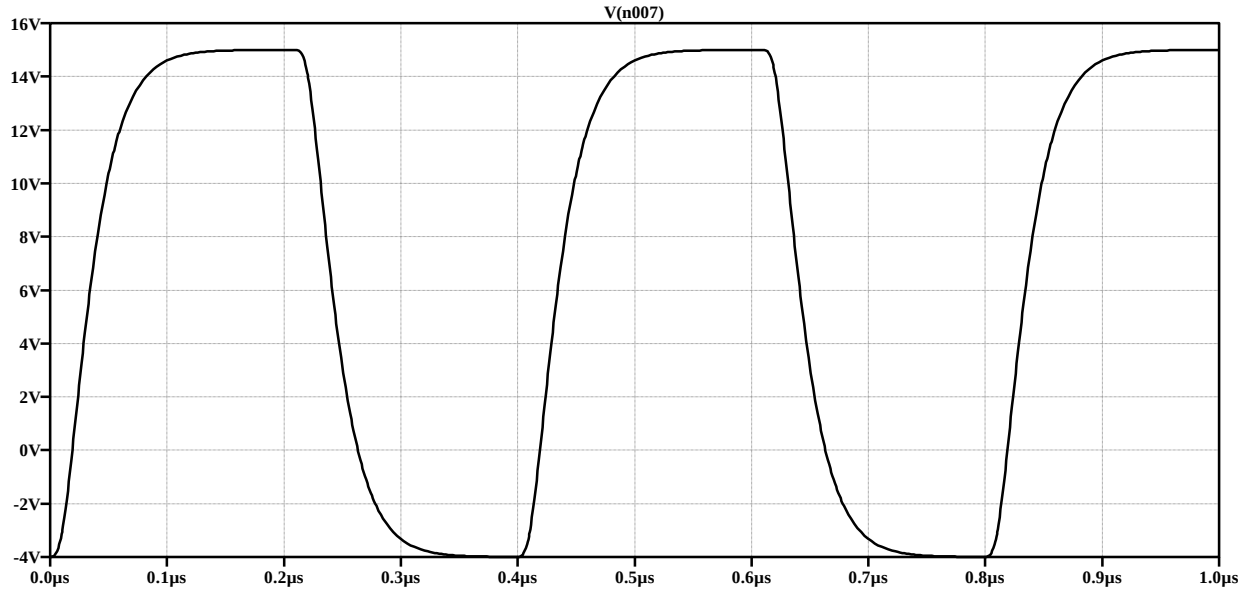

Figure 26. Verification of $R_{G\text{-}INT}$ in the Series RLC Circuit of Last MOSFET Position

Now that a value for $R_{G\text{-}INT}$ has been selected, it must be verified in the complete gate network model. Using the model shown in Figure 25, the values for $R_{G\text{-}INT}$, C_{GS}, and $R_{ON\text{-}CHIP}$ are updated

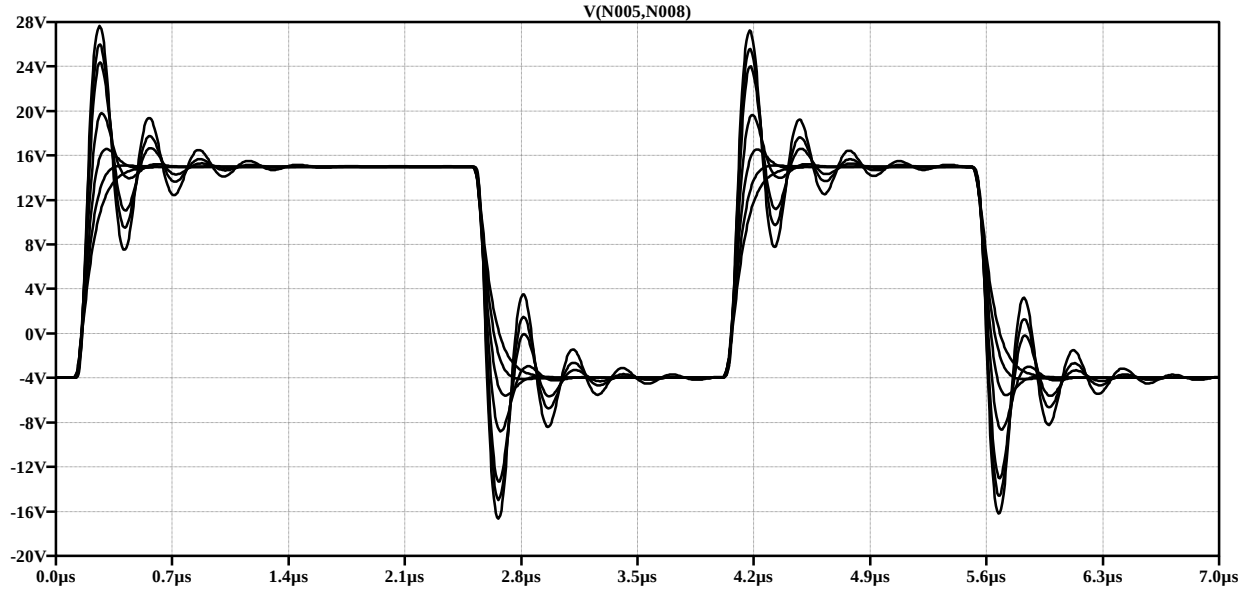

Figure 27. Verification of $R_{G\text{-}INT}$ in the Full Gate Network Model

to the CPM3-0900-0010A's values in Table 9. The simulation is set up to sweep $R_{G\text{-}INT}$ over a list of resistances including 0 Ω, 1 Ω, 5.59 Ω, 10 Ω, 15 Ω, and 20 Ω to verify that the calculated resistance is adequate for damping overshoots at each position. The resulting waveform of the gate-source voltage of the last FET position is displayed in Figure 27. The waveforms containing higher magnitude over and undershoots represent lower $R_{G\text{-}INT}$ values with 0 Ω being the largest magnitude oscillation reaching nearly +28 V and -16 V. As the 5.59 Ω parameter simulation contains overshoot, the simulation proves that treating each MOSFET position as a unique and independent RLC network does not accurately portray the behavior of the position. According to the parametric simulation, an $R_{G\text{-}INT}$ value of 15 Ω is required to achieve critical damping on V_{GS} at the last MOSFET position for the third generation, 900 V, 10 mΩ MOSFET. This will be the new selected value moving forward with this study.

3.2.2 *Propagation Delay Between MOSFET Positions*

When operating MOSFETs in parallel, the various devices will never turn on or turn off at the exact same instance. This phenomenon is caused by many issues including tolerance differences in device parameters such as threshold voltage as well as from the delay of the gate signal introduced from parasitics in the gate path [4]. This section examines the effects of the propagation delay of the module's gate network on the individual MOSFET transient times including the resulting mismatches in current sharing and switching loss due to dissimilar turn on and turn off timing. The effect of dissimilar voltage threshold due to tolerance differences will be examined in a later section.

The gate network model used in the previous section is used to determine the time at which each MOSFET position reaches the rated threshold voltage during both the turn-on and turn-off

transitions. As determined in the previous section, the $R_{G\text{-}INT}$ resistance is set to 15 Ω and the parameters for the CPM3-0900-0010A MOSFET are entered into the simulation parameters.

The simulation is performed and the gate-to-source voltage for each MOSFET is measured on the same plot. Next, the turn-on transient is zoomed into view such that the difference in propagation delay can be extracted using cursors for each trace at the MOSFET's rated threshold voltage of 1.7 V. The resulting waveform is shown in Figure 28 below. As would be expected, the MOSFET closest to the gate driver, also known as the first MOSFET and denoted with a 1 in the waveform, is the first to turn on just as the last MOSFET, denoted with a 14, is the last device to turn on. Using the cursors, the exact time that each MOSFET reaches 1.7 V is extracted and recorded. Finally, the difference in time between each position is calculated from this data, and the propagation delay is determined for the turn-on transition. The data is normalized to the first position such that there is zero propagation delay at the first position and the second position is the first device to exhibit propagation delay. The data collection is repeated in the same manor at the

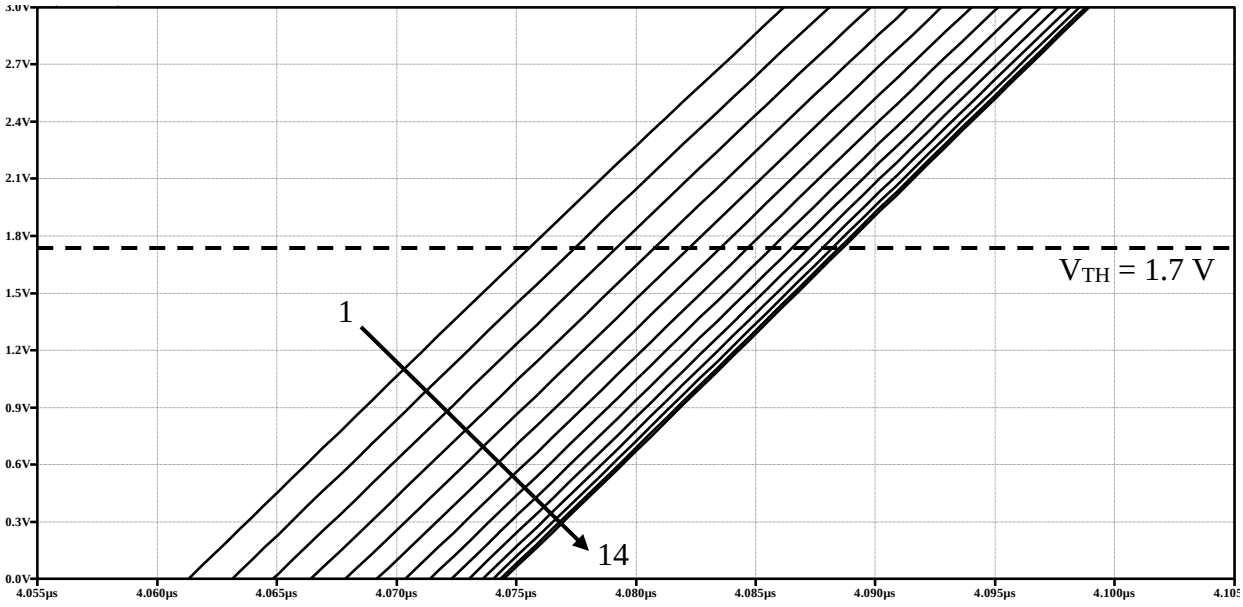

Figure 28. Zoomed Turn-On Transient of each MOSFET's V_{GS} at the Threshold Voltage

turn-off transition, and the delays of the two transitions are plotted in Figure 29. As can be seen in the plot, the delay curves are parabolic and exhibit a much higher difference in delay between the first few positions when compared to the last few positions. Also, the turn-on delay is much larger than the turn-off delay, which is caused by the level of the threshold voltage in the V_{GS} range. As the threshold voltage of +1.7 V is relatively low in the -4 V to +15 V range that the gate-to-source voltage transitions, the delay is longer on the way up and much less on the way down. If the threshold voltage were much higher in the V_{GS} range, the curves would be flipped, and the delay would be shorter during the turn-on than during the turn-off. As the majority of MOSFETs operate in a similar way to the devices in this study with a V_{TH} close to the negative

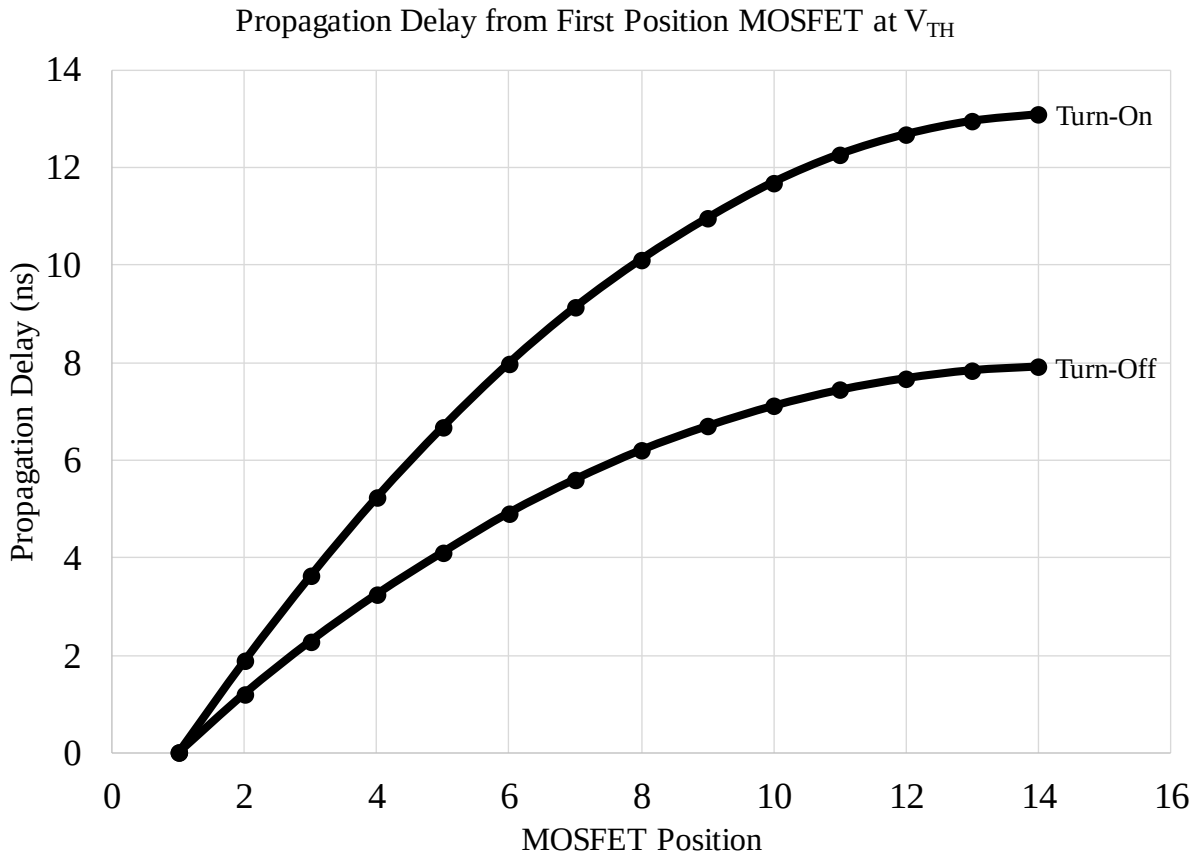

Figure 29. Propagation Delay of each MOSFET for Turn-On and Turn-Off Transitions

range of V_{GS}, it is safe to assume that most MOSFET-based power modules will exhibit a larger turn-on propagation delay compared to its turn-off delay as shown in Figure 29.

With the propagation delay values examined, the next stage is to determine its effect on the module's dynamic behavior including transient current sharing and differences in switching loss. Twenty-eight CPM3-0900-0010A MOSFET models are added to the current SPICE model of the gate network: fourteen MOSFETs for the positions on the low-side and fourteen MOSFETS to fill the positions on the high-side. A standard double-pulse, clamped-inductive-load test is established in the simulation with a load inductor of 10 µH, a DC bus voltage of 600 V, and pulse widths to create a switched current of about 20 A per MOSFET or 280 A per module. The high-side position is held at -4 V while the low-side is switched using the third-generation voltage rails of -4 V and +15 V. The simulation is conducted and the individual MOSFET source currents of the low-side are measured as well as the drain-to-source voltage across the low-side position.

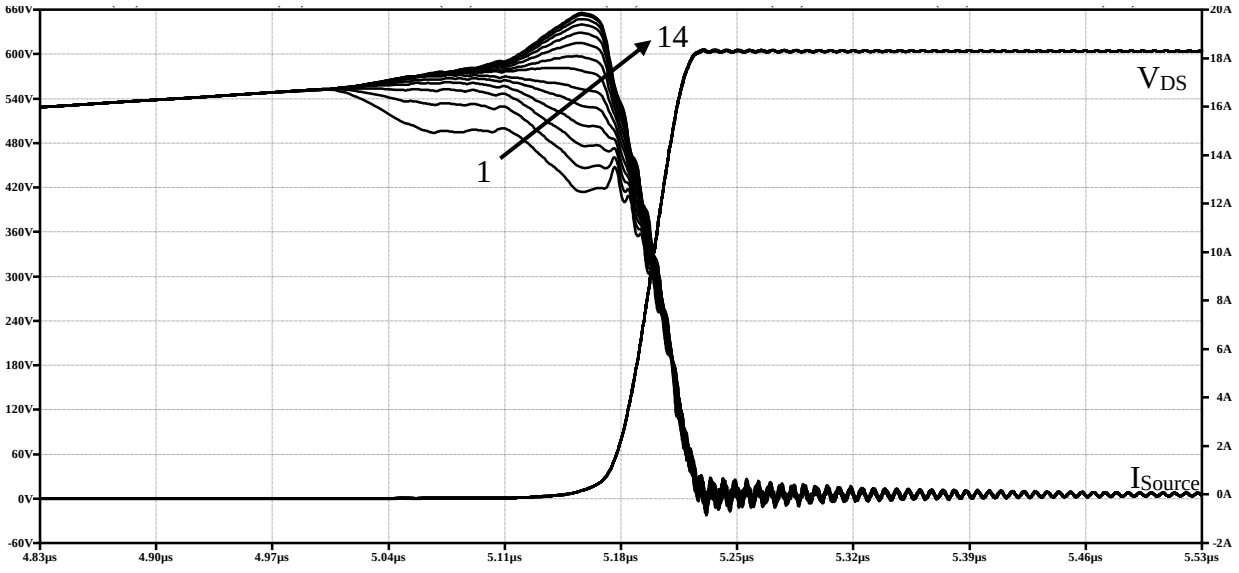

Figure 30. Turn-Off Transition of 14 Paralleled MOSFETs in Power Module

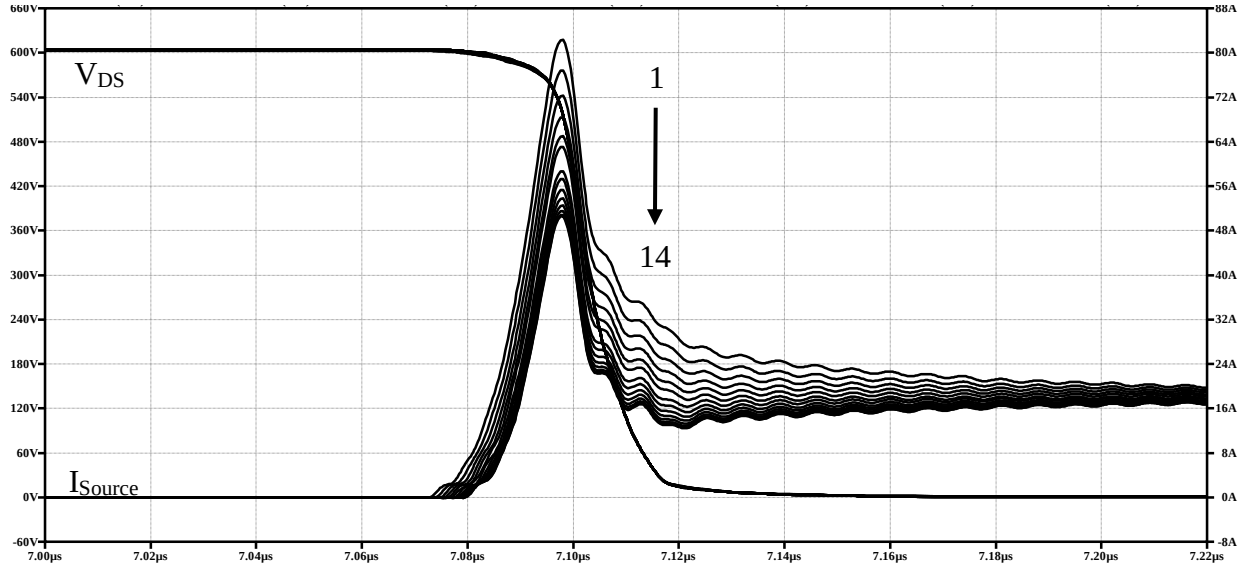

Figure 31. Turn-On Transition of 14 Paralleled MOSFETs in Power Module

The source current traces in the two transient waveforms of Figure 30 and Figure 31 illustrate the effect of the propagation delay on the individual MOSFETs in a power module. As Figure 29 described, the first MOSFET turns on a few nanoseconds before the other MOSFETs; therefore, it alone is responsible for carrying the entire current of the module until the next MOSFET reaches its threshold voltage. As the first device has a head start on conducting current, it will exhibit the lowest R_{DSON} during the transition and observe the largest peak current resulting from the reverse recovery of the high-side position's body diodes as shown in Figure 31. Moving down the module, the peak currents decrease as the MOSFETs exhibit gradually higher R_{DSON} values when compared to the first MOSFET.

A very similar phenomenon takes place during the turn-off transition. The first MOSFET begins to stop conducting current before the other devices, which forces the other devices to divvy up the current that was being carried by the first position. This behavior continues until the last MOSFET is carrying more current than all of the devices turning off before it. Figure 30 illustrates this effect very clearly. It is now necessary to determine the consequences of this non-uniform dynamic

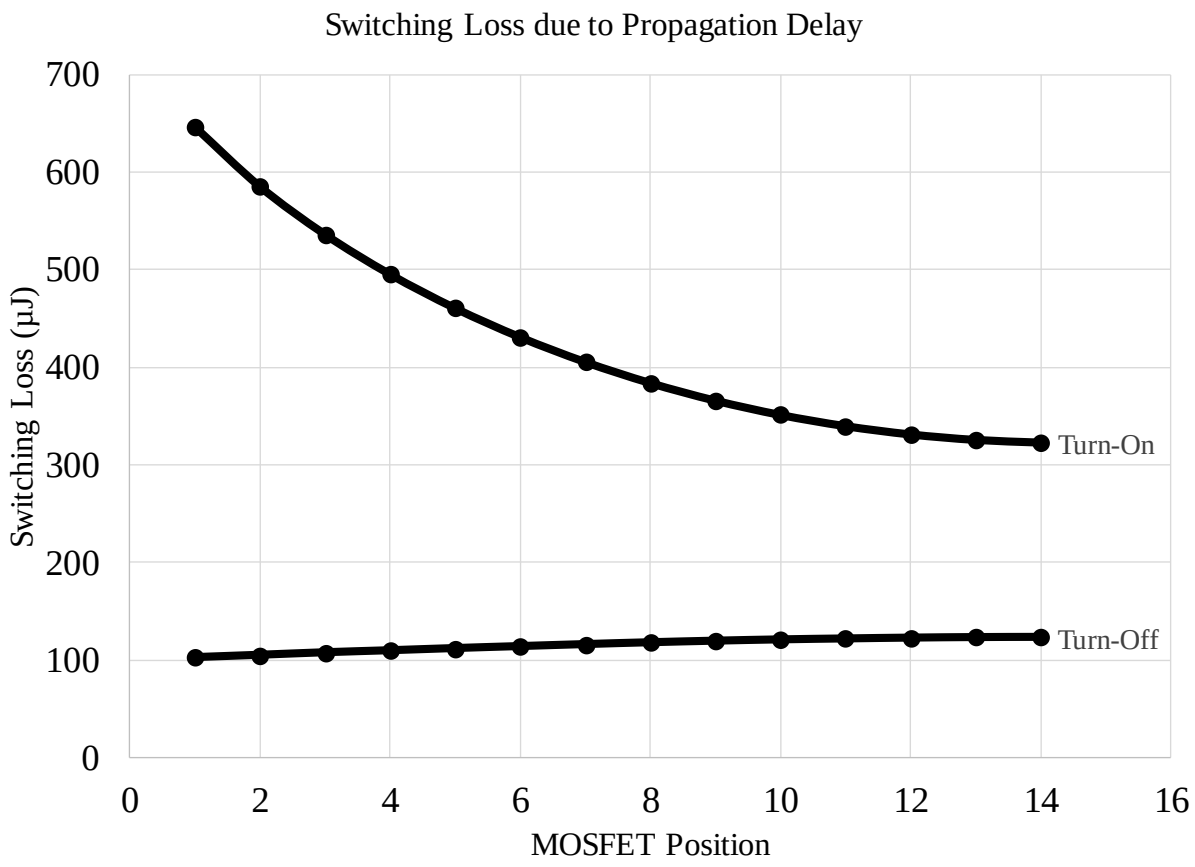

Figure 32. Individual MOSFET Switching Loss Values during Turn-On and Turn-Off

current sharing, which will materialize as a difference in switching loss for each MOSFET in the module.

Using the results shown in Figure 30 and Figure 31, the switching loss of each MOSFET can be calculated by multiplying its source current by the V_{DS} across the device and integrating the resulting waveform as described in Equations 3.10 and 3.11.

$$E_{OFF} = \int_{t_{(v_{DS}=0)}}^{t_{(i_S=0)}} i_S * v_{DS}\, dt \tag{3.25}$$

$$E_{ON} = \int_{t_{(i_S=0)}}^{t_{(v_{DS}=0)}} i_S * v_{DS}\, dt \tag{3.26}$$

This is a simple task for SPICE, and the resulting energy values for the turn-on and turn-off transitions are plotted in Figure 32. As expected, the turn-on energy loss is largest for the first position MOSFET, which observes the highest peak current while the last position experiences the least amount of turn-on loss due to its smallest peak current. In turn, the opposite effect occurs in the turn-off transient as the last position conducts the largest amount of current and therefore exhibits the largest amount of switching loss. Figure 32 illustrates that this effect does not provide balancing of the total switching loss values as the difference in turn-on energy greatly outweighs the difference in turn-off energy.

For this example, MOSFET 1 experiences 67 % more switching loss than MOSFET 14, which is quite significant when operating at high switching frequencies. It is commonly known that MOSFETs exhibit a positive temperature coefficient in regard to R_{DSON}, which balances the conduction losses of paralleled MOSFETs. This effect only applies to steady-state current conduction and does not assist with differences in switching loss [5]. Therefore, applications that are switching loss dominated will experience the effects of propagation delay greater than conduction loss dominated applications.

Possible methods to mitigate this effect include individually tuned gate resistors per MOSFET position to minimize propagation delay. This method is realistically impossible as will be shown in future sections; the device parameter tolerance distribution outweighs the effects of propagation delay and introduces too many variables to accurately tune the gate network to counteract this phenomenon. There is also the limitation of obtainable resistor values as this method would require many specific and unobtainable values of resistance. This issue ultimately results in a derating of the power processing capability of the power module.

3.2.3 *Oscillatory Behavior and Stability Criteria*

As discussed in the previous section, MOSFETS operating in parallel never transition at the exact same instance in time, but there are more detrimental effects that can arise other than a mismatch in switching loss. When the fastest MOSFET turns off first, either due to its position in the module or its low value of threshold voltage, the voltage across the device rises rapidly. This large dv/dt event on the drain of this MOSFET forces current through the reverse transfer capacitance, C_{RSS} or C_{GD}, which can charge the gate-to-source capacitance, C_{GS}, or even induce high-frequency oscillations of the other MOSFETs in parallel [6]. The path that allows this oscillation to occur is illustrated in Figure 33 below [5]. As the drains of the devices are tightly coupled due to the physical structure of the MOSFET and the packaging of the module, the values of L_{D1} and L_{D2} are very small. Without any internal gate resistance per device, R_{G1} and R_{G2}, the parallel combination of MOSFETs form a resonant circuit commonly referred to as a Colpitts oscillator [6]. According

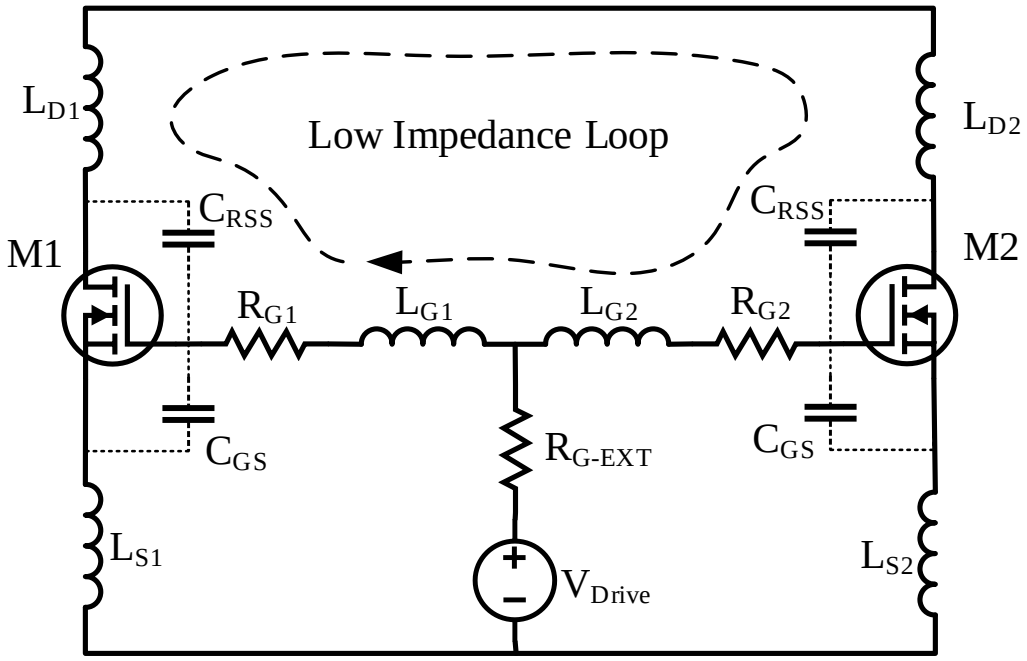

Figure 33. Low-Impedance Path of Two Parallel MOSFETs Capable of Inducing Parasitic Self-Oscillations

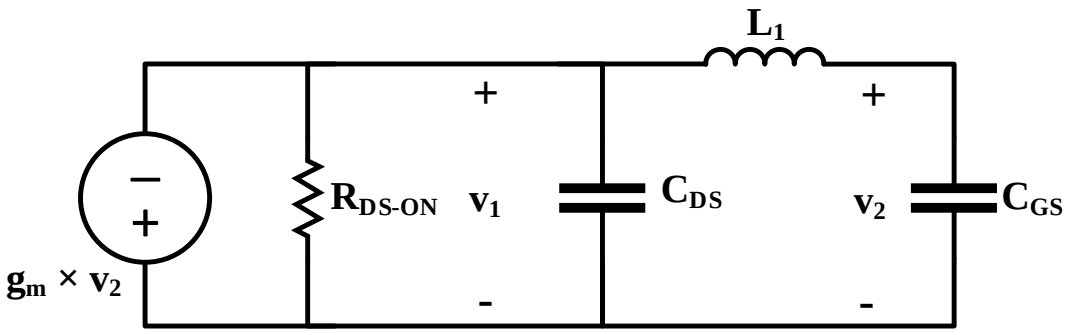

Figure 34. Colpitts Oscillator Formed from Two Paralleled MOSFETs

to Toshiba in Power Parasitic Oscillation between Parallel Power MOSFETs, "Consequently, parallel MOSFETs form a resonant circuit with a high Q factor, which is highly susceptible to oscillation because of a high-gain feedback loop." This high-gain feedback loop is comprised of the transconductance of the MOSFET, g_m, the on-state resistance of the FET, $R_{DS\text{-}ON}$, the gate-to-source capacitance, C_{GS}, and the drain-to-source capacitance, C_{GD}. This article also provides an analysis of the Colpitts oscillator equivalent circuit shown in Figure 34. The inductance, L_1, is a substitution for the parallel resonant circuit comprised of the gate-to-drain capacitance, C_{GD}, and the drain inductance, L_D, between the FETs when oscillating at frequencies below its resonance [6]. The gain equation is found below in Equation 3.12.

$$\frac{v_2}{v_1} = \frac{-g_m \times r_{DS-ON}}{1 - \omega^2 L_1 C_{DS} + j\omega(C_{DS} + C_{GS} - \omega^2 L_1 C_{DS} C_{GS}) r_{DS-ON}} \tag{3.27}$$

To ensure that the circuit does not oscillate, the real part of the gain equation must be less than one. Simplifying the gain equation results in Equation 3.13 below, which can be used to determine the stability of a power MOSFET and verify its aptitude for paralleling.

$$g_m \times R_{DS-ON} \leq \frac{C_{GS}}{C_{DS}} \tag{3.28}$$

Table 10. Stability Verification for Three Common SiC MOSFETs

Parameter	CPM3-1200-0013	CPM2-1200-0025	CPM3-0900-0010	Units
C_{GS}	7658	2773	4488	pF
C_{DS}	243	205	338	pF
$R_{DS\text{-}ON}$	0.013	0.025	0.010	Ω
g_m	76	23.6	97	S
$R_{DS-ON} \times g_m \times \frac{C_{DS}}{C_{GS}}$	0.031	0.044	0.073	V/V
Stability	Stable	Stable	Stable	-

Using Equation 3.13, the three common SiC MOSFETs are verified for stability. As the product of the on-state resistance, the transconductance, and the ratio of C_{DS} to C_{GS} is much less than one, all of the MOSFETs are stable. This is largely due to the low on-state resistance as well as the extremely small C_{DS} to C_{GS} ratio exhibited by the SiC power MOSFETs.

It is shown throughout literature that the presence of an individual gate resistor per MOSFET is crucial for stable, parallel operation of the FETs [5], [6], [7], [8], [9], [10]. This resistor increases the impedance of the 'low-impedance loop' illustrated in Figure 33 above and serves to circumvent high-frequency oscillations from cultivating during turn-on and turn-off transients. The only negative aspect to this resistor is the increased switching loss resulting from slower operation of the power FETs. Commonly, this resistance is small and the increase in switching loss is well worth the trade for stable operation and improved reliability. However, there is another solution that allows both the minimal switching loss of a small gate resistance and the elimination of oscillatory behavior, which is offered in an Advanced Power Technology application note: "It has been found that a ferrite bead combined with a resistor on each MOSFET gate eliminates parasitic oscillation while minimizing switching losses. In fact, adding a ferrite bead is more effective than using gate resistance alone because the impedance of the ferrite bead is directly proportional to

frequency." As the parasitic, high-frequency oscillations that plague parallel-operated MOSFETs are in the 100 MHz to 200 MHz range, the ferrite bead is an ideal addition to the 'low-impedance loop' in Figure 33. The ferrite bead allows the much lower frequency gate signal to pass through at a much lower impedance than seen by the high-frequency oscillations. From the Advanced Power Technology application note, a reduction in switching loss is observed by reducing the individual gate resistor from 4.3 Ω to 1 Ω while the parasitic gate oscillations are also eliminated by adding a ferrite bead in series with the 1 Ω resistor [11]. One downside to the inclusion of a ferrite bead to the gate network, and therefore inside the power module, is the inability to obtain beads rated for high temperature (>150°C).

3.2.4 *Kelvin-Source Resistors*

To provide another example of unfavorable performance in the parallel operation of MOSFETs, consider the source of one of the devices in the high-side position of a traditional half-bridge power module. If this MOSFET turns on before its paralleled peers, the source of that device will transition to the drain voltage, which is commonly the bus voltage, $+V_{DC}$. This creates an unbalance in the high-side source node, which cannot exist and must be remedied by means of a large balancing current. The high-side is coupled with many, large wirebonds to the midpoint trace of the DBC inside the module as well as with smaller, kelvin-source wirebonds in the gate network. The problem arises when the power-source current path through the large bonds and the DBC has a similar or larger impedance than the kelvin-source current path through small bonds and sensitive, signal traces. This issue is illustrated in Figure 35 where the power-source current path is much longer than the kelvin-source current path, and in-turn exhibits a higher impedance than the kelvin-source path as well. A smaller impedance in the kelvin-source path

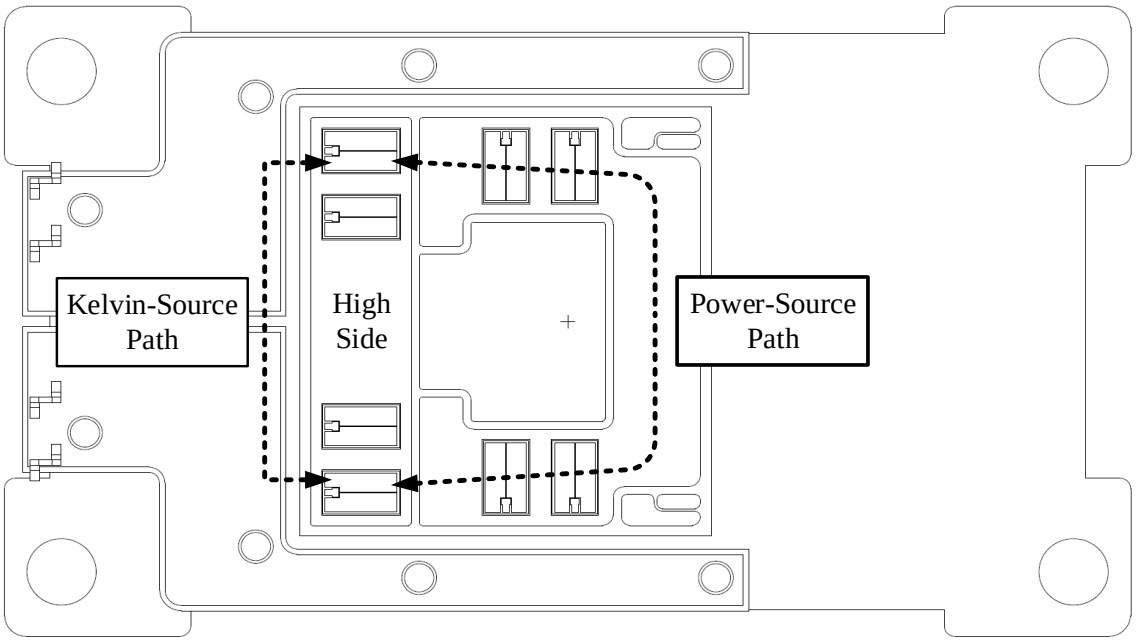

Figure 35. Kelvin-Source Current Path vs. Power-Source Current Path

allows the majority of the large balancing current due to the high-side source imbalance to flow through the gate network rather than the power-source path. The current is capable of being in the range of tens to hundreds of amps at very high frequencies, which can be devastating for the sensitive signals on the gate network. Symptoms including high-frequency gate oscillation can be observed as well as faults in the form of kelvin-source wirebonds fusing due to the extremely high current through the small bonds [12]. Fortunately, there is a simple solution to prevent the large balancing current from flowing in the kelvin-source path, which is comprised of individual source resistors per MOSFET inside the module.

The internal source resistor is effectively in series with the internal gate resistor as they both provide additional resistance to the gate driver when charging or discharging C_{GS}. The sum of the two resistors determines the R components in the RC time constant of the gate network. The source resistor can also be used to measure the kelvin-source current seen by each MOSFET. This experiment was conducted on the 62 mm power module displayed in Figure 35 to confirm

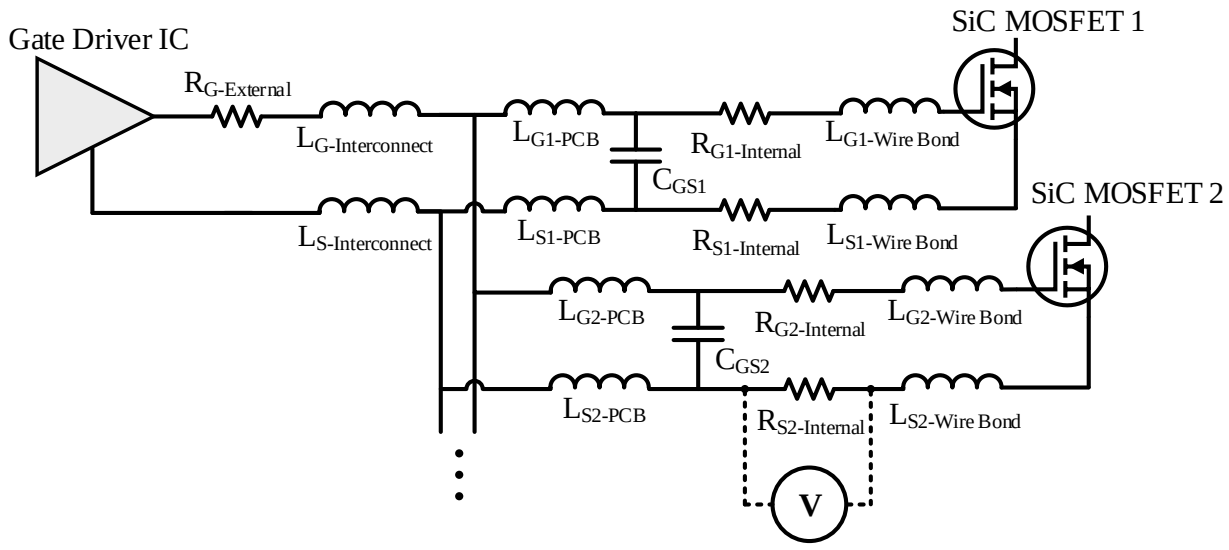

Figure 36. Kelvin-Source Current Measurement Circuit

the presence of the large balancing current. A Tektronics IsoVu, TIVH05, fiber-optically isolated voltage probe was used to measure the precise voltage across the internal source resistance. Figure 36 describes the measurement circuit with the internal parasitic components shown as well. Equation 3.14 is employed to determine the kelvin-source current seen by the MOSFET under test. In order to determine the effectiveness of the internal source resistor at preventing the large balancing current from flowing in the gate network, a small source resistor of 0.1 Ω and a larger source resistor of 1 Ω are used in the experiment.

$$I_{Source-M_x} = \frac{V_{Pre-R_{Sx}} - V_{Post-R_{Sx}}}{R_{Sx-Internal}} \tag{3.29}$$

After the experiment is conducted, the data from the oscilloscope is plotted concurrently using Excel. The resulting waveform is shown in Figure 37. As expected, the 1.0 Ω waveform is slightly delayed in time to the 0.1 Ω waveform. The magnitude of the high-frequency ringing during the 0.1 Ω test case is substantially higher than the 1 Ω with peaks reaching greater than sixty amps and less than negative sixty amps. The 1.0 Ω source resistor effectively eliminates the current in the kelvin-source path confirming the effectiveness of the internal source resistor.

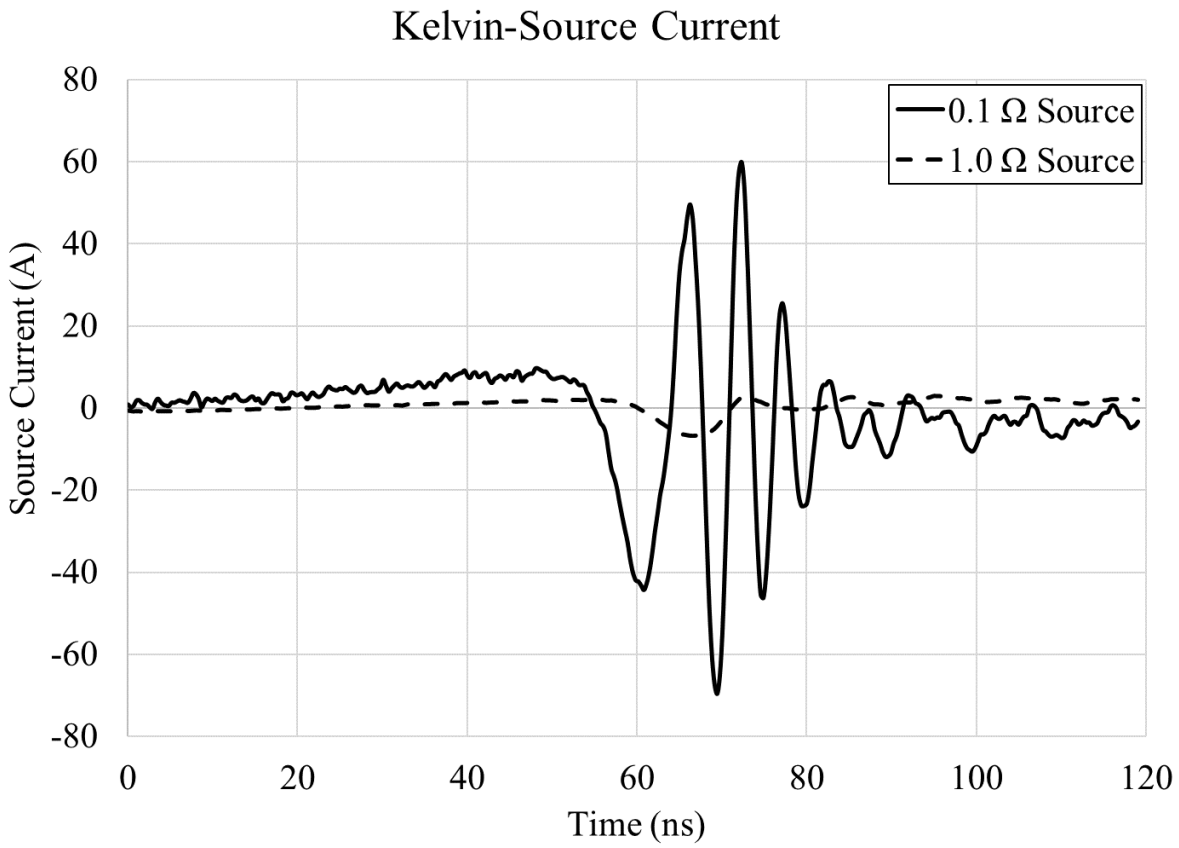

Figure 37. Kelvin-Source Current for Two Values of $R_{S\text{-}Internal}$

The only remaining factor to consider is the ratio of the internal gate resistor, $R_{G\text{-}INT}$ to the internal source resistor, $R_{S\text{-}INT}$. Fortunately, literature has provided a solution to this question as shown in Equation 3.15 and 3.16 below [12].

$$R_G = R_{G-INT} + R_{S-INT} \tag{3.30}$$

$$R_{S-INT} = \frac{1}{3} R_G \tag{3.31}$$

The source resistance is recommended to be one-third of the sum of the internal gate resistance and the source resistance. Therefore, for a 15 Ω total gate resistance, the internal gate resistance is 10 Ω while the source resistance is 5 Ω.

Using the parasitic values obtained in Chapter 2, a SPICE model of the gate network was developed in this chapter and was used to analyze four pertinent issues in WBG-based power modules including internal gate resistance for damping voltage transients at the gate of each device, differences in switching loss between paralleled devices due to propagation delay, high-frequency oscillations on the gate due to low-impedance paths between paralleled MOSFETs, and large current equalizing through the kelvin-source signal path, which required the addition of internal source resistors.

3.3 References

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CHAPTER 4

PARAMETER VARIANCE EFFECTS

The challenges of designing a high-performance power module don't cease when the electrical, thermal, and mechanical considerations are finished; the processing and manufacturability of the product are equally as demanding. To construct an identical power module thousands of times requires close monitoring of how each material and component of the system vary between lots. For the electrical considerations, the parameter variance of importance is almost entirely governed by the SiC MOSFET, which likely portrays differences in on-state resistance, threshold voltage, and transconductance. In this chapter, the effect of a variance in threshold voltage, V_{TH}, and of on-state resistance, $R_{DS\text{-}ON}$, of the paralleled MOSFETs within a high-performance power module will be examined through simulation and experiment.

4.1 SiC MOSFET Parameters: Threshold Voltage (V_{TH})

As previously discussed in the section covering propagation delay of the gate network, the turn-on and turn-off timing of paralleled MOSFETs is incredibly important; a few nanoseconds of delay between transitions can cause a large dissimilarity in switching loss. The delay or advancement of transition timing can also originate from parameter variance in the SiC MOSFETs in the form of threshold voltage mismatch [1], [2]. If one device exhibits a marginally lower threshold voltage than its paralleled associate, it will begin to conduct drain current earlier and therefore consume higher switching loss.

This phenomenon can be demonstrated through simulation using the model created at the beginning of this chapter. First, the die-to-die inductance and resistance values are removed from the model to eliminate any effects of propagation delay between the FETs. This isolates the

Table 11. Simulated ΔV_{TH} vs. Energy Loss

ΔV_{TH}	E_{ON}		E_{OFF}		$E_{ON} + E_{OFF}$		Units
+1.500	70	17%	84	79%	154	29%	µJ
+1.250	112	27%	84	80%	196	37%	µJ
+1.000	159	38%	85	80%	244	46%	µJ
+0.750	214	51%	86	81%	300	57%	µJ
+0.500	276	65%	88	83%	364	69%	µJ
+0.250	345	82%	94	89%	439	83%	µJ
0.000	421	-	106	-	527	-	µJ
-0.250	506	120%	125	118%	631	120%	µJ
-0.500	599	142%	157	148%	755	143%	µJ
-0.750	699	166%	204	193%	904	171%	µJ
-1.000	809	192%	272	257%	1081	205%	µJ
-1.250	928	220%	366	345%	1293	245%	µJ
-1.500	1055	250%	488	461%	1543	293%	µJ

mismatch in V_{TH} to provide the difference in timing and switching performance. Next, independent DC voltage sources are added to the gates of each MOSFET with values ranging from -1.5 V to +1.5 V in 0.25 V increments. After the simulation is conducted, the drain-to-source voltage, V_{DS}, and the drain current, I_D, for each MOSFET is multiplied together to obtain the power lost during the turn-on and turn-off switching transitions. The results are displayed in Table 11 for the V_{DC} = 600 V and I_S = 330 A (20 A/die) test condition. The MOSFET in the center of the module provides the control sample and exhibits a switching loss of 527 µJ. Even comparing to the next-best V_{TH} variance of +0.25 V or -0.25 V, there is approximately a 20% decrease or increase of switching loss respectively. Examining the extremes of the V_{TH} mismatch show a difference of 150 µJ at the most positive V_{TH} to 1500 µJ at the most negative. Clearly, this difference has a massive impact on temperature disparity and module performance.

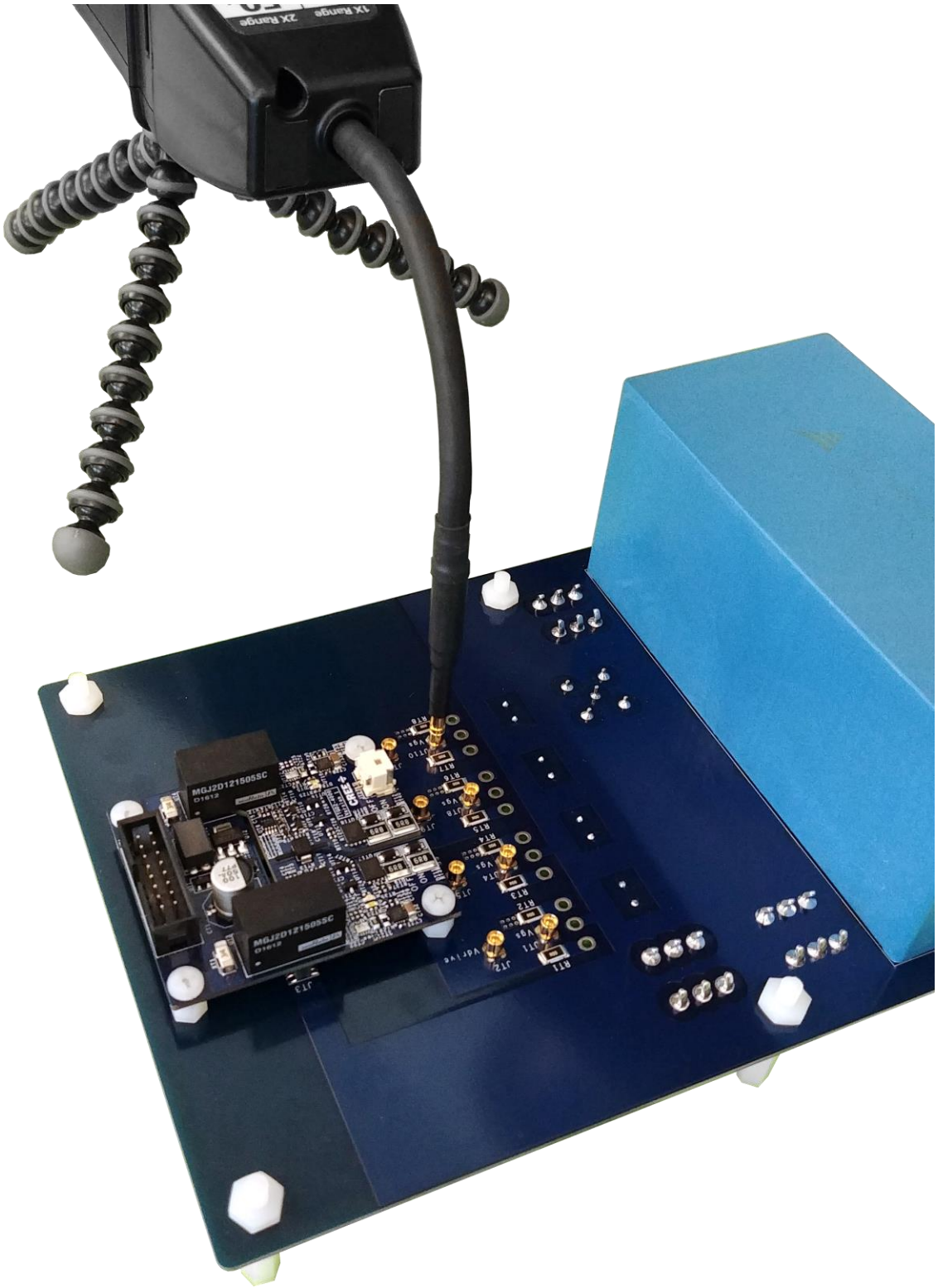

Figure 38. Parameter Variance Test Fixture for 3-Pin, TO-247 Discrete Devices

Next, the same phenomenon is verified with experimental results using precisely characterized bare die packaged into custom, discrete TO-247s. The MOSFETs used for this study are experimental MOSFETs provided by Wolfspeed, and are third-generation, 1200 V MOSFETs with very low on-state resistance. A clamped inductive load (CIL) test fixture was designed for paralleling two of the discrete devices per position in a half-bridge configuration. This test fixture is displayed in Figure 38 and consists of the power bussing PCB, an ITGD2-4011 half-bridge gate driver from Wolfspeed, and a Tektronix IsoVu optically-isolated voltage probe. The gold MMCX connectors enable measurement of the gate-to-source voltage, V_{GS}, at the terminals of the device after the individual gate and source resistors. Two 300 A Rogowski current probes are used to measure the source current of each of the MOSFETs in the low-side position.

A small sample of devices were selected out of the characterized lot, which exhibited a worst-case range of mismatch in threshold voltage and on-state resistance. With the devices packaged and soldered into the test fixture, a double-pulse test was performed on the setup at V_{DC} = 800 V, I_D = 100 A, $R_{G\text{-}Ext}$ = 0 Ω, $R_{G\text{-}INT}$ = 3, and $R_{S\text{-}INT}$ = 1 Ω. Test 1 comprised closely matched threshold voltages with a ΔV_{TH} = 0.001 V, while Test 5 boasted the worst-case ΔV_{TH} = 0.914 V. The source current waveforms of each MOSFET are shown in Figure 39 with the closely matched, Test 1, on top and the poorly matched, Test 5, on bottom. In agreeance with the simulations, the MOSFET current waveforms overlap nicely in test with ΔV_{TH} = 0.001 V, while the current waveforms are wildly dissimilar for the ΔV_{TH} = 0.914 V case. The energy loss follows suit with a difference in energy loss, ΔE_{Loss}, of 0.6 mJ, which correlates to 6% of the total energy loss for Test 1. For Test 5, ΔE_{Loss} = 4.2 mJ, which compares to 34% of the total energy loss. The results for the five tests are visualized in Figure 40.

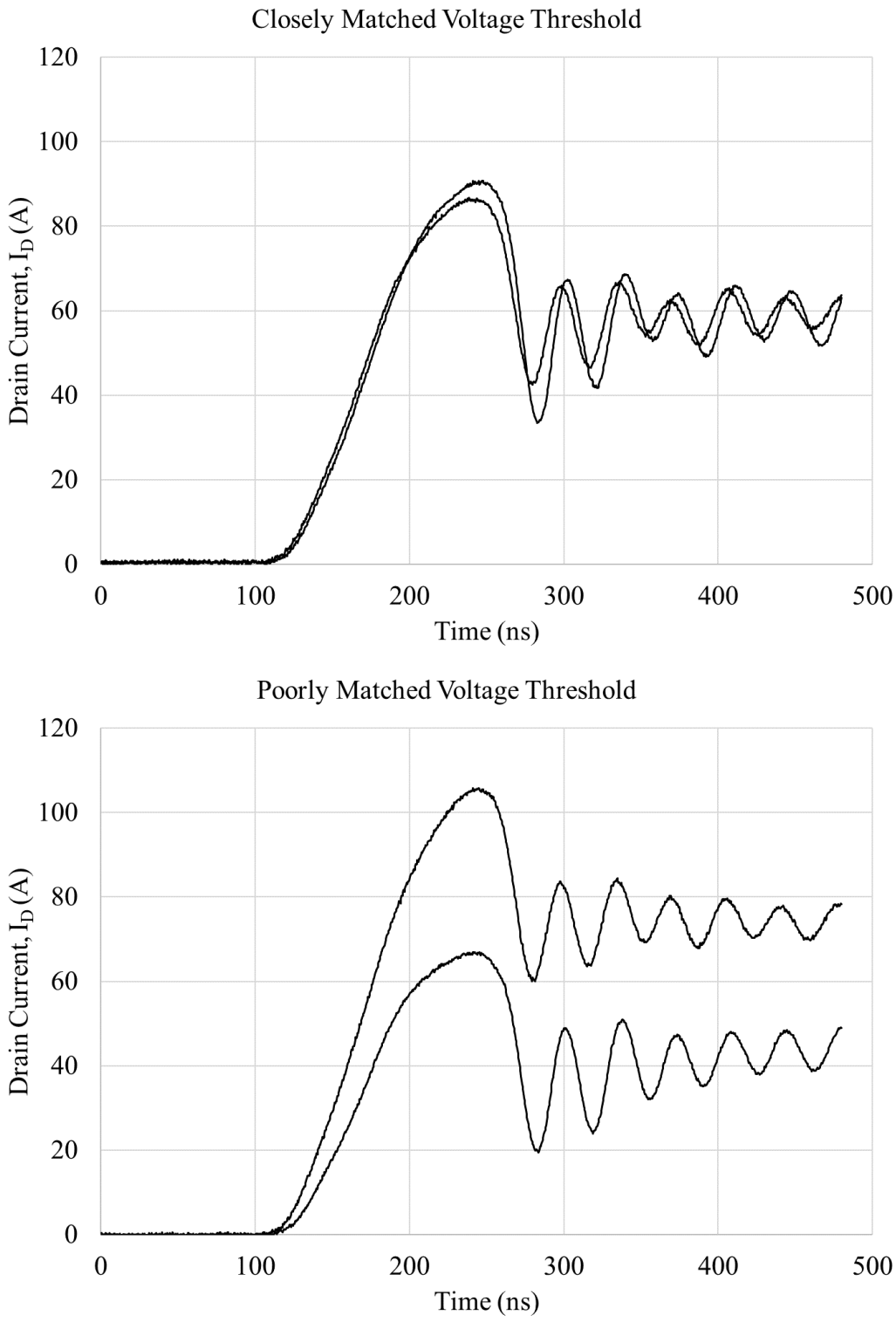

Figure 39. Measured Turn-On Current for Parallel MOSFETs with Closely Matched (Top) and Poorly Matched (Bottom) Threshold Voltages

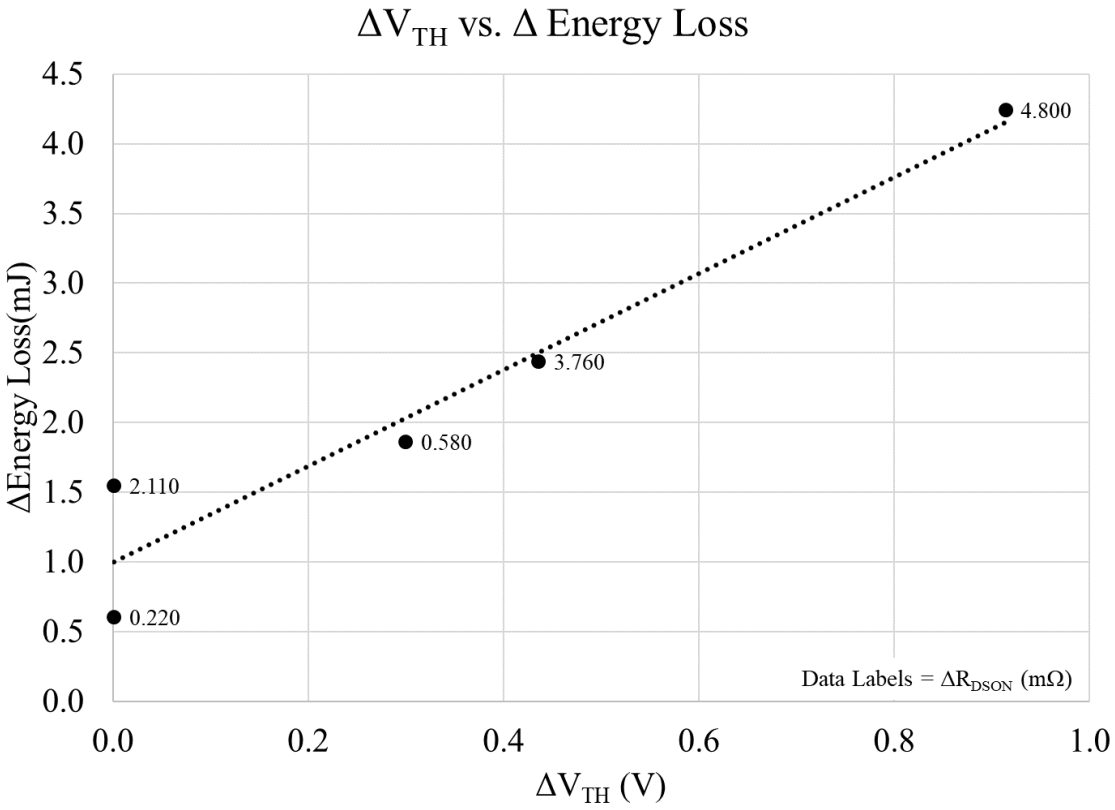

Figure 40. Measured Δ in Energy Loss vs. Δ in V_{TH} between Two Parallel MOSFETs

The five tests incorporate a wide range of threshold voltage mismatches in order to provide a clear trend between ΔV_{TH} and ΔE_{LOSS}. Predictably, the data displays an increase in the difference in switching loss between the devices ($\uparrow \Delta E_{LOSS}$) when the difference in threshold voltage increases ($\uparrow \Delta V_{TH}$). Figure 40 illustrates this trend as well as provides the difference in on-state resistance values as data labels to the right of each marker. As each parameter of variance cannot be completely isolated during physical testing of the devices, the consequence of the other variables needs to be considered. As can be seen in Figure 40, tests with equal ΔV_{TH} can exhibit different ΔE_{LOSS} when other parameter variances are present. The next section will describe the effect of $\Delta R_{DS\text{-}ON}$ on ΔE_{LOSS}.

4.2 SiC MOSFET Parameters: On-State Resistance (RDS-ON)

The different on-state resistances of paralleled MOSFETs is not commonly of concern to module manufacturers as the intrinsic positive temperature coefficient of $R_{DS\text{-}ON}$ provides natural protection for the MOSFETs with lower resistance. These MOSFETs that initially conduct more current than the others in parallel, increase in temperature and therefore exhibit a higher $R_{DS\text{-}ON}$, which balances the junction temperatures of the FETs. As stated in [2], "Differential RDS (on) will cause current unbalance and extra conduction losses as expected, but these are limited due to the positive temperature coefficient for MOSFET resistance. The thermal 'runaway' characteristic of other semiconductor technologies does not apply to MOSFETs." That being stated, this effect only applies during conduction through the MOSFET channel. Body diode conduction as well as switching loss do not behave in the same manner and actually provide a negative temperature coefficient. Also, $R_{DS\text{-}ON}$ can fluctuate switching loss by changing the turn-off current that the MOSFET must extinguish.

The experiment described in the previous subsection characterized the $\Delta R_{DS\text{-}ON}$ for the five tests, which included a range from a closely matched case of 0.22 mΩ to a poorly matched case of 4.8 mΩ for the low-$R_{DS\text{-}ON}$, experimental MOSFET. As this experiment employed a double-pulse, clamped inductive load test, there is little influence of $R_{DS\text{-}ON}$'s positive temperature coefficient as the devices do not have enough time to heat during test. As a precaution, this fact may slightly exacerbate the ΔE_{Loss} data obtained during this test. Similar to the trend uncovered in the ΔV_{TH} vs. ΔE_{Loss} plot, an increase in the difference in switching loss ($\uparrow \Delta E_{LOSS}$) is observed when the difference in threshold voltage increases ($\uparrow \Delta R_{DS\text{-}ON}$) as illustrated in Figure 42. Studying the waveforms provided in Figure 41, it can be observed that the turn-off current is dissimilar in the poorly matched case while the closely matched case is relatively uniform.

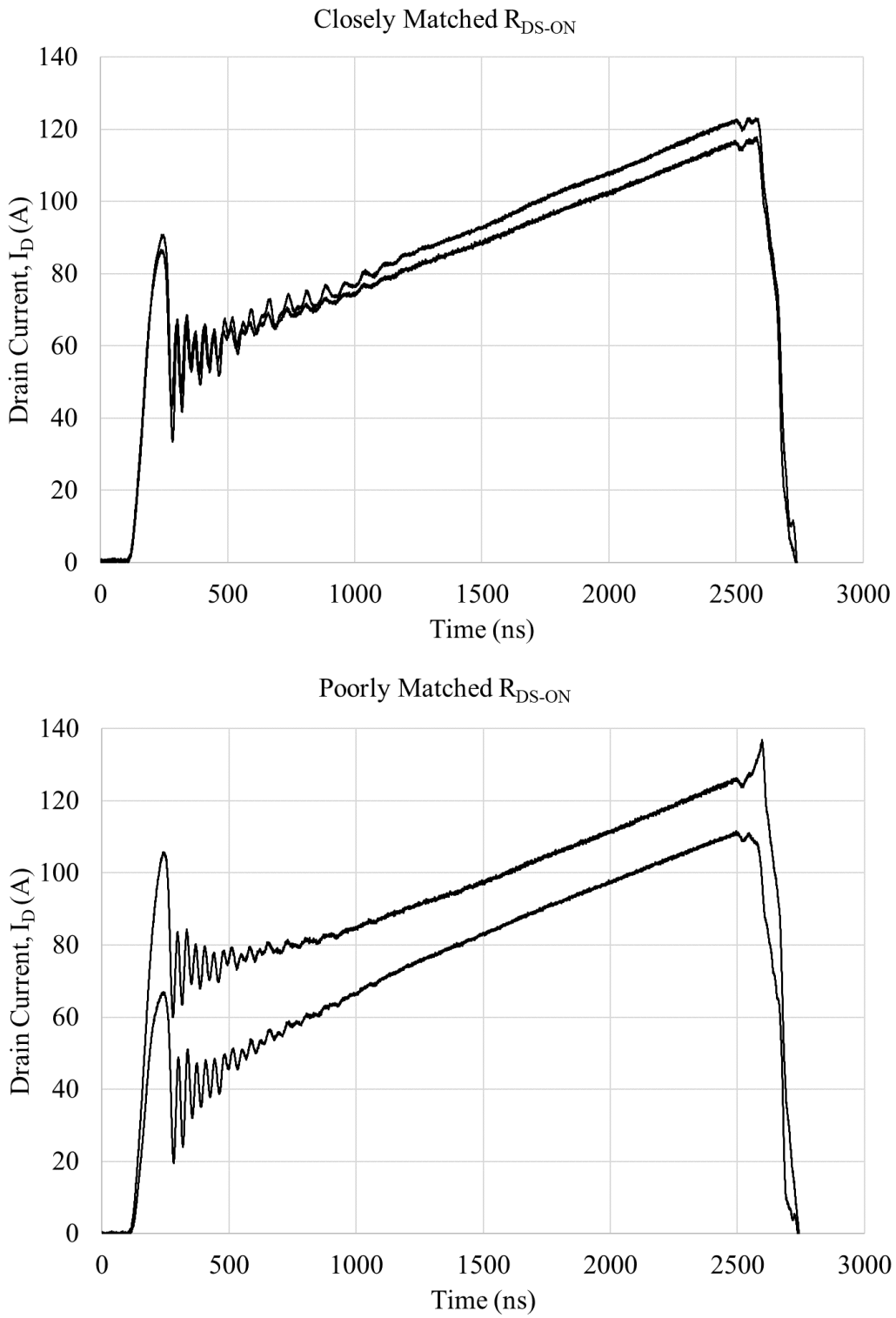

Figure 41. Measured Turn-On Current for Parallel MOSFETs with Closely Matched (Top) and Poorly Matched (Bottom) R_{DS-ON}

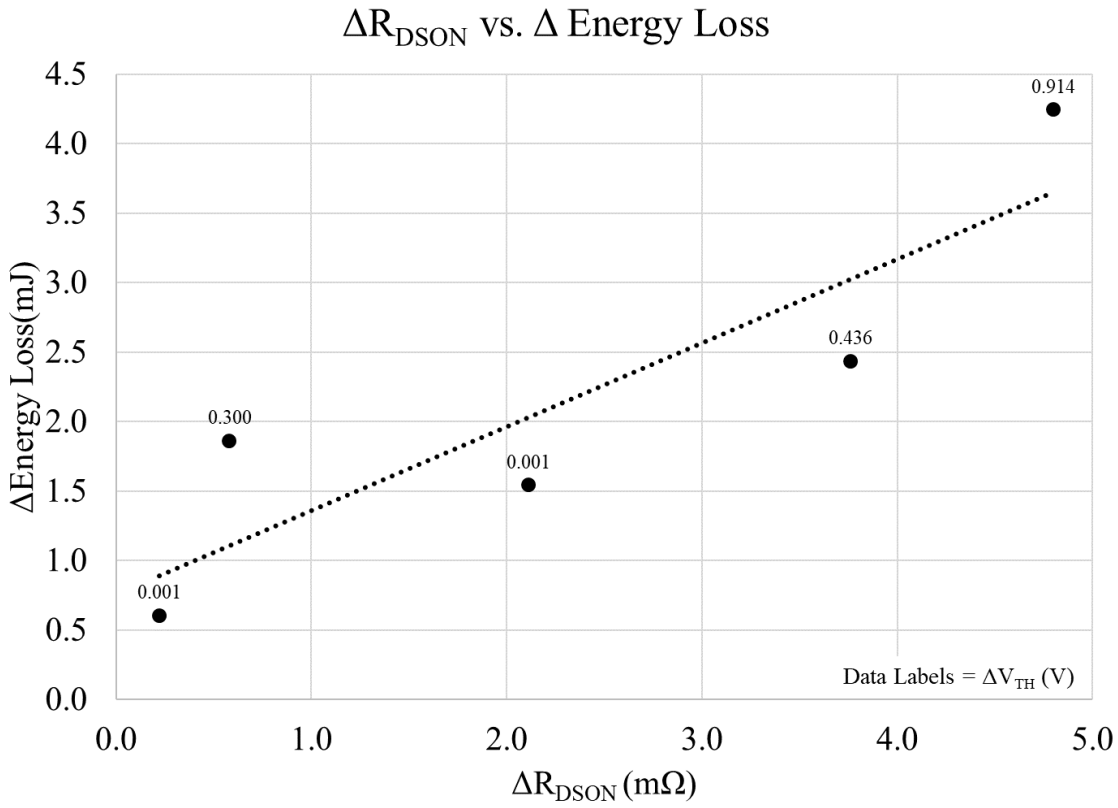

Figure 42. Measured Δ in Energy Loss vs. Δ in $R_{DS\text{-}ON}$ between Two Parallel MOSFETs

This difference in turn-off current will obviously result in higher energy loss during the off transition, E_{OFF}, but for the turn-on transition, the difference in energy loss is largely due to the difference in threshold voltage. For this reason, Figure 40 and Figure 42 display both variance parameters in this study; the main parameter is shown on the x-axis while the secondary parameter is displayed as a data label next to each point. Fortunately, the lot of die used for this experiment allowed for an isolated comparison of $\Delta R_{DS\text{-}ON}$ as there were two test cases where ΔV_{TH} = 0.001 V. At these two test conditions, the first with a $\Delta R_{DS\text{-}ON}$ = 0.22 mΩ, and the second with $\Delta R_{DS\text{-}ON}$ = 2.11 mΩ, an increase in ΔE_{LOSS} of about 1 mJ is observed with the increase of $\Delta R_{DS\text{-}ON}$. This comparison provides strong evidence to the trends described in this section; as MOSFETs exhibit larger dissimilar parameters, the loss that they observe is also increasingly dissimilar.

A difference in energy loss is extremely significant when a power electronics designer wants to take advantage of the one of the most popular advertised benefits of SiC: high switching frequency. To gain a realistic grasp on the consequences described in this section, the difference in switching loss can be multiplied by the switching frequency to determine the switching losses as shown in Equation 3.17 below.

$$P_{SW} = \left(E_{On} + E_{Off}\right) \times f_s \tag{4.32}$$

Assume a switching frequency of 40 kHz and the switching loss values measured in Test 5 with roughly 8 mJ observed by one MOSFET and 12 mJ observed by the other. The power loss due to switching seen by the first device is 320 W while the second device is 480 W using Equation 3.17. Utilizing a junction-to-case thermal resistance, R_{JC}, of a single device in a power module of 0.5 °C/W, the junction temperature of the first MOSFET is 160 °C while the second device is 240 °C. Therefore, a designer may believe that a module is operating within its safe operating area while, in fact, one MOSFET is potentially operating at a junction temperature considerably surpassing its rating. This will lead to a premature failure of the device, and likely, the entire power module will fail before its expected life time.

This chapter provides simulated and experimental evidence to support the process of sorting or binning devices by their threshold voltage and their on-state resistance for use in power modules. To create a reliable and high-performance power module, the paralleled MOSFETs must be of similar variance in order to maximize the module's current carrying capability and to guarantee a safe operating temperature of every device.

4.3 References

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CHAPTER 5

MILLER CLAMP TOPOLOGIES FOR SIC POWER MODULES

This chapter presents the theory and simulation of various Miller Clamp (MC) topologies for use with SiC power modules. A brief background on the Miller Clamp is presented followed by the investigation of three clamping techniques. The first, a gate-drive-mounted Miller Clamp, which is referred to as an external Miller Clamp, provides a baseline for what is commonly available and utilized in the industry at the time of writing. The next topology moves the clamp inside the SiC power module providing a shorter, lower impedance path for the high-frequency, Miller-charge-up current. This technique offers better performance at the cost of increased complexity and reliability concerns from routing MC gating signals and additional voltage rails into the power module. Finally, an approach for eliminating the Miller-charge-up effect and providing an equal, low-impedance path for each MOSFET inside the power module is presented.

5.1 Theoretical Background

In a half-bridge circuit, assume there is current flowing through the low-side position's anti-parallel diode. When the high-side MOSFET or IGBT turns-on, there is a reverse recovery event of the low-side device's diode, which allows the low-side device to begin blocking voltage [1]. As the voltage rises across the low-side device, a change in voltage with respect to time (dv/dt) is observed at the midpoint of the half-bridge. The parasitic capacitance found between the drain and the gate of a MOSFET, C_{DG}, or the collector and the gate for an IGBT, C_{CG}, directly experiences this dv/dt event. As the basic equation of capacitor current states, the capacitor current is directly proportional to the capacitance and to the magnitude of the dv/dt across the capacitor as shown in Equation 4.1 [2].

$$i = C_{DG} \frac{dV_{DS}}{dt} \tag{5.33}$$

The current flowing into the drain-to-gate capacitor can take two paths on its way to the source of the low-side device. It can flow through the intended off-state gate drive path including the turn-off gate resistor or it can flow directly into the parasitic gate-to-source capacitance of the low-side device. As current will take the path of lowest impedance, a large majority of this current, also known as the Miller-charge-up current, will flow into the gate-to-source capacitance, C_{GS} due to the high-impedance exhibited by the off-state driver path and the turn-off gate resistor. The charge-up current flowing into C_{GS} causes the gate-to-source voltage, V_{GS}, to rise as depicted in Figure 43.

A rise in V_{GS} during the off-state of the low-side device can be incredibly dangerous for the half-bridge circuit. If V_{GS} reaches the threshold voltage, V_{TH}, of the device, unintended turn-on can

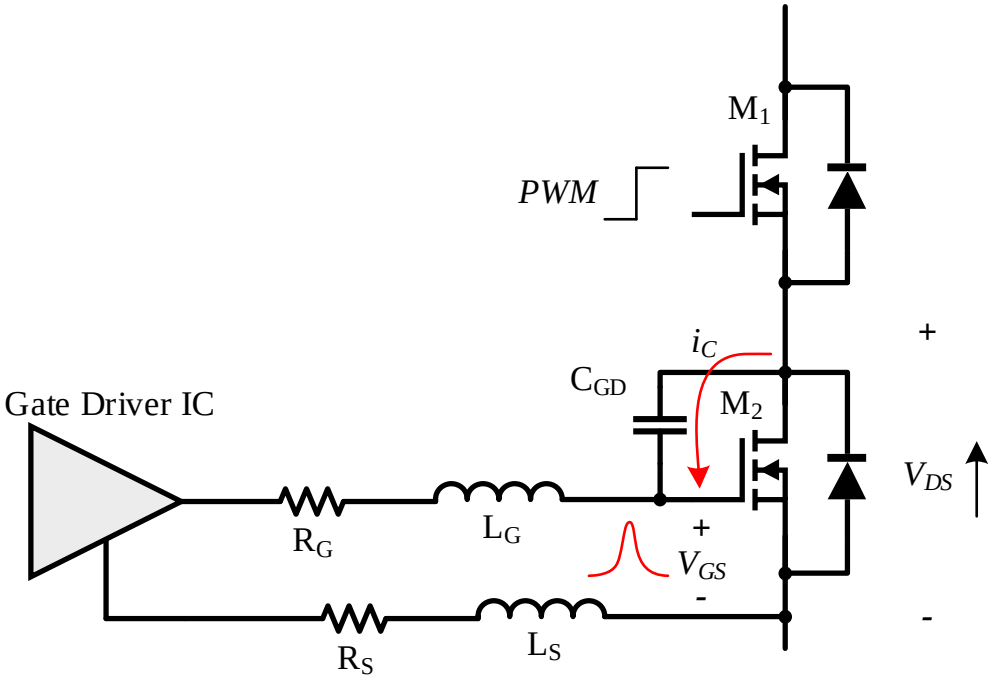

Figure 43. Miller Charge-Up Phenomenon in High dv/dt Half-Bridge Systems

occur leading to a shoot-through event in the half-bridge likely causing catastrophic failure of the system. This problem is compounded with the invent of wide bandgap semiconductors capable of switching at considerably faster speeds than Si IGBTs. The dv/dt experienced by C_{GD} is commonly much larger in SiC MOSFETs than in Si half-bridge systems [3]. This creates an important issue that much be addressed during the design of the SiC MOSFET and power module [2, 4, 5].

In Equation 4.1, it can be observed that the size of the drain-to-gate capacitance directly governs how much Miller-charge-up current will flow into the gate network. From a MOSFET designer's perspective, it is most beneficial to minimize this capacitance as much as possible. Moreover, the same equation also applies to the charging of the gate-to-source capacitance, and therefore, $V_{GS.}$ A larger capacitance value for a given Miller-charge-up current will provide a smaller dv/dt across C_{GS}. For this reason, it is most beneficial to create a MOSFET with a large C_{GS}. Therefore, one figure of merit that can be used to determine a SiC MOSFET's susceptibility to Miller-charge-up is the C_{GS} to C_{GD} ratio, which will further be referred to as the Miller Capacitance Ratio (MCR) [5]. In Table 12, the MCR value for three common SiC MOSFETs from Wolfspeed are provided. It is easily observed that a significant improvement in the SiC MOSFET's susceptibility to Miller-charge-up was accomplished between the Generation 2 and Generation 3 MOSFETs. The MCR value of the 900 V, 10 mΩ MOSFET is just over twice the MCR value of the 1200 V, 25 mΩ

Table 12. Miller Capacitance Ratio for Three Common SiC MOSFETs

Parameter	CPM3-1200-0013	CPM2-1200-0025	CPM3-0900-0010	Units
C_{ISS}	6,909	2788	4500	pF
C_{RSS} (C_{GD})	22	15	12	pF
C_{GS}	6,887	2773	4488	pF
C_{GS}/C_{GD}	313	185	374	-

MOSFET [6, 7, 8]. For this reason, the SiC MOSFET model of the Generation 2, 25 mΩ will be used in this chapter. The Generation 3 MOSFETs do not exhibit enough Miller-charge-up with the proposed gate and source resistors from the previous chapter to warrant a meaningful investigation on this subject.

In order to determine the effectiveness of the three various Miller Clamp topologies outlined in the introduction, a double-pulse, clamped-inductive-load test in SPICE will be conducted on each of the topologies. An example of the test is portrayed in Figure 44 and Figure 45, which will suffice as the control for the experiment as there is no Miller Clamp present in the gate network. As can be seen on the second turn-on pulse at roughly 420 A, there is a large voltage spike on the high-side V_{GS} plot (top plot), which is induced by the Miller-charge-up effect. During this time, the low-side device is turning on, and the voltage at the midpoint is falling rapidly causing a large dv/dt across the high-side MOSFET as described previously.

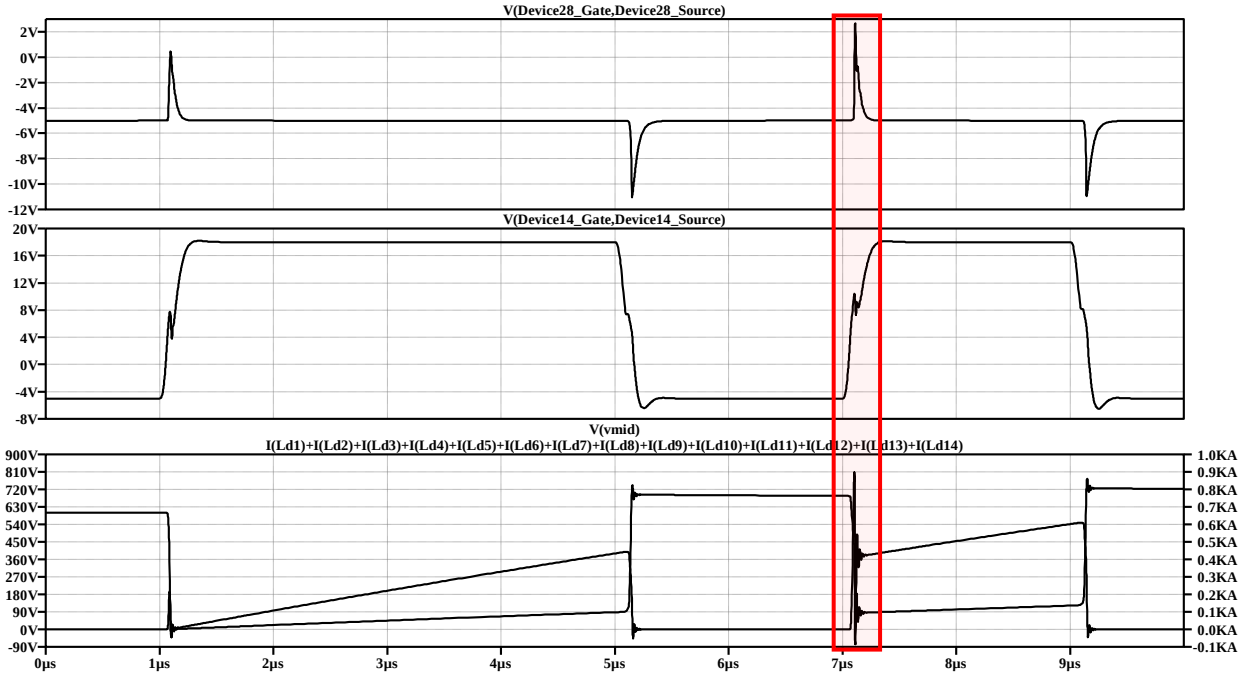

Figure 44. Double-Pulse Testing with No Miller Clamp

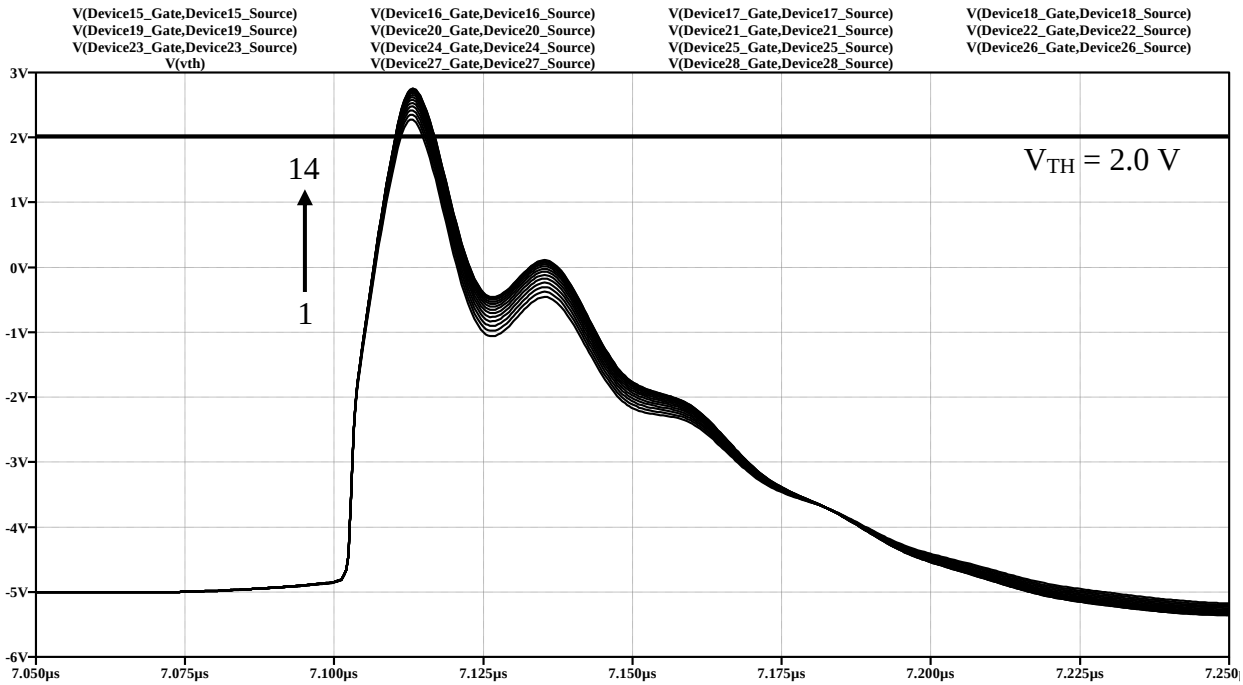

Figure 45. High-Side V_{GS} with No Miller Clamp During Low-Side Turn-On (Control)

Figure 45 provides a zoomed look into the charge-up spike between the gate and source of each of the fourteen paralleled MOSFETs inside the SiC power module. The MOSFETs farther from the gate driver's connection to the module exhibit a larger magnitude of V_{GS} during charge-up. This is expected as the impedance seen by the farther positions is greater than the closer positions forcing more of the Miller-charge-up current to flow into the C_{GS} of the device as opposed to the intended off-state gate drive path. With the Generation 2, 25 mΩ MOSFET and the proposed values for $R_{G\text{-}INT}$ and $R_{S\text{-}INT,}$ the charge-up of V_{GS} far exceeds the rated threshold voltage of the device at 175 °C. This result mandates a solution to guarantee reliable operation of the SiC power module at its rated junction temperature. As stated by Andrew Lemmon, et al., "In the case that the reduction of switching speed is accomplished by increasing the value of the series gate resistance, this solution also increases the risk of Miller turn-on (and shoot-through in half-bridge circuits). Clearly, better techniques are needed to reduce the susceptibility of applications to self-

sustained oscillation without trading away the low-loss switching behavior that is one of the major attractions of WBG devices." [5] One of these better techniques is the Miller Clamp, which is investigated thoroughly in the next three sections.

5.2 External Miller Clamp

To begin the investigation of various Miller Clamp topologies, the common external Miller Clamp is examined. This circuit arrangement is often found integrated into an all-in-one gate driver IC that provides isolation, fault reporting, gate signal buffering, and an active clamp. When the Miller Clamp is located inside the gate driver IC, an alternative off-state path is created around the turn-off gate resistor. This clamp topology provides practically no gate-network impedance reduction, and is only beneficial for systems with high turn-off gate resistance. The equivalent schematic for this arrangement is visualized in Figure 46. The external Miller Clamp may also be a discrete MOSFET that is located on the gate driver PCB with discrete logic circuitry for control and actuation. As shown in the figure, the difference between the red current path, exemplifying no MC, and the blue current path, demonstrating an external MC, is simply $R_{G\text{-}External}$ or the turn-off

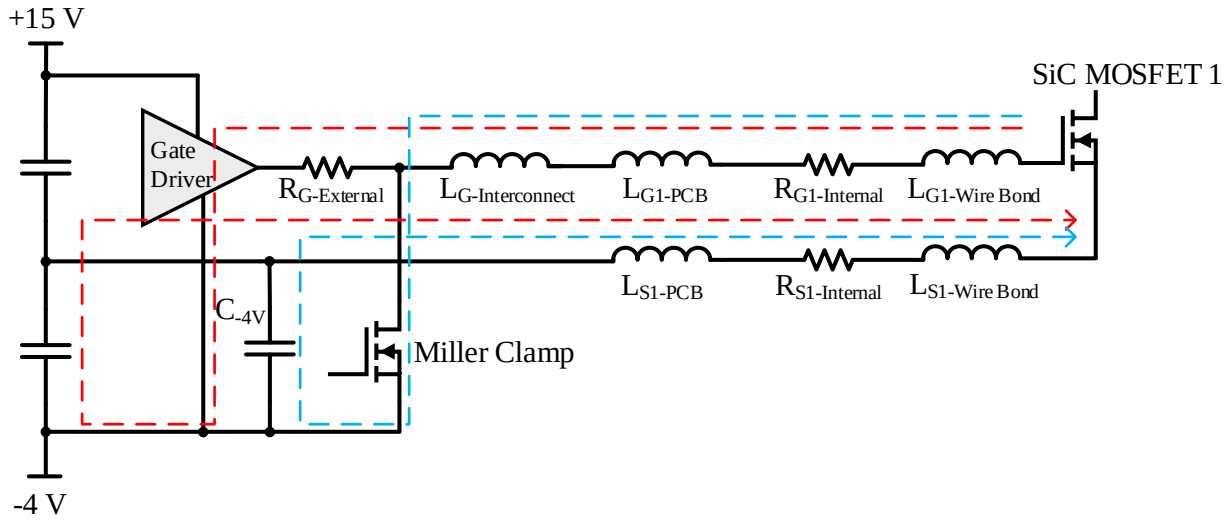

Figure 46. Schematic of External Miller Clamp Illustrating Difference in Current Paths

resistor if separate turn-on and turn-off resistors are present. For systems utilizing low gate resistance or low turn-off resistance, the external Miller Clamp provides little benefit.

To prove this theory, a simulation is conducted to determine the tangible benefit of the external MC. First, a clamping MOSFET is selected; moreover, a low-on-state resistance and low-inductance-packaged MOSFET is desired. STMicroelectronics offers a 30 V, 21 mΩ FET in a SOT23-6 package, which meets all of the requirements for this application and will be utilized as the active clamp device for all of the following SPICE simulations [9]. ST also provides a SPICE model of the part as well as the parasitic inductances of the package. This MOSFET is inserted into the gate-network model from the previous chapter in the location of the external Miller Clamp for the high-side of the power module. Conducting the simulation results in Figure 47, which portrays the Miller-charge-up that occurs on the high-side V_{GS} during the turn-on of the low-side position at roughly 420 A. As in the control waveform, the paralleled SiC MOSFETs that are

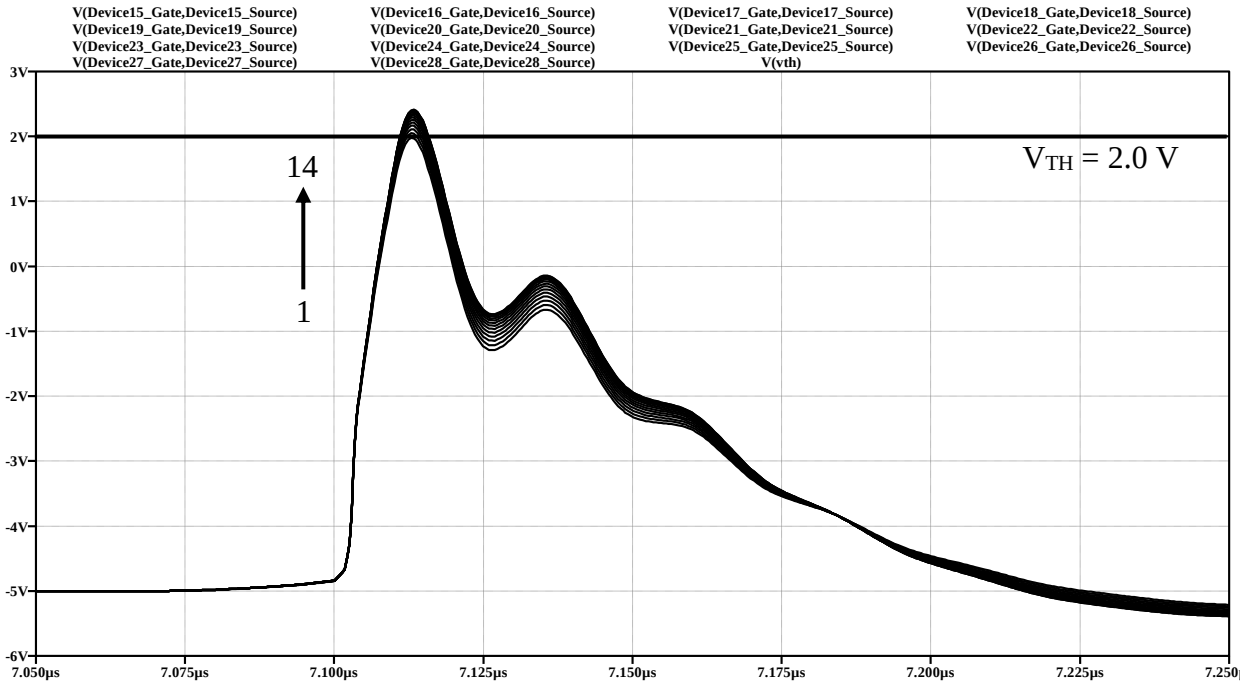

Figure 47. High-Side V_{GS} with External Miller Clamp During Low-Side Turn-On

farthest from the gate driver's connection to the module exhibit the largest magnitude V_{GS}. Comparing the waveform in Figure 47 to the control in Figure 46, it is clear that very little benefit is exuded by the external Miller Clamp. This is due to the external gate resistance in this experiment being zero excluding small parasitics in the model. Operating at this extremely low gate resistance is enabled due to the optimizations of the previous chapters that provide sufficient damping of the power module through the internal gate and source resistors. For this reason, the external Miller Clamp is rendered practically useless, and a more advanced topology is required.

5.3 Internal Miller Clamp

The second topology to be examined is referred to as the internal Miller Clamp, which denotes that the clamping MOSFET is located inside the SiC power module. The advantage of this Miller Clamp method is the reduction of parasitic inductance in the clamping path compared to the standard, external Miller Clamp as illustrated in Figure 48. As before, the gate-driver-mounted, external gate resistor is bypassed, but for the internal clamp's case, the inductance produced from the gate driver's connection to the power module is bypassed as well [4]. The disadvantage of this

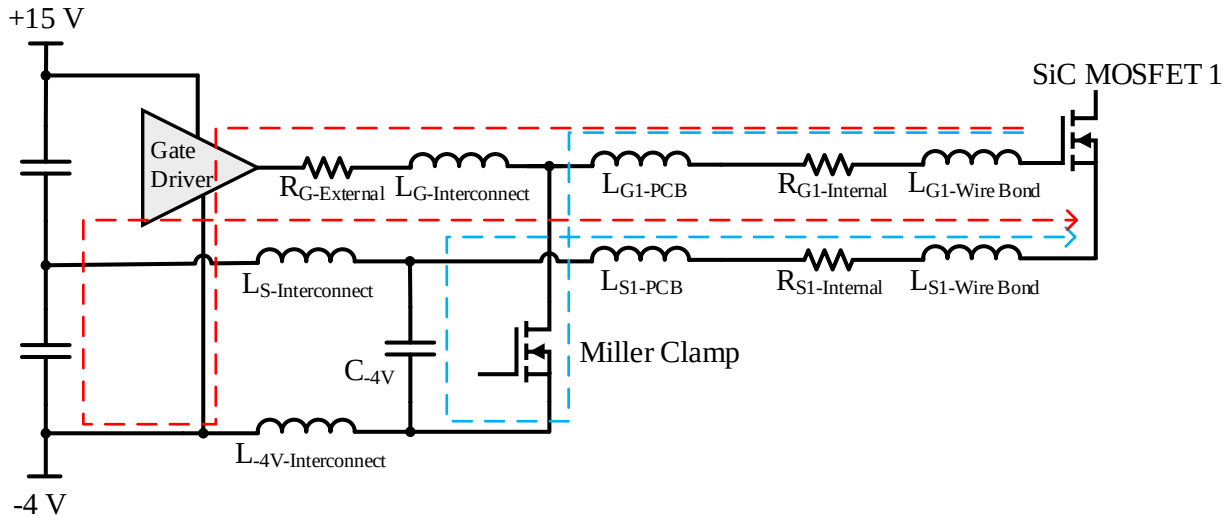

Figure 48. Schematic of Internal Miller Clamp Illustrating Difference in Current Paths

method is that the Miller Clamp's gating signal and the negative gate voltage rail, $-V_{SS}$, must be routed into the power module. There is also the reliability concern of the clamping Si MOSFET being damaged and rendering the entire power module useless.

The internal Miller Clamp is added to the SPICE simulation of the gate network and the double-pulse test is conducted. The resulting waveform for the V_{GS} of each MOSFET position is portrayed in Figure 49. Similar to the external Miller Clamp, the position closest to the clamp, position 1, observes the greatest benefit from the clamp and experiences the lowest peak voltage. For the internal clamp case, the first three positions do not peak above the threshold voltage of the device, which indicates that the internal clamp offers better performance than external clamp. However, the internal clamp is not an adequate solution for guaranteeing that all of the positions remain in their safe-operating-area below the threshold voltage. Yet again, another Miller Clamp method must be explored.

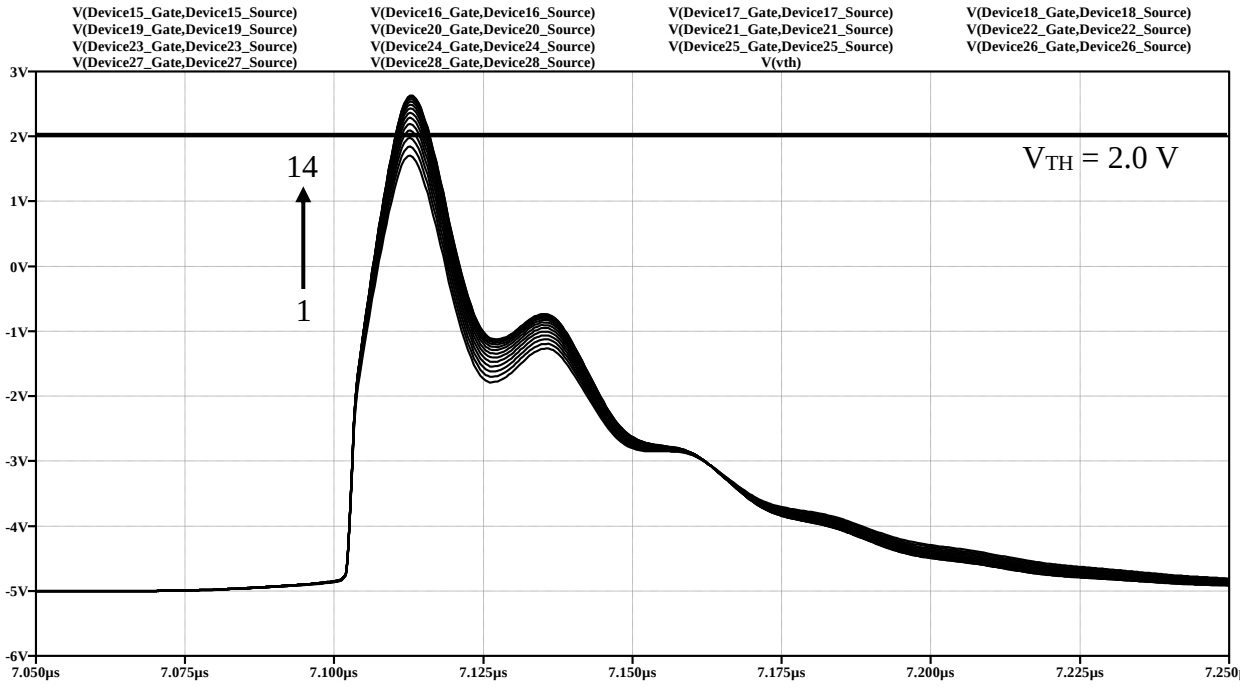

Figure 49. High-Side V_{GS} with Internal Miller Clamp During Low-Side Turn-On at 420 A

5.4 Individual Miller Clamp per MOSFET Position

The final Miller Clamp topology, the individual Miller Clamp, denotes a clamping MOSFET per SiC power MOSFET inside the power module directly next to the wirebonds that connect the gate network PCB to the devices. This strategy provides the highest reduction of parasitic inductance in the clamping path as well as the removal of the relatively high-valued internal gate and source resistors, which dramatically reduces the off-state impedance. Figure 50 illustrates the difference in the standard turn-off current path through the gate driver in red and the individual Miller Clamp current path in blue. There must also be an individual ceramic, bypass capacitor per device inside the module to provide a low-impedance path to $-V_{SS}$. With this topology, the only impedance seen during the clamped off-state is the parasitic inductance and resistance of the wirebonds from the device to the PCB, the ESR and ESL of the bypass capacitor, and the $R_{DS\text{-}ON}$ and parasitic inductance of the Si MOSFET. There is also the advantage of an evenly distributed, low-impedance clamping path at each power MOSFET in the module as opposed to a gradual increase in impedance at each position.

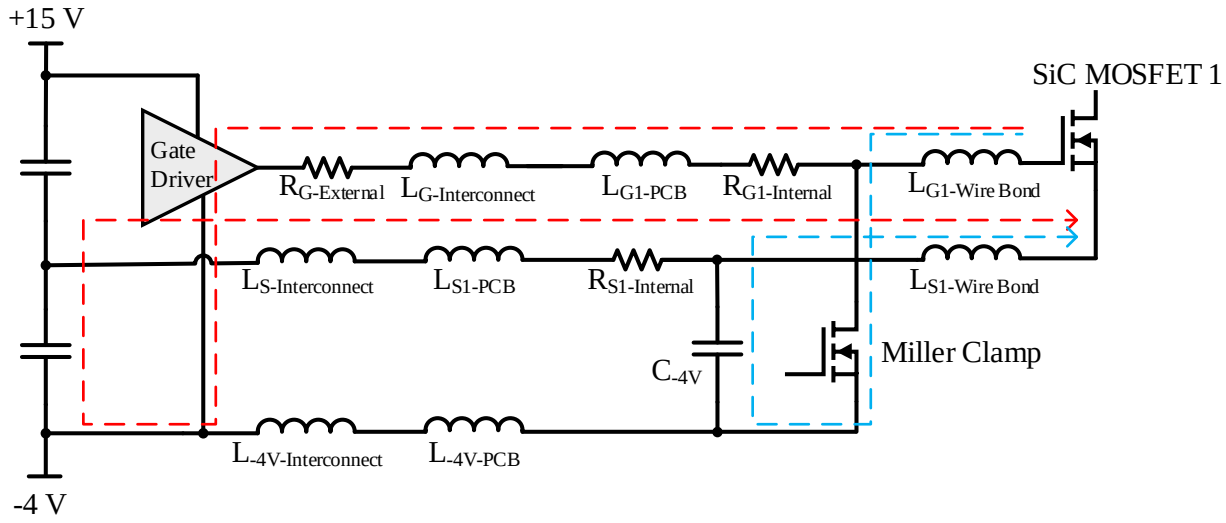

Figure 50. Schematic of Individual Miller Clamps Illustrating Difference in Current Paths

Figure 51 portrays the simulation results for in the individual Miller Clamp topology. Noticeable differences between this result and the previous two topologies include the completely overlapping behavior of all fourteen V_{GS} waveforms, which is due to the matched low-impedance off-state path of the individual clamps. Also, the V_{GS} peak remains very distant from the threshold voltage of the power devices; in fact, the V_{GS} peak does not even reach a positive value. One observation to note is the natural ringing of V_{GS} that exceeds the negative recommended operating voltage of the SiC device, which is largely due to the parasitic inductance of the clamping MOSFET interacting with the parasitic capacitances of the SiC devices. In order to minimize this ringing, a very low-inductance Miller Clamp MOSFET should be selected.

The individual Miller Clamp topology provides a solution to the fortuitous parasitic turn-on of SiC power modules with relatively low C_{DG}/C_{GS} ratios. The addition of several Si MOSFETs and ceramic capacitors inside a power module may be a large reliability concern, but the massive

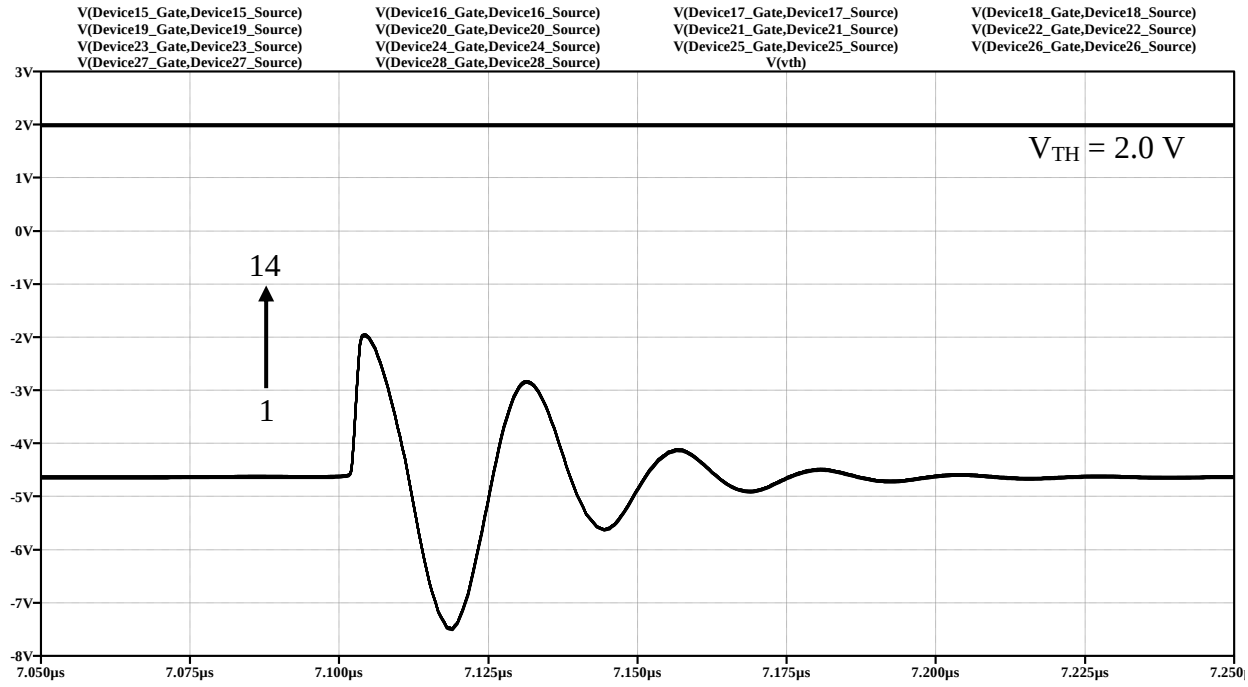

Figure 51. High-Side V_{GS} with Individual Miller Clamp During Low-Side Turn-On

reduction in Miller-charge-up from the individual Miller Clamp topology could prove advantageous for some high-performance applications that experience extremely high dv/dt.

5.5 References

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CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The main objective of this effort was to determine points of weakness in the gate network of a high-performance SiC power module and to offer remedies to these issues to increase the overall lifetime and reliability of the technology. In order to accomplish this goal, a highly accurate model of the gate network was required, which was summarized in Chapter 2 with three portions of the gate network analyzed through three different methods of parameter extraction: calculation, simulation, and measurement. Using the parasitic values obtained in Chapter 2, a SPICE model of the gate network was developed in Chapter 3 and was used to analyze four electrical issues in high-speed, WBG-based power modules including adequate internal gate resistance per power MOSFET for damping under-voltage and over-voltage transients at the gate of each device, disparity in switching loss between paralleled devices due to propagation delay, high-frequency oscillatory behavior on V_{GS} due to die-to-die interactions, and large power current equalization in the kelvin-source signal path and the addition of internal source resistors per power device. Chapter 4 provides experimental results for parameter variance between paralleled MOSFETs and outlines the consequences of mismatched threshold voltage and on-state resistance on switching loss and junction temperature. Finally, in Chapter 5, three Miller Clamp topologies were simulated and assessed for effectiveness. A solution for high dv/dt systems was provided in the form of the individual Miller Clamp internal to the power module.

6.2 Future Work

6.2.1 MOSFET Binning or Sorting Algorithm Development

As discussed in Chapter 4, the parameter variance of a MOSFET in a power module must be kept to a determined minimum value in order to maximize performance while ensuring each paralleled device remains below its rated junction temperature. This minimum variance amount must be determined as well as the complex process of binning or sorting the MOSFETs in an efficient, cost-sensitive manner.

6.2.2 Experimental Testing of the Individual Miller Clamp

The individual Miller Clamp topology needs to be verified with experimental testing. For this to occur, a gate network PCB must be designed to comprise the clamping MOSFETs, the ceramic bypass capacitors, the clamp gate signal, and the $-V_{SS}$ supply rail. This PCB will also need to provide probing points for the fiber-optically isolated IsoVu probe to measure V_{GS} at the gate of each power device.