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Very Low Power Cockcroft-Walton Voltage Multiplier for RF Energy Harvesting Applications

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Submitted by

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ABSTRACT

A device was required that could harvest the electromagnetic energy present in ambient radio frequency (RF) signals. A part of this device must convert the AC RF signal received by the antenna into a DC signal that can be used in an embedded application. Since the RF signal amplitude is small, it must first be amplified and rectified to become a usable signal. The Cockcroft-Walton voltage multiplier is a subsystem of the design which ideally converts a 100 mV AC signal coming from the antenna to a 350 mV DC signal. The output of the voltage multiplier is used to power another subsystem. At 10 MHz, the Cockcroft-Walton multiplier was able to output a DC voltage of 350 mV given an AC input signal of 140 mV. The results of the testing show verifiable proof-of-concept that the Cockcroft-Walton voltage multiplier has the potential to be used for low power RF energy harvesting applications.

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ACKNOWLEDGEMENTS

I would like to thank my team members: Cason Morse, Steven Dorch, and Houston Anderson, for their support. This voltage multiplier design would be meaningless without all the hard work they put towards the final RF energy harvesting design.

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1. INTRODUCTION

Typical applications of a Cockcroft-Walton generator usually involve very high DC voltages. They are used in high voltage devices such as x-ray machines, microwave ovens, cathode-ray tubes, air ionizers, and particle accelerators. Generally, a Cockcroft-Walton voltage multiplier is used when a high DC voltage is needed but the power supply is a low voltage AC signal with a frequency of 50 or 60 Hz. For the purposes of this project, a Cockcroft-Walton multiplier will need to be designed to work at a very low voltage and a very high frequency. Although the basic principles remain the same, these alterations create significant challenges when designing a Cockcroft-Walton multiplier for RF energy harvesting applications.

The voltage amplifier discussed in this paper is part of a larger circuit intended to harvest and store energy from ambient electromagnetic signals in the radio frequency (RF) band. These frequencies include signals from AM and FM radio stations, VHF and UHF television broadcasting, as well as Wi-Fi communications. The energy harvesting device will store the energy captured from RF signals in a storage device, which can then be used to power a wide range of remote sensors or other passive electronic devices. For example, this device would allow the placement of a temperature sensor in a remote location, which uses the stored energy to wirelessly transmit temperature information on a regular basis. The benefit this device has over other remote sensors is its ability to recharge itself using the ambient energy contained in electromagnetic signals. The RF energy harvesting device eliminates the need to change batteries, allowing sensors to be placed in more exotic locations.

The RF energy harvesting device first uses an antenna or antenna array to convert the ambient radio signals into an AC voltage signal. After going through an impedance matching network, the AC voltage will be rectified and pre-amplified by a modified Cockcroft-Walton voltage multiplier. This signal will then be further amplified by a DC-DC step up converter in the form of a charge pump. Afterwards, the higher voltage DC signal will be used to charge a bank of supercapacitors. which act as the energy storage device to used to power whatever load is connected to the device.

The main challenge to overcome when designing this device was the low power densities of the RF signals. The Federal Communications Commission states the protected service area of commercial FM radio stations covers areas with at least 60 dBμ received signal strength [1]. This is equivalent to an electromagnetic field with an electric field strength of 1.0 millivolts per meter. In other words, as long as the RF harvester is placed in a location within the intended broadcast range of the radio station, it is guaranteed to receive a signal of at least 1.0 millivolts per meter. Research into local radio stations led to the conclusion that a target frequency of 103.9 MHz would yield the best results for a harvester with a single antenna. This means the voltage produced by a single quarter-wave monopole antenna could be as low as 0.75 millivolts. However, this is a worst-case scenario. A spectrum analyzer was used to measure the power received from a 0.75 meter monopole antenna. At a frequency of 103.9 MHz, the antenna was able to receive 0.1 mW of power. Assuming the antenna had a characteristic impedance of 50 Ohms, the resultant voltage would be 71 mV. This will be the target input voltage to the voltage multiplier.

Hardly any DC-DC step-up converters have an extremely low minimum input voltage. Of those that do have low minimum requirements, most are still not low enough to connect directly to a rectified antenna signal which has not been amplified. The topic of this paper, the modified Cockcroft-Walton voltage multiplier, is one of the most critical components of the RF energy harvesting device. The rectification and pre-amplification of the antenna's voltage signal is necessary before forwarding the signal to a better DC-DC step-up converter.

2. THEORETICAL BACKGROUND

The most basic form of the Cockcroft-Walton voltage multiplier is the single-stage voltage doubler seen in Figure 1. When source voltage v_s is on its negative peak, diode D1 is forward biased and capacitor C1 gets charged to the peak source voltage V_m. When using ideal diodes, there will be

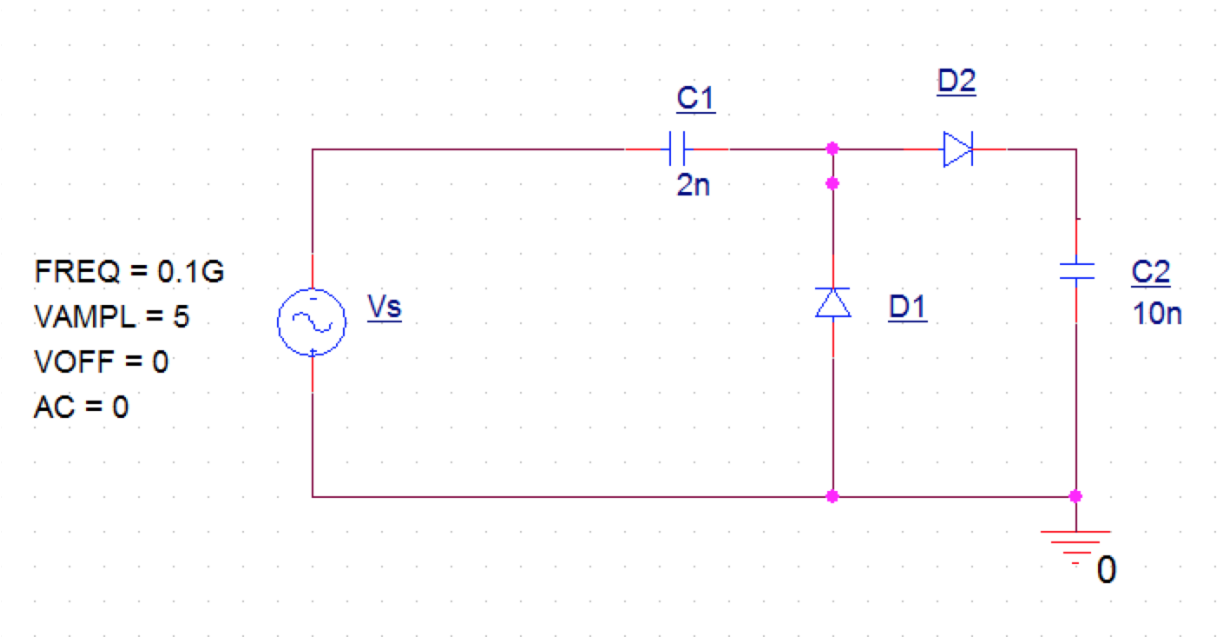

Figure 1 – Voltage Doubler Schematic

no voltage differential across capacitor C2, so there will be no stored charge. On the positive half cycle, the peak voltage from the source is now in series with the voltage differential across capacitor C1, so they add together. Diode D1 is now reverse biased with a voltage difference of twice the magnitude of the peak source voltage. Diode D2 and capacitor C2 work to reduce the ripple voltage of the output waveform. Ideally, this creates a voltage differential across capacitor C2 equal to twice the magnitude of the peak source voltage. This theory assumes ideal diodes and that the capacitors charge near-instantaneously. In reality, it will take several cycles for the voltage across C2 to reach its peak at $2V_m$.

In theory, more stages can be added to create a voltage tripler, voltage quadroupler, etc. In practice, however, it is not recommended to go beyond 12 stages [2]. Adding more stages not only slows the charge time, but it also reduces voltage regulation by increasing output ripple. Increasing the number of stages increases the output DC voltage, but it also incurs more losses, resulting in less overall power transferred to the load. These problems will be examined in the next section.

The Cockcroft-Walton voltage multiplier design is ideal because it relies only on passive components. This design eliminates the need for active switching components commonly seen in rectifiers and boost converters. The switching components seen on these types of devices typically require some separate power supply to regulate the timing of the switch. Switching regulators are more efficient than passive power regulation, however, the power supplied by ambient RF signals alone is not enough control any switch-mode power regulators. Thus, it is necessary for the Cockcroft-Walton voltage multiplier to use only passive components. Cockcroft-Walton design allows the input signal to act as the power supply to the entire circuit.

3. CIRCUIT DESIGN AND ANALYSIS

3.1 Hardware Selection and Design Considerations

The output of the voltage multiplier is connected to a charge pump. Finding a charge pump that could be implemented in the final design of the RF energy harvester was difficult; the charge pump must output at least 1.2 volts, could not use an external power supply, and it had to have a very low minimum input voltage. The charge pump used in the final design uses the input signal as its power source and has a minimum input voltage of 350 mV. This is the target output voltage of the modified Cockcroft-Walton voltage multiplier. The datasheet of this part [3] provides the $V_{in} - I_{in}$ characteristics of the device. At $V_{in} = 0.35\ V$, the datasheet provides a typical input current of $74\ \mu A$. At minimum operating conditions, the equivalent resistance of the component is approximately 4.7 kΩ.

To summarize, the RF energy harvesting device requires a circuit which can convert an AC signal with a peak of 70 mV (worst case scenario) to a 350 mV DC signal when connected to a 4.7 kΩ load. Major design considerations include: power consumption, output ripple voltage, input impedance, and cost-efficiency.

The main challenge in modifying a typical Cockcroft-Walton voltage multiplier for a low voltage, high frequency application is the voltage drop across the diodes. A typical silicon diode will have a forward voltage drop of about 700 mV while forward biased. This is an unavoidable result of silicon pn-junctions. Germanium diodes fare somewhat better with an approximate 300 mV forward voltage drop [4, pp. 187][5, pp. 204]. The forward bias voltage drops of these types of diodes are too high to support extremely low voltage applications. Schottky Diodes promise a

much better alternative. Due to their metal-semiconductor contacts, as opposed to semiconductor-semiconductor contacts, Schottky diodes can have a forward voltage drop as low as 120 mV. In addition, Schottky diodes typically have much faster reverse-recovery times [6, pp. 70]. This allows Schottky diodes to work at very high frequencies, which is expected for the RF energy harvester. A Schottky diode was found with a forward voltage drop of 120 mV at 10 mA [7]. If the current through the diodes is kept under 10 mA, the forward bias voltage drop can potentially be kept under 100 mV. In high voltage Cockcroft-Walton voltage multipliers, the diodes need to be properly rated for peak forward surge current. In this RF energy harvesting application, it is unlikely that the peak forward surge current will exceed the chosen diode's rating of 5 A.

Capacitor selection is also important when designing a Cockcroft-Walton voltage multiplier. Proper capacitor values can dramatically reduce output ripple voltage and charge time. One of the best capacitor sequences is when they are in arithmetic progression [8, Case 3]. The size of the capacitors used in a Cockcroft-Walton voltage multiplier are inversely proportional to the frequency of the input signal [9][10]. An input signal of 100 MHz would require capacitors in the 1 nF to 10 nF range. The final circuit design implemented capacitors in arithmetic sequence starting from the last capacitor at 1 nF, and adding 1 nF for each previous stage, i.e. the next-to-last stage will have a capacitance of 2 nF and the one before it would have a 3 nF capacitor.

3.2 Topology

The most significant design consideration is the topology of the circuit. How many stages should the voltage multiplier have? Too few stages would result in an output voltage that is too low to power the charge pump. Too many stages would create a very large output ripple voltage which would harm the efficiency of the charge pump. It is also important to consider the incremental cost-efficiency for each stage added. The diodes to be used for the final circuit are cost about fifty cents per diode. The capacitors cost nearly $5.00 each. Their high costs are due to their high frequency rating and low equivalent series resistance, inductance, and capacitance. It is just as important to keep the cost of the project low as it is to have a high efficiency. These design trade-offs led to the conclusion that the voltage multiplier should be designed for a gain of 8 V/V.

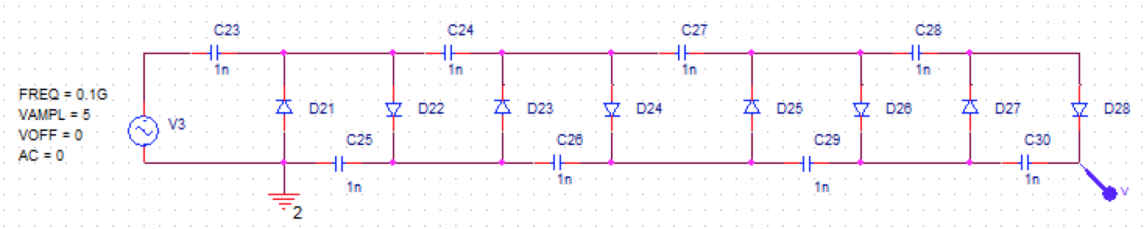

Figure 2 – Eight Stage Cascade Multiplier with Uniform Capacitance

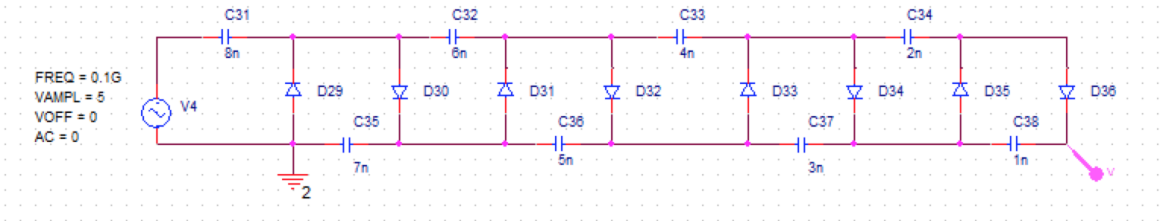

Figure 3 – Eight Stage Cascade Multiplier with Arithmetic Capacitance

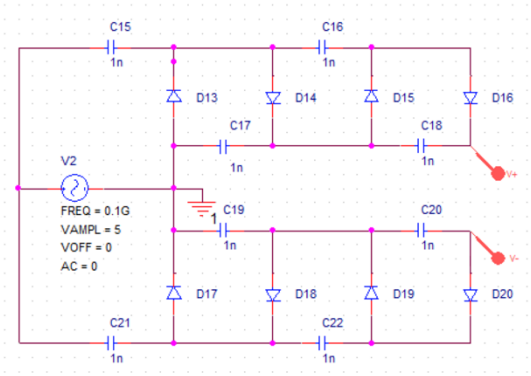

Figure 4 – Four Stage Differential Multiplier with Uniform Capacitance

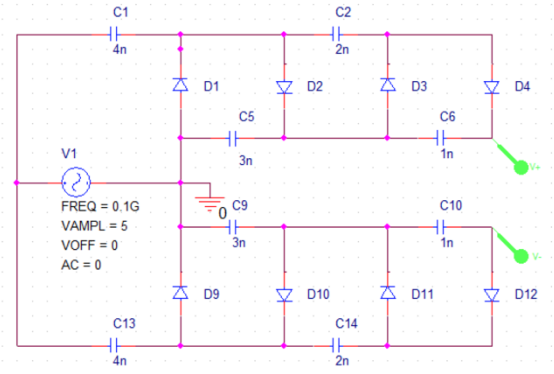

Figure 5 – Four Stage Differential Multiplier with Arithmetic Capacitance

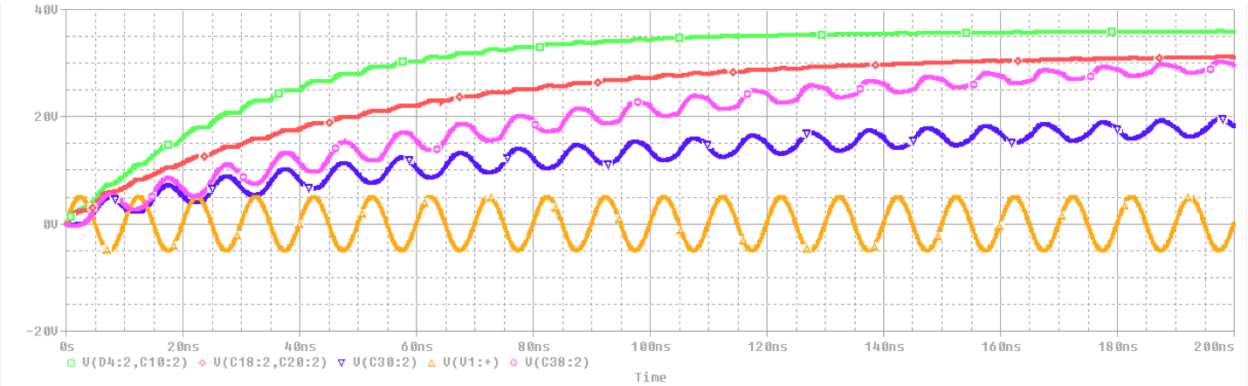

Figure 6 – Comparison of 8x Voltage Multipliers

Input signal (orange), Eight stage cascade with uniform capacitance (blue), Eight stage cascade with arithmetic capacitance (pink), Four stage differential with uniform capacitance (red), Four stage differential with arithmetic capacitance (green)

The effects of topology and capacitor values can be seen in Figure 6 when using various 8x voltage multipliers. Both cascade multipliers (Figures 2 and 3) had significantly higher ripple voltage and lower gain compared to the differential designs (Figures 4 and 5). The cascade multipliers also had longer startup times. The effects of arithmetic capacitance were also clear. The designs which implemented arithmetic capacitance had better gain than those with uniform capacitance.

The single stage cascade with uniform capacitance has the worst performance of these designs, with the largest ripple voltage and lowest gain. The differential multiplier configuration with capacitor values in arithmetic sequence provided the best results, therefore, it will be the one used in the final design within the RF energy harvester.

The design of the voltage multiplier circuit began before accurate power measurements of the local electromagnetic spectrum could be taken. Initially, the voltage multiplier was designed to have a four stage differential output. Additional stages could be added later, should the electromagnetic power density in the area not support the current design. The diodes were simulated to have the same characteristics of [7] and a 4.7 kΩ load was added to simulate the charge pump. The circuit was simulated to account for non-ideal losses to determine the minimum input voltage necessary to get 350 mV (the minimum input voltage of the charge pump) on the output. This was done by successive approximation. The minimum source voltage was 113 mV as seen in Figure 7. This gives the circuit a minimum necessary gain of 3.10 V/V. A microstrip antenna was later designed to meet this input voltage specification, so no additional stages were necessary.

Figure 7 – Output Waveform, Minimum Operating Conditions

Input voltage (red) and differential output voltage (green)

3.3 Analysis of Intermediate Stages

This section explicitly shows how the differential design actively works to reduce output voltage ripple. First, consider the outputs of only the positive half of the amplifier. The locations of the intermediate output stages are marked in Figure 8. The important thing to note is the large ripple voltages, especially on odd numbered stages.

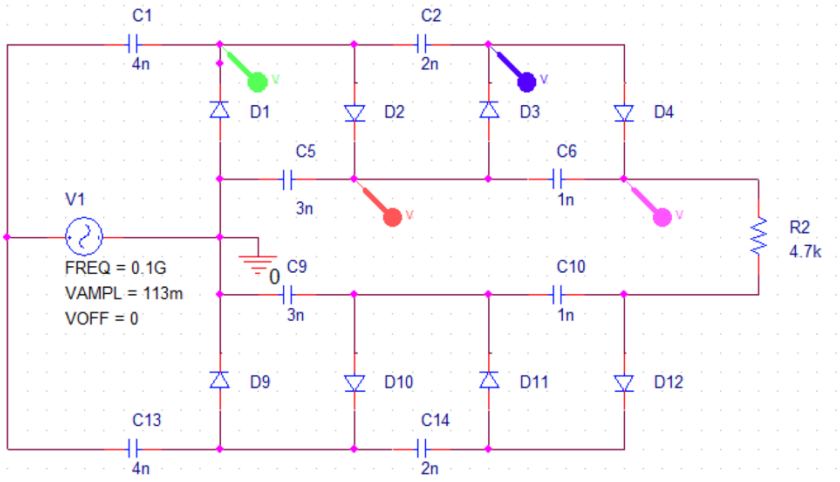

Figure 8 – Intermediate Positive Output Voltage Markers

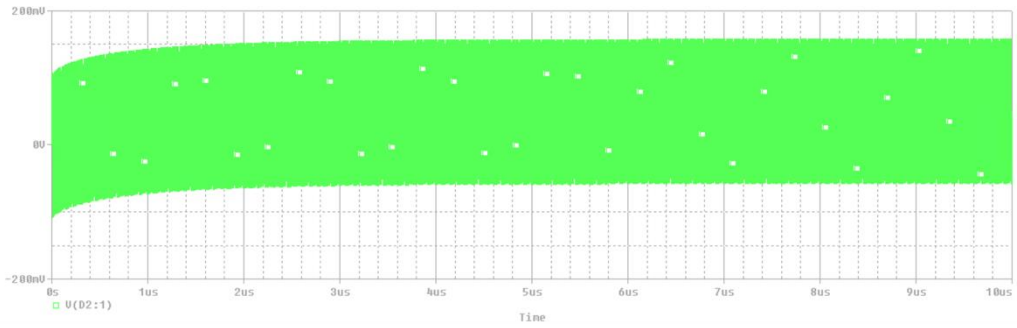

Figure 9 – Stage 1+ Output Voltage

The output voltage level after the first stage is too large to be useful for most applications. The first stage on the positive output has an DC voltage of 50 mV and a peak to peak ripple voltage of 216 mV.

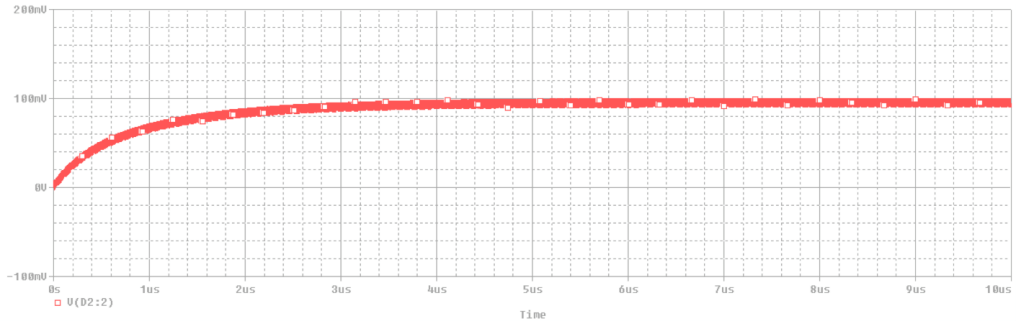

Figure 10 – Stage 2+ Output Voltage

The second stage has a much more manageable output ripple

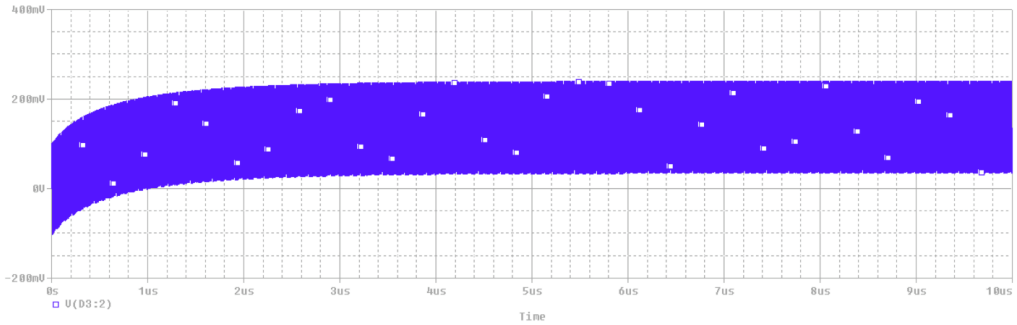

Figure 11 – Stage 3+ Output Voltage

The stage 3+ output also has a large ripple voltage. The output of this stage is too unstable for most power supply applications

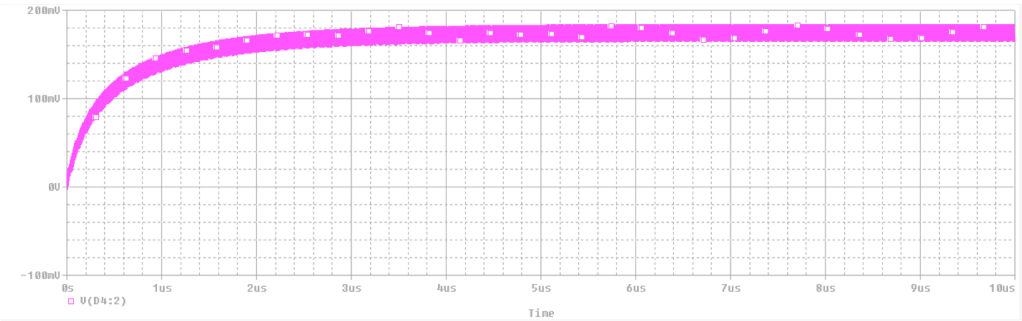

Figure 12 – Stage 4+ Output Voltage

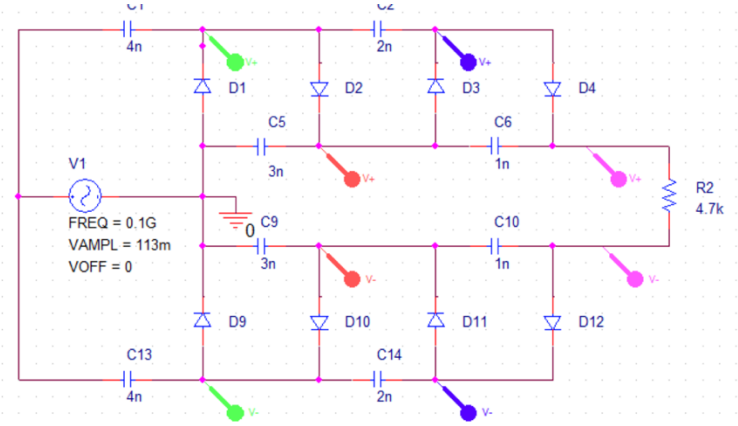

Figure 13 – Intermediate Differential Output Voltage Markers

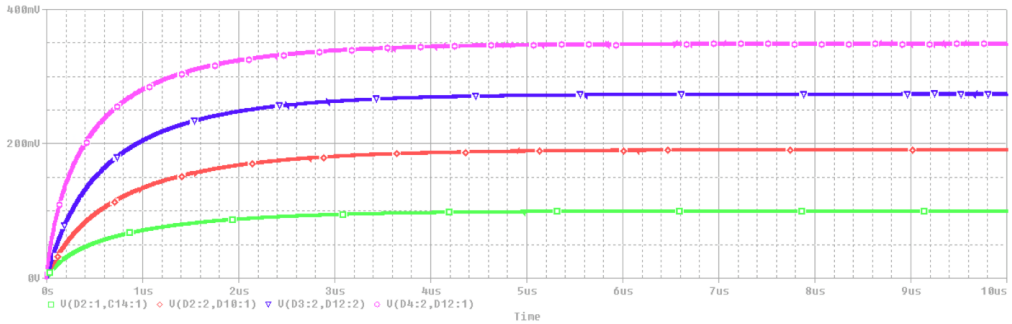

Figure 14 – Differential Output Voltages

Stage 1 (green), stage 2 (red), stage 3 (blue), and stage 4 (pink)

Table 1 – Single and Differential Intermediate Outputs

Single Stage Output				Differential Output		
Stage	**DC (mV)**	**Ripple (mV)**		**Stage**	**DC (mV)**	**Ripple (mV)**
1+	49.8	108		1	99.6	0.030
2+	95.3	4.70		2	191	0.240
3+	137	103		3	274	0.080
4+	174	9.40		4	350	1.000

If, however, the outputs are taken differentially, the ripple voltages from the positive and negative outputs cancel each other out. This significantly reduces the ripple voltage seen by the load. Figures 13 and 14 show waveforms of the voltage multiplier when the outputs are taken differentially. The figures are unable to properly show just how much the ripple voltage has been reduced. Refer to Table 1 to see just how significant the change is. The DC voltage levels of the outputs were doubled by measuring the output differentially, but the AC ripple voltage has been reduced by several orders of magnitude.

3.4 Diode Parameters

At this point, the surge currents through the diodes were checked to ensure they were within acceptable parameters. They were tested at the minimum input voltage of 113 mV. It should be noted that at these low voltages, there was significant reverse saturation current through the diodes. This was intentional, as the diodes were performing just barely good enough to reach the desired voltage on the output.

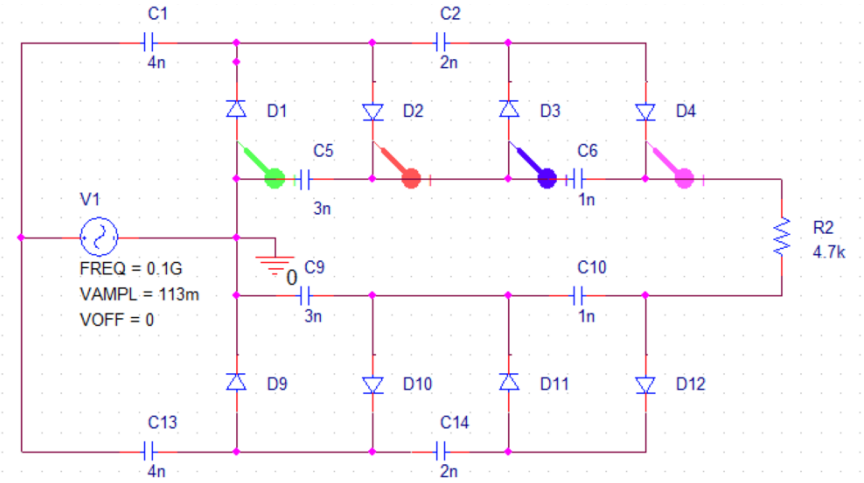

Figure 15 – Diode Current Marker Placements

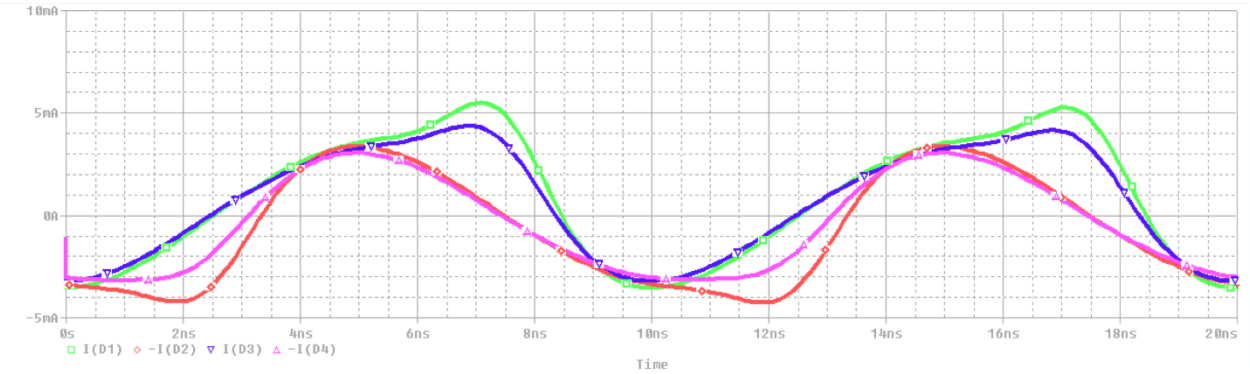

Figure 16 – Startup Diode Currents

From Figure 16, the maximum current through the diodes is about 5 mA, which is well under the rated surge current of 5 A. In steady state conditions, the diodes have peak current of 4 mA. If the input voltage is raised above the diode's rating of 120 mV, then large current surges do appear. However, even with an input signal of 5 V, the maximum surge current through the diodes was only 3 A, which remains within the acceptable parameters.

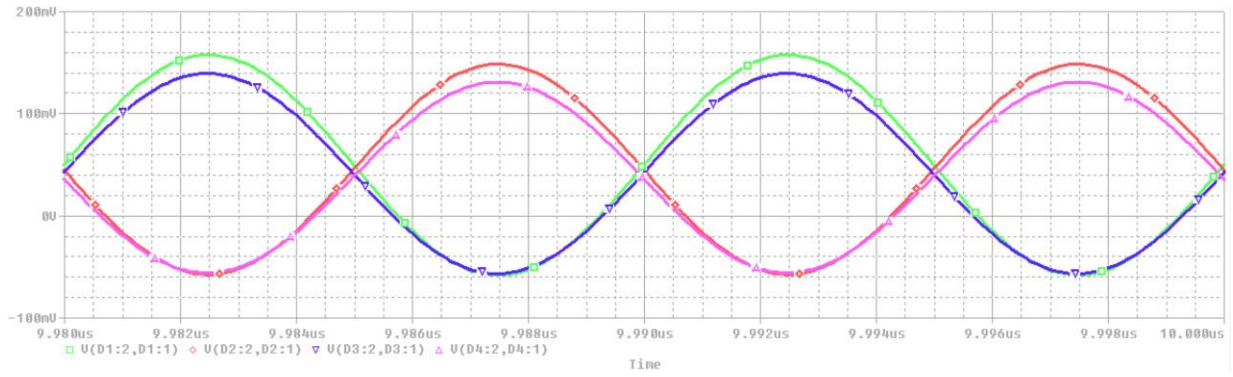

Figure 17 – Steady-State Diode Voltages

Figure 17 shows the diode forward voltage drops in steady state conditions. The waveform shows a 150 mV drop across the Schottkey diodes, which is slightly higher than expected. The figure also shows negative voltages across the diodes. This is another downside of using non-ideal diodes. Even though the diodes do not block current perfectly, they do their job good enough to grant the circuit a gain of 3.10 V/V.

3.5 Frequency Dependence

The voltage multiplier was designed to operate at 100 MHz, however, the frequency dependence of the output will still be explored. Multiple simulations were ran at various frequencies. The DC output voltage, voltage gain, and output voltage ripple were recorded for each frequency. An input voltage of 5 V was used in order to assure the circuit was operating under ideal conditions. Table 2 and Figure 18 show that there is an approximate two-orders of magnitude window above and below the target frequency of 100 MHz. The gain of the circuit is peaks at just above 7 V/V. The maximum gain is appropriate, given the expected losses in the circuit.

Table 2 – Frequency Dependency of Voltage Multiplier Circuit

Frequency	Output Voltage (V)	Gain (V_{ac} / V_{dc})	Output Ripple Voltage (mV, pk-pk)
1 kHz	0.165	0.033	330
10 kHz	7.00	1.400	1000
100 kHz	32.4	6.480	900
1 MHz	36.5	7.300	120
10 MHz	36.7	7.340	50
100 MHz	36.5	7.290	40
1 GHz	35.9	7.176	40
10 GHz	35.5	7.100	60
100 GHz	26.4	5.280	30

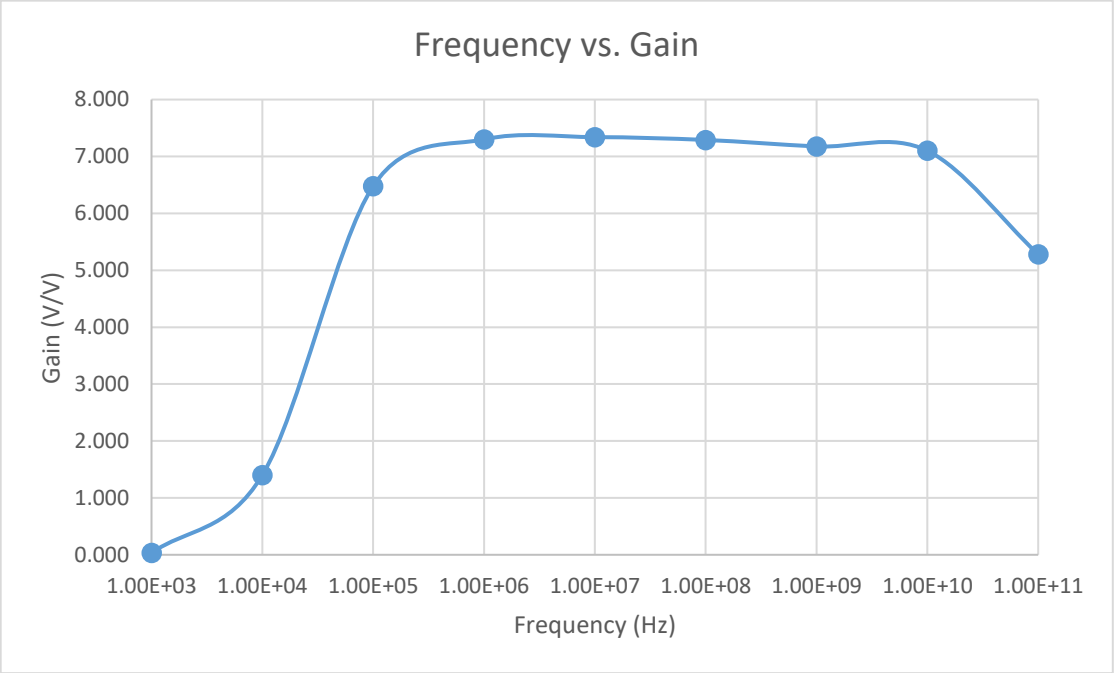

Figure 18 – Frequency Dependence Plot

3.6 Input-Output Characteristics

The next relationship that should be tested is the one between input voltage and gain. Through experimental analysis, the voltage multiplier circuit appears to have three distinct operating regions. No literature was found on this specific analysis, so there appear to be no formal names for these regions. For the sake of simplicity, they will be referred to as the quadratic, linear, and saturation regions.

Figure 19 is more complex than it appears. While V_{in} is less than approximately 50 mV, the output voltage of the Cockcroft-Walton multiplier increases quadratically. This can be seen by how the output voltage has a slope of approximately 2. Note when plotting on a log-log scale, the slope can be interpreted as the exponent of a monomial function of the form $y = ax^k$. A slope of 2 means that the relationship is quadratic.

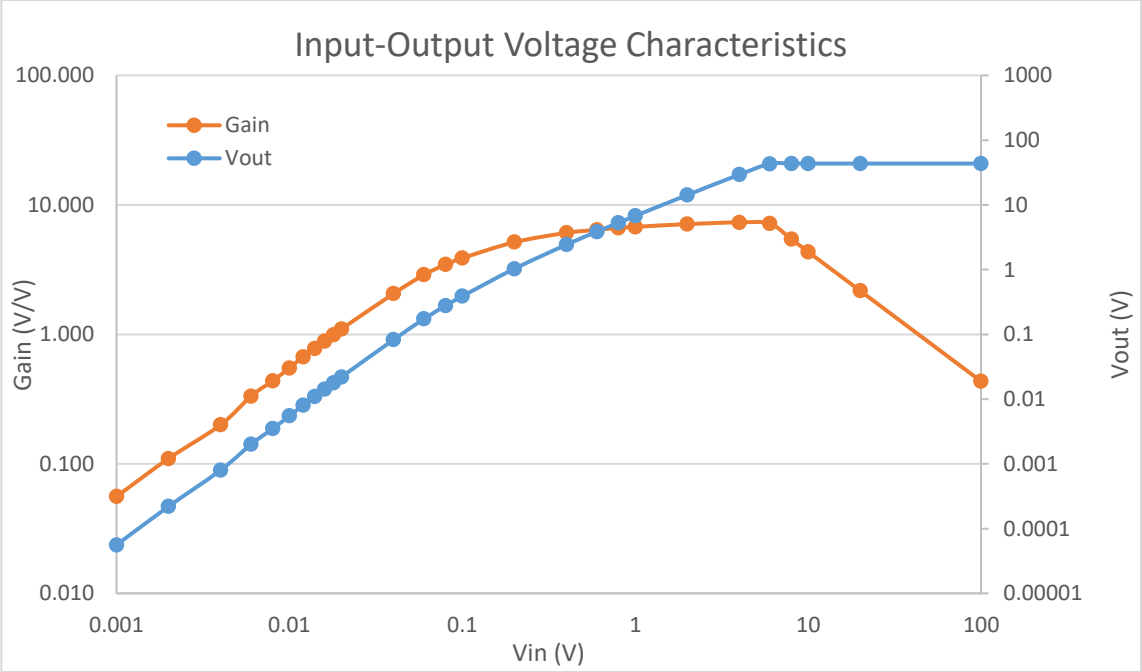

Figure 19 – Gain and Output Voltage vs. Input Voltage

There appears to be a gradual transition to the next region: the linear region. In the linear region, output voltage increases linearly with input voltage. The transition is difficult to see on the output voltage curve from Figure 19. However, notice how the gain curve levels off and becomes nearly constant between 300 mV and 7 V. A constant gain shows that the input voltage and output voltage are increasing in linear proportion. In this case, the gain levels off at around 7.2 V/V.

The final region of note is the saturation region. This occurs when the output voltage reaches its maximum possible output. At this point, even if the input AC voltage is increased, the output DC voltage remains the same. The Cockcroft-Walton voltage multiplier design used in this circuit saturates at $V_{out} = 43.4\,V$. In this region, the output voltage curve stays at a constant value and the slope of the gain plot is negative one.

The cause of these distinct regions lie within the diodes. The diodes used in this experiment have a rated forward voltage of 120 mV. When the input voltage is less than this value, the diodes do not conduct properly. Thus, the circuit is expected to perform poorly and have a relatively low gain. It was determined experimentally that the output voltage of the circuit increases quadratically with input voltage within this region. As the amplitude of the input voltage is increased, the diodes begin to conduct more reliably. This is a gradual change that becomes more noticeable as the conduction losses within the diodes and the reverse saturation currents become relatively less important. This trends towards a more linear input-output relationship as the gain begins to asymptotically approach its maximum value. The final region most likely occurs due to the breakdown voltage of the diodes. The breakdown voltage of all eight diodes in series leads to an accumulated voltage drop of 43.4 V across the load. The circuit simulation can be measured for

peak current through the diodes, which show currents higher than the rated parameters. In reality, the high currents through the diodes would cause the them to break and short circuit. This would lead to the complete failure of the voltage multiplier. The circuit simulation is operating under the assumption that the diodes never break, which is why the output voltage saturates at 43.4 V. Further research will need to be performed in order to study the different regions of the input-output voltage characteristics of the Cockcroft-Walton voltage amplifier.

3.7 Input Impedance

The ultimate goal of the low voltage Cockcroft-Walton voltage amplifier is for it to be powered by an antenna. The implementation of an impedance matching network will be critical for the success of the project. Matching the antenna and transmission line impedances to that of the load ensures maximum power transfer by reducing the reflection coefficient of the system. The size and shape of the impedance matching network will be strongly dependent on the input impedance of the Cockcroft-Walton voltage multiplier. The input impedance can be calculated from the input voltage and current waveforms.

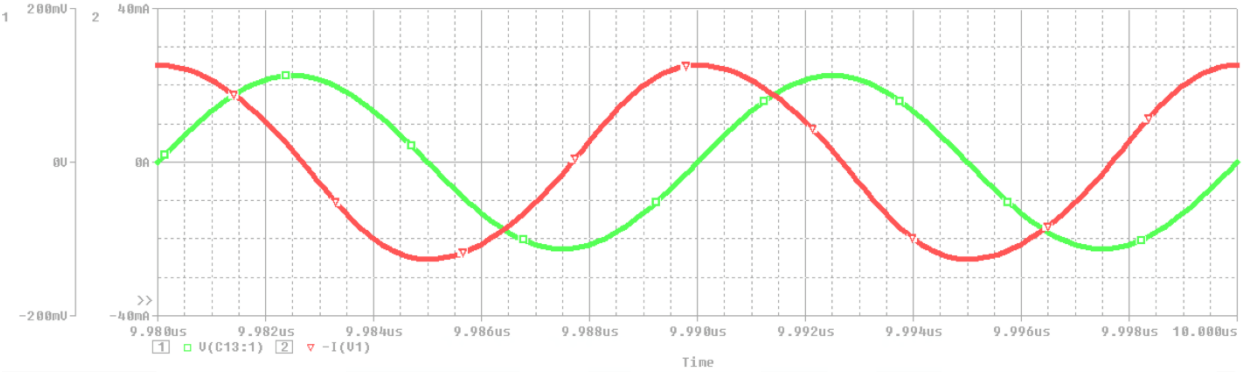

Figure 20 – Input Voltage and Input Current

From Figure 20, it can be determined that $\mathbb{V}_{in} = 113 \angle 0° \, mV$ and $\mathbb{I}_{in} = 25.3 \angle 86.4° \, mA$. Thus, the input impedance of the voltage multiplier is:

$$Z_{in} = \frac{\mathbb{V}_{in}}{\mathbb{I}_{in}}$$

$$= \frac{113 \angle 0° \, mV}{25.3 \angle 86.4° \, mA}$$

$$= 4.466 \angle -86.4° \, \Omega$$

$$= 0.280 - j4.458 \, \Omega$$

Then the inductance required to match the complex component is:

$$L = \frac{-Im\{Z_{in}\}}{2\pi f} = \frac{4.458 \, \Omega}{2\pi * 100 \cdot 10^6 \, Hz} = 7.09 \, nH$$

This value can only serve as an estimate to the actual value. Various parasitic inductances and ohmic losses are bound to occur on the fabricated PCB. As such, the input impedance of the board will need to be physically measured before a true matching network can be implemented. With an impedance matching element included, the minimum input voltage required to output 350 mV decreases dramatically. The impedance matched circuit only requires an input signal with an amplitude of 10 mV (Figure 21). Additionally, the power factor of the circuit is increased to near-unity (Figure 21), meaning there is less wasted power.

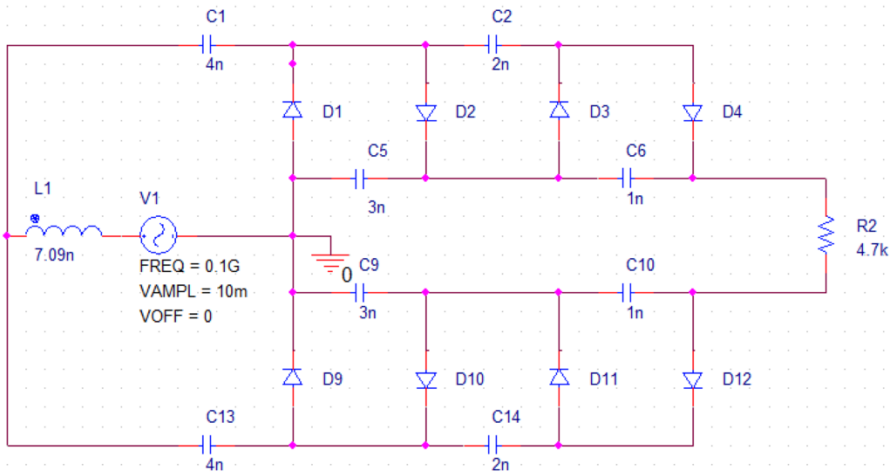

Figure 21 – Impedance-Matched Voltage Multiplier Circuit

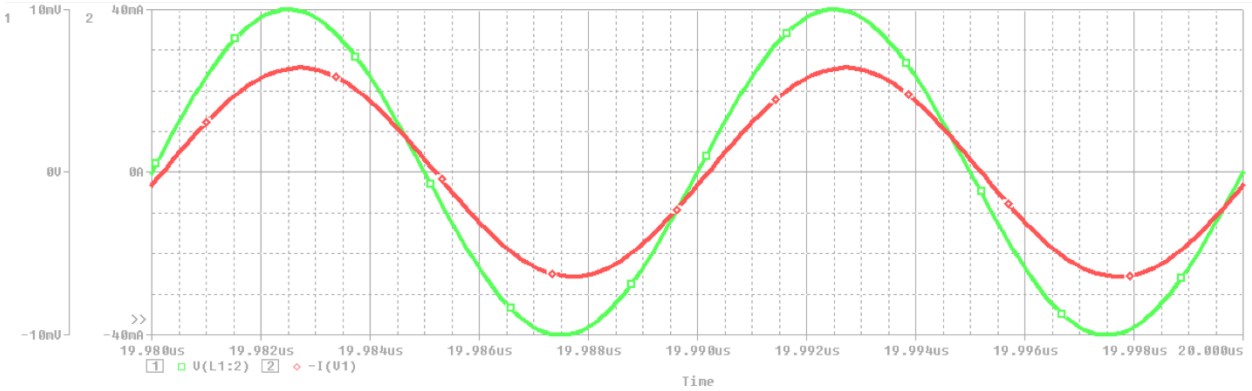

Figure 22 – Input Voltage and Input Current with Impedance Matching

3.8 Power Conversion Efficiency

In this section, power measurements will be referring to RMS and apparent power values. The apparent input power is the product of the RMS voltage and current. Since the input voltage and current are sinusoidal signals, the RMS values are easy to calculate.

$$S_{in} = V_{rms}I_{rms} = \frac{V_{in}}{\sqrt{2}} \cdot \frac{I_{in}}{\sqrt{2}} = \frac{V_{in}I_{in}}{2}$$

The actual antenna used to power the circuit will have additional harmonics. Of course, these higher order harmonics should be negligible compared to the main resonant frequency of the antenna. Therefore, the equation provided is a good approximation for the input power. Similarly, the ripple voltage and ripple current on the output of the amplifier is negligible compared to the DC voltage. As such, the output power can be approximated as:

$$S_{out} \approx P_{out} = V_{DC}I_{DC}$$

With or without impedance matching, the target output voltage and current is 350 mV and 74µA.

$$P_{out} = (350\ mV)(74\ \mu A) = 26\ \mu W$$

Without impedance matching, Figure 20 shows us that

$$S_{in} = \frac{(113\ mV)(25.3\ mA)}{2} = 1.43\ mW$$

Then the power transfer efficiency of the circuit without impedance matching is

$$\eta = \frac{P_{out}}{S_{in}} = \frac{26\ \mu W}{1.43\ mW} = 1.81\ \%$$

With impedance matching, however, the input power is only

$$S_{in} = \frac{(10\ mV)(25.0\ mA)}{2} = 124\ \mu W$$

and the efficiency becomes

$$\eta = \frac{26\ \mu W}{124\ \mu W} = 20.8\ \%$$

Part of the reason why the efficiency is so low is that the circuit is operating at the minimum input conditions. As input voltage is increased, more power would go to the load and relatively less would be lost by the passive components, improving overall efficiency.

4. FABRICATION AND TESTING PROCEDURE

The low power nature of this design means parasitic losses can have a huge influence on the performance of the circuit. These parasitic components include the ohmic losses of the PCB traces as well as their induced parasitic inductances. The extremely low capacitor values used for this circuit make it very sensitive to the effects of parasitic inductances. Because of this, the PCB needs to be as compact as physically possible so that the distances between components are minimized.

The voltage multiplier circuit would eventually need to be integrated into the main board. However, for testing purposes, a separate board will be created that consists of just the Cockcroft-Walton voltage multiplier. This allows the voltage multiplier to be tested on its own. Additionally,

a separate board allows the input impedance of the physical circuit to be measured. The results of this test will determine how the impedance matching elements will be connected to the final RF energy harvesting PCB.

The voltage multiplier PCB was designed using Allegro PCB Designer. Footprints and padstacks had to be created for each component. The 4nF and 3nF capacitors ended up sharing the same footprint, as did the 2nF and 1nF capacitors. Single jumpers were placed on the positive and negative terminals of the voltage source. Single jumpers were also placed on the positive and negative output terminals. The final board dimensions were 1.0 inches by 1.4 inches. The final design required only a single side of copper.

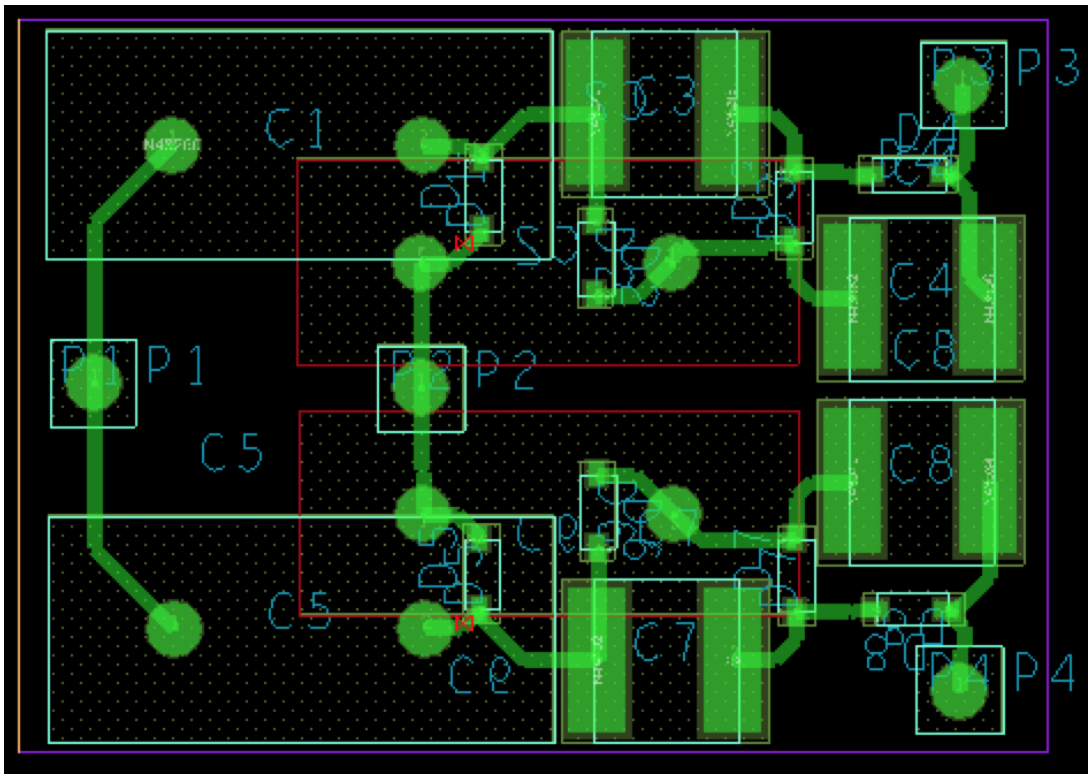

Figure 23 – Voltage Multiplier PCB Layout

Figure 23 shows just how compact the circuit was made to be. On the left, P1 connects to the positive voltage terminal and to the right of it is P2, which connects to the negative terminal of the power supply. On the right side of the board are P3 and P4, which are the positive and negative output terminals of the device, respectively. The 3nF capacitors, shown in red, would be placed on the back side of the board and soldered from the top side. This was done as a space saving measure, which reduced the size of the design significantly. The longest traces on the board (the ones going from P1 to C1 and C5) were about 9.2 mm each. By modelling the copper trace as a flat rectangular wire, the inductance can be calculated by the formula provided by [11, pp 51]. Although [11] states that the formula is to be used for low frequencies, studies such as those by [12] show that low frequency analysis can be used to approximate inductance at higher frequencies.

$$L = 0.002 \cdot l \cdot \left[\ln\left(\frac{2l}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{l}\right)\right] \mu H \quad (1)$$

Here, $l, w,$ and t represent of the length, width, and thickness of the copper wire. Given that the line width of the PCB trace is 20 mils (0.508 mm) and the thickness of 1 oz. copper clad substrate is 0.033 mm, the inductance of the longest trace on the voltage multiplier PCB is approximately 7.4 nH. This value gives hope that the impedance matching for this circuit can be accomplished by the length of the traces on the PCB alone. However, this hypothesis can only be confirmed through physical measurement of the device.

The voltage multiplier PCB was milled out on a single-sided piece of copper-clad FR4 substrate. The milling process only included the etching of the copper traces and footprints, as well as a rubout region and all drill holes for through-hole components. Surface mount capacitors were

placed first, followed by the diodes. Then the through hole capacitors were soldered to the board. Lastly, the jumpers were put in place.

Before the placement of each capacitor, a digital multimeter was used to test their nominal capacitance. This was done to ensure the accuracy of the design. After the placement of each diode, the digital multimeter was used to ensure unidirectional conductivity. It was also decided that all four through-hole capacitors would be placed on the back side.

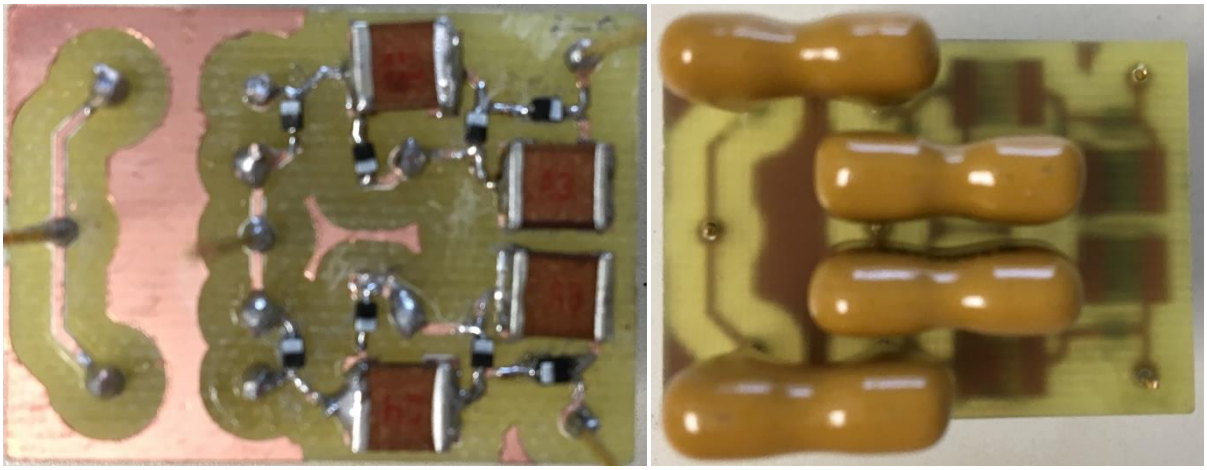

Figure 24 – Fabricated Cockcroft-Walton Voltage Multiplier

To test the device, a function generator was connected to the input pins and set to output a variable amplitude, sinusoidal voltage signal at 100 MHz. The amplitude of the input signal would be swept to find the minimum input voltage the device requires in order to output 350 mV. The output of the device was measured by connecting an oscilloscope probe to the positive output terminal of the device and grounding the probe on the negative input terminal. The negative output of the device was measured by connecting a second probe to the negative output terminal and grounding the probe on the negative input terminal. Then the MATH function on the oscilloscope was used

to measure the difference. The differential output was not measured directly due to the lack of a differential voltage probe.

5. RESULTS

Table 3 – Results of Voltage Multiplier at 100 MHz

Input Voltage (Amplitude, mV)	Output Voltage (DC, mV)	Ripple Voltage (peak-to-peak, mV)
100	0.0	174
200	10.2	357
400	35.4	800
600	82.6	1190
800	116	1570
1000	182	2030

The voltage multiplier did not fare will with an input signal of 100 MHz. Based on the output ripple voltage, it appears that the signal was not being rectified as it passed through the circuit. The DC voltage on the output changed only by a miniscule amount, if at all. By all appearances, it seemed that there was a short circuit somewhere on the board. However, when probing different locations on the board to find where the short circuit was, it was found that every part of the board

was excited to the same voltage as the input. Based on these findings, it was hypothesized that the diodes were not conducting properly.

Continuity tests of the circuit were performed again to test this hypothesis. Interestingly, the diodes were found to be conductive only in their forward biased direction. The diodes were working as intended when measured with the digital multimeter. To further investigate this strange phenomenon, a test circuit was set up consisting of a single diode in series with a 4.7 kΩ resistor. The two terminals of the test circuit would be connected to the function generator. The function generator would be swept for voltage and frequency to determine why the diodes were failing.

It was found that the diodes would stop blocking current when the input frequency rose above 10 MHz. The diodes used in this circuit simply did not have a short enough reverse recovery time to support switching frequencies with periods less than 100 nanoseconds.

When a forward biased diode is quickly shifted to reverse bias conditions, there is a finite amount of time that the space charge region with in the pn-junction remains conducting. This leads to high reverse current for a few moments before the charge carriers within the pn-junction disperse. Once the space charge region returns to its unexcited state, the reverse current flowing through the diode drops to the small leakage current level. The charge carriers within the space charge region of the diodes used in this project do not dissipate quickly enough once the current reverses direction. As such, they become unable to block current at high switching frequencies.

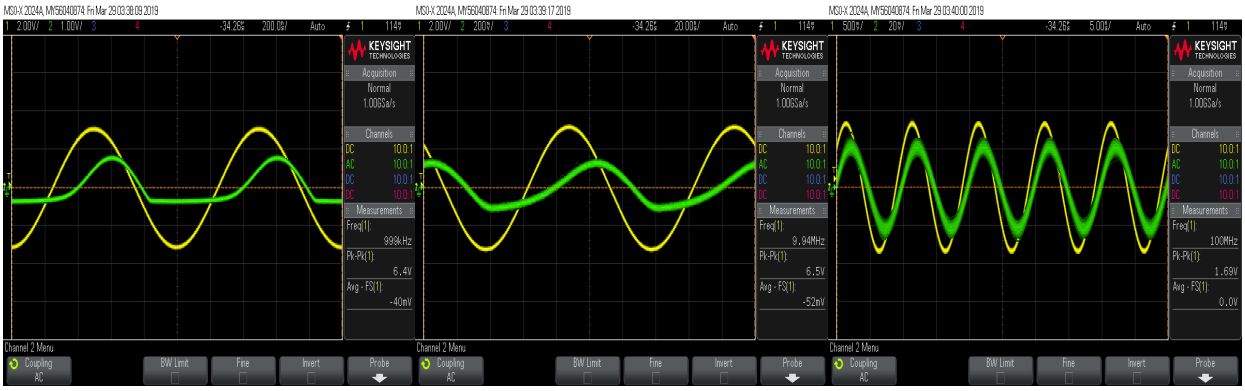

Figure 25 – Results of Diode Test

(left) At 1 MHz , the diode blocks current when the voltage signal goes into its negative half-cycle. The transition is clean as seen by the sharp edges of the waveform.

(middle) At 10 MHz, the diode begins to show breakdown properties. The transition from conduction to blocking is not very clean. The sharp edges typical of a transition from conducting to blocking can not be seen clearly.

(right) At 100 MHz, the blocking effects of the diode are no longer present. The charge carriers never leave the space charge region of the diode. In other words, the diode is always conducting.

As proof-of-concept of the voltage multiplier design, the device was tested at a frequency of 10 MHz. This was low enough that the diodes would work while still being high enough that the capacitor sizing would allow the circuit to operate as intended. The optimal capacitor designs for a frequency of 10 MHz would be an order of magnitude greater than what was used in the physical circuit. Yet, the results of the frequency dependency analysis from the theoretical background section (Figure 18) show that the gain of the device should not suffer too much as a result of frequency-capacitor mismatch. Compare Figures 26 and 27 to see how diode reliability effects the output of the voltage multiplier.

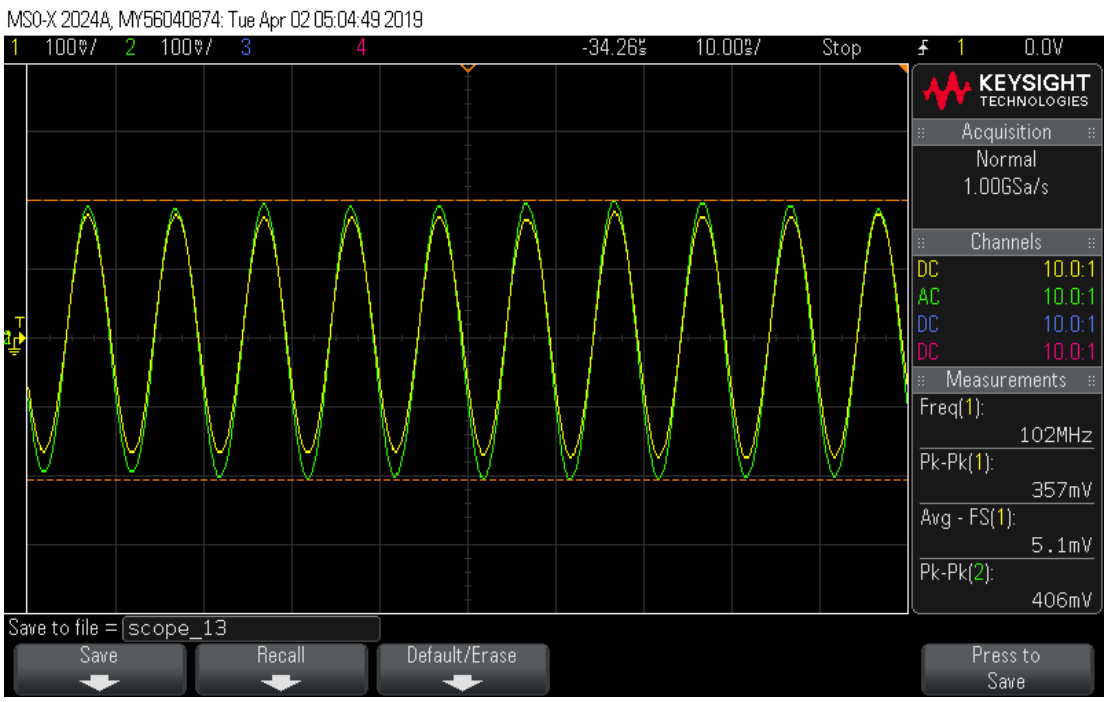

Figure 26 – Voltage multiplier, positive output, input of 200 mV at 100 MHz

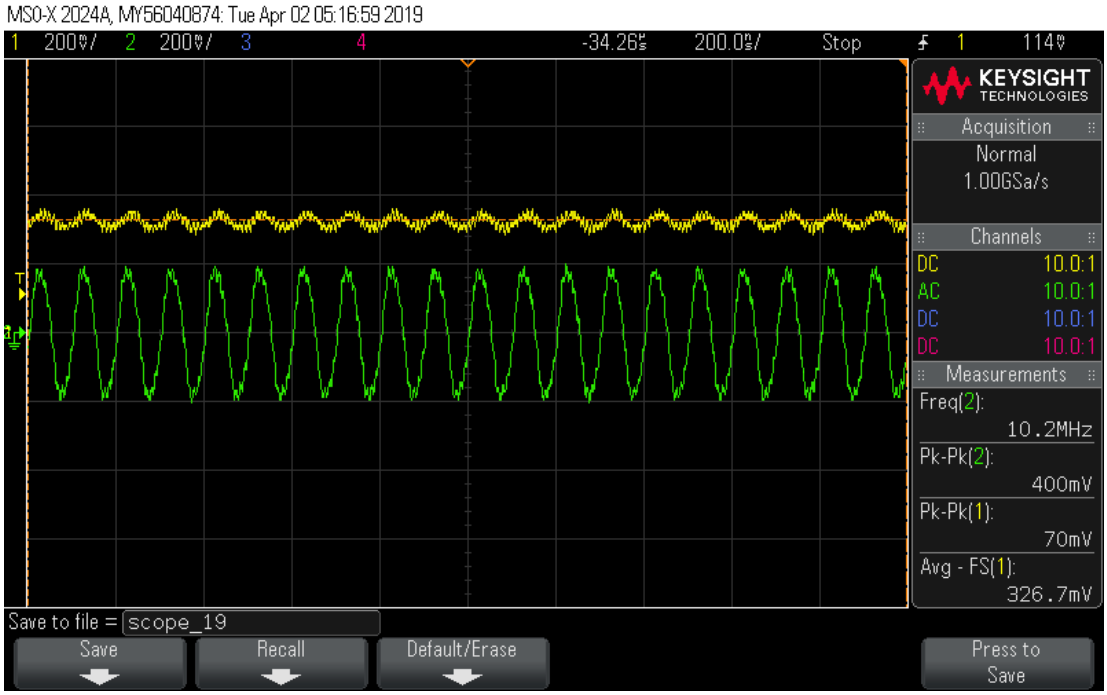

Figure 27 – Voltage multiplier, positive output, input of 200 mV at 10 MHz

Table 4 – Results of Voltage Multiplier at 10 MHz

Input Voltage (Amplitude, mV)	Output Voltage (DC, V)	Ripple Voltage (peak-to-peak, mV)
100	0.208	60
140	0.350	65
200	0.654	70
400	1.646	120
600	2.630	160
800	3.724	200
1000	4.762	200

The results of the Cockcroft-Walton voltage multiplier operating at 10 MHz show its potential as an ultra-low power AC-DC converter. The circuit was able to achieve a DC output of 350 mV when the input signal had an amplitude of 140 mV. The output ripple voltage at this point would mean that the output drops below 350 mV half of the time. Fortunately, previous testing performed on the charge pump showed that it could operate with inputs as low as 300 mV. In this case, the output of the voltage multiplier only drops below the minimum requirement for a fraction of the time. Furthermore, with inputs above 150 mV, the voltage multiplier would never output a voltage less than 300 mV.

6. CONCLUSIONS

The device was able to successfully output a DC voltage of 350 mV at a frequency of 10 MHz when the input voltage had an amplitude of 140 mV. This does not meet the requirements of 350 mV at a frequency of 100 MHz and an input of 100 mV. An input of 140 mV is worse than expected, but it is an acceptable value. The 40 mV difference can be explained by the parasitic inductances and ohmic losses present in the PCB that were not accounted for in the simulations. The problem can be solved by attaching a better antenna or larger antenna array to the input of the circuit.

The frequency disparity, on the other hand, is a big problem. When choosing parts for this circuit, the low power requirements led to the false conclusion that the diodes with the lowest forward voltage drop should have highest priority. Upon further investigation, it was found that diodes with extremely low forward voltage drops and diodes that are rated for radio frequencies are almost mutually exclusive. The RF energy harvester circuit will need to switch to RF diodes in order for the device to have a chance at working. This will undoubtedly come at the cost of increasing the minimum input requirements to the Cockcroft-Walton voltage multiplier. This means an even larger antenna array will be needed to harvest the ambient electromagnetic signals.

Something that has yet to be discussed in detail is the impedance matching network. Without an impedance matching network built into the design of the Cockcroft-Walton multiplier, most of the power supplied by the antenna will be reflected back. A proper impedance matching network ensures most of the power received by the antenna goes to the load. The simulated voltage

multiplier was found to have an input impedance of $0.280 - j4.458\ \Omega$. The reactive component of the impedance can be handled by extending the traces of the PCB to create a matching parasitic inductance. The real component of the impedance, however, poses a much more serious problem. The initial plan was to connect the antenna (milled on a separate board) to the main board through coaxial ports. Coaxial cables and connectors are designed to have a characteristic impedance of $50\ \Omega$. Without some way to increase the input impedance of the voltage multiplier, there will be a lot of power that gets reflected back to the antenna. Potential solutions include adding $100\ \Omega$ resistors to the parallel branches leading to the 4nF capacitors, but this would reduce power transferred to the load as most of it would be consumed by the resistors. An alternative solution is to remove the coaxial components and connect a $0.2\ \Omega$ wire directly from the antenna to the circuit. It is unknown how this would effect the behavior of the circuit. The last alternative is to integrate the antenna directly to the rest of the circuit by milling them on the same board. However, the size of a patch antenna with a resonant frequency of 100 MHz would be too large to be practical.

In conclusion, the Cockcroft-Walton voltage multiplier design has good potential for RF energy harvesting applications. It is recommended that diodes with extremely fast reverse recovery times be used in the design. This would allow the RF harvester to operate at higher frequencies. Gigahertz range frequencies seem to be a good choice, as this would make microstrip patch antennas small enough to be a viable option for a power supply. The microstrip antennas can also be designed to match the input impedance of the voltage multiplier, which is preferable to designing a Cockcroft-Walton voltage multiplier to match the antenna impedance.

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