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Comparative Study of Power Semiconductor Devices in a Multilevel Cascaded H-Bridge Inverter

Kenneth Mordi
University of Arkansas, Fayetteville

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Multilevel Cascaded H-Bridge Inverter

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Kenneth Mordi
Madonna University
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University of Arkansas

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_____
Alan Mantooth, Ph.D.
Thesis Director

_____
Yue Zhao, Ph.D.
Committee Member

_____
Fang Luo, Ph.D.
Committee Member

ABSTRACT

This thesis compares the performance of a nine-level transformerless cascaded H-bridge (CHB) inverter with integrated battery energy storage system (BESS) using SiC power MOSFETs and Si IGBTs. Two crucial performance drivers for inverter applications are power loss and efficiency. Both of these are investigated in this thesis. Power devices with similar voltage and current ratings are used in the same inverter topology, and the performance of each device is analyzed with respect to switching frequency and operating temperature. The loss measurements and characteristics within the inverter are discussed. The Saber® simulation software was used for the comparisons. The power MOSFET and IGBT modeling tools in Saber® were extensively utilized to create the models of the power devices used in the simulations. The inverter system is also analyzed using Saber-Simulink cosimulation method to feed control signals from Simulink into Saber. The results in this investigation show better performances using a SiC MOSFET-based grid-connected BESS inverter with a better return of investment.

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CHAPTER ONE

INTRODUCTION

1.1 Background

Semiconductor devices are the main driving force of today's power converter systems. Some of the widely used semiconductors include the silicon insulated gate bipolar transistor (IGBT), silicon carbide metal oxide semiconductor field effect transistor (MOSFET) and gallium nitride high electron mobility transistor (HEMT). The multilevel cascaded H-bridge inverter is a major candidate for semiconductor applications. Making the right choice of semiconductor device for the implementation of a cascaded H-bridge is a decision of great importance because every semiconductor has its own challenge in terms of implementation. For example, SiC MOSFETs have very low short-circuit withstand time (SCWT) as compared to Si IGBTs. For this reason, a comparative analysis is crucial for best performance and reliability of the multilevel CHB inverter. Multilevel converters are promising converters in the power electronics industry. Medium and high voltage applications use a multilevel inverter in most cases because of its modularity [1], [2]. Before this time, many investigations were carried out on the switching speed, thermal behaviors, loss and efficiency of SiC and Si power devices in different converter applications [3-7]. Results show that SiC MOSFETs are better compared to Si IGBT in inverter applications. PSCAD and Matlab/Simulink models were used in [3] to conduct comparisons between SiC MOSFET and Si IGBT. The dc bus of the converter was investigated to determine how it can influence the switching loss of the devices. In [8], a permanent magnet synchronous motor (PMSM) torque and speed control was investigated to determine the feasibility of modular multilevel converters (MMC) in PMSM. In the report, the Si IGBT device was found to have performance degradation in extreme/harsh environments. In the investigation, a MATLAB Simulink model was used to

compare performance. Also, a regenerative cascaded H-bridge multilevel converter was used to study thermal conductivity of Si IGBT [9]. The Si IGBT showed inferior thermal conductivity compared to SiC MOSFET. The cooling required, thermal cycling stress, and switching transient speed were limitations for the Si IGBT. To mitigate this problem, a larger heat sink will be required, and directly proportional to its cost. The SiC MOSFET higher blocking voltage feature is also an advantage over the Si IGBT

1.2 Thesis objective and methodology

In most power electronic converter design simulations, the switching devices used are ideal models. Therefore, the simulation results will not show practical operations of the converter. It is important to use practical models of switching devices during simulations to accurately forecast the operation of power electronic systems during design. However, most simulation software does not have built-in features to model power devices from their datasheet. Saber has this required feature and allows one to characterize power semiconductor devices such as the SiC MOSFET and Si IGBT. However, its control toolbox is strongly typed unlike Simulink and requires a series of type casting to match data types during control logic implementations. For large systems, this will increase system complexity and execution time. Therefore, using Saber-Simulink Co-Simulation strategy helps to study practical operations of power electronic converters without increasing the complexity of the control system. One objective of this research is to evaluate efficiency, cost and the potential of optimizing the operating conditions of SiC MOSFET and Si IGBT devices in a nine-level cascaded H-bridge inverter with a battery energy storage system (BESS). The advantages and disadvantages of these operating conditions will be highlighted while keeping in mind the long-term benefits of the inverter using either SiC MOSFET or Si IGBT. One of the main design efforts in power electronic systems is to increase the efficiency while keeping minimal

the cost and weight of the system. Wide band gap devices such as SiC MOSFETS have lower switching loss, but they have significantly higher cost than Si IGBTs. Therefore, their operational advantages for specific application needs to be investigated to validate their benefits. In this thesis work, a comparative analysis of Si IGBT and SiC MOSFET was done for a nine-level cascaded H-Bridge inverter.

Reviewing other work done on multilevel cascaded H-bridge (CHB) inverter that were implemented using Si IGBT, along with the problems encountered, it is pertinent to compare performances of possible power devices that can be used for implementation. After this is done, the better device can be selected for the application. Because power losses and efficiency are crucial issues for inverter operation, it is important to select the right power device.

This thesis work compares crucial performance factors of an inverter which includes switching loss, conduction loss, efficiency, and thermal performances. The power devices under investigation are the SiC MOSFET and Si IGBT switches. Cree SiC power MOSFET C2M0040120D and a similarly rated Infineon Si IGBT IKW25N120T2 were selected for the comparative analysis to identify their performances. The analysis process includes modeling the power devices using Saber in the built-in model architect tool. This process is aimed at creating a real life power device model for simulation purposes. The characteristics of these models are similar to physical power devices after characterization. These characterized models are tested at different temperatures using simulations prior to running it in the inverter circuitry. The power losses were calculated at different junction temperatures and switching frequencies using cosmosScope^{TM} and the embedded waveform calculator. Theoretical equations are also presented to support simulation results and findings.

1.3 Thesis outline

The outline of this thesis is in this sequence: Chapter Two is a literature review on battery energy storage system (BESS), multilevel converters and power semiconductor devices. Chapter Three describes the CHB BESS inverter topology, benefits and controls. Chapter Four describes the theoretical analysis. Chapter Five describes the comparative methodology and discusses the comparison results obtained. And, finally, Chapter Six states the conclusion.

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CHAPTER TWO

LITERATURE REVIEW

2.1 Power semiconductor devices

Power semiconductors are the switching devices in switch-mode power converters. Switching is a common mode of operation that is associated with this kind of power electronics circuits. One driving force in most research and development of power semiconductors is aimed at achieving minimal power losses in power devices during switching operation.

The type of switching associated with a power device will determine the level of power loss to expect during operation. Power semiconductors can be operated using different switching methods. These switching methods can be classified into two regimes:

2.1.1 Hard switching – Hard switching is a stressful switching behavior of power semiconductor devices. This method of switching subjects power devices to high voltage and current during the turn-on and turn-off processes. As a result, the device undergoes high stress with more switching losses. Passive snubbers are usually added to the power circuits with this type of switching. The passive snubbers help to reduce *dv/dt* and *di/dt*, switching loss and divert switching stress to the snubber circuit [1]. Hard switching requires fewer inductors and capacitors in the circuit. This implies that there will be a reduction in cost and complexity of the system. Some drawbacks of hard switching includes high power loss peak and electromagnetic noise generated in the switching moment.

2.1.2 Soft switching – Soft switching is characterized with turning on/off of a power device while there is no current flow or voltage potential across the device. There is a significant loss reduction in this type of switching where the waveform is smoothed with no transient spikes. Zero

voltage switching (ZVS) and zero current switching (ZCS) techniques are beneficial in reduced switching stress and better efficiencies at high switching frequencies. Soft switching converters can be operated at very high switching frequencies between 500 kHz to few mega Hertz. This is because of the reduced switching loss and switching stress. Soft switching converters are a better solution in the suppression of electromagnetic interference (EMI) [2].

Conventional PWM converters are dominated with switching losses when operated in switch mode. Table 2.1 compares between hard and soft switching

Table 2.1. Comparison between Hard Switching and Soft Switching [2]

Parameter	Hard Switching	Soft Switching
Hardware count	Norm	More
Switching loss	Severe	Almost zero
Overall efficiency	Norm	Possibly Higher
Overall power density	Norm	Possibly higher
Modulation scheme	Versatile	Limited
Heat–sinking requirement	Norm	Possibly high
EMI	Severe	Low
dv/dt issues	Severe	Low
Maturity	Mature	Developing
Cost	Norm	Higher

2.2 Power Semiconductor Applications

The successful development of power semiconductors will last for as long as power electronics is in existence. This is because of the increasing need for energy conversion, resource conservation, and the need for other alternatives to combustive/fossil fuels. Alternatives to fossil

fuel are becoming successful with regard to hybrid and electric cars. The development of alternatives to fossil fuels depends so much on system costs, amount of energy consumption during production and gaining the market after production – this is determined on how much energy and cost can be saved during operation of the end product [1]. Some forms of renewable energy conversions are photovoltaics and wind power. They need power semiconductors to convert this renewable energy to electrical energy. The converted electrical energy can also be stored in batteries and utilized when needed. In addition, the development aims at "low materials consumption/ low costs" and "high efficiency". These factors are gaining more importance by the day [3]. One good application of power semiconductors is the transformerless multilevel CHB inverter. Semiconductors are used to realize the required voltage level without a bulky 60 Hertz line transformer.

The directions for the further development of power semiconductors and their applications are as follows:

a) Reduce losses in power semiconductors
b) Increase the switching performance – current and voltage
c) Expand the operating temperature range
d) Reduction required controls and protection circuitry
e) Component behavior in case of failure
f) Long life span, robustness and reliability
g) Cost reduction

The development directions of power semiconductors can be subdivided into:

1) Semiconductor materials – new material development, e.g. wide bandgap materials

2) Chip technology – reduction of chip area, improvement of chip characteristics
3) Degree of integration – Device complexity, integration of drivers, monitors and protective functions will reduce system cost.
4) Packaging – the package structure of power semiconductors has a lot to do with its performance. These include:

a) Improvement of heat dissipation
b) Increase in thermal and power cycling capability
c) Optimization of internal connections and connection layouts regarding parasitic elements
d) User-friendly package optimization
e) Reducing packaging costs and improve the environmental compatibility during operation production, and recycling [4].

Power semiconductors like MOSFETs IGBTs, GTOs and thyristors are controllable power semiconductors. These semiconductors can be connected in series and parallel, meaning that any amount of electric power generated can be transformed. Although, the higher the power level becomes, the more complex the system will be.

Modern semiconductor research focuses on more complex technologies, smaller semiconductor structures and precise process control. There are inevitably driving forces of modern power semiconductors (SiC and GaN) towards the physical limits of silicon. Today, wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN) are in the forefront of power semiconductor research [1]. Compared to silicon (Si), SiC and GaN have higher energetic gaps between their valence and conduction band. As a result, SiC and GaN have lower forward on-state losses, permits higher temperatures on the chip, and have better heat conductivity than Si [5]. Figure 2.1 show the material properties of SiC and Si and their impact.

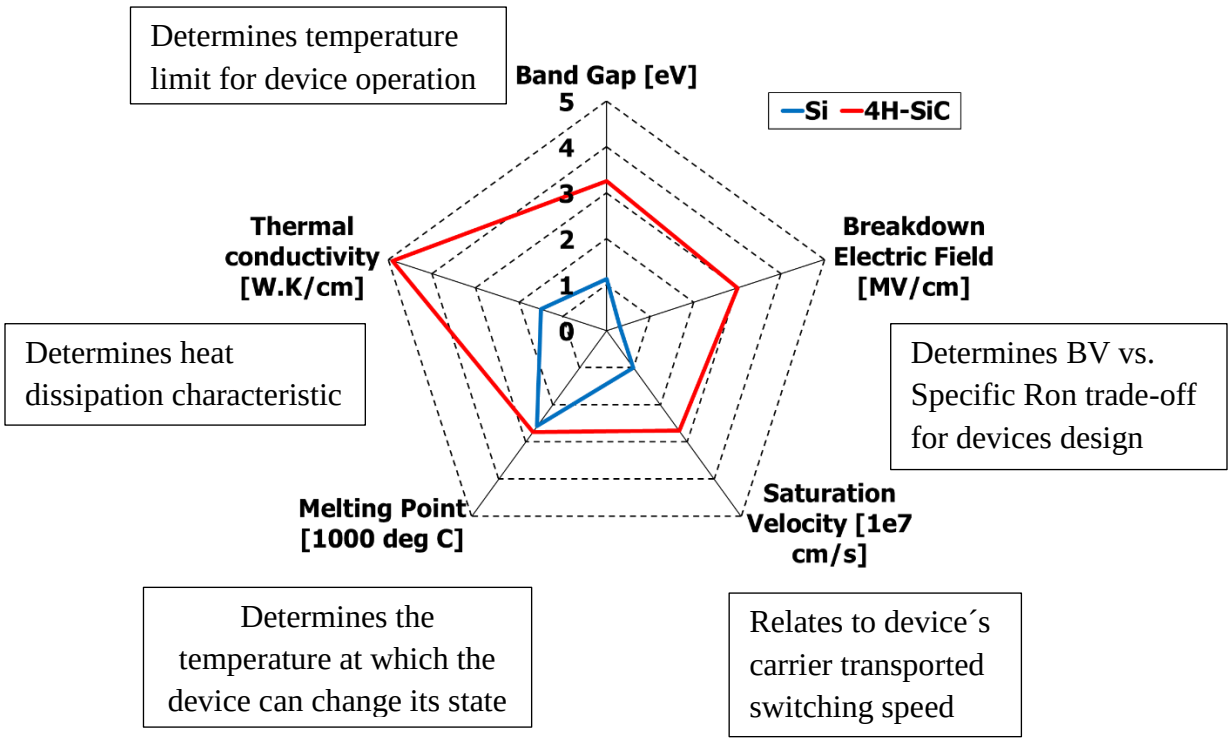

Figure 2.1. Impact of different physical parameters of semiconductor materials [5]

2.3 Structure and Functional Principle of Power MOSFETs and IGBTs

There is a lot of difference in the properties of power MOSFETS and IGBT. One of them is the structure of the third electrode. In MOSFETs the third electrode is the drain, and for IGBT it is the collector. This distinct structure results in different principles in terms of functionality. When a sufficient positive control voltage from a driver is applied to the MOSFET's gate and source, or the IGBT's gate and emitter, an n-conducting channel is generated below the gate terminal region. Electrons conducted at this region move from the source/emitter through the conducting channel into an n-drift area down to the bottom terminal. At this point the charge carrier region is depleted. Because MOSFETs are unipolar, these electrons conduct the drain current alone [1].

The IGBT structure resembles a MOSFET structure up to the n-region of both devices. IGBTs, unlike MOSFETs are bipolar, and the presence of both carriers in the n-drift region is the reason for the lower on-state voltage of the IGBT. As a result, the IGBT can be designed for much higher voltages and currents while having similar chip area to a MOSFET. Conversely, minority carriers will have to be dissipated again from the n-drift region during turn-off, and this leads to higher switching loss [1].

The compensation principle concepts in MOSFETs enables the link between blocking voltage and doping of the n^- region to be broken, and significantly reduces the resistance of the MOSFET. In [7], for such a power MOSFET:

$$R_{DS\ (on)} = k * V_{(BR)} \quad (1)$$

Where: k is the material constant for 1 cm^2 of the chip area, and $V_{(BR)}$ is the Drain-source breakdown voltage.

One vital advantage a unipolar device has over a bipolar device is that there is no charge storage effect. Very short switching time can be achieved in a unipolar device because the majority charge carriers are solely in control of charge transfer in the device.

2.3.1 Silicon carbide MOSFET

Silicon carbide (SiC) power MOSFET devices are gradually replacing silicon IGBTs in most power electronic applications, most of which requires high power density, high efficiency, and high temperature operation capability [8]. In the research and development sector, large investments have been made by government research programs because of the level of attention SiC power devices have received.

Before the commercialization of SiC MOSFETs, MOSFET manufacturing was Si-based. This is because the electronic passivation has enough dangled bonds at the surface of the semiconductor, and could only be realized by growing SiO_2 with heat as the gate dielectrics [11]. However, Si-based MOSFETs show certain limitation in their performance which are a characteristics of Si materials. One of the characteristics is the thickness of the drain-drift region. The structure of several MOSFETs have been developed with efforts to resolve the problem of on-resistance [12]

Wide bandgap materials such as SiC have undergone tremendous advancements in their material properties which now features low $R_{DS(on)}$ with exceptional switching performances. These advantageous features translate into a more compact and efficient device. Because of the exceptional switching performance and low on-resistance of SiC (even at high temperature operation), thermal designs of power electronics system are simpler because of fewer cooling requirements [13].

At lower power levels, SiC has considerable benefit in terms of conduction losses especially at low output currents. SiC MOSFETs do not experience tail currents during turn-off, thereby leading to greatly reduced turn-off losses which sometimes can be negligible. These advantages of SiC MOSFETs are because of its unipolar nature [14]. Conduction loss is inversely proportional to the size of the transistor. In other words, as the switching transistor gets bigger, its $R_{DS(ON)}$ decreases, and also resulting in the reduction of conduction loss. Conversely, if the MOSFET's physical size increases, its capacitance is bound to also increase, and this will increase the switching loss of the MOSFET [15]. This is to say that the architecture of SiC MOSFETs plays an important role in its performance. There will be a different relationship between the on-resistance and capacitance of the device whether the architecture is trench or lateral. The $R_{DS(ON)}$

ratio per unit area and capacitance per unit area are different for each case and therefore demonstrates different benefits [16].

One feature of power MOSFET that protects the devices against unexpected voltage overstress is the in-built avalanche. The avalanche energy in MOSFETs help to prevent failure when the breakdown voltage of the device is exceeded during operation. SiC MOSFET is observed to be rugged as it is capable of dissipating 17J/cm2 [17]. SiC MOSFET has found its application in various power electronics systems, such as the automotive industry, and particularly in hybrid and electric vehicles. The advantages of power semiconductors using SiC MOSFET are significant even in the automotive industry. Space and weight are a very big concern in automotive manufacturing, and therefore power density is crucial [18].

SiC power MOSFETs can switch faster than any other devices with its class of power. Looking at all these system-level benefits of SiC MOSFETs, there is still a drawback associated with SiC MOSFETs as a result of its fast switching capability. This side effect manifests in its high dv/dt and di/dt during voltage ramping. As shown in Figure 2.2, *dv/dt* is the rate of change in the drain-source voltage, while *di/dt* is the rate of change in drain current. As the voltage begins to rise and exceeds 80 V/ns, there is a possibility that common-mode noise and control circuitry failure may occur. The drain current – *di/dt* at this point is also high and can result in voltage overshoot and resonant effects which can overstress the device and limit its performance [19].

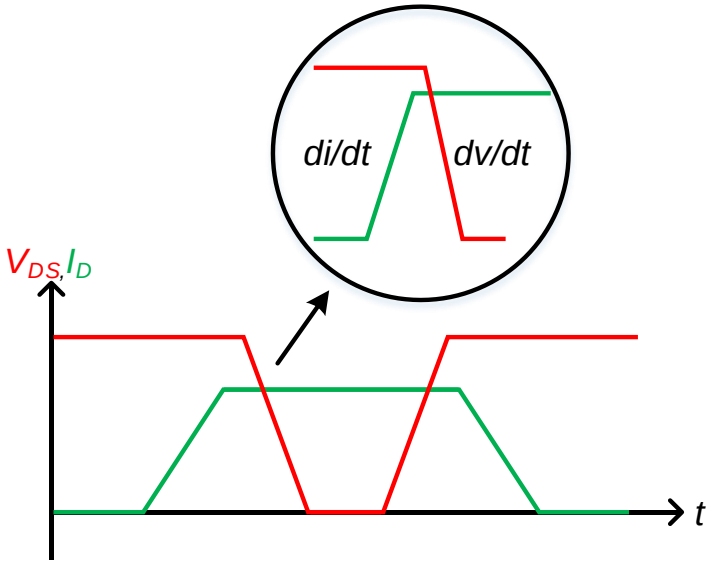

Figure 2.2 dv/dt and di/dt of a semiconductor device.

2.3.2 Silicon IGBT

Silicon insulated-gate bipolar transistor (Si IGBT) is a three-terminal power semiconductor device primarily used as an electronic switch. These terminals comprise of the gate, emitter and collector terminals. Si IGBT is used to switch electric power in numerous applications where power conversion is needed. Some of the applications include motor drives, electric/hybrid cars, trains, air conditioners and so on. Si IGBTs have developed from one generation to another, with third generation rivaling SiC MOSFETS under certain conditions [20]. Si IGBT has a lower forward voltage drop in higher blocking voltage devices. One major drawback of Si IGBT is that reverse current conduction is not possible. If a reverse conduction is needed in a circuit, a freewheeling diode is added parallel to the Si IGBT switch to enable current conduction in the opposite direction.

The continual research and development of Si IGBT has gained solid improvement for high-power device packaging. One of these developments is the addition of body diode which will

allow for reverse current conduction, and as a result the device can turn-off softly. This feature of integrating a body diode will increase power density of Si IGBT in terms of its package footprint [20]. One other area of research regarding Si IGBT is its operating junction temperature. Presently, the operating junction temperature of Si IGBT is at 175°C. This achievement is because the power chips of the device are sintered to a direct bonded copper [21]. Power losses in an IGBT for the most part comprises of conduction and switching losses. Switching loss is estimated by adding the ON and OFF switching energies of the device during operation. The losses in the diode is estimated by reverse recovery [22]. The totality of switching energies of the device and reverse recovery of diodes, multiplied by operating frequency (switching frequency) gives the overall switching loss of the device. Switching loss contributes to a substantial amount of a system total loss in power electronics. Whereas in the case of conduction, the total conduction loss of the IGBT and freewheeling diode are the product of current during conduction that flows through the collector, and the saturation voltage of the device. The freewheeling diode of an IGBT allows current only in one direction during conduction. When switching from the conduction to the blocking state, the diode stores energy that has to be discharged before blocking reverse voltage. The amount of time it takes for the diode to discharge is called the reverse recovery time (T_{rr}). During discharge time, the current flowing through the diode may flow in the opposite direction. Also the time taken to recover when the device is in the off-state generates losses. This time is called the reverse recovery time [23]. A device experiences instantaneous power loss when the current and voltage flowing through the device are significantly higher than zero during transition from off to on.

The determining factors for conduction losses are load current, duty cycle, and junction temperature. And the switching loss factors are junction temperature, dc link voltage, load current and switching frequency. Switching frequency is directly proportional to switching losses. Heat

sinks are required for IGBT devices with high power to help extend device lifespan and increase efficiency [23].

Current overshoots in IGBT occur primarily as a result of the time it takes the device to generate current form zero level to the device's rated current level during switching. At this point, the current at the collector increases swiftly, while the collector to emitter voltage decreases. This is the on-state of the device, and the voltage and current transitions results in turn-on loss [22].

2.4 Multilevel converters

Multilevel converters have remained under research and development work for over three decades. The demand over the years for increased power and voltage of inverters has led to the construction of multilevel voltage source inverters and, not often current source inverters. The problem of improved quality of the converted energy and voltage in inverters are also a concern. Semiconductors switching devices are employed in inverters to improve the energy and voltage quality of inverters. The input voltage of a voltage source inverter is connected in series, and it produces multilevel output voltages. This process uses the nearest instant value of the needed sinusoid of the output voltage. This result in the formation of an instant wave of output voltage. This is achieved by using the amplitude modulation that is added by pulse width modulation between the close voltage levels [24].

Recent developments in multilevel converters have successfully advanced into high power industry applications, and therefore they are considered a mature and proven technology in power electronics. Today, multilevel converters are commercialized in customized and standard products that power a wide range of applications. These applications include pumps, grinding mills, high voltage direct current (HVDC), gas turbines, medium and high voltage grid connected, to mention

a few [25]. Despite the fact that multilevel converters are a proven technology, they pose several challenges. Because of these challenges, and the quest for solutions to these challenges, the research and development of multilevel converters are still on-going. Efficiency, power density, reliability and cost of multilevel converters leaves a great concern which researchers throughout the world are contributing to their improvement [26].

2.5 Multilevel Converter System Configurations

Multilevel converter is known for its multilevel stair-case style of waveform. Series connected H-Bridge configuration, which is also known as cascaded H-bridge converter was introduced in the late 1960s [27]. The introduction of cascaded H-bridge inverter was followed by the low power flying capacitor configuration. In the late 1970s, the diode-clamped converter was introduced [28]. Diode clamped converter configuration developed gradually into three-level NPC (3L-NPC) [29] which is considered as the first medium-voltage multilevel power converter. These three multilevel converters topologies/configurations are considered outstanding in the multilevel converter family. Although cascaded H-bridge, flying capacitor, and diode-clamped converter configurations are commercialized at different power ratings, the diode-clamped 3L-NPC and CHB are the most prevalent multilevel converter topologies used in the industry. Fig. 2.1 is a multilevel converter classification. It comprises of other multilevel converter topologies, one of which has found practical application in industry.

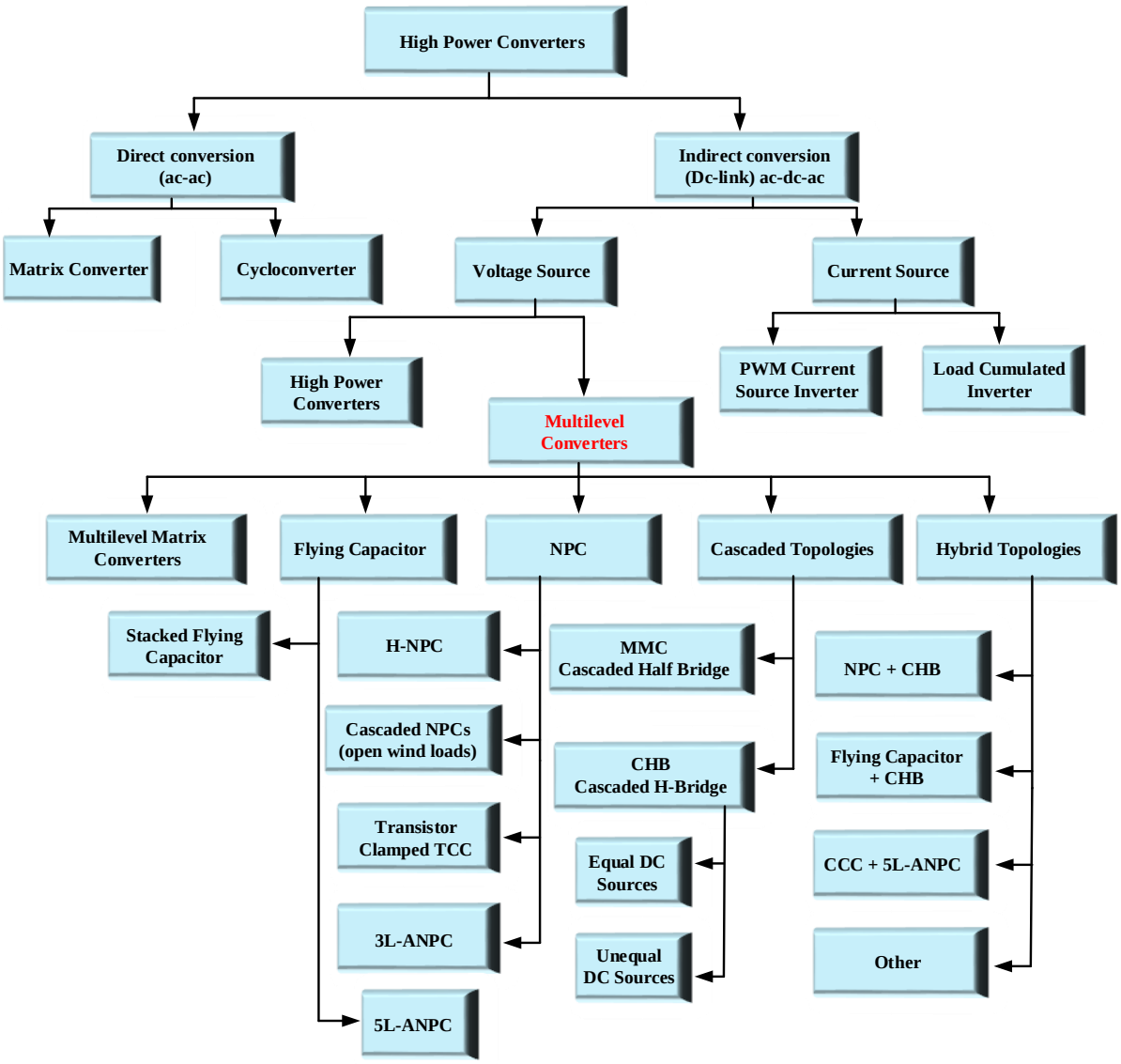

Figure. 2.3. Multilevel converter classifications [24].

2.5.1 Cascaded H-Bridge Inverter

The cascaded H-bridge inverter is an appropriate topology for applications with high-power. This is because of its modular structure, which can allow operations at higher voltages with low breakdown voltage power devices. In this type of configuration, the phase shifting of the carrier signals changes the position of the frequency harmonics. It moves the frequency harmonics

to the higher frequency side. The result of this movement, together with the high number of levels, makes it possible for the power devices to switch at low frequencies with lower losses [30]. The cascaded H-bridge inverter operation requires high number of dc sources which help to improve the power factor, and reducing the input current harmonics. These dc sources are isolated from each of the H-bridge to avoid a short circuit at the dc links. Fig 2.2 is a five-level structure of a single phase Cascaded H-bride inverter.

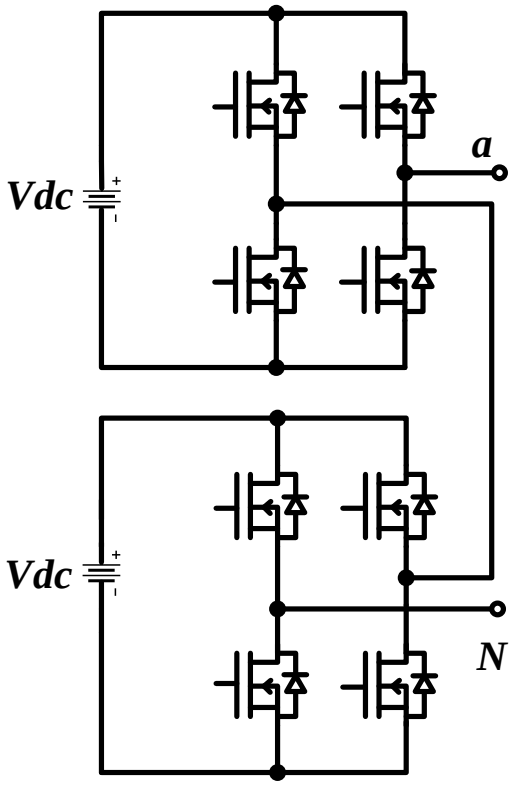

Figure. 2.4. A single phase five-level cascaded H-bridge inverter.

Table 2.2. Switching States of a Single Phase 5-Level Cascaded H-Bridge Inverter

Switching State				V_{H1}	V_{H2}	Voltage V_{AN}
S_{11}	S_{31}	S_{12}	S_{32}			
1	0	1	0	E	E	2E
1	0	1	1	E	0	E
1	0	0	0	E	0	
1	1	1	0	0	E	
0	0	1	0	0	E	
0	0	0	0	0	0	0
0	0	1	1	0	0	
1	1	1	1	0	0	
1	1	0	0	0	0	
1	0	0	1	E	-E	
0	1	1	0	-E	E	
0	1	1	1	-E	0	-E
0	1	0	0	-E	0	
1	1	0	1	0	-E	
0	0	0	1	0	-E	
0	1	0	1	-E	-E	-2E

2.5.2 Neutral Point Clamped (NPC) Inverter

The 3-level Neutral point clamed (3-L NPC) is popular in the industry because of its simple transformer rectifier power circuit structure. The device count of the NPC inverter is low for an inverter and rectification applications which also include fewer capacitors. Modifying NPC to have

higher voltage levels will increase losses and create an uneven loss distribution in the inner and outer switches [31]. That is, the period of conduction of inner switches will be more than the outer switches in one fundamental switching cycle. This results in unequal losses in the devices. The NPC inverter is characterized with fluctuations at the dc bus midpoint voltage [32]. The dc-link capacitor voltage balancing cannot be achieved with higher level (> 3-L) topologies having a passive front end when implementing conventional modulation strategy. This is not a favorable condition for the inverter. For example, a stable dc-link is important for the smooth functioning of the inverter to drive brushless motors [33]. Fig. 2.3 is a single phase NPC inverter.

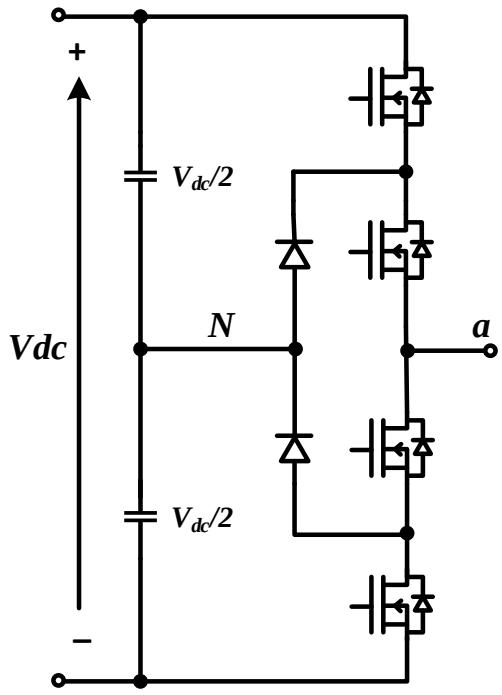

Figure 2.5. A single phase NPC inverter.

Table 2.3. Single Phase 3-L NPC Inverter Switching States

Switching state	Device switching status				Inverter Terminal voltage
	S_1	S_2	S_3	S_4	
+	ON	ON	OFF	OFF	$V_d/2$
0	OFF	ON	ON	OFF	0
-	OFF	OFF	ON	ON	$-V_d/2$

2.5.3 Flying Capacitor Inverter

The flying capacitor (FC) has a modular structure, just like the CHB. Its presence in the industry is less frequently found as compared to CHB and NPC. This is so because higher switching frequencies are typically required for capacitor balancing, usually greater than 1200 Hz [29]. Another drawback is that configuration requires initialization of the flying capacitor voltages. Fig 2.4 is a typical structure of a single phase flying capacitor inverter.

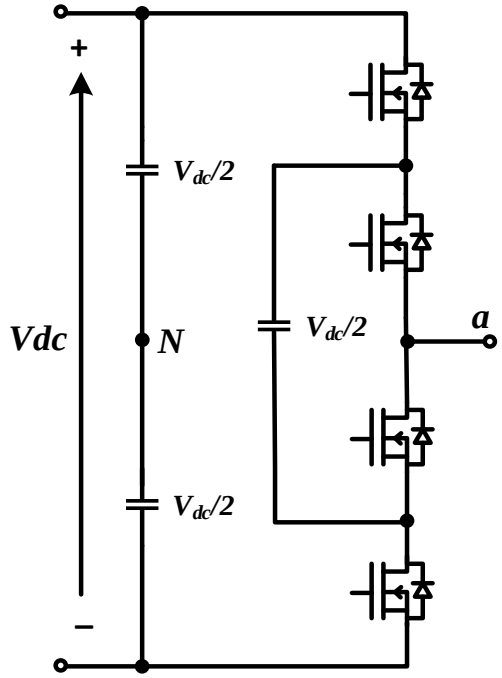

Figure 2.6. A single phase flying capacitor inverter.

Table 2.4. Single Phase Flying Capacitor Inverter Switching States

switching state				Inverter Terminal voltage
S_1	S_2	S_3	S_4	
1	1	0	0	$V_d/2$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$-V_d/2$

There are significant differences between the NPC and CHB inverters which are worthwhile to note:

a) The NPC inverter topology is more appropriate for back-to-back regenerative applications, while the CHB needs considerably higher number of semiconductor devices to achieve regeneration.

b) The CHB inverter attains higher voltage and higher power levels than NPC because of the higher number of semiconductors employed.

c) The NPC has a smaller footprint because of its simple circuit structure. The CHB structure becomes even more complex as the number of levels increases, thereby increasing its footprint.

2.6 Multilevel Inverter System Component Count

The multilevel inverter comprises of voltage levels, active switches, and DC sources / DC capacitors. The number of active switches and dc sources depends on the voltage level that is to be considered. Table 2.5, 2.6 and 2.7 are the component counts of a cascaded H-bridge, diode clamped (NPC) and flying capacitor inverters, respectively.

Table 2.5. Component count of a 3-phase multilevel cascaded H-bridge inverter

SN	Voltage Level	Active Switches	Clamping Diodes	DC sources
1	3	12	0	3
2	5	24	0	6
3	7	36	0	9
4	9	48	0	12

Table 2.6. Component Count of a 3-Phase Diode Clamped (NPC) Multilevel Inverter

SN	Voltage Level	Active Switches	Clamping Diodes	DC Capacitors
1	3	12	6	2
2	4	18	18	3
3	5	24	36	4
4	6	30	60	5
5	7	36	90	6

*All diodes and active switches have the same voltage ratings

Table 2.7. Component Count of a 3-Phase Flying Capacitor Multilevel Inverter

SN	Voltage Level	Active Switches	Clamping Diodes	DC Capacitors
1	3	12	0	5
2	4	18	0	12
3	5	24	0	22
4	6	30	0	35
5	7	36	0	51

Table 2.8 shows a simple equation to determine the number of active switches, clamping diodes, dc sources / capacitors, and balancing capacitors per phase of multilevel inverters.

Table 2.8. Equation Table for Multilevel Inverters

SN	Topology	Cascaded	Diode Clamped	Flying Capacitor
1	Power semiconductor switches	2(*m*-1)	2(*m*-1)	2(*m*-1)
2	Clamping diodes per phase	0	(*m*-1) (*m*-2)	0
3	DC bus capacitor	(*m*-1)/2	(*m*-1)	(*m*-1)
4	Balancing capacitors per phase	0	0	(*m*-1) (*m*-2)/2
5	Voltage unbalancing	Very small	Average	High
6	Applications	Battery systems, motor drives systems, PV, fuel cells	Motor drive systems, STATCOM	Motor drive systems, STATCOM

*****where *m* represents the number of levels

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CHAPTER THREE

MULTILEVEL CASCADED H-BRIDGE INVERTER STRUCTURE

3.1 Introduction

Power devices are the building block of power converters. The essential task of power electronics is to ensure that the current and power consumed by power converters and their loads meet the requirements of electric energy sources. Figure 3.1 shows a fundamental description of power electronics.

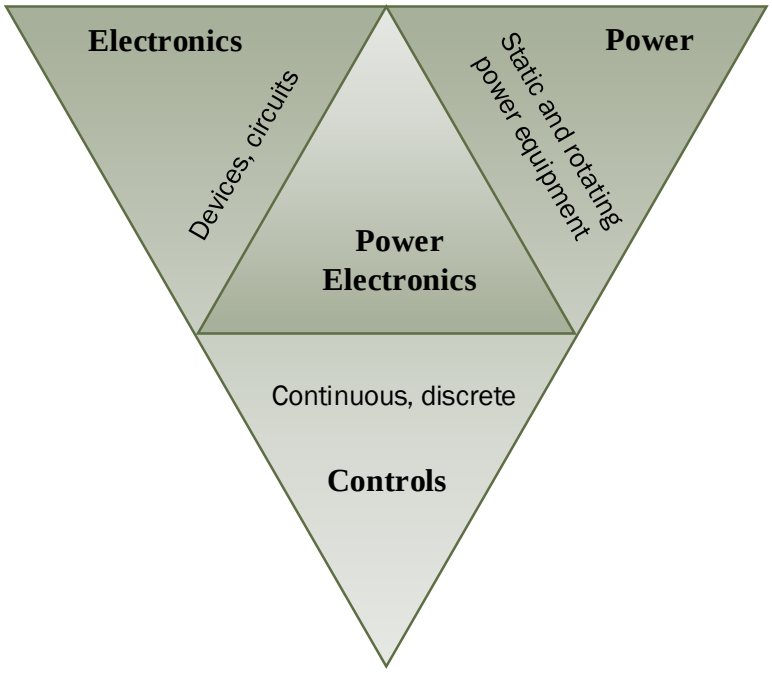

Figure 3.1. Fundamentals of power electronics.

The functionality of a multilevel cascaded H-bridge inverters is made possible by power electronics. Series connections of power semiconductors and dc sources form the main circuitry of a multilevel CHB inverter. Multilevel CHB inverter is of great interest because of high demand

for medium-voltage high-power inverters. It is preferred because of its power-quality operational characteristics and modular structure [1].

3.2 Topology description

Multilevel CHB is a series connection of H-bridge power cells. The CHB is also known as a multi cell inverter where each cell comprises of a single-phase three-level H-bridge inverter. It is important to know that this inverter topology is operated using power semiconductor devices. These semiconductors serve as the main power electronics interface of the system. Medium voltage semiconductor devices are selected for the operation of the inverter. These semiconductors includes SiC MOSFET and Si IGBT – they are investigated and evaluated for better performances during operation in a BESS. This is the main focus of this thesis work.

Figure 3.2 is a CHB inverter topology under investigation. It is a three phase nine-level CHB inverter with BESS composed of power semiconductors, dc-link and an isolated dc voltage source. The dc voltage is generated by the BESS. A synchronous buck/boost converter is attached to the CHB. The synchronous buck/boost converter stage is used to boost the battery voltage at the battery bank, charge the batteries in the system, and regulates the dc bus voltage as it absorbs energy from the battery storage connected to the converter [2].

The inverter topology is a transformerless topology. There is no need for a bulky 60 Hertz step-up transformer. Although using a transformer will provide convenient isolation, it will also lead to higher leakage inductance. Without a transformer, there is the possibility of higher power transfer capability with minimized losses. This transformerless topology has the capability of integrating low voltage battery strings into the modular structure. Scaling up to higher voltages can simply be done by addition of switches. Each phase of the inverter consists of four cells.

The output of the nine-level CHB topology is 4E, 3E, 2E, E, 0, -E, -2E, -3E, and -4E. The output voltage in single phase configuration V_{AN} is the summation of v_{H1} to v_{HN}, where N is the number of CHB cells. The maximum output voltage $V_{AB(\max)}$ is obtained with the expression:

$$[V_{AB(\max)} = 0.612\ (m-1)\ Vdc] \quad (1)$$

Where: m = 2N+1 and is defined as the number inverter level, N is number of H-bridge cells per phase.

The total number of active switches for a three-phase can be calculated using:

$$N_{sw=}\ 6(m-1) \quad (2)$$

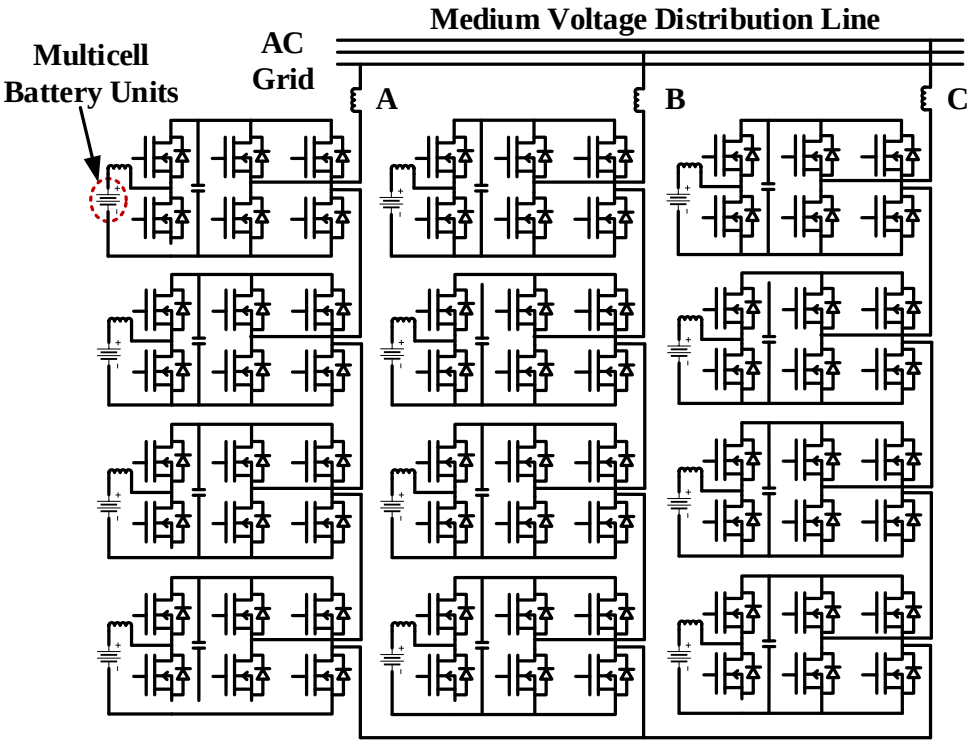

Figure. 3.2. A three-phase nine-level CHB inverter.

3.3 Topology Operations and Benefits

The multilevel cascaded H-bridge inverter with a BESS can maintain smooth and continuous operation even for the most severe voltage-sag conditions. This verifies that the system

is readily available and flexible. It is known that sometimes electricity generation companies experience stability issues like voltage and frequency fluctuations. In events of this nature the BESS can release active power, it can also absorb active power from its installation. This is a mitigation measure for such voltage and frequency fluctuations in a power distribution system [3]. Because of the modular structure of the inverter, only a few batteries can be taken out of service in case of in the event of overheating or battery fault. During open-circuit or short-circuits faults in the cell, the fault tolerance-continuous operation is another advantage that is considered in this topology. This is a plus in terms of the reliability and availability of the system [4]. This inverter topology is also of a great benefit to utilities during peak shaving, harvesting the benefit of BESS in the distribution system. During peak periods of electricity demand, utilities can reduce generation cost by discharging electricity which was stored at off-peak periods.

3.3.1 Peak Load Shaving Using BESS

Grid-connected renewable power generation systems have been cutting edge research a topic in the power generation industry. This is because of the problems associated with fossil fuel usage in power generation. One major problem with fossil fuel is the emission of carbon dioxide (CO_2) into the atmosphere. Interests in BESS is growing because of the numerous benefits it can offer to grid-connected applications and power generation [5]. Peak shaving using BESS can eliminate peaks and valleys combined power demands in the grid system. It is proven that the peak-shaving approach can guarantee that there are no constraints violations as to the state of charge of batteries. The batteries in the system can also take part in volt-var optimization where the reactive power is controlled at the point of common coupling with power distribution grids [5].

In grid systems, peak load is an inevitable phenomenon. It happens infrequently, usually for a short period of time in the day. To tackle this problem, power additional capacity is usually

employed into the grid, which is the traditional method. This method is not economically reasonable because of the type of power generators used to generate more power during peak periods since the utility company only needs a few hours in a day to sustain peak demands [6]. High fuel consumption CO_2 emissions during combustion, early deterioration of generators/equipment, and the high cost of maintenance are some of the drawbacks of using fossil fuel generators [7]. Peak loading shaving using BESS is a better method to use to mitigate related issues with fossil fuel generators. BESS plays an important role for utilities in terms of peak load shaving strategy, and it is worthwhile to differentiate between effects and benefits of BESS for grid applications. The BESS market is broad and spans from transmission and distribution (T & D) grid operators, power producers, electricity brokers, down to consumers [7], [8]. The benefits of BESS can however be classified into three groups which are: grid operator benefits, end-user benefits, and environmental benefits

1) Benefits to the grid operator:

a) Power quality: Electricity demand and generation is a major challenge in the utility sector. They strive to maintain a balance between the amounts of power generated versus power demanded. If there is a mismatch, there could be possible voltage fluctuation, grid system instability and sometimes total black out. These mismatch issues can lead to reduced power quality and fatigue on generators [9], [10].

b) Cost reduction: Utilities that do not have storage systems sometimes might generate more electricity than demanded, and ends up as waste. This excess will still add up to the per-unit cost of electricity generation which is not in favor of utilities because there was no demand and thus no profit made. For this reason, grid designs will try to match supply and demand which sometimes cannot be perfectly feasible. But introducing a storage system will help reduce energy waste during

off-peak periods. This is so because the excess electricity generated during off-peak periods can be used to charge the BESS. And during peak periods the BESS can be discharged to provide demand balance. This approach will result in the reduction of additional electricity production cost and maintenance if using fuel generators.

c) Renewable energy integration: Carbon emissions during fossil fuel combustion is a serious environmental problem. The use of BESS is developing to help sustain the environment by reducing CO_2 emissions into the atmosphere [11].

d) Power reliability: Power reliability is a crucial issue in electricity generation. Peak demand occurs almost every day, and increases as the day goes by. This significant change can affect grid reliability. Therefore utilizing BESS for peak load shaving purpose will improve power reliability [12].

2) Benefits to end-users – Peak shaving using BESS to balance peak demand improves the quality and reliability of power distributed to end users. This is because the BESS can deal well with reactive power in the distribution system.

3) Benefits to the environment **–** Carbon emission reduction***:*** Because of the extra fuel that needs to be consumed/burnt during peak demand periods, more carbon is released into the environment during this process. Peak loading shaving BESS will ensure more efficient operation of power plants with reduced carbon emission and load variability.

BESS stands to be promising compared to other storage types. BESS delivers peak shaving service for a time scale of minutes to a few hours (less than 5 hours) [7], [13]. The main purpose of BESS is to reduce per kWh energy production cost and peak electrical demand by utilizing the storage system. To investigate the economic feasibility of BESS for peak shaving, three parameters

can be considered and analyzed, which includes: peak demand charge, price differencing between high and low electricity pricing, and the investment cost for BESS

Integrating BESS to the grid is a potential strategy of peak shaving. In industries and residential buildings BESS can also be used for peak shaving purposes. BESS method of peak shaving involves the process storing energy by charging the batteries of the system when the demand for power is low, this is called the off-peak periods. When power demand is high, the stored energy is discharged into the system, this is called the peak period [14]. Fig. 3.3 illustrates the charging and discharging schedules of the system.

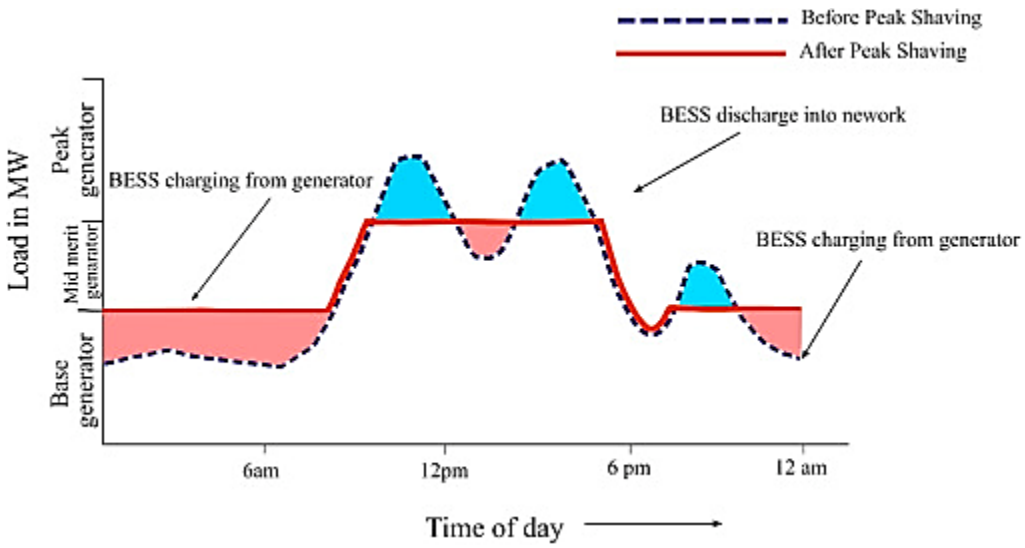

Figure 3.3 Peak load shaving using BESS [13].

The factors that affect the use of BESS for peak shaving can be divided into three categories:

a) Sizing of storage system: BESS plays a significant role in grid operations, and as such, the sizing of the BESS is necessary for correction operation of the grid. If BESS is installed at a random and non-optimized size, it can increase cost, system losses, and larger energy storage

system capacity. But if the sizing of BESS is balanced, then it can accrue maximum financial benefit for the grid operator [7].

b) Optimum operation of BESS: A key challenge in the operation of BESS as a peak shaving strategy is its optimum operation. This factor has to do with the controls/commands of the system in regards to when to "charge" and "discharge" stored energy. In [15], the BESS was configured with two commands which were to charge at low demand when demand is below 10 kW, and discharge at peak demand when demand is above 400 kW – that is BESS will accept a charging command only if the state of charge is below 10%. And the BESS will stop charging when the state of charge goes above 90%. Also in [16], a control was developed for the BESS state of charge by setting its demand limit from the grid. The control was developed in a way that when the aggregate demand exceeds its demand limit, the energy stored in the system will be discharged to meet excess demand from the grid. And when demand is less, the storage systems absorbs power from the grid to charge the batteries.

c) Economic feasibility analysis: The implementation of BESS is associated with high capital cost, and is a major barrier. For this reason, a thorough economic feasibility study is needed. All cost of investment and benefits should be taken into considerations for peak shaving to be justified in a grid-connected system. Economic benefits of BESS to the utility company are highlighted as follows:

1) Grid energy loss reduction. [17]

2) Injection/absorption of reactive power to maintain grid voltage. [18]

3) Reducing the impact of peak period electricity demand in the grid system – This is so because transmission and distribution system upgrade is deferred, and the system can be used for a longer

time. This is a delay strategy for the need of costly upgrades in the transmission and distribution system. [19]

4) Displacement of less efficient and expensive peaking plants used to meet the day-to-day increase on peak demand [20]

5) Carbon dioxide emission reduction – BESS provides peaks shaving services to the grid at lower carbon dioxide emissions. This is because the combustible peaking plants are being substituted with BESS.

6) Economic arbitrage – taking advantage of electricity price difference through peak shaving. The energy stored in BESS during off-peak periods when electricity price is low can be sold to customers during peak demand periods when prices are high.

The services provided by BESS is not limited to peak shaving. BESS provides several other types of services which are conditions for maintaining reliability and stability of the grid system – reactive power support, voltage regulation & support, frequency control, spinning reserve, and emergency power backup during an outage. Figure 3.4 [21] shows the different types of BESS for grid-connected application from low-voltage to medium-voltage integration level. These application families include: Ancillary service, energy trade, behind-the-meter, and grid support and investment deferral.

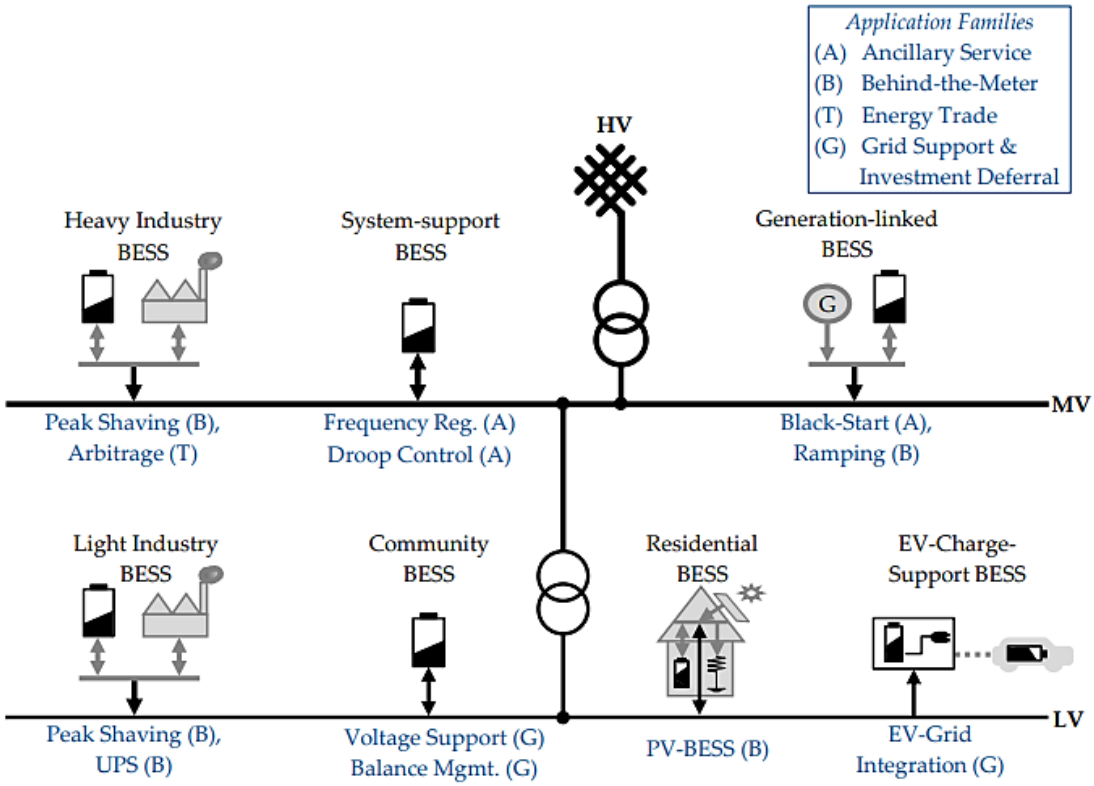

Figure 3.4 types of BESS for grid application according to voltage levels [20].

3.3.2 Average Electricity Rate versus Return of Investment (ROI) Using BESS

It is true that where you live in the US affects your electricity rate. The latest available data which was in July 2018, shows that the average residential price of electricity in US is 13.12 cents per kilowatt hour (kWh) [22]. The data holds that Louisiana pay the lowest average residential electricity rates of any state in the country – 9.37 cents per kWh. And Hawaii residents pay the highest electricity rates in the country – 33.45 cents per kWh. The average business in US consumes 6,278 kWh of electricity per month and thus receives a bill of nearly $655 each month. Although these rates vary greatly by the type of industry and function of the company.

Because the energy market is volatile, energy supply prices may fluctuate throughout the year. There could be random fluctuations as the case maybe, but there are few major factors that determine how much customers pay for electricity they consume. These factors include:

1) Energy usage time – in some cases utility companies provide discounts for time-of-use which could span from 9 pm to 6 am the following day.

2) Energy usage month – during the summer, rates can be higher in the warmer states due to high energy demand required for cooling homes and businesses. Winters rates are presumably lower.

3) State of residence – electricity rates vary from state to state and among utility companies/areas irrespective of the energy choice of the state.

4) Energy production has a couple of different source like coal, natural gas, nuclear and renewable sources. BESS plays an important role in all of these sources mainly to meet the conditions of grid operations. A recent review reveals the high number of publications regarding BESS, and it exceeds any other types of energy storage technology. This is because of the advantages over other forms of energy storage technologies. BESS is fast in its response time, it has low self-discharge, high efficiency, and scaling feasibility because of its modular structure compared to other competing storage technologies [23].

BESS market growth/development and future cost analysis prediction was conducted in [24, 25] for electric vehicles and stationary/grid system integration. The analysis show similar trend in both cases with a significant decline in cost of battery cell production capacity. The return of investment was proposed for the economic analysis of a residential BESS [26, 27]. A simplified cost-benefit analysis is presented in Eq. (3):

$$ROI = \frac{A_{return} - C_{inv}}{C_{inv}} = \frac{(P_{APL} - C_{OPEX} - C_{degrade}) - C_{inv}}{C_{inv}} \quad (3)$$

Where: A_{return} is the overall project return, C_{inv} is investment cost, P_{APL} is the annual profit which may come from direct profit generation like arbitrage energy trade, C_{OPEX} is operational cost, and $C_{degrade}$ is the degradation related replacement cost of batteries. Other factors that may be considered on the cost side include: maintenance, insurance, taxes, interest rates, grid fees and warranty contracts [21]. Table 3.1 presents an overview of cost and profitability drivers for technical valuation of BESS.

Table 3.1. Cost and Profitability Drivers for BESS

SN	Cost factor	Symbol	Major Contributors
1	Investment cost	C_{inv}	Cost of storage (battery, periphery, casing) cost of grid coupling (power electronics)
2	Profit and savings	P_{APL}	Application-specific profit or savings (power-related, energy-related and/or reliability-related)
3	Operational cost	C_{OPEX}	Conversion losses (power electronics, battery) auxiliary consumption (TMS, control and monitoring) other operational cost (labor, insurance, maintenance)
4	Degradation and replacement cost	$C_{degrade}$	Battery degradation (capacity fade, resistance increase) replacement cost for fatigued materials (e.g., battery, power electronics)

3.3.3 Life expectations of a grid-connected inverter

The characteristic life of a grid-connected inverter is a key factor to estimate the payback period of the inverter. For electric equipment, a key index for checking reliability is the mean time to first failure (MTTF). Technologies of current commercial grid-connected inverters that are available are said to have life expectancy of about 10 years [28]. Factors that affect the characteristic life of an inverter include the following:

a) Turn On/Off cycles

b) Average on-time cycles

c) The type of load – constant loading or variable loading (more fatigue)

d) Use condition – temperature, moisture, radiation

The life expectancy of batteries is between 5 to 10 years. As such there is the possibility of replacing batteries at least once before the end of the lifetime of the inverter. Batteries with longer lifetime will generally cost more because of the superior materials used in production stage [29]. Factors which affect the lifetime of a battery are:

a) Its ambient temperature

b) Undercharging/overcharging

c) Expansion and corrosion

d) Load sizing

e) Number of discharge

f) Age – battery chemical depletion

g) Lack of maintenance

3.4 Bidirectional Converter

The battery energy storage system is attached to bidirectional converter. This converter absorbs energy from the grid – working as a rectifier. When it is time to discharge the stored energy back to the grid, the bidirectional converter works as an inverter at a certain given reactive and active power commands [30]. The output voltage and current of the convert are measured, where the voltage is used directly. And the output current is compared to the reference current signal so that it provides voltage reference to a pulse width modulator which produces gating signals for the semiconductor switches used in the converter.

3.5 Control Strategy

Modulation technique in power electronic converters is a key performance driver, and therefore should be carefully selected. There are different types of multilevel inverter modulation techniques, which are classified according to their switching frequencies. Fig 3.5 illustrates this classification. For high switching frequencies, one method that is used most frequently is the carrier-based sinusoidal pulse width modulation (SPWM). The high switching frequency is characterized by several commutations of the power semiconductor in use in one period of fundamental output voltage. While other methods with low switching frequencies are characterized with one or two commutations of the power semiconductor in one cycle of the output voltage. An example of this method is the space-vector control (SVC). The SPWM method uses a phase-shifting technique which allows for the reduction of harmonics in the load voltage [31]. SPWM is the method used in the topology under investigation.

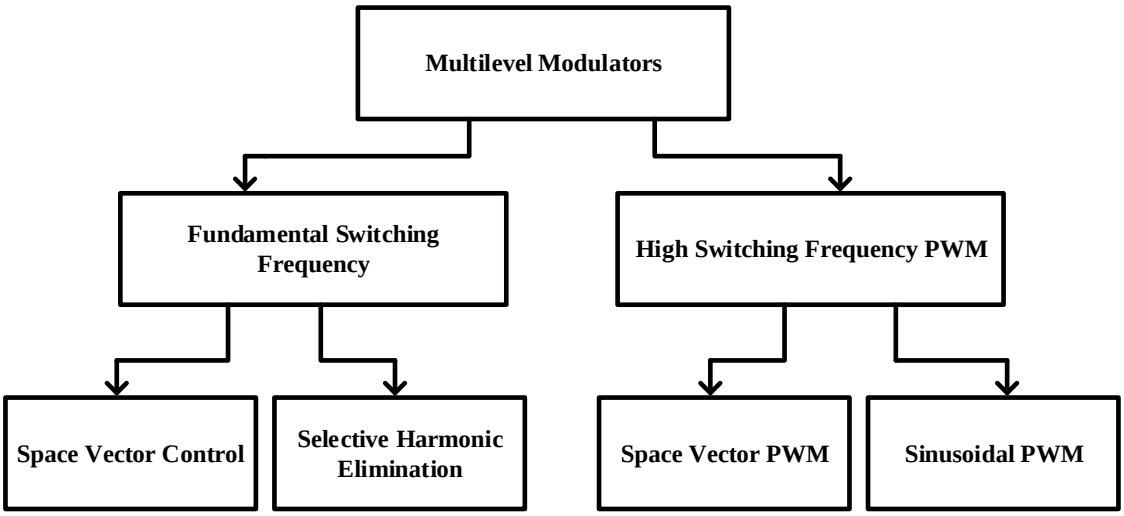

Figure 3.5. A modulation classification of multilevel inverters [30].

3.6 Controller Design

The controller manages the entire inverter system. During operation, the controller directs, regulates, and the commands other subsystems which includes charging and discharging of the batteries. The conversion form dc-to-ac is controlled by a decoupled current control. This is responsible for charging and discharging of the batteries. The inverter is the current source for sinking the grid power to charge the batteries. An active power control is introduced to control converter cells [32], [33]. The ideas is to inject a zero sequence voltage reference v_0^* into the reference voltage. The implementation is detailed in [2], and using the following equation:

$$v_0^* = \sqrt{2}V_0 \sin(wt + \emptyset_0) \quad (3)$$

V_0 is the amplitude and $\emptyset_0$ is the phase angle.

The active power control is of two parts which are:

1) Active-power control of individual converter cells
2) Active-power control of all the

In Fig 3.6, at the dc side, the power handling of the twelve battery banks are equal. There is a feedback loop that ensures that the dc side power command of each cell, P_{un} is equal to the individual command at the ac side, P^*_{un} as shown in fig. 3.6

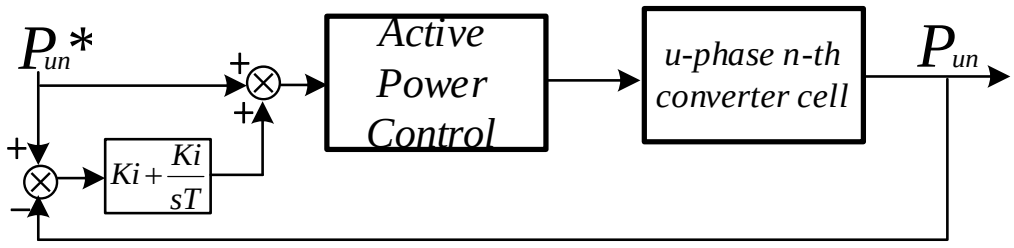

Figure 3.6. Active power control block.

The decoupled current control is used to charge or discharge the batteries at the battery bank of each cell after a power command P^* is initiated. In fig 3.7 the current signals before the filter are sensed for each. The grid voltages are also sensed for each phase and the dq transformation is applied on the sensed current and voltages of the phases. The reference current $i_d{}^*$ is computed to be proportional to the power command P^* [32], [33].

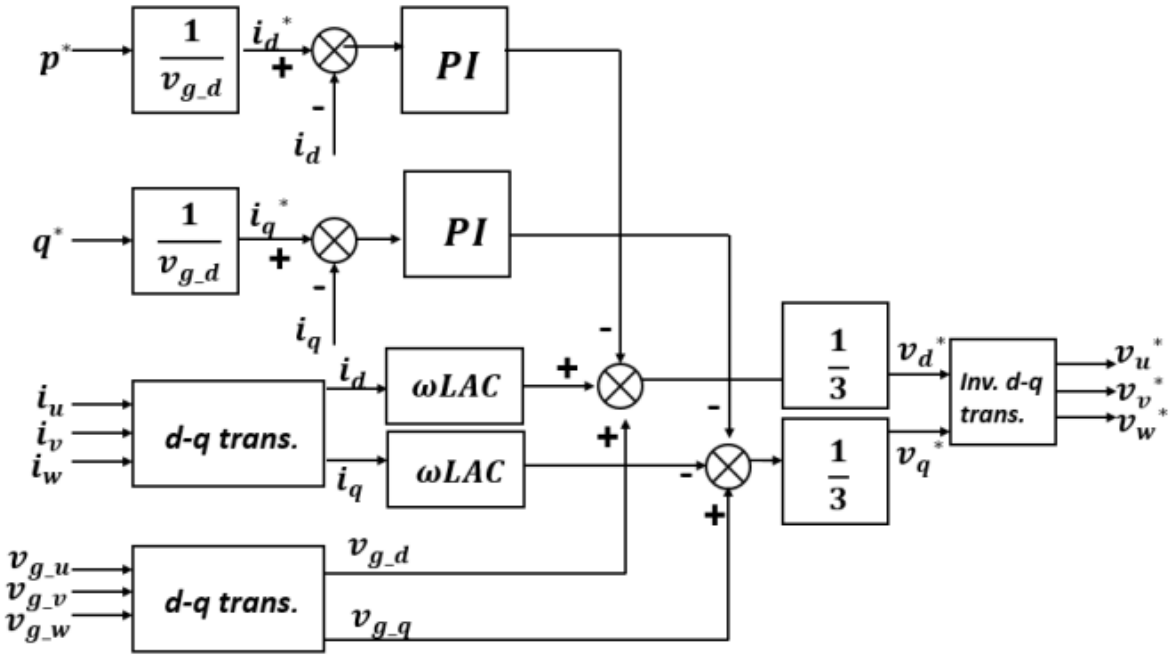

Figure 3.7. Decoupled current control block [5].

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CHAPTER FOUR

THEORETICAL ANALYSIS

4.1 Power losses

Power loss is a vital parameter in investigating power electronic systems. A precise computation of power losses significantly impacts the economic and technical assessment of the system. Some of the basic parameters to consider in the design of multilevel inverters are the operating temperature, heat-sink sizing/cooling system, failure rate and mean time to failure (MTTF). These factors depends on the inverter losses when in operation [1]. Multilevel inverters have various applications. One advantage for its vast applications is that it is characterized with low harmonics at low switching frequencies [1].

The behavioral study of power semiconductors devices is important because of the key role it plays in multilevel inverters. Practically, loss estimation in multilevel inverter is not simple, but substantially more difficult compared to a two-level inverters [1]. Multilevel inverter loss estimation involves more process primarily because of the number of devices present in the inverter.

The power losses in semiconductor devices primarily consist of conduction loss and switching loss. There is also a leakage loss which is not significant. These power devices have resistive component that dissipates power when current flows through it during conduction. The resistive component in the device is called as the on-resistance. Conduction loss is inversely proportional to die size of the transistor. If the die size of the transistor is large, the on-resistance will be low which means less conduction loss, and vice versa. Switching loss is seen when the

semiconductor device transitions from off to on state and vice versa. During this process, energy is stored and dissipated by parasitic capacitance throughout switching transitions [2].

Switching loss in power semiconductors has direct proportion to the applied switching frequency. The physical size of a transistor has direct proportion to its capacitance, meaning that if the transistor size is increased, the capacitance will also increase. These factors increase the amount of switching losses in the device. For example, a MOSFET with bigger area will have a lower on-resistance which will result in a low conduction loss. Conversely, the bigger area of the MOSFET will buildup parasitic capacitance, and this will increase switching loss [2]. The challenge here is how to create a balance between conduction and switching losses which sums up to be the device's total power loss. Power loss calculation is associated with several other factors as semiconductors differs from one another. Converter power levels affects the amount of power loss to be expected, the semiconductor characteristics also impact on power losses.

In the literature, different methods have been suggested to calculate the power losses in multilevel inverters. Some of these power loss calculation techniques depend on models generated via simulations. Some others are mathematical-based analysis. In [1] and [3] a general method for calculating switching and conduction losses was recommended for (MMC). In [1], a three-phase nine level cascaded H-bridge inverter was designed to model the inverter loss. The conduction loss of the inverter is calculated by introducing a coefficient into a conduction loss equation that considers the percentage on-time of an active device for one period. In most power loss estimation methods, the results are narrowed to their simulation outputs.

In this thesis work, the Saber simulator is used to estimate the conduction and switching losses of a nine-level cascaded H-bridge (CHB) inverter integrated with (BESS). The proposed

loss estimation method is supported with theoretical analysis to compare with simulation results, and to gauge percentage error.

4.1.1 Conduction Loss

The losses that a power semiconductor experience when it is on and current flowing through it is called conduction loss. In multilevel CHB inverter, the total conduction loss in the inverter is proportional to the sum of all cascaded cells that make up the inverter [4]. Conduction loss can be calculated theoretically and by simulation. One major factor in calculating conduction loss is knowing the conduction time of the device which is challenging to achieve [1]. The integration of the instantaneous power losses over specified switching cycle will give an average value of conduction losses. In [5], the conduction losses for MOSFETs is calculated from the equation:

$$P_{CONDMOSFET} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{CM}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (R_{DSon} \, . i^2(t))dt = R_{DSon}. I_{rms}^2 \quad (4)$$

Where: R_{DSon} is the on-resistance and I_{rms}^2 is the rms value of the on-state current of the MOSFET.

Again, in [1] conduction loss is calculated using:

$$P_{CON} = V_{CE(ON)} * I_{C(ON)} * D_{CON} \quad (5)$$

Where: $I_{C(ON)}$ and $V_{CE(ON)}$ are collector current and collector-emitter voltage. D_{CON} is the correction coefficient. The value for D_{CON} can be found using:

$$D_{CON} = \frac{t_{Level-i}}{T} \quad (6)$$

Where: T is the period and $t_{Level-i}$ is the total ON state time of the switch in Ith level.

Conduction loss contributes significantly to total power loss. The quest for reduced size and weight of converters in terms of its filter components have led to switching power converters

at high frequencies. Switching at high frequencies will create more switching losses. Thus, if the converter has a reduced conduction loss, then this gives rise to concerns regarding switching loss. This is why selecting the right power device for the right converter application is important for creating a balance between conduction losses and switching losses.

In [6] the conduction loss of an IGBT device is calculated by the given expression in Eq. (7)

$$P_{COND\ IGBT} = \frac{1}{T_0}\int_0^{T_0/2}(V_{CE0} + r\hat{\imath}sin\,(\omega t)) * \hat{\imath}sin(\omega t) * (\frac{1}{2}(1 + m\,sin(\omega t + \varphi)))dt$$

$$= \frac{1}{2}(V_{CE0}*\frac{\hat{\imath}}{\pi} + r * \frac{\hat{\imath}^2}{4}) + m * cos\,\varphi * V_{CE0}*\frac{\hat{\imath}}{8}+\frac{1}{3\pi} * r\hat{\imath}^2) \quad (7)$$

Where V_{CE0} is the zero-current collector to emitter voltage, r is the collector to emitter on-state resistance, m is modulation index, and $\hat{\imath}$ is the peak current.

4.1.2 Switching Loss

Switching loss is the summation of a device's switching on and off energies multiplied by the switching frequency. In other words, switching loss is the energy dissipated when the power device is turning on and off during switching operation. Switching loss is also an important part of a converter's total power loss. Power semiconductors have turn-on (E_{on}) and turn-off (E_{off}) energy losses. The antiparallel diodes attached also have turn-on and turn-off losses. The turn-on losses of the diode are quite negligible because of swift conduction (forward biased). These turn-on losses contribute less than 1% of the diode's turn-off loss [7].

In Figure 4.1, a voltage source inverter (VSI) topology is presented with an H-bridge configuration. The switching losses in the H-bridge is seen in two of the devices which are S_1 and

S_4. Switch S_2 and S_3 do not have switching losses, only the diodes conduct during one switching cycle transition. S_1 and S_4 have turn-on and turn-off losses in one switching cycle [8]. Hence:

$$P_{sw} = \frac{4}{2\pi} \cdot f_s \cdot E_T \tag{8}$$

Where: f_s is the switching frequency and E_T is the total energy loss.

In Eq. (8), switching loss is expressed as the integration of all the turn-on and turn-off switching energies at the switching instants. In the equation, variable switching time is considered and integrated:

$$P_{SW} = f_{sw} \cdot \frac{1}{T_0} \int_0^{T_0/2} (E_{on} + E_{off})(t, \hat{\imath}) dt \tag{9}$$

The summation of conduction and switching losses gives the power loss of the device:

$$P_{loss} = P_{cond} + P_{sw} = R_{DSon} \times I_{rms}^2 + (E_{on} + E_{off}) \times f_{sw} \tag{10}$$

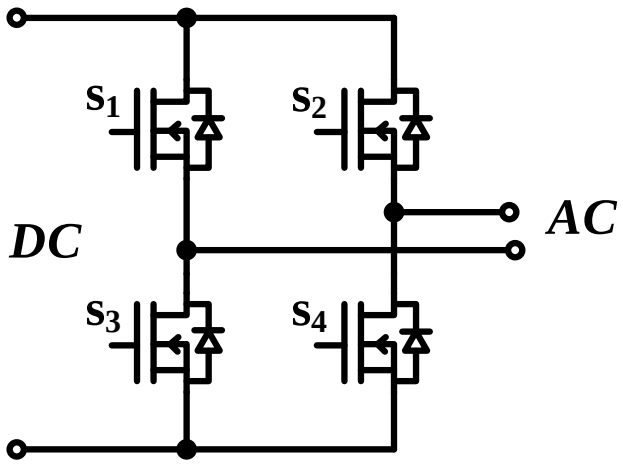

Figure. 4.1. Voltage source H-bridge inverter

Switching losses in power devices cannot be calculated with total accuracy. Be that as it may, knowing the ON-state and OFF-state during switching transitions can give more accurate estimations [9].

During turn-on operation of power semiconductors, a gate pulse is applied to increase the gate voltage slowly. The amount of the gate voltage that is applied to the device is relative to the device's input capacitance and the gate resistance. For example in Figure 4.1, the instance at which the gate voltage at S_1 reaches its threshold V_{th}, the current in the device begins to increase quickly. At this point, the current in the freewheeling diode located at S_4 slowly transfers to the device. The speed at which the current increases can be determined by the device rise time which is specified is datasheets [10]. Figure 4.2 shows an ideal switching behavior of SiC MOSFET and Si IGBT at turn-on (t_r) and turn-off (t_f).

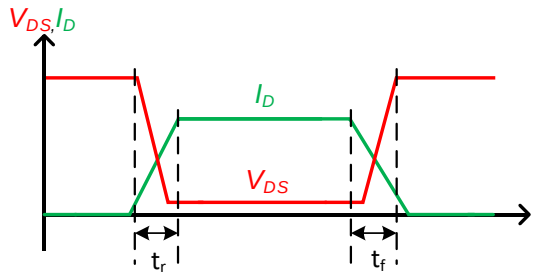

Figure 4.2 (a) rise/fall time of SiC MOSFET

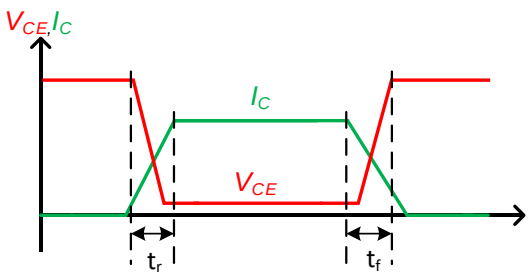

Figure 4.2 (b) rise/fall time of Si IGBT

Practically, there are five significant elements that affect the behavior of switching losses. They are: switching current, junction temperature, gate resistor, blocking voltage, and stray inductance [8].

4.2 Inverter Efficiency

The quest for power inverters that are efficient has been the focus of researchers in the power electronics industry. It is assumed that the global energy demand is expected to increase by nearly twice of what it is now by 2050 [11]. One important component that affects an inverter efficiency is the power semiconductor in use – its behavior during operation. Power MOSFETs and IGBTs are ideal devices that can be used in power inverter applications. Analyzing the operation of a power inverter, we can assume that the efficiency of the inverter will be a total of every component that make up the system, especially the power semiconductors, which constitute the most part of the inverter loss [12]. Therefore, it is important to properly analyze power semiconductor devices to determine best choice for an inverter system.

In this thesis work, the efficiency of the inverter system is calculated using:

$$\text{Efficiency, } \eta = \frac{Outout\ Power}{Input\ Power}\ x\ 100\ \% \tag{11}$$

$$\eta = \frac{Input\ Power - Losses}{Input\ Power}\ x\ 100\ \% \tag{12}$$

$$\eta = 1 - \frac{Losses}{Input\ Power}\ x\ 100\ \% \tag{13}$$

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CHAPTER FIVE

METHODOLOGY AND SEMICONDUCTOR DEVICE PERFORMANCES

5.1 Introduction

This paper describes the comparative study of Si IGBT and SiC MOSFET in a cascaded H-bridge inverter. A co-simulation interface between Saber and Simulink is used to investigate the performance of the devices in the inverter system. The voltage level of the power semiconductor devices used for this investigation were selected to be 1200 V and 1700 V for both Si and SiC. These devices were characterized in Saber to create a real-world model. All other system components and controls are designed in Simulink. The inverter is simulated and different switching frequencies and temperature range. Results were obtained for the power loss, efficiency, thermal performance, and total harmonic distortion (THD) of the inverter system.

In most inverter simulation designs, the semiconductors used are mostly ideal devices. This does not give real life situation of the inverter systems. Therefore it is important to characterize practical devices that can give practical results. Saber is used to create real case model of SiC MOSFET and Si IGBT. It provides real-world device as against an ideal device. The performances of SiC and Si are shown in the results. Power losses and efficiency total harmonic distortions (THD) are great factors of interest in inverter operation. Some of these factors are to a great extent dependent on the switching devices. The investigation is to validate for the performance of a 5 level cascaded H-bridge inverter. One advantage of this simulation method is the accuracy of simulation models which is shown in the characterization result.

5.2 Methodology

In this paper, the following methodologies are followed to conduct the study. First, power devices are characterized using saber IGBT tool and then the multilevel cascaded H-bridge inverter is designed using the practical models of switches. Finally Saber-Simulink cosimulation is performed to validate the operation of the inverter system and the results are collected.

5.2.1 Compact modeling of SiC MOSFET and Si IGBT

The Saber power MOSFET and IGBT characterization tools were used to build and characterize models from the device datasheets. The models were built at temperature scales [1]. The gate voltages of both SiC MOSFET and Si IGBT were measured with a test circuit in Saber to verify the characterization at different gate voltages. Other SiC MOSFET devices measurements and plots such as drain current versus gate-to-source voltage, ON resistance versus drain current, diode current versus voltage, capacitance, gate charge, and diode reverse recovery were also characterized. On the other hand, Si IGBT device measurements and plots which were characterized include the collector current versus gate-to-emitter voltage, diode current versus voltage, capacitance, gate charge, tail current, and diode reverse recovery. Figure 5.1 (a) shows the Saber characterization tool window where SiC MOSFET was characterized for its drain-to-source current (I_{DS}) vs. gate-to-source voltage (V_{GS}), drain-to-source current (I_{DS}) vs. drain-to-source voltage (V_{DS}), and capacitances vs. drain-Source voltage (V_{DS}). The I_{DS} – V_{DS} is characterized with sweeps of different $V_{GS.}$ The input capacitance (C_{iss}), output capacitance (C_{oss}), and the reverse transfer capacitance (C_{rss}). Similarly, Si IGBT was characterized for its collector current (I_C) vs. emitter-to-gate voltage (V_{GE}), collector current (I_C) vs. collector-to-emitter voltage (V_{CE}) and capacitances vs. collector-to-emitter voltage (V_{CE}) as shown in figure 5.1 (b). Appendix A shows the characterization tool with all other features embedded.

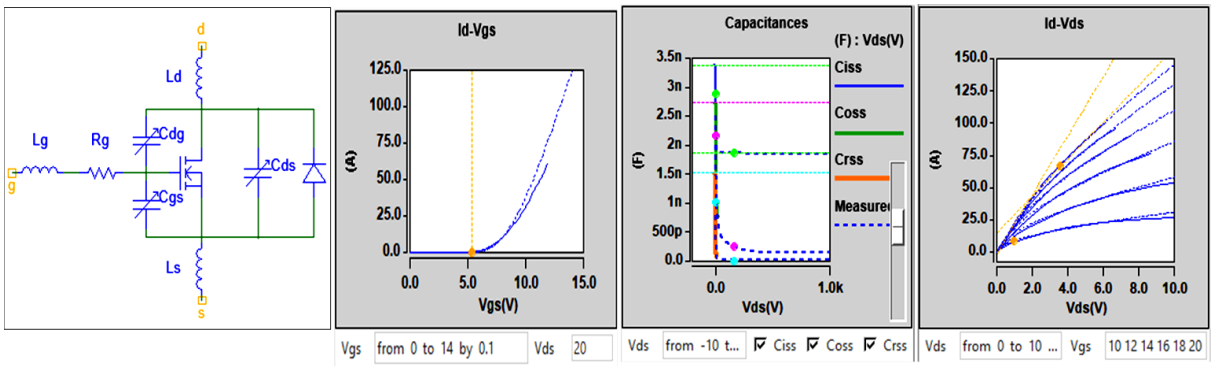

Figure 5.1(a) MOSFET characterization tool window.

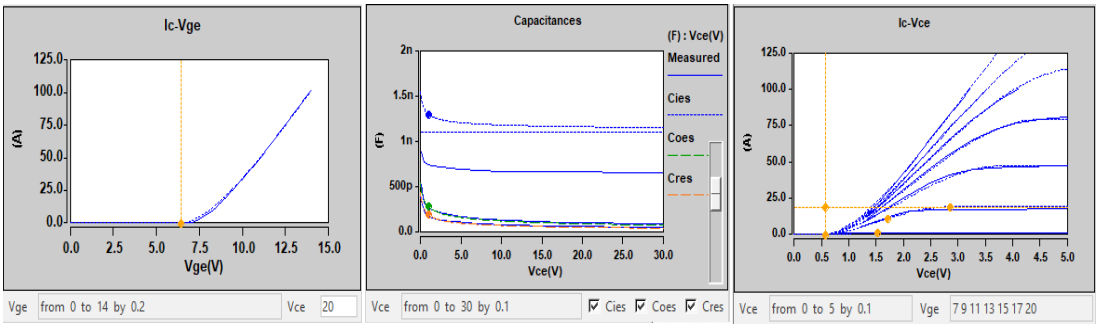

Figure 5.1(b) IGBT characterization tool window.

The I_{DS} – V_{DS} curves of the characterized SiC MOSFET and the datasheet are shown in Figure 5.2 (a) and (b), respectively. The gate voltages sweeps between 10V to 20V at five different gate voltage levels. Figure 5.3 (a) and (b) also shows the *Ic – Vce* curves of Si IGBT where the gate voltages sweep between 7 V and 20 V with seven gate voltage level. It is interesting to note that the modeled device characteristics closely matched with the datasheet curve with less than 1% error.

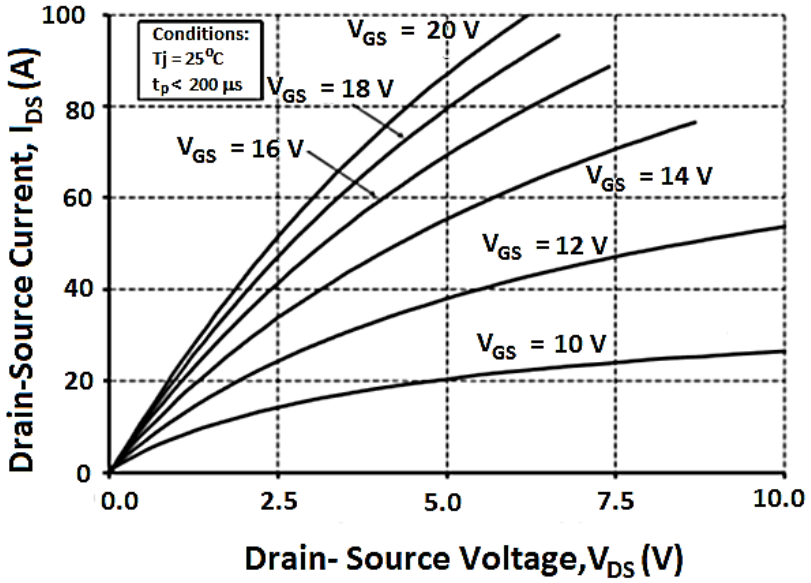

Figure. 5.2. (a) Id – Vds datasheet plot.

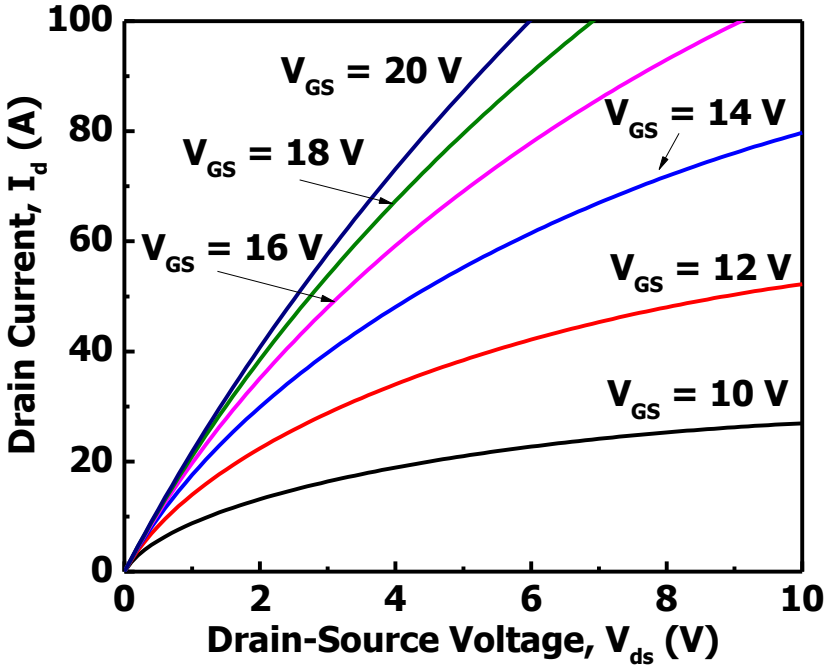

Figure. 5.2. (b) Id – Vds characterization plot.

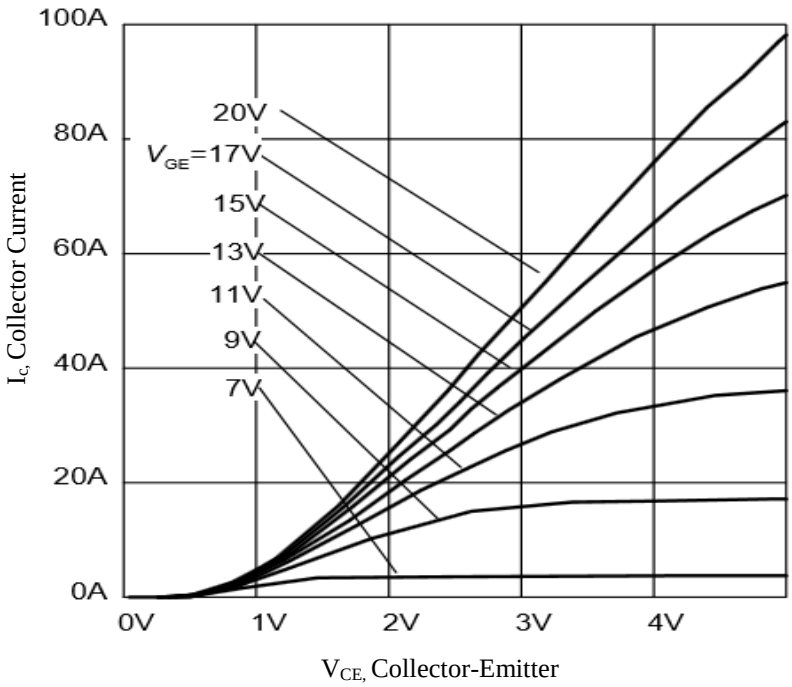

Figure. 5.3. (a) Ic – Vce datasheet plot.

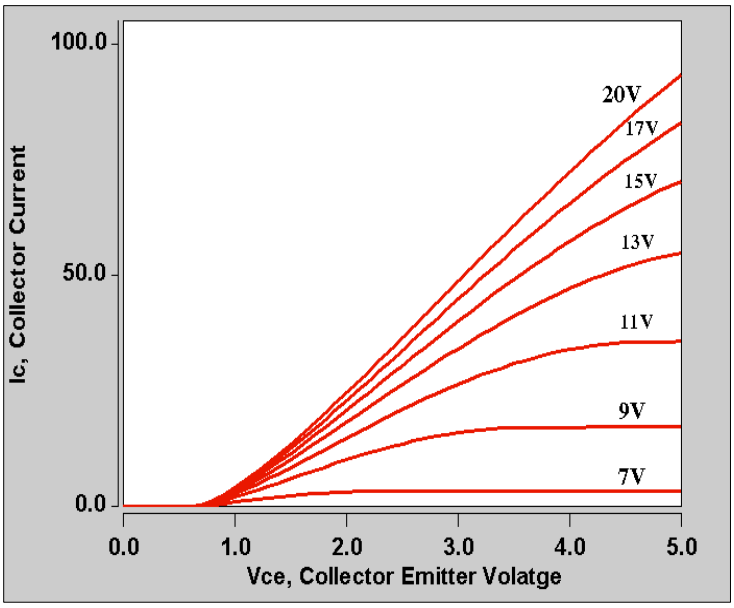

Figure. 5.3. (b) Ic – Vce characterization plot.

5.2.2 Compact modeling methods

The compact modeling of semiconductors are of different types and involves different methods of characterization. They include:

1) *Physics-based models*: This type of models are based on the device physics. The device parameters has its physical significance, and are technology dependent. For example, the physics parameters of an IGBT will not be the same for a MOSFET.
2) *Empirical model*: In empirical modeling, the equations are non-physical. Empirical models can be developed by digitizing a device datasheet. In other words, they are datasheet driven. The temperature scaling of this type of model is not too difficult to implement
3) *Lookup table models*: In this method, measured data of a device are collected and computed into a computer software. During simulation or runtime, the computer look up the data and extract point as necessary. The more measured data points computed, the better the accuracy of the results. This is because less measured data points will leave more room between interpolations.

5.2.3 Saber-Simulink Co-simulation

Mixed-signal simulation is the computer modeling and analysis of electronic designs that contain both digital and analog signals. The Saber-Simulink co-simulation interface forms a coupled mixed-signal simulation environment consisting of two independent simulators which are the Saber simulator and Matlab Simulink. The Saber simulator simulates analog and digital signals of a design.

The Saber-Simulink co-simulation interface allows the two simulators to work in synchronization to simulate the mixed-signal circuit designs and provide the behavioral information, which makes it easy to evaluate the design. In this simulation method, Saber acts as

the master simulator. Saber initiates the simulation process and also serves as the user interface to Simulink. Figure 5.4 shows the block diagram of Saber-Simulink co-simulation. Signal measurements are done in the Saber while Simulink initiates the controls. The two simulators send and receive communication through the co-simulation interface block. Figure 5.5 shows the flow chart of the co-simulation approach used in this work.

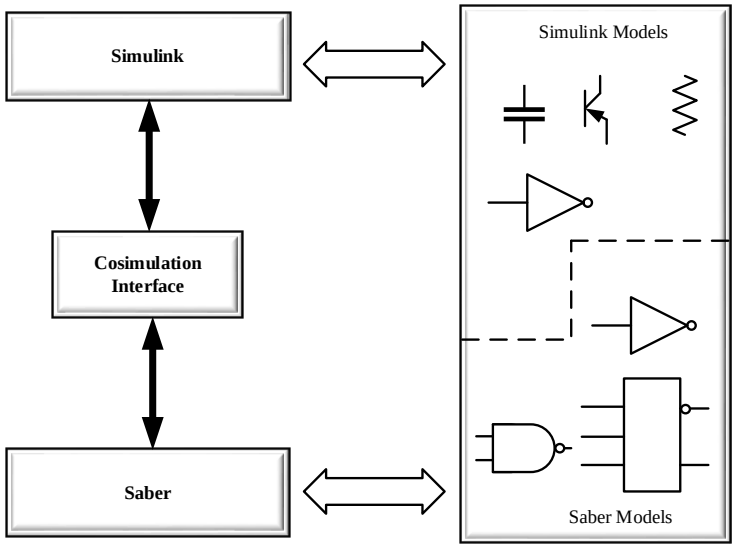

Figure 5.4. Block diagram of Saber-Simulink co-simulation.

Results in Saber can be views in CosmosScope waveform analyzer. This is a feature in Saber that display and analyze waveforms for both digital and analog signals of a design, using plot files created by the simulator. Analysis waveforms can also be viewed using DesignProbes in the Saber sketch environment.

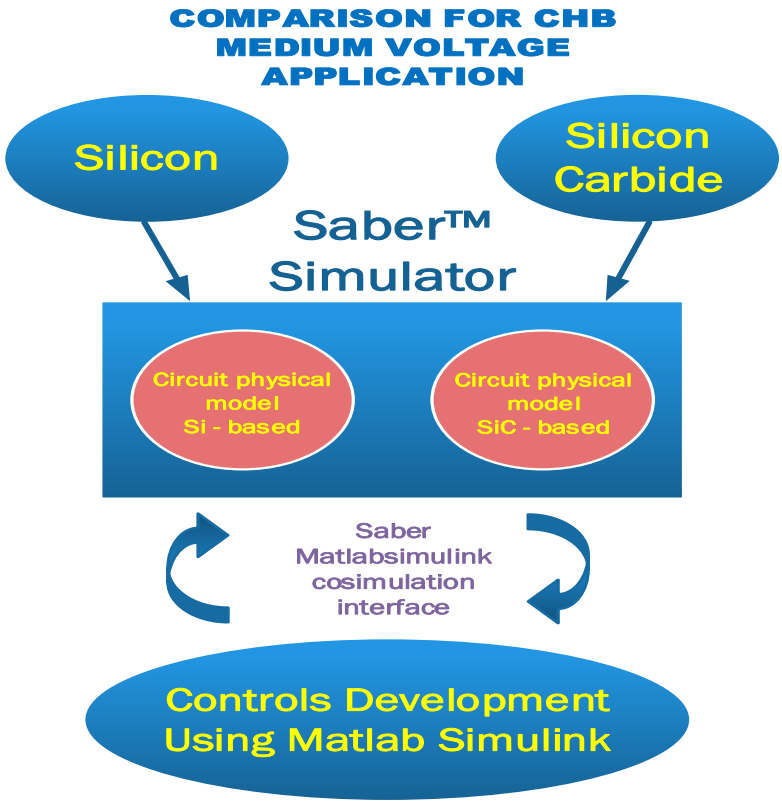

Figure 5.5. A flow chart of Saber-Simulink co-simulation.

The Saber-Simulink co-simulation approach was used in this thesis work to run performance analysis of power semiconductors in the multilevel CHB inverter system. The modulation of the CHB inverter cells were accomplished via Saber-Simulink co-simulation. The carrier signals, modulating signal and phase shifts are implemented in Simulink. A co-simulation block is used to interface between Simulink and Saber as shown in figure 5.6. The Mux and Demux block shown in the figure is used to combine signals from various ports in the Simulink to conform to the port configuration of the SaberCosim block. These signals are received in the Saber environment via the co-simulation block and are fed into the semiconductor circuitry to activate the devices. These signal can be viewed both in Saber and Simulink using CosmosScope and Scope respectively.

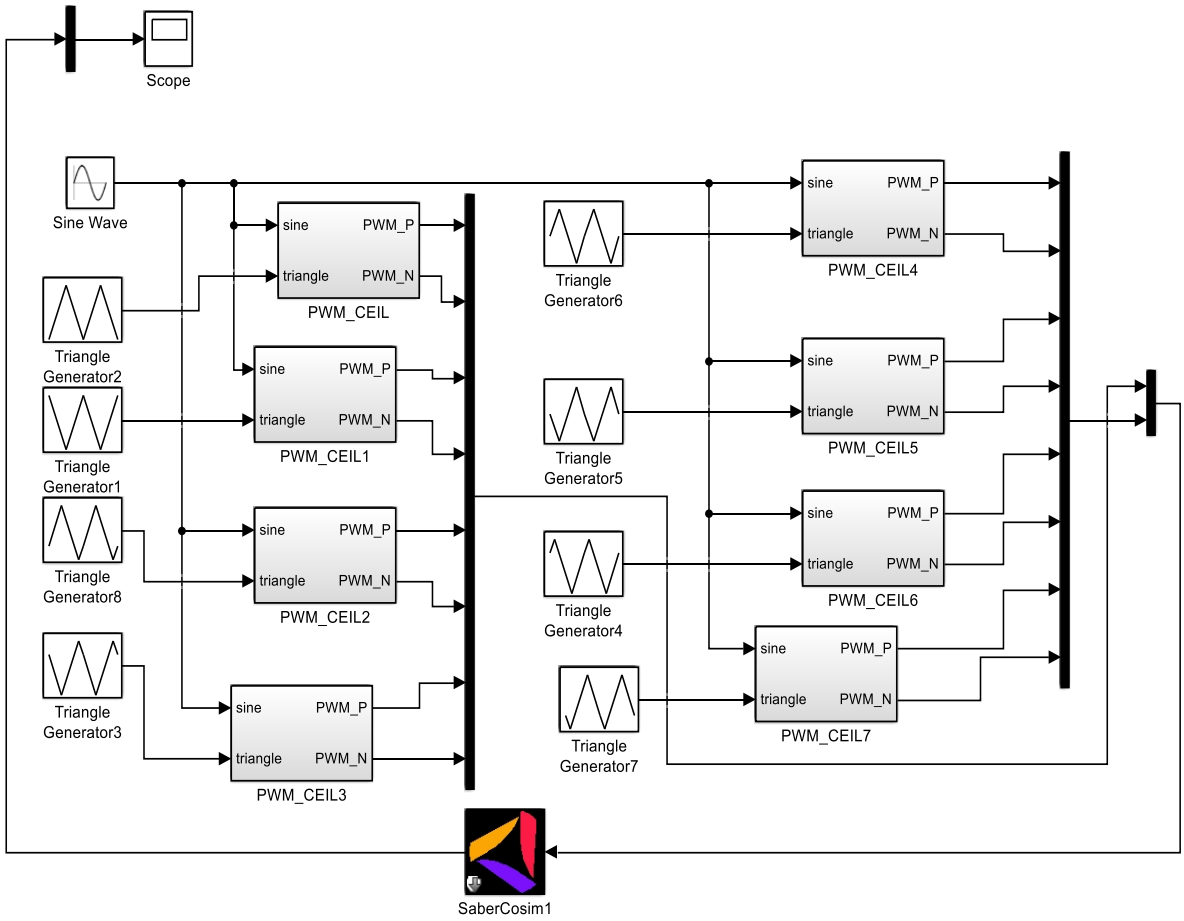

Figure 5.6. Saber-Simulink interface showing SaberCosim block and PWM blocks.

5.3 Semiconductor Device Performances

From the simulations, results were obtained and the following performances were recorded for SiC MOSFET and Si IGBT. These semiconductor devices – SiC MOSFET and Si IGBT were used in the multilevel CHB inverter. The conduction loss, switching loss, total harmonic distortion (THD) and efficiency results of the multilevel CHB inverter were obtained using cosimulation as shown in figure 5.7. The inverter is simulated with the characterized device models to study the performances of SiC MOSFETs and Si IGBTs in the inverter system

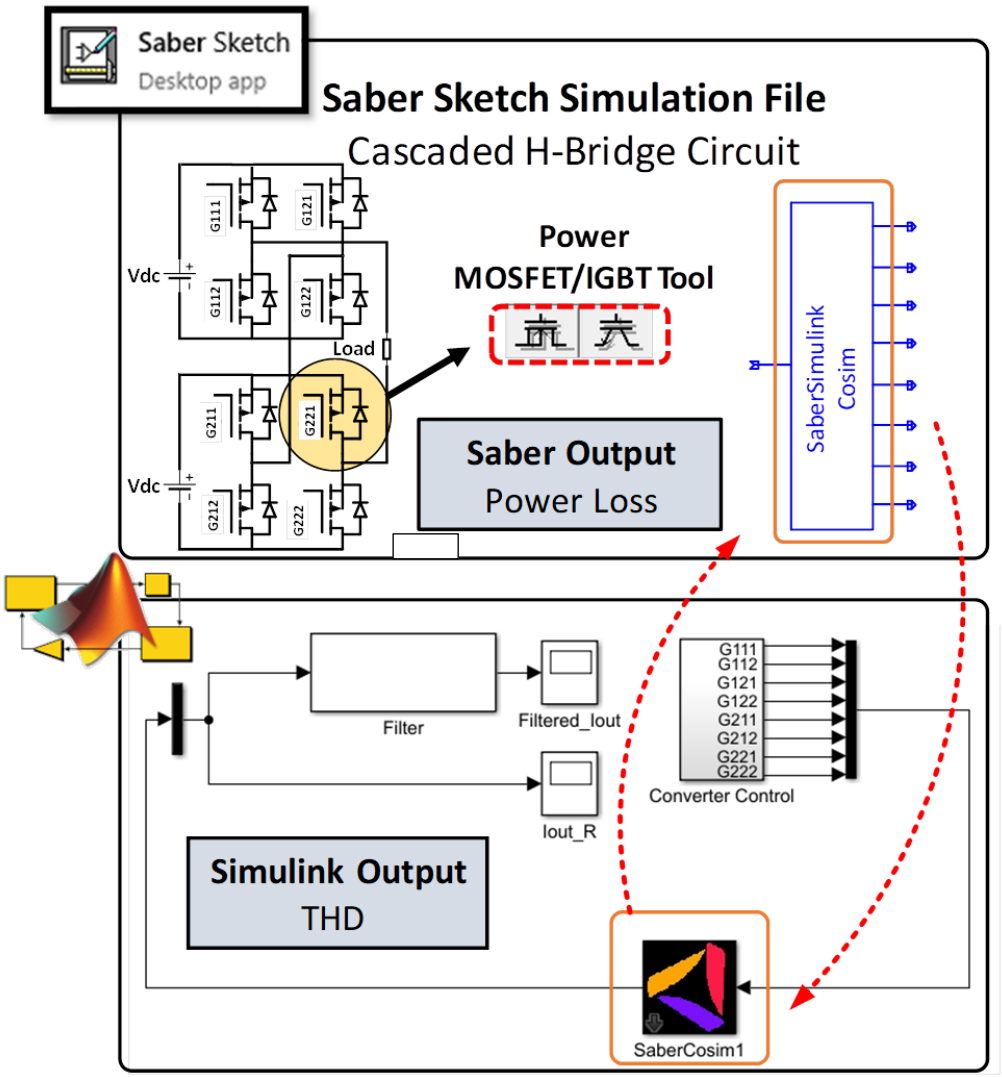

Figure 5.7. Saber-Simulink co-simulation.

5.3.1 Switching transients

Figure 5.8 (a) and (b) shows the switching characteristics of SiC MOSFET and Si IGBT. SiC MOSFET is characterized with shorter switching transient times compared to Si IGBT which constitutes high *di/dt* and *dv/dt*. This factor is a drawback for SiC MOSFET. In Figure 5.8 (a), the tail current of Si IGBT is shown, which is also a drawback for Si IGBT.

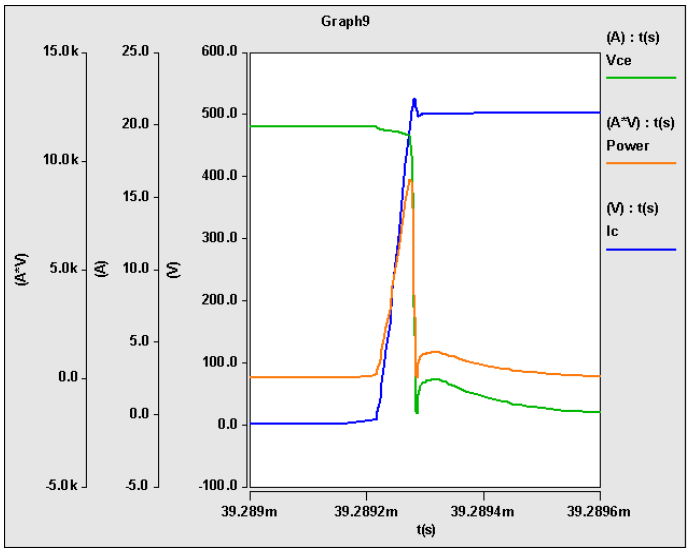

Figure 5.8 (a) Turn-on characteristics of Si IGBT.

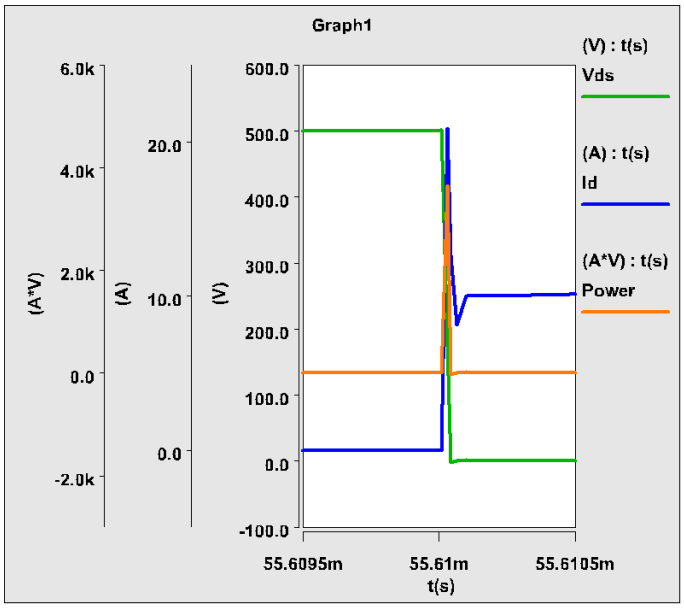

Figure 5.8 (b) Turn-on characteristics of SiC MOSFET.

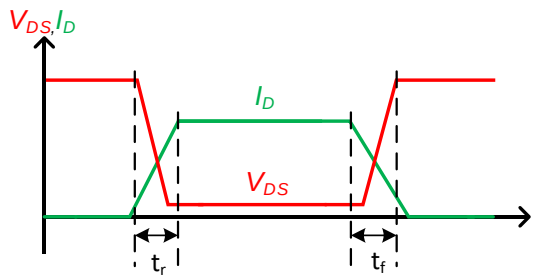

Figure 5.9 (a) Rise/fall time of SiC MOSFET.

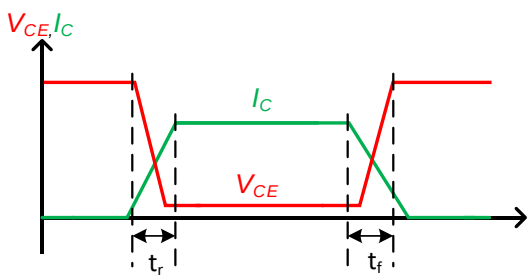

Figure 5.9 (b) Rise/fall time of Si IGBT.

Table 5.1 shows the rise and fall times of both devices which matches closely with their datasheet values.

Table 5.1. Rise and Fall Time of Sic MOSFET and Si IGBT at 25ºc

Time	SiC MOSFET	Si IGBT
(*ns*)	***T = 25ºC***	
Rise time (t_r)	59	25
Fall time (t_f)	37	97

5.3.2 Conduction loss

Conduction loss is a function of voltage drop across semiconductor and the amount of current flowing through the semiconductor when it is conducting [2]. Conduction loss identifies as a crucial factor in the loss profile of power semiconductor devices. In Table 5.2, the conduction loss data of CHB inverter with BESS is presented. The inverter power level considered is a 13.3 kW CHB BESS. The temperature is varied from 25°C to 125°C and the conduction loss results at these points are compared below.

From results in the table, it is observed that the conduction loss of SiC MOSFET (C2M0040120D) at 13.3 kW of power experiences a 44.8% loss increase during operation from of 25°C to 125°C. While in the case of Si IGBT (IKW25N120T2) the conduction loss increase measures to 7.3% with the same operating conditions. The conduction loss of SiC MOSFET devices increase significantly with increasing operating temperature compared to Si IGBT devices for the same temperature increase and operating power.

Table 5.2. Conduction Loss Data – 13.3 Kw

	13.3 kW *(W)*	
Temp	*SiC MOSFET*	*Si IGBT*
25°C	129.42	125.49
125°C	187.47	134.67

Table 5.3. Conduction Loss Percentage Increase

Conduction loss vs temp at 13.3 kW				
Temp	*SiC MOSFET (W)*		*Si IGBT (W)*	
25°C	129.42	44.8% ⬆	125.49	7.3% ⬆
125°C	187.47		134.67	

Using the Eq. (4), the error margin of the conduction loss result of SiC MOSFETs using theoretical calculations is at 8% error from the simulated result

$$P_{COND\ MOSFET} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{CM}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (R_{DSon} \,.\, i^2(t))dt = R_{DSon}.\, I_{rms}^2\,, \qquad (4)$$

where: R_{DSon} is the drain-source on-state resistance and I_{rms}^2 is the rms current through the MOSFET which can be expressed as: $\frac{1}{2} * \frac{\hat{\imath}^2}{4} + (\frac{1}{3\pi} * \hat{\imath}^2\ m\ cos\ \varphi)$

In addition, in Eq. (7), the conduction loss of Si IGBT was calculated. The error margin between theoretical and simulated result is at a 7% error margin.

$$P_{COND\ IGBT} = \frac{1}{2}(V_{CE0} * \frac{\hat{\imath}}{\pi} + r * \frac{\hat{\imath}^2}{4}) + m * cos\ \varphi * V_{CE0} * \frac{\hat{\imath}}{8} + \frac{1}{3\pi} * r\hat{\imath}^2) \qquad (7)$$

where: V_{CE0} is the zero-current collector-emitter voltage, m is modulation index $\hat{\imath}$ is the peak current through the IGBT, r is the collector to emitter on-state resistance, and φ is the power factor angle.

The conduction loss of both SiC MOSFET and Si IGBT increases with increasing temperature. This is because resistance increase with increasing temperature. The bulk resistance of Si IGBT is low because it is a bipolar device. This results in lower conduction loss for Si IGBT compared SiC MOSFET as seen in Table 5.2.

5.3.3 Switching loss

Switching loss is the product of the total energy loss times the switching frequency. In the investigation, Figure 5.10 (a) shows the switching loss data at 1, 3, 10, 30 and 50 kHz frequencies. The data shows that the switching loss is relative to the switching frequency and temperature. At 13.3 kW, SiC MOSFET has significantly reduced losses compared to Si IGBT at the specified switching frequencies.

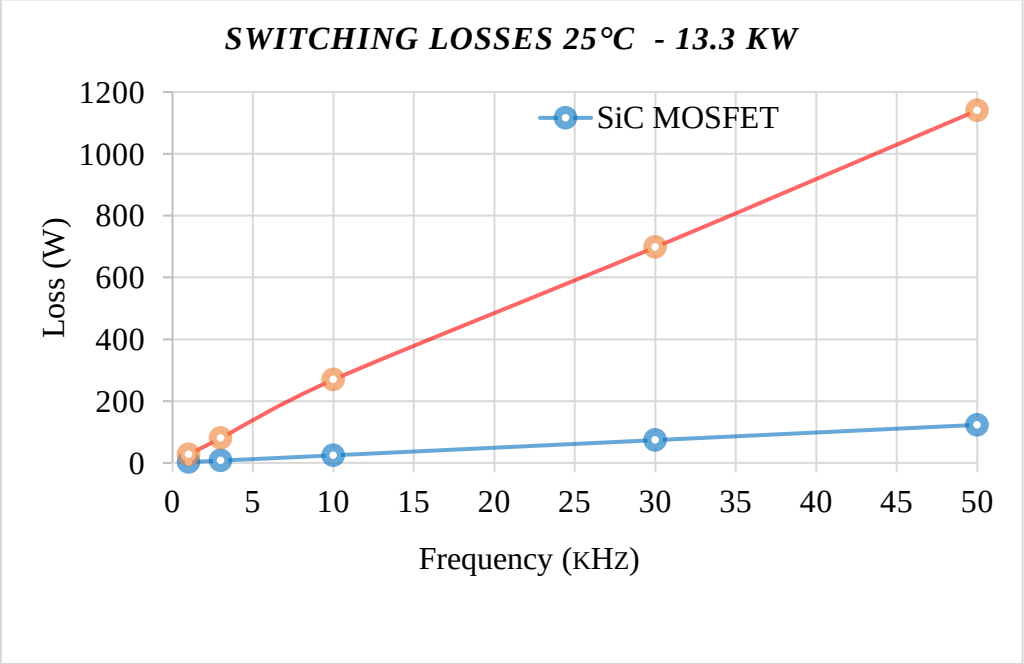

Figure 5.10 (a) Switching loss vs. switching frequency at 25°C – 13.3 kW.

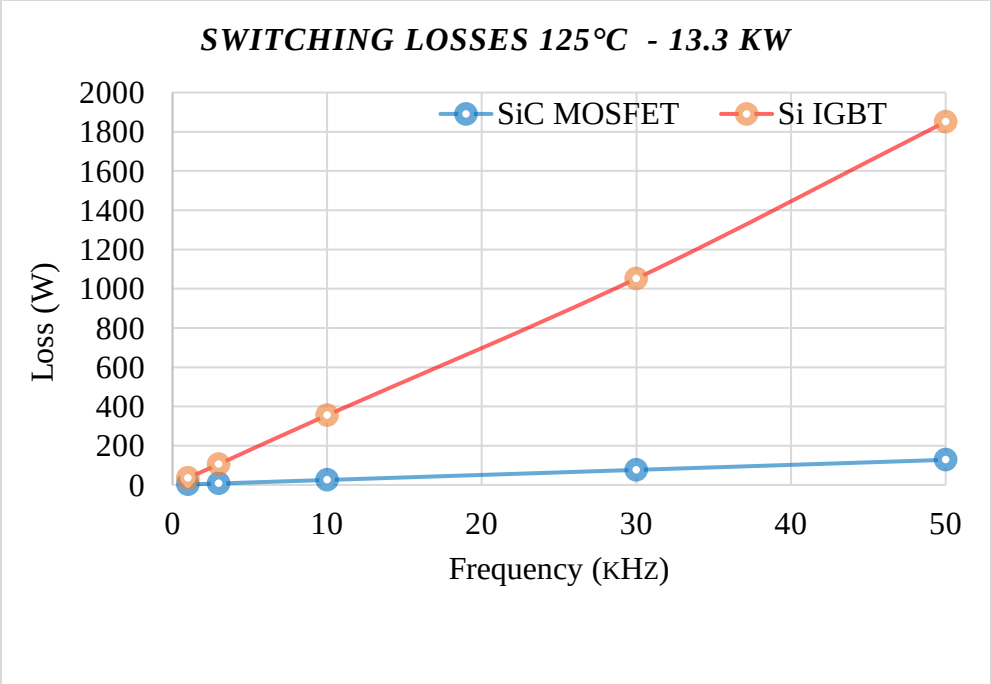

Figure 5.10 (b) Switching loss vs. switching frequency at 125°C – 13.3 kW.

5.3.4 Total harmonic distortion (THD)

The total harmonic distortion of the inverter system met the grid requirement of less than 5% THD. The filter inductance is calculated using 5% maximum allowable current ripple for grid connection. Keeping all other factors constant, and swapping power devices, the THD remained constant. In the hardware implementation, there could be a difference in THD using different power devices because of possible ringing/parasitics during switching.

Output filters are important components of PWM grid-connected inverters. Filter configurations commonly used are L, LC, LCL, and LLCL. One advantage of multilevel CHB inverter to THD is that an "L" filter is adequate to mitigate the harmonics of output current at low switching frequency to meet grid requirements. The grid side inductor and the capacitor are used to suppress high frequency ripples of which at low switching frequency, they will be insignificant [3].

5.3.5 Efficiency

The efficiency of the inverter is measured at different switching frequencies; and shows that as the switching frequency increases, the efficiency decreases. This is because switching loss is proportional to increasing switching frequency. The devices used in the investigation are SiC MOSFET – C2M0040120D and Si IGBT – IKW25N120T2. These two devices are selected because they are comparable in terms of application, device generation (2nd generation), device package (TO-247-3), device dimensions (16.13 x 5.21 x 21.1mm), device weight (1.340411 oz), breakdown voltage (1200V), and current ratings. Figure 5.11 shows the efficiency performance of the inverter at 13.3 kW. The efficiency data considered are mainly for the semiconductor devices. It does not account for efficiencies due to filter losses. There is a significant efficiency difference in favor of SiC MOSFET compared to Si IGBT, especially at higher switching frequencies between 30 kHz and 50 kHz.

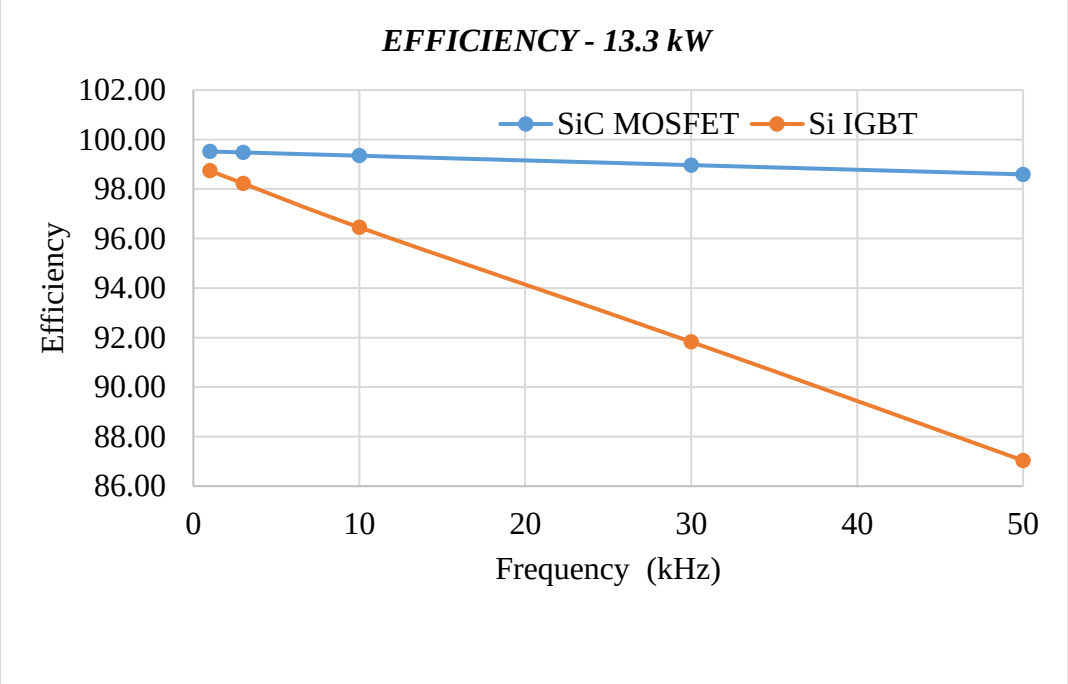

Figure 5.11 Efficiency data at 13.3 kW.

5.3.6 Economic feasibility

Cost is an important factor to consider in the implementation of a CHB inverter with BESS. The topology used in this comparative study is the same with using a SiC MOSFET or Si IGBT device. The filter requirements for SiC MOSFETs will be lower that than of Si IGBTs because they can operate at higher switching frequencies. Other passive component costs will be the same if the inverter is implemented with either of the semiconductor devices.

The SiC MOSFET-based inverter is characterized with higher efficiency and improved performance. Therefore there is a potentially cost-effect advantage of the CHB BESS inverter using SiC MOSFET technology. In [5], a comparison was done for 50kW string inverters developed using Si IGBT and SiC MOSFET technologies. The investigation shows that the SiC-based inverter under study was approximately one-fifth the weight and volume of the Si IGBT-based inverter.

In this comparative analysis, the highest efficiency attained using Si IGBT devices in the BESS inverter system was 98.74% at a switching frequency of 1 kHz. The equivalent efficiency to using SiC MOSFET devices was 98.59%. This was attained at a switching frequency of 50 kHz against 1 kHz for Si IGBT. This means reduced filter requirements for SiC MOSFET at 50 kHz than 1 kHz at which the Si IGBT based inverter achieved a 98.74% efficiency. This data indicates that high power density, efficiency, system cost, and system payback period can be an improvement using SiC MOSFET devices. Also, the size and weight of the SiC-based inverter projects to be smaller than Si IGBT-based inverter. The performance improvement of a SiC MOSFET-based inverter counts on 3 major factors. One is the significantly lower switching losses of SiC MOSFETs compared to Si IGBT, which amounts up to 10 times at 50 kHz switching frequency. This allows SiC MOSFETs to operate at much higher switching frequencies with

minimal cooling requirements (reduced size of possible heatsinks), reduced size and weight of filtering components, higher power density (reduced raw materials), and thus, reduced components and installation costs.

Table 5.4 show the unit cost of SiC MOSFEt and Si IGBT devices. It is seen that SiC MOSFET is more than five time higher that Si IGBT. But other component like the inductor size and heatsink size will compensate for the high cost of SiC MOSFET devices. This is so because the size of the inductor for the SiC MOSFET-based inverter compared is smaller compared to Si IGBT-based inverter. SiC MOSFETs have better thermal characteristics than Si IGBTs, therefore the size of the heat sink for SiC MOSFET-based inverter will be smaller. Thus, the bill of material (BOM) cost for the SiC MOSFET-based inverter is lower because of the smaller inductor size, smaller heat sinks size, and smaller enclosures. All these reduces the cost of the SiC MOSFET-based inverter by about 15% compared to the Si IGBT-based inverter.

Table 5.4. Power Semiconductor Cost

Power device	Quantity	Unit Price	Total
SiC MOSFET	72	$34.12	$2,456.64
Si IGBT	72	$6.48	$466.56

Figure 5.12 shows the component costs of SiC MOSFET-based and Si IGBT based CHB BESS inverter with cost reduction in favor of the SiC MOSFET technology.

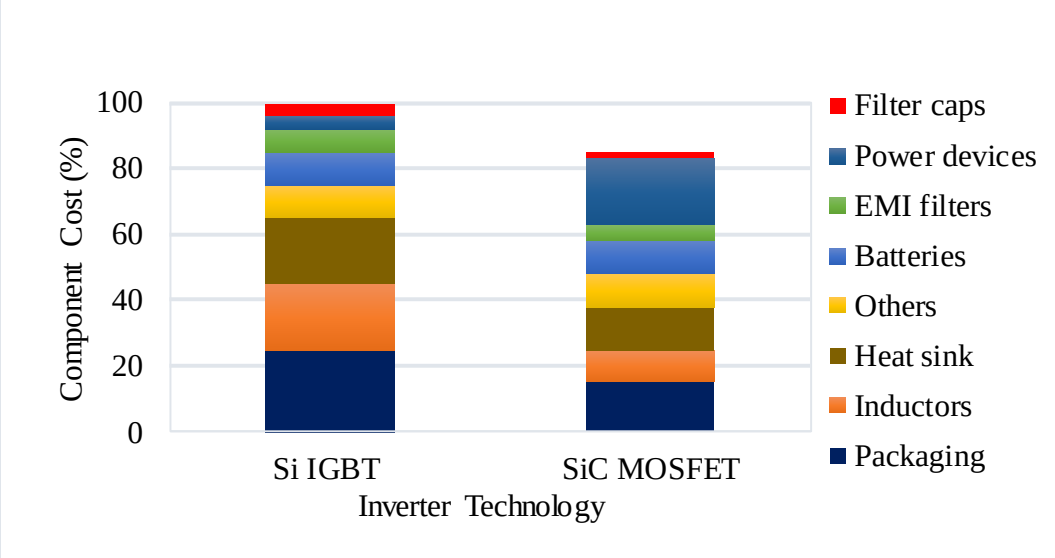

Figure 5.12 Cost components of SiC MOSFET and Si IGBT BESS inverters.

The SiC MOSFET-based inverter has a closer payback period because of its higher efficiency and reduced BOM cost. The higher efficiency results in higher power/electricity production which when sold can be used to offset the total investment cost faster compared to Si IGBT-based inverter. This is to say that the efficiency gain of power converters has an important economic implication in its return of investment. Table 5.5 is the of-the-shelf prices of components for the inverter system

Table 5.5. Off-The-Shelf Component Pricing [4]

Cost Factor	SiC MOSFET	Si IGBT
Switching device	$2,456.64	$466.56
BOM cost	$8,300.95	$9,765.83
Annual Maintenance (fixed)	$850	$1,000
Total estimated investment cost	**$11,607.59**	**$11,232.39**

The economic feasibility of this comparative analysis considers 10 years of life time of grid-connected inverters. The annual energy yield considers the inverter efficiencies of SiC MOSFET-based inverter and Si IGBT-based inverter which at 30 kHz switching frequency. Table 5.6 is the relative economic feasibility factors of the two types of inverters.

Table 5.6. Relative Economic Feasibility Table

Relative factors	SiC MOSFET	Si IGBT
Avg. Electricity Price/kWh (US)	$0.1330	$0.1330
Avg. operational hours/day (peak shaving)	4 hours	4 hours
Power rating	13.3 kW	13.3 kW
Efficiency	98.97 %	91.83 %
$ value of energy/year	$2,555.99	$2,371.59
Payback period	6.8 years	8.2 years
Savings in 10 years	**$5,452.31**	**$2,483.51**

The payback period (PBP) is defined as the total estimated investment cost, divided by annual $ value of energy. PBP = [(initial estimated investment cost) / (annual income – maintenance cost)]. And the annual income = power rating x electricity price x efficiency

5.4 References

[1] Mordi K, Mhiesan H, Umuhoza J, Hossain M. M, Farnell C and Mantooth H. A, "Comparative Analysis of Silicon Carbide and Silicon Switching Devices for Multilevel Cascaded H-Bridge Inverter Application with Battery Energy storage," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, pp. 1-5, 2018,.

[2] Anthon A, Zhang Z, Andersen M. A. E, Holmes D. G, McGrath B and Teixeira C. A, "The Benefits of SiC <sc>mosfet</sc>s in a T-Type Inverter for Grid-Tie Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2808-2821, April 2017.

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[4] https://www.mouser.com

[5] Schupbach M., "SiC MOSFET and Diode Technologies Accelerate the Global Adoption of Solar Energy," *2015 Bodo's Power Systems*

CHAPTER SIX

CONCLUSIONS AND RECOMMENDATION

6.1 Summary and Conclusions

Semiconductor devices are building blocks of power electronic converters. Some these semiconductors include SiC MOSFET and Si IGBT. These semiconductors are used to implement a cascaded H-bridge inverter for battery energy storage system. The cascaded H-bridge is a good candidate for battery storage systems at medium high voltage application because of its modularity [1]. The required voltage levels can be reached easily, and utilizes less than half the power device voltage in some cases. In Chapter 1, the thesis background, objectives and methodology were described.

Chapter 2 discussed the switching modes of power semiconductors, which includes hard and soft switching. A comparison between these two switching methods was made. Some of the applications of power semiconductors were pointed out, and some further development areas were listed. Furthermore, Chapter 2 discussed the structure of power MOSFETs and IGBTs with a diagram that indicates the impact of different physical parameters of semiconductor materials. Some basic advantages of SiC MOSFET and Si IGBT were also identified. Different multilevel converter system configurations were discussed in Chapter 2. A flow chart was also used to simplify multilevel converter classifications [2].

In Chapter 3, the multilevel cascaded H-bridge inverter was discussed in detail, and the analysis of the topology was done which highlights the benefits of CHB inverter to BESS. The benefits and drawbacks of BESS in grid-connected applications were also discussed. One area of BESS applications that was discussed extensively in Chapter 3 is peak load shaving. Factors that

affect the use of BESS for peak shaving were discussed. The return of investment (ROI) factors of CHB BESS were also highlighted. These factors are complex for grid-connected applications than residential applications [3, 4, 5]. Factors that affect the characteristic life of a grid-connected inverter was described. And the controls of the converter and inverter side of the system were also described.

Chapter 4 is the theoretical analysis of the performance factors of SiC MOSFET and Si IGBT devices. These factors include the conduction loss, switching loss and efficiency analysis. Literatures were cited that considered different methods and approaches to theatrical analysis regarding power losses.

In Chapter 5, the methodology and performance results were obtained. The power semiconductor devices used for the investigation were characterized using Saber. A Saber-Simulink co-simulation environment was implemented to investigate the performances of SiC MOSFET and Si IGBT devices using similar topology. Saber is used to characterize the devices and develop the power stage of the inverter while its controls were developed in Simulink. The inverter was simulated with SiC MOSFET or Si IGBT at different switching frequencies and operating temperatures. Results were obtained for conduction loss, switching loss, total harmonic distortion (THD), and efficiency. These results were used to compare the performance of SiC MOSFET and Si IGBT in a nine-level CHB inverter with BESS.

6.2 Recommendations

The comparison of SiC MOSFET and Si IGBT were performed with the intention to ascertain which one between these two devices will be more suitable for the implementation in a nine-level CHB inverter integrated with BESS. From the results obtained, SiC MOSFET show

better performances compared to Si IGBT with regards to power losses which are associated with the device operating temperature, switching frequencies and current through the device. Thus, the SiC MOSFET is a better recommendation for the inverter topology even at higher power levels, not considering the cost of power devices. Finally, a future work targets 13.8 kV (rms) CHB inverter with BESS, and utilizing 10 kV SiC MOSFET device when commercially available. The availability of a 10 kV SiC devices will reduce the number of active switches in the inverter, and thus reduce controls complexity of the system.

6.3 References

[1] Zhong Y, Roscoe N, Holliday D, Lim T. C and Finney S. J, "High-Efficiency MOSFET-based MMC Design for LVDC Distribution Systems," in *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1-1

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[3] Jayasekara N, Masoum M. A and Wolfs P. J, Optimal operation of distributed energy storage systems to improve distribution network load and generation hosting capability. IEEE Trans Sustain Energy 2016;7:250–61

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APPENDIX A

Device Physics Modeling

Parameter extraction sequence needs only the characteristics that are readily available in the device datasheets. To measure the accuracy of the characterized parameter (curve), a simulated parameter should be appended with datasheet parameter. Datasheet curves can be digitized using a plot digitizer: https://automeris.io/WebPlotDigitizer/ After digitizing, save the data in .csv format.

Parameter Extraction - MOSFET:

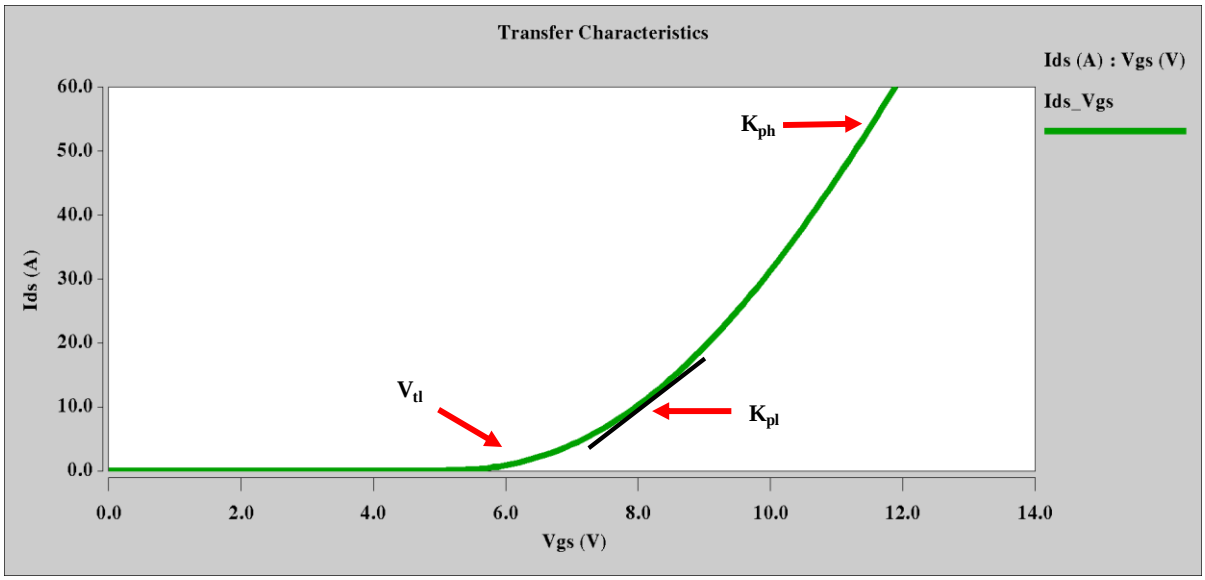
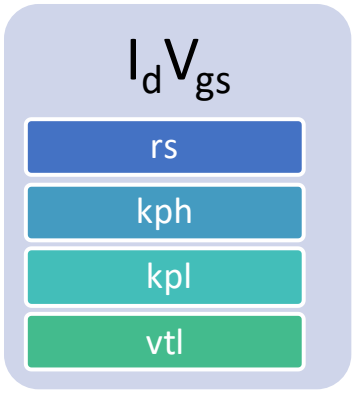


Figure A.1. Transfer characteristics



- ***r_s*:** Parasitic Drain Resistance
- ***k_{ph}*:** Transconductance parameter high threshold region
- ***k_{pl}*:** Transconductance parameter low threshold region
- ***v_{tl}*:** low current threshold voltage

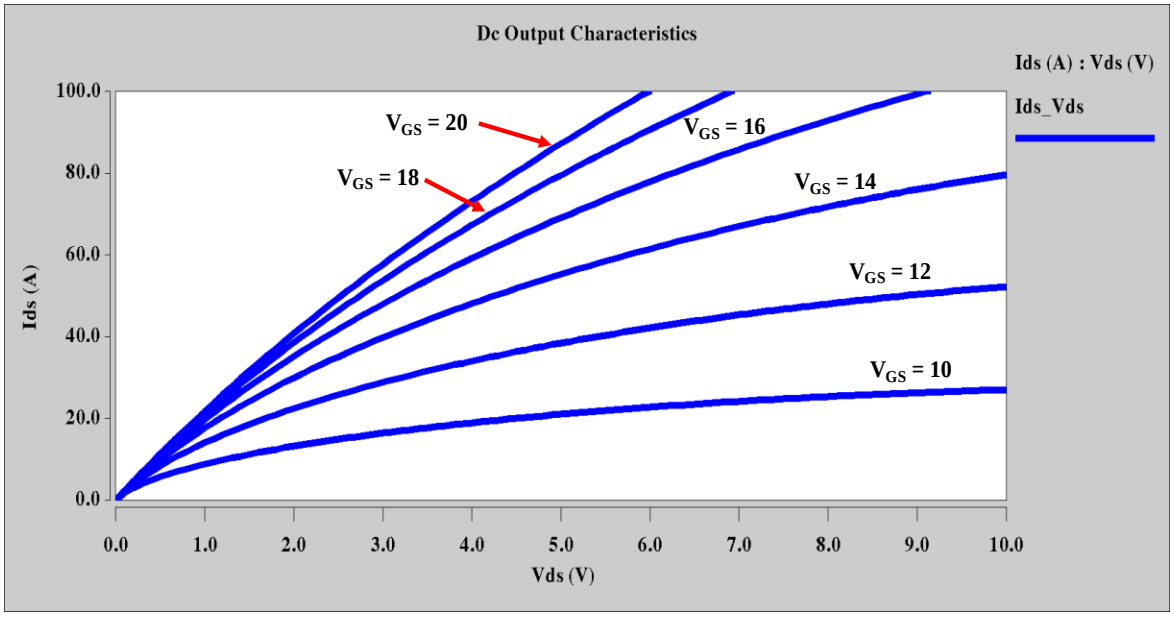
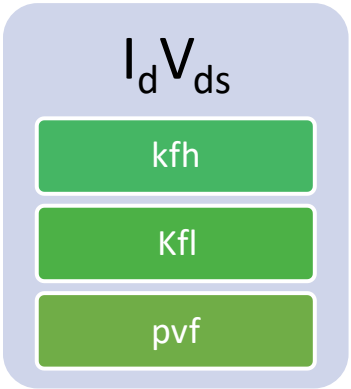


Figure A.2. Dc output characteristics



- ***kfh:*** transconductance parameters to scale current in troode and high threshold region
- ***kfl:*** transconductance parameters to scale current in troode and low threshold region
- ***pvf:*** pinch-off voltage parameter to adjust Vds(sat)

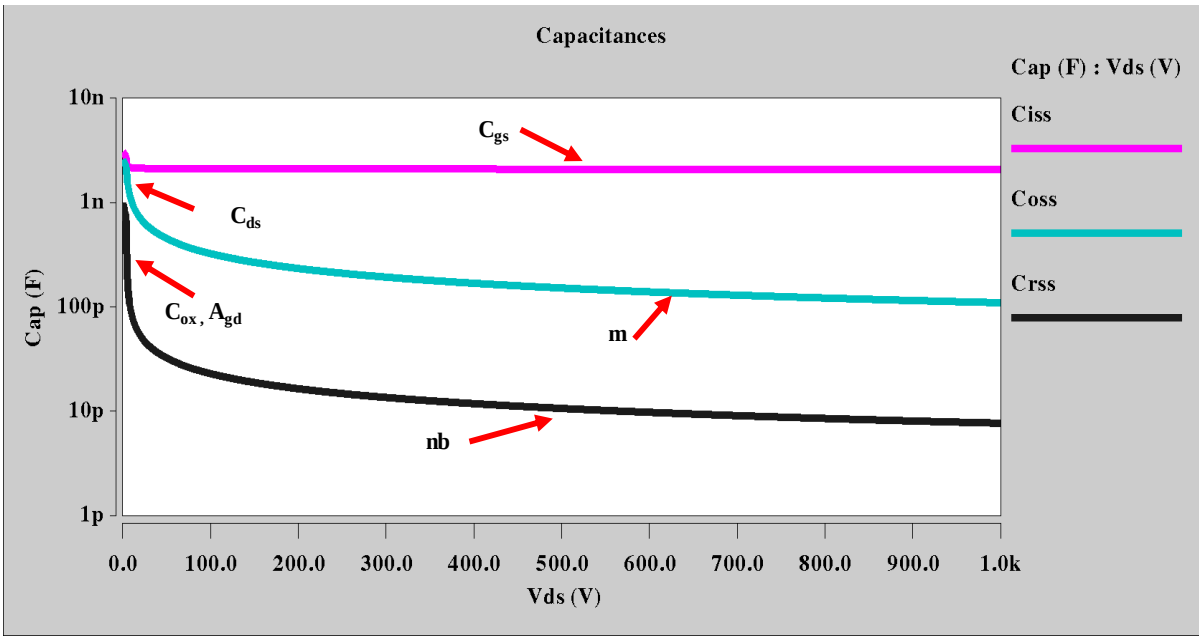
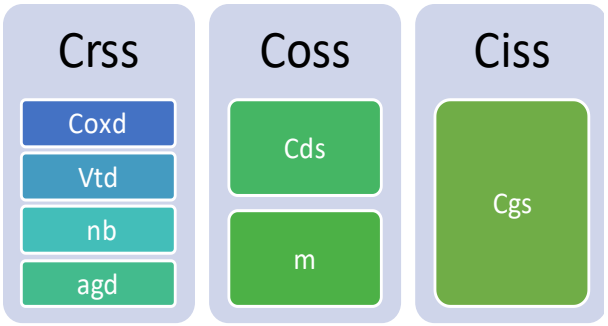


Figure A.3. Capacitance



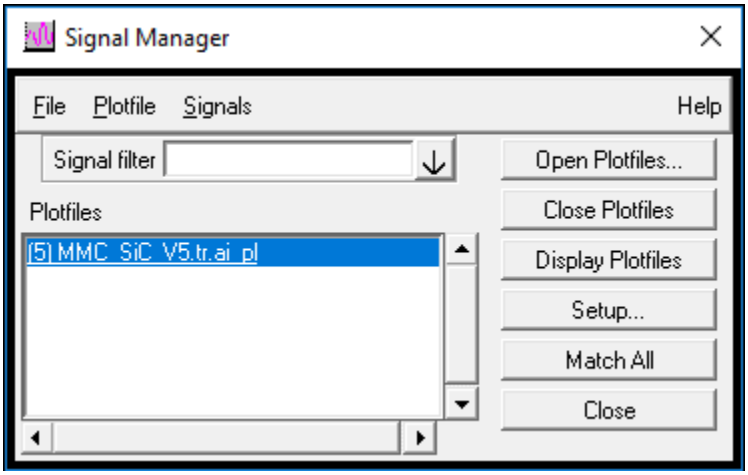
- ***Coxd:*** Gate oxide capacitance
- ***Vtd:*** Gate drain overlap depletion threshold voltage
- ***nb:*** Base doping concentration
- ***agd:*** Gate drain overlap active area
- ***Cds:*** Drain to source zero bias capacitance
- ***m:*** Junction grading coefficient
- ***Cgs:*** Gate to source capacitance

Capacitance definition

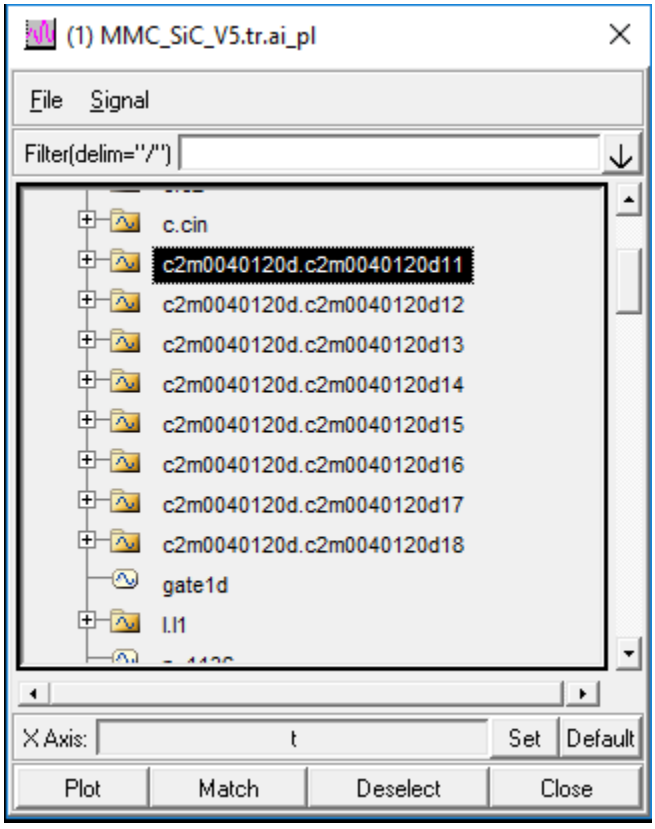
- ***Coxd*** = cgd + cgs
- ***Coss*** = cgd + cdsdep
- ***Crss*** = cgd

Power loss measurement using CosmosScope

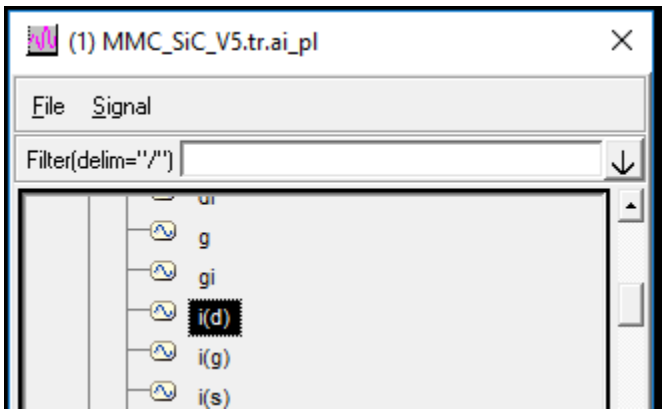
- Simulates circuit and view in CosmosScope
- Open plotfiles in “Signal Manager” by clicking “Display Plotfiles



- Double click power switch signal to analyze



- Select and plot i(d) and vds signals individually



- Open “Waveform Calculator”, click middle scroll on mouse to drop i(d) and vds signals in the calculator tab
- Multiply both signals in the calculator tab, double click result to plot the waveform

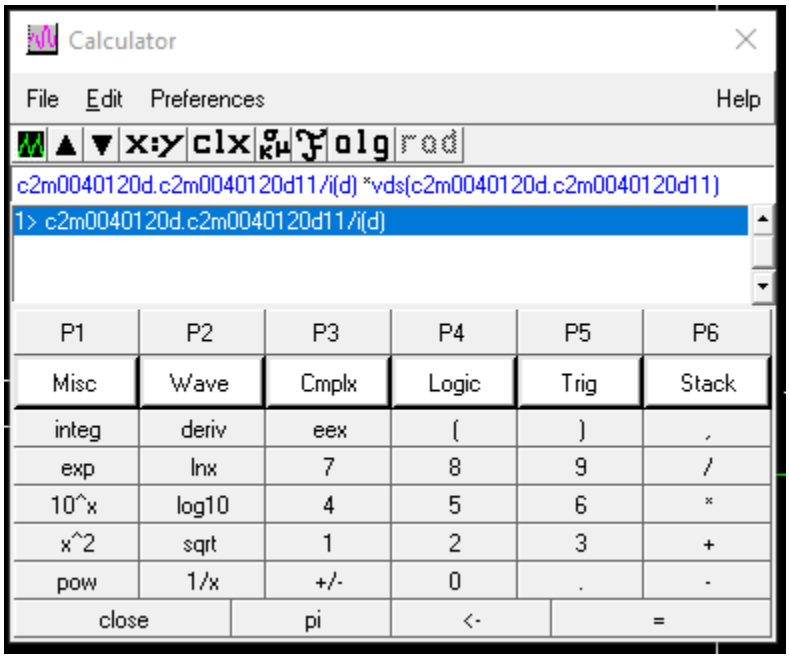


Figure A.4. Waveform calculator

- Zoom into the waveform to measure (see fig. A4 below)

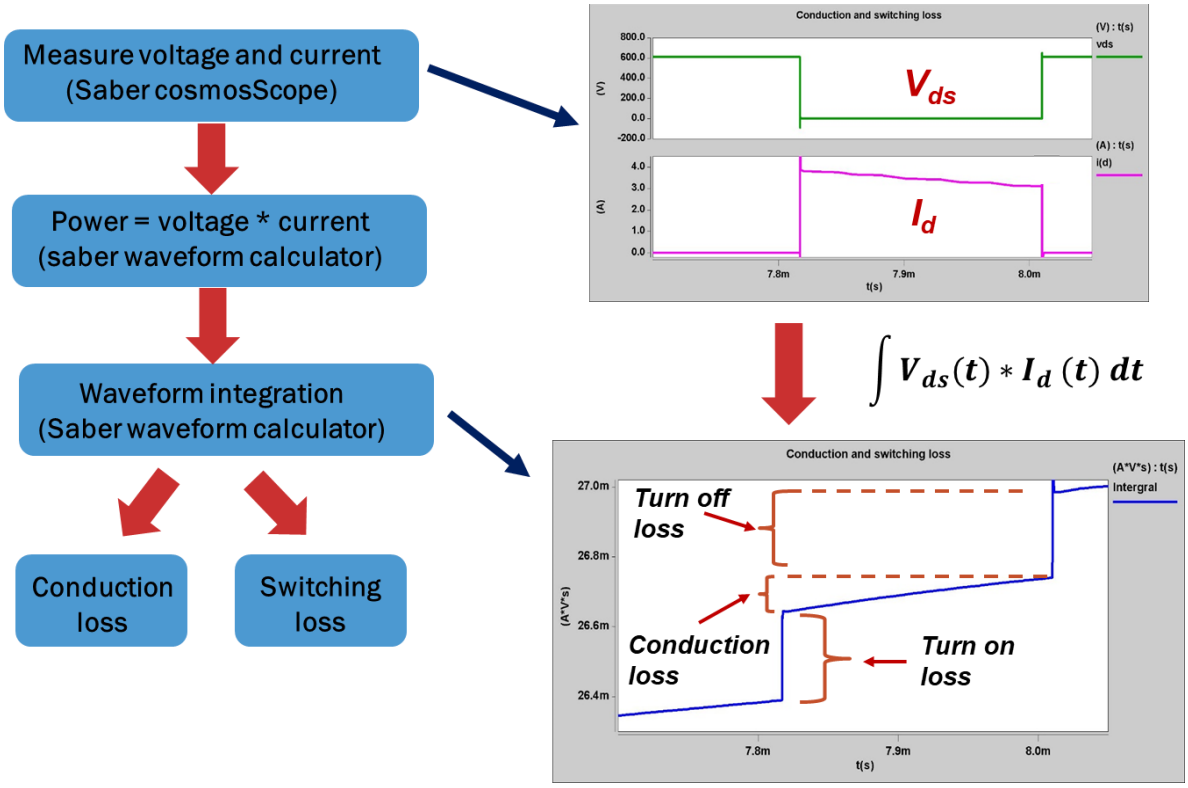
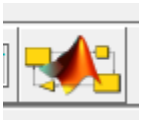


Figure A.5. Power loss measurement

Saber-Simulink Co-Simulation

Configuration:

- Clicking the SaberSimulinkCosim icon on “Saber Sketch” window



- Click on help, then click “Help on SaberSimulink Cosim tool”. Follow the prompt to configure Cosim with the Matlab version on your computer

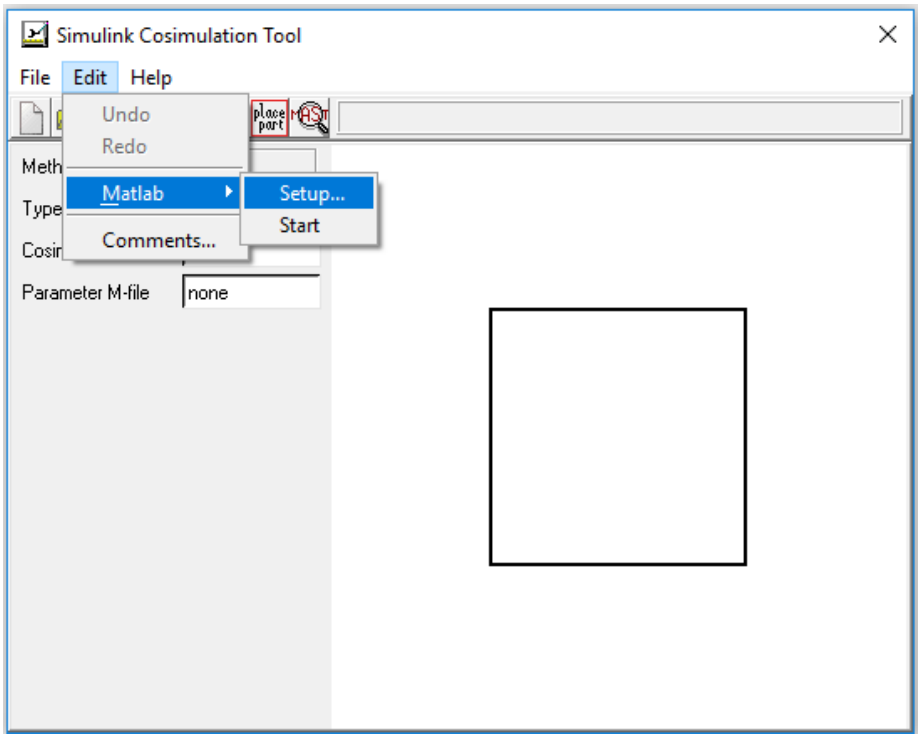


Figure A.6. Simulink Cosimulation configuration window

- Simulate the example on “Help on SaberSimulink Cosim tool” by following the prompt

Locate the SaberCosim block in Simulink:

- In Simulink, click the open file folder

- Follow the prompt below to locate SaberCosim block in the “work directory”
- Click “Open” to create a new work space with the SaberCosim block

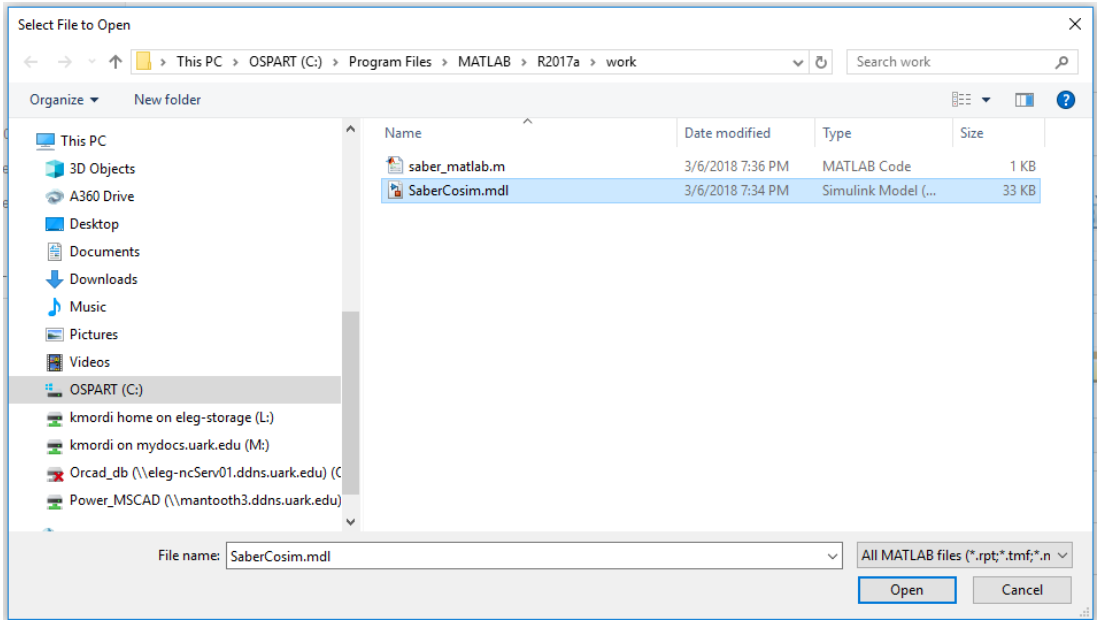


Figure A.7. SaberCosim block directory

- The multilevel cascaded H-bridge inverter circuit topology used in the investigation
- The co-simulation block is seen at the top-left of the figure

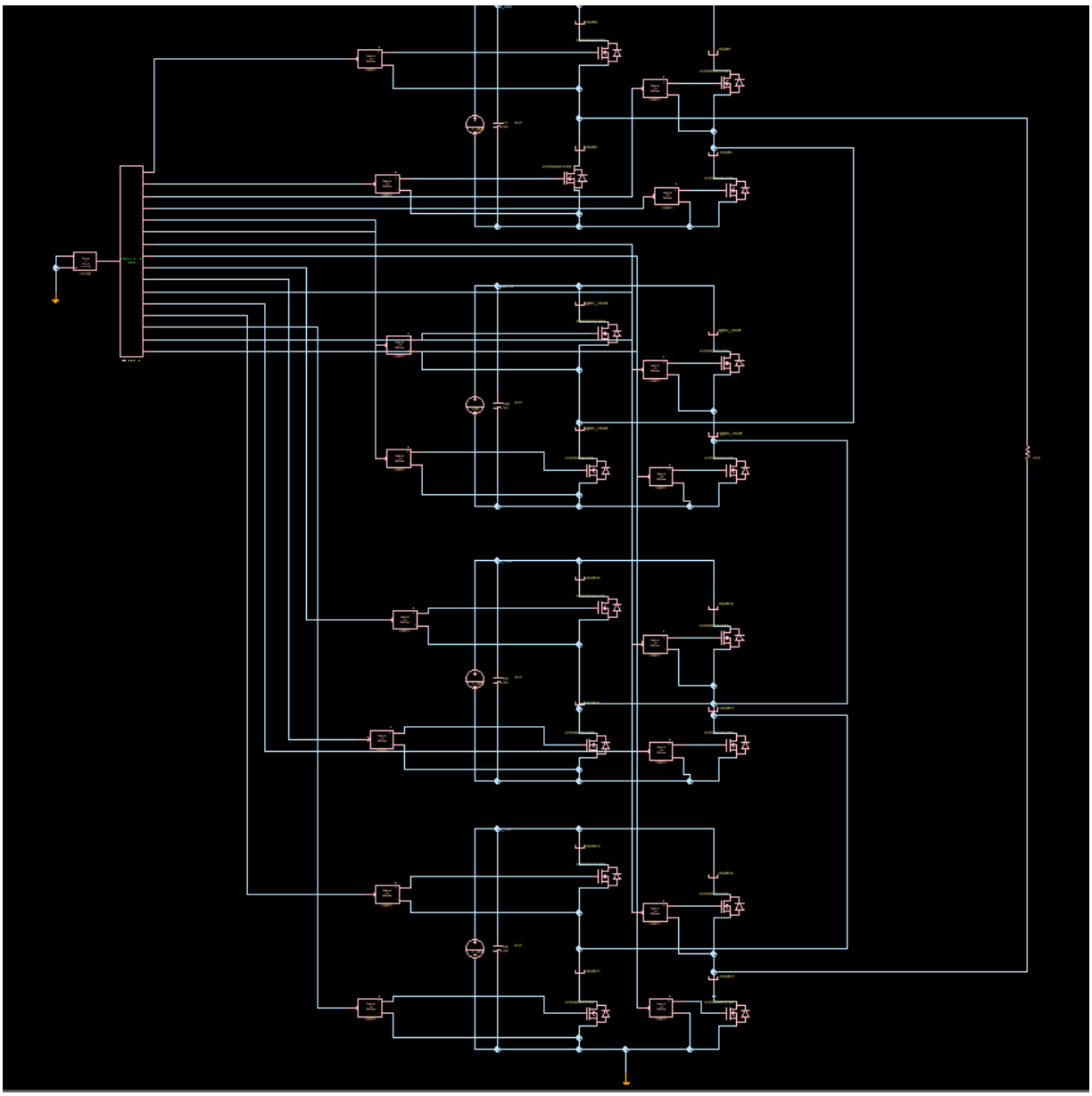


Figure A.8. Inverter power stage in Saber

- The PWM and controls of the inverter were implemented in Simulink
- The SaberCosim block is responsible for transferring the signals from Simulink into Saber

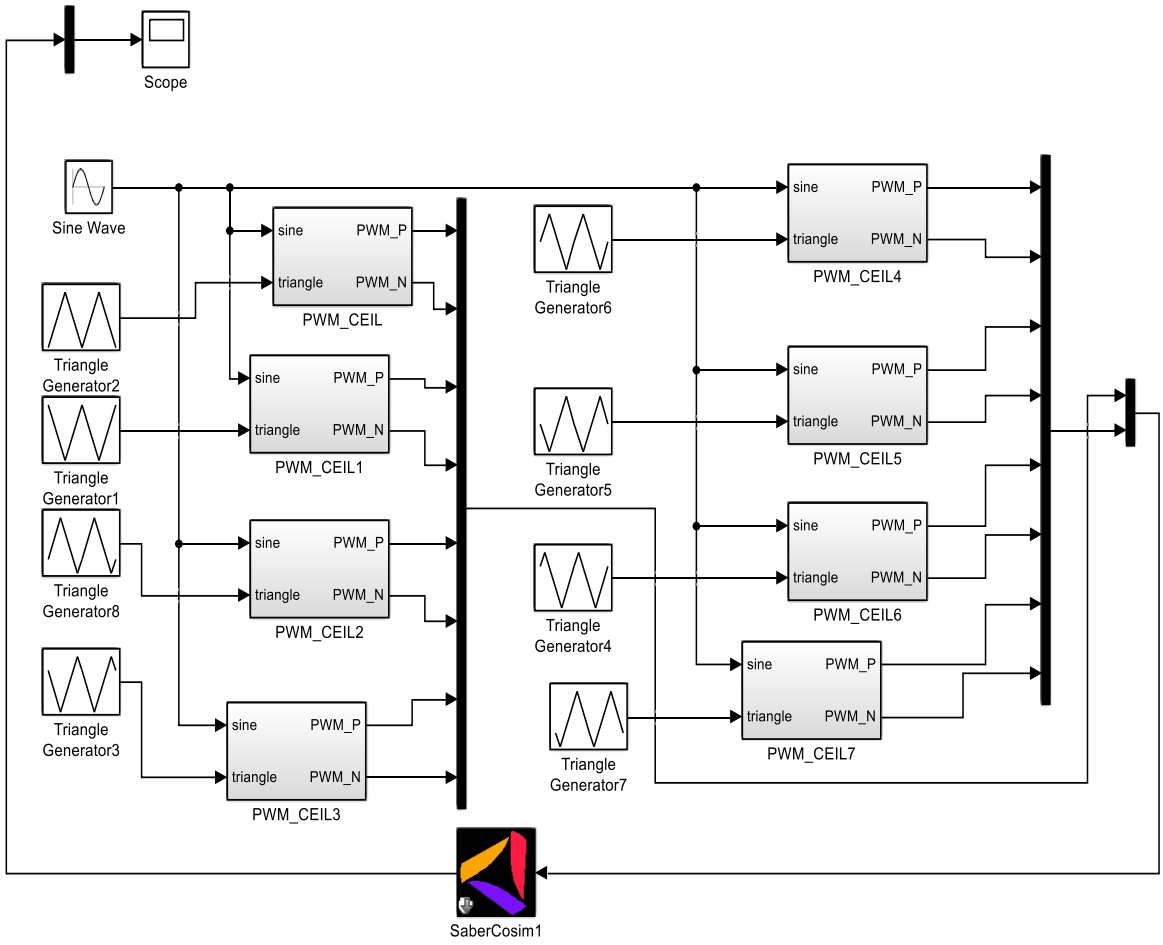


Figure A.9. Inverter controls stage in Simulink

- The saber model architecture tool is used to perform empirical modeling of power devices

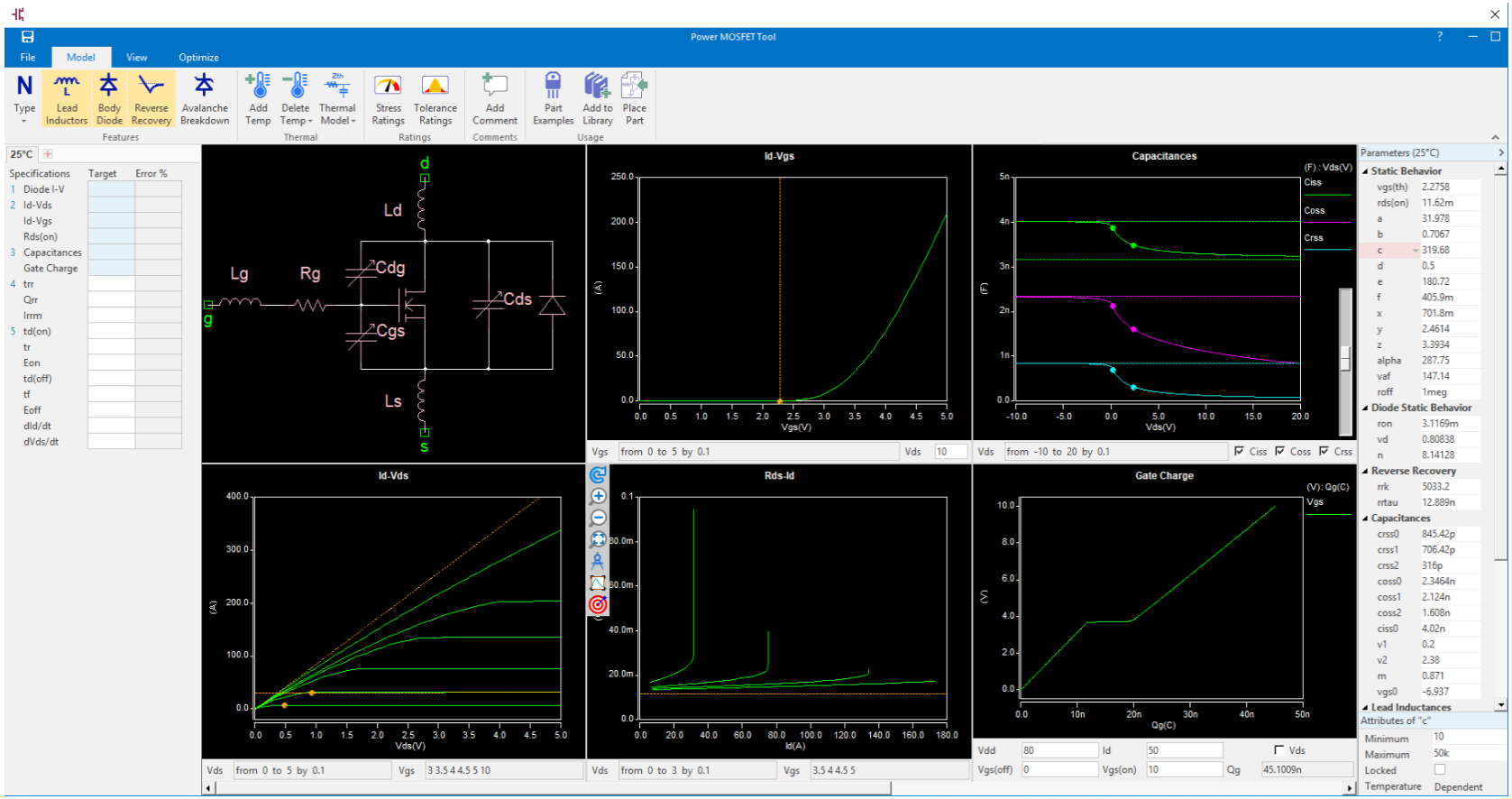


Figure A.10. Saber model architect