12-2018

Fully Analog Laser Driver With Robust Active Feedback Control

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A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science In Electrical Engineering

by

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California State University, Fullerton
Bachelor of Science in Electrical Engineering, 2014

December 2018
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

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Abstract

The objective of this project was to go through a real life engineering development cycle, document and justify the design choices, and use background experience in electronic design and control systems to implement the best design possible. The laser driver implemented in this project is designed for the general use of a large variety of diodes in continuous wave mode, much like off the shelf laser drivers. The design goals included improving upon off the shelf laser drivers by decreasing steady state error, setting time, response time, and overshoot. Many different feedback control systems were evaluated, and a modified PID controller was chosen which was designed to overcome the operational behavior of real-life electronics. The system was designed from the ground up, the electronics were simulated in the time domain, the entire system derived into the Laplace Domain and simulated using Matlab/Simulink. A printed circuit board was designed and assembled to verify performance in a real system.

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1 Introduction

The process for designing and implementing a fully analog control system for driving laser diodes will be outlined and stepped through. Weaknesses in off-the-shelf laser drivers are identified and design goals are created to improve upon these weaknesses. An general analog laser driver must be conceptualized and realized. A robust feedback mechanism must be designed in order to accurately and automatically control the output of the laser. Once the driver and feedback have been designed they can be merged to create a closed loop automatic power control laser driver. This stage is where most off-the-shelf drivers stop, however, taking it one step further and implementing a control system will improve performance with minimal drawbacks. This project will step through design process in detail including electronic design, time domain simulation, frequency domain simulation, derivation of transfer functions, control system simulation, as well as real life testing results.

Laser drivers typically focus on a specific operating conditions such as modulation, stability, low noise, or power. A combination of a closed loop stable modulation laser driver [13] is common for the telecom industry however these drivers are typically low power and do not have the ability to drive lasers with high bias currents as opposed to the design in this paper. Another type of laser driver is modulated with high output power [14] for LiDAR systems, but these laser drivers don't have accurate or stable output powers. Low noise laser drivers are also popular for RF applications [16], and achieving a SNR of 55.2dB on a custom wafer is considered outstanding performance while this project was able to accomplish a SNR of 54 dB with off the shelf components. This research focuses on a non-modulated, closed loop stable, high drive current, low noise, optically stable, feedback controlled laser driver. Sacrificing modulation allows a performance boost of the other parameters as well as breaking into a niche market.

2 Develop Specifications

In this chapter the weaknesses and opportunities for improvement for off-the-shelf (OTS) laser drivers are identified, and aggressive design goals are realized for maximum performance improvements.

2.1 Photodiode Input Current

The feedback mechanism used in laser drivers to lock the set point for automatic power control is the output of a photodiode. Typically, OTS drivers can accept current in the range of 100's of micro-amps before saturation. It is speculated that this specification is due to noise, which will be touched upon in later chapters. The low current will improve noise performance, however it does not allow for large laser bias currents. This specification can be improved upon with design a goal of accepting up to 5 milli-amps of photodiode current.

2.2 Optical Drift

This is not a typical specification found in a laser driver IC data sheet because it is a liability to guarantee. The laser used to test the system will be new and not show any degradation, therefore it will be guaranteed that the optical power will not drift more than 2% over a period of 2 hours.

2.3 APC Loop Speed

Typical frequency response of an APC loop for an OTS laser driver is $80kHz < f_{3dB} < 200kHz$. The faster the feedback loop the quicker it can respond to the photodiode current and make adjustments to the drive current. Also, this pushes out noise peaks due to resonant frequency. For this specification, faster is not necessarily better, so a loop speed of about 50kHz will be chosen. The lower frequency will improve on noise due to the Photodiode Input Current specification. The control loop will also compensate for the tracking error and steady state error seen by OTS drivers.

2.4 Over and Undershoot

There are a variety of situations were overshoot and undershoot can occur. If the bias current of the laser diode is being driven close to the maximum operating point, then overshoot and undershoot can become critical parameters as to not cause any catastrophic damage to the device. Manufacturers for OTS drivers have seemed to conveniently leave these scenarios and specifications out of their data sheets. Since the main goal of this project is design a robust control system, these specifications need to be defined.

2.4.1 Startup

The overshoot/undershoot during startup will not exceed 10% of the set point.

2.4.2 Step Change

During a step change of 0.1V, the overshoot/undershoot will not exceed 10%

2.4.3 Shutdown

The overshoot/undershoot during shutdown will not exceed 10% of the set point.

2.5 Settling Time

The percent overshoot and the settling time are trade offs.

2.5.1 Startup

The settling time during startup will not exceed 1ms

2.5.2 Step Change

The settling time during a step change of 0.1V will not exceed 500us.

2.6 Settling Accuracy

This specification is equivalent to steady state error, and since OTS drivers do not have active feedback control, they can only guarantee about 10%. The integrator in this design will allow us to easily guarantee 2%.

2.7 Current Noise

The current noise introduced by the laser driver should be less than $10nA/\sqrt{Hz}$. There may be some OTS laser drivers that are specifically designed for low noise operation that are quieter than this, but this specification is better than most.

2.8 Signal to Noise Ratio

The SNR isn't a typical specification, but it gives a good overall picture of noise performance for the laser driver. A minimum SNR of 50dB will be the target design goal.

2.9 Data Sheet

The analysis of weaknesses from off-the-shelf laser drivers has led to development of the data sheet found in figure 1.

ANALOG ACTIVE FB CONTROL LASER DRIVER SPECIFICATIONS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER SUPPLY						
Single Supply	V_{CC}	Voltage input	3.75	5	15	V
Supply Current	I_{CC}	Supply current w/o laser bias	50	80	100	mA
LASER BIAS						
Bias-Current-Setting Range		Range of voltage set points for output current	0		3	V
Bias-Current-Setting Range		Range of laser bias current set points	0		100	mA
Bias Off Current		Laser bias during shutdown			0.5	mA
Bias-Current Monitor Ratio		Bias current monitor volt/amps reading		30		V/A
AUTOMATIC POWER CONTROL						
Photo Diode Input Current	I_{PD}	Range of acceptable input currents for PD	0		1	mA
Photo Diode Voltage Out	V_{PD}	Range of TIA set points for current control	0		3	V
Photo Diode Current Monitor Ratio		Photo current monitor volt/mA reading		0.6		V/mA
Optical Drift		Amount of optical drift over a 2 hour period		2		%
Electrical Stability		Laser bias current drift over a 2 hour period			1	%
APC Loop Time Constant		Analog feedback loop speed		20		us
ACTIVE FEEDBACK CONTROLS						
Startup Overshoot/Undershoot		Over/under shoot percentage at startup			5	%
Shutdown Overshoot/Undershoot		Over/under shoot percentage at shutdown			5	%
Step Change Overshoot/Undershoot		Over/under shoot with 0.1V step change			10	%
Startup Settling Time	$T_{S\text{-}STRT}$	Time to reach 2% steady state at startup		5		ms
Step Change Settling Time	$T_{S\text{-}STEP}$	Time to reach 2% steady state from step change			1	ms
Settling Accuracy		Actual steady state vs theoretical			10	%
LASER SAFETY						
Turn-Off Delay		Time to turn off from shutdown signal			100	us
Overcurrent Protection Delay		Time of turn off during over-current			125	us
NOISE PERFORMANCE						
Current Noise	I_{TN}	Total Current Noise of Laser Driver		9		nA/√Hz
Signal to Noise Ratio	SNR	SNR of feedback detection	50	56		dB

Figure 1: Laser driver data sheet derived from weaknesses in off-the-shelf ICs.

3 Design ACC Laser Driver

An automatic current control (ACC) driver sources a constant current through the users device choice. In order to tackle a daunting task such as designing an APC laser driver, first a stable current source to build off of needs to be designed. A voltage controlled current source was chosen as a starting point because most integrated systems are now mixed signal with digital to analog converters being used to control set points. The particular design used allows for easy adjustment to increase the laser bias current, and allows for a large laser bias without damaging the system. The complexity of this system will increase exponentially once a control system is introduced, so it is important to keep the skeleton of the design simple.

3.1 ACC Schematic

The proposed schematic for the diode driving circuitry is shown in Figure 2.

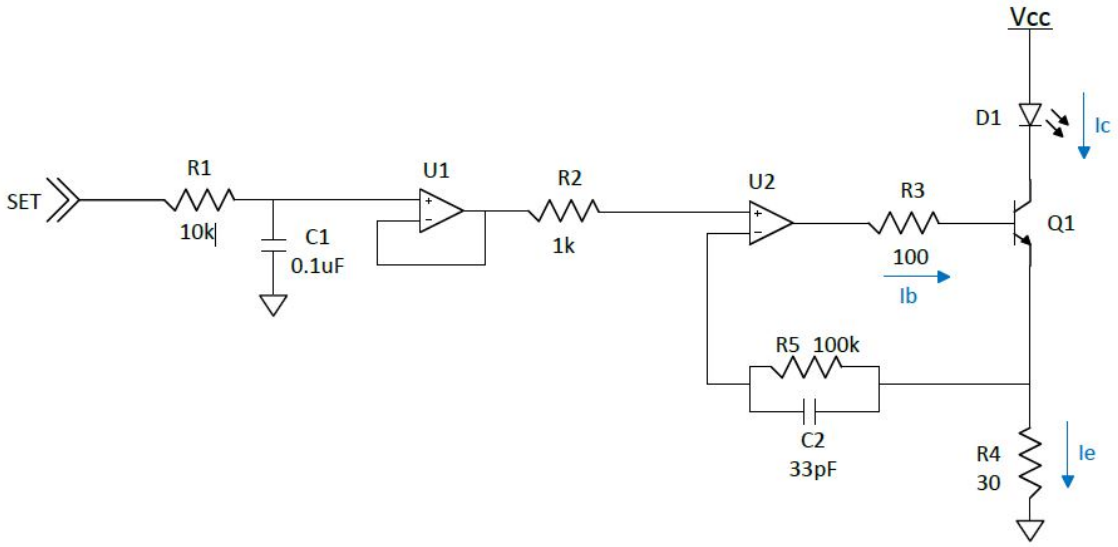

Figure 2: Automatic Current Control (ACC) laser driver schematic.

3.2 ACC Theory of Operation

The off-sheet port 'SET' is the voltage controlled current set point. For this design, the voltage set point varies from 0-3V. 'SET' is put though a passive low pass filter in order to keep the set point stable during small unwanted variations from the voltage input. The low pass filter is fed into a voltage follower buffer to isolate the impedance from the input of the driving amplifier U2. R2 is placed as a bridge between U1 output and U2 non-inverting input serving as a current sink in the case of saturation. Ideally, the input voltage 'SET' will be seen at the non-inverting input of U2 which would make the inverting input want to level out to the same voltage because they are virtually the same node. The feedback is taken from the emitter of the NPN transistor. Since the inverting input wants to be the same as the non-inverting, that means the voltage at the emitter of Q1 will also be the same as 'SET'. The voltage is controlled at the emitter, defining the current through the emitter. The collector current is related to emitter current through beta, meaning the

the diodes bias current is voltage controlled. The feedback network of U2 is chosen to be 50kHz because this is the expected frequency response of the feedback that will be applied at a later time.

3.3 Transient Simulation

The circuit shown in Figure 2 was simulated with SPICE to derive transient behavior. Figure 3 shows the simulated values vs. the theoretical calculations. Figure 4 graphs the simulations output for the values shown in the table from Figure 3. Figure 3 shows that the calculated values

TRANSIENT SIMULATION 1ms				
In/Out	Parameter	Theoretical	Simulation	Units
In	VIN	1.000	1.000	V
Out	U1 IN+	1.000	1.000	V
Out	U1 IN-	0.999	0.999	V
Out	U1 OUT	0.999	0.999	V
Out	U2 IN+	0.998	0.999	V
Out	U2 IN-	0.998	0.999	V
Out	Q1 E	0.998	0.999	V
Out	Ie	33.270	33.310	mA
Out	Ic	33.100	33.140	mA
Out	Ib	165.500	176.700	uA

Figure 3: ACC laser driver SPICE simulation results of theoretical values vs. simulated values.

are very close to the simulated values. The SPICE model operating points were not evaluated and these differences are the expected reason for the slight variance from the calculations.

3.4 AC Analysis

The driving circuitry is going to be used in the final design, so it is important to nip any instability issues in the bud at the early phases of the design. Figure 5 shows the gain margin and phase margin of the driving amplifier.

Figure 5 shows that the driving amplifier is stable through 400kHz, which is plenty for this design which requires 50kHz.

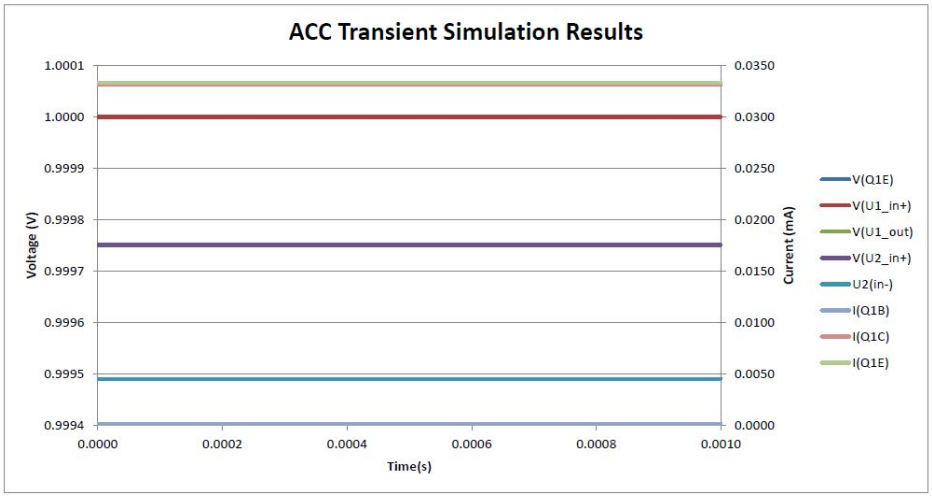

Figure 4: ACC laser driver results graphed from SPICE simulation.

3.5 ACC Laser Driver Conclusions

The design of the ACC laser driver has been successful. The stability shows that there is enough margin for the expected frequency response. The design is scalable so the photodiode feedback mechanism can be implemented painlessly. Since this design is going to do a lot more growing, the transfer function of the ACC driver will not be derived.

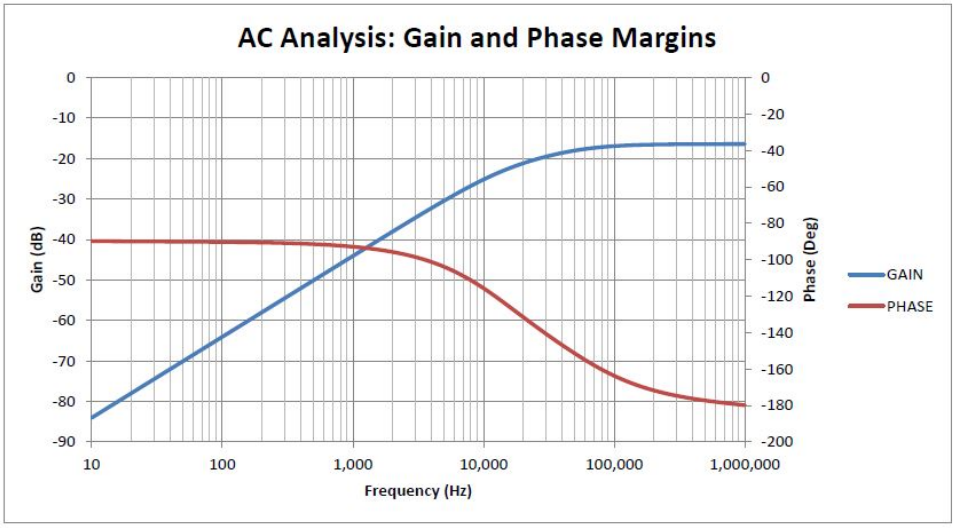

Figure 5: Gain and phase margin graph of ACC laser driver derived from SPICE simulation.

4 Feedback Mechanism

The standard feedback device for laser diodes would be current from a photodiode. Photodiodes are most commonly placed on the back facet of the laser diode, as shown in Figure 6, and used to pick off a constant amount of light. Locking the set point to the photodiode current is the key for stable operation in this design. Since the system has been chosen to be voltage controlled, there are two reasonable methods that can be used to obtain the feedback. First would be to feed the photodiode current through a resistor to obtain a voltage and second would be to use a transimpedance amplifier. In order to make an educated design choice regarding feedback mechanisms, calculations should be made for direct comparison of detector types.This chapter will be used to discuss both options and choose the best design.

Consider the following values for both detectors.

- Photo Current, $I_L = 1mA$
- Dark Current, $I_D = 5nA$
- Junction Capacitance, $C_j = 10pF$
- Shunt Resistance, $R_{SH} = 10M\Omega$

- Resistance, $R = 3k\Omega$
- Bandwidth, $\Delta f = 50kHz$
- Wavelength, $\lambda = 635nm$

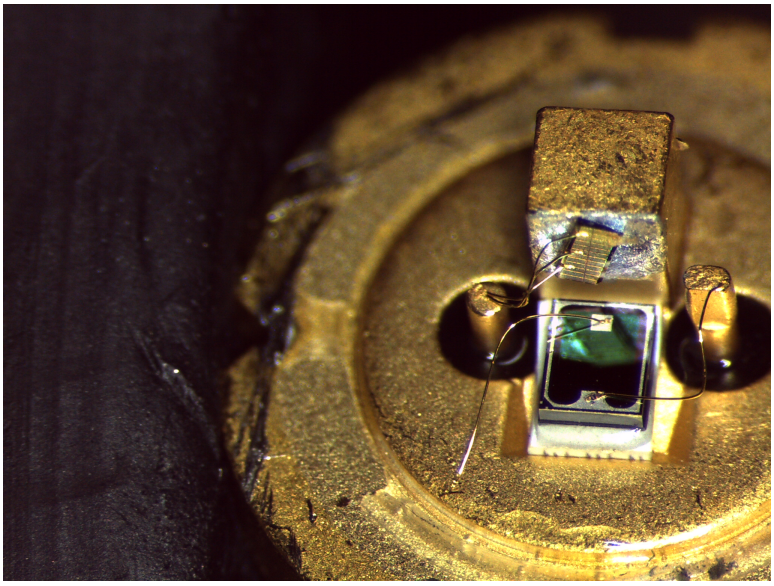

Figure 6: TO can removed from a laser diode to expose photodiode on the back facet.

4.1 Photodiode Background

The photodiode used in this project is a silicon semi-conductor device. In order to accurately model feedback it is important to derive the equivalent electrical model which is shown in Figure 7 [4].

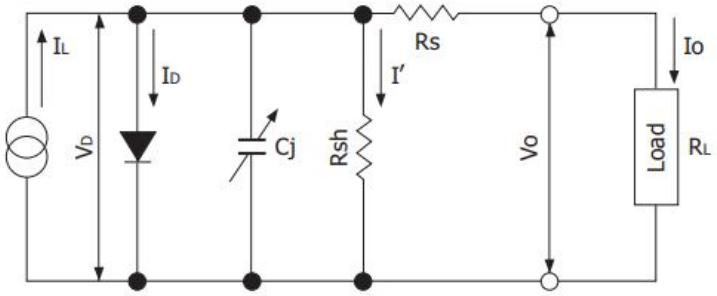

Figure 7: Equivalent electrical model of a silicon photodiode.

4.1.1 Photo Current

From Figure 7, I_L represents the photo current incident on the detector, or the current to be used as feedback. Ideally, this would be a perfect current source with no leakage, but that is never the case during actual applications.

4.1.2 Dark Current

I_D is the dark current which is defined as the electric current flowing in a photoelectric device when there is no incident light [5]. This is similar to leakage current in a standard diode. In many cases the dark current of a photodiode will be upwards of a few nano-amps and can be ignored. It is important to remember that the dark current increases when the reverse bias voltage is increased. The shot noise will also increase with an increase in dark current, which will be discussed in this chapter.

4.1.3 Junction Capacitance

C_j is the junction capacitance and the main contributor to the frequency response of the photodiode. Depending on the size of the active area, this value can range from hundreds of femto-farads to hundreds of pico-farads. The junction capacitance is the product of a very interesting phenomena of P-N junction semi-conductor devices; The boundaries of the depletion region act as a parallel plate capacitor [9]. When the reverse bias voltage on the photodiode is increased the depletion region increases, which will decrease the capacitance. Reverse biasing the photodiode is a trade-off of increased noise vs. increased frequency response.

4.1.4 Shunt Resistance

The shunt resistance, R_{SH}, is the slope of the current-voltage curve of the photodiode at the origin. Ideally the shunt resistance would be infinite, but in practice this value usually sits around $10M\Omega$.

4.1.5 Series Resistance

The series resistance, R_S, is the resistance of the contact pads, bonding wires, solder pins, and the under depleted silicon [4]. This value is usually in the milli-ohms and by comparison is the least important photodiode parameter for this project.

4.1.6 Photodiode Noise

Photodiodes have two main noise sources that the designer needs to be aware of; First is shot noise and second is Johnson Noise [4].

4.1.6.1 Shot Noise

The shot noise is an artifact of the statistical nature of photons arriving at random intervals. This means the number of electron-hole pairs that are feed is random as well as the electrons producing the photocurrent due to recombination [9]. Calculating the shot noise is essentially a way to quantize the fluctuation in photocurrent and dark current. The equation for shot noise can be found in equation 2.

$$I_{SN} = \sqrt{2q(I_L + I_D)\Delta f} \tag{1}$$

4.1.6.2 Johnson Noise

The Johnson noise of a photodiode can be attributed to the shunt resistance. This noise source is found in all resistive elements and is cause by thermal agitation of charge carriers at equilibrium [5]. The equation for Johnson noise can be found in (3).

$$I_{JN} = \sqrt{\frac{4K_B T \Delta f}{R_{SH}}} \tag{2}$$

The total noise of the photodiode is the magnitude of the shot noise and Johnson noise which can be seen in equation 4 [4].

$$I_{TN} = \sqrt{I_{SN}^2 + I_{JN}^2} \tag{3}$$

4.2 Photodiode Resistor Feedback

A simple detector can be made using only a photodiode, resistor, and an optional voltage source. An example of this circuit can be seen in Figure 8 [5].

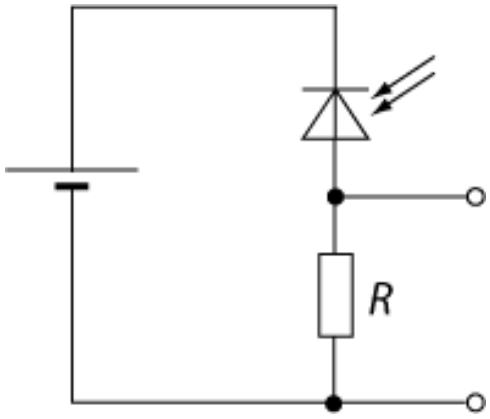

Figure 8: Basic photodiode detector with response equivalent to RC low pass filter.

4.2.1 RC Detector Schematic

Due to the equivalent electrical model of a photodiode the output voltage be calculated using equation 5.

$$V_{out} = (I_L - I_D)R \tag{4}$$

The junction capacitance of the photodiode effectively turns this circuit into a low pass filter. The

cutoff frequency for the detector can be found from equation 6 [5].

$$f_{dB} = \frac{1}{(2\pi)(R)(C_j)} \tag{5}$$

4.2.2 RC Detector Noise

The design considerations from above are used in the following calculations. The bandwidth of the RC detector cannot be accurately controlled, so the natural cutoff frequency needs to be calculated applied to the bandwidth for the noise calculations.

$$f_{dB} = \frac{1}{(2\pi)(3e3)(10e-12)} = 5.3Mhz \tag{6}$$

$$I_{SN} = \sqrt{(2)(1.6e-19)(1e-3+5e-9)(5.3e6)} = 41.2\frac{nA}{\sqrt{Hz}} \tag{7}$$

$$I_{JN} = \sqrt{\frac{(4)(1.38e-23)(300)(5.3e6)}{10e6}} = 93.7\frac{pA}{\sqrt{Hz}} \tag{8}$$

$$I_{TN} = \sqrt{41.2e-9^2 + 93.7e-12^2} = 41.2\frac{nA}{\sqrt{Hz}} \tag{9}$$

Equations 7 - 10 calculated the noise of the RC detector. A parameter called noise equivalent power (NEP) is an industry standard measurement for direct comparison of different detectors and can be found in equation 11 [5].

$$NEP = \frac{I_{TN}}{R_\lambda} = \frac{41.2\frac{nA}{\sqrt{Hz}}}{0.4} = 103\frac{nW}{\sqrt{Hz}} \tag{10}$$

The SNR can be calculated now that the NEP is known.

$$SNR = \frac{MaxPower}{NEP} = \frac{2.5mW}{103nW} = 43.8dB \tag{11}$$

4.3 Photodiode Transimpedance Feedback

A basic transimpedance amplifier (TIA) can be seen in figure 9 and will be used for calculations in this section. Due to the equivalent electrical model of a photodiode the output voltage be calcu-

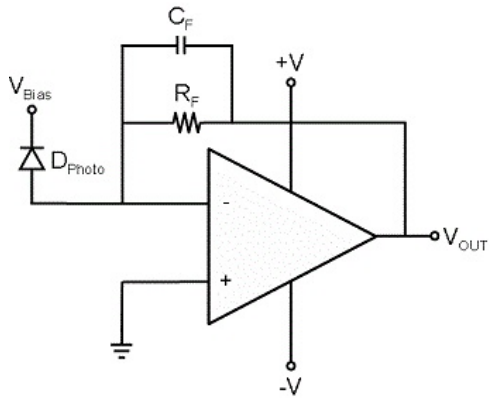

Figure 9: Typical schematic of a transimpedance amplifier.

lated using equation 13.

$$V_{out} = (I_L - I_D)(R_{FB}) \tag{12}$$

The bandwidth of the TIA is less dependent on the junction capacitance, especially if the bandwidth is being decreased. The new bandwidth can be calculated based off the feedback resistor and capacitor as shown in equation 14.

$$f_{dB} = \frac{1}{(2\pi)(R_{FB})(C_{FB}}) \tag{13}$$

4.3.1 TIA Detector Noise

The design considerations from above are used in the following calculations. The bandwidth of the TIA will be set to the desired cutoff frequency of 50kHz.

$$I_{SN} = \sqrt{(2)(1.6e-19)(1e-3+5e-9)(50e3)} = 4.0\frac{nA}{\sqrt{Hz}} \tag{14}$$

$$I_{JN} = \sqrt{\frac{(4)(1.38e-23)(300)(50e3)}{10e6}} = 9.1\frac{pA}{\sqrt{Hz}} \tag{15}$$

$$I_{TN} = \sqrt{41.2e-9^2 + 93.7e-12^2} = 4.0\frac{nA}{\sqrt{Hz}} \tag{16}$$

Equations 15-17 show that the noise current noise has been decreased by an order of magnitude in comparison to the RC detector.

$$NEP = \frac{I_{TN}}{R_\lambda} = \frac{4.0\frac{nA}{\sqrt{Hz}}}{0.4} = 10\frac{nW}{\sqrt{Hz}} \tag{17}$$

The SNR can be calculated now that the NEP is known.

$$SNR = \frac{MaxPower}{NEP} = \frac{2.5mW}{10nW} = 54.0dB \tag{18}$$

4.4 Feedback Mechanism Conclusion

First thing to note is that the bandwidth of the RC detector will fall outside of the stable range of the laser driving circuit, so the TIA is an absolute necessity for this design. The current noise contribution due to the RC detector will also fall outside of the the current noise specifications stated in Figure 1. The signal to noise ratio of the TIA has an improvement of 10dB over the RC

detector, which isn't a deal breaker by itself, but considering the other issues at hand the TIA is the clear choice for the feedback mechanism.

5 Transimpedance Amplifier Design

A transimpedance amplifier is exactly what the name suggests, a current to to voltage converter. Since the photodiode is a nearly ideal current source, the TIA is a useful analog design to output stable voltage. This chapter will go through the design steps to design a stable and reliable transimpedance amplifier.

5.1 Transimpedance Amplifier Theory of Operation

The TIA pictured in Figure 10 shows an ideal current source being fed into the inverting input of the op-amp. Section 4.1 showed that photodiodes are close to perfect current sources, so it will be modeled as such. In an ideal op-amp it is well known that the inputs draw no current. Since no current is going into the op-amp, all of the current from the photodiode must go through the feedback network. This means that the output voltage must follow Ohm's Law, $V_O = -(R_{FB})(I_P)$

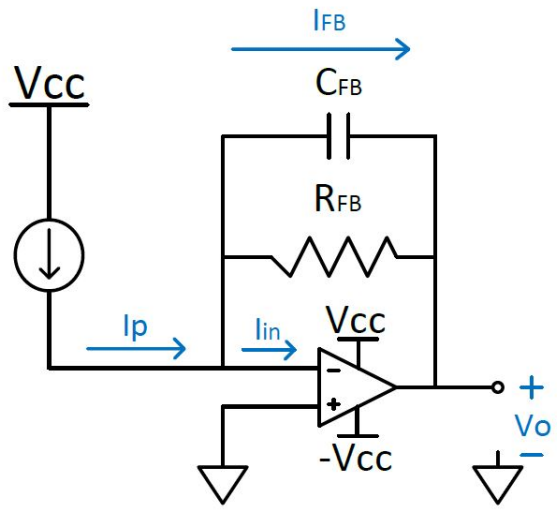

Figure 10: TIA schematic and current flow used for Laplace and time domain analyses.

5.2 Choosing the Right Amplifier

The key to a stable and reliable TIA is the amplifier choice. Just remember that not all op-amps are created equal. This section is focused on choosing the right component and narrowing down the search.

5.2.1 Amplifiers to Avoid

- Instrumentation amplifiers look harmless from the outside, but they often have undesirable traits and caveats. Proceed with extreme caution if an instrumentation amplifier is chosen for a TIA.
- Chopper amplifiers may seem like a good idea because they have a very small offset voltage, but they can have interesting behavior in the frequency domain.
- Bi-Polar amplifiers can be dangerous due to the high input bias current. Input bias current will get pulled across the feedback resistor producing an unwanted gain.

5.2.2 Amplifiers to Consider

The type of amplifiers under consideration for the transimpedance amplifier will be general purpose CMOS and JFET. The below list identifies the important design parameters.

- Gain Bandwidth Product $<$ 5MHz
- Input Bias Current $<$ 5pA
- Input Offset Current $<$5pA
- Supports Dual Supply $> \pm$5V
- Unity Gain Stable
- Offset Voltage $<$ 5mV

- Rail to Rail Output
- Current Noise $<$ 1nA/$\sqrt{Hz}$

The Analog Devices website provides a parametric search option which gave the results shown in Figure 10. The requirement for input offset voltage was increased in order to give more parts to compare. There are 4 parts that meet all of the criteria: ADA4665-2, AD795, LT1462, and LT1464. The GBP for the LT1462 is too low for this design, leaving 3 parts to choose from. Any of these 3 amplifiers would work just fine, however the AD795 only has one operational amplifier per package, so a part with two amplifiers per package will be chosen to accommodate the dual stage TIA. The LT1464 is not a rail to rail amplifier, which is important because ground sensing on the inputs will affect performance. This leaves one part to choose from, which is the ADA4665-2.

Part #	Current Noise (A/rtHz)	Ios (max) (A)	Rail to Rail	GBP (typ) (Hz)	Vos (max) (V)	Ibias (max) (A)	Vs span (V)
ADA4665-2	50f	1p	Both	1.2M	4m	1p	16
AD795	600a	1p		1.6M	500µ	2p	36
LT1462	500a	1.2p		175k	800µ	2p	40
LT1464	400a	1.2p		1M	800µ	2p	40
AD820	800a	10p	Output	1.8M	1m	10p	30
AD822	800a	12p	Output	1.8M	1.5m	12p	30
AD8663	50f	35p	Output	540k	300µ	45p	16
AD8667	50f	35p	Output	540k	300µ	45p	16
AD8657	100f	40p	Both	230k	350µ	20p	18
LT6003	12f	80p	Both	2k	500µ	90p	16
LT6004	12f	80p	Both	2k	500µ	90p	16
LT1495	10f	100p	Both	2.7k	375µ	1n	36
LT1673	10f	100p	Both	12k	375µ	1n	36
LT1672	10f	100p	Both	12k	375µ	1n	36
LT1494	10f	100p	Both	2.7k	375µ	1n	36
LT1008	20f	100p		1M	120µ	100p	40
OP297	20f	100p		500k	50µ	100p	40

Figure 11: Parametric op-amp search from Linear Technology and Analog Devices.

5.3 Designing the Feedback Network

The datasheet from Figure 1 states that the APC loop speed will be 20us which correlates to a speed of 50kHz. Figure 1 also states that the APC loop set range will vary from 0-3V and the maximum photodiode current will be 1mA. This is all the information needed to design the feedback network.

$$f_{APC} = \frac{1}{(2\pi)(R_{FB})(C_{FB})} \tag{19}$$

$$R_{FB} = \frac{V_{PD-max}}{I_{PD-max}} = \frac{3V}{1mA} = 3k\Omega \tag{20}$$

$$50kHz = \frac{1}{(2\pi)(3k)(C_{FB})} \rightarrow C_{FB} = 1nF \tag{21}$$

5.4 Compensating for Non-Ideal Situations

In the real world, nothing is ideal so the designer needs to be aware of and compensate for these cases whenever possible. There are two issues with the TIA that need be addressed. First, the op-amp does draw some current on the inputs, so balancing the loads seen by the input terminals will balance the input offset current of the amplifier and keep the amplifier from translating this current into the overall gain of the circuit. Second, a small capacitor should be placed at the non-inverting input to ground to help filter out any high frequency noise on the reference input rail. Figure 12 is the TIA design up until this point.

5.5 Voltage Supply Rails

The op-amp chosen, ADA4665-2, is a rail to rail op-amp meaning the inputs can sense Vcc to -Vcc and the output can swing from Vcc to -Vcc. Most rail to rail op-amps can't actually swing the full rail, they usually fall short by about 10mV, so this needs to be taken into consideration. The output needs to swing from 0 to 3V, so the minimum Vcc should be $\pm$3.3V. In this configuration the TIA can sense the reference ground because the negative rail will be pulled to -Vcc.

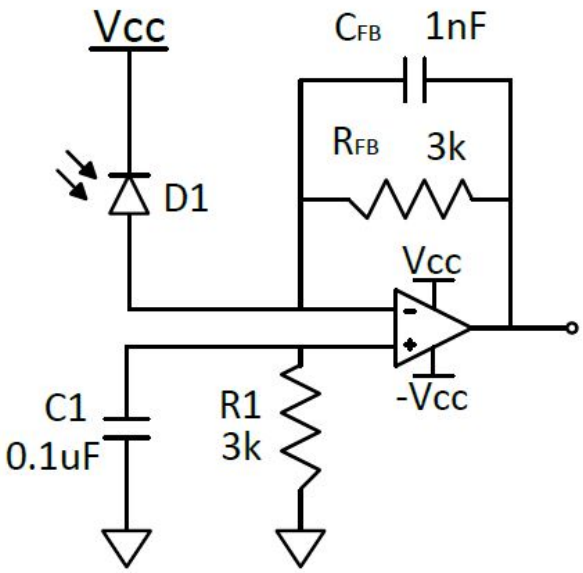

Figure 12: Modified TIA schematic to compensate for non-ideal op-amp behavior.

5.6 TIA Stage 1 Stability

During the general electronic design, the majority of circuitry will be simulated using SPICE. After the electrical design is complete, the entire system will be modeled in the Laplace domain and simulated in Matlab to confirm the performance of the control system.

5.6.1 Gain and Phase Margin

The gain and phase vs. frequency can be plotted from the SPICE simulation to derive the gain and phase margins. Figure 13 shows the phase at a gain of 0dB is 62, so the phase margin of this design is 62 degrees. The sweet spot for stability in transimpedance amplifiers is a phase margin between 45 and 90 degrees [7]. The gain margin for this design is infinite as the phase never drops below -180 degrees. The SPICE simulation shows that the raw amplifier design will be stable.

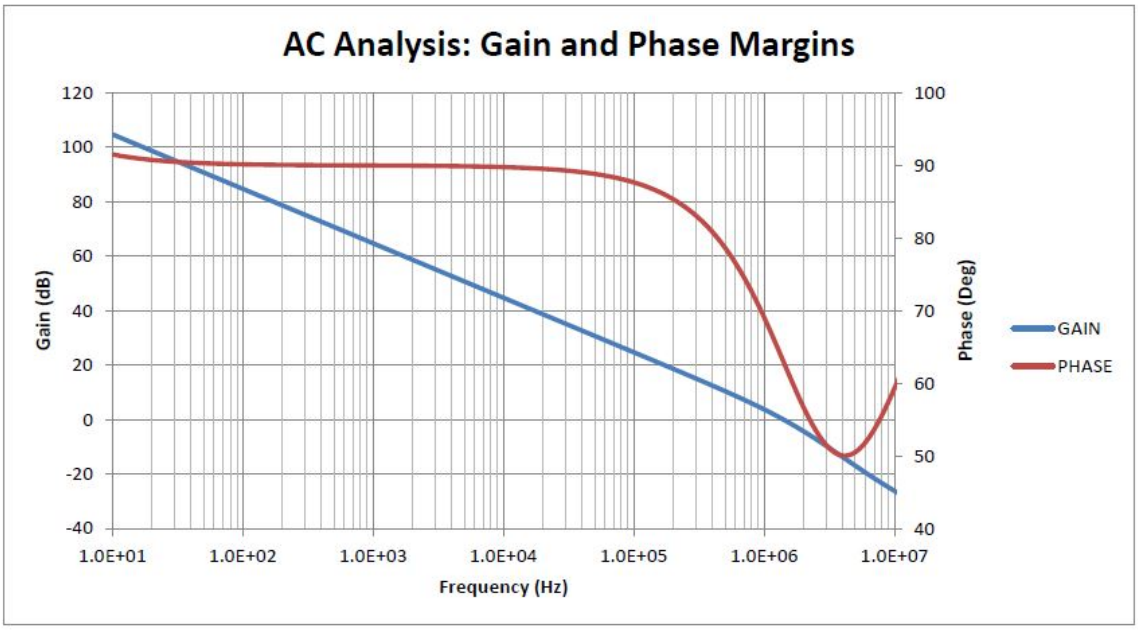

Figure 13: Gain and phase margin graph of modified TIA derived from SPICE simulation.

5.6.2 Feedback Factor

Like any circuit with an operational amplifier and feedback, the TIA can be broken down into an amplifier with open-loop gain and a feedback network which will include the feedback resistor, capacitor, and the photodiode. The stability analysis in section 5.6.1 simulates the electronics with a perfect current source. This section will focus on analyzing the stability with the introduction of the a photodiode in place of the perfect current source.

Start by mathematically defining the open loop gain of the amplifier for a single pole system.

$$A_{VOL(j\omega)} = \frac{A_{VOL}}{1 + j\frac{\omega}{\omega_{PD}}} \tag{22}$$

The feedback network comprised of a one pole RC filter, the junction capacitance of the photodiode, and the input capacitance of the op-amp as seen in Figure 14.

$$\beta(j\omega) = \frac{X_{Cin}}{R_{FB}//X_{FB} + X_{Cin}} \tag{23}$$

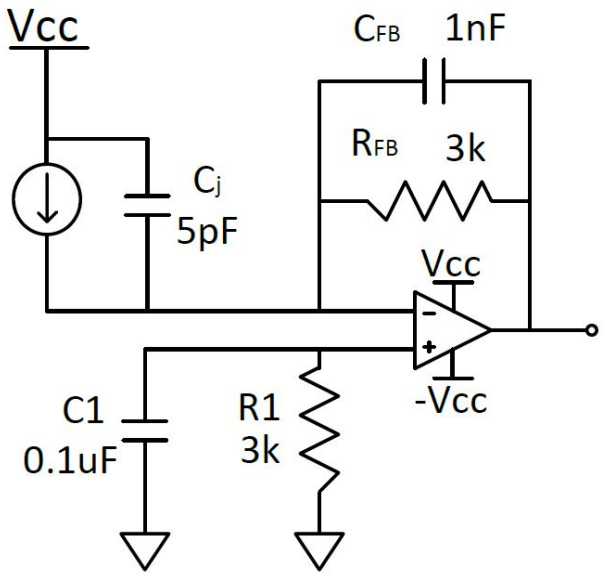

Figure 14: TIA modeled with photodiode equivalent model to account for input impedance.

$$\beta(j\omega) = \frac{1 + j\omega R_{FB} C_{FB}}{1 + j\omega R_{FB}(C_{FB} + C_{in})} \tag{24}$$

Equation 23 and 25 [7] can be used to graph the open loop gain vs. the feedback network to visually determine the stability. The Barkhausen stability criterion states that a closed loop system can become unstable if there is not sufficient phase margin, $A_{VOL}\beta \geq 1$. Before graphing the feedback and open loop gain, it is important to find the minimum stable frequency of the feedback. If the system does not provide enough margin then overcompensation should be built into the system to ensure the circuit never becomes unstable [7].

$$f_{min} = \sqrt{\frac{f_{GBWP}}{2\pi R_{FB}(C_{FB} + C_{in})}} \tag{25}$$

Taking a look figure 15, it is clear that the feedback system is flat when crossing over the roll off of the open loop gain of the amplifier. If the feedback factor was climbing at a rate of 20dB/dec

and the open loop gain was decreasing at a rate of 20dB/dec when they crossed, then the circuit would be doomed to fail and oscillate wildly. This design is showing that the TIA will be stable and approximately 10kHz of overcompensation has been designed in.

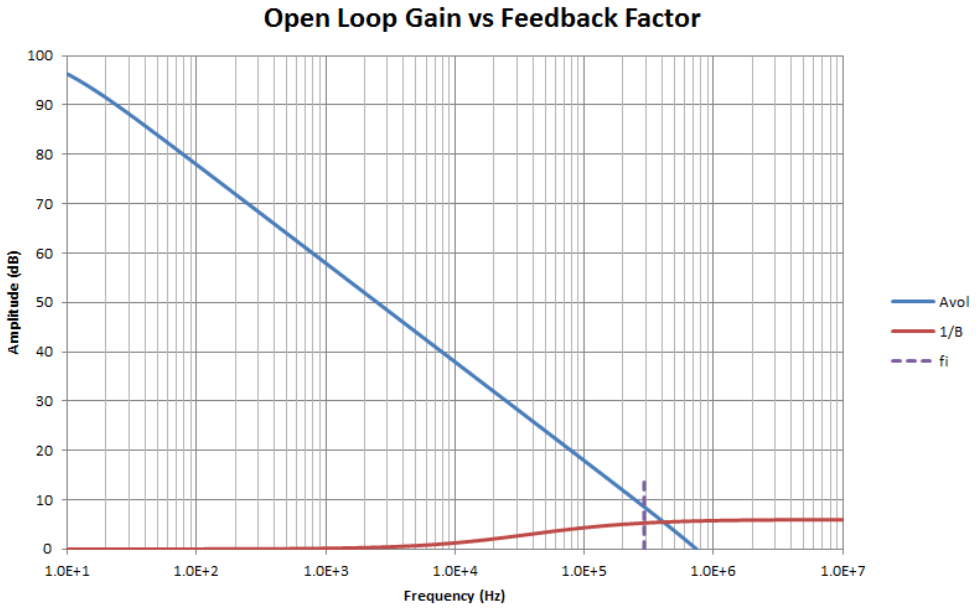

Figure 15: Graph of open loop gain vs. feedback factor for modified TIA with photodiode input.

5.6.3 TIA Noise Performance

The equations from chapter 4 were taken and applied to the actual values in the design. Figure 16 [10] shows the noise contribution due to all of the components in the design such as the op-amp, the photodiode, and the feedback network. Figure 17 [10] is the noise equivalent power of the receiver, which determines the noise floor of the system.

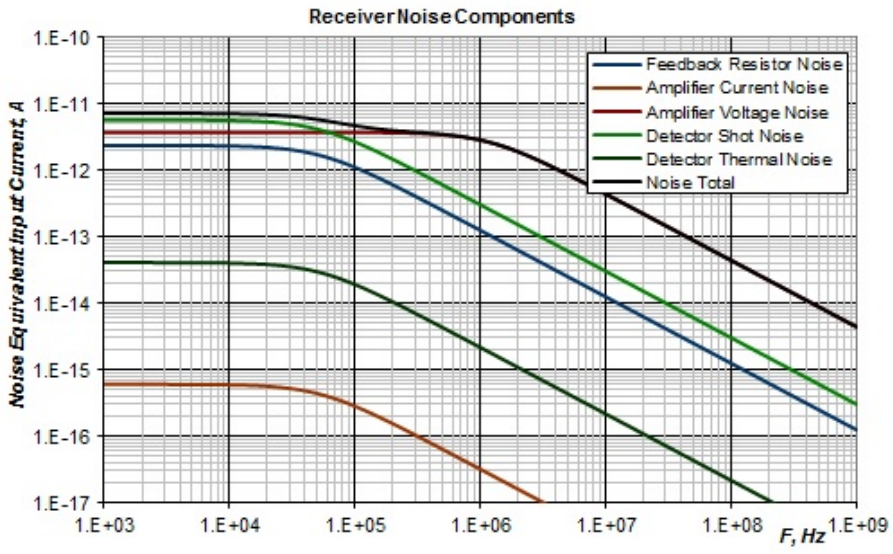

Figure 16: Noise contributors and magnitude for modified TIA.

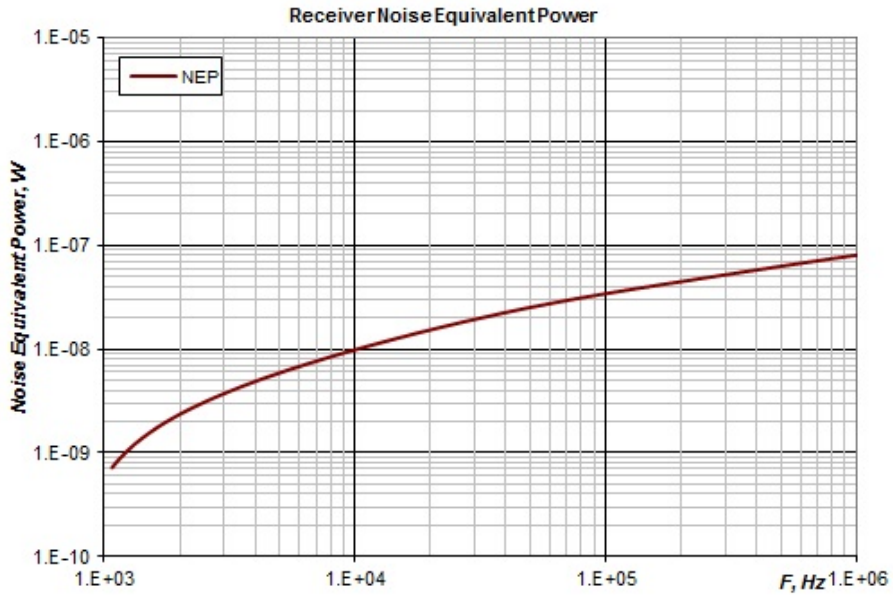

Figure 17: Noise equivalent power of modified TIA.

5.6.4 TIA Stage 2

The purpose of this stage is simple, to invert the output voltage generated by stage 1 back into a positive voltage. This amplifier is effectively seen as a buffer by the rest of the system. There

should be no attenuation of the analog signal from the first stage to pass through this second stage, so the cutoff frequency will be set at least 5 times larger than the first stage. The gain bandwidth product of the amplifier, ADA 4665-2, needs to be greater than 250kHz, which it is at 1.2MHz. The second stage of the TIA is low risk and easy to implement, therefore it is not worth the time or effort to simulate. The final TIA design will look like Figure 18.

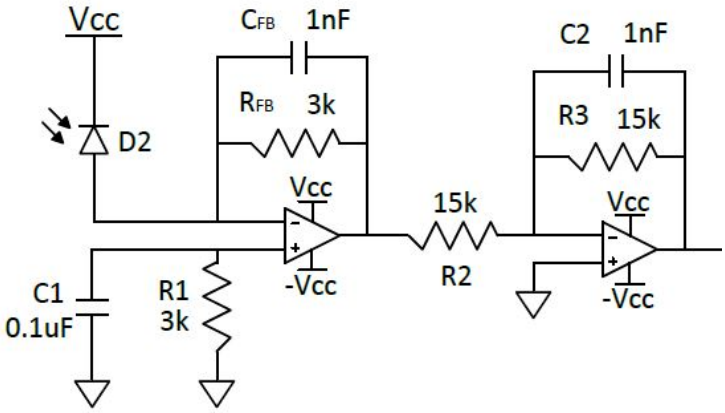

Figure 18: Dual stage transimpedance amplifier design to be used as the feedback mechanism.

5.6.5 Component Selection

Now that the design is complete and the performance is satisfactory, the remainder of components should be chosen for maximizing performance.

The noise calculations assumed that thin or thick film chip resistors will be used. To have a slight noise improvement, but much higher cost a metal foil resistor could be used. For this design high quality chip resistors with tight tolerances (0.1%) and small drift over temperature (50ppm/C) will suffice.

For the capacitors, ceramic with a high quality temperature coefficient will be an excellent choice. For the 1nF capacitors a temperature coefficient of NP0 or C0G should be chosen. For the 0.1uF capacitor, X7R will be sufficient. These temperature coefficients are very stable over a wide temperature range and would be suitable for this design. Mica or film capacitors could also be a valid

choice, but they typically come in larger package sizes and they are only available in very low capacitive values.

5.7 TIA Design Conclusions

This chapter extensively and exhaustively stepped through the design, simulation, and stability analysis of the transimpedance amplifier which will be providing feedback for the control system. The TIA is the backbone of the entire system, so stability and reliability of this circuit is critical to the design. Upon the conclusion of this chapter, there is high confidence that the TIA will perform as expected.

6 APC Design and Integration

The previous chapters were dedicated to understanding the opto-electronics behind the system and designing robust building blocks for the purpose of integrating them into an automatic power control laser driver.

6.1 APC Block Diagram

The basic idea behind the APC laser driver is to use a constant current source to drive a laser and use a photodiode as a feedback mechanism to lock the optical output power to the current set point as seen in Figure 19.

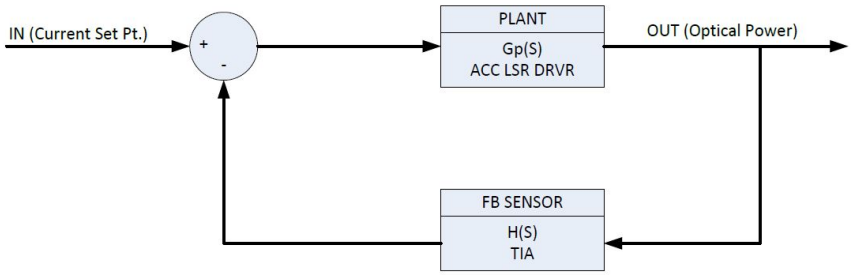

Figure 19: Block diagram for automatic power control laser driver feedback system.

6.2 Integration

Following the block diagram from 6.1 the schematics for the APC laser driver can be derived and seen below in figure 20.

6.3 Derivation of System Transfer Function

In order to put the system into Simulink/Matlab and run analyses on the theoretical performance, the transfer function for each circuit needs to be derived.

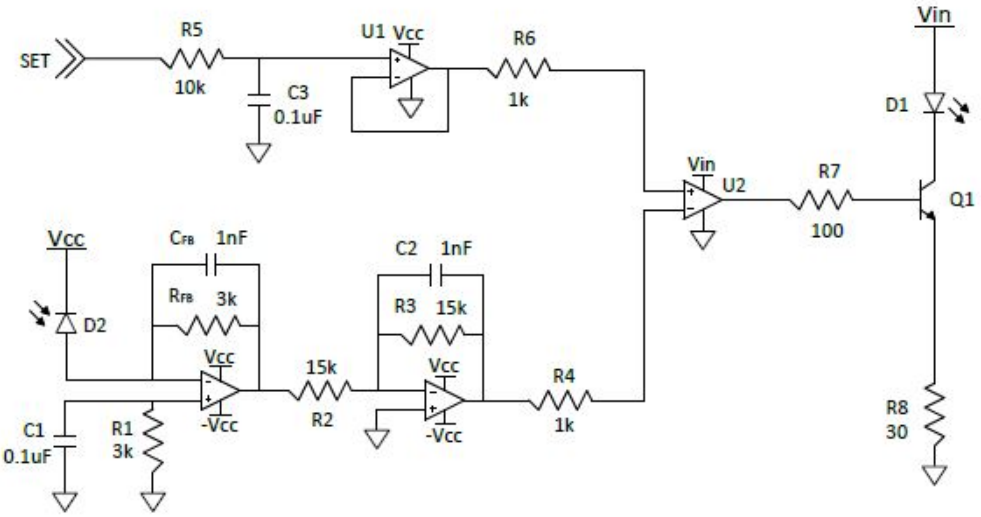

Figure 20: Schematic for APC laser driver.

6.3.1 Set-Point Circuit

The operational amplifier is in a unity gain voltage follower configuration with a passive low pass filter at the non-inverting input. Figure 21 will visualize the mathematical analysis below.

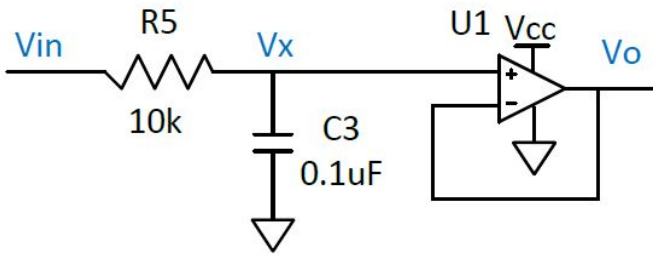

Figure 21: Current set point schematic for transfer derivation.

Assumptions for derivation of transfer function.

- The non-inverting and inverting input of the op-amp are held at the same potential
- Vo = Vx
- The op-amp input bias current is approximately 0.

Now nodal analysis can be performed at Vx

$$\frac{V_{in} - V_x}{R_5} - \frac{V_x}{\frac{1}{sC_3}} = 0 \tag{26}$$

Substituting in Vo for Vx

$$V_{in} - V_o = sR_5C_3(V_o) \tag{27}$$

$$V_{in} = V_o(sR_5C_3 + 1) \tag{28}$$

Therefore the transfer function for the set circuit is

$$G_{set}(s) = \frac{V_o}{V_{in}} = \frac{1}{(sR_5C_3 + 1)} \tag{29}$$

6.3.2 TIA Stage 1 Transfer Function

The transfer function of stage 1 will be derived first, then the second stage, then the transfer function of entire TIA gain block can be found. An important note to remember is that the transfer function for the TIA will be output voltage over input current because the laser driver set point it locked to photodiode current. Assumptions for stage 1

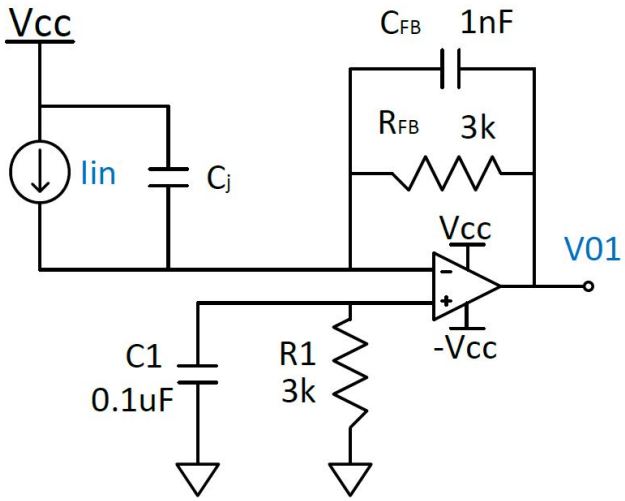

Figure 22: First stage TIA schematic for derivation of transfer function.

- The non-inverting and inverting input of the op-amp are held at the same potential, 0V
- The op-amp input bias current is 0, so C1 and R1 can be ignored.

Kirchoff's current law states the sum off all currents into a node is equal to zero.

$$I_{in} = I_{Cj} + I_{FB} \tag{30}$$

$$I_{in} = \frac{Vin-}{\frac{1}{sC_j}} + \frac{V_{in-} - V_{O1}}{R_{FB} \| C_{FB}} \tag{31}$$

$$R_{FB} \| C_{FB} = \frac{R_{FB} \frac{1}{sC_{FB}}}{R_{FB} + \frac{1}{sC_{FB}}} = \frac{R_{FB}}{1 + sC_{FB}R_{FB}} \tag{32}$$

The potential of Vin- is 0 due to Vin+, therefore the system simplifies down to the following

$$I_{in} = -\frac{V_{O1}}{\frac{R_{FB}}{1+sC_{FB}R_{FB}}} \tag{33}$$

The transfer for stage 1 becomes

$$G_{TIA1}(s) = \frac{V_{O1}}{I_{in}} = -\frac{R_{FB}}{1 + sC_{FB}R_{FB}} \tag{34}$$

6.3.3 TIA Stage 2 Transfer Function

The second stage is essentially just an inverting unity gain buffer with an active low pass filter as seen in figure 23.

Nodal analysis can be performed at Vx to obtain the following equation

$$\frac{V_{in} - V_x}{R_2} + \frac{V_{O2} - V_x}{R_3 \| C_2} = 0 \tag{35}$$

$$\frac{V_{O2}}{V_{O1}} = -\frac{R_3 \| C_2}{R_2} \tag{36}$$

$$R_3 \| C_2 = \frac{R_3 \frac{1}{sC_2}}{R_3 + \frac{1}{sC_2}} = \frac{R_3}{1 + sC_2R_3} \tag{37}$$

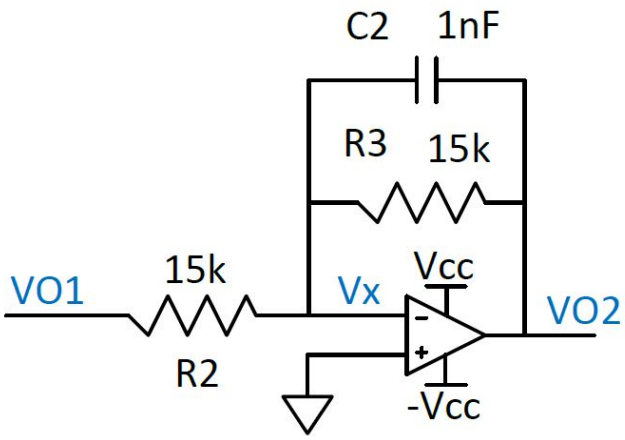

Figure 23: Second stage TIA schematic for derivation of transfer function.

$$G_{TIA2}(s) = \frac{V_{O2}}{V_{O1}} = -\frac{R_3}{R_2 + sC_2R_3R_2} \tag{38}$$

6.3.4 TIA Transfer Function

Multiplying the transfer functions derived for stage 1 and stage 2 will result in the overall transfer function for the transimpedance stage.

$$G_{TIA}(s) = G_{TIA1}(s)G_{TIA2}(s) = \frac{V_{O1}}{I_{in}}\frac{V_{O2}}{V_{O1}} = \frac{V_{O2}}{I_{in}} \tag{39}$$

$$\frac{V_{O1}}{I_{in}}\frac{V_{O2}}{V_{O1}} = \frac{-R_{FB}}{1 + sC_{FB}R_{FB}}\frac{-R_3}{R_2 + sC_2R_3R_2} \tag{40}$$

$$G_{TIA}(s) = \frac{R_{FB}R_3}{(1 + sC_{FB}R_{FB})(R_2 + sC_2R_3R_2)} \tag{41}$$

6.3.5 Driving Transistor Transfer Function

Thevenin's Theorem can be used to derive the transfer function of the BJT. Also, remember that the goal of the system is a voltage controlled current source, so the gain of this block will be output current over the input voltage. Refer to Figure 24 for a starting point.

Figuring out the exact impact the transistor will have on the circuit will start by substituting the

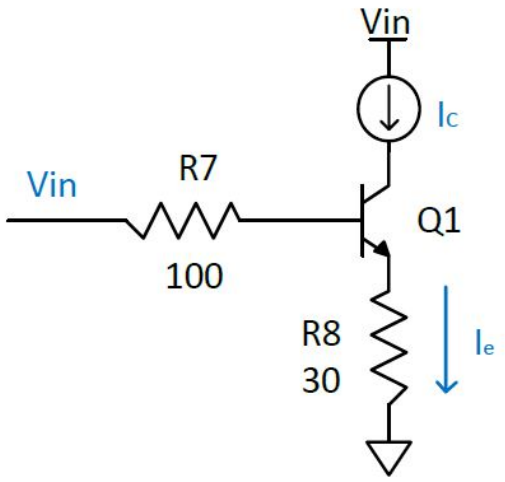

Figure 24: Laser driving transistor schematic for analysis of transfer function.

BJT with it's equivalent model seen in Figure 25. Thevenin's Theorem requires the circuit to be

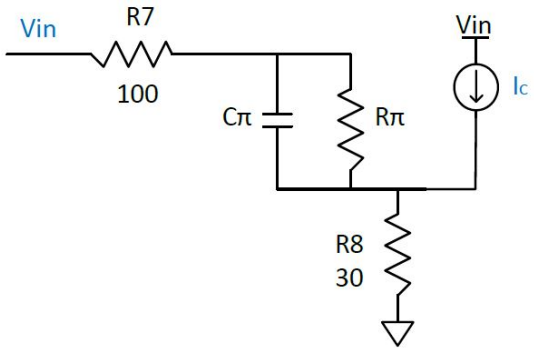

Figure 25: Equivalent electrical model of BJT for deriving the transfer function.

analyzed in two ways, first with an open circuit voltage, and second with a short circuit current [8]. An open circuit is first placed at R8 to achieve the following:

$$V_{oc} = V_{in} - I_b(R_7 + R_\pi \| C_\pi) \tag{42}$$

Since R8 has been removed for this evaluation the following is true:

$$I_b + I_c = 0 \tag{43}$$

$$V_{oc} = V_{in} \tag{44}$$

Next step is to find the short circuit current be replacing R8 with a short.

$$I_{sc} = I_b + I_c = I_b + \beta I_b \tag{45}$$

$$I_{sc} = \frac{V_{in}}{R_7 + R_\pi \| C_\pi}(1+\beta) \tag{46}$$

The Thevenin resistance can be found by dividing the open circuit voltage and short circuit current.

$$R_{th} = \frac{V_{oc}}{I_{sc}} = \frac{V_{in}}{R_7 + R_\pi \| C_\pi}(1+\beta) \tag{47}$$

$$R_{th} = \frac{V_{in}}{\frac{V_{in}}{R_7 + R_\pi \| C_\pi}(1+\beta)} \tag{48}$$

$$R_{th} = \frac{R_7 + R_\pi \| C_\pi}{1+\beta} \tag{49}$$

The Thevenin equivalent circuit is shown in Figure 26 and the transfer function will be derived from this model.

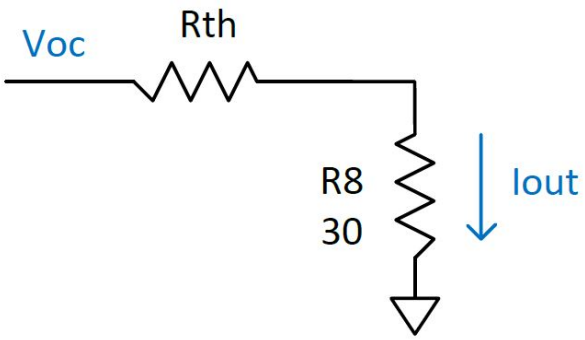

Figure 26: Thevenin equivalent circuit of driving transistor.

$$V_{in} = (R_{th} + R8) I_{out} \tag{50}$$

$$\frac{I_{out}}{V_{in}} = \frac{1}{R_{th} + R8} \tag{51}$$

$$G_{LSR}(s) = \frac{I_{out}}{V_{in}} = \frac{1}{\frac{sR_7R_\pi C_\pi + R_7 + R_\pi}{(1+\beta)(sR_\pi C_\pi + 1)} + R8} \tag{52}$$

7 Laplace Simulation with Matlab

The transfer functions from chapter 6 are put into Matlab and the step response along with the bode plots are analyzed to ensure system stability

7.1 Current Set Point Amplifier

The transfer function derived in chapter 6 was put into Matlab and simulated. The simulation results match the theoretical calculations which is expected due to the circuitry being a simple single pole RC filter. The step response shown below is displaying a 10-90 rise time of 2.2ms. The bode plot shows that the set point circuit is closed loop stable, has a cut off frequency of 150Hz, and a phase margin of 90 degrees.

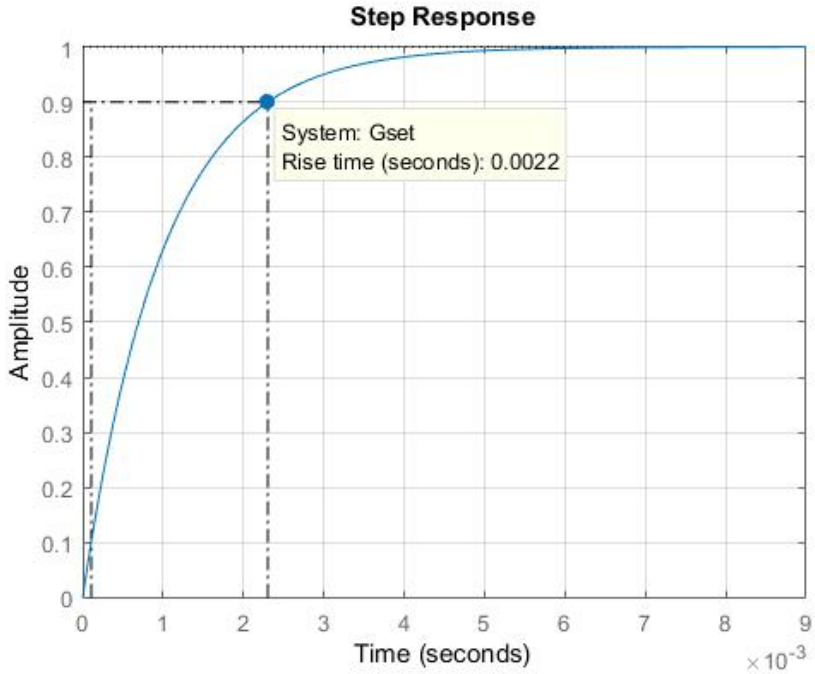

Figure 27: Current set point amplifier response to step input.

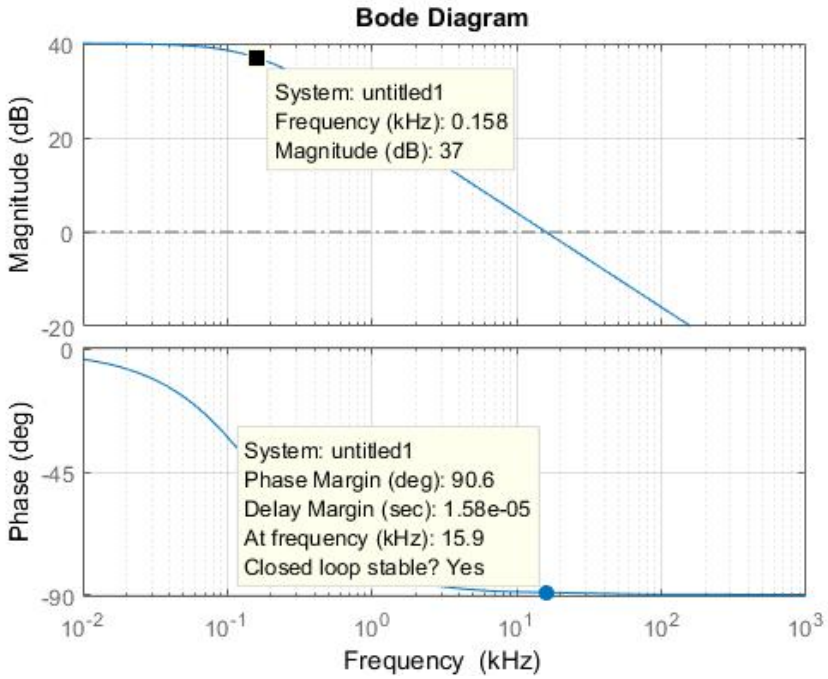

Figure 28: Current set point amplifier frequency response.

7.2 Transimpedance Amplifier

7.2.1 Stage 1

The first results from the first stage are shown below. The step response rise time matches with the theoretical value. The amplitude y-axis is also the output of the first stage in milli-volts. The bode plot cutoff frequency matches the expected value of 50kHz, however the phase margin shown is 90 degrees which is not correct. The effect of the photodiode and amplifier input capacitance were not taken into consideration in the model, so the analysis mimics a single pole RC filter.

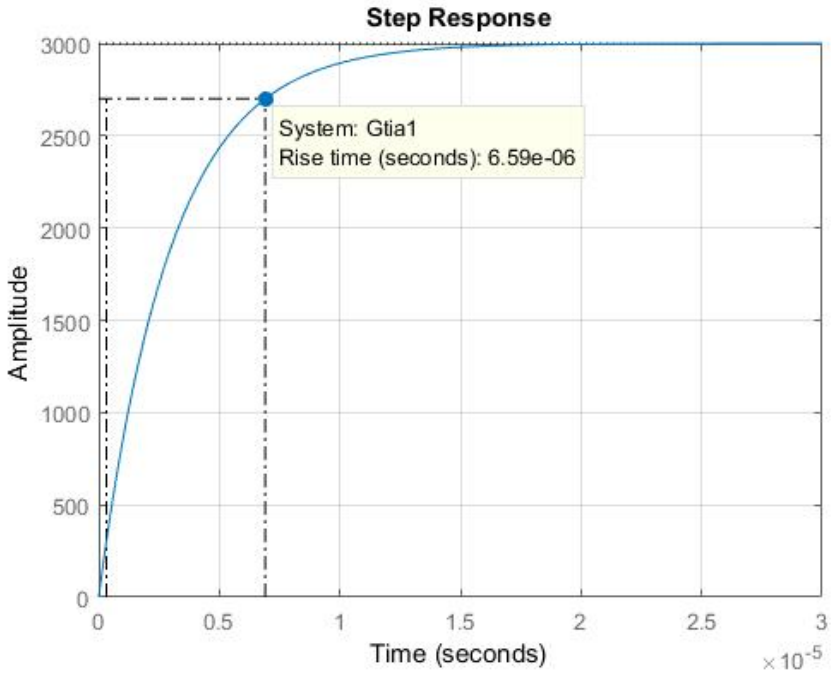

Figure 29: First stage of TIA response to step input.

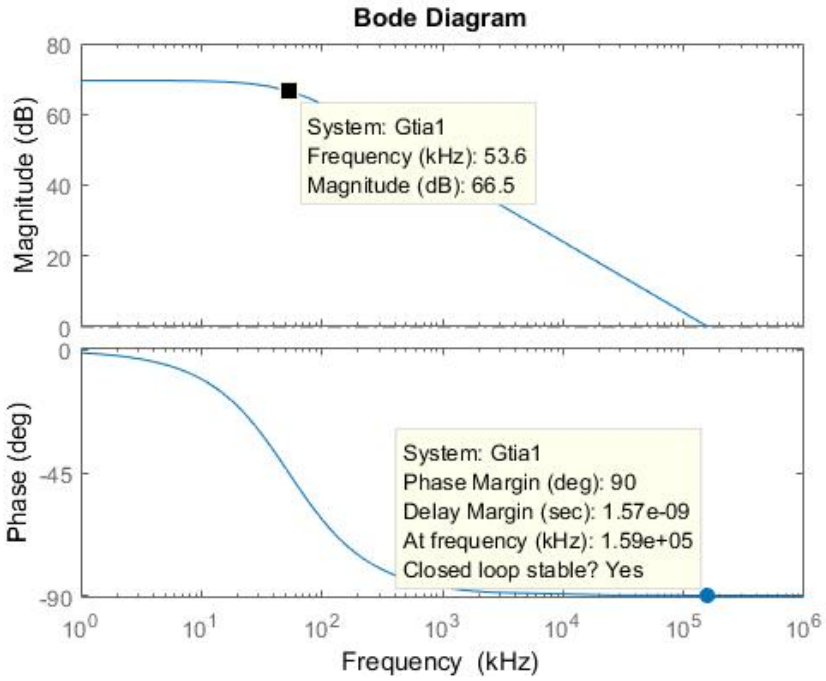

Figure 30: First stage of TIA frequency response.

7.2.2 Stage 2

The purpose of this stage is to pass through all the analog information from the first stage and invert the voltage back to a positive feedback signal. The output in practice will mimic the first stage, however this simulation does not show an amplitude of 3000 because the input from stage 2 is isolated from stage 1 during this simulation. The rise time is 10 times quicker than stage 1 matching the design and the cutoff frequency is 10 times greater than the first stage as dictated by the design. This stage is also closed loop stable.

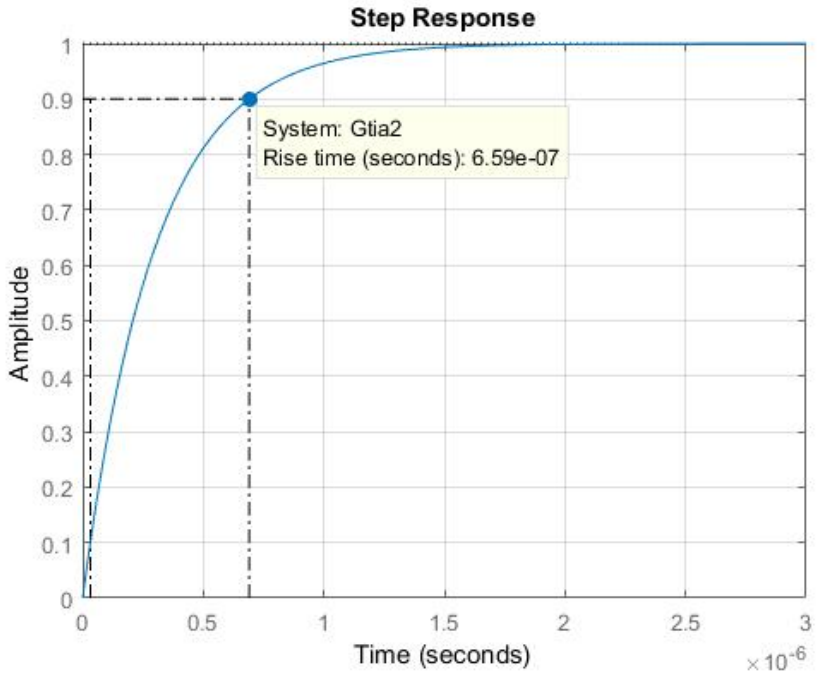

Figure 31: Second stage of TIA response to step input.

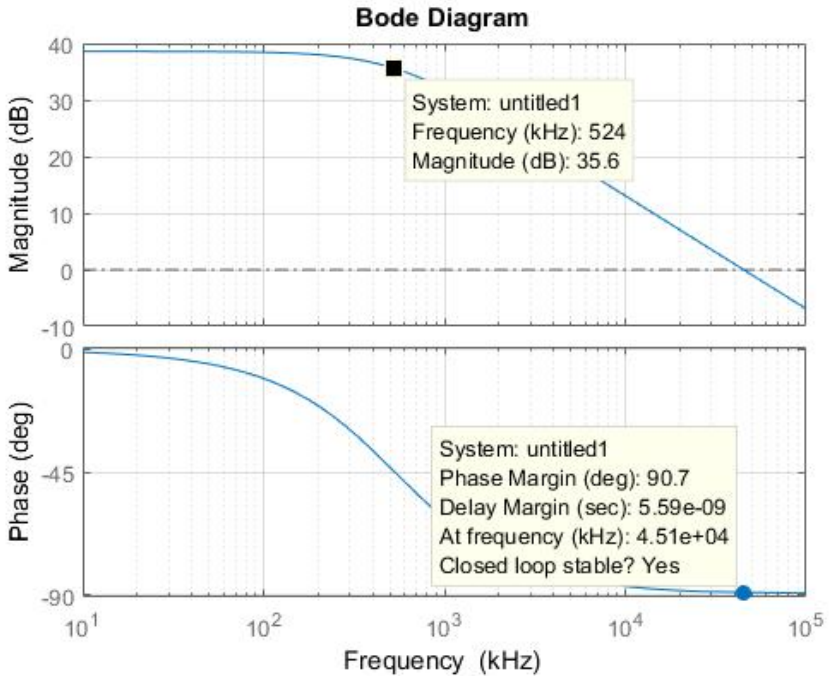

Figure 32: Second stage of TIA frequency response.

7.2.3 Dual Stage Transimpedance Amplifier

When stage 1 and stage 2 are integrated together the output performance mimics stage 1 which is the desired performance.

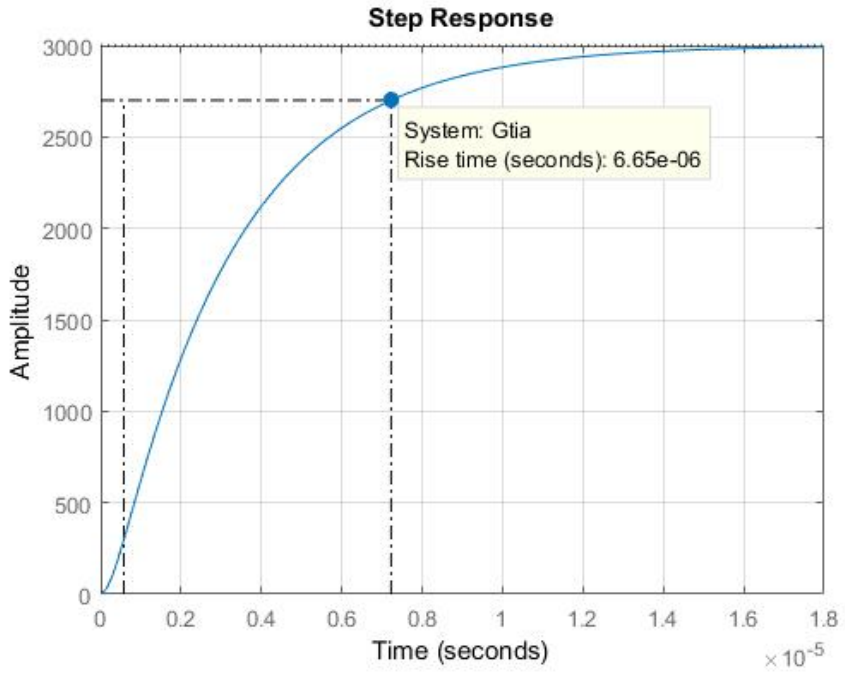

Figure 33: Dual stage transimpedance amplifier response to step input.

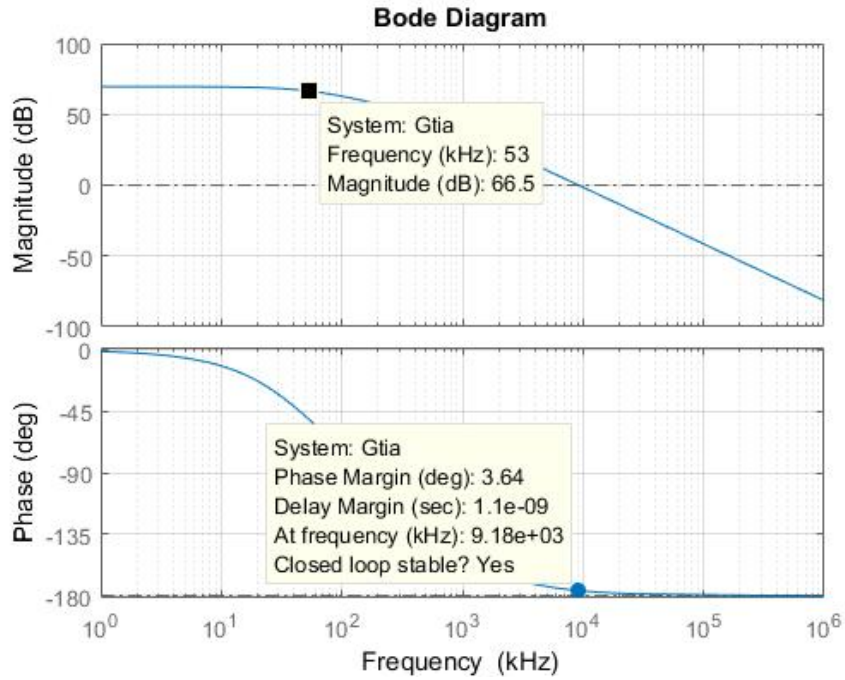

Figure 34: Dual stage transimpedance amplifier frequency response.

7.3 Driving Transistor

It is a universal knowledge that an emitter follower circuit has a gain very close to 1. The theoretical limit approaches 1, but in practice the transfer function will be just shy of 1. The simulation of the driving circuit shows this to be true. The rise time is very quick because the capacitance of the equivalent model is small. The transfer function is the collector current versus the input voltage with a maximum current of 100mA so the y-axis of the step plot is in milli-amps. The bode plot shows that the impedance of the transistor is almost completely resistive, so it is very stable over a large range of frequencies. The knowledge of emitter-follower gain can also be observed in the magnitude of the bode plot.

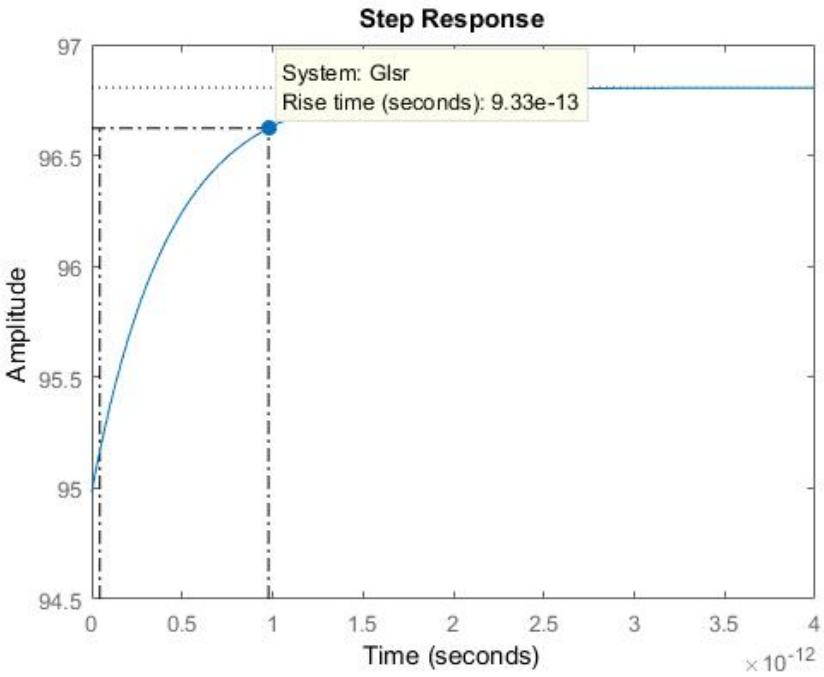

Figure 35: Driving transistor response to step input.

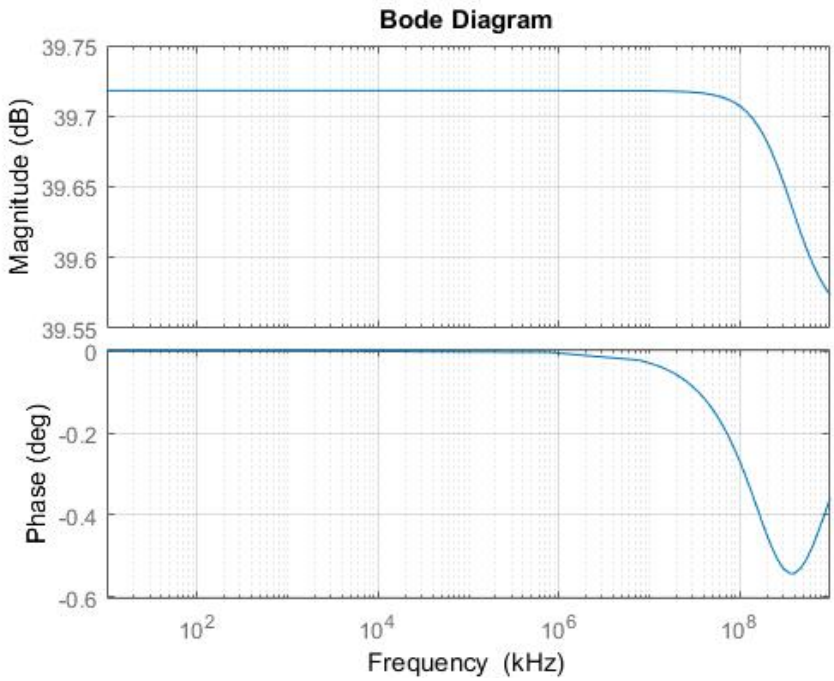

Figure 36: Driving transistor frequency response.

7.4 Matlab Script

```
% John Petrilli
% ELEG 600V
% Fully Analog Laser Driver w/ Active FB Control
% APC Laser Driver
% 15.Apr.2018

clear all
s = tf('s');
w = logspace(-1,2,200);
t = [0:0.01:10];

%Define Variables
Rin = 300;
```

```
14 R1 = 3000;
15 R2 = 3000;
16 R3 = 3000;
17 R4 = 1000;
18 R5 = 10000;
19 R6 = 1000;
20
21 R7 = 100;
22 R8 = 30;
23 Rfb = 3000;
24 Rpi = 60;
25
26 C1 = 0.1e-6;
27 C2 = 100e-12;
28 C3 = 0.1e-6;
29 Cpi = 25e-12;
30 Cfb = 1e-9;
31
32 Beta = 100;
33
34 %Define Transfer Functions
35 Gset = 1/(s*R5*C3+1)
36 Gtia1 = Rfb/(1+s*Cfb*Rfb)
37 Gtia2 = R3/(R2+s*C2*R3*R2)
38 Gtia = Gtia1*Gtia2;
39 Glsr1 = (R8*(Beta+1))/( (R8*(Beta+1))+R7+(s*Rpi*Cpi/(Rpi+s*Cpi))
       )
40 Glsr = Glsr1*100;
41
```

```
% Stability & Response Analysis of TIA Stage 1
figure(1)
bode(Gtia1)
figure(2)
step(Gtia1)
% Stability & Response Analysis of TIA Stage 2
figure(3)
bode(100*Gtia2)
figure(4)
step(Gtia2)
% Stability & Response Analysis of TIA
figure(5)
bode(Gtia)
figure(6)
step(Gtia)
% Stability & Response Analysis of Set Point Ckt
figure(7)
bode(100*Gset)
figure(8)
step(Gset)
%Stability & Response Analysis of Drvr Ckt
figure(9)
step(Glsr)
figure(10)
bode(Glsr)
```

7.5 APC System Simulation

The model shown below takes the transfer functions of the individual blocks and puts them into a Simulink model.

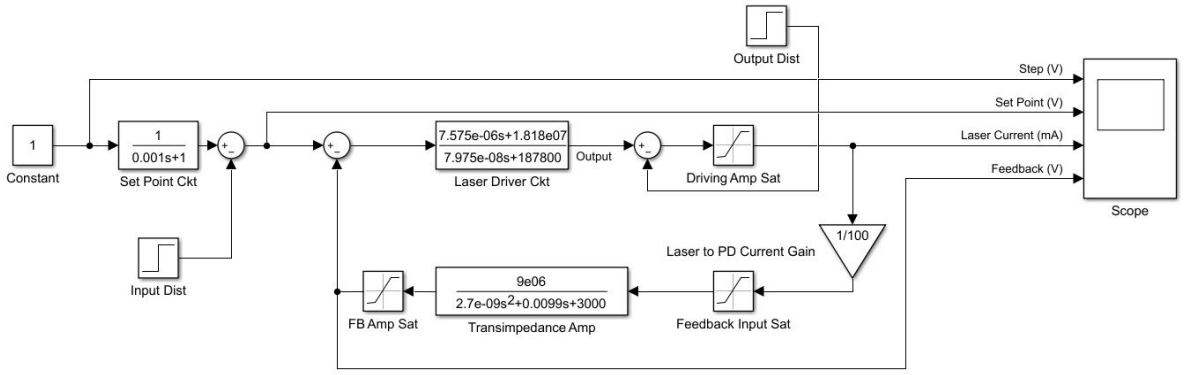

Figure 37: Simulink model of automatic power control laser driver.

The below figure from the Simulink scope is confirmation that the system is stable and working as expected. The step function comes in from 0-3V which is the input range available to the user. The feedback signal tracks the input signal because its bandwidth is about 300 times faster. The laser current shows that it stabilizes at 100mA which is expected by design.

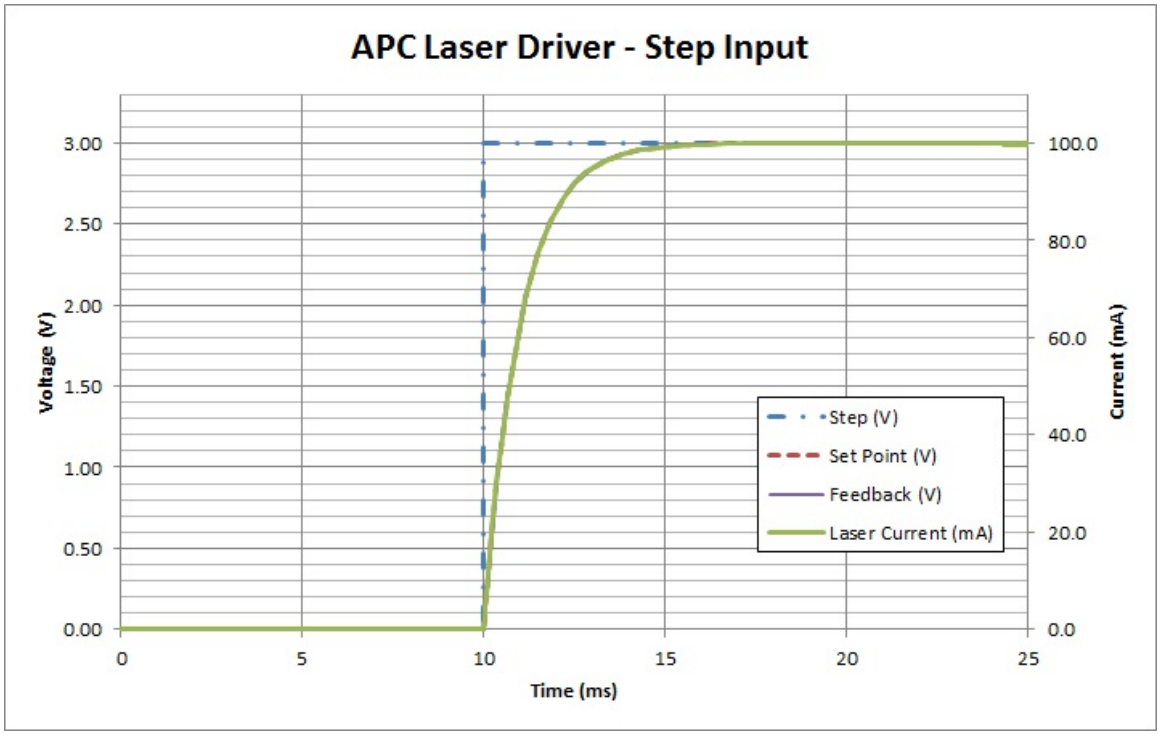

Figure 38: Simulink response to step input on APC laser driver system.

When an output disturbance of 10% is introduced into the system an overshoot of 20% and undershoot to ground is observed.

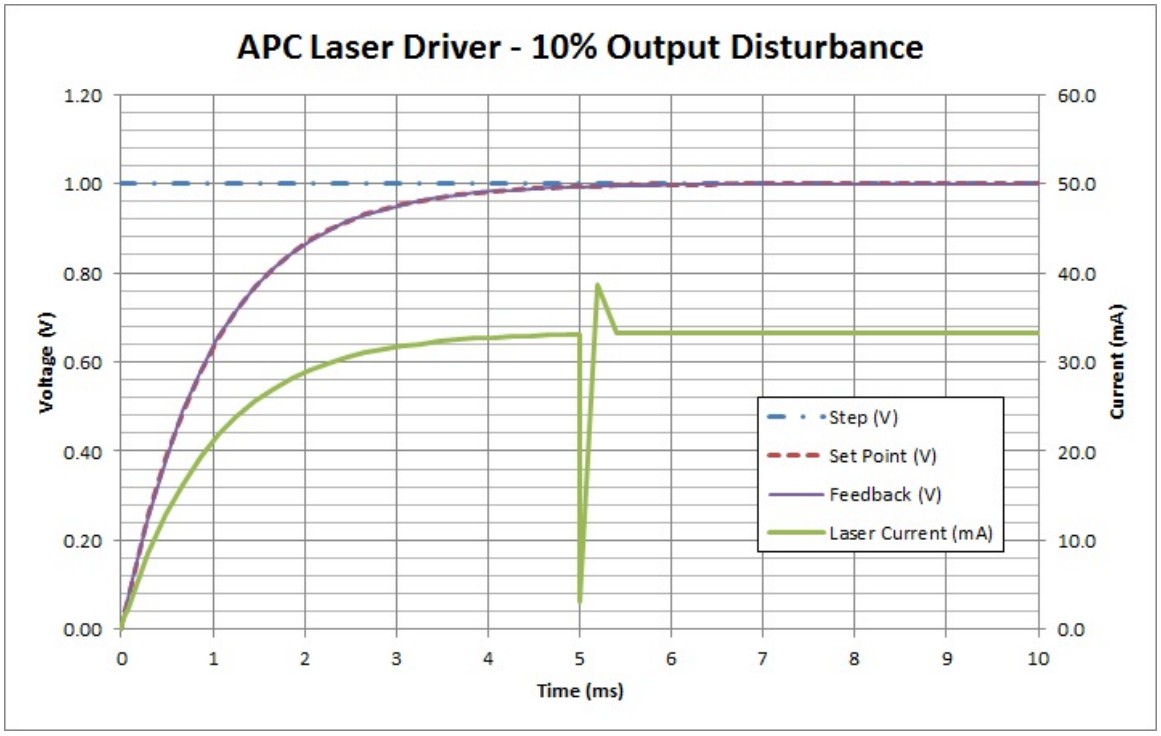

Figure 39: Simulink response to output disturbance on APC laser driver system.

When a disturbance of 10% is seen on the set point an overshoot of 36% and undershoot to ground is observed before the system output recovers to the new set point caused by disturbance.

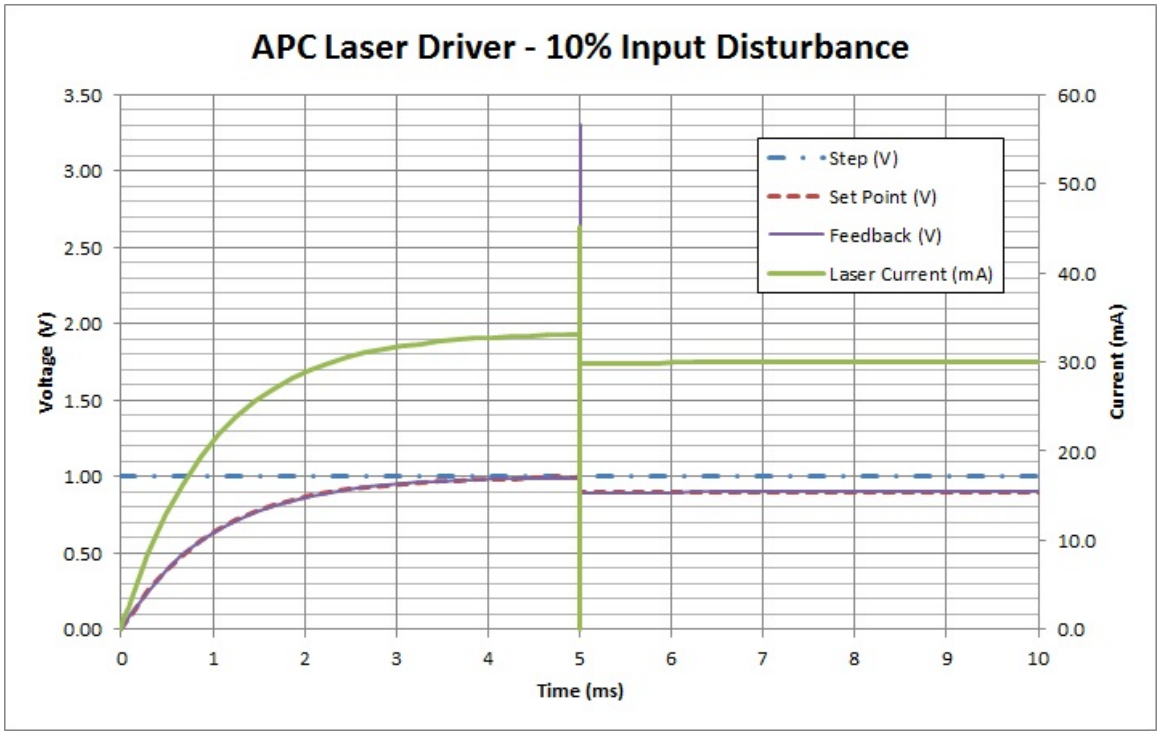

Figure 40: Simulink response to input disturbance on APC laser driver system.

7.6 Laplace Domain Conclusion

The individual building blocks of the system have proven to be stable in both simulation of the transfer function in the Laplace Domain as well as electrical SPICE simulations. The entire APC laser driver is a stable system that a control system can be integrated into.

8 Analog Control System

This chapter will step through the reasoning used to choose a type of control system as well as the design and simulation of the control system.

8.1 Choosing A Control System

There are a lot of choices for control systems that have excellent performance. This section will briefly go over the different control methods considered and the control system chosen to go forward with in the design

8.1.1 Optimal Controls

The performance of optimal controls is far superior to tunable systems, however with that performance comes a price. In an analog system that is designed to drive a plethora of laser diodes, the ability to perfectly model the feedback system and the plant model becomes nearly impossible. The optimal control systems need a reliable system model in order to have the expected performance improvement over other control methods. Since this particular design is completely analog, the complexity of the system is increased and room for error is drastically reduced. A completely analog optimal control system is a huge risk when a high pressure compressed schedule is present. For this project there is not room for multiple board spins and many months of testing and tweaking. A LQR or H-Inifinity controller would be ideal, however it is not practical for this application.

8.1.2 Non-Optimal Controls

A non-optimal tunable control system is more realistic for this design. These types of systems don't use state variables to perfectly calculate the next set-point to produce an exact output. Instead they react to the output and do their best to reduce the error as quickly as possible. The ability to tune

each system on a unit to unit basis could be very beneficial for system performance over a wide range of diode sources. A tuneable control system would be best for this application

8.1.3 Lead, Lag, and Lead-Lag Compensators

The design goals dictate that zero steady-state is an important parameter. That being said a lead compensator by itself it out. The lag compensator can provide minimal steady-state error. Equation 54 shows that an equal number of poles and zeros are introduced into the system. This will provide stability to the system and minimal steady-state error at the expense of response time. The settling time design goal is defined as 500us, which would be difficult to hit with the lag compensator.

$$C(s) = \frac{s+z}{s+p} \rightarrow p < z \tag{53}$$

A lead-lag compensator could provide benefits and split the difference between the performance of the individual lead and lag compensators. The overshoot and settling time performance will increase when comparing to the lead compensator, but the stead-state error will increase [1]. Theoretically, the lead-lag compensator will be able to meet all of the design goals. The analog implementation of the lead-lag controller can be easily implemented by cascading a lead and lag controller. The performance of the lead-lag compensator is highly dependent on the plant model. The plant model will be consistent for the same diode, but if a new diode is introduced the performance will suffer.

$$C(s) = K_p \frac{(s+z_1)(s+z_2)}{(s+p_1)(s+p_2)} \tag{54}$$

8.1.4 PI, PD, and PID Controllers

Just like the lead compensator, the overall design goals dictate that zero steady-state is an important parameter, so the PD controller is not an intelligent design choice. The PI controller will be sufficient in eliminating steady state error, however the quicker the response the better. The PID will have a very fast response, zero steady-state error, and have stable electrical performance.

8.2 System Implementation of the Analog PID Controller

8.2.1 Theoretical PID Tuning

The first step is to tune the system theoretically. Although this method includes quite a bit of math and a few hours of number crunching, it will get the system close to the desired performance criteria and manual tuning will be much less painful later on.

First step is to linearize the Simulink model. Luckily, Matlab can do this for us using the Simulink model that was derived earlier and a little scripting.

```
%%% control system modeled in simulink, %%%
%%% use that model to linearize the system %%%
%open the model
mdl = 'APC_Block';
open_system(mdl)
%specify linearization input
io(1) = linio('APC_Block/Set Point Ckt',1,'input');
%specify linearization closed loop output
io(2) = linio('APC_Block/Laser Driver Ckt',1,'output');
%linearize the model using specified IO
linsys = linearize(mdl,io)
%Convert Linearized System Back to Transfer Function
[NUM,DEN] = ss2tf(linsys.A,linsys.B,linsys.C,linsys.D)
sys = tf([NUM],[DEN])
```

The linearized system now becomes the following.

$$G_P(s) = \frac{94.95s + 2.28e14}{s + 2.355e12} \tag{55}$$

The target system performance is a third order ITAE system.

$$s^3 + 1.75\omega_n s^2 + 3.25\omega_n^2 s + \omega_n^3 \tag{56}$$

Using Mason's gain formula on the control system (Gp = linearized system, Gc = PID) [1]:

$$G_{sys}(s) = \frac{G_P G_C}{1 + G_P G_C} \tag{57}$$

The PID controller introduced to the system will take the following form [1]:

$$G_C = \frac{K_D s^2 + K_P s + K_I}{s} \tag{58}$$

For simplification of the calculations the coefficients from the plant model will be referred to as a, b, and c.

- $a = 94.98$
- $b = 2.28e14$
- $c = 2.355e12$

Plug the plant model and control system into equation 58 to get the following:

$$G_{sys}(s) = \frac{\frac{K_D s^2 + K_P s + K_I}{s} \frac{as+b}{s+c}}{1 + \frac{K_D s^2 + K_P s + K_I}{s} \frac{as+b}{s+c}} \tag{59}$$

$$G_{sys}(s) = \frac{(K_D s^2 + K_P s + K_I)(as + b)}{s(s + c) + (K_D s^2 + K_P s + K_I)(as + b)} \tag{60}$$

$$G_{sys}(s) = \frac{1}{\frac{s^2 + sc}{(K_D s^2 + K_P s + K_I)(as+b)} + 1} \tag{61}$$

$$G_{sys}(s) = \frac{(K_D s^2 + K_P s + K_I)(as + b)}{(s^2 + sc) + (K_D s^2 + K_P s + K_I)(as + b)} \tag{62}$$

$$G_{sys}(s) = \frac{(K_D s^2 + K_P s + K_I)(as + b)}{s^2 + sc + aK_D s^3 + aK_P s^2 + aK_I s + bK_D s^2 + bK_P s + bK_I} \tag{63}$$

$$G_{sys}(s) = \frac{(K_D s^2 + K_P s + K_I)(as + b)}{s^3 + (\frac{1+aK_P+bK_D}{aK_D})s^2 + (\frac{c+aK_I+bK_P}{aK_D})s + \frac{bK_I}{aK_D}} \tag{64}$$

The system equation has been manipulated enough to solve for Kp, Ki, and Kd.

$$T_S = 1e-3 = \frac{4}{\zeta\omega_n} \tag{65}$$

For and ITAE system the damping factor should be around 0.5.

$$\omega_n = \frac{4}{(0.5)(0.001)} = 8000 \tag{66}$$

Looking at equation 65, it seems like it would be most beneficial to solve the control coefficients in terms of Kd.

Solving for the s^2 term.

$$1.75\omega_n = \frac{1 + aK_P + bK_D}{aK_D} \tag{67}$$

$$K_D = \frac{aK_P + 1}{1.75a\omega_n - b} \tag{68}$$

Solving for the s term.

$$3.25\omega_n^2 = \frac{c + aK_I + bK_P}{aK_D} \tag{69}$$

$$(3.25\omega_n^2)(aK_D) - c - aK_I = K_P = \frac{1.75\omega_n a - b)K_D - 1}{a} \tag{70}$$

$$(3.25a\omega_n^2)(^2aK_D) - ac - a^2K_I + 1 = 1.75\omega_n a - b)K_D \tag{71}$$

$$1 - ac - a^2K_I + 1 = 1.75\omega_n a - b - 3.25a\omega_n^2)K_D \tag{72}$$

$$K_I = \frac{1.75\omega_n a - b - 3.25a\omega_n^2)K_D + ac - 1}{a^2} \tag{73}$$

Solving for the last term.

$$\frac{a\omega_n^3}{b} = \frac{(1.75\omega_n a - b)[-K_D(1.75a\omega_n - b - 3.25a^2\omega_n) + ac - 1]}{a^3K_D + a} \tag{74}$$

$$\frac{a\omega_n^3}{b}(a^3K_D + a) = (1.75\omega_n a - b)[-K_D(1.75a\omega_n - b - 3.25a^2\omega_n) + ac - 1] \tag{75}$$

$$K_D[\frac{a^4\omega_n^3}{b} + (1.75\omega_n a - b - 3.25a^2\omega_n)(1.75\omega_n a - b)] = (ac-1)(1.75\omega_n a - b) - \frac{a^2\omega_n^3}{b} \quad (76)$$

Plug in the values for ω_n, a, b, and c to get the following PID constants:

- $K_P = 0.0235$
- $K_I = 247$
- $K_D = 1e-10$

The PID values calculated seem like they are in the ballpark of what should be expected. The derivative term should be very low because the system and amplifier bandwidth is already very fast. The gain is handled with the negative feedback from the photodiode, so the proportional term should be low but still able to compensate for the non-ideal voltage follower on the laser driver circuit. The integral term should be relatively high when compared to the other constants because the system needs to correct steady-state errors in a rapid fashion.

Taking a look at the output from the Simulink simulation, the step input is clean and meets specifications, the output disturbance meets specifications, but it looks like there is room for improvement on the input disturbance.

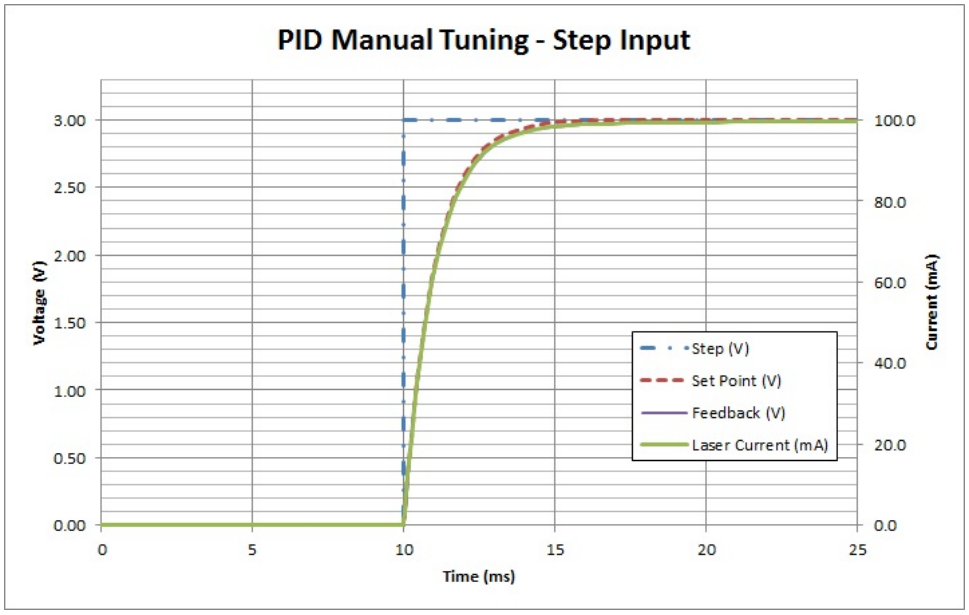

Figure 41: Simulink response to step input of APC PID for third order hand calculated ITAE system.

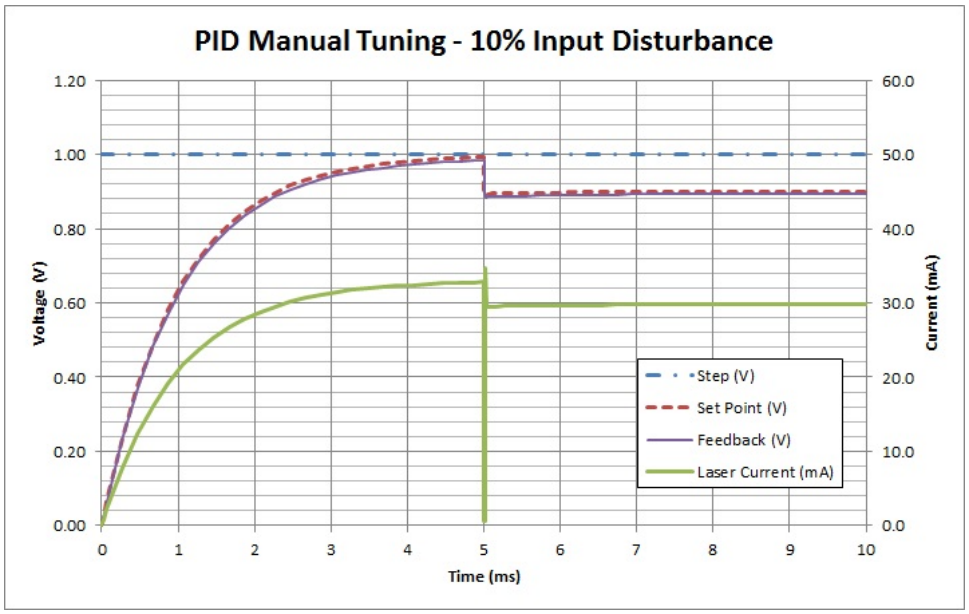

Figure 42: Simulink response to input disturbance of third order hand calculated ITAE system.

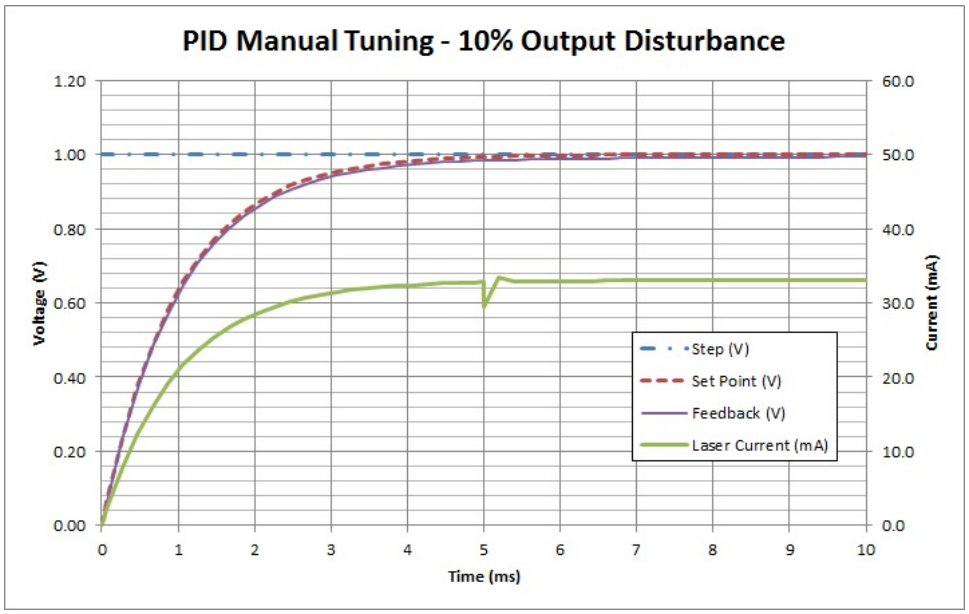

Figure 43: Simulink response to output disturbance of third order hand calculated ITAE system.

8.2.2 Simulink Auto Tuning PID Tools

Click on the PID block in the system below to get started using the Simulink auto PID tuner. An options window should appear along with a tune button.

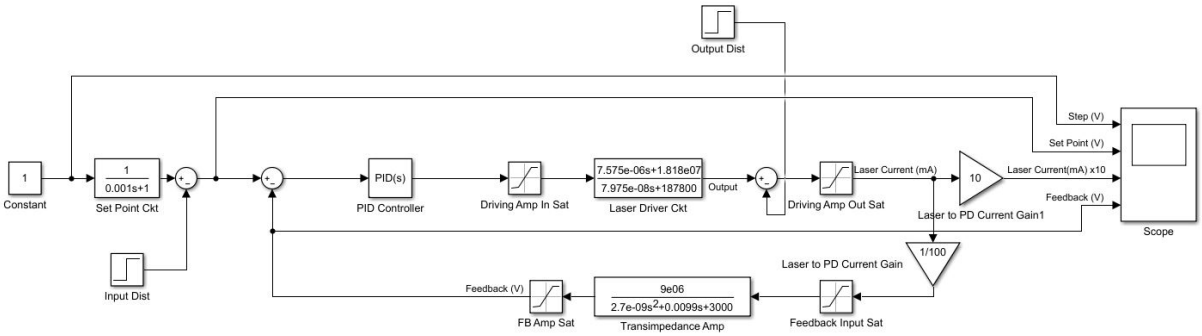

Figure 44: Continuous PID controller integrated into previous APC model.

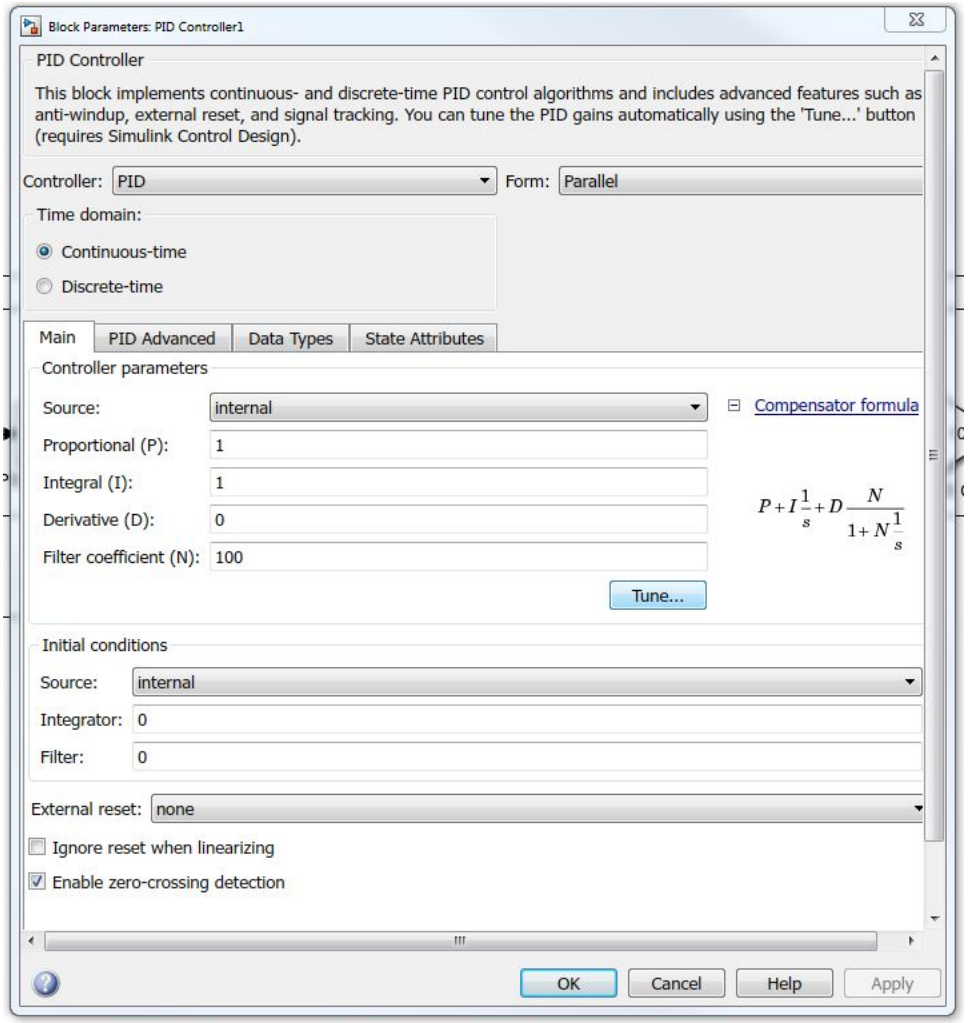

Figure 45: Simulink PID block auto-tuning menu.

By clicking tune the below window becomes visible and the option to tune the PID is available. System robustness was maximized sacrificing settling time. The settling time goal is more relaxed than the steady-state and overshoot goals.

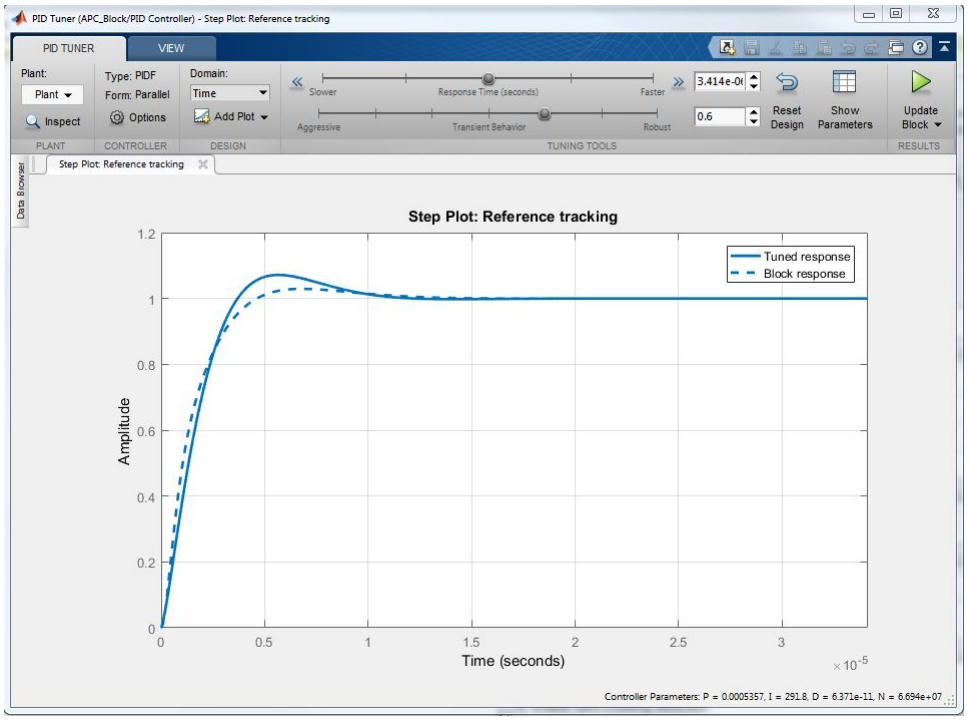

Figure 46: Simulink auto-tune step response menu used to trade off robustness for speed.

8.2.3 Simulink PID Response

In chapter 7 the system without feedback control was taken and a disturbance of 10% was injected onto the output and the input. This step will be repeated with the control loop in the system for the purpose of directly comparing the performance.

The figure below displays the systems response to a step input from 0 to 1. The system gracefully turns on in approximately 5ms, and there is no overshoot on the startup.

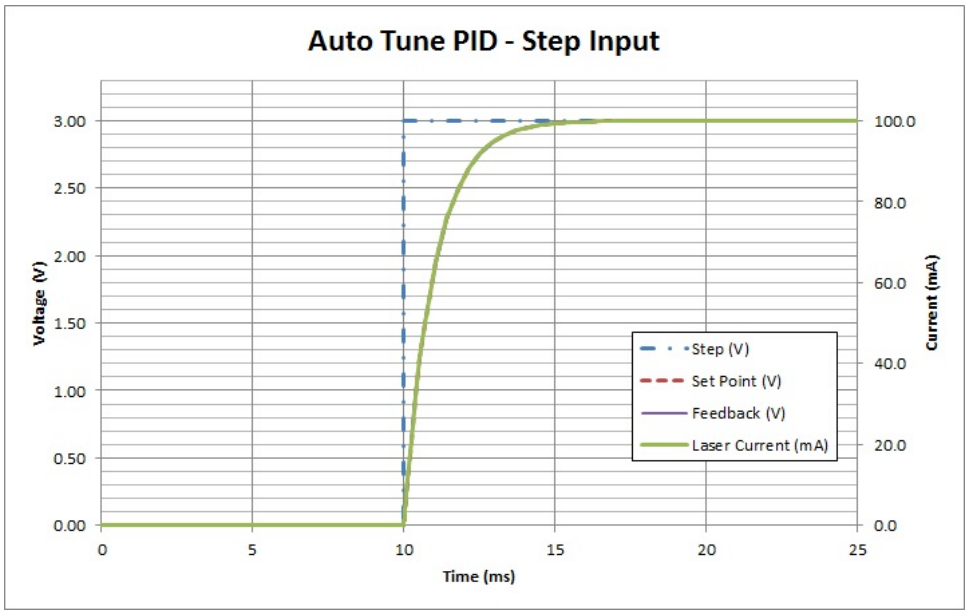

Figure 47: Simulink model response to step-up input with auto-tuned PID.

The figure below displays the system responding to a step input from 1 to 0. The shutdown has no overshoot and it gracefully decays to 0 in about 5ms.

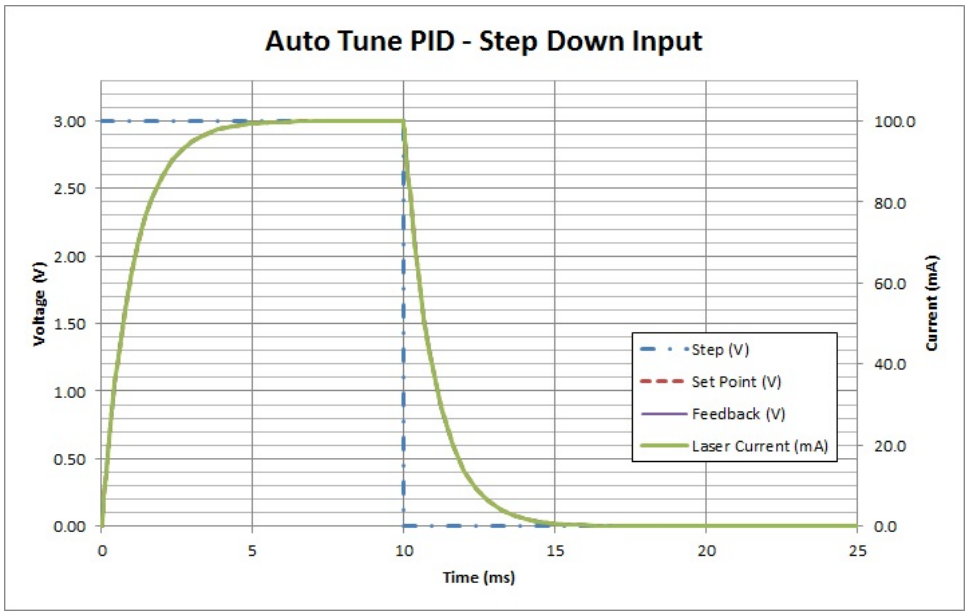

Figure 48: Simulink model response to step-down input with auto-tuned PID.

The next figure pictured shows the systems response to a disturbance on the input after the set point amplifier. This is not a real situation and the following figure is just to display the robustness

of the control system. There is approximately a 24% undershoot shown in the system.

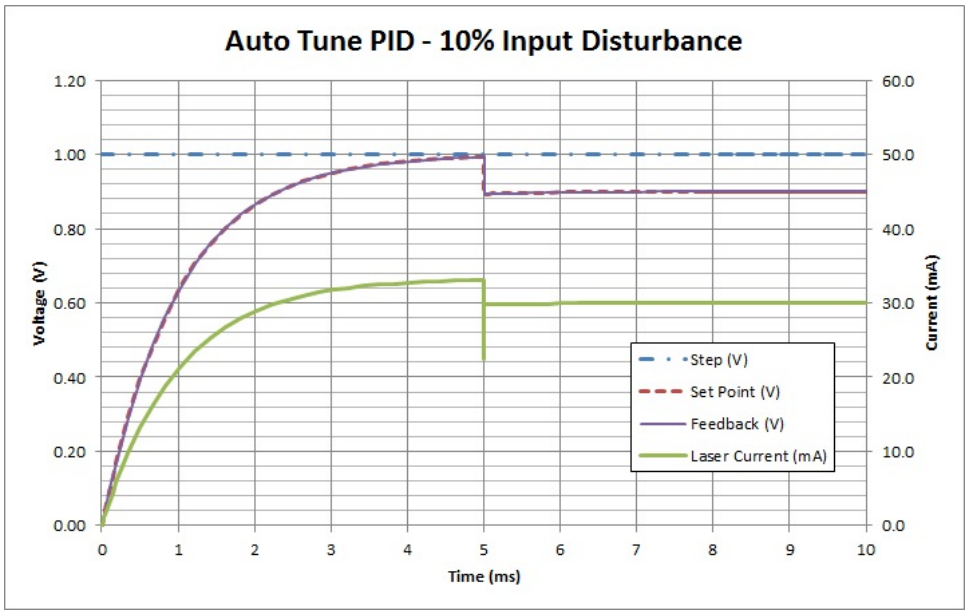

Figure 49: Simulink model response to input disturbance with auto-tuned PID.

The last simulation ran using the Simulink model is the output disturbance. This is a very likely case in the actual system and this response is important to overall system performance. The design goals dictate that 10% overshoot is acceptable for the system. An overshoot of 9% is observed and meeting the design goals.

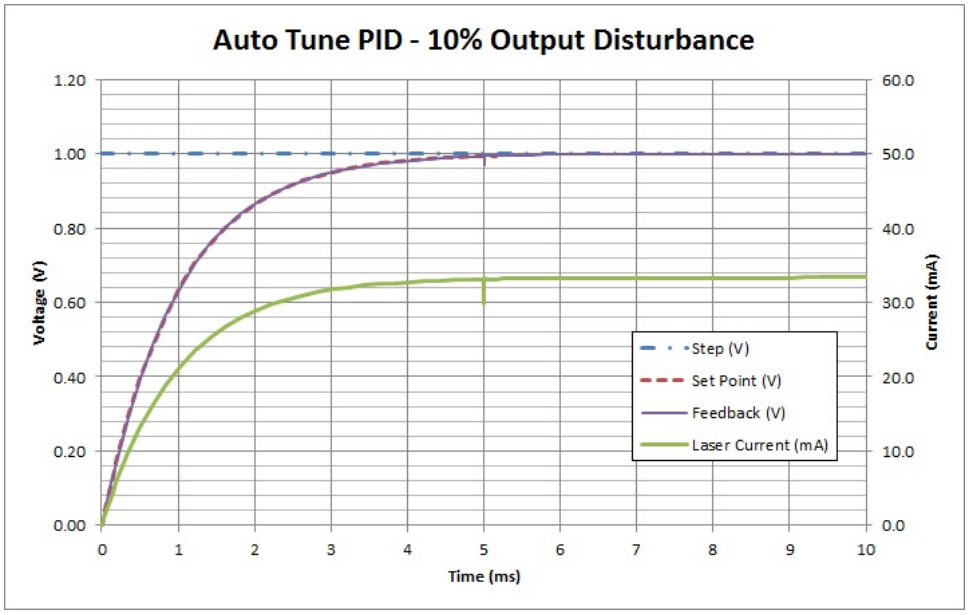

Figure 50: Simulink model response to output disturbance with auto-tuned PID.

9 Practical Implementation of Analog PID Controller

Matlab and Simulink are nice tools for theoretical simulation and calculation and give us a good starting point for designing the electronics. The Kp, Ki, and Kd terms derived from the PID tuner in Simulink can be used for the physical electronics. This section will go over the behavior of analog electronics and the techniques that can be used to mitigate potential problems. Some things to watch out for include:

- Derivative Overrun
- Integral Windup
- Saturation

9.1 Derivative Overrun

The parallel implementation of the PID, as opposed to cascaded, presents a practical problem that needs to be addressed. Changes in the set point causes a step in the error, and since the derivative responds to the rate of change; Saturation and large overshoot along with long recovery times [2] will be observed. The bandwidth of the amplifiers only apply to non-saturated conditions, and since it typically takes a few milliseconds to break an op-amp out of saturation, unwanted behaviors such as ringing, overshoot, and long settling times may be observed.

An easy way to overcome this situation is to have the derivative term operate on the feedback (present value) instead of the error. What is left is a PI controller on taking care of the steady-state error and the derivative speeding up the response time which can be observed in figure 51.

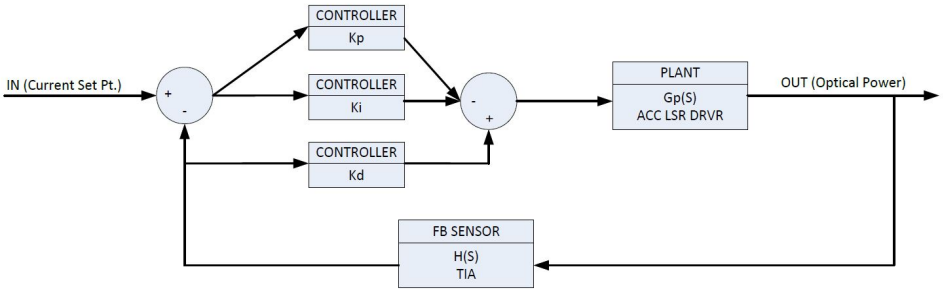

Figure 51: Block diagram of approach used to avoid derivative overrun.

9.2 Integral Windup

The integral controller will continue to build its output until there is zero error. Tunable compensators and controllers work by eliminating an error term, so the majority of the time there is some sort of error present. As long as there is an error the integrator output will continue to build until saturation. Once a non-zero error is seen when the integral is in saturation it will have to reverse polarity to discharge then quickly charge back up [2]. The response out of saturation is slow, so the integral windup will cause overshoot and ringing.

There isn't really an elegant work around for this. All that is required is a clever designed to keep the integral amplifier out of saturation. One way to do this is to feed the output of the summing amplifier into a comparator which controls a switch that can stop the integrator. Briefly stopping the integrator is a trade-off to saturation.

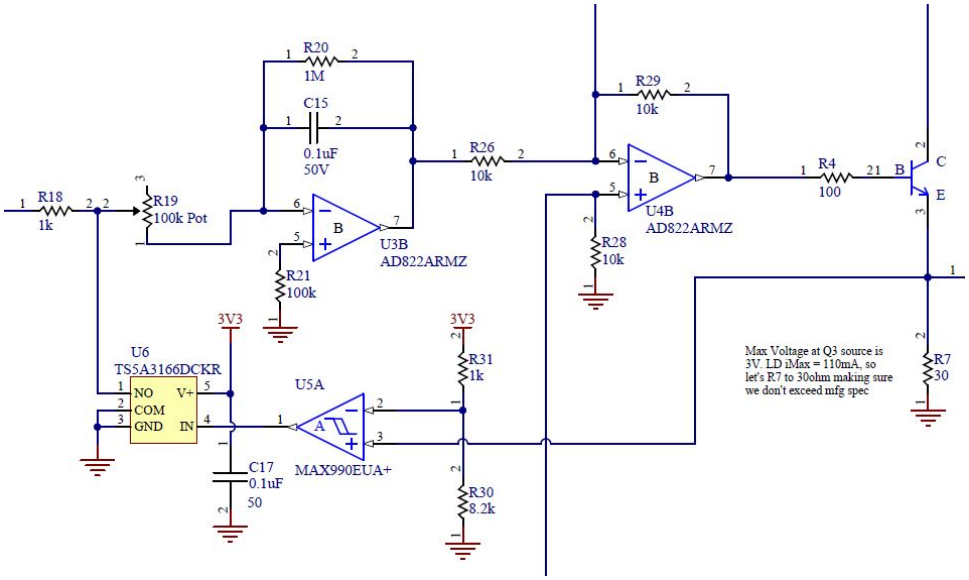

Figure 52: Schematic to display approach used to avoid integral windup.

9.3 Saturation

The feedback capacitor on the integral amplifier can cause the amplifier to saturate because the input bias current of the op-amp will slowly charge/discharge the capacitor causing the output to runaway. This problem would be tough to troubleshoot because it would seem as though it happened intermittently. A bleed resistor put in parallel with the capacitor can save a lot of head scratching later on. The resistor R20 in Figure 52 above will accomplish this.

10 PCB Design and Fabrication

This chapter will share the final schematic design and any relevant notes or calculations, the PCB design, the BOM, and general explanations of the the process to fabricate and assembly the printed circuit board.

10.1 Schematics

The laser driver is composed of three schematic sheets in a hierarchical design.

10.1.1 Top Level

The purpose of the 'Top Level' schematic sheet is to make physical connections of ports at a higher level. The green boxes represent each schematic sheet under the top level.

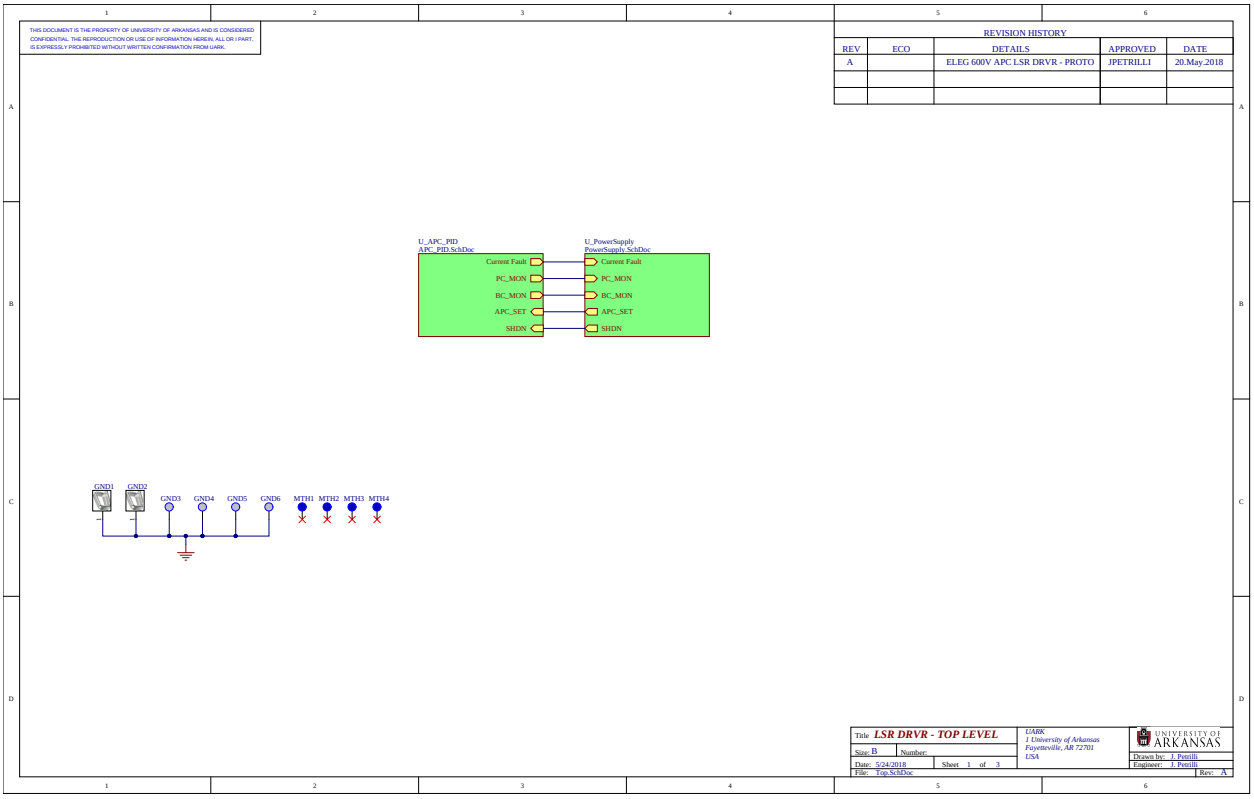

Figure 53: Top level hierarchical schematic for PCB design.

10.1.1.1 Mounting Holes

The blue circles with the reference designator MTH represent the PCB's physical mounting holes. It is cheaper to specify the mounting holes as a thru-hole pad in the schematic sheet as opposed to a cutout in the board outline. If the holes are designed into the board outline the PCB tool will typically call out a router to make the cutout, instead of a drill hole, which will increase cost.

For this design the preference for the mounting holes is to be completely isolated from all return paths. The testing may occur on a stainless steel optical bench which could potentially introduce a ground loop if the mounting was not isolated.

10.1.1.2 Ground Test Points

Multiple ground test points will be scattered through the PCB. This will prove to be convenient for possible rework situations as well as general testing.

10.1.2 Power Supplies

For the convience of the end user a single voltage input of 5V is required for operation. All necessary voltage rails are generated from that single input supply.

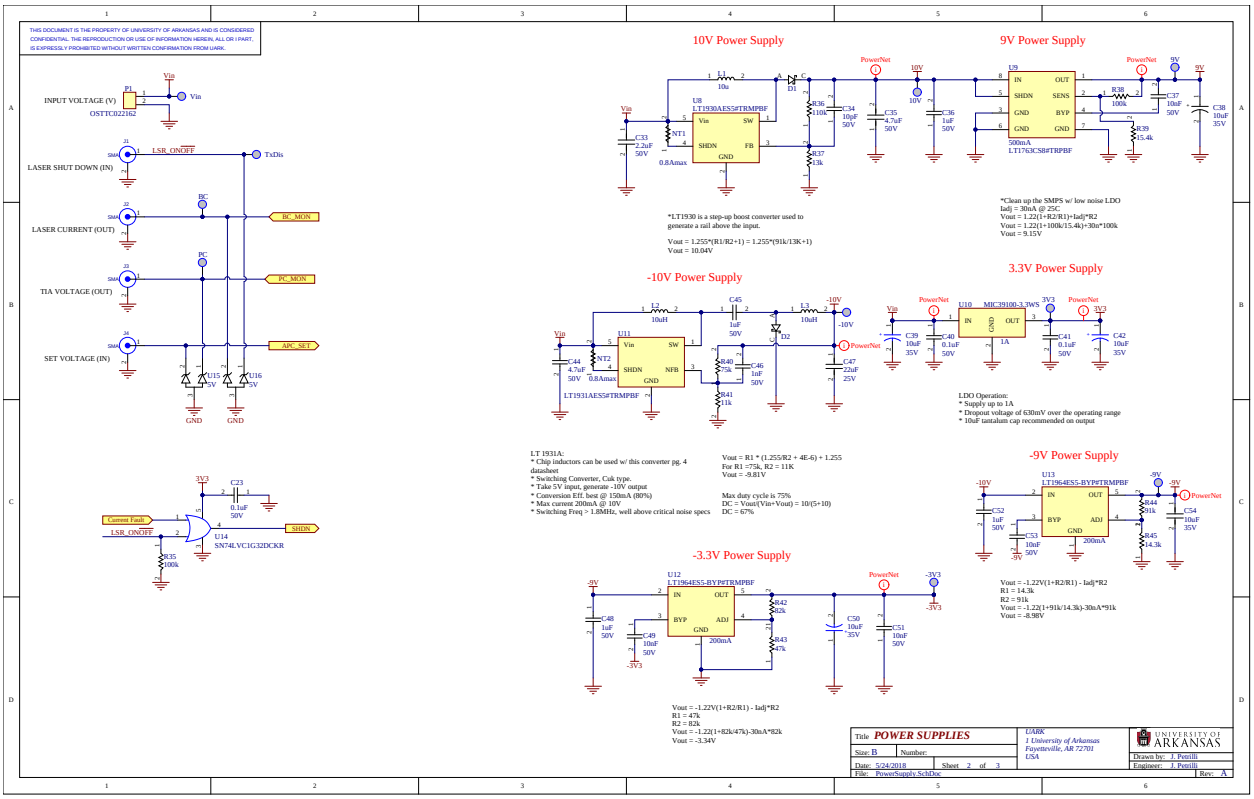

Figure 54: Schematic to generate power supplies for driving and controller laser.

10.1.2.1 12V Power Supply

The 12V power supply is generated using a boost converter. This power supply could potentially pull around 300mA, so the part chosen is the LT1930 which can source up to 1A of current. The output voltage equation is taken from the data sheet and can be seen in equation 78.

$$V_{out} = 1.255(1 + \frac{R_{37}}{R_{36}}) \tag{77}$$

$$V_{out} = 1.255(1 + \frac{110k}{13k}) = 11.87V \tag{78}$$

10.1.2.2 9V Power Supply

The output of the 12V Supply is used as the input to the 9V supply. Switching mode power supplies have a significant amount of ripple on the output, so the LT1763 low dropout (LDO) linear regulator is used to clean up the noise. The ripple rejection for this IC is 50dB or better which theoretically meets the specifications. This power supply will be the positive rail for the op-amps in the control system as well as the optional laser supply. The output voltage is calculated from the data sheet and can be seen in equation 80.

$$V_{out} = 1.22(1 + \frac{R_{38}}{R_{39}}) + I_{adj}R_{38} \tag{79}$$

$$V_{out} = 1.22(1 + \frac{100k}{15k}) + (30n)(100k) = 9.15V \tag{80}$$

10.1.2.3 -10V Power Supply

The switching converter chosen is the LT1931A with Cuk topology. The output voltage can be calculated from equation 82.

$$V_{out} = R_{40}(\frac{1.255}{R_{41}} + 4e - 06) + 1.255 \tag{81}$$

$$V_{out} = 75k(\frac{1.255}{11k} + 4e - 06) + 1.255 = -9.81V \tag{82}$$

10.1.2.4 -9V Power Supply

The -9V supply is generated from the -10V supply using a low noise LDO by Linear Technology, LT1964. The output voltage can be calculated using the equation found in 84.

$$V_{out} = -1.22(1 + \frac{R_{44}}{R_{45}}) - I_{adj}R_{44} \tag{83}$$

$$V_{out} = -1.22(1 + \frac{91k}{14.3}) - (30n)(91k) = -8.98V \tag{84}$$

10.1.2.5 3.3V Power Supply

The 3.3V power rail is generated from the 5V input signal using a standard linear LDO. This rail is used to bias the operational amplifiers used in the feedback circuit as well as the rail for the digital signals.

10.1.2.6 -3.3V Power Supply

The -3.3V rail is generated from the -9V rail using the same LDO, LT1964. The efficiency of this circuit will be 35% which would typically be a deal breaker however the rail will only bias 2 amplifiers and source a small amount of current.

10.1.2.7 OR Gate

The OR gate controls the p-channel MOSFET controlling the laser bias voltage. The laser can be disabled from user input or from a current fault.

10.1.3 APC Laser Driver

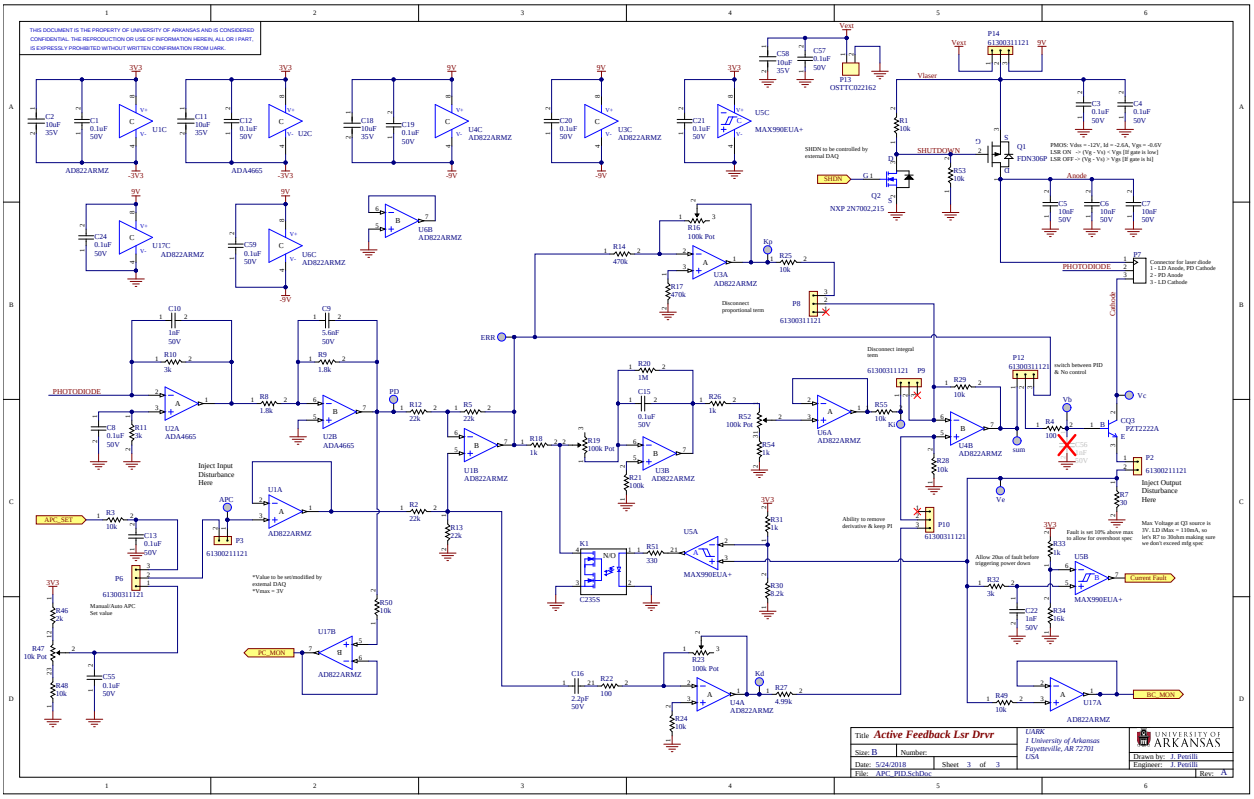

Figure 55: Schematic for APC laser driver with a parallel PID control system.

10.1.3.1 APC SET Port

The input goes through a low pass filter that is fed into a voltage follower and eventually meets up with the feedback signal at the error amplifier U1B. The user may choose to control this input externally or internally with a potentiometer.

10.1.3.2 Transimpedance Amplifier

The TIA takes the current from the photodiodes and converts it to voltage to be used as feedback. The TIA is comprised of U2A and U2B amplifiers and meets the set-point at the error amplifier.

10.1.3.3 PID

The proportional term created from U3A and it can be connected or disconnected for the purpose of tuning and testing. The integral term is U3B. A bleed resistor, R20, was put in the feedback of the integral term, so in order to compensate for it U6A was incorporated to remove the added gain. Also K1 is operating on feedback from the drive current which will shut down the integral term before saturation is reached. The derivative term is operating on the feedback and can be observed at U4.

10.1.3.4 Summing Amplifier

The summing amplifier, U4B, controls the driving transistor and is the output from the control system. This amplifier may be disconnected from the driving transistor for testing purposes.

10.1.3.5 Current Fault Port

The current fault port allows a current spike for approximately 20us before it shuts the laser bias voltage off.

10.1.3.6 BC/PC Monitor

Voltage followers, U17A and U17B, which output to connectors to be monitored for testing purposes. BC is the laser bias current and PC is the photodiode current.

10.1.3.7 SHDN Port

This port controls the laser bias voltage and can shut it down by turning off the p-channel MOSFET Q1.

10.2 PCB Layout

This section will go over the design choices made during the PCB layout phase.

10.2.1 Design Rules

This design is self funded, so cost is a major factor. Assembly costs can triple the price and time of a turnkey quote. For this reason, the PCB will be assembled by hand. There are many companies that fabricate cost effective PCBs. After price matching, the board was sent to fabrication at OSH Park.

- Minimum finished drill size is 10mill
- 2 layer board
- Core material is FR-4
- Apply silkscreen to both sides using white epoxy ink
- Solder mask is purple LPI, both sides
- Minimum trace/clearance is 8/8mil
- Board thickness is 62 mil

10.2.2 Top and Bottom Pour

A copper ground pour was put on the top and bottom of the PCB. Vias were used to stitch the top pour to the bottom pour for the purpose of eliminating EMI and creating a make shift Faraday cage since this PCB is 2 layer instead of 4 due to cost reasons.

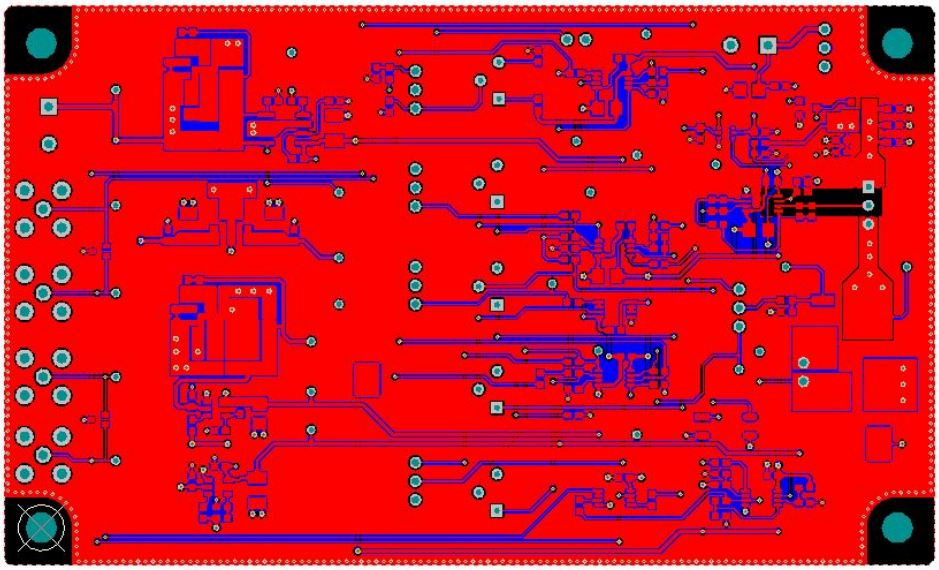

Figure 56: Printed circuit board copper pour on top layer.

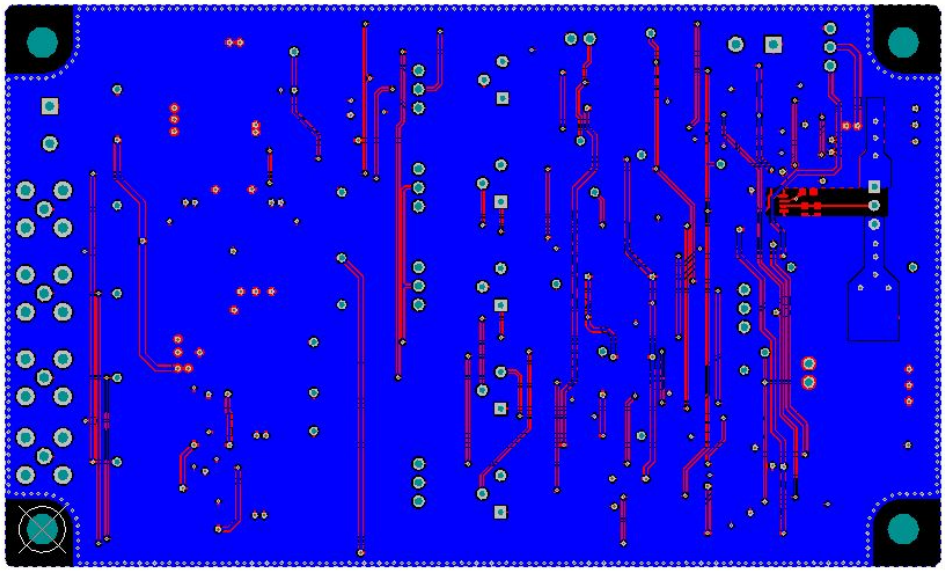

Figure 57: Printed circuit board copper pour on bottom layer.

10.2.3 Power Supplies

The data sheets of the switching mode and linear regulators have suggested layout patterns to achieve optimal performance. The suggestions were taken into consideration during the layout.

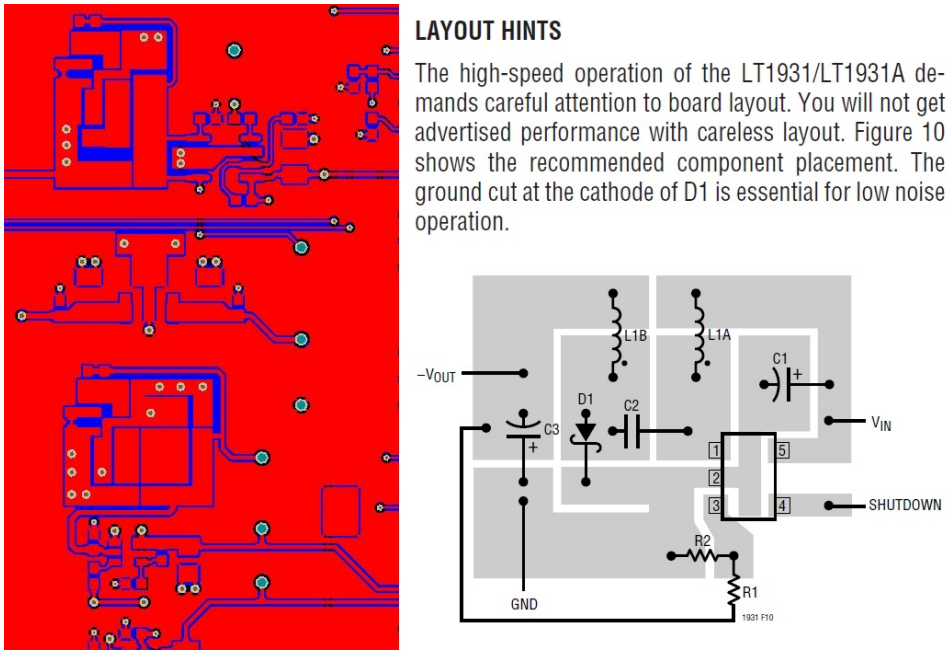

Figure 58: Layout and routing of power supplies to achieve optimal performance.

10.2.4 EMI and Edge Emission Consideration

Ideally the PCB would be 4 layer to reduce noise due to edge radiation and electro-magnetic interference, but for this proof of concept the PCB is 2 layer. Stitching the top ground pour to the bottom ground pour around the perimeter of the PCB with vias creates a make-shift Faraday cage and reduces EMI along with edge emissions [11]. The figure below shows an example of via stitching.

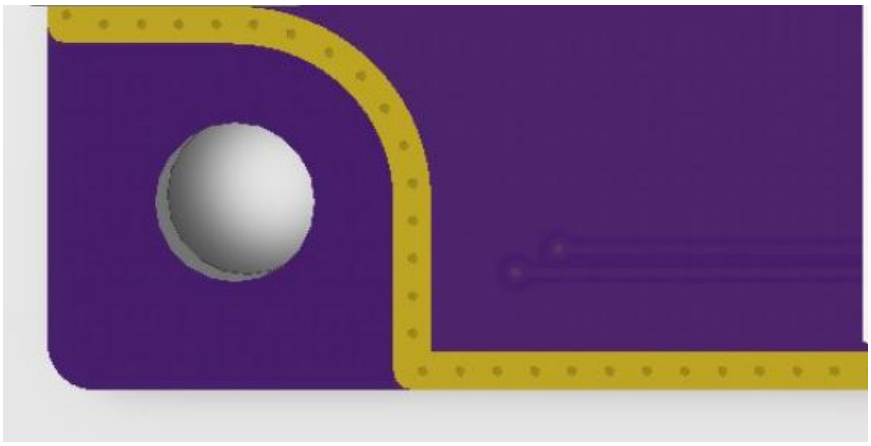

Figure 59: Stitching the perimeter of the PCB with vias to mitigate edge radiation and EMI.

10.2.5 TIA Layout Technique

The trace of the photodiode anode is susceptible to current leakage and cross talk. Pulling back the copper pour from the top and bottom can help prevent unwanted currents from coupling into the trace. Keeping the trace as short as possible is also helpful for signal integrity. Keeping power signals from running in parallel with the trace and keeping all other traces away from the anode is good design practice [12].

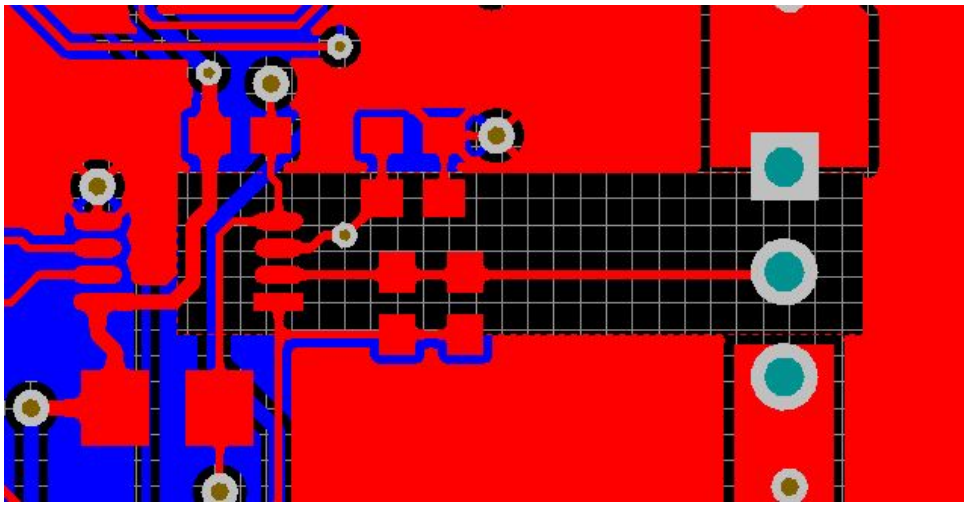

Figure 60: Layout and routing of the TIA to achieve best performance on two-layer PCB.

10.3 Fabrication Files

The fabrication of a PCB requires a few drawings and files. A fabrication drawing will specify out the design rules, the drill table, the layer stack, revision record, and dimensioning. Gerber files are essentially positive or negative photo prints for each layer of the PCB. The drill file is a list of drill sizes and locations of each hole in the PCB.

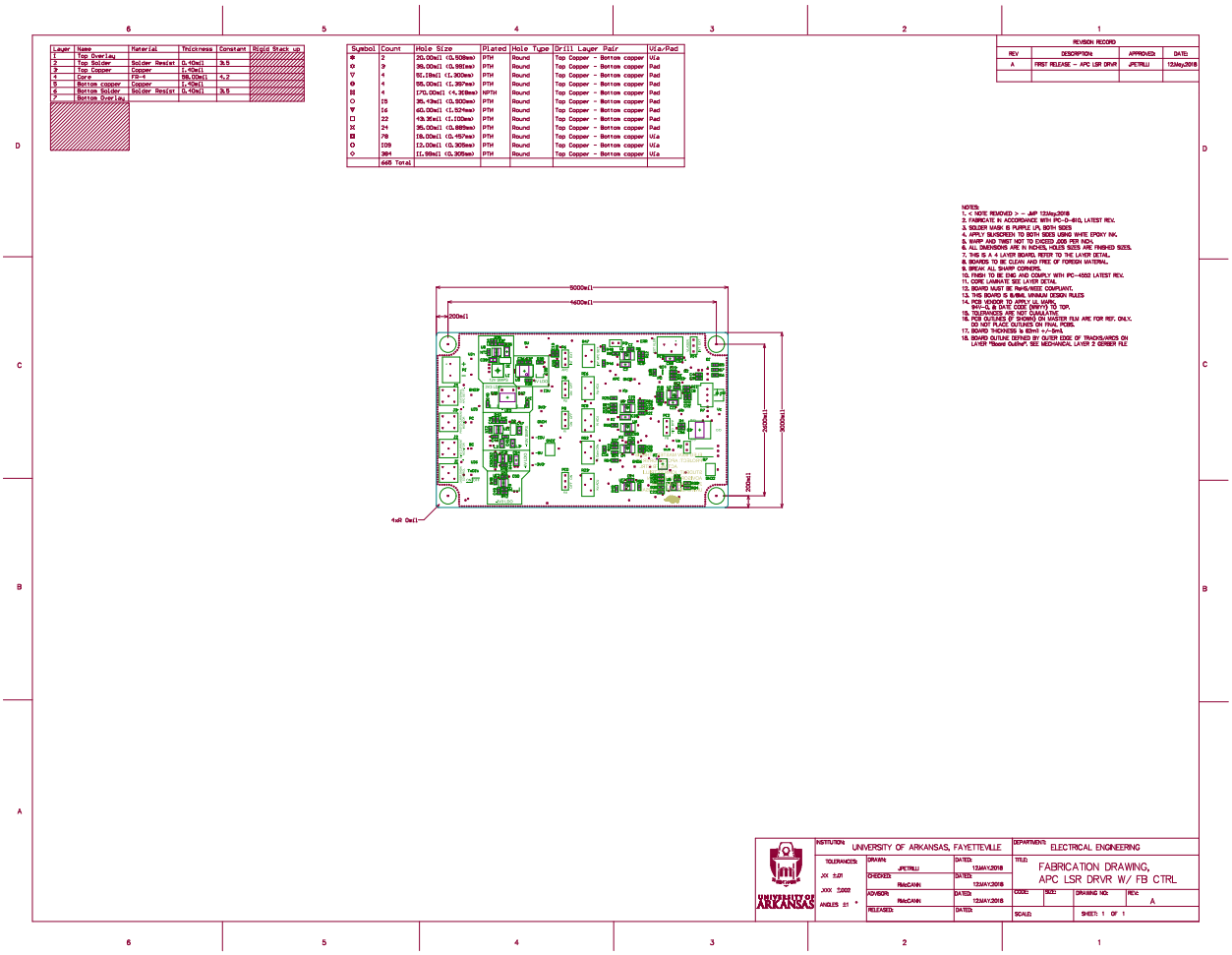

Figure 61: Drawing of the PCB to provide information regarding bare board fabrication.

10.4 Final PCB 3D CAD

The schematic capture and PCB layout tool used was Altium Designer. Altium supports 3D CAD outputs of the PCBs which is convenient for mechanical fit checking, checking footprints and exposed copper, and checking silkscreen.

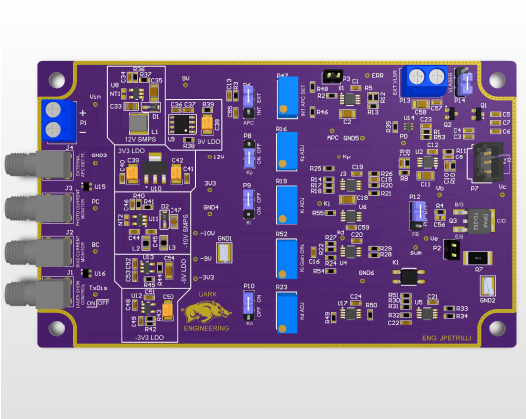

Figure 62: 3D rendered top view of the PCBA using Altium Designer 2017.

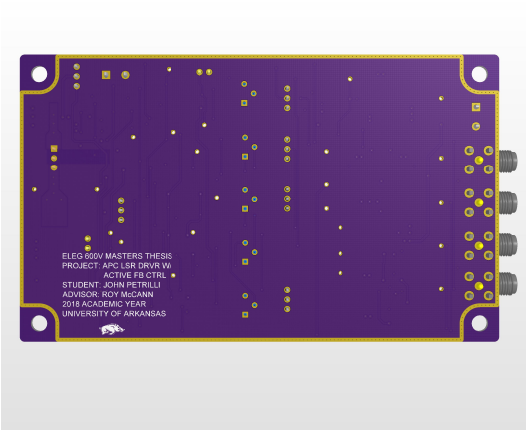

Figure 63: 3D rendered bottom view of the PCBA using Altium Designer 2017.

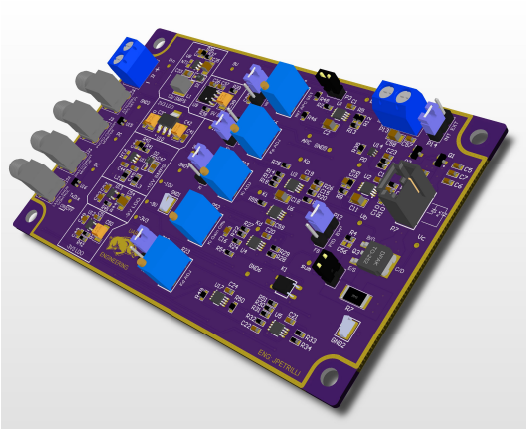

Figure 64: 3D rendered angled view of the PCBA using Altium Designer 2017.

11 PCB Assembly

Professional PCB assembly is a very expensive process. For prototyping electronics, typically a breadboard would be created to confirm functionality. For this project time and cost were a contributing factor, so the confidence to spin the board lied in simulation. Manual assembly of PCB's saves time and money, but workmanship issues can contribute to unexpected behavior of electronics. Proper assembly and cleaning techniques can help mitigate workmanship issues. This chapter will highlight the do-it-yourself assembly process.

11.1 Equipment

Utilizing the proper equipment can save time during this tedious process. The following is a list of equipment and items that will either be necessary or convenient during assembly.

1. Bare Printed Circuit Board
2. Solder Stencil
3. Solder Paste and Solder (Non-Leaded RoHS)
4. Soldering Iron
5. Flux
6. Kimtech Non-Static Wipes
7. Q-tips and Stiff Brissle Brush
8. 99% Isoprophyl Alcohol
9. Ultrasonic Bath
10. Reflow or Environmental Oven
11. Temperature Sensor

12. Masking Tape
13. Clamp
14. Electronic Components from BOM
15. Tweezers

11.2 Prepping the PCB

On an ESD safe surface, tape the PCB down with masking tape.

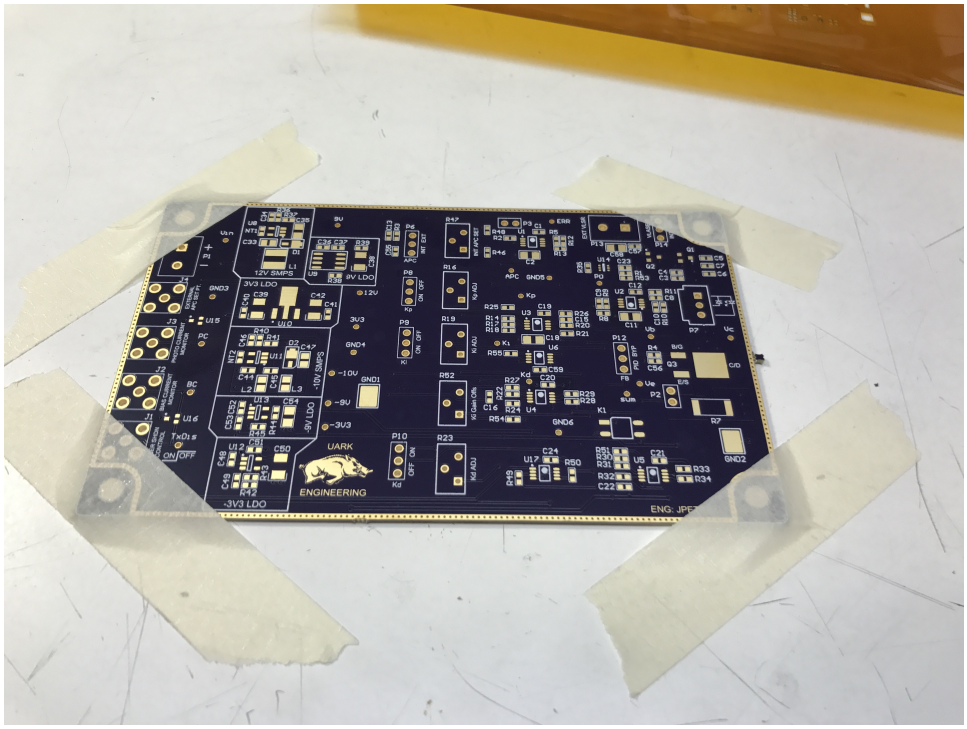

Figure 65: Bare PCB taped to ESD safe surface.

After the PCB is taped down to the ESD safe surface, take time to align and tape the solder stencil over the bare PCB so the openings of the stencil line up with the surface mount pads.

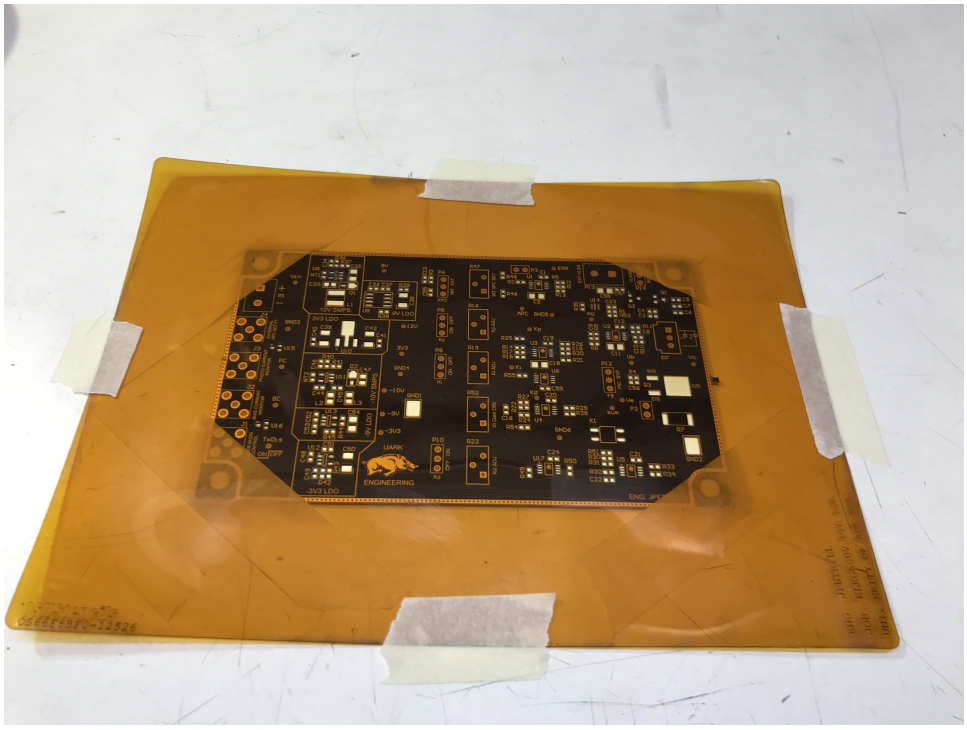

Figure 66: Solder stencil aligned to bare PCB.

11.3 Applying Solder Paste

Once the stencil is aligned and secured down, apply solder paste.

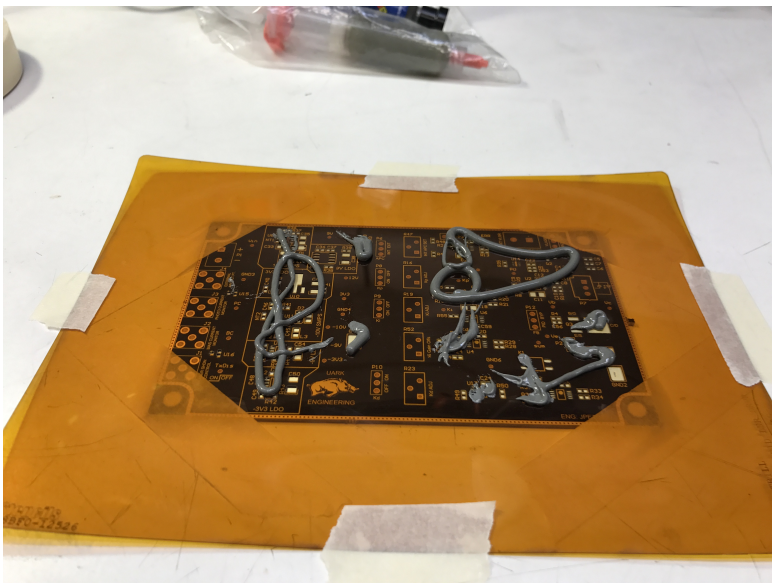

Figure 67: Solder Paste applied to the aligned solder stencil.

Most stencils come with a paste spreader, but if it does not then a credit card will work the same. Spread the solder evenly into the openings on the PCB's surface mount pads.

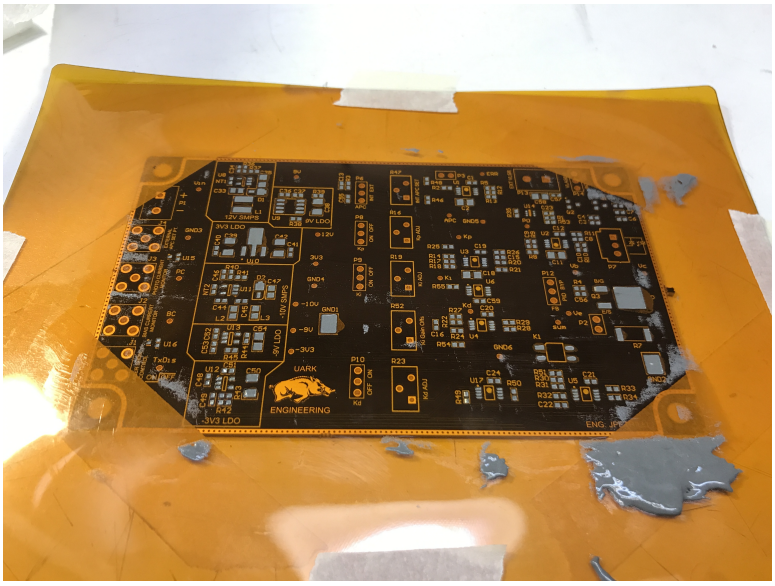

Figure 68: Results from solder paste being spread into stencil openings.

When the solder has been spread, removed the stencil to expose the PCB which is now ready for components.

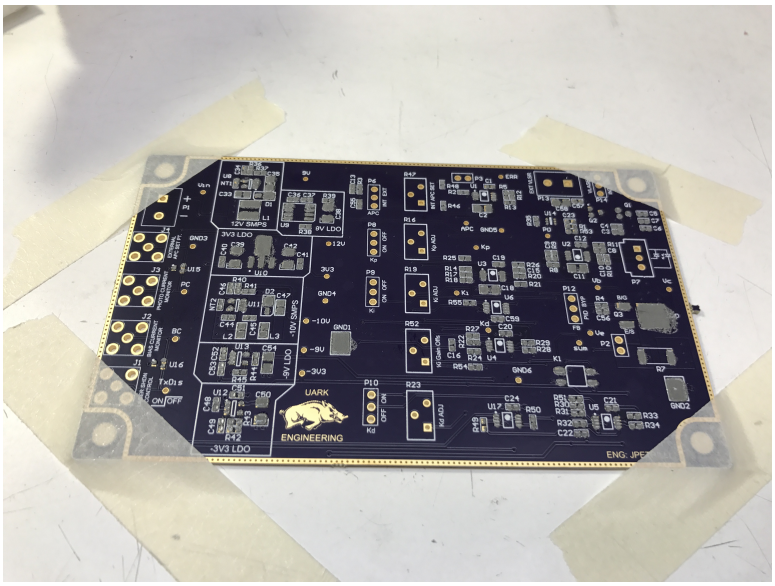

Figure 69: PCB with solder paste on surface mount pads.

11.4 Pick and Place

Now it is time to do manual pick and place. This step is very tedious, but it is the most important part so extreme care must be taken. When placing components onto the footprints the surface tension from the solder paste will hold the components in place.

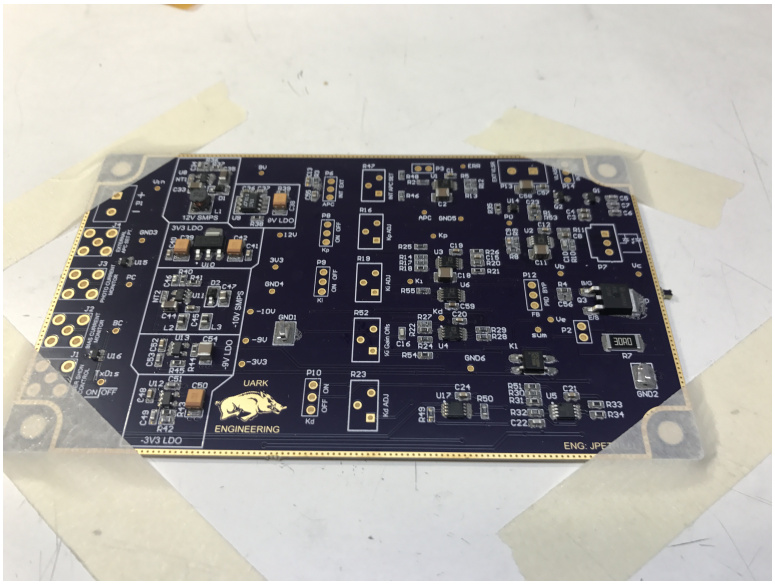

Figure 70: All SMT components have been manually placed on PCB and ready for reflow.

11.5 Reflow

The R&D laboratory does not have a reflow oven, but it does have an environmental chamber, temperature sensor, and heat guns. The goal during this step is to watch and adjust the temperature of the environmental chamber to match the ideal reflow profile.

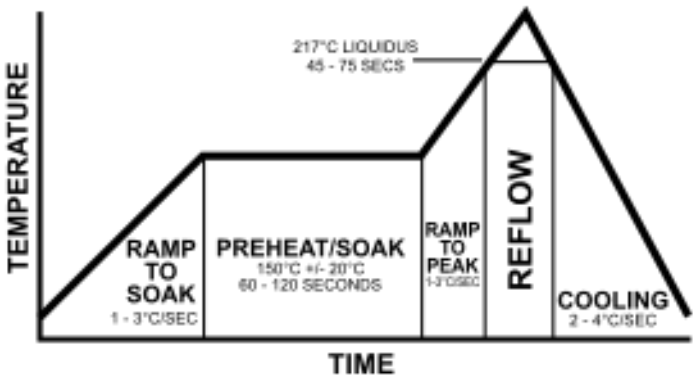

Figure 71: Ideal temperature profile for solder reflow.

Figure 72: Environmental chamber modified to work as reflow oven.

11.6 Finishing the Assembly Process

When the reflow was complete, some joints required touch up with a soldering iron. There was residual flux and dried solder paste on the PCB. The board was put into an isoprophyl ultrasonic

bath for cleaning.

Figure 73: Ultrasonic cleaning of the PCB using 99% isoprophyl alcohol.

The through hole components were soldered onto to the PCB next. The PCB was given another ultrasonic bath after the assembly of the through hole components.

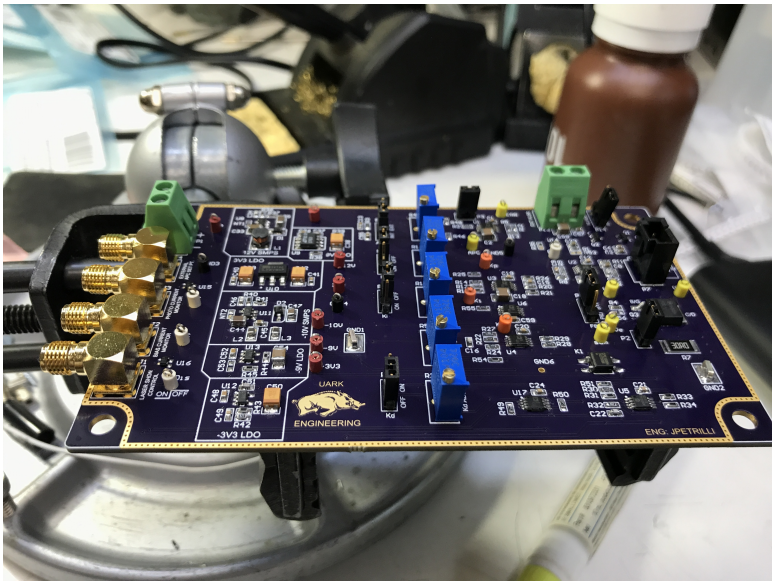

Figure 74: Complete assembled PCBA ready for testing.

12 Testing

Now that there is an assembled board testing can begin. The goal for this chapter is to confirm that the laser driver meets the specs from the data sheet in figure 1.

12.1 Equipment

The following equipment is necessary to accurately test the electronics while driving a laser diode.

1. Oscilloscope and Probes
2. Testing Cables
3. Stand-Offs
4. Manual Linear Stage
5. Integrating Sphere Silicon Detector
6. Thermally Controlled Laser Diode Mount and Linear Stage
7. Digital Multi-Meter (DMM)
8. Source Measure Unit (SMU)
9. Power Supply
10. Power Meter
11. Thermo-Electric Cooler (TEC) Controller
12. Thermal Camera
13. PC
14. Data Acquisition Software

12.2 Description of Test Setup and Equipment

Testing laser diodes and free-space optics is a bit of an art. All of the environmental parameters can effect the performance and behavior from ambient light, to temperature, to humidity, and more. It is important to recognize possible errors in testing setups and mitigate these errors.

The diode is mounted in a thermally controlled clamp which is controlled by the TEC controller. When diodes are emitting light they dissipate power and start to heat up. If the temperature is not regulated then the drive current will change and the output power will also change.

Ambient light can have a big effect optical measurements. To mitigate this measurement error the diode mount is snugged up to an integrating sphere. The integrating sphere reflects all of the light from the laser diode into a detector which can be observed on the power meter. Making the diode and integrating sphere light tight helps with the errors seen from ambient light.

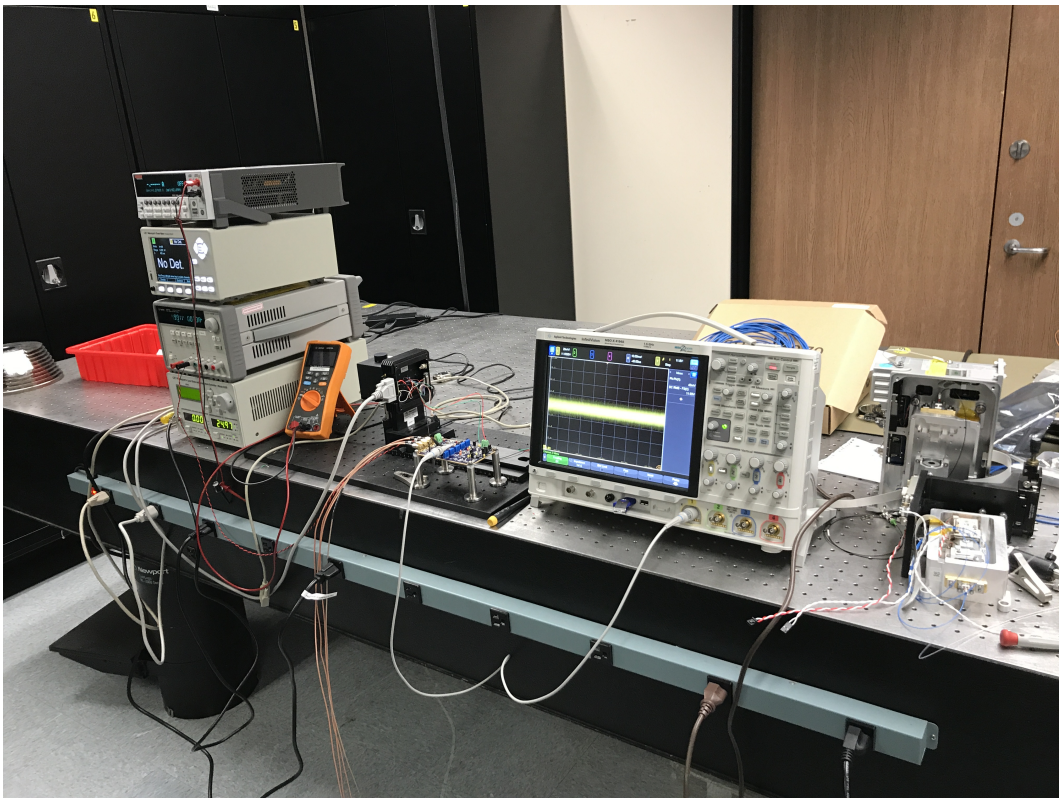

Figure 75: Testing station and equipment used during verification of performance.

12.3 Initial Power Up

When testing new electronics the first step is to confirm general functionality of each circuit. The input should be correct, the output should be correct based on the input, nothing should be saturated, current draw should be expected, no components should be in a thermal run-away. The picture below is a thermal image of the PCB. The power supplies on the left side of the picture are warm, which is expected. The driving transistor and current setting resistor are also warm which is expected. The PID op-amps are drawing current and working as well. This is a great start.

Figure 76: Thermal image of PCB on startup.

12.3.1 Power Supplies

The input is 5V and the current draw from the power supply is 80mA which is about expected. All of the voltage rails are giving the expected output with low peak to peak noise.

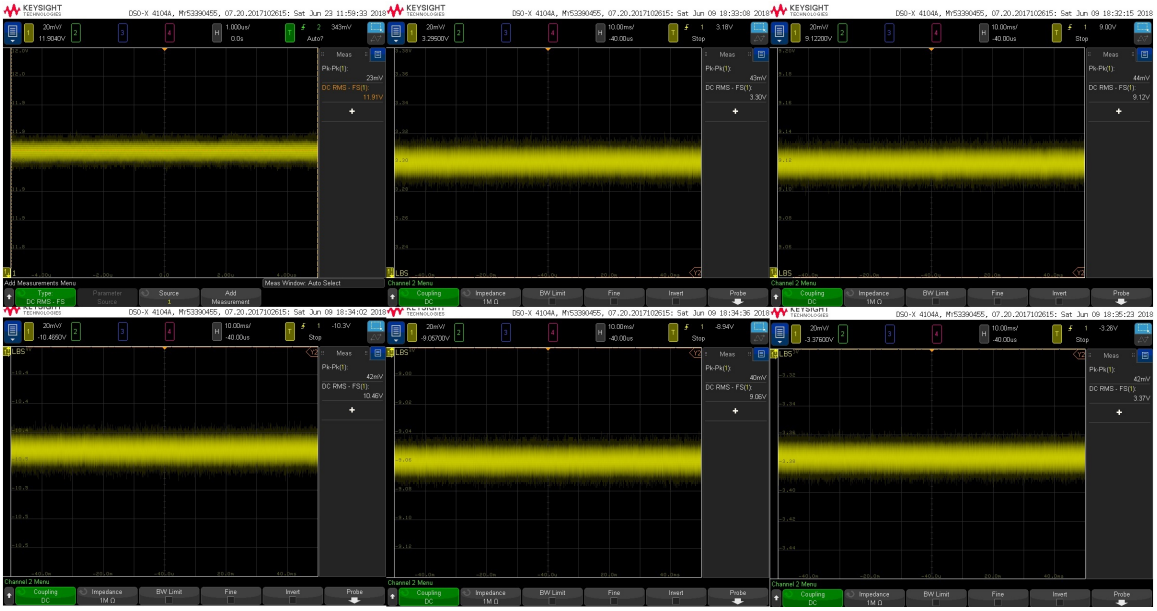

Figure 77: Power supply noise measured with Keysight Technologies 4104A oscilloscope.

12.3.2 Issues Found

Only three issues for a fairly complex PCB on the first spin is considered a huge success. The time spent simulating has paid off.

1. The first issue found was that the error amp, U1B, is driven from a 3.3V rail instead of 9V. The power supply trace was cut and a jumper wire was soldered from pin 8 to the 9V test point.

2. The second issue encountered was that the or gate, U14, was the incorrect logic gate. For testing the this is an easy fix. The input signal was inverted to turn on or off the laser.

3. The third issue was that the derivative term, U4A, was operating on the set-point, not the present value. A cut trace and jumper wire fixed this.

12.4 Power Supply Specifications

The laser diode driver specifications calls out two specifications to meet; Single supply range and supply current.

12.4.1 Single Supply

The single supply was tested by scanning the voltage input range that allows the laser driver to still operate to specifications. The low end was measured to be 3.5V and the upper end was 16V. The absolute max of the switching mode converters is 16V so that value was not exceed to avoid catastrophic failure.

12.4.2 Supply Current at 5V

The total current draw by the PCB when no laser is being driven and an input signal of 5V is applied. The power supply has a current reading which was used for this test. The PCB measured 74 mA of current draw.

12.5 Laser Bias

The data sheet for the laser driver calls out certain set point ranges and ratios.

12.5.1 Bias Current Setting Range

The voltage controlled current set point range. The user may cycle 0-3V in order to achieve 0-100mA of drive current. The actual measurements were 0-3V input would cause a drive current of 33uA to 102mA. This value will depend on the accuracy of the input signal, the voltage offset of the amplifiers, and the absolute value of the current setting resistor.

12.5.2 Bias Off Current

The measured current when the set point is requesting 0 mA. A value of about 30uA was measured when the input voltage was 0. This is due to the voltage offset of the amplifiers.

12.5.3 Bias Current Monitor Ratio

This value is essentially the ratio between the voltage set point and current output. The measured value for this specification is 29.8V/A, which is very close to the expected value of 30V/A.

12.6 Automatic Power Control

The following specifications refer to performance of the APC loop of the laser driver.

12.6.1 Photodiode Input Current

The maximum input current is 1mA, however the laser testing with had a maximum value of 330uA.

12.6.2 Photodiode Voltage Out

0-1mA input should correspond to 0-3V output. The values here will depend on the input bias current of the op-amp, the equivalent electrical model of the photodiode, and the absolute value of the gain resistor. The measured output was exactly as expected. This was expected because great care was taken in designing the TIA in previous chapters.

12.6.3 Photodiode Current Monitor Ratio

The typical value of 0.6V/mA, is just a ratio that may be expected. This value highly depends on the responsivity of the photodiode, the pick-off percentage, and drive current of the laser diode. A value of 0.3V/mA was measured during the testing this system.

12.6.4 Optical Drift

With a constant driving current and the diode held at a constant temperature, the drift of the optical reading should be less than 2% over a 2 hour period. This test required a computer and data acquisition system to collect data over 2 hours. The stability passes with 1.48% drift, however the results are disappointing. This value should be well under 1% drift. This parameter will be revisited at a later date.

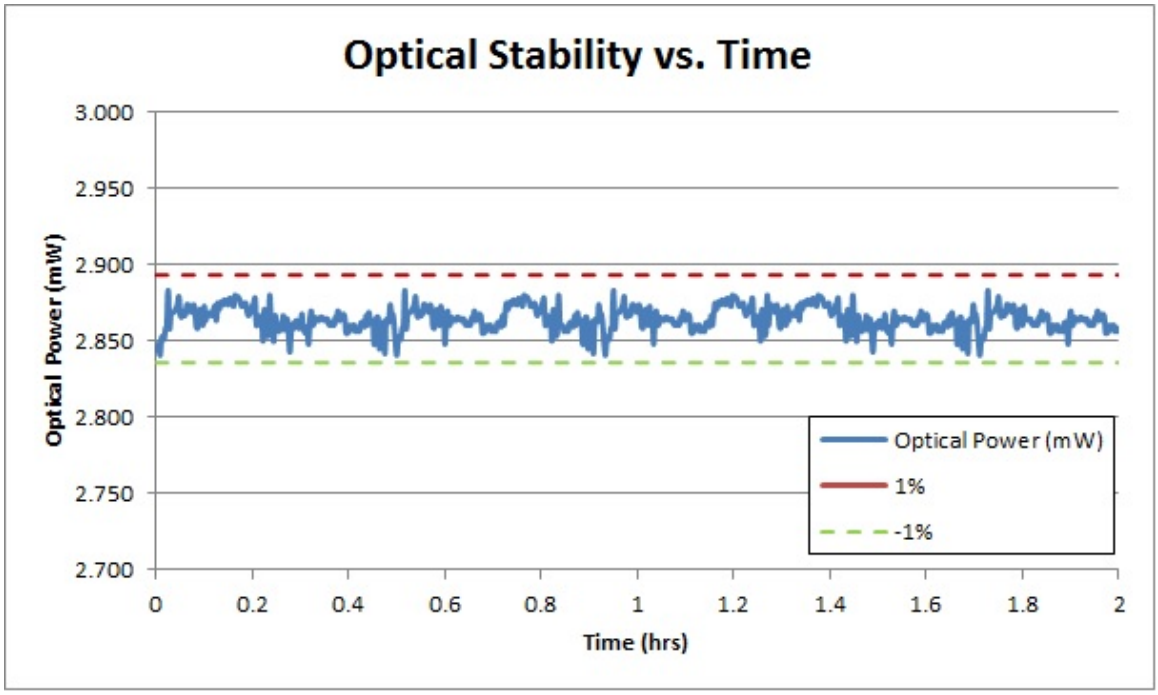

Figure 78: Optical stability measured over a period of two hours using a data acquisition system.

12.6.5 Electrical Stability

This parameter was measured while the optical stability test was running. The bias current was monitored on the oscilloscope with infinite persistence for a period of two hours. The electrical stability also passed with a drift of 0.9%, but it disappointing as well. A more stable driving current was expected.

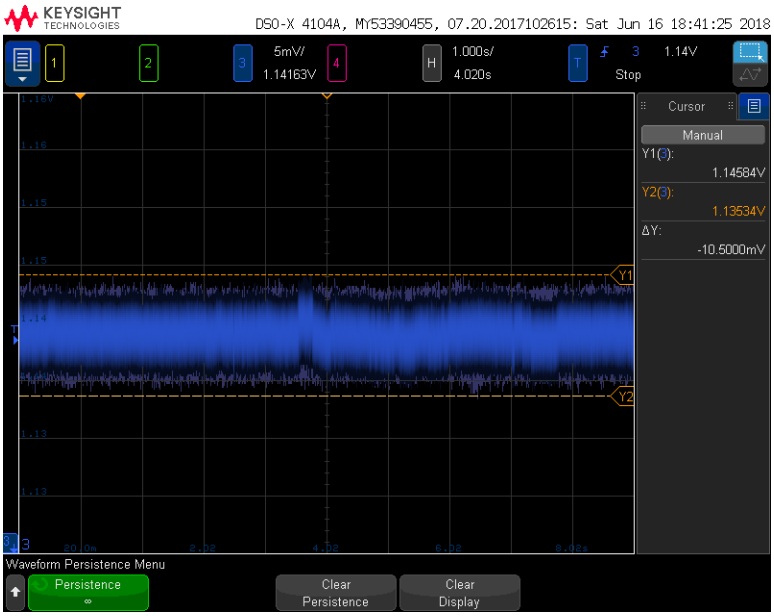

Figure 79: Electrical stability measured over a period of two hours using Keysight 4104A scope.

12.6.6 APC Loop Time Constant

This value was measured by taking a frequency response measurement of the transimpedance amplifier on the oscilloscope. The output was measured at the first stage, which becomes obvious when looking at figure 80. The cutoff frequency was measured to be 47.9kHz making the loop speed 20.9us.

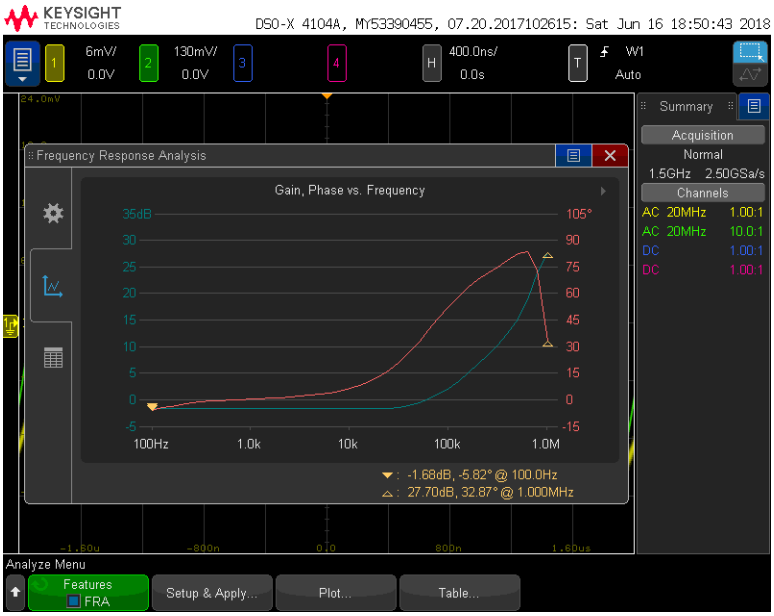

Figure 80: Frequency response TIA using Keysight Technologies 4104A oscilloscope.

12.7 Active Feedback Controls

The specifications in this section are aimed to measure the response of the control loop.

12.7.1 Startup Overshoot/Undershoot and Startup Settling Time

The allowed overshoot on startup is 5%, the measured overshoot is 0%. The typically startup settling time expected is 5ms due to the low pass filter. The measured startup settling time within 2% of the steady state value is 5ms.

Figure 81: APC PID laser driver response to step-up input.

12.7.2 Shutdown Overshoot/Undershoot

The allowed over/under shoot is 5%. The measured over/undershoot for this design is 0%.

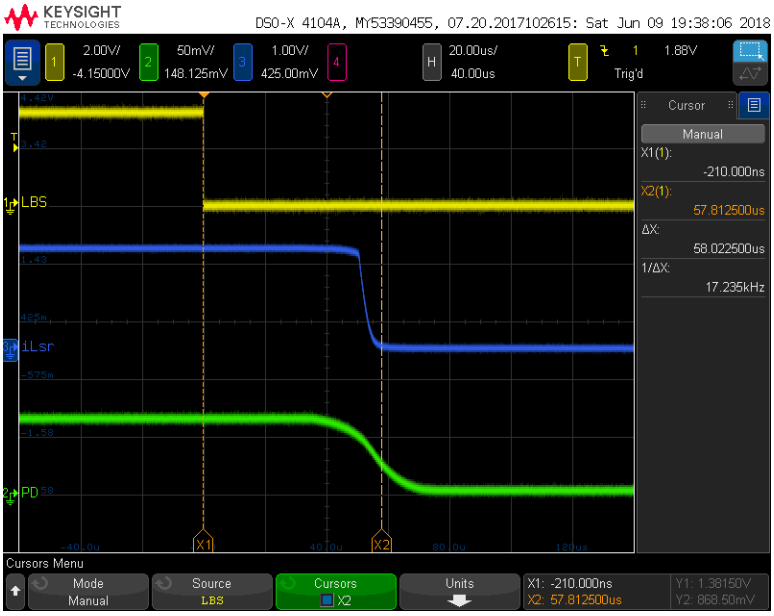

Figure 82: APC PID laser driver response to step-down input.

12.7.3 Step Change Overshoot/Undershoot

The allowed overshoot in response to a step in the set point is 10%. The measured overshoot is 1.4%.

Figure 83: APC PID laser driver response to an output disturbance change in set point.

12.8 Step Change Settling Time

The allowed time to respond and correct the current due to a step change in the set point is 1ms. The measured time is 0.7ms.

Figure 84: APC PID laser driver settling time to an output disturbance change in set point.

12.8.1 Settling Accuracy

This value is the expected driving current vs. the set point. When bypassing the control loop, this value should follow the bias current monitor ratio. When the PID loop is active and tuned, this value can be slightly altered due to the overall gain of the PID. The gain between Kp, and the gain compensation on Ki was measured to be 0.57. Figure 81 shows that the driving current is 1.8V when the set point is 3V. From the calculations below settling accuracy is 5.3%.

$$V_{settle,expected} = (Vapc)(GAIN_{PID}) \tag{85}$$

$$V_{settle,expected} = (3)0.57 = 1.71V \tag{86}$$

$$V_{settle,measured} = 1.8V \tag{87}$$

$$Accuracy_{settle} = \frac{1.8 - 1.71}{1.71} = 5.3\% \tag{88}$$

12.9 Laser Safety

The ability to quickly extinguish a laser diode is an important safety feature in a laser driver.

12.10 Turn-Off Delay and Overcurrent Protection Delay

These two values are measured using the laser shutdown control line. The allowed turn-off delay is 100us and overcurrent protection delay is 125us. The difference in measurements is an added RC time delay on the overcurrent protection. The measured shutdown time is 58us for the turn-off delay and 78us for the overcurrent protection.

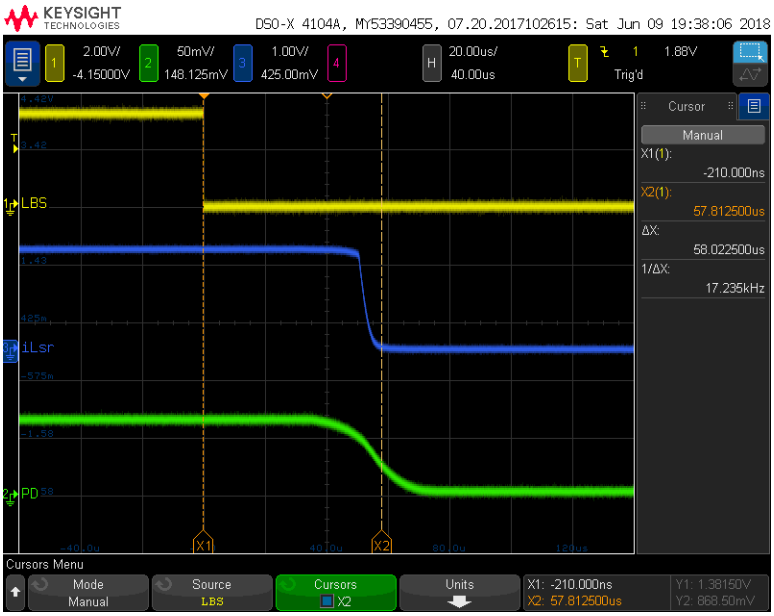

Figure 85: APC PID laser driver response to shutdown and overcurrent fault.

12.11 Noise Performance

The noise performance will have a large dependence on the laser diode and photodiode characteristics. The calculations in previous chapters mathematically proved that these numbers are achievable for a real system.

12.12 Testing Conclusion

The data sheet dictated the design goals for this project. According the simulations and test results this project has been successful. There are improvements to make regarding stability of the optical output and the drive current, however the specifications were all met. For a first pass prototype from scratch this was a quick bring up with excellent results.

LASER DRIVER SPECIFICATIONS					TESTING RESULTS				PASS/FAIL
PARAMETER	MIN	TYP	MAX	UNITS	MIN	TYP	MAX	UNITS	
POWER SUPPLY					**POWER SUPPLY**				
Single Supply	3.75	5	15	V	3.5	5	16	V	PASS
Supply Current (@ 5V)	50	80	100	mA		74		mA	PASS
LASER BIAS					**LASER BIAS**				
Bias-Current-Setting Range	0		3	V	0		3	V	PASS
Bias-Current-Setting Range	0		100	mA	0.033		102	mA	PASS
Bias Off Current			0.5	mA		0.03		mA	PASS
Bias-Current Monitor Ratio		30		V/A		29.8		V/A	PASS
AUTOMATIC POWER CONTROL					**AUTOMATIC POWER CONTROL**				
Photo Diode Input Current	0		1	mA		0.33		mA	PASS
Photo Diode Voltage Out	0		3	V	0		3	V	PASS
Photo Diode Current Monitor Ratio		0.6		V/mA		0.3		V/mA	PASS
Optical Drift		2		%		1.48		%	PASS
Electrical Stability			1	%		0.9		%	PASS
APC Loop Time Constant		20		us		20.9		us	PASS
ACTIVE FEEDBACK CONTROLS					**ACTIVE FEEDBACK CONTROLS**				
Startup Overshoot/Undershoot			5	%		3.6		%	PASS
Shutdown Overshoot/Undershoot			5	%		0		%	PASS
Step Change Overshoot/Undershoot			10	%		1.4		%	PASS
Startup Settling Time		5		ms		5		ms	PASS
Step Change Settling Time			1	ms		0.7		ms	PASS
Settling Accuracy			10	%		0		%	PASS
LASER SAFETY					**LASER SAFETY**				
Turn-Off Delay			100	us		58		us	PASS
Overcurrent Protection Delay			125	us		78		us	PASS

Figure 86: Data sheet specifications vs. test results.

13 Conclusion

The goals laid out in the introduction have been addressed and met throughout this project. Weaknesses in off the shelf laser diodes were identified and a data sheet to improve upon these weaknesses was developed. A scalable laser driver was designed using purely analog electronics. A closed loop APC laser driver was realized from the original laser driver design. A robust feedback mechanism was designed and added to the laser driver which automatically controlled the output

of the laser to maintain the set point. The steps for electronic design were carefully explained and stepped though. Time and frequency domain simulations were completed using a mixture of SPICE, Matlab, and Simulink. After all of the simulation results proved to be acceptable, a PCB was designed, assembled, and actual test results were gathered and compared against the original specifications. This project is an accurate representation of a real life engineering design cycle.

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