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Thermally activated reversible threshold shifts in $YBa_2Cu_3O_{7-\delta}$/ yttria-stabilized zirconia/Si capacitors

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$YBa_2Cu_3O_{7-\delta}$/yttria-stabilized zirconia (YSZ)/silicon superconductor–insulator–semiconductor capacitors are characterized with capacitance-voltage (C-V) measurements at different gate-voltage sweep rates and under bias-temperature cycling. It is shown that ionic conduction in YSZ causes both hysteresis and stretch-out in room-temperature C-V curves. A thermally activated process with an activation energy of about 39 meV in YSZ and/or at YSZ/Si interface is attributed to trapping/detrapping mechanisms in the SiO_x interfacial layer between YSZ and Si. The negative mobile ions in YSZ can be moved by an applied electric field at room temperature and then "frozen" with decreasing temperature, giving rise to adjustable threshold voltages at low temperatures.

Electrical characterization of $YBa_2Cu_3O_{7-\delta}$(YBCO)/yttria-stabilized zirconia (YSZ)/Si superconductor–insulator–semiconductor (SuIs) capacitors was recently reported.[1–3] The performance of those devices is comparable to that of conventional metal–oxide–semiconductor (MOS) capacitors, with the exception of a high-temperature superconducting gate and considerable ionic effects due to the presence of oxygen vacancies in the insulator layer.[4,5] This device structure is suitable for determining the electrical properties of each material component, namely, YBCO, YSZ, and Si, as well as their interfaces. Since understanding the properties of the capacitor serves as a precursor to the development of a superconductor–insulator–semiconductor field-effect transistor (SuIsFET), this letter reports a finding on thermally activated threshold voltage shifts, which will have a significant impact on the operation of future SuIsFETs at superconducting temperatures.

The YBCO/YSZ/Si capacitors were fabricated from films of YBCO and YSZ deposited *in situ* on *p*-type Si wafers using pulsed laser deposition.[6] Resistivity measurements for the YBCO films yield a critical temperature of 86 K with a transition region of less than 2 K. YBCO and YSZ thicknesses are greater than 1500 Å to avoid high leakeage current. The YBCO layer was patterned and etched to form the gate of the capacitor. Gold contacts were evaporated onto the YBCO gate and the Si substrate under a background pressure of 4×10^{-6} Torr to yield low-resistance ohmic contacts.

High-resolution cross-sectional transmission electron microscopy revealed a nearly atomically abrupt YBCO/YSZ interface and a thin SiO_x interfacial layer (~ 40 Å) between YSZ and Si.[7] This interfacial layer, formed in the later stage of YSZ deposition,[8] serves to stabilize the structure, resulting in reproducible electrical characteristics and a low interface trap density.[2,3]

Room-temperature (RT) current-voltage (I-V) measurements were performed on the SuIs capacitors prior to capacitance-voltage (C-V) measurements. The I-V characteristics exhibit typical ionic conduction with a RT leakage current density of about 15 nA/cm^2 at 3 V. This behavior corresponds to a resistivity of about 10^{14} Ω cm, which is much smaller than that of bulk YSZ.[9] This difference in resistivity is most likely due to defect-assisted ionic conduction in thin film YSZ.

The RT C-V characteristics of the YBCO/YSZ/Si SuIs capacitor are shown in Fig. 1. The gate voltages were swept in positive and negative directions at various sweep rates as shown. "Point-by-point" measurements are conducted by applying an extremely low sweep rate so the device can fully relax prior to each capacitance reading. The hysteresis present in each set of C-V curves confirms the presence of mobile ions in YSZ. In comparison with the point-by-point curve, the C-V curves with higher sweep rates are clearly more stretched out; this phenomenon is also consistent with the existence of mobile ions. At higher sweep rates, the mobile ions are delayed in reaching their equilibrium positions at each voltage step. Accordingly, a larger range of gate voltages is then required for the capacitor to cover the depletion state. Thus the C-V curve is stretched out along the gate-voltage axis. The higher the sweep rate, the more the C-V curve stretches out. Further, for a positive sweep from accumulation or a negative sweep from inversion, the negative mobile ions are initially concentrated near the YSZ/Si or YBCO/YSZ interfaces, respectively. The drift motion of mobile ions is less likely to keep up with higher sweep rates, giving rise to variations in the effective YSZ charge and in the magnitude of hysteresis. Thus the magnitude of the hysteresis is expected to increase with sweep rate. These effects of sweep rates are clearly evident in Fig. 1.

Figure 2 shows the positive-sweep and negative-sweep C-V curves measured during cooling without bias on the YBCO gate. When the capacitor is cooled from room temperature, the clockwise hysteresis of the C-V curves in the depletion region decreases due to "freezing" of mobile ions.
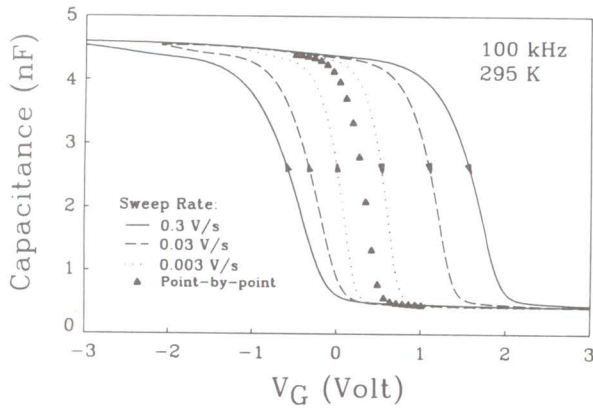
FIG. 1. Room-temperature C-V characteristics of a YBCO/YSZ/Si capacitor at 100 kHz for positive and negative voltage sweep directions and at various sweep rates.

FIG. 3. Temperature dependence of flatband voltage and effective YSZ charge for the capacitor with C-V characteristics shown in Figs. 1 and 2.

Upon further cooling below −50 °C, the hysteresis seems to change in direction, which is attributed to a difference in temperature dependence of emission/capture rates at the YSZ/Si interface traps.[10] With temperature approaching 80 K, deep depletion prevails over strong inversion. Another important feature exhibited in Fig. 2 is the negative shift in threshold voltage with cooling. In general, the flatband voltage component of the threshold voltage is given by

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i},\qquad(1)$$

where ϕ_{ms} is the work function difference between YBCO and Si, Q_i is the effective insulator charge, and C_i is the insulator capacitance. The voltage-dependent interface trapped charge is ignored in this discussion. Assuming that the temperature dependencies of ϕ_{ms} and C_i are negligible, the flatband shift can be simplified as

$$\Delta V_{FB} = \frac{Q_i(T_0)}{C_i} - \frac{Q_i(T)}{C_i},\qquad(2)$$

where T_0 is chosen to be room temperature, 295 K, then the temperature dependence of the effective YSZ charge can be expressed as
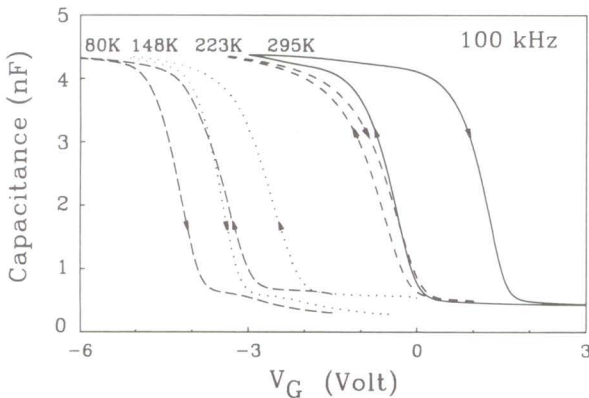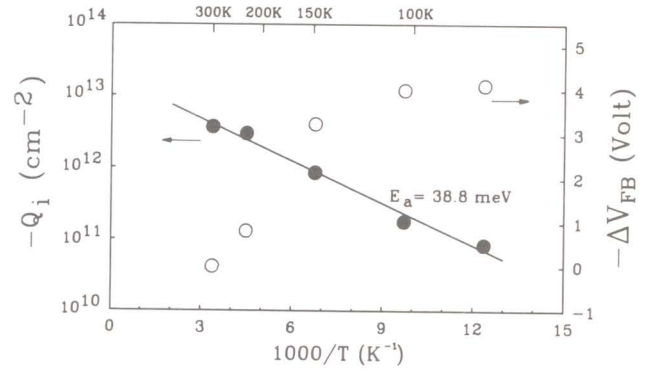
$$Q_i(T) = Q_i(T_0) - C_i \Delta V_{FB}.\qquad(3)$$

The flatband shifts are determined from point-by-point C-V measurements at various temperatures in comparison with RT data. A linear regression of $\log |Q_i(T)|$ vs $1/T$ produces an activation energy of $E_a = 38.8$ meV, as shown in Fig. 3. Thus Q_i follows a thermally activated Arrhenius behavior:

$$Q_i(T) = Q_0 e^{-E_a/kT}.\qquad(4)$$

We attribute this process to trapping/detrapping in the SiO_x interfacial layer in the temperature range studied.[11]

Since the flatband shift is associated with a thermally activated process, the threshold voltage of the capacitor at low temperature can be "set" by simply cooling the device from room temperature with a suitable bias on the YBCO gate. This procedure is known as bias-temperature cycling (BTC).[10] During BTC, the mobile ions are redistributed by the applied electric field, and then "frozen" at the lower temperatures. Therefore, the increase or decrease in $|Q_i|$ over the zero-bias case must be accompanied by a corresponding positive or negative threshold shift at low temperatures, respectively. If one considers only the drift motion of mobile ions, then the magnitude of this change in threshold voltage should be at most the same as the applied bias during cooling.

Measurements were performed to verify these predicted threshold shifts. Figure 4 shows C-V plots for a capacitor cooled to 80 K at several biases. The shifts in the BTC curves with respect to zero-bias agree qualitatively with the above arguments. For the positively biased capacitor, the negative threshold shift is enhanced by an amount almost equal to that of the applied bias. The discrepancy between the threshold shift and the negative bias is possibly due to electric field effect on the SiO_x/Si interface trap charges as reported previously for MOS capacitors.[12] This thermally activated process and the resulting electrical adjustment of threshold voltage at superconducting temperatures can have a significant impact on the operation of SuIsFETs utilizing this capacitor as the gate structure.

In summary, C-V characteristics of YBCO/YSZ/Si SuIs capacitors are obtained by varying the sweep rate and by using the BTC technique. At room temperature, the mobile ions in YSZ are responsible for stretch-out and hys-
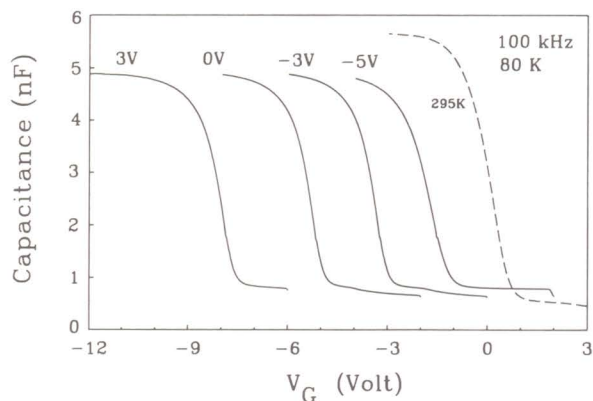

FIG. 2. C-V characteristics of a YBCO/YSZ/Si capacitor during cooling from room temperature to 80 K.

FIG. 4. *C-V* characteristics of a YBCO/YSZ/Si capacitor cooled to 80 K under different biases. The gate voltages are swept in the negative direction and the room-temperature behavior is shown as a reference.

teresis of the *C-V* curves at fast sweep rates. A thermally activated process exists in the YSZ layer and/or at the YSZ/Si interface during cooling, which is attributed to trapping/detrapping in the SiO_x interfacial layer. The distribution of mobile ions in YSZ can be set via gate bias and then frozen by lowering the temperature. Therefore, the threshold voltage of the capacitor can be adjusted at superconducting temperatures with an appropriate bias on the YBCO gate during cooling.

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