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Determination of density of trap states at Y_2O_3-stabilized ZrO_2/Si interface of $YBa_2Cu_3O_{7-\delta}$/Y_2O_3-stabilized ZrO_2/Si capacitors

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$YBa_2Cu_3O_{7-\delta}$/yttria-stabilized zirconia (YSZ)/silicon superconductor-insulator-semiconductor capacitors are characterized with current-voltage and capacitance-voltage (C-V) measurements at different temperatures between 223 and 80 K. As a result of "freezing" of mobile ions in YSZ, effects of trapped charge at the YSZ/Si interface dominate the device electrical properties at superconducting temperatures. Density of interface states and its temperature dependence are determined using a modified high frequency C-V method, in which the temperature dependences of band gap, Fermi level, and active dopant and intrinsic carrier concentrations are considered. At superconducting temperatures, e.g., 80 K, the interface state density within the band gap is reduced to lower than 1×10^{11} cm^{-2} eV at midgap. The low interface state density at the YSZ/Si interface is important for acceptable performance and reliability devices made up of such capacitors.

Recent efforts in incorporating high-critical-temperature (T_c) superconductor thin films into existing silicon technology have been focused on using buffered silicon,[1,2] since the reactions between these cuprate films and Si preclude their direct deposition onto Si substrates.[3] Yttria-stabilized zirconia (YSZ) is a good candidate for such a buffer because of its structural and electrical properties, on which high-T_c superconductor thin films, $YBa_2Cu_3O_{7-\delta}$ (YBCO), with $T_c>87$ K and critical current density $>10^6$ A/cm^2 at 77 K have been deposited.[4] Studies on the material components and their interfaces in this system have been recently carried out on YBCO/YSZ/Si superconductor-insulator-semiconductor (SuIS) capacitors.[5,6] High-resolution cross-sectional transmission electron microscopy revealed an atomically abrupt YBCO/YSZ interface and a thin SiO_x interfacial layer (~40 Å) between YSZ and Si.[7] Thus, the YSZ/Si interface is actually a YSZ/SiO_x/Si multilayer system. Since carrier transport near the YSZ/Si interface is a critical issue in developing superconducting gate SuIS transistors, investigation of effects of interface trapped charge on the electrical properties of the SuIS capacitors and determination of interface state density and its temperature dependence are of particular importance.

The YBCO/YSZ/Si capacitors were fabricated from films of YBCO and YSZ deposited *in situ* on p-type Si wafers using pulsed laser deposition.[1] Resistivity measurements for the YBCO films yield a critical temperature of 86 K with a transition region of less than 2 K. YBCO and YSZ thicknesses are about 1500 Å each. The YBCO layer was patterned and etched to form the gate of the capacitor. Gold films were evaporated onto the YBCO gate and the Si substrate under a background pressure of 4×10^{-6} Torr to yield low-resistance Ohmic contacts.

Electrical characterization of the YBCO/YSZ/Si capacitors was carried out using current vs voltage (I-V) and capacitance vs voltage (C-V) measurements. During these measurements, the gate bias was swept in both positive and negative directions. The room-temperature I-V and C-V characteristics have been determined to be dominated by the existence of mobile ions in YSZ.[8] When temperature decreases, these electrical characteristics of the capacitor are dominated by trapped charges at the YSZ/Si interface.[9] This effect is evidenced by C-V measurements from room temperature down to 80 K, obtained under the condition of weak illumination. Figure 1 shows effects of illumination on low-temperature (80 K) C-V characteristics. An ideal C-V curve, which is computed under the assumptions of no insulator charge, no interface trapped charge, no work function difference between YBCO and Si, and constant doping in the substrate, is shifted from its original position of zero flatband voltage for comparison. Illumination of the device increases the emission/capture rates of the YSZ/Si interface traps, resulting in decreased hysteresis between positively and negatively swept C-V curves and increased stretchout in both curves. At the same time, true inversion is obtained due to an optically induced increase in generation/recombination rates of minority electrons near the Si surface.

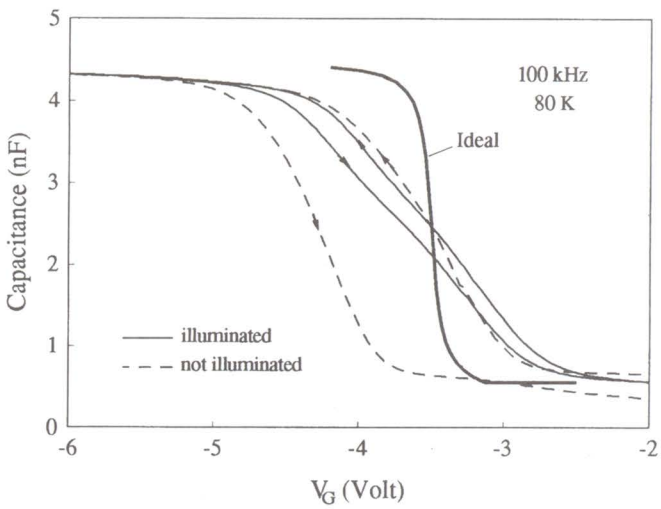

FIG. 1. Effect of illumination on hysteresis and stretchout of the C-V characteristics at 80 K.

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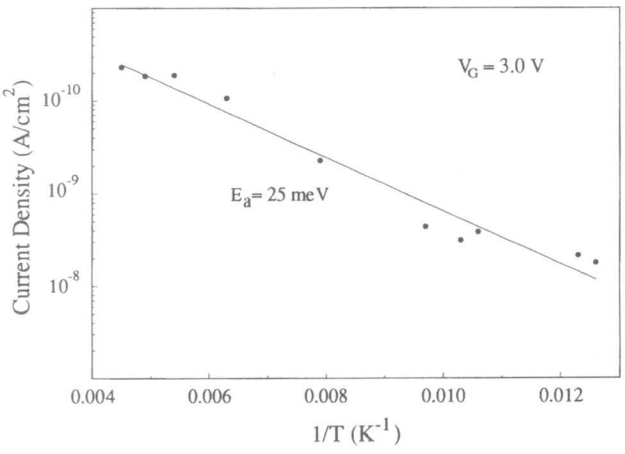

FIG. 2. Temperature dependence of the leakage current density for a YBCO/YSZ/Si capacitor.

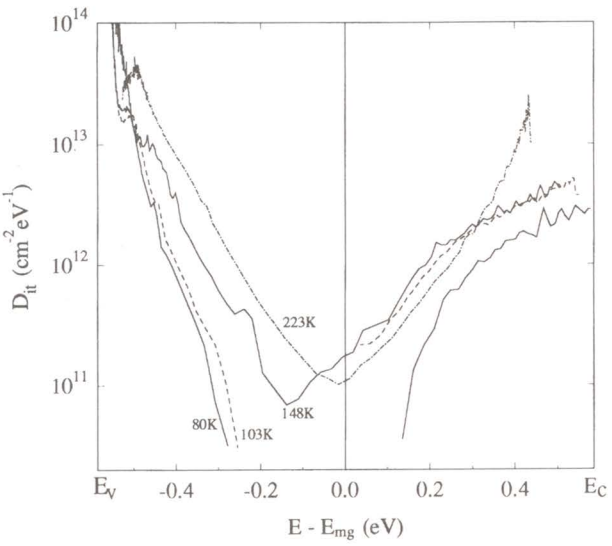

FIG. 3. Temperature dependent D_{it} distributions. E_v, E_x, and E_{mg} are valence-band level, conduction-band level, and midgap level, respectively.

Effects of interface trapped charge on the capacitor is further examined by I-V measurements at different temperatures between 223 and 80 K. A plot of device leakage current density versus temperature is shown in Fig. 2, which exhibits an Arrhenius behavior. A linear fit of the experimental data produces an activation energy of 25 meV. Comparing this quantity with the activation energies obtained from the temperature dependence of effective YSZ charge[8] and studies on the stressed SiO_2/Si interface,[10] we conclude that this temperature behavior of the capacitor leakage current at low temperature is a manifestation of charge trapping/detrapping at the YSZ/Si interface.

The results summarized above have clearly established that the trapped charge at the YSZ/Si interface is primarily responsible for the electrical behavior of the SuIS devices at superconducting temperatures. In order to understand better the mechanism underlying such behavior, it is essential to determine the interface state density, D_{it}, and to observe its temperature behavior. Based on a technique developed by Terman for determination of capacitance due to interface traps for metal-oxide-semiconductor capacitors using high-frequency C-V measurements,[11] a method which includes the temperature dependencies of ionized dopant concentration (N_A^-), intrinsic carrier concentration (n_i), band gap (E_g), and Fermi level (E_F) is developed to determine D_{it} at the YSZ/Si interface.

Generally, interface traps do not respond to the ac gate voltage during a high-frequency C-V measurement because their emission/capture rates are not high enough for trapping/detrapping to follow the ac signal, especially at low temperatures. Therefore, the interface trapped charge does not contribute to the measured capacitance. However, the dc gate bias, V_G, changes at a sufficiently low sweeping rate, such that the interface traps can follow and respond to the change. This response causes the high-frequency C-V curve to stretch out in the depletion regime along the voltage axis since interface trap occupancy as well as depletion layer charge must change with dc voltage sweep. This stretchout is clearly illustrated in Fig. 1 where comparison with the ideal curve is included.

In determination of D_{it}, we first computed the ideal capacitance as a function of band bending or Si surface potential, ψ_s. By comparing measured capacitance with the ideal capacitance, a $\psi_s - V_G$ plot is generated. A distribution of interface state density in the band gap is then determined from the $\psi_s - V_G$ plot.

For low-temperature D_{it} calculations, one should also consider the temperature dependences of E_g, E_F, n_i, N_A^-, and ϕ_B $[\equiv kT/q \ln(N_A^-/n_i)]$. We computed D_{it} of the YBCO/YSZ/Si capacitor using the high-frequency C-V characteristics obtained with a V_G sweeping rate of 0.3 V/s for several temperatures between 223 and 80 K. The results are shown in Fig. 3.

Figure 3 shows the D_{it} distribution in the band gap as a function of temperature. Since the room temperature C-V behavior is dominated by mobile ions, D_{it} is obtained for temperatures below 223 K. It is clear that D_{it} decreases with decreasing temperature, except for the 223 K curve in the region above midgap, which might be due to residual effect of mobile ions. The broken curves of the 103 and 80 K behaviors near midgap are probably due to interface state densities below the minimum detectable limit, which can be understood by considering the exponential temperature dependence of interface trap emission/capture rates.[12] The low YSZ/Si interface state density can facilitate carrier transport near the Si surface at superconducting temperatures, and it also indicates that YSZ is an effective buffer layer for preventing Si from YBCO "poisoning."[13]

In summary, trapped charge effects at the YSZ/Si interface are examined by performing I-V and C-V measurements on the YBCO/YSZ/Si capacitor at low temperatures. Based on a modified C-V method, the distribution and temperature dependence of interface state density are determined. With decreasing temperature, interface state density decreases to lower than 1×10^{11} cm^{-2} eV^{-1} near midgap. Such low interface state density can result in acceptable performance and reliability of superconducting devices using this SuIS structure.

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