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Current Feedback-Based High Load Current Low Drop-Out Voltage Regulator in 65-nm CMOS Technology

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CURRENT FEEDBACK-BASED HIGH LOAD CURRENT LOW DROP-OUT VOLTAGE REGULATOR IN 65-NM CMOS TECHNOLOGY

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by

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ABSTRACT

CURRENT FEEDBACK-BASED HIGH LOAD CURRENT LOW DROP-OUT VOLTAGE REGULATOR IN 65-NM CMOS TECHNOLOGY

by Melody Teoh

The motivation for this paper was to design a current feedback-based high load current, low drop-out (LDO) voltage regulator. A bandgap voltage reference (BGR) was also designed in conjunction with the LDO to simulate realistic environments. The schematic was designed with Cadence Virtuoso Schematic XL, using the Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS library, used for Internet of Things (IoT) System on Chip (SoC) applications. The proposed capacitor-less LDO with BGR provided an average temperature coefficient (TC) of 13.34 ppm/℃ within the range of -40 to 125 ℃. This was in accordance with military standards to gain a higher stability and power supply rejection ratio (PSRR). The proposed capacitor-less LDO also achieved a 200 mA load current with an error percentage of 0.246% and a -21.47 dB PSRR at 100 KHz with a current based structure. This thesis concluded with the application of capacitor-less LDO in medical IoT devices, followed by the future of medical device development.

ACKNOWLEDGEMENTS

There were times where I was demotivated. There were also times where I really wanted to give up. There were a lot of struggles. There were times where I thought my work would be overdue. I am blessed to be surrounded by amazing people in my life. It would be impossible to complete this work without their support and wisdom.

First and foremost, many thanks to my thesis advisor, Dr. Sotoudeh Hamedi-Hagh, for providing the TSMC 65-nm technology library and the Cadence software for my thesis research purposes. I am especially thankful to Chi-Hsien Yen and Rahul Sreekumar, my colleagues of the Radio Frequency Integrated Circuit (RFIC) lab for their endless help and support for this work.

Without hesitation, I want to offer my deepest gratitude to my parents and my boyfriend for their love and companion. They make me the person I am today.

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LIST OF ABBREVIATIONS

ASIC – Application-specific integrated circuit

BGR – Bandgap voltage reference

BJT – Bipolar junction transistor

BOM – Bill of materials

CMOS – Complementary metal-oxide-semiconductor

DC – Direct current

DRC – Design Rule Check

ECG – Electrocardiogram

ESL – Effective series inductance

ESR – Effective series resistance

IC – Integrated circuit

IoT – Internet of Things

LDO – Low drop-out

LVS – Layout Versus Schematic

mIoT – Medical Internet of Things

MOSFET – Metal-oxide-semiconductor field-effect transistor

NMOS – N-type metal-oxide-semiconductor

Op-amp – Operational amplifier

PASS – Pass device

PCB – Printed circuit board

PMOS – P-type metal-oxide-semiconductor

PSRR – Power supply rejection ratio

RC – Resistance and capacitance

RFID – Radio-frequency identification

SoC – System on chip

TC – Temperature coefficient

T_{MAX} – Maximum temperature

T_{MIN} – Minimum temperature

V_{BE} – Base-to-emitter voltage

V_{DSAT} – Saturated drain voltage

V_{EB} – Emitter-to-base voltage

V_{GS} – Gate-to-source voltage

V_{OUT} – Output voltage

V_{REF} – Reference voltage

V_T – Thermal voltage

V_{TH} – Threshold voltage

τ – Time constant

Chapter 1
Introduction

The proposed architecture consists of differential amplifiers (op-amps), bandgap voltage regulators (BGR) and low drop-out (LDO) voltage regulators. All of them are applicable in a wide range of applications.

In this work, the Internet of Things (IoT) technology is emphasized as the application of a proposed high load current capacitor-less LDO architecture. This architecture is intended to be designed and embedded on-chip and can target several application-specific integrated circuit (ASIC) products and medical devices. Recently, temperature-sensing devices have been introduced to the market as personal healthcare monitoring units. In the near future, these devices could stand out more, taking their place in public and private healthcare systems instead of acting as mere individual health trackers. The low power feature makes it possible for the product to be embedded into consumer products, such as wearable devices.

The proposed architecture could be further investigated and developed into an economical and convenient medical device for patients with disabilities or those who are bedridden for a long period of time. This device will collect accurate data that could be logged into medical records during doctor's appointments to assist doctors in making more precise diagnoses.

Chapter 2
IoT Technology

2.1 Introduction

Wired connection among devices has been succeeded by IoT. New technological advances, including sensing devices, have been discovered by this new generation technology. Sensing devices lead to the development of a new industry in IoT connections with challenges such as low power consumption, power supply stabilization, smaller chip sizes and wireless features.

2.2 Key Factors of IoT

Although IoT provides the benefit of connecting and facilitating communication between devices, there are various key factors to IoT that are necessary to create a realistic IoT environment.

One of the key factors is device connectivity. The main concern for IoT devices is their reliability within a working environment. Devices and hardware in our current non-IoT infrastructure have a low tolerance towards failure. However, IoT devices that communicate closely with each other have an even lower tolerance for such failures or bugs within themselves. The consequences of such IoT devices failing during operation are far more severe than for normal devices.

Another key factor is device robustness. IoT infrastructures are usually in a much more sensitive environment than others. For these IoT devices, there is a need to include for security measures, such as tamper-proofing and authentication, as the industry standard for security in them is much greater than for regular devices.

Finally, another key factor of IoT is cost-effectiveness. IoT devices are small devices with low power consumption. Determining the cost of these devices requires a trade-off between robustness and effectiveness, and this issue needs to be addressed within the grander scheme of IoT infrastructure [1].

2.3 Applications of IoT

Since their inception, IoT environments have been designed and implemented within non-technical fields and within traditional non-IoT infrastructure. This was a result of multiple factors such as the important and efficient usage of data collection and the cost-effectiveness of IoT devices.

Currently, IoT is being applied in the development of smart city infrastructure as well. Wen and Chen (2018) described the smart city infrastructure implemented in Taiwan, where the country has implemented an indigenous RFID-based toll collection system on its freeways that converted the standard flat-rate toll system to a system that charges based on distance travelled [2]. Taiwan was the first country to design and implement this unique system.

One of the more well-known applications of IoT is big data collection. Smart city infrastructures have also implemented IoT devices for an accurate data collecting system to generate better research and analysis on the city's current infrastructure. Ansari and Mehrotra (2018) explained that urban data are essential to understanding city society, which can lead to scientific opinions on city culture and socioeconomic status [3]. With urban IoT devices being implemented in various public services, areas and networks,

more data can be generated that will help develop a better understanding of a city's status.

Another known application of IoT is medical IoT (mIoT). Dimitrov (2016) stated that by 2020, 40% of IoT-related technologies will be within the field of healthcare and health monitoring [4]. A variety of sensor devices such as pacemakers, ECG sensors and X-ray scanners generate large amounts of data in a short period of time. All of these data create a more accurate and technical diagnosis. This brings a more dynamic perspective of the patient's current situation, assisting the users of these data such as doctors and nurses in monitoring the patient's current health status. Incorporating this data collection mIoT infrastructure into hospitals would make it easier to record and retrieve a patient's medical information throughout a large medical network. This would not only benefit the doctors in treating patients by a scientific and data-oriented approach, but it also would provide personal treatment to the patients themselves.

2.4 Summary

Chapter 2 has reviewed the parameters of the IoT in a general technology spectrum. Wireless features and low energy consumption are the main aspects that define IoT technology. The use of IoT devices is affordable due to the small chip area and power consumption performance. The applications of IoT are scalable, ranging from usage in smart city infrastructures to healthcare and finally to households. The use of IoT in data collection would facilitate accurate scientific analysis.

Chapter 3
Differential Amplifier Theory

3.1 Introduction

Operational amplifiers (op-amps), especially differential amplifiers, are versatile and functional circuit building blocks used in analog integrated circuits. They are applicable in both bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). The main purpose of a differential amplifier within an analog integrated circuit is to step up the voltage difference found between the inverted and non-inverted inputs.

3.2 Theory

The output voltage of a differential amplifier was based on a constant factor. This constant factor, known as the differential gain is determined by the ratio of the input and feedback resistors found within the differential amplifier. Figure 3.1 shows the basic circuit diagram of an inverting op-amp.

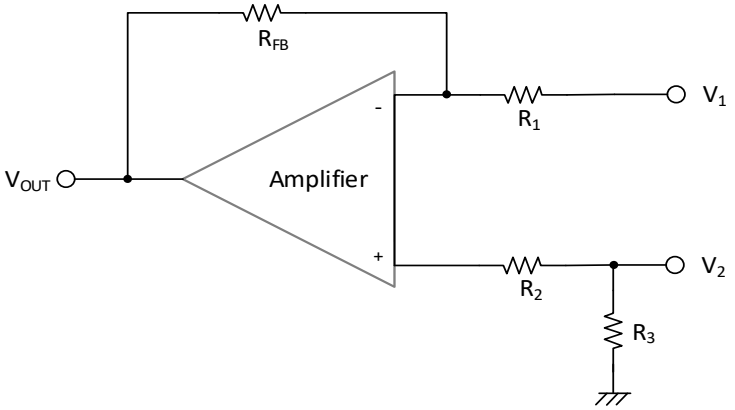

Figure 3.1 Inverting op-amp.

The constant factor also determined the multiplication magnitude of the voltage difference between the two inputs [6]. The calculation for determining output voltage of the differential amplifier is expressed in Equation 3.1 [5].

$$V_{OUT} = \frac{R_{FB}}{R_1}(V_2 - V_1) \quad (3.1)$$

The common mode signal, which is common to both inputs, is rejected within a differential amplifier, as it bears no value to the outcome of the output voltage [6].

3.3 Types of Differential Amplifier

Differential amplifiers of different structures provide varied results. Different structures provide optimum output voltages based on the constraints of the application.

3.3.1 Folded Cascade

The folded cascade topology is widely used for differential amplifiers. Its popularity is due to its folding characteristic, which reduces the size of the amplifier within the circuit and require a smaller voltage input than other topologies without losing performance. Furthermore, the folded cascade topology increases the resistance output, sequentially increasing the gain of the amplifier [7].

3.3.2 Common Source

Common source differential amplifiers normally contain two-stage CMOS op-amps, whereby the additional amplifier is added to increase the gain. More stages within an op-amp result in an increase of poles within the output voltage, meaning higher noise levels and unstable output voltages. Therefore, a two-stage system results in two poles, causing phase margin problems of much less than 60°.

3.4 RC Circuit

A resistance and capacitance (RC) circuit compensates for the differential amplifier by improving stability and phase of the output voltage. The RC circuit helps reduce the noise and number of poles within the output voltage, leading to a better phase margin. The section below provides an analysis of both the parallel and series RC circuits.

3.4.1 Parallel RC

The time constant of the parallel RC circuit can be expressed by Equation 3.2 [8]. When the circuit is open, the impedance of the capacitor is large. Likewise, when the circuit is shorted, the impedance of the inductor is zero. Instead of a voltage gain, a current gain is generated by a parallel RC circuit, creating an opposite reaction of maximizing impedance at resonant frequency.

$$\tau = RC \tag{3.2}$$

where

τ is the time constant

R is the resistance

C is the capacitance

3.4.2 Series RC

When a resistor and a capacitor are placed in series, the capacitor acts as an energy storing medium. The resistor, which is connected in series with the capacitor, will determine the charging and discharging states of the capacitor. Equation 3.2 distinguishes

the charging and discharging speeds of the circuit when a larger resistor or capacitor is used. Figure 3.2 shows the basic circuit diagram of an RC circuit.

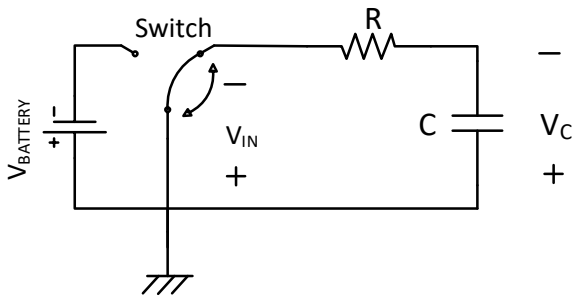

Figure 3.2 RC circuit

3.5 Summary

This chapter explained the function and characteristics of differential amplifiers. To summarize, the output voltage of a differential amplifier is dependent on the difference between the strength of two input signals. The input signals received can be in three different states, being in phase, 180° out of phase or out of phase at an angle other than 180°. Due to an increased number of poles from a two-stage differential amplifier, an RC circuit is added to help regulate the output voltage. This reduces the number of poles that occur from multi-stage amplifiers, resulting in an improved phase margin.

Chapter 4
Bandgap Voltage Reference

4.1 Introduction

Bandgap voltage references, also known as a BGR circuit, provide a DC voltage that is accurate and stable, insusceptible to changes in temperature and voltage. A BGR circuit is deemed independent of temperature because the temperature dependence of the voltage found in threshold voltage (V_{TH}) and base-emitter voltage (V_{BE}), when combined, is zero. Based upon the characteristics of a BJT, such that both the temperature dependence of V_{TH} and V_{BE} are linearized at room temperature, we can assume the same for a BGR circuit as it naturally adopts a BJT. Fundamentally, there is an increasing trend on smaller system power supplies, further amplifying the use of BGR circuits as they operate at voltages below 1.2 V.

4.2 Theory

According to Todorova et. al., the reason that a stable voltage supply is unaffected by temperature is dependent on the "principle of compensating the temperature drift of a bipolar transistor base-emitter voltage (V_{BE}) with the positive temperature coefficient of the thermal voltage (V_T)" [9]. Whenever a negative temperature coefficient from the V_{BE} occurs, a positive temperature coefficient is produced due to V_T, subtracting the negative change and eventually achieving temperature independence. This subtraction between negative and positive changes is the theory behind BGR circuits.

The mode of operation of BGR circuit is demonstrated in Figure 4.1 and expressed in Equation 4.1 below [10].

$$V_{REF} = V_{EB3} + K\Delta V_{EB} \tag{4.1}$$

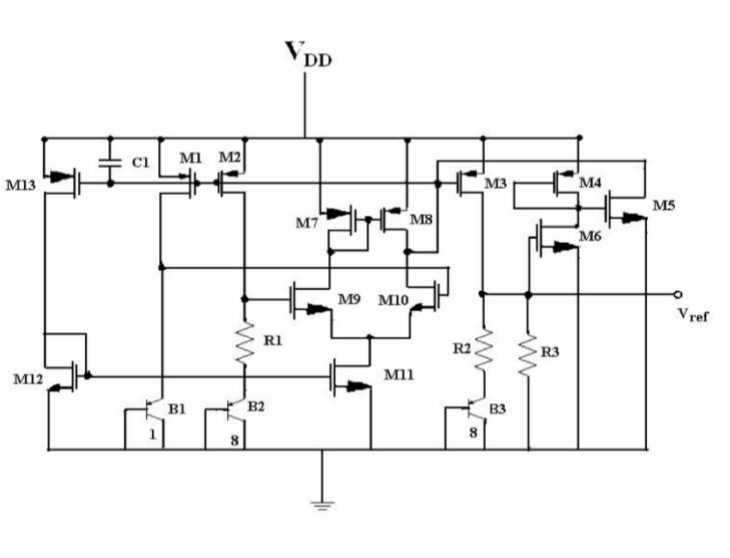

Figure 4.1 Bandgap reference circuit. Adapted from [10]

Assuming V_{REF} is the output voltage provided by the op-amp, V_{BE3} represents the negative change in temperature while $K\Delta V_{BE}$ represents the positive change, thus resulting in temperature independence.

4.3 Brokaw Bandgap Voltage Reference Circuit

Brokaw bandgap reference is most commonly used in IC designs, producing an output voltage of 1.25 V with minimal temperature dependence. The implementation of Brokaw BGR circuit cannot be realized directly in CMOS technology, as it requires the usage of bipolar transistors.

Similar to bandgap references that are temperature-independent, summing the negative and positive temperature coefficient produced by the two voltage sources nullifies the temperature dependence. The V_{BE} and V_T can also be used for temperature sensing.

Brokaw BGR circuit uses negative feedback generated from external sources such as an op-amp to constantly force current through two bipolar transistors with different emitter areas.

4.4 Noise and Stability

Using a BGR circuit in IC designs is popular due to its simplicity and the lack of zener diodes. The absence of zener diodes makes it an attractive option as the circuit structure eliminates the noise that is generated from those zener diodes as well. The noise found within voltage references is important to the system design, despite it being overlooked by many system designers as they assume voltage references make no contribution to system noise. When considering the implementation of a voltage reference, their behaviors during start-up and during transient loads are to be taken note of. Voltage references require time to power up, making it non-conventional to turn on, making a reading and turn off again instantaneously, despite its energy saving opportunities.

With that being said, BGR circuits are still a stable voltage reference design as it is implementable within systems that have a low power supply, usually below 5 V. Although it generates a fair drift and hysteresis, it has a downside of generating high noise at high power supply.

4.5 Summary

When designing portable IoT devices, low power usage and low voltage are factored into the design. Designs are constantly being shrunk, which consequently reduces the power supply voltage. Therefore, based on the analysis and theory above, a BGR circuit

is highly compatible in low power supply voltage designs for implementation due to its low voltage requirement, long term stability and temperature independence.

Chapter 5
Low Drop-Out Voltage Regulator

5.1 Introduction

Low drop-out (LDO) voltage regulators are types of circuitry that provide stable voltage supplies for integrated circuit blocks, especially power management integrated circuits. An LDO is made up of a Brokaw bandgap voltage reference (BGR), error amplifier and pass elements. The rule of thumb for an LDO's performance is that the power supply rejection ratio (PSRR) is inversely proportional to load current. The power efficiency of an LDO increases when the power dissipation from the error operation is reduced. LDOs are gaining popularity due to the demands of smaller sizes for on-chip load capacitances. The overall chip layout area is constantly being minimized as well, as their demand is slowly increasing.

5.2 Low Drop-Out Structure

LDOs require smaller voltage differences between their input and output for proper input voltage regulation. Inside of the LDO also contains a resistor feedback network, providing scaled output voltage equivalent to the reference voltage whenever the output is of nominal voltage. Figure 5.1 shows the basic circuit diagram of a linear voltage regulator.

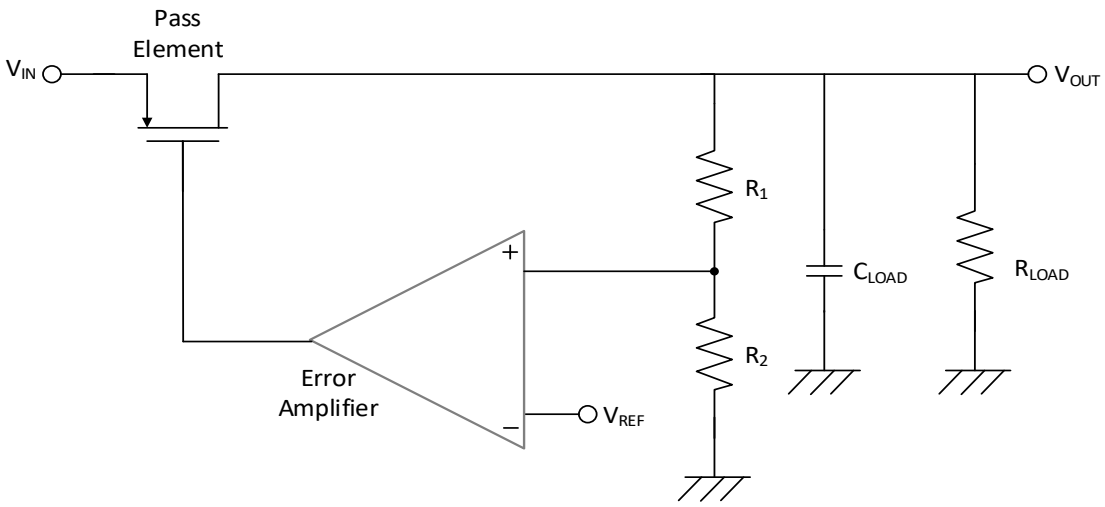

Figure 5.1 Basic linear voltage regulator.

As seen in the diagram, the error amplifier compares the reference voltage with the voltage from the voltage divider, amplifying its difference and regulating the output voltage level.

5.2.1 Voltage Reference

Voltage references, specifically BGR, provide the starting point for the error amplifier and consequently the entire LDO. BGR possesses the characteristics of temperature independence and accuracy, making it favorable for implementation in linear regulator design. Also, the drawbacks of the BGR circuits, such as the high output noise and negative effect of PSRR, can be rectified and countered with RC filters easily.

5.2.2 Error Amplifier

Selecting the proper error amplifier topology is very crucial, as there are many other constraints that are related to external constraints from other devices such as the pass element and buffer. Balancing the performance and current consumption in error amplifier is to be considered when designing an error amplifier. The error amplifier

should be of a simple design to prevent high current consumption, while still maintaining accuracy and PSRR, providing a stable system. The error amplifier adjusts the resistance of the pass element based on a comparison between the reference voltage and output voltage from the voltage divider. This resistance reduces the error signal to a near zero value.

5.2.3 Feedback Network

The V_{REF} provided by the error amplifier is used for comparison to scale the V_{OUT}. With V_{VREF} being a variable, the output voltage can only be changed through the ratio of R_2/R_1. Low current consumption makes it important to scale the resistor values such that they correspond with the current consumption of the error amplifier.

The alternative approach of using a MOSFET divider, as opposed to the conventional resistive method described above, can be used if area is a large factor in the design. The reason for this design to be used is that it has a smaller area than that of the resistive method, as it uses MOS transistors instead of resistors. However, as Cermák (2016) described, "the parasitic capacitance of transistors increases and can impose a slew rate reduction," negatively influencing the error amplifier capabilities on the output voltage [11].

5.2.4 Pass Element

Pass element is a one-way medium between the input and the load for sending large currents. It is powered by the error amplifier through a feedback loop.

The operating region of the pass element depends on the drop-out voltage. The pass element operates in the linear region when the drop-out voltage is larger than the input

voltage. The open-loop gain and accuracy of the system are affected when the pass element operates in linear region. Due to the nature of PMOS transistor, the gate voltage is inversely proportional to the load current, causing a decrease towards ground while the load current increases. The drop-out voltage for PMOS is defined in Equation 5.1 [11].

$$V_{DROP-OUT,PMOS} = V_{OUT} + V_{DSAT,PASS} \tag{5.1}$$

In order to prevent the pass element from operating in a linear region, a larger pass device or an increased input voltage is necessary. For that, the PMOS pass element is not to be used for very low voltage applications.

On the other hand, the NMOS pass element is beneficial for low voltage applications, as it has a source follower configuration. This results in a lower output resistance due to the output node being located at the source of the transistor. Ergo, this should lead to an improvement in stability, however the stability also depends on the output capacitor size.

$$V_{DROP-OUT,NMOS} = V_{OUT} + V_{GS,PASS} \tag{5.2}$$

Equation 5.2 above describes how the minimum required voltage of the NMOS is based on the voltage V_{GS}, which is required to be higher than the output voltage [11].

5.2.5 Output Capacitor

The function of the output capacitor (also known as off-chip capacitor or load capacitor) is to ensure that current is being delivered instantaneously to the load, during load transients, while waiting for the error amplifier to catch up. It also contributes to the stability distress throughout the system by producing a pole at low frequency and a zero at high frequency.

Effective series resistance or equivalent series resistance (ESR) of the capacitor is associated with the zero produced at high frequency. This ESR performs like a resistor in series with a capacitor. It controls the current flow from the capacitor to the load; thereby affecting the overshoots and stability of the system.

5.3 Types of LDO

Typically, a conventional LDO is made up of a voltage reference, error amplifier, feedback network, pass element and output capacitor. In the past decade, the demand of yielding cheaper LDOs with improved reliability has drastically increased. For that, the recent trends show the elimination the off-chip capacitor from the LDOs, as it is cost-effective. The two aforementioned LDOs — conventional LDO and capacitor-less LDO, are discussed in detail in the sections below.

5.3.1 Conventional LDO

The standard conventional LDO requires off-chip output capacitors. This is because their topology has good stability and reasonable PSRR. The variations in capacitor materials could affect the performance of the LDO applications in full strength. The most commonly used off-chip capacitors are made of ceramic. They are typically cheap and have a small footprint size. However, the use of these external capacitors on the LDO are usually non-ideal and cause adverse effects, such as effective series resistance (ESR) and effective series inductance (ESL). This consequently prevents the capacitor from achieving peak performance values. Likewise, choosing the wrong external load capacitor can bring adverse effects to the overall circuit, for instance stability issues,

power dissipation and extra noise. These effects will negatively impact the battery health and product life.

5.3.2 Capacitor-less LDO

A capacitor-less LDO, on the contrary, is an LDO that is designed without the need of an off-chip load capacitor. The alluring essence of this design is that it reduces the chip and printed circuit board (PCB) die area, thereby lowering the bill of materials (BOM) costs. The cause of failure also decreases, as there is one less component to be tapeout or soldered. The elimination of off-chip capacitor will get rid of the non-ideality factor, ESR.

As described, conventional LDOs are extremely reliant on the off-chip capacitor's capabilities. Unlike the conventional LDOs topology that consist of an output dominant pole, the capacitor-less LDOs have an internal dominant pole that very based on the load current. Capacitor-less LDO design faces serious design difficulty in providing a stable LDO. Consequently, a significant tradeoff can be seen in the transient performance and PSRR.

5.4 Drop-Out Voltage

Drop-out voltage is measured based on the output node of the voltage regulator subtracted with its input counterpart. Drop-out voltage occurs when the circuit is unable to regulate the decreasing the input voltage. The transistors inside the regulator are set to saturation for the circuit to be responsive to output voltage changes. Thus, when the transistors fall out of saturation and into triode, the output voltage will begin to diverge from the specified output voltage, affecting the system gain.

5.5 Efficiency

The efficiency of an LDO voltage regulator is constrained by both the factor of the drop-out voltage and the quiescent current. The quiescent current represents the difference of the input and output voltage. Hence, achieving the highest possible efficiency is possible by lowering the dropout voltage and quiescent current to a minimum. The low drop-out voltage reduces the power dissipation, making it the key factor on the efficiency of the voltage regulator.

5.6 Transient Response

The overall transient response of the LDO is determined by the stability and crossover frequency. Crossover frequency enhances the PSRR when it is high; however, it also increases the output noise. Likewise, low crossover frequency decreases the output noise, but also diminish the PSRR at the same time. The crossover frequency, when increased, shortens the time of the transient condition. The dominant pole found within an LDO is usually formed with the output capacitor and its respective ESR, meaning that the output capacitor will decrease the intensity of the transient response while increasing the settling time. The stability is measured by the gain and phase margins of the loop response. Stable LDOs create a smooth transient, while its unstable counterpart generates fluctuating transient response. Only the output capacitor can be tuned to ensure stability, as the internal compensation of the LDO is fixed. Since this can be difficult to achieve, the manufacturers usually provide constraints of the capacitance and the ESR to help with LDO design.

5.7 Power Supply Rejection Ratio

Input voltage variation causes fluctuation in the regulated output voltage. PSRR is used to prevent the unfavored fluctuation. The equation for PSRR calculation is shown in Equation 5.3 [11].

$$PSRR(\omega) = 20\log_{10}\frac{A(\omega)}{A_{SUPPLY}(\omega)} \tag{5.3}$$

where

PSRR is the power supply rejection ratio

$A(\omega)$ is the circuit gain

$A_{SUPPLY}(\omega)$ is the power supply gain

5.8 Summary

The anatomy of an LDO consists of a reference circuit, a feedback network, an error amplifier and a pass element. LDOs are constantly in demand due to their increasing usage found within many applications in today's market. The stability and low noise produced by LDOs make it appealing in the design of mobile devices such as cellphones and laptops. This appealing characteristic is due to the simplicity in the design of the LDO. Therefore, the architecture and design of the LDO satisfies the requirements of the current and future applications.

Chapter 6
Circuit Implementation and Schematic Design

6.1 Introduction

Chapter 6 will be the implementation and simulation of the LDO voltage regulator in the Cadence ADE using the TSMC 65-nm technology library. The results from the simulations performed will also be presented in this chapter. The design of the LDO voltage regulator is divided into voltage reference, error amplifier, feedback network and pass element. The voltage reference is implemented using a Brokaw BGR circuit with a two-stage common source differential amplifier. The simulation results will highlight the factors that define the performance of the LDO voltage regulator, such as gain, maximum load current and LDO die area.

6.2 Design Considerations

Tables 1, 2 and 3 below describe the design specifications for differential amplifier, BGR circuit and LDO voltage regulator, respectively. A two-staged common source operational amplifier was used for its simplicity and efficiency. The Brokaw BGR circuit was selected as it is usually found in IC design. The LDO voltage regulator was carefully designed with consideration towards stability and die size.

Table 1. Differential Amplifier Design Specifications

Parameters	**Specifications**
Power Supply	$1 - 2.5\ V$
Gain	$60\ dB$
Phase	$60°$

Table 2. Bandgap Voltage Reference Design Specifications

Parameters	**Specifications**
Power Supply	$1 - 2.5\ V$
Temperature Coefficient	$< 15\ ppm/℃$
Output Voltage	$1\ V$

Table 3. Low Drop-Out Voltage Regulator Design Specifications

Parameters	**Specifications**
Drop-Out Voltage	$1 - 2.5\ V$
Maximum Load Current	$< 15\ ppm/℃$
On-Chip Capacitor	$None$
PSRR	$> -20\ dB$
Error Percentage	<1%

6.3 Proposed Designs

The proposed designs for differential amplifier, BGR and LDO voltage regulator are discussed in depth in the following sub-sections.

6.3.1 Differential Amplifier

The high gain op-amp was used as the differential amplifier for the BGR circuit, balancing the current and ensuring stability of the voltage source to the LDO. Figure 6.1 shows the proposed two-stage common source op-amp.

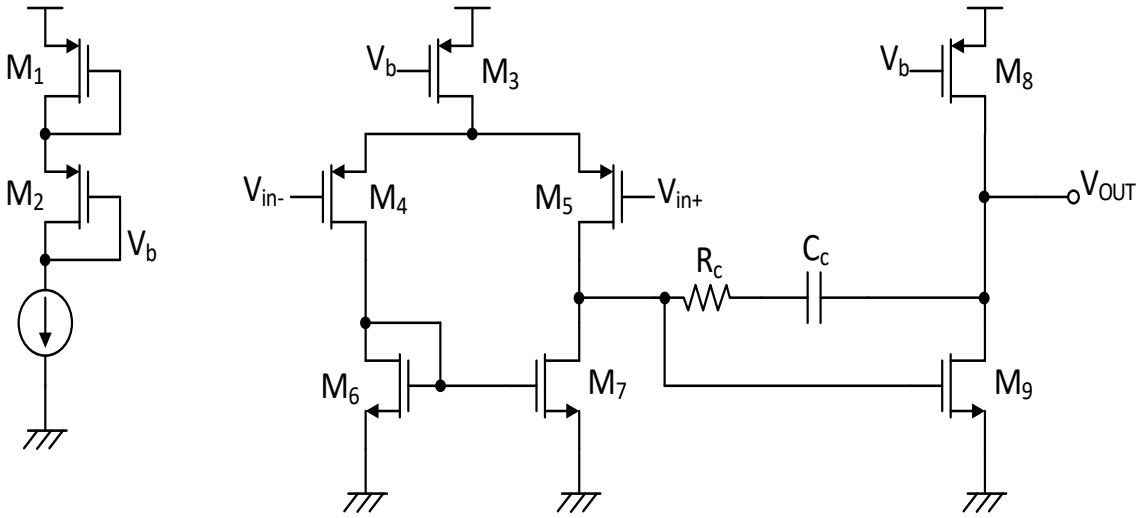

Figure 6.1 Proposed two-stage common source op-amp

Instead of using a complex folded cascaded op-amp like in previous works, a simple common source op-amp was the preferred choice as its die area is smaller and is sufficient for the current LDO design specifications. Though increasing stages lead to an increased gain, it also increases the number of poles and causes significant drawbacks. The common source op-amp for this work is two-stage. It is of simple design and spans less chip area inside the circuit.

6.3.2 Bandgap Voltage Reference

The BGR circuit is a Brokaw cell designed with the two-stage common source op-amp, which results in an estimate of 60 dB gain, thereby consistently providing an average voltage output of 1 V to the LDO voltage regulator. As the frequency approaches 100 MHz, poles begin to develop. In order to compensate the presence of poles, an RC

compensation circuit is added to the BGR circuit. The proposed BGR circuit is presented in Figure 6.2.

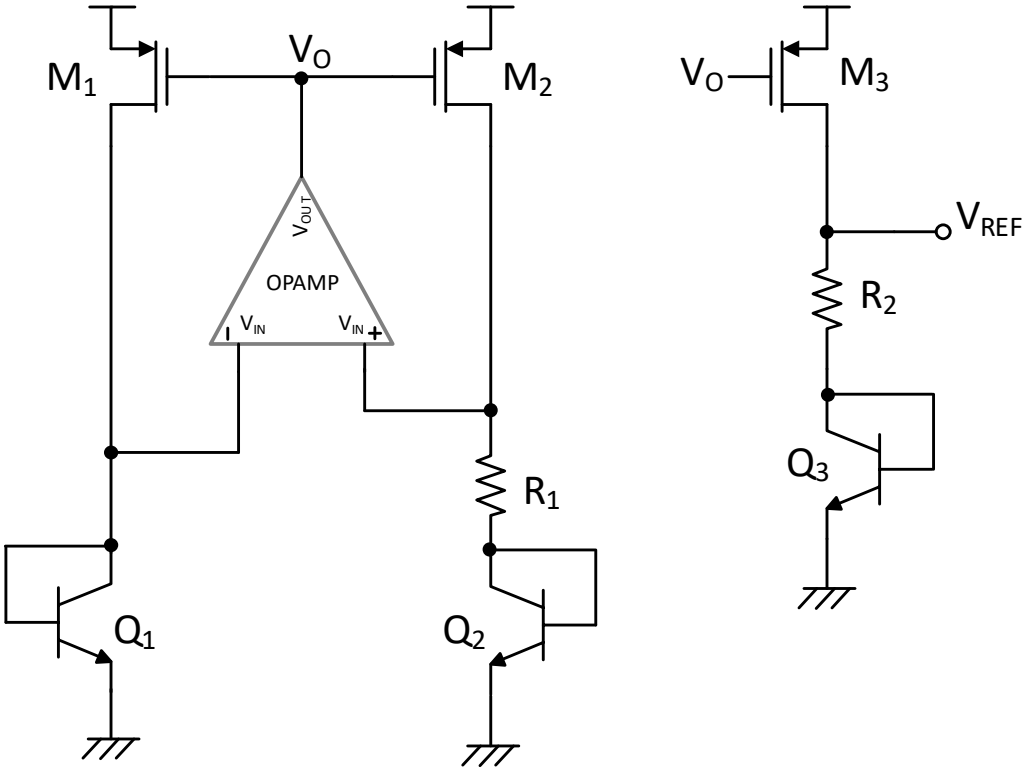

Figure 6.2 Proposed BGR circuit

The temperature coefficient is measured in Equation 6.1 below [12]. The range of the temperature coefficient is from -40 ℃ to 125 ℃, as it is compliant with military standards. This range is to ensure stability throughout the BGR circuit.

$$TC = \frac{(V_{REF(MAX)} - V_{REF(MIN)})}{V_{REF}} \times \frac{10^6}{T_{MAX} - T_{MIN}} \quad (6.1)$$

6.3.3 Low Drop-Out Voltage Regulator

The LDO voltage regulator is designed to be capacitor-less, a common topology for IoT applications and power management due to its Always-On Domain. Because of its Always-On Domain, there is no need for a capacitor to reduce the noise present in the voltage regulator [13]. The current is injected into the second stage of the amplifier using a replica circuit. The proposed LDO voltage regulator is presented in Figure 6.3.

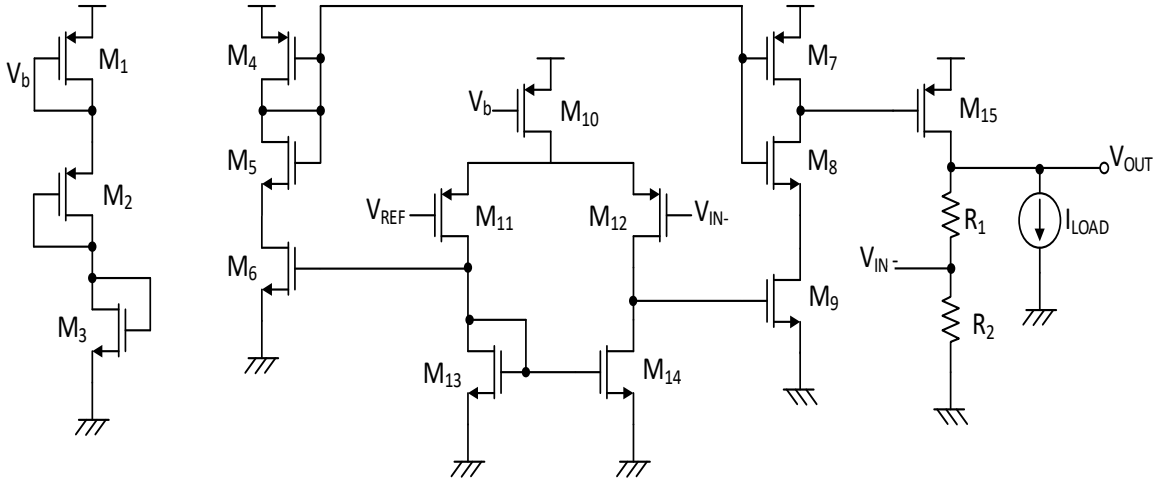

Figure 6.3 Proposed capacitor-less LDO

The feedback voltage divider is designed with respect to Equation 6.2 [11]. The ratio of the feedback β_{FB} determines the division of the output voltage. This division is performed prior to comparing with the reference voltage.

$$\beta_{FB} = \frac{V_FB}{V_O} = \frac{R_{FB2}}{R_{FB1}+R_{FB2}} \tag{6.2}$$

where

β_{FB} is the feedback factor

V_FB is the feedback voltage

V_O is the output voltage

R_{FB1} is the feedback resistance of R_1

R_{FB2} is the feedback resistance of R_2

The pass element is designed with respect to Equation 6.3 stated below [11].

$$I_D = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2 \tag{6.3}$$

where

I_D is the drain current

μC_{ox} is the transconductance parameter

$\frac{W}{L}$ is the channel width over channel length ratio

V_{GS} is the gate to source voltage

V_{TH} is the threshold voltage

To prevent the pass element from entering triode region, the pass element is scaled to increase the W/L ratio, according to the worst corner in simulation [11]. However, this ratio should not be too high, as too large of a gate area will worsen the system response and stability due to the increased capacitance.

6.4 Simulation Results

The simulated graphs for differential amplifier, BGR and LDO voltage regulator are presented in the following sub-sections.

6.4.1 Schematic Designs

The schematic design presented in Figure 6.4 depicts the schematics of the differential amplifier, BGR circuit and LDO voltage regulator when combined into one large circuit.

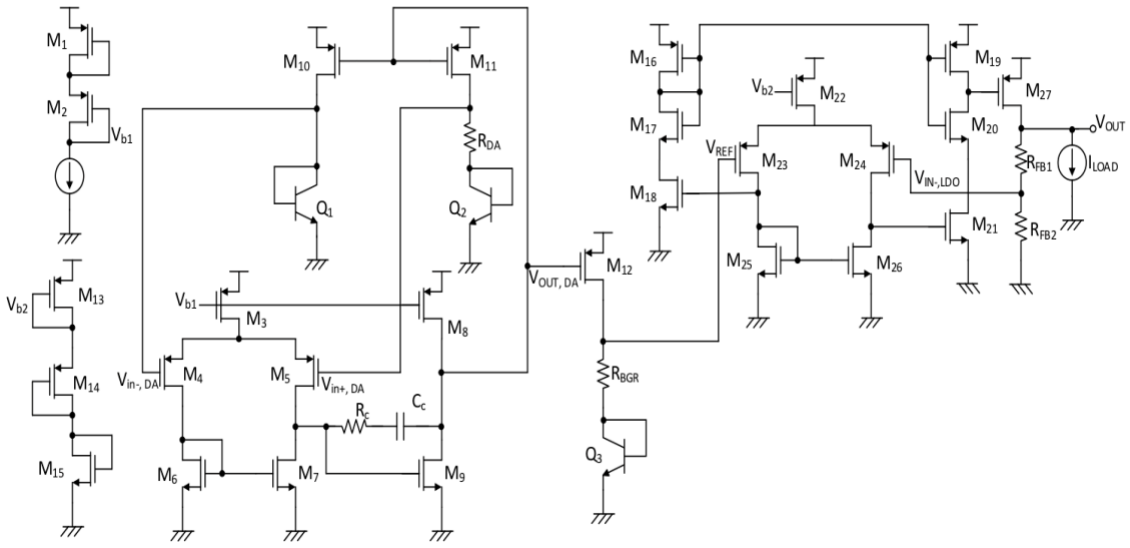

Figure 6.4 Proposed capacitor-less LDO, differential amplifier and BGR

6.4.2 Differential Amplifier

The common source op-amp used in the BGR circuit achieved a gain of 60 dB with a power supply of 2.5 V, using TSMC 65-nm technology, as shown in Figure 6.5. When compared to previous works, the performance of this op-amp design is significantly better than a previous common source op-amp design and a folded cascaded op-amp design.

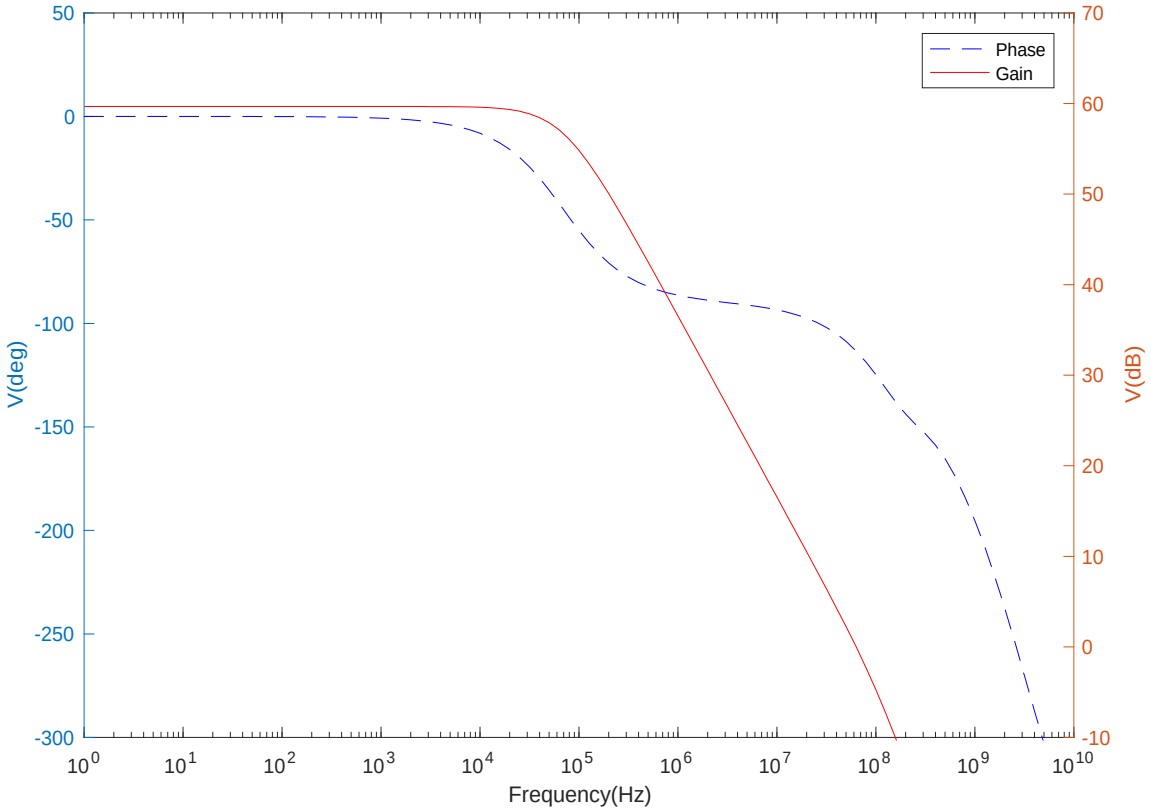

Figure 6.5 Gain and phase of op-amp

A folded cascaded op-amp is used to provide a better gain and phase margin. The proposed common source op-amp achieved a phase margin of 66.72°, which is higher than the folded cascaded op-amp from previous works with a value of 62.3° [14]. Although the aforementioned folded cascaded op-amp has a much higher gain of above 80 dB, the proposed simple two-stage common source op-amp is able to yield a gain of 60 dB, achieving a consistent 1 V average output voltage. Furthermore, the proposed common source op-amp is far simpler in design, as compared to the complex folded cascaded op-amp design.

Subsequently, the proposed common source op-amp is chosen for this work, as it provides a consistent average output voltage using only a simple design.

6.4.3 Bandgap Voltage Reference

The design specifications listed in Table 2 specified the BGR circuit to be less than 15 ppm/℃, in order to create a stable BGR circuit with a high PSRR. When performing within military standards of the temperature coefficient, the Brokaw BGR circuit achieved an average temperature coefficient of 13.34 ppm/℃. This the proposed Brokaw BGR circuit has met the standards of the design objectives. The DC response of the BGR circuit is demonstrated in Figure 6.6.

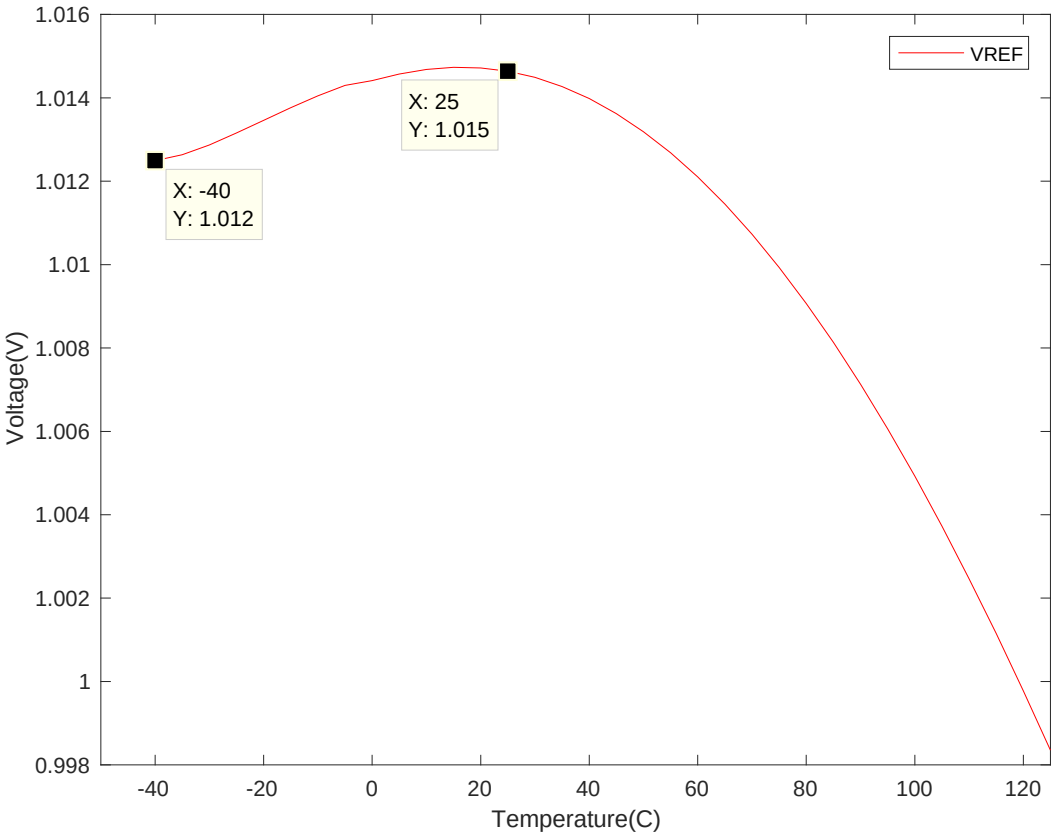

Figure 6.6 DC response of BGR circuit

6.4.4 Low Drop-Out Voltage Regulator

When given a power supply of 2.5 V, the LDO voltage regulator achieved a voltage output of 2.032 V, creating a low drop-out voltage of 468 mV. The maximum load current of 200 mA achieved by the proposed LDO voltage regulator is much higher than the previous works [15][16][17]. This includes a 200% increase from the nearest previous work [16]. Although this maximum current is manageable by the LDO voltage regulator, this requires in a large pass element and feedback network, resulting in a larger chip layout area. The chip layout area of the LDO voltage regulator, reached the size of 0.0317 mm^2, twice the size of the compared previous work's area of 0.069 mm^2 [15].

Figure 6.7 describes the transient response of the proposed LDO with BGR circuit. When the BGR circuit is connected to the LDO, the output voltage of the BGR (labeled as V_{REF} in the schematic design in Figure 6.2) will feed into the input of the LDO (labeled as V_{REF} in the schematic design in Figure 6.3). This reference voltage is demonstrated in Figure 6.7 as V_{in+}, with the average maximum peak voltage of 1 V and average minimum peak voltage of -1 V. The feedback input voltage, identified as V_{in-} in Figure 6.7, acts as the feedback input voltage at the feedback network that is made up of R_1 and R_2. Although this feedback voltage is closely in sync with the reference voltage provided by the BGR circuit, the average maximum and minimum peak voltages are more ideal. Instead of having an average minimum peak voltage of -1 V, the average minimum peak voltage is slightly passing -1 V. The average maximum and minimum output voltages, demonstrated as V_{out}, are seen at 2 V and -2.1 V, respectively, in accordance to the V_{in+} and V_{in-}. This has further proven that the LDO and BGR circuit are

working, as the feedback input voltage is able to tune the average maximum and minimum peak voltages of the provided reference voltage to the ideal values and the output voltage is near two times the value of the input voltage.

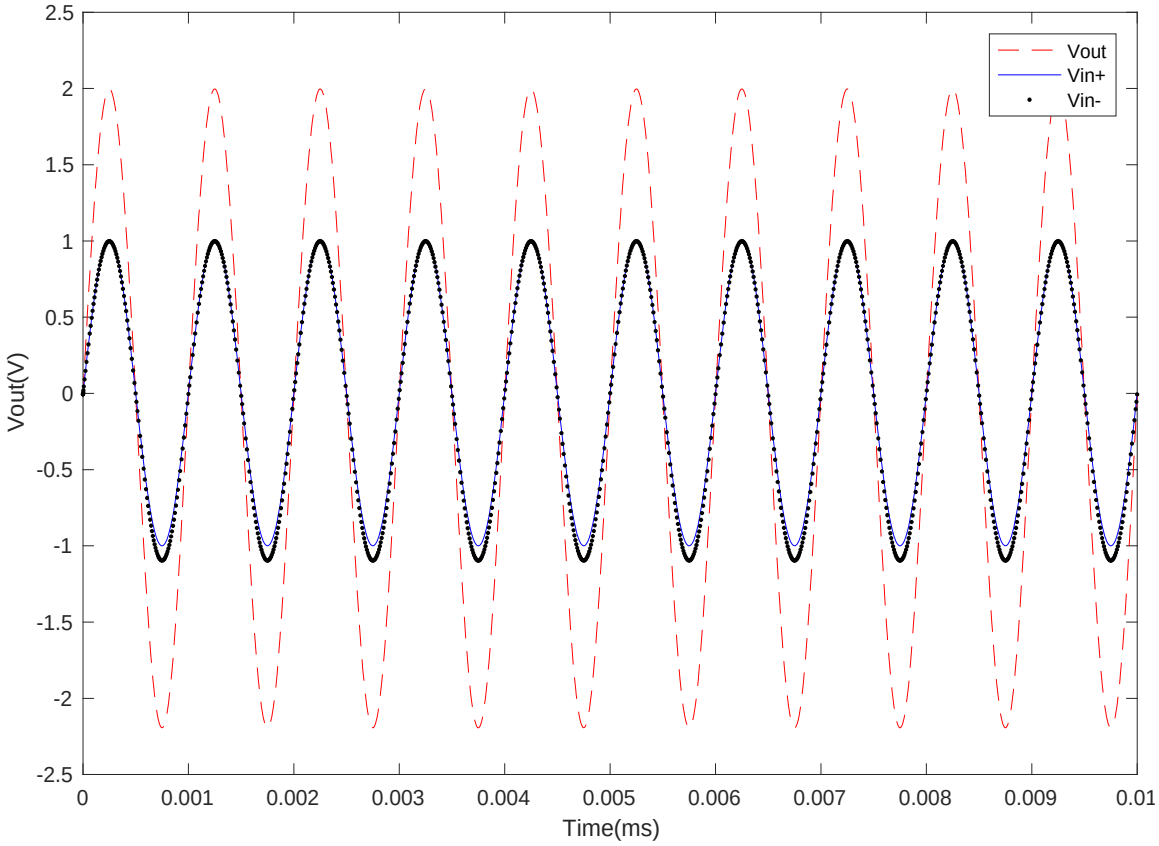

Figure 6.7 Transient response of the proposed LDO with BGR circuit

Figure 6.8 describes the DC analysis of the proposed LDO with BGR circuit. As the LDO voltage regulator approaches the maximum load current of 200 mA, the voltage output dropped from 2.032 V to 2.027 V, achieving an error percentage of 0.246%, meeting the design specifications of a below 1% error percentage. The error percentage is calculated with the formula as expressed in Equation 6.4.

$$Error\ Percentage = \frac{V_{OUT1} - V_{OUT2}}{V_{OUT1}} \times 100\% \quad (6.4)$$

With the error percentage of a mere 0.246%, this has once again proven that the LDO is functioning in accordance with the BGR circuit.

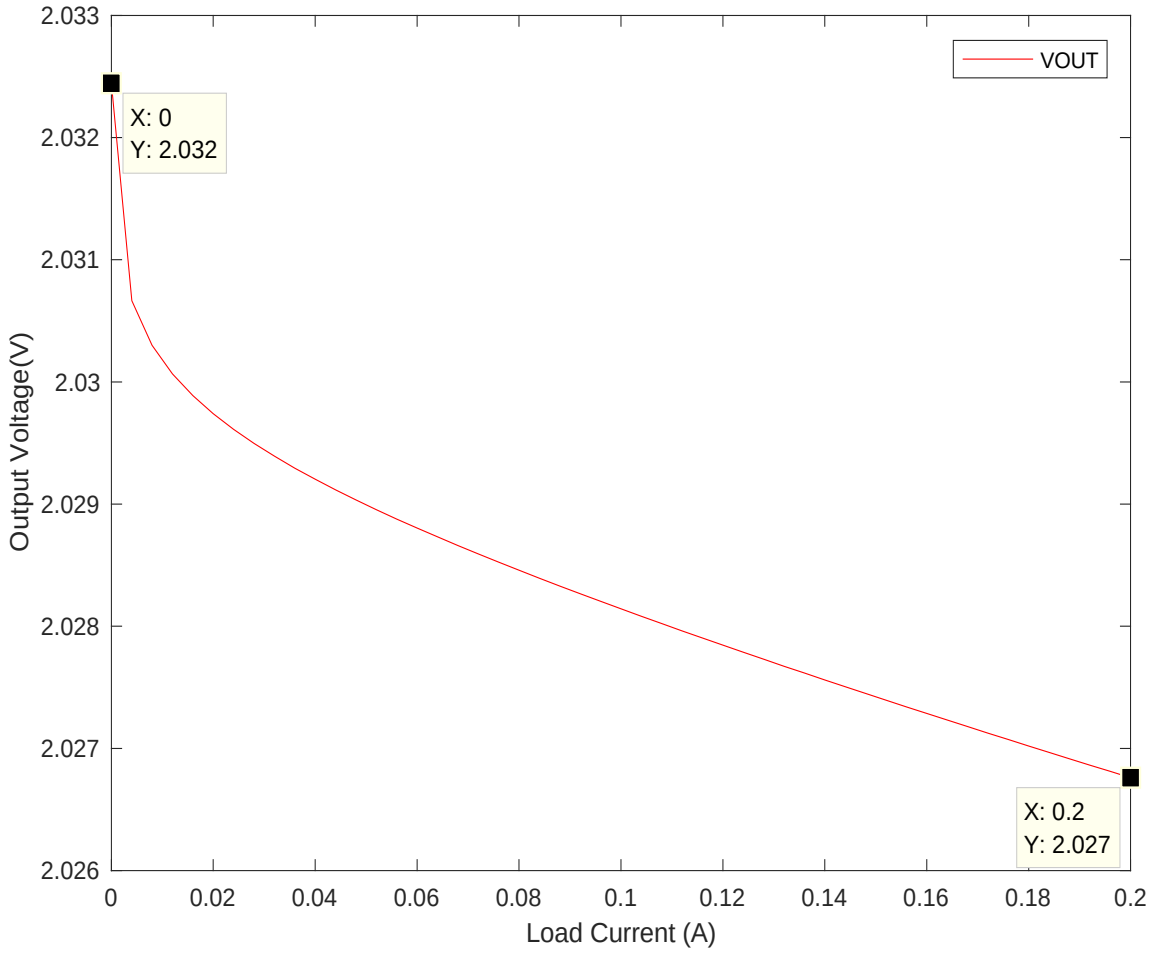

Figure 6.8 DC analysis of the proposed LDO with BGR circuit

Figure 6.9 describes the PSRR of the proposed LDO with BGR circuit. The motivation for this design proposal is to minimize the chip size while still providing a high load current powered by a realistic BGR with a reference voltage of 1 V, maintaining a regular PSRR value. Under the design consideration in section 6.2, the ideal PSRR is fixed at -20 dB and above. In Figure 6.9, the PSRR of the LDO is seen at -21.47 dB for both 10 KHz and 100 KHz. Although the design did not realize a very high PSRR value, it meets the design consideration.

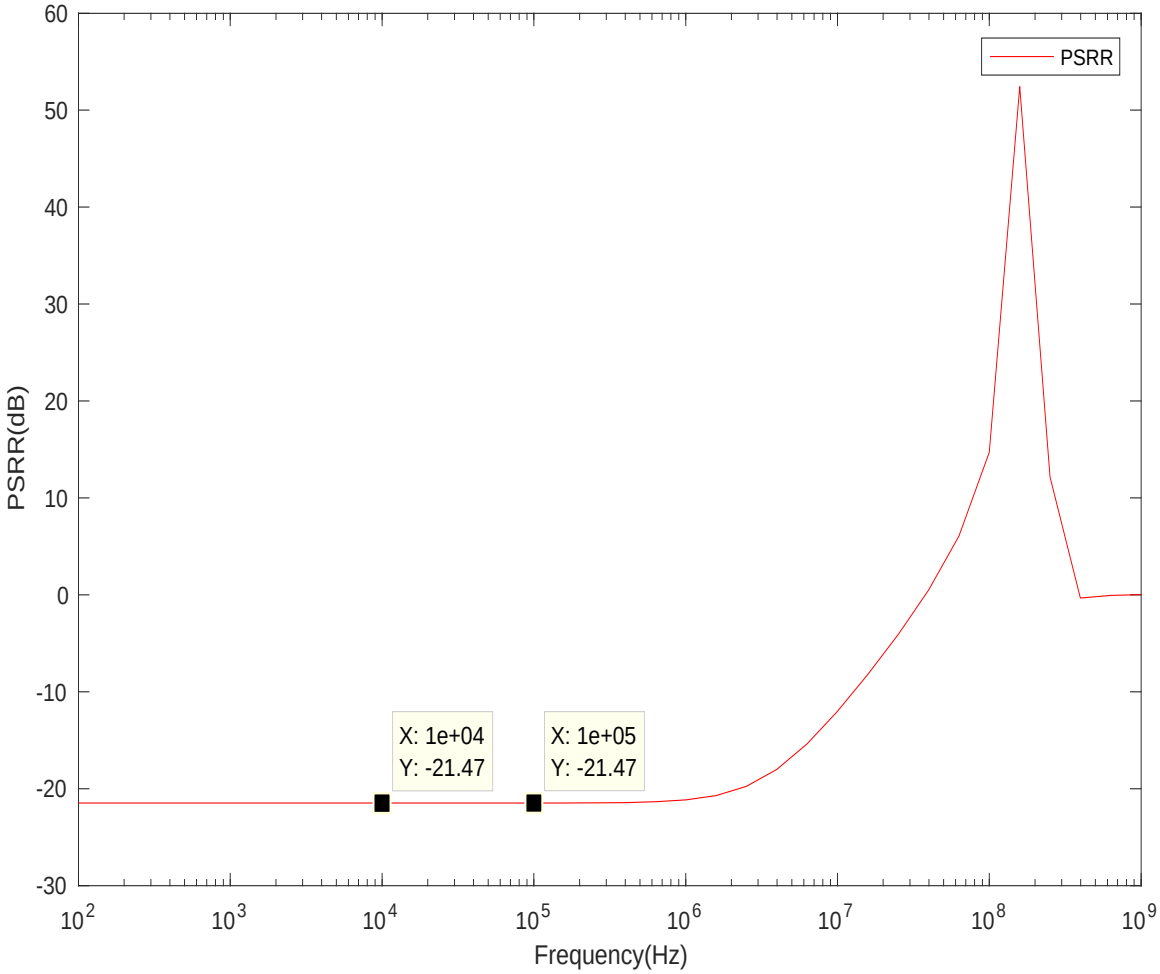

Figure 6.9 PSRR of the proposed LDO with BGR circuit

6.5 Layout

The layout area of the design, including BGR and LDO, has an area of 0.051 mm^2. The design was tested and verified using Design Rule Check (DRC) and Layout Versus Schematic (LVS) tests found in Cadence Virtuoso Layout Suite XL. The proposed BGR circuit is presented in Figure 6.10.

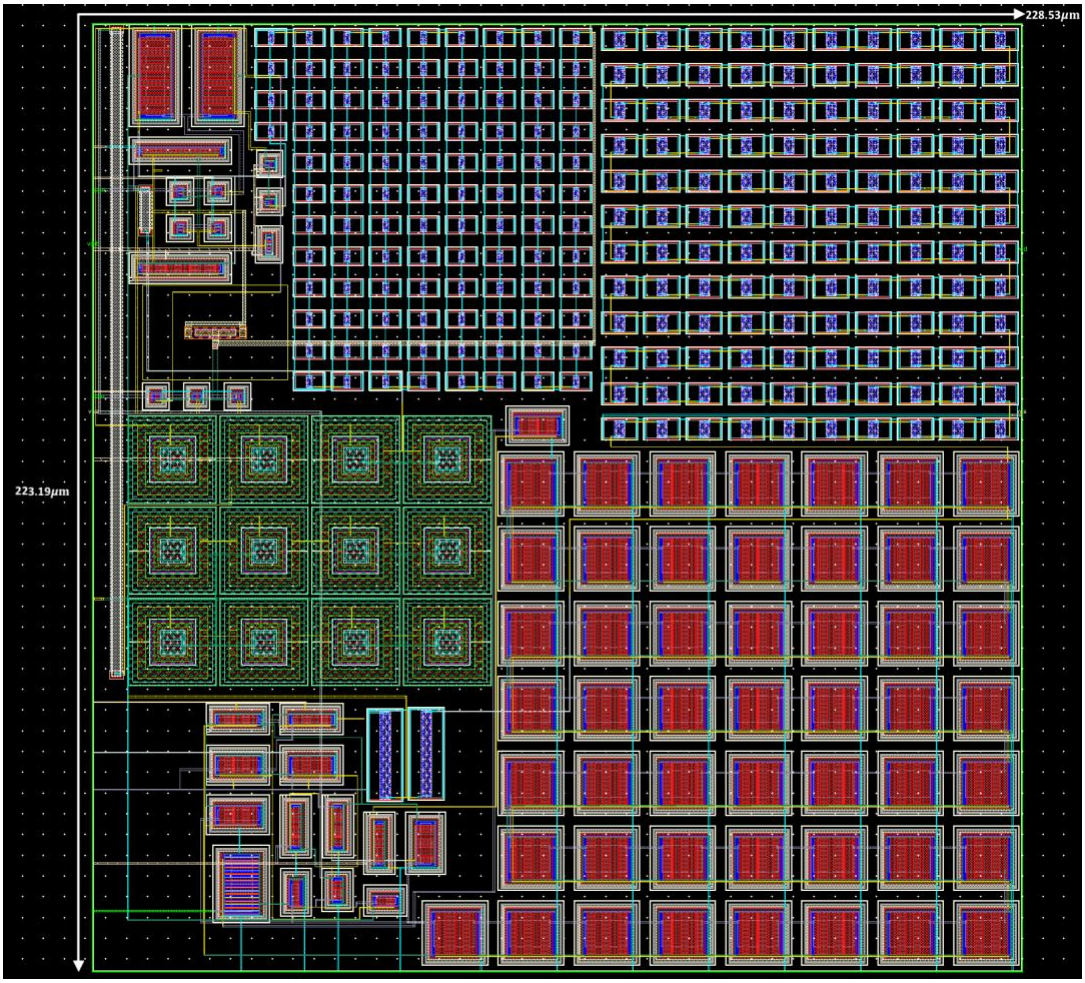

Figure 6.10 Proposed LDO and BGR full chip layout

6.6 Performance Summary

The comparison of the op-amp design against previous works is shown in Table 4, while the comparison of LDO voltage regulators against previous works is shown in Table 5. Among all the works shown in both tables, the proposed design used the smallest technology of 65-nm. The op-amp met the sufficient standards of providing a 1 V stable average voltage output, without needing a higher gain. The LDO regulator has a higher maximum load current than previous works, achieving a smaller load die area as well.

Table 4. The Performance of Op-Amp Design

Op-Amp Type	**[14]**	**[18]**	**This Work**
	Folded Cascaded	**Common Source**	**Common Source**
Technology	0.18-μm	0.35-μm	65-nm
Power Supply	1.8 V	3.3 V	2.5 V
Gain	>80 dB	78 dB	~60 dB
Phase Margin	62.3°	63.9°	66.72°
GBW	1.437 GHz	5.82 MHz	3.79 GHz

Table 5. Performance Comparison Table

		[15]	**[16]**	**[17]**	**This Work**
Technology (nm)		180	350	350	65
V_{OUT} (V)		1.5	2.8	2.8	2.03
$V_{DROP-OUT}$(mV)		300	200	500	470
Max. I_{LOAD} (mA)		25	100	50	200
On-chip Capacitor		100pF	Cap-Less	Cap-Less	Cap-Less
PSRR (dB)	10 KHz	-62	-56	N/A	-21.47
	100 KHz	-62	-56	-45	-21.47
LDO Die Area (mm^2)		0.069	N/A	N/A	0.0317

Chapter 7
Conclusion

7.1 Contribution

The LDO voltage regulator design in this thesis uses a 65-nm technology, a much more common layout size found within designs. In comparison to other similar works, the size is 36% smaller than the next smallest technology used.

The simulation performed on said LDO voltage regulator was designed to be in a practical environment because of the use of a designed BGR to provide a stable yet realistic output voltage. Because of this simulation, the results achieved from this design are more realistic than other comparable works. The design in this paper also achieved a 200 mA maximum current load, a 100% increase from the closest results from comparable works. The die size of the design was 0.0317 mm^2, which is much smaller than other known die sizes.

In conclusion, the LDO voltage regulator design is well suited for biomedical IoT applications, mostly due to its 200 mA maximum current load as well as its comparatively small die size.

7.2 Future Work

The proposed project contains four major segments. Each segment has its own distinct feature that is applicable to many advanced applications, especially to the IoT technology in SoC and medical fields. This work proposed the capacitor-less LDO with high load current and stable reference voltage, which is cost efficient in medical device development. The purpose of the work is aiming at publishing at least two papers in 2018, and the remaining work and results could be served as valuable references for

developing next generation's products. This proposal could also coordinate industrial projects' cost-efficient medical devices, which target lower income or budget consumers. This work can be further published in IEEE journals or electronic letters, and even file for patents.

7.3 Summary

The thesis explained the concepts and applications of the LDO voltage regulator in IoT technology in SoC and medical fields. This work is broken down into chapters explaining the components of the LDO voltage regulator such as the op-amp, BGR and finally the LDO. This proposed capacitor-less LDO with high load current and stable reference voltage achieved a maximum load current of 200 mA, while maintaining a smaller die size.

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