CRITERIA FOR THE DESIGN OF "FAST," "SAFE" ASYNCHRONOUS SEQUENTIAL FLUIDIC CIRCUITS

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CHAPTER I

INTRODUCTION

The recent invention of pure fluid or fluidic switching devices created a new perspective in the fluid controls area with regard to the possible complexity and operational speed of future fluid control systems. These fluidic components combine no moving parts operation, high density packaging and sufficient response times to offer fluid circuit designers the appropriate hardware required to construct highly complex fluid-operated control systems. The need for this type of system exists since hydraulic system designers, particularly in the mobile equipment industry, have conceptions and designs for complex fluid-operated machines which must be partially or completely controlled automatically.

Automatic control for these machines requires the controlled performance of individual machine tasks together with proper sequencing of the individual tasks to accomplish an over-all job. This type of control requires a machine to possess both individual and master control ability. Digital switching or sequential circuits implemented with fluidic components offer the fluid circuit designer a way of providing over-all machine operation sequencing and in some instances a method of performing the smaller individual tasks. Thus, the purpose of this dissertation will be to develop and suggest advantageous ways of designing

digital fluid control circuits by incorporating sequential circuit theory and fluidic hardware.

Sequential circuit control of machine operation can be represented schematically as shown in Figure 1. The sequential control system coordinates the activities of the individual power systems required to perform given tasks. Input signals to the sequential control system are derived from meaningful environmental conditions which the power systems encounters during the execution of a task. In turn, the sequential system emits output signals to the power systems to properly control their respective responses to particular encountered environmental situations. For hydraulic circuit application, the power control systems could be servo-systems, on-off power valves, or other sequential control systems.

Sequential circuits can be divided into two types: synchronous and asynchronous. The synchronous sequential circuit must be externally timed to produce correct circuit operation. An asynchronous circuit is designed to be internally self-timed. This self-timing feature coupled with faster over-all response time than the synchronous circuit make the asynchronous circuit desirable for fluidic circuit applications. The faster response time of the asynchronous circuit is important in fluidic circuit implementations since fluidic component reaction times, although somewhat faster than conventional "moving parts" fluid hardware, are very slow in comparison with electronic computing elements. Because of the advantages offered by the asynchronous sequential circuit for fluidic circuit design, only this circuit type will be considered in the subsequent discussion.

An asynchronous sequential circuit can always be implemented as a

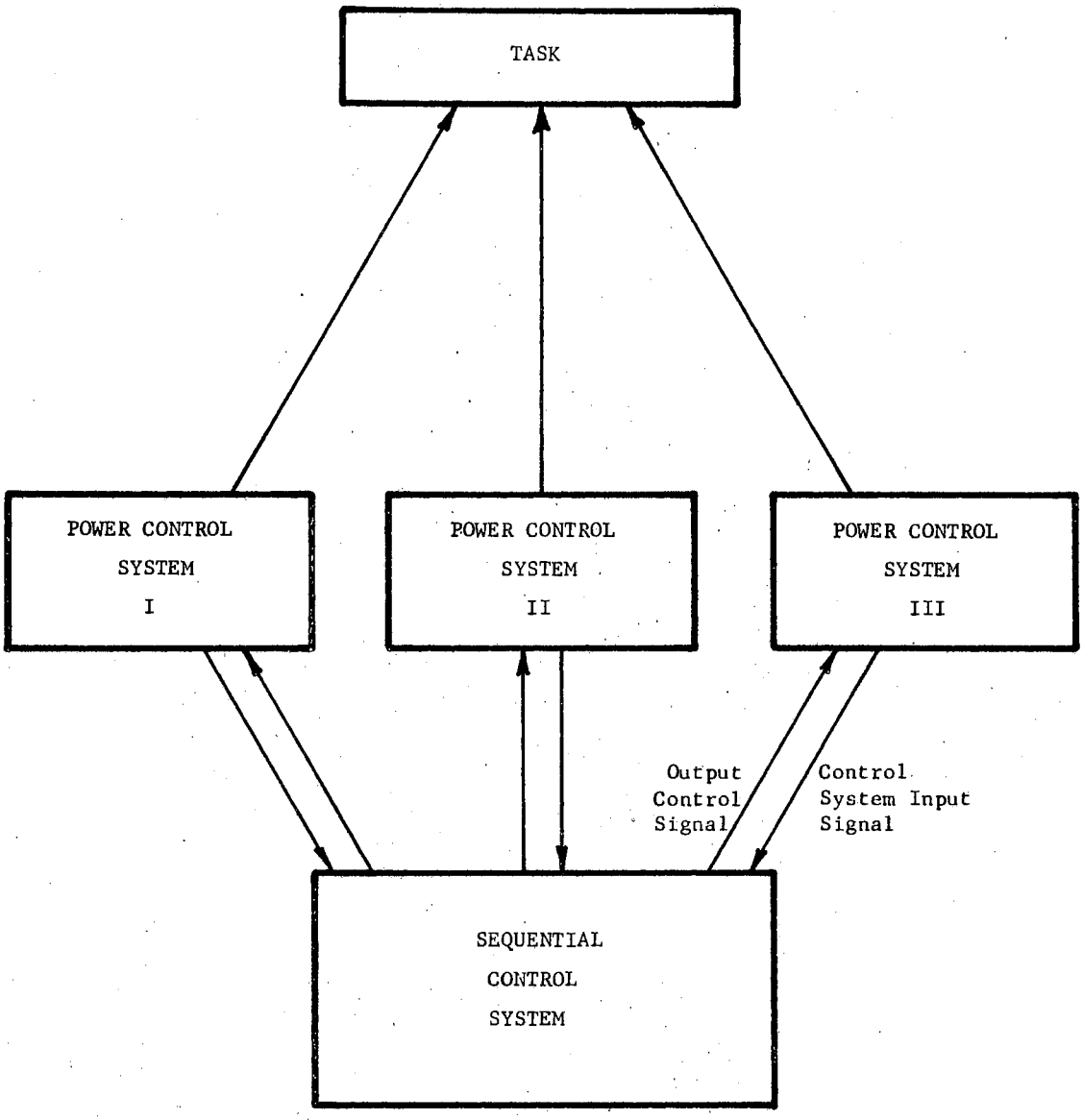


Figure 1. Schematic of Sequential Machine Control

combinational switching circuit in conjunction with feedback delay elements which define internal states for the total sequential circuit. A schematic of the asynchronous sequential circuit implemented in this manner is given in Figure 2. The outputs of the combinational circuit depend on the unique total states of the combinational circuit inputs. The combinational circuit inputs are derived from the combination of external input signals and delayed internal state outputs. A particular unique combination of the combined combinational circuit inputs defines a sequential circuit total state. The combinational circuit outputs consist of external working outputs and internal outputs which serve as inputs to the internal state identification elements of the circuit. By observing only the external outputs of the sequential circuit for given changes in external inputs, the circuit appears to possess "memory" or "decision-making" power since the external outputs are not unique functions of the external input combinations.

The formalized synthesis procedure for the asynchronous sequential circuit was first conceived in 1954 by Huffman (12). This procedure has been employed extensively in the design of electrical and electronic circuits (3, 17) and to a limited but very successful degree in the design of hydraulic control circuits (5, 6). The steps involved in the design of the asynchronous sequential circuit can be summarized as:

1. Derivation of the logic requirements of the circuit from logic specifications.
2. Reduction of these requirements to give a suitable minimal or near-minimal state circuit.
3. Assignment of values to the internal states of the

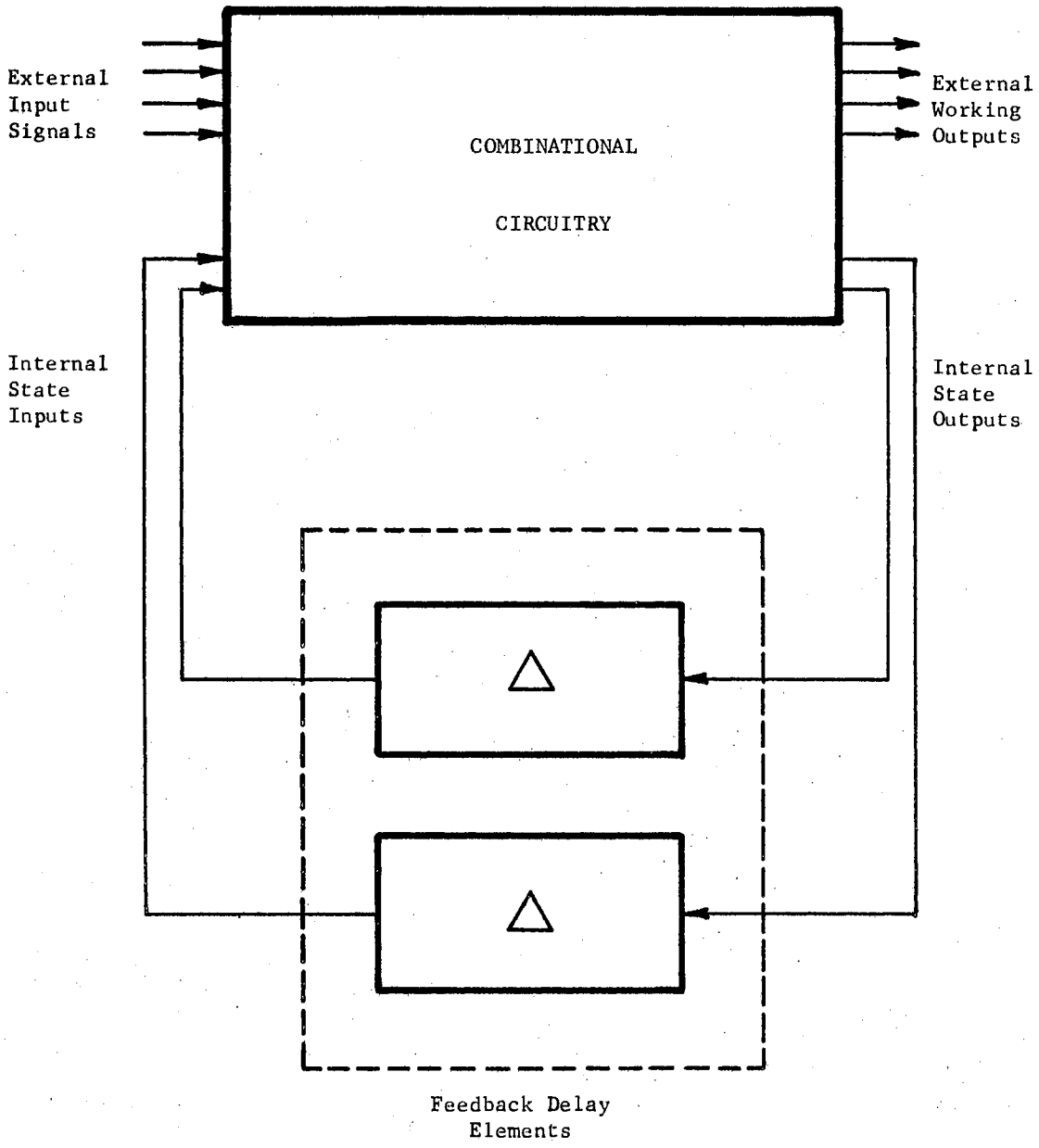


Figure 2. Schematic of Asynchronous Sequential Circuit

circuit to provide uniqueness of the circuit's total state.

4. Derivation of the equations representing the logic representations of the circuit's external and internal outputs.
5. Proper implementation of the logic equations with working hardware to perform the required logic operations.

Numerous different sequential circuits which will perform equivalent control functions can be implemented from a given logic specification. Thus, the sequential circuit designer can have different circuit design criteria dependent on the application for which the circuit is to be employed. Due to the premium placed on the operational speed of most fluid control systems, the achievement of maximum operating speed along with maintaining correct circuit operation will be defined as the design criteria to be employed in the synthesis of fluidic sequential circuits.

To satisfy the above design criteria, it is necessary to evaluate the importance of each step in the circuit synthesis procedure in relation to the selected criteria. Step 1 of the synthesis procedure determines the necessary logic requirements of a given system to perform a given task. The logic structure and complexity of the final circuit are influenced by the decisions made in the execution of Step 2. However, neither of these first two steps, when correctly performed, directly influence the final operating speed or correct operation of the circuit. Each of the last three steps does affect both the operational speed and correctness of operation. Therefore, succeeding work will be primarily concerned with investigating the details of each of these

three last design steps with the purpose of satisfying the design criteria defined above for fluidic asynchronous circuits.

In Chapter II, a review of sequential circuit theory will be presented together with an illustration of the physical circuit model which can be employed to design asynchronous sequential fluidic circuits. The criteria which assures the fast, safe operation of an asynchronous circuit are also given. The problem of assigning unique binary code representation to each internal state of an asynchronous circuit is discussed in Chapter III. A general method of internal state representation is reviewed which provides safe internal circuit operation and the fastest over-all circuit action for given logic components.

After the internal state representation for an asynchronous circuit has been determined, the Boolean algebra equations can be obtained for representing the logic properties of the combinational portion of the asynchronous circuit. The discussion in Chapter IV is concerned with implementing these combinational circuit equations such that:

1. Hazard free circuit operation will result during input transitions.
2. The transmission delay of an input signal through the combinational circuit is minimized.

It is first noted that techniques are available for implementing hazard free combinational circuitry without considering the operational timing of the logic elements used to implement the circuit. A method is then presented for minimizing the number of logic stages required to implement a given Boolean equation in AND-OR logic circuit form with limited fan-in logic elements. Minimizing the logic stages in a combinational circuit minimizes the transmission delay of a signal through the circuit.

The logic stage minimization procedure provides estimates of both the maximum total signal delay encountered in the combinational circuit and the maximum and minimum signal delays experienced in the AND portion of the AND-OR combinational circuit. These delay time estimates are employed in Chapter V to determine the timing requirements needed to control the response of the feedback delay elements in the circuit and for approximating the maximum allowable frequency for external input changes to the circuit. Physically providing the control specified by these requirements assures the safe operation of the asynchronous circuit.

The operational timing requirements for the fluidic components used to implement an asynchronous circuit are considered in Chapter VI. Due to the required response control of the feedback delay elements in an asynchronous circuit, emphasis is placed on developing techniques which can be utilized for predicting the response of a basic fluidic component that can be employed as a feedback delay element. An analytical model is developed to predict one component of the total response time for the fluidic feedback delay element. The analytical model indicates that the response time of the delay element could be controlled by adjusting the shape and magnitude of the input control signal to the element. Experimental data for the total switching time of the feedback element substantiates this prediction.

The control signal trends observed in the combined analytical experimental response time study are utilized to formulate a method for timing the fluidic feedback delay elements to satisfy the timing requirements of an asynchronous circuit. By necessity, this timing method requires experimental switching time data from which the stray

delay bounds of the feedback element can be determined for a specified operational reliability. Physical sizing of the feedback delay elements and adjustments in magnitude and shape of the control signals to the elements are suggested as methods for timing the feedback delay elements such that safe operation of the asynchronous circuit will result.

CHAPTER II

ASYNCHRONOUS SEQUENTIAL CIRCUIT MODELS AND DEFINITIONS

A sequential circuit is an input-output logic circuit whose output depends both on present and past history of the input state. An asynchronous sequential circuit is defined as a sequential circuit with each internal state being a stable state and whose operational timing is internally controlled. The asynchronous sequential switching circuit is particularly suited for fluidic circuit application since when properly designed, the resulting asynchronous circuit produces the fastest possible circuit response times for a given type of logic hardware. The internally timed characteristic of the asynchronous circuit is also important since fluid timing sources are difficult to design and control.

To appreciate the problems associated with synthesizing and implementing the asynchronous sequential circuit, it is necessary to understand the fundamentals of sequential circuit theory and how the theory can be implemented to produce a physical circuit. This chapter will present a cursory treatment of asynchronous sequential circuit theory and physical circuit implementation. Also, a summary will be given detailing the sufficient requirements for designing the fastest responding, safe operating asynchronous sequential circuitry.

Mathematical Definition of an Asynchronous Sequential Circuit

The asynchronous sequential circuit is a logic circuit which has a finite number of binary-valued inputs, outputs, and internal states. Thus, the circuit is referred to as a finite-state asynchronous sequential circuit. The mathematical model of a finite-state asynchronous sequential circuit is referred to as a finite-state asynchronous sequential machine usually shortened to asynchronous machine.

The asynchronous machine, M, can be defined by the following (20):

1. A finite set of outputs, Z.
2. A finite set of inputs, X.
3. A finite set of internal states, Q.
4. An output map of M termed z of a subset D_z of Q x X onto Z.
5. A transition map of M termed τ of a subset D_τ of Q x X onto Q.
6. Each state $q_j \subseteq Q$ is stable.

Where:

A state is termed stable for any input $x \subseteq X$ such that if

$$\tau(q_k, x) = q_j$$

it follows that

$$\tau(q_j, x) = q_j$$

($\tau(q_k, x)$ denotes the next state of machine M if the machine is presently in state, q_k and receives input, x).

The type of asynchronous machine considered in this work will be limited to receiving only level signal inputs. Level signals are binary valued signals which assume a value of 1 or 0 for a length of time greater than the response time of the circuit. Level input asynchronous machines are referred to as fundamental mode sequential machines.

The internal states, q_i, of an asynchronous machine consist of a set of machine total states. A total state is defined by a unique combination $(q_i \times x_i)$ of the internal state, q_i, with input x_i. Total states can be stable under input, x_i, thus they are termed stable states. Or the total states can be transition states under input, x_i, and are referred to as unstable states. Total states can have outputs, z_i, associated with them in both the stable and unstable condition. Also the total state may not be defined for particular combinations of $(q_i \times x_i)$, thus producing "don't care" conditions in the τ map. A similar nondefinitive condition can exist for the output designations.

If a machine, M, has all total states and outputs defined, then M is called complete. If M is not complete, it is referred to as incompletely specified. The incompletely specified type of asynchronous machine is the more general case and the type usually encountered in practice, thus this type will be assumed in the following sections.

Graphical Representation of Asynchronous Machines

The two principle methods of representing asynchronous machines are by the state diagram and the flow table. The two particular representations described below were formulated by Mealy (18) and Huffman (12), respectively.

The State Diagram

The state diagram of an asynchronous machine, M, is constructed by representing each internal state, q, by a circle in which the particular internal state, q_i, is inscribed. The circles are interconnected by lines which correspond to the transitions designated by the transition map, τ. The input, which produced the transition, together with the particular stable state output involved are assigned to the corresponding transition line. Thus, if $\tau(q_i, x_i) = q_k$ with output z_i, a line is drawn between q_i and q_k with an arrowhead at q_k and with x_i/z_i assigned to the line. The stable states of an internal state are indicated by drawing a looping line from state q_i back to q_i with proper input-output assignment. An example of this type of state diagram for a four state asynchronous machine is given in Figure 3.

The state diagram is used principally to formulate the logic requirements of a machine and for use in studying the logic structure and behavior of the machine. Also, most of the published literature describing the theoretical aspects of sequential machines use the state diagram for descriptive purposes.

The Flow Table

The flow table representation of an asynchronous machine is formed by assigning a table column to each unique machine input and a table row to each internal state. Individual locations in the table define a total state $(q_i \times x_i)$ of the machine. Entries into these individual locations correspond to the machine's next state and corresponding external output when it is in the particular total states. Three

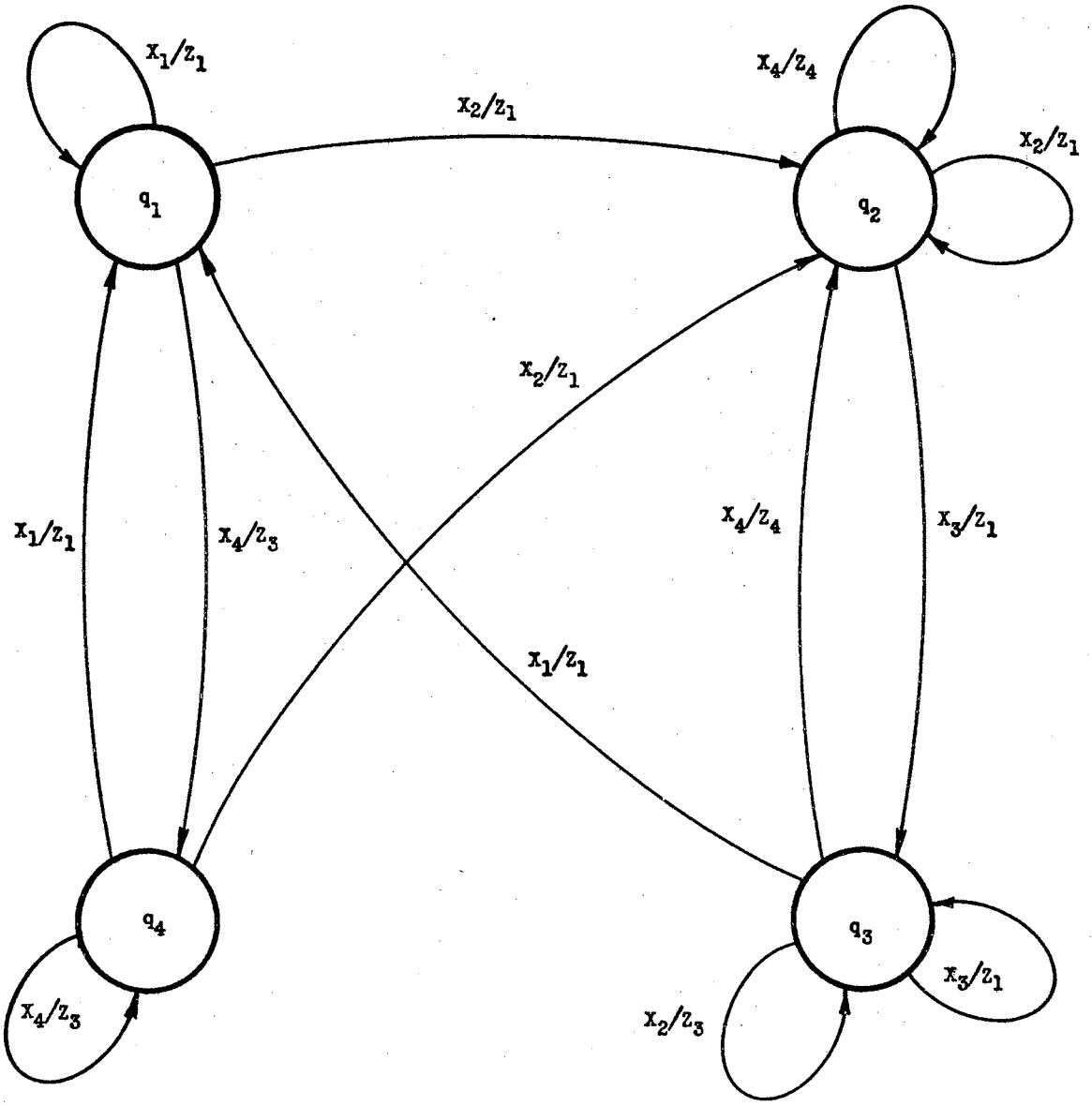


Figure 3. State Diagram for a Four-State Asynchronous Machine

conditions exist for possible machine action with respect to a particular state:

1. The machine is in a stable state, thus the total state entry corresponds to the internal state.
2. The machine is in a transitory or unstable mode, thereby, causing the total state entry to correspond to the next internal state which the machine will occupy.
3. The machine action is not specified for the particular total state.

The stable state condition is designated in the total state location by a circle in which the corresponding internal state is inscribed. The unstable state is identified by placing the internal state to which the machine is transferring in the total state location. The unspecified condition is indicated by placing a dash in the total state location. The machine outputs can also be placed in each total state with the internal state designated as q_i/z_i or can alternatively be represented in a separate output map. Figure 4 shows the flow table representation for the machine given in state diagram form in Figure 3.

	X_1	X_2	X_3	X_4
q_1	$(q_1)/z_1$	q_2/z_1	—	q_4/z_3
q_2	—	$(q_2)/z_1$	q_3/z_1	$(q_2)/z_4$
q_3	q_1/z_1	$(q_3)/z_3$	$(q_3)/z_1$	q_2/z_4
q_4	q_1/z_1	q_2/z_1	—	$(q_4)/z_3$

Figure 4. Flow Table for a Four State Asynchronous Machine

Asynchronous Machine Synthesis Procedure

The synthesis procedure commonly employed to design asynchronous machines makes extensive use of the flow table. The initial step of the procedure is to form the flow table such that each individual stable state of the machine is assigned a unique internal state; i.e., one stable state per flow table row. The designer then designates the required machine action by specifying the machine's outputs and transitions for each possible total state that can ever exist in the operational history of the machine. The flow table formed in this manner is called a primitive flow table.

An example is given in Figure 5 of how a primitive flow table might have looked for the machine represented in Figure 4. The use of one internal state per stable state in the primitive flow table is very wasteful with regard to internal state utilization. The number of rows in the primitive flow table can be reduced by a process termed "merging." Merging the rows of a primitive flow table reduces the number of internal states of the circuit. The resulting reduced table is referred to as the merged "flow" table. The state reduction problem for incompletely specified machines is very complex, especially when attempting to minimize the final cost of the circuit.

Many state reduction techniques are based on finding the minimum number of internal states with which to represent a given machine (7, 25). This does not solve the over-all circuit cost minimization problem, however, since the answer is strongly dependent on the cost of the particular hardware components used to implement the total circuit. The speed and reliability of circuit operation are not directly related

to the number of internal states which are employed in the representative machine; thus, the state reduction problem will not be considered in this study.

	X_1	X_2	X_3	X_4
q_1	$(q_1)/Z_1$	q_2/Z_1	——	q_4/Z_3
q_2	——	$(q_2)/Z_1$	q_3/Z_1	q_5/Z_4
q_3	q_1/Z_1	q_6/Z_3	$(q_3)/Z_1$	q_5/Z_4
q_4	q_1/Z_1	q_2/Z_1	——	$(q_4)/Z_3$
q_5	——	q_2/Z_1	——	$(q_5)/Z_4$
q_6	q_1/Z_1	$(q_6)/Z_3$	q_3/Z_1	——

Figure 5. Primitive Flow Table for an Asynchronous Machine

After a suitable reduced state machine has been found, the next step in the synthesis procedure is to assign an appropriate set of binary-valued state variables to represent the internal states of the machine. For asynchronous machines, the state variable assignment must be made such that machine transitions between stable states are definite and will lead to the proper stable state regardless of the response speed of the circuit elements used to generate the state variables. This type of assignment assures that "critical racing" among the state variable elements will not determine the next stable state of an

asynchronous machine following a transition. The state variable assignment influences both the speed and correctness of operation of the circuit. The state variable assignment problem will be discussed in detail in Chapter III.

When suitable state variable assignment has been made, the circuit synthesis problem becomes identical to the design of a combinational switching circuit. In a combinational circuit, the circuit outputs depend only on the present value of the circuit inputs, thus the past history of circuit operation is not a factor. There are hazards which arise in the combinational circuit design that must be eliminated for proper asynchronous circuit action. These hazards are associated with the imperfect response characteristics of the elements used to implement the combinational circuit and can be alleviated by proper selection of the logic representation for the combinational circuit outputs. Details of the problems associated with implementing combinational circuitry are given in Chapter IV. The general aspects of implementing a properly timed asynchronous circuit are introduced in the next section of this chapter.

Physical Models for Asynchronous Machines

The General Model

The asynchronous machine can always be implemented as a combinational switching circuit with feedback delay elements as shown in Figure 6.

This model utilizes n external inputs x_i, m external outputs Z_i, and k state variables y_i to perform the asynchronous machine function.

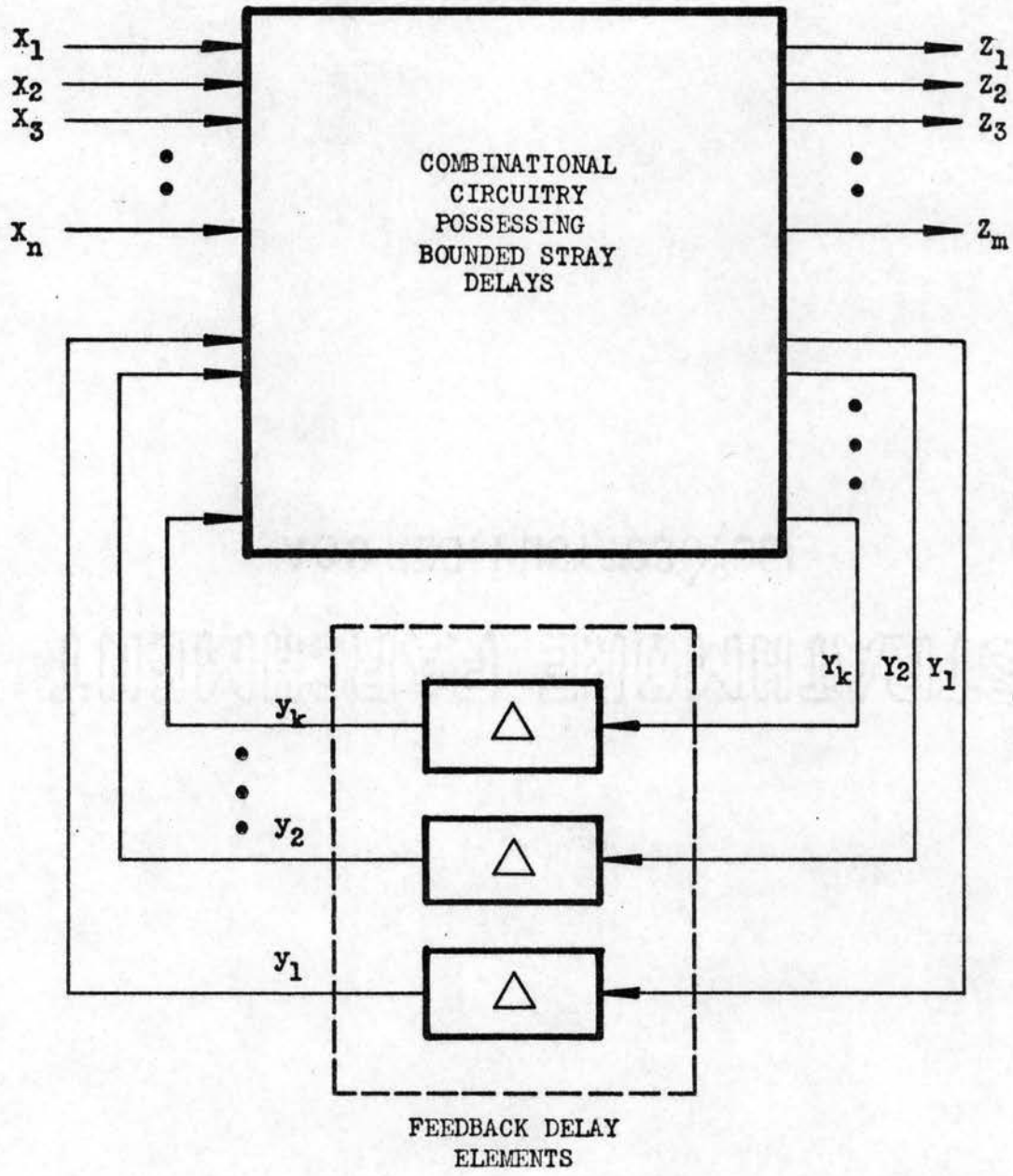


Figure 6. General Asynchronous Machine Model

An internal state of the machine is defined as a particular unique set of the secondary state variables. An example of an internal state for a four state variable asynchronous machine could be represented by the particular values of the state variables $y_1 = 0$; $y_2 = 1$; $y_3 = 1$; $y_4 = 0$. The group of binary digits, 0110, which represent the respective values of the binary variables y_1, y_2, y_3, y_4 is commonly referred to as a 4-tuple.* This example illustrates a single element set for internal state representation, although multi-element sets can also be used for defining internal states. The combination of a particular state variable tuple with a particular external input tuple defines a total state of the machine.

The external outputs, Z_i, and the internal outputs, Y_i, of the combinational circuit are binary-valued functions of the internal and external inputs, thus functions of the total state. These outputs are expressed by the Boolean relationships.

$$
\begin{aligned}
Z_1 &= Z_1(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_i, \cdots, y_k) \\
Z_2 &= Z_2(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_i, \cdots, y_k) \\
&\vdots \\
Z_i &= Z_i(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_i, \cdots, y_k) \qquad (2\text{-}1) \\
&\vdots \\
Z_m &= Z_m(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2 \cdots, y_i, \cdots, y_k)
\end{aligned}
$$

---

*An n-tuple is an n digit binary representation; i.e., $e = (e_1, e_2, \cdots, e_i, \cdots, e_n)$ is an n-tuple where $e_i = 0$ or 1.

$$Y_1 = Y_1(x_1, x_2, \cdots, x_i, \cdots, x_m ; y_1, y_2, \cdots, y_i, \cdots y_k)$$
$$\vdots$$
$$Y_k = Y_k(x_1, x_2, \cdots, x_i, \cdots, x_m ; y_1, y_2, \cdots, y_i, \cdots y_k) \quad (2\text{-}2)$$

The objective of the asynchronous circuit synthesis procedure is to arrive at appropriate Boolean expressions as indicated by Equations (2-1) and (2-2) for the combinational circuit outputs. The Y_i defined by Equation (2-2) are known as next state equations and are derived from the τ-map defined previously in this chapter.

In the implementation of the asynchronous model with physical components, a delay always exists for the transmission of an input signal through the combinational circuit to form a circuit output. This delay is created by the response times of the logic elements used to implement the combinational circuit. The response time of an operational logic element must be finite, thus the element delay time can be considered bounded by a maximum delay of Δ_{MAX}. Since fluctuations in operating conditions can cause the switching time of a logic element to vary from one operating time to another, the delay time of the logic element can stray in value at different actuation times. The delay time of a logic element can be considered a time varying delay defined by an upper and lower bound. Such a variable delay logic element is termed a bounded stray delay logic element, where the bounded stray delay, $\Delta(t)$, is defined as $\Delta_{MIN} \leq \Delta(t) \leq \Delta_{MAX}$. The minimum stray delay limit for the combinational circuit element is not important with respect to the correct operation of an asynchronous circuit; therefore, the combinational element delay can be defined by $0 \leq \Delta(t) \leq \Delta_{MAX}$, would be determined from experimental switching time data for the combinational circuit elements.

For certain transitional properties of an asynchronous circuit, the feedback delay elements shown in Figure 6 must be controllably timed to assure correct circuit operation. The purpose of timing the feedback delay elements is to allow the combinational circuit to stabilize before the state variable signals change. This feedback delay timing requirement represents the most critical problem encountered in the internal physical design of an asynchronous circuit. The switching time of the feedback element must be controlled between the defined delay bounds of Δ_{MIN} and Δ_{MAX}. The lower delay bound, Δ_{MIN}, is determined by the amount of delay required to assure safe operation of the circuit. The upper delay bound, Δ_{MAX}, would be obtained from the variance in the switching time data for an element operating with a lower bound of Δ_{MIN}. The required reliability for the switching time of the feedback delay element determines the magnitude of the delay bound difference, $\Delta_{MAX} - \Delta_{MIN}$. The upper delay bound, Δ_{MAX}, would influence the maximum allowable operating speed of the circuit.

The general scheme for physically implementing a fast responding asynchronous circuit will be to construct the combinational circuit with fast-acting bounded delay components and control the feedback element response time to properly time the over-all circuit. It should be noted that the stray delay times for the combinational elements have to be known or measured, but not controlled to properly implement the asynchronous circuit. This design philosophy constitutes the reason for developing the methods for controlling the timing of the fluidic feedback delay element which are presented in Chapter VI.

Asynchronous Machine Model Utilizing S-R Flip-Flop Elements for Feedback Delay Elements

To achieve the most advantageous implementation of an asynchronous circuit with a particular type of logic hardware requires that circuit logic and physical requirements be matched with the chosen hardware's operating properties. For the case of employing fluidic components to implement asynchronous circuitry, it proves advantageous to use set-reset flip-flops for the feedback delay elements. The set-reset (S-R) flip-flop is a two input, two output basic memory device as shown schematically in Figure 7. The logic equations for the S-R flip-flop can be expressed as

$$y = S + \bar{R}y$$
$$RS = 0 \qquad (2\text{-}3)$$

From Equation (2-3), it can be seen that the S-R flip-flop will be set to the output state y = 1 by the set signal S. This y = 1 signal will be held in memory by the flip-flop until a reset signal, R, is received. This hold feature of the flip-flop device is represented by the term $\bar{R}y$. The condition, RS = 0, is specified to prevent a reset and set signal from being applied simultaneously to the flip-flop device.

The fluidic S-R flip-flop can be constructed as a basic one-piece component. This one fluidic element can provide needed signal amplification in the circuit and produce both the uncomplemented and complemented value of the state variable signals. In addition, the flip-flop element creates the required controllable delay in the feedback lines. The

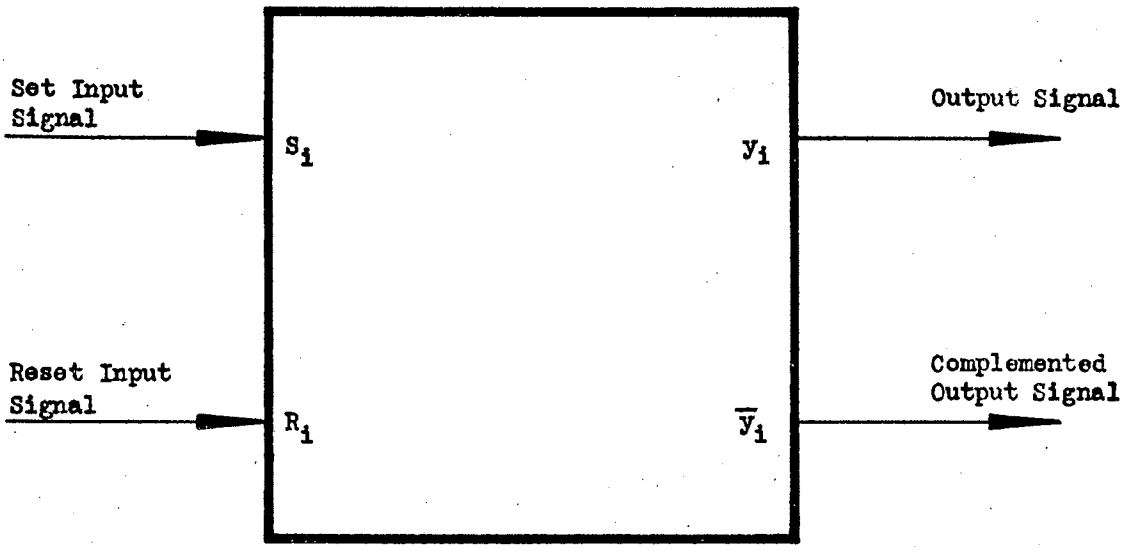


Figure 7. Schematic of Set-Reset Flip-Flop

one-component fluidic flip-flop represents a significant implementation advantage over the multi-component construction of an electronic flip-flop.

When the general asynchronous model in Figure 6 is implemented with S-R flip-flops in the feedback delay line, the machine model is as shown in Figure 8. The representative next state equations for the S-R flip-flop inputs in Figure 8 are:

$$
\begin{aligned}
S_1 &= S_1(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_2, \cdots, y_i, \cdots, y_k) \\
R_1 &= R_1(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_2, \cdots, y_i, \cdots, y_k) \\
&\vdots \\
S_i &= S_i(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_{i-1}, y_{i+1}, \cdots, y_k) \\
R_i &= R_i(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_{i-1}, y_{i+1}, \cdots, y_k) \\
&\vdots \\
S_k &= S_k(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_i, \cdots y_{k-1}) \\
R_k &= R_k(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_i, \cdots, y_{k-1})
\end{aligned}
\qquad (2\text{-}4)
$$

Summary of "Fast," "Safe" Asynchronous Circuit Design Criteria

The general properties of the asynchronous circuit have been discussed in this chapter. The design criteria sufficient to insure safe circuit operation and fastest possible circuit response can now be defined more closely.

Safe Operating Requirements

The requirements for designing safe operating asynchronous circuits can be separated into two distinct groups as shown by Miller (20). These are:

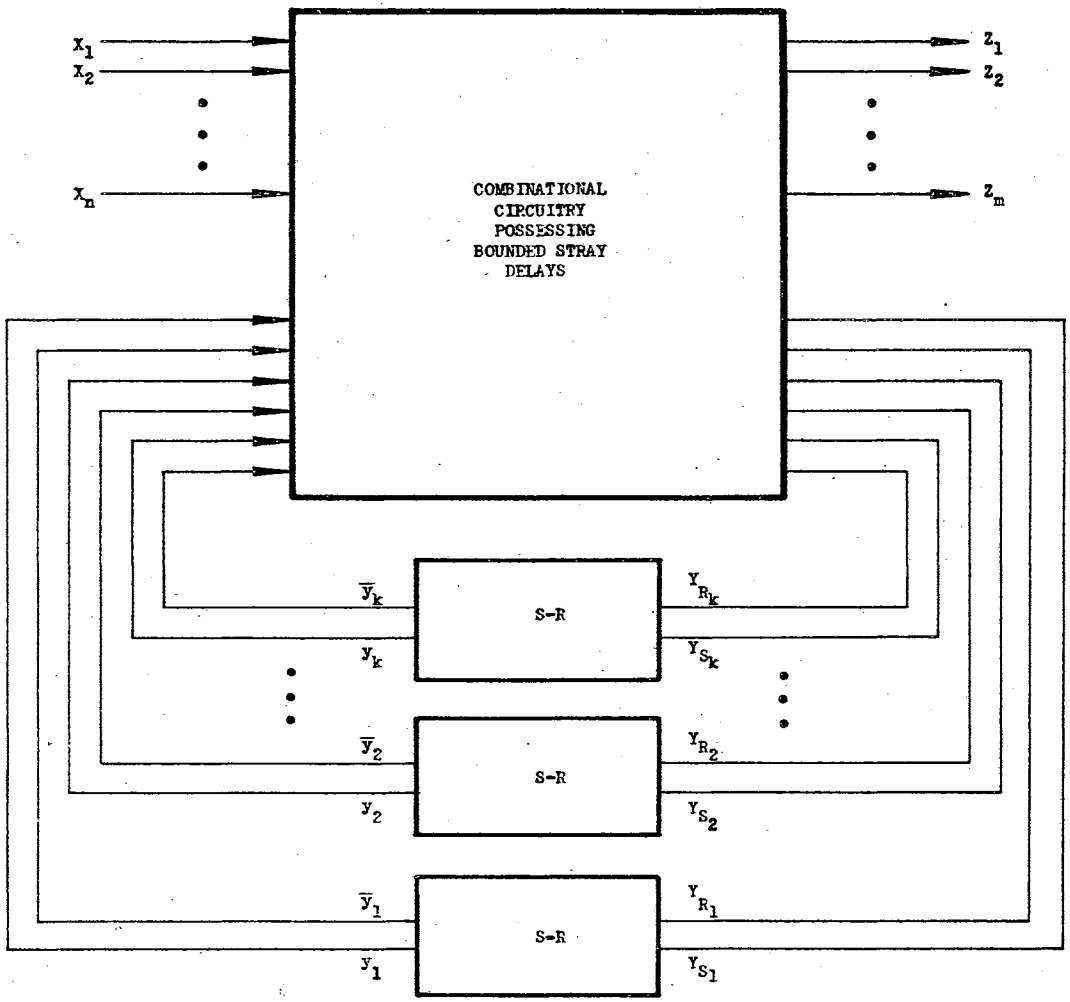


Figure 8. Asynchronous Machine Model With S-R Flip-Flops in the Feedback Delay Lines

1. The requirements which insure correct operation of the internal circuit.
2. The restrictions placed on the external environment which communicates with the asynchronous circuit.

The internal circuit requirements have been discussed previously in this chapter and can be summarized by:

1. The elimination of hazards in the combinational portion of the asynchronous circuit.
2. The assignment of a state variable code such that no critical races will occur among the secondary state elements during circuit transitions.
3. The proper timing of the secondary state elements so that the combinational circuit will stabilize before the secondary state signals change.

The first and second internal circuit requirements can be fulfilled in the synthesis stage when deriving the logic equations which describe the circuit. The third requirement must be satisfied by physically timing or delaying the secondary state elements to allow stabilization of the combinational circuit.

The restrictions which must be placed on the external environment that furnishes inputs to the asynchronous circuit are defined by the following:

1. The external inputs must change one at a time; i.e., the next input must be adjacent* to the present input.

---

*Consider $(x_1, x_2, \ldots, x_n)$ to be an input combination to the circuit, where $x_i = 0$ or 1. Two input combinations $(x_1, x_2, \ldots, x_n)$ and $(x_1', x_2', \ldots, x_n')$ are said to be <u>adjacent</u> if $x_i \neq x_i'$ with all other x's equal.

2. The rate at which the external inputs can be changed must be limited to allow the total asynchronous circuit to settle and thus reach a stable state.

The first external restriction can be met by physically allowing only adjacent external inputs to the asynchronous circuit. The second restriction limits the frequency at which the external inputs can be changed. This limiting frequency is a function of both the response times of the elements used to implement the internal circuitry and the way that state variable and output assignments are made in the circuit synthesis procedure.

Fast Operating Requirements

To maximize the operating frequency of an asynchronous circuit, one must consider circuit speeding techniques in the synthesis procedure together with the use of fast-acting logic components to implement the circuit. The techniques employed in the synthesis procedure to obtain the fastest possible asynchronous circuit action are concerned with the type of assignments made to the secondary state variables, with the specification of any possible external output changes and with the type of logic equations used to represent the combinational portion of the asynchronous circuit. The fastest possible asynchronous circuit for given logic hardware can be obtained when the following techniques are employed:

1. Only one state variable is allowed to change during any given circuit transition, thus eliminating any cycling of the state variables.
2. If an external output change is specified for a

particular transition, the output change will be initiated at the start of the transition.

3. The delay time of a signal passing through the combinational portion of the circuit is minimized.

These requirements do not conflict with the previously defined safe operating requirements for the asynchronous circuit. In fact, the first of the above requirements represents a much more severe restriction on the type of state variable assignments which can be made for a given asynchronous circuit.

One general state variable assignment which satisfies the above requirement of one state variable change per transition will be discussed in Chapter III. The specific effects of specifying the output change stipulated by the second requirement will be given in Chapter V. The minimization of the delay time of a signal passing through the combinational circuit can be achieved by employing two-level logic* equations to represent the logic requirements of the circuit. This type of equation representation will be discussed in more detail in Chapter IV.

---

*Two-level logic refers to a logic circuit in which a signal never has to pass through more than two circuit elements to generate a specified logic function. Common two-level logic circuits are AND-OR circuits represented by a sum of products Boolean equations and OR-AND circuits represented by a product of sums Boolean equation.

CHAPTER III

STATE VARIABLE ASSIGNMENT

The internal states of an asynchronous circuit provide memory capacity which a circuit designer can utilize to give an automated machine "decision-making" ability. To physically implement the asynchronous circuit, a unique assignment of secondary state variables must be made to each internal state. In addition to being unique, the state variable assignment must produce safe circuit action regardless of the individual operating speeds of the physical elements used to implement the state variables. The latter requirement is commonly referred to as the avoidance of "critical racing" among the state variable elements during circuit transitions. The fast operating requirement defined in Chapter II for asynchronous fluidic circuits specifies that only one state variable will be allowed to change during a transition from one stable state to another. State variable assignments which satisfy this requirement automatically eliminate the critical race problem and must then meet only the uniqueness requirement.

This chapter will first consider by illustrative example the problems encountered in making a state variable assignment to achieve safe circuit operation. A technique will then be presented which meets both the safe and fast operating criteria defined for the design of asynchronous fluidic circuits. This technique was originally proposed by Huffman (11) and has been recently discussed by Miller (20). An example

will be given of the application of the technique for making state variable assignment to a typical reduced flow table.

The State Variable Assignment Problem

As defined previously, the state variable assignment problem consists of assigning an appropriate set of binary-valued state variables to represent the internal states of a circuit. This assignment must provide uniqueness to each state and cause proper circuit action during any transitions. The following discussion should illustrate and define the aspects of the problem.

Consider the reduced flow table shown in Figure 9. There are four internal states which must have unique safe operating state variable assignments. At least two state variables must be used to represent the four internal states of the circuit. In general, if N represents the

X_1	X_2	X_3	X_4
(q_0)	q_1	q_2	(q_0)
q_2	(q_1)	(q_1)	q_0
(q_2)	q_3	(q_2)	q_3
q_0	(q_3)	q_1	(q_3)

Figure 9. Reduced Flow Table for a Circuit With Four Internal States

number of internal states, the minimum number of state variables, R_o,

which could be used to represent the circuit is given by the condition

$$2^{R_o} \geq N$$

or

$$R_o \geq \log_2 N \tag{3-1}$$

The four possible binary combinations for the two state variables y_1, y_2 are shown in 2-cube representation by Figure 10.

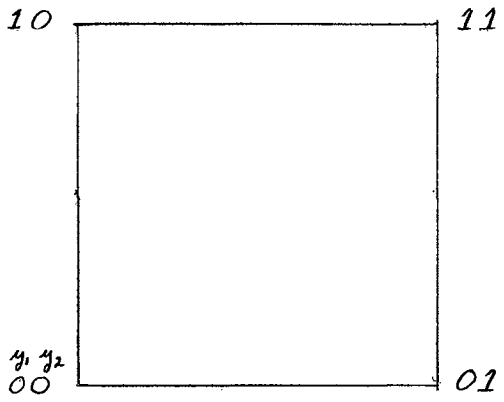


Figure 10. The 2-Cube Representation for Possible Two State Variable Combinations

Adjacent state variables are represented by adjacent vertices on the 2-cube. Thus, the objective of the state variable assignment methods considered in this work will be to make assignment of adjacent cube vertices to the internal states of a circuit between which transitions exist. When adjacent state variable assignment is achieved with n

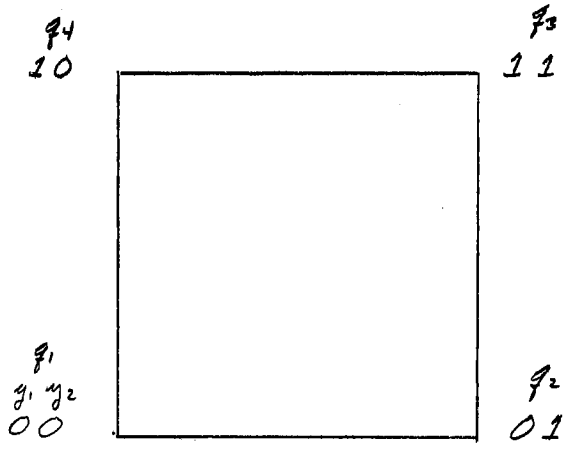
state variables, the states of the circuit are defined as being embedded in the n-cube. Embedding the state of a circuit in an n-cube assures that critical racing among the state variable elements cannot happen since only one state variable is allowed to change during a transition from one state to another. It should be noted that to achieve safe circuit operation while disregarding the circuit speed, the states involved in transitions can be unstable transitory states as well as stable states.

The circuit represented in Figure 11(a) cannot be embedded in a 2-cube since the requirement of changing one y_i at a time cannot be satisfied for all required transitions. For example, refer to the state variable assignment shown in Figure 11(b).

Transitions between states q_3 and q_2, q_3, and q_4, q_4 and q_1, q_1 and q_2 are possible by changing only one y_i. However, transitions between q_3 and q_1, q_4 and q_2 involve simultaneous changes of both state variables. This creates a critical race condition in the state variable assignment. For instance, notice the transition which occurs when the circuit is in stable state q_1 and receives input x_3. The flow table dictates that the circuit state be transferred to stable state q_3; therefore, both state variables receive signals to change from $y_1 = 0$, $y_2 = 0$ to $y_1 = 1$, $y_2 = 1$. If the y_2 state variable element reacts faster than the y_1 element, the state variables will change to $y_1 = 0$, $y_2 = 1$. This assignment identifies stable state q_2, thus the excitation signal which originally called for y_1 to change will be lost and the circuit could terminate in an erroneous stable state. The same condition exists if the y_1 element is faster than the y_2 element. For assured correct circuit operation, the reaction times of the two state

X_1	X_2	X_3	X_4
(q_1)	q_2	q_3	(q_1)
q_3	(q_2)	(q_2)	q_1
(q_3)	q_4	(q_3)	q_4
q_1	(q_4)	q_2	(q_4)

(a) Reduced Flow Table



(b) State Variable Assignment

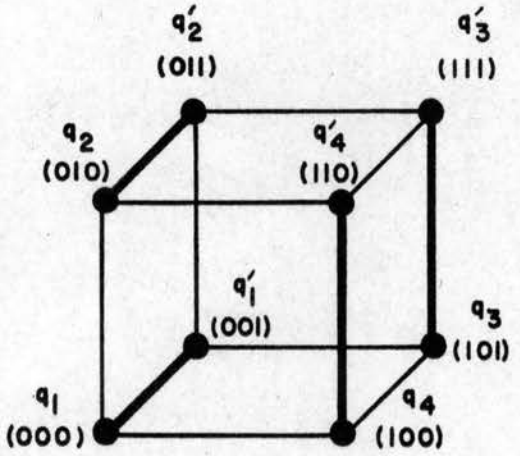
Figure 11. Example State Variable Assignment

variable elements must be identical, which for practical purposes is physically impossible. Therefore, a different state variable assignment must be made to eliminate the critical race condition. This can be done through the process of "splitting" the stable states of the original flow table to obtain the adjacency requirement for embedding the circuit states in the n-cube. In general, when the original number of state variables is equal to the minimum as determined by Equation (3-1), state splitting to achieve embedding requires additional state variables.

For the example problem, one can intuitively split the states as shown in Figure 12. As indicated by the arrows in Figure 12, more than one transition is sometimes required to transfer from one stable state to another stable state. For these multiple transitions, the state variables are "cycled" through unstable transitory states which provides circuit action with only one y_i state variable change per transition. In Chapter V, it will be shown that state variable cycling could substantially decrease the frequency at which a given asynchronous circuit can be operated. This decreased operating frequency results from the additional time which must be allowed for the state variable signals to traverse the combinational circuit for each cycle.

The state assignment in Figure 12 splits the four original internal states into eight states or, viewed differently, the assignment has provided four sets of two 3-tuple state variables y_1, y_2, y_3 to represent the internal states. These sets of 3-tuples possess special properties which make it possible to transfer from one to any other of the internal states while meeting the requirement that only one y_i change occur during a state transition. These properties can be summarized by:

1. The n-tuples included in each state set, S, are



(a) 3-CUBE STATE ASSIGNMENT

$q_1 \left\{ (000)^{S_1}, (001) \right\}$

$q_2 \left\{ (010)^{S_2}, (011) \right\}$

$q_3 \left\{ (101)^{S_3}, (111) \right\}$

$q_4 \left\{ (100)^{S_4}, (110) \right\}$

(b) STATE ASSIGNMENT SETS

	y_1	y_2	y_3	X_1	X_2	X_3	X_4
q_1	0	0	0	(q_1)	q_2	q'_1	(q_1)
q'_1	0	0	1	–	–	q_3	–
q_2	0	1	0	q'_2	(q_2)	(q_2)	q_1
q'_2	0	1	1	q'_3	–	–	–
q_3	1	0	1	(q_3)	q_4	(q_3)	q_4
q'_3	1	1	1	q_3	–	–	–
q_4	1	0	0	q_1	(q_4)	q'_4	(q_4)
q'_4	1	1	0	–	–	q_2	–

Figure 12. Example of State Splitting

connected*, thus the S sets are connected sets.

2. The four S sets are adjacent since there exists at least one n-tuple in each S set that is adjacent to at least one n-tuple in the other S sets.
3. The four S sets are coupled since each connected S set is adjacent to the other S sets.
4. Since the S sets are coupled, they are defined as intermeshed sets when associated with the internal states, q_i, of a circuit.

When the internal states of a circuit can be assigned intermeshed sets of n-tuple state variables, the states can always be embedded in an n-cube, thus eliminating concern about critical racing among the state variable elements. General methods which generate intermeshed sets with no trial and error involved have been developed and are discussed by Huffman(11), McCluskey (15) and Miller (20). The minimum number of state variables required for formulating intermeshed sets by a general method has been shown to be $2R_o - 1$(11). This method guarantees that no more than four cycles will be required during a transition from one stable state to another. Thus, a limit can be set on the number n of state variables needed to represent a N internal state asynchronous circuit if cycles can be permitted in the state variable assignment. This limit can be defined as:

$$\log_2 N \leq n \leq 2R_o - 1 \qquad (3\text{-}2)$$

---

*A pair (k_1, k_2) of n-tuples $(y_1, y_2, \ldots, y_n)$ is called connected if there is a sequence of adjacent n-tuples of S that starts with k_1 and ends with k_2.

The asynchronous circuit designer can be guided by Equation (3-2), when searching for an acceptable state variable assignment since it is usually possible to find an assignment by exhaustive search (i.e., examining all possible cases) which will require less than $2R_o - 1$ state variables. However, for circuits with more than eight internal states, such a search can become extensive* and the trend would be to employ a general method of assignment for larger circuits.

After state assignment has been made to a flow table, the excitation matrix can be written to represent the input signals for the elements used to physically implement the state variables. This is accomplished by assigning present state variable values to the stable states and next state values to the unstable transitory states. Figure 13 illustrates the excitation matrix for the state variable assignment shown in Figure 12. The excitation signals for the state variable elements can be read from the excitation matrix in Boolean algebra equation form. This solves the state variable assignment problem for the particular example considered in the above discussion. This example problem and associated description should provide insight into the state variable assignment problem and aid the reader in understanding the method presented in the next section.

---

*McCluskey and Unger (16) show that the state assignment possibilities for a nine state synchronous circuit with four state variables would number approximately 10.8 million. For asynchronous circuits, the number would be less due to the critical race elimination requirement, but the trial of all possible remaining cases would still represent a formidable task.

	y_1	y_2	y_3	X_1	X_2	X_3	X_4
q_1	0	0	0	(q_1)	q_2	q_1'	(q_1)
q_1'	0	0	1			q_3	
q_2	0	1	0	q_2'	(q_2)	(q_2)	q_1
q_2'	0	1	1	q_3'			
q_3	1	0	1	(q_3)	q_4	(q_3)	q_4
q_3'	1	1	1	q_3			
q_4	1	0	0	q_1	(q_4)	q_4'	(q_4)
q_4'	1	1	0			q_2	

(a) STATE ASSIGNMENT

Y_1, Y_2, Y_3 – represent next state values for $y_1 y_2 y_3$.

	y_1	y_2	y_3	X_1	X_2	X_3	X_4
q_1	0	0	0	(q_1) $Y_1\ Y_2\ Y_3$ 0 0 0	q_2 010	q_1' 001	(q_1) 000
q_1'	0	0	1	- - -	- - -	q_3 101	- - -
q_2	0	1	0	q_2' 011	(q_2) 010	(q_2) 010	q_1 000
q_2'	0	1	1	q_3' 111	- - -	- - -	- - -
q_3	1	0	1	(q_3) 101	q_4 100	(q_3) 101	q_4 100
q_3'	1	1	1	q_3 101	- - -	- - -	- - -
q_4	1	0	0	q_1 000	(q_4) 100	q_4' 110	(q_4) 100
q_4'	1	1	0	- - -	- - -	q_2 010	- - -

(b) EXCITATION MATRIX

Figure 13. Excitation Matrix

Fast Operating State Assignment

The state variable assignment used for the example problem in the preceding section did not meet the fast operating criteria presented in Chapter II. This criteria allowed only one state variable, y_i, to change during a transition from one stable state to another stable state. This requirement excludes the method of using cycling among unstable transitory states to avoid critical races. A general method for meeting the specified fast operating conditions with regard to state variable assignment is given in the following section.

Formulation of Technique

The circuit operating requirement imposed by the fast operating criterion specifies that only one state variable change during transition from one stable state to another stable state. A state assignment method which meets this requirement has been suggested by Huffman (11). To facilitate understanding of this method, it is convenient to introduce the following symbology:

S_i - The sets of state variable n-tuples $(y_1, y_2, \ldots, y_n)$ assigned to the internal states, q_i, of the circuit.

y_i - Binary-valued state variables.

q_i - Internal states of the circuit.

n - Number of state variables required in the assignment.

N - Number of internal states in the circuit.

R_o - Minimum number of state variables required to represent N internal states.

$\oplus$ - Symbol for modulo-two sum.

The method assumes the number of internal states involved to be a

power of two and requires N-1 state variables to represent the internal states. Therefore, $N = 2^{R_o}$ and the internal states are denoted by q_0, q_1, ..., q_{N-1}. To determine how the (N-1)-tuples for the y_1, y_2, ..., y_{N-1} state variables are to be assigned to the internal states, a group of R_o-tuples $(z_1, z_2, \ldots, z_{R_o})$ is formed. Each z_i is defined by the modulo-two sum of certain y_i state variables. The state variable y_i enters into the z_{R_o} modulo-two sum if the binary representation of i has a 1 bit in the least significant place. The state variable y_i is included in the z_{R_o-1} sum if i has a 1 bit in the second least significant place, etc.

Thus, the R_o-tuples $(z_1, z_2, \ldots, z_{R_o})$ can be formed as shown in the following set of equations:

$$
\begin{aligned}
z_{R_o} &= y_1 \oplus y_3 \oplus y_5 \oplus \cdots \\
z_{R_o-1} &= y_2 \oplus y_3 \oplus y_6 \oplus \cdots \\
z_{R_o-2} &= y_4 \oplus y_5 \oplus y_6 \oplus \cdots \\
&\vdots \\
z_1 &= y_{\frac{N}{2}} \oplus \cdots \oplus y_{N-2} \oplus y_{N-1}
\end{aligned}
\qquad (3\text{-}3)
$$

The decimal equivalents of the binary valued R_o-tuples $(z_1, z_2, \ldots z_{R_o})$ are then derived by assigning all possible tuple values to the y_i's involved in the modulo-two sums given by Equation (3-3). These decimal numbers will range from 0 to N-1. The S_i set of state variables y_i, y_2, ..., y_{N-1}, is obtained by assigning to S_i all the N-1 state variable tuples which give the decimal number equivalent of i to the R_o-tuple $(z_1, z_2, \ldots, z_{R_o})$. The set S_i of state variable tuples is then assigned to the internal state q_i. Miller (20) shows that the S_i

sets generated in this manner are intermeshed, thus it is always possible to obtain transition from one S_i set to another by changing only one y_i state variable. Therefore, this state variable assignment can be used for synthesizing a fast operating asynchronous circuit.

Example of Method

The method can be illustrated by assuming the number of internal states for a circuit to be four; i.e., q_0, q_1, q_2, q_3. Therefore, $N = 4$, $R_o = 2$ and $n = 3$. The state variables y_1, y_2, y_3 will be used to identify the internal states of the circuit. The R_o-tuples $(z_1, z_2, \ldots, z_{R_o})$ will be represented by the 2-tuple (z_1, z_2) which can be generated by:

$$z_2 = y_1 \oplus y_3$$
$$z_1 = y_2 \oplus y_3 \qquad (3\text{-}4)$$

The S_i sets of the state variables employed to represent the internal states q_i can be formed by considering the decimal equivalent values of the binary numbers represented by the 2-tuples (z_1, z_2). For instance, let

$$(y_1, y_2, y_3) = (0, 0, 0)$$

Equation 3-4 gives,

$$z_2 = y_1 \oplus y_3 = 0 \oplus 0 = 0$$
$$z_1 = y_2 \oplus y_3 = 0 \oplus 0 = 0$$

Binary Number	Decimal Equivalent

then $(z_1, z_2) = (0, 0) =$ 0

Thus, the 3-tuple $(y_1, y_2, y_3) = (0, 0, 0)$ would be assigned to set S_0. Likewise, if

$$(y_1, y_2, y_3) = (0, 0, 1)$$

then from Equation (3-4)

$$z_2 = y_1 \oplus y_3 = 0 \oplus 1 = 1$$

$$z_1 = y_2 \oplus y_3 = 0 \oplus 1 = 1$$

and

	Binary Number	Decimal Equivalent
(z_1, z_2)	(1, 1)	3

The 3-tuple $(y_1, y_2, y_3) = (0, 0, 1)$ would be assigned to set S_3. This operation for the total state assignment is summarized in the table shown in Figure 14(a). The state variable tuples are assigned to the internal state sets which have checks in the corresponding columns. Figure 14(b) gives a compact table representation for the state variable assignment.

If a circuit possesses eight internal states, the state variable assignment could be generated from the 3-tuple (z_1, z_2, z_3), where

$$z_3 = y_1 \oplus y_3 \oplus y_5 \oplus y_7$$

$$z_2 = y_2 \oplus y_3 \oplus y_6 \oplus y_7$$

$$z_1 = y_4 \oplus y_5 \oplus y_6 \oplus y_7$$

The procedure outlined above for the 4-state assignment could then be followed for obtaining the particular state assignments for the 7-tuples $(y_1, y_2, y_3, y_4, y_5, y_6, y_7)$.

If the number of internal states for a circuit is not a power of

STATE VARIABLE TUPLE (y_1, y_2, y_3)			z – TUPLE (z_1, z_2)		DECIMAL EQUIVALENT OF z-TUPLE	INTERNAL STATE SETS, S_i			
y_1	y_2	y_3	$z_1 = y_2 + y_3$	$z_2 = y_1 + y_3$		S_0	S_1	S_2	S_3
0	0	0	0	0	0	V			
0	0	1	1	1	3				V
0	1	0	1	0	2			V	
0	1	1	0	1	1		V		
1	0	0	0	1	1		V		
1	0	1	1	0	2			V	
1	1	0	1	1	3				V
1	1	1	0	0	0	V			

(a) STATE ASSIGNMENT GENERATION

y_3 \ $y_1 y_2$	00	01	10	11
0	0	2	1	3
1	3	1	2	0

Decimal numbers represent i subscript on S_i

(b) SUMMARY OF STATE ASSIGNMENT

Figure 14. Summary of Fast Operating State Variable Assignment for Four Internal States

two, the state variable assignment generated for the next largest power of two can be used to represent the circuit; i.e., if N = 3, then the state variable assignment for N = 4 could be used.

The use of the fast operating state variable assignment can be demonstrated by considering the problem of making state variable assignment to the reduced flow table in Figure 9.

For a circuit with four internal states, q_0, q_1, q_2, q_3, the state variable assignment can be obtained from the state variable chart in Figure 14(b) as

$$S_0$$

$$q_0 - (000), (111)$$

$$S_1$$

$$q_1 - (011), (100)$$

$$S_2$$

$$q_2 - (010), (101)$$

$$S_3$$

$$q_3 - (001), (110)$$

The S_1 sets contain two single connected sets from which any of the other states can be reached with only one y_i change. This can easily be seen on the 3-cube representation of the state variable assignment shown in Figure 15. The resulting flow table with state assignment is shown in Figure 16(b) and the excitation matrix for this assignment is given in Figure 17.

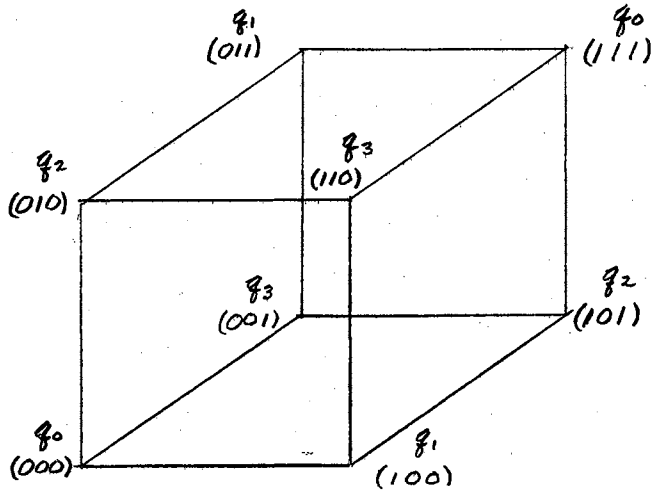


Figure 15. The 3-Cube Representation of State Variable Assignment for Four Internal States

Summary

The state variable assignment problem for asynchronous sequential circuits was discussed in this chapter. In general, this problem consists of making a state variable assignment to the internal states of an asynchronous circuit to provide uniqueness for each internal state and also assure that each circuit transition can be safely executed. An intuitive approach was employed to provide an example state variable assignment which satisfied the above two requirements. This state assignment utilized state splitting to achieve a safe assignment in which the state variables were cycled through unstable transitory states to avoid critical racing among the state variable elements. This state variable assignment example illustrated the general aspects of the state assignment problem encountered in the design of asynchronous circuits.

X_1	X_2	X_3	X_4
(q_0)	q_1	q_2	(q_0)
q_2	(q_1)	(q_1)	q_0
(q_2)	q_3	(q_2)	q_3
q_0	(q_3)	q_1	(q_3)

(a) REDUCED FLOW TABLE

	y_1	y_2	y_3	X_1	X_2	X_3	X_4
q_0	0	0	0	$[q_0]$	q_1	q_2	$[q_0]$
	1	1	1	$[q_0]$	q_1	q_2	$[q_0]$
q_1	0	1	1	q_2	$[q_1]$	$[q_1]$	q_0
	1	0	0	q_2	$[q_1]$	$[q_1]$	q_0
q_2	0	1	0	$[q_2]$	q_3	$[q_2]$	q_3
	1	0	1	$[q_2]$	q_3	$[q_2]$	q_3
q_3	0	0	1	q_0	$[q_3]$	q_1	$[q_3]$
	1	1	0	q_0	$[q_3]$	q_1	$[q_3]$

(b) FLOW TABLE WITH STATE ASSIGNMENT

Figure 16. Fast Operating State Variable Assignment

	y_1	y_2	y_3	X_1	X_2	X_3	X_4
q_0	0	0	0	(q0) $Y_1\ Y_2\ Y_3$ 0 0 0	q_1 1 0 0	q_2 0 1 0	(q0) 0 0 0
q_0	1	1	1	(q0) 1 1 1	q_1 0 1 1	q_2 1 0 1	(q0) 1 1 1
q_1	0	1	1	q_2 0 1 0	(q1) 0 1 1	(q1) 0 1 1	q_0 1 1 1
q_1	1	0	0	q_2 1 0 1	(q1) 1 0 0	(q1) 1 0 0	q_0 0 0 0
q_2	0	1	0	(q2) 0 1 0	q_3 1 1 0	(q2) 0 1 0	q_3 1 1 0
q_2	1	0	1	(q2) 1 0 1	q_3 0 0 1	(q2) 1 0 1	q_3 0 0 1
q_3	0	0	1	q_0 0 0 0	(q3) 0 0 1	q_1 0 1 1	(q3) 0 0 1
q_3	1	1	0	q_0 1 1 1	(q3) 1 1 0	q_1 1 0 0	(q3) 1 1 0

Figure 17. Excitation Matrix

In the fast operating requirements defined for fluidic circuit design in Chapter II, cycling of the state variables was not permitted. In the present chapter, a general method was reviewed which provided only one state variable change per transition from stable state to stable state thereby satisfying the defined fast operating requirement. This type of state variable assignment produces the fastest possible circuit action for given logic elements. Once the state variable assignment is made, the Boolean algebra equations representing the excitation signals for the state variable elements can be obtained. Equations for the external circuit outputs can also be written.

CHAPTER IV

COMBINATIONAL CIRCUIT IMPLEMENTATION

The assignment of a unique set of state variables to each internal state of an asynchronous circuit defines each total state as a unique combination of state variables and external inputs. This state variable assignment permits the external outputs for the circuit and the excitation signals for the internal state variable elements to be written as Boolean functions of the circuit total state. The resulting Boolean equations can then be used to design the combinational portion of the asynchronous circuit. This design is accomplished by implementing the equations with appropriate logic hardware to form physical circuits.

The designer is confronted with three major problems when deriving and physically implementing the combinational portion of an asynchronous circuit. First, the representative logic equations must be hazard-free to prevent erroneous circuit outputs during circuit input transitions. These erroneous outputs are caused by the imperfect logic properties of the physical components used to implement the circuit. Combinational circuit hazards are conventionally eliminated by the addition of more terms in a logic equation. The hazard elimination problem has been extensively studied and sufficient conditions for eliminating hazards are well known. Appendix C reviews the hazard elimination problem and

presents examples of techniques which can be employed to derive hazard-free logic equations.

A second problem encountered in combinational circuit implementation is that of economics. In general, increasing the complexity of a logic equation requires that additional hardware be used to implement the equation. This additional hardware usually increases the cost of the final circuit; therefore, the circuit designer must ordinarily consider minimizing the number of components employed in a circuit to reduce cost. A general solution to the problem of producing the most economical circuit using known cost components does not exist. However, the economics problem as related to fluidic circuit implementation does not appear to be critical since the cost of a fluidic circuit is not necessarily proportional to the number of components used to implement the circuit. Current manufacturing techniques are available for engraving fluidic circuits on relatively large plates at a fixed cost per plate.

Only when the size of the circuit creates the need for additional plates would the reduction of the number of elements included in a circuit affect the circuit cost. This unique cost feature can be used to advantage by the designer to simplify and generalize the asynchronous circuit design procedure and speed the operation of the circuit. Thus, economy by reducing a circuit to a minimum number of elements will not be considered in this work. The above cost feature for fluidic circuits was implicitly assumed in the state variable assignment method considered in Chapter III since permitting only one state variable change per stable state transition can increase the amount of hardware needed to implement a circuit.

The third problem which the combinational circuit designer must solve is that of minimizing the transmission delay of an input signal through the combinational circuit. The difficulty of this problem is usually increased by the limited number of inputs (i.e., limited fan-in) which can be connected to the individual logic elements. The use of limited fan-in elements creates the need for staging the elements when complex logic equations are implemented. Each stage added to the logic circuit increases the signal delay time through the circuit; therefore, for logic elements with known fan-in, it is necessary to minimize the logic stages required to implement a given logic equation to minimize the signal transmission delay.

This chapter will be principally concerned with solutions for the stage minimization problem when limited fan-in AND and OR logic elements are used to implement the combinational circuit. As in Chapter III, the emphasis will be on the description of known general methods which define sufficient conditions for solution. Definitions concerning the terminology used to describe the Boolean functions in the following sections are given in Appendix A.

Problem Definition

The objective of the implementation schemes considered will be to minimize the number of logic stages through which a signal must traverse to reach a circuit output. The following assumptions will be made in each of the cases considered:

1. AND and OR logic elements will be used to implement the circuit and each procedure will strive to decrease the number of logic stages required toward the absolute

minimum of two level AND-OR logic.

2. The equations to be implemented will be hazard-free.
3. The logic equation will be in sum of products form.
4. Each AND and OR logic element will have a signal transmission delay of Δ.
5. The transmission delay of the interconnecting lines between elements will be neglected.

Implementation With Unlimited Fan-in Elements

An example of implementing combinational AND-OR circuitry with unlimited fan-in elements will first be considered to illustrate the basic implementation problem. When the logic elements being used to implement the combinational circuitry have unlimited fan-in, the circuit can always be realized in two logic stages. The conjunctions required by each of the terms in the sum of products logic equation can be realized by one AND element and the summation of all terms can be implemented with one OR element. The signal delay for such a two-level AND-OR circuit would be 2Δ. If the logic equation being implemented contains more than one product term, this 2Δ delay represents the minimum delay which could ever be achieved with AND-OR implementation. The following example illustrates two level AND-OR logic implementation.

Example

Suppose a circuit output function is expressed by the equation

$$Z_1 = X_1\bar{X}_4\bar{X}_5 + X_1\bar{X}_3 + X_1X_5 + X_3X_4X_5 + \bar{X}_1\bar{X}_3\bar{X}_5 + \bar{X}_2X_3\bar{X}_4 + X_2\bar{X}_3\bar{X}_4X_5.$$

This equation can be implemented in two level logic form by the circuit shown in Figure 18. Each literal in each conjunction represents an input to an AND element. Each term of the equation represents an input to an OR element. The cumulative delays involved in passing through the logic circuit are represented by the delay numbers written on each of the element outputs. It can be readily seen that the output Z_1 of the circuit has a cumulative delay of 2.

Circuit implementation with unlimited fan-in elements is hypothetical since there will always be a bound on the number of inputs which a single element can handle. This is particularly true for fluidic elements since fan-in capabilities of commercially available AND and OR fluidic elements are limited from approximately two to four inputs.

Implementation With Limited Fan-in Elements

A method which provides a solution to the problem of obtaining minimum stage AND-OR circuits with arbitrarily specified fan-in elements has been developed by Hicks and Bernstein (9). The problem is separated into two basic parts:

1. Obtaining a minimum stage circuit without factoring the Boolean equation.
2. Investigating the possibilities of reducing the number of required stages by factoring common literals from terms of the Boolean equation.

The method developed for use with the unfactored Boolean equation is a general (non-trial and error) technique for providing an upper bound on the number of stages required to implement a circuit. If

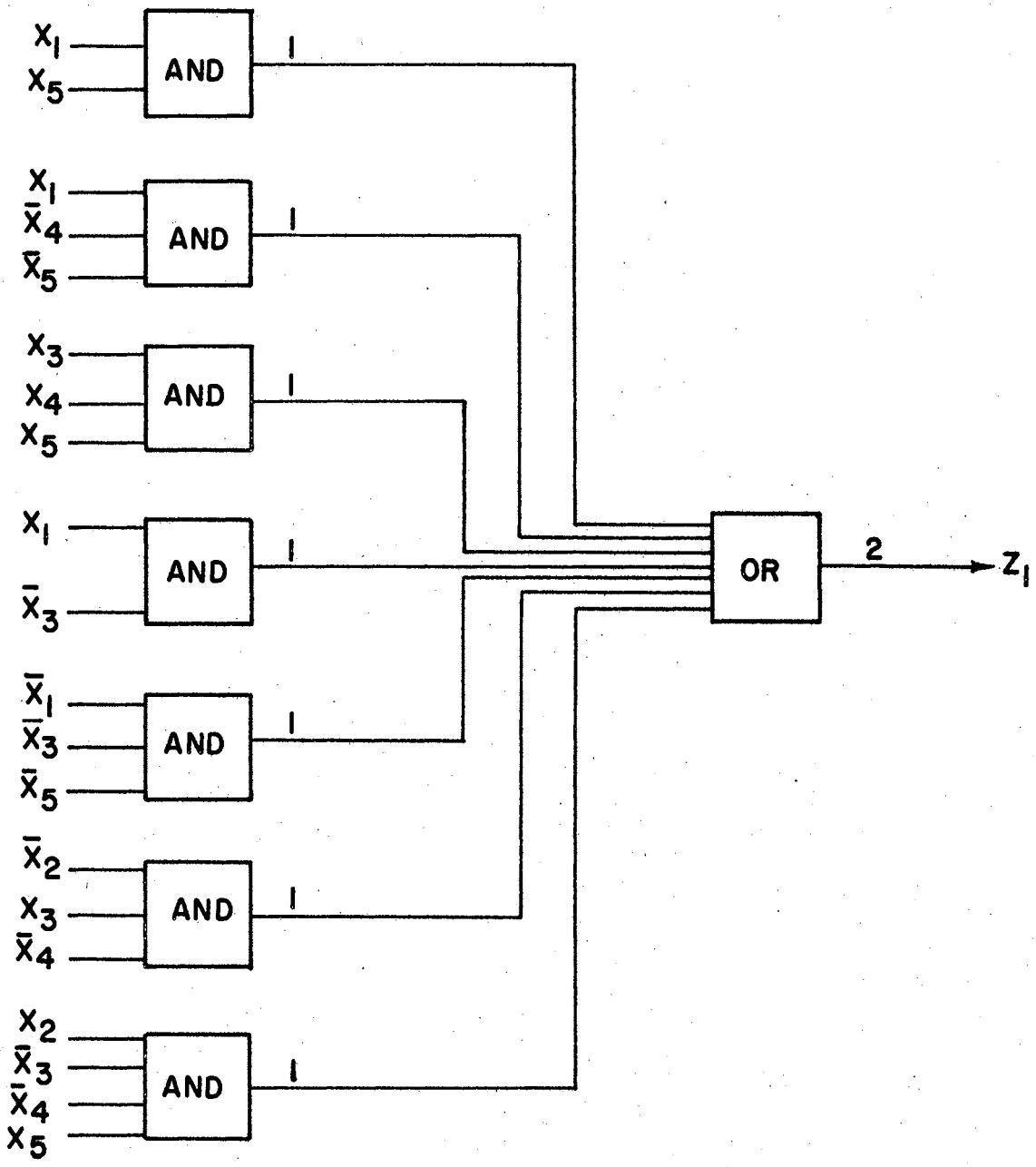


Figure 18. Implementation With Unlimited Fan-in Elements

factoring of the equation is performed, the required number of stages may or may not be further reduced. Factoring the equation becomes a very detailed and laborious procedure since all factorizations which have a possibility of reducing the required number of circuit stages must be investigated to assure that a minimum solution is obtained. General guidelines for the procedure can be established; however, a general method is not available. Due to the trial and error nature of the factoring problem, it will not be considered further, but stage reduction possibilities by factoring should not be forgotten. The details of the Hicks and Bernstein method for obtaining a minimum stage circuit without factoring the Boolean equation will be considered in the remainder of this chapter.

The results of this method can be used to obtain an estimate of the maximum delay time required for an input signal to travel through the combinational portion of an asynchronous circuit. In addition, the maximum and minimum times required for a signal to transmit through the AND stages of the combinational circuit can be approximated. As shown in Chapter V, these delay times are all that are needed to estimate the timing requirements for the feedback delay elements and the external input operating frequency limitations which will assure proper operation of the over-all asynchronous circuit.

State Minimization Without Factoring

If the Boolean equation representing a logic function is left in unfactored form, two possibilities exist for implementing the equation with minimum state AND-OR logic. The equation can be implemented in an optimum number of stages or a minimum non-optimum number of stages must

be used. The criteria for determining if an optimum solution is possible depends on the relative complexity of the Boolean equation with respect to the fan-in capabilities of the logic elements being employed in the implementation. Conditions for optimum and non-optimum solutions will be considered in the following sections.

Optimum Solution

When the logic function to be implemented meets certain conditions imposed by the fan-in requirements of the logic elements used in the implementation, the function can be realized in an optimum number of stages. To develop the conditions required for optimum realization, consider the requirements for realizing the conjunctions represented by the terms of a sum of products logic equation. If the maximum fan-in capability of each AND element is denoted by a, then the conjunction of not more than a^y literals can be accomplished in y logic stages. In general, if N represents the number of literals in a conjunction, then the following condition will hold:

$$a^{(y-1)} < N \leq a^y \qquad (4\text{-}1)$$

An example of this condition is shown in Figure 19 for the conjunction $X_1\bar{X}_2X_3\bar{X}_4X_5$ implemented with AND elements with fan-in limitations as shown in the figure. This example clearly shows that the signal delay through the AND portion of an AND-OR combinational circuit is a function of the fan-in capabilities of the elements used in the implementation.

After the conjunctions for the terms of a sum of products logic equation are formed according to Equation (4-1), an optimum method is needed for summing the conjunctive terms with limited fan-in OR

elements so that the total combinational circuit delay is minimized. To formulate the method for staging the limited fan-in OR elements, the following quantities will be defined:

n - fan-in for the OR gates.

k_i - number of conjunctive delays of delay i.

m - largest delay of the conjunctions formed by staging the AND elements.

s - shortest delay of the conjunctions formed by staging the AND elements.

The minimum delay which can ever be accomplished for an AND-OR circuit will be m + 1. The additional 1 delay comes from the OR

(a) For $X_1\bar{X}_2X_3\bar{X}_4X_5$,

N = 5

Let, a = 2,

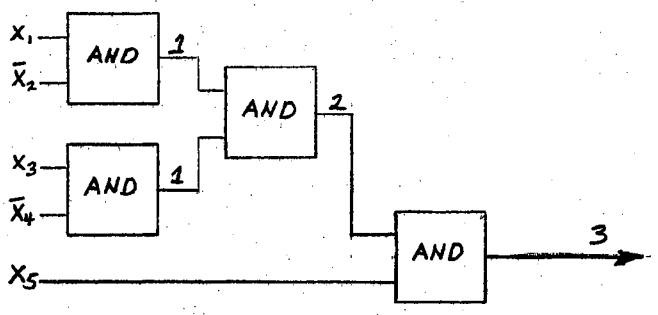
Then Equation (4-2) gives

$a^{y-1} < N \leq a^y$

$4 < 5 \leq 8$

for $y = 3$

The resulting 3-stage circuit is



(b)

Let, a = 3

Then Equation (4-2) gives

$a^{y-1} < N \leq a^y$

$3 < 5 \leq 9$

for $y = 2$

The resulting 2-stage circuit is

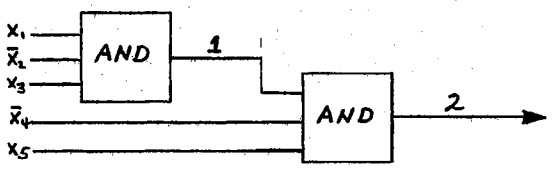


Figure 19. Example of Limited Fan-in AND Elements

element which must be used to complete the function by summing the conjunctions. Thus, the objective of the designer will be to realize a logic function in m + 1 logic stages using given fan-in OR elements. The realization of a sum of products function in m + 1 stages is defined as an optimum implementation. Hicks and Bernstein prove sufficient conditions for a particular sum of products function to be realized optimally. These conditions are:

$$1.\quad k_a \leq n$$

$$2.\quad k_i \leq n-1 \quad \text{for } a < i \leq m \qquad (4\text{-}2)$$

The implications of these conditions can be illustrated by example.

Consider implementing the Boolean function,

$$f = X_1X_2\bar{X}_3 + \bar{X}_3X_4 + \bar{X}_1\bar{X}_2\bar{X}_3 + X_2X_3 + \bar{X}_1X_3 + X_1\bar{X}_2X_3\bar{X}_4X_5 \qquad (4\text{-}3)$$

Solutions for different fan-in limits are presented in the following examples:

Example 1

Let $a = 2$; $n = 3$

As determined by Equation (4-1), the conjunction delays for Equation (4-3) would be

$(\bar{X}_3X_4)$	(X_2X_3)	$(\bar{X}_1X_3)$	$(X_1X_2\bar{X}_3)(\bar{X}_1\bar{X}_2\bar{X}_3)$		$(X_1\bar{X}_2X_3\bar{X}_4X_5)$
1	1	1	2	2	3

Therefore:

$$a = 1 \; ; \; m = 3$$
$$k_a = k_1 = 3 \; ; \; k_2 = 2 \; ; \; k_m = k_3 = 1$$

Employing the conditions of Equation (4-2) yields

$$k_a \leq n \quad (i.e., \; 3 \leq 3)$$
$$k_i \leq n-1 \quad for \; 1 < i \leq 3$$

Thus, it is assured that the function can be realized optimally in m + 1 or 4 stages. A possible circuit implementation is shown in Figure 20.

Example 2

Let: $a = 2 \; ; \; n = 2$

From Example 1,

$$a = 1 \; ; \; m = 3$$
$$k_a = 3 \; ; \; k_2 = 2 \; ; \; k_m = 1$$

The conditions specified by Equation (4-2) cannot be met for this OR fan-in limitation and it may not be possible to implement the circuit in 4 stages. Examination of various possibilities indicate that a 4-stage implementation is impossible, thus a non-optimum solution with a minimum number of OR stages will be needed. A method for achieving this type of solution is described in the next section.

Non-Optimum Solution

When the conditions for optimal circuit implementation as defined by Equation (4-2) are not satisfied and an optimal solution cannot be found for m + 1 logic stages, the objective will be to achieve an implementation with the minimum possible number of additional OR stages. To formulate a procedure which gives a minimum number of stages for the

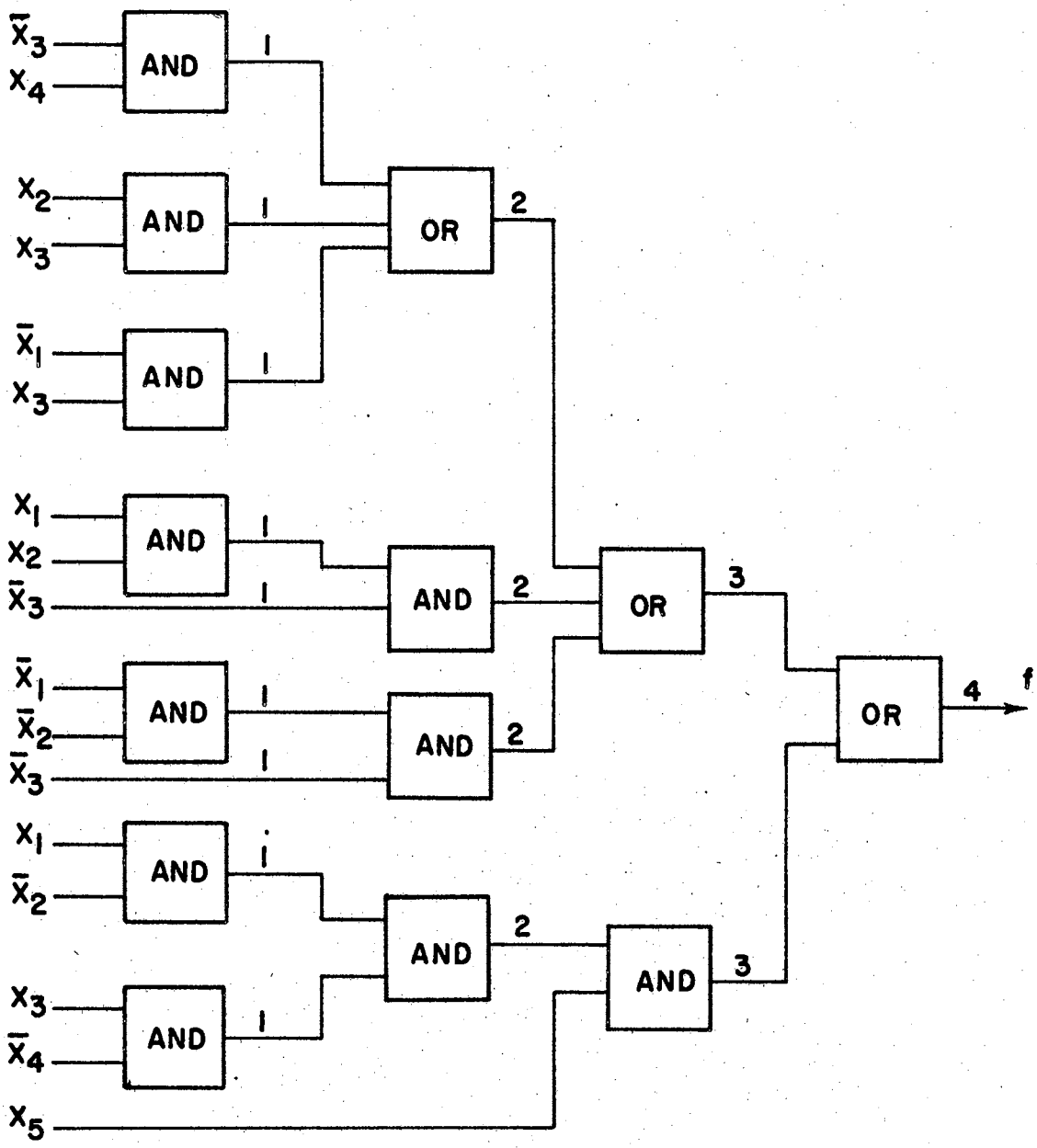


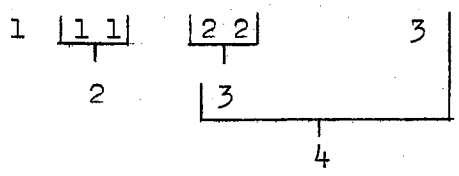
Figure 20. Optimum Solution for Limited Fan-in Logic Elements

non-optimum case, an input of delay i is defined as a connection in a circuit such that the largest number of logic stages between this connection and an external circuit input is i. It should be understood that the i delays can be formed either by conjunctions only or by a disjunction of conjunctions since the delays of the AND and OR elements are assumed equal. For a function with a $k_i > (n-1)$, where $a \leq i \leq m$, it has been proven that a minimum delay realization exists for the function if OR gates with n inputs of equal delay i are included in the implementation (9).

Therefore, to form a minimum stage circuit when $k_i \geq n$, OR elements will first be employed with n inputs of delay i. This procedure is repeated for all other j delays when $k_j \geq n$. An illustration of this procedure can be shown by considering again the problem posed in Example 2 of the previous section. The i delays of the conjunctions formed by the AND gates which had to be implemented with disjunctions were:

1 1 1 2 2 3

The fan-in for the OR gates was defined to be n = 2. To implement the circuit in a minimum number of stages, the scheme would be to implement one OR gate with two inputs of delay 1, another with two inputs of delay 2, and another with two inputs of 3. The remaining disjunctions required to complete the circuit can be made according to the optimum procedure described in the previous section. The over-all implementation of the example circuit would be as follows:



The remaining delays are: 1 2 4. These can be implemented in an optimum manner or m + 1 stages where m is now defined as 4. The schematic diagram for the minimum stage circuit is shown in Figure 21.

A physical interpretation of the above minimization procedure can be seen if the number k_i is written as a base n number. The least significant digit in the base n number indicates the number of original i delays which does not have to be included in the implementation of the OR gates with n inputs of delay i. The second digit in the base n number provides the number of n-input disjunctions which can be used to yield an output with i + 1 delay. The third digit indicates the number of subcircuits with n-input disjunctions which would be used to form an output with i + 2 delay. The number of original i delay inputs included in this subcircuit would be $(n)^2$. The more significant digits of the base n number can be similarily interpreted.

To illustrate this physical interpretation of the circuit structure, let n = 2 and k_i = 7. The number k_i written as a base 2 number would be:

1 1 1

The least significant digit of this number shows that one of the original i delays in the circuit is undisturbed in forming the two input OR gates of delay i. The second digit indicates that one OR gate with two inputs of delay i will be employed to form a disjunction of i + 1 delay. The third digit is interpreted as requiring one subcircuit of delay

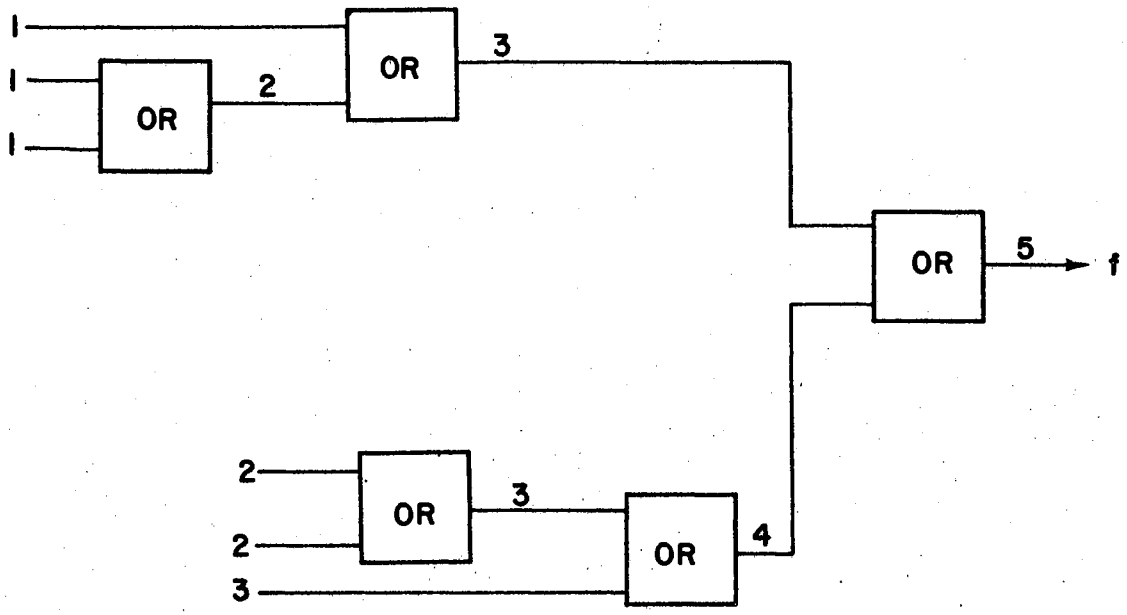


Figure 21. Minimum Solution for Limited Fan-in Elements

i + 2 formed with two-input disjunctions as shown in Figure 22. Four of the original i delay inputs are included in the subcircuit.

The reason for the above interpretation can be seen by considering a general k_i written as a base two number.

$$k_i = b_j(2)^j + \cdots + b_3(2)^3 + b_2(2)^2 + b_1(2)^1 + b_0(2)^0$$

The powers on 2 can be related to the delay which will be added to i if a 1 digit appears in that column. The decimal values of 2 raised to the given powers indicate the number of i delays which are involved in the subcircuitry that must be formed if a 1 appears in that column. If k_i is multiplied by $(2)^i$, then the exponents of 2 will represent the actual delays which will exist in the circuit due to the implementation of k_i delays of delay i. The number of digits in this resultant product represents the number of stages required to implement k_i delays of delay i. The product $k_i(2)^i$ would be of the form

$$k_i(2)^i = b_j(2)^{j+i} + \cdots + b_3(2)^{3+i} + b_2(2)^{2+i} + b_1(2)^{1+i} + b_0(2)^i$$

For an example of $k_i = 7$ and i = 1, the $k_i(2)^i$ product would be

$$7(2)^1 = (111)(10) = 1110$$

Thus, the minimum number of stages required to implement 7 delays of delay 1 would be 4. It should be remembered that the $k_i(2)^i$ product formed using base 2 arithmetic pertains only to OR elements with a fan-in of 2.

To minimize the number of stages required to implement an over-all

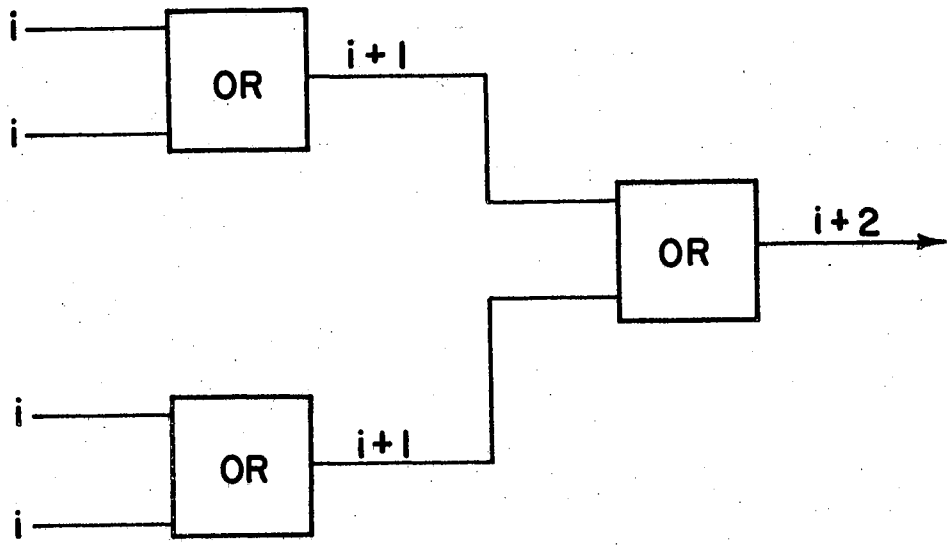


Figure 22. Subcircuit of Delay i + 2 for an OR Fan-in of 2

circuit, the $k_i(2)^i$ products can be summed using base 2 arithmetic. The number of digits in the resultant sum will represent the minimum number of stages required to implement the circuit. An exception occurs when the sum is 1000--0. Then, the minimum number of stages required will be one less than the number of digits in the sum. This procedure can be illustrated by reconsidering a previous example. Let n = 2 and the delays of the conjunctions be defined as:

1 1 1 2 2 3

A table can be formed to show the operations involved in obtaining the $k_i(2)^i$ summations. This table is given in Figure 23. The number of digits in the summation of $k_i(2)^i$ products is five. This corresponds to the number of stages required in the minimum solution of the example problem illustrated in Figure 21.

i	k_i	k_i BASE 2	$k_i \cdot (2)^i$ BASE 2	$k_i \cdot (2)^i$ BASE 2
1	3	11	(11)(10)	110
2	2	10	(10)(100)	1000
3	1	01	(01)(1000)	1000
			$\sum_{i=0}^{m} k_i(2)^i$	= 10110

Figure 23. Procedure for Forming $k_i(2)^i$ Sum

It is convenient to assign a delay number representation to the digits in the $k_i(2)^i$ sum of the form $D = d_r d_{r-1} \cdots d_1 d_0$. The value of each r subscript in the delay number corresponds to the ith delay involved in the circuit implementation. In forming the $k_i(2)^i$ summation, a carry in the ith column of the summation indicates that a disjunction must be formed with 2 subfunctions of delay i.

The stage minimization procedure can be generalized to handle OR gate fan-ins of n if the summation of $k_i(n)^i$ is formed by doing the required multiplication and addition operations in base n arithmetic. The number of digits in the sum will give the minimum number of stages required to implement a given logic function with known fan-in elements if no factoring of the representative Boolean equation is performed. The one exception to the rule is when the sum is 1000..0. Then, the number of stages required will be one less than the number of digits in the sum. An example will illustrate the above procedure for n = 3.

Example

Assume the circuit to be implemented requires conjunctions with the following delays:

2222 444444 33333 55

For n = 3, the $k_i(n)^i$ summation procedure in base 3 arithmetic* can be summarized in Figure 24.

The delay number is 1120100. The number of digits in the delay number is 7, thus seven stages are required to implement the circuit.

---

*See Appendix B for base 3 conversion procedures and the addition and multiplication tables required to perform base 3 arithmetic.

The OR portion of a possible resultant circuit is shown in Figure 25.

i	k_i	k_i BASE 3	$k_i \cdot (3)^i$ BASE 3	$k_i \cdot (3)^i$ BASE 3
2	4	11	(11)(100)	1100
4	6	20	(20)(1000)	200000
3	5	12	(12)(1000)	12000
5	2	2	(2)(100000)	200000

$$\sum_{i=2}^{m} k_i(3)^i = 1120100$$

Figure 24. Procedure for Forming $k_i(3)^i$ Sum

Summary

To utilize the fast operating capabilities of asynchronous circuits, it is necessary to minimize the signal delay through the combinational circuit portion of the circuit. This signal delay minimization can be achieved by reducing the number of logic stages through which a signal must pass to produce an output. This chapter has described methods for implementing minimum stage combinational circuitry with limited fan-in AND and OR logic elements from unfactored logic equations.

Sufficient conditions are defined for realizing a circuit in an optimal number of stages with given fan-in elements. These conditions are dependent on the number of equal conjunction delays which must be

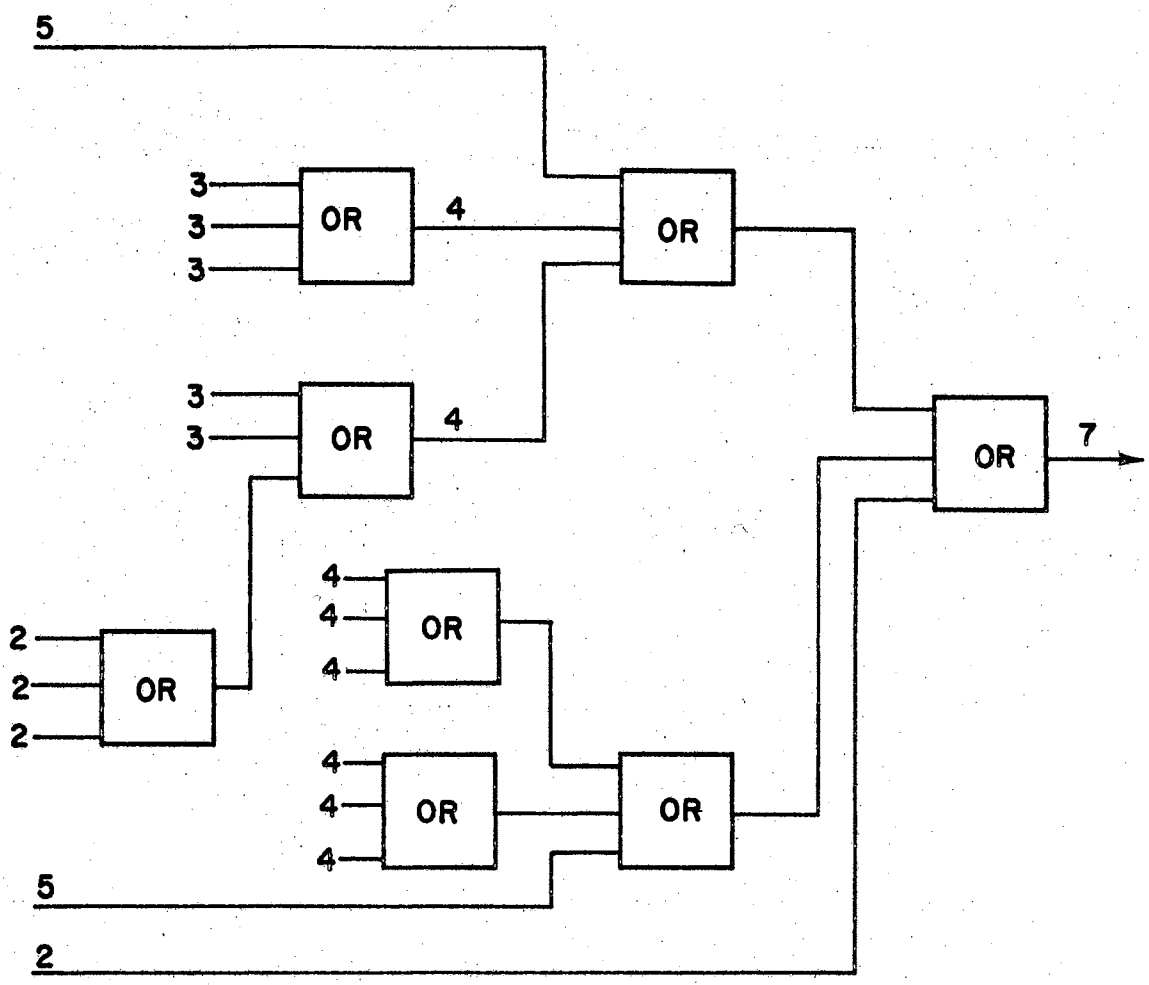


Figure 25. Minimum Stage Implementation for n = 3

summed with given fan-in OR elements. For conditions that do not permit an optimal solution, a general procedure is developed which will yield a minimum stage non-optimal solution.

The circuit implementation procedures presented in this chapter provide an estimate of both the maximum total signal delay encountered in the combinational circuit and the maximum and minimum signal delays experienced in the AND portion of the combinational circuit. These delay times will be employed in Chapter V to provide information needed in determining the timing requirements for the feedback delay elements and the maximum frequency of the external input changes in the circuit.

CHAPTER V

ASYNCHRONOUS CIRCUIT TIMING REQUIREMENTS

After the combinational circuit portion of an asynchronous circuit has been designed, the timing requirements to assure proper operation of the over-all asynchronous circuit can be determined. The physical timing requirements for the asynchronous circuit were given in Chapter II as:

1. Providing delay values in the state variable feedback elements such that the combinational circuit disturbances created by an external input change could settle before the state variable signal y would change.
2. Restricting the external input change frequency so that the total circuit disturbance caused by a previous external input could settle before another external input was changed.

Unger (30) has shown the need for the feedback delay if essential hazards* are present in the flow table which represents the circuit. Essential hazards are commonly encountered in most flow tables, thus feedback delay will be assumed necessary. Erroneous stable states can result in an asynchronous circuit if extraneous external inputs are allowed to mix with transitory signals occurring within the circuit

*Essential hazards are defined in Appendix C.

during a transition. Therefore, the external input change frequency to the circuit must be restricted. Huffman (12) and Miller (20) state the timing requirements for the asynchronous circuit, but neither give methods for determining these requirements. Other authors have usually ignored the timing problems which must be considered in the design of asynchronous circuits.

Accurate timing requirements for an asynchronous circuit can be determined by experimental trial and error measurement once the combinational portion of the circuit has been physically implemented. It is possible, however, to obtain estimates of the asynchronous circuit timing requirements in the preliminary stage of the design. One such method would be to trace the delays on a circuit diagram while following the circuit action on the reduced flow table. This would provide an accurate description of the required timing for the feedback delay elements and the input frequency change restrictions without physically constructing the circuit. However, this delay tracing procedure could be very laborious for relatively large circuits since many transitions and circuit paths would have to be examined.

A method of determining proper asynchronous circuit timing requirements from the delay properties of the Boolean algebra equations representing the combinational circuit would be useful for design estimates and evaluations. This chapter will present an original method which can be used to predict these timing requirements from the representative Boolean equations. The timing estimates obtained by this method will assure the designer that an asynchronous circuit can always be constructed to operate safely at an external input frequency not less than the predicted value.

Problem Definition

The objective of the first method formulated in this chapter will be to determine the timing requirements for the feedback delay elements of an asynchronous circuit such that proper over-all circuit action will occur. Once the feedback element delays are determined, the maximum safe operating frequency for the circuit can be estimated. A method for approximating this limiting frequency will also be presented.

To formulate the methods for estimating the asynchronous circuit timing requirements, the following assumptions are made:

1. The combinational portion of the asynchronous circuit will be implemented as a minimum stage AND-OR circuit according to the procedure described in Chapter IV.
2. Only one state variable element will be allowed to change during a stable state transition.
3. Only one external input signal will be allowed to change at a time.
4. The turn-off time of a combinational circuit element will be assumed equal to the turn-on time.
5. The delay times for the AND and OR elements used to implement the combinational circuit are assumed equal. For the purpose of simplifying the presentation, this assumption ignores the stray delay switching properties of the combinational circuit elements, however; the essential timing requirements for designing a safe operating asynchronous circuit are adequately displayed.

It is convenient to introduce the following nomenclature and

definitions for use in describing the circuit timing requirements:

X - The external inputs to the asynchronous circuit.

Y - The state variable excitation signals in an asynchronous circuit

Z - The external output signals from the asynchronous circuit

S - the set signal to a set-reset flip-flop

R - the reset signal to a set-reset flip-flop

y - The state variable signal in an asynchronous circuit

i - Subscript used for external inputs X

j - Subscript used for internal state y

m - Subscript used for external output Z

Δ_{fj} - The delay time for the jth state variable feedback element

Δ_{fSj} - The delay time for the set signal S_j of the jth S-R flip-flop element

Δ_{fRj} - The delay time for the reset signal R_j of the jth S-R flip-flop element

Δ_{Yj} - The maximum combinational circuit delay for the state variable excitation signal Y_j

Δ'_{Yj} - The minimum combinational circuit delay for state variable excitation signal Y_j

Δ_{Sj} - The maximum combinational circuit delay for the jth state variable set signal S_j

Δ'_{Sj} - The minimum combinational circuit delay for the jth state variable set signal S_j

Δ_{Rj} - The maximum combinational circuit delay for the jth state variable reset signal R_j

Δ'_{Rj} - The minimum combinational circuit delay for the jth state variable reset signal R_j

Δ_z - The maximum combinational circuit delay of external output signal Z

Δ_T - The maximum total settling time of the asynchronous circuit after a disturbance due to changing any of the external input values

Δ_{TS} - The maximum total combinational circuit delay required to produce all excitation signals S

Δ_{TR} - The maximum total combinational circuit delay required to produce all excitation signals R

Δ_{TY} - The maximum total combinational circuit delay required to produce all excitation signals Y

δ_{AY} - The maximum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce excitation signal Y

δ_{AZ} - The maximum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce signal Z

δ'_{AY} - The minimum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce excitation signal Y

δ_A - The maximum delay experienced by any signal traversing the AND circuit in the combinational circuit

δ_{AS} - The maximum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce the excitation set signal S

δ'_{AS} - The minimum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce the excitation set signal S

δ_{AR} - The maximum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce the excitation reset signal R

δ'_{AR} - The minimum delay experienced by a signal in traversing the AND portion of the combinational circuit to produce the excitation reset signal R

Timing Requirements for the Feedback Delay Elements

The requirement for timing a particular jth feedback delay element can be obtained by considering the settling time for the combinational circuit disturbances caused by the external input signals which produce the excitation signal Y_j. A schematic of the signal paths which could be disturbed by a change in external input signal X_i are shown in Figure 26. Referring to Figure 26, it can be seen that the external input signal X_i must pass through the AND-OR combinational circuit to produce the excitation signal Y_j. The jth feedback delay element is actuated by signal Y_j after delay Δ_{fj} and produces state variable signal y_j. Signal y_j then enters the combinational circuit to set the AND portion of the combinational circuit to receive the next external input

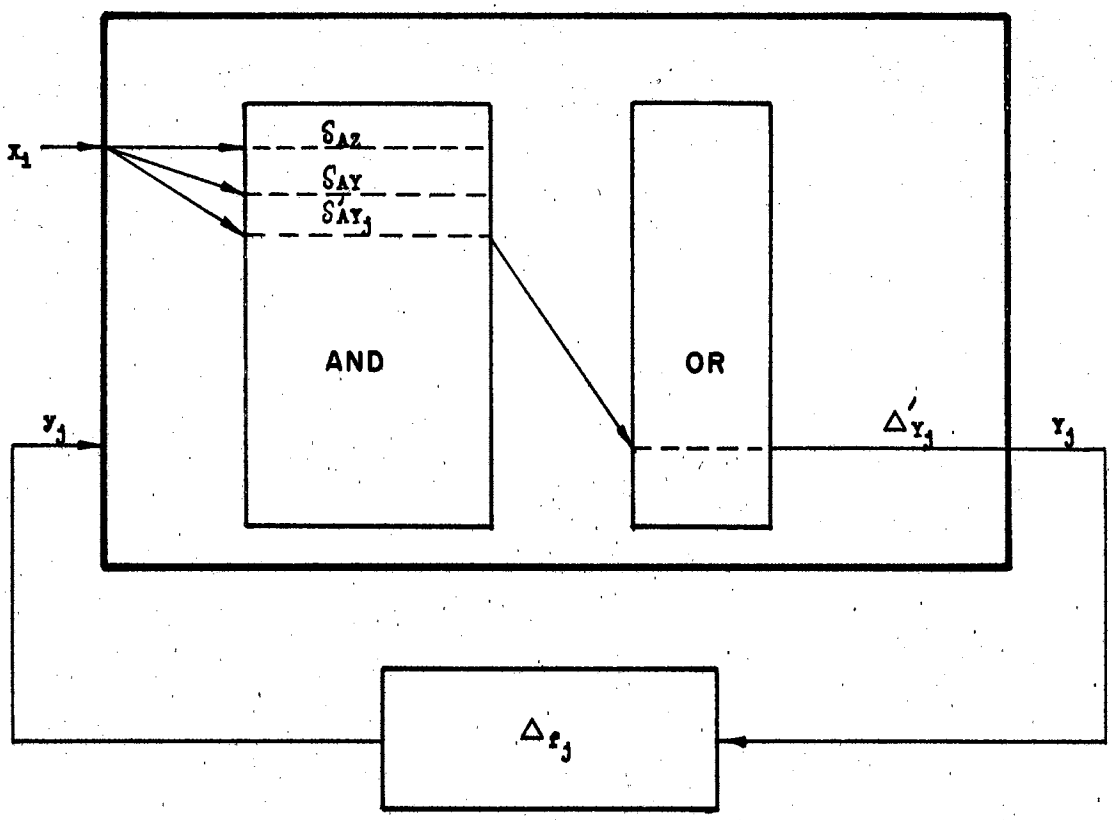


Figure 26. Signal Paths for External Input Signal X_i and State Variable Signal y_j

signal and possibly to create external output signals.* To assure correct circuit action, the feedback delay Δ_{fj} must be properly adjusted to prevent the signal y_j from entering the combinational circuit before the disturbance created in the AND circuitry by external input X_i has settled. All the Z and Y AND circuits which are functions of the external input X_i would be disturbed by the X_i input change. Since Y_j would, in general, be a function of more than one external input, all the disturbances created by the X_i's for which Y_j was dependent would have to be considered in determining the longest AND circuit disturbance created in producing signal Y_j.

From these considerations, the necessary delay time for the jth feedback element can be determined. In particular, the jth feedback element delay plus the minimum delay experienced by any X_i input signal in traversing through the combinational circuit to produce signal Y_j must be greater than the maximum time required for the Y and Z AND circuitry to settle after being disturbed by the external input signal. All X_i's for which Y_j is a function would have to be considered, and the value for the feedback delay would be chosen as the maximum delay value which occurred for all possible cases. This timing criterion is conservative since it does not account for the possibility of different input signals creating the minimum and maximum signal delays which define the timing requirement. A more accurate determination could be obtained by making a detailed study of the transition behavior of the circuit. However, when the complexity of all the involved Y and Z

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*External output signals will be created by the y_j signal if an external output is specified to change at the end of a transition.

equations is comparable, the answers given by the method for the above defined criterion would closely approximate the results of a detailed circuit study.

To formulate equations for determining the feedback delay value, refer to Figure 26. The minimum delay ever required for an external signal X_i to produce signal Y_j would never be less than the minimum delay, Δ'_{yj}, through the AND and OR stages of the combinational circuit. If the Boolean equation representing Y_j has more than one product term, this minimum delay Δ'_{yj} would be determined by

$$\Delta'_{Y_j} = \delta'_{AY_j} + 1 \tag{5-1}$$

where:

δ'_{AY_j} is the minimum delay of signal Y_j through the AND portion of the combinational circuit. The 1 is due to the requirement that at least one OR gate be between the AND circuit output and the Y_j signal output.

If the Boolean equation representing Y_j possesses only one product term, the delay Δ'_{Y_j} would be

$$\Delta'_{Y_j} = \delta'_{AY_j} \tag{5-2}$$

The maximum settling time ever required for the Z AND circuits could be determined by examining the maximum AND delays for all the Z equations that were functions of the internal inputs X_i for which Y_j was dependent. The maximum settling time determined in this manner will be denoted by the delay, δ_{AZ}. Therefore,

$$\delta_{AZ} = \underset{Z(X_i)}{MAX} \left(\delta_{AZ\,Z(X_i)} \right) \tag{5-3}$$

where: X_i includes all the X_i's for which Y_j is dependent.

In a similar manner, the maximum time which would ever be incurred by the settling of a Y AND circuit which was a function of the X_i's for which Y_j was dependent, could be determined as

$$\delta_{AY} = \underset{Y(X_i)}{MAX}\left(\delta_{AY_{Y(X_i)}}\right) \tag{5-4}$$

The maximum delay between the two values defined by Equations (5-3) and (5-4) can be denoted by

$$\delta_A = MAX(\delta_{AZ}\ ;\ \delta_{AY}) \tag{5-5}$$

Therefore, the timing requirement for the jth feedback element could be determined from the relationship

$$\Delta_{fj} + \Delta'_{yj} > \delta_A$$

or

$$\Delta_{fj} > \delta_A - \Delta'_{yj} \tag{5-6}$$

Since Equation (5-6) by nature is conservative, a safe value for the feedback delay value could be obtained by equating this delay value to $\delta_A - \Delta'_{yj}$. Therefore,

$$\Delta_{fj} = \delta_A - \Delta'_{yj} \tag{5-7}$$

Both of the quantities on the right hand side of Equation (5-7) can be determined from the results of the AND-OR combinational circuit implementation scheme presented in Chapter IV. Thus, Equation (5-7) allows the designer to obtain an assured safe estimate on the required feedback delay time by considering only the Boolean equations which represent the

combinational circuit and the fan-in capabilities of the elements used to implement the combinational circuit.

Determination of the External Input Frequency Limitation

When the feedback element delay requirements for the asynchronous circuit have been determined, a maximum external input frequency can be established for external input changes which will assure safe operation of the circuit. The method for estimating this safe operating frequency is based on determining the longest time ever required for the circuit to settle after an external input is changed. To develop the method for determining this maximum circuit settling time, the time at which the external outputs of the circuit are specified to change during a circuit transition must be considered. In general, the external outputs of an asynchronous circuit can be specified to change either at the beginning or at the end of a state transition. The circuit settling times for both output change specifications will be considered in the following sections.

External Output Change Specified at the End of a Transition

When the external output changes are specified at the end of a circuit transition, the signal paths in the general asynchronous circuit model will be as shown in Figure 27. The external output can be seen to be a function of the state variable signal which changes during the transition. This dependency usually slows the circuit output response since the state variable element must change before the external output signal can be produced.

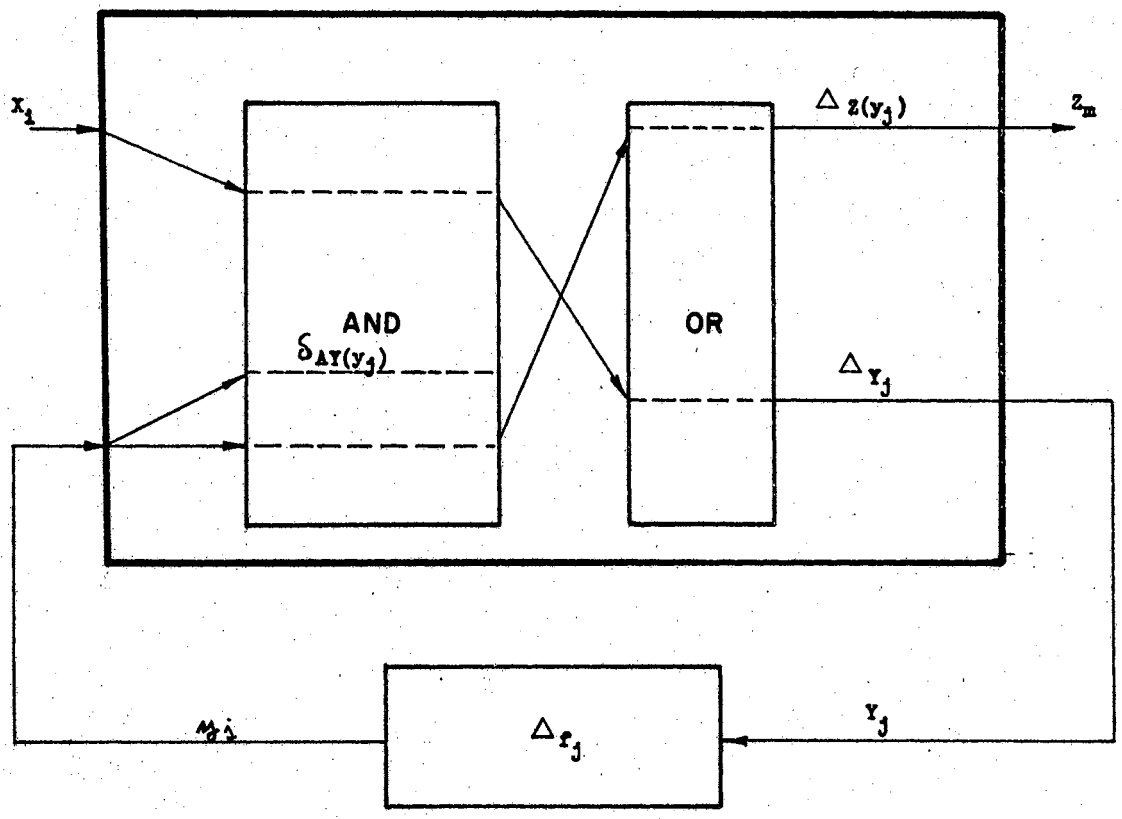

Figure 27. Signal Paths When the External Outputs are Specified to Change at the End of a Transition

Also, the permissible operating frequency can be decreased by this type of output specification. This is due to the additional time which must be allowed for the state variable signal to traverse the entire combinational circuit to produce the external output signal before the external input signals to the circuit can be changed. The maximum settling time of an asynchronous circuit can be estimated by determining the maximum delay which could ever be experienced within the circuit during all possible circuit transitions.

The circuit settling time for a change in external input X_i can be determined by tracing the delays which the signals, that are created by the external input change, experience as they traverse the asynchronous circuit model shown in Figure 27. Referring to Figure 27, it can be seen that the maximum delay required for an external input signal to create state variable signal Y_j would be Δ_{Yj}. The Y_j signal would be delayed by Δ_{fj} due to the feedback delay element and then signal y_j would be created. This y_j signal would re-enter the combinational circuit and could experience a maximum delay of $\Delta_{Z\,z(y_j)}$ in creating an external output signal Z_m. The y_j signal would also disturb all Y AND circuits which were functions of y_j. The maximum delay time required for these Y AND circuits to settle due to a y_j disturbance would be $\Delta_{AY\,y(y_j)}$. The settling time required for the complete circuit to settle due to an X_i input change that produced a state variable signal y_j would be given by appropriately summing the above described individual delay values. For example, the total maximum circuit settling time for external input X_i would be obtained by choosing the maximum of the following two sums:

$$\Delta_{Yj} + \Delta_{fj} + \Delta_{Z\,z(y_j)}$$

or

$$\Delta_{y_j} + \Delta_{f_j} + \delta_{AY\,Y(y_j)}$$

where: The y_j's involved would be all the y_j's which are functions of X_i.

Similar maximum settling times could be determined for all external input changes. Then the maximum of all these times would be chosen as the value to be employed in determining the maximum frequency at which the circuit could be safely operated. A procedure for performing these operations is given in the following discussion.

The various individual maximum state variable signal delays which can exist in the combinational circuit will first be determined. The maximum delay that a particular state variable signal y_j would ever experience in producing an external output signal could be determined by examining all Z equations which are functions of y_j. The operation for determining this maximum delay can be represented by

$$\Delta_{Z(y_j)} = \underset{Z(y_j)}{MAX} \left(\Delta_{Z\,Z(y_j)}\right) \tag{5-8}$$

where: $Z(y_j)$ - denotes all Z outputs that are functions of y_j.

$\Delta_{Z(y_j)}$ - the maximum delay obtained from examining all Z equations that are functions of y_j.

The maximum delay encountered by the y_j signal in traversing the Y AND combinational circuitry could be obtained by examining the maximum delays of all the Y equations which are functions of the signal y_j. This delay could be found by the operation

$$\delta_{AY(y_j)} = \underset{Y(y_j)}{MAX} \left(\delta_{AY(y_j)}\right) \tag{5-9}$$

where: $Y(y_j)$ represents all the Y equations that are functions of y_j.

The maximum total circuit delay experienced by the signals which were produced by changing external input X_i could then be approximated by determining the maximum of the following two sums for all the y_j's which are dependent on X_i.

$$\Delta_y y_j(x_i) + \Delta_f y_j(x_i) + \Delta_z y_j(x_i) \tag{5-10}$$

$$\Delta_y y_j(x_i) + \Delta_f y_j(x_i) + \delta_{Ay} y_j(x_i) \tag{5-11}$$

This maximization operation can be represented by

$$\Delta_T(x_i) = MAX\left[\Delta_y y_j(x_i) + \Delta_f y_j(x_i) + \Delta_z y_j(x_i);\ \Delta_y y_j(x_i) + \Delta_f y_j(x_i) + \delta_{Ay} y_j(x_i)\right] \tag{5-12}$$

where: $\Delta_T(x_i)$ = The maximum total disturbance time of the circuit for changes in external input X_i.

The maximum total disturbance time of the circuit which could ever occur can be obtained by examining the $\Delta_T(x_i)$ delay values for all possible external input changes. This examination can be denoted by

$$\Delta_T = \underset{x_i}{MAX}\left(\Delta_T(x_i)\right) \tag{5-13}$$

The maximum frequency at which the circuit could be safely operated can be obtained by

$$\omega_{MAX} = \frac{1}{\Delta_T} \tag{5-14}$$

Each of the delay values which are considered in determining Δ_T can be

obtained from the delay properties of the Boolean equations which represent the combinational circuit.

External Output Specified at the Beginning of a Transition

Signal paths for the asynchronous circuit with external output changes specified at the beginning of a circuit transition are shown in Figure 28. For this case, it can be seen that an external output change is produced explicitly by the external input X_i. This feature can increase the output response of the circuit over that of the case considered in the previous section. Also, notice that the feedback signal y_j does not have to traverse the OR portion of the combinational circuit to end the circuit transition. This feature can decrease the total settling time of the circuit and, thus, increase the maximum allowable operating frequency of the circuit.

The maximum allowable external input frequency to the circuit will be determined in the same manner as that described in the previous section. The signal paths shown in Figure 28 will be employed to determine the settling time of the circuit. The different maximum individual delays which exist in the combinational circuit will be determined first. The maximum delay experienced by input signal X_i in producing any of the Z external output signals can be determined by considering all possible delays for the Z signals which are functions of X_i. This procedure for finding the maximum Z signal delay can be expressed by:

$$\Delta_{Z(X_i)} = \underset{Z(X_i)}{MAX} \left(\Delta_{Z\,Z(X_i)} \right) \qquad (5\text{-}15)$$

The maximum time for the AND circuit to settle due to the disturbance from feedback signal y_j can be found by obtaining the maximum of the two

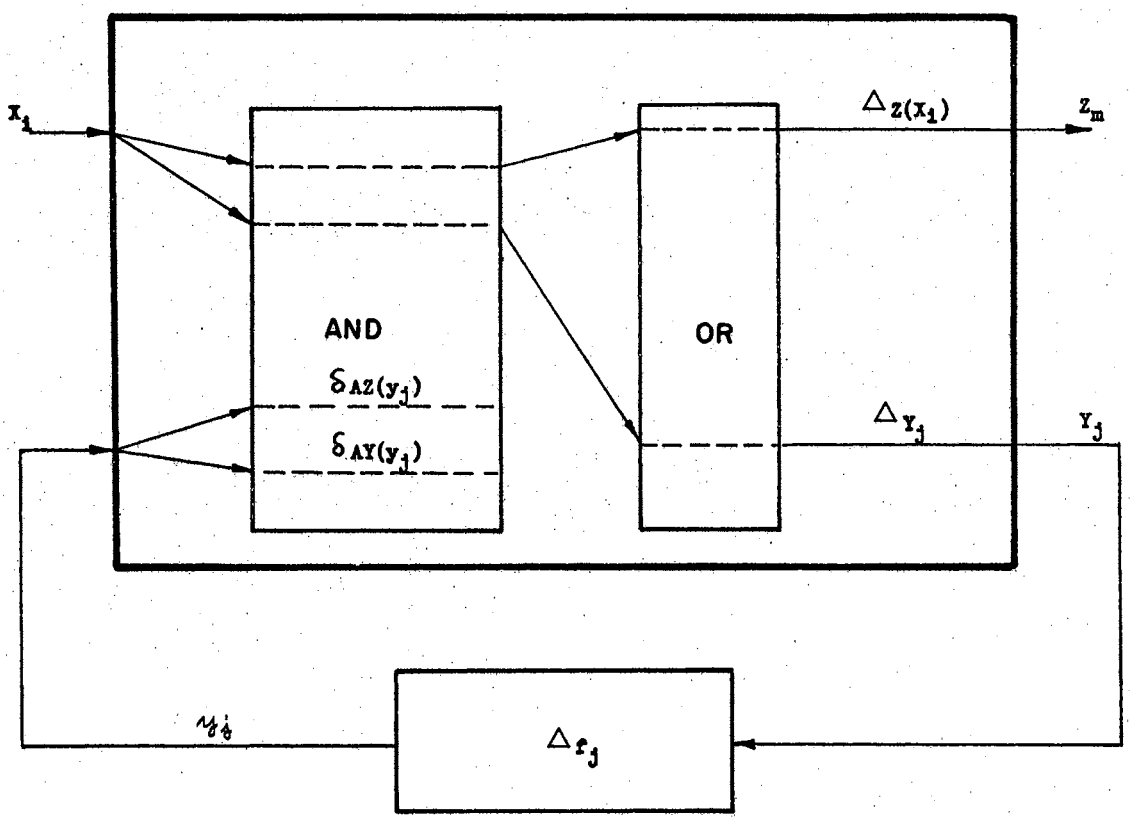

Figure 28. Signal Paths for an Asynchronous Circuit for External Output Changes Specified at the Beginning of a Transition

maximum delays experienced in the Z and Y AND circuitry by signal y_j. For the Z AND circuit, the maximum delay experienced by signal y_j would be

$$\delta_{AZ(y_j)} = \underset{Z(y_j)}{MAX}\left(\delta_{AZ\,Z(y_j)}\right) \tag{5-16}$$

Similarly, the maximum delay experienced by signal y_j in the Y AND circuit would be

$$\delta_{AY(y_j)} = \underset{Y(y_j)}{MAX}\left(\delta_{AY\,Y(y_j)}\right) \tag{5-17}$$

The maximum of the two values expressed in Equations (5-16) and (5-17) gives the maximum settling time for the AND circuit for disturbance created by signal y_j. This maximum settling time can be expressed by

$$\delta_{A(y_j)} = MAX\left(\delta_{AZ(y_j)}\ ;\ \delta_{AY(y_j)}\right) \tag{5-18}$$

The maximum time required for the total asynchronous circuit to settle due to the creation of a state variable signal y_j by a change in external signal X_i can be found by performing the maximizing operation indicated in Equation (5-19).

$$\Delta_{TY(x_i)} = MAX\left(\Delta_{Y\,y_j(x_i)} + \Delta_{f\,y_j(x_i)} + \delta_{A\,y_j(x_i)}\right) \tag{5-19}$$

The maximum delay value between the two delays $\Delta_{Z(x_i)}$ and $\Delta_{TY(x_i)}$ for all external inputs, X_i, gives the maximum total disturbance time which would ever be produced in the asynchronous circuit due to a change in external input. This maximum time can be expressed by

$$\Delta_T = \underset{x_i}{MAX}\left(\Delta_{Z(x_i)}\ ;\ \Delta_{TY(x_i)}\right) \tag{5-20}$$

The maximum frequency at which the circuit could be operated safely can

be obtained by

$$\omega_{MAX} = \frac{1}{\Delta_T} \tag{5-21}$$

Again, all the delay values which make up the delay Δ_T can be obtained from the delay properties of the Boolean equations which represent the circuit.

The general requirements have been established in the previous three sections for timing the feedback delay element and determining the maximum safe operating frequency for an asynchronous circuit. The reasoning which went into the determination of these timing requirements can now be employed to establish the timing conditions for an asynchronous circuit implemented with set-reset flip-flops as the state variable delay elements.

Timing Requirements for the Asynchronous Circuit Implemented With Set-Reset Flip-Flop Delay Elements

In Chapter II, the decision was made to employ set-reset flip-flops for feedback delay elements in the implementation of fluidic asynchronous circuits. It is necessary, therefore, to determine the timing requirements for the asynchronous circuit model implemented with S-R flip-flops in the feedback delay lines. The representative Boolean equations for the asynchronous circuit implemented with S-R flip-flops were given in Chapter II as

$$z_1 = z_1(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_j, \cdots, y_k)$$
$$\vdots$$

$$
\begin{aligned}
\dot{z}_m &= z_m(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_j, \cdots, y_k) \\
s_1 &= s_1(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_2, \cdots, y_j, \cdots, y_k) \\
R_1 &= R_1(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_2, \cdots, y_j, \cdots, y_k) \\
&\vdots \\
s_j &= s_j(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_{j-1}, y_{j+1}, \cdots, y_k) \\
R_j &= R_j(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_{j-1}, y_{j+1}, \cdots, y_k) \\
&\vdots \\
s_k &= s_k(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_j, \cdots, y_{k-1}) \\
R_k &= R_k(x_1, x_2, \cdots, x_i, \cdots, x_n ; y_1, y_2, \cdots, y_j, \cdots, y_{k-1})
\end{aligned}
\qquad (5\text{-}22)
$$

where:

$$y_j = s_j + \bar{R}_j y_j$$

and

$$R_j s_j = 0$$

The delay properties of these equations will be employed to determine the necessary timing of the flip-flop elements and to obtain the safe operating frequency of the over-all circuit for the two possible external output specifications.

Timing Requirements for the Flip-Flop Elements

The signal paths involved in the creation of signals for the S-R

flip-flops by changing external signal X_i are illustrated in Figure 29. The minimum delay ever required for an external signal X_i to produce set signal S_j would never be less than the minimum delay, Δ'_{Sj}, through the AND and OR stages of the combinational circuit. If the Boolean equation representing S_j has more than one product term, the minimum delay could be approximated by

$$\Delta'_{Sj} = \delta'_{ASj} + 1 \tag{5-23}$$

For only one product term in the S_j Boolean equation, the delay would be

$$\Delta'_{Sj} = \delta'_{ASj} \tag{5-24}$$

The maximum settling time required for the Z AND circuit could be determined by considering all the maximum AND delays for the Z equations that were functions of the external inputs X_i on which S_j was dependent. This maximum settling time will be represented by δ_{AZS}. Thus,

$$\delta_{AZS} = \underset{Z(X_i)}{MAX}\left(\delta_{AZS}(Z(X_i))\right) \tag{5-25}$$

where: X_i includes all the X_i's for which S_j is dependent.

Similarly, the maximum delay which would ever be encountered by the signals X_i in traversing all S AND circuits could be found by

$$\delta_{ASS} = \underset{S(X_i)}{MAX}\left(\delta_{ASS}(S(X_i))\right) \tag{5-26}$$

where: X_i includes all X_i's for which S_j is dependent.

Also, the maximum settling time required for stabilization of the R AND circuitry due to a change in input X_i could be obtained by

$$\delta_{ARS} = \underset{R(X_i)}{MAX}\left(\delta_{ARS}(R(X_i))\right) \tag{5-27}$$

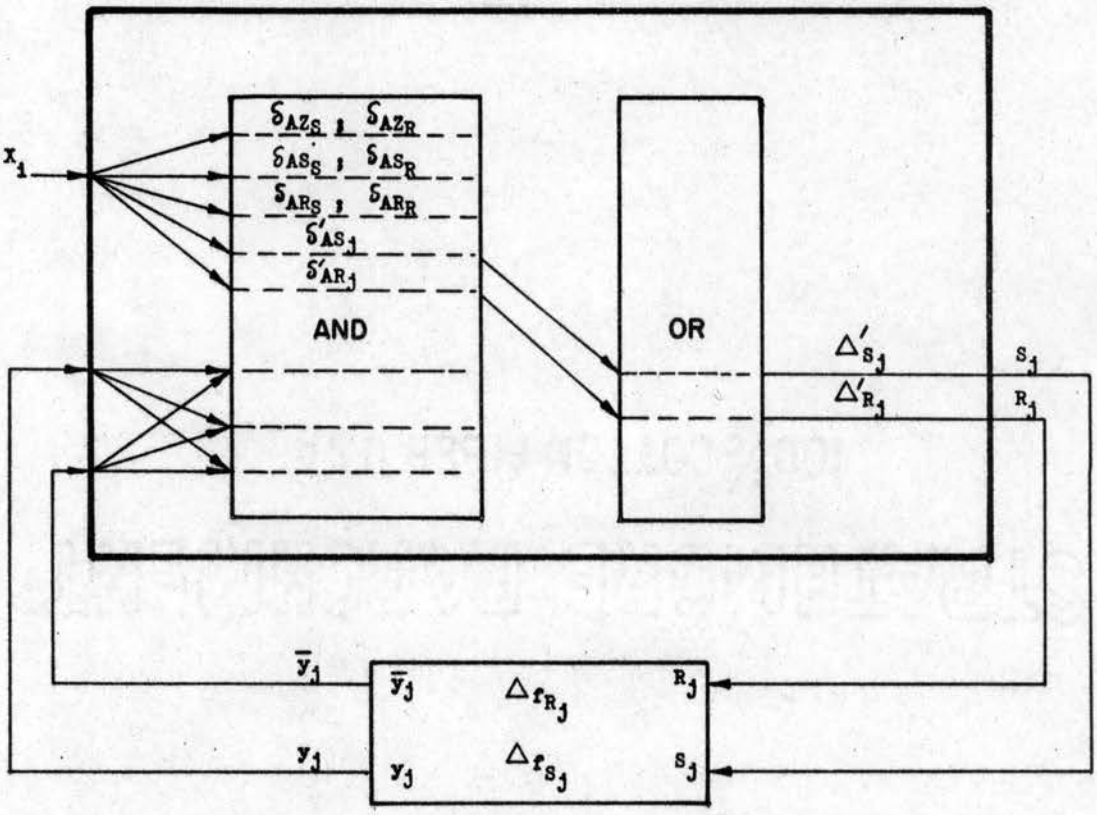

Figure 29. Signal Paths for an Asynchronous Circuit Implemented With S-R Flip-Flops

The maximum delay created in the AND portion of the combinational circuit by changing X_i input signals for which S_j is dependent, can be found by selecting the maximum of the three delays defined in Equations (5-25), (5-26), and (5-27). This maximum delay can be denoted by

$$\delta_{A_S} = MAX(\delta_{AZ_S}\ ;\ \delta_{AS_S}\ ;\ \delta_{AR_S}) \tag{5-28}$$

The timing requirement for the jth feedback flip-flop in response to the set signal S_j would be determined by

$$\Delta_{fS_j} = \delta_{A_S} - \Delta'_{S_j} \tag{5-29}$$

The respective equations for determining the timing requirement for the reset signal of the jth flip-flop can be derived as shown below.

$$\Delta'_{R_j} = \delta'_{AR_j} + 1 \tag{5-30}$$

or

$$\Delta'_{R_j} = \delta'_{AR_j} \tag{5-31}$$

Equation (5-30) is used if the Boolean equation for R_j has more than one product term; Equation (5-31) is used if R_j has only one product term.

$$\delta_{AZ_R} = \underset{Z(X_i)}{MAX}\left(\delta_{AZ_R(Z(X_i))}\right) \tag{5-32}$$

$$\delta_{AS_R} = \underset{S(X_i)}{MAX}\left(\delta_{AS_R(S(X_i))}\right) \tag{5-33}$$

$$\delta_{AR_R} = \underset{R(X_i)}{MAX}\left(\delta_{AR_R(R(X_i))}\right) \tag{5-34}$$

where: X_i includes all X_i's for which R_j is dependent.

The maximum AND delay created by input signals on which R_j is dependent can be found by

$$\delta_{A_R} = MAX(\delta_{AZ_R}\ ;\ \delta_{AS_R}\ ;\ \delta_{AR_R}) \tag{5-35}$$

The timing requirement for the jth feedback flip-flop in response to the reset signal R_j would be

$$\Delta_{fR_j} = \delta_{A_R} - \Delta'_{R_j} \tag{5-36}$$

Input Frequency Limitation With External Output Specified at the End of a Transition

Again the safe operating frequency will be based on the longest time ever required for the asynchronous circuit to settle after an external input is changed. The signal paths for the asynchronous circuit implemented with S-R flip-flops are illustrated in Figure 30. The maximum delay that signal y_j would ever experience in producing external output signals Z would be given by

$$\Delta_{Z(y_j)} = \underset{Z(y_j)}{MAX}\,(\Delta_{Z\,Z(y_j)}) \tag{5-37}$$

where: $Z(y_j)$ - denotes all Z outputs that are functions of y_j.

The maximum delays encountered by the y_j signal in traversing the S and R AND circuitry can be obtained by examining the maximum delays of all the S and R equations which are functions of y_j. These delays could be represented by

$$\delta_{AS(y_j)} = \underset{S(y_j)}{MAX}\,(\delta_{AS\,S(y_j)}) \tag{5-38}$$

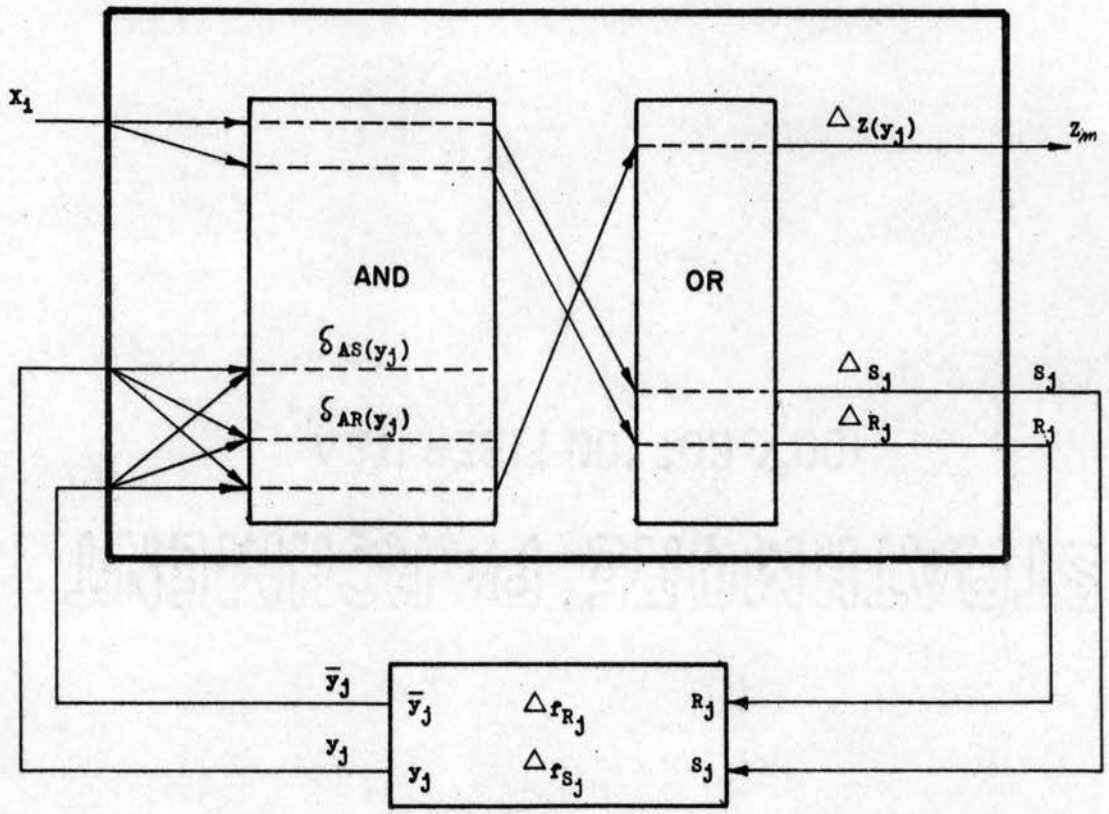

Figure 30. Signal Paths for an Asynchronous Circuit Implemented With S-R Flip-Flops for External Output Changes Specified at the End of Transitions

and

$$\delta_{AR(y_i)} = \underset{R(y_j)}{MAX} \left(\delta_{AR\,R(y_j)} \right) \tag{5-39}$$

where: $S(y_j)$ and $R(y_j)$ represent all the S and R equations that are functions of y_j.

The maximum of the two delay values given by Equations (5-38) and (5-39) can be denoted as

$$\delta_{AY(y_j)} = MAX\left(\delta_{AS(y_j)} \; ; \; \delta_{AR(y_j)}\right) \tag{5-40}$$

The maximum total circuit delay experienced by the signals produced when an external input X_i is changed can be determined by considering the total delay times involved when a set, S, or a reset, R, signal is produced by the input signal change. For the case where S is produced, the maximum total delay can be determined by

$$\Delta_{TS(x_i)} = \underset{y_j(x_i)}{MAX} \begin{bmatrix} \Delta_{S(y_j(x_i))} + \Delta_{fs(y_j(x_i)} + \Delta_{Z(y_j(x_i))} \\ \Delta_{S(y_j(x_i))} + \Delta_{fs(y_j(x_i)} + \delta_{AY(y_j(x_i))} \end{bmatrix} \tag{5-41}$$

where: $y_j(X_i)$ denotes all y_j's which are dependent on X_i.

Likewise, the maximum total circuit delay caused by an external input signal X_i producing a R can be found by

$$\Delta_{TR(x_i)} = \underset{y_j(x_i)}{MAX} \begin{bmatrix} \Delta_{R(y_j(x_i)} + \Delta_{fR(y_j(x_i))} + \Delta_{Z(y_j(x_i)} \\ \Delta_{R(y_j(x_i)} + \Delta_{fR(y_j(x_i))} + \delta_{AY(y_j(x_i))} \end{bmatrix} \tag{5-42}$$

The maximum total disturbance time of the circuit which could ever occur for any external input change can be obtained by determining the maximum of the delays $\Delta_{TS(x_i)}$ and $\Delta_{TR(x_i)}$ for all possible external

input changes. This maximum could be found by

$$\Delta_T = \underset{(X_i)}{MAX} \left(\Delta_{TS}(X_i) \; ; \; \Delta_{TR}(X_i) \right) \tag{5-43}$$

Then, the maximum frequency at which the circuit could be operated safely would be given by

$$\omega_{MAX} = \frac{1}{\Delta_T} \tag{5-44}$$

The delay values which constitute Δ_T in Equation (5-44) can be obtained from the delay properties of the Boolean equations given in Equation (5-22).

Input Frequency Limitation With External Outputs Specified at the Beginning of a Transition

The signal paths for the signals involved in a circuit transition with the external outputs specified at the beginning of a transition are shown in Figure 31. The maximum delay experienced by input signal X_i in producing any of the Z external output signals can be determined by

$$\Delta_Z(X_i) = MAX\left(\Delta_Z(Z(X_i))\right) \tag{5-45}$$

The maximum time for the AND circuit to stabilize after receiving feedback signal y_j can be found by obtaining the maximum of the three delays experienced in the S, R and Z AND circuitry by signal y_j. For the Z AND circuit, the maximum delay experienced by signal y_j would be

$$\delta_{AZ}(y_j) = MAX\left(\delta_{AZ}(Z(y_j))\right) \tag{5-46}$$

The maximum delay experienced by signal y_j in the S AND circuitry would

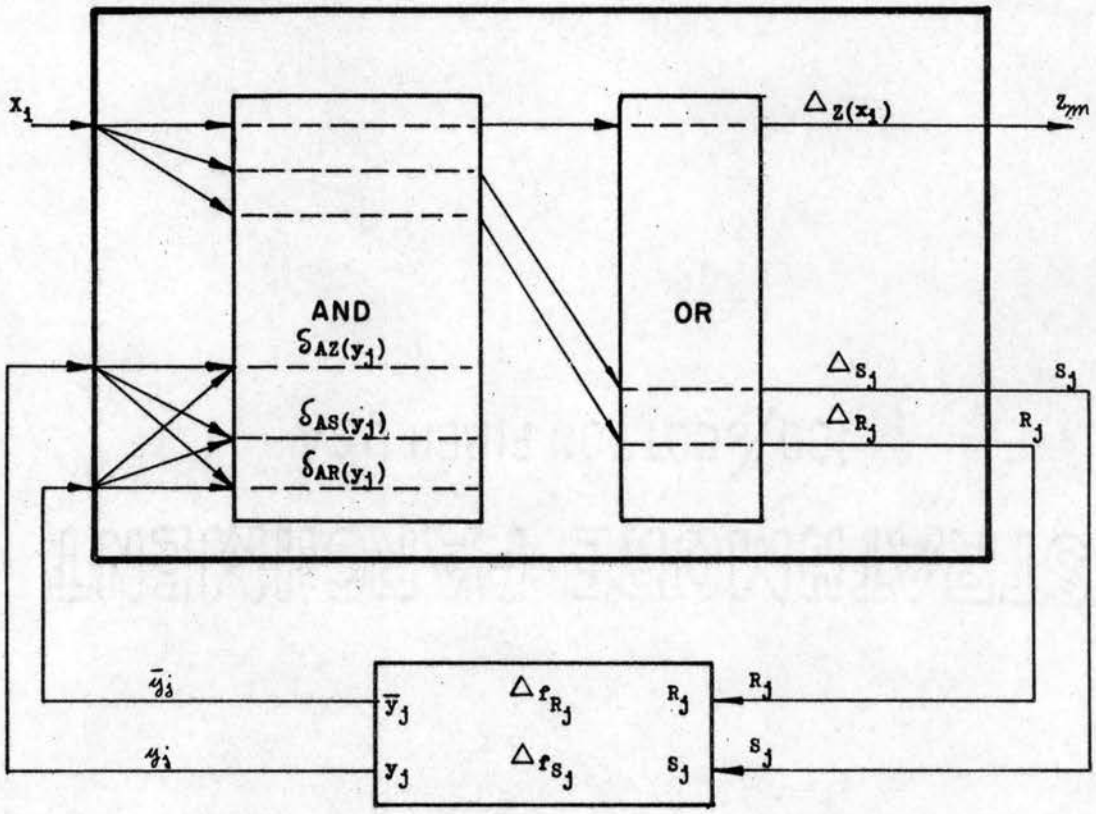

Figure 31. Signal Paths for an Asynchronous Circuit Implemented With S-R Flip-Flops for External Output Changes Specified at the Beginning of Transitions

be given by

$$\delta_{AS}(y_j) = \underset{S(y_j)}{MAX}\left(\delta_{AS}(S(y_j))\right) \tag{5-47}$$

Likewise, the maximum delay experienced by signal y_j in the R AND circuitry can be obtained by

$$\delta_{AR}(y_j) = \underset{R(y_j)}{MAX}\left(\delta_{AR}(R(y_j))\right) \tag{5-48}$$

The maximum of the values expressed in Equations (5-46), (5-47), and (5-48) gives the maximum settling time for the AND circuitry for disturbances created by signal y_j. This time can be expressed as

$$\delta_A(y_j) = MAX\left(\delta_{AZ}(y_j);\ \delta_{AS}(y_j);\ \delta_{AR}(y_j)\right) \tag{5-49}$$

The maximum time for the total asynchronous circuit to settle, due to the generation of a state variable signal y_j caused by a change in external signal X_i creating an S signal, can be found by

$$\Delta_{TS}(x_i) = \underset{y_j(x_i)}{MAX}\left(\Delta_S(y_j(x_i)) + \Delta_{fs}(y_j(x_i)) + \delta_A(y_j(x_i))\right) \tag{5-50}$$

Similarly, the total circuit settling time for a disturbance caused by the generation of signal y_j created by a change in external signal X_i creating an R signal, can be obtained by

$$\Delta_{TR}(x_i) = \underset{y_j(x_i)}{MAX}\left(\Delta_R(y_j(x_i)) + \Delta_{fR}(y_j(x_i)) + \delta_A(y_j(x_i))\right) \tag{5-51}$$

The maximum delay time which would ever be required for the circuit to settle for all external input changes, could be found considering the maximum value of $\Delta_Z(x_i)$, $\Delta_{TS}(x_i)$ and $\Delta_{TR}(x_i)$. This maximum can be expressed by

$$\Delta_T = \underset{x_i}{MAX} \left(\Delta_z(x_i) \; ; \; \Delta_{TS}(x_i) \; ; \; \Delta_{TR}(x_i) \right) \tag{5-52}$$

The maximum frequency at which the circuit could safely operate could then be obtained by

$$\omega_{MAX} = \frac{1}{\Delta_T} \tag{5-53}$$

As in the previous case, the delay values needed to evaluate Δ_T can be obtained from the Boolean equations in Equation (5-22). An example problem follows which demonstrates the procedure for obtaining Δ_T from the delay properties of the combinational circuit equations.

Example Problem

To illustrate the use of the procedures developed in the previous section, consider the problem of determining the timing requirements for the feedback signals and estimating the maximum safe operating frequency for the circuit represented by Boolean equations which have the following functional dependencies and delay properties.

Functional Dependency

$$\left.\begin{aligned} z_1 &= z_1(x_1, x_3, y_1) \\ z_2 &= z_2(x_2, x_3, y_2) \\ z_3 &= z_3(x_1, y_1, y_2) \\ S_1 &= S_1(x_1, x_2, y_2) \\ R_1 &= R_1(x_2, y_2) \\ S_2 &= S_2(x_3, y_1) \\ R_2 &= R_2(x_2, x_3) \end{aligned}\right\} \text{ which implies that } \begin{aligned} Y_1 &= Y_1(x_1, x_2, y_1, y_2) \\ Y_2 &= Y_2(x_2, x_3, y_1, y_2) \end{aligned}$$

Delay Properties

The conjunctive delays for the respective equations which represent the circuit are given as:

z_1	-	111	2222	33	4
z_2	-	11	22	333	
z_3	-		2222	333	44
S_1	-	111	2	3333	
R_1	-	1	222		
S_2	-			333	4
R_2	-	111	22	3	

It is specified that AND-OR minimum stage implementation will be employed for the combinational circuit and that S-R flip-flops will be employed in the feedback lines. The output is specified at the beginning of the transitions and the fan-in of the OR elements used in the combinational will be equal to two.

Solution

Immediately the minimum and maximum delays for each of the AND circuits can be determined from the given delay properties.

z_1	-	δ'_{Az_1}	=	1	;	δ_{Az_1}	= 4
z_2	-	δ'_{Az_2}	=	1	;	δ_{Az_2}	= 3
z_3	-	δ'_{Az_3}	=	2	;	δ_{Az_3}	= 4
S_1	-	δ'_{AS_1}	=	1	;	δ_{AS_1}	= 3
R_1	-	δ'_{AR_1}	=	1	;	δ_{AR_1}	= 2
S_2	-	δ'_{AS_2}	=	3	;	δ_{AS_2}	= 4
R_2	-	δ'_{AR_2}	=	1	;	δ_{AR_2}	= 3

Employing the stage minimization procedure given in Chapter IV, the

maximum combinational circuit delays for the equations can be determined. For an OR fan-in of 2:

Z_1 - DELAY NUMBER = 110110 $\therefore \Delta_{Z_1} = 6$

Z_2 - DELAY NUMBER = 100100 $\therefore \Delta_{Z_2} = 6$

Z_3 - DELAY NUMBER = 1001000 $\therefore \Delta_{Z_3} = 7$

S_1 - DELAY NUMBER = 101010 $\therefore \Delta_{S_1} = 6$

R_1 - DELAY NUMBER = 1110 $\therefore \Delta_{R_1} = 4$

S_2 - DELAY NUMBER = 101000 $\therefore \Delta_{S_2} = 6$

R_2 - DELAY NUMBER = 10110 $\therefore \Delta_{R_2} = 5$

The timing requirement for the set signal S_1 can be determined from Equations (5-23) through (5-29).

From Equation (5-23),

$$\Delta'_{S_1} = \delta'_{AS_1} + 1$$

or

$$\Delta'_{S_1} = 1 + 1 = 2$$

$$\underline{\Delta'_{S_1} = 2}$$

Equation (5-25) gives

$$\delta_{AZ_{S_1}} = \underset{Z(X_i)}{MAX}\left(\delta_{AZ_S\, Z(X_i)}\right)$$

The set signal S_1 is a function of external inputs X_1 and X_2. The Z output equations for Z_1, Z_2, and Z_3 are also functions of X_1 and X_2. The maximum δ_{AZ} delay from these three equations is 4.

$$\therefore \delta_{AZ_{S_1}} = 4$$

From Equation (5-26)

$$\delta_{AS_{S_1}} = \underset{S(X_i)}{MAX}\left(\delta_{AS_S}(S(X_i))\right)$$

S_2 is not a function of X_1 or X_2, thus S_2 would not be considered in the maximization. The maximum δ_{AS} delay for S_1 is 3.

$$\therefore \delta_{AS_{S_1}} = 3$$

From Equation (5-27)

$$\delta_{AR_{S_1}} = \underset{R(X_i)}{MAX}\left(\delta_{AR_S}(R(X_i))\right)$$

Both R_1 and R_2 are functions of X_2. The maximum δ_{AR} delay is $\delta_{AR_2} = 3$. Therefore,

$$\delta_{AR_{S_1}} = 3$$

The maximum delay δ_{AS} required for the AND circuitry to settle from external inputs producing signal S_1 can be found from Equation (5-28)

$$\delta_{A_{S_1}} = MAX(\delta_{AZ_{S_1}}\ ;\ \delta_{AS_{S_1}}\ ;\ \delta_{AR_{S_1}})$$

or

$$\delta_{A_{S_1}} = MAX(4\ ;\ 3\ ;\ 3) = 4$$

$$\therefore \delta_{A_{S_1}} = 4$$

The timing requirement for the S_1 input signal can be obtained from Equation (5-29) as

$$\Delta_{f_{S_1}} = \delta_{A_{S_1}} - \Delta'_{S_1}$$

or

$$\Delta_{f_{S_1}} = 4 - 2 = 2$$

$$\therefore \Delta_{f_{S_1}} = 2$$

Thus, the feedback delay for signal S_1 should be delayed by a factor of two times the operational delay times of the AND and OR elements which are used to implement the combinational circuit. Similarly, the timing requirements for the other three feedback signals R_1, S_2 and R_2 can be obtained as follows:

For R_1

$$\Delta'_{R_1} = 1 + 1 = 2$$

$$\delta_{AZ_{R_1}} = 3$$

$$\delta_{AS_{R_1}} = 3$$

$$\delta_{AR_{R_1}} = 3$$

$$\delta_{A_{R_1}} = 3$$

$$\therefore \Delta_{f_{R_1}} = 3 - 2 = 1$$

$$\underline{\Delta_{f_{R_1}} = 1}$$

For S_2

$$\Delta'_{S_2} = 3 + 1 = 4$$

$$\delta_{AZ_{S_2}} = 4$$

$$\delta_{AS_{S_2}} = 4$$

$$\delta_{AR_{S_2}} = 3$$

$$\therefore \delta_{A_{S_2}} = 4$$

which gives

$$\Delta f_{S_2} = 4 - 4 = 0$$

A zero or negative delay time can be interpreted as meaning that the timing of the feedback element is not critical. A delay time value of 1 will be assumed for these cases for use in determining the operating frequency.

For R_2

$$\Delta'_{R_2} = 1 + 1 = 2$$

$$\delta_{AZ_{R_2}} = 4$$

$$\delta_{AS_{R_2}} = 4$$

$$\delta_{AR_{R_2}} = 3$$

$$\therefore \delta_{AR_2} = 4$$

$$\Delta f_{R_2} = 4 - 2 = 2$$

Determination of Maximum Operating Frequency

From Equation (5-45)

$$\Delta_z(x_1) = 7 \; ; \quad \Delta_z(x_2) = 6 \; ; \quad \Delta_z(x_3) = 6$$

From Equation (5-46)

$$\delta_{AZ}(y_1) = 4 \; ; \quad \delta_{AZ}(y_2) = 4$$

From Equation (5-47)

$$\delta_{AS}(y_1) = 4 \; ; \quad \delta_{AS}(y_2) = 3$$

From Equation (5-48)

$$\delta_{AR}(y_1) = 0 \; ; (R_1 \text{ and } R_2 \text{ are not functions of } y_1) \; ; \quad \delta_{AR}(y_2) = 2$$

Therefore, from Equation (5-49)

$$\delta_A(y_1) = MAX(4, 4, 0) = 4$$

$$\delta_A(y_2) = MAX(4, 3, 2) = 4$$

Equation (5-50) gives

$$\Delta_{TS}(X_1) = MAX\begin{bmatrix} \Delta_S y_1(x_1) + \Delta_{fs} y_1(x_1) + \delta_A(y_1) \\ 0 \end{bmatrix}$$

The zero results from the fact that S_2 is not a function of X_1; therefore, S_2 cannot be produced by a change in X_1.

$$\Delta_{TS}(X_1) = MAX\begin{bmatrix} 6+2+4 \\ 0 \end{bmatrix} = MAX\begin{bmatrix} 12 \\ 0 \end{bmatrix} = 12$$

$$\Delta_{TS}(X_2) = MAX\begin{bmatrix} \Delta_S y_1(x_2) + \Delta_{fs} y_1(x_2) + \delta_A(y_1) \\ 0 \end{bmatrix} = 12$$

$$\Delta_{TS}(X_3) = MAX\begin{bmatrix} 0 \\ \Delta_S y_2(x_3) + \Delta_{fs} y_2(x_3) + \delta_A(y_2) \end{bmatrix}$$

$$\Delta_{TS}(X_3) = MAX\begin{bmatrix} 0 \\ 6+1+4 \end{bmatrix} = 11$$

Equation (5-51) yields

$$\Delta_{TR}(x_1) = MAX\begin{bmatrix} 0 \\ 0 \end{bmatrix} = 0$$

This results from the fact that R_1 and R_2 are not functions of X_1.

$$\Delta_{TR}(x_2) = MAX\begin{bmatrix} \Delta_{R y_1}(x_2) + \Delta_{f R y_1}(x_2) + \delta_A(y_1) \\ \Delta_{R y_2}(x_2) + \Delta_{f R y_2}(x_2) + \delta_A(y_2) \end{bmatrix}$$

$$\Delta_{TR}(x_2) = MAX\begin{bmatrix} 4+2+4 \\ 5+2+4 \end{bmatrix} = MAX\begin{bmatrix} 9 \\ 11 \end{bmatrix} = 11$$

$$\Delta_{TR}(x_3) = MAX\begin{bmatrix} 0 \\ \Delta_{R y_2}(x_2) + \Delta_{f R y_2}(x_2) + \delta_A(y_2) \end{bmatrix}$$

$$\Delta_{TR}(x_3) = MAX\begin{bmatrix} 0 \\ 11 \end{bmatrix} = 11$$

Then, the total maximum settling time of the circuit can be determined by obtaining the maximum delay value for all X_i as defined by Equation (5-52).

$$\Delta_T = MAX\begin{bmatrix} \Delta_z(x_1) \; ; & \Delta_{TS}(x_1) \; ; & \Delta_{TR}(x_1) \\ \Delta_z(x_2) \; ; & \Delta_{TS}(x_2) \; ; & \Delta_{TR}(x_2) \\ \Delta_z(x_3) \; ; & \Delta_{TS}(x_3) \; ; & \Delta_{TR}(x_3) \end{bmatrix}$$

$$\Delta_T = MAX\begin{bmatrix} 7 \; ; & 12 \; ; & 0 \\ 6 \; ; & 12 \; ; & 11 \\ 6 \; ; & 11 \; ; & 11 \end{bmatrix} = 12$$

The maximum frequency at which the external inputs could be changed with assured safe circuit operation can be defined by Equation (5-53) as

$$\omega_{MAX} = \frac{1}{\Delta_T} = \frac{1}{12}$$

This estimate of the operating frequency would necessarily be conservative in value. A faster safe operating frequency might be obtained for the actual circuit but the designer can be assured that the given circuit could always be designed to operate at least as fast as the above estimate. This makes the method useful for evaluating the worst possible response which could be expected from a circuit represented by a given set of Boolean equations.

Summary

This chapter has considered the requirements for timing the input signals to an asynchronous circuit so that correct circuit operation will occur. The two physical requirements which the designer must provide to insure proper asynchronous circuit operation were defined as:

1. Providing delay values in the internal feedback lines to allow time for the combinational circuit disturbances to settle before the internal state variable signal changes.
2. Restricting the external input frequency so that the previous transition disturbances in the total circuit have time to settle before other external inputs change.

A procedure for establishing necessary delay values for the internal feedback signals was formulated by considering the delay properties of the Boolean equations which represent the circuit. It was assumed that the combinational circuit portion of the asynchronous circuit would be implemented as a minimum stage AND-OR circuit. The fan-in capabilities of the elements used to implement the combinational circuit were

implicitly included in the procedure. Also, the restrictions of one state variable element change per stable state transition and adjacent external input changes were defined for the circuit operating conditions. The feedback delay values obtained from the procedure represent an upper bound on the amount of delay needed in the respective feedback lines to assure correct circuit action.

A method for estimating the maximum allowable frequency for changing external input signals while maintaining proper circuit action was then developed. This frequency prediction utilized the feedback signal delay estimate described above together with the delay properties of the Boolean equations which represent the combinational circuit. The method formulated for predicting the safe operating frequency was based on determining the longest settling time for the circuit after any of the external inputs to the circuit were changed. It was shown that this maximum settling time would be dependent on the time at which the external outputs of the circuit were specified to change during a circuit transition. The external outputs of the circuit were shown to be functions of the state variable signal which changed during a transition when the output changes were specified at the end of a circuit transition. When the output changes were specified at the beginning of a transition, the outputs were seen to be functions of the external inputs that initiated the circuit transition. It was concluded that this latter specification would usually result in faster output response and greater allowable operating frequencies since less combinational circuitry would have to be traversed to produce the external outputs. A definite comparison cannot be made; however, since the circuit equations representing the two specifications will not necessarily be the same.

The asynchronous circuit timing method developed in this chapter provides the designer with a way to establish approximate operating values for the feedback delay signals and to estimate the slowest maximum operating frequency which will ever be required to achieve safe circuit operation. These estimates allow comparisons to be made of the operating speeds which could be expected from equivalent circuits represented by different Boolean equations.

Also, the results of this chapter should provide understanding of the basic timing requirements for the asynchronous circuit. This understanding can be employed as a guide for experimentally fine tuning the asynchronous circuit after physical implementation. Perhaps most important, the work presented in this chapter should bring attention to the often ignored circuit timing requirements which must be considered to design safe operating asynchronous circuits.

CHAPTER VI

FLUIDIC COMPONENT TIMING CONSIDERATIONS

The previous chapters of this work have discussed and identified the requirements for designing fast, safe operating asynchronous sequential circuits implemented with bounded delay logic elements. It was noted that all but two of the critical problems encountered in the design of an asynchronous circuit could be resolved in the synthesis procedure employed to derive the logic equations which represent the circuit. The two problems which could not be eliminated in the equation synthesis procedure had to be solved by physically controlling the timing of certain signal changes during circuit operation. The physically controlled timing requirements needed to assure a safe operating circuit were defined by:

1. The restriction of the external input frequency to the circuit such that previous input transition disturbances in the circuit would have time to settle before another external input changed.
2. The delay of the change of the internal state variable feedback signals to allow previous combinational circuit disturbances to settle before the state variable signal changed.

Restricting the change of external input signals to the circuit is a design stipulation which can be handled external to the asynchronous

circuit. Thus, the first of the above requirements does not need to be included in the interior circuit design. Control of the state variable feedback signals creates an interior circuit design problem that must be solved by providing, within the circuit, a physical means of controlling the response times of the feedback delay elements.

The feedback delay element control problem for fluidic flip-flop elements constitutes the major subject for discussion in this chapter. The chapter begins with a brief definition of the timing requirements for the fluidic components that are to be used in implementing asynchronous circuits. This description is followed by the development of an analytical-empirical model which is employed to estimate a component of the total switching time of a S-R fluidic flip-flop element as a function of the magnitude and shape of the input control signal to the element. Subsequent total switching time experimental tests are presented which indicate that the internal timing requirements for maintaining correct operation of an asynchronous fluidic circuit can be obtained by properly sizing the feedback delay elements and/or controlling the input control signal to the feedback elements.

Combinational Circuit Elements

The non-memory logic elements used to implement a fluidic combinational circuit can be either active or passive AND and OR logic elements.* Numerous different configurations of fluidic elements are

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*It should be realized that any combinational elements (i.e., NOR, NAND, COINCIDENCE, etc.) which could be used to obtain the required logic function, can be employed to implement the combinational circuit.

available from commercial suppliers for generating the AND and OR logic functions.

For the purpose of implementing combinational circuits to be used in asynchronous circuits, it is important that the combinational AND-OR logic components be as fast-acting as possible and possess large fan-in and fan-out capabilities to avoid multistaging within each logic level (see Chapter IV) when implementing complex logic equations. Most significant, however, is the fact that the operational speed of the combinational elements does not need to be precisely controlled to produce a safe operating combinational circuit.* The only timing requirement imposed on the combinational circuit elements which are employed in an asynchronous circuit is that the elements operate within the times imposed by the bounded stray delays of the elements; i.e., the delay time, $\Delta(t)$, of the element must be defined by $0 \leq \Delta(t) \leq \Delta_{MAX}$. Thus, the timing of the combinational circuit element response is not critical with respect to correctness of asynchronous circuit operation if the delay time of the element remains within the upper bound of the stray delay limit.

Feedback Delay Element

As noted in Chapter II, the bistable jet attachment device shown schematically in Figure 32 can be employed as the state variable feedback delay element in an asynchronous circuit. The general physical configuration of this bistable jet element is given in Figure 33. This

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*It is assumed that hazards created by the stray delays in the combinational circuit have been eliminated from the circuit (see Appendix C).

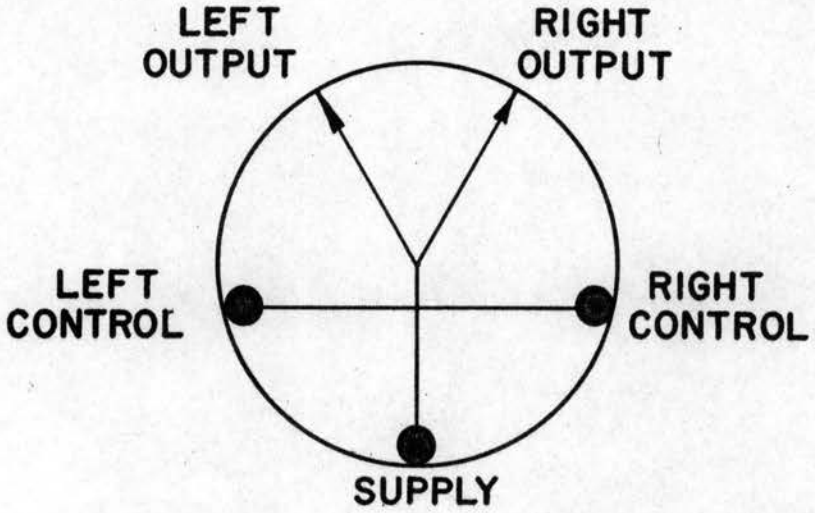

Figure 32. SAE Logic Symbol of the Bistable Jet Wall Attachment Device

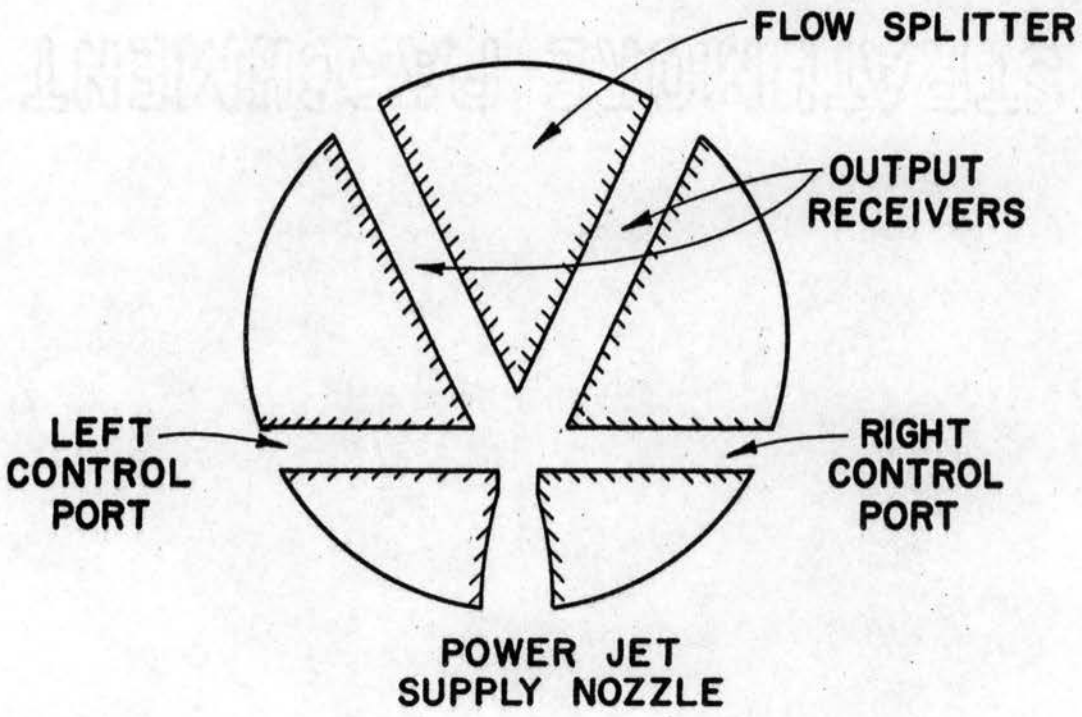

Figure 33. Geometric Configuration of the Bistable Jet Wall Attachment Device

type of fluidic device utilizes a submerged power jet issuing through a supply nozzle to deliver necessary energy at the output receivers to create physical signals for driving other logic circuit components. The power jet has two stable operating positions which are determined by the attachment of the power jet to one of the two offset-inclined walls of the device. This bistability of the power jet is obtained due to the Coanda effect created by the jet flowing past the offset-inclined walls confining the jet. The output state of the bistable element can be changed by introducing sufficient flow in the control port at the wall side on which the jet is attached to cause the jet to switch to the opposite wall. The jet remains in the position to which it was last switched when all control signals are removed. Therefore, this type of bistable element can be employed to perform the function of a S-R flip-flop feedback delay element in an asynchronous sequential fluidic circuit. As noted previously, the response or switching time of the feedback delay element in an asynchronous circuit must be controlled to assure safe circuit operation if essential hazards are present in the circuit. The requirements and methods for timing the S-R fluidic feedback delay elements are defined in the succeeding sections of this chapter.

Definition of the S-R Feedback Delay Element Timing Problem

The feedback delay elements in an asynchronous circuit with essential hazards present must be operated at a stray delay value defined by $\triangle_{MIN} \leq \triangle(t) \leq \triangle_{MAX}$. The minimum delay $\triangle_{MIN}$ is fixed by the amount of delay needed to assure safe operation of the circuit (see Chapter V).

The upper delay Δ_{MAX} is determined by the statistical variance in the switching time data for the feedback element and should be maintained as close to Δ_{MIN} as practical to avoid unnecessary retardation of the allowable circuit operating frequency. For an asynchronous fluidic circuit design, it would seem convenient to define the following specifications concerning the operation and design of the feedback delay elements. These specifications are:

1. That the configuration of all feedback delay elements be fixed to standardize the circuit fabrication procedure.
2. That the maximum operational speed of the feedback elements be as fast as the combinational circuit element operational speed to provide maximum circuit operating speed when essential hazards are not present.
3. That the feedback elements be operated at a fixed power jet flow rate to facilitate fulfilling the fan-out requirements imposed on the feedback elements.

Satisfying these specifications require that the switching time of the feedback element be controlled by varying the physical size of the element or by adjusting the control flow signal to the element.

Previous investigators (13, 21, 24) have indicated that the switching time of a bistable jet attachment device would be a function of the magnitude of the control signal to the element. These previous studies were conducted by varying the magnitude of a step input control signal to jet attachment devices and measuring the resulting response times. The results of these studies offered optimistic information with regard

to controlling the response of bistable fluidic devices with control signal adjustment, but did not evaluate the effects of applying imperfect control signals to the bistable elements. Since the feedback delay elements in an actual fluidic circuit would always operate with imperfect inputs, a study was conducted to determine and evaluate the effects of imperfect control inputs on the response of a bistable element. One of the prime objectives of the study was to obtain an estimation of the range of switching time control which could be achieved for a bistable element by varying the shape and magnitude of the input control flow signal to the element. The plan of attack for the study was to develop a combined analytical-empirical model to mathematically predict the jet detachment time component of the total switching time of an attached jet for control signals characterized by a given shape and magnitude. The results obtained from the mathematical model were then supplemented with experimentally determined total switching time information to obtain an indication of the degree of switching time control which could be expected by varying the form of input signal to a bistable fluidic flip-flop device. The details of this study are presented in the remainder of this chapter.

Development of the Attaching Jet Response Time Model

The bistable jet wall attachment fluid amplifier operates on the basic principle of a submerged jet issuing from a power nozzle and attaching to an adjacent offset-inclined wall. A schematic of the basic geometry of this bistable device is shown in Figure 34. After the power jet becomes attached to the adjacent wall, a flow circulation region is established in the low-pressure separation bubble formed

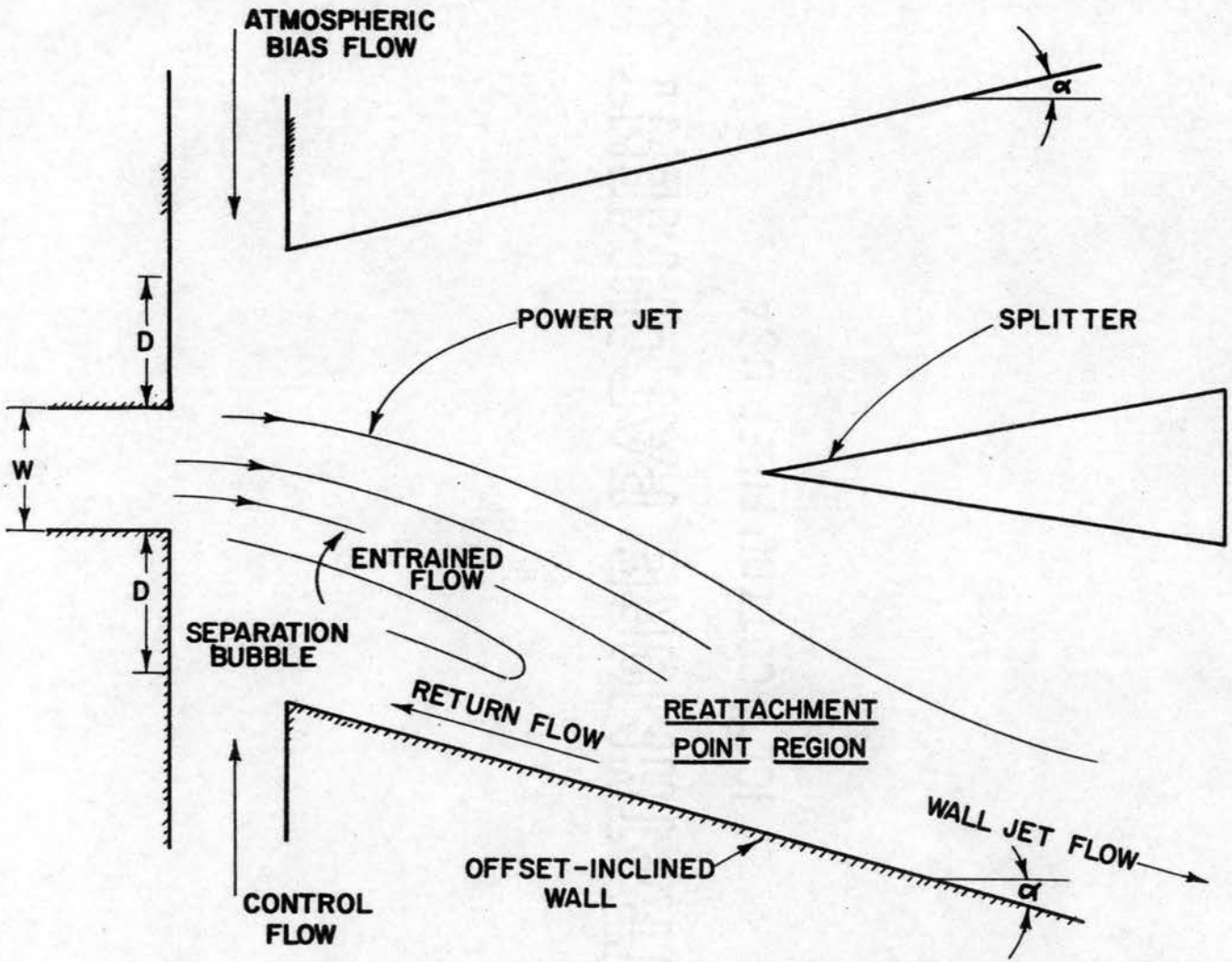

Figure 34. Basic Physical and Geometric Characteristics of the Bistable Jet Device

between the edge of the submerged jet and the confining wall. Under steady-state conditions, with no control flow into the separation bubble, the flow returned to the separation bubble at the reattachment location of the jet equals the flow entrained along the inner side of the power jet. The formulation of a dynamic model to predict the attached jet movement along the wall and its subsequent switching to the opposite wall when control flow is introduced into the separation bubble region requires that the mechanism involved in switching the jet be examined. Previous visual studies (13, 21) of the bistable jet switching mechanism have led to the conclusion that the total switching time of the device can be separated into two time components defined as:

1. Jet Detachment Time - The time required for the reattachment location of the power jet to shift from its initial attached position on the wall to the wall location where switching is triggered and the jet detaches from the wall.
2. Jet Traverse Time - The time required for the detached power jet to travel across and attach to the opposite wall of the device.

Dynamic models which have been developed previously to study attached jet response to step input control signals are reviewed in the next section. A modification of these techniques will be employed to predict the effect of non-step control inputs on attached jet response.

To the author's knowledge, a means of modeling the jet traverse time for the geometrical configuration shown in Figure 34 has not yet been devised. In a comprehensive study by Gurski (8), the dynamic modeling of a submerged power jet issuing past a single offset knife-edge was considered. This study was limited to considering the

dynamics of the power jet and a single control bubble region. At low operating frequencies, the results of Gurski's work indicated that the dynamics associated with predicting the traverse characteristics of a submerged jet primarily depended on the vortex lag associated with the control port region of the pure fluid device. As the operating frequency was increased beyond the break frequency of the vortex lag, both the dynamics of the submerged jet and the vortex lag had to be included in the dynamic jet model. Gurski's study is related to the problem of predicting the traverse time of a switching jet; however, the effects of geometric boundaries for a bistable jet device and the power jet receiver loading were not considered. The present study will be limited to obtaining empirical data relating the traverse time of the jet for a particular geometric configuration and loading condition to control signal magnitude and shape. This data can be employed to qualitatively indicate the factors which influence the traverse time of a switching bistable jet.

Previous Related Dynamic Jet Modeling Studies

One of the first dynamic studies of turbulent jet reattachment amplifiers was conducted by Johnson (13) in 1962. A dynamic model for predicting the detachment time of an attached jet from a wall was formulated to relate the separation bubble volume, the elapsed time from the beginning of the control flow, the control flow rate and the control flow entrained by the main power jet during the separation process. This relationship was expressed in differential equation form as:

$$q_c(t) = q_e(t) + \frac{d\,v_b(t)}{dt} \qquad (6\text{-}1)$$

where: $q_c(t)$ - Instantaneous control flow into the separation bubble region

$q_e(t)$ - Instantaneous control flow entrained by the power jet and carried downstream of the jet reattachment point. This flow represents one component of the total flow entrained by the power jet. The flow returned to the separation bubble region comprises the other component of the total entrained flow.

$\mathcal{V}_b(t)$ - Instantaneous separation bubble volume.

Equation (6-1) states that the control flow injected into the separation bubble region of an attached jet either goes to increase the volume of the bubble region, thus moving the power jet reattachment location downstream or is entrained by the power jet and carried out of the separation bubble region. Johnson did not identify the time dependent quantities in Equation (6-1) quantitatively, but he did make enough assumptions and restrictions concerning the wall jet detachment phenomenon to allow an experimental evaluation of the equation. For a constant power jet Reynolds number and fixed single wall geometry, the change in separation bubble volume from the time control flow begins to the time of jet detachment from the offset-inclined wall was assumed to be a constant, ΔV_b, for all control flow magnitudes. Also, an average control flow entrainment rate over the entire time needed for jet detachment was defined by:

$$Q_{eav} = \frac{1}{t_s}\int_0^{t_s} Q_e(t)\, dt \qquad (6\text{-}2)$$

where: Q_{eav} - average control flow entrained by the power jet

over the jet detachment time, t_s.

In addition, the instantaneous control flow was assumed to be a step function. The above assumptions reduce Equation (6-1) to:

$$\Delta V_b = t_s (Q_c - Q_{eav}) \quad \text{for } t > 0 \tag{6-3}$$

The constant terms ΔV_b and Q_{eav} were determined empirically by conducting transient detachment time measurements for two different known control flow rates and measuring the jet detachment times. Equation (6-3) could then be employed to predict the detachment time of the jet for other control flow magnitudes. Experimental results using single wall jet attachment models were presented which showed good agreement with the results predicted by Equation (6-3). It was concluded that this agreement suggested that the hypothesized mechanism of detachment for an attached wall jet as given by Equation (6-1) followed the actual jet detachment mechanism in its main aspects. Other measurements by Johnson on double-walled models indicated that the traverse time of a constant Reynolds number power jet from one wall to the other wall remained essentially constant for all input control flow magnitudes. Johnson suggested that further work be conducted on double-walled models to determine if the total switching time of the jet could be predicted by simply adding the jet detachment time to a constant jet traverse time.

Johnson's work contributed considerable insight into the switching mechanism of an attached wall jet and identified a form of differential equation which could be employed to dynamically model the detachment time of the jet from the wall. The work suffered, however, from the restrictions and assumptions which were made to solve the differential

equation for the dynamic model. In particular, the results obtained from the study were limited to fixed geometries and power jets operating at a constant Reynolds number.

Olson (24) in 1964, published work completed on a study of the factors affecting the time response of bistable fluid amplifiers. This study was mainly concerned with predicting the time required for a step input flow control signal to shift a jet attached to a wall from one position on the wall to a given downstream wall position. The flow mechanism employed in the analysis was the same as that used by Johnson, thus, Equation (6-1) was again assumed to characterize the dynamics of the jet detachment mechanism. By assuming quasi-steady flow into the separation bubble, Olson defined the entrained control flow rate and the separation bubble volume as functions of the jet reattachment location. Equation (6-1) could then be rewritten as:

$$q_c(t) = q_e\left(\frac{X_R}{W}\right) + \frac{dF\left(\frac{X_R}{W}\right)}{d\left(\frac{X_R}{W}\right)} \frac{d\left(\frac{X_R}{W}\right)}{dt} \tag{6-4}$$

where: $\frac{X_R}{W}$ - power jet reattachment location nondimensionalized with respect to the power jet nozzle width.

q_e - entrained control flow defined as a function of $\frac{X_R}{W}$.

F - separation bubble volume function expressed as a function of $\frac{X_R}{W}$.

This equation was then rearranged and integrated as shown in Equation (6-5) to calculate the time required to shift the jet reattachment location from an initial position, $\frac{X_{R_o}}{W}$, to a final downstream location, $\frac{X_R}{W}$, for step input control flows.

$$t = \int_{\frac{X_{R_o}}{W}}^{\frac{X_R}{W}} \frac{F'}{q_c - q_e} d\left(\frac{X_R}{W}\right) \tag{6-5}$$

where:

$$F' = \frac{d\left(F\left(\frac{X_R}{W}\right)\right)}{d\left(\frac{X_R}{W}\right)}$$

To evaluate the control flow entrainment function, q_e, Olson observed that for quasi-steady flow into the separation bubble region, the flow entrained from the separation bubble at any instant of time would equal the value of control flow which would produce a steady-state power jet reattachment location that corresponded to the instantaneous reattachment location in the transient case. This quasi-steady flow assumption allowed the control flow entrainment function, q_e, to be determined by experimentally measuring the steady-state power jet reattachment location for values of steady-state control flow which ranged from zero to the value of control flow which caused the jet to detach from the wall. The derivative of the separation bubble volume function, F, with respect to the reattachment location, was obtained from the geometry of the offset inclined wall configuration.

The experimental results of Olson's study displayed excellent correlation with the response times predicted by Equation (6-5) for offset-inclined wall geometries typical to those employed in bistable wall-attachment devices. An important trend was also established which indicated that the response time associated with moving the attached jet from an initial reattachment location to a downstream location by introducing a step input control signal into the separation bubble was a function of the magnitude of input control flow rate relative to the minimum magnitude of control flow rate (i.e., the steady state value) required to shift the jet to the downstream location. This trend was

observed to hold until the response time of the jet approached the jet transport time.

Olson nondimensionalized the response time of the jet with a transport time calculated as the time required for a fluid particle moving at the average velocity of the power jet to travel the distance from the power jet nozzle exit to the reattachment location to which the jet was shifting. This nondimensionalization effectively removes the power jet Reynolds number as a parameter to consider in the results as long as the power jet flow remains in the subsonic, turbulent region where the jet reattachment location is independent of the Reynolds number.

The results of Olson's work indicated that the total detachment time of the attached jet could be accurately predicted by Equations (6-5) for various geometries and different step input control flow rate magnitudes if the location on the wall at which the jet would detach could be predicted. This approach assumes that the steady-state and transient detachment locations are the same. Subsequent work published by Olson (22) provided an empirical correlation for predicting the location of jet detachment for normalized double boundary wall configurations.

Concurrent with Olson's initial paper on attached jet response, Müller (21) described a dynamic switching model used for predicting the jet detachment time for double walled jet attachment elements. Again, the basic form of differential equation given by Equation (6-1) was employed to formulate the analytical model. The entrained control flow function was assumed to be an empirically determined quadratic function of the separation bubble volume. The model was employed to graphically calculate the time required for the jet to detach from the wall for step

input control flow signals. Müller described the results predicted by the model as promising and concluded from the study that the dynamic switching characteristics of a bistable wall attachment jet were similar to statically determined switching characteristics.

Wilson (31) employed a jet detachment model similar to that of Olson's to obtain an estimate of the effects of varying the magnitude of a step input to an attached jet element. A linearized estimate of the entrained control flow rate function was obtained from a steady-state reattaching jet model similar to that developed by Brown (2) and later modified by Sher (29). By assuming that the jet would detach when the reattachment location of the power jet reached the end of the attachment wall, Wilson was able to evaluate the total jet detachment time with an equation similar to Equation (6-5). The results of Wilson's calculation resulted in the same general conclusion reached in previous studies, i.e., that the detachment time of the jet would decrease as the magnitude of the step input control flow signal to a jet attachment element was increased. No experimental results were provided by Wilson to evaluate his particular jet detachment model, but it was implied that control flow magnitude adjustment was employed to control the response times of wall attachment elements used to implement portions of a pulse data control system.

The results of the previous studies reviewed in the preceding paragraphs indicated that a practical engineering model for predicting the response of an attached jet for non-step control inputs could be developed using Equation (6-1) to characterize the switching mechanism and by employing quasi-steady flow techniques to identify the entrained control flow function. The jet detachment model described in the next

section is developed on this basis.

It should be noted that modeling procedures such as those presented in this section will never describe the detailed fluid mechanics which occur within the confines of the bistable fluid amplifier. However, usable trends can be established for guiding individual element design and for aiding in the incorporation of the elements into integrated systems.

To accurately describe the dynamics of the fluid amplifier elements, from a fluid mechanics standpoint, would require that the basic time dependent equations of fluid motion be solved. Due to the geometric boundaries and complex flows encountered in the bistable fluidic devices, solution of the describing fluid flow equations represents a formidable task. Invariably, numerical techniques which involve dividing the flow field into a large number of discrete mesh points must be employed to approximate an accurate solution. Current work is being conducted in this very promising area of fluid dynamics at Los Alamos, Sperry Utah Company, University of Michigan, and Oklahoma State University.

Jet Detachment Model for Non-Step Control Inputs

The importance of possessing the ability to control the switching time of the bistable fluidic flip-flop element over a range of switching time values has been stressed in previous chapters since this would enable the fluidic circuit designer to properly time the feedback delay elements of an asynchronous fluidic circuit. Therefore, the purpose of the following mathematical model development will be to evaluate the effects which varying shape and magnitude control signals could have on the switching time of a bistable jet element.

The basic two-wall flow model employed in the study was shown schematically in Figure 34. The switching time of the bistable jet was divided into the time required for the jet to detach from the wall and the time required for the detached jet to travel to the opposite wall, i.e., detachment time and traverse time, respectively. In this study, the detachment times are determined from a combined analytical-empirical model and then used with experimentally measured total switching times to evaluate the traverse time.

The mathematical model for predicting jet detachment time for non-step control flow inputs can be formulated by employing the differential equation given by Equation (6-1):

$$q_c(t) = q_e(t) + \frac{dv_b(t)}{dt} \tag{6-1}$$

As explained previously, this equation equates the instantaneous control flow into the separation bubble of the attached power jet to the flow entrained by the power jet and the flow which goes to increase the size of the separation bubble.

Preliminary experimental observations showed the separation bubble volume to be a function of both the reattachment location of the power jet and the control flow. Thus, the total derivative of the separation bubble volume with respect to time can be written as:

$$\frac{dv_b}{dt} = \frac{dv_b}{dq_c}\frac{dq_c}{dt} + \frac{dv_b}{dX_R}\frac{dX_R}{dt} \tag{6-6}$$

By assuming quasi-steady flow into the separation bubble region, the entrained flow rate, $q_e(t)$, can be obtained experimentally as a function of the jet reattachment location, X_R. This entrained flow rate

was determined by measuring the steady-state reattachment location of the power jet for steady-state control flows into the separation bubble region. The value of the steady-state control flow ranged from zero to a value which caused the jet to switch to the opposite wall. The geometry of the bistable device and the technique employed to determine the particular entrained flow rate used in the mathematical model will be described in a later section of this chapter. For the present, the entrained flow rate will be represented by:

$$q_e(t) = q_e(X_R) \tag{6-7}$$

where: X_R is considered a function of t.

Combining Equations (6-1), (6-6), and (6-7), then nondimensionalizing flow rates with the power jet flow rate, q_s, and the reattachment location with the power nozzle width, w, gives:

$$\frac{q_c(t)}{q_a} = \frac{q_e\left(\frac{x_R}{w}\right)}{q_a} + \frac{1}{q_a}\frac{dv_b}{d\left(\frac{q_c(t)}{q_a}\right)}\frac{d\left(\frac{q_c(t)}{q_a}\right)}{dt} + \frac{1}{q_a}\frac{dv_b}{d\left(\frac{x_R}{w}\right)}\frac{d\left(\frac{x_R}{w}\right)}{dt} \tag{6-8}$$

or

$$Q_c(t) = Q_e(X) + \frac{1}{q_a}\frac{dv_b}{dQ_c(t)}\frac{dQ_c(t)}{dt} + \frac{1}{q_a}\frac{dv_b}{dX}\frac{dX}{dt} \tag{6-9}$$

where:

$$Q_c(t) = q_c(t)/q_a$$

$$Q_e(X) = q_e(X)/q_a$$

$$X = x_R/w$$

By experimental observation, it was found that the angle, φ, which the control flow would deflect the power jet at the power jet nozzle could be approximated by:

$$\phi = \tan^{-1} Q_c(t) \tag{6-10}$$

Utilizing this angular deflection permits the volume of the separation bubble to be determined from the geometry of the offset inclined wall configuration. The detailed representation for expressing the separation bubble volume as a function of the power jet reattachment location and deflection angle is derived in Appendix D. From this representation, the bubble volume can be written as:

$$v_b = \frac{w^2}{2} F(\phi, X) \tag{6-11}$$

Substituting Equation (6-11) into (6-9) yields:

$$Q_c(t) = Q_e(X) + \frac{w^2}{2 g_a} \frac{dF}{dQ_c} \frac{dQ_c(t)}{dt} + \frac{w^2}{2 g_a} \frac{dF}{dX} \frac{dX}{dt} \tag{6-12}$$

or

$$Q_c(t_D) = Q_e(X) + \frac{dF}{dQ_c(t_D)} \frac{dQ_c(t_D)}{dt_D} + \frac{dF}{dX} \frac{dX}{dt_D} \tag{6-13}$$

where

$$t_D = \frac{2 g_a t}{w^2}$$, a dimensionless time variable.

The time variant control flow input is arbitrarily characterized by the exponential function; thus:

$$Q_c(t_D) = Q_0 (1 - \exp(-a t_D)) \tag{6-14}$$

where: a is a constant.

This representation allows the control signal to be defined in terms of the final signal magnitude and the signal rise time. The signal rise time can be defined as the time required for $Q_c(t)$ to go from 10% to 90% of its final value, Q_o. This type of signal characterization gives:

$$Q_c(t_D) = Q_o\left(1 - \exp\left(\frac{-2.1972}{t_{DRISE}} t_D\right)\right) \qquad (6\text{-}15)$$

where: Q_o = normalized final signal magnitude

$$t_{DRISE} = t_{D_{90\%}} - t_{D_{10\%}}$$

Also,

$$\frac{dQ_c(t_D)}{dt_D} = \frac{2.1972}{t_{DRISE}} Q_o \exp\left(\frac{-2.1972}{t_{DRISE}} t_D\right) \qquad (6\text{-}16)$$

Substituting Equations (6-15) and (6-16) into (6-13) yields a differential equation which relates the reattachment location of the power jet to the final value and rise time of the input control flow signal. The solution of Equation (6-13) can be used to predict the detachment time of an attached jet for non-step control flow inputs. Due to the implicit, non-linear nature of Equation (6-13), a numerical technique was developed to approximate a solution. This calculation algorithm is described in the next section.

Algorithm for Calculating Jet Detachment Time for Non-Step Control Flow Inputs

To calculate the jet detachment time for various control flow magnitudes and rise times, a numerical procedure was developed using

Equation (6-13) to predict the time response of the jet reattachment location as the jet shifted along the wall toward the point of detachment. To develop this procedure, Equation (6-13) was rearranged and integrated to give:

$$X_2 - X_1 = \Delta X = \int_{t_{D_1}}^{t_{D_2}} \left(\frac{Q_c(t_D) - Q_e(X) - \frac{dF}{dQ_c}\frac{dQ_c}{dt_D}}{\frac{dF}{dX}} \right) dt_D \quad (6\text{-}17)$$

where: X_1 - initial jet reattachment location at time, t_{D_1}

X_2 - final jet reattachment location at time, t_{D_2}.

By piecewise linearizing the functions of X under the integral in Equation (6-17) over the increment X, average values for $Q_e(X)$, $\frac{dF}{dX}$, and $\frac{dF}{dQ_c}$ can be obtained for instantaneous values of dimensionless time. The calculation scheme is to divide the attachment wall into many small increments and iteratively search for the upper integration limit, t_{D_2} which makes the right hand side of Equation (6-17) equal the ΔX value on the left hand side of the equation. The initial time at which the control flow is initiated is used as the first value of t_{D_1} (i.e., at $t_{D_1} = 0$). The time increment, $t_{D_2} - t_{D_1}$, is the time required for the jet to travel ΔX distance along the attachment wall. The integral term of Equation (6-17) was numerically evaluated by employing Simpson's rule for integration. The functions $Q_c(t_D)$ and $\frac{dQ_c}{dt_D}$ were obtained from Equations (6-15) and (6-16), respectively. A value for the entrained flow $Q_e(X)$ was found from the experimentally determined function defined by Equation (6-7). This flow value was assumed a constant average value over the increment, ΔX. The partial derivative, $\frac{dF}{dQ_c}$, was obtained by numerically differentiating F with respect to instantaneous values of Q_c

at the appropriate average value of X. The partial derivative, $\frac{dF}{dX}$, was evaluated by numerically differentiating F with respect to the appropriate average value of X at instantaneous constant values of Q_c. A central difference scheme was employed to perform the above differentiations.

Due to the well behaved monotonic nature of the functions involved in the integration, a simple bracket and search routine was found sufficient to converge on the value of t_{D_2} which balanced the two sides of Equation (6-17). After a value of t_{D_2} had been determined for a given ΔX, this t_{D_2} could then be used as the initial value of time for the next ΔX increment. The calculations were continued in this fashion until the value of X reached the experimentally determined point of jet detachment. The total value of dimensionless time required for the jet to travel from the initial reattachment location to the jet detachment point was obtained as the cumulative sum of the Δt_D increments obtained for each of the ΔX increments.

The block diagram for the digital computer program used to implement the above iterative integration procedure is given in Figure 35. The Fortran IV computer program used for the actual calculations is included in Appendix E. Typical computed results for a particular bistable model geometry are shown in Figure 36. The curves in Figure 36 represent the displacement of the dimensionless reattachment location of the power jet as a function of time for a constant control signal magnitude with different control signal rise times.

Calculated Jet Detachment Response Times

The mathematical model developed in the previous section was used

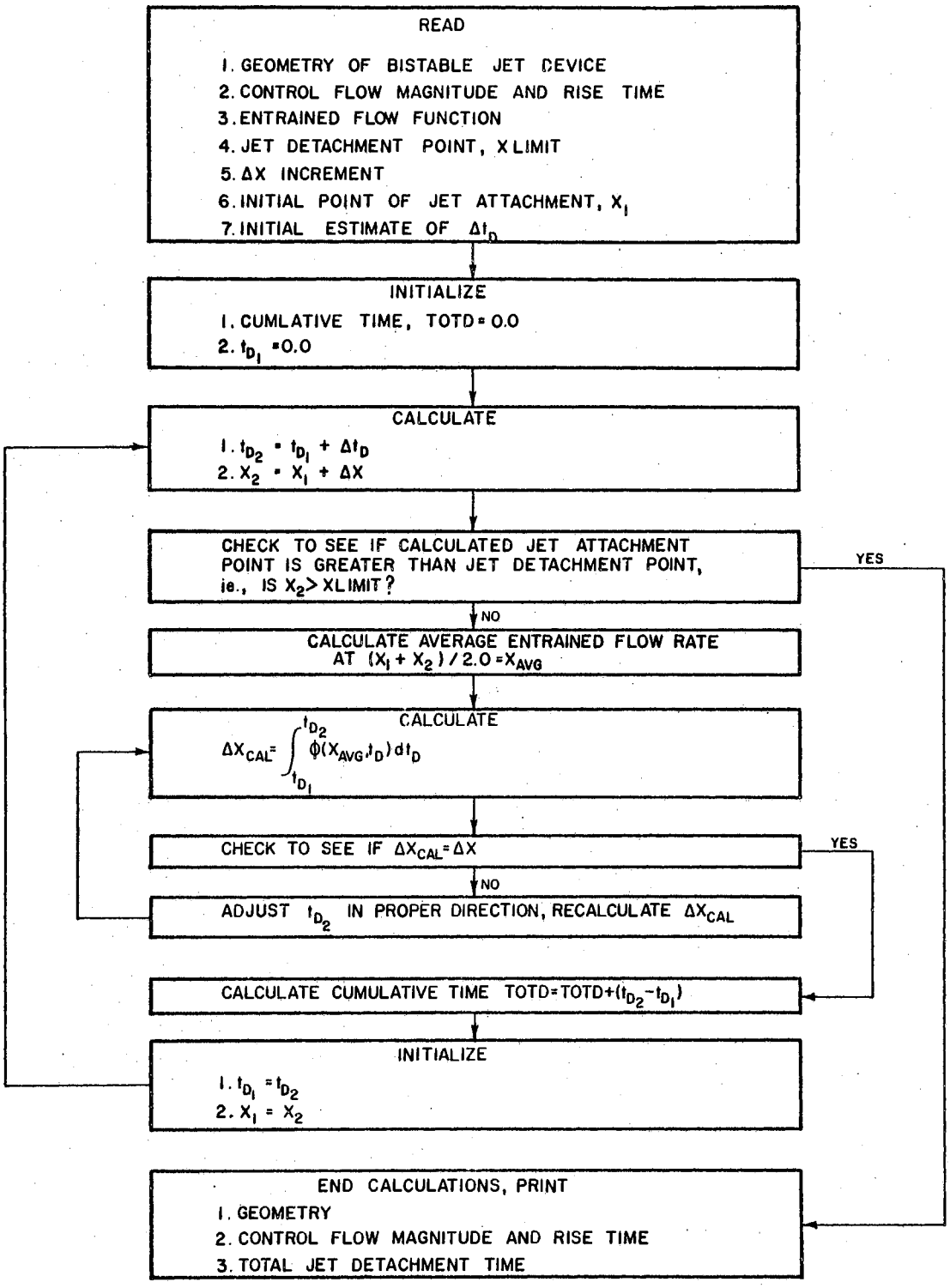

Figure 35. Computer Program Block Diagram for Computing Attached Jet Response Time

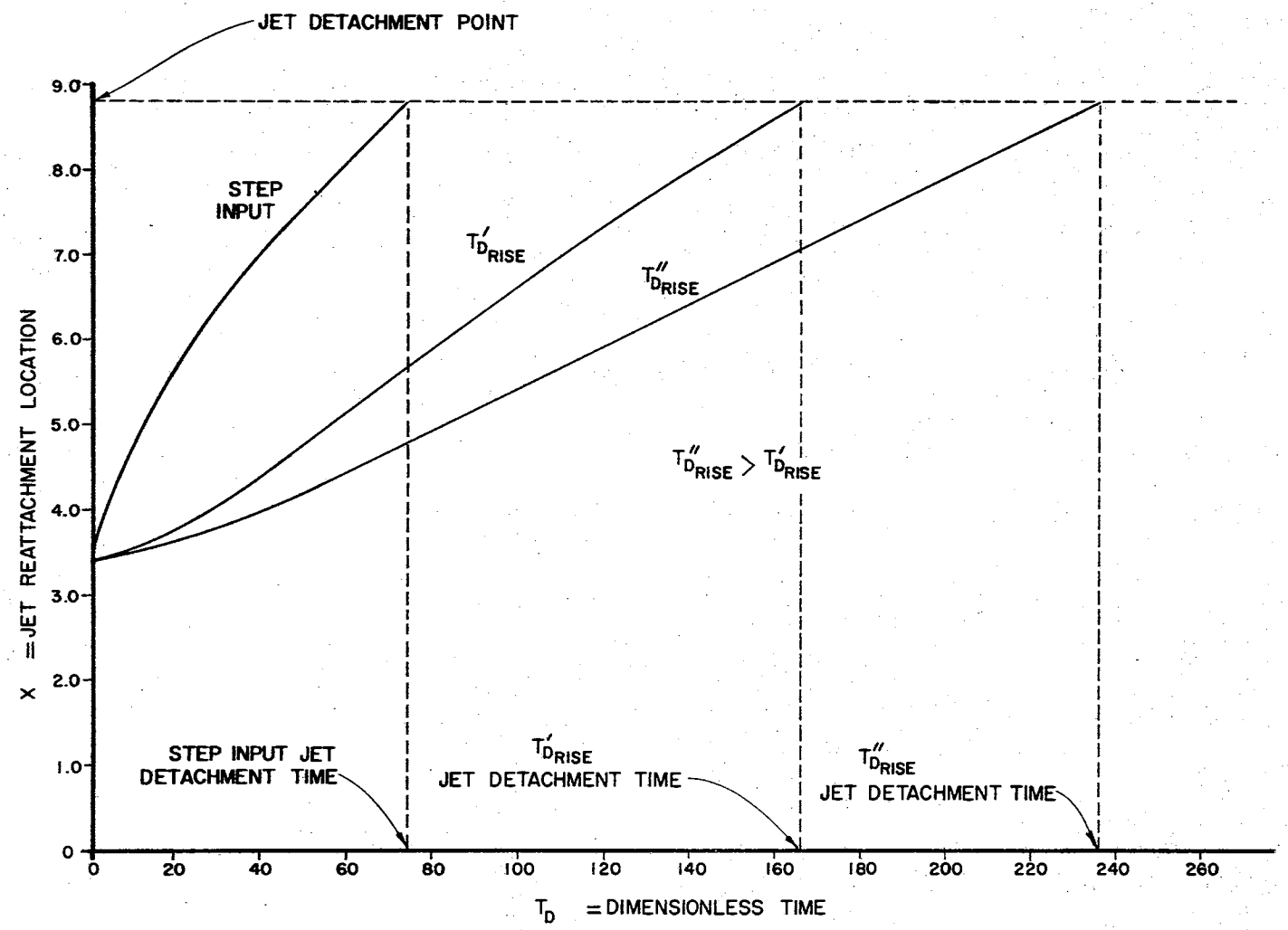

Figure 36. Typical Calculated Attached Jet Response Time

to calculate the detachment time of an attached jet for non-step control flow inputs. This calculation required that the entrained control flow rate function be determined experimentally by employing a specific geometric configuration to measure the steady-state attachment location of the jet as a function of the steady-state control flow. The procedure employed for obtaining this entrained control flow function is explained in the following discussion.

Entrained Control Flow Rate

As noted in the formulation of Equation (6-7), by assuming quasi-steady flow into the attached jet separation region, the flow entrained from the separation bubble region during the detachment process would equal the value of steady-state control flow required to maintain the jet at a steady-state reattachment location. To obtain an experimental estimate of the entrained flow function, the planar reattaching submerged jet model shown schematically in Figure 40 was employed. Water was used as the operating fluid for the device. The power jet of the model was maintained at a constant flow rate while a constant control flow was supplied into the separation bubble region for each reatrachment location measurement. The opposite control port was open to the atmosphere during all experimental tests.

The reattachment region of the power jet was detected at the various control flows by injecting minute air bubbles through the attachment wall and observing which direction the bubbles were carried when they first made contact with the power jet. The bubbles upstream of the reattachment region were carried up the plate toward the power nozzle exit and back into the separation bubble region. The air bubbles

downstream of the reattachment location were carried down the wall out of the separation bubble region. The reattachment region obtained in this manner is shown in Figure 37. The reattachment point locations for use in the computer calculations were obtained by interpolating to the midpoint of the experimentally determined reattachment region. The discontinuities in the experimental data can be attributed to the finiteness of the number of injection holes which could be drilled in the attachment wall. The steady-state control flow rate representing the entrained flow rate was nondimensionalized with the power jet flow rate; the reattachment location with the power nozzle width at the nozzle exit.

It should be noted that numerous investigators (14, 23, 26) have expended considerable effort in attempting to derive analytical reattaching jet models which can be used to predict the entrained flow function. The development of an accurate analytical reattaching jet model for universal bistable jet geometries and operating conditions represents a very complex fluid mechanics problem and to the author's knowledge, no such model exists.

A simplified reattaching jet model described by Sher (29), who modified previous work by Brown (2) and Bourque and Newman (1), was used in the present work in an attempt to analytically predict the entrained flow function. These results are compared with the author's experimental data in Figure 38. For the modified Bourque and Newman model, the usual procedure for matching the analytical calculations with experimental data, for a given geometry, is to vary the constant,

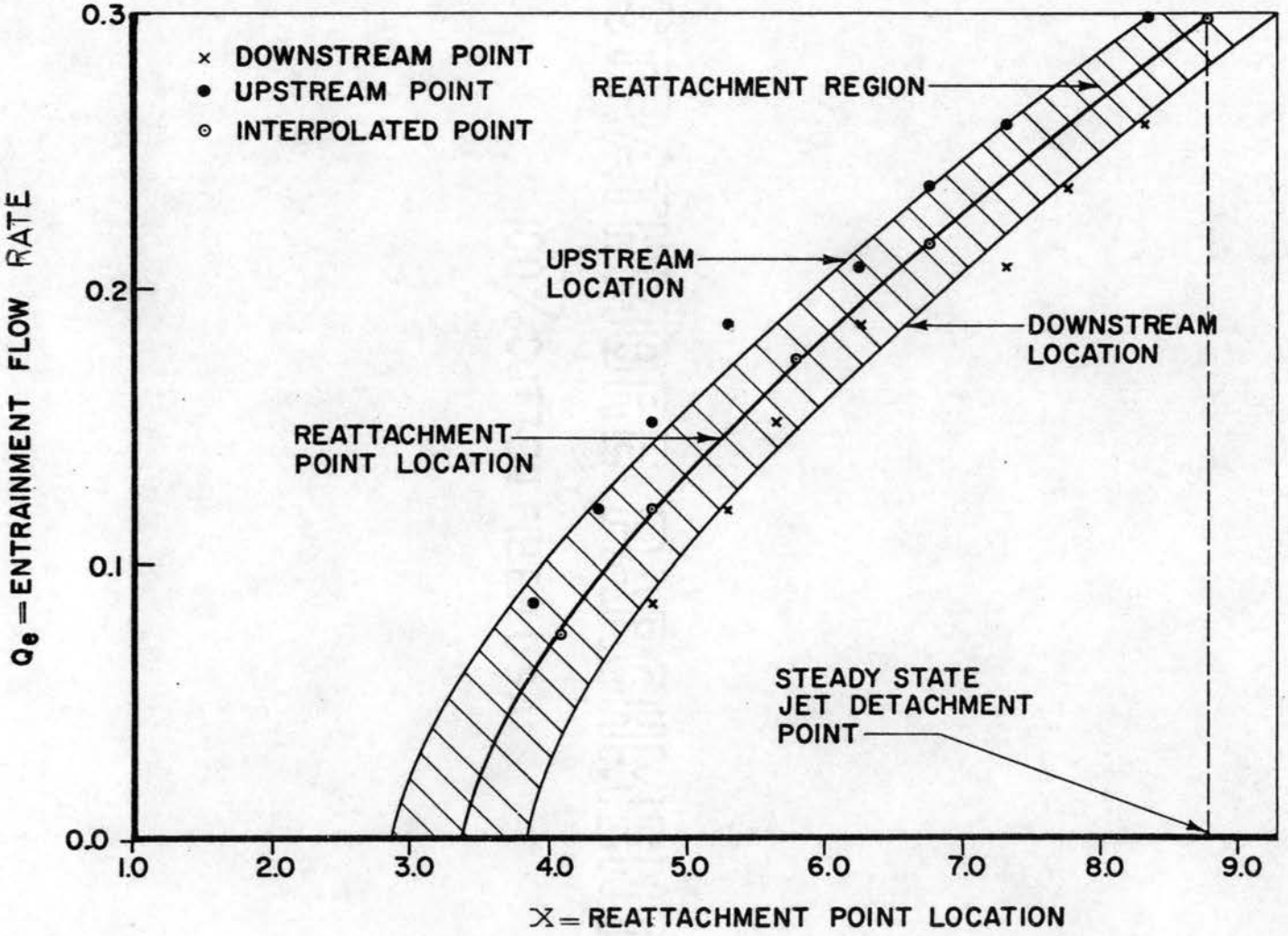

Figure 37. Experimentally Determined Entrained Control Flow Rate

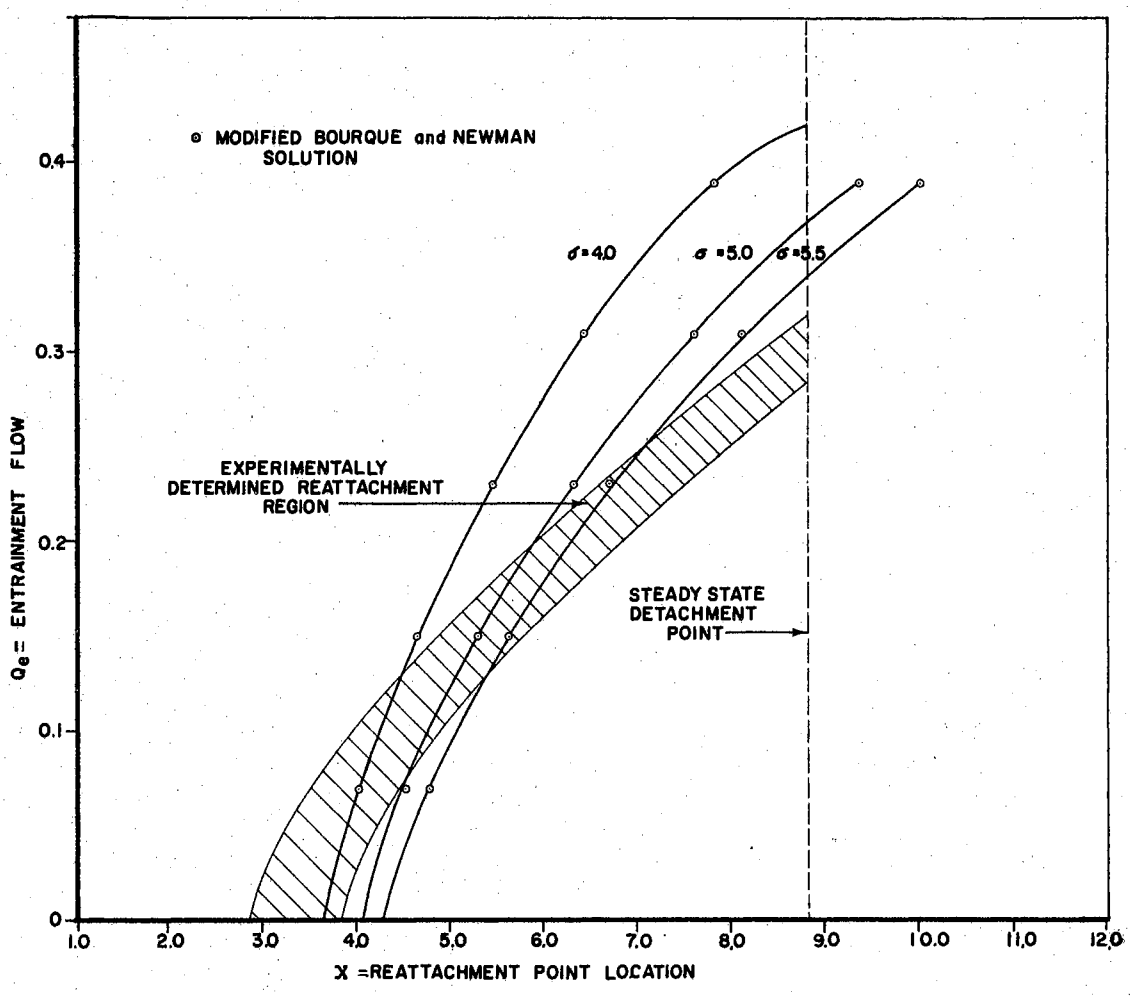

Figure 38. Comparison of Experimental Entrained Flow With Analytical Predictions of a Modified Bourque and Newman Reattaching Jet Model

σ,* in the reattaching jet equations which describe the model. It can be seen that considerable error would result, in this case, by employing any of the entrainment flow functions predicted by the modified Bourque and Newman model.

Sher (29) concluded that $\sigma = 4.0$ could be employed to define the modified Bourque and Newman reattaching jet model of similar double wall geometry (i.e., aspect ratio = 4.0; wall offset = 0.89; inclined wall angle = 10°) to that employed in the present study. However, the experimental reattachment region in Figure 38 was determined with the opposite control port open to atmospheric pressure; whereas, Sher's experimental data was obtained for a closed opposite control port. Closing the opposite control port decreases the pressure drop across the attached jet which decreases the amount of control flow required to detach the jet from the wall. For this reason, the entrained flow function employed in the present study and that determined by Sher do not represent comparable situations.

Other reattaching jet models such as the one proposed by Olson (23) were considered for use in the present study; but due to insufficient experimental data concerning the shear rates on the two sides of the power jet , these models were not incorporated into the work.

Calculated Results

The algorithm described previously for solving Equation (6-17) was

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*For a free jet issuing into a quiescent body of fluid, σ can be related to the spread rate of the jet (27). For a reattaching jet, this constant represents an empirical parameter that is used to take care of everything in the jet flow which cannot be otherwise described.

employed to calculate jet detachment times for a range of input control signal rise times at various control flow magnitudes. Numerical values for the dimensions needed in the calculations were obtained from the physical dimensions of the experimental attaching jet model shown in Figure 40.

Dimensionless time defined by the parameter, $\frac{2g_o t}{w^2}$, was used in the computations. This dimensionless time was then converted to a different dimensionless time scale defined by the ratio of jet response time to the transport time of the power jet employed in the experimental attaching jet model. The transport time of the power jet was calculated as the time required for a fluid particle moving at the average velocity of the power jet to travel from the power nozzle exit to the point of steady-state jet detachment. This transport time was employed to nondimensionalize all real time scales used in the study. A response time nondimensionalized with a characteristic transport time is usually designated as the Strouhal number. This designation will be employed to describe the time responses involved in the following discussion.

The results of the jet detachment time calculations are shown in Figure 39. The parameter, S_D, represents the Strouhal number for the jet detachment time; S_{RISE} denotes the Strouhal number for the control signal rise time. The dimensionless flow rate, Q_c, was defined previously as the ratio of control flow magnitude to power jet supply flow magnitude. A new dimensionless flow rate, $\bar{Q}_c$, was defined as the ratio of control flow magnitude to the control flow magnitude required to switch the jet under steady-state conditions. The parameter, $\bar{Q}_c$, was interpreted to be a measure of the excess flow being supplied to switch the bistable jet as compared to the minimum amount of flow required to

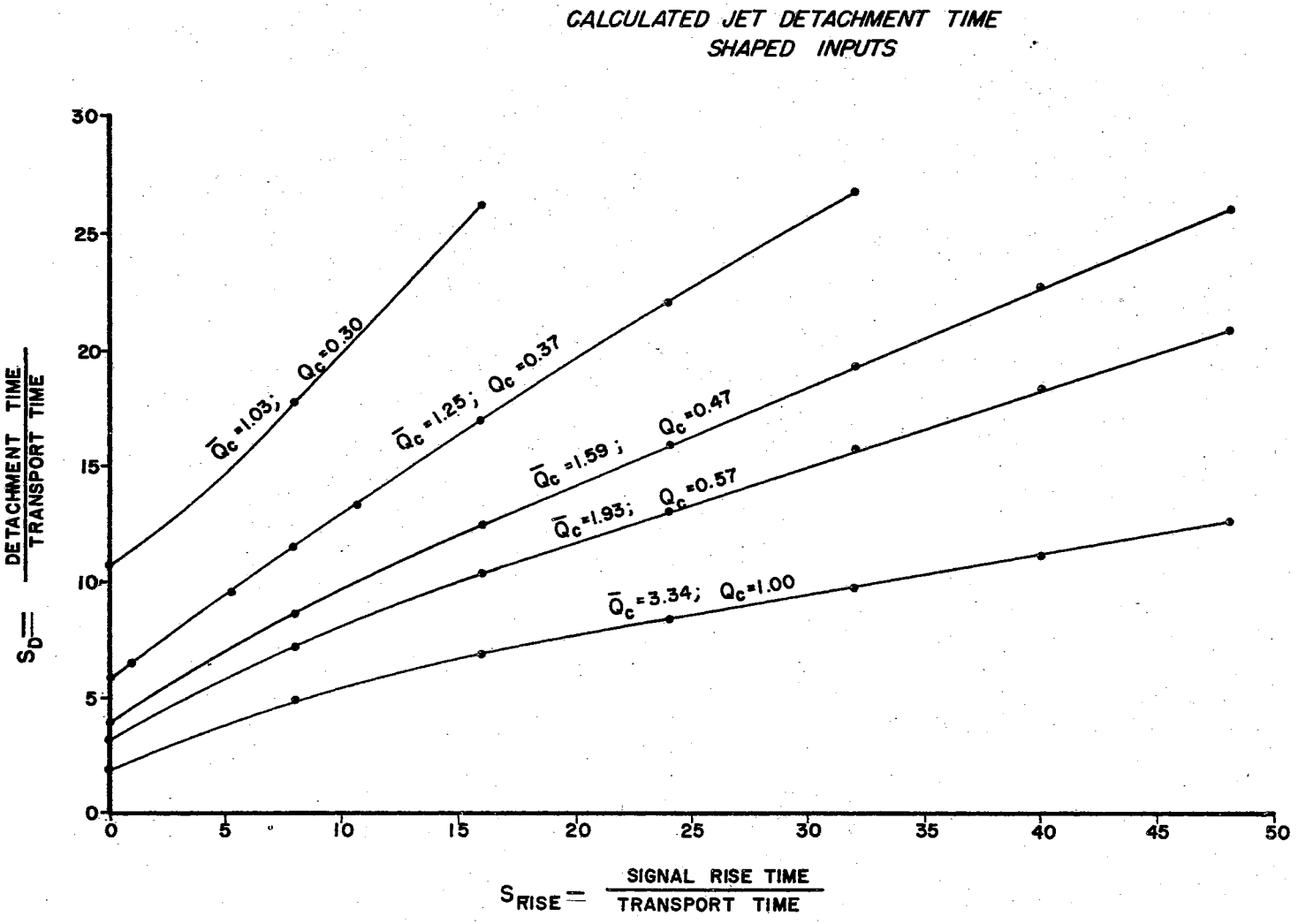
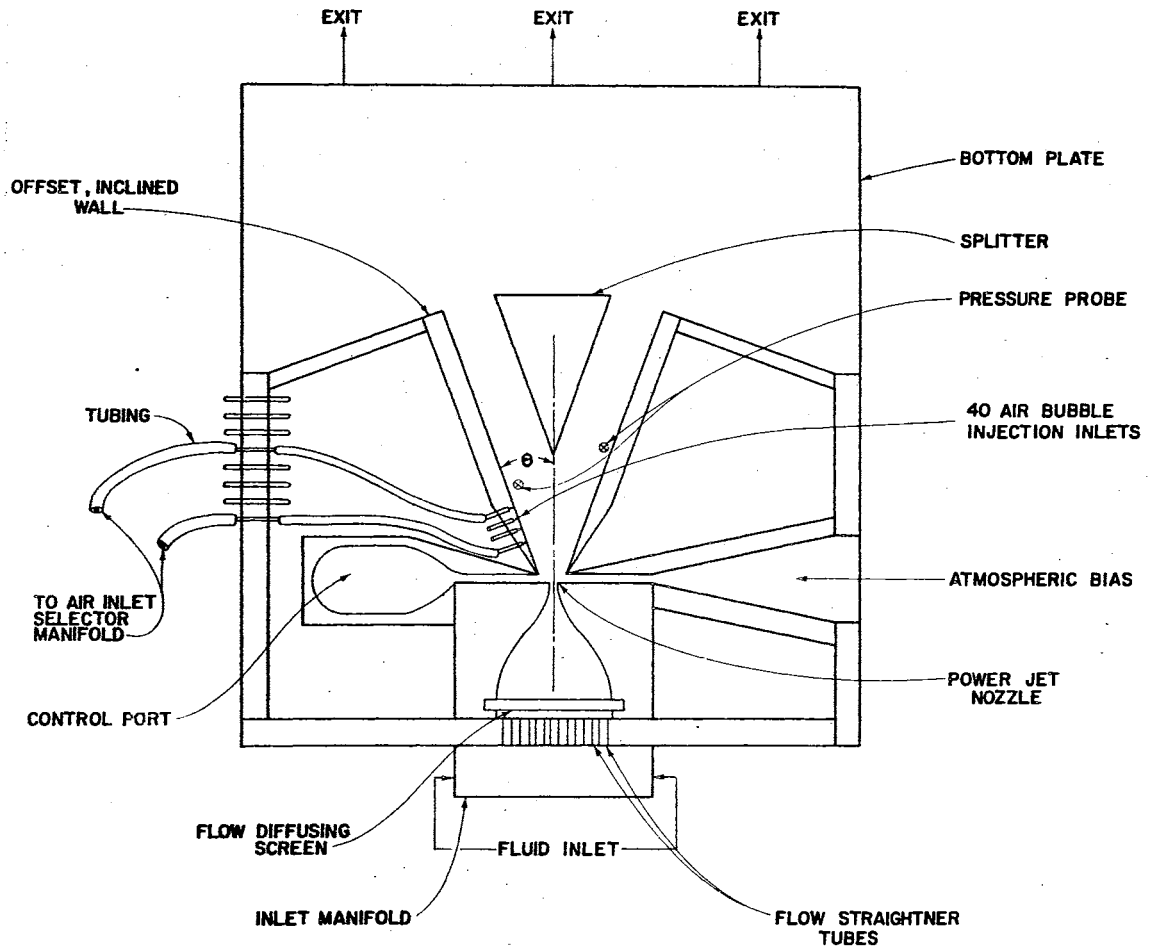


Figure 39. Calculated Jet Detachment Time for Exponentially Shaped Input Control Signals



PERTINENT
BISTABLE JET MODEL DIMENSIONS

Overall Width	- 12 in.
Overall Length	- 12 in.
Power Nozzle Width	- 0.25 in.
Power Nozzle Height	- 1.0 in.
Nozzle Contraction Ratio	- 5.0 in.
Inclined Wall Offset	- 0.221 in.
Inclined Wall Length	- 4.27 in.
Inclined Wall Angle	- 10°
Distance to Splitter from Nozzle Exit	- 2.53 in.
Control Port Width	- 0.25 in.

Figure 40. Schematic of Experimental Reattaching Jet Model

switch the jet (i.e., a measure of how much the bistable jet amplifier was being overdriven). As shown in Figure 39, values of jet detachment time were calculated over a $\bar{Q}_c$ range of 1.03→3.34 for signal rise times varying from 0 (step input) to 48 times the transport time of power jet. The value, $\bar{Q}_c = 3.34$, corresponded to the ratio $Q_c = 1.00$ or where the control flow to the experimental jet equaled the power jet supply flow.

Some interesting and potentially useful trends for use in controlling the switching time of a bistable jet device can be seen to occur to the jet detachment time as the rise time of the control signal increases. For example, consider the case of controlling the detachment time of the bistable jet using a control signal with a constant rise time of $S_{RISE} = 8.0$. The jet detachment time is predicted to vary from $S_D = 5.0$ for $\bar{Q}_c = 3.34$ to $S_D = 11.5$ for $\bar{Q}_c = 1.25$. Thus, the jet detachment time could be adjusted by a factor of 2.3. by varying only the control signal magnitude. However, if the rise time of the control signal could be increased to $S_{RISE} = 32$, the jet detachment time could be increased to $S_D = 27$, a factor of 5.4 slower than the original detachment time of $S_D = 5.0$.

By using control signal adjustment to control the response time of a bistable jet, the asynchronous fluidic circuit designer could construct a bistable jet feedback delay element capable of very fast operating times, but which would also possess the ability of being slowed in a controlled manner to provide additional delay in the asynchronous circuit feedback paths when essential hazards in the circuit created the need for such delays. This method of control would depend on whether the total switching time of the bistable jet followed the same trend for non-step inputs as that mathematically predicted for the jet detachment

response times. The experimental program described in the next section was concerned with investigating the effects of control input signal shape and magnitude on the total switching time of a bistable jet.

Experimental Program

The trends exhibited by the analytical jet detachment time model indicated that the total switching time of a bistable jet fluid amplifier might be varied significantly by adjusting the shape and/or magnitude of the control signal to the element. Thus, an experimental program was initiated to further investigate and evaluate the effects of control signal adjustment on the total time response of the bistable jet device. A secondary purpose of the experimental program was to check the validity of the analytical jet detachment model calculations. To accomplish these objectives, a bistable jet model with appropriate accompanying circuitry was constructed to measure jet response times for variable input control signal shapes and magnitudes.

Description of Experimental Apparatus and Testing Procedure

The two-walled, bistable jet model employed in the experimental program is shown schematically in Figure 40. A photograph of the device is given in Figure 41. The various parts of the device were cemented into position on a bottom plexi-glass plate, then an upper plexi-glass cover plate was fastened through to the bottom plate to form a sandwich type, two-dimensional model. Sealing of the flow passages with the side plates was accomplished with flat rubber-gaskets and silicon rubber glue. The power nozzle exit width was set at 0.25

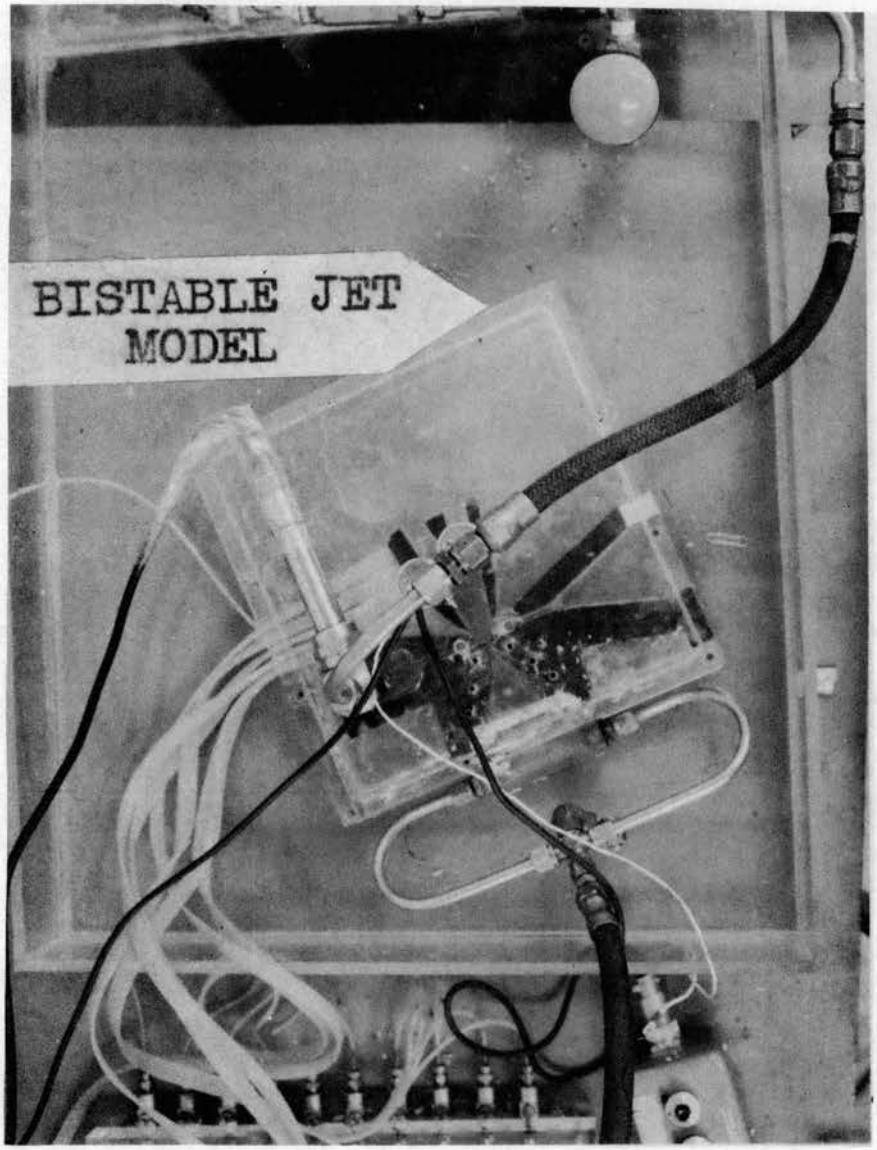


Figure 41. Photograph of Experimental Reattaching Jet Model

inches; the height of the nozzle block was 1.0 inches making the aspect ratio for the device equal to 4.0.

Water was supplied to the power nozzle at a constant rate of 2.41 gallons per minute at a temperature of 70°F. A power jet Reynolds number, based on the power nozzle width, of approximately 6070 was maintained with this flow. The power jet was vented to atmospheric pressure for all tests. During operation, the model was submersed under water in an open tray. The tray was constructed such that a constant water height was maintained over the model. The water was exhausted to drain over a weir at the end of the tray.

The power jet was biased to one of the offset-inclined walls of the device by closing one control port and opening the other control port to atmospheric pressure. The offset wall to which the power jet was biased (i.e., the attachment wall) contained forty air bubble injection holes located at the centerline of the wall and spaced approximately 0.1 inch apart. These air bubble injection holes were used to determine the entrained control flow function required to identify the previous described mathematical jet detachment model. A fixed position pitot pressure probe was located at the steady-state detachment point (X = 8.8x (nozzle width)) along the attachment wall. Another fixed position pitot pressure probe was located at X = 11x (nozzle width) distance along the opposite side wall.

The control port widths of the device were constructed to equal the power nozzle width. The walls of the model were offset a distance of 0.885x (nozzle width) from the power nozzle exit. The inclination angle of the walls was set to be 10° from a line running parallel with the power nozzle centerline. The length of the offset-inclined walls was

approximately 17x (nozzle width). The flow splitter was located at a distance 10x (nozzle width) from the nozzle exit on the centerline of the power nozzle.

The schematic diagram in Figure 42 illustrates the circuitry used in conjunction with the bistable jet model to perform the transient switching time tests. The exponentially shaped control flow signals into the separation bubble region of the attached jet were generated using a quick opening valve followed by an air volume accumulator in the control line leading to the control port of the bistable jet model. The rise time of the control flow signals was varied by changing the volume of the air accumulator. The magnitude of the signal was varied by adjusting a valve in the control line upstream from the quick opening valve. Step inputs were generated by removing the accumulator from the control line. A dynamic impact flow meter was used to obtain an instantaneous measure of the flow into the separation bubble region. A pressure transducer was employed to measure the total stagnation pressure signals at the probe locations along the offset-inclined walls. The pressure transducer signal and flow meter signal were displayed simultaneously on a dual beam oscilloscope.

The response times of the wall attached jet for the various control signals were determined by measuring the time which elapsed between the beginning of the control flow signal and the time required for the pressure at the respective pressure probe to decrease or increase to 50% of its final value. This 50% value was arbitrarily chosen for establishing a reliable and convenient location on the transient pressure trace to determine jet response time. An estimate of the jet detachment time for

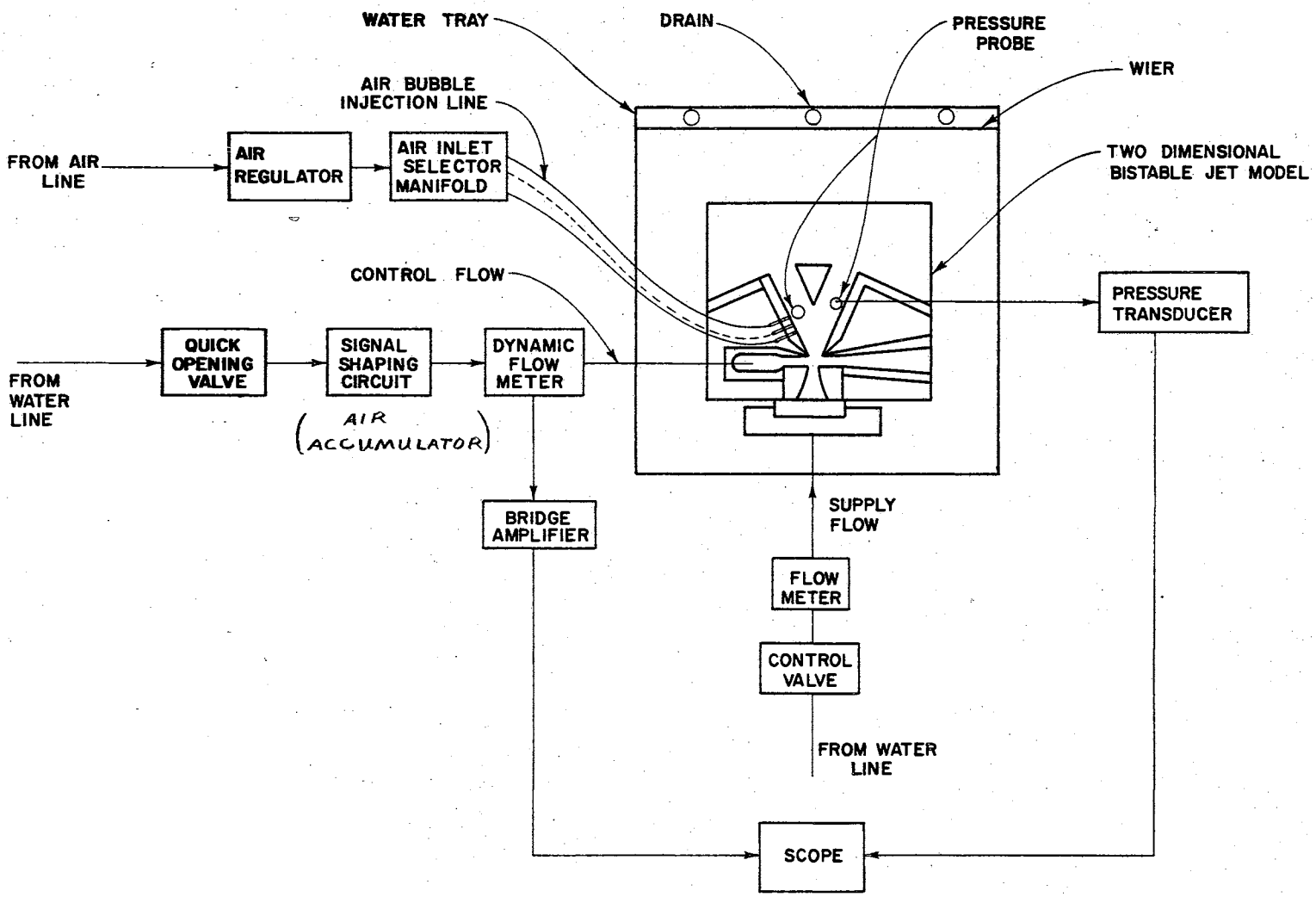
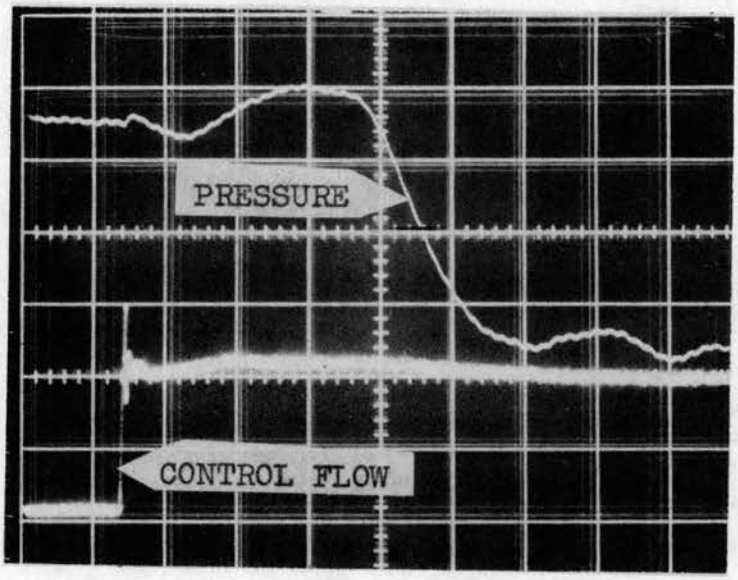


Figure 42. Schematic of Test Circuit for the Reattaching Jet Model Study

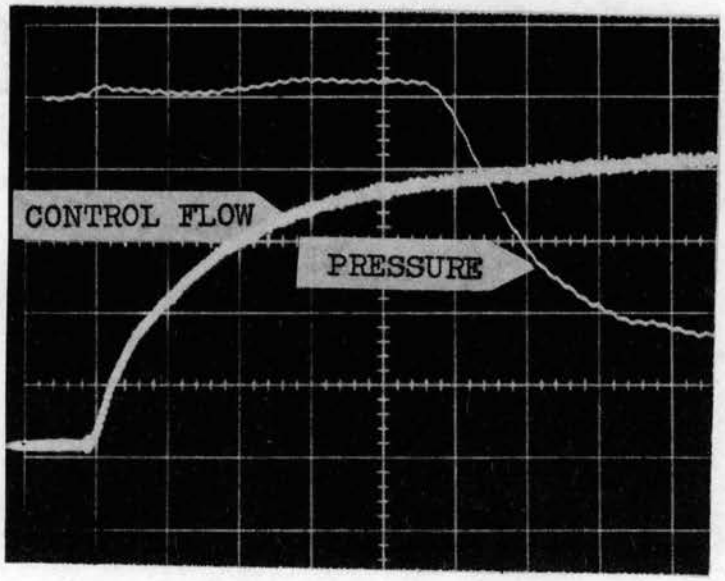
step inputs was obtained in this manner by measuring the pressure at the probe on the attachment wall. An example of one of the oscilloscope photographs obtained for the step input response is shown in Figure 43 (a). It was estimated that the step input signal reached final magnitude in a time less than 1% of the response time of the switching jet during all experimental step input tests. A similar estimate for the total switching time of the jet was obtained by measuring the pressure at the probe location near the opposite wall. The photograph shown in Figure 43 (b) illustrates a typical total switching time response for a shaped input control signal.

Definition of Reliable Switching Region

Preliminary response time tests on the experimental jet model revealed that limits would have to be established on both the magnitude and rise time of the control signals used to switch the jet before reliable jet switching could be expected. Qualitatively, this meant that certain regions on the detachment time curves given in Figure 39 had to be excluded to achieve a controlled switching time of the bistable jet. The preliminary test results showed that the unshaded portion of Figure 44 could be employed to approximately define the limits of this controlled switching region for the particular geometry and loading conditions of the bistable jet model employed in the study. This figure shows clearly that the limits of the controlled region are a function of both the magnitude and rise time of the control signal to the bistable jet element. The limits of the control region will also likely depend on the geometry and loading conditions of the particular bistable element being controlled together with the required operational



(a) Step Input Response



(b) Shaped Input Response

Figure 43. Typical Transient Data Obtained From the Reattaching Jet Model Study

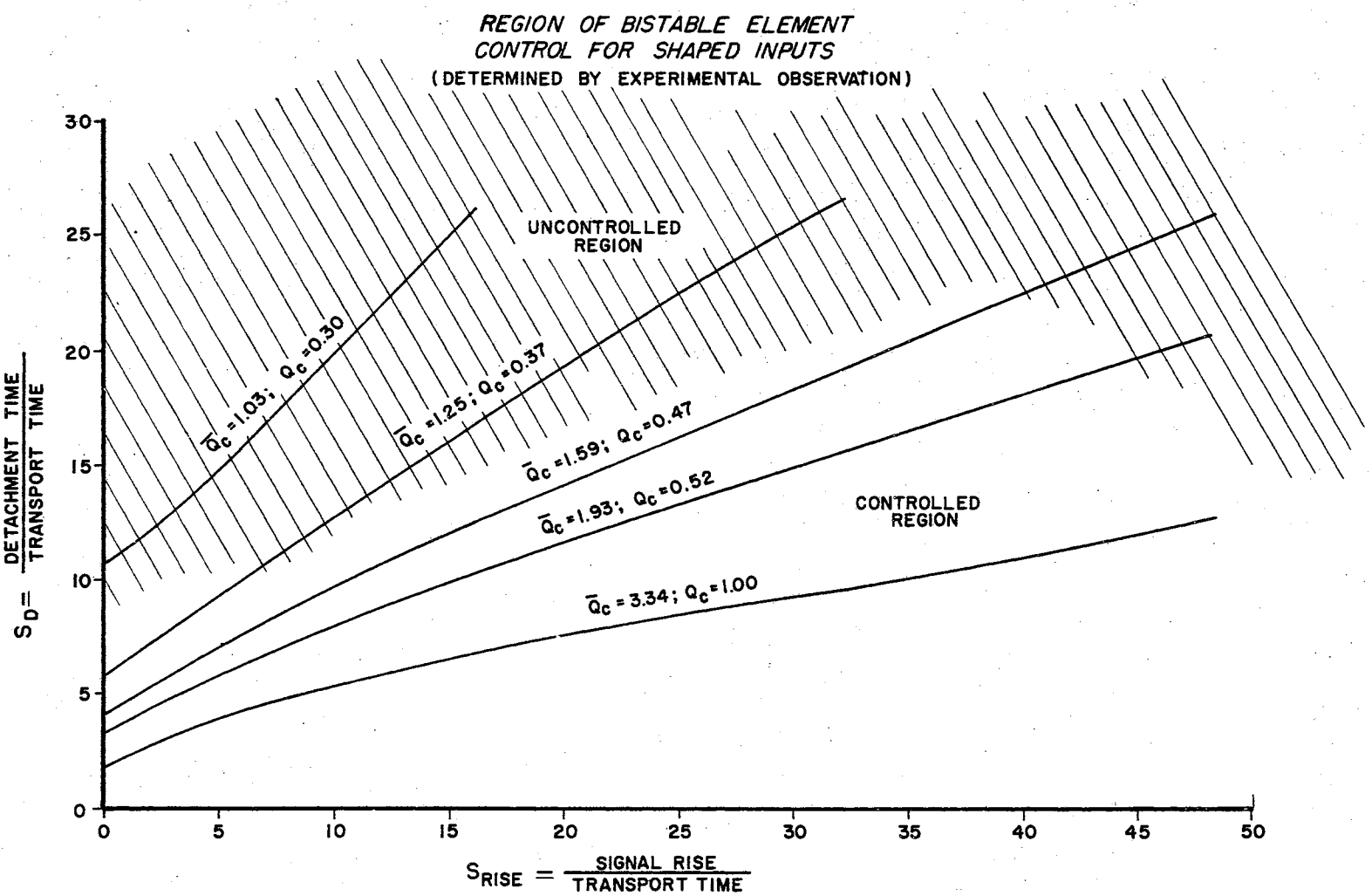


Figure 44. Definition of Control Region for the Experimental Bistable Jet Model

reliability of the element.

The definition of such a controlled switching region implies that similar practical limits will always be encountered when the switching time of a bistable jet element is being controlled by varying the control signal to the element. Further study concerning a more quantitative definition of the factors which effect the limits of the observed control region was not pursued.

Analytical Model Verification

The jet detachment time predicted by the analytical model used to derive Equation (6-17) was verified by comparing the predicted response times with experimentally determined estimates of the jet detachment time. The experimental detachment times were obtained from pressure responses at the steady-state detachment point of the experimental model for step input control flow signals into the control port of the model. As described previously, the pressure response time was determined as the time required for the pressure at the probe to decrease to 50% of its final magnitude.

All involved times were nondimensionalized with the jet transport time. This particular nondimensionalization was also employed by Olson (24) in a related attaching jet response time study. Olson employed a single wall model to measure the response of an attached jet to a step input control signal. Olson's jet response data together with the 50% pressure response time data derived from the present study is shown in Figure 45. It can be seen that the 50% pressure response time data and Olson's experimental jet response time data bracket the calculated jet detachment time.

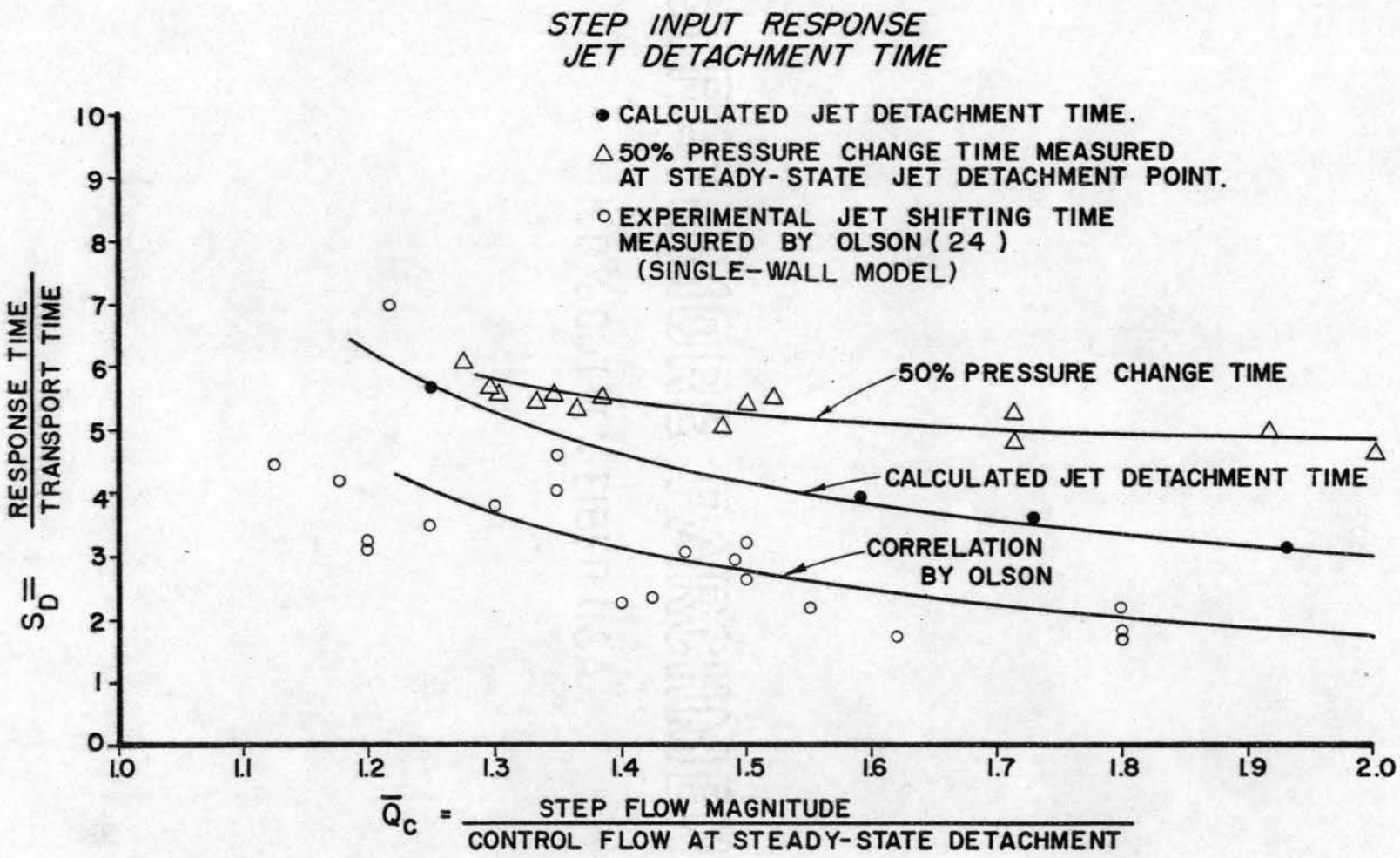


Figure 45. Experimental Verification of Numerical Calculations for Jet Detachment Time

As noted previously, the 50% pressure change time value was chosen arbitrarily for convenience in interpreting the pressure traces. If a different reference, say 10% pressure change time, had been selected to experimentally represent the jet detachment point, the correspondence between analytical prediction and experimental measurement could be improved over that shown in Figure 45. Due to the uncertainty involved in defining an experimental jet detachment time base, a detailed appraisal of the calculated jet detachment times was not possible. It was concluded, however, that the analytical model developed previously in this chapter could be employed to reasonably estimate jet detachment time trends.

Total Switching Time Results

An experimental estimate of the total switching times for the bistable jet model was determined by measuring the pressure response at the wall opposite the active control port of the model. A switching time correlation for step input control signals to the model was first established. The results of the step input tests are shown in Figure 46. The total switching time of the model can be seen to increase more rapidly than the jet detachment time as the magnitude of the step input control flow is decreased. This would suggest that the traverse time of the switching jet is not a constant for all control flow magnitudes as suggested by Johnson (13).

After the step-input switching time tests had been completed, similar total switching response time determinations were conducted for shaped input control signals. The results of the shaped input tests are shown in Figure 47. The experimental results indicate that the effects produced on the total switching time of a bistable jet element by

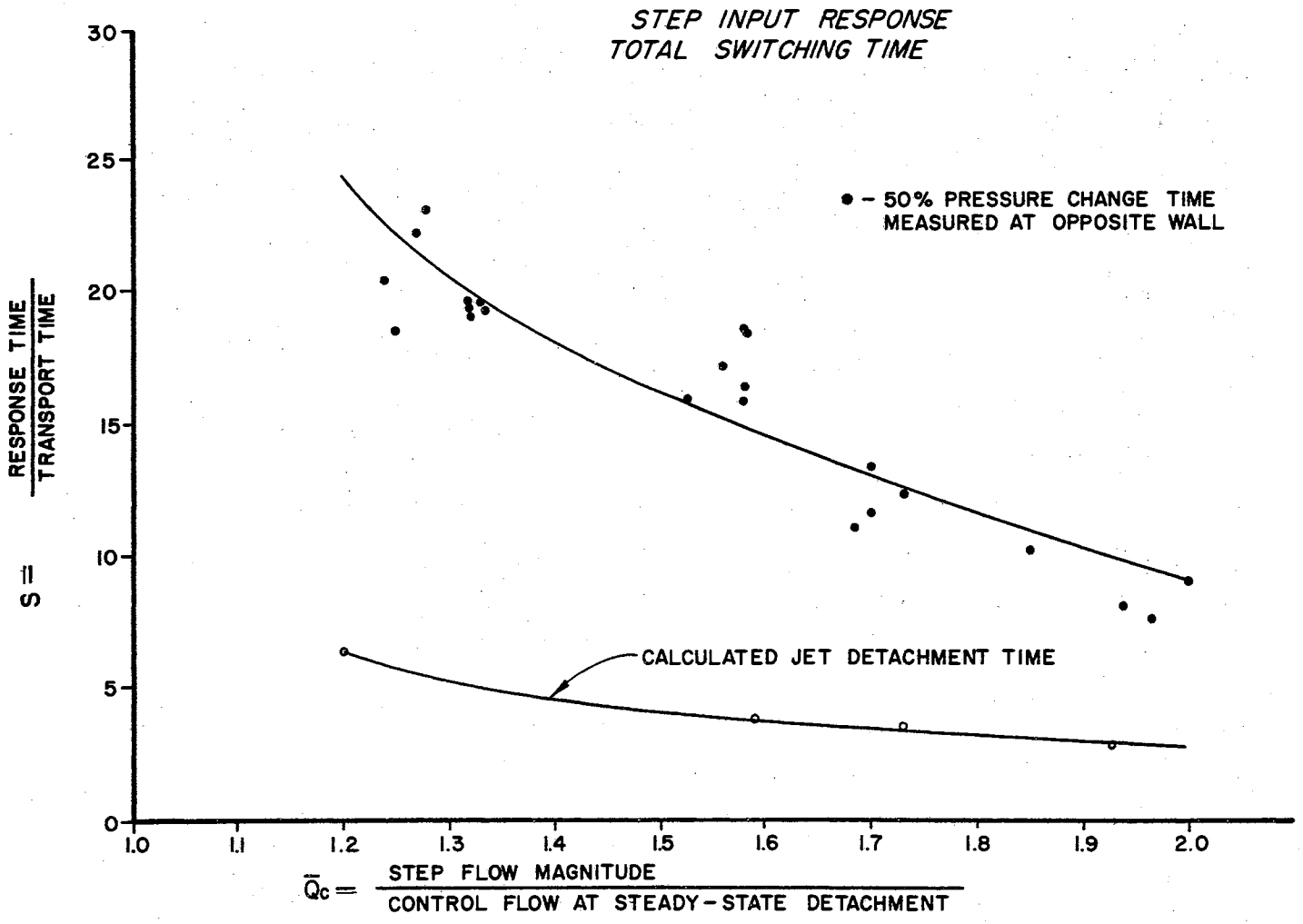


Figure 46. Total Switching Time Correlation for Step Input Control Signals

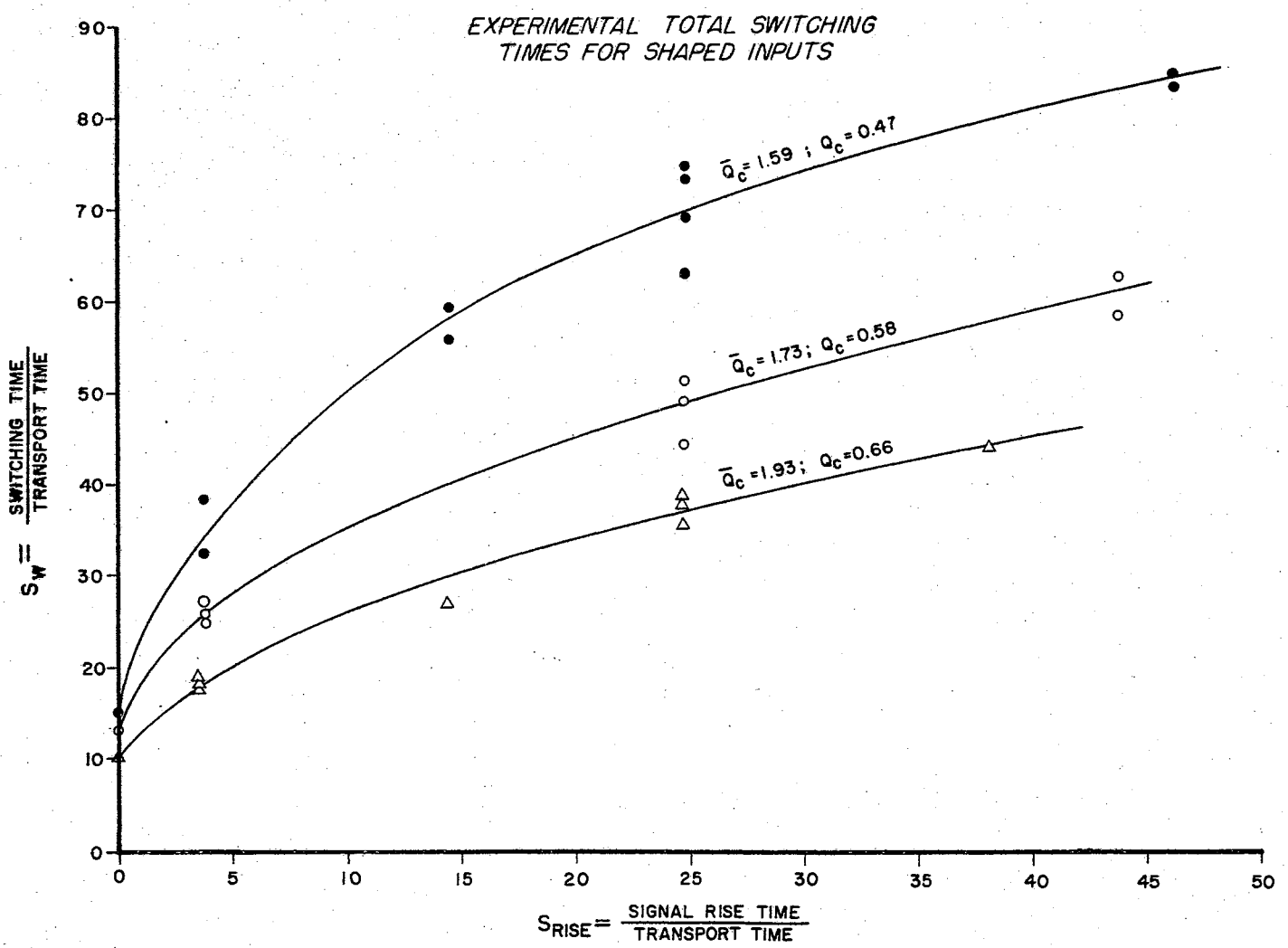


Figure 47. Total Switching Time Experimental Results for Exponentially Shaped-Input Control Signals

control signal adjustment would be similar to the trend predicted for the jet detachment time by the analytical jet detachment time calculations. As shown in Figure 47, the total switching time of a bistable jet model can be slowed by a factor of approximately 3 to 4 over the range of signal magnitudes and shapes employed in the study. It can be seen that signal shaping effects become more influential on the total switching time as the control flow magnitude decreases. Also evident is the possibility of further decreasing the total switching time by increasing the control signal magnitude, thus increasing the switching time control range at constant signal rise times. However, the results of the step input tests in Figure 46 indicate that an asymptotic switching time limit would be reached for large control flow magnitudes.

Traverse Time Determination

The effects of the shaped control inputs on the traverse time for the switching jet can be estimated by subtracting the calculated jet detachment time from the experimentally determined total switching time. This subtraction operation is shown in Figure 48. The traverse time for shaped signal inputs nondimensionalized with the traverse time for step inputs is shown in Figure 49 as a function of the control signal rise time. This figure indicates that the traverse time would increase rapidly as the control signal magnitude was decreased below the minimum flow employed in the tests. Reference to Figure 44 shows that as the control signal magnitude is decreased, the region of uncontrolled switching will be approached. This would offer an explanation for the above anticipated rapid increase in jet traverse time.

To further show the effects of signal shaping on the traverse time,

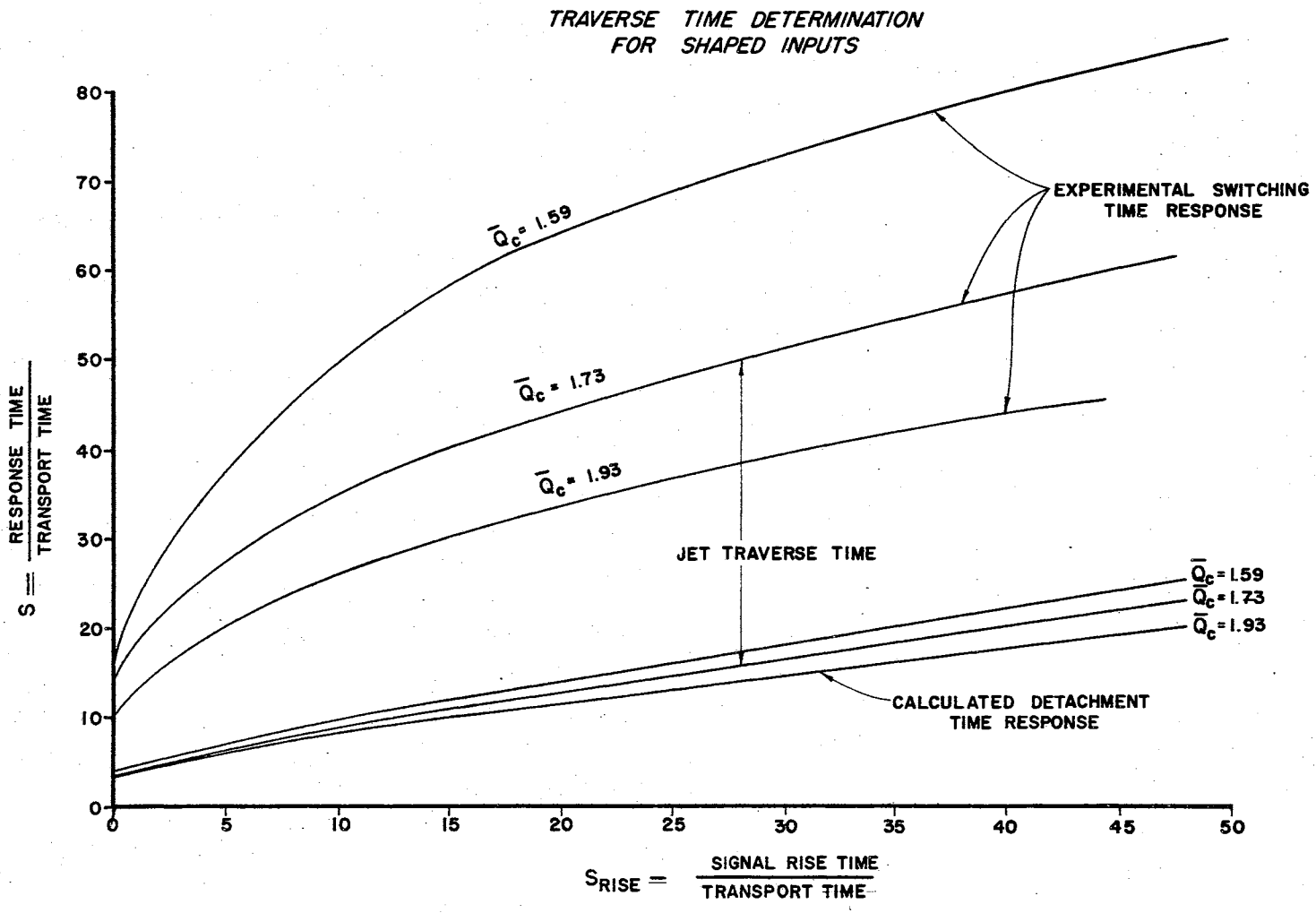


Figure 48. Traverse Time Determination

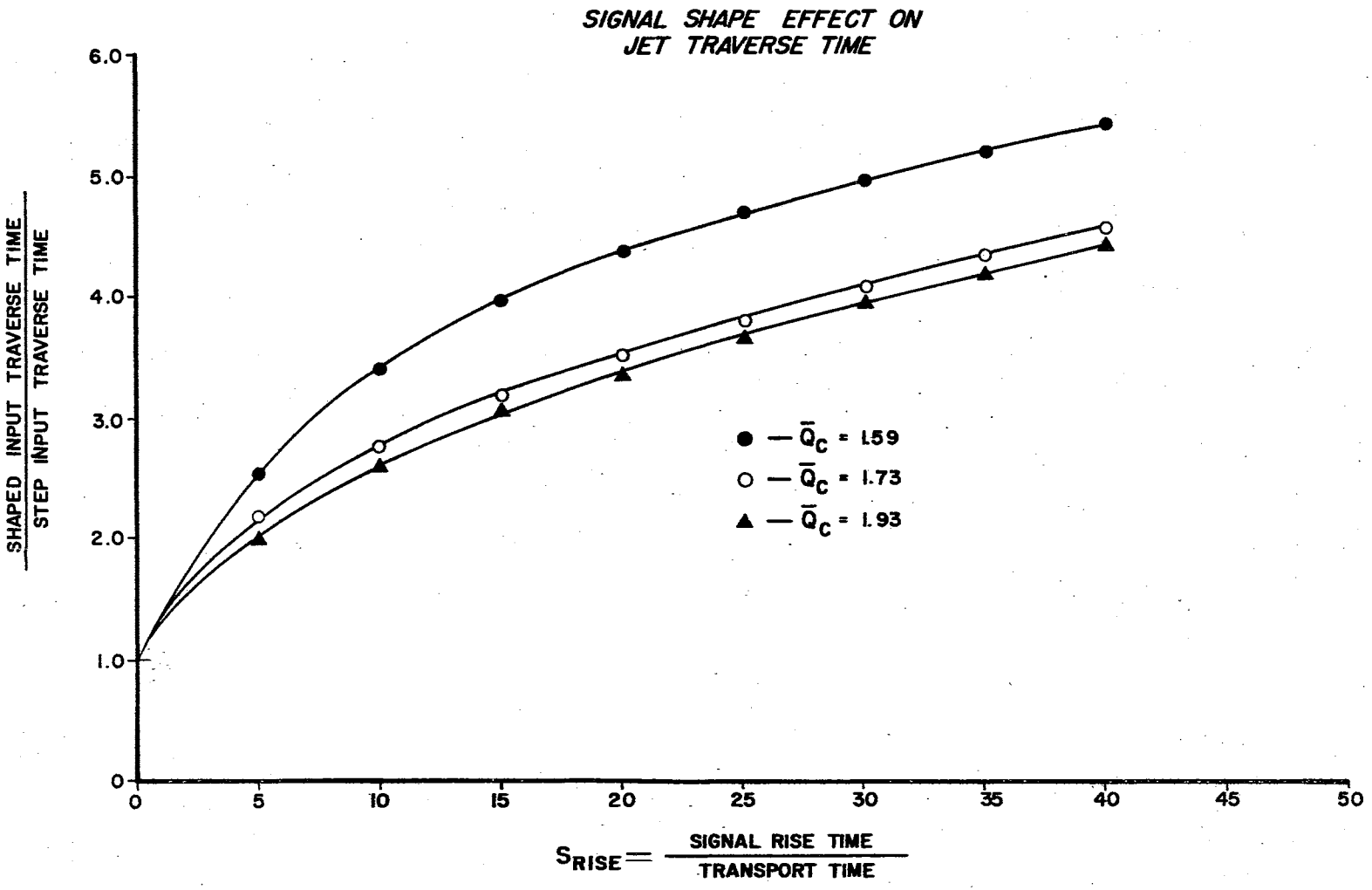


Figure 49. Effect of Non-Step Control Input on the Traverse Time of a Switching Bistable Jet

the ratio of traverse time to total switching time is given in Figure 50 as a function of the control signal rise time. This figure indicates that a sharp increase in traverse time percentage will occur as the control signal first begins to deviate from a step input. As the control signal rise time increases, the traverse time percentage again decreases and tends toward an asymptotic constant value. These results indicate that the jet traverse time will be a function of both the shape and magnitude of the input control signal to a bistable jet element.

Control Implications for Actual Bistable Fluidic Components

The analytical and experimental programs described in this chapter indicated that the switching time of a bistable fluid amplifier could be controlled over a significant range by varying the shape and magnitude of the control signal to the element. The results of this study cannot be directly extrapolated to predict the switching times of actual bistable fluidic elements since different geometries and loading conditions could affect the switching behavior of the element. However, the trends established by the study can be utilized to formulate methods and identify parameters useful in controlling the actual elements.

From an application viewpoint, perhaps the most important conclusion, which can be made concerning the results of the switching time study, is the implication that the previously defined operation and design specifications for a bistable jet element could usually be met by employing input signal adjustment to control the operating speed of the element. It is anticipated that a practical method of input signal adjustment could be achieved by varying the magnitude of a constant rise time signal to the jet element. The signal magnitude could be varied by

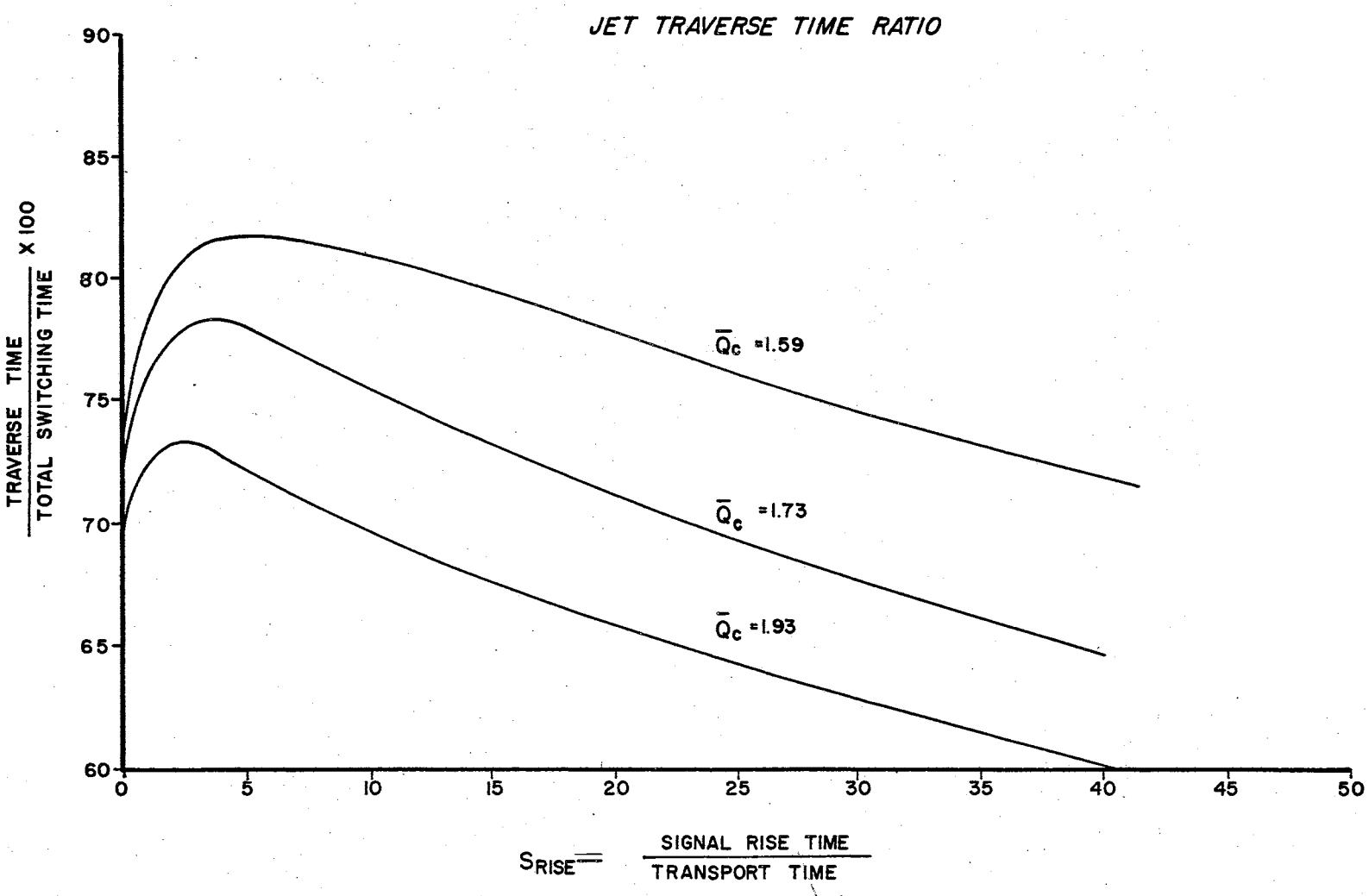


Figure 50. Ratio of Jet Traverse Time to Total Jet Switching Time

placing adjustable bleeds in the control lines leading to the bistable jet element.

The use of control signal adjustment to vary the switching time of a bistable jet element implies that:

1. The geometric configuration and power jet flow requirements of the feedback delay elements in an asynchronous sequential fluidic circuit could usually be standardized.
2. When no essential hazards were present, the maximum operational speed of the feedback elements could be made approximately as fast as that of the combinational circuit elements.
3. When necessary, the operational speed of the feedback elements could be decreased by control signal adjustment to eliminate essential hazards in the asynchronous circuit. This feature assumes that the feedback element in question will possess the range of input signal control necessary to adequately decrease the operational speed of the element.*

By necessity, the methods required to time a bistable jet element must rely on empirically determined information. If a particular geometric configuration for the bistable element can be selected, the amount of

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*Physical sizing can also be employed to adjust the switching time of the feedback element. Sizing would likely be used as a preliminary design tool to coarsely adjust the switching time of a feedback element to the point where control signal adjustment could be employed for additional timing changes. The output requirements for the combinational circuit elements driving the feedback elements would have to be determined after the feedback elements had been appropriately sized.

experimental information needed to predict the response time of the element for variable control signal inputs can be minimized by utilizing the trends observed in the above switching time study. The experimental information required to time a given bistable jet element design, operating under fixed loading conditions, would be shaped input switching time response curves similar to the response time results shown in Figure 47. The following sections define and outline a possible method for determining the timing requirements and control capabilities of a hypothetical bistable jet element design. The method could be used to design the feedback delay elements in an asynchronous sequential circuit.

Switching Time Curves

The first step in the feedback element timing procedure would be to experimentally determine shaped-input switching times for a bistable jet model geometrically similar to the actual desired element design and operating under the loading conditions expected in the actual fluidic circuit.* By referring to the experimental response curves in Figure 47, it can be concluded that the shaped input switching curves will possess the general features exhibited in Figure 51. For each control flow magnitude, the dimensionless stray delay,** S(t), associated with the switching time of the bistable element would range between a minimum and maximum value (i.e., $S_{MIN} \leq S(t) \leq S_{MAX}$) as determined by the

*It is reasonable to assume that the same loading conditions can be imposed on all feedback elements in the asynchronous circuit.

**The real time stray delay values for the feedback delay elements will be denoted by $\Delta_{MIN} \leq \Delta(t) \leq \Delta_{MAX}$.

statistical variance in the switching time data. In general, the difference between the bounds of the stray delay, $S_{MAX} - S_{MIN}$, would be expected to increase as the rise time of the control signal increased at a constant control flow magnitude. Also, the stray delay bound difference would tend to increase as the control flow magnitude decreased at a constant signal rise time.

These trends for the stray delay bounds are significiant since the magnitude of the delay bound difference will determine if a particular feedback delay element operating at a given condition can be employed in a specific asynchronous circuit. For example, consider the case of employing the element represented in Figure 51 in an asynchronous circuit feedback line. The operating control signal conditions for this hypothetical element will be defined by a rise time of S'_{RISE} and a magnitude of Q_{c_2}. These specifications can be assumed to have been derived from the requirement that a delay equal to S_{MIN_2} be placed in the feedback line to eliminate an essential hazard in the asynchronous circuit. The real time value for S_{MIN_2} could have been determined by feedback delay estimation procedures such as:

1. The Boolean equation delay estimation methods described in Chapter V.
2. Tracing the logic diagram of the combinational circuit.
3. Conducting actual experimental timing tests on the combinational circuit.

The S_{MIN_2} delay value for the feedback element switching time is essential to the safe operation of the asynchronous circuit; however, the important point is that the asynchronous circuit must now be designed to operate at an external input frequency based on the stray

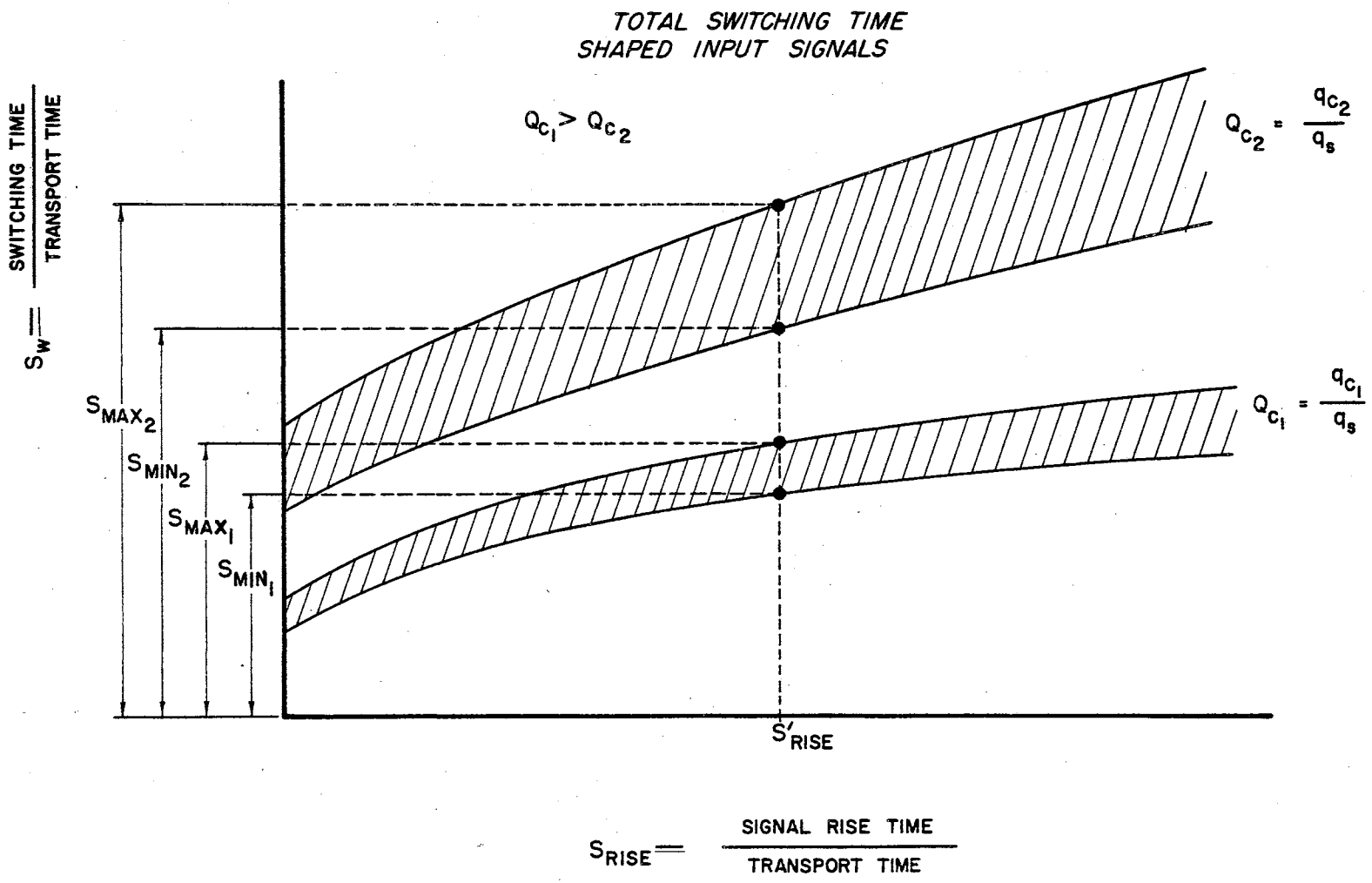

Figure 51. Typical Total Switching Time Curves Expected for a Bistable Jet Element

delay limit, S_{MAX_2}.* If the stray delay bound difference is large, the operating speed of the circuit could be reduced below that which could be tolerated by the systems being controlled with the asynchronous circuit.

Defining the bound limits for the stray delays in a switching circuit is intimately associated with the operational reliability required of the circuit. Thus, the definition of the usable control region for bistable jet element operation discussed previously in this chapter would depend on:

1. The confidence intervals which would have to be placed on the switching time data of the individual feedback element to insure a specified over-all circuit reliability.
2. The operating speed requirements of the circuit in which the element was to be employed.

A similar reliability-speed requirement argument could be used to define the upper stray delay bound of the combinational circuit elements. However, for the following discussion, it will be assumed that the bounds on the switching time curves displayed in Figure 51 represent acceptable reliability limits on the switching times for a typical feedback delay element. Thus, the problem will be to use the information contained in Figure 51 to determine the physical size and control

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*For simplicity, the bounded feedback delay was not considered in the asynchronous circuit timing analysis presented in Chapter V. For actual circuit implementation, this analysis could be modified by calculating Δ_{MIN} to satisfy the timing requirements for the feedback delay elements and employing Δ_{MAX} for calculating the allowable circuit operating frequency.

signal requirements of actual size bistable fluidic components to meet specified asynchronous circuit timing requirements. This procedure is outlined in the following section.

Design Procedure

Certain parameters characterizing the switching jet model must be identified to design an actual size feedback delay element operating at a given speed. The non-variable parameters involved in the design procedure will be defined as:

1. The experimentally determined family of nondimensional switching time curves for the particular feedback element configuration that is to be employed in the asynchronous circuit. It is assumed that the reliability requirements of the feedback delay element are employed to define the stray delay bounds of the element on the switching time curves.
2. The supply flow of the power jet as determined by the output requirements of the feedback element. This power jet flow will be designed by q_s and will have the units of:

$$\frac{\text{flow rate}}{\text{unit length}}; \text{ for example, } in^3/sec/in$$

3. The position along the attachment wall at which the jet detaches under steady-state conditions. In the switching time study described previously in this chapter, the steady-state detachment point was experimentally measured. This method would be

inconvenient for other model studies, thus a recommended estimate of the jet detachment point would be the distance from the power nozzle exit to the entrance of the output receiver section. This distance would be nondimensionalized with the power nozzle width and used as a characteristic parameter to calculate the transport time for the bistable jet device. Therefore, the steady-state detachment point will be defined as $\frac{X}{w}$, where:

X = distance from the power nozzle exit to the receiver entrance.

w = power nozzle width.

The characteristic parameters involved in the design which could be considered variable are:

1. The control flow magnitude, Q_c, where:

$$Q_c = \frac{q_c}{q_s}$$

q_c = control flow rate in units of $\frac{\text{flow rate}}{\text{unit length}}$

The maximum value of q_c available to drive the feedback delay element will be determined by the output capabilities of the combinational circuit element which drives the feedback element.

2. The rise time of the control signal, S_{RISE}. The physically realizable values of control signal rise times would be determined by the type of signal obtained from the combinational circuit driving element, the characteristics of the transmission line between

driver and driven elements and the input impedance of the feedback element.

3. The desired minimum switching time, Δ_{MIN}, for the feedback delay element. This minimum time would be determined by the timing requirements imposed on the feedback delay element to eliminate essential hazards in the asynchronous circuit or would be set at an absolute minimum to speed the circuit operation if no essential circuit hazards were present.
4. The maximum allowable switching time, Δ_{MAX}, for the feedback delay element. The time, Δ_{MAX}, could be determined from the over-all operating speed requirements of the asynchronous circuit.

The following two examples are given to illustrate the possible design uses of the above information.

Example 1

Consider the case where:

1. The power nozzle width is fixed.
2. The minimum switching time, Δ_{MIN}, has been obtained for the feedback delay element.
3. The maximum switching time, Δ_{MAX}, for the feedback delay element is fixed.

The problem is to determine the control signal characteristics necessary to produce the required switching time for the fixed size bistable jet element.

The transport time of the element can be calculated by

$$\tau = \frac{\left(\frac{X}{\omega}\right)}{\left(\frac{g_a}{\omega^2}\right)} \tag{6-18}$$

The dimensionless minimum switching time, S_{MIN}, can then be computed by:

$$S_{MIN} = \frac{\Delta_{MIN}}{\tau} \tag{6-19}$$

Similarly, the dimensionless maximum switching time value, S_{MAX}, can be computed by

$$S_{MAX} = \frac{\Delta_{MAX}}{\tau} \tag{6-20}$$

The values S_{MIN} and S_{MAX} can now be entered on the switching time curves as shown in Figure 52. When a switching time curve can be found that is bracketed by the dimensionless time values, S_{MIN} and S_{MAX}, the control signal magnitude and rise time values can be obtained as illustrated in Figure 52. These conditions would define the control signal characteristics required to switch the fixed design feedback element at a speed sufficient to meet the specified timing requirements of the asynchronous circuit. It can be noted that the rise time of a control signal with magnitude Q_{C_1} can vary between the values S_{RISE_1} and S_{RISE_2} and yet satisfy the circuit timing requirements.

Example 2

Consider the case where:

1. The control signal rise time is fixed at a constant value of S'_{RISE}.

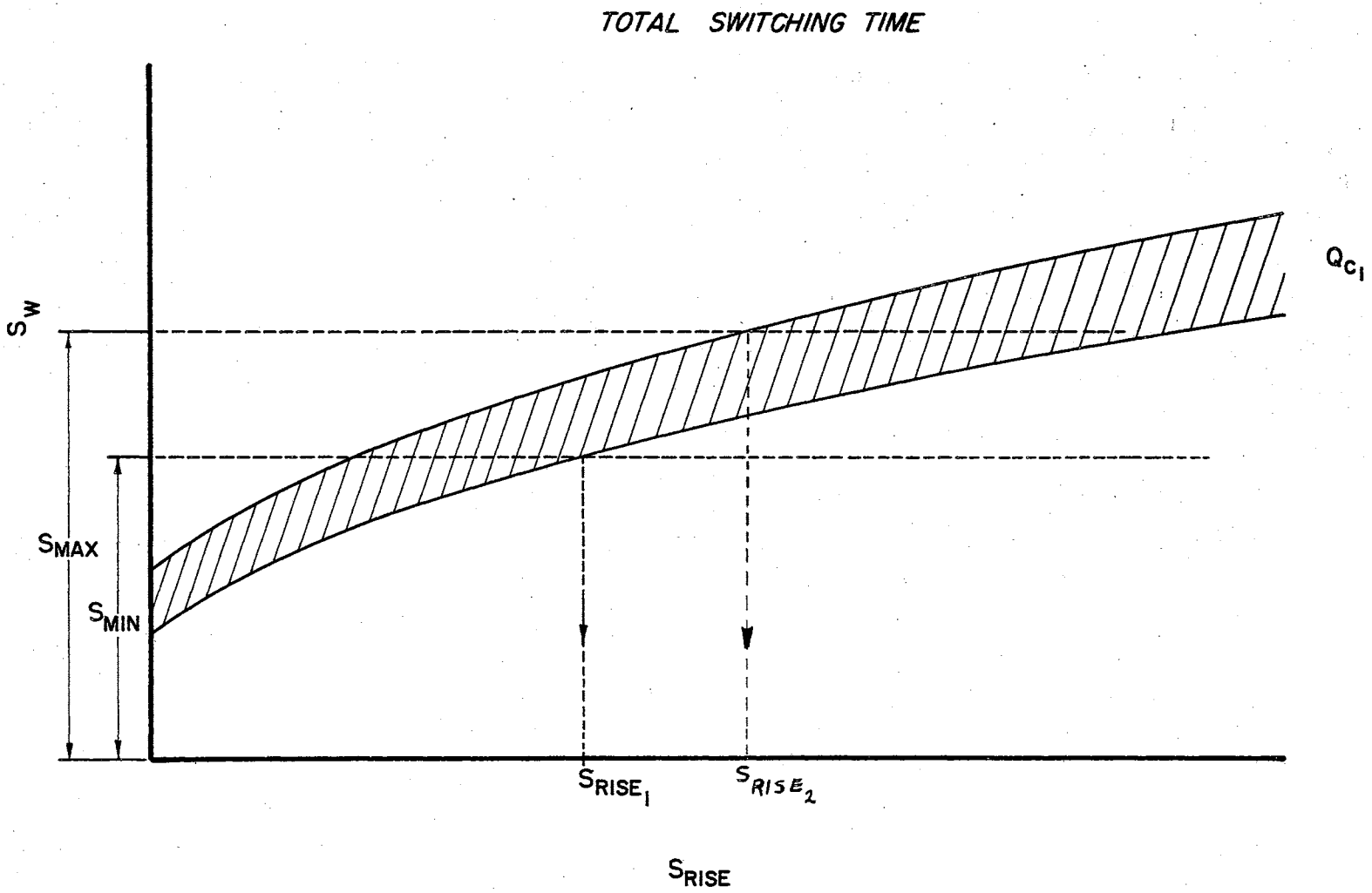

Figure 52. Total Switching Time Curve for Example 1

2. A value for the control signal magnitude is set at a constant value of q_c'.

3. The minimum switching time, Δ_{MIN}, is fixed.

The problem is to size the bistable jet element to meet the specified minimum switching time requirements.*

The control flow ratio can be calculated as

$$Q_c' = \frac{q_c'}{q_a} \tag{6-21}$$

The point on the switching time curves defined by Q_c' and S'_{RISE} can be determined as shown in Figure 53. The value of S'_{MIN} can be read from the S_w scale of the figure. Then, the transport time of the device can be calculated by:

$$\tau = \frac{\Delta_{MIN}}{S'_{MIN}} \tag{6-22}$$

The power nozzle width can be calculated by combining Equations (6-18) and (6-22) as:

$$w = \sqrt{\frac{\Delta_{MIN}(q_a)}{S'_{MIN}\left(\frac{x}{w}\right)}} \tag{6-23}$$

The maximum switching time, Δ_{MAX}, for this element size can be determined from the switching time curves as:

$$\Delta_{MAX} = \frac{S'_{MAX}}{S'_{MIN}} \Delta_{MIN} \tag{6-24}$$

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*It is tacitly assumed in this example that the experimental switching time curves are insensitive to changes in the aspect ratio of the bistable jet element. Otherwise, experimental switching time data would have to be available for different aspect ratios and the sizing problem becomes one of trial and error.

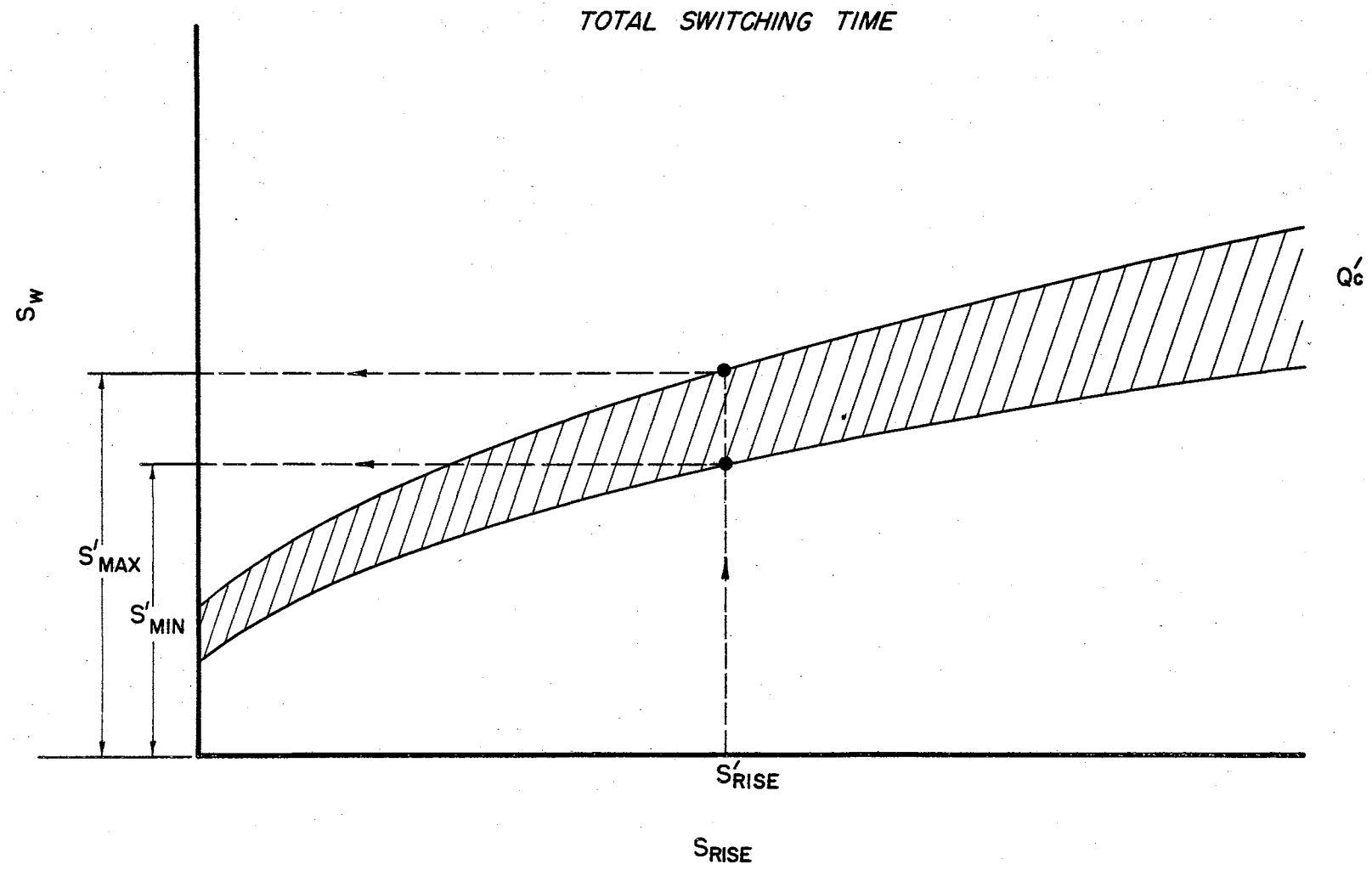

Figure 53. Total Switching Time Curve for Example 2

The value of Δ_{MAX} as obtained from Equation (6-24) could be used to establish the operating frequency limits on the asynchronous circuit which had the bistable jet element defined by Equation (6-23) in a feedback loop.

These two examples should provide the reader with an insight into the possibilities of employing the switching time curves to determine the various operating parameters required to properly time the feedback delay elements in an asynchronous circuit. It should be realized that physical limitations placed on the involved design parameters will make certain timing requirements impossible to achieve for certain operating conditions and specified switching time curves. Design compromises will then become necessary. The information obtained from the switching time curves can readily serve as a guide for determining an appropriate compromise design.

The above examples suggest that experimental switching time curves of the same general form as those displayed in Figure 47, represent the type of dynamic response data needed to incorporate a bistable fluid amplifier component into an asynchronous circuit. General catalog information displaying this type of dynamic response data for acceptable ranges of aspect ratio would enhance the use of a given element configuration in designing fluidic control circuits.

Summary

To insure the safe operation of an asynchronous circuit, certain specifications must be defined for the operating time of the logic components used to implement the circuit. The response time specifications for the combinational circuit elements required that the stray delay

associated with the switching time of the element be bounded such that the element delay time can be expressed as $0 \leq \Delta(t) \leq \Delta_{MAX}$. This specification means that the response times of a combinational circuit element are not critical with respect to the operational correctness of an asynchronous circuit if the element responds within the time defined by the upper bound of the stray delay limit.

The switching time specifications for the feedback delay element of an asynchronous circuit are determined by the transitional properties of the asynchronous circuit. If essential hazards are present in the circuit transition map, then the feedback delay elements must be restricted to operate with a stray delay value defined by $\Delta_{MIN} \leq \Delta(t) \leq \Delta_{MAX}$. The minimum delay bound, Δ_{MIN}, is determined by the amount of delay needed to assure safe operation of the circuit. This Δ_{MIN} delay value depends on the upper stray delay bound of the combinational circuit elements. When essential hazards are not present in the asynchronous circuit, the response time of the feedback delay element would be set at an absolute minimum value to speed the circuit operation. The upper stray delay bound, Δ_{MAX}, for the feedback delay element is determined by the operational reliability required of the feedback delay element. This feedback component reliability would be determined from the specified over-all asynchronous circuit reliability. The upper delay bound, Δ_{MAX}, influences the allowable circuit operating frequency.

This chapter has considered the design of set-reset fluidic flip-flops to meet the timing conditions specified by the operating requirements of an asynchronous circuit. The characterizing parameters involved in the fluidic flip-flop design and operation were investigated to determine a convenient method of response time control for the

bistable jet flip-flop element. Review of previous related work indicated that the switching time of a bistable jet element could be adjusted by varying the magnitude of a step-input control signal to the element. However, these previous studies did not consider the control effects of shaping the input signal to the bistable jet element.

To initially investigate the possibilities of employing shaped input signals to control the switching time of a bistable jet element, an analytical model was formulated to mathematically predict the jet detachment time component of the total bistable jet switching time for exponentially shaped input control signals. The offset-inclined wall geometry incorporated in the analytical jet detachment time model was typical of the geometry employed in actual bistable jet element designs. The calculated results from the analytical model indicated that the jet detachment time could be varied over a suitable control range by adjusting both the shape and magnitude of the control signal to the model.

An experimental program was conducted to determine if the control signal trends predicted by the analytical jet detachment time model would hold for the total switching time of the bistable jet device. The experimental program consisted of measuring the total switching time of a bistable jet in response to shaped, variable magnitude control signals. The results of the experimental program verified that the total switching time of a bistable jet could be expected to follow the same general response time trend as that predicted analytically for the jet detachment time.

Additional experimental jet detachment times were employed to show that the predicted analytical jet detachment time could be used to estimate the actual jet detachment time for step input control signals. By

making the assumption that the analytical model would provide suitable jet detachment time estimates for shaped input signals, the traverse time component of the total jet switching time was determined by subtracting the calculated jet detachment time from the experimental total switching time. The results of this operation indicated that the traverse time of the jet would be a function of both the magnitude and shape of the control signal to the jet.

The control signal trends observed in the bistable jet switching time study were employed to formulate a method for appropriately timing the feedback delay elements in an asynchronous circuit. This timing method requires the experimental determination of shaped-input switching times for a bistable jet model similar in geometry and loading conditions to the actual feedback element design. Information defining the timing and reliability requirements of the asynchronous circuit feedback delay components was combined with the experimental switching time data to calculate the design specifications for the feedback delay elements. Physical sizing of the feedback delay elements and adjustments of magnitude and shape of the control signals to the elements were employed to satisfy the operational timing requirements of the bistable jet devices.

CHAPTER VII

CONCLUSIONS AND RECOMMENDATIONS

The general purpose of this dissertation has been to define methods and requirements for designing safe operating asynchronous sequential fluidic circuits while retaining the fast operating capabilities of the asynchronous circuit. By necessity, the logic structure and transitional behavior of the asynchronous circuit must be considered, together with the physical operating properties of the logic components used to implement the circuit, to achieve both operational reliability and maximum speed for a particular asynchronous circuit design.

The basic problem encountered in the design of a safe operating asynchronous circuit occurs when the designer employs binary-valued Boolean equations, with the assumption that the involved binary variables have perfect instantaneous switching properties, to represent a physical circuit implemented with logic components which possess imperfect stray delay switching characteristics. This inconsistency produces hazards in the operation of the physical circuit which must be removed to insure safe circuit operation. The previous chapters of this work have reviewed methods of hazard elimination which will assure the safe operation of an asynchronous circuit.

The allowable operating speed of the asynchronous circuit is intimately associated with the hazard elimination problem. In general, increasing the operational reliability of an asynchronous circuit will

tend to slow the allowable operating speed of the circuit. The reliability specifications must necessarily be achieved; therefore, to maintain a maximum circuit operating speed, the designer must employ circuit speeding techniques in both the logic equation synthesis procedure and the physical implementation of the circuit. Specific circuit speeding techniques have been emphasized throughout this dissertation.

The most critical problem encountered in the internal design of an asynchronous circuit is controlling the response of the feedback delay elements of the circuit such that an erroneous stable state will not be reached when essential hazards are present in the circuit transition map. The bistable jet flip-flop device was arbitrarily selected as a convenient feedback delay element to employ in the implementation of an asynchronous fluidic circuit. The logic function performed by the bistable jet element is that of a set-reset flip-flop. The assumption was also made that AND-OR components would be used to implement the combinational portion of the asynchronous circuit. Employing these assumptions and the Boolean equations representing the circuit, a method was developed to estimate the delay required in the feedback lines of the circuit to prevent erroneous circuit action. This delay estimate was used to approximate a maximum allowable operating frequency for the total asynchronous circuit.

The operating parameters which could be employed to control the response of a bistable jet flip-flop element were then studied in a combined analytical-experimental program. The results of this study indicated that the operational timing of the bistable jet device could be controlled by sizing the device and varying the shape and magnitude of the control signal to the element. Based on the trends observed in

this study, it can be concluded that the bistable jet element could be suitably timed to satisfy the timing requirements of a feedback delay element in an asynchronous sequential fluidic circuit.

In the opinion of the author, the major over-all contribution of this dissertation is the introduction of the bounded stray delay concept into the description of the operating characteristics of fluidic logic components. Although this concept has been formerly utilized to design electronic circuits, the unifying effects derived from employing the bounded stray delay concept to synthesize and implement asynchronous circuitry have never, to the author's knowledge, been used in the design of fluid logic circuits. From the bounded stray delay concept, sufficient information can be obtained to define the response specifications for the components employed to implement a safe operating asynchronous circuit. In addition, the frequency at which the circuit will operate can be estimated.

The following specific individual topics included in this dissertation work should contribute to the knowledge required to design complex asynchronous fluidic circuits for automating fluid power circuits.

1. The procedures for estimating the feedback element delay and operating frequency of an asynchronous circuit from the Boolean algebra equations which represent the circuit. It is anticipated that these procedures will prove valuable for obtaining preliminary design specifications for the timing requirements of large complex asynchronous circuits.
2. The formulation and solution of a mathematical model for predicting the detachment time component of the total

switching time of a bistable jet in response to non-step control flow inputs. Experimental verification of the numerical solution for the model was obtained for step input control signals.

3. Experimental data which showed the trends that could be expected for the total switching time of a bistable jet element when non-step control signals were used to change the state of the element.
4. Proposed design procedures for timing the bistable jet feedback delay elements in an asynchronous fluidic circuit by employing experimentally determined switching time curves.

As a result of the work reported in this dissertation and other related fluid logic studies, it is recommended that further investigations be conducted in the following areas:

1. The continued development of mechanized techniques for synthesizing asynchronous circuits should be pursued with the objective of extending and improving the present techniques used for this purpose.
2. Work should be initiated on the development of mechanized methods for detecting hazards in asynchronous circuitry which could be programmed on the digital computer. These hazard detection methods should possess the ability of detecting a potential hazard and assessing whether the elimination of the hazard was essential to the safe operation of the circuit.
3. A continued effort should be made to extend the

concepts presented in Chapter V to develop accurate automated techniques for determining the required delays in the feedback loops of an asynchronous circuit.

4. Study should continue on determining the predominate factors which control the switching time of a bistable jet element with the purpose of establishing quantitative design data to use in guiding the selection of a basic geometric configuration for the bistable jet device. Such studies would hopefully result in a feedback delay element design which would possess a wide range of response time control with a minimum stray delay bound difference.
5. Standardized test procedures should be established for determining the transient switching time curves of a bistable jet model operating under realistic environmental conditions.

It is believed that the continued development of these methods and procedures combined with the work reported in this dissertation will result in automating the design of asynchronous sequential fluidic circuits from the initial statement of the logic requirements for the circuit to the final fluidic circuit design.

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APPENDIX A

BOOLEAN FUNCTION REPRESENTATION AND DEFINITIONS

Boolean functions expressed in the form of Boolean equations are employed to represent the outputs of switching circuits. A Boolean function is a binary valued function whose value depends on the value of the binary valued variables which compose the function. A Boolean function of n binary-valued variables X_1, X_2, ..., X_i, ..., X_n can be represented by $F(X_1, X_2, \ldots, X_i, \ldots X_n)$. The variables $X_1, X_2, \ldots, X_i, \ldots X_n$ can possess the values $e_1, e_2, \ldots, e_i, \ldots, e_n$ where $e_i = 0$ or 1 for $1 \leq i \leq n$. Therefore, the function $F(X_1, X_2, \ldots, X_n)$ can be defined as either 0 or 1 or can be undefined for $F(e_1, e_2, \ldots, e_i, \ldots, e_n)$. The undefined condition leads to what are commonly called "don't care" states.

The function $F(X_1, X_2, \ldots, X_i, \ldots, X_n)$ is expressed in Boolean equation form. The Boolean equation is formed as logic sums of logic products of binary valued variables or as logic products of logic sums of binary variables. The sum of products form of equation is referred to as <u>disjunctive</u> form and the products are called <u>conjunctions</u>. The product of sums form of equation is designated as <u>conjunctive</u> form and the sums are called <u>disjunctions</u>. The sum of products form is more commonly employed in logic circuit synthesis and will be employed in the following discussion.

The occurrence of a variable, either complemented or uncomplemented, in an equation term is denoted as a <u>literal</u>. A product of

literals form P-terms of a Boolean equation. For example, the equation $F(X_1, X_2, X_3) = X_1 X_2 + \overline{X}_2\overline{X}_3 + \overline{X}_1\overline{X}_2$ represents a Boolean function of three variables. The equation is in sum of product (disjunctive) form, contains six literals and three P-terms. The value of this example Boolean function can be defined as 1 according to the truth table shown in Figure 54. Boolean functions are said to be <u>equivalent</u> when they are both equal to 1 or 0 for the same variable combinations. For instance, the function $G(X_1,X_2,X_3) = X_1X_2X_3 + \overline{X}_2\overline{X}_3 + \overline{X}_1\overline{X}_2 + X_1X_2\overline{X}_3$ is equivalent to $F(X_1,X_2,X_3)$ in Figure 54 since $G(X_1,X_2,X_3)$ will equal 1 for the same combinations of the X_1,X_2,X_3 variables which produce a 1 value for F.

X_1	X_2	X_3	X_1X_2	$\overline{X}_2\overline{X}_3$	$\overline{X}_1\overline{X}_2$	$F[X_1, X_2, X_3]$
0	0	0	0	1	1	1
0	0	1	0	0	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	0	1

Figure 54. Truth Table of Boolean Function

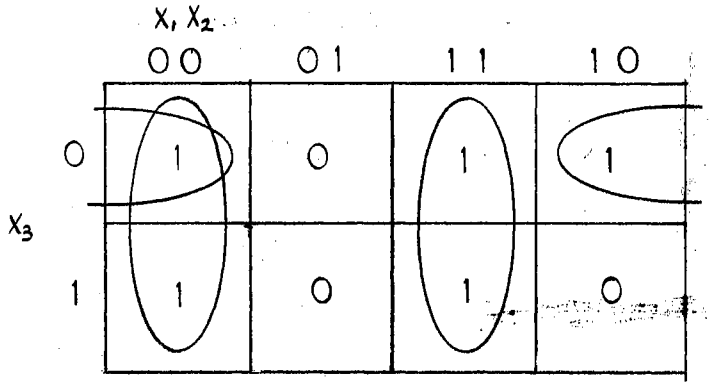
The P-terms in the above example function $F(X_1,X_2,X_3)$ are unique in

that they are prime implicants of the function. In general, a prime implicant P-term of a function is a product of literals such that the number of literals contained in the term cannot be further reduced by simplification techniques. The sum of all the prime implicants of a function is referred to as the complete sum of the function. A sum of products which contains only prime implicants of which no term can be removed is called an irredundant sum. The prime implicants in an irredundant sum are essential prime implicants.

The outputs of a logic circuit can be defined by Boolean functions in which the variables of the function represent the inputs to the circuit. The outputs of an asynchronous sequential circuit are identified by assigning appropriate 0, 1, or "don't care" values as determined from the problem specification to each of the unique total states defined by the state variable and external input combination; i.e., the $(q_i \times X_j)$ states described in Chapter II. The Boolean functions generated to represent the circuit outputs are then reduced by simplification techniques to prime implicant form. The usual practice is to choose as few of the prime implicants as possible to represent the output function, since the amount of hardware required to implement the circuit is usually proportional to the complexity of the representative Boolean equation. The minimal sum of prime implicants cannot always be employed to represent a function since reduction to minimal sum form can introduce operational hazards in the resulting circuitry.

The Boolean function can be represented graphically by the Karnaugh map as shown in Figure 55. The individual cells of the Karnaugh map represent the fundamental products in P-term form of potential Boolean functions which can be represented on the map. The use of the Karnaugh

map for simplifying Boolean functions is well known and the interested reader is referred to references (17), (3), and (19) for more complete details.



$$F(x_1, x_2, x_3) = \bar{x}_1 \bar{x}_2 + x_1 x_2 + \bar{x}_2 \bar{x}_3$$

Figure 55. Karnaugh Map Example

APPENDIX B

BASE CONVERSION PROCEDURE AND ARITHMETIC OPERATIONS FOR BASE n NUMBERS

The logic stage minimization technique described in Chapter IV required that base 10 numbers be converted to base n and that the base n arithmetic operations of addition and multiplication be used. These operations are described in the following sections.

Conversion From Base 10 to Base n Numbers

A generalized procedure for converting base r_1 numbers to base r_2 numbers is given by Scott (28). For base 10 conversion to base n numbers, the procedure is as follows:

Suppose a number N_o is expressed in base 10 and a conversion of N_o to base n is desired. The number N_o can be expressed as

$$N_o = A_k(n)^k + A_{k-1}(n)^{k-1} + \cdots + A_1(n) + A_o .$$

The conversion procedure must then give the coefficients, A_j. The N_o polynomial in n can be rewritten in the form

$$N_o = \left(\left[(A_k n + A_{k-1})n + A_{k-2}\right]n + \cdots\right)n + A_o$$

or $N_o = N_1 n + A_o$

where: $N_1 = N_2 n + A_1$, a polynomial one degree lower than N_o. The A_j

coefficient can be found as the remainder of repeated divisions of the N_j by n.

For example, consider converting the base 10 number, 956, to a base 4 number.

Remainder

$$
\begin{array}{rl}
4 \,|\, 956 & \\
4 \,|\, 239 & -\ 0 = A_0 \\
4 \,|\, 59 & -\ 3 = A_1 \\
4 \,|\, 14 & -\ 3 = A_2 \\
4 \,|\, 3 & -\ 2 = A_3 \\
0 & -\ 3 = A_4
\end{array}
$$

The equivalent base 4 number would be

$$N_o = 3(4)^4 + 2(4)^3 + 3(4)^2 + 3(4)^1 + 0(4)^0$$

or

$$32330.$$

Base n Arithmetic

The following addition and multiplication tables can be used to perform the base n arithmetic required in Chapter IV.

Base 2

1. Multiplication

X	0	1
0	0	0
1	0	1

2. Addition

+	0	1
0	0	1
1	1	10

Base 3

1. Multiplication

X	0	1	2
0	0	0	0
1	0	1	2
2	0	2	11

2. Addition

+	0	1	2
0	0	1	2
1	1	2	10
2	2	10	11

Base 4

1. Multiplication

X	0	1	2	3
0	0	1	2	3
1	1	2	3	10
2	2	3	10	11
3	3	10	11	12

2. Addition

+	0	1	2	3
0	0	1	2	3
1	1	2	3	10
2	2	3	10	11
3	3	10	11	12

APPENDIX C

ASYNCHRONOUS CIRCUIT HAZARDS

The use of binary valued Boolean functions to represent a physical switching circuit assumes that perfect instantaneous state changes will occur for the logic elements used to implement the switching circuit. This assumption implies that these logic elements have no switching delay time and that the outputs of these elements be either in a 0 or 1 state with no intermediate values. The physical properties of all actual switching elements violate the above two conditions, thus an actual physical switching circuit output can be different than predicted by the Boolean equation used to represent the circuit.

The deviations of the actual circuit output from the theoretically predicted output can create operational hazards in an asynchronous circuit which could destroy the intended sequential action of the circuit or produce momentary spurious external outputs. To insure safe operation of an asynchronous circuit, the designer must be aware of the various kinds of hazards which can occur and have methods of eliminating the hazards when circuit operation is affected. The known types of operational hazards which can be present in an asynchronous circuit can be classified as:

1. Critical Races.
2. Function Hazards.
3. Essential Hazards.

4. Transient Hazards

   a. Static

   b. Dynamic.

All of these hazards can be defined by considering the bounded stray delay properties of the logic elements used to implement a switching circuit. Each logic element in the circuit will require time interval $\Delta(t)$ to change state after an input signal is received by the element. This $\Delta(t)$ time interval can be assumed to possess values such that $0 \leq \Delta(t) \leq \Delta_{MAX}$, where Δ_{MAX} is the upper bound on the element delay. The element delay can be different for the various signals which change the element state, thus the delay time can stray in value from approximately 0 to the upper bound Δ_{MAX}. Each of the asynchronous circuit hazards will be discussed in the following sections by considering that bounded stray delay logic elements are used to implement the circuit.

Critical Race

A critical race occurs in an asynchronous circuit when two or more state variable feedback elements are changing and the order of the changes can determine the final stable state of the circuit. Since the delay of each of the state variable elements can stray*, it is usually impractical to rely on precise timing of the state variable elements to produce correct circuit action. The critical race hazard can be

---

*As shown later in the description of essential hazards, there are circumstances where the state variable element response time must be delayed in a controlled manner. This delay would still be of a stray nature for which a lower and upper bound could be defined; i.e., $\Delta_{MIN} \leq \Delta(t) \leq \Delta_{MAX}$. The timing of this delay would not require the preciseness of that which could be needed to avoid critical races.

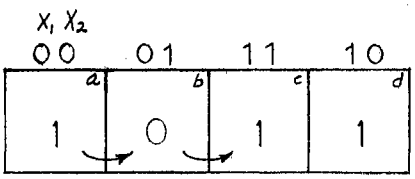
eliminated in the state variable assignment stage of the circuit synthesis by allowing only one state variable element to change per circuit transition. The critical race and appropriate state variable methods for eliminating the critical race are discussed in detail in Chapter III.

Function Hazard

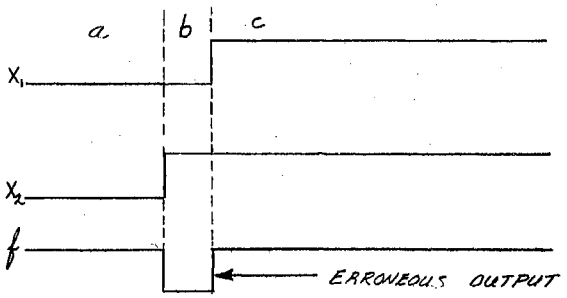
The function hazard is an inherent hazard in the Boolean function employed to represent a logic circuit and cannot be eliminated by adding more hardware to the logic circuit (4). The function hazard occurs when two or more inputs to the combinational portion of the asynchronous circuit are changed simultaneously. An example of a function hazard is illustrated in Figure 56.

If the state of the circuit represented by the flow table in Figure 56 is initially in cell "a" of the table, the circuit output f would be 1. When an input transition is specified from X_1X_2 = 00 to X_1X_2 = 11, a momentary erroneous output of f = 0 will occur if the stray delay associated with signal X_1 is greater than the X_2 delay. As shown in Figure 56, the circuit action will momentarily exist in cell b which has a specified output of f = 0. This momentary output change was not intended for the circuit output and constitutes a function hazard. The occurrence of a function hazard is dependent on the stray delay values which exist in the combinational circuit for output f. The possibility of the occurrence of the function hazard cannot be eliminated by adding additional logic hardware to the switching circuit. Since it is infeasible to attempt control of the stray delay values in the combinational circuit, the external inputs to an asynchronous circuit must be

restricted to only change one at a time. This stipulation limits external input changes to adjacent changes and eliminates the possibility of a function hazard occurring in the operation of the circuit.



(a) Flow Table for Boolean Function f



(b) Timing Chart

Figure 56. Illustration of a Function Hazard

Essential Hazard

The basic operation of an asynchronous circuit involves a change in external input to the circuit which creates an excitation signal for changing a state variable element and also causes other disturbances in the combinational circuit. The state variable signal created by the

excitation signal is directed back into the combinational circuit portion of the asynchronous circuit. If the delay time of the state variable element is insufficient to allow the combinational circuit to settle from the external input signal disturbance before the state variable signal enters the combinational circuit, a race can occur between the external input and the state variable signals in traversing the combinational circuit. When the results of this race affect the terminal behavior of the circuit, the asynchronous circuit is said to contain an essential hazard. Unger (30) has defined sufficient conditions for detecting the possibility of an essential hazard in an asynchronous circuit by examining the transitory behavior of the flow table for the circuit. These conditions can be summarized by the following definition (15):

> "A total state q_j and an input X_i represent an <u>essential hazard</u> for a flow table, if and only if, when the table is in state q_j, the state reached after one change of X_i is different from the state reached after three successive changes of X_i."

When an essential hazard exists in a circuit, the delay of the state variable element involved in the hazard must be of sufficient magnitude to allow the external input signal to always win the race through the combinational circuit. The following example will illustrate the effects of the essential hazard.

Consider the flow table with state variable assignment shown in Figure 57. This flow table contains an essential hazard since when the circuit is initially in state q_1 and signal X is changed three times, the table will be in state q_4 instead of state q_2. A physical circuit which produces the circuit action given by the flow table in Figure 57 is shown in Figure 58. If this circuit is assumed to be in state q_1,

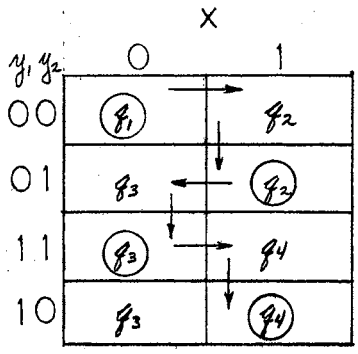


Figure 57. Flow Table With Essential Hazard

(i.e., X $y_1 y_2$ = 000) the effects of the essential hazard in the circuit can be seen by observing possible circuit action upon the change of external input X. When X is changed from 0 to 1, AND gate No. 2 will be activated creating set signal S_2 which changes the state of flip-flop No. 2. The y_2 signal from flip-flop No. 2 could activate AND gate No. 1 if the stray delay for the inversion of signal X was greater than the actuation time of signal y_2. Actuation of AND gate No. 1 would produce set signal S_1 which would, in turn, change the state of flip-flop No. 1 and produce signal y_1. Signals y_1 and X would then produce reset signal R_2 and change the state of flip-flop No. 2 again, thus leaving the circuit in state q_4 instead of q_2 as intended by the flow table specifications. The essential hazard in this circuit must be eliminated by delaying the first change of flip-flop No. 2. The amount which the flip-flop must be delayed is determined by the settling time of the combinational circuit disturbances created by the change in external input.

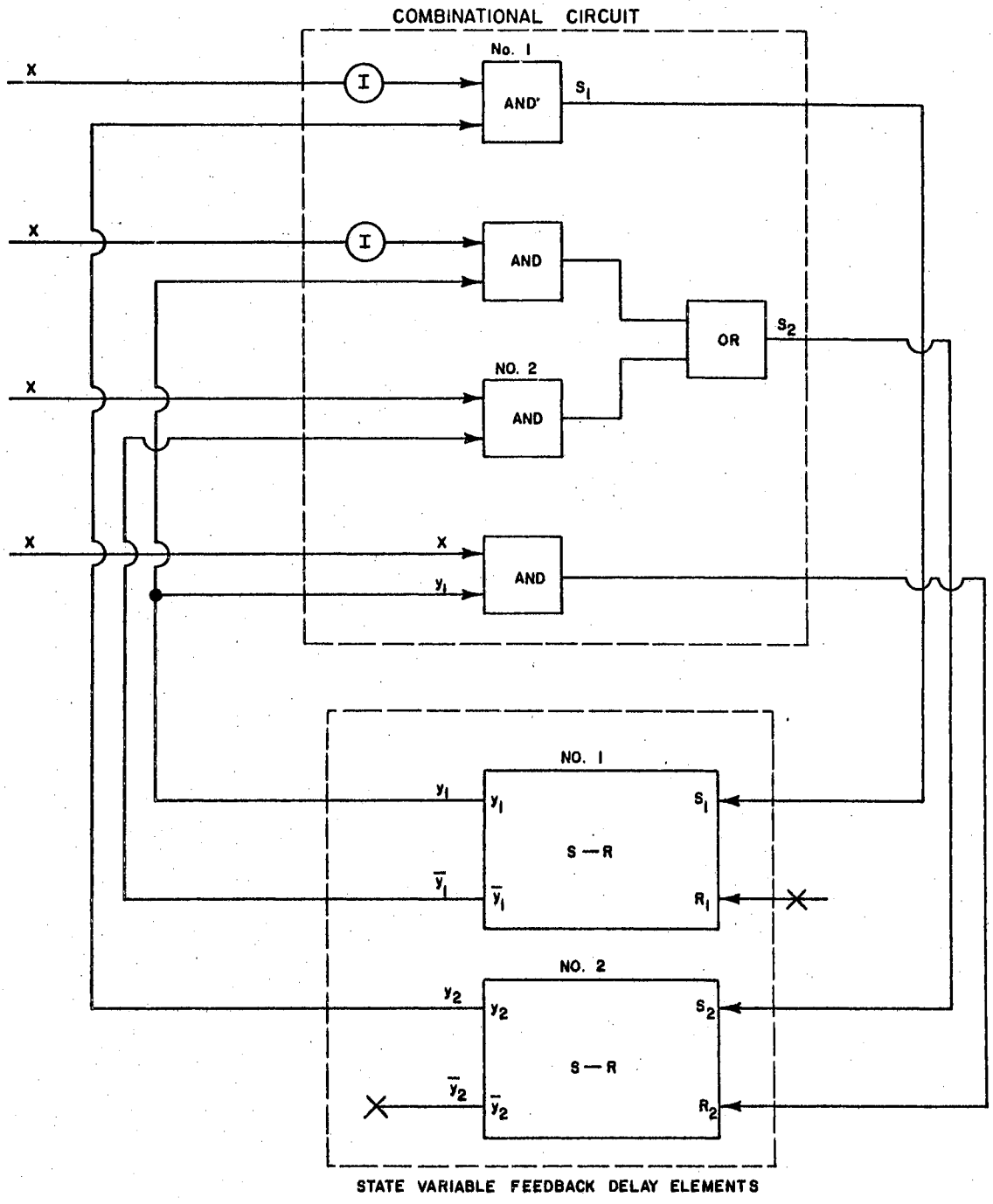


Figure 58. Asynchronous Circuit With Essential Hazard

Although the timing effects of the feedback delays on the external outputs of the asynchronous circuit are not discussed in currently available literature, momentary spurous external outputs could also be produced by races between the state variable signals and the external inputs. The results of these erroneous external outputs would not produce incorrect transitory behavior such as those created by essential hazards, but the erroneous external outputs which did result could be objectionable and unwanted. To assure that the intended circuit outputs occur, a feedback delay timing scheme such as that outlined in Chapter V can be employed. This type of feedback timing will always produce a correct operating circuit if all other operational hazards have been eliminated from the circuit.

Transient Hazards

The stray delays which exist in the combinational circuit portion of an asynchronous circuit can create temporary erroneous combinational circuit outputs during the time that is required for the circuit to settle from disturbances caused by a change in the external circuit inputs. Since these erroneous outputs are of a temporary nature, they are referred to as transient hazards in the combinational circuit. Transient hazards can be of two general types: (1) static hazards, and (2) dynamic hazards. To define these transient hazards, consider the restrictions under which the combinational circuit is required to operate in the asynchronous circuit. First, the requirement that function hazards must be avoided requires that only one external input to the combinational circuit be allowed to change at a time. Second, the time between input changes must be controlled to allow the combinational

circuitry time to settle from a previous input disturbance before another input change is allowed.

The Boolean function, $f(X_1, X_2, \ldots, X_n)$ will be employed to represent the combinational circuit output. The n inputs to the circuits are $X_1, X_2, \ldots, X_n$. The n-tuple $(e_1, e_2, \ldots, e_n)$ will be employed to represent the binary values of the input variables. If only adjacent input changes are allowed to the combinational circuit, transient hazards can be defined as follows (20):

1. Assume that the combinational circuit output function $f(X_1, X_2, X_3, \ldots, X_n)$ is stable for the input combination $(e_1, e_2, \ldots, e_n)$. Let input combination $(e_1', e_2', \ldots, e_n')$ be adjacent to $(e_1, e_2, \ldots, e_n)$ and $f(e_1, e_2, \ldots, e_n) = f(e_1', e_2', \ldots, e_n')$. If, when the input $(e_1', e_2', \ldots, e_n')$ is received by the circuit, it is possible for the circuit output to assume a value not equal to $f(e_1, e_2, \ldots, e_n)$ during the circuit transition, the input transition from $(e_1, e_2, \ldots, e_n)$ to $(e_1', e_2', \ldots, e_n')$ is termed a <u>static hazard</u> for the combinational circuit. When a static hazard is present in a circuit, the circuit output values could vary from $1, \ldots, 0, \ldots, 1$ for a stable output of 1 or from $0, \ldots, 1, \ldots, 0$ for a stable output of 0.
2. Let the combinational circuit output function $f(X_1, X_2, \ldots, X_n)$ be stable for input combination $(e_1, e_2, \ldots, e_n)$ and an adjacent input combination $(e_1', e_2', \ldots, e_n')$ be applied to the circuit when $f(e_1, e_2, \ldots, e_n) \neq f(e_1', e_2', \ldots, e_n')$. If a sequence of output values

$f(e_1,e_2,\ldots,e_n),\ldots,f(e_1',e_2',\ldots,e_n'),\ldots,f(e_1,e_2,\ldots,e_n),$ $\ldots,f(e_1',e_2',\ldots,e_n')$ can occur during the circuit transition, the input transition from $(e_1,e_2,\ldots,e_n)$ to $(e_1',e_2',\ldots,e_n')$ is termed a dynamic hazard for the combinational circuit. The sequence of output values for a dynamic hazard could be $1,\ldots,0,1,\ldots,0$ or $0,\ldots,1,0,\ldots,1$.

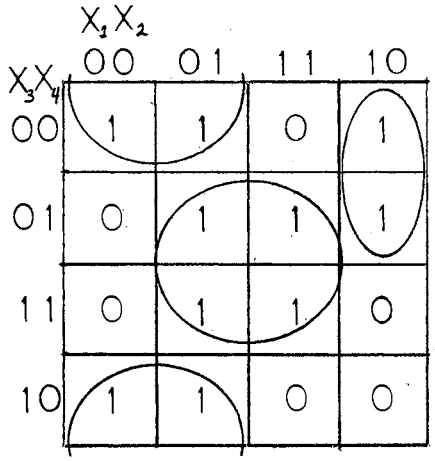
When designing combinational circuits for use in safe operating circuits, it is necessary to eliminate both the static and dynamic hazards in the combinational circuit. A combinational circuit which contains no transient hazards is said to be hazard free.

It has been shown by Eichelberger (4) that when all prime implicant terms of a sum of products Boolean function are retained in the Boolean equation utilized to represent the combinational circuit, the resulting circuit will be transient hazard free. For economic reasons, it is impractical to use this complete sum of the Boolean function to represent the circuit. Thus, the transient hazard elimination problem becomes one of selecting the minimum number of prime implicants of the Boolean function which will yield a hazard free circuit representation. When a sum of products form of Boolean equations is used to represent the 1 states of the combinational circuit, McCluskey (15) has shown that to achieve a hazard free circuit equation, a sufficient number of prime implicants of the Boolean function must be chosen such that each pair of adjacent input states which both produce 1 outputs is included in a single prime implicant term. This requirement produces AND gates in the AND-OR circuit implementation which "hold" the circuit output constant during input transitions and, thus, eliminates the occurrence of transient

hazards in circuit outputs.

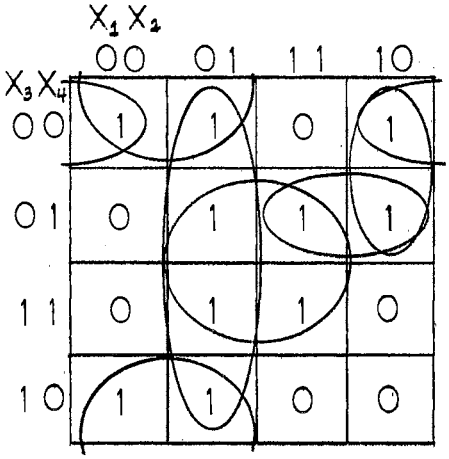
When a Karnaugh map is employed to derive the Boolean equation for designing the combinational circuit, the necessary prime implicants required to produce a hazard free circuit can be readily determined by linking all adjacent inputs with prime implicant terms. This procedure is illustrated in Figure 59. As circuits get larger and involve more inputs, the Karnaugh map method becomes inconvenient to use. Tabular methods of generating the prime implicants for a Boolean function, which are computer programmable, are discussed by Marcus (17) and McCluskey (15). After the prime implicants of a function are available, the problem then becomes one of selecting enough prime implicants to include all adjacent input transitions which could produce a transient hazard. A method for determining these necessary prime implicants is presented by McCluskey (15) and will be reviewed in the following example problem.

Suppose the Boolean function which represents a combinational circuit is given as shown in the map of Figure 60. The prime implicants of the functions are first determined by some method such as the tabular method illustrated in Figure 61. Then, the prime implicants which must be included in the final sum of products expression to yield a transient hazard free circuit can be obtained by forming a table with a column for each pair of adjacent input states and selecting only those prime implicants needed to include all adjacent inputs. The procedure for selecting these necessary prime implicants is illustrated in Figure 62.



$$f = x_2 x_4 + \bar{x}_1 \bar{x}_4 + x_1 \bar{x}_2 \bar{x}_3$$

(a) Minimum Sum Representation



$$f = x_2 x_4 + \bar{x}_1 \bar{x}_4 + x_1 \bar{x}_2 \bar{x}_3 + \bar{x}_2 \bar{x}_3 \bar{x}_4 + \bar{x}_1 x_2 + x_1 \bar{x}_3 x_4$$

(b) Hazard Free Sum Representation

Figure 59. Map Method for Eliminating Transient Hazards

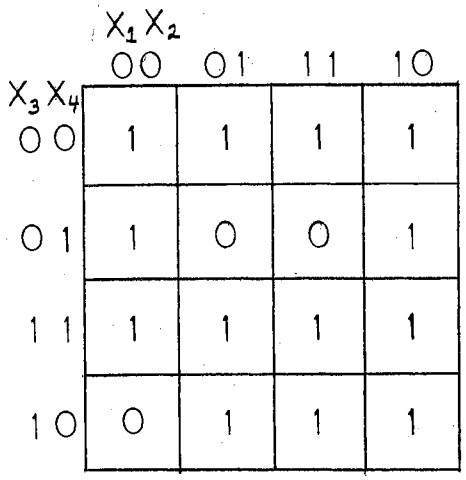


Figure 60. Map Representation of a Boolean Function

Summary

All presently known hazards which can occur in an asynchronous circuit have been reviewed in this appendix. A brief summary of these possible hazards and the methods for eliminating them is given in the following list.

Hazard	Method of Elimination
1. Critical Race	Assignment of adjacent state variable changes for all possible transitions between the internal states of the circuit.
2. Function Hazard	Limit the external input changes to adjacent changes.
3. Essential Hazard	Delay the state variable signal changes to allow external input

Decimal Equivalent	$X_1X_2X_3X_4$		$X_1X_2X_3X_4$		$X_1X_2X_3X_4$
0	0 0 0 0	(0-1)	0 0 0 -	(0,1,8,9)	- 0 0 -
		(0-4)	0 - 0 0	(0,4,8,12)	- - 0 0
		(0-8)	- 0 0 0	(1,3,9,11)	- 0 - 1
1	0 0 0 1			(4,6,12,14)	- 1 - 0
4	0 1 0 0			(8,12,10,14)	1 - - 0
8	1 0 0 0	(1-3)	0 0 - 1	(8,9,10,11)	1 0 - -
		(1-9)	- 0 0 1	(3,7,11,15)	- - 1 1
		(4-6)	0 1 - 0	(10,14,11,15)	1 - 1 -
3	0 0 1 1	(4-12)	- 1 0 0	(6,14,7,15)	- 1 1 -
6	0 1 1 0	(8-12)	1 - 0 0		
12	1 1 0 0	(8-9)	1 0 0 -		
9	1 0 0 1	(8-10)	1 0 - 0		
10	1 0 1 0				
		(3-7)	0 - 1 1		
7	0 1 1 1	(3-11)	- 0 1 1		
14	1 1 1 0	(6-7)	0 1 1 -		
11	1 0 1 1	(6-14)	- 1 1 0		
		(12-14)	1 1 - 0		
		(9-11)	1 0 - 1		
15	1 1 1 1	(10-14)	1 - 1 0		
		(10-11)	1 0 1 -		
		(7-15)	- 1 1 1		
		(14-15)	1 1 1 -		
		(11-15)	1 - 1 1		

The prime implicants are: $\bar{X}_2\bar{X}_3$; $\bar{X}_3\bar{X}_4$; $\bar{X}_2X_4$; $X_2\bar{X}_4$; $X_1\bar{X}_4$; $X_1\bar{X}_2$; X_3X_4; X_1X_3; X_2X_3

Figure 61. Tabular Method for Determining Prime Implicants of the Function in Figure 60

ADJACENT INPUT STATES

PRIME IMPLICANTS	0-1	0-4	0-8	1-3	1-9	4-6	4-12	8-12	8-9	8-10	3-7	3-11	6-7	6-14	12-14	9-11	10-14	10-11	7-15	14-15	11-15	
$\bar{x}_2\,\bar{x}_3$	(x)		x		x				x													*
$\bar{x}_3\,\bar{x}_4$		(x)	x				x	x														*
$\bar{x}_2\,x_4$				(x)	x							x				x						*
$x_2\,\bar{x}_4$						(x)	x							x	x							*
$x_1\,\bar{x}_4$								x		(x)					x		x					*
$x_1\,\bar{x}_2$									x	x						x		(x)				*
$x_3\,x_4$											(x)	x							x		x	*
$x_1\,x_3$																	x	x		x	x	
$x_2\,x_3$													(x)	x					x	x		*

The necessary prime implicants for a hazard free circuit would be:

$$\bar{x}_2\bar{x}_3;\ \bar{x}_3\bar{x}_4;\ x_2\bar{x}_4;\ \bar{x}_2x_4;\ x_1\bar{x}_2;\ x_3x_4;\ x_2x_3;\ x_1\bar{x}_4$$

Thus the hazard free Boolean equation for the circuit would be:

$$f = \bar{x}_2\bar{x}_3 + \bar{x}_3\bar{x}_4 + \bar{x}_2x_4 + x_2\bar{x}_4 + x_1\bar{x}_2 + x_3x_4 + x_2x_3 + x_1\bar{x}_4$$

Figure 62. Procedure for Obtaining a Hazard Free Boolean Equation From the Prime Implicants

	signal disturbances in the combinational circuitry to settle before the state variable signal enters the combinational circuit.
4. Transient Hazards	Include enough prime implicant terms in the Boolean equations representing the combinational circuit to allow each pair of adjacent inputs to the circuit to be represented by at least one prime implicant term.

Perhaps the most important aspect of implementing a physical asynchronous circuit with bounded stray delay logic elements is the ability to recognize and eliminate the different type hazards which can occur in the circuit. If the designer possesses this hazard recognition and elimination ability, then only the rate of external input change need be controlled to assure a safe operating circuit design. The important implication of hazard elimination is that the operational timing of the logic elements which comprise the circuit (except for the feedback delay elements) does not have to be controlled as long as the elements operate within the limits of their bounded stray delays.

APPENDIX D

SEPARATION BUBBLE VOLUME DETERMINATION

The separation bubble volume for the jet detachment calculations in Chapter VI can be approximated from the basic geometry of the bistable jet amplifier shown in Figure 63. The power jet of the amplifier is assumed to be deflected by angle φ by the control flow. From Figure 63,

$$R^2 = X_u^2 + (R\cos\phi - D - X_R \sin\alpha)^2 \tag{D-1}$$

and

$$X_u = X_R\cos\alpha - R\sin\phi \tag{D-2}$$

$$\therefore \quad X_u^2 = X_R^2\cos^2\alpha - 2X_R R\sin\phi\cos\alpha + R^2\sin^2\phi$$

Also:

$$(R\cos\alpha - D - X_R\sin\alpha)^2 = R^2\cos^2\phi - 2DR\cos\phi$$

$$- X_R R\cos\phi\sin\alpha + D^2 + 2X_R D\sin\alpha + X_R^2\sin^2\alpha$$

Equation (D-1) then gives

$$R = \frac{X_R^2 + 2X_R D\sin\alpha + D^2}{2(D\cos\phi + X_R\sin(\phi+\alpha)}$$

Non-dimensionalizing R with w yields

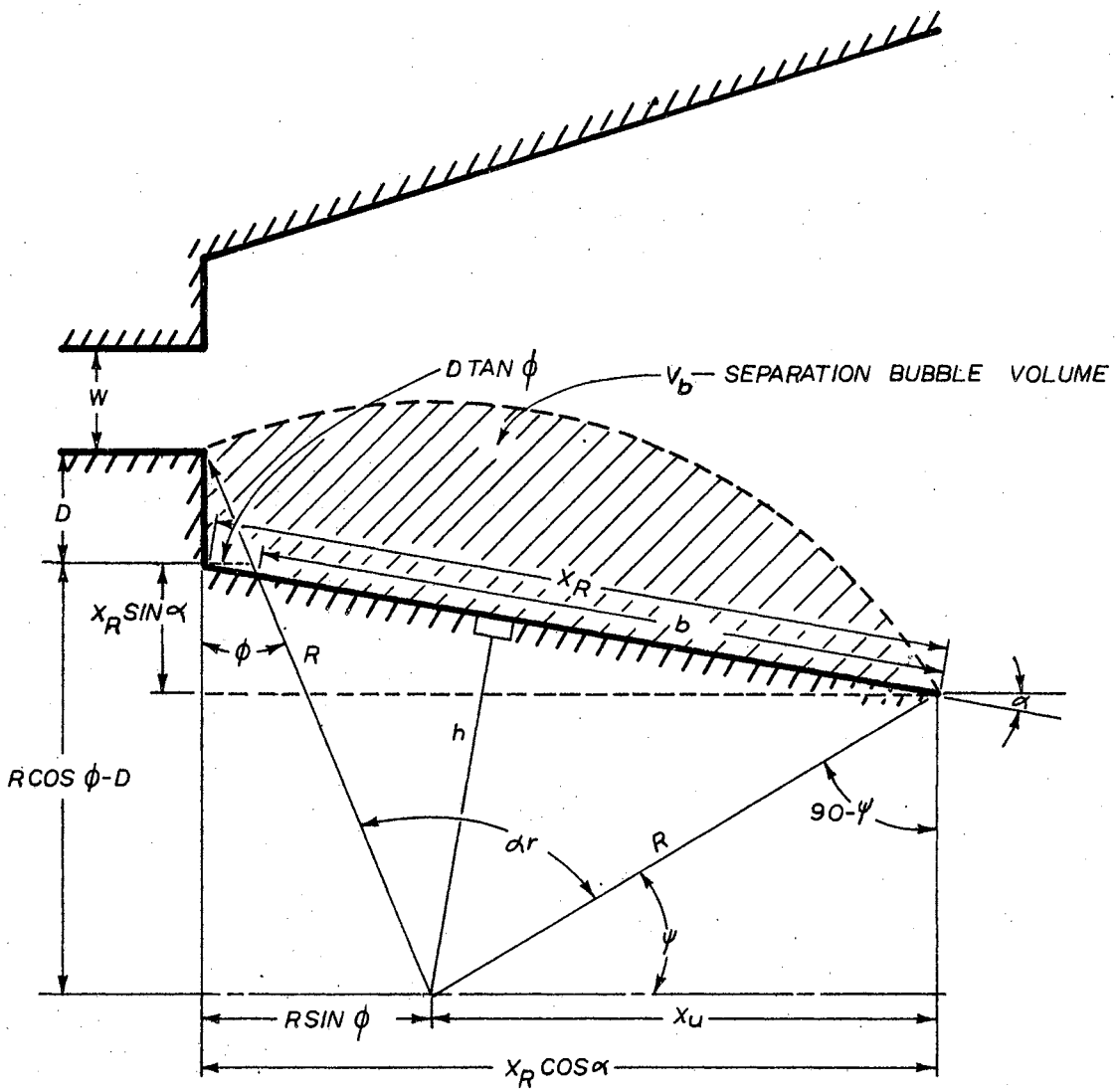


Figure 63. Geometry for Bubble Volume Determination

$$\frac{R}{w} = \frac{\left(\frac{X_R}{w}\right)^2 + 2\left(\frac{X_R}{w}\right)\left(\frac{D}{w}\right)\sin\alpha + \left(\frac{D}{w}\right)^2}{2\left(\frac{D}{w}\cos\phi + \frac{X_R}{w}\sin(\phi+\alpha)\right)} \tag{D-3}$$

Again, from Figure 63

$$\alpha_r = \pi - \left(\frac{\pi}{2} + \phi\right) - \psi = \frac{\pi}{2} + \phi - \psi \tag{D-4}$$

The angle, ψ, can be obtained from the relationship,

$$\cos\psi = \frac{X_u}{R} = \frac{X_R\cos\alpha - R\sin\phi}{R}$$

or

$$\psi = \cos^{-1}\left[\frac{X_R\cos\alpha - R\sin\phi}{R}\right]$$

Nondimensionalizing with w gives

$$\psi = \cos^{-1}\left[\frac{\frac{X_R}{w}\cos\alpha - \frac{R}{w}\sin\phi}{\frac{R}{w}}\right] \tag{D-5}$$

The angle, α_r, can then be defined as

$$\alpha_r = \frac{\pi}{2} + \phi - \cos^{-1}\left[\frac{\frac{X_R}{w}\cos\alpha - \frac{R}{w}\sin\phi}{\frac{R}{w}}\right] \tag{D-6}$$

The separation bubble volume, v_b, can be approximated by

$$v_b = \frac{1}{2}R^2\alpha_R + \frac{1}{2}D^2\tan\phi + \frac{1}{2}D^2\tan^2\phi\tan\alpha - \frac{1}{2}bh \tag{D-7}$$

Now,

$$b = X_R - \frac{D \tan\phi}{\cos\phi}$$

and

$$h = R \sin(\alpha + \psi)$$

This gives

$$\frac{1}{2} bh = \frac{1}{2}\left(X_R - \frac{(D)\tan\phi}{\cos\alpha}\right)\left(R \sin(\alpha+\psi)\right) \tag{D-8}$$

Employing Equation (D-8), the separation bubble volume equation can be expressed by

$$v_b = \frac{1}{2} R^2 \alpha_R + \frac{1}{2} D^2 \tan\phi + \frac{1}{2} D^2 \tan^2\phi \tan\alpha - \frac{1}{2}\left(X_R - \frac{D\tan\phi}{\cos\alpha}\right)\left(R \sin(\alpha+\psi)\right)$$

Introducing nondimensional parameters into the equation gives

$$v_b = \frac{\omega^2}{2}\left[\left(\frac{R}{\omega}\right)^2 \alpha_R + \left(\frac{D}{\omega}\right)^2 \tan\phi + \left(\frac{D}{\omega}\right)^2 \tan^2\phi \tan\alpha - \left(\frac{X_R}{\omega} - \frac{\frac{D}{\omega}\tan\phi}{\cos\alpha}\right)\left(\frac{R}{\omega}\sin(\alpha+\psi)\right)\right] \tag{D-9}$$

Now let

$$F(\phi, X_R) = \left(\frac{R}{\omega}\right)^2 \alpha_R + \left(\frac{D}{\omega}\right)^2 \tan\phi + \left(\frac{D}{\omega}\right)^2 \tan\phi \tan\alpha - \left(\frac{X_R}{\omega} - \frac{\frac{R}{\omega}\tan\phi}{\cos\phi}\right)\left(\frac{R}{\omega}\sin(\alpha+\psi)\right)$$

The bubble volume can then be given by

$$v_b = \frac{\omega^2}{2} F(\phi, X_R) \tag{D-10}$$

The deflection of the power jet by the control flow is assumed to be a function of the ratio of the control flow momentum to the power

jet flow momentum. Preliminary experimental determinations indicated that this momentum function could be expressed as

$$\tan \phi = \sqrt{\frac{J_c}{J_s}} \tag{D-11}$$

where: J_c - control flow momentum

J_s - supply flow momentum

φ - jet deflection angle.

If the width of the control port is assumed equal to power nozzle width, then the defection angle can be expressed as

$$\phi = \tan^{-1}\left(\frac{q_c}{q_s}\right) = \tan^{-1} Q_c \tag{D-12}$$

where: q_c - control flow

q_s - power jet supply flow.

Equations (D-3), (D-6), (D-12) can be employed to calculate the separation bubble volume given by Equation (D-10) for given amplifier geometry and control flow.

APPENDIX E

COMPUTER PROGRAM FOR COMPUTING JET DETACHMENT TIME

The computer program listed on the following pages can be used to calculate the detachment time of wall attached jet for imperfect non-step control flow inputs. The calculation procedure is described in detail in Chapter VI.

The input to the program is as follows:

DATA CARD 1:

All of the following variables are in floating point form with a field width of 10 with 3 decimals.

OFFST - Nondimensional inclined wall offset; $\frac{D}{w}$.

XWALL - Nondimensional inclined wall length; $\frac{L}{w}$.

ALPHA - Angle of wall inclination, radians; α.

RAT1 - Dummy variable.

DATA CARD 2:

The following variables are floating point variables with a field width of 10 with 3 decimals.

QMAG - Nondimensional control flow signal magnitude; q_c/q_s.

TDRS - Nondimensional control flow signal rise time; $2\, q_s\, t/w^2$.

DATA CARD 3:

The first five of the following variables are floating point variables with a field width of 10 with 3 decimals. The sixth variable in the card is a fixed point number which must be right justified in a field width of four.

DEL - Increment of jet reattachment locations; $X_2 - X_1$.

TDI - Dimensionless time increment; $t_{D_2} - t_{D_1}$.

TDII - Initial value of dimensionless time correction factor.

DELTD - Dummy variable.

DELQ - Dummy variable.

N - Number of points to be taken in the numerical integration procedure.

DATA CARD 4:

All of the following variables are in floating point form with a field width of 10 with 3 decimals.

X_0, X_1, X_2, X_3, X_4, X_5, X_6 - Dimensionless values of the reattachment location at which the entrained flow function is defined; $X_{R/w}$.

DATA CARD 5:

All of the following variables are in floating point form with a field width of 10 with 3 decimals.

Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 - Dimensionless values of the entrained flow magnitudes at the reattachment locations identified on DATA CARD 4; q_c/q_s.

DATA CARD 6:

The following variables are in floating point form with a field width of 10 with 3 decimals.

TDRSL - The limiting value of control flow signal rise time; $2\ q_s t/w^2$.

QMAGL - The limiting value of control flow signal magnitude; q_c/q_s.

The output of the program is as follows:

LINE 1:

The following variables are written as floating point numbers with a field width of 10 and 3 decimals.

OFFST - Nondimensional inclined wall offset; $\frac{D}{w}$.

XWALL - Nondimensional inclined wall length; $\frac{L}{w}$.

ALPHA - Angle of wall inclination, radians; α.

RAT1 - Dummy variable.

QMAG - Nondimensional control flow signal magnitude, q_c/q_s.

XLIMIT - Steady-state jet detachment location; $X_{R/w}$.

LINE 2:

The following variable is written as a fixed point number.

N - Number of points that was taken in the numerical integration procedure.

LINE 3:

The following numbers are written as floating point numbers with a field width of 10 and 3 decimals.

TOTD - Calculated dimensionless jet detachment time, $^{2\,q_s\,t}/_{w^2}$.

TDRS - Nondimensional control flow signal rise time, $^{2\,q_s\,t}/_{w^2}$.

```
      DIMENSIONXR(1),FRAT(101),COPR(1),THETA(51),TF(1),THET(1)
      DIMENSIONX(100),Q(100),PR(100)
      DIMENSIONXD(7),DV(7),CQ(7),CDV(7),XA(2)
  130 FORMAT(8F10.3)
  131 FORMAT(5F10.3,I4)
  132 FORMAT(I4)
      READ(5,130)OFFST,XWALL,ALPHA,RAT1,SIGMA
      READ(5,130)QMAG,TDRS
      READ(5,131)DEL,TDI,TDII,DELTD,DELQ,N
      READ(5,130)X0,X1,X2,X3,X4,X5,X6
      READ(5,130)Q0,Q1,Q2,Q3,Q4,Q5,Q6
      READ(5,130)TDRSL,QMAGL
      CALL XSWIT(OFFST,XWALL,ALPHA,XLIMIT)
      XD(1)=X0
      XD(2)=X1
      XD(3)=X2
      XD(4)=X3
      XD(5)=X4
      XD(6)=X5
      XD(7)=X6
      CALL CONST(X0,X1,X2,X3,X4,X5,X6,Q0,Q1,Q2,Q3,Q4,Q5,Q6,CQ(1),CQ(2),
     1CQ(3),CQ(4),CQ(5),CQ(6),CQ(7))
  500 TOTD=0.0
      XA(1)=X0
      TD=0.0
      CALLDVOL(ALPHA,OFFST,X0,TD,QMAG,TDRS,DFVX,DFVQ,QCON,DQTD)
      TD=(TDRS*ALOG(1.0+(2.1972*DFVQ/TDRS)))/2.1972
      TOTD=TD
      TDI=TD+TDII
  118 CJ=1.0
      KJ=1
      TNI=1.005
      IKK=1
      CALL FUNCT(CQ(1),CQ(2),CQ(3),CQ(4),CQ(5),CQ(6),CQ(7),X0,X1,X2,X3,
     1X4,X5,X6,AE1,XA(1))
      XA(2)=XA(1)+DEL
      IF(XA(2)-XLIMIT)117,117,119
  117 CALL FUNCT(CQ(1),CQ(2),CQ(3),CQ(4),CQ(5),CQ(6),CQ(7),X0,X1,X2,X3,
     1X4,X5,X6,AE2,XA(2))
      AE=(AE1+AE2)/2.0
      XRAV=(XA(1)+XA(2))/2.0
  108 CALL SIMI(N,TD,TDI,TDSUM,QMAG,TDRS,AE,ALPHA,OFFST,XRAV)
      IF(ABS(TDSUM-DEL)-0.0005)105,105,106
  106 IF(TDSUM-DEL)109,107,107
  107 IK=1
      GO TO 111
  109 IK=2
  111 IF(IK-IKK)116,112,116
  112 GO TO (113,114),IK
  113 TDI=TDI-TDII/TNI
      GO TO 115
  114 TDI=TDI+TDII/TNI
  115 IKK=IK
      KJ=KJ+1
      IF(TDI-TD)122,122,108
  122 IK=2
      GO TO 121
  116 IF(KJ-1)112,112,121
  121 CJ=CJ*2.1
      TNI=CJ
      GO TO (113,114),IK
  105 TOTD=TOTD+TDI-TD
      TD=TDI
      TDI=TDI+TDII
      XA(1)=XA(2)
      GO TO 118
  119 WRITE(6,130)OFFST,XWALL,ALPHA,RAT1,QMAG,XLIMIT
      WRITE(6,132)N
      WRITE(6,130)TOTD,TDRS
      TDRS=TDRS+150.0
      IF(TDRS-TDRSL)500,501,501
  501 QMAG=QMAG+0.05
      TDRS=0.01
      IF(QMAG-QMAGL)500,502,502
  502 CONTINUE
      STOP
      END
```

```
$IBFTC XSWIT
      SUBROUTINE XSWIT(OFFST,XWALL,ALPHA,ALIMX)
      SI=ATAN((OFFST+XWALL*SIN(ALPHA))/(XWALL*COS(ALPHA)))
      ALIMX=XWALL*(0.08*57.3*SI-0.5)
      IF(XWALL-ALIMX)20,20,21
   20 ALIMX=XWALL
   21 CONTINUE
      RETURN
      END
$IBFTC DVOL
      SUBROUTINE DVOL(ALPHA,OFFST,XRAV,TI,QMAG,TDRS,DFVX,DFVQ,QCON,DQTD)
  180 FORMAT(8F10.4)
      I=1
      TDRAT=TI/TDRS
      XR=XRAV+0.01
      QCON=QMAG*(1.0-EXP(-2.1972*TDRAT))
    6 PHI=ATAN(QCON)
    4 A6=XR**2+2.0*XR*OFFST*SIN(ALPHA)+OFFST**2
      A7=2.0*(OFFST*COS(PHI)+XR*SIN(ALPHA+PHI))
      RATW=A6/A7
      A1=ARCOS((XR*COS(ALPHA)-RATW*SIN(PHI))/RATW)
      ALPR=1.5708+PHI-A1
      A2=XR-((OFFST*TAN(PHI))/COS(ALPHA))
      A3=(OFFST**2)*((TAN(PHI))**2)*TAN(ALPHA)
      A4=(OFFST**2)*TAN(PHI)
      A5=(RATW**2)*ALPR
      VOLFUN=A5+A4+A3-A2*RATW*SIN(ALPHA+A1)
      GO TO(2,3,10,11),I
    2 VOLR=VOLFUN
      I=2
      XR=XR-0.02
      GO TO 4
    3 VOLL=VOLFUN
      DFVX=(VOLR-VOLL)/0.02
      I=3
      XR=XRAV
      QCON=QCON+0.02
      GO TO 6
   10 VOLR=VOLFUN
      I=4
      QCON=QCON-0.02
      GO TO 6
   11 VOLL=VOLFUN
      DFVQ=(VOLR-VOLL)/0.02
      DQTD=(2.1972*QMAG*EXP(-2.1972*TDRAT))/TDRS
      RETURN
      END
$IBFTC SIMI
      SUBROUTINE SIMI(N,TD,TDI,TDSUM,QMAG,TDRS,AE,ALPHA,OFFST,XRAV)
  180 FORMAT(8F10.4)
      FN=N
      JR=1
      H=(TDI-TD)/FN
      SUM4=0.0
      SUM2=0.0
      IJ=1
      TI=TD+H
  100 CALL DVOL(ALPHA,OFFST,XRAV,TI,QMAG,TDRS,DFVX,DFVQ,QCON,DQTD)
      GO TO (101,102,105,106,107),JR
  101 SUM4=SUM4+((QCON-AE-(DQTD*DFVQ))/DFVX)
      TI=TI+H
      JR=2
      GO TO 100
  102 SUM2=SUM2+((QCON-AE-(DQTD*DFVQ))/DFVX)
      IF(IJ-N+3)103,104,104
  103 IJ=IJ+2
      TI=TI+H
      JR=1
      GO TO 100
  104 TSUM1=4.0*SUM4+2.0*SUM2
      TI=TD
      JR=3
      GO TO 100
  105 TSUM2=(QCON-AE-(DQTD*DFVQ))/DFVX
      TI=TDI-H
      JR=4
      GO TO 100
  106 TSUM3=(4.0*(QCON-AE-(DQTD*DFVQ)))/DFVX
      TI=TDI
      JR=5
      GO TO 100
  107 TSUM4=(QCON-AE-(DQTD*DFVQ))/DFVX
      TDSUM=(H/3.0)*(TSUM1+TSUM2+TSUM3+TSUM4)
      RETURN
      END
```

```
$IBFTC CONST
      SUBROUTINE CONST(X0,X1,X2,X3,X4,X5,X6,Q0,Q1,Q2,Q3,Q4,Q5,Q6,QE0,QE1
     1,QE2,QE3,QE4,QE5,QE6)
      QE0=Q0/((X0-X1)*(X0-X2)*(X0-X3)*(X0-X4)*(X0-X5)*(X0-X6))
      QE1=Q1/((X1-X0)*(X1-X2)*(X1-X3)*(X1-X4)*(X1-X5)*(X1-X6))
      QE2=Q2/((X2-X0)*(X2-X1)*(X2-X3)*(X2-X4)*(X2-X5)*(X2-X6))
      QE3=Q3/((X3-X0)*(X3-X1)*(X3-X2)*(X3-X4)*(X3-X5)*(X3-X6))
      QE4=Q4/((X4-X0)*(X4-X1)*(X4-X2)*(X4-X3)*(X4-X5)*(X4-X6))
      QE5=Q5/((X5-X0)*(X5-X1)*(X5-X2)*(X5-X3)*(X5-X4)*(X5-X6))
      QE6=Q6/((X6-X0)*(X6-X1)*(X6-X2)*(X6-X3)*(X6-X4)*(X6-X5))
      RETURN
      END
$IBFTC FUNCT
      SUBROUTINE FUNCT(QE0,QE1,QE2,QE3,QE4,QE5,QE6,X0,X1,X2,X3,X4,X5,X6,
     1FUNCX,X)
      F0=(X-X1)*(X-X2)*(X-X3)*(X-X4)*(X-X5)*(X-X6)*QE0
      F1=(X-X0)*(X-X2)*(X-X3)*(X-X4)*(X-X5)*(X-X6)*QE1
      F2=(X-X0)*(X-X1)*(X-X3)*(X-X4)*(X-X5)*(X-X6)*QE2
      F3=(X-X0)*(X-X1)*(X-X2)*(X-X4)*(X-X5)*(X-X6)*QE3
      F4=(X-X0)*(X-X1)*(X-X2)*(X-X3)*(X-X5)*(X-X6)*QE4
      F5=(X-X0)*(X-X1)*(X-X2)*(X-X3)*(X-X4)*(X-X6)*QE5
      F6=(X-X0)*(X-X1)*(X-X2)*(X-X3)*(X-X4)*(X-X5)*(QE6)
      FUNCX=F0+F1+F2+F3+F4+F5+F6
      RETURN
      END
$ENTRY
```

VITA

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Doctor of Philosophy

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Personal Data: Born in Enid, Oklahoma, June 16, 1937, the son of Arthur M. and Ida DeMoss.

Education: Attended grade school at Southard, Oklahoma; graduated from Southard High School in May, 1955; received the Bachelor of Science degree and Master of Science degree from Oklahoma State University, with a major in Mechanical Engineering, in May, 1960 and August, 1961, respectively; completed requirements for the Doctor of Philosophy degree in May, 1967.

Professional Experience: During the summers of 1957, 1958, and 1959, was employed as an engineering trainee for Socony Mobil Petroleum Company, Healdton, Oklahoma; during the summer of 1960, was employed as a junior petroleum engineer for Pan American, Liberal, Kansas; during the 1960, 1961 school year, was employed as a graduate assistant on a Phillips Petroleum Research Project at Oklahoma State University; during the summer of 1961, was employed as research technologist for Socony Mobil Research Laboratory, Dallas, Texas; from December, 1961 to September, 1962, was employed as research assistant on AF-TAFB Research Project in the Fluid Power and Controls Laboratory at Oklahoma State University; from September, 1962 to September, 1966, was employed as research project leader of the Ford Fluid Circuits Project in the Fluid Power and Controls Laboratory at Oklahoma State University.

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