PROPOSAL FOR A 3.3V/5V LOW LEAKAGE HIGH TEMPERATURE DIGITAL CELL LIBRARY USING STACKED TRANSISTORS

By

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Glossary

ASIC	Application Specific Integrated Circuit
C_{ox}	Gate Oxide Capacitance
C_{Box}	Buried Oxide Capacitance
C_L	Load capacitance
$C_{depletion}$	Depletion capacitance
DIBL	Drain Induced Barrier lowering
ENIAC	Electronic Numeric Integrator and Calculator
GIDL	Gate Induced Drain Leakage
g_x	Horizontal grid spacing
g_y	Vertical grid spacing
h	Height of the cell
I_{ON}	ON current
I_{OFF}	OFF current
k	Boltzmann constant
L	Length of transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NL	Low threshold voltage NMOS transistor
PNR	Placement and Routing Tools
RN	Regular threshold voltage NMOS transistor

RTL	Register Transfer Level
S	Sub-threshold slope
$\mathbf{S_s}$	Safety zone required to avoid butting DRC errors
SOI	Silicon on Insulator
SOS	Silicon on Sapphire
UTSi	Ultra-thin Silicon
$\mathbf{V_{DD}}$	Supply Voltage
$\mathbf{V_{DS}}$	Drain to Source Voltage
$\mathbf{V_{GS}}$	Gate to Source Voltage
VTC	Voltage Transfer Characteristics
$\mathbf{V_T}$	Thermal Voltage
$\mathbf{V_{th}}$	Threshold Voltage
W	Width of transistor
$\mathbf{w_p}$	Width of power rail
$\mathbf{w_{use}}$	Usable cell width
μ	Mobility

CHAPTER 1

INTRODUCTION

1.1 Introduction

Electronics have been revolutionizing the world today ever since the invention of the first transistor in 1947. The size of electronic components has been shrinking gradually as a result of technology scaling. The effect of technology scaling has been tremendous and has resulted in transistors with feature sizes of less than 45nm. The first digital computer ENIAC was built using thousands of vacuum tubes and weighed nearly 30 tons, occupied a large area about the size of a room and consumed 150KW of power. In contrast, the modern day dual core processor which is about the size of a quarter consumes less than 50W of power[1].

Today the semiconductor industry is moving towards very deep submicron feature sizes which have resulted in higher density of transistors per unit area. As a result of this technology scaling, it is possible to accommodate more transistors and build in more functionality in a small area resulting in smaller size electronic devices. Power dissipation is becoming a major concern nowadays as more portable electronic devices

like cell phones, laptops and PDA's are growing in terms of complexity. High power dissipation elevates the operating temperature of these devices and hence more cooling is needed which in turn leads to more power consumption. These devices rely heavily on batteries as their source of power. High power consumption necessitates larger batteries or will result in shorter operating times.

1.2 Leakage Power

In order to reduce the power dissipation in electronic devices, the power supply voltage is scaled down, as we know that the average power is directly proportional to square of the supply voltage V_{dd}. Along with technology scaling, supply voltages have also been scaled from 5V to 3.3V to 2.5V to less than a volt for processor cores. However, reduction in supply voltage leads to increased propagation delay through logic gates and decreased noise margins. To partially avoid these undesirable effects, threshold voltages have been lowered as well, to maintain adequate performance. However, the decrease in threshold voltage leads to a substantial increase in sub-threshold leakage currents of MOSFET's, which offsets the power savings obtained from the supply voltage reduction. The sub-threshold leakage power component is becoming as significant as active and short-circuit power and needs to be taken into consideration and can no longer be ignored.

1.3 High Temperature Design

Circuits that operate at temperatures exceeding 200°C are defined in the context of this thesis to be extreme temperature circuits. High temperature applications like down-hole gas and oil well drilling and monitoring, aviation electronics and internal combustion

engine sensors are examples of a few applications requiring circuits that can operate in these harsh environments[2]. The operating temperature in these applications can reach as high as 300°C. As the operating temperature increases, bulk Silicon devices fail to operate due to substrate diode leakage currents. Silicon on Insulator (SOI) is found to overcome most of the problems of bulk silicon at high temperatures [3].

As designs grow in complexity day by day, it is becoming increasingly difficult to layout these circuits by hand. Hence a custom ASIC (Application Specific Integrated Circuit) cell library approach is desirable. This approach enables the designer to convert a design from its functional description in high level RTL (Register Transfer Level) code such as Verilog or VHDL to layout with minimum effort using automatic Placement & Routing (PNR) tools. The cell library would contain a set of combinatorial and sequential logic cells of different drive strengths with their corresponding layout, schematic and symbol views and their characterized timing and power models.

The objective of this research is to propose a method for developing a low leakage digital cell library capable of performing at extreme temperatures of up to 275°C in harsh environments. The leakage current at extreme temperatures is a dominant factor and plays an important role in determining circuit performance. It is found that in the Peregrine 0.5um SOS process, the PMOS devices leak less than the NMOS. Hence leakage control is necessary in the case of NMOS. It is found that replacing a regular NMOS transistor with stacked NMOS transistors reduces leakage with very little area penalty and minimal loss in performance. A method of stacking low threshold voltage

NMOS transistors over regular threshold voltage NMOS transistors will be shown to reduce leakage currents at extreme temperatures of 275°C, while exhibiting excellent I_{ON} /I_{OFF} ratios. The I_{ON}/I_{OFF} ratio is a figure of merit for digital circuits and is defined as the ratio of the current when the transistor is 'ON' to the current when the transistor is 'OFF'.

1.4 Thesis Organization

This thesis consists of 6 chapters. Chapter 2 describes the details of Silicon on Insulator (SOI) implementation and its advantages at high temperatures. Chapter 3 describes the details of the cell library, its format, library design guidelines and characterization of cells for timing. Chapter 4 deals with the literary review on leakage current components and various leakage mechanisms in transistors. Chapter 5 describes the stacked transistor principle developed in this thesis for low leakage NMOS devices along with the measurements of leakage of stacked NMOS transistors. The Voltage Transfer Characteristic (VTC) of Inverter, NAND and NOR gate's with stacked NMOS transistors is presented to demonstrate the adequacy of logic noise margin levels. Chapter 6 summarizes the leakage measurement results and discusses future work in this direction.

CHAPTER 2

SILICON ON INSULATOR

2.1 Introduction

At elevated temperatures in excess of 100°C to 150°C, conventional bulk silicon devices fail to operate due to the drift in device parameters. In bulk technology, the active devices and transistors are formed on a thin surface layer and a depletion layer isolates these active devices from each other. In bulk technology, leakage is dominated by thermal generation currents of well diode junction as a result of large junction area along with weak inversion currents. In SOI leakage currents are comprised of sub-threshold leakage currents, tunneling currents and side wall interface leakage.

The leakage current in bulk silicon and SOI increases exponentially with temperature and the I_{ON} /I_{OFF} ratio becomes smaller with increasing temperature. All devices are eventually no longer functional and are unreliable at very high temperatures. Excessive leakage power and the resulting higher power dissipation in bulk limit the operation of bulk silicon devices at extreme temperatures. The drift in device parameters of bulk silicon devices at extreme temperature affects the correct operation of analog and digital circuits in terms of bandwidth and switching speed or delay.

2.2 Bulk vs. SOI

Bulk CMOS technology has the following limitations when the operating temperatures exceed 125°C:

a) Excessive leakage currents due to the large area associated with reverse biased substrate PN junction.

b) Greater Sub-threshold Leakage currents.

c) Increased latch-up.

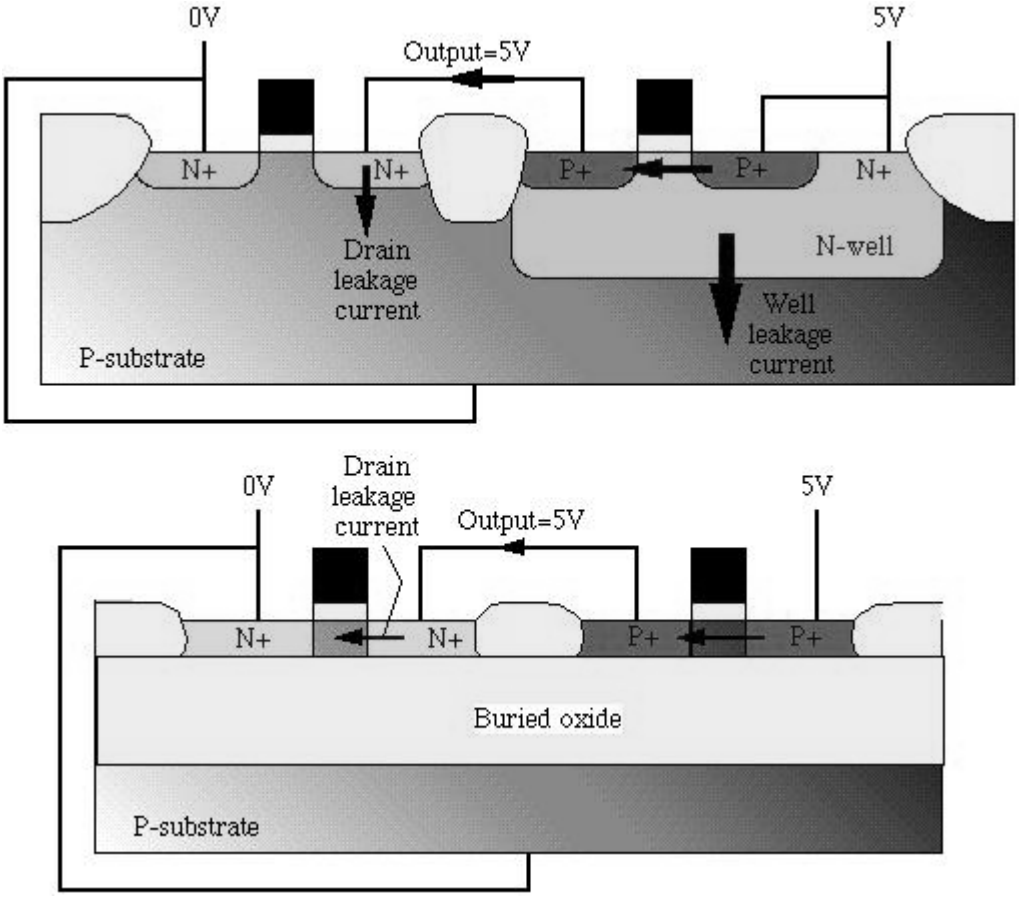


Figure 2.1 Cross section of Bulk CMOS and SOI CMOS inverter showing the leakage current paths [11].

Leakage currents and latch-up are the biggest source of failure with bulk CMOS. SOI overcomes this problem as the PMOS and NMOS devices are isolated by an insulating oxide layer which prevents latch-up, reduces leakage currents and device capacitance, increases bandwidth and have an increased sub-threshold slope which reduces leakage and overall power consumption[4].

Silicon-On-Insulator (SOI) and Silicon-On-Sapphire (SOS) technology is a popular contender to the traditional bulk silicon technology. SOI/SOS transistors have lower drain and source parasitic junction capacitances which results in low power and high speed analog and digital circuits at equivalent device nodes[5]. As a consequence of the buried oxide structure used in SOI for isolating devices, the NMOS and PMOS devices can be placed in closer proximity to each other without concerns of latch-up occurrences. Since no wells are needed to separate the NMOS and PMOS devices, the smaller layout of SOI CMOS circuits leads to reduced parasitic capacitances. Since SOI devices do not need reverse biased junctions for well isolations, their device density is higher and leakage currents lower. Hence SOI CMOS circuits have higher speed performance and lower power consumption at equivalent device nodes.

SOI presents some unique advantages at higher temperatures like higher I_{ON}/I_{OFF} ratios, lower threshold voltage temperature coefficients and absence of thermally induced latch-up. These advantages make SOI the preferred technology of choice for high temperature operation. The threshold voltage temperature coefficients for the Peregrine Semiconductor's 0.5um SOS process were found to be 0.75mV/$^{\circ}$C and 1.1mV/$^{\circ}$C for

NMOS and PMOS respectively. In contrast for bulk processes these values lied between 0.5mV/°C and 4mV/°C[6].

In Bulk process, the transistors and active devices are formed in a layer of single or mono crystalline silicon over the substrate. In SOI, this thin monocrystalline silicon active layer is separated from the substrate by a layer of thick buried oxide as illustrated in Figure 2.2 below.

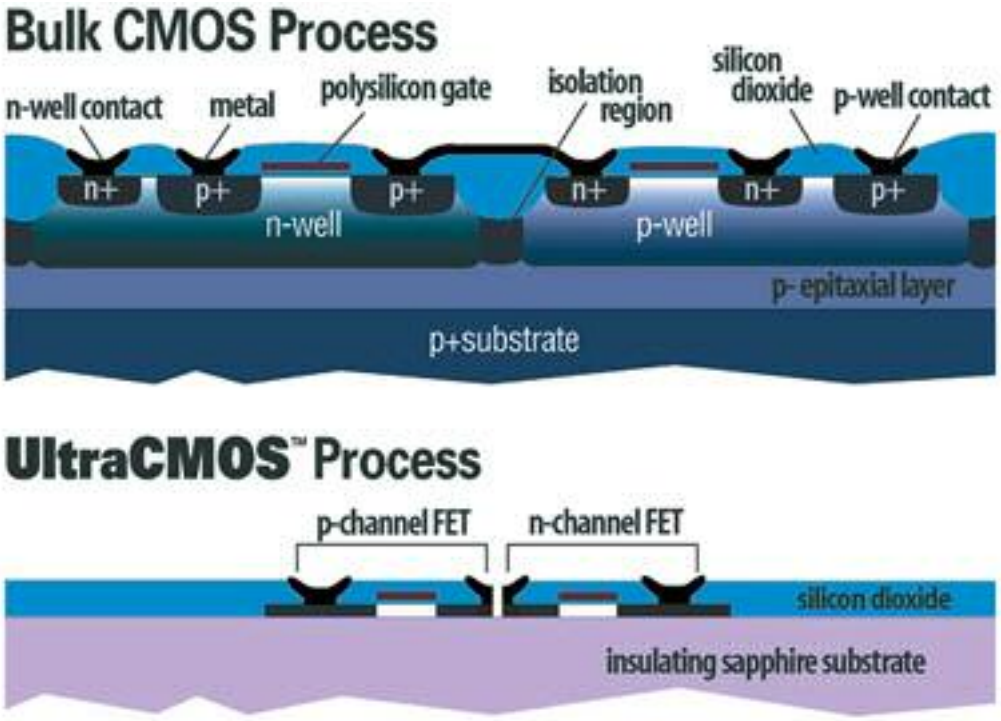


Figure 2.2 Bulk CMOS vs. Peregrine UTSi process[7].

The differences between bulk and SOI in terms of device structures and circuit performance are explained in the following sections.

2.2.1 Reduced Parasitic Capacitance

Due to the oxide isolation structure in SOI, the source/drain parasitic capacitances are smaller which leads to high speed performance of SOI CMOS circuits while operating at lower power supply voltages.

The dynamic power consumption of CMOS circuits is given by the equation

$$P_{dyn} = \alpha C_L V_{dd}^2 f \qquad (2.1)$$

where C_L is the switching load capacitance, V_{dd} is the supply voltage, f is the frequency at which the circuit is switched and α is the switching probability. It can be seen that power dissipation decreases as the capacitance is reduced.

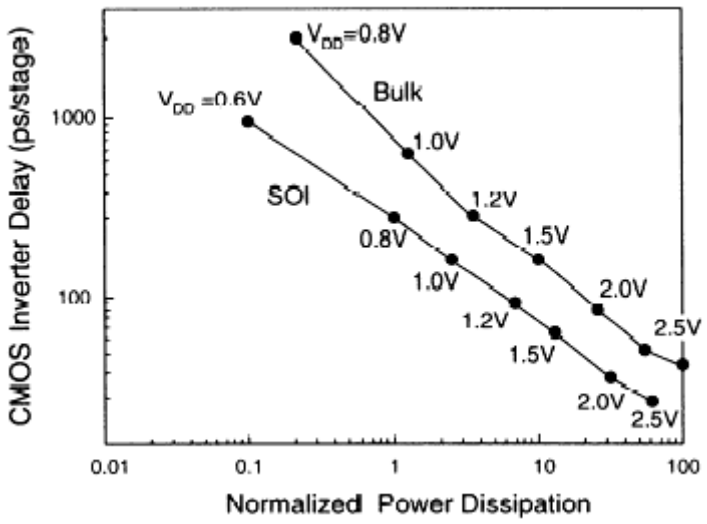


Figure 2.3 Normalized power dissipation and delay of 0.35um Bulk and SOI technologies for various operating voltages[8].

It is clear from figure 2.3 that for same dimensions and supply voltage SOI has reduced delays and lower power dissipation.

2.2.2 Latch-up in Bulk and SOI

In bulk silicon, the formation of a thyristor like PNPN structure with a parasitic PNP and NPN transistor connected back to back results in latch-up. Latch-up is the creation of a low impedance path between the power and ground rails by triggering the thyristor structure. Once triggered both transistors start conducting and large amounts of current start flowing through the devices until the power is switched off. Latch-up degrades circuit performance and results in destruction of the device due to over currents. In SOI, there is no direct path between the various devices and the devices are isolated by a layer of thick oxide which surrounds each device[4]. Hence latch-up can never occur in SOI. This is an advantage when using SOI for high temperature applications.

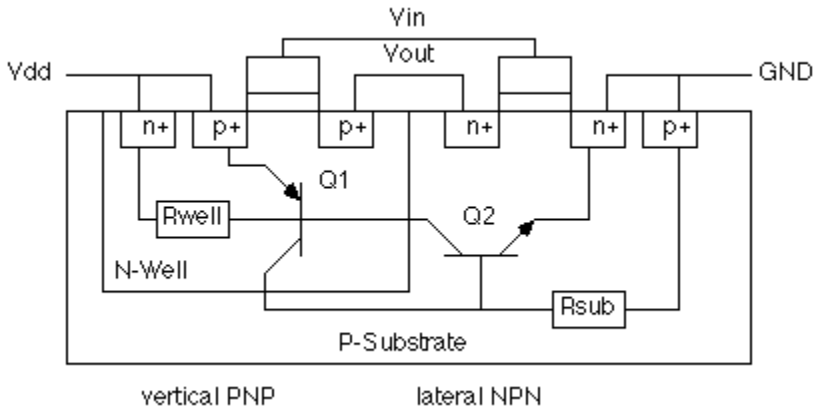


Figure 2.4 Cross section of an Inverter in Bulk showing the parasitic PNP and NPN transistors.

2.2.3 Leakage currents

In today's deep-submicron era, leakage currents account for a significant portion of the total power consumption and cannot be ignored. SOI leakage currents are comprised of sub-threshold leakage currents, tunneling currents, surface or interface and side wall

interface leakage. In bulk technology, leakage is dominated by thermal generation currents of well diode junction as a result of large junction area along with weak inversion currents.

The sub-threshold leakage current can be expressed by the following equation[9]:

$$I_{sub} = k \exp\left(\frac{V_{gs} - V_{th}}{S / \ln 10}\right)\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{2.2}$$

Where k is a process parameter, V_{th} is the threshold voltage, S is the subthreshold swing and V_T is the thermal voltage *(KT/q)*. Sub-threshold slope is a key parameter in leakage current analysis and is defined as the slope of the logarithm of drain current plotted as a function of gate voltage.

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_{Leak})} = \frac{\eta V_T}{\log_{10} e} = 2.3\left(1 + \frac{C_{eq}}{C_{ox}}\right)\frac{kT}{q} \quad \textbf{Bulk} \tag{2.3}$$

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_{Leak})} = \frac{\eta V_T}{\log_{10} e} = 2.3\frac{kT}{q} \quad \textbf{SOI} \tag{2.4}$$

A smaller value of sub-threshold slope implies better leakage performance and good I_{ON}/I_{OFF} ratios. The advantage of having lower value of S is that it allows lower threshold voltages for an identical I_{ON}/I_{OFF} ratio. Typical values of S for SOI and bulk is around 65mV/decade and 80-85mV/decade respectively. A lower threshold voltage allows the possibility of lower power supply voltages for the same or greater drive strength resulting

in reduced power dissipation. As temperature increases, the threshold voltage is reduced resulting in higher off current I_{OFF}. Hence it is apparent that devices with lower sub-threshold slope have better leakage performance at high temperatures.

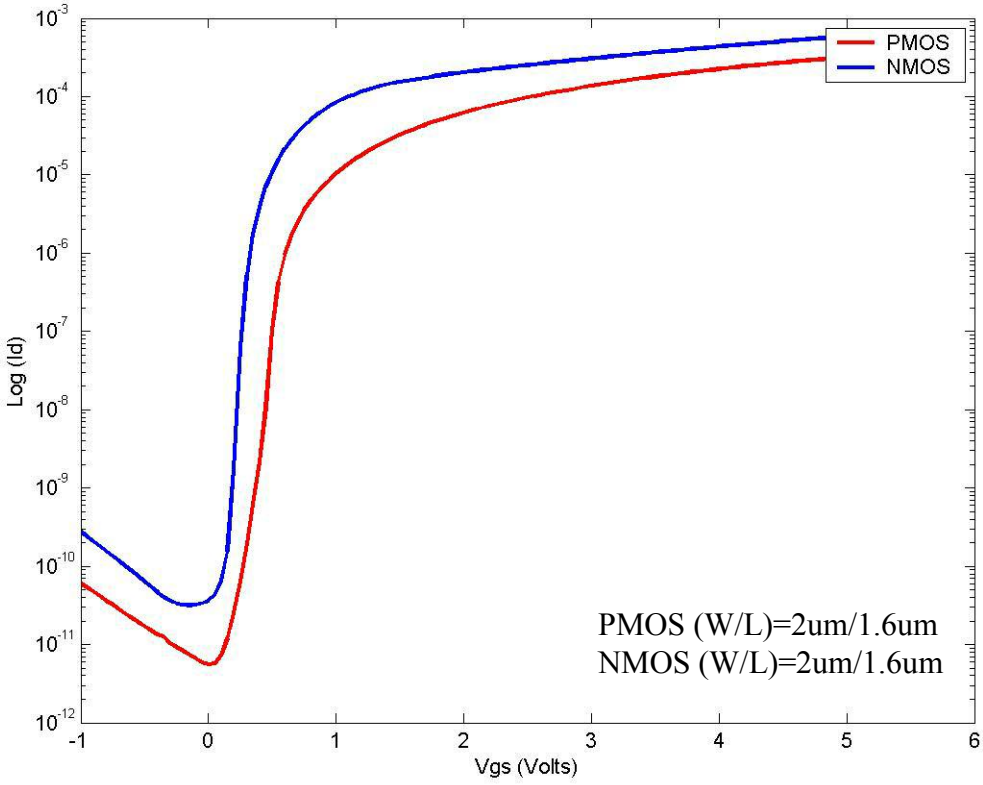


Figure 2.5 Plot of Log (I_D) vs. V_{GS} for regular threshold voltage for Regular PMOS & NMOS transistors.

2.2.4 Short Channel Effects

Short channel devices are devices whose channel length is comparable to the depletion regions of drain/source junctions. In the case of short channel transistors, the channel is no longer under the control of just the gate but under the influence of both gate and drain. Velocity saturation, hot carriers, DIBL (Drain Induced Barrier Lowering) and output impedance variation with drain voltage are some important short channel effects[10].

DIBL is one of the predominant short channel effects. In a short channel device, the potential barrier is controlled by the electric fields due to gate and drain. As the drain voltage increases, the depletion region due to drain extends more into the channel reducing the gate voltage required to create an inversion layer of charge and hence leading to a reduction in threshold voltage[10]. The reduced value of threshold voltage increases the off state leakage current. The effect of DIBL is less pronounced in SOI than bulk due to the buried oxide layer in SOI devices. The threshold voltage variation due to DIBL is suppressed in SOI by the thin-film structure of SOI [4]. The thin-film in SOI results in better control of the gate over the active region.

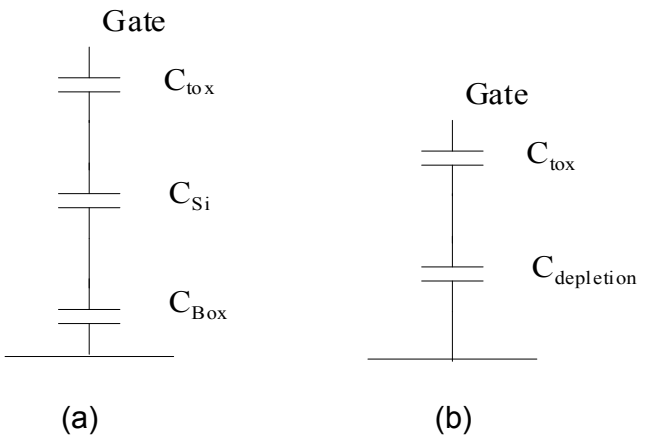


Figure 2.6 Capacitance of (a) Fully depleted SOI and (b) Bulk.

The capacitance of Fully-Depleted (FD) SOI with C_{Si} in series with C_{Box} (B_{ox}-Buried Oxide) can be considered equivalent to the depletion capacitance $C_{depletion}$ by the following equation

$$C_{eq} = \frac{C_{Si}.C_{Box}}{C_{Si} + C_{Box}} \approx C_{Box} \tag{2.5}$$

The capacitance C_{eq} is dominated by C_{Box} as it is the smaller of the two capacitances. C_{eq} = C_{Box} is smaller than $C_{depletion}$ of bulk. The smaller equivalent capacitance of SOI results in better coupling of the gate voltage to the active region resulting in reducing the influence of DIBL in addition to decreasing the sub-threshold slope.

CHAPTER 3

CELL LIBRARY

3.1 Introduction

In the recent years there has been a significant increase in the complexity of integrated circuits. As the complexity of circuit designs grows, it is becoming more difficult to design and layout these circuits by hand. An ASIC standard cell library approach is preferred in these cases. A standard cell library is a set of combinatorial and sequential logic cells of different drive strengths with their corresponding layout, schematic and symbol views and their characterized timing and power models. It enables a designer to easily translate a design from it's high level description in Verilog or VHDL to a layout using placement and routing tools.

3.2 ASIC Design Flow

In general, ASIC based designs are realized using the following steps:

1. Description of circuit behavior in some high level language such as Verilog or VHDL.
2. Compilation of behavioral or RTL (Register Transfer Level) description into a logical netlist using logic synthesis tools such as Cadence Ambit Synthesizer or Synopsys Design Compiler.

3. Translation of the logical netlist into a geometric netlist, followed by placement and routing with PNR tools.

Figure 3.1 shows the various steps involved in the ASIC design flow. The standard cell library contains the description of all the cells:

a) to facilitate synthesis of designs

b) for translation of behavioral code to a netlist

c) to have the physical description of the cells to enable routing.

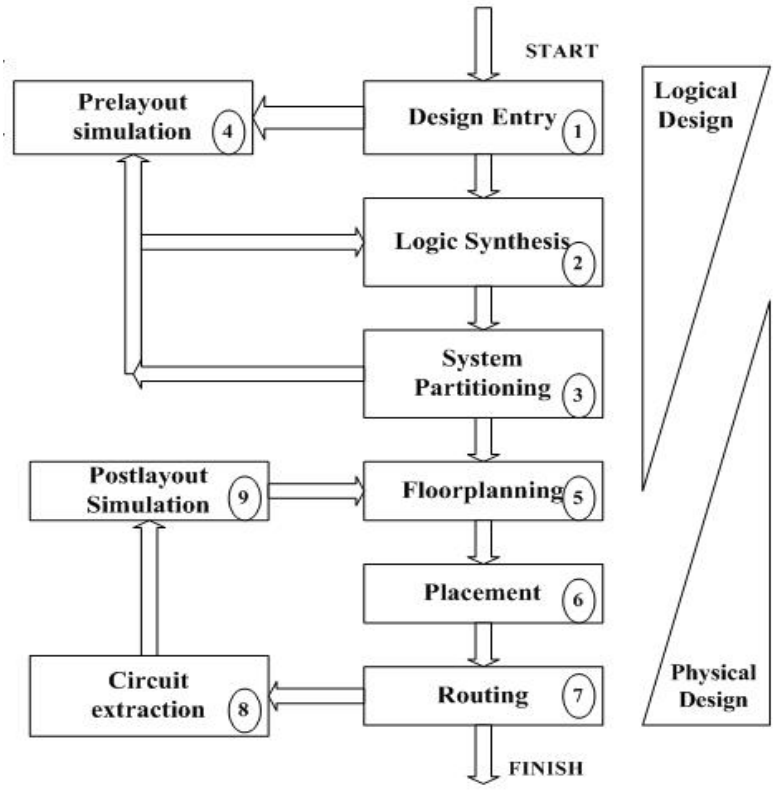


Figure 3.1 ASIC Design Flow [12].

The various steps in the ASIC design flow are as follows [12]:

1) **Design Entry** – Entering the design into an ASIC design system using a hardware desciption language such as Verilog or VHDL.

2) **Logic Synthesis** – Use a hardware description language (Verilog or VHDL) and a logic synthesis tool to produce a netlist which is a description of the logic cells and their connections.
3) **System Partitioning** – This step involves dividing a large system into manageable pieces.
4) **Prelayout Simulation** – In this step we check the functionality of the design.
5) **Floorplanning** – Arranging the blocks of the netlist on the chip.
6) **Placement** – Deciding the location of cells in a block.
7) **Routing** – Make the connection between cells and blocks.
8) **Extraction** – Determine the resistance and capacitance of the interconnects.
9) **Post Layout Simulation** – Confirm that the design still works with the added interconnect parasitics.

There are two main stages in the ASIC design flow:

1) **Logical Design** – Steps 1-4 comprise the logic design phase. In this phase the designer has more control over the design. The timing model file is used to translate the RTL description of the design into a netlist and several iterations are performed in order to optimize the circuit to meet speed, area and power requirements. If there are any errors in the logic, they are fixed at this level.
2) **Physical Design** – Steps 5-9 comprise the physical design. In this phase the designer has more control over the area and static timing. The LEF (Library Exchange Format) file which contains the physical description of the cells and design rules related to placement and routing process(such as metal and via

spacings, pitch and direction of metal tracks) is provided to the PNR tool to generate the layout of the design from the synthesized netlist.

3.3 Design of High temperature Standard Cell Library

There are certain factors that need to be considered when designing a standard cell library for harsh high temperature applications. The factors that need to be considered are:

1) Selection of proper lengths for transistors to meet leakage current, bandwidth and noise margin requirements at high temperatures.
2) Beta matching the transistors to maximize the noise margins versus optimal delay or minimum geometry as appropriate to the application.
3) Avoiding or minimum usage of transmission gates to eliminate potential floating body problems in SOS.
4) Maximizing the usage of NAND over NOR type structures to reduce leakage currents as NMOS's leakage per micrometer of device width is greater than PMOS devices of equal length. NOR type structures have multiple parallel paths for NMOS to leak. Peregrine Semiconductor's PMOS devices have lower leakage/um of gate length when compared to an equivalent length NMOS device.
5) Limiting the number of series connected transistors to four or less. When the number of series connected transistors is large, the rise/fall times degrade due to higher resistance and greater self capacitance.

3.4 Standard Cell Library

3.4.1 Cell Library Design Flow

The standard cell library design process involves three stages which are illustrated in Figure 3.2 and explained in detail below.

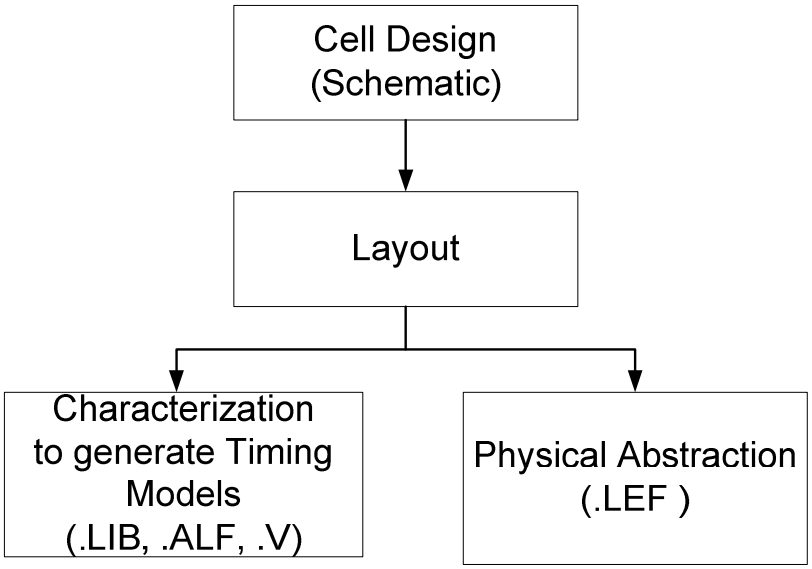


Figure 3.2 Standard Cell Library Generation Flow.

1. **Creating Standard Cells** – This involves selecting the correct set of cells for the library,creating schematics and symbol views, drawing layouts according to specifications, performing DRC (Design rule Check) and LVS (Layout versus Schematic) checks and extracting the SPICE netlist for each cell. The cell library should consist of a variety of cells like:
    a) Posistive Logic Cells – Buffer, AND, OR, XOR
    b) Negative Logic Cells – Inverter, NAND, NOR, XNOR, AND-OR-INVERT, OR-AND-INVERT

c) Sequential Logic Cells – D-Flipflops and Latches with Preset and Clear inputs, including scan functions.

d) Arithmetic Cells – Full adder, Full subtractor, Half adder, Half subtractor.

e) Clock Buffer Cells – Clock buffers with drive strengths ranging from 1X-10X for clock tree synthesis.

f) Special Cells – Multiplexers, Tristate Inverters and Buffers, Pull up and Pull down cells.

2. **Extraction of Timing and Power** – The timing values of each cell namely the intrinsic rise time, intrinsic fall time, rise resistance, fall resistance, setup time and hold time for the cells are characterized using Signalstorm (a Cadence Design Suite tool). The power models are also generated for each cell which gives information about the power dissipation associated with each input to output transistion and the leakage power. The timing and power information is put together to form a ".lib" file which can be used by the synthesis tool to convert the behavioral code to a Verilog netlist that meets the timing constraints.

3. **Physical Description of Cells** – This step involves creating the abstract view of each cell which is basically a physical description of the cell having the information about the different layers of metals used in the layout, the different metal layers available and the preferences of these layers for routing, the area of each cell along with the dimension of the power and ground rails and the pin positions so that the router can route the I/O pins.

3.4.2 Components of a Cell Library

Each cell in the cell library must contain the following:

1. A physical layout which describes the physical dimensions of the cell with all the I/O pin connections
2. A circuit schematic which is used to extract timing and power information and perform LVS check to ensure the layout matches the schematic.
3. A behavioral model which describes the functionality of each cell without any cell dimensions.
4. A Verilog/VHDL model which describes the function of the cell in Verilog/VHDL to be used in synthesis of the design.
5. A detailed timing model which is used during synthesis to optimize the design and verify the timing requirements of the design.
6. A test strategy to evaluate the functionality and performance of the cell library.
7. A symbol view which is useful to generate the schematic views of the design.
8. A wire load model to estimate the RC delay associated with the interconnects.
9. A routing model for proper routing of the design in order to avoid design rule errors.

3.4.3 Format of a Standard Cell

The layout of a typical standard cell is illustrated in Figure 3.3 below.

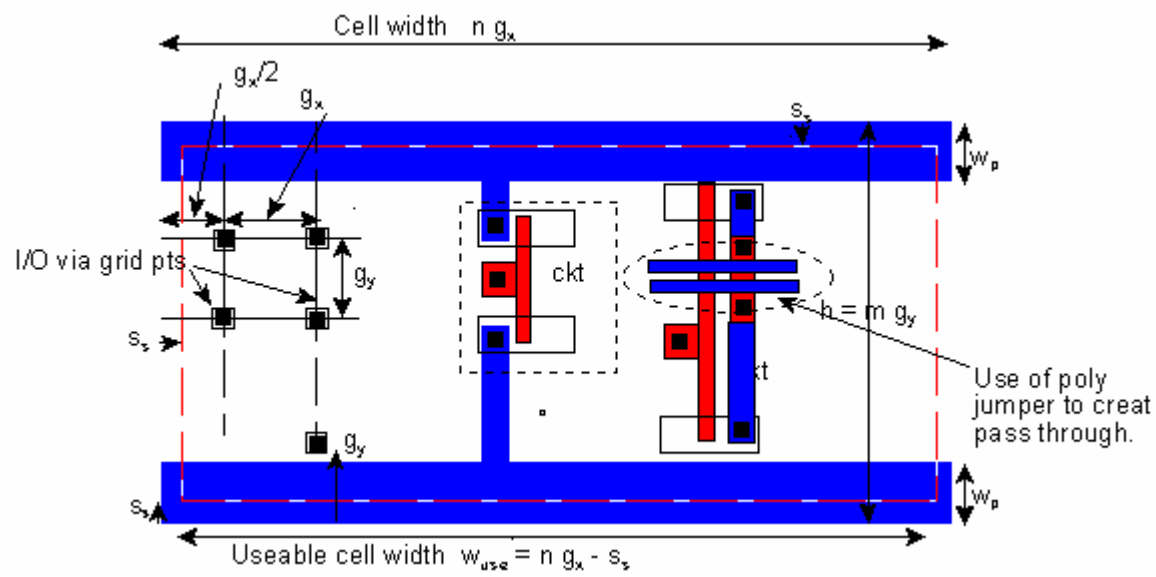


Figure 3.3 Layout of a typical Standard Cell [13].

The power and ground rails are approximately 2.4μm wide and routed horizontally in METAL1. The input and output of the cell is routed vertically in METAL2 (horizontally in METAL3) over the cell connecting to the terminal pins defined by labeled pins. All I/O pins are placed on a g_x by g_y routing grid referred to as the routing pitch, which starts g_x inches from both vertical edges and $g_y/2$ inches from the horizontal cell edge. The overall width of the cell is an integer multiple of g_x.

All METAL1 used in the cell must be wholly contained within the cell between the power and ground rails. Polysilicon, p-diffusion and LOCOS are allowed to extend to with a distance s_s of the cell boundary. METAL2 runs vertically whereas METAL1 runs both vertically and horizontally. The grid spacing g_x and g_y are typically set respectively by the minimum spacing of two METAL1-METAL2 vias. The routing

pitch should be atleast via-to-via spacing in order to satisfy design rules for metal-to-metal separation [13].

The cells are usually stacked over each other by flipping every other row so that the power and ground rings are overlapping alternately to save area.The standard cells are placed horizontally abutting each other and there should be no design rule violations when the cells are abutted. Hence, all the polysilicon,LOCOS and METAL1 must be contained within the cell boundary within a distance of s_s from the north, south, east and west edges of the standard cell. METAL1 should not be used in the cell layout outside the power rails as this would conflict with the router causing design rule violations. Generally METAL2, METAL3 and greater are not used in cell layouts as they are used for external routing and I/O connections. For each metal layer, a preferred direction of routing is assigned. Usually METAL1 is routed horizontally and METAL2 is routed vertically etc. The placement and routing of the cells is done according to the Verilog netlist given to the PNR tool.

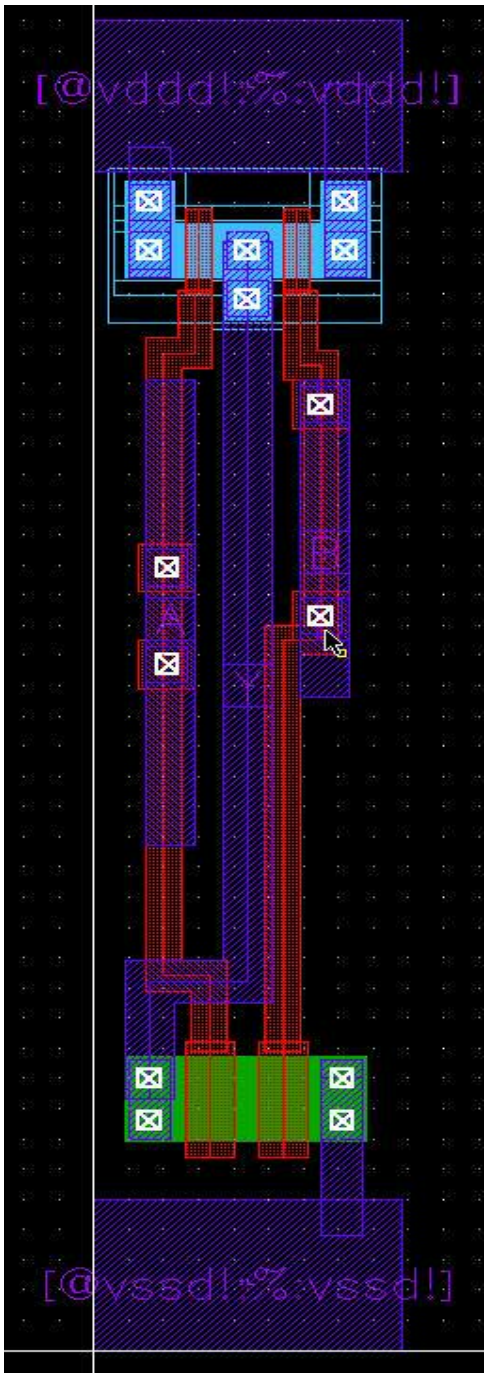


Figure 3.4 Layout of a 2-input NAND gate cell.

3.5 Characterization of a Cell Library

A cell library needs to be characterized for timing and power to generate a detailed timing model file for use by the synthesizer to optimize the design and verify that the

timing constraints are met. Once the standard cells are characterized, the abstraction shifts the design from transistor-level to gate level synthesis, floorplanning and place and route.

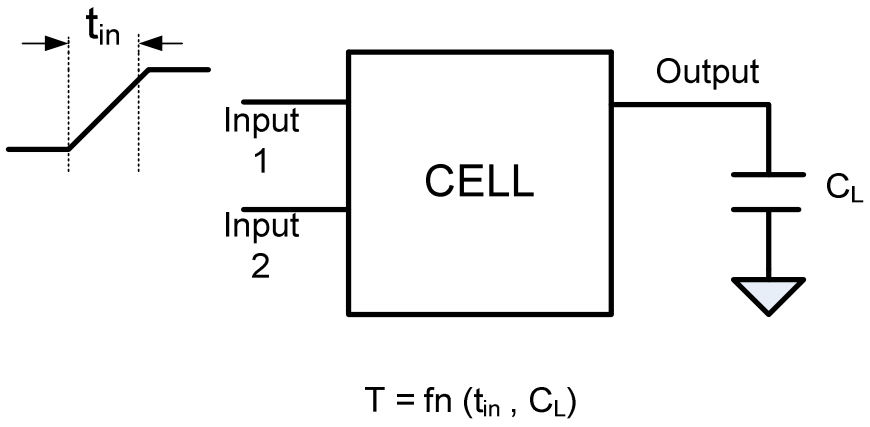


Figure 3.5 Characterization of delay in terms of input slew and output load capacitance.

A standard cell is usually characterized in terms of input slew rate "t_{in}" and output load capacitance "C_L" for different supply voltages, temperatures and process corners such as slow, typical and fast corners. The standard cells are characterized for output transistion time, propagation delay from each input pin to the outputs, internal switching power, leakage power dissipation and input pin capacitances. In addition to these, sequential cells are characterized for setup time and hold time.

3.5.1 Delay Models

There are a number of models available for characterizing the timing of a cell library. The quality and accuracy of the synthesized circuit is dependent on the level of details and accuracy with which the individual cells have been characterized. There are a number of

delay models which trade off between accuracy and performance. In general the delay of a standard cell is a function of the fan-out and the rise and fall times of the input signals. One of the popular delay models is illustrated in Figure 3.6 and is briefly described here.

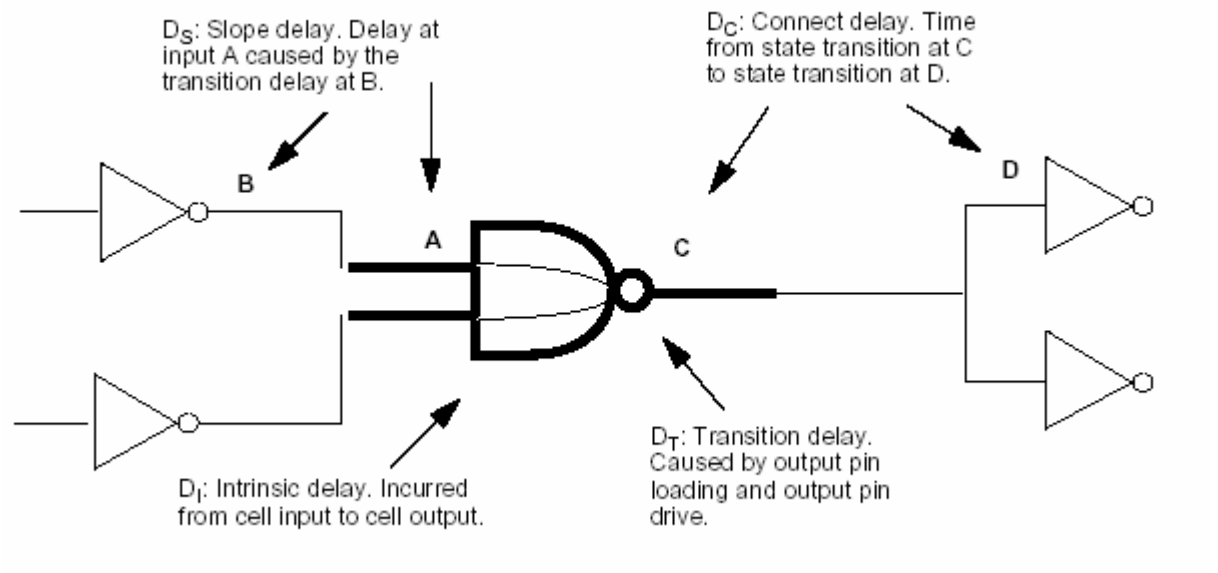


Figure 3.6 Delay components of a combinational logic gate[14].

The total delay of a combinational logic gate, D_{TOTAL} has four main delay components which are represented by the following equation:

$$D_{TOTAL} = D_I + D_T + D_S + D_C$$

The first term D_I represents the intrinsic delay which is the delay with no output loading on the cell. The second term D_T is the transition delay which is due to the output load capacitance C_L. The third term D_S is the delay due to the input slope. The last term D_C is the delay for the signal to propagate from the output of one gate to the input of another gate or also called as the interconnect delay.

3.5.2 Timing Characterization

Each standard cell is characterized to determine the propagation delay from each input pin to the output pin and the output transition time. These values are usually measured between pre-determined threshold values of the signal edges. The measurement of these two delay values is illustrated in Figure 3.7.

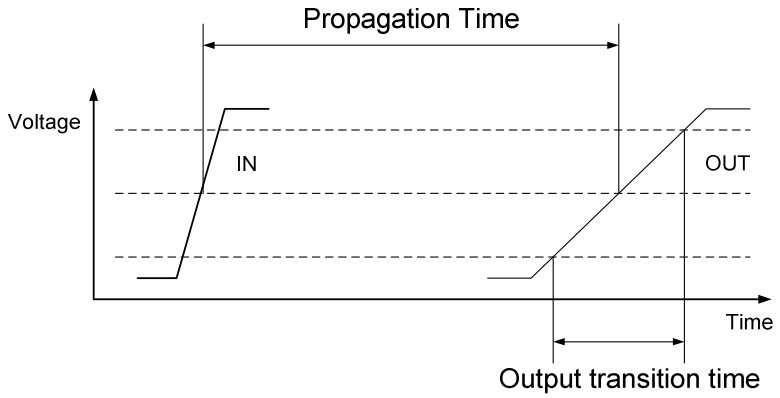


Figure 3.7 Measurement of propagation time and output transition time.

The propagation time is usually measured between the two threshold points of 50% of the voltage range of the input signal to 50% of the voltage range of the output signal. The output transition time is measured between the two threshold points which are chosen to be either from 10% of the voltage range to 90% of the voltage range of the output signal or 20% to 80% or 0% to 100% of the output voltage level.The values of output transition time and propagation time are required for gate level synthesis and delay calculation tools. In synthesis, the output transition time is used for estimating the input slew rates of successive cells and the propagation time of each cell is extracted from the delay table based on the input slew rate and output load. Hence, the delay between two nodes in a

design can be calculated with the propagation time and output transition time of each cell on the path between two nodes.

3.5.3 Setup and Hold Time Characterization

Sequential cells like D-flipflops and latches are usually characterized to determine the setup time and hold time requirements of these cells. The setup time of a sequential cell is generally defined as the minimum allowed time between the arrival of data and the transition of the Clock signal, so that the output of the clock signal will reach the expected logical value within a specific delay. The hold time of a sequential cell is defined as the minimum time that an input signal must remain stable after the active edge of the clock signal to ensure that input value is correctly latched at the output.

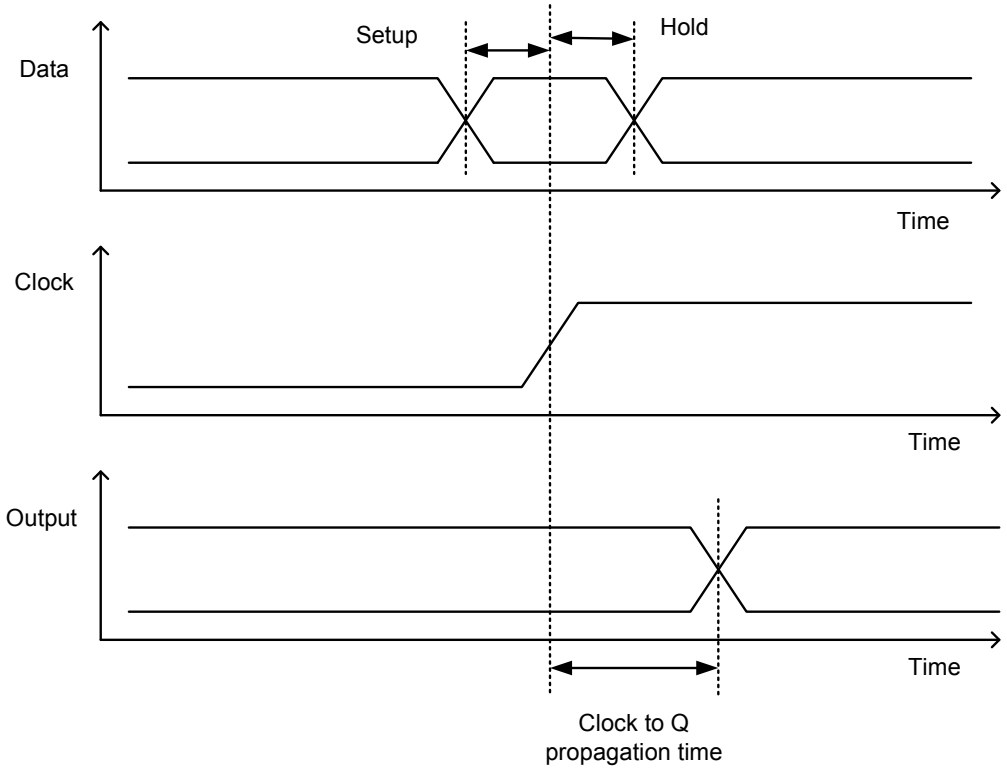


Figure 3.8 Setup and Hold time constraint for an edge triggered flipflop.

If the data makes a transition during the setup time, an incorrect value will be latched at the output of the cell. The setup time should also be such that it does not degrade the Clock-to-Q propagation time beyond a pre-determined tolerance value.

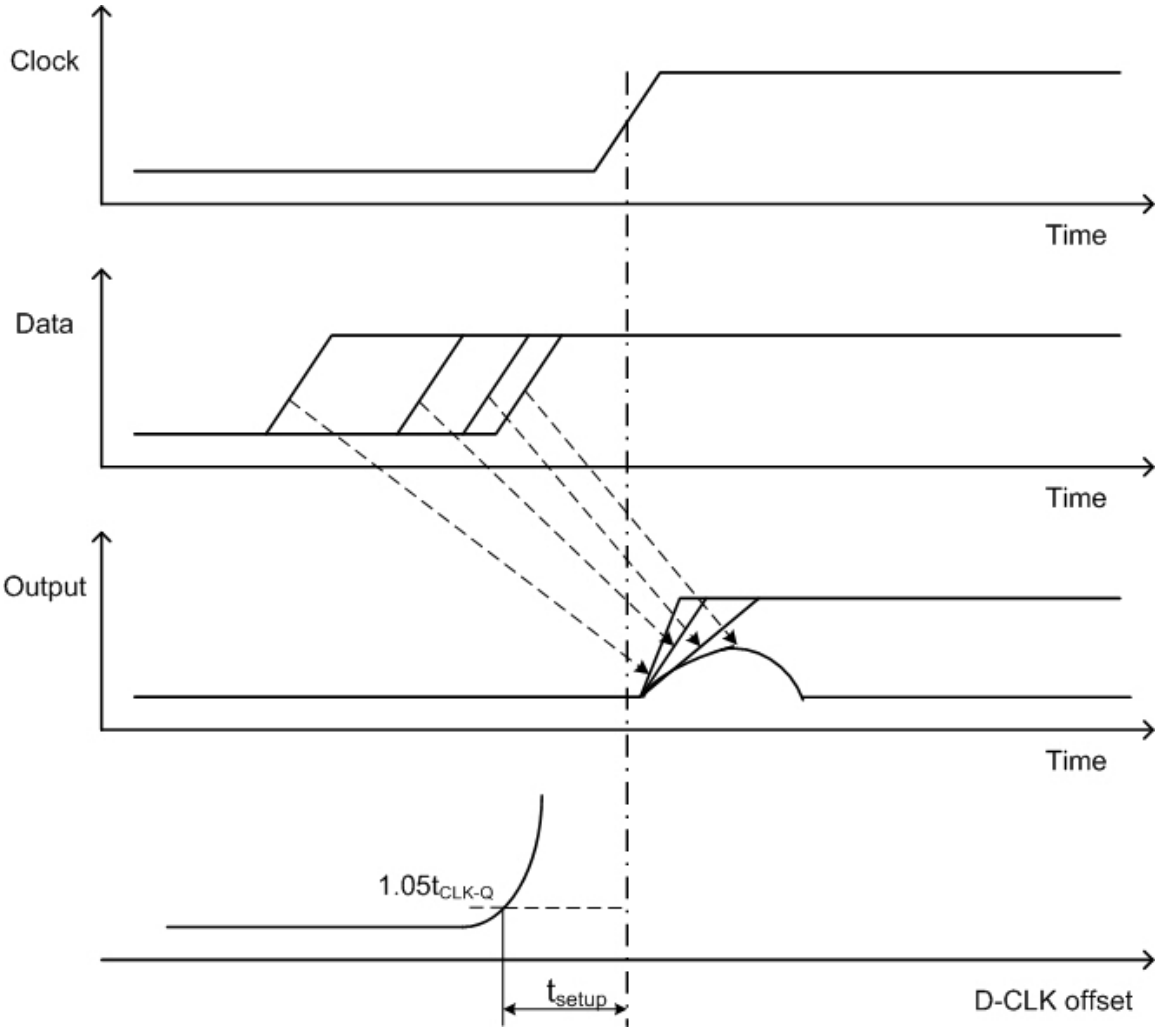


Figure 3.9 Determination of setup time of a sequential cell[15].

The characterization of setup time is based on a method of varying the D-CLK offset iteratively and observing the output Q and the CLK-Q delay. Figure 3.9 illustrates the method of determining the setup time by varying the data transistion with respect to the CLK. As the time interval between the arrival of the data at D input and Clock edge

narrows down, this leads to a gradual degradation of the output at Q and the CLK-Q delay increases. When the D input changes a long time before the Clock edge, the CLK-Q delay has a constant value. As the transition at the D input moves closer to the Clock edge, the CLK-Q delay starts to increase. If the data changes too close to the clock edge, the sequential cell fails to latch the correct output. If the setup time is defined as the minimum D-CLK offset that barely produces the right output at Q, the combinational logic following the sequential cell would have an excessive delay. The best way of defining the setup time is the value of D-CLK offset that minimizes the sum of the D-CLK offset and the CLK-Q delay[16]. For automatic characterization of sequential cells, setup time and hold time are defined as D-CLK offset that corresponds to some fixed percentage increase in the CLK-Q delay like 5%. Once the value of CLK-Q delay increases beyond the tolerance value of 5%, the previous value of D-CLK offset is taken as the setup time. The hold time is measured in an identical way as the setup time.

The setup time is measured using a binary search method, which is an optimization method to find the value of an input variable associated with a goal value of an output variable. In this method a binary search is done to locate the output variable goal value within a search range of the input variable by iteratively halving that range to converge rapidly on the target value. The measured value of the output variable is compared with the goal value for every iteration. Figure 3.10 illustrates the setup time measurement using binary search.

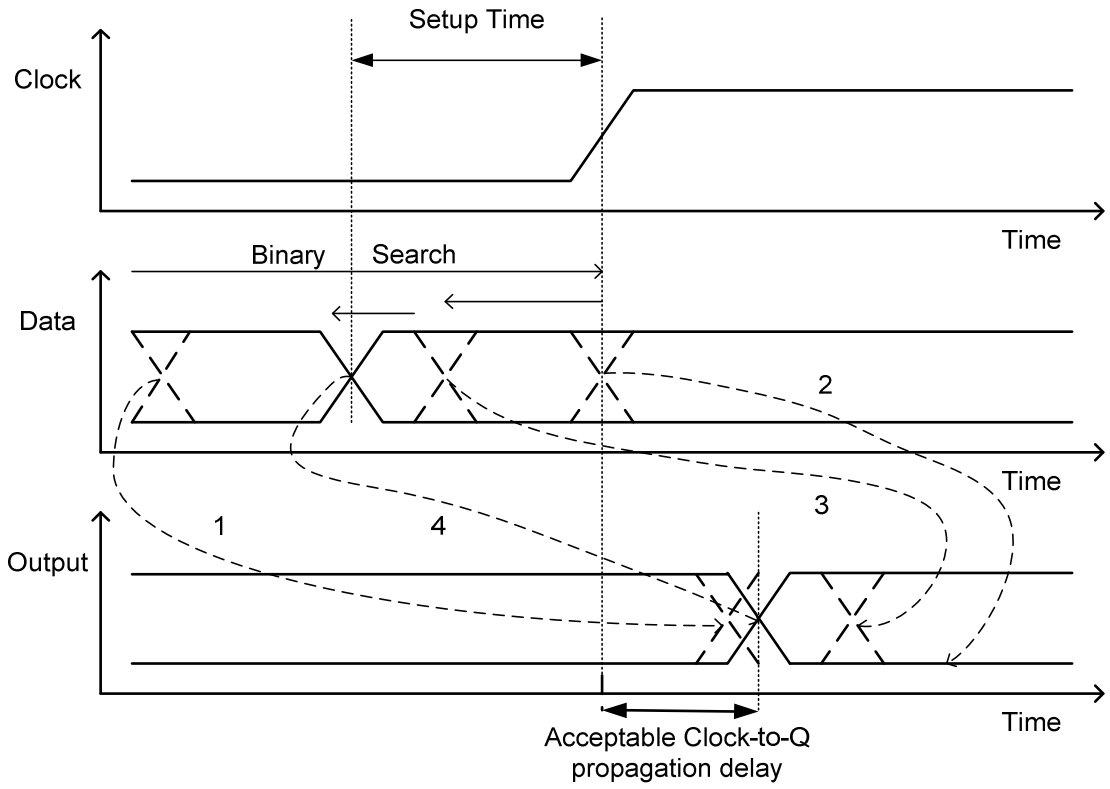


Figure 3.10 Setup time measurement using binary search.

In our case of setup time measurement, the goals are output transition time and allowable Clock-to-Q propagation delay. To start the binary search, a lower boundary and upper boundary are specified. Data transition 1 at the lower boundary is early enough to cause a good output signal. Data transition 2 at the upper boundary is too late to change the output signal. Hence the setup time constraint lies between the upper and lower boundaries. The binary search algorithm tests data transition at the midpoint between the upper and lower boundaries, points 1 and 2. Data transition 3 at the midpoint changes the output signal but causes a longer Clock-to-Q propagation delay and hence does not satisfy the setup time constraint. The algorithm now sets point 3 as the upper boundary and tests the data transition at the new midpoint. If the data output has an acceptable Clock-to-Q delay, the new midpoint is set as the new lower boundary. Then the algorithm

tests data transition at the new midpoint within the new range again. In this way the binary search algorithm, iterates by setting a new boundary and a midpoint until the binary search reaches the correct value of setup time. The data transition 4 is found to be the latest point that satisfies the setup time constraint with an acceptable Clock-to-Q delay. Hold time measurement is similar to setup time which follows the iterative binary search algorithm.

It is also possible to have negative setup and negative hold times for a sequential cell. A negative setup time in a cell is due to the internal delay of the Data signal with respect to the Clock. This means that the input can change after the Clock edge and still the input would be properly latched at the output. For example, if a D flip flop has a setup time of −1ns, the data present at the D input from 1 ns after the clock edge is the data latched at the output Q, provided the data remains stable from that moment. A negative hold time in a cell is due to the internal delay of the Clock signal. This means that the input can change before the Clock edge and the input would be latched correctly. For example, if a D flip flop has a hold time of −1ns, the data present at the D input up to 1 ns before the clock edge is the data latched at the output Q, provided the data was stable up to that moment.

CHAPTER 4

REVIEW OF LEAKAGE MECHANISMS IN SOS/SOI

4.1 Introduction

In comparison to the vacuum tube of yesteryears which consumed few watts of power, today's transistor requires only a few milliwatts of power. In the early 1990's, power dissipation was of little concern and the emphasis was more on performance and miniaturization of electronic devices. As more and more portable electronic devices started dominating the market, there was a push to have a longer battery life. In order to improve the performance of the circuits it became a requirement to integrate more functions into each chip, becoming the driving force behind device scaling. As a result the power per unit area is growing,requiring additional cooling and/or devices which are more robust to high temperature performance. In the past leakage currents were very small and was not much of a concern. But as we move towards smaller feature sizes, leakage currents due to phenomenon such as sub-threshold leakage, DIBL, GIDL etc. start to dominate and account for nearly 50% of the total power consumption. The reason for this is that the supply voltage has continually scaled down to reduce the dynamic power consumption of integrated circuits which depends on the square of the supply voltage. As the supply voltage is scaled down, to maintain performance, the threshold voltage has to be scaled in the same proportion. As threshold voltages are scaled,

subthreshold leakage rises exponentially. The leakage current is mainly influenced by factos such as the threshold voltage, channel physical dimensions, channel doping profile, gate oxide thickness, supply voltage, drain and gate voltages. This increase in leakage currents drains the battery more quickly limiting the operating time of portable devices.

At higher temperature of operation, the problem gets progressively worse as threshold voltages decrease with increasing temperatures and the sub-threshold leakage currents are higher at these high temperatures compared to room temperature of operation. Sub-threshold currents rise as a result of the shift in threshold voltages due to threshold voltage degradation at high temperatures. The higher leakage current leads to poor I_{ON} /I_{OFF} ratios and to eventual device failure at high temperatures. Hence some form of leakage control is essential to ensure that the transistor circuits perform reliably at these high temperatures.

4.2 Sources of Power Dissipation

There are three major sources of power dissipation in digital CMOS circuits which are represented by the following equation[17]:

$$P_{total} = \alpha \,.\, C_L \,.\, V \,.\, V_{dd} \,.\, f_{clk} \;+\; I_{sc} \,.\, V_{dd} \;+\; I_{leakage} \,.\, V_{dd} \qquad (4.1)$$

The first term represents the switching component of power. This power is attributed to the transition of the output nodes between two logic levels such as ‘1’ and ‘0’ in a CMOS circuit which results in the charging and discharging of parasitic capacitances. This

component of power is directly proportional to the supply voltage V_{dd}, the load capacitance C_L that is being switched, the clock frequency f_{clk} and the transistion switching probability α . V is the voltage swing at the node which in most cases is equal to the supply voltage V_{dd} .

The second term represents the power dissipation due to the short circuit currents that flow directly from supply to ground when the PMOS and NMOS transistors are both conducting simultaneously. I_{sc} represents the short circuit current. When the inputs to a gate are stable at either logic levels, only one of the two networks – either PMOS or NMOS conducts and no short circuit current flows. But when the output of a gate changes in response to the input, both PMOS and NMOS conduct simultaneously for a brief interval of time. The duration of this interval depends on input and output rise and fall times. The switching and short circuit power dissipation are collectively referred to as "dynamic power dissipation".

The third term represents the leakage power that flows when the inputs and outputs of a gate are not changing. The sub-threshold currents and gate leakage currents are accounted by this term $I_{leakage}$. As the threshold voltage is scaled down because of lower supply voltages, the lower is the degree to which the MOSFET's are turned off and higher is the sub-threshold leakage current. Figure 4.1 illustrates the dynamic power dissipation in CMOS circuits.

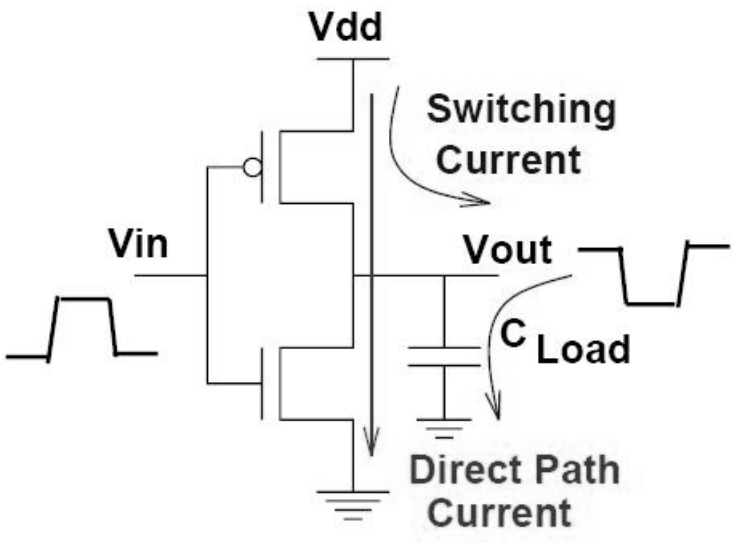


Figure 4.1 Dynamic Power Dissipation in CMOS circuits[18].

4.3 Transistor Leakage Mechanisms

The scaling of supply voltages and threshold voltage has a large impact on the magnitude of leakage currents. The off-state current in a transistor is the drain current when the gate-source voltage V_{GS} is zero. This off-state current is termed as leakage current. Ideally, the drain current should be zero when V_{GS} is zero. The leakage current is influenced by the threshold voltage, channel physical dimensions, channel doping profile, gate oxide thickness, supply voltage, drain and gate voltages. The various leakage current mechanisms are illustrated in Figure 4.2.

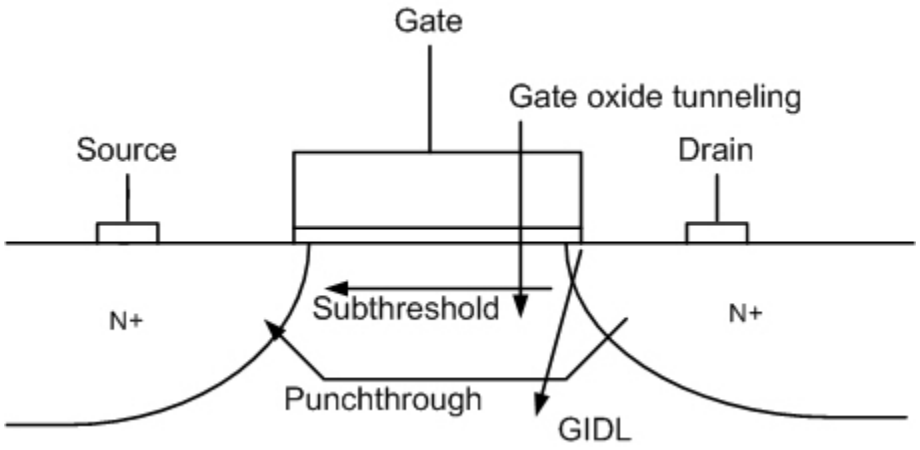


Figure.4.2 Leakage current mechanisms in transistors[9].

4.3.1 Subthreshold Leakage Current

Subthreshold leakage current is defined as the current that flows between the drain and source junctions in a MOSFET when the gate voltage is below the threshold voltage V_{th} .

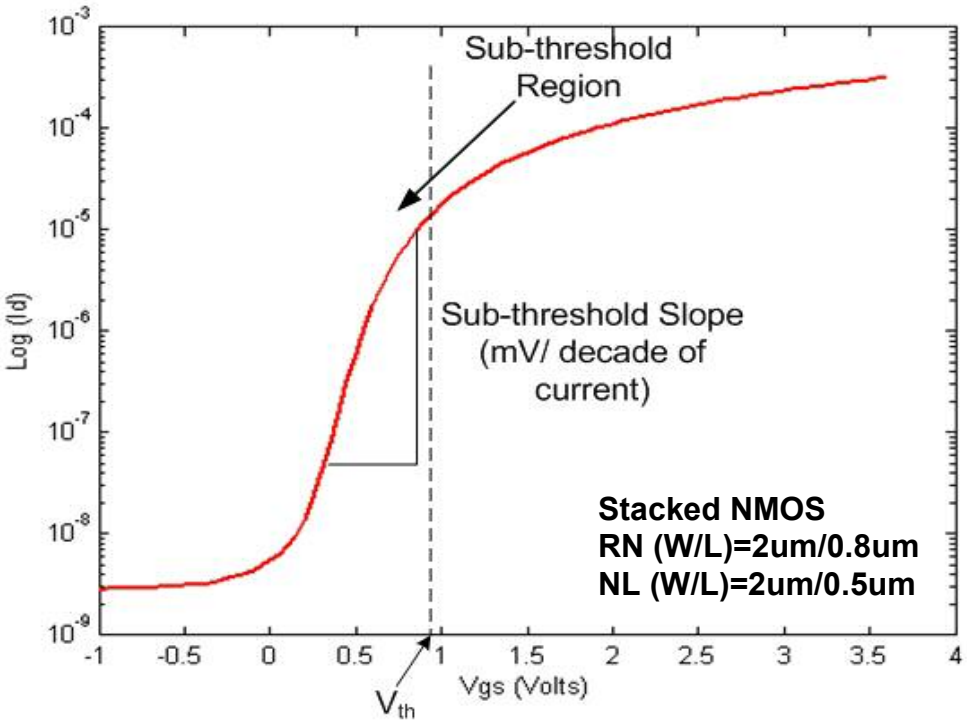


Figure 4.3 Log (I_D) vs. V_{GS} curve showing the subthreshold region and sub-threshold slope at 27^{o}C.

The subthreshold region is the linear region in the plot of log (I_D) vs. V_{GS} . In the subthreshold region, the minority carrier concentration is small but not zero. The subthreshold current is dominated by diffusion current as opposed to drift currents in strong inversion regions. Sub-threshold leakage currents is the dominant leakage mechanism in deep submicrometer devices as the threshold voltage is scaled down in these devices along with supply voltage.

The sub-threshold leakage current is given by the equation[9]:

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(v_T)^2 \times e^{(V_g - V_{th})/mv_T} \times (1 - e^{-v_{DS}/v_T}) \tag{4.2}$$

where $$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}}$$

where V_{th} is the threshold voltage, and $v_T = KT/q$ is the thermal voltage, C_{ox} is the gate oxide capacitance; μ_0 is the zero bias mobility and m is the sub-threshold swing coefficient. W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of depletion layer. From the above equation, the leakage current decreases with increase in the length of the transistor.

In long-channel devices, the sub-threshold current is independent of drain voltage for V_{DS} larger than a few v_T . The dependence of sub-threshold current on gate voltage is exponential. The inverse of the slope of $log(I_D)$ versus V_{GS} curve is called the sub-threshold slope S . The equation for S is given by:

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_{Leak})} = \frac{\eta V_T}{\log_{10} e} = 2.3\left(1 + \frac{C_{eq}}{C_{ox}}\right)\frac{kT}{q} \tag{4.3}$$

Sub-threshold slope determines how effectively a transistor can be turned off when V_{GS} is decreased below V_{th}. Sub-threshold slope S is measured in millivolts per decade of drain current. Typical values of S can range from 70-120 mV/decade for bulk process and 60-90 mV/decade for SOI. A low value of S is desirable as it allows lower threshold voltages with acceptable I_{ON}/I_{OFF} ratios. The value of sub-threshold slope can be made smaller by using a thinner oxide layer or a lower substrate doping concentration.

4.3.2 Drain Induced Barrier Lowering (DIBL)

In long channel devices, the source and drain junctions are separated far apart and their depletion regions do not interact with each other. For these devices, the threshold voltage is independent of the channel length and drain bias voltage. In short channel devices, the source and drain depletion widths are closer and interact with each other to lower the source potential barrier. Under 'OFF' condition, the potential barrier between the drain and source prevents electrons from flowing. The barrier of a short channel device reduces with an increase in drain voltage, which in turn increases the sub-threshold leakage current due to lower threshold voltage.

In short channel devices the threshold voltage is influenced by the drain voltage and this effect is called Drain Induced Barrier Lowering (DIBL). The effect of DIBL is more pronounced at higher drain voltages and shorter channel lengths. DIBL does not change the sub-threshold slope S, but lowers the threshold voltage. Higher surface and channel

doping and shallow source/drain junction depths are found to reduce the DIBL effect on sub-threshold leakage current.

4.3.3 Gate Induced Drain Leakage (GIDL)

Gate Induced drain Leakage (GIDL) is due to high field effects in the drain junction of MOSFET's. When the gate is biased in accumulation mode, there is an accumulation of holes at the surface and the surface behaves like a P-type region more heavily doped than the substrate. As a result, the depletion layer is much narrower at the surface. This narrowing of the depletion layer at or near the surface causes an increase in local electric field. When the gate is biased at zero or negative and the drain is biased at V_{DD} , GIDL occurs and generates minority carriers in the drain region from surface traps or band-to-band tunneling. This effect is localized along the channel width between the gate and drain. Since the substrate is at a lower potential, the minority carriers that have been accumulated at the drain depletion region underneath the gate are swept to the substrate, creating a low resistance path for current to flow. It is found that thinner gate oxide t_{ox} and higher V_{DD} enhances the effect of GIDL.

4.3.4 Punchthrough

Punchthrough occurs when the drain and source junction depletion regions touch each other. An increase in reverse bias across the junction with increase in V_{DS} pushes the source and drain depletion regions closer to each other. When the channel length and reverse bias are at the right combination, punchthrough occurs. A way of preventing punchthrough is to use a V_{th} adjust implant to have a higher doping at the surface than in

the substrate. This causes a greater expansion of the depletion region below the surface as compared to the surface. When the drain voltage increases beyond the value required for punchthrough, the potential barrier for majority carriers in the source is lowered. This results in the carriers moving towards the drain crossing the energy barrier. The net effect is an increase in sub-threshold leakage current. Punchthrough degrades the sub-threshold slope S . Punchthrough is controlled by the use of higher doping and halo implants at the source and drain junctions.

4.3.5 Gate Oxide Tunneling Current

The reduction of the gate oxide thickness results in an increase in electric field across the oxide. The high electric field coupled with the low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substarte through the gate oxide, resulting in gate oxide tunneling current. As the oxide thickness is small, the electrons at the strongly inverted surface can tunnel into or through the oxide layer and give rise to gate current. If a negative gate bias is applied, electrons from the polysilicon can tunnel into or through the oxide layer and give rise to gate current.

The gate breakdown voltages were measured for the Regular threshold voltage PMOS and NMOS transistors with geometries of (W/L) = 50um/50um at 275^{o}C and are graphically illustrated in Figure 4.4 and 4.5 for the PMOS nd NMOS respectively. The gate breakdown voltages for the regular PMOS and NMOS were found to be -8.6V and 8.5V respectively at a temperature of 275^{o}C.

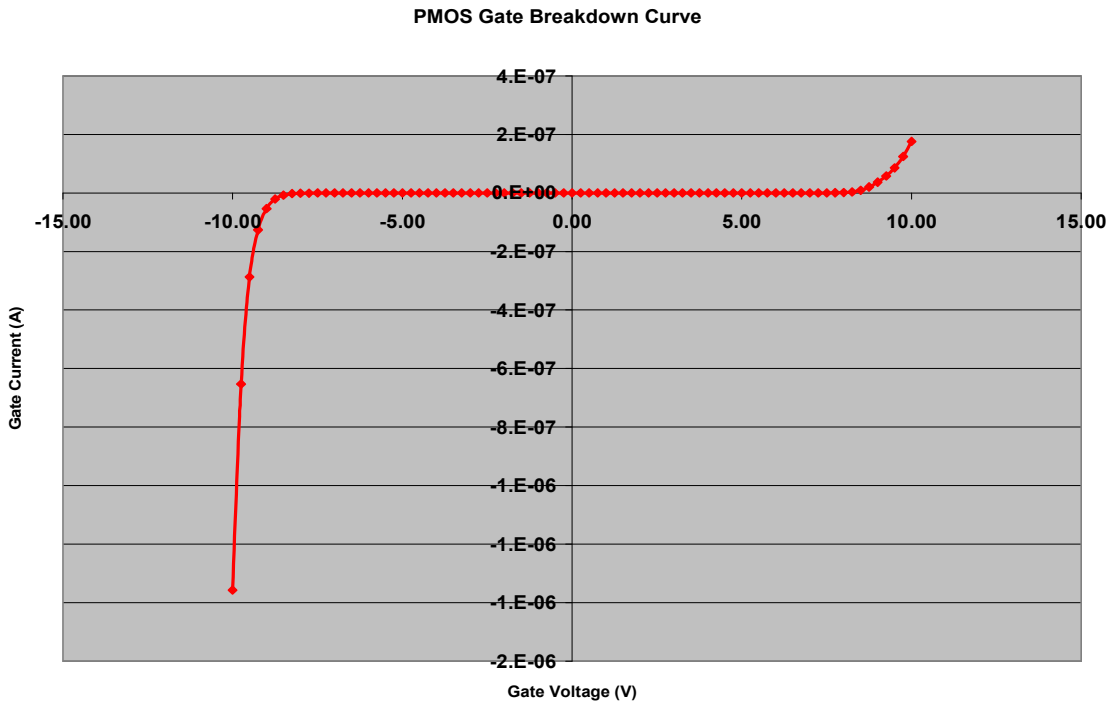


Figure 4.4 Gate breakdown voltage of Regular PMOS (W/L) = 50um/50um at 275^{o}C.

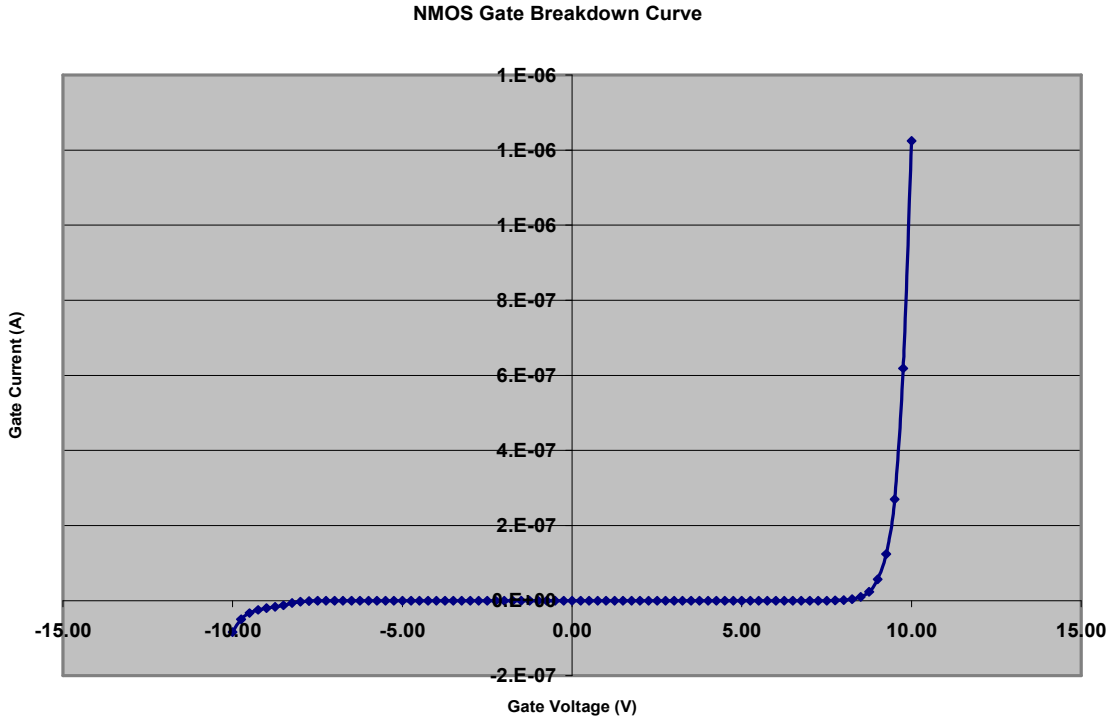


Figure 4.5 Gate breakdown voltage of Regular NMOS (W/L) = 50um/50um at 275^{o}C.

4.4 Leakage Reduction Techniques

The leakage power of a CMOS circuit is expressed by the following equation[19]:

$$P_{LEAK} = I_{LEAK} \ . \ V_{dd} \tag{4.4}$$

where I_{LEAK} is the total leakage current due to various leakage mechanisms and V_{dd} is the supply voltage. Due to the reduction of threshold voltage along with supply voltage scaling in order to achieve high performance, the sub-threshold leakage current increases. Leakage power becomes a significant component of the total power consumption in both active and standby modes of operation. Leakage reduction can be achieved using both process and circuit level techniques. Some examples of process level leakage reduction techniques include controlling the various parameters such as length of the transistor, the oxide thickness, junction depth and doping profile. At the circuit level, leakage current and threshold voltage are mainly controlled by the voltages at different terminals of the MOSFET such as gate, drain and source. Some of the circuit level leakage reduction techniques have been described in the following sections.

4.4.1 Leakage Control using Transistor Stacks

Stacking of transistors is found to reduce the subthreshold leakage current considerably. When there is more than one 'OFF' device in a transistor stack, the subthreshold leakage current flowing through this series connection of two transistors is reduced considerably. This effect is called 'stacking effect'. The two series connected 'OFF' transistors have lower leakage currents compared to a single 'OFF' transistor due to self-reverse biasing. This is because the internal node between the two transistors causes the upper transistor to have a negative value of V_{GS} and the lower transistor has a lower V_{DS} compared to a

single ‘OFF’ transistor. In the absence of two transistors which are stacked, the single ‘OFF’ transistor will have a V_{DS} equal to V_{DD} . It has been found that the standby leakage current reduces by a factor of two for a 32-bit static CMOS adder in low threshold 0.1um technology with supply voltages below 1V [20]. The principle of stacked transistors will be presented in detail in the following chapter.

4.4.2 Multiple V_{th} Transistor Designs

CMOS processes which offer two types of transistors – high-threshold and low-threshold voltage transistors on the same chip can be used for leakage control. The high-threshold voltage transistors can be used to reduce the sub-threshold leakage current while the low-threshold voltage transistors are used to achieve high performance. Figure 4.6 illustrates a Multiple threshold voltage CMOS circuit with sleep transistors.

In this circuit, sleep control PMOS and NMOS transistors (High V_{th} transistors) are added along the power and ground rails. When the circuit is in active mode of operation, the sleep control signal SL is set to low and this turns on the High V_{th} PMOS and NMOS ON. The virtual power and ground rails VDDV and VSSV act as real power and ground lines. In standby mode of operation, SL is set to high and this turns off the sleep control transistors MN and MP. As a result of this, the circuit is isolated from the actual power and ground rails and there is no leakage path. Hence leakage currents are low in the standby mode of operation. However, this scheme can only be used for standby leakage power reduction and has certain disadvantages like increased area and delay because of the added sleep transistors.

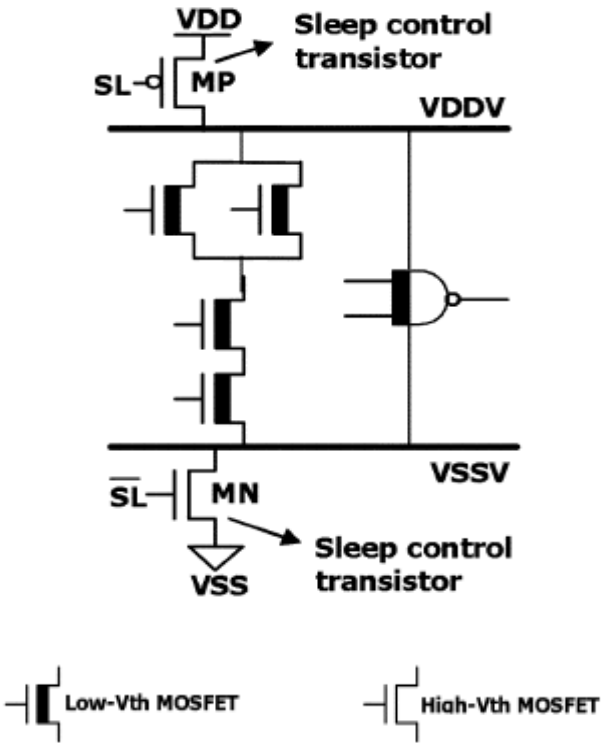


Figure 4.6 Multiple Threshold Voltage CMOS circuit with Sleep transistors inserted[21].

Multiple threshold voltage transistors can be obtained by adjusting the channel doping densities, multiple oxide thicknesses and multiple channel lengths. The threshold voltage can be varied by varying the thickness of the gate oxide for different transistors. A thicker gate oxide results in high threshold voltage transistors and a thinner oxide results in low threshold voltage transistors. A thicker oxide is preferred for reducing the sub-threshold leakage currents, gate oxide tunneling currents and reducing the dynamic power consumption by reducing the value of gate capacitance. Different threshold voltage transistors can be realised using different channel lengths for transistors. The threshold voltage reduces as the channel length decreases[22].

4.4.3 Dual Threshold Voltage Circuits

Circuits can employ the dual threshold voltage scheme to reduce leakage in which a detailed analysis of critical and non-critical paths is needed. In this scheme, high threshold voltage transistors are used in non-critical paths of the ciruit to reduce the leakage currents and low threshold voltage transistors are used in the critical paths to achieve high performance[23]. This scheme has the advantage that no additional sleep transistors are needed and high performance and low power designs can be realised easily without any area overhead. This technique can be used to reduce leakage power in active and standby modes of operation.

4.4.4 Dynamic Threshold CMOS

An alternative to the multiple threshold voltage technique is the dynamic control of transistor threshold voltage by tying together the gate and the floating body of a SOI MOSFET. The threshold voltage is dynamically controlled by the state of the circuit. If the circuit is in active mode of operation, the gate-body bias is maintained at a small value of around 0.6V to lower the threshold voltage for higher drive currents. On the other hand if the circuit is in standby mode of operation, the threshold voltage is made high which results in lower sub-threshold leakage currents.

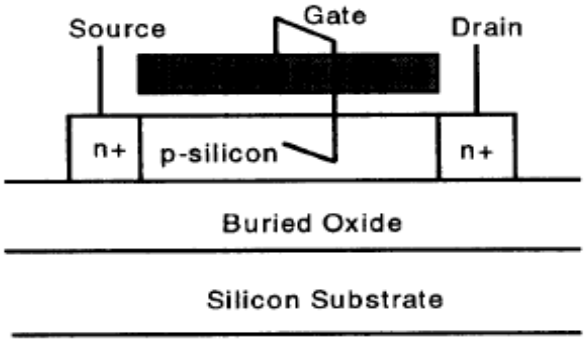


Figure 4.7 Structure of SOI DTMOS with gate and body tied together[24].

CHAPTER 5

STACKED TRANSISTORS

5.1 Introduction

In Chapter 4 various leakage current mechanisms and some circuit level techniques to control the leakage was discussed. In this chapter the method of stacked transistors to control leakage is presented in detail. The leakage current of transistors increases with increasing temperatures. It has been found that in the Peregrine Semiconductor's 0.5um SOS process, the PMOS device leaks less than the NMOS device. Hence some form of leakage control is necessary for the NMOS transistors in order to achieve good I_{ON}/I_{OFF} ratios.

The I_{ON}/I_{OFF} ratio is a figure of merit for digital circuits and is defined as the ratio of the 'ON' current to the 'OFF' current of the transistor. The 'ON' current is the current flowing through the transistor when the transistor is fully 'ON' and the circuit is functional. The current flowing through the transistor when $V_{GS} = 0$ is defined as the OFF current. The 'OFF' current is also called the leakage current which flows through the transistor when no inputs are applied to the circuit and the circuit is in a standby mode of operation. Ideally the 'OFF' current should be zero or a small value in the range of

picoampere/um of gate width. A higher value of I_{ON}/I_{OFF} ratio is always preferred and is needed for proper functionality of the circuit and to distinguish between the ON and OFF states of the transistor.

5.2 Leakage Performance of Regular PMOS and NMOS Transistors

The I_{ON}/I_{OFF} ratios of regular threshold voltage PMOS and NMOS transistors were measured for lengths of 1.6um at a power supply of 5V over temperatures ranging from 200^{O}C to 275^{O}C. The values are presented in Table 5.1 and the graphs showing the variation of the I_{ON}/I_{OFF} ratios for the Regular PMOS and NMOS are illustrated in Figure 5.1 and 5.2 respectively.

TEMPERATURE	**200^{O}C**	**225^{O}C**	**250^{O}C**	**275^{O}C**
PMOS	23,220	8527	3645	1625
NMOS	313	301	139	93

Table 5.1 I_{ON}/I_{OFF} ratios of regular threshold voltage PMOS and NMOS transistors with (W/L) =2um/1.6um and 5V Power supply.

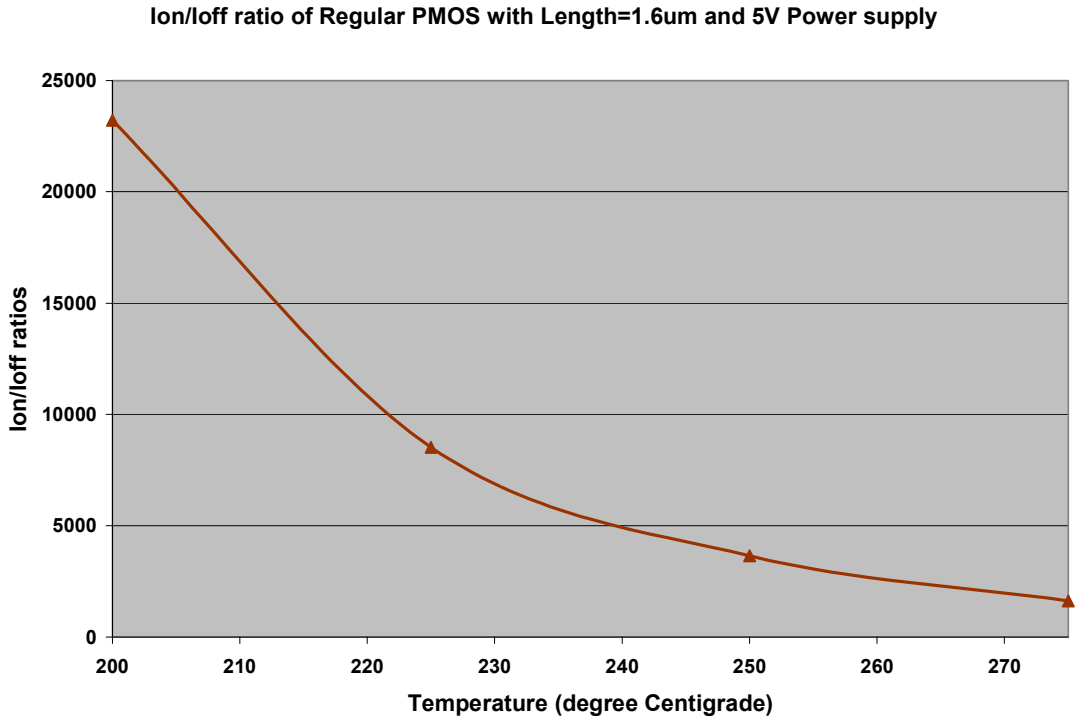


Figure 5.1 I_{ON}/I_{OFF} ratios of Regular PMOS with (W/L) =2um/1.6um and 5V supply.

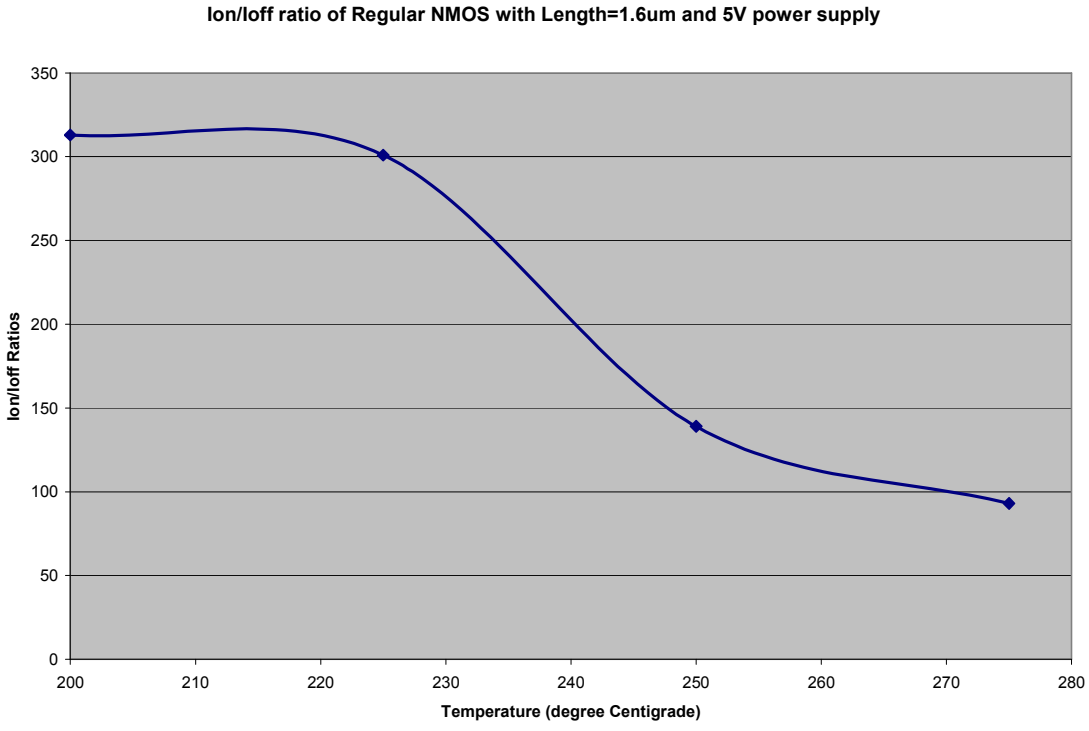


Figure 5.2 I_{ON}/I_{OFF} ratios of Regular NMOS with (W/L) =2um/1.6um and 5V supply.

The leakage performance of regular threshold voltage NMOS with a length of 1.3um was measured at a power supply of 3.3V over a temperature range of 200^{O}C – 275^{O}C. The I_{ON} /I_{OFF} ratios are presented in Table 5.2. Figure 5.3 illustrates the graph showing the variation of I_{ON}/I_{OFF} ratios for the regular NMOS transistor.

TEMPERATURE	**200^{O}C**	**225^{O}C**	**250^{O}C**	**275^{O}C**
NMOS	238	76	50	44

Table 5.2 I_{ON}/I_{OFF} ratios of regular threshold voltage NMOS transistor with (W/L)=2um/1.3um and 3.3V Power supply.

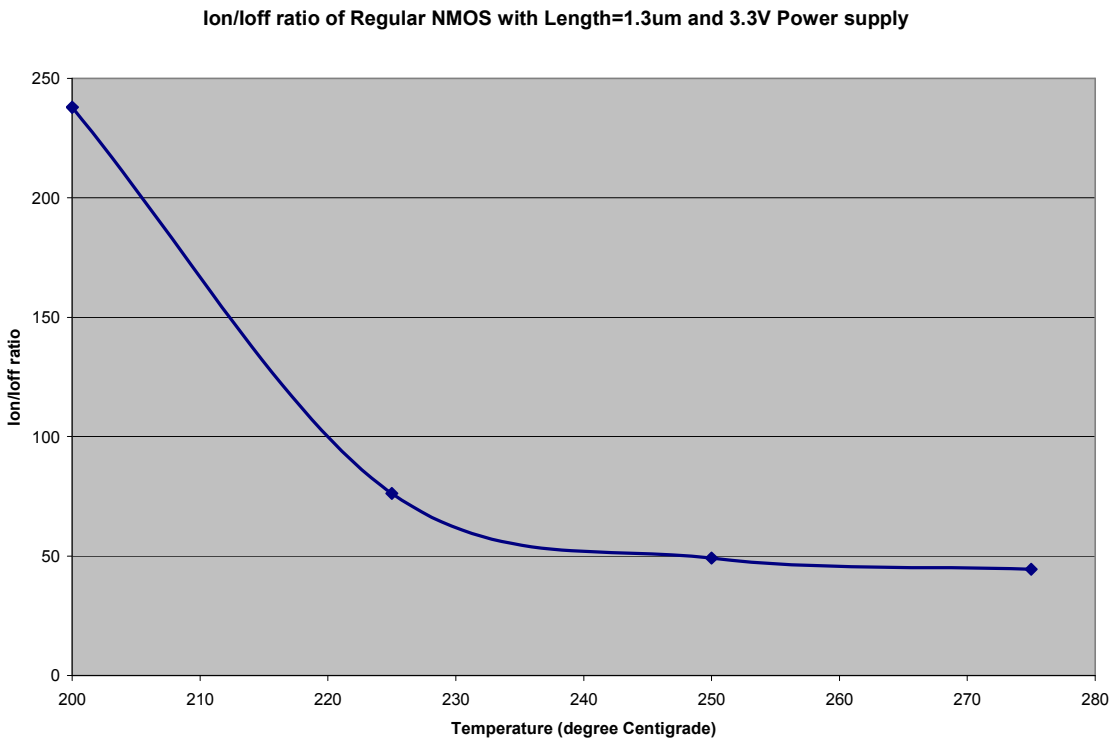


Figure 5.3 I_{ON}/I_{OFF} ratios of Regular NMOS with (W/L) =2um/1.3um and 3.3V power supply.

It can be seen from these values that the regular threshold voltage PMOS transistor has higher I_{ON}/I_{OFF} ratios and lesser leakage current when compared to the regular NMOS transistor in the Peregrine Semiconductor's 0.5um SOS process. The I_{ON}/I_{OFF} ratio for the NMOS is very poor with a value of 93 for a length of 1.6um and 44 for a length of 1.3um, which makes it difficult to distinguish between the 'ON' and 'OFF' states of the circuit. Leakage current is worse in the regular NMOS than the regular PMOS and degrades the I_{ON}/I_{OFF} ratios. This results in the standard logic standby currents also being excessive. This inhibits the acceptability of operation of the circuits at extreme temperatures exceeding 200^{O}C. In order to build efficient and robust circuits that can perform efficiently and reliably at these extreme temperatures, some form of leakage control is necessary for the NMOS transistors. The method of transistor stacking is a highly efficient leakage control mechanism which is described in detail in the next section.

5.3 Stacked NMOS Transistors

In case of extreme temperature circuits, the threshold voltage degrades as temperature rises. As the threshold voltage keeps decreasing, the 'OFF' current increases resulting in poor I_{ON}/I_{OFF} ratios. Figure 5.4 illustrates the effect of degradation in threshold voltage V_{th}.

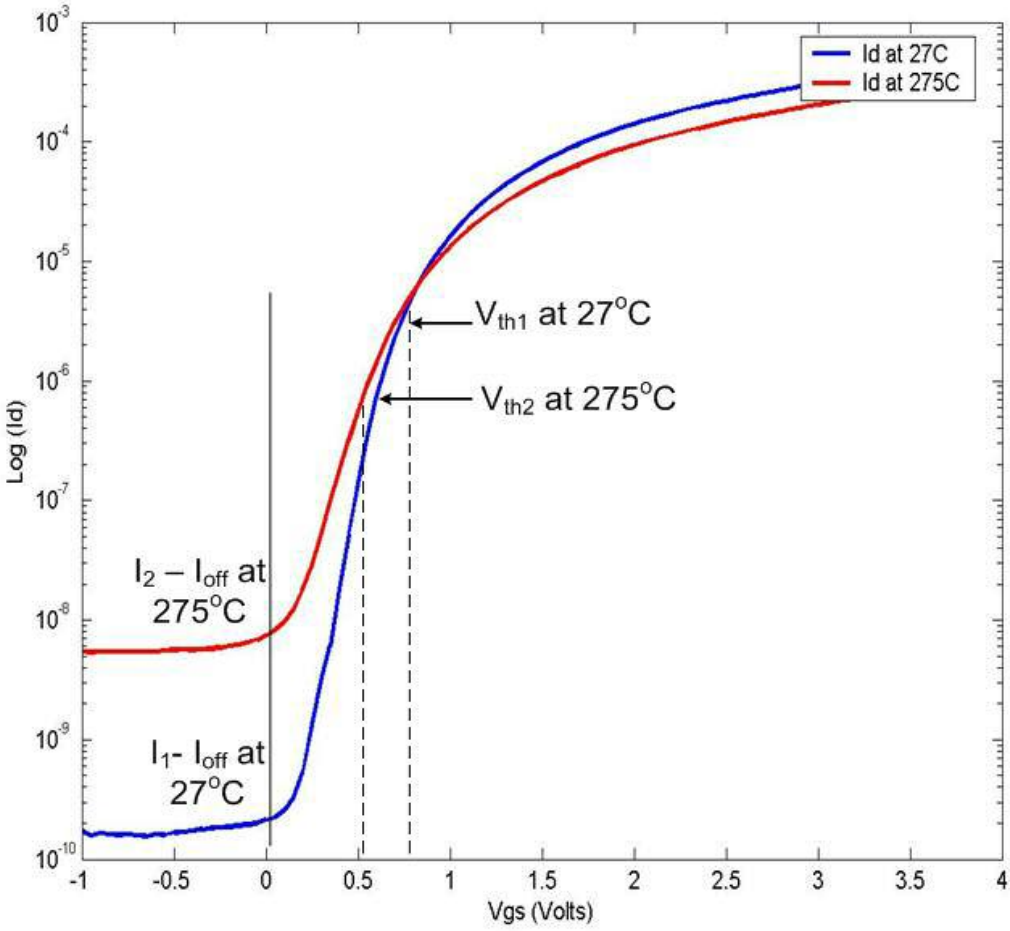


Figure 5.4 Increase in 'OFF' current due to degradation in threshold voltage V_{th} for stacked NMOS with (W/L) = 2um/1.3um at 3.3V.

In Figure 5.4 we can see that as the threshold voltage V_{th} degrades from V_{th1} to V_{th2} due to increase in temperature and the 'OFF' current or the leakage current increases from I_1 to I_2. In order to maintain the leakage current at the same value of I_1 as the threshold voltage degrades to V_{th2}, we need to reverse bias the gate to source voltage. This effective reverse bias on the gate to source voltage will substantially reduce the sub-threshold leakage

current flowing through the transistor. This reverse bias can be achieved through the method of stacked transistors.

In the Stacked transistor principle developed and presented here, the regular NMOS transistor is replaced with a stacked transistor pair which is a low threshold voltage NMOS (NL) transistor placed over a regular threshold voltage NMOS (RN) transistor. Figure 5.5 illustrates the regular NMOS transistor and the stacked NMOS transistor.

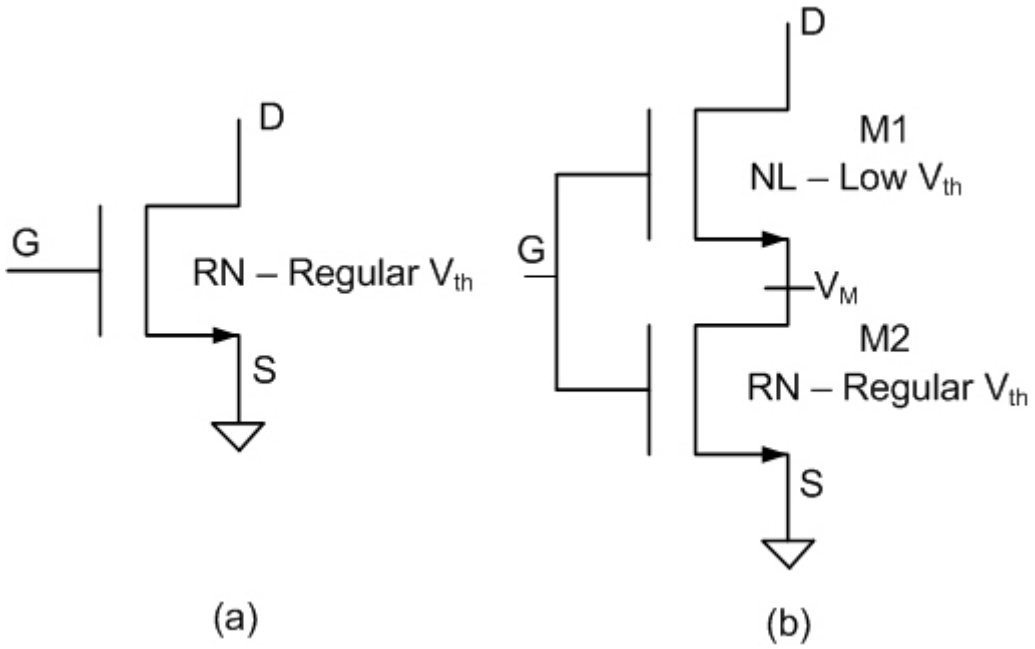


Figure 5.5 (a) Regular NMOS transistor and (b) stacked NMOS transistor.

Consider the transistor stack illustrated in Figure 5.5, in which we tie the gate inputs of the NL and RN transistor together and consider the gate input to be common to both transistors. Consider the case when the gate input is '0' or low, now both the transistors are turned off in the stack. We can observe that the intermediate node "V_M" between the two transistors is positive. The positive voltage "V_M" at this node has some advantages.

1. When the input gate voltage is low, the positive source voltage V_M of the NL device causes the gate to source voltage V_{GS1} of the NL transistor M1 to be negative, which causes a reverse bias at the gate to source junction of M1. This reverse bias effect limits the sub threshold leakage current that flows through transistor M1. This effect is also known as "self-reverse biasing" [25].
2. The positive node voltage V_M decreases the drain to source voltage V_{DS1} of transistor M1. As the drain to source voltage of M1 decreases, this results in an increase in the threshold voltage due to lesser DIBL effect. The effect of DIBL is more pronounced at higher drain voltages and therefore a reduction in drain voltage of the NL transistor limits the effects of DIBL and prevents the lowering of the threshold voltage. Hence the sub-threshold leakage current decreases substantially.
3. The drain to source voltage of regular threshold voltage transistor M2 in the stacked device is a small value V_M as compared to the voltage drop of VDD in a regular NMOS transistor without stacking. This small voltage drop across the stacked device further helps in limiting the flow of leakage current due to both the reduction of DIBL and the lower V_{DS}.

The regular NMOS transistor and the stacked NMOS transistor were simulated to determine the voltage drops across the intermediate node V_M for a VDD of 3.3V and these voltage drops are illustrated in Figure 5.6.

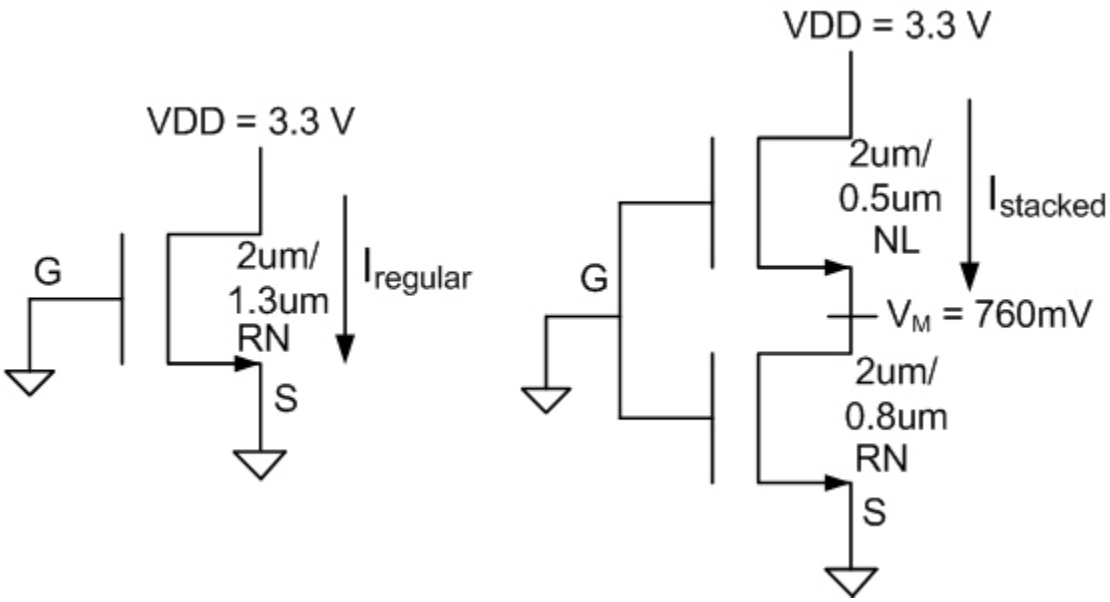


Figure 5.6 Leakage currents and voltage drop in (a) Regular NMOS transistor and (b) Stacked NMOS transistor.

The regular NMOS transistor, RN had geometry of W/L = 2um/1.3um and the stacked NMOS transistor had geometry of W/L=2um/0.8um for the RN device and W/L=2um/0.5um for the NL device. Both these devices were simulated at 150^{O}C to determine the voltage drops. The regular NMOS transistor had a voltage drop of 3.3V which is equal to the value of VDD. Whereas, in the case of the stacked NMOS device, the NL device had a V_{DS} of 2.54V and the RN device had a V_{DS} of 760mV. The intermediate node V_M had a positive voltage of 760mV. Due to this positive voltage at node V_M, the gate to source voltage V_{GS} of the NL transistor is reverse biased with a negative value of -760mV. This large negative value of VGS of the NL device is sufficient enough to limit the sub-threshold leakage current to a small value. $I_{regular}$ denotes the leakage current flowing through a regular NMOS transistor and $I_{stacked}$ denotes the leakage current flowing through a stacked NMOS transistor pair.

5.4 Leakage Performance of Stacked Transistors

The leakage performance of stacked transistors was studied for two different lengths of transistors at two different supply voltages of **3.3V** and **5V**. The first stacked device has geometry of **(W/L)=2um/0.8um** for the **RN** device and **(W/L)=2um/0.5um** for the **NL** device. The threshold voltage of the regular NMOS transistor, **RN** equals **0.755 V** and that for the low threshold NMOS, **NL** equals **0.235 V**. Figure 5.7 illustrates the 1.3um length Stacked NMOS device. This device was tested on silicon to measure the leakage performance at a supply voltage of 3.3V with temperature ranging from 200^{O}C to 275^{O}C. The 'ON' current was measured by setting the drain to source voltage V_{DS} = 50mV and the 'OFF' current was measured by setting the value of V_{DS} = 3.6V, while sweeping the gate to source voltage V_{GS} from -1V to 3.6V in both cases. The 'ON' current is the current measured at V_{GS}=3.6V when V_{DS}=50mV. The 'OFF' current is the current measured at V_{GS}=0V when V_{DS}=3.6V. The value of I_{ON}/I_{OFF} ratios for the 1.3um length stacked transistor is presented in Table 5.3 for a set of dies.

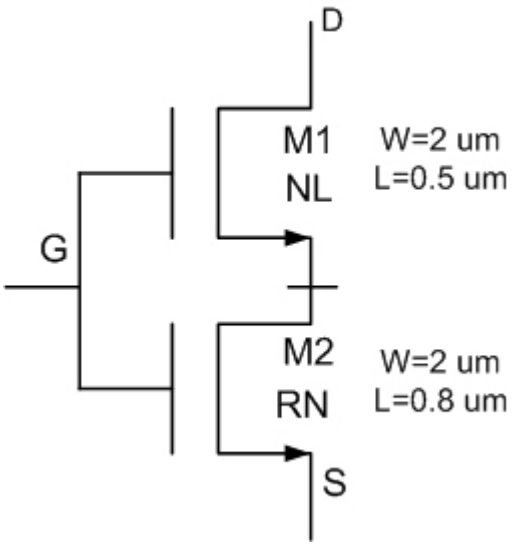


Figure 5.7 Schematic of stacked NMOS transistor with Length of 1.3um.

TEMPERATURE	200^{O}C	225^{O}C	250^{O}C	275^{O}C
DIE 1	3,408	2,566	1,476	984
DIE 2	2314	1707	1021	845
DIE 3	1,727	1,117	721	435
DIE 4	1,566	863	509	389
DIE 5	6,877	4,250	2,704	1,819
DIE 6	1,083	738	474	320
DIE 7	2,367	1,465	874	622
DIE 8	3034	1,830	1,169	821
DIE 9	1,953	1,190	948	647
DIE 10	15,058	9183	8171	2,904
DIE 11	46,926	28,183	28,138	9,956
DIE 12	605	448	399	272
DIE 13	230	187	143	109

DIE 14	178,051	89708	61051	27,846
DIE 15	110	85	73	58
DIE 16	91,306	57,511	38,546	17,243
DIE 17	411	292	222	179
DIE 18	196	169	120	102

Table 5.3 I_{ON}/I_{OFF} ratios of (W/L) =2um/1.3um stacked NMOS transistor at supply voltage of 3.3V.

The variation of I_{ON}/I_{OFF} ratios with temperature ranging from 200^{O}C to 275^{O}C is graphically illustrated in Figure 5.8 and the error bar plot of the I_{ON}/I_{OFF} ratios at 275^{O}C for 95% confidence level is presented in Figure 5.9.

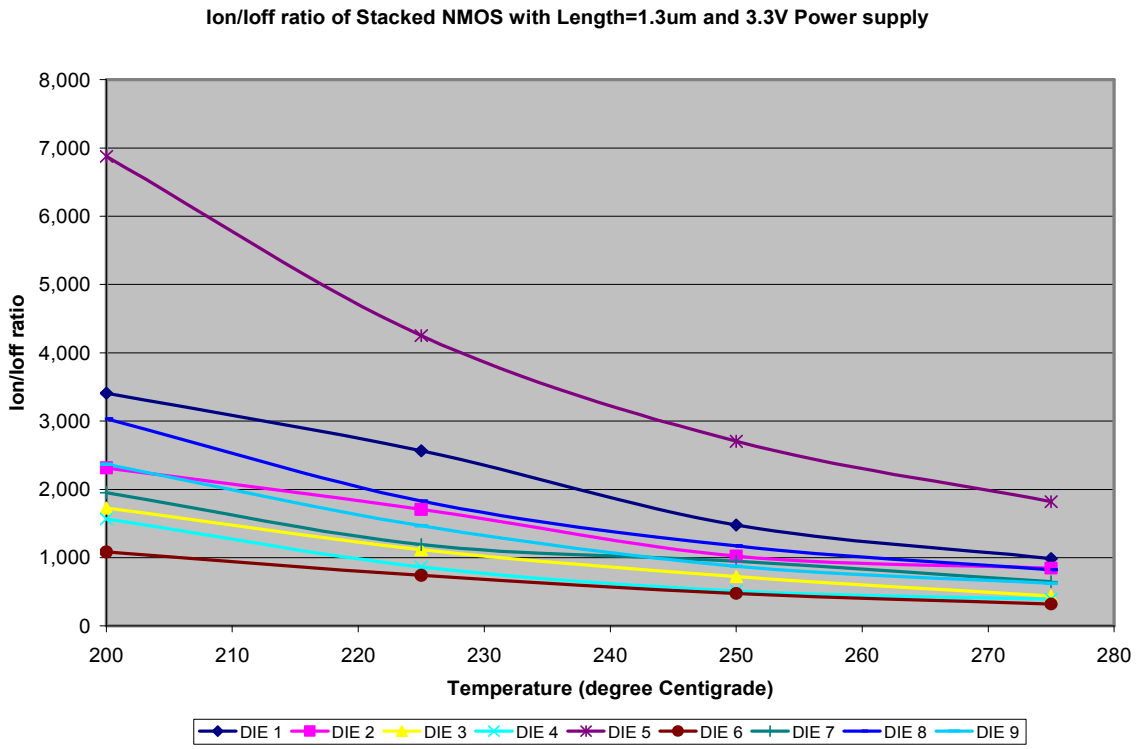


Figure 5.8 Variation of I_{ON}/I_{OFF} ratios with temperature for (W/L) =2um/1.3um stacked NMOS transistor and power supply of 3.3V.

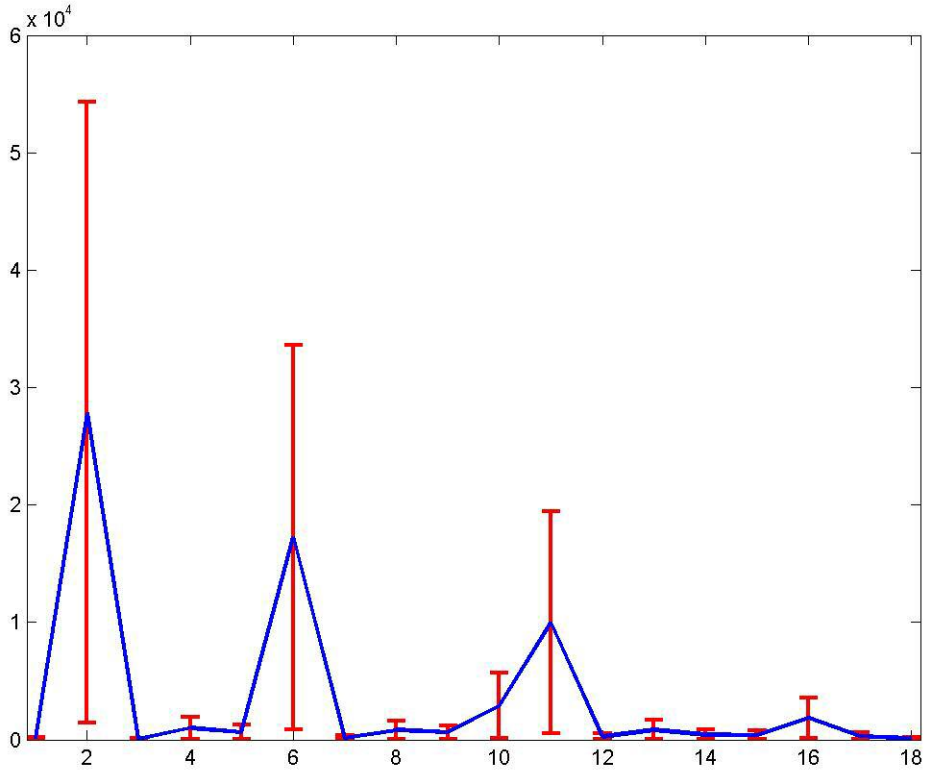


Figure 5.9 Error bar plot of (W/L) =2um/1.3um stacked NMOS transistor at 275^{O}C for 95% confidence levels for a set of dies as given in Table 5.3.

The second stacked device has geometry of **(W/L)=2um/0.8um** for the **RN** device and **(W/L)=2um/0.8um** for the **NL** device. Figure 5.10 illustrates the 1.6um length Stacked NMOS device. This device was tested on silicon to measure the leakage performance at a supply voltage of 5V with temperatures ranging from 200^{O}C to 275^{O}C. The 'ON' current was measured by setting the drain to source voltage V_{DS} = 50mV and the 'OFF' current was measured by setting the value of V_{DS} =5.5V while sweeping the gate to source voltage V_{GS} from -1V to 5.5V in both cases. The 'ON' current is the current measured at V_{GS}=5.5V when V_{DS}=50mV. The 'OFF' current is the current measured at V_{GS}=0V and

when V_{DS}=5.5V. The value of I_{ON} /I_{OFF} ratios for the 1.6um length stacked transistor is presented in Table 5.4 for a set of dies.

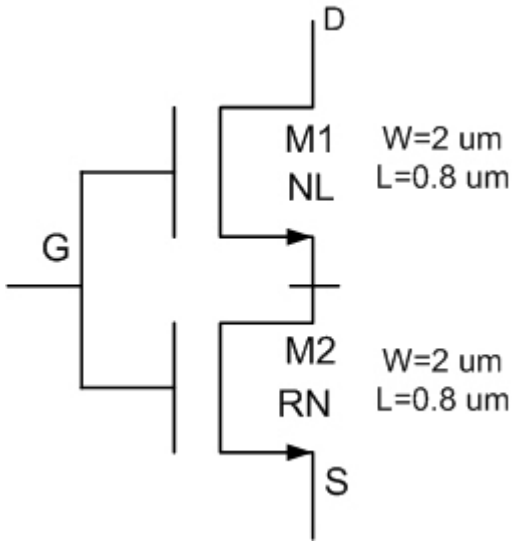


Figure 5.10 Schematic of stacked NMOS transistors with Length of 1.6um.

TEMPERATURE	200^{O}C	225^{O}C	250^{O}C	275^{O}C
DIE 1	160000	96000	63,000	32,000
DIE 2	110000	75000	51,000	19,000
DIE 3	115000	57,496	39,778	17,369
DIE 4	145608	67,114	40,407	22,584
DIE 5	4000	2500	1700	1100
DIE 6	1500	1090	955	715
DIE 7	138	106	91	69
DIE 8	102	88	75	64
DIE 9	2,112	1,114	776	724
DIE 10	1,708	938	540	387
DIE 11	559	351	681	551

DIE 12	764	395	275	254
DIE 13	1,726	1,403	838	665
DIE 14	1,214	727	560	345
DIE 15	695	550	397	288
DIE 16	485	307	203	158
DIE 17	412	243	169	122
DIE 18	702	455	350	256
DIE 19	1,654	1,178	1,156	632
DIE 20	40	35	31	26

Table 5.4 I_{ON}/I_{OFF} ratios of (W/L) =2um/1.6um stacked NMOS transistor at supply voltage of 5V.

The variation of I_{ON}/I_{OFF} ratios for the 1.6um length stacked NMOS transistor with temperature ranging from 200^{O}C to 275^{O}C is graphically illustrated in Figure 5.11 and the error bar plot of the I_{ON}/I_{OFF} ratios at 275^{O}C for 95% confidence level is presented in Figure 5.12.

From the data of the I_{ON}/I_{OFF} ratios for the 1.3um and 1.6um stacked NMOS device, we can conclude that as a result of stacking there is an improvement of at least three orders of magnitude in I_{ON}/I_{OFF} ratios of stacked NMOS device compared to a regular NMOS device of same length. These high values of I_{ON}/I_{OFF} ratios at an extreme temperature of 275^{O}C enables the designer to build circuits for high temperature applications that would perform efficiently.

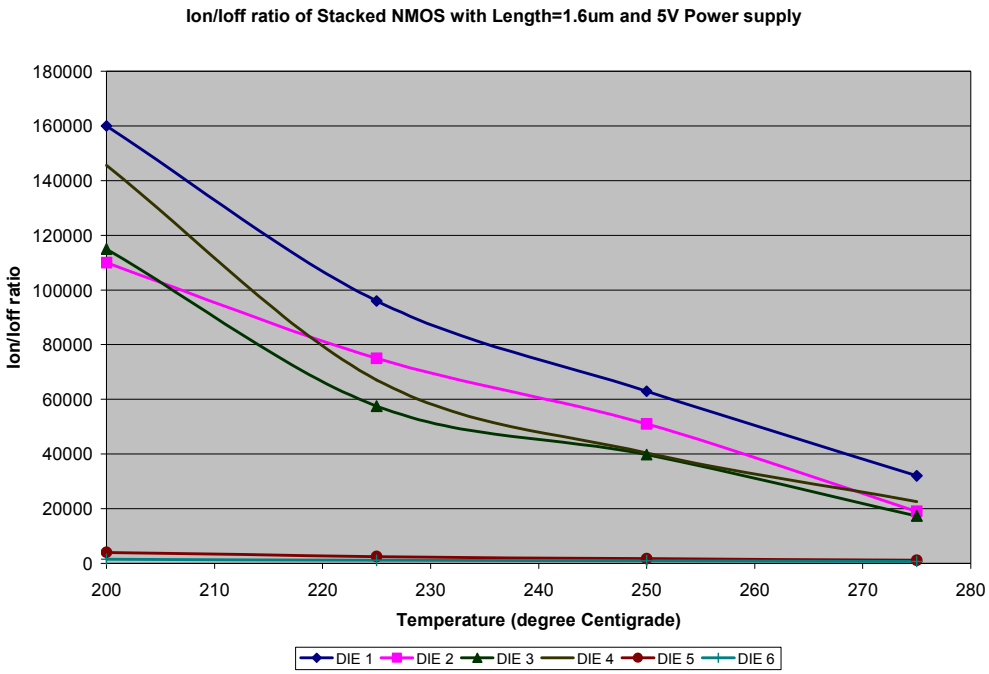


Figure 5.11 Variation of I_{ON}/I_{OFF} ratios with temperature for (W/L) =2um/1.6um stacked NMOS transistor and power supply of 5V.

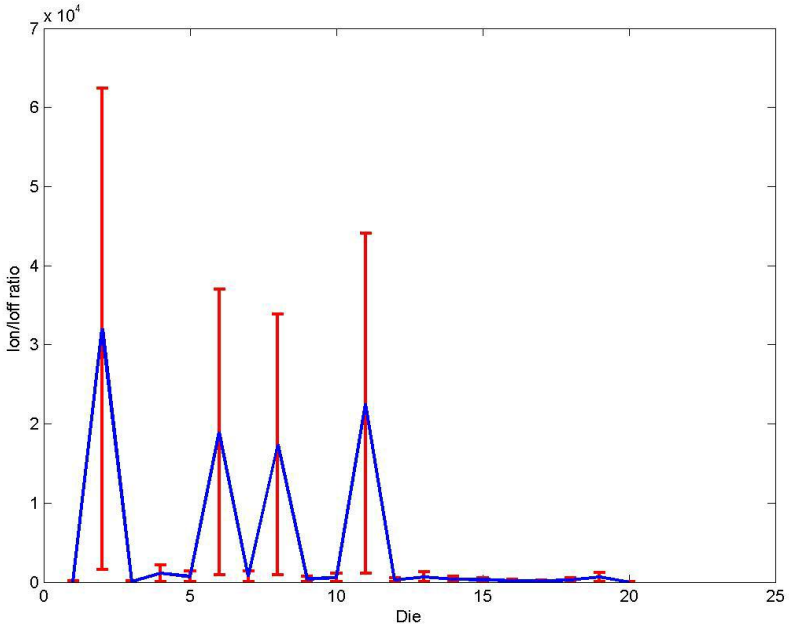


Figure 5.12 Error bar plot of (W/L) =2um/1.6um stacked NMOS transistor at 275^{O}C for 95% confidence levels for a set of dies as given in Table 5.4.

5.5 Performance of Stacked Combinational gates

In order to ensure the proper functionality of circuits using stacked transistors certain basic combinational logic gates like Inverter, 3-input NAND and 3-input NOR gates using stacked NMOS transistors were fabricated and tested. Figure 5.13 illustrates the schematics of these combinational gates. The voltage transfer characteristic (VTC) curves were measured for these three combinational gates at 3.3V and 5V power supply and compared with identically sized regular combinational gates for the same set of inputs switching at a temperature of 275^{O}C. The VTC curves for the Inverter, 3-input NOR gate and 3-input NAND gate are displayed in Figures 5.14-5.19.

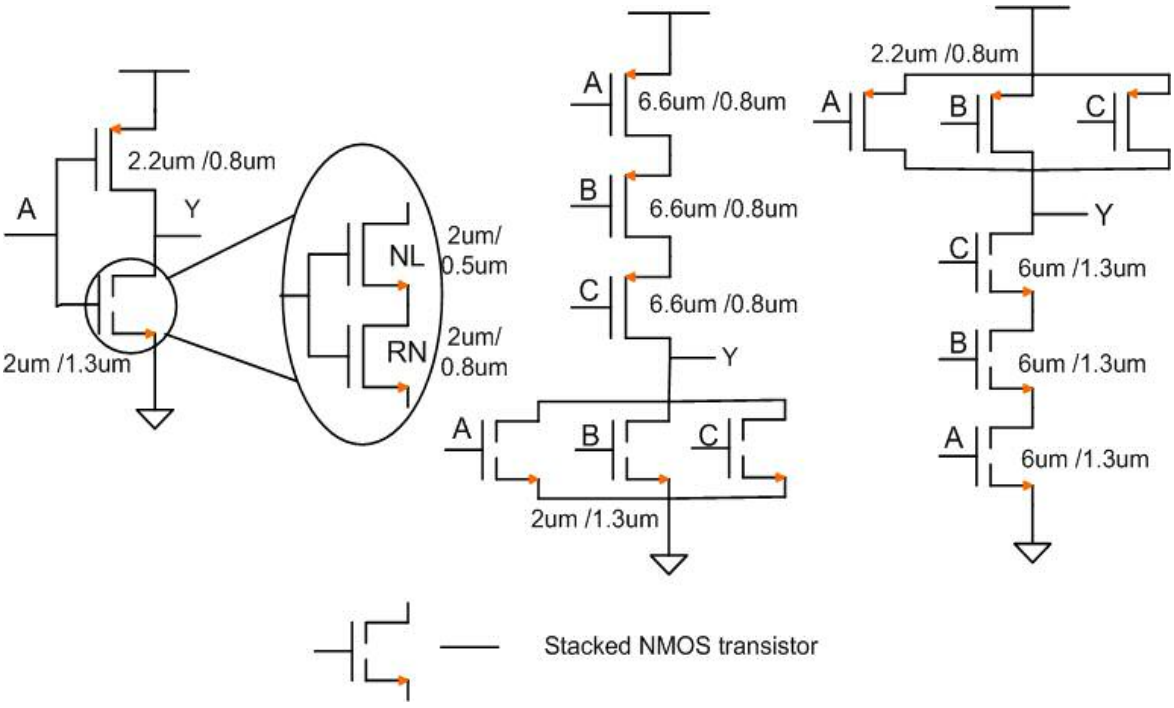


Figure 5.13 Schematics of (a) Stacked Inverter, (b) Stacked 3-input NOR gate and (c) Stacked 3-input NOR gate.

By observing the plots of the comparison of the VTC curves of the three stacked combinational gates, we see that there is a very little deviation in the switching threshold of these gates. The VTC curve of the stacked combinational gates closely follows the behavior of the regular combinational gates. Hence we can conclude that without much loss in performance the stacked combinational gates perform reliably at temperatures of $275^{O}C$.

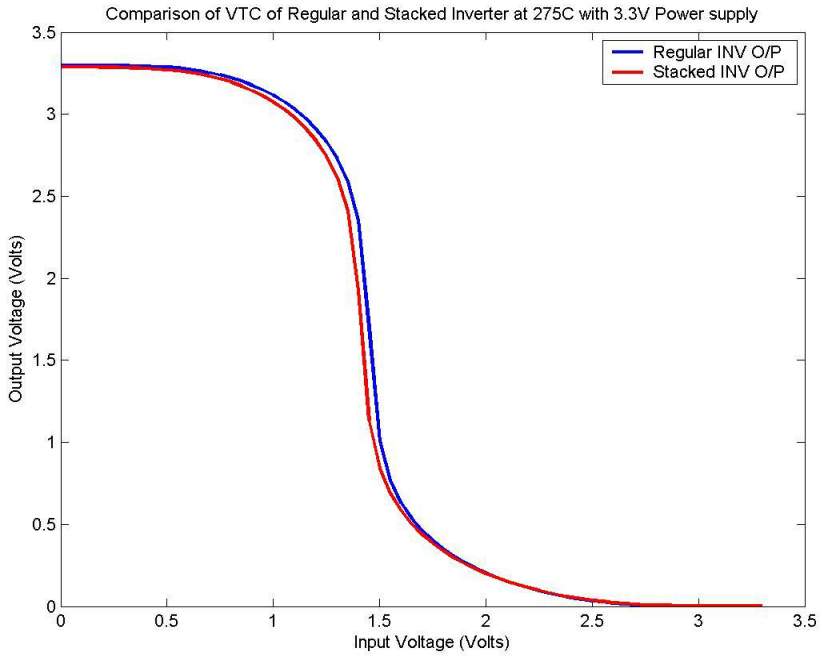


Figure 5.14 Comparison of VTC curve of Regular and Stacked Inverter at $275^{O}C$ with 3.3V power supply.

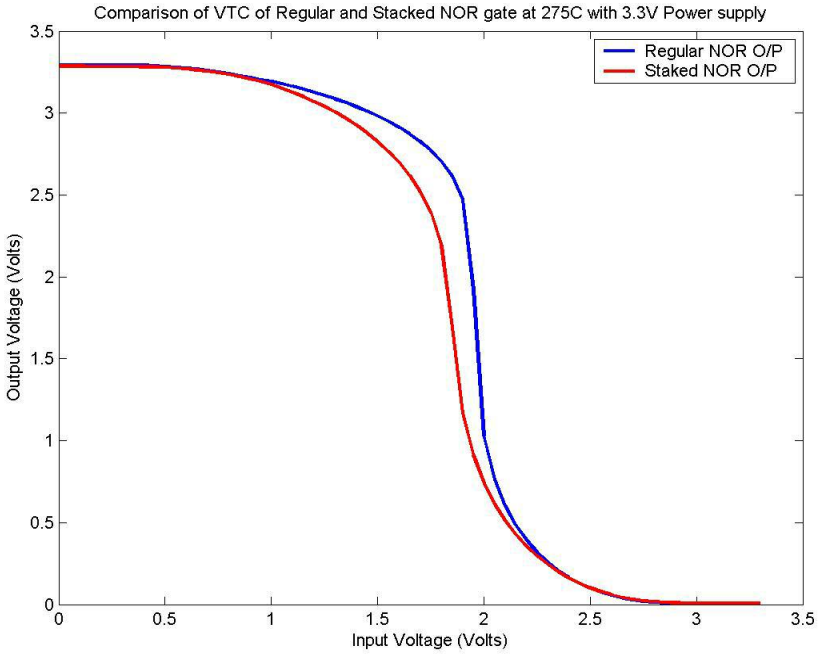


Figure 5.15 Comparison of VTC curve of Regular and Stacked 3-input NOR gate at 275^{O}C with 3.3V power supply.

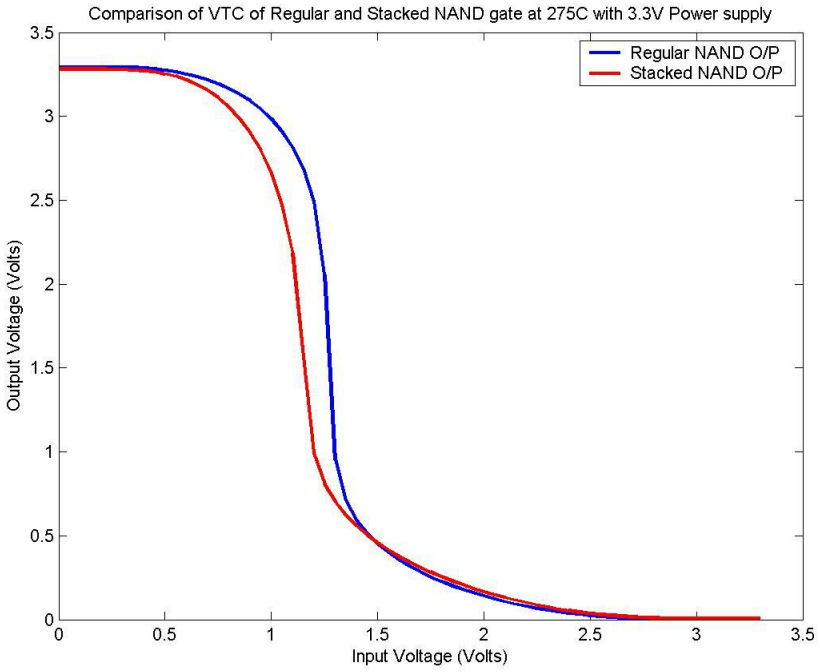


Figure 5.16 Comparison of VTC curve of Regular and Stacked 3-input NAND gate at 275^{O}C with 3.3V power supply.

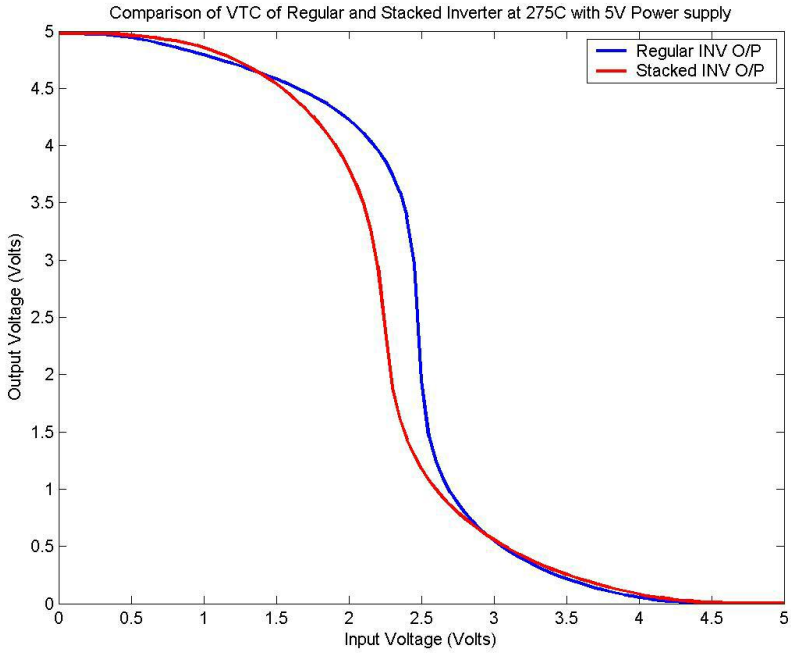


Figure 5.17 Comparison of VTC curve of Regular and Stacked Inverter at 275^{O}C with 5V power supply.

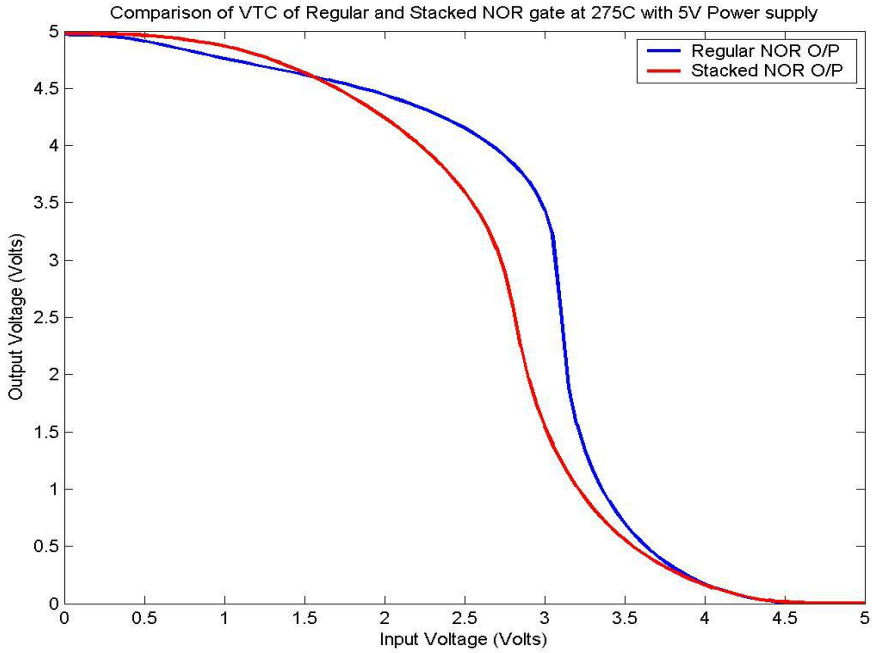


Figure 5.18 Comparison of VTC curve of Regular and Stacked 3-input NOR gate at 275^{O}C with 5V power supply.

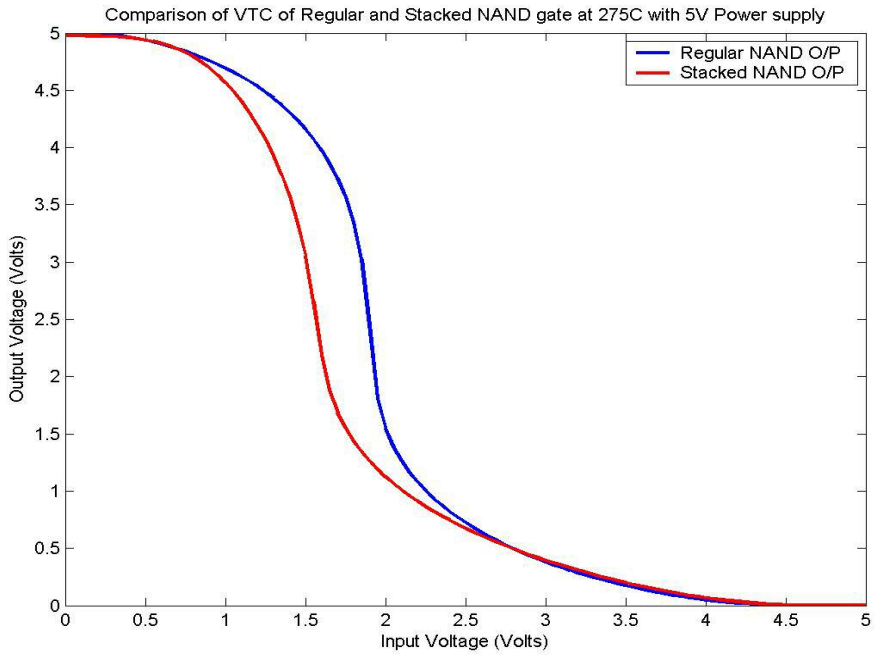
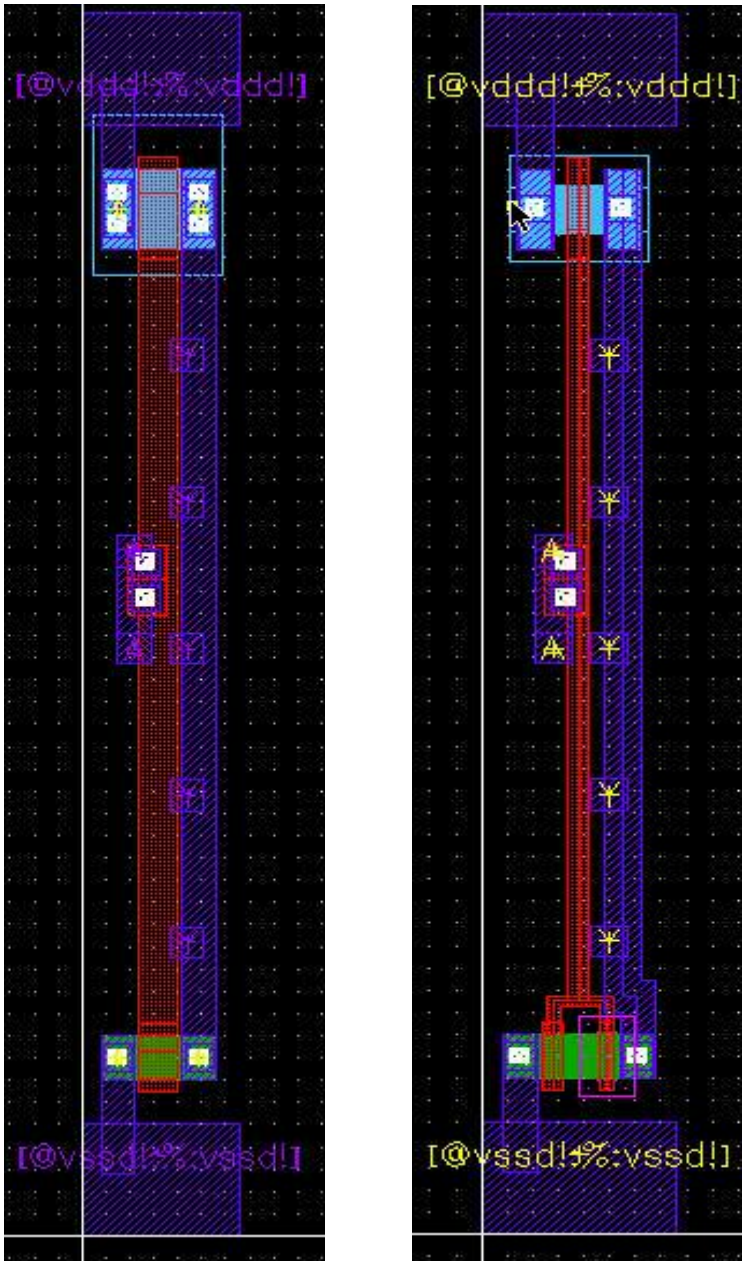


Figure 5.19 Comparison of VTC curve of Regular and Stacked 3-input NAND gate at 275^{O}C with 5V power supply.

The layouts of the standard cells of Inverter, 3-input NAND and 3-input NOR gate for regular and stacked NMOS transistors is illustrated in Figures 5.20-5.22. Table 5.5 lists the comparison of the areas of the standard cells with regular and stacked NMOS transistors and the percentage difference in the areas.

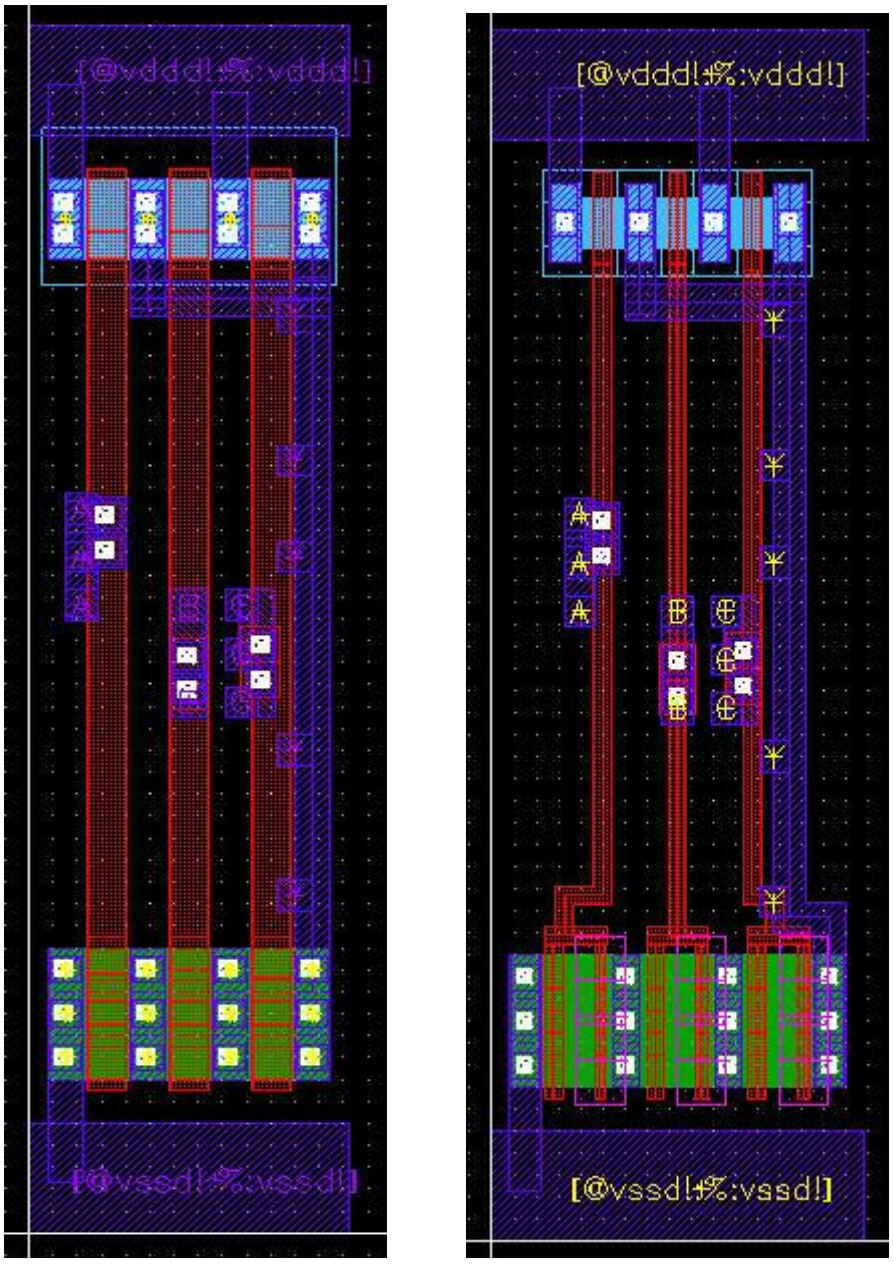
Type of Cell	Inverter	3-input NAND	3-input NOR
Area of Regular Cell	363um	726um	726um
Area of Stacked Cell	418um	924um	924 um
% Difference in Area	14%	24%	24%

Table 5.5 Comparison of areas of regular and stacked standard cells.



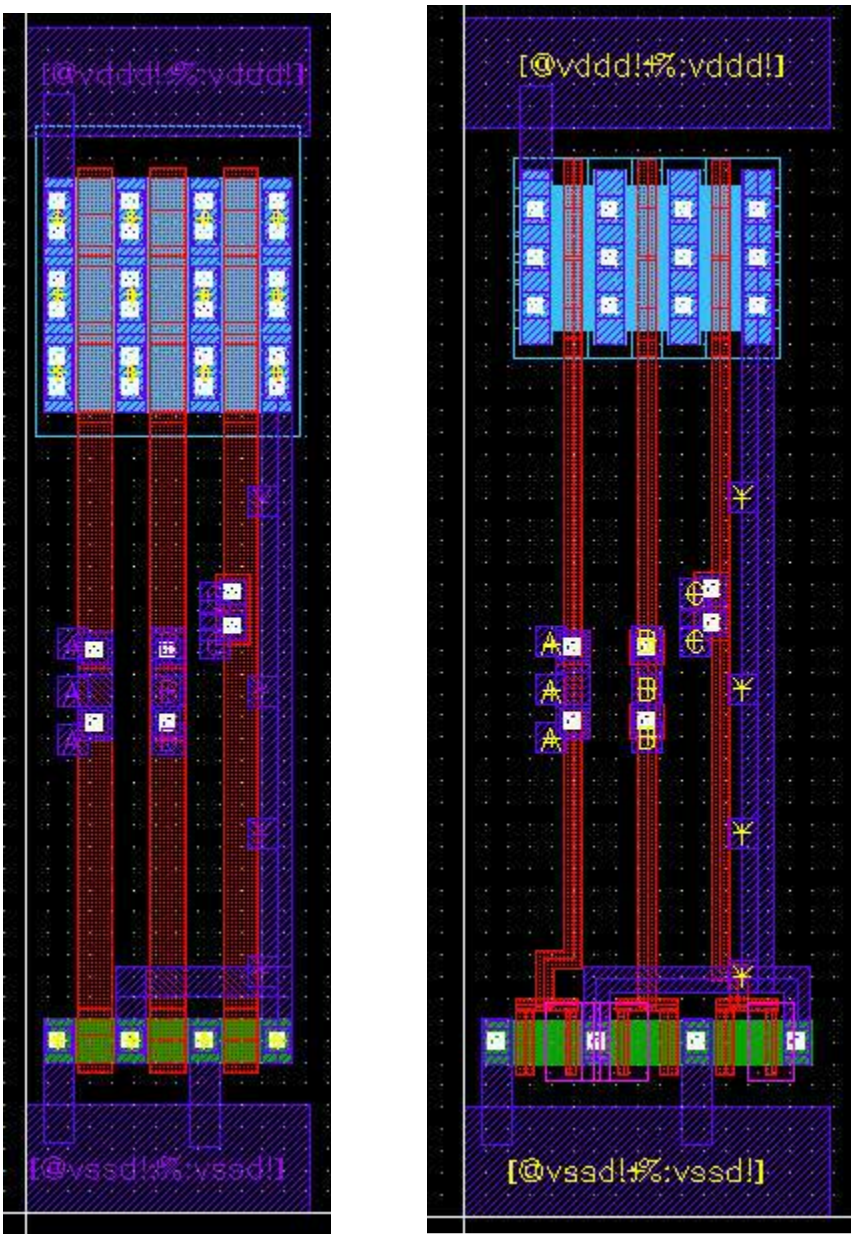
(a) (b)

Figure 5.20 Layouts of (a) Regular NMOS Inverter and (b) Stacked NMOS Inverter Standard Cell.



(a) (b)

Figure 5.21 Layouts of (a) Regular NMOS 3-input NAND and (b) Stacked NMOS 3-input NAND gate standard cell.



(a) (b)

Figure 5.22 Layouts of (a) Regular NMOS 3-input NOR and (b) Stacked NMOS 3-input NOR gate standard cell.

From the leakage data measured for the stacked transistors and from the VTC curves of the stacked combinational gates; we can conclude that the stacked transistors provide better leakage performance at extreme temperatures without much loss in performance. The stacked combinational gates performed excellently at $275^{O}C$ and exhibit very little deviation in the switching thresholds. Hence, from these observations we could propose to build a digital cell library with stacked transistors, which include a set of combinatorial and sequential cells that would perform efficiently at extreme temperatures of $275^{O}C$ with reduced leakage currents.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

A method to develop low leakage digital standard cells for synthesis of high temperature circuits has been proposed in this thesis. High temperature applications like down-hole measurement while drilling and data logging, aviation and automotive electronics need circuits that perform reliably at temperatures exceeding 200^{O}C. Power dissipation is a major concern in applications like automobiles as they rely on batteries as their source of power. We observed that the leakage currents are high at such extreme temperatures and leakage control is necessary to minimize the power dissipation in the 'OFF' state or standby mode of operation.

The method of stacking low threshold voltage NMOS transistors over regular threshold voltage NMOS transistors was proposed as an effective leakage control method which is based on the principle of "self-reverse biasing". The stacked transistor method has been shown to be effective in minimizing the 'OFF' state leakage currents and increasing the I_{ON}/I_{OFF} ratios. Two different lengths of stacked NMOS transistors were studied and the leakage performance was measured for the 1.3um stacked device at 3.3V and for the 1.6um stacked device at 5V. The stacked NMOS transistors demonstrated an

improvement of greater than two orders of magnitude increase in I_{ON}/I_{OFF} ratios over the regular transistors. The feasibility of a low leakage high temperature cell library was validated with basic combinational gates i.e. Inverter, NAND and NOR. The voltage transfer characteristic curve was measured for these gates and these gates exhibited very little deviation in the switching thresholds when compared to an identically sized regular combinational gate without stacking.

6.2 Future Work

There is a lot of scope for improvement on this topic like developing an entire library of standard cells using stacked NMOS transistors with various combinatorial and sequential cells of different drive strengths. The cell library could be validated on silicon by synthesizing certain benchmark circuits using the library and measuring their leakage performance on chip at high temperatures. The stacked transistor concept could also be applied to high temperature SRAM circuits like row and column decoders and 6-T SRAM cells where over 99.9% of the transistors remain in the standby mode most of the time. The effect of stack transistor logic shows great promise to reduce the leakage of SRAM and other denser circuits where the leakage power dissipation per unit area is high when compared to the levels of dynamic power or CV^2.

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VITA

Singaravelan Viswanthan

Candidate for the Degree of

Master of Science

Thesis: PROPOSAL FOR A 3.3V/5V LOW LEAKAGE HIGH TEMPERATURE DIGITAL CELL LIBRARY USING STACKED TRANSISTORS

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Biographical:

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Title of Study: PROPOSAL FOR A 3.3V/5V LOW LEAKAGE HIGH TEMPERATURE DIGITAL CELL LIBRARY USING STACKED TRANSISTORS

Pages in Study: 77 Candidate for the Degree of Master of Science

Major Field: Electrical Engineering

Scope and Method of Study:

The objective of this research is to propose a method for developing a low leakage digital cell library capable of performing at extreme temperatures of up to 275^{O}C. The leakage current at extreme temperatures is a dominant factor and plays an important role in determining the circuit performance. A method of stacking low threshold voltage NMOS (NL) transistors over regular threshold voltage NMOS (RN) transistors has proven to reduce the leakage currents at extreme temperatures without much area penalty and loss in performance.

Findings and Conclusions:

The stacked NMOS transistors were fabricated and leakage data was measured on silicon. The 1.3um (Length: RN=0.8um, NL=0.5um) stacked NMOS device at 3.3 Volts supply voltage and 1.6um (Length: RN=0.8um, NL=0.85um) stacked NMOS device at 5 Volts supply voltage, had I_{on}/I_{off} ratios of 2566 and 1114 respectively at 225^{O}C. The 1.3um and 1.6um length stacked NMOS transistors exhibited 34X and 8X improvement in I_{on}/I_{off} ratios over regular threshold NMOS transistors. The I_{off} currents for the 1.3um and 1.6um length stacked devices were 31nA and 81nA respectively at 225^{O}C. The 1.3um length stacked NMOS device at 3.3 Volts supply voltage and 1.6um length stacked NMOS device at 5 Volts supply voltage, had I_{on}/I_{off} ratios of 984 and 724 respectively at 275^{O}C. The 1.3um and 1.6um length stacked NMOS transistors exhibited 22X and 6X improvement in I_{on}/I_{off} ratios over regular threshold NMOS transistors. The I_{off} currents for the 1.3um and 1.6um length stacked devices were 76nA and 117nA respectively at 275^{O}C. Three basic combinational gates - Inverter, 3-input NAND and 3-input NOR gates with stacked NMOS transistors were tested on silicon for their Voltage Transfer Characteristic curves and these exhibited very little shift in the switching thresholds at temperatures of 275^{O}C compared to identically sized regular NMOS combinational gates.

ADVISER'S APPROVAL: Dr. Chris Hutchens