A PROPOSAL FOR AN 8-BIT RADIATION HARDENED FLASH A/D CONVERTER

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PREFACE

This thesis attempts to implement the building blocks required for the realization of a radiation-hardened, 8-bit flash analog to digital (A/D) converter. All the building blocks were designed and verified by simulating on PSPICE. All the building blocks were laid out using the layout tool MAGIC. The results of this study can be used to realize a high resolution A/D converter employed in space communication systems.

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This work is dedicated to my parents.

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NOMENCLATURE

A_{vx}	Voltage gain of the subscripted operational
C_{gdx}	Gate to drain capacitance of the subscripted operational
C_{gsx}	Gate to source capacitance of the subscripted operational
C_{dbx}	Drain to body capacitance of the subscripted operational
C_{dsx}	Drain to source capacitance of the subscripted operational
g_{dsx}	Small signal drain to source transconductance of MOSFET X
g_{mx}	Small signal channel transconductance of MOSFET X
I_{DX} (I_X)	Drain current of MOSFET X
MX	Subscripted MOSFET
VDD	Positive supply voltage
V_{gsx}	Gate to source voltage of MOSFET X
V_{id}	Differential input voltage
ΔV_x	(Vgs-V_T) of MOSFET X
VSS	Negative supply voltage
V_{TX}	Threshold voltage of MOSFET X
$(W/L)_{MX}$	Channel width to length of MOSFET X
β_X	Transconductance of MOSFET X
λ_X	Channel length modulation parameter of MOSFET X

CHAPTER I

INTRODUCTION

1.1 Overview

Analog-to-Digital converters are used throughout modern military systems. Common applications include image processing, communication links, analog sensors, control systems, and digital video [1,7,23]. The digital video field, which includes image recognition and high-definition television, has created the need for inexpensive, high-speed (between 5 and 100Msamples/s), and moderate resolution (between 6 and 12 bits) analog-to-digital (A/D) converters.

Image and signal processing systems in the field of space communication operate in a high-level radiation environment. Such systems are susceptible to threshold shift, increased leakage current, and FET mobility fall-off [5]. These effects of radiation are addressed by the use of new IC processing technologies like CMOS/SOS and CMOS/SOI [6] which offer superior radiation tolerance, low leakage current, latch up free CMOS, and high speed. This work presents the design of an 8-bit radiation-hardened high-speed A/D converter in CMOS/SOS technology. Such a high-speed A/D converter leads to increased power dissipation. It is also the objective of this thesis to design an 8-bit radiation-hardened very low-power A/D converter in

CMOS/SOS technology. Such a low-power A/D converter leads to reduced speed.

One major approach in the design of very high-speed analog-to-digital (A/D) converters has been a parallel conversion technique [7]. Parallel (or flash) conversion can be defined as the technique of 2^n comparators simultaneously comparing the analog input with the reference voltage for an n-bit conversion. Comparison, encoding, and latching are done in one clock cycle. The key to realizing a flash A/D converter is to achieve a low-power, high-speed, and low-offset comparator.

The converter power consumption should be small to obviate the forced cooling, and costs should be low for most applications. The first video A/D converters (ADC) were expensive hybrids, and later the 8-bit monolithic flash converters were made in bipolar technology [8,9]. Current advanced CMOS processes are capable of achieving video conversion rates of 5 - 20 Msamples/s [10,11].

The need for low-cost, low-power, high-speed, radiation-hardened A/D converters is continuously increasing in military applications. It has been difficult to develop low-power, radiation-hardened, video speed, 7 - 8 bit A/D converters using bulk CMOS technology [7,12,13,14]. Hitherto, very little work has been reported on the design of high-speed radiation-hardened A/D converters [5]. Historically, high-speed radiation-hardened A/D converters have been designed using bipolar technology at the expense of power dissipation.

A MOS integrated circuit operating in a high level radiation environment should operate virtually independent of transistor threshold voltage shift, increased device leakage current, and electron-hole mobility fall-off [1,3,4,5,15]. These problems

can be addressed by the use of thin-film CMOS/SOS technology for the following reasons. CMOS/SOS devices are made with epitaxial silicon islands on a sapphire substrate, which isolates the n and p transistors from each other. Hence, this structure is highly resistant to transient and total-dose radiation. Overall, the CMOS/SOS technology offers superior radiation tolerance, high speed, low power, and good noise immunity.

The currently available radiation-hardened A/D converters do not have the capability to operate at a high-speed (25 - 50 Msamples/s), high resolution (8 bits) and low power [5]; therefore, the development of a high-speed, low-power analog- to-digital converter that is highly immune to radiation effects is needed.

The design of comparators, bias circuits, and PLA encoders (building blocks of this A/D converter) were verified by simulation on PSPICE. All these building blocks were laid out using the layout tool MAGIC.

1.2 Objectives

The primary objective of this work is to design a radiation-hardened CMOS/SOS comparator circuit processed using thin-film technology and implement it in an 8-bit fully parallel (flash) A/D converter IC. This A/D converter features a high-speed (more than 25Msamples/s) operation, a low-power consumption (less than 600mW), and a total-dose radiation goal of 1Mrad(Si).

Additional objectives include designing a very low-power, radiation-hardened CMOS/SOS comparator and implementing it in an 8-bit very low-power, low-speed

radiation tolerant flash A/D converter. This A/D converter features very low power consumption (less than 20mW), low speed (less than 1MHz) and a total-dose radiation goal of 1Mrad(Si).

The contents of this thesis are presented in four chapters. Chapter II discusses in detail the effects of ionization radiation on the ICs and different types of flash A/D converters. The major schemes for reducing the radiation effects are discussed. Chapter III describes the design of a novel comparator circuit, a bias circuit, a PLA encoder, a reference string, and a low-power version of a flash A/D converter. This chapter includes a thorough discussion and analysis of each of the building blocks of this flash A/D converter, along with simulation results. Chapter III also includes a discussion on the layout of all the building blocks. Chapter IV offers conclusions based on these results. Suggestions for future work connected with investigations of this proposed A/D converter system are also offered.

CHAPTER II

LITERATURE REVIEW

This chapter discusses in detail the types of radiation environments and the basic effects of ionization radiation on the circuits, along with schemes for reducing the radiation effects. Different types of A/D (full-flash and two-step) converters are presented along with the analysis of resistor and capacitor reference strings and their advantages and disadvantages. Different types of comparators are also described, along with the necessity for autozeroing techniques.

2.1 Radiation Effects

The exposure of an integrated circuit (IC) to nuclear radiation alters the electrical properties of the active components of the circuit, which results in the degradation of circuit performance and possible circuit failure [15]. The primary goal of the radiation effects community is to harden electronic systems against degradation, failure, or upset when circuits are subjected to radiation exposure. Radiation hardening may be accomplished by one or more of the following methods: proper design and control of IC processing, appropriate device and circuit design, circumvention and error-correcting techniques, and careful hardness-assurance procedures.

There are a variety of radiation sources and environments to which electronic

systems may be exposed. The different radiation environments can be classified into three types of the most practical interest [15]:

i. Space radiation environment: Systems to be used in space may have to withstand large doses of radiation which are accumulated slowly over long periods of time. This environment has a low ionization dose rate of less than 1 rad/s and a total dose of more than 10^3 rad.

ii. Radiation from nuclear explosion: Systems to be used in the vicinity of nuclear explosions need to be hardened against radiation delivered in very short pulses and at very high dose rates. This environment has a high dose rate gamma flux of more than 10^8 rad/s and total dose of more than 10^4 rad.

iii. Nuclear reactor radiation environment: Systems to be used in this environment must withstand a steady state neutron flux and a low to moderate ionizing dose rate (i.e., gamma rays).

In spite of the seemingly complex interactions of radiation with matter, there are two dominant effects on solid state electronics [15]: ionization (generation of electron/hole pairs) and displacement damage (dislodging atoms from their normal lattice sites). For charged particle irradiation (even though a certain amount of atomic displacement can occur in general), the primary modes of degradation of electronic devices occur as a result of ionization [15]. For this reason, only ionization effects are considered in this section.

2.1.1 Ionization Effects

The part of an MOS structure most sensitive to ionizing radiation is the oxide insulating layer (SiO_2), which in present-day devices is generally less than 100ηm thick. In insulators (SiO_2), radiation-induced photocurrents are generally not a problem because of the much lower carrier mobilities and lower numbers of electron/hole pairs created. However, insulators generally contain relatively large densities of charge trapping centers at which the radiation-induced charges can be trapped for extended periods of time. In SiO_2, the radiation-generated electrons are much more mobile than the holes, and are swept out of the oxide (collected at the gate electrode) in times measured in picoseconds. In that first picosecond or two, some fraction of the electrons and holes will recombine. The holes which escape initial recombination are relatively immobile and remain behind near their points of generation, causing negative voltage shifts in the electrical characteristics of MOS devices; i.e., shifts occur in threshold voltage (V_T) for MOS transistors or the flatband voltage (V_{fb}) for MOS capacitors [15]. This *voltage offset* (threshold shift) in the MOSFETs is a major radiation-effects problem. As shown in Figure 1, the NMOS and PMOS threshold voltages will undergo a negative shift during total-dose irradiation. This negative shift results in an increased(decreased) current drive and an increased(decreased) subthreshold leakage current for NMOS(PMOS).

The above discussion of the radiation response of MOS devices addresses the gate oxide layer and the consequences of trapped-charge buildup in the gate oxide layer, primarily that of induced shifts in threshold voltages. The same physical

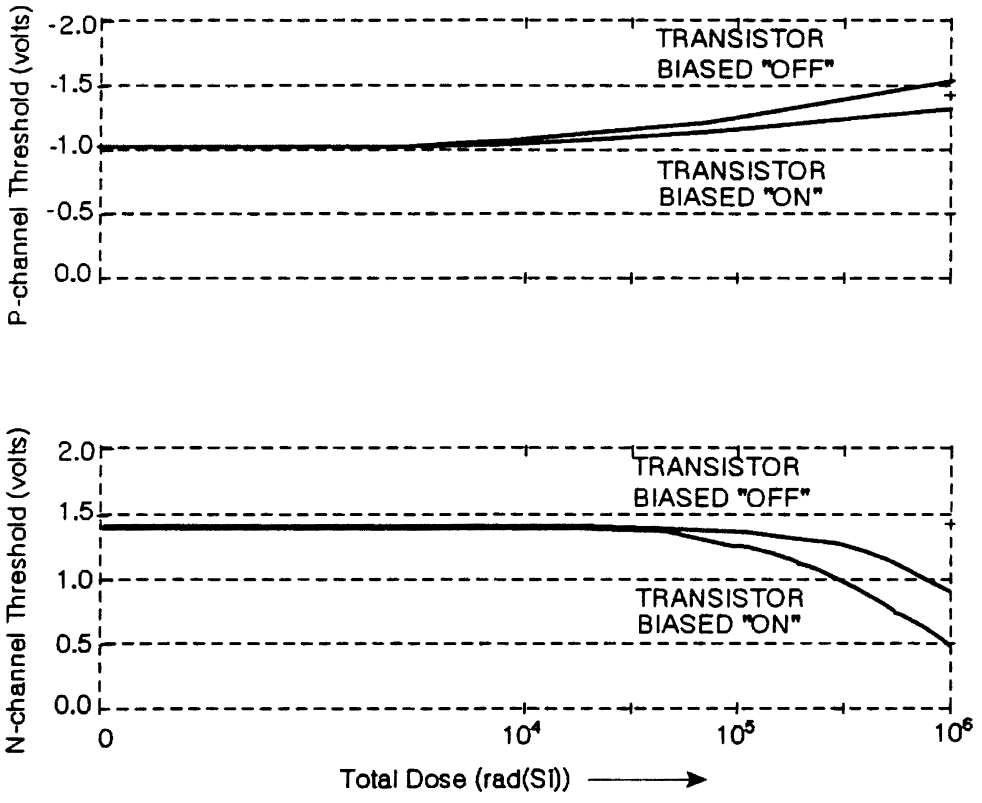


Figure 1. Variation of Threshold Voltage as a Function of Total Dose

processes leading to charge buildup in the oxide layers also occur in the thicker oxides used as field regions, isolation, or passivation oxides in IC technologies. The effects of charge buildup in these oxides on circuit operation involves generation of undesirable parasitic current leakage paths. Specifically, charge buildup in field, passivation, and isolation oxide regions can induce formation of inversion channels in the surface regions of adjoining semiconductor regions. In the presence of any potential gradients, this will result in parasitic current leakage (field oxide transistor) paths. These *induced current leakage paths* can be important failure modes not only in bulk CMOS technologies, but also in Silicon on Sapphire (SOS) and Silicon on Insulator (SOI) structures, as well as in bipolar technologies [15]. This induced leakage current alters the dynamic behaviour of the circuit so that the device would not operate according to the dynamic range specifications. This problem can be addressed by either increasing the oxide thickness or by design techniques such as making the quiescent bias current very large compared to the leakage current.

Ionization radiation also causes an increase in the density of fast interface traps, which results in charge accumulation in the dry gate oxide devices. The increase in the density of interfacial defects changes the channel charge and mobility in inversion, causing an increase in the channel time-constant by several orders of magnitude [15]. The increase is larger in the weak inversion region where mobility is significantly reduced by increased columbic scattering from the generated defects, and tends to saturate in a strong inversion where other scattering phenomenons dominate. The *increase in the channel time constant* is one of the major radiation effects problems,

and results in slower device response, which in turn reduces the gain bandwidth product for both n- and p-channel devices. This problem can be addressed by employing a mobility-independent circuit design; however, this solves only the gain problem.

The primary basic effects of total dose radiation on MOSFETs based on the work by McLean (1987) are summarized below:

i. The threshold voltages of NMOS & PMOS will undergo a negative shift during total-dose radiation.

ii. Radiation increases the device leakage current, which alters the dynamic behaviour of the circuit under consideration.

iii. Radiation lowers the mobility of the MOSFETs, which results in a reduced gain bandwidth product for both n- and p-channel devices.

From a circuit perspective, the shift in threshold voltage results in increased(decreased) transconductance of NMOS(PMOS), and the increase in the device leakage current reduces the output impedance.

2.2 Conventional Flash A/D Converters

In the very strictest sense, a flash converter operates no faster than the propagation delay of the system, which in turn is limited by the parasitic capacitances. A fully parallel converter is often referred to as full flash [16]. The full and two-stage flash techniques are generally used with conversion rates greater than 10MHz.

2.2.1 Full-flash A/D Converter

Full flash (single-step or parallel or flash) converters use 2^n comparators, 2^n+1 ladder resistors/capacitors, a 2^n-to-n encoder, a clock generator, and n output buffers. A block diagram of a conventional n-bit flash A/D converter is shown in Figure 2. A major component in realizing a high performance flash A/D converter is a low-power, high-speed and low-offset comparator circuit. Simultaneously, 2^n comparators compare an input voltage with each ladder tap voltage, which is achieved by dividing the reference voltage by the resistor ladder. The ladder tap voltage which most closely approximates the input signal is determined by testing the output of each comparator with the comparator outputs immediately above and below it. The encoder circuit converts the identified ladder tap voltage to a binary code. The n outputs of this encoder circuit are followed by n output registers and buffers.

The drawback of this converter is that when the resolution is increased by 2 bits (for example, from 8 to 10 bits), the flash converter's area and power increase by a factor of 4 with a resulting decrease in yield and reliability [7]. As the die area increases, the propagation delay differences also increase, adding to timing delays and related errors. Currently, the full flash converters are the best solution for fewer than 8-bits ADC.

2.2.2 Two-step flash A/D Converter

The block diagram of a classical two-step n-bit flash A/D converter (ADC) is shown in Figure 3. The converter consists of a sample-and-hold amplifier, an MSB

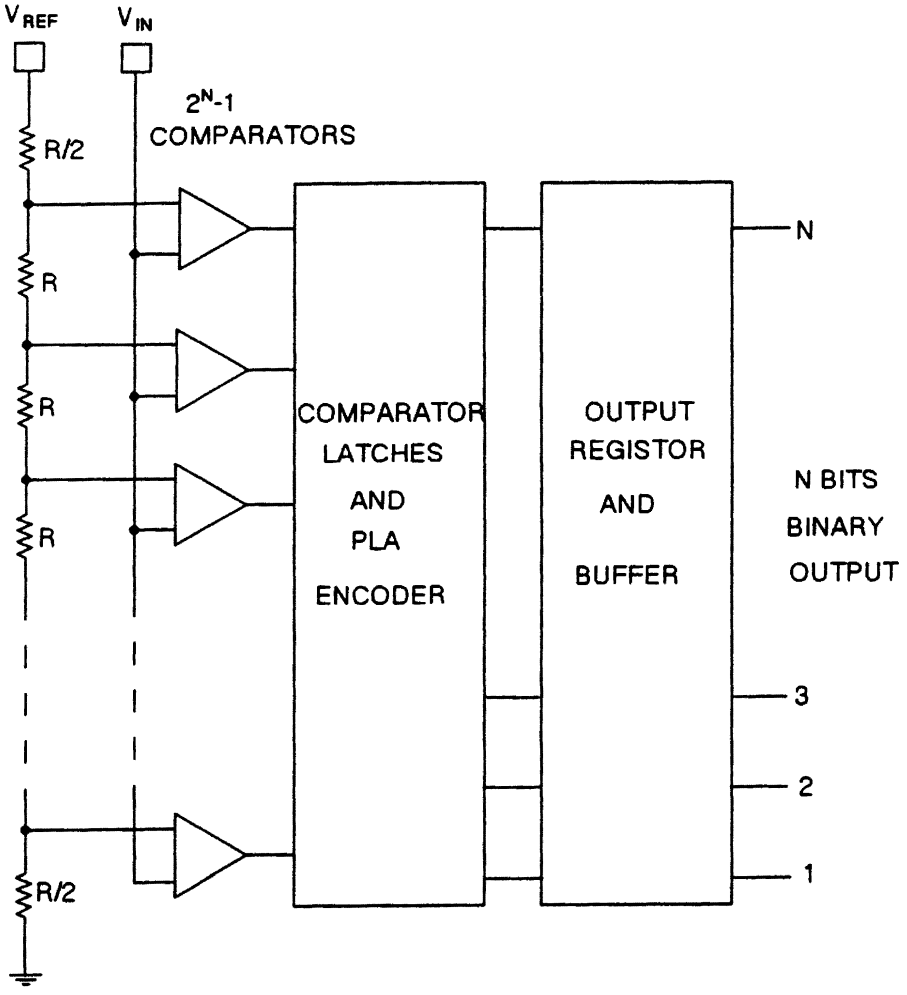


Figure 2. Block Diagram of a Typical Flash (parallel) A/D Converter

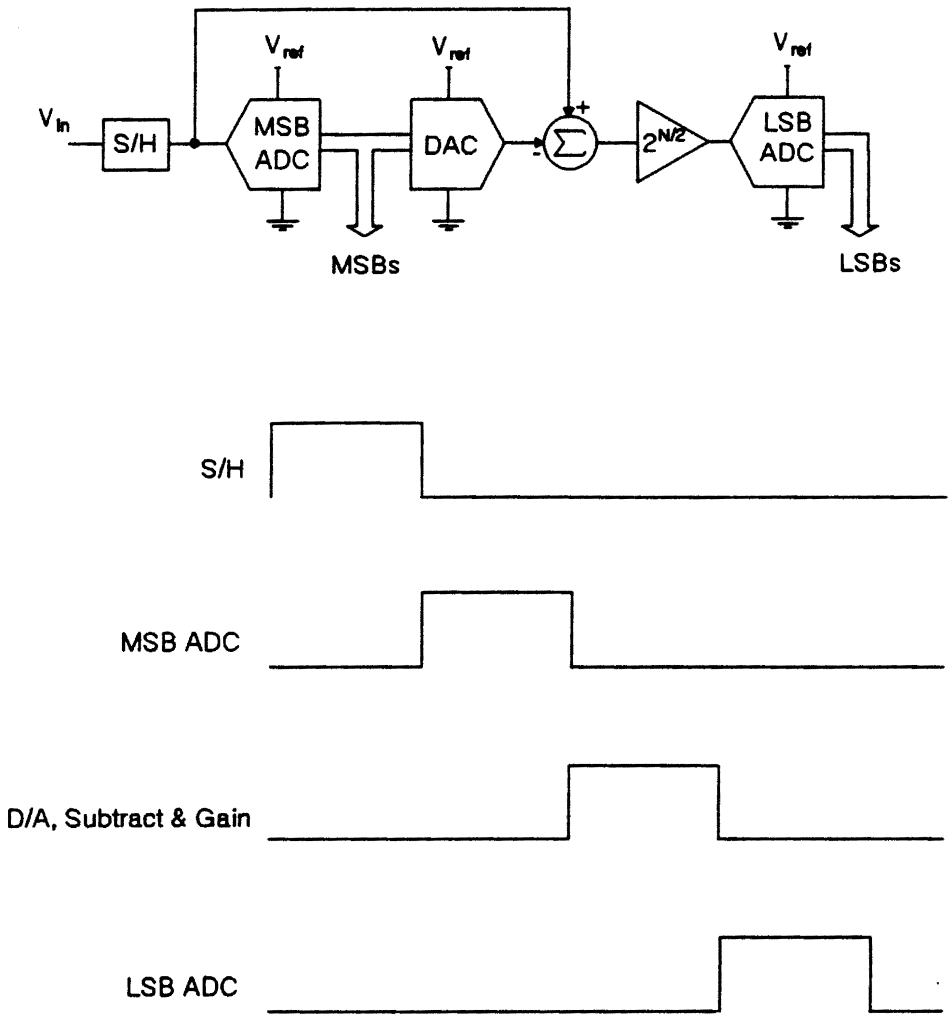


Figure 3. Block Diagram of a Classical Two-step Flash ADC

ADC (coarse ADC), a DAC, a subtractor, a gain block, and an LSB ADC. The operation is easily understood with the accompanying timing diagram. In the first phase the input is sampled and held. In the second phase MSBs are converted. In the third phase the DAC reconverts the input, which is subtracted from the held input and the result is amplified. The fourth phase is the "second step" in which the LSBs are converted.

This architecture uses $2^{n/2}$ comparators rather than the 2^n comparators used in a flash (fully parallel) converter. This yields a large savings in area and power with a resulting improvement in yield and reliability at the expense of two rather than one clock cycle for the conversion. The main drawbacks to classical two-step converters have been the need for high-speed, high-gain op amps and the difficulty of matching ADCs and DACs to each other [7].

2.3 Analysis of a Resistor/Capacitor Reference Ladder

The reference ladder is a critical building block in the design of A/D converters because it is responsible for providing reference voltage to each of the comparators. The inaccuracies in the reference voltage due to the reference ladder results in the degradation of the performance of the A/D converters. The major source of error in flash A/D conversion has been determined to be the loading of the reference ladder by the string of comparators which sample each ladder tap [17]. Surprisingly, small values of loading on the reference ladder have been shown to degrade accuracy significantly. When dynamic loads are applied to the ladder taps, the tap voltages are perturbed and

the integral non-linearity (INL) is degraded. Because of this, many resistor ladder designs have taps at the quarter points brought out to pins so that compensation voltage sources can be applied [7].

In this section a comparison of the resistor reference ladder and capacitor reference ladder approaches is presented. There are two major issues involved which influence the selection of reference ladder: the effect of loading on the performance of the ladder, and the effect of a component mismatch on the performance of ladder.

2.3.1 Loading Errors

Reference loading errors are of two types:

Transient error: This is the error associated with instantaneous ladder loading during a single measurement. For a resistor ladder, a bypass capacitor at the midpoint of array along with internal capacitances will reduce this error by a factor of four compared to static error [17]. In the case of a capacitor ladder, this error will be greater due to the RC time constant associated with the capacitances of ladder and the finite source resistance associated with the voltage reference [17].

Long term recovery error: This is the error associated with a new input level after the ladder has been loaded for a long period by an input at another level. This is the static error which cannot be bypassed and hence is the major source of error in A/D conversion.

The discrete resistor ladder model which was investigated by Dingwall (1979) is modified as shown in Figure 4. This figure shows the ladder network loaded by the

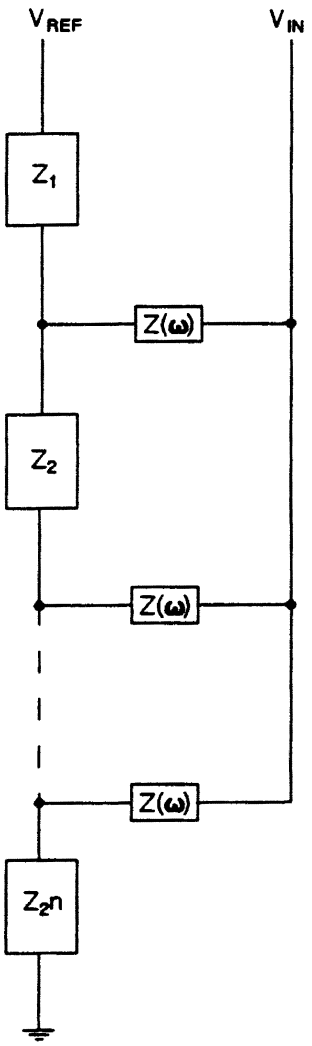


Figure 4. Discrete Reference Ladder Model

parasitic capacitance corresponding to each of the input comparator stages. During alternate half cycles, these parasitic capacitors are alternately discharged to input voltage potential and then to the appropriate ladder tap voltage [14]. Charging currents abstracted from the reference ladder network result in a nonuniform current flow in the ladder and produces a nonlinear division of the reference voltage. In this model the ladder load has been numerically simulated by an impedance $Z(\omega)$, which will result in removal of the same amount of charge from ladder nodes each full cycle as the comparator parasitics remove each half-cycle. $Z(\omega)$ is related to the input parasitic capacitance of the comparator C_{comp}:

$$Z(\omega) = \frac{2\Pi}{\omega C_{comp}} \tag{1}$$

The equivalent parasitic load-to-ladder section impedance ratio is given by:

$$K = N\sqrt{\frac{Z_{tap}}{Z(\omega)}} \tag{2}$$

where

Z_{tap} = the ladder impedance between two adjacent taps,

$Z(\omega)$ = the loading at each ladder tap point by comparator input parasitics,

N = the number of ladder taps, and

K = the loading constant.

The analysis by Dingwall (1979) shows that ladder loading is a strong function of V_{IN} and loading ratio $Z(\omega)/Z_{tap}$, and the greatest errors are caused by input voltages of 0 or V_{ref}, corresponding to the extremes of reference ladder voltages. It has been

shown that worst case loading occurs when the parasitics are initially charged to zero and then to the reference voltage. For 8-bit accuracy a load ratio of $Z(\omega)/Z_{tap}$ in excess of 100,000 is required [17].

If a resistor ladder is used with R_{tap}=10 ohms, and C_{comp}=0.2fF and if the circuit is operated at 25MHz, then we have a loading ratio of

$$\frac{Z(\omega)}{R_{tap}} = \frac{2\Pi}{25*10^6*0.2*10^{-15}*10} \cong 20*10^6 \quad (3)$$

which is well above the loading ratio required.

If a capacitor ladder is used, then to achieve the required loading ratio

$$\frac{Z(\omega)}{Z_{tap}} > 100,000 \quad (4)$$

In this case,

$$\frac{C_{tap}}{C_{comp}} > 100,000 \quad (5)$$

For C_{comp}= 0.2fF, C_{tap} > 20pF. So to achieve a required loading ratio, a large capacitor is required which in turn requires a very large area for an 8- to 10-bit A/D converter.

Thus it is seen that the area requirement and loading effects are closely related. In case of a resistor string, as R_{tap} decreases, the loading error decreases as does the area. However, if R_{tap} is reduced, then various resistances, such as lead resistance of the package and bonding wire resistance, cannot be neglected. Then trimming of resistors is required or power consumption in the chip increases due to low resistance. Also, if R_{tap} is reduced, then the finite source resistance of the voltage reference forms

a voltage divider along with the resistor string, leading to an error in the tap voltage. Thererfore, it is required that R_{tap} be much greater than R_{source}. Hence, a compromise concerning the allowable error is required due to the voltage divider formed by the source impedance.

In case of a capacitor string, to decrease the loading effects the capacitor should be large; this requires increased area. Thus, a tradeoff is again required in regards to the permissible loading effect that can be tolerated and how much real estate is available on the chip.

2.3.2 Mismatch Errors

The component mismatch and the leakage current at the input of the comparator influence the performance of the reference ladder. Doernberg (1989) considered an n-bit resistor string with the resistor values normally distributed with mean R and standard deviation σ_R. The worst case error that can be tolerated is ± 1/2 LSB, which occurs at the middle tap. At that tap the ratio of tap voltage to V_{ref} is

$$\frac{V_{tap}}{V_{ref}} = \frac{1}{2} * \left(1 \pm \frac{1}{2^n}\right) \tag{6}$$

This ratio of voltages is the ratio of resistance of half of the string to the total resistance. The maximum mismatch for less than 1/2 LSB error is [7]

$$\frac{\sigma_R}{R} = \frac{1}{\sqrt{2 * 2^n}} \tag{7}$$

For 8-bits this leads to (σ_R / R) < 0.0442. The same analysis applied to a capacitor

string results in a similar matching requirement, $(\sigma_C / C) < 0.0442$.

Capacitor matching is typically easier to achieve than resistor matching [18]. Better matching accuracy can be expected from a capacitor string. MOS capacitors have a low voltage coefficient (appx 20ppm/v) and a temperature coefficient (appx 25ppm) than resistors [18].

The major sources of component mismatches in integrated circuits are the uncertainties in photolithographic edge definition [19]. In the case of a pair of nominally identical resistors, an edge uncertainty in resistor length (ΔL) and width (ΔW) results in a mismatch given by

$$\frac{\Delta R}{R} = \frac{\Delta L}{L_r} - \frac{\Delta W}{W_r} = -\frac{\Delta W}{W_r} \tag{8}$$

because $L_r >> W_r$.

For a pair of nominally identical capacitors this mismatch due to edge uncertainties is

$$\frac{\Delta C}{C} = \frac{\Delta L}{L_c} + \frac{\Delta W}{W_c} \tag{9}$$

Since the capacitance value is determined by the capacitor area as opposed to L/W for resistors, the freedom exists to optimize capacitor geometries in order to reduce the mismatch sensitivity due to uncertainties in edge definition. Thus, for a given area it is possible to have

$$L_c = W_c >> W_r \tag{10}$$

Hence,

$$\frac{\Delta C}{C} < \frac{\Delta R}{R} \tag{11}$$

Thus it is seen that it is easier to achieve a high degree of matching with a capacitor string as opposed to a resistor string. To achieve a high degree of matching in a resistor string, the reference banks must be trimmed; this is a lengthy and therefore costly process. Thus a capacitor string typically offers better performance. But a mismatch in the case of a resistor string will only cause nonlinearity without producing non-monotonic behaviour [18] which cannot be guaranteed in case of a capacitor array. Therefore, a tradeoff is again involved as to how much mismatch can be tolerated and how crucial the monotonicity requirement is for the reference string.

Very often the resistor string is a better choice because it occupies less space and the recovery error can be minimized. The error in the tap voltage (caused due to the formulation of a voltage divider between the source impedance of a reference voltage and a reference ladder) can be minimized by making the tap resistance much larger than the source impedance of the reference voltage. As previously noted, the mismatch in the resistor string does not result in non-monotonic behaviour, which can be the case in a capacitor ladder.

2.4 Comparator Circuit

The most critical component of a flash ADC design is the analog comparator [7]. In particular a comparator operating in a radiation environment requires a circuit design that is virtually independent of threshold voltage shift, increased leakage, and

reduced mobility of the MOSFETs. In a flash ADC, internal comparators must amplify small voltages into logic levels. In general the comparators either feed a PLA encoder or latches, which in turn feed the encoder. In either approach, the encoding process can often be pipelined with the comparator function. The encoding process is faster than the comparator function; for this reason the maximum conversion rate for the ADC is limited by the response time of its comparators. Therefore, the design and optimization of the comparators is of critical importance.

A comparator design focuses on meeting several specifications; typically, these are gain, propagation delay, and associated offset cancellation. The main comparator-related errors are: fast high-gain comparators, offset voltage from transistor mismatches, power supply noise, and the charge injection error from the comparator's autozero switches. As a rule-of-thumb, comparator gain is usually about 2^n for an n-bit ADC [7]. This requirement comes from the need to amplify a voltage that is less than 1/2 LSB up to a compatible logic level. The total error due to the feedback switch charge injection, the offset voltage, the power supply noise, and a mismatch in the reference ladder must be less than 1/2 LSB [7,23]. This section deals with the optimization of the number of comparator stages and autozeroing techniques along with a review of previous A/D architectures.

2.4.1 Optimum Number of Comparator Stages

Doernberg (1989) studied analytically and verified experimentally the optimum of number of comparator stages required to achieve a fixed gain, a maximum

bandwidth, and minimum area requirements. For n gain stages, each with gain A, the total gain will be

$$G=A^N \tag{12}$$

Each stage is assumed to have a single dominant pole and will have a constant gain-bandwidth product (GBW),

$$GBW=A\omega_s=\frac{A}{\tau}=\frac{G^{\frac{1}{n}}}{\tau} \tag{13}$$

where τ= the single stage delay = 1/stage bandwidth (ω_s).

The comparison time (n-stage delay) is

$$t_d=n\tau=\frac{nG^{\frac{1}{n}}}{GBW} \tag{14}$$

To minimize the comparison delay with respect to the number of stages, the partial differentiation of t_d with respect to n is set equal to zero and n is found:

$$n=\ln(G) \tag{15}$$

From equations (12) and (15), A = e.

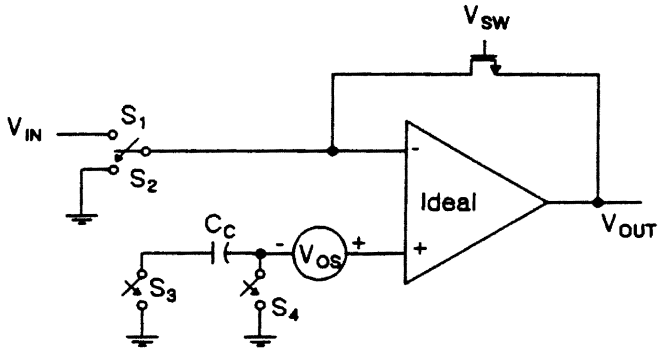
The optimum number of stages (n) for the fastest response is ln(G), and the gain per stage (A) is 'e'. For an 8-bit ADC, the optimum number of stages is 5 and the gain per stage is 2.718. The fastest response is obtained with five stages, but conversion time remains almost constant from three to over ten stages [7]. It can be concluded that 3 stages as practical solution for most A/D converters, since the increased conversion delay is negligible, while the savings in area and power is

approximately 50 percent.

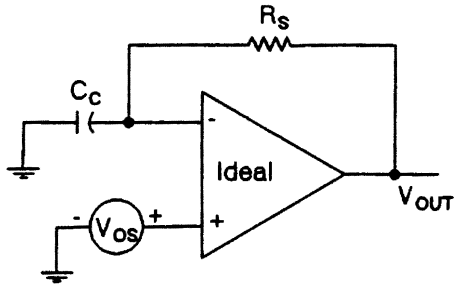
2.4.2 Autozero Technique

Autozeroing is the process of cancelling the offset voltage of the comparator by storing the offset voltage on a series coupling capacitor [22]. If the input terminals of a comparator are connected to ground, the voltage which appears at the output of the comparator is refered to as the amplified input offset voltage. The offset voltage is typically a small dc voltage in the range of 1 to 20mv. Offset voltage is a serious problem in the design of ladder comparators which are used in A/D converters of more than 6 bits [7,23]. Using offset cancellation techniques, a significant portion of the offset voltage can be removed. Conceptually offset reduction is limited by the willingness to compromise area and speed by increasing the value of C_c. Offset voltage is measured, stored on the capacitor, and summed with the input offset voltage, effectively canceling the offset [22].

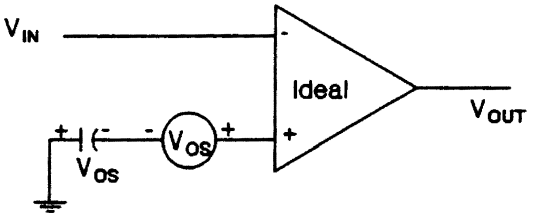
A practical implementation of an auto-zeroed comparator is shown in Figure 5. This inverting comparator is modeled with an offset-voltage source V_{os}. A known polarity is given to the offset voltage for convenience. Neither the polarity nor the value can be predicted [22]. Figure 5(b) shows the state of the circuit during the first phase of an autozero cycle when switches S_2 and S_4 are closed. The offset voltage is stored across the capacitor C_C. Figure 5(c) shows the circuit in the second phase of the autozero cycle when switches S_1 and S_3 are closed. The offset is cancelled by the addition of V_{os} to the potential across C_C. It is during this portion of the cycle that the



(a) Setup for the Autozero circuit



(b) Comparator during autozero state



(c) Offset is cancelled by addition of V_{os} to V_{cc}

Figure 5. Autozero Operation

circuit functions as a comparator. Applying KCL to node A in Figure 5(b) results in

$$V^{-}C_{C}S+\frac{(V^{-}-V_{O})}{R_{S}}=0 \tag{16}$$

Output voltage of comparator is given by

$$V_{0}=(V^{+}-V^{-})A_{VOL}=(V_{OS}-V^{-})A_{VOL} \tag{17}$$

Substituting equation (17) in (16) and solving the equation results in the following transfer function:

$$V^{-}C_{AZ}S+\frac{V^{-}}{R_{S}}=\frac{(V_{OS}-V^{-})A_{VOL}}{R_{S}} \tag{18}$$

$$V^{-}[C_{C}S+\frac{1}{R_{S}}+\frac{A_{VOL}}{R_{S}}]=\frac{V_{OS}A_{VOL}}{R_{S}} \tag{19}$$

$$V^{-}[R_{S}C_{C}S+1+A_{VOL}]=V_{OS}A_{VOL} \tag{20}$$

$$V^{-}=\frac{V_{OS}}{\frac{R_{S}C_{C}S}{A_{VOL}}+\frac{(1+A_{VOL})}{A_{VOL}}} \tag{21}$$

With a time constant

$$\tau=\frac{R_{S}C_{C}S}{A_{VOL}} \tag{22}$$

for X% accuracy, k time constants are required [23], which results in an accurate settling time of

$$\tau_{settling}=\frac{kR_{S}C_{C}}{A_{VOL}} \tag{23}$$

where $\tau_{settling}$ is the time required for the input signal of the circuit to settle after the autozero switches are closed. Gain considerations demand that the differential signal be transmitted essentially unattenuated via coupling capacitor C_c. For this reason $C_c >> C_{amp} + C_{sw}$, where C_{amp} is the parasitic capacitance losses of the input stage and C_{sw} is the parasitic capacitance of the autozero switch. Typically, C_c is more than 10 times the parasitic capacitance losses of the input stage [17]. This maintains accuracy in the subtraction of common-mode charge injection errors and the balanced differential gain, which requires an accurate Cc.

2.5 Radiation-hardened CMOS logic circuits

Chen et al. (1992) proposed a technique for the design of digital CMOS circuits that are almost insensitive to radiation. By adding three n-channel transistors to the conventional digital CMOS circuits, good radiation hardened behaviour is observed in the inverter, NOR, and NAND gates under SPICE simulation. The method, its merits and its demerits will be discussed in this section.

As noted previously, for a NMOSFET with a positive threshold voltage V_{TN} and a PMOSFET with a negative threshold voltage V_{TP}, radiation results in the decrease of $|V_{TN}|$ and the increase of $|V_{TP}|$. Also it is known that ΔV_{TN} is much greater than ΔV_{TP} in general operating conditions [25]. It is noted that I-V characteristics of a MOSFET under radiation exposure changes slightly except for the V_T shift [25]. Thus, the design of a radiation-hardened circuit can be simplified as the design of a threshold voltage variation inherent circuit.

This technique of design of radiation-hardened CMOS logic circuits will be discussed with respect to the inverter circuit. The same technique can be applied to NOR and NAND gate circuits. For a traditional CMOS inverter circuit as shown in Figure 6, the transfer curves before and after irradiations are quite different and are shown in the same figure. Also in Figure 6, V_{01} and V_{10} represent the transition point of output changing from 0 state to 1 stateand from 1 state to 0 state, respectively. The noise margin of this circuit is defined as

$$NM_0 = V_{10} \simeq V_{TN}^0 \tag{24}$$

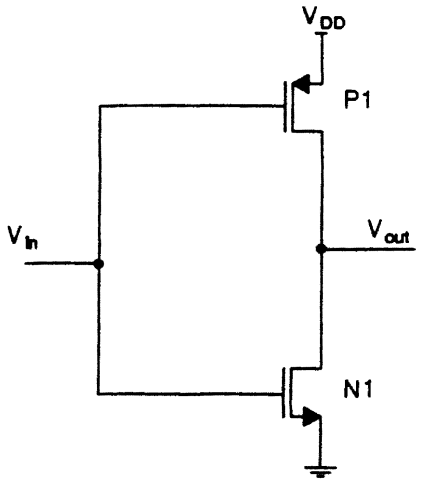
$$NM_1 = V_{DD} - V_{01} \simeq |V^{TP^0}| \tag{25}$$

where NM_0 and NM_1 are the noise margins of input at 0 state and at 1 state, respectively. After radiation both V'_{01} and V'_{10} shift toward the left, and equations (24) and (25) can be written as

$$\begin{aligned} NM_0^1 &= V_{10}^1 \\ &\simeq V_{TN}^1 \\ &= V_{TN}^0 - |\Delta V_{TN}| \end{aligned} \tag{26}$$

$$\begin{aligned} NM_1^1 &= V_{DD} - V_{01}^1 \\ &\simeq |V_{TP}^1| \\ &= |V_{TP}^0| - |\Delta V_{TP}| \end{aligned} \tag{27}$$

where ΔV_{TN} and ΔV_{TP} are the threshold voltage shifts due to the radiation of NMOS and PMOS, respectively. From equations (26) and (27), it can be seen that the noise margin of 0 state after radiation exposure (NM'_0) will be smaller and that of 1 state will be larger. Hence, the main aim of the author was to design some compensation



Traditional CMOS Inverter

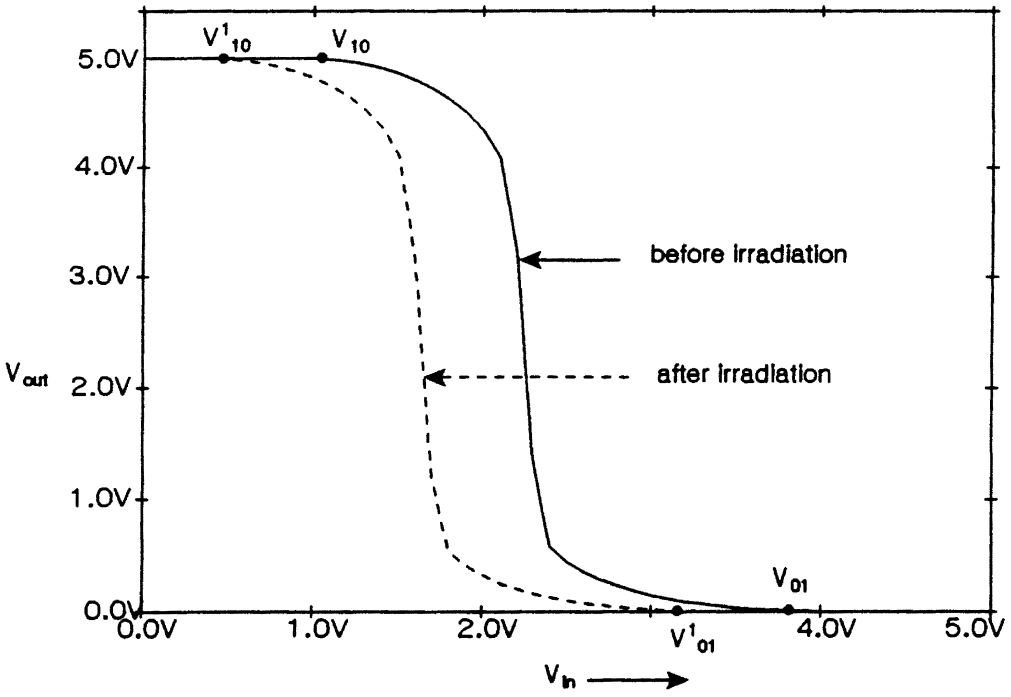


Figure 6. Transfer Curves of Traditional CMOS Inverter Before and After Radiation Exposure

circuits to make NM^1_0 as little correlated to ΔV_{TN} as possible.

An improved CMOS inverter with three additional NMOSFETs (i.e., N2, N3, and N4), is shown in Figure 7. Since it is necessary to improve NM^1_0, just consider the case that V_{out} varies from 1 state to 0 state. If this circuit is designed to let V_x follow ΔV_{TN} (i.e., $V_x = \Delta V_{TN}$) by the way of adjusting the gate bias of N4, then the transition point of V_{out} changing from 1 to 0 becomes

$$\begin{aligned} NM_0^1 &= V_{10}^1 \\ &\simeq V_x + (V_{TN}^1) \\ &= \Delta V_{TN} + (V_{TN}^0 - |\Delta V_{TN}|) \\ &= V_{TN}^0 \\ &= NM_0 \end{aligned} \tag{28}$$

From the above equation it can be seen that NM_0 does not vary with ΔV_{TN}; therefore NM_0 is not affected by radiation exposure.

To make V_x follow ΔV_{TN}, gate bias voltages $2V_g$-V^0_{TN} and V_g-ΔV_{TN} should be applied to transistors N3 and N4, respectively, where V_g is an arbitrary voltage. Assuming both N3 and N4 operate in saturation region results in the limitation that

$$V_g - \Delta V_{TN} - V_X \leq V_{TN}^1 \tag{29}$$

According to current equality,the following equations can be written:

$$\frac{\beta_3}{2}(2V_g - V_{TN}^0 - V_X - V_{TN}^1)^2 = \frac{\beta_4}{2}(V_g - \Delta V_{TN} - V_{TN}^1)^2 \tag{30}$$

For $\beta_4 = 4\beta_3$, the above equation simplifies to

$$V_X = \Delta V_{TN} \tag{31}$$

Obviously, the result of the above equation is the required condition as described in

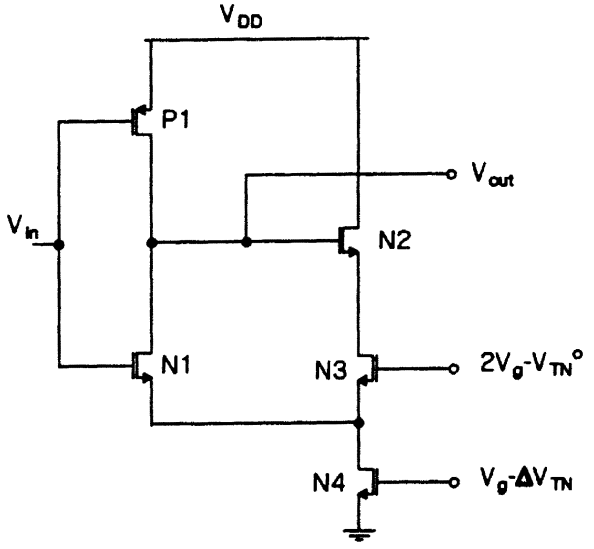


Figure 7. Radiation Hardened CMOS Inverter

equation (28). Substituting equation (31) into (29) results in

$$V_g \leq V_{TN}^0 + \Delta V_{TN} \tag{32}$$

A constant current bias circuit has been proposed by the author, which can be used to bias the transistor N4. However, equation (32) is the limitation for ΔV_{TN}. Also, the addition of three extra transistors, N2, N3, and N4, slows down the switching speed considerably. Another limitation of this approach is need for bias voltage $2V_g$-V^0_{TN} to bias N3 into saturation. Apparently, this bias voltage has to be supplied externally.

2.6 Previous work on flash A/D Converters

Heuner et al. (1988) conducted studies on the design of radiation-hardened data converters. They used a radiation hardening CMOS/SOS process to minimize the threshold shifts and the device leakage current. CMOS/SOS devices are made with epitaxial silicon islands on a sapphire substrate. This technique greatly reduces device capacitance and completely eliminates latch-up.

The most critical component of a radiation-hardened A/D converter is the analog comparator. The necessity of a rail to rail (V_{DD} to V_{SS}) dynamic range for the comparator ruled out the use of conventional CMOS type comparator. This A/D converter uses a McGrogan comparator, which consists of two sampling transmission gates AC coupled to a self-biasing autozeroed CMOS/SOS inverter amplifier. The autozeroing property of this inverter automatically compensates for dynamic threshold variations. Under radiation the threshold (V_{TN}) of an n-channel MOSFET shifts

towards depletion and channel transconductance (g_{mn}) increases, while g_{mp} of the p-channel MOSFET tends to decrease. Over a limited radiation dose (i.e., up to 1Mrad), the increasing g_{mn} and the decreasing g_{mp} tend to add up to a constant value.

Another characteristic of this comparator for operation in radiation environments is its relative insensitivity to increased leakage current. The inverter amplifiers are typically biased in a class A configuration with an approximately 50μA bias current. The leakage current associated with this comparator is less than 50ηA, so any radiation-induced leakage current is a small portion of the overall quiescent bias current.

Yukawa (1985) reported the design of a high-speed (20Msamples/s), low-power dissipation (350mW), 8-bit fully parallel A/D converter IC. This converter basically consists of 259 identical transistors, 256 comparators, 255 AND gates, a PLA, a gray code to binary code converter, and n+1 output latches. The outputs of all the comparators are transfered to the AND gates, which detect the transition point from logical '0' to '1'. This information obtained at the 255 AND gates is converted to an 8-bit gray code by the PLA. When the PLA latches the data from the AND gates at transition, there is the possibility that two successive AND gates will give a logical 1 level. The gray code is employed to eliminate a large code jump in this condition. The code conversion logic, from the gray code to binary code, is placed between the master and slave output latches.

This paper emphasizes the importance of transistor dimension optimization in the design of comparator circuits, instead of employing an offset canceling technique.

A standard deviation of the offset voltage has been designed at less than one third of the A/D converter minimum resolution for ±1 LSB accuracy, through a novel comparator circuit design. The comparator circuit consists of a differential amplifier and a novel CMOS latch circuit. The differential amplifier with p-channel input transistors increase the input voltage range to V_{SS} level, protects signals from noise sources, and decreases the feedthrough from the latch stage to the reference voltage network. The latch stage consists of discharge transistors, an n-channel flip-flop with a pair of n-channel transfer gates for strobing, a p-channel flip-flop, and p-channel precharge transistors. Advantages for a flip-flop strobed at drain node over a flip-flop strobed at source node exist in regard to the regeneration speed and offset. Offset voltage caused by a channel-length fluctuation is much lower at a zero substrate bias. Therefore, transistor channel lengths can be decreased and the flip-flop speed can be increased.

Kumamoto et al. (1986) reported the design of an 8-bit high-speed (30 Msamples/s) and low-power (60mW) flash A/D converter in a 1.5μm bulk CMOS technology. The architecture of this converter is similar to the previous architecture. Simultaneously, 256 comparators compare an input voltage with each ladder tap voltage, which is made by dividing the reference voltage by the resistor ladder. The minimum ladder tap voltage which exceeds the input voltage is identified by the transition detection logic. The encoder circuit converts the identified ladder tap voltage to a binary code. In this encoder circuit, the gate voltages of load transistors are controlled by a clock signal, which reduces the power dissipation.

In order to achieve a high-speed, low-power A/D converter, a fine pattern process technology and a new capacitor structure, referred to as shielded-capacitor structure, have been employed and the transistor sizes of a chopper-type comparator have been optimized. This shielded-capacitor structure has two advantages: decreasing the parasitic capacitance, and shielding from noise at the output node.

The primary objective of this work is to design a radiation-hardened CMOS/SOS comparator circuit processed using thin-film technology and implement it in an 8-bit, fully parallel (flash) A/D converter IC. This A/D converter features a high-speed (greater than 25 Msamples/s) operation and a lowpower consumption (less than 800mW) and a total-dose radiation goal of 1Mrad. The design of the comparator is discussed thoroughly in the next chapter.

CHAPTER III

SYSTEM BUILDING BLOCKS

This chapter discusses in detail the design of all the building blocks of a prototype radiation-hardened, high-speed, low-power 8-bit CMOS/SOS A/D converter. The design, analysis, and simulation results of the novel comparator circuit and other building blocks are presented. The error sources in the architecture are described. The layout topology of comparators and ladder resistors is also presented.

The primary objective of this thesis is to design a radiation-hardened high-speed CMOS/SOS comparator circuit processed using thin-film technology, and to implement it in an 8-bit fully parallel (flash) A/D converter IC. The specifications of this A/D converter are as given below:

- Conversion rate in excess of 25 MHz
- Power dissipation less than 800mW
- Total-dose radiation of 1Mrad(Si)
- Analog full-scale range of ±1v
- Binary output code

3.1 CMOS/SOS Process

The major CMOS technologies used in the radiation-hardened community are

bulk CMOS and CMOS/SOS (Silicon on Sapphire); however, CMOS/SOI (Silicon on Insulator) is under active evaluation. A cross-section of these CMOS IC technologies is shown in Figure 8. The bulk CMOS technology uses a silicon substrate (sometimes epitaxial substrate), and junction isolation to form both n- and p-channel transistors. The CMOS/SOS process utilizes an epitaxial silicon film, which is deposited on an insulating substrate (i.e., sapphire). CMOS/SOI structures can be formed with a variety of processes, including ion implanted oxygen (SIMOX), recrystallized polysilicon, and anodic oxidation of silicon, but generally they all utilize silicon substrate. The merits and demerits of CMOS/SOS will be discussed in this section, since it has been selected as the technology of choice for the design of radiation-hardened A/D converter.

The CMOS/SOS technology employs insulator isolation, as opposed to the junction isolation of the bulk technology. This approach offers a substantial advantage in latch-up, transient upset, single event upset (SEU), and elevated temperatures. Bulk CMOS devices, for example, require a generic cure for latch-up, while latch-up for SOS devices is physically precluded due to the insulator junction isolation. Similarly, bulk devices also have parasitic field devices that may have a considerable impact on circuit performance in a radiation environment, while these particular parasitic devices do not exist in SOS circuits.

The polysilicon gates of the transistors are deposited over the thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the

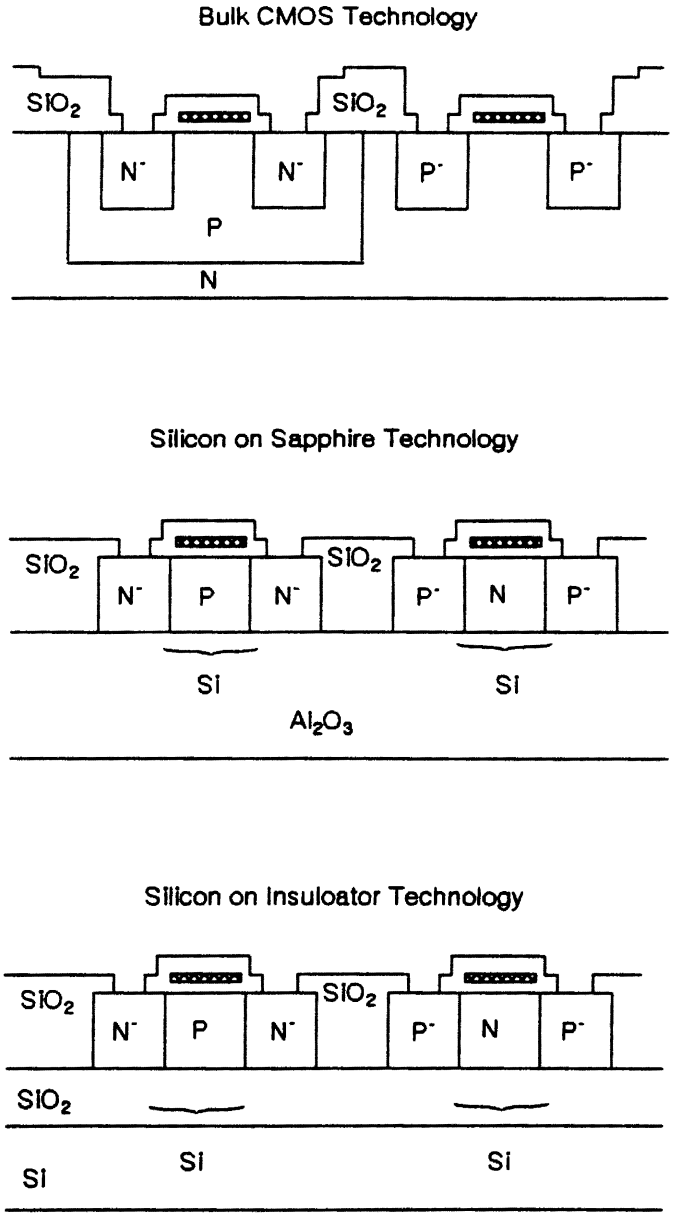


Figure 8. Cross-section of Major CMOS IC Technologies used in Radiation Hardened Environment

implantation. The source and drain are automatically aligned to the gate; hence the expression "self-aligned-gate process". In this way, gate-to-source and gate-to-drain capacitances are minimized. Since the devices are made with epitaxial silicon islands on a sapphire substrate, there is no body (substrate) contact on the device. Basically, CMOS/SOS devices are three terminal devices. Thus, for CMOS/SOS devices the bulk threshold parameter (γ) is approximately zero. All though in practice this is not the case, the threshold voltage (V_T) for an n-channel transistor is given by

$$V_T = V_{T0} + \gamma \left[\sqrt{2|\Phi|_F + V_{SB}} - \sqrt{2|\Phi|_F}\right] \quad (33)$$

where

V_{TO} = V_T at zero source to body potential

γ = bulk threshold parameter

Φ = strong inversion surface potential

V_{SB} = source to body potential

For CMOS/SOS devices, $V_T = V_{TO}$. Thus threshold shifts are minimized to a great extent. Also source-to-body and drain-to-body capacitance is very negligible. The only parasitic capacitance which affects the speed of operation of SOS circuits is gate-to-source capacitance. The analysis by Dingwall (1979) showed that the accuracy of A/D converters is critically dependent upon minimum input capacitance. CMOS/SOS devices with "dielectrically-isolated" transistors formed over insulating sapphire have exceptionally low capacitive parasitics and can also perform complex logic functions in excess of 1.0GHz clock rates. This level of high speed performance is necessary in carrying out a high speed A/D conversion.

Since the CMOS/SOS process isolates n- and p-channel transistors from each other, this structure is highly immune to transient radiation, total-dose radiation, and single event upset. Overall, the CMOS/SOS technology not only offers superior radiation tolerance, high-speed, low-power, and good noise immunity, but also operates well over the entire military temperature range (-55° to +125°C).

CMOS/SOS technology, however, has its own set of unique limitations, which includes a back-channel parasitic MOS device as well as a sidewall MOS device [6]. The formation of a back-channel parasitic transistor leads to a radiation-induced, back-channel leakage current. Consider an n-channel SOS transistor. Under radiation, positive charges will be trapped in the sapphire substrate immediately under the active p-type Si layer. The normal device channel occurs in the p-type Si region next to the gate oxide region. However, because of the positive charging of the sapphire substrate, an inversion layer can be induced on the backside of the p-type Si region, resulting in the back channel leakage current between source and drain.

A second unique radiation concern for SOS structures is the sidewall SOS region where the gate electrode covers a gate oxide in the channel width direction as it traverses to its next appointed node. This region, like the back channel, may also provide a parallel depletion-mode device to the active transistor. The side wall parasitic transistor can be eliminated, however, by defining the SOS island beyond the gate region at the expense of packing density.

Finally, the substrate in SOS circuits is not necessarily connected to a fixed potential, which may permit abnormal potentials during a radiation exposure; such as a

negative substrate bias on an n-channel device. Usually the bias dependent threshold voltage shift is significantly worse for these conditions, so it is prudent to clamp all substrate regions for SOS circuits designed for a radiation environment.

3.2 Circuit Configuration

A block diagram of the radiation-hardened flash A/D converter is shown in Figure 9. The A/D converter is composed of 255 fully differential comparators, 258 identical ladder resistors, tap detection logic, a 255-to-8 PLA encoder, a clock generator, and eight output buffers. Simultaneously, 255 comparators compare an input voltage with each ladder tap voltage; the comparison is achieved by dividing the reference voltage through the use of a resistor ladder. The minimum ladder tap voltage which exceeds the input voltage is identified by the transition detection logic. The encoder circuit converts the identified ladder tap voltage to a binary code. The eight outputs of this encoder circuit are followed by eight output registers and buffers.

3.3 Radiation-Hardened Comparator Circuit

The key effects of total dose radiation on MOSFETs (refer to Section 2.1.1) are: a negative shift in the threshold voltages of n- and p-channel transistors, which results in the increased(decreased) transconductance of NMOS(PMOS); an increased device leakage current, which reduces the output impedance and alters the dynamic behavior of the circuit; also reduced mobility in the MOSFETs, which results in a reduced gain bandwidth product for both n- and p-channel devices. The operation of

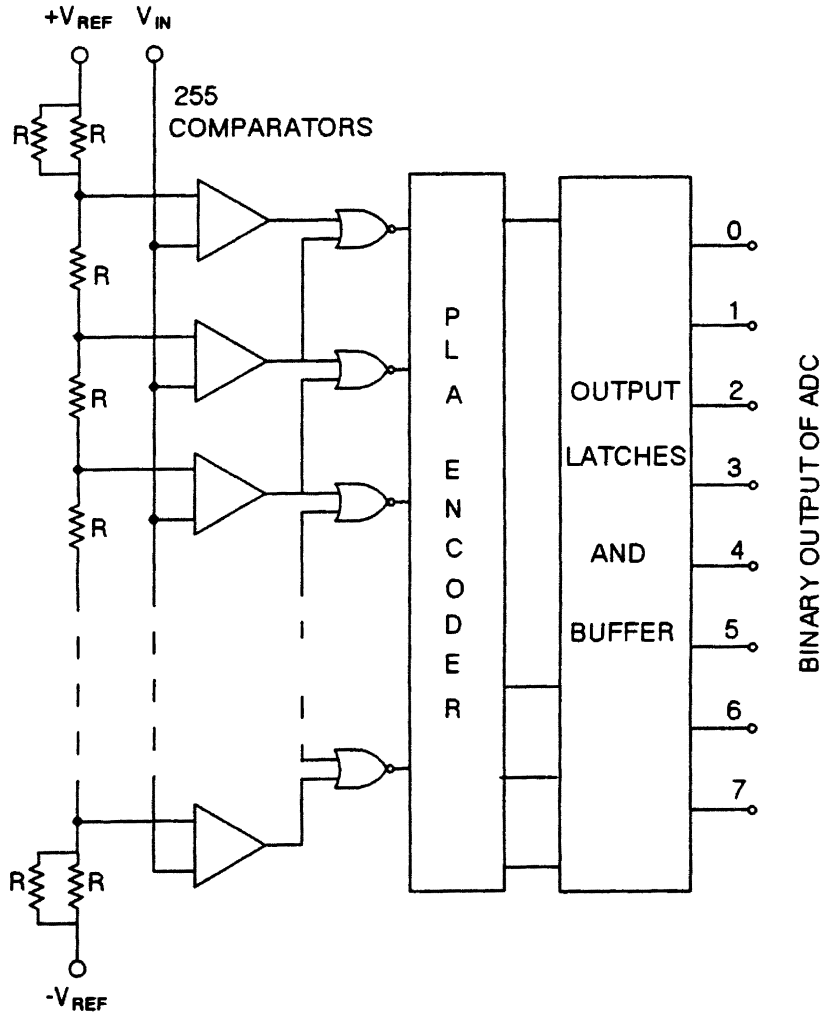


Figure 9. Block Diagram of Radiation Hardened A/D Converter

comparators in a radiation environment requires a circuit design that is insensitive to threshold voltage shifts, increased leakage, and reduced mobility of the MOSFETs. Such a high radiation-immune analog comparator is described in this section.

The comparator design is essential in meeting several specifications, including gain, propagation delay, slew rate, and common mode range, in addition to the associated offset cancellation. The critical comparator performance issues are: high gain and high bandwidth, monotonicity, the power supply rejection ratio, and the charge injection error from the comparator's autozero switches. In order to reject power supply noise and reduce charge injection errors, the circuits are fully differential. To insure monotonicity the comparators utilize an offset cancellation technique which will be explained later. Multistage feedforward comparators are employed in order to achieve fast and high-gain comparators.

The comparator design is centered on meeting several specifications. In general the comparator gain is about 2^n for an n-bit A/D convertor [7], so that it can amplify a voltage that is less than 1/2 LSB up to a compatible logic level. Here a gain of 1000 is desired. The motivation for the gain of 1000 was for future use in a 10-bit A/D converter. As described in Section 2.4.1, a 3-stage comparator with a gain of 10 per stage is employed in this design.

The total error due to the feedback switch charge injection, the offset voltage, the power supply noise, and a mismatch in the reference ladder must be less than 1/2 LSB. Charge injection errors are minimized by: using a fully differential architecture, choosing small feedback switches, and cancelling any residual error as shown in the

next section. The comparator offset voltage must be less than 1 LSB to guarantee monotonicity. This is achieved by storing the offset voltage on the coupling capacitor during the first phase of an autozero cycle as explained in Section 2.4.2.

3.3.1 Analysis of First and Second Stage Comparators

As previously noted, the most speed critical component of a flash A/D converter design is the analog comparator. Under the effects of radiation, the operating point and dynamic range of a conventional CMOS comparator will normally shift so that the device would not operate according to the specified dynamic range, even with autozero techniques. For this reason the use of a conventional CMOS-type comparator is not desirable. To circumvent this problem, a novel all-NMOS differential comparator is employed and is shown in Figure 10. It is similar to a conventional CMOS comparator, except that the active loads are realized using NMOS transistors and all bias currents are independent of radiation exposure. The radiation independent bias circuit will be explained in Section 3.5.

The small signal analysis of the differential-in/differential-out comparator of Figure 10 can be accomplished with the assistance of the model shown in Figure 11. A valid assumption has been made in this simplified model that both sides of the amplifier are perfectly matched. If this condition is satisfied, then the point where the two sources of transistors M1 and M3 are connected can be considered as AC grounded. Assuming that the differential stage is unloaded, the voltage transfer function of this amplifier can be written as follows:

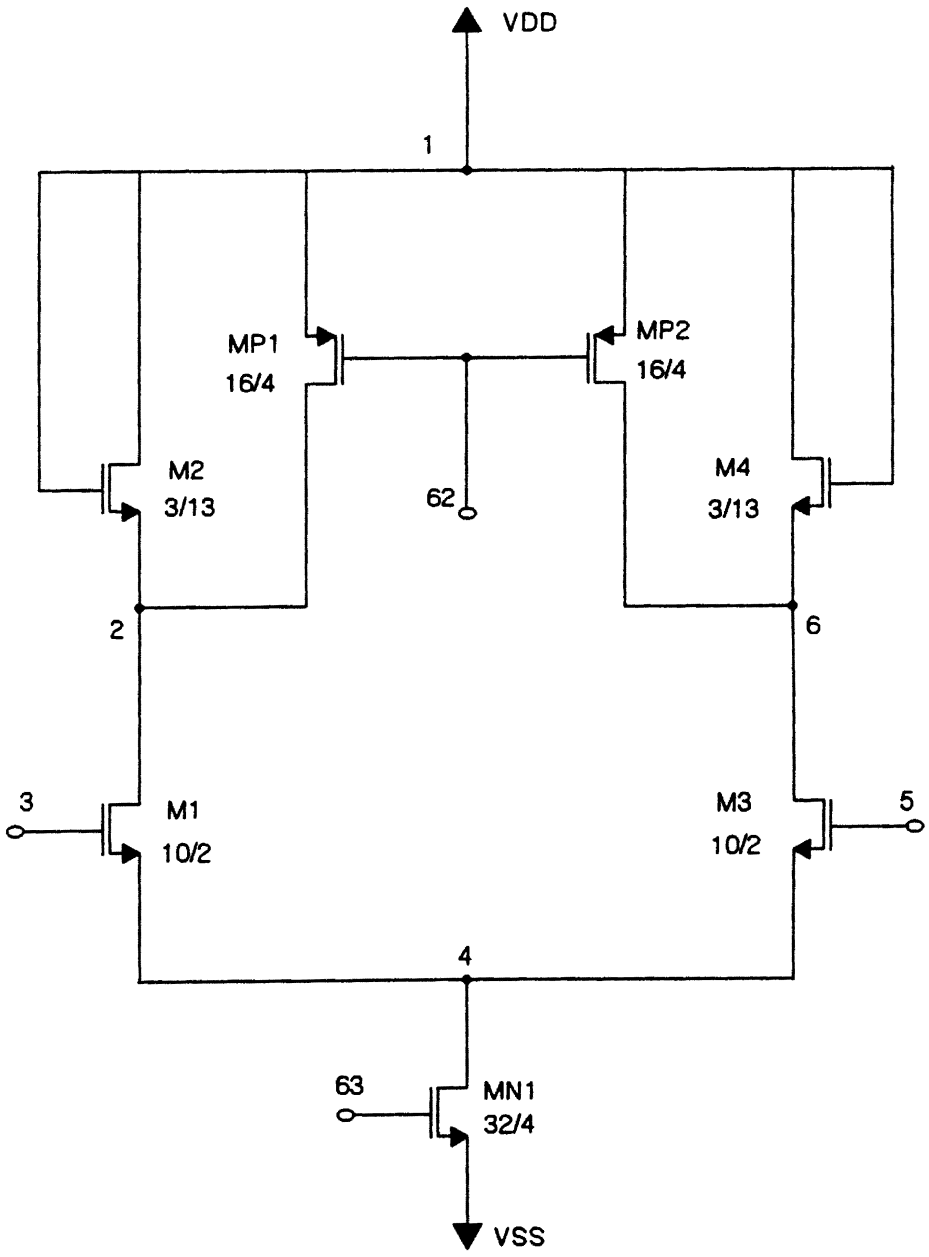


Figure 10. Radiation Hardened Single Stage Comparator

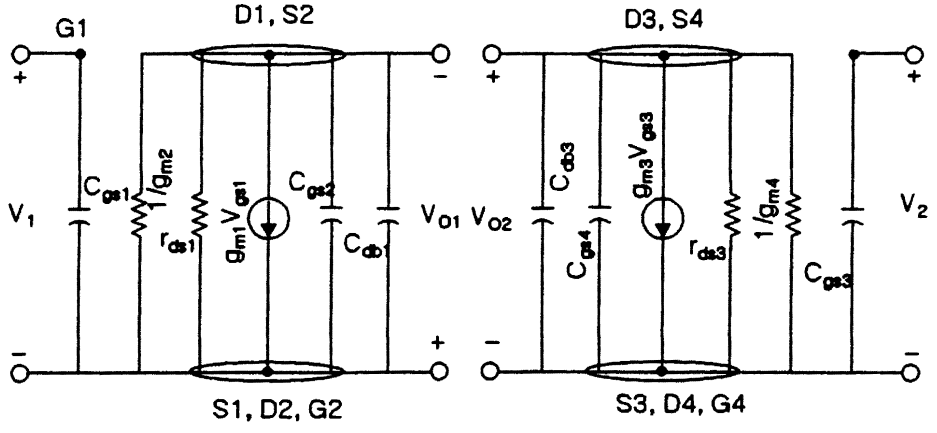


Figure 11. Small Signal Model of the Comparator of Figure 10.

The node equation for the left half of the circuit is

$$g_{m1}V_{gs1}(S) + V_{O1}(S)\,[g_{m2}+g_{ds1}+SC_{gs2}+SC_{db1}] = 0 \qquad (34)$$

where $V_{gs1} = V_1$ and $g_{ds1} << g_{m2}$.

Equation (34) can be written as

$$V_{O1} \simeq -\frac{g_{m1}}{g_{m2}}\frac{\omega_1}{(S+\omega_1)}V_1 \qquad (35)$$

where ω_1 is given as

$$\omega_1 = \frac{(g_{m2}+g_{ds1})}{(C_{gs2}+C_{db1})} \simeq \frac{g_{m2}}{C_{gs2}} \qquad (36)$$

The node equation for the right half of the circuit is

$$g_{m3}V_{gs3} - V_{O2}\,[g_{m4}+g_{ds3}+SC_{gs4}+SC_{db3}] = 0 \qquad (37)$$

where $V_{gs3} = -V_2$ and $g_{ds3} << g_{m4}$.

Equation (37) simplifies to

$$V_{O2} \simeq -\frac{g_{m3}}{g_{m4}}\frac{\omega_2}{(S+\omega_2)}V_2 \qquad (38)$$

where ω_2 is given as

$$\omega_2 \simeq \frac{g_{m4}}{C_{gs4}} \qquad (39)$$

From equations (35) and (38), the differential voltage transfer function can be written as

$$\frac{V_{O2}(S) - V_{O1}(S)}{V_1(S) - V_2(S)} = \frac{V_{out}(S)}{V_{id}(S)} = \frac{g_{m1}}{g_{m2}}\frac{\omega_1}{(S+\omega_1)} \qquad (40)$$

Thus, the first-order analysis of the frequency response of the differential amplifier consists of a single pole at the output given by g_{m2}/C_{gs2}.

The output resistance of the left half of the circuit is

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{1}{g_{m2}+g_{ds2}} \approx \frac{1}{g_{m2}} \tag{41}$$

Similarly, for the right half of the circuit

$$r_{out} = \frac{1}{g_{m4}} \tag{42}$$

The output capacitance of this circuit is

$$C_{out} = C_{gs2}+C_{db1} \approx C_{gs2} \tag{43}$$

From equations (41) and (43), the bandwidth of this circuit is

$$BW = \frac{1}{r_{out}C_{out}} = \frac{g_{m2}}{C_{gs2}} \tag{44}$$

From equations (40) and (44),

$$GBP = \frac{g_{m1}}{C_{gs2}} \tag{45}$$

Thus the following gain, gain bandwidth product, and bandwidth equations describe the performance of the first two stages of the comparator:

$$A_{v1} = A_{v2} = \frac{g_{m1}}{g_{m2}} \tag{46}$$

where g_{m1} and g_{m2} are given as

$$g_{m1} = \sqrt{2\beta_1 I_{D1}} = \sqrt{2K(W/L)_1 I_{MN1}/2} \tag{47}$$

and

$$g_{m2} = \sqrt{2\beta_2 I_{D2}} = \sqrt{2K_N(W/L)_2 I_2} \quad (48)$$

Substituting equations (47) and (48) in (46) results in

$$A_{v1} = A_{v2} = \frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2(1-2X)}} \quad (49)$$

where $X = I_{MP1}/I_{MN1}$.

From equation (44), the bandwidth of this circuit is

$$BW = \omega_{3dB} = \frac{1}{r_{out}C_{out}} = \frac{g_{m4}}{C_{gs4}} \quad (50)$$

Substituting for g_{m4} and C_{gs4} in the above equation results in

$$\omega_{3dB} = (3/2)\frac{\sqrt{2\mu_N C_{OX} I_4 (W/L)_4}}{C_{OX}(WL)_4} \quad (51)$$

Substituting for g_{m1} and C_{out} in equation (45) results in

$$GBP = (3/2)\frac{\sqrt{\mu_N C_{OX} I_{MN1} (W/L)_1}}{C_{OX}(WL)_4} \quad (52)$$

Both the differential transistor and the load are NMOS transistors; therefore, gain (refer to equation (49)) is strictly a function of device geometry ratios and constant current ratios. Only the BW and GBP (refer to equations (51) and (52)) are proportional to the square root of the mobility variation. Therefore, under total dose radiation conditions, this comparator circuit works as desired with some reduction in bandwidth. The comparator, therefore, is designed for more bandwidth than actually required in anticipation of the reduction in bandwidth.

3.3.2 Design of First and Second Stage Comparators

The main requirements in designing this comparator are: a differential gain of 10, a bandwidth of 50MHz, a less than 1mW power dissipation and a minimized layout area. This circuit operates on a ±3.3v dual power supply. The power dissipation requirement limits the current sourced or sunk into the output capacitor to 100uA. Of this 100uA, the current sources MP1 and MP2 supply 40uA each and 10uA flows through each of the active loads M2 and M4. Substituting Av=10 and X=0.4 in equation (49) results in

$$10 = \frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2(1-0.8)}} \tag{53}$$

Substituting L1=Lmin=2μ and W2=Wmin=3μ in the above equation results in

$$\left(\frac{W1}{L1}\right) = \frac{10\mu}{2\mu} \quad , \quad \left(\frac{W2}{L2}\right) = \frac{3\mu}{12\mu} \tag{54}$$

Since the device geometry of both the differential transistors and the active loads is the same, then

$$\left(\frac{W1}{L1}\right) = \left(\frac{W3}{L3}\right) = \frac{10\mu}{2\mu} \tag{55}$$

and

$$\left(\frac{W2}{L2}\right) = \left(\frac{W4}{L4}\right) = \frac{3\mu}{12\mu} \tag{56}$$

The drain current of an NMOS transistor is given by

$$I_D = \frac{K_n (W/L)\ (V_{GS}-V_T)^2}{2} \quad (57)$$

Substituting $V_{GS}=2V_T$, $I_D=100\mu A$ and $K_n=25\mu A/v^2$ in the above equation and simplifying it results in the device geometry of transistor MN1 as

$$\left(\frac{W}{L}\right)_{MN1} = 8 = \frac{32\mu}{4\mu} \quad (58)$$

Similarly, substituting $V_{GS}=2V_T$, ID=40μA, and $K_p=20\mu A/v^2$ in the above equation and simplifying it results in the device geometry of current sources MP1 and MP2 as

$$\left(\frac{W}{L}\right)_{MP1} = \left(\frac{W}{L}\right)_{MP2} = \frac{16\mu}{4\mu} \quad (59)$$

3.3.3 Simulations

The SPICE simulations of the DC transfer characteristics of the first stage comparator along with the differential gain is shown in Figure 12. The second stage comparator is exactly identical to the first stage. This simulation was performed by ramping the differential input voltage from -500mV to +500mV. The output voltage is almost linear for the range -150mV to +150mV of input voltage and a DC gain of 10 is achieved for this range.

The SPICE simulation of the transient characteristics of the first stage comparator is shown in Figure 13. The figure indicates the response of the comparator for a differential pulse signal of ±2mV. The propagation delay was found to be 8ήS. Figure 14 shows the frequency response of the comparator. A bandwidth of 42MHz

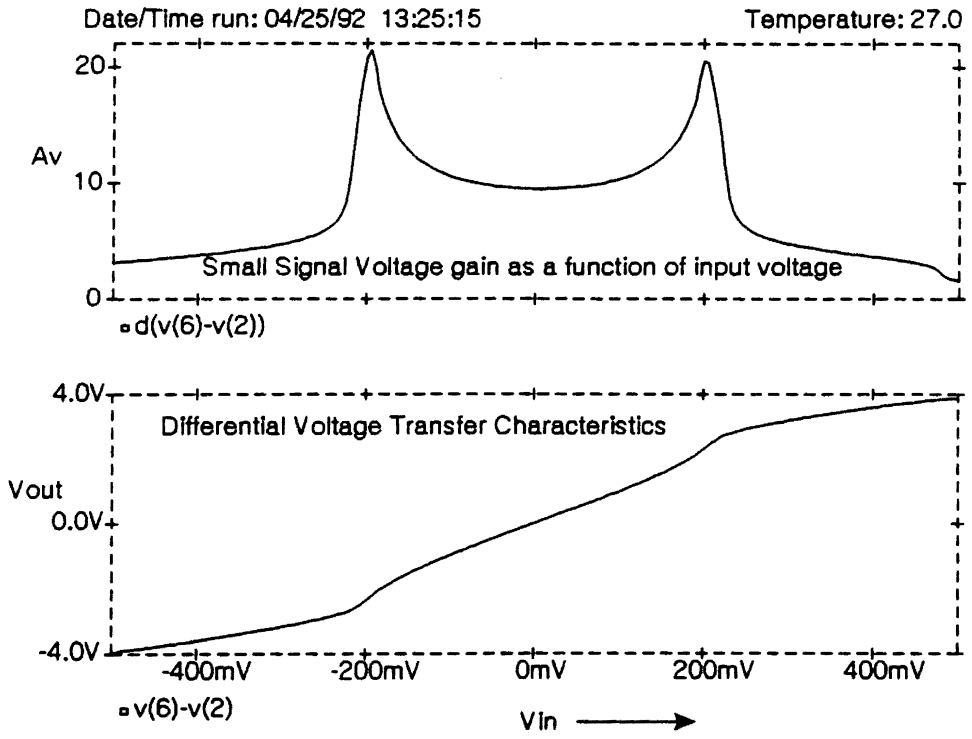


Figure 12. Gain and DC Transfer Characteristics of Single Stage Comparator

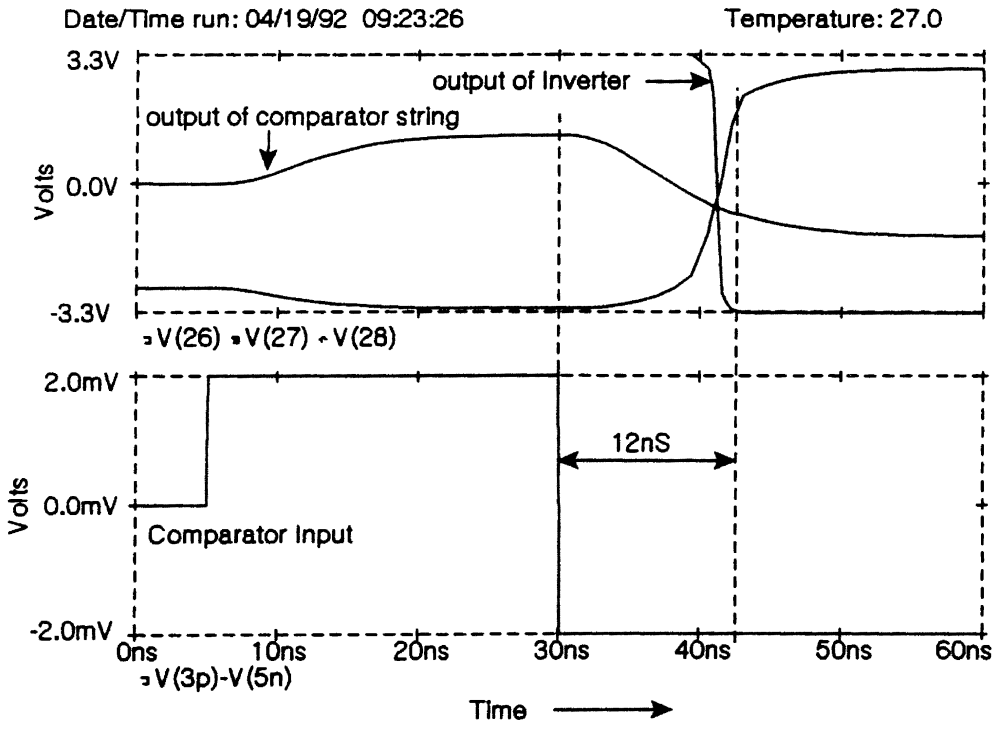


Figure 13. Transient Response of 3-Stage Comparator

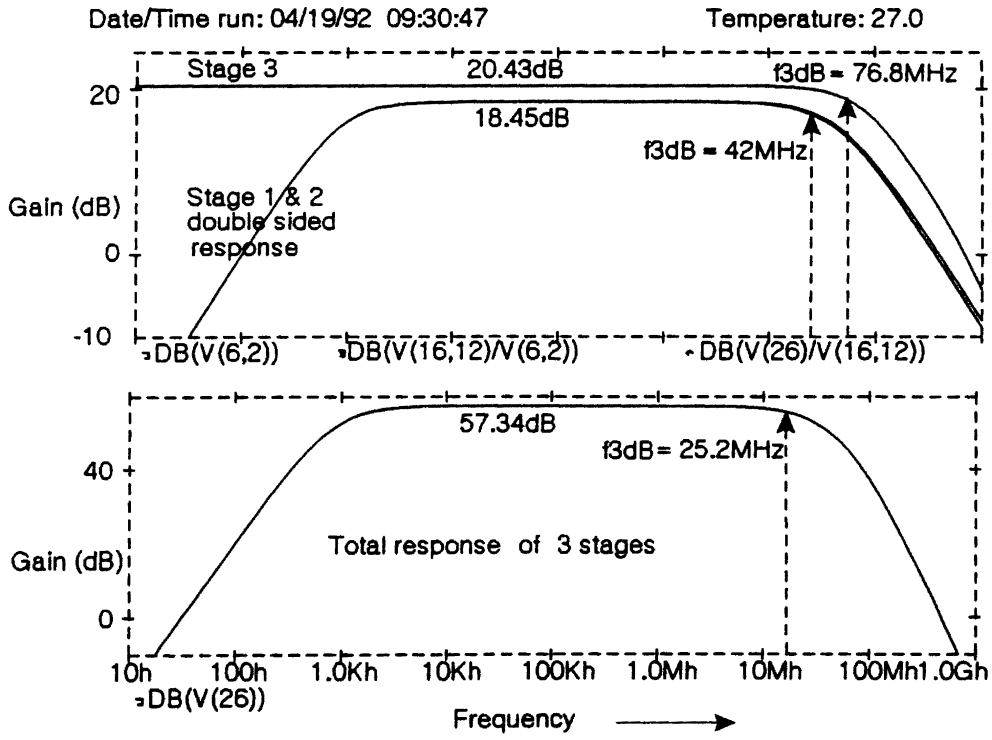


Figure 14. Comparator AC Response

with a gain of 18.45dB is achieved.

3.3.4 Analysis of Third Stage Comparator

The third stage comparator, along with its small signal model, is shown in Figure 15. This is a standard CMOS differential-in, single-ended amplifier. This comparator uses p-channel MOS devices, M2PA and M2PB, as the differential pair. The loads for M2PA and M2PB are obtained from a simple n-channel current mirror. The performance of this comparator is dependent on the threshold shift and mobility variations, unlike the first- and second-stage comparators. Therefore, the third stage comparator should be designed to anticipate performance degradation under radiation exposure as explained in the next section. The node equation for this small signal model (refer to Figure 15) is

$$-g_{mPB}V_{gsPB}(S) + g_{mPA}V_{gsPA}(S) + V_{out}(s)\, g_{dsNB}+g_{dsPB}+SC_{dbNB}+SC_{dbPB}+2\,(S)\,C_{gs} \tag{60}$$

where $2C_{gsMIN}$ is the input capacitance of the inverter connected at the output of the comparator. The above equation is simplified to obtain the differential gain as

$$A_{v3} = \frac{V_{out}(S)}{V_{id}(S)} = \frac{g_{mPB}}{g_{dsPB}+g_{dsNB}} \frac{\omega_3}{S+\omega_3} \tag{61}$$

where V_{id} is the differential input voltage and

$$\omega_3 = \frac{g_{ds3}+g_{ds4}}{C_{dbNB}+C_{dbPB}+2C_{gsMIN}} \approx \frac{g_{ds3}+g_{ds4}}{2C_{gsMIN}} \tag{62}$$

Thus, the first-order analysis of the frequency response of this comparator consists of a

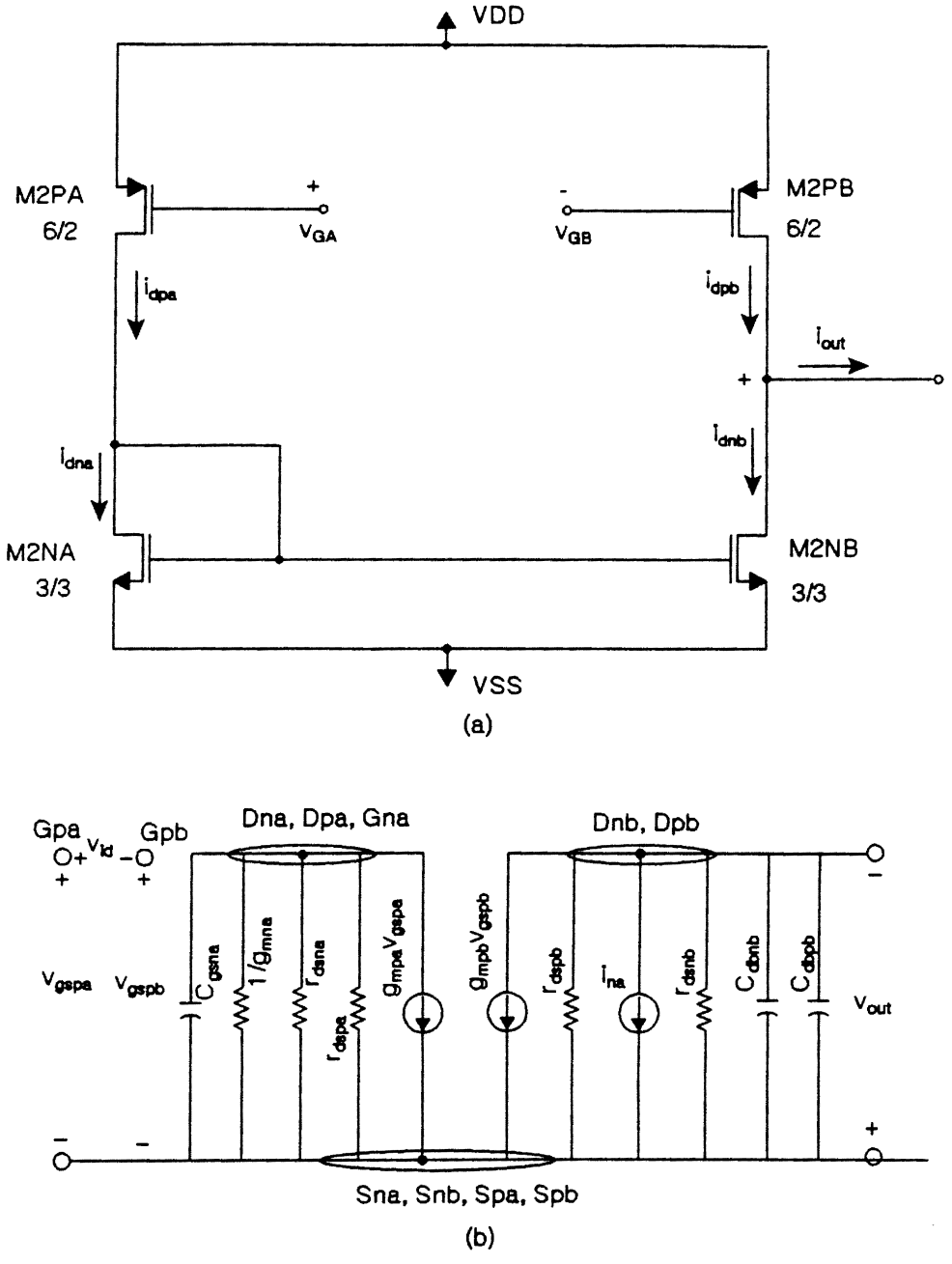


Figure 15. Circuit Diagram of 3rd Stage Comparator along with Small Signal Model

single pole at the output given by ω_3.

The output resistance of this circuit is

$$r_{out} = \frac{1}{g_{dsNB}+g_{dsPB}} \tag{63}$$

The output capacitance of this circuit is

$$C_{out} \approx 2C_{gsMIN} \tag{64}$$

From equations (63) and (64), the bandwidth of this circuit is

$$BW = \omega_3 dB = \frac{g_{dsNB}+g_{dsPB}}{2C_{gsMIN}} \tag{65}$$

From equations (61) and (62) the gain-bandwidth product of this circuit is,

$$GBP = \frac{g_{mPB}}{2C_{gsMIN}} \tag{66}$$

Thus the following gain, bandwidth, and gainbandwidth product equations describe the performance of the third stage comparator:

$$A_{v3} = \frac{g_{mPB}}{g_{dsPB}+g_{dsNB}} \tag{67}$$

where gmPB, gdsPB, and gdsNB are given as

$$g_{mPB} = \beta_{PB}\Delta V_{PB} \tag{68}$$

$$g_{dsPB} = \lambda_P I_{DPB} \tag{69}$$

and

$$g_{dsNB} = \lambda_N I_{DNB} \tag{70}$$

Substituting equations (68), (69), and (70) in equation (67) and simplifying results in

$$A_{v3} = \frac{2}{(\lambda_N+\lambda_P)\,\Delta V_{PB}} \tag{71}$$

Substituting equations (69) and (70) in equation (65) and simplifying results in

$$BW = \frac{(\lambda_P+\lambda_N)\,\beta\,(\Delta V)^2}{4C_{gsmin}} \tag{72}$$

Substituting equation (67) in equation (66) and simplifying results in

$$GBP = \frac{\beta_P \Delta V_P}{2C_{gsMIN}} \tag{73}$$

Since the gain of the third stage comparator (refer to equation (71)) is inversely proportional to threshold voltage, under radiation exposure the gain increases. Bandwidth reduces proportionally to mobility variation and the square of the threshold variation.

3.3.5 Design of Third Stage Comparator

As noted earlier, the bandwidth of the comparator reduces under radiation exposure; therefore, the third stage comparator is designed for a bandwidth of 75MHz instead of 50MHz (required BW) in anticipation of the reduction in bandwidth. Substituting ω_{3dB}=75MHz, λN=0.0345, λP=0.033, KP=20μA/v2, Vgs=2VT, and CgsMIN=8fF in equation (72) results in

Since μN ≈2μP, the aspect ratio of M2NA and M2NB is 1.5; therefore,

$$\left(\frac{W}{L}\right)_{PA} = \left(\frac{W}{L}\right)_{PB} = \frac{6\mu}{2\mu} \tag{74}$$

$$\left(\frac{W}{L}\right)_{NA} = \left(\frac{W}{L}\right)_{NB} = 1.5 \approx \frac{3\mu}{3\mu} \tag{75}$$

3.3.6 Simulations

The SPICE simulation of the DC transfer characteristics of second and third stage (double-stage) comparator is shown in Figure 16. The simulations were done on the circuit given in Figure 17. The simulation was performed by ramping the differential input voltage from -100mV to +100mV. A differential gain of 90 was achieved for the second and third stage comparators together.

The SPICE simulation of the transient characteristics of the second and third stage comparators together is shown in Figure 13. The figure shows the response of the circuit for a differential input signal of 16mV. The propagation delay was found to be 10nS. Figure 14 shows the frequency response of the circuit, and indicates that a bandwidth of 45MHz with a gain of 38.5dB was achieved.

3.4 Three-Stage Comparator Bank

In order to reject power supply noise and reduce charge injection errors, the first two stages of comparators are fully differential and capacitor coupled as shown in Figure 18. Below the circuit diagram is a timing diagram for opening the autozero switches. In this circuit the first two comparators are identical differential-in/ differential-out amplifiers designed in the earlier sections. The third comparator is the

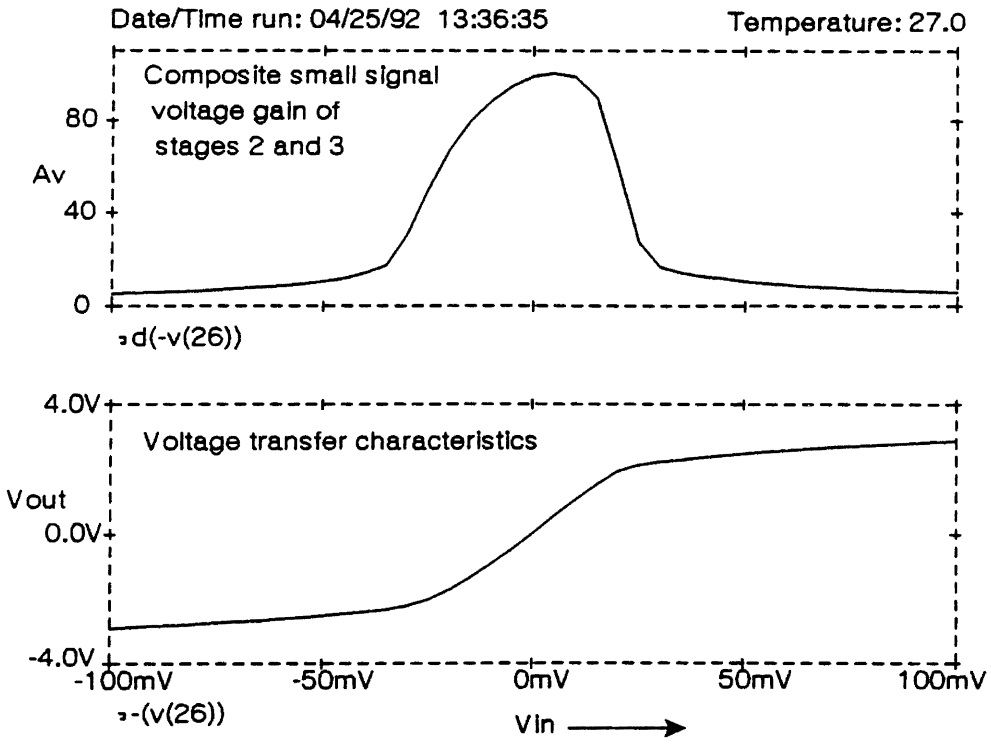


Figure 16. Gain and DC Transfer Characteristics of Double Stage Comparator

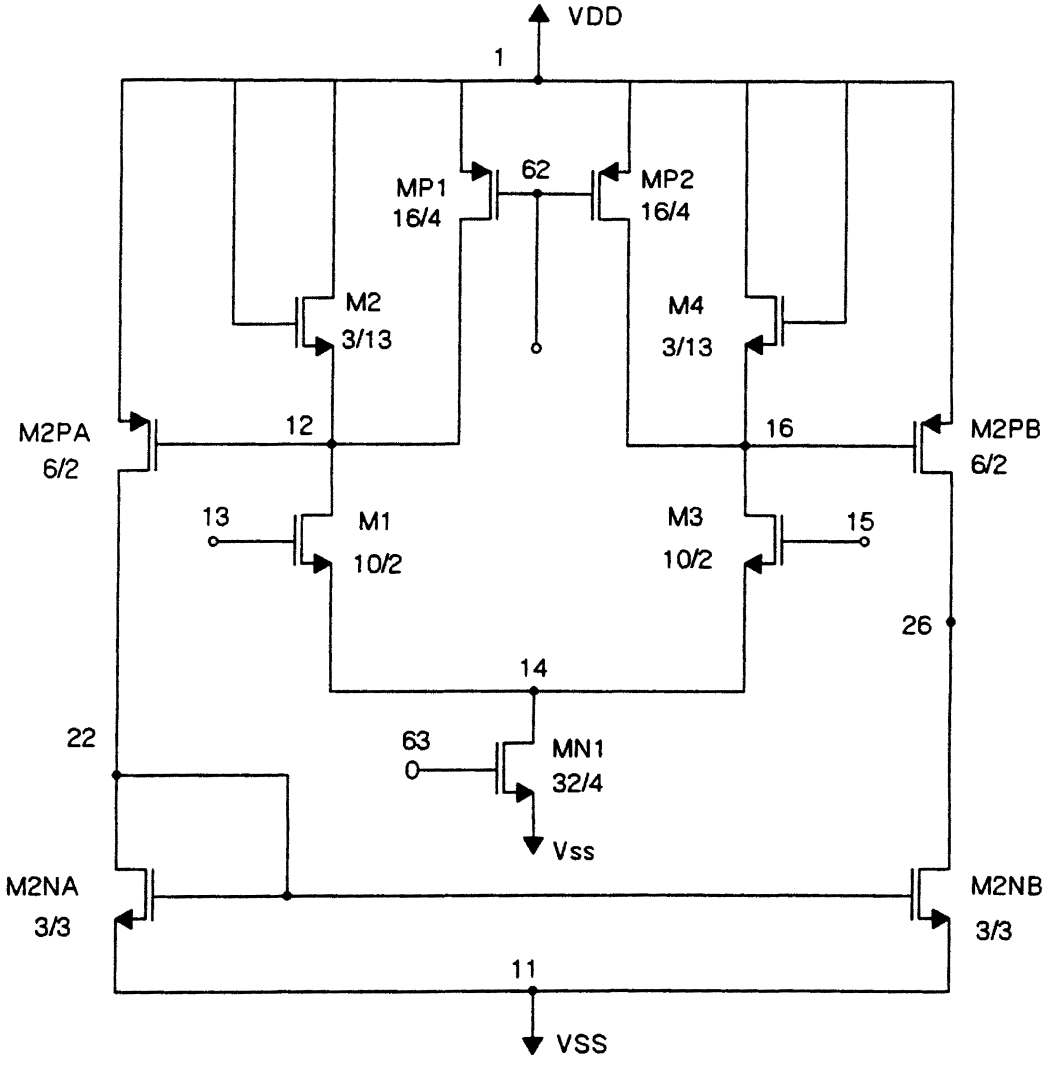


Figure 17. Radiation Hardened Double Stage Comparator

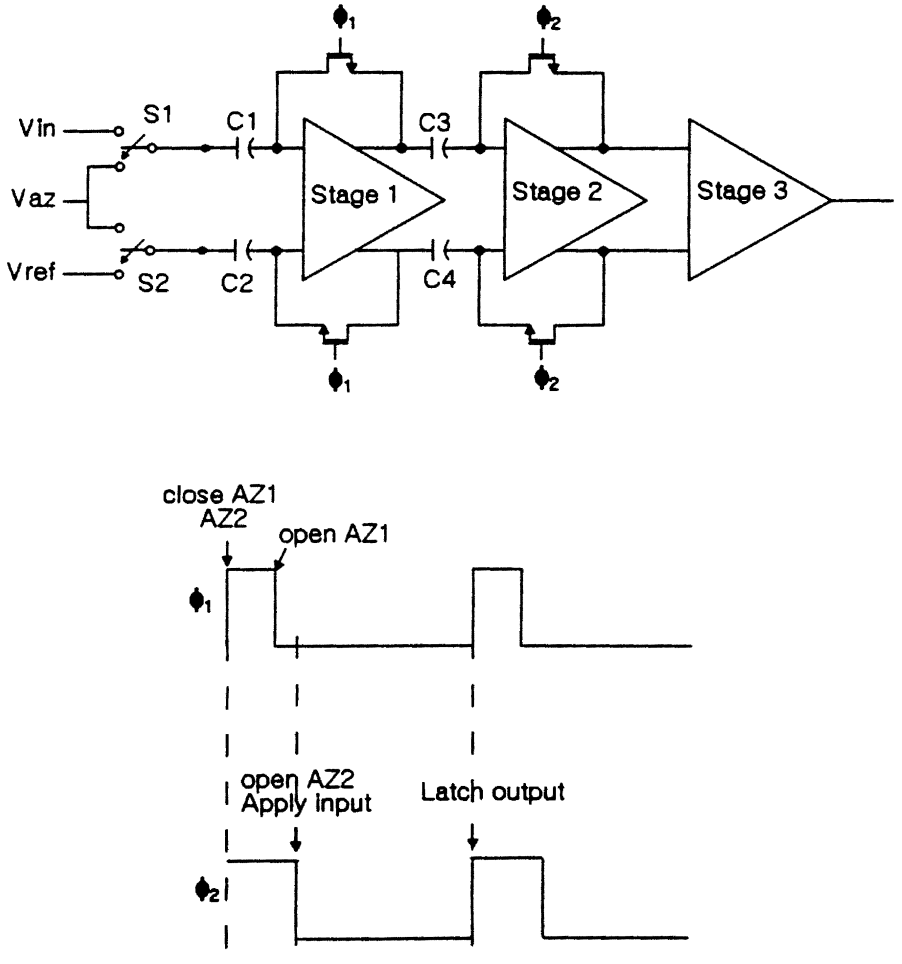
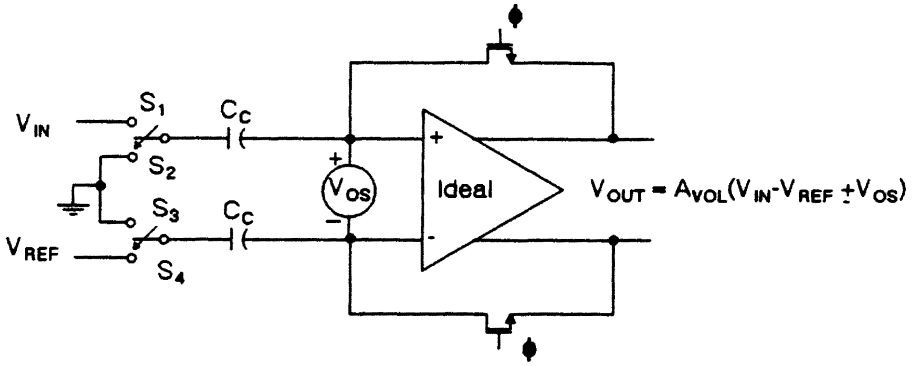


Figure 18. Capacitor Coupled 3-stage Comparator

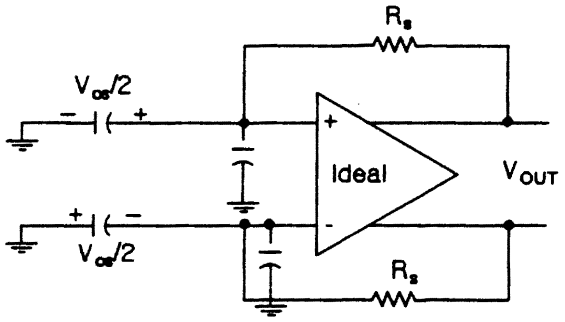
differential-in, single-ended amplifier which was designed in the previous section. This comparator bank has a gain of 10 per stage and a total bandwidth of 50MHz.

Offset cancellation ensures monotonicity for the comparator bank. This offset cancellation method is common to most CMOS flash ADCs [5,7]. First, the feedback switch is closed around each individual comparator, one at a time, storing the comparator's offset voltage on coupling capacitors. At the same time the capacitor input switch is in the autozero position, storing the unknown input voltage on the capacitor. Thus the comparator offset voltage is canceled and does not cause an error. Next, the feedback switches are opened and the bottom-plate switch is thrown to the compare postion. Charge injection due to switch closure results in both differential and common mode errors. By implementing the timing diagram shown in Figure 18 and developed by Allstot (1982), the differential charge injection error from the first stage is canceled. Cancellation of the common mode charge injection error depends on the amplifier's CMRR. When switch $\phi 1$ opens, its charge injection error results in a voltage on the capacitors C_{c1} and C_{c2} and it is amplified by the first stage and stored on capacitors C_{c3} amd C_{c4} before the second feedback switches $\phi 2$ are opened.

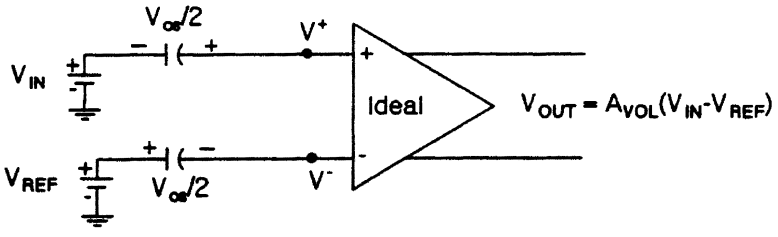
A practical implementation of a fully differential autozeroed comparator is shown in Figure 19(a). This comparator is modeled with an offset voltage source, Vos. Figure 19(b) shows the state of the circuit during the first phase of the autozero cycle when switches $\phi 1$, S_2, and S_3 are closed. Due to the presence of offset voltage, both the capacitors C_{c1} and C_{c2} will be charged equally to a voltage Vos/2 with the polarity shown. Figure 19(c) shows the circuit in the second phase of the autozero cycle when



(a) Setup for the Autozero circuit



(b) Comparator during autozero state



(c) Offset is cancelled by addition of V_{os} to V_{cc}

Figure 19. Autozero Operation

switches S_1 and S_4 are closed. Now the appropriate input and reference voltages will be applied to the circuit. Applying KVL to each arm of the comparator of Figure 19(c) results in

$$V^+ = V_\epsilon - \frac{V_{os}}{2} \tag{76}$$

and

$$V^- = V_{ref} + \frac{V_{os}}{2} \tag{77}$$

The differential output of this comparator is given by

$$V_o = A_v(V^+ - V^- + VOS) \tag{78}$$

Substituting equations (76) and (77) in the above equation and simplifying it results in

$$V_o = A_v(V_\epsilon - V_{ref}) \tag{79}$$

Thus the offset voltage is effectively cancelled. An analysis was performed in Section 2.4.2 regarding the time required for the input signal of the circuit to settle after the autozero switches are closed. Settling time (τ_s) is given by

$$\tau_s = \frac{kR_sC_c}{A_{vol}} \tag{80}$$

Settling time is not readily predictable from other amplifier parameters, such as bandwidth, slew rate, or overload recovery time, although it depends on all of these [23]. The settling time of the comparator is composed of two regions of operation: large signal and small signal. By combining the time in both regions, the estimated

settling time is given by

$$T_S = T_{LS} + T_{SS} \tag{81}$$

where T_{LS} = time due to large signal response, and

T_{SS} = time due to small signal response.

Simplifying the above equation results in

$$T_S = \frac{I_O}{C} V_{FS} - \tau \ln\left(\frac{V_{FS}}{A V_{diff} 2^N}\right) \tag{82}$$

3.5 Radiation-Hardened Bias Circuit

As explained in the Section 3.3.1, the gain of the comparator is a function of the device geometry ratios of differential transistors and of current ratios; therefore, the gain performance of comparators under radiation depends only on the accuracy of the current ratio. Such a bias circuit, which will supply constant current under radiation, is described in this section.

Under the effects of radiation, the operating point and dynamic range of a conventional CMOS voltage reference circuit will normally shift so that the device will not operate according to the specified dynamic range. To circumvent this problem, a bias circuit is employed in the design of the flash A/D converter which will supply a constant current under radiation. The functionality of this bias circuit is based on the current conveyor concept.

Current conveyor circuits began to emerge as an important class of circuits

during the early 70s. They have proven to be functionally flexible and versatile, gaining acceptance as both theoretical and practical building blocks and offering an alternative way of abstracting complex functions. Current conveyors offer several advantages over conventional opamps [27]. The block diagram of a current conveyor is shown in Figure 20, although a detailed discussion of a CC is beyond the scope of this thesis. Class-I (CCI±) and Class-II (CCII±) conveyors have defined properties [26]. A CCII± can be expressed mathematically as

$$\begin{vmatrix} I_y \\ V_x \\ I_z \end{vmatrix} = \begin{vmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{vmatrix} \begin{vmatrix} V_y \\ I_x \\ V_z \end{vmatrix} \tag{83}$$

The above equation states that no current flows into terminal Y; thus terminal Y exhibits an infinite input impedance. The operation of this device is such that if a voltage is applied to the input terminal Y, an equal potential will appear on the input terminal X. Also, an input current on terminal X is conveyed to high impedance output terminal Z. The positive sign denotes that at any instant both I_x and I_z flow into or away from the conveyor, signifying CCII+, while the negative sign denotes the opposite direction of the currents, signifying CCII-.

The radiation-hardened bias circuit is shown in Figure 21. The functionality of this circuit is based on the negative current conveyer (CCII-) principle. The right half of the circuit is a classical bias circuit, while the left half is composed of a radiation-hardened, double-stage comparator that was designed earlier. As mentioned in the design of the comparator, the total current sunk in the circuit is 100μA. For convenience this bias circuit is designed to supply 100μA constant current with

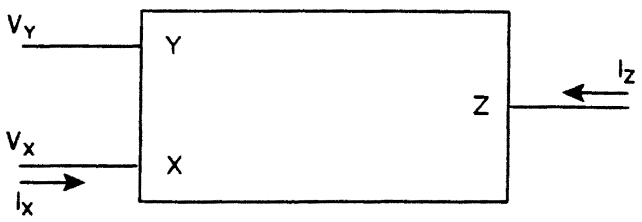


Figure 20. Block Diagram of the CC-II ±

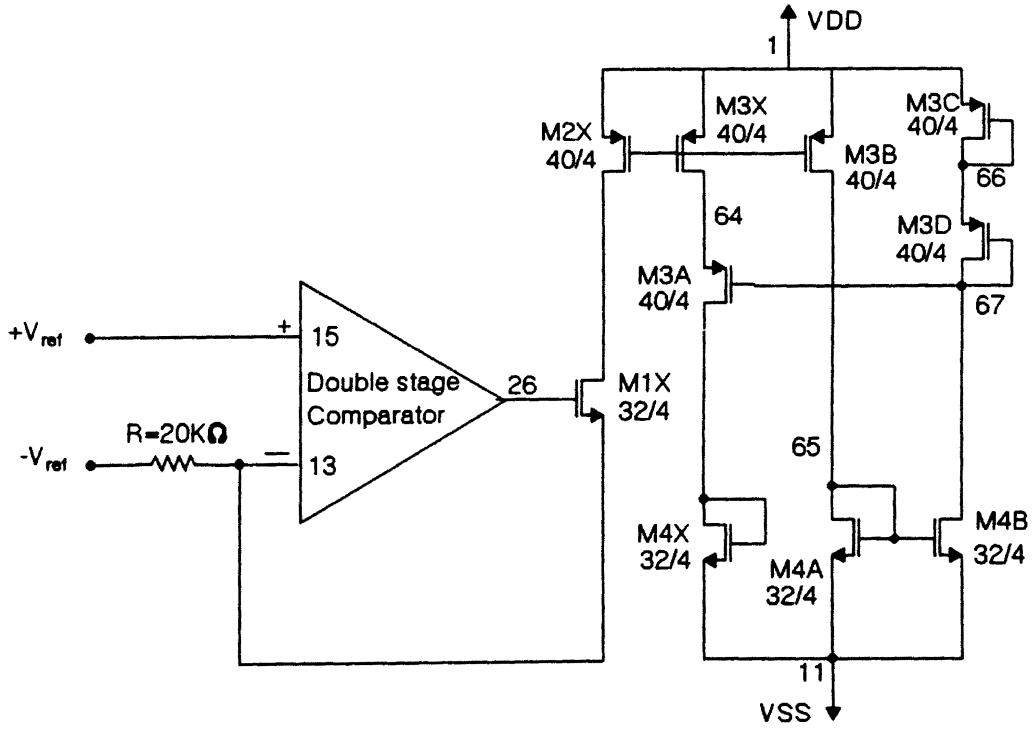


Figure 21. Radiation Hardened Bias Circuit

$V_{DD}+2V_{TP}$ and $V_{SS}+2V_{TN}$ bias voltages for current source and current sink, respectively, in the comparator circuit. In this circuit the accuracy of the constant current under radiation depends primarily on the accuracy of the poly resistor and to a lesser degree, on the opamp gain (see equation (86)).

The left half of the circuit in Figure 21, which is comprised of a NMOS transistor in the negative feedback loop of a comparator, constitutes a negative current conveyer. In this CCII- realization, current is restricted to flow out of terminal X. A voltage source, V_{ref}, is applied to the positive terminal of the comparator and $-V_{ref}$ is applied to the negative terminal through a poly resistor R. As described previously, when a potential V_{ref} is applied to terminal Y of the comparator, an equal potential will appear at terminal X. So the current that flows through the NMOS transistor M1X is the current that must flow through R, which is given by

$$I_x = \frac{V_x-(-V_{ref})}{R} = \frac{2V_{ref}}{R} \qquad \textbf{(84)}$$

This is the current that flows through all the four arms of the bias circuit due to the use of complementary current mirrors. It was decided earlier that I_x should be 100μA and V_{ref} be 1v. From equation (84) the value of R can be found as 20Kohm.

The above equation represents the desired current. The actual current is given by

$$I_x^1 = \frac{V_x+V_{ref}}{R} \qquad \textbf{(85)}$$

From equations (84) and (85), the error in the bias current can be written as

$$\Delta I = \frac{\sqrt{\frac{2I}{\beta}} + V_{TN} + I_O R - V_{ref}}{AR} \tag{86}$$

where I_O is the bias current, A is the gain of opamp, and β, V_{TN}, and I correspond to the transistor M1X. Under radiation the gain of opamp (A) remains almost constant and V_{TN} decreases. So it is clear from the above equation that the accuracy of the bias current depends on the accuracy of poly resistor R.

The operation of this bias circuit (refer to Figure 21) is simple. The current through transistor M1X, which constitutes the first arm of the bias circuit, will be constant (100μA) even under radiation. Of course, the accuracy of this constant current depends on the accuracy of the poly resistor alone. This constant current will be mirrored in the second and third arms through the use of a p-type current mirror. Since the current ratio ($I_{D(M3X)}/I_{D(M2X)}$) of the current mirror depends only on the device geometry ratio of transistors M2X and M3X, it is guaranteed that even under radiation the same current will be flowing in all the first three arms of the bias circuit. The current in the third arm will be mirrored on to 4th arm through n-type current mirror formed by M4A and M4B. Here the diode-configured transistors M3C and M3D are used to generate the bias for cascode transistor M3A. To reduce the channel length modulation (lambda) effect of transistor M4X, the cascode transistor has been used.

Since the bias voltage (V_{BP}) needed for the current sources in the comparator circuit is $V_{DD}+2_{VTP}$, the device geometry of transistor M2X is calculated as follows:

$$I_{D(M2X)} = \frac{K_N}{2}(W/L)_{M2X}(V_{GS}-V_{TP})^2 \tag{87}$$

Substituting I_D=100μA, K_N=25μA/V^2, and V_{GS}=2V_{TP} in the above equation and simplifying results in

$$(W/L)_{M2X} = 10 \tag{88}$$

Since the same current (100μA) is mirrored in all three arms of the bias circuit, the device geometries of the other PMOS transistors will be

$$(W/L)_{M2X}=(W/L)_{M3X}=(W/L)_{M3A}=(W/L)_{M3B}=(W/L)_{M3C}=(W/L)_{M3D}=10=\frac{40\mu}{4\mu} \tag{89}$$

The bias voltage required for the current sink in the comparator circuit is V_{SS}+2V_{TN}. As done for the PMOS transistors, the device geometries of all the NMOS transistors can be found as

$$(W/L)_{M1X}=(W/L)_{M4X}=(W/L)_{M4A}=(W/L)_{M4B}=8=\frac{32\mu}{4\mu} \tag{90}$$

3.6 Ladder Resistor

For the reasons explained in Section 2.3, a resistor ladder is employed to generate voltage reference potentials. This resistor ladder is formed from a linear string of polysilicon with equidistantly spaced contacts providing an input to the CMOS/SOS comparators. The low resistance of the polysilicon ladder network makes it relatively immune to total-dose radiation exposure [5]. In addition, equidistant voltage taps on the ladder makes the network dependent only on resistor ratios rather than on individual resistor values. No ohmic contacts are necessary to connect the ladder

resistors to the differential comparators.

The ladder resistors are made of doped polysilicon whose sheet resistance is 6Ω/sq; the ladder resistor is approximately 8 ohms. The total ladder impedance is 2K ohms. The matching of individual resistors is not critical, but the matching requirement increases for series combinations of these resistors. According to the analysis performed in Section 2.3.2, the matching requirement of the resistor ladder to achieve 8-bit accuracy is 4 percent. This matching requirement is readily accomplished by dividing the resistor string into four equal lengths [20] and locating them in close proximity. This approach reduces the effect of the resistivity gradient across the die.

The comparator bank should be laid out in a straight line configuration [5]. The monolithic design requires that each of the comparators track each other, and the straight line configuration does not produce extraneous boundary conditions that could lead to comparator mismatch and differential nonlinearity.

3.7 PLA Encoder Design

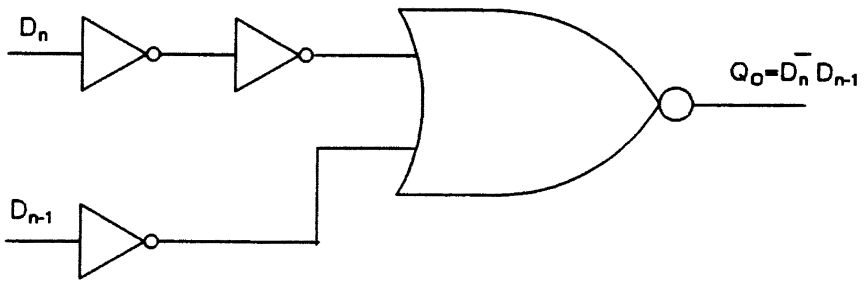
In this A/D converter, 256 comparators simultaneously compare an input voltage with each ladder tap voltage, which is made by dividing the reference voltage through the use of a resistor ladder. The resulting comparator outputs are in a thermometer code: ONEs up to the comparator whose input is the resistor string tap voltage below the unknown input voltage, then ZEROs above the tap that is just below the input voltage. This information is transferred to a series of NOR gates which form the transition detection logic. There a transition point from logical 0 to 1 is detected

by two adjacent comparator products. The transition information, obtained at 255 NOR gates, is converted to an 8-bit binary code by the PLA encoder.

Two CMOS minimum geometry inverters are connected at the output of each comparator string which forms the part of thermometer code discontinuity detection logic. Under radiation the transfer curve simply shifts towards the left, corroborating the previously described threshold variations [5]. The inverter will continue to operate along its region of maximum small-signal gain. As described in Section 2.6, the g_{mn} tends to increase and g_{mp} tends to decrease. Over a limited radiation dose (i.e., up to 1Mrad) the increasing g_{mn} and the decreasing g_{mp} tend to sum to a constant value [5]. However, the post-radiation noise margin of the 0 state will be slightly reduced, while that of the 1 state will be increased, due to uneven shifts in V_{TN} and V_{TP}. But the traditional inverter gate continues to perform with a reduced noise margin.

The outputs of two successive comparators will be fed to a NOR gate which forms the transition detection logic. The input to these 255 NOR gates is in the form of thermometer code. The transition detection logic circuit is shown in Figure 22 along with the truth table. The operation of the circuit is clear from the truth table. All the transition detection logic does is to detect the position of two adjacent comparators whose outputs are different. The output of transition detection logic is fed to the PLA encoder.

The PLA encoder shown in Figure 23 is comprised of two levels of encoding to speed up the encoding operation and the reduction of the parasitic capacitances. This encoder converts the 256 inputs into an 8-bit binary code which feeds the output



Truth table

D_n	D_{n-1}	Q_O
0	0	0
0	1	1
1	1	0
1	0	X

Figure 22. Cicuit Diagram of Transition Detection Logic

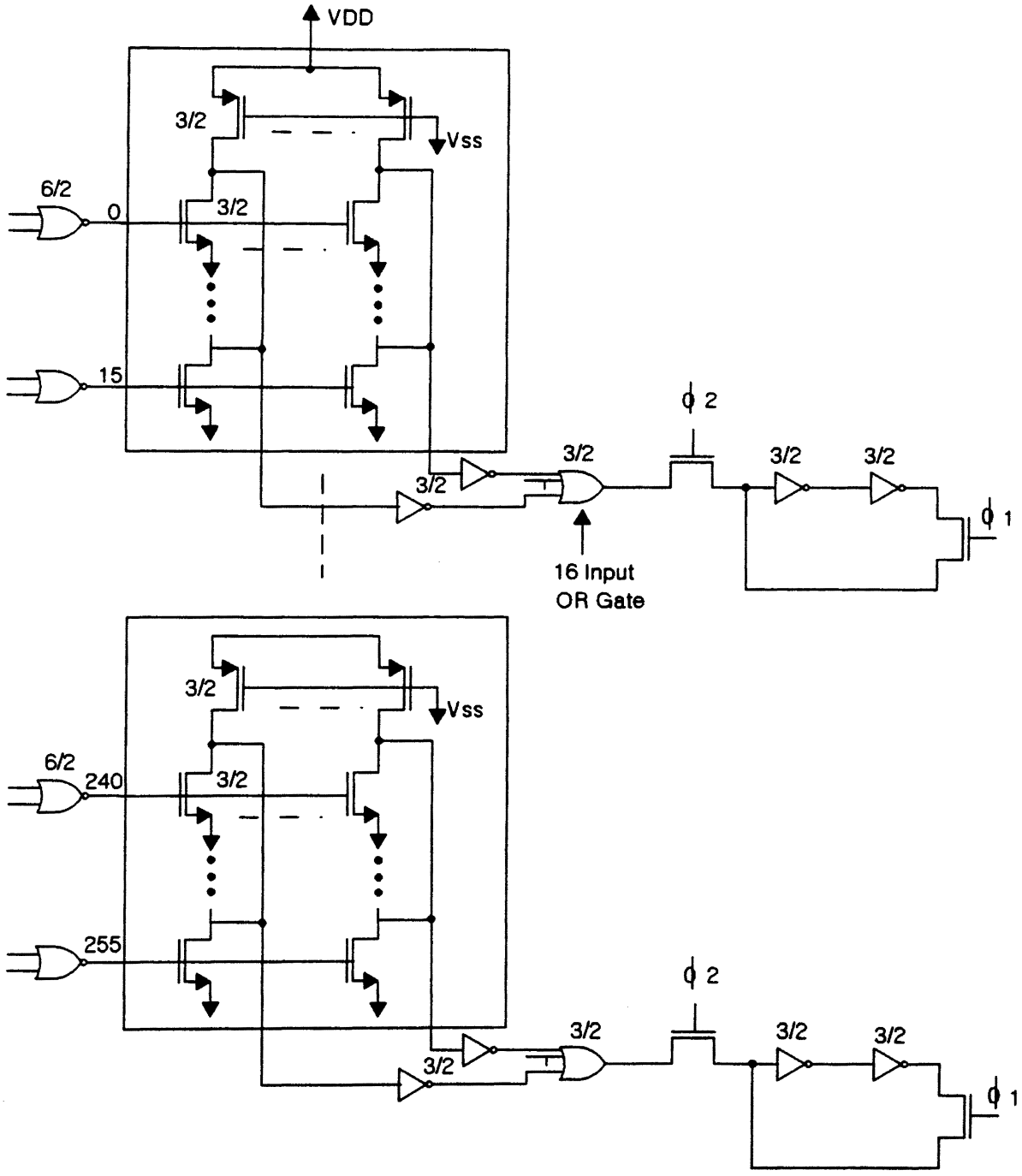


Figure 23. PLA Encoder along with the Latch

buffers. The first level encoder is an OR plane comprised of sixteen 16-to-8 blocks. The second level encoder is comprised of eight, eight-input NOR gates, the outputs of which are the binary outputs of the A/D converter. Finally, the output buffers consist of four stages of inverters with a scale factor of six. The output buffers are designed to drive a 2pF load.

3.7.1 Simulations

The SPICE simulation of the transient response of the PLA encoder along with the tap detection logic are shown in Figure 24. The encoder simulation was realized by lumping all the parasitic capacitances into a single capacitor as shown in Figure 25. The propagation delay of the encoder from simulation was found to be 4nS for a ±3.3v input signal.

The SPICE simulation of the transient characteristics of the output buffers is shown in Figure 26. The propagation delay of the output buffers is 7.2nS. The total delay of the digital circuitry is 7.2nS. Now that the propagation delay of all the building blocks are available, the timing diagram of the flash A/D converter is realized as shown in Figure 27.

Since the comparator delay is 17nS and the encoder delay is 4ns, the A/D converter's output will be available in 21nS. Through the use of a pipelined operation, the A/D converter can easily achieve a 50MHz conversion rate. The autozeroing operation can be pipelined with the result latching. Figure 27 indicates that the A/D operation starts with all the autozero switches closed and the input to the comparators

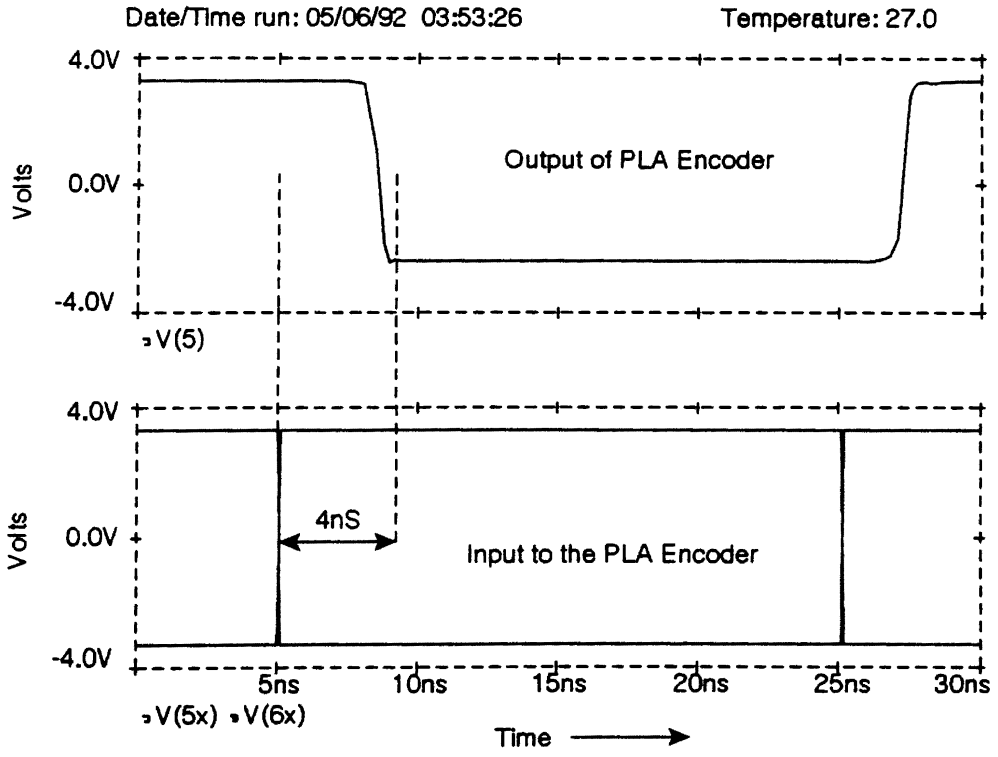
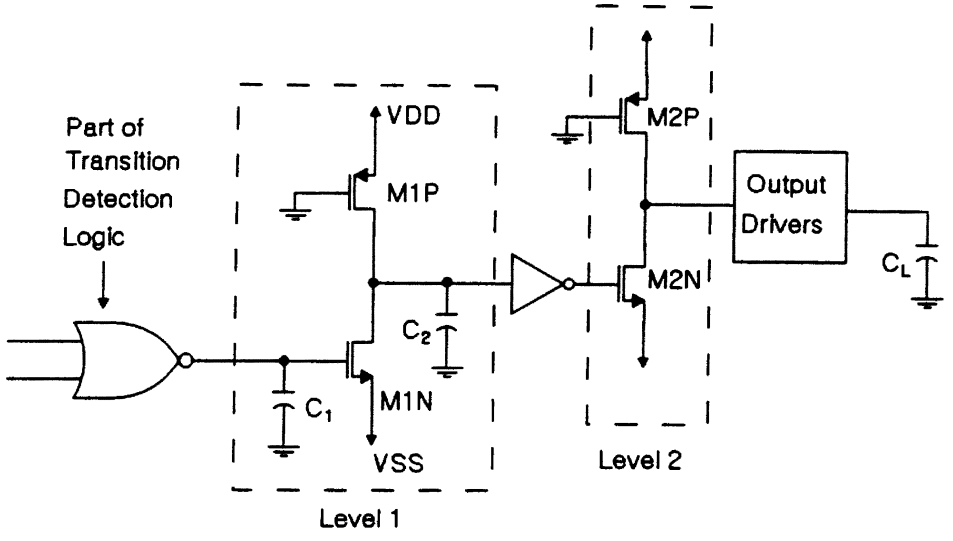


Figure 24. Transient Response of PLA Encoder for a ± 3.3v Signal



C_1 = Lumped capacitance of level 1 = 7 C_{gsMIN}

C_2 = Lumped capacitance of level 2 = 16 C_{db}

C_L = Load capacitance = 2pF

Figure 25. PLA Realization for Simultation Purpose

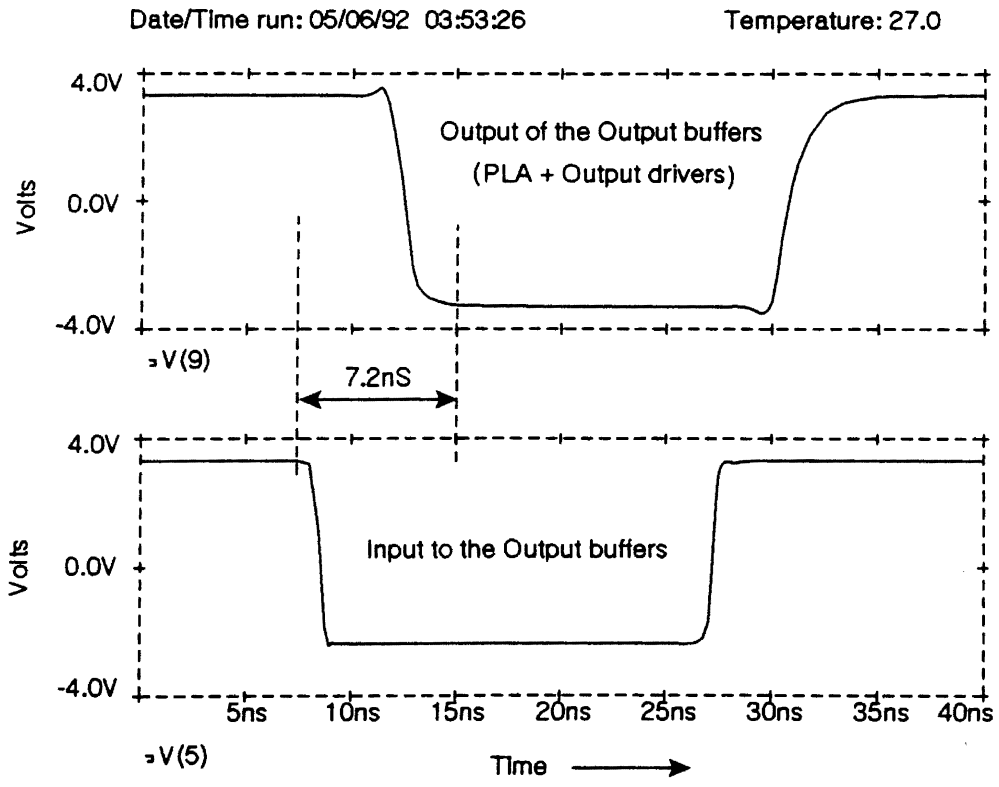
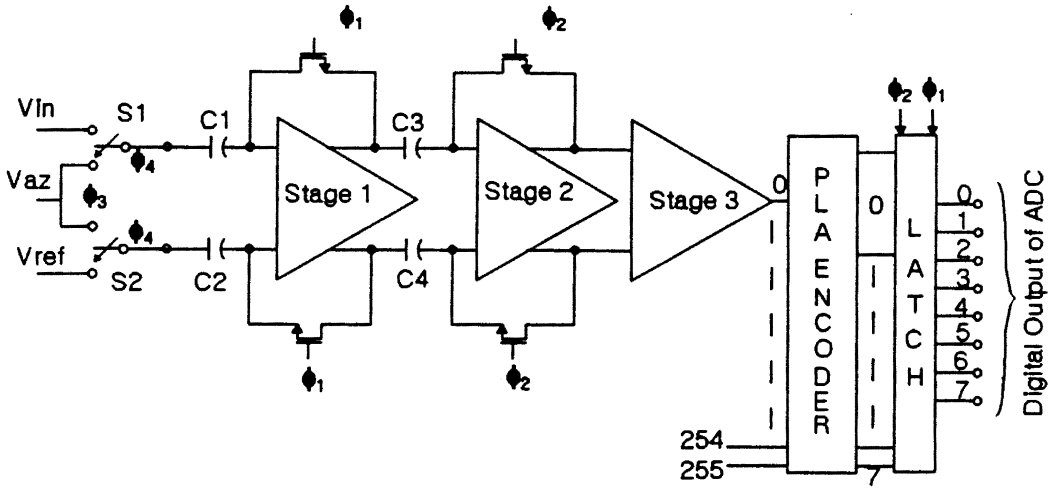


Figure 26. Transient Response of the Digital Circuitry of A/D Converter



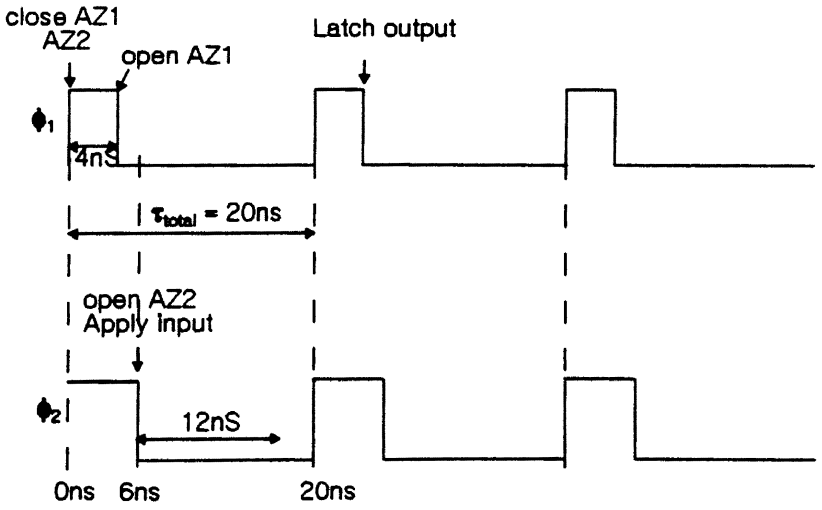
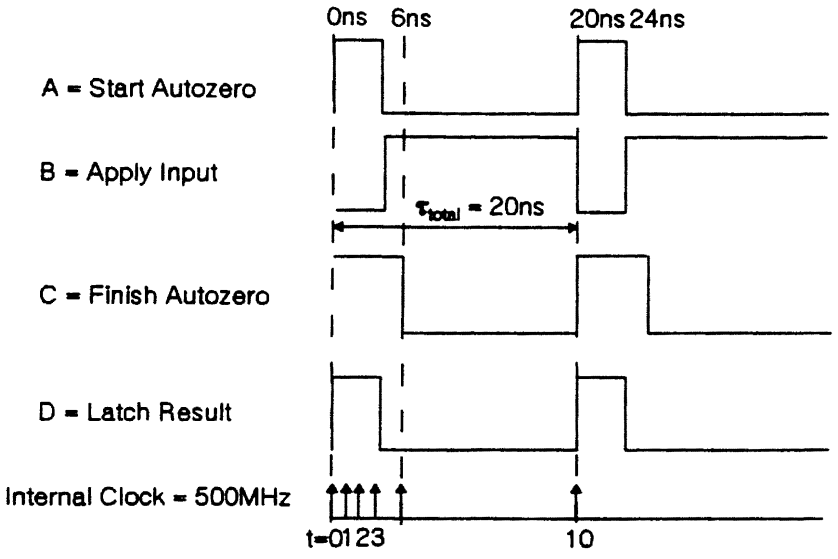


Figure 27. Timing Diagram for the High-speed A/D Converter

connected to ground. The autozero switches of the first stage comparator will be opened after 4nS, while the autozero switches of the second stage comparator will be opened after 6nS. See Section 3.4 for an explanation on autozero operation. From the timing diagram and the state diagram of Figure 28, it is clear that this high-speed, radiation-hardened, 8-bit A/D converter runs at a speed of 50Msamples/s.

3.8 Summary

Table I shows the A/D converter's measured (SPICE simulation) performance characteristics and other key specifications. An 8-bit, 50Msamples/S A/D converter in a radiation environment and fabricated in CMOS/SOS process is now possible with a new, fully-parallel (flash) architecture based on the resistor string. Key to the design was the 3-stage radiation-hardened fully-differential comparator.



Timing diagram

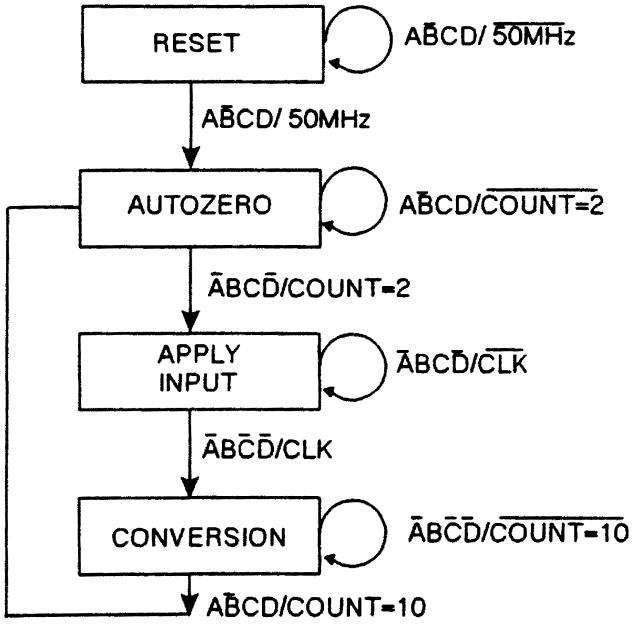


Figure 28. The State Diagram for the Clock Generator and Timing Diagram

TABLE I

HIGH-SPEED A/D CONVERTER PERFORMANCE AND SPECIFICATIONS

Summary	
Resolution	8 bits
Conversion rate	50MSamples/S
Technology	2μ CMOS/SOS
Power supply voltage	±3.3v
Input voltage range	±1v
Linearity	±1/2 LSB
Signal bandwidth	25MHz
Power dissipation at 25MHz clock rate	500mW
Ladder impedance	2KΩ

3.9 8-bit Radiation-Hardened Low-power A/D Converter

The second objective of the thesis is the design of an 8-bit radiation-hardened, "very low power", flash A/D converter. This A/D converter features very low power (less than 10mW), low speed (less than 1MHz) and a total-dose radiation goal of 1Mrad(Si). The design procedure is exactly the same as the design of high-speed A/D converter explained in Sections 3.2 to 3.6. The only two building blocks that differ from the high-speed version are: the design of the analog comparators and the radiation-hardened bias circuit. Therefore, only these two circuits will be discussed in this section.

As discussed in Section 3.3, a three-stage comparator with a differential gain of 10 per stage is employed here. The autozero operation used here is exactly like the one discussed in Section 3.4. Since the power dissipation was the main criteria here, the current sourced or sunk into the output capacitor of the comparator was limited to less than 2μA. The need for such a low current eliminates the use of current sources in the comparator. Basically, the low-power, radiation-hardened comparator consists of two differential transistors, two active loads and a current sink constituting an "all NMOS" design. For the reasons explained in Section 3.3, this comparator would function satisfactorily under radiation environment. This low-power first stage comparator is shown in Figure 29, and the corresponding SPICE simulations in Figures 30, 31, and 32.

The double-stage (second and third stage) comparator is shown in Figure 33. This circuit is similar to the high-power version except for the absence of current

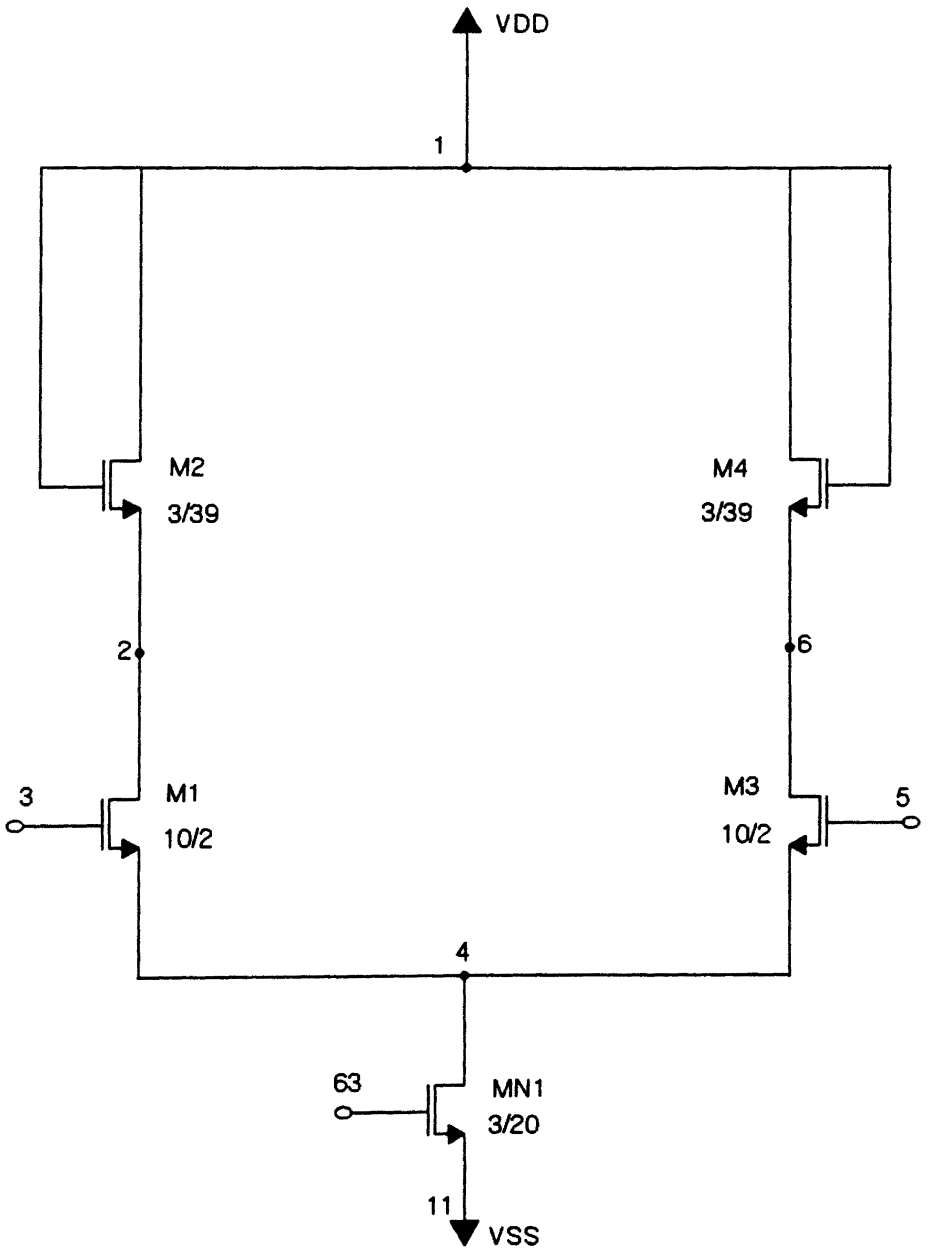


Figure 29. Radiation Hardened Single Stage Comparator

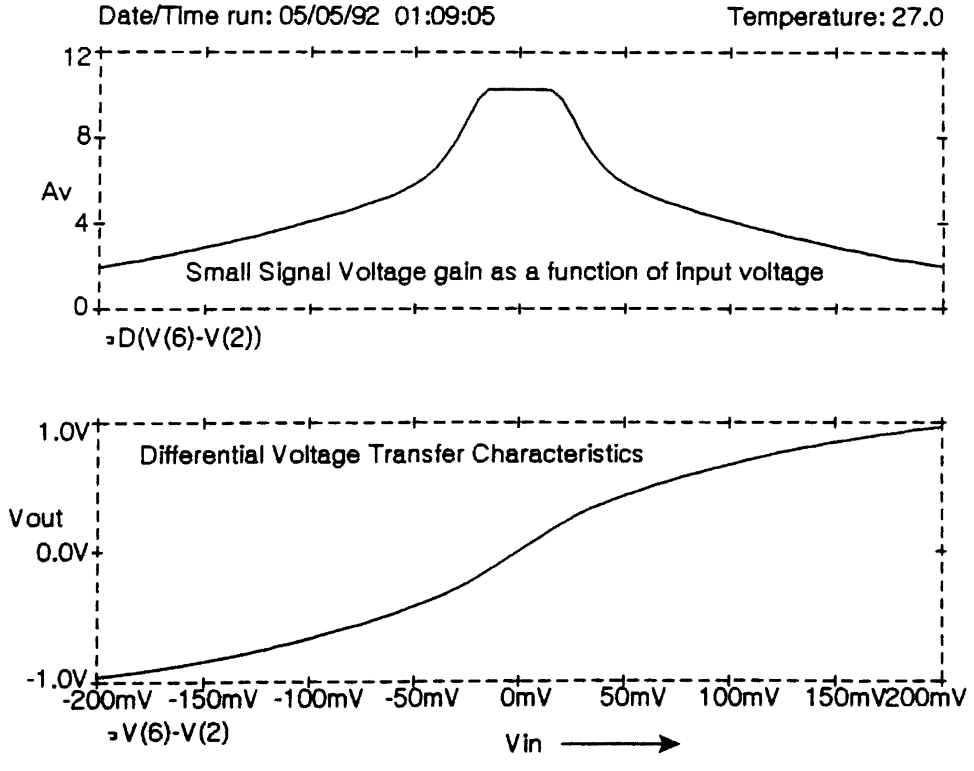


Figure 30. Gain and DC Transfer Characteristics of Single Stage Comparator

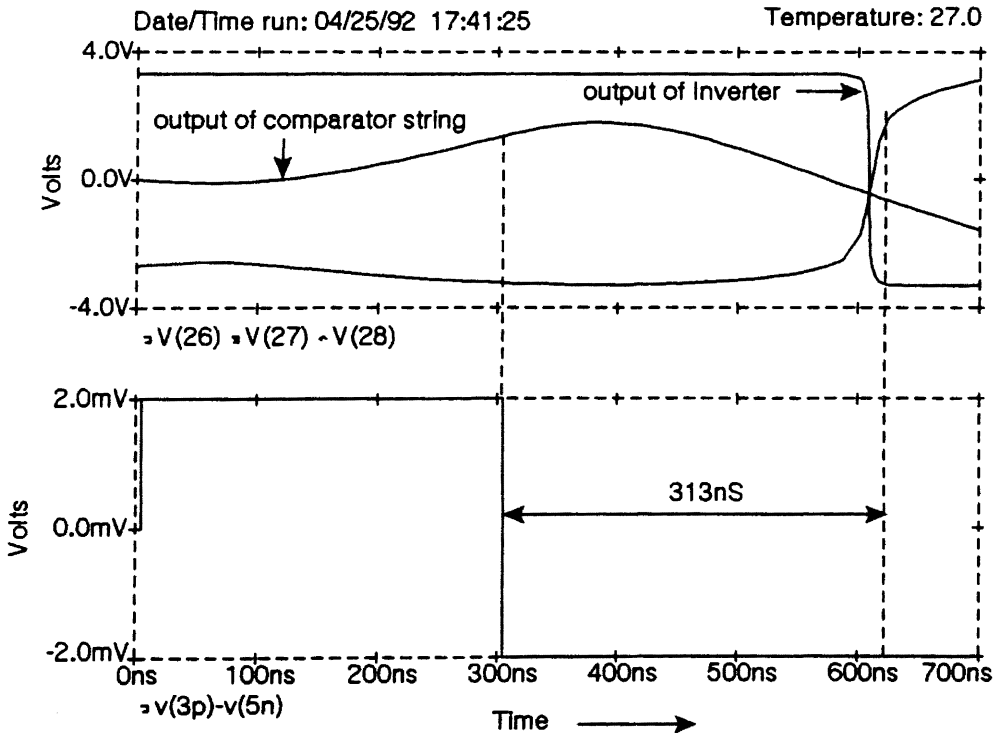


Figure 31. Transient Response of 3-Stage Comparator

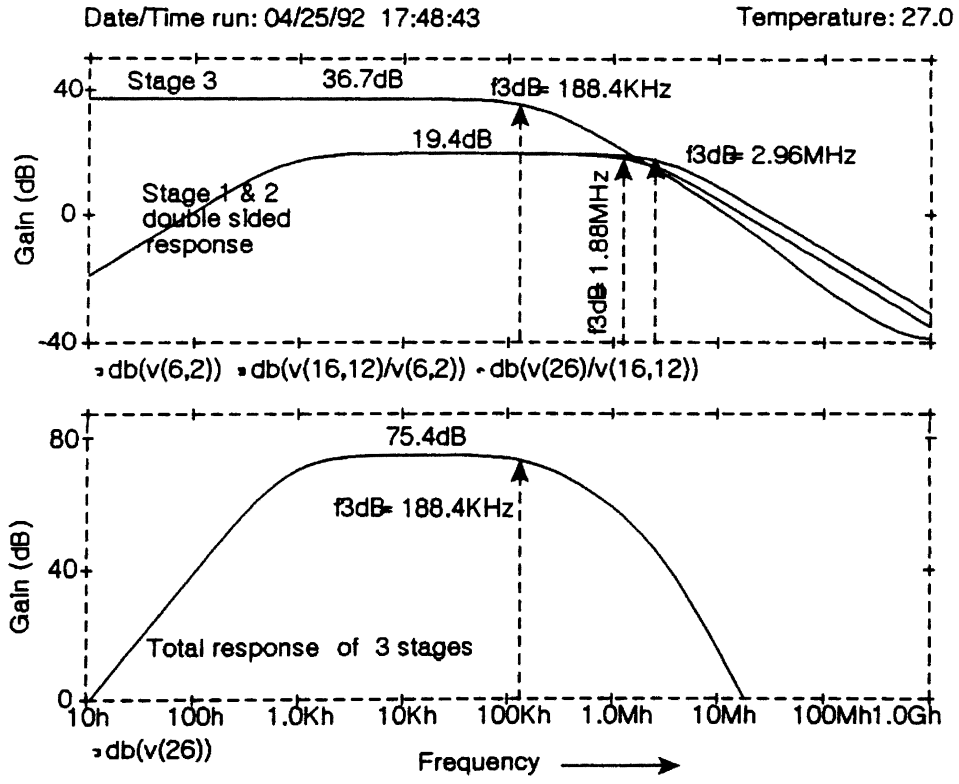


Figure 32. Comparator AC Response

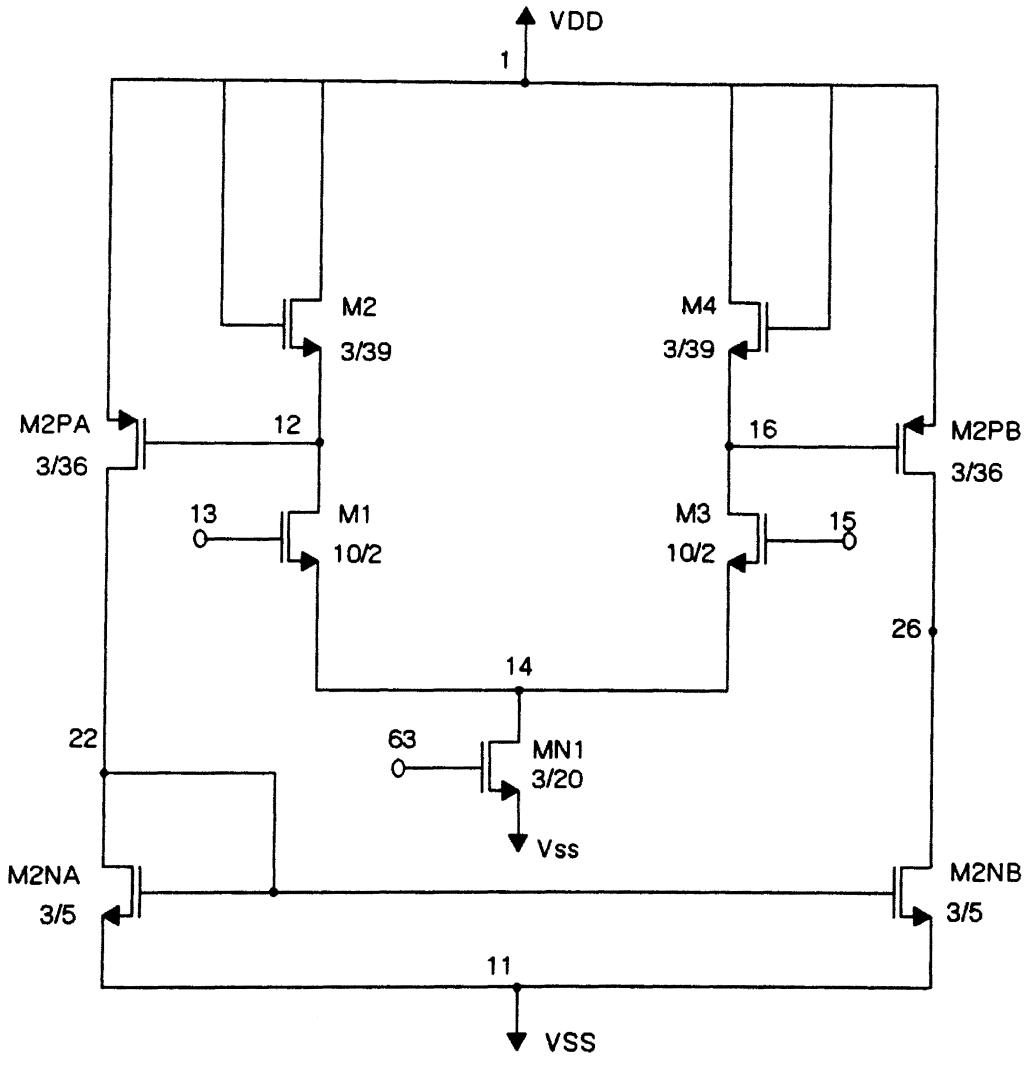


Figure 33. Radiation Hardened Double Stage Comparator

sources. The differential-in, single ended output third stage comparator uses PMOS transistors (M2PA and M2PB) as a differential pair. The loads for M2PA and M2PB are obtained from a simple n-channel current mirror. The performance of this comparator is dependent on the threshold shift and mobility variations, unlike the first- and second-stage comparators. Thus the third-stage comparator is designed to anticipate performance degradation under radiation exposure as explained in Section 3.3.5. The SPICE simulations for Figure 33 are given in Figures 34, 31, and 32.

The radiation-hardened bias circuit is exactly the same as the bias circuit explained in Section 3.5. The only difference is that this bias circuit is designed to supply a constant current of 1.9μA and a bias voltage of $2V_{TN}$. The bias circuit is shown in Figure 35. The transition detection logic and PLA encoder explained in Sections 3.6 and 3.7 are used here also. The timing diagram employed in this A/D converter is shown in Figure 36.

Table II shows the A/D converter's measured (SPICE simulation) performance characteristics and other key specifications. An 8-bit, radiation-hardened CMOS/SOS flash A/D converter which consumes only 10mW power is achieved.

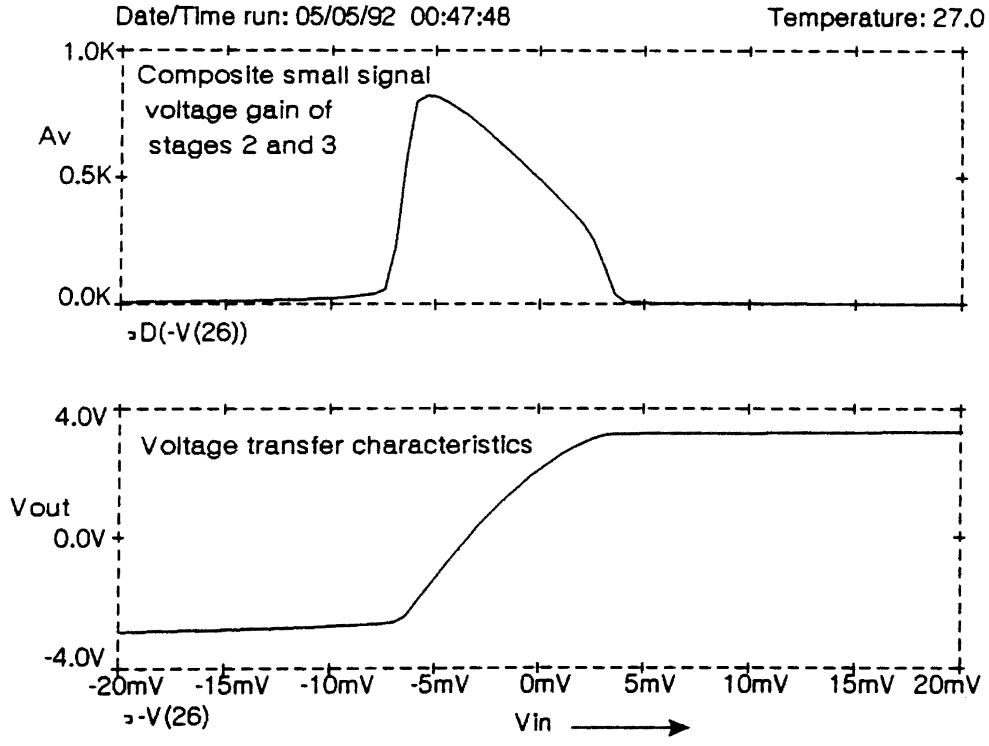


Figure 34. Gain and DC Transfer Characteristics of Double Stage Comparator

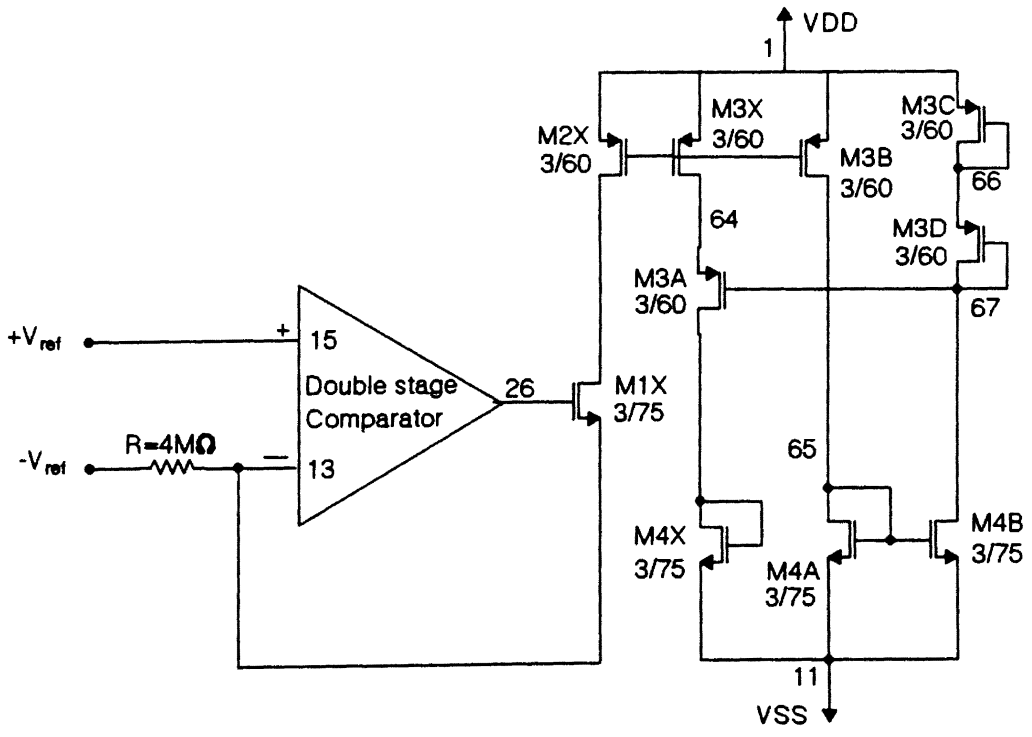
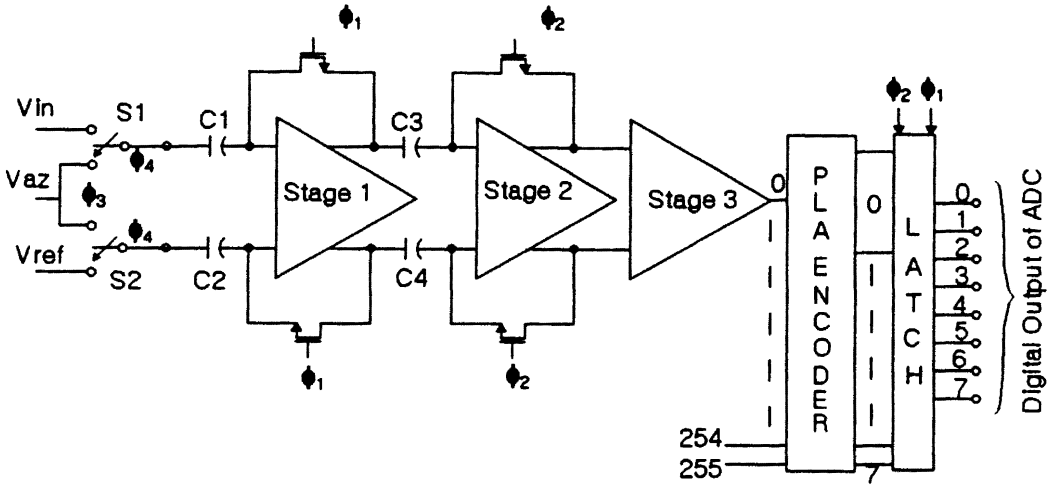


Figure 35. Radiation Hardened Bias Circuit



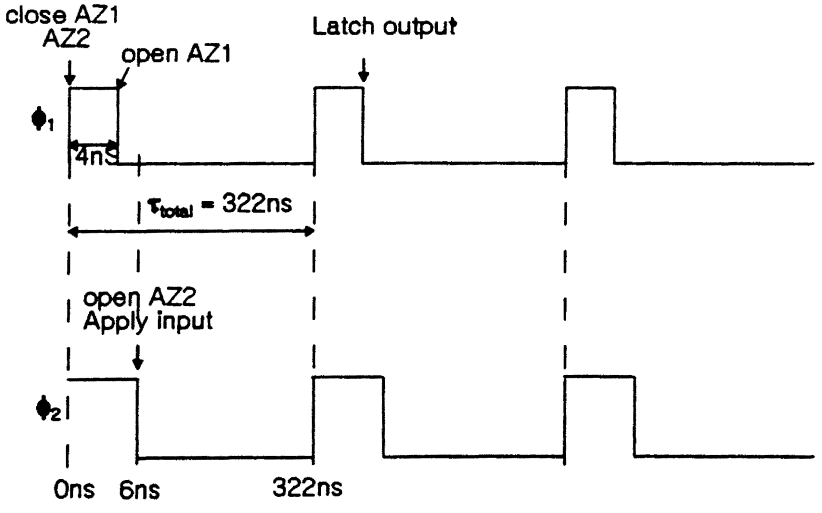


Figure 36. Timing Diagram for the Low-power A/D Converter

TABLE II

LOW-POWER A/D CONVERTER PERFORMANCE AND SPECIFICATIONS

Summary	
Resolution	8 bits
Power dissipation	10mW
Conversion rate	1MSamples/S
Technology	2μ CMOS/SOS
Input voltage range	±1v
Linearity	±1/2 LSB
Power supply	±3.3v
Signal bandwidth	188KHz
Ladder impedance	2KΩ

CHAPTER IV

CONCLUSIONS AND RECOMMENDATIONS

The design of an 8-bit, high-speed CMOS/SOS flash A/D converter has been proposed with a tolerance to total-dose radiation up to 1Mrad(Si). The A/D converter features high-speed (50Msamples/s) operation and low power consumption (500mW). The heart of the radiation-tolerant A/D design is a novel "all NMOS" differential comparator. The comparator is tolerant to voltage threshold variations associated with total-dose radiation.

Also, an 8-bit, very low power CMOS/SOS flash A/D converter has been proposed which is tolerant to total-dose radiation of up to 1Mrad(Si). This A/D converter features a low-speed (1Msamples/s) operation with a power dissipation of only 10mW. The radiation-hardened A/D converter presented here is open to many improvements. The following recommendations have been made for further improvement of the radiation-hardened A/D converter.

There is scope for improvement in the design of the logic gates used in the A/D converter. As discussed in Section 2.5, Chet and others (1992) have proposed a technique for the design of radiation-hardened CMOS logic circuits. This technique has its own drawbacks. A better design technique is required to improve the noise margin of radiation-hardened logic circuits.

The clock generator circuit needs to be developed in accordance to the timing diagram proposed in Section 3.7. The state diagram given in Figure 28 will be helpful in developing the clock generator. This circuit should be immune to a total-dose radiation of 1Mrad.

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