INVESTIGATION AND VALIDATION OF ANALOG FLOATING GATE REFERENCES FOR ADC APPLICATIONS

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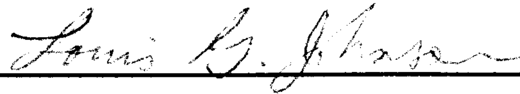

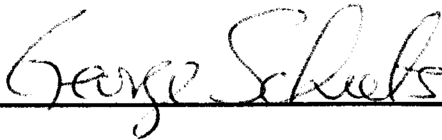

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NOMENCLATURE

$V_{\gamma+}$	Positive programming onset
$V_{\gamma-}$	Negative programming onset
I_{tunnel}	Tunneling current
V_{ti}	Voltage across the tunneling injector
V_{fg}	Voltage across the floating gate
I_D	Drain current
V_S	Source potential
V_T	Threshold voltage
V_{TN}	NMOS threshold voltage
V_{TP}	PMOS threshold voltage
t_{pulse}	Programming pulse duration
Q_{fg}	Floating gate charge
V_{IBK+}	Maximum programming voltage (positive)
V_{IBK-}	Maximum programming voltage (negative)
V_{pgm}	Programming voltage
$Q(t)$	Charge at time 't'

$Q(0)$	Charge at time '0'
ϕ_B	Energy barrier at the polysilicon - oxide interface
γ	Dielectric relaxation frequency of electrons in polysilicon
k	Boltzmans constant
T	Temperature in degree kelvin
t	Charge retention time
T_s	Sampling time
f_m	Frequency
R	Resistance
C	Capacitance
LSB	Least significant bit
MSB	Most significant bit
FG	Floating gate
P_d	Power dissipation
C_L	Load capacitance
V_{DD}	Positive power supply
V_{SS}	Negative power supply
A	Large signal amplification
A_S	Small signal amplification
g_m	Transconductance parameter
R_o	Output impedance
g_{ds}	Drain to source transconductance parameter

V_q	Voltage due to a charge q
I_{DSn}	Drain to source current for NMOS
I_{DSp}	Drain to source current for PMOS
V_{IN}	Input voltage
V_{OUT}	Output voltage
V_{trip}	Trip point voltage
C_{INJ}	Injector capacitor
C_B	Blocking capacitor
C_{gs}	Gate to source capacitance
C_{gd}	Gate to drain capacitance
V_{CTR}	Control voltage
T_a	Amplification time
Q_{OBS}	Observable quantum
t_{LR}	Long term charge retention time
t_{pgm}	Programming time
DUT	Device under test
CLK	Clock signal
V_REF	Reference voltage

CHAPTER 1

OVERVIEW OF ANALOG TO DIGITAL CONVERTERS

Nature is continuous, i.e. analog. One of the important roles of analog circuits in the sub - micron era is the interface between VLSI systems and the physical world.

With progress in portable electronic equipment and scaling down of design technologies, the necessity for low voltage (LV) / low power (LP) circuits has increased greatly, not only for digital circuits but also for analog circuits [1]. In the field of digital video signal processing and data acquisition there has been an increasing requirement for low cost and low power analog to digital converters (ADCs). In applications such as PCS (personal communication systems), cellular phones, camcorders and portable storage devices, low power dissipation and hence longer battery lifetime is a must. Sigma - Delta modulation is currently a popular technique for making ADCs. These oversampled data converters have several advantages over conventional Nyquist converters including insensitivity to analog component imperfections, elimination of quantization noise from the band of interest and reduced accuracy requirements in the sample & hold. Restricting Sigma - Delta approaches to one bit quantizers for second and third order 16 bit systems

requires higher oversampling ratios in excess of 128 and 50 respectively. These values are approximately three times higher for 20 bit systems [2]. Modulator power consumption is directly dependent on the oversampling frequency. Any effort to achieve a significant reduction in power consumption focuses on reducing the oversampling ratio, and using multi - bit quantizers. Thus gaining the benefits of reduced power consumption for both analog and digital components.

The use of multi - bit quantizers is the only feasible approach when high dynamic range at high bandwidths are to be achieved in the light of limitations of oversampling due to process bandwidth (f_T). Floating gate quantizers are the lowest power approach to achieve the goals of high dynamic range performance primarily due to the elimination of the conventional resistor string.

Also the trend of increasing the integration level for integrated circuits has forced the ADC interface to reside on the same silicon with large DSP or digital circuits. By sharing the same supply voltage between ADC and digital circuit, it reduces the overhead cost for extra DC - DC converters to generate multiple supply voltages, however at the expense of greater cost in design and layout. Therefore an ADC operating at the same voltages is desirable.

To achieve the above goals of low voltage (LV), low power (LP) and high speed (HS), CMOS technology is very attractive. The lower cost and higher integration density have made CMOS technology superior over Bipolar. Several LP CMOS design techniques have been developed and by device scaling, CMOS technology can achieve higher speeds which was once reserved for Bipolar process.

1.1 OBJECTIVE

The main objective of this thesis was validation of the floating gate approach to fabricating quantizers for ADCs including Sigma - Delta approaches. The main design and development challenge in realizing these quantizers in silicon was characterization of injector structures. To prove functional and concept feasibility it was necessary to build floating gate injector structures with comparators along with quantizers in silicon for both BULK and SOI technologies. Their performance was to be characterized in the time frame of this research. The characterization of injector structures will demonstrate the suitable models to be used as guidelines in future designs of floating gate quantizers as well as prove the validity of the approach to low power ADC design.

1.2 ORGANIZATION

This thesis is organized into five chapters. Chapter 2 deals with the overview of the floating gate applications. A summary of the literature review is presented along with the theory of the floating gate structure and the mechanism of operation. The characteristics of the injector structure is dealt with in detail. The evolution and overview of ADC systems is covered in later part of the chapter.

Chapter 3 deals with the BULK and SOS ADC architecture implementation. The circuit schematics, design, theory and layout issues of the comparator and injector circuits are presented. Specifications for both the comparators and injectors are also covered.

The test setup for characterization of FG comparator circuits, injector structures along with ADC systems are covered in chapter 4. The later half of the chapter 4 involves characterization results and inferences. A detailed study on the charge retention properties for the circuits is presented along with the results.

Finally chapter 5 discusses the scope of the thesis along with the future prospects and conclusions based on the results obtained by characterization. The results of the feasibility study along with the validity of the approach adopted is presented.

CHAPTER 2

LITERATURE REVIEW AND THEORY

This chapter focuses on the theory of floating gate injectors, factors limiting accuracy of floating gate structures and a literature review of these devices. Finally the flash architecture is reviewed along with schemes for reference voltage generation.

2.1 OVERVIEW OF FLOATING GATE APPLICATIONS

Floating gate (FG) MOS devices have found widespread use in neural networks, and several attempts have been made to develop FG analog memories. The main requirements of these devices is that they must be small, consume low power, be able to accurately control the stored analog data to high degree of resolution and also be able to retain stored charge over a long period of time. An increasing demand exists for these devices in applications where adjustable components are required. They are typically being

used to cancel offsets in differential amplifiers, in adaptive filters and in neural networks for weight storage [5]. It is not easy to control stored analog data with high resolution in FG devices. The data is represented by a certain amount of electric charge on the FG and this charge is injected through a tunnel junction by using Fowler Nordhiem (FN) tunneling process [3]. The tunneling current has nonlinear (exponential) dependence on the junction voltage making fine charge control difficult. It is possible to use feed back circuits for fine control.

2.2 FOWLER NORDHIEM TUNNELING MECHANISM

The FN tunneling mechanism can be explained as follows; there exists an energy barrier of approximately 3.2 eV that prevents electrons in the silicon or polysilicon from entering SiO_2. At room temperature, the electrons can tunnel through only an oxide barrier of 50 A° thickness. If the potential within a 50 A° range of Si / SiO_2 interface is below 3.2 eV, the electrons that tunnel through into the SiO_2 will always return to the Si and no current will flow. However if the electric field in the SiO_2 is strong enough (0.64V/nm), then the few electrons that tunnel into the SiO_2 will be carried away by the electric field and there will be a small current flow away from the Si surface. Increasing the electric field increases the electron flow and thus the electron current. It takes a gate to diffusion voltage of approximately 25V to remove electrons from the gate given an oxide thickness of 400 A°. This voltage is well below the gate oxide breakdown voltage for a given process [17].

The current density through the tunneling injector can be represented by the following characteristic equation as [18]

$$J = \alpha E^2 \exp(-\beta/E) \tag{1}$$

where α and β are characteristic constants given by

$$\alpha = 6.49 - \log(\phi_B) \tag{2}$$

and

$$\beta = 21.0\ (\phi_B^3)^{1/2}\ \text{MV/cm} \tag{3}$$

ϕ_B is the barrier height and E is the electric field. The equation implies that increasing the electric field, increases the current density exponentially. The electric field E is related to the voltage across tunneling oxide by the relation:

$$E = V/t_{ox} \tag{4}$$

where t_{ox} represents the tunneling oxide thickness. The structure is programmed by injecting or removing electrons from the floating gate. This is done by applying a large voltage across the tunneling injector.

2.3 FLOATING GATE DEVICES

Unlike charge trapping devices, the floating gate device has charge stored in a conducting or semiconducting floating layer sandwiched between insulators. Three different types of floating gate devices are discussed in this section.

- Avalanche Injection Floating Gate Device.

- Thin Tunneling Oxide Floating Gate Device.
- Thick Oxide Floating Gate Device.

The first type is distinguished from the other two types by the charge injection mechanism.

2.3.1 AVALANCHE INJECTION FLOATING GATE DEVICE

A well known example of this type of structure is the FAMOS (floating gate avalanche injection MOS). A typical structure is shown in figure (1). FAMOS utilizes charge transport to the floating gate by avalanche injection of electrons from the p-n junction. For a p-channel FAMOS, a reverse p-n junction voltage in excess -30V will cause the onset of high energy electrons from the p-n junction avalanche region to the floating gate. The amount of injected charge is a function of the amplitude of the junction voltage [25]. Due to a relatively thick oxide, this type of device has good charge retention properties. However it is difficult to discharge or erase the stored charge on the floating gate. Also the injecting process is insufficient as only a small fraction of the avalanche current is injected into the floating gate.

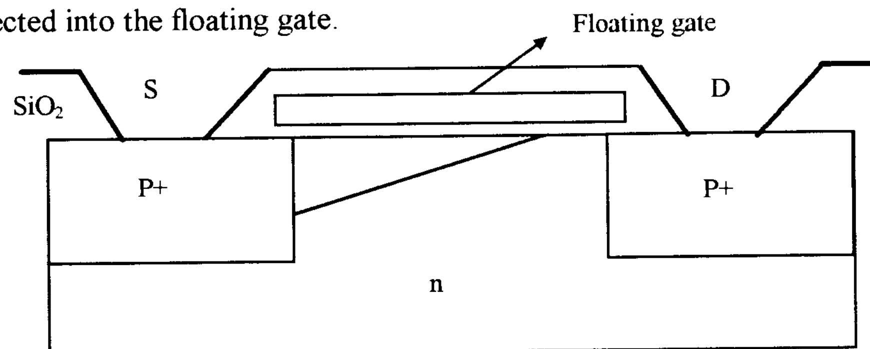

Figure 1: A typical p-channel FAMOS structure.

2.3.2 THIN TUNNELING OXIDE FLOATING GATE (ThinOX FG) DEVICE

The device structure reported in [4] is a floating gate MOS structure, fabricated by a double polysilicon NMOS technology with a thin oxide tunneling region at the drain and an implant under the thin oxide. Poly 1 is the floating gate and poly 2 is the control gate.

Analog Programming : Programming is achieved by applying a large voltage across the gate and drain, while floating the source and substrate to create a sufficiently high electric field across the tunneling oxide for FN tunneling to take place [7]. The tunneling current is predominantly due to electrons. This is because the Si - SiO_2 barrier height is much smaller for electrons than for holes [17]. Depending on the polarity of the programming voltage, the tunneling current either injects or removes electrons from the floating gate. Thus changing the stored analog information and its manifestation as a threshold voltage.

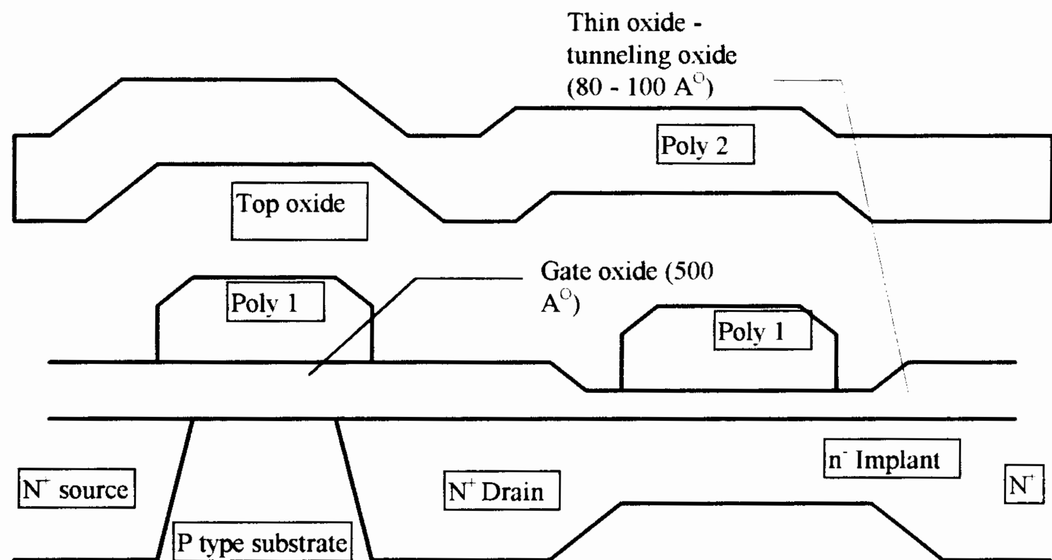

Figure 2: Layout and cross section of ThinOX FG device.

Several modified versions of the structure shown in figure (2) have been reported in the literature. In this particular structure poly1 on the right acts as a charge injection gate and poly1 on the left is the floating MOS gate. Introduction of a high resistance of the order of 150 G – ohm between the floating MOS gate and charge injection gate of the above structure leads to fine control of injected charge up to a resolution of 10 bits [3].

2.3.3 THICK OXIDE DUAL POLY FLOATING GATE (ThickOX DP FG) DEVICE

To fabricate thin oxide FG devices, special fabrication techniques like ultra - thin tunneling oxides are required. Furthermore, very thin tunneling area degrades the retention characteristics [12]. To overcome these drawbacks, the floating gate devices fabricated in a standard CMOS process with thick oxide have been reported by using a geometric trick to enhance the field strength at SiO_2 interface. It is also desirable to avoid the use of the drain of the transistor for programming the floating gate [11].

The bulk device reported here was fabricated using an inexpensive standard double polysilicon technology. Tunneling occurs at the crossover of poly1 and poly2.

A coupling capacitor separates the floating MOS gate from the tunneling injector. Unlike in a capacitor layout the upper polysilicon layer overlaps the edge of the lower layer. The sharp edge of the bottom polysilicon slab causes field enhancement and the thinning of the oxide. A high voltage between the two polysilicon layers causes bi - directional conduction to occur. Appropriate sizing of the transistors - capacitor ratios allows a controlled fraction of the potential developed across the divider circuit to appear

across the oxide layer between the polysilicon layers. The amplitude of the voltage pulse appearing across the oxide layer depends on both the amplitude of the pulse applied to the capacitor divider and on the initial voltage of the floating gate before the pulse was applied [4].

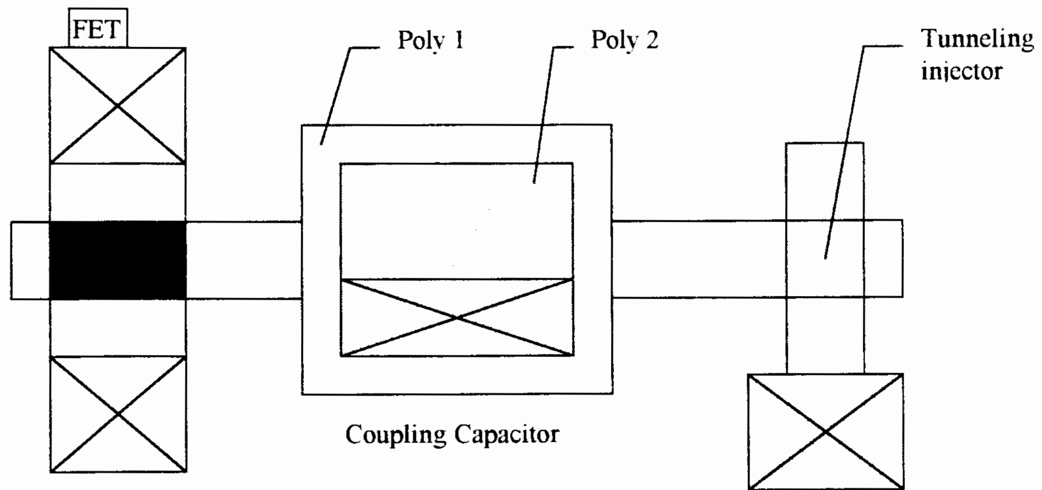

Figure 3. Schematic drawing of the device.

Several modifications of the structure shown in figure have been reported in literature. Use of two tunneling injectors that allows bi - directional programming of devices has been reported [11]. The device had two control gates for measurement purposes. This allowed a measurement of the floating gate charge or the threshold voltage as seen from the control gate without having to disconnect the device [8]. The injector area does not have any effect on the range of programming voltages, however the number of corners and perimeter does have an effect. Increasing the number of corners between poly1 and poly2 from the conventional 4 to 28 resulted in smaller programming voltages as reported in literature [4].

2.3.4 THICK OXIDE SINGLE POLY FLOATING GATE (ThickOX SP FG) DEVICE

The proposed structure uses a single poly and the control gate of these devices is achieved by an N^+ diffusion layer under the polysilicon gate. The device was fabricated in a standard process. The polysilicon rectangle ends in the middle of the N^+ diffusion, the electric field at the corners of the poly rectangle is increased as explained earlier. A field enhancement factor of 2 to 4 has been reported in the literature. This factor is less than the value obtained by using textured polysilicon injector wherein it is suggested that spikes are introduced on the upper surface of the bottom plate of the poly - poly tunneling structure described earlier [17].

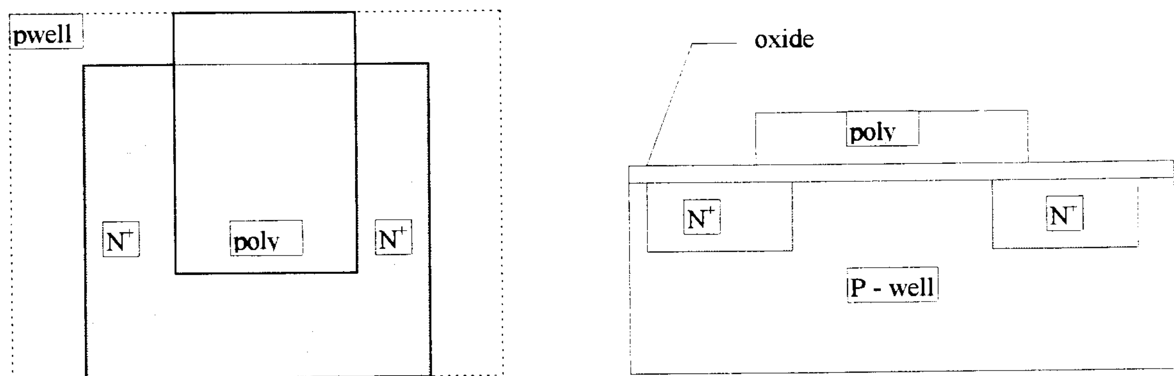

Figure 4. Top and cross - sectional view of ThickOX SP FG injector.

As per A. Thomson in [11], by using field enhancement at the corners of a polysilicon slab over a diffusion region, has the disadvantage of very different programming characteristics, for charging and discharging of the floating gate. The use of poly - island type injector makes the characteristics un - symmetric making bi - directional programming very difficult. However this behavior has not been observed in the devices fabricated on 1.2um NRaD SOS process.

Different types of floating gate devices are available in the literature. Depending on the fabrication process and the application modifications to the types discussed have been developed .

2.4 CHARACTERISTICS OF FLOATING GATE INJECTORS

When FG devices are used for digital memory, they are optimized for small area, high writing speed and low failure rate. In applications like circuit trimming and setting of reference voltages other requirements like accurate control of FG charge and good charge retention properties are important [17]. Typically this requires moderate size injectors to maintain accuracy and high storage capacitor to injector ratio. There are several important properties that must be considered for design of a FG injector circuit [21].

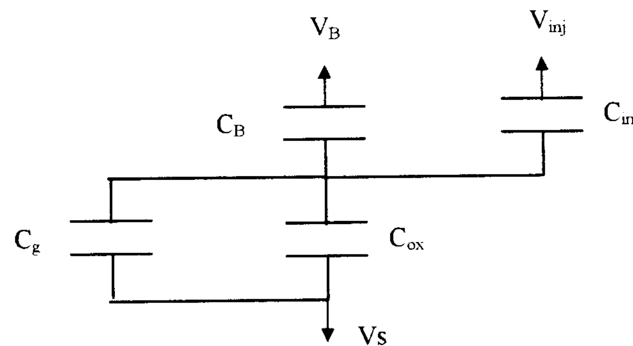

Figure 5. Simplified model of a floating gate MOS device.

In the figure (5) C_B is the capacitance between the control gate and the floating gate (blocking capacitor), C_{inj} is the injector capacitance, C_g is the gate capacitance under the channel of a measuring transistor and C_{ox} is the capacitance between the floating gate

and the substrate. Now the voltage across the tunneling injector can be calculated as a function of the applied voltage V_B and injector voltage V_{inj}.

The writing operation is defined as an operation to tunnel electrons into the floating gate through the oxide. The programming voltage for the operation is determined by the voltage coupling ratio ($K_w = C_B/C_T$) and the internal charges [21].

$$V_{tun} = K_w V_B + Q_{float}/C_T \quad (5)$$

Here Q_{float} represents the stored charge on the floating gate and C_T is the total capacitance given by ($C_T = C_B + C_{inj} + C_{ox} + C_g$).

Similarly for the erase operation the programming voltage is determined by the voltage coupling ratio ($K_e = (C_B + C_{ox} + C_g)/C_T$) and the internal charges [21].

$$V_{tun} = K_e V_{inj} - Q_{float}/C_T \quad (6)$$

For the structure C_B is designed to be an order larger than C_g and C_{inj} is small as compared to C_g. Hence most of the applied voltage V_B appears across the tunneling capacitor by capacitance division.

The main design goal is the characterization of floating gate injector structures. In the following section the properties of injector structures are developed and discussed.

2.4.1 PROGRAMMING ONSET ($V_{\gamma+}$, $V_{\gamma-}$)

This is the minimum programming voltage to initiate charge injection into the floating gate. The tunneling current is controlled by the voltage across the tunneling injector [8].

$$\mathbf{I_{tunnel} = f(V_{ti} - V_{fg})} \quad \textbf{(7)}$$

V_{ti} *is the voltage across the tunneling injector,*

V_{fg} *is the potential of the floating gate.*

The drain current I_D of the FG MOS device can be modeled as :

$$\mathbf{I_D = \beta(V_{fg} - V_s - V_T)^2} \quad \textbf{(8)}$$

β *is the transconductance parameter,*

V_s *is the source potential*

V_T *is the threshold voltage. Equation (8) is valid only for saturation mode.*

Tunneling through SiO_2 exhibits an exponential relationship between programming voltage and tunneling current. A simplified behavior of the tunneling injector is given below [8].

For programming voltages below a 'tunneling threshold' no noticeable charge transfer occurs due to the fact that in this region the exponential is practically zero. The effects are considered on the same level as leakage. Including the leakage factor into the Fowler Nordhiem equation discussed earlier, we get

$$\mathbf{J = \alpha E^2 \exp(-\beta/E) + G_S V} \quad \textbf{(9)}$$

where G_S is the leakage resistance per square area and V is the programming voltage. At programming voltages less than the onset of programming the leakage term dominates and this is normally for small values programming voltage. At the onset of charge injection into the floating gate the exponent dominates. This value of programming voltage is defined as programming onset $V_{\gamma+}$ & $V_{\gamma-}$ for charging and discharging respectively and it is the point of departure from the ohmic or resistive region of the injector.

For high programming voltages tunneling occurs until the voltage across the floating gate is at the tunneling threshold / programming onset. If the programming pulses are of long enough duration that is :

$\mathbf{I_{tunnel} \; X \; t_{pulse} >> Q_{fg}}$.

For this case tunneling will happen until :

$$\mathbf{V_{fg} - V_{ti} = V_{\gamma+}} \quad \textbf{(10a)}$$

or

$$\mathbf{V_{fg} - V_{ti} = V_{\gamma-}} \quad \textbf{(10b)}$$

For intermediate voltages incremental charge transfer occurs according to the exponential relationship. In reality there is a small tunneling current flowing when the programming voltage is slightly below the programming onset. This current is similar to the charge leakage from the floating gate. It is of no importance during programming, but is crucial for long term accuracy expectations [8].

The underlying idea of operation is that although high voltages are required for tunneling it is actually a low voltage range required to control tunneling. A wide range of voltages exists in which no tunneling occurs.

The dead band can be described as:

$$\mathbf{I_{tunnel} = 0 \text{ for } V_{\gamma+} > V_{fg} - V_{ti} > V_{\gamma-}} \quad (11)$$

2.4.2 MAXIMUM PROGRAMMING VOLTAGE (V_{IBK+}, V_{IBK-})

This is the maximum programming voltage that can be applied to the tunneling injector without breakdown of the oxide. This depends on the quality of the oxide. Refer to figure 6 for plot of ln(programming current) +/- ln(Ipgm) and programming voltage +/-Vpgm. As can be seen the plot has a dual slope. The programming onset and maximum programming voltage parameters are marked. The tunneling currents are normally of the order of pA. FN tunneling current increases with increase in applied voltage. The dual slope on the characteristic can be attributed to the field enhancement tunneling currents occurring at the onset of the tunneling process.

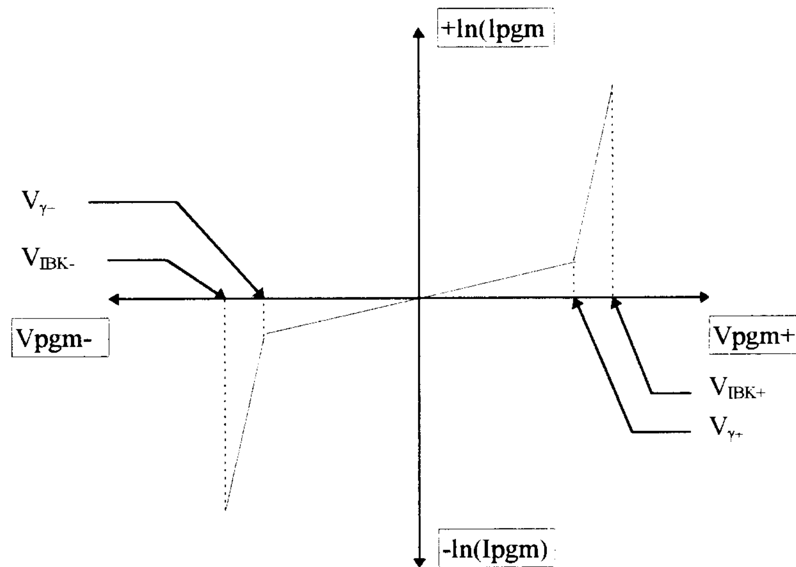

Figure 6. Programming current characteristics.

2.4.3 AGING CHARACTERISTICS

The charge retention of analog memory depends on the property of the oxide and chemical processing involved in fabrication of the device. Thicker the oxide, better the retention characteristics. However thick oxide FG devices will have better charge retention properties as compared to thin oxide FG devices. The FG devices with a standard thick oxide of 400A° have charge loss of the order of 0.1% in 10 years at operating temperatures of 100 °C [17]. The results from this work confirms similar results. Therefore precise voltages can be stored over a long period of time. In this section long term stability characteristics and short term stability characteristics will be considered. The two main charge retention characteristics for FG devices are :

- Long Term Charge Retention and
- Short Term Charge Retention.

2.4.3.1 LONG TERM CHARGE RETENTION

The retention characteristics at elevated temperatures can be described by a thermionic emission model [17].

$$\frac{Q(t)}{Q(0)} = (\exp(-t\gamma \ \exp(\frac{\Phi_B}{kT})) \tag{12}$$

where ϕ_B is the Energy barrier at the polysilicon - oxide interface,

γ is the dielectric relaxation frequency of electrons in polysilicon,

k *is the Boltzmans constant,*

T *is the temperature in degree Kelvin,*

t *is the charge retention time.*

The above equation describes the ratio of the retained charge at time 't' Q(t) to charge at time 't = 0' Q(0) at elevated temperatures T. For thick oxides, i.e. 400A° the charge loss would be in the range of 0.1% in 10 years [17].

2.4.3.2 SHORT TERM CHARGE RETENTION

After inducing a voltage change at the floating gate, one observes that the gate tends to move back towards to its original voltage over a period of time. It has been speculated that this short term drift is due to trap sites with long time constants near the SiO_2 interface settling to a new equilibrium. The size of the return appears to be proportional to the change in gate voltage induced. *This implies slower programming voltage increments and hence greater accuracy.* As described in [17] the observed change in the gate voltage for the prototype structure reported was less than 1% of the change in the floating gate voltage and was smaller for slower rates of change in the FG voltage. If the error described above is unacceptable for the application, it can be decreased at the system level by simply taking longer time in the trimming process.

2.4.4 ENDURANCE CHARACTERISTICS

As described in [7] temperature and cycling effects are important reliability issues to be considered for analog FG applications. They require high precision and good stability and thus the behavior of the structure over time and performance due to cycling induced temperature effects are of concern. The change in threshold due to stressing can be positive or negative and is rather in random in nature. However this random nature is not due to charge loss or gain but is a consequence of noise. Though theoretically the change in threshold can occur due to the addition of a single electron, but the true limit imposed by noise is around +/-5mV. The decrease in threshold of the FG structure with temperature occurs at a constant rate of 2.8mV/°C and this does not indicate charge loss but change in the fermi level of the FG and the substrate as descried in [7]. The effects described in [7] are cycling induced temperature effects leading to changes in threshold. But the application that the structures described in this thesis will be subjected to is rather static. The FG voltage is set to a particular value and subsequent operation causes only a small change in the value.

2.4.5 RESOLUTION

The resolution is theoretically very high because the minimum injection charge could be a single electron. However it is difficult to control the amount of injected charge, because it depends on temperature, charge concentration and the process variation

induced effects. The smallest changes will be limited by the ability of the external circuit to detect the change. For example 25 million electrons (equivalent capacitance of 20pF) injected onto the floating gate will cause a 2V change in threshold. To date the best resolution is approximately 8 - 10 bits [3].

In order to control the stored analog value precisely, programming will have to be done in 4 -5 iteration steps to set the threshold to the desired value. Based on our experience the programming speed is not an issue as only 4-5 trims are necessary to set to the necessary values. In a production environment it is estimated that trimming could be completed in a few mSec. Due to temperature and age variations it must be anticipated that these circuits will have to be recalibrated 2-3 times only over a 15 year period to maintain the desired accuracy.

2.5 EVOLUTION AND OVERVIEW OF ADC ARCHITECTURES

Since the existence of DSP, ADCs have been playing an ever increasingly important role in interfacing between analog and digital domains. They perform digitization of analog signals at fixed time period (frequency) which is defined as the speed of the ADC. This fixed time period is generally specified by the application. As per the Nyquist sampling theorem :

"A band limited signal having no spectral components above f_m Hz can be determined uniquely by values sampled at uniform intervals of T_s seconds, where $T_s = 1/2f_m$".

This condition needs to hold in order to reconstruct the original analog signal completely. Since algorithms can be implemented very inexpensively in the digital domain and if samples acquired satisfy the Nyquist sampling theorem, signals can be reconstructed perfectly after DSP within a desired dynamic range. Hence the ADC acts as a very critical bridge between the 2 domains and its accuracy is very critical to the performance of the system. In simple terms the performance of most if not all systems is limited by the accuracy of the ADC and the MIPS of the processor.

2.5.1 FLASH ARCHITECTURE

The most straight forward way to perform analog to digital conversion is to compare the sampled analog signals with different reference levels. Figure 6 shows a conceptual diagram of such a converter.

The input signals is first acquired by the sample and hold (S/H) circuit. During the hold cycle the comparators make decisions as to whether or not the sampled value is greater or smaller than the reference voltages. The output digital data is then typically encoded and latched.

Assuming a N bit ADC, the number of comparators required is 2^N. Due to direct comparison, each reference level needs to be one LSB apart from each other. If we assume a full scale voltage input of 1V, then the LSB size is 2^{-N}. Therefore the offset of the comparator needs to be much less than this value. For a 10 bit resolution this has to be less than 1mv. In a CMOS process this offset requirement is often difficult to achieve.

Special offset compensation techniques are necessary to achieve this. However these circuits are power hungry and may not be practical due to speed requirements.

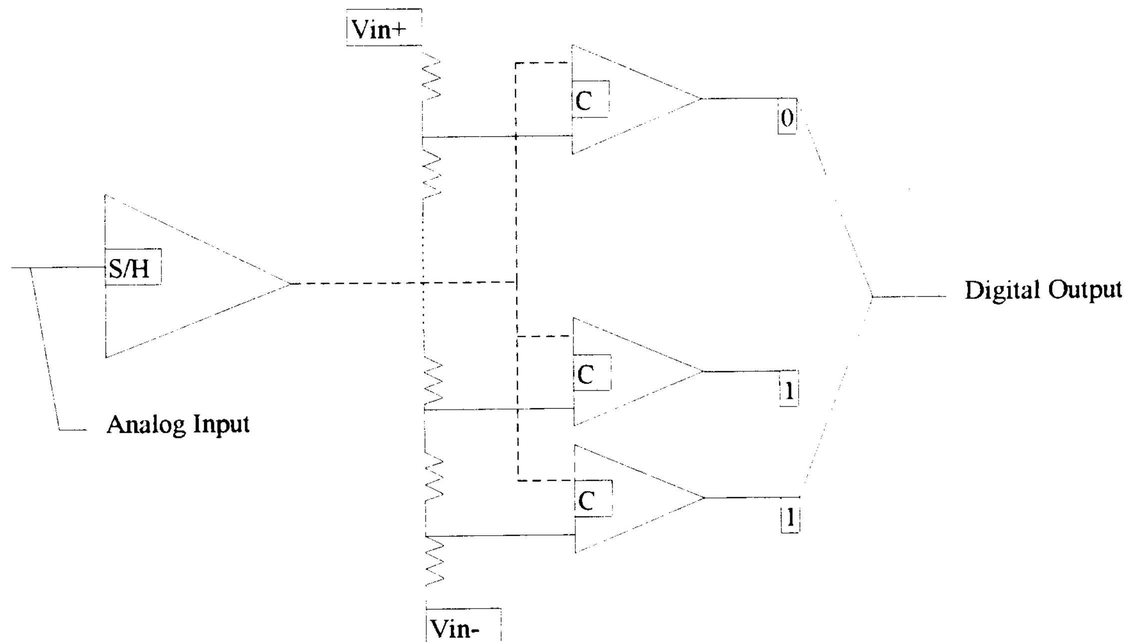

Figure 7. A Conceptual diagram of a Flash ADC.

The advantage of this architecture is that fast conversion rate. Simulations of this type of architecture indicate conversion rates in excess of 1GSPS.

2.6 REFERENCE VOLTAGE GENERATOR

In many ADC systems, reference voltage generators are required to set the reference for a sampled input to be compared to. The accuracy of the references need to be as linear as the converter itself in most cases. Any error present in the references directly reflects on the non - linearity of the ADC. The problem becomes more severe at

higher resolution. At higher speeds switching noise can be coupled onto the reference lines and can corrupt the conversion process.

Traditionally there have been two ways to generate reference voltages either by using a resistor string or a capacitor array. Each has its own limitations. Floating gate references introduced in this thesis are free from power consumption and switching noise effects. Higher resolution at lower power can be achieved by this novel approach.

2.6.1 RESISTOR STRING REFERENCE VOLTAGE GENERATOR

By using multiple passive resistors, one can generate several potentials between supply and ground. In the case of flash converters the number of reference voltages needed are 2^N, where N is the resolution of the ADC. By using 2^N equal value resistors in a string, one can interpolate different potentials. The major problems with this method are matching of resistors, the large power dissipation and lack of desired performance at higher speeds of operation.

Since flash converters rely on the absolute accuracy of the reference voltages, mismatch between the resistors due to process fabrication will directly effect the linearity of the ADC. For higher resolution where the LSB is smaller, the tolerance on the reference voltages becomes even more tighter.

For high speed operation, many sampling capacitors might be switched to a reference voltage on the resistor string. The reference string, needs to settle (with the RC time constant) to the required accuracy within the period allowed. The largest RC time constant appears on the center tap of the resistor string, where the equivalent resistor

value is $2^{N-1}R \parallel 2^{N-1}R$. In order to settle fast enough a small resistor value can be used, however this leads to large power dissipation.

2.6.2 CAPACITOR ARRAY REFERENCE VOLATGE GENERATOR

Another way to generate reference voltages is to use an array of binary weighted capacitors. The input is first sampled onto capacitors and then compared with a reference voltage to determine the MSB. Then the quantized MSB is added or subtracted from the input signal to zoom into the next bit resolution.

This method does not require static power but still depends on the matching of the capacitors.

2.6.3 FLOATING GATE INJECTOR REFERENCE VOLTAGE GENERATOR

The proposed method to generate reference voltages is to store charge on floating gates to set the different potentials. Charge injection is used to remove or inject charge from the floating gate. A trimming circuit can be used to accurately set the values. The scheme does not suffer from any power dissipation. Matching is not an issue as feedback in conjunction with programming adjustments can be used to store the required charge for each reference value.

CHAPTER 3

BULK AND SOS ADC ARCHITECTURE IMPLEMENTATION

This chapter describes the implementation of the floating gate ADC architecture for both the MOSIS BULK and NRaD 0.5um SOS technologies. The circuit schematics, layout procedures, functional description and factors effecting performance are covered. The first part of the chapter deals with the MOSIS BULK implementation followed by the NRaD process quantizer architecture. The proposed ADC, quantizer and injector structures have been built in silicon to verify the functional concept of implementing reference voltage generators using floating gate injector structures and for the purpose of developing injector models. Chapter 4 summarizes the test procedures and results in detail.

3.1 BULK ADC AND INJECTOR IMPLEMENTATION

MOSIS is a multiproject fabrication service run by ARPA (The Advanced Research Projects Agency). It stands for Metal Oxide Semiconductor Implementation

Service. The process handles full custom VLSI chip fabrication in a double poly, double metal BICMOS 2-um feature size process with buried channel CCD implant. The above process was chosen for fabrication of the proposed ADC as the service was available from the university at an economical cost. The following section summarizes the building blocks for the proposed ADC implementation.

3.1.1 ADC ARCHITECTURE

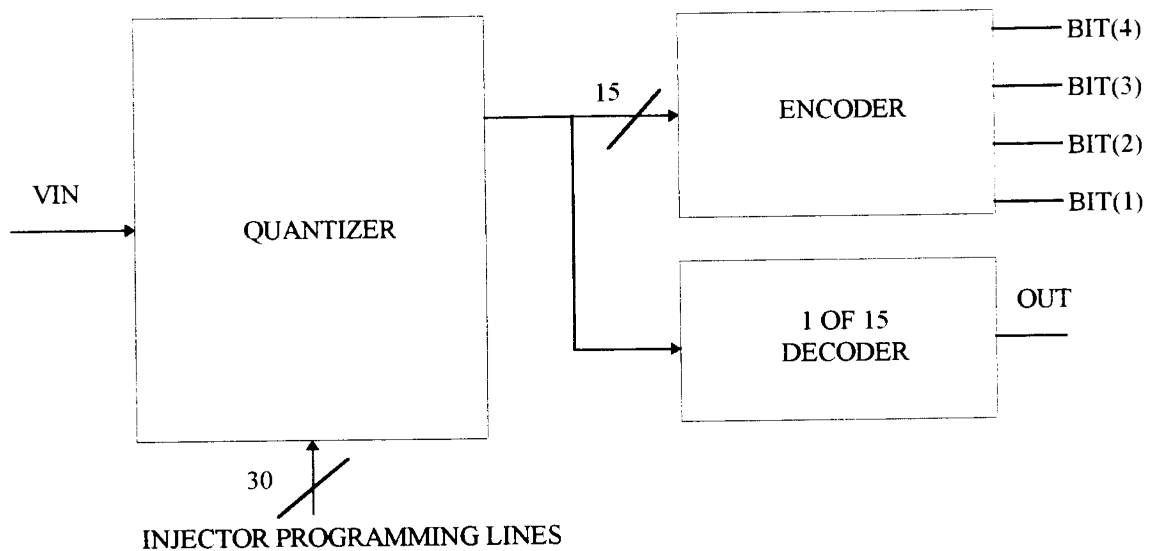

Figure 8. Block Schematic for 4-bit BULK-ADC with Encoder and Decoder.

The proposed BULK-ADC architecture is a 4 bit flash with encoder and decoder circuits. The quantizer resolves 4 bits of the input signal. To determine all of the possible quantization levels 2^4-1 ie 15 comparators are needed. A reference decision level for each comparator is typically generated by each voltage division of a reference. The comparator bank generates thermometer coded outputs. Suitable digital logic in the encoder is then

used to obtain the digital word equivalent to the value of the detected quantization level. The decoder is a 1 of 15 decoder is used to verify the trip point setting of each comparator after setting the reference values, by suitable programming of the injector structures. Encoder and decoder blocks used in this architecture are the straight forward digital logic functions and will not be discussed in this thesis.

3.1.2 COMPARATOR DESIGN

The function of the comparator is a crucial, and often a limiting component in the design of data conversion systems due to its finite accuracy, comparison speed and power consumption [24]. This section describes the design considerations to obtain comparator amplification, analysis of the comparator with floating gate injectors and the concept of trip point control using trimming. The following comparator circuits are proposed.

- Dual Blocking Dual Injector Comparator.
- Single Blocking Single Injector Comparator.
- Stacked Comparator.

3.1.2.1 DESIGN CONSIDERATIONS

Power consumption is a critical design issue that has to be weighed carefully. One of the simplest circuits that can be used as a comparator in CMOS is an inverter. As one

of the transistors is always off during the inverter circuit operation, there is no dc path from V_{DD} to V_{SS}. Hence the static power dissipation is always zero. However there will be dynamic power dissipation during the transition from V_{DD} to V_{SS} and vice versa (transition between the logic levels) as both the transistors will be on during this short period of time. The power dissipation during this period is given by :

$$\mathbf{P_d = C_L\ (\ V_{DD} - V_{SS}\ )^2\ f_P} \qquad \textbf{(13)}$$

where f_P is the clock rate of the circuit. For a given sampling rate and supply voltage the power dissipation is only a function of the capacitance. This capacitance is now a function of the input capacitance of the following stage or the load capacitance.

The general techniques to obtain amplification using a simple inverter circuit is either by single stage amplification or a multistage amplification. The amplification 'A' for one stage of the circuit is defined as the ratio of the output V_O to an input step amplitude V_i after an amplification time T_a if the transistor output conductance are neglected. The relationship between T_a and A for a single stage amplification approach is given by [22]:

$$\mathbf{T_a = \frac{C_L}{g_m}\ x\ A} \qquad \textbf{(14)}$$

Gain A is the small signal gain and depends on process parameters and equals g_mR_O. Gain is a very important characteristic describing comparator operation, for it defines the minimum amount of input voltage change necessary to make the output voltage swing between the two logic levels.

For a multistage approach, that consists of identical single stage amplifiers cascaded, the relationship between T_a and A is given by [22]:

$$T_a = \frac{C_L}{g_m} x \left(A \times N\right)^{\frac{1}{N}} \quad (15)$$

N is the number of stages. For such an approach there exists an optimum number of stages for which T_a is minimized. The relationship is given by [23] and is valid for $A < 1000$:

$$N_{op} = 1.1 \times \ln(A) + 0.79 \quad (16)$$

To obtain an insight into the amount of gain required for amplification, say for a 4 bit quantizer, with logic levels defined as +/-1.65V and noise margin of 70%, then (V_{OH} - V_{OL}) is approximately 2.3V. For the 16 level quantizer with an input of 2V FS, 1 LSB is equal to 125mV. The required amplification for a 1 LSB difference in inputs of the comparator, is approximately equal to (2.3V/125mV) that is 19. This amplification may be obtained in 2 stages for an SOS approach as compared to a single stage amplification for the BULK process. This indicates the minimum gain the quantizer should have to achieve the amplification function. Summarizing, the minimum gain required for the comparator is given by :

$$A_{min} = \frac{0.7(V_{OH} - V_{OL})}{\frac{V_{FS}}{2^n}} \quad (17)$$

3.1.2.2 DUAL BLOCKING DUAL INJECTOR COMPARATOR

The proposed circuit schematic for the comparator is shown in figure 9. The comparator is a 'Dual Blocking Dual Injector' type. It consists of (1) current injector pairs C_{INJ1}, C_{INJ2} for injecting and removing electrons to and from the floating gate, (2) a

bootstrap capacitor C_{B1}, C_{B2} to allow external control and programming of the floating gate voltages without having an electrical connection between programming and the floating gate and (3) basic inverter circuit with transistors M1, M2 that acts as the comparator.

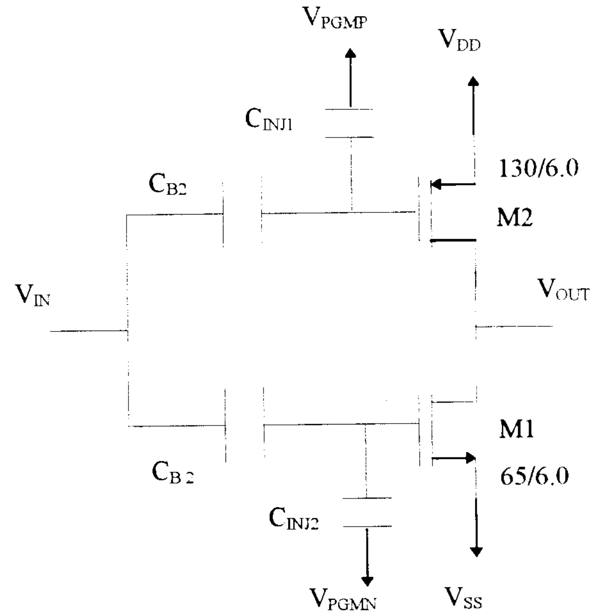

Figure 9. Circuit Schematic for Dual Blocking Dual Injector Comparator

The gain and time constant for the comparator circuit are given by equation (18) and (19).

$$gain = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \tag{18}$$

$$\tau = \frac{C_{Load}}{g_{m1} + g_{m2}} \tag{19}$$

The injector structures along with the blocking capacitors control the amount of stored charge on the floating node and hence the trip point of the circuit. The narrow range where both the transistors in the inverter circuit are in saturation is exploited for use in analog comparison.

At the 'trip point' change over between the two logic levels occurs. The value of V_{in} equals V_{out} at the trip point. Both the transistors M1, M2 are in saturation, in this region and they act as current sources. The equivalent circuit in this region of operation is two current sources between the supply rails, with the output at their common point. This region is highly unstable and the change over between the two logic levels at the trip point is very rapid. Thus a small input voltage change causes a large effect at the output.

ANALYSIS :

The saturation currents for the two transistors including a floating gate charge of +/- V_q is given by:

$$I_{DSn} = \frac{\beta_n}{2}(V_{in} \pm V_q - V_{ss} - V_{TN})^2 \quad (20)$$

$$I_{DSp} = \frac{\beta_P}{2}(V_{in} \pm V_q - V_{dd} - V_{TP})^2 \quad (21)$$

where β_n, β_p, V_{TN}, V_{TP} take on their standard notations and V_{in} is the applied input voltage.

The trip point can be derived as the point where the currents of the two transistors are equal, ie. : $\mathbf{I_{DSn} = I_{DSp}}$

Solving for V_{in}, based on the above condition and assuming that the sum of the total charge on the two floating nodes is +/-V_q, gives :

$$V_{in} = \pm V_q + \frac{(V_{SS} + V_{TN})\sqrt{\frac{\beta_n}{\beta_P}} + V_{TP} + V_{DD}}{2} = V_{TRIP} \quad (22)$$

Now if V_q is written as the sum of the charges on floating gates of M1 and M2, ie.

$$\pm \mathbf{V_q} = \pm \mathbf{V_{qn}} \pm \mathbf{V_{qp}} \quad (23)$$

and assuming $\beta_n = \beta_p$ and $V_{DD} = -V_{SS}$ gives:

$$V_{TRIP} = \pm V_{qn} + \frac{V_{TN} + V_{TP}}{2} \pm V_{qp} \tag{24}$$

As is clear from equation (24) the trip point is now a function of floating gate charge on the two floating nodes. Ideally for an inverter under the above conditions with no charge on the floating gates, and equal and opposite thresholds for the transistors the trip point is at zero.

The trip point can be shifted either in a positive or in a negative direction based on the following conditions :

- ***A positive charge on the floating node of M1, and M2 will shift the Trip point in a positive direction.***
- ***A negative charge on the floating node of M1 and M2 will shift the Trip point in a negative direction.***
- ***An equal and opposite charge on the floating nodes of the transistors will shift the Trip point to zero (assuming equal and opposite thresholds for the transistors).***
- ***Unequal and opposite charge on the floating nodes of the transistors will shift the Trip point in a direction governed by the magnitude of the charges and specified as per equation (24).***

This shift in trip points is achieved by the effective change in the thresholds of the two transistors. The effective threshold voltage of the NMOS is varied in a positive direction by injecting electrons onto the gate. The effective threshold of the PMOS is varied in a negative direction by injecting electrons onto its gate. Removing electrons from the gates, will shift the trip point towards zero in a negative direction for the NMOS,

and towards zero in a positive direction for the PMOS. To validate the theory explained earlier simulation was performed to NMOS and PMOS devices in PSPICE with positive and negative charges stored on a capacitor and connected to the gate of the devices. The simulation results are shown below, the dotted lines on the curves indicate the actual threshold of a naïve device without any FG charge.

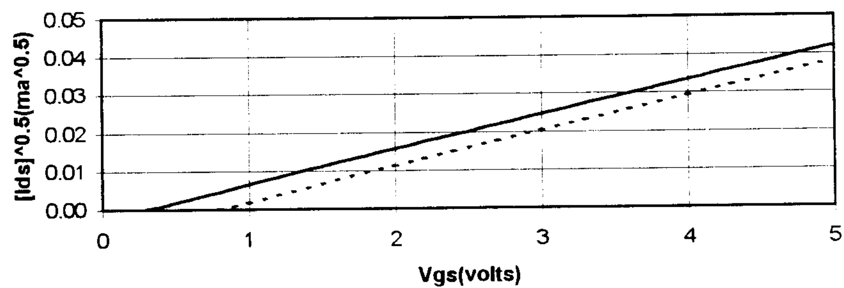

Figure 10. Simulated effective threshold voltage shift in NMOS due to a +ve charge.

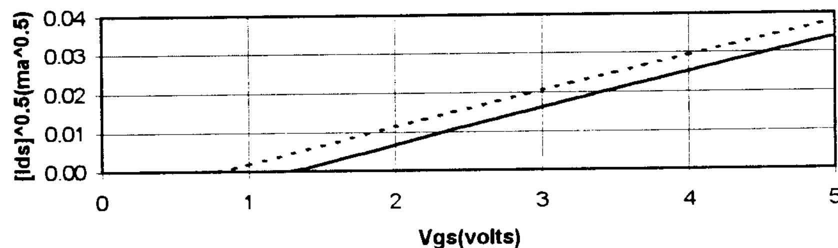

Figure 11. Simulated effective threshold volatge shift in NMOS due to a -ve charge.

To summarize:

- ***The threshold voltage shifts in a negative direction due to a positive charge on gate.***
- ***The threshold voltage shifts in a positive direction due to a negative charge on gate.***

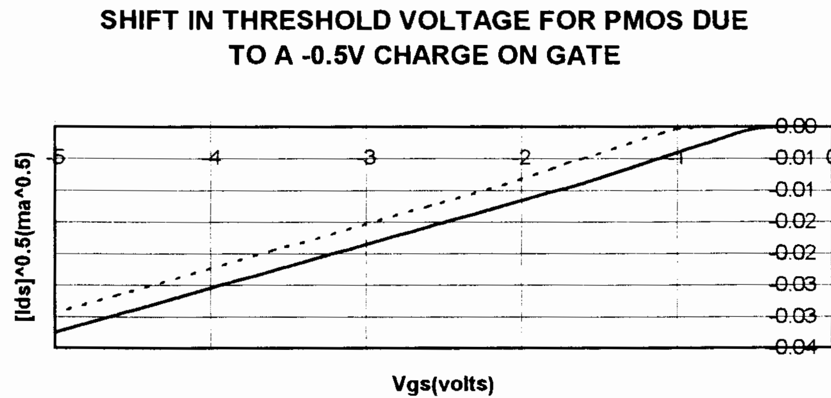

Figure 12. Simulated effective threshold voltage shift in PMOS due to a -ve charge

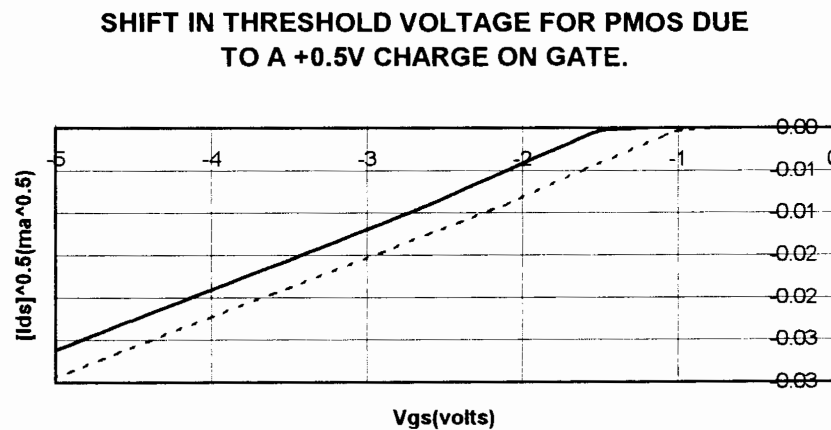

Figure 13. Simulated effective threshold voltage shift in PMOS due to a +ve charge

To summarize :

- ***The threshold voltage shifts in a negative direction due to a positive charge on gate.***

- ***The threshold voltage shifts in a positive direction due to a negative charge on gate.***

3.1.2.3 SINGLE BLOCKING SINGLE INJECTOR COMPARATOR

The use of dual blocking dual injector structure for the comparator has the disadvantage that there are a large number of programming lines for the ADC architecture.

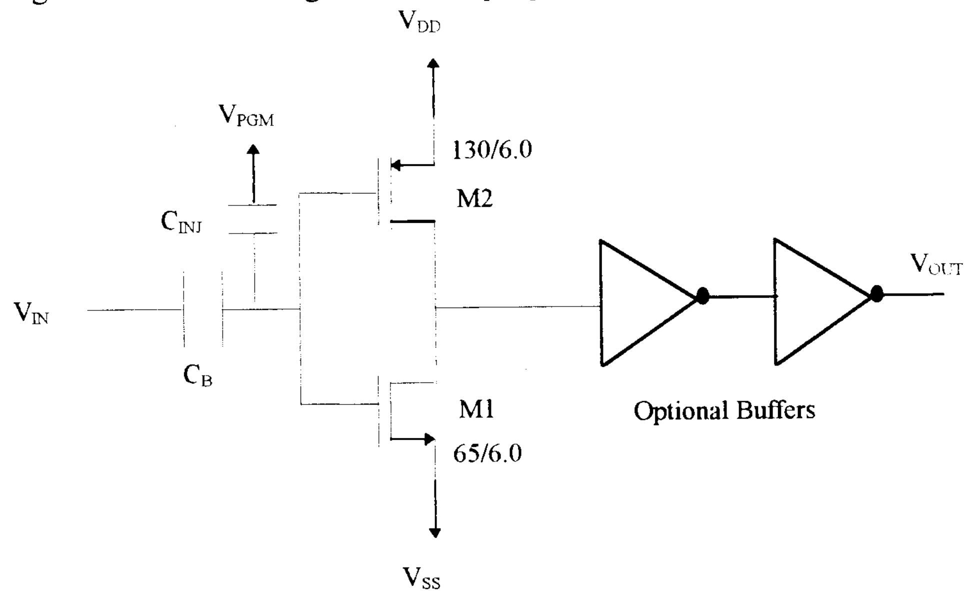

Figure 14. Circuit Schematic for Single Blocking Single Injector Comparator

The number of programming lines can be reduced in half by using a single blocking single injector structure for the comparator as shown in figure (14). This has the additional advantage of better control of trip point as the amount of stored charge on the two floating nodes now is equal and charge injection and removal now occurs through only one injector. The trip point for the circuit shown in figure (14) is now specified by equation (25).

$$V_{TRIP} = \pm 2V_q + \frac{V_{TN} + V_{TP}}{2} \qquad \textbf{(25)}$$

The analysis for the gain, time constant, setting of trip point analysis remain same as discussed before. An optional buffer stage may be incorporated into the design to achieve the amplification by using a multistage approach. This approach may be essential to realize a comparator with a resolution in excess of 4 bits.

3.1.2.4 STACKED COMPARATOR

The circuit shown in figure (15) is a stacked comparator circuit. Transistors M1, M2 form the basic inverter circuit and transistors M3, M4 act as a variable resistor.

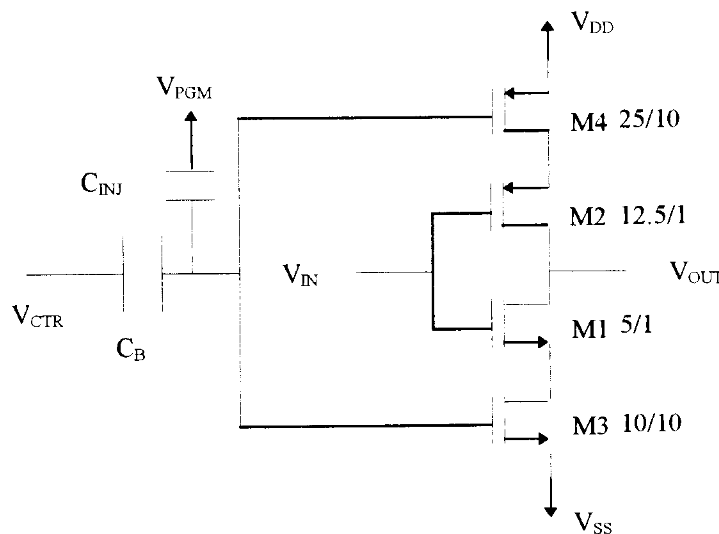

Figure 15. Circuit Schematic for Stacked Comparator.

As the control voltage V_{ctr} increases (electrons are removed from the floating gate), the on resistance of transistor M3 increases and that of M4 increases. This reduces the effective power supply range for the basic inverter. As V_{ctr} increases the inverter threshold decreases.

3.1.2.5 INJECTOR STRUCTURE

The proposed injector structure is a thick oxide dual poly floating gate device as shown in figure (16).

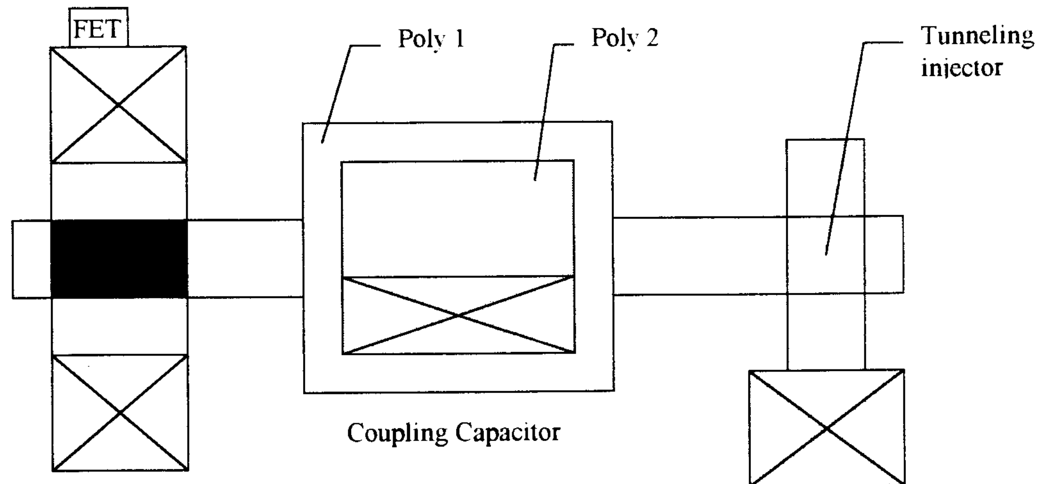

Figure 16. Proposed Injector Structure.

The comparator amplifies the difference between the input and the reference voltage, generating a decision bit. The reference voltage in this case is stored on the floating gate. Corresponding to the various values of reference voltages ie. stored charge, the trip points for the inverter are set. This is achieved by varying the effective threshold voltages of either M1 or M2.

The percentage of programming voltage that appears across the floating gate, assuming no charge on the floating gate depends on the capacitive coupling ratio K, and is given by :

$$K = \frac{1}{1 + \frac{C_{gs}}{C_B}} \qquad (26)$$

where C_B is the bootstrap capacitor between the floating gate and the control gate, and C_{gs} is the floating gate to source capacitance. C_{gd} (gate to drain capacitance) and C_{inj} (injector capacitance across the gate oxide) are assumed to be relatively small based on the assumption that the transistor is in saturation.

For a given tunneling voltage tighter coupling minimizes the required programming voltage. For this reason the it is desired that C_B be at least one order of magnitude larger than C_{gs}. Taking into account the circuit area, proper trade off between the size of the capacitor and the programming voltages should be made. The chosen coupling ratio used in this design is 9/10.

3.2 NRaD SOS QUANTIZER AND INJECTOR IMPLEMENTATION

The NRaD CMOS/SOS (silicon on sapphire) is a mesa isolated, double level metal, single poly salicide process. The cornerstone of the process is the use of improved 100nm thick silicon films on sapphire which allow for fully depleted, low leakage operation. These MOSFET's are different from conventional BULK MOSFET's because the body is thin and floating. These differences make the devices behave slightly different. The most commonly observed difference is the 'Kink effect' which occurs at high drain to source voltages. This calls for low voltage operation. Also due to a very short channel length the intrinsic self gain of the transistor is small (of the order of 20-25db) as compared to 40-

50db for a long channel BULK MOSFET. A very important advantage of these devices is the elimination of junction capacitance at the source and drain of the transistor.

3.2.1 ADC ARCHITECTURE

The proposed ADC architecture is very similar to the one proposed earlier, except for an important difference that the architecture has a DAC block for loop back.

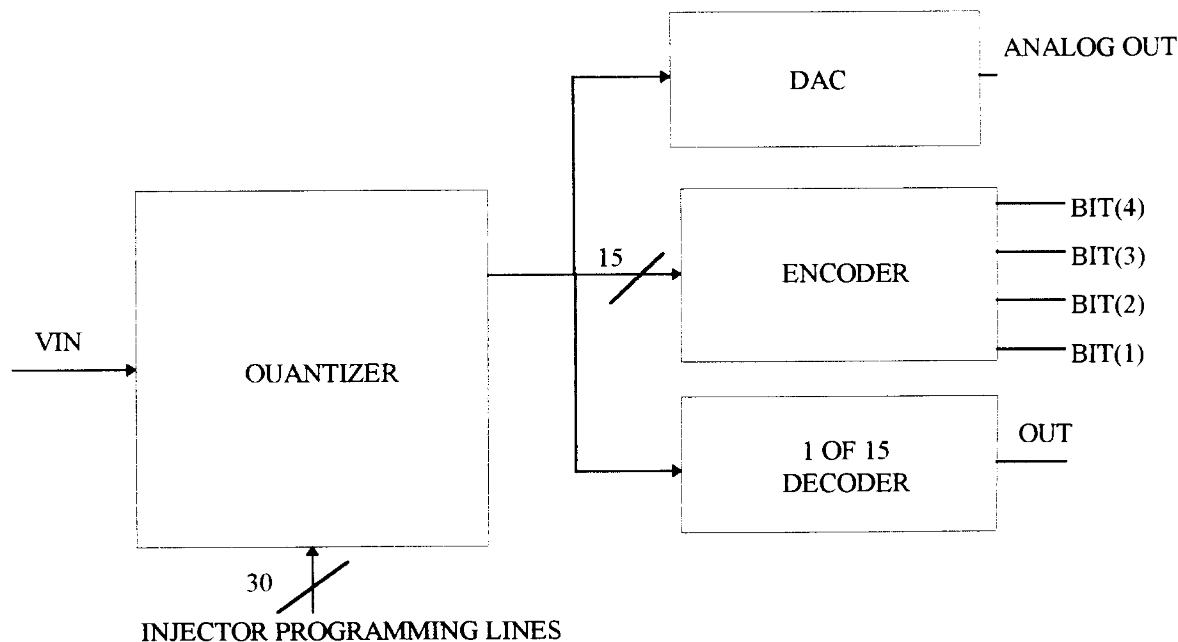

Figure 17. Block Schematic for NRaD-SOS ADC with Encoder, Decoder and DAC.

The proposed architecture shown above is for a 4-bit ADC. The quantizer, encoder and decoder blocks serve the same functions as explained earlier. The digital output of the quantizer is then fed into the DAC that converts it to an analog signal.

3.2.2 COMPARATOR DESIGN

The comparator circuit implementations discussed in the previous section suffers from a major drawback that the trip point of the circuit is dependent on the power supply voltage as indicated by equation (22). There is a limited range in which the circuits can be placed while still maintaining adequate gain. The use of a differential approach to obtain comparator amplification gives the advantages of good CMRR (common mode rejection ratio), CMR (common mode range) and PSRR (power supply rejection ratio) in addition to setting of the trip points independent of the power supply voltages.

A regenerative amplifier can also be used as a non-linear gain stage. The large signal amplification A can be defined as the ratio of the differential output to the initial unbalance, ie. :

$$A = \frac{V_1(t) - V_2(t)}{V_1(0) - V_2(0)} \tag{27}$$

The amplification time T_a is then related to A by :

$$T_a = \frac{C_L}{g_m} X \ln(A) \tag{28}$$

The use of a differential amplifier stage has the key attribute that the circuit has the ability to amplify the difference between the inverting and non-inverting inputs. As a result the trip point can be made independent of the process and supply variations to the first order.

The comparator circuit is shown in figure (18)[24]. The comparator circuit consists of a differential input pair (M3, M4), a CMOS latch circuit and a bias circuit. The

CMOS latch is composed of a n-channel flip flop (MN6, MN7) with a pair of n-channel pre-charge transistors (MN5, MN8). A n-channel switch MN9 is used for resetting and a pair of p-channel flip flop (MP5, MP6). CLK1 and CLK2 are two overlapping clocks, with CLK2 being a delayed version of CLK1.

The dynamic operation of the circuit is divided into a reset time interval and a regenerative time interval. During the reset interval current flows through the resetting switch MN9, which forces the two logic states to be equal. After the pre-amplifier settles, a voltage proportional to the input voltage difference is established between the two nodes X and Y. This voltage will act as the initial unbalance for the regeneration time interval. The regeneration period is started by opening of the switch MN9. In the meantime as the p-channel flip flop is set, the n-channel flip flop is reset by the two closed pre-charge transistor pairs (MN5, MN8). This pre-charges the two nodes to the negative power supply voltage. As a result the CMOS latch is set to an astable high-gain mode.

Since the transistor pairs (MP7, MP8) isolate the n-channel flip flop from the p-channel, the use of two overlapping clocks performs the regenerative process in two steps. The first regenerative process is within the short time interval between Φ_1 getting low and Φ_2 getting high. The second regeneration is when Φ_1 gets high. The voltage difference between nodes C and D is amplified to a voltage swing nearly equal to the power supply voltage.

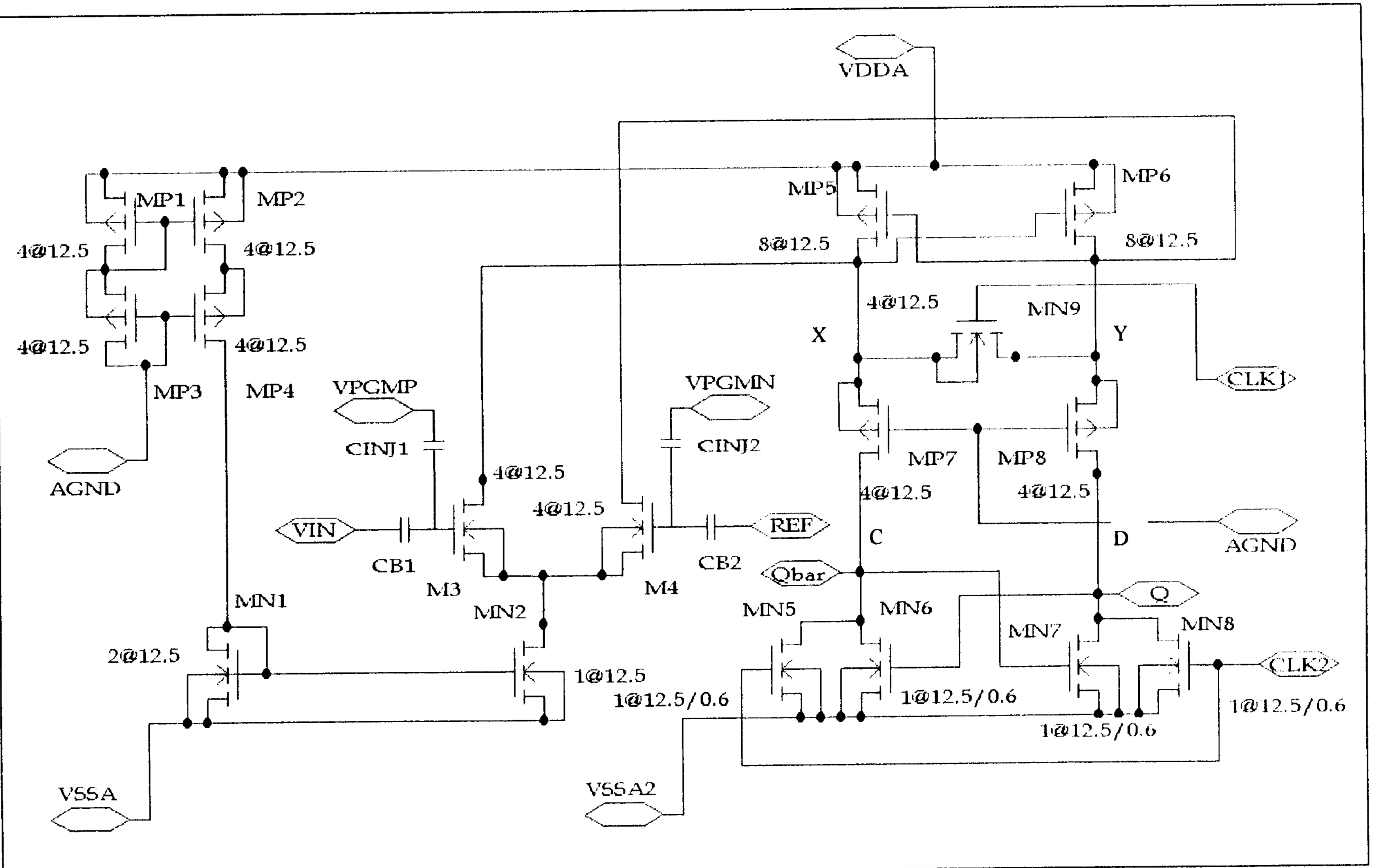

Figure 18: Circuit Schematic Comparator_differential_floating_gate.

3.3 SPECIFICATIONS OF CONVERTERS

To obtain insight into the design for converters it is important to arrive at a unanimous definition of specifications. The DC specifications for converters are well known in literature. In this section the DC and dynamic specifications are discussed.

3.3.1 DC SPECIFICATIONS

Accuracy of converters should not be confused with linearity and resolution. In addition accuracy includes the errors of quantization, non-linearity's, short term drift, offset, harmonic distortion and noise [26].

3.3.1.1 ABSOLUTE ACCURACY

The absolute accuracy of a converter is the actual full-scale input or output (analog to digital or digital to analog) signal (voltage, current or charge) referred to the absolute standards. This absolute accuracy is mostly related to the reference source used in the converter. This reference source should have a low noise with respect to the resolution of the converter. Temperature coefficients in the ideal case should be so small that the accuracy of the reference source over the specified temperature range stays within the resolution of the converter (1/2 LSB over the full temperature range) [26].

3.3.1.2 RELATIVE ACCURACY

The relative accuracy is the deviation of the output signal or code from a straight line drawn through zero and full scale. Output signal or output codes must be corrected from a possible zero offset. This relative accuracy is called *Integral Non Linearity (INL)* or sometimes linearity. The boundaries for the non linearity deviation should be not more than +/-1/2 LSB of a straight line through zero and full scale. This +/-1/2 LSB INL definition implies a monotonic behavior for the converter. Monotonicity of a converter means that the output of the DAC never decreases with an increasing digital input code. A minimum increase of zero is allowed for 1 LSB increase in input signal of the DAC. In an ADC monotonicity means that no missing codes can occur. It can be pointed out that converters can be designed that are guaranteed monotonic but do not have the 1/2LSB linearity specification [26].

Thus the monotonic specification does not include that a converter has a +/-1/2 LSB INL error. However a converter is always monotonic when the INL specification is less than or equal to +/-1/2 LSB. But when a converter is specified to be always monotonic, then this specification does not automatically imply an INL error of less than or equal to +/-1/2LSB.

3.3.1.3 DIFFERENTIAL NONLINEARITY

Differential non-linearity (DNL) error describes the difference between the two adjacent analog signal values compared to the step size (LSB weight) of a converter generated by transitions between adjacent pairs of digital code numbers over the full range of the converter. The DNL is zero if every transition to its neighbors equals 1LSB. In a monotonic converter [26].

3.3.1.4 OFFSET

Input amplifiers, output amplifiers and comparators have inherently built in offset voltage and offset current. This offset is caused by the mismatch in components. The offset results in non-zero input or output voltage, current or digital code although a zero signal is applied to the converter [26]. Offset can be minimized by trimming or auto zeroing procedures, adopting careful layout procedures and avoiding thermal coupling or thermal gradients over an integrated circuit.

3.4 INJECTOR SPECIFICATIONS

For characterization of floating gate comparator circuits it is essential to characterize the injector structures. This characterization will aid in setting the

programming voltages necessary to inject or remove charges. The specifications developed for these structures were specific to the application they are being used. The injector specifications are as follows: (refer to Figure 4, chapter 2)

- **PROGRAMMING ONSET** : Minimum programming voltage to initiate charge injection or removal into or from the floating gate. The onset is indicated by both positive and negative programming voltages and specified as $\mathbf{V_{\gamma+}}$ and $\mathbf{V_{\gamma-}}$ respectively.
- **OBSERVABLE QUANTUM** : Minimum observable unit of charge injection per programming cycle and indicated as - $Q_{obs} = \frac{\Delta V_{TRIP_POINT_SHIFT}}{C}$. This parameter sets the LSB of the ADC system as the trip point is to be shifted in a positive or negative direction by one quantum.
- **LONG TERM CHARGE RETENTION** : This parameter specifies the charge retention on the floating gate in terms of the number years and indicated as $\mathbf{t_{LR}}$. The variation of floating gate charge over a period of time, say 10 years is specified as - $\mathbf{t_{LR} < ½(LSB)}$. This specification dictates the feasibility of building floating gate ADC systems.
- **SHORT TERM CHARGE RETENTION** : The variation of charge on the floating gate during a 15 minute recovery post programming is indicated as a shift in the trip point voltage and the notation used is ΔV_{SR}.
- **MAXIMUM PROGRAMMING VOLATGE** : This parameter specifies the maximum programming voltage that can be applied to the floating gate injector's programming terminals without breakdown of the oxide - $\mathbf{V_{IBK+}}$, $\mathbf{V_{IBK-}}$.

- **DC PROGRAMMING VOLTAGE** : The magnitude of the programming voltage that has to be applied for a fixed duration to get the desired trip point shift is indicated by - $\mathbf{V_{pgm}}$.
- **PROGRAMMING TIME** : This parameter indicates the duration of the programming voltage to get a desired trip point shift - $\mathbf{t_{pgm}}$.

3.5 LAYOUT ISSUES

The layout process should be carried out very carefully to preserve the matching properties and to minimize the parasitic capacitance. The most common ways in which the layout influences matching are through device proximity and device orientation. Matching of components is degraded by placing them apart. Therefore two devices intended to match should be placed in close proximity, decreasing their mismatch.

One technique for improving the matching is called "common centriod" layout style. Both the differential pair, p-channel and n-channel pair of latch in the regenerative comparator are laid out using this technique. Each transistor, capacitors in all the layouts are have been divided into fingers. Dividing a single transistor into fingers diminishes the sensitivity of mismatch to quadratic spatial variations in the process parameters and in turn improves accuracy.

Any sufficiently large capacitance mismatch between nodes X and Y in the latch of the regenerative comparator leads to an erroneous result due to charge injection and clock

feed through error of switch MSW. To guarantee that two parts of the symmetric circuit match, all the wires on each side must contain the same length at each wiring layer and have the exact crossings with other devices or wires. The whole latch structure is laid out symmetrically, the left part of the latch is just the mirror image of the right part. This reduces the dynamic offset errors. It is also necessary to pay extreme attention to prevent noisy interaction of analog circuit (pre - amplifier) and digital circuit (latch).

CHAPTER 4

TEST PROCEDURES AND CHARACTERIZATION RESULTS FOR FLOATING GATE CIRCUITS

This chapter describes the testing procedures developed for the characterization of floating gate injector structures along with a detailed overview of the results obtained. The main purpose of developing the test procedures is for the purpose of developing injector models that will determine the feasibility of the approach being adopted along with building significant insight into the behavior of the floating gate injector structures. Thus the main design and development issue for a 4 bit floating gate injector trimmed is the characterization of the injector structures in the process of interest. Comparators and quantizers were fabricated as per the designs explained in chapter 3. The two main fabrication technologies of interest were the MOSIS BULK process and the NRaD SOS process. Circuits in these two technologies were fabricated with a packaged IC being

made available from the MOSIS process and a wafer test structure from the NRaD SOS process. However the test setup and procedures were nearly identical for the two with minor variations.

4.1 GENERALIZED TEST SETUP

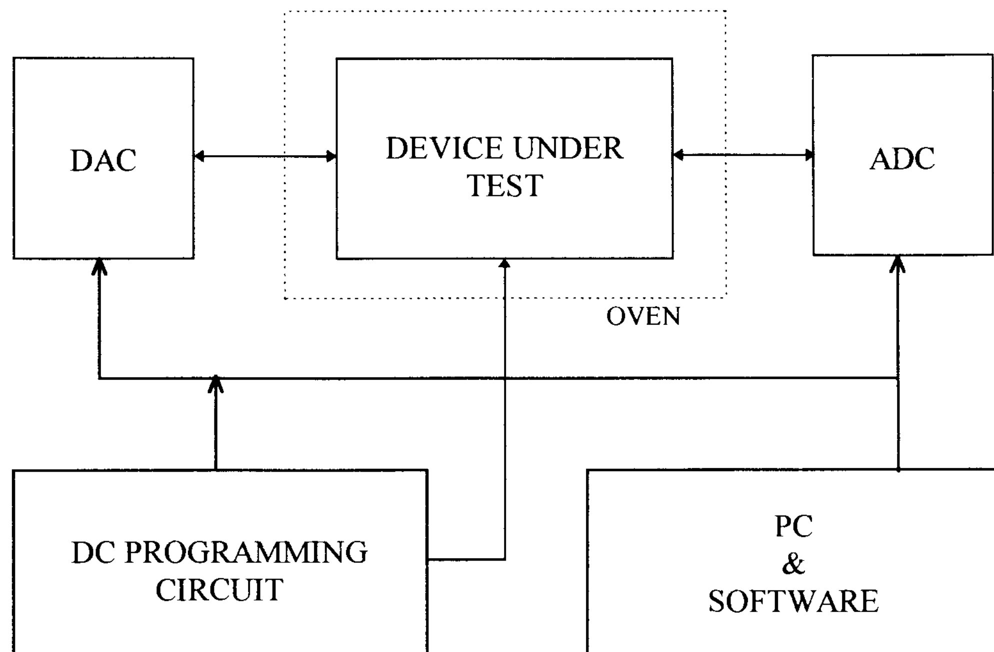

Figure 19: Test setup for characterization of Quantizers and Injectors.

The figure above shows a generalized test setup for characterization of floating gate injector circuits. The "DEVICE UNDER TEST-DUT" in this setup can be a simple injector structure, a floating gate comparator or a quantizer test structure. The ADC/DAC blocks along with the PC and its related test routine software serve the purpose of data acquisition and applying the required inputs in terms of voltages. A DC programming

circuit block is also included that serves the purpose of generating a DC programming pulse for programming the injector structure. The DUT block may be baked in a oven to study the charge retention properties of the injector structure. Detailed test procedure for the characterization of floating gate injector structures is explained in the following sections.

4.2 TEST MODES FOR CHARACTERIZATION

The following test modes have been designed for the purpose of characterization of injector structures.

- **INPUT SWEEP MODE:** With the injector programming lines shorted to the inputs this mode is used to determine the comparator/quantizer characteristics like the trip point-V_{TRIP}, along with the injector parameters like short term charge retention-ΔV_{SR} and the observable quantum-Q_{obs}.
- **DC-PROGRAMMING MODE:** To get either +/- injection a programming voltage of magnitude +/-V_{pgm} is applied across the input and the appropriate injector terminal for a required duration t_{pgm} to store the desired amount of charge on the FG. The range of programming voltages needed is ascertained based on parameters like programming onset-$V_{\gamma+}/V_{\gamma-}$ and maximum programming voltage-V_{IBK+}/V_{IBK-} that are obtained by injector characterization.

- **OVEN EXPOSURE MODE:** The DUT is baked for a required duration to infer the long term charge retention t_{LR}.

4.3 TEST PROCEDURE FOR CHARACTERIZATION

To ascertain the injector parameters explained in chapter 3 and characterize the comparator/quantizer test structures the following test procedures have been developed.

4.3.1 TEST PROCEDURE FOR INJECTOR CHARACTERZATION

For characterization of floating gate comparator circuits it is essential to characterize the injector structures. This characterization will aid in setting the programming voltages necessary to inject or remove charges. The fabricated injector structures in both the BULK and SOS process was a two terminal device with poly as one terminal and poly2 as the other in the case of BULK and island in the case of the SOS process. The charge injection and removal occurred across this interface by means of a tunneling mechanism as explained in chapter 2. As the injection current is of the order of a nA, it was essential to fabricate at least 1000 such injectors in parallel in order to enable the available test equipment to sense significantly larger currents. The injector was to be characterized based on the parameters explained in chapter 3 and the Fowler Nordhiem equivalent model.

The two terminal test structure was grounded on one end and a linear sweep ranging from +/-15V was applied at the other end in increments of 0.1V using the HP-4145 semiconductor parametric analyzer. The current was sensed to characterize the structure.

4.3.1.1 BULK INJECTOR CHARACTERIZATION RESULTS AND INFERENCES

The two terminal injector structure in the MOSIS BULK technology was a poly1 - poly2 test structure composed of cells described previously in section 2.3.4. The test procedure explained in the previous section was performed on the DUT and the results are summarized as follows.

- **MOSIS BULK POLY1-POLY2 INJECTOR CHARACTERIZATION**

  –Maximum Programming Voltage V_{IBK+}/V_{IBK-} = +27V/-27V

  –Measurable Programming Onset = +12V/-12V

  –The injector structure was observed to be symmetrical in nature (refer to the data characteristic plot in figure 20)

BULK POLY1-POLY2 INJECTOR CHARACTERISTICS

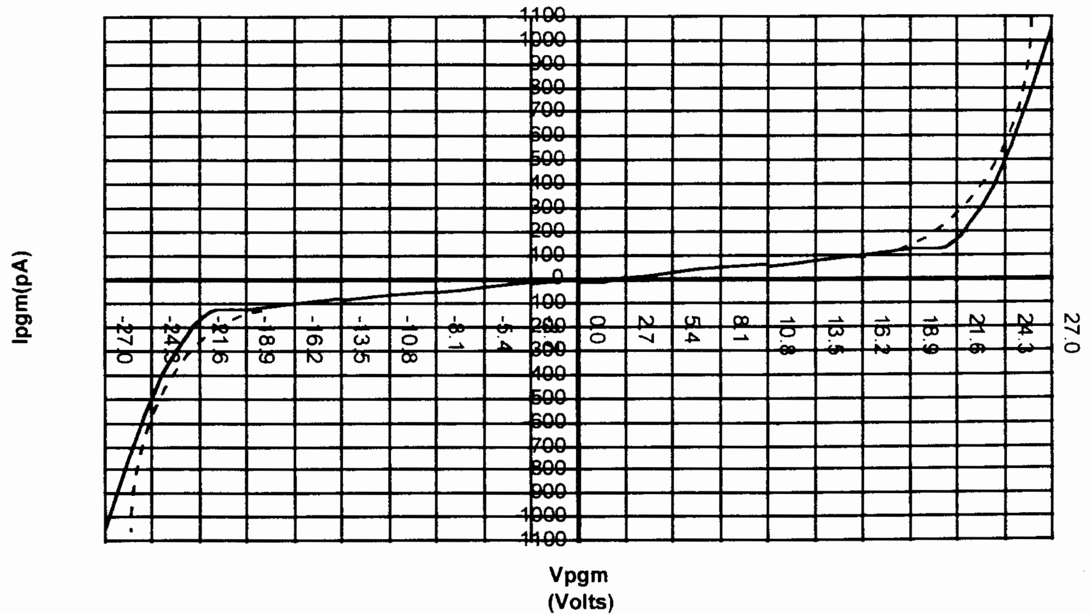

Figure 20 : Injector characteristics obtained by testing.

Injector Modeling : The values for α and β in equation (9), section 2.4.1 can be estimated based on the injector characteristics obtained by testing. Repeating the Fowler Nordhiem equation :

$$\mathbf{J = \alpha E^2 \exp(-\beta/E) + G_S V} \qquad \textbf{(29)}$$

Based on the estimate of ϕ_B obtained by baking comparator test structures to project charge retention time as explained in section 4.3.5.2, the values for α and β can be calculated as per equations (30) and (31).

$$\alpha = \mathbf{6.49 - \log(\phi_B)} \qquad \textbf{(30)}$$

and

$$\beta = 21.0\ \mathbf{(\phi_B{}^3)^{1/2}\ MV/cm} \qquad \textbf{(31)}$$

The values obtained: $\boldsymbol{\alpha = 6.027}$ and $\boldsymbol{\beta = 0.93 \times 10^9}$ **V/m**. The leakage resistance was estimated as 160Mohm/unit injector. It can be noted that for values of the programming

voltages given by equation (32) the current density term is dominated by the α term. that is $J = \alpha E^2$.

$$V > (\beta\ T_{OX})/\ln[10] \qquad (32)$$

For an oxide thickness of $400A^{\circ}$ this value of programming voltage was 16.2V for the structure. Based on the extracted data from the 1000 injector in parallel structure the effective injector area for a single injector was calculated as $2.25 \times 10^{-19} \mu m^2$. From this estimate of the injector area it can be inferred that tunneling occurs at the edges of the interface of poly1 and poly2 where oxide thinning occurs. Increasing the number of edges between the interface will lead to a larger effective injector area and hence lower programming voltages.

Based on the extracted values the plot in figure (20) shows the actual data fit curve (dotted lines) and the curve obtained from real characterization data.

4.3.1.2 SOS INJECTOR CHARACTERIZATION RESULTS AND INFERENCES

The two terminal injector structure in the NRaD SOS technology was a poly1 to island overlap test structure. The test procedure explained in the previous section was performed on the DUT and the results are summarized as follows (refer to figure 21).

- Programming Onset = +/-8V.
- Maximum Programming voltage is approximately = +/-13V.

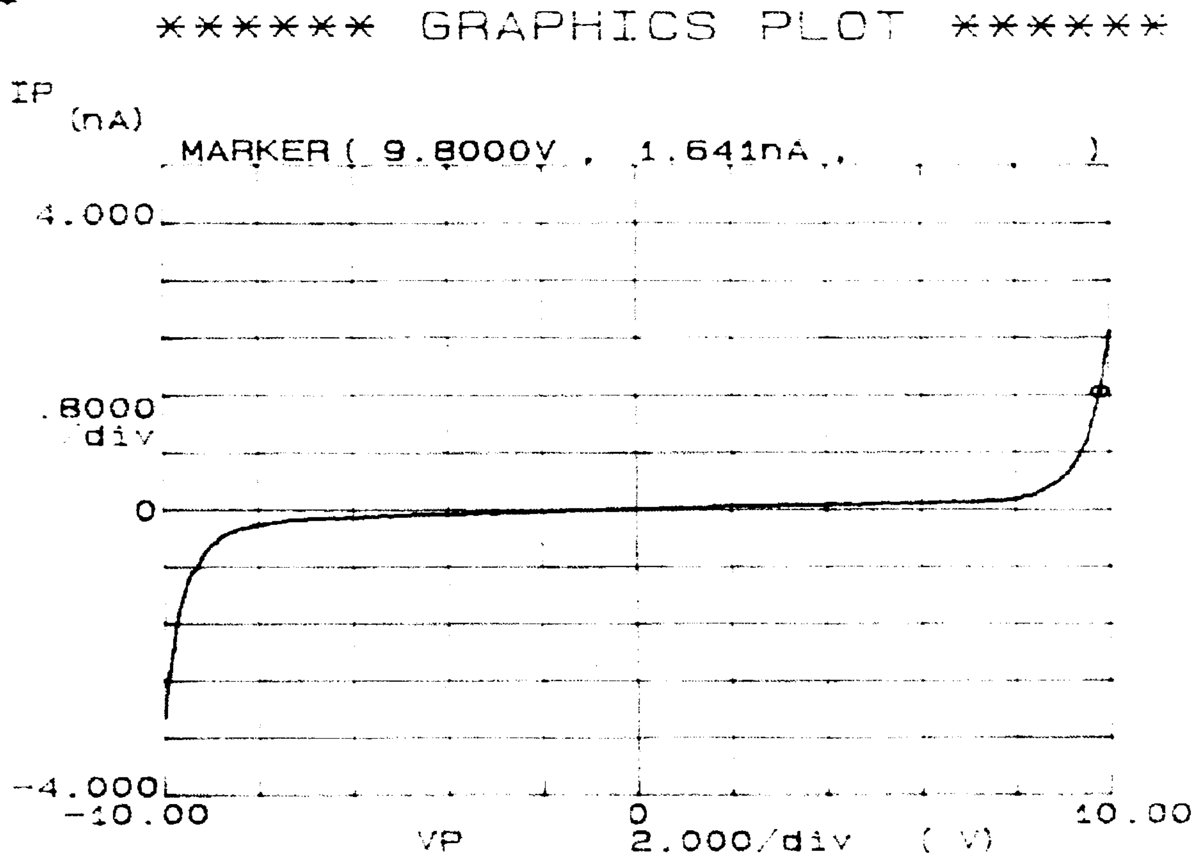

Figure 21: Injector characteristics obtained by testing.

- The plot of Vpgm and Ipgm indicated a symmetrical injector structure.
- A current of 1.641nA was sensed on the test structure at a programming voltage of 9.8V.

Injector Modeling : The characteristic constants in equation (29) was extracted based on the data obtained. The values obtained: **α = 6.07** and **β = 1.2 X 10^9 V/m**. The leakage resistance was estimated as 50Mohm/unit injector. For an oxide thickness of 120A° the value of programming voltage at which the current density is dominated by the α term (as per equation 32) , was 6.5V for the structure. Based on the extracted data from the 1000 injector in parallel structure the effective injector area for a single injector was calculated as 4.05 X $10^{-19}\mu m^2$. A similar inference as given earlier on the tunneling interface can be drawn based on the above result.

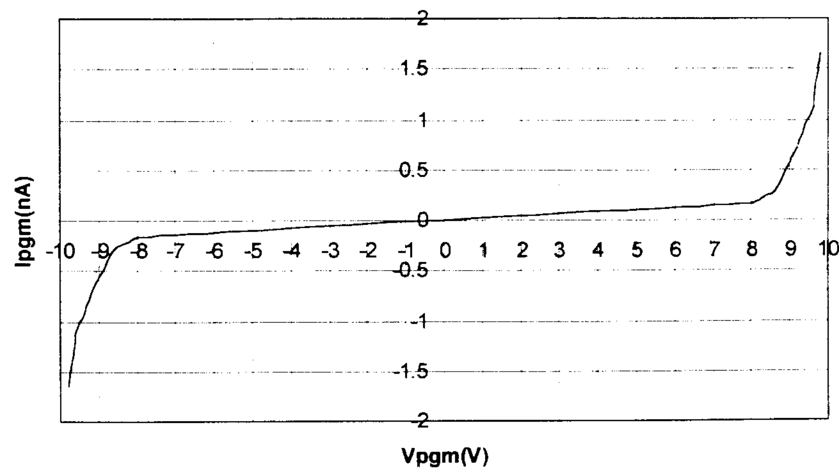

Figure 22 : Injector characteristics obtained by testing & extracted data plot.

Figure (22) shows the plot obtained by characterization in comparison with the plot obtained from data extraction. The actual data fit curve (dotted lines) is in close agreement with the characterization results indicating the validity of the values of the characteristics constants in Fowler equation obtained.

4.3.2 TRANSFER CURVE CHARACTERIZATION FOR COMPARATOR

Before trip point characterization by programming can be done on floating gate comparator circuits it is essential to demonstrate functionality. The test structures used were a 'Dual blocking dual injector type comparator' circuit from the MOSIS BULK process and a 'Clocked regenerative comparator' from the NRaD SOS process. To characterize the test structures the circuits were placed in the 'Input sweep mode' with the

injector programming lines shorted to the input. The transfer curve characterization indicates the trip point of the circuit. Since these devices have FG structures on the gates, it is essential to erase the DUT using UV light for a specified period of time before characterization can be done.

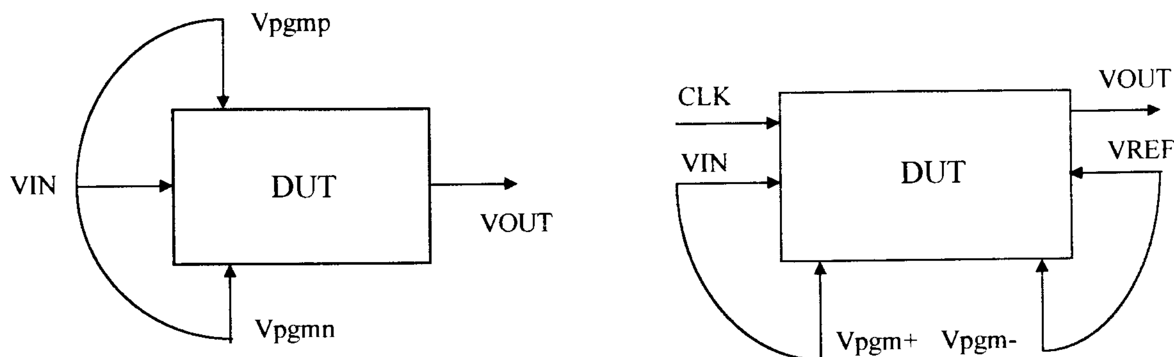

Figure 23. Test setup for dual injector comparator and regenerative comparator.

The trip point thus obtained is inferred as the 'Trip point before any charge has been transferred to the gate'. An alternate method to infer this information is to characterize a circuit that does not have any FG structures on it.

4.3.2.1 BULK COMPARATOR CHARACTERIZATION RESULTS AND INFERENCES

The DUT was 'Dual blocking dual injector type comparator' circuit with a poly1-poly2 injector structure. The DUT was placed in the input sweep mode as shown in figure 23 The DUT had power supplies that ranged from +/-2.5V (refer to the circuit schematic in chapter 3 - figure 9).

In this mode the trip point of the comparator is measured.

- The programming terminals VPGMP and VPGMN are grounded in this entire mode of operation.
- The comparator input VIN is swept in increments of 10mv starting from Vss to Vdd.
- The output is measured for each input voltage and a plot of Vin versus Vout gives the transfer characteristics.

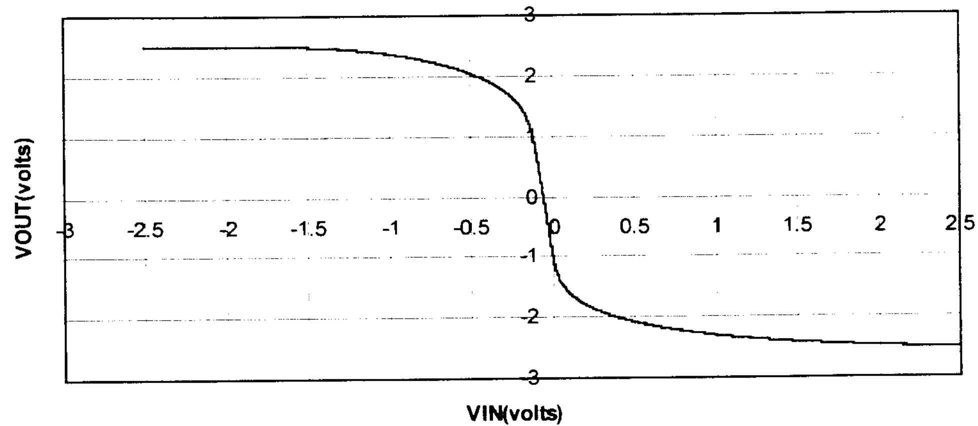

Figure 24: Transfer curve characterization obtained by testing.

Transfer curve characterization results: Prior to device characterization in input sweep mode the DUT was UV erased for a period of 24 hours. Functionality was obtained when the DUT was operated in this mode. The circuit was able to trip with Vin resolutions of 10mv (refer to the transfer curve plot in figure 24).

4.3.2.2 REGENERATIVE COMPARATOR CHARACTERIZATION RESULTS AND INFERENCES

The DUT here was a clocked regenerative comparator with injector terminals for programming (refer to the attached schematic).The circuit operated in two modes: - trip point measurement mode and programming mode. To demonstrate functionality the DUT was operated in the trip point measurement mode as shown in figure 18. The comparator has +/-3.3V analog power supplies for the pre-amplifier and +/-1.65V digital power supplies for the digital latch. The clock levels for CLK1 and CLK2 ranged from -1.65V to +3.3V (refer to the circuit schematic in chapter 3, figure 18).

Programming mode test setup :

- The programming terminals **V_PGMP & V_PGMN** are grounded along with **V_REF** in this entire mode of operation.
- Comparator is reset with **CLK1 LOW** and **CLK2 HIGH** before each measurement. During reset operation **VIN** is also grounded.
- A particular value of **VIN** is then applied (**VIN** is swept in the desired range of operation).
- Comparator is clocked with **CLK1 HIGH & CLK2 LOW**.
- The output **Q or Q_BAR** is measured.
- The comparator is reset again and **VIN** incremented in the range of operation.
- A plot of **Q_BAR vs VIN** gives an indication of the trip point.
- For **coarse** trip point measurements **VIN is incremented in 500mv - 100mv steps.**

- For **fine** trip point measurements **VIN is incremented in 10mv - 1mv steps**.

Transfer curve characterization results: No UV erasure was done on the DUT as the they were wafer structures. Functionality was obtained when the DUT was operated in this mode. The circuit was able to trip with Vin resolutions of 500mv, 250mv, 100mv, 10mv and 1mv (refer to figure 25 for a 10mv resolution transfer curve plot in figure 24).

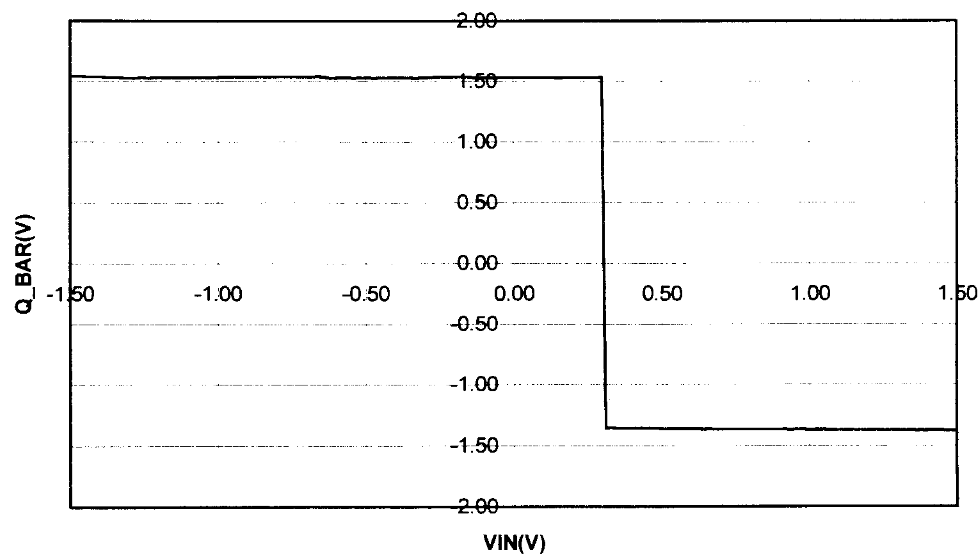

Figure 25: Transfer curve characterization obtained by testing.

4.3.3 TRIP POINT CHARACTERIZATION FOR COMPARATOR

To demonstrate trip point characterization by programming the comparator is programmed and trip point measurements were made alternately between each programming epic. It is essential to demonstrate both fine and coarse trip point shifts with programming. For this purpose a program was written that incremented programming

voltages with the desired resolution and measured the trip point with a fine degree of resolution. The program thus set the test circuit in the programming mode and trip point measurement were made alternatively to characterize the trip point with programming increments.

Initially programming is done with a positive pulse and the trip point is shifted in a positive direction. The range of programming voltages is based on the desired range of the trip points. Negative programming pulses are then applied to shift the trip point in a negative direction.

To build a 4-bit ADC it is necessary to shift the trip points by 125mv with +/-1V range of operation. Finer shifts in trip points would indicate the feasibility of building an ADC with larger number of bits. However it is necessary for the injector structures to retain charge over a short period of time as well as over a long period of time. Before fine programming increments can be applied it is essential to know whether the trip point can be shifted with coarse programming increments. This gives an indication of the range in which the trip points can be shifted. The quantum of charge that can be injected or removed can be inferred from fine programming voltage increments trip point characterization. It is essential that we are be able to inject/remove at least 1LSB or125mV equivalent of charge to use the comparator as a building block for our ADC.

4.3.3.1 BULK COMPARATOR CHARACTERIZATION RESULTS AND INFERENCES

The comparator trip points were programmed in incremental steps of 50mv. The plot on figure (26) shows the trip point characteristics obtained by negative programming.

Programming mode : Programming on the DUT here can be done either on negative programming terminal VPGMN or on the positive programming terminal VPGMP or on both together to get the desired trip point shift based on the set of conditions and governed by the equations presented in chapter 3.

- During the programming mode power supply terminals are set to ground or their respective values. However the setup has to remain essential consistent for each programming epic.
- Programming on VPGMN is done by grounding the input VIN and VPGMP. A DC programming pulse that is either positive or negative in magnitude is applied to VPGMN for a fixed duration of time. Programming on VPGMP is done similarly by grounding VPGMN.
- Choice of programming voltages can be inferred from the injector characteristics obtained earlier.
- Programming time ranged from 1sec. to 30sec. duration with no noted variation in performance.

The shift in trip point with programming voltage increments was observed to be approximately 100mv. This indicated that the quantum for the ADC can be set to a fair

degree of accuracy with 100-125mV range. The range of trip point shifts observed were as far as +/-2.5V or 5 plus bits of accuracy.

4.3.3.2 REGENERATIVE COMPARATOR CHARACTERIZATION RESULTS AND INFERENCES

To obtain the trip point characterization by programming the DUT is repeatedly set between the trip point measurement mode and a programming mode with programming increment between each trip point measurements. The trip point measurement mode has already been explained in the earlier section.

Programming mode : In this mode the comparator is programmed to shift the trip point in a specific direction.

- Programming is done by charge injection or removal by applying a **DC programming voltage** for a fixed time only on the **V_REF** end.
- In this mode **VIN, V_PGMP & V_REF** are grounded for the entire mode of operation.
- Comparator is in a **reset mode** during this entire mode of operation.
- A DC programming pulse for a fixed duration is applied to **V_PGMN**.
- **A positive pulse** is applied to remove electrons from **V_REF** floating node.(this shifts the trip point in a positive direction)
- **A negative pulse** is applied to inject electrons onto the **V_REF** floating node. (this shifts the trip point in a negative direction)

- **Choice of programming voltages** must be inferred from the injector characterization results shown earlier.
- **Programming time** ranges from **10ms to 1sec** (a **0.5ms rise time** on the pulse was used). It is better to use programming pulses of longer duration as the programming current saturates with time.
- Repeated programming at the same voltage will not shift the trip point.

After programming, the comparator is switched to the Trip point measurement mode.

Trip point measurements with coarse programming increments :

- Trip point was shifted in a positive and negative direction with coarse programming voltage increments of 500mv and 250mv.
- The shift in trip point with coarse programming voltage increments was observed to be linear in both the positive and negative directions.
- Trip point shifts as far as +/-2.5V were observed.

(refer to figure 27).

Trip point measurements with fine programming increments :

- The trip point was shifted in the positive and negative direction with fine programming increments of 10mv.
- The shift in the trip point with fine programming increments was observed to be more linear in the negative direction than in the positive direction.
- A 20mv shift approximately was observed in trip point with every 10mv step in programming voltages.

(refer to figure 28, 29 &30)

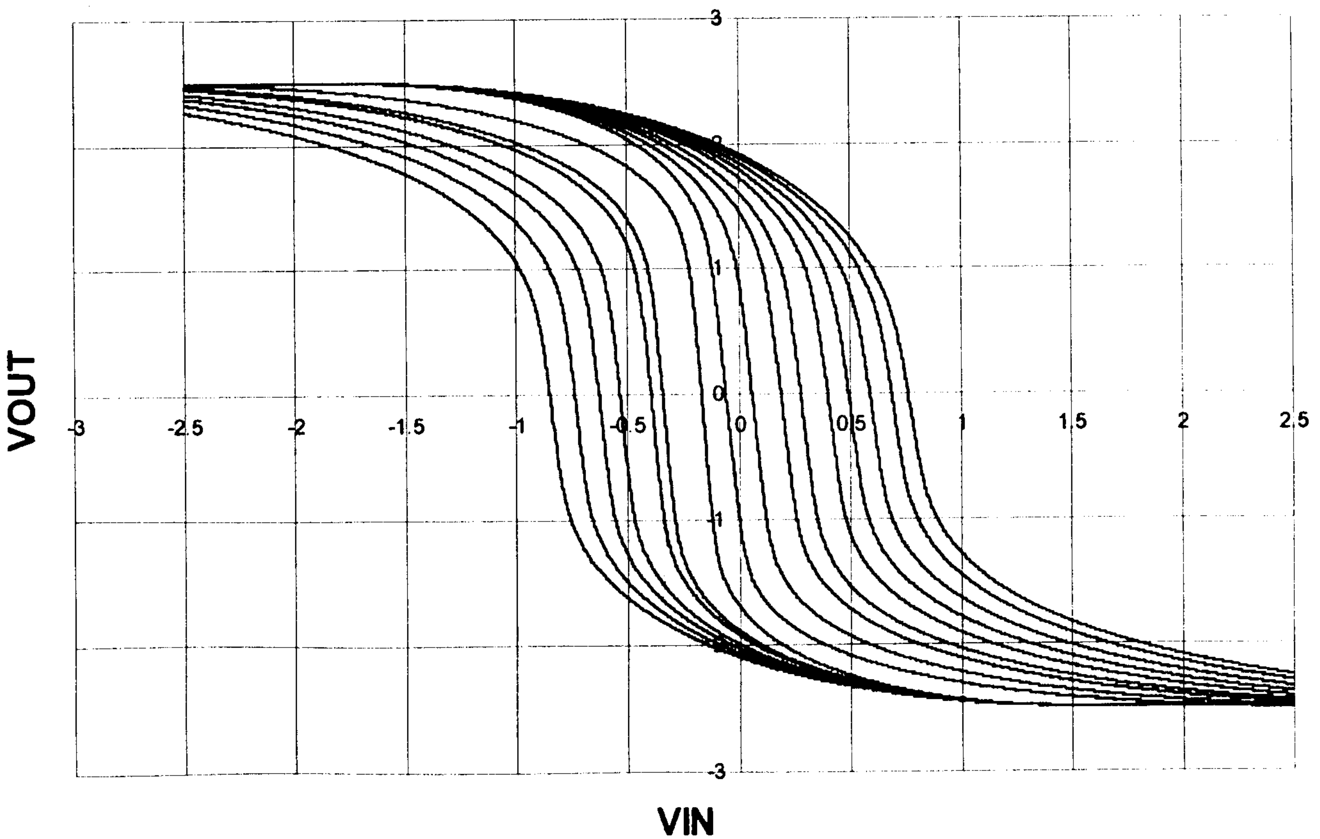

Figure 26: Bulk Comparator trip point characteristics obtained by testing.

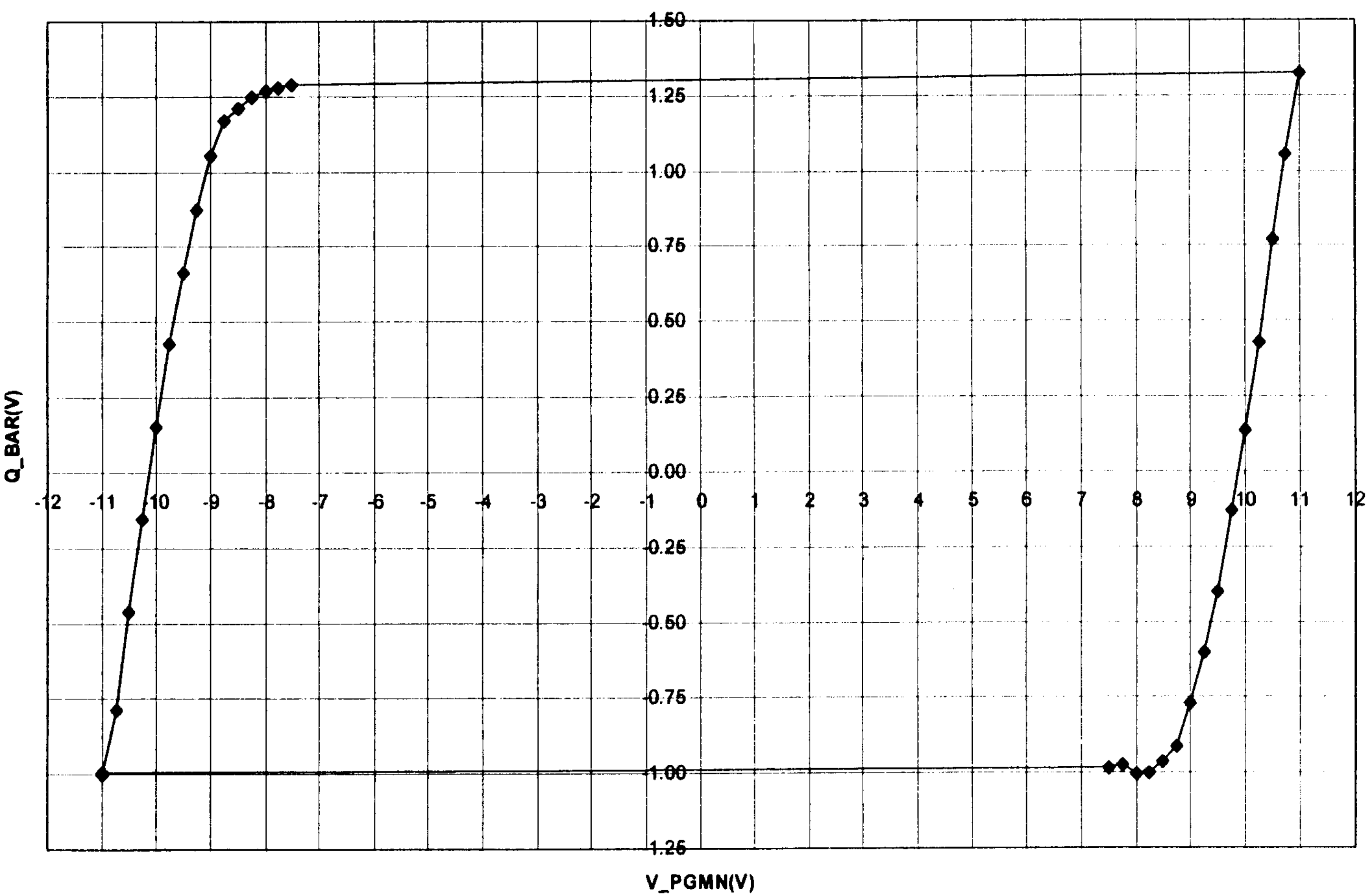

Figure 27: Coarse programming trip point characteristics obtained by testing.

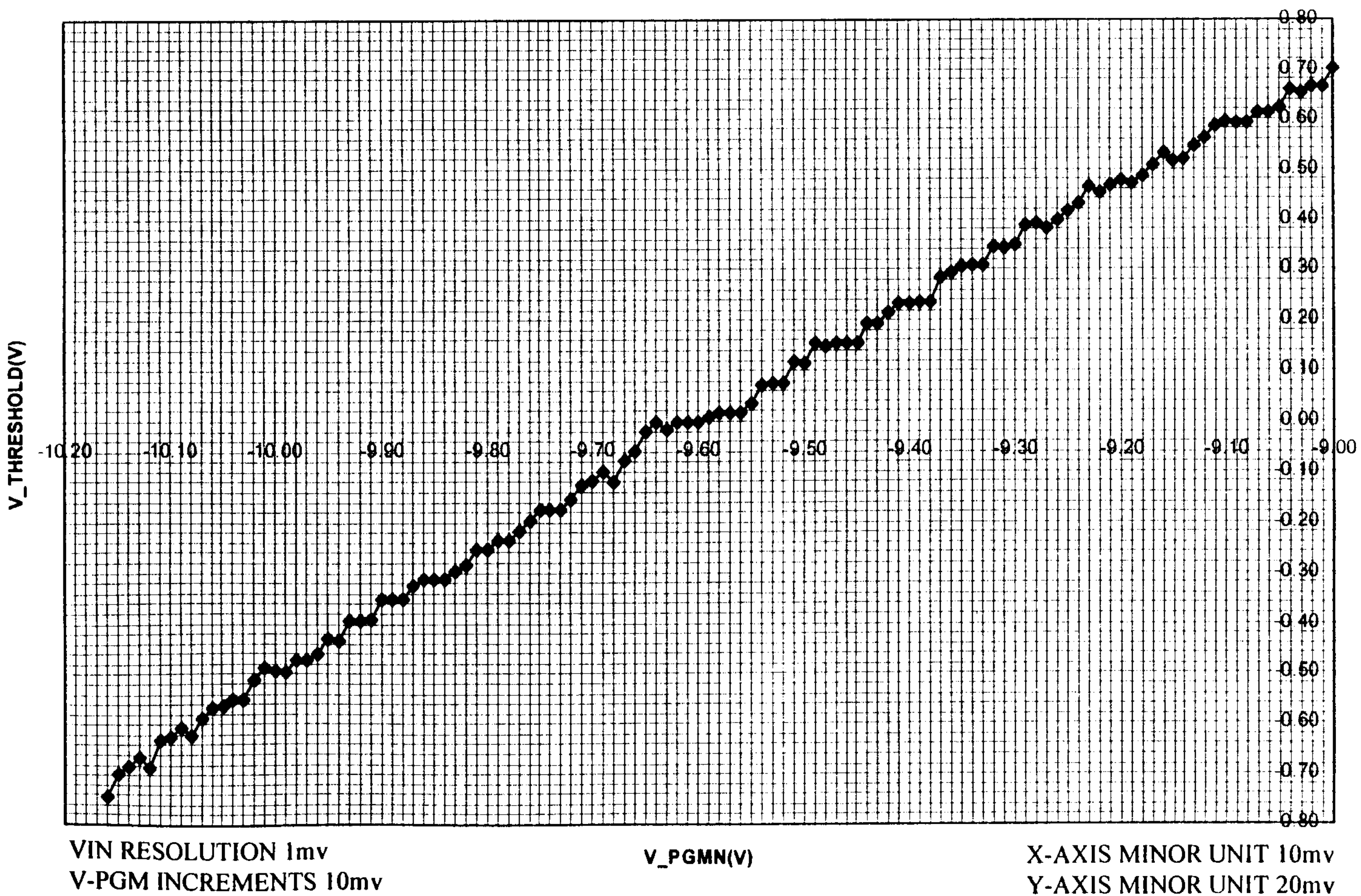

Figure 28: Fine negative programming voltage increments trip point characteristics.

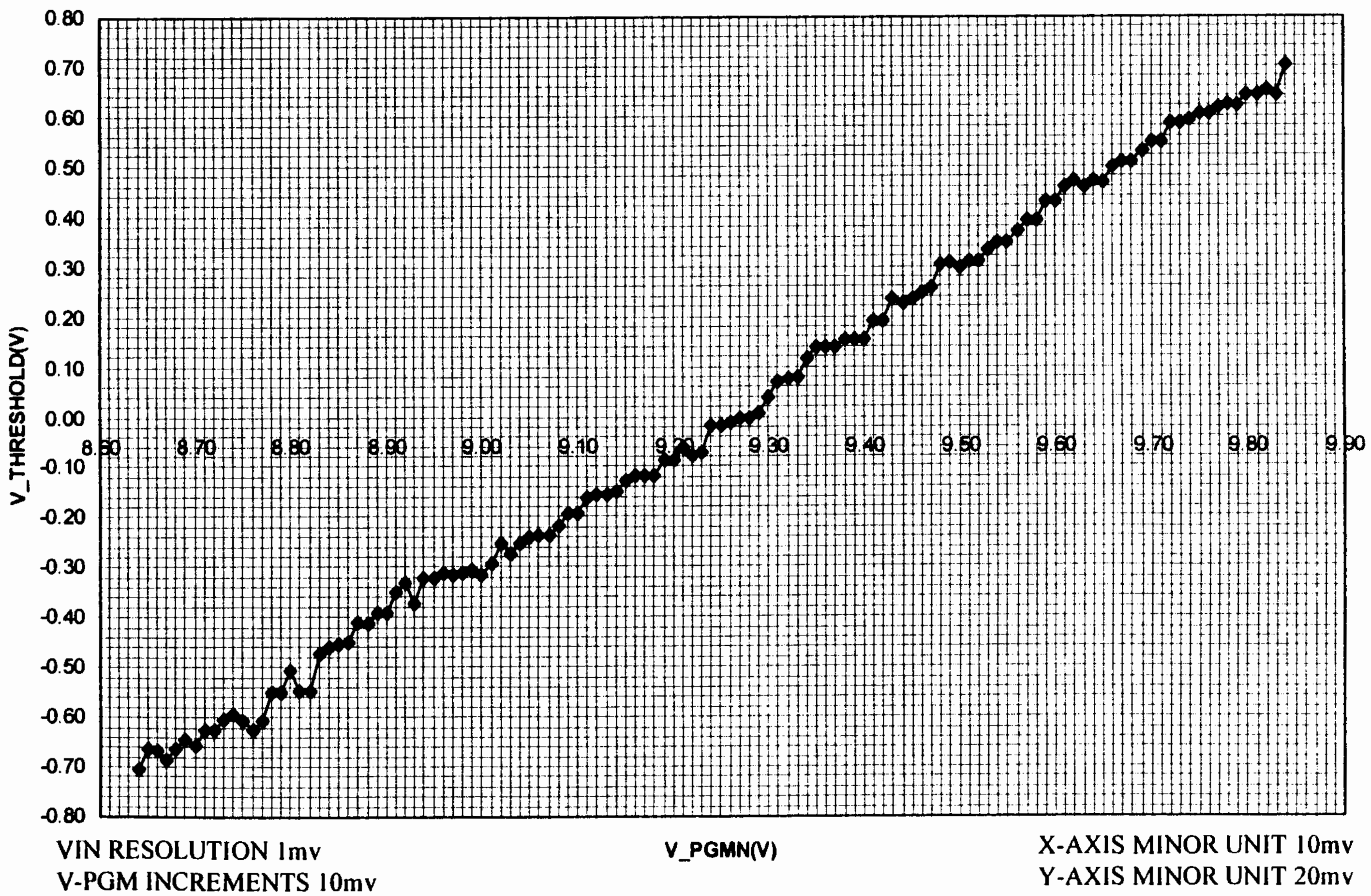

Figure 29: Fine positive programming increments trip point characteristics obtained by testing.

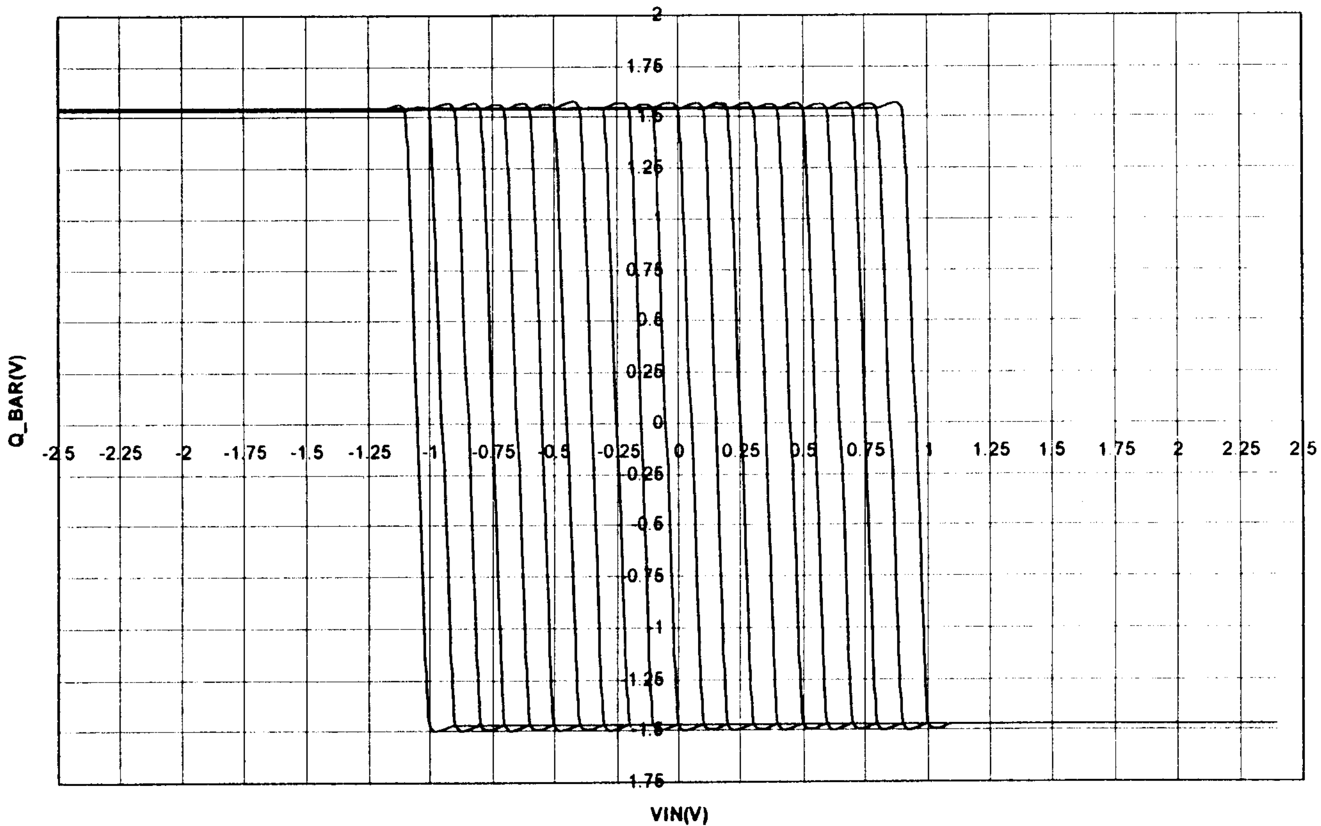

Figure 30: Trip point characteristics obtained by negative programming.

4.3.4 SHORT TERM CHARGE RETENTION STUDY ON FG COMPARATORS

To characterize floating gate circuits for short term retention, the variation in trip point with time is to be measured at room temperature. There is no fixed choice of time when measurements have to be made [11]. However trip point measurements every few minutes, few hours, and few days of completing programming is a good measure of charge retention. It is essential for our application to measure the trip point with at least a 10mv accuracy or less. A program that can do repeated measurements in short intervals of time and run overnight is a good way to characterize the circuit for short term variation in charge. It is critical that the variation of charge on the FG be maintained less than ½(LSB) for use as a building block for an ADC. The test setup allowed measurement to 1mV accuracy.

4.3.4.1 SHORT TERM CHARGE RETENTION STUDY ON BULK DEVICES

The short term charge retention for the bulk devices was done during a 15 minute recovery period as well as over extended periods of time lasting a few days. The following observations were made :

- Variation of charge during a 15 minute recovery period post programming was < +/-2.5mv.

- Negligible variation within constraints of the test setup was observed on the devices over extended periods of time, in this case 15 to 30 days.

4.3.4.2 SHORT TERM CHARGE RETENTION STUDY ON SOS DEVICES

At this point it is believed that an exposed M2 layer on the floating node of the comparator circuit is the cause of significant charge loss in addition to the lack of passivation on the wafers. In future designs and fabrication runs it is desirable to eliminate this exposed M2 layer from the floating node before any more retention tests can be done. Alternatively the existing wafer could be passivated.

Test wafers were programmed and left overnight with and without storage in a dry box and the following observations were made.

SHORT TERM RETENTION STUDY WITH MEASUREMENTS IN 1hr INTERVALS & WITHOUT STORING IN A DRY BOX: [wafer - 11, die 2 3]

- TRIP point before programming = +0.1V
- TRIP point after programming -ve $V_{TRP(0)}$= -0.39V
- TRIP point after 1hr of the above measurement $V_{TRP(1hr)}$ = -0.35V

  The shift in trip point by 40mv can be attributed to a charge (electrons) loss.

- TRIP point after 2hrs of completing programming $V_{TRP(2hrs)}$ = -1.1V

This significant shift in the trip point can be attributed to a charge gain in some unknown manner.

All the above measurements were made with the wafer on the probe station and probes on the circuit.

SHORT TERM RETENTION STUDY WITH MEASUREMENTS MADE IN 72hrs & WITHOUT STORING IN A DRY BOX: [wafer - 11, die 1_1, 1_2, 2_2, 2_3]

4 devices were programmed in and around +/-1V and left in a wafer carrier. The devices were probed after 72 hours.

- Significant shift of the order of 900mv in trip points were observed on all the devices.

All shifts were in a direction to indicate charge loss.

SHORT TERM RETENTION STUDY WITH MEASUREMENTS MADE IN 16hrs & WITH STORING IN A DRY BOX: [wafer - 11, die 1_4, 1_3]

2 devices were programmed and placed in a wafer carrier to be stored in a dry box overnight. Measurements were made by probing the circuit after this period on the probe station.

DEVICE 1:[die 1_4]

- TRIP point before programming = +0.25V

- TRIP point after programming +ve $V_{TRP(0)}$= +1.07V
- TRIP point after 16hrs of the above measurement $V_{TRP(16hrs)}$ = +1.04V

DEVICE 2:[die 1_3]

- TRIP point before programming = +0.40V
- TRIP point after programming -ve $V_{TRP(0)}$= -0.78V
- TRIP point after 16hrs of the above measurement $V_{TRP(16hrs)}$ = -0.69V

A drastic reduction in charge loss/gain was observed. This validates the need for passivation and / or preferable removal of the exposed M2 layer from the floating node.

SUMMARY:

- Probing the wafers on the probe station did not have any significant influence on charge retention as repeated measurements were made on the same device with negligible variation in trip point.
- Storing the wafers in a dry box did have significant control on the charge retention.
- Future designs need removal of exposed M2 layer from floating node.
- Passivation of wafers is essential for charge retention study.

4.3.4.3 TECHNIQUES FOR SUPERIOR DATA RETENTION

It has become well known through out the industry that the use of oxy-nitride or UV transparent nitride passivation is a general technique to improve data retention. The use of LPCVD (low pressure chemical vapor deposition) nitride between the double poly

gate structure and the poly metal isolation dielectric is the proposed technique suggested in the literature to reduce the possibility of contamination of the floating gate area.

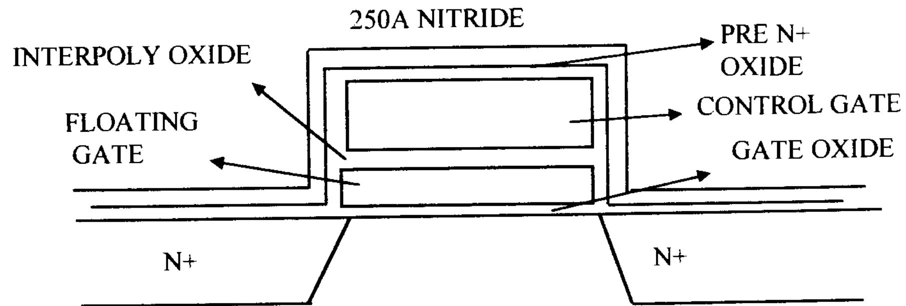

Figure 31: Schematic cross section showing LPCVD 250A Nitride passivation on FG device.

4.3.5 LONG TERM CHARGE RETENTION STUDY

A good measure of long term charge retention of floating gate comparator circuits is to bake the circuits at elevated temperatures and measure the variation in trip point. Based on the amount of charge on the floating gate before and after bake, we can predict circuit charge retention at room temperature. This is based on the assumption that the retention time characteristic at elevated temperatures is described on the following thermionic emission model [17].

$$\ln \frac{\ln\left(\frac{Q(0)}{Q(t)}\right)}{tv} = -\phi_B \frac{1}{KT} \tag{33}$$

$$\frac{Q(t)}{Q(0)} = \frac{V_{TRP(t)} - V_{TRP0}}{V_{TRP(0)} - V_{TRP0}} \tag{34}$$

where,

ϕ_B is the Energy Barrier at the polysilicon - oxide interface.

γ is the dielectric relaxation frequency of electrons in polysilicon.

K is the Boltzmans constant.

T is the temparature in degree kelvin.

V_{TRP0} is the TRIP POINT before any charge has been transferred onto the floating gate.

(best results are obtained when UV erasure preceeds measurement of V_{TRP0})

$V_{TRP(0)}$ is the initial TRIP POINT obtained and set by programming.

$V_{TRP(t)}$ is the TRIP POINT after time oven exposure at time t.

We can extrapolate a straight line based on a LMS fit of atleast three different readings when plotting :

$$\ln\frac{\ln\left(\frac{Q(0)}{Q(t)}\right)}{t\gamma} \text{ vs } \frac{1}{KT}$$

From the slope and Y - intercept of the above plot we can obtain ϕ_B and γ.

METHODOLOGY FOR BAKING CIRCUITS:

1. To ascertain the ***TRIP point before any charge has been transferred to the gate*** is a) UV erase the circuit or b) measure the TRIP point of a naive circuit without any injector devices on them. The later is the only approach when charge cannot be erased using UV light on wafer structures.

2. Programming the devices to trip at *+/-1V* is a good choice as the comparator is desired to operate within this range. This is the ***initial TRIP point***. The choice of programming voltages must be inferred from the floating gate comparator characterization results obtained previously. Any voltage exceeding full scale reference but not forcing the circuit out of its linear range of operation is acceptable.

3. The choice of bake temperatures is critical in the experiment. Analysis has shown that temperature is the most critical parameter effecting charge retention measurements. A 1 % variation in temperature causes a 7 % variation in estimate of ϕ_B and a 1 % variation in the estimate of ϕ_B leads to 16 % variation in the estimate of retention time. Thus setting the temperature to a high degree of accuracy is essential. It is also essential to keep the bake temperatures less than 200c to ensure that Fowler Nordhiem is the dominant tunneling mechanism[2]. At this point it has been determined to bake the circuits at four different temperatures to ensure best LMS fit for a fixed period of time. The temperatures being ***120c to 180c in 20c intervals*** were selected for best results.

4. A good choice of bake time is probably a ***2hr time with a 15min interval before measurement and after bake.*** Care has to be taken to make sure that the wafer is placed on a cold chuck after oven exposure to ensure that wafer equilibrates to room temperature in the same amount of time that it took to equilibrate to oven temperature when placed on a hot chuck to ensure a known time - temperature exposure or dose. Thus the wafer has equally quick rise and fall times as far as temperature changes are concerned. Thus ***placing the wafer on the probe station chuck after oven exposure*** is a simple approach taking into consideration the above concerns.

To summarize the procedure :

- Measure V_{TRP0} from a naive circuit or an UV erased circuit with injectors.
- Measure $V_{TRP(0)}$ based on the trip point set by programming the circuit.
- Bake the wafer to start with at a temperature 120c for a 2hr period.
- Measure $V_{TRP(t)}$ after 15min of taking the wafer out of oven and placing on a cold chuck.

- Repeat baking the wafer at an elevated temperature. (20c increment in temp each time)
- Ensure temperature setting to a 1 % accuracy.
- Ensure trip point measurements to a 1mv accuracy.
- Analysis and inference of retention time can be done based on the analysis given earlier.

4.3.5.1 LONG TERM CHARGE RETENTION STUDY ON NRaD SOS TECHNOLOGY

Due to lack of passivation and an exposed M2 layer on the floating node charge retention study could not be done effectively on the FG regenerative comparator structures. However the study was performed on neural test weights fabricated in the same process to infer the data retention properties. The results that were obtained are expected to be same for the FG injector structures as well as the data retention is a highly process dependent parameter.

TEST PROCEDURE FOR CHARGE RETENTION OF WEIGHT MATRICES

To measure the charge retention of the weight matrices, **TEST_WEIGHT_1** cells of neural net **TEST CHIP 1** were used. All the tests were completed avoiding as much light exposure as possible. The following procedure was used to collect the data for determining charge retention,

1) The wafer was exposed to ultra violet light before making the measurement for the naive current referred to as I(**NC**).

2) All the weights were programmed "Up" and "Down" four times before programming to a specific current. Then, four of the weights were programmed "Up" and the others were programmed "Down" for a fifth programming cycle. These programmed currents were referred to as **I(initial)**.

3) After programming the weights, they were baked for 1hr time at 120c, 140c and 160c respectively. Each time after baking the wafer it was cooled on a cold chuck for about 20 minutes and the currents were then measured. These currents are referred to as **I(t-120), I(t-140)** and **I(t-160).**

Now, with the values of I(NC), **I(initial), I(t-120), I(t-140)** and **I(t-160)** charge retention of weight matrices was evaluated using the procedure explained below.

The table below shows the temperature bake data obtained from the test weights.

DIE	NC	I(initial)	I(t-120)	I(t-140)	I(t-160)	Q(t1)/Q(0)	Q(t2)/Q(0)	Q(t2)/Q(0)
(-10,-7)	-1.61	-0.679	-0.77	-0.95	-1.57	0.902256	0.708915	0.042965
(-9,-5)	-1.66	-0.7	-0.749	-0.903	-1.54	0.948958	0.788542	0.125
(-9,-6)	-1.64	-0.678	-0.719	-0.848	-1.51	0.95738	0.823285	0.135135
(-9,-8)	-1.59	-0.685	-0.72	-0.926	-1.53	0.961326	0.733702	0.066298

Table 1: Physical data from the neural test weights.

SUMMARY OF CALCULATIONS FOR LONG TERM DATA RETENTION STUDY ON TEST WEIGHTS:

Based on the test data that was obtained by baking the wafer at elevated temperatures the following procedure was adopted to project the charge retention time:

The following equations were used to describe the characteristics:

$$\frac{Q(t)}{Q(0)} = \frac{I(t) - I(NC)}{I(initial) - I(NC)} \quad (35)$$

I(NC) is the Naive Current.

(best results are obtained when UV erasure precedes measurement of I(NC))

I(initial) is the initial current set by programming.

I(t) is the current after time oven exposure at time t.

We can extrapolate a straight line based on a LMS fit of at least three different readings when plotting :

$$\ln\frac{\ln\left(\frac{Q(0)}{Q(t)}\right)}{t\gamma} \quad \text{vs} \quad \frac{1}{KT}$$

From the slope and Y - intercept of the above plot we can obtain ϕ_B and γ .

From the 3 different bake temperature measurements Q(t1)/Q(0), Q(t2)/Q(0), Q(t3)/Q(0) was calculated based on I(t-120), I(t-140), I(t-160). Now, using the equation of a straight line and considering ,

$$\mathbf{Y = -\ln(-\ln[\frac{Q(t)}{Q(0)}])} \quad \mathbf{(36)}$$

and

$$\mathbf{X = \frac{1}{kT}} \quad \mathbf{(37)}$$

three data points (X1,Y1; X2,Y2; X3,Y3) were determined based on the 3 bake temperatures from the above two equations.

Slope and intercept was then inferred from a linear regression fit on the 3 points for each data set.

Slope indicated the value of the barrier height, (ϕ_B). From the intercept, 'gamma (γ)' the dielectric relaxation frequency was calculated using the equation,

$$\gamma = \frac{e^{-\text{int ercept}}}{\text{bake} - \text{time}} \quad (38)$$

The table below gives the three points obtained from a linear regression fit of the above data as explained earlier.

Y1	Y2	Y3	X1	X2	X3	SLOPE	INT	GAMMA
2.274412	1.067057	-1.14657	1.59E+16	1.51E+16	1.44E+16	2.26E-15	-33.5059	9.88E+10
2.949032	1.437293	-0.7321	1.59E+16	1.51E+16	1.44E+16	2.44E-15	-35.7183	9.03E+11
3.133744	1.637564	-0.69389	1.59E+16	1.51E+16	1.44E+16	2.53E-15	-36.7851	2.62E+12
3.232931	1.172304	-0.99827	1.59E+16	1.51E+16	1.44E+16	2.82E-15	-41.4647	2.82E+14

Table 2: Linear regression fit data.

Based on the above values the retention time (considering a 1% effective charge loss at room temperature and a 6-7 bits accuracy for the system) 't' was estimated using the equation (39) derived from the model equation (33) & (34) :

$$\ln(t) = \frac{\phi_B}{kT} + \ln\left[-\ln\left(\frac{Q(t)}{Q(0)}\right)\right] - \ln(\gamma) \quad (39)$$

The terms of the equations were considered as

$$A = \ln(t) \quad (40)$$

$$B = \frac{\phi_B}{kT}\text{ , T is room temperature -300K} \quad (41)$$

$$C = -\ln(-\ln[\frac{Q(t)}{Q(0)}]) \quad (42)$$

$$D = \ln(\gamma) \quad (43)$$

and the equation is reduced to, A=B-C-D. So, the projected time is,

$$t = e^{-A} \text{ in seconds} \quad (44)$$

The projected time indicates the retention time at room temperature.

Based on the linear regression fit obtained earlier in table 2 the data retention time is projected as explained before. The results are summarized below in table 3.

B	C	D	A	TIME PROJECTED
47.13323	4.91	25.31636	16.90687	**254 DAYS** ON DIE (-10, -7)
50.84852	4.91	27.52899	18.40953	**3YRS** ON DIE (-9, -5)
52.64542	4.91	28.5942	19.14122	**6.5 YRS** ON DIE (-9, -6)
58.64584	4.91	33.27293	20.46291	**24 YRS** ON DIE (-9, -8)

Table 3: Projected data retention time.

RESULTS :

- Using the procedure described above and data obtained the mean values of ϕ_B and γ were found to be 1395.034 ev & 5.7E+13 s^{-1} respectively.
- The projected long term charge retention with an accuracy of 6-7 bits (1%) is 6.8 years (mean) at less than 27C°.
- Projected performance for the 4 bit quantizer that comprised of the regenerative comparator is expected to track that of TEST_WEIGHT_1 after the replacement of metal 2 in the comparator cell.

4.3.5.2 LONG TERM CHARGE RETENTION STUDY ON MOSIS BULK TECHNOLOGY

Using a similar procedure as explained in the earlier section the dual blocking dual injector comparator was exposed to bake temperatures in the range of 160C to 200C for a period of 1 hour with 3 bake turns. Trip point measurements were made before and after bake to infer the charge retention time. The charge variation was estimated using equation (34).

The results of the study are summarized below.

Summary:

At room temperature, a 50% yield was estimated (from a lot of 8 device measurements made) with a charge retention of ½ quantum. The mean of the charge retention time was estimated to be in excess of 10 years. Also consistency was observed in terms of the retention time for the devices that were on the same die.

4.3.5.3 SUMMARY OF SENSITIVITY OF PARAMETERS IN THE LONG TERM CHARGE RETENTION STUDY MODEL

The various parameters that are involved in the model play a significant role in estimating the charge retention time. Accurate estimation of trip points, currents as explained earlier are essential. A summary of the sensitivity issues are presented below.

1. Variation in estimate of trip point measurements by 1% leads to variation in estimate of ϕ_B by 0.011%.

2. Variation in temperature by 1°C leads to variation in the estimate of ϕ_B by 7%.
3. The variation in estimate by ϕ_B by 1% in turn leads to a variation in the estimate of time by 30 to 40 minutes.

The above observations calls for accurate measurements of the trip points, and setting of the temperatures in the oven. Hence measurement of trip points was done with a 1mv resolution and temperature settings were accurately monitored to +/-1°C.

4.3.5.4 EFFECT OF OXIDE THICKNESS ON CHARGE RETENTION TIME :

The charge retention time of floating gate devices depends on the property of the oxide and the chemical process involved in fabrication of the device. Thicker the oxide, better the retention characteristics. Thick oxide floating gate devices will have better charge retention properties as compared to thin oxide floating gate devices [1,2]. The addition of thin layers of silicon nitride is naturally used in commercial processes to greatly enhance retention time.

The charge retention characteristics will be drastically degraded, if oxide thickness of less than 60A^0 are used, because of the direct tunneling effect in the oxide. However up to this thickness, the retention characteristics are mainly dominated by the barrier height of the Field Oxide (FOX) layer, surrounding the floating gate, rather than that of the gate oxide.

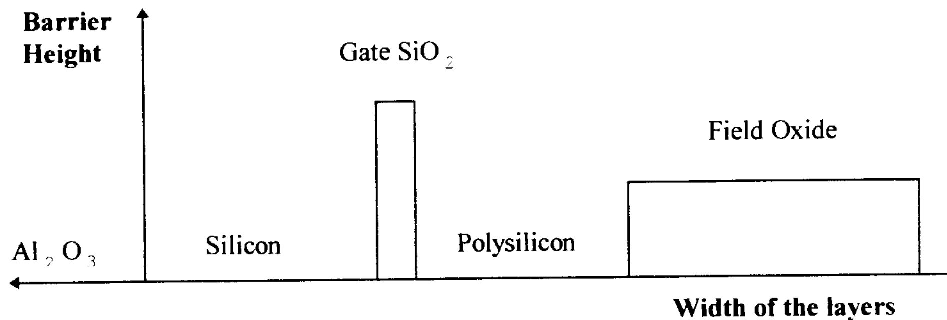

Figure 32: Dominating effect of gate oxide over field oxide.

4.4 SUMMARY OF CHARACTERIZATION RESULTS

This section summarizes the characterization results for both the BULK and SOS technologies based on the characterization results obtained by testing and inferences on the feasibility of the approach are presented.

4.4.1 MOSIS BULK RESULTS

- **Programming Onset :** The Onset of charge injection into and out of the floating gate was determined empirically to be approximately +/- 12.00 Volts. A symmetrical injector structure was laid out and tested. The maximum programming voltage on the

structure was estimated as +/-27V. The Fowler Nordhiem characteristic constants were extracted to be $\alpha = 6.027$ and $\beta = 0.93 \times 10^9$ V/m.

- **Comparator Trip points** were programmed in incremental steps with programming Steps of 50 mVolts. The comparator trip points were set to a good degree of accuracy to a 100mv resolution indicating the feasibility of building a 4-bit quantizer at +/-1V full-scale.
- **Short Term Degradation :** Variation of the charge during a 15 minute recovery period post programming was less than +/-2.5 mVolts. Thus the structures had good charge retention properties as far as short term effects are concerned.
- **Long Term Degradation:** At room temperature, a 50% yield was estimated for the comparators from a lot of 8 devices tested. The mean charge retention time for 1/2 Quantum (62.5 mv) was in excess of 10 years. A 50% yield on the devices tested within the constraints of the test measurements was observed to be good as the no special processing techniques were employed. The projected Accuracy for the quantizer at +/-1 Volt FS, in-situ calibration of floating gate voltages, +/-2.5 mVolts of Short Term Degradation, the accuracy is greater than 6 bits.

4.4.2 SOS RESULTS

- **INJECTOR CHARACTERIZATION :** Programming voltage to initiate charge injection or removal was observed to be +/-8V. The maximum programming voltage was approximately +/-13V before breakdown. The injector structure was observed to

be symmetrical in nature. The Fowler Nordhiem characteristic constants were extracted to be $\alpha = 6.07$ and $\beta = 1.2 \times 10^9$ V/m.

- **COMPARATOR CHARACTERIZATION :** Functionality of the comparator was demonstrated Trip point measurements were made with VIN resolutions of 500mv, 250mv, 100mv, 10mv & 1mv.
- **COMPARATOR TRIP POINT CHARACTERIZATION & PROGRAMMING**: Comparator trip points were shifted in the positive and negative direction. Approximately a 20mv shift in trip point was observed with every 10mv step in programming. Effects of the test measurement setup, or lack of passivation on the wafers has to be identified to explain the erroneous drift in certain trip points with programming. The overall observations made leads to the inference that a 6-7 bit quantizer is feasible.
- **SHORT TERM RETENTION STUDY :** It is believed that an exposed M2 layer on the floating node and lack of passivation on the wafers is causing this significant charge loss. Future designs will require removal of this exposed M2 layer. For further data retention study existing wafer passivation is essential.
- **LONG TERM RETENTION STUDY :** The projected long term charge retention with an accuracy of 6-7 bits (1%) is 6.8 years (mean) at less than 27C°. Projected performance for the 4 bit quantizer that comprises of the regenerative comparator is expected to track that of TEST_WEIGHT_1 cells after the replacement of metal 2 in the comparator cell.

CHAPTER 5

CONCLUSION AND FUTURE PROSPECTS

Validation of the approach of building floating gate references for ADCs through investigation and development of injector models by means of device characterization has indicated a clear possibility of a scope for an application. The designed devices though have certain critical limitations in terms of their charge retention time, special fabrication procedures as suggested in chapter 4 can be extended to future designs to overcome the inherent limitations.

Future designs in bulk can aim at achieving a higher number of bits on the order of 7-8 bits by either thinning of the oxide, increasing the irregularities at the tunneling interface by means of laying out poly slabs with 8 to 10 edges versus 4 edges for the current design or decreasing the relative area of the injector. Irregularities in the texture of the poly interface has revealed the feasibility of a resolution of 10 bits as suggested in the chapter 2. Future designs can explore this possibility. These modifications not only explore the possibility of realizing larger number of bits of resolution, but also lower programming voltages due to field enhancement.

The developed injector structures can be extended to use in neural network weights and other wide area of applications as analog memory.

Future SOS injector designs can aim at lower programming voltages by any of the techniques mentioned above. Also techniques for superior data retention have to be utilized to improve the charge retention time on these structures.

An in-situ programming algorithm should be developed and extended to silicon to build a fully self calibrating quantizer with programmable references based on the methods verified in this research. The designed ADC will find wide applications in low power applications, especially in telecommunications.

For the charge retention properties, future designs will have to utilize Nitride passivation of the structures as explained earlier which in turn will greatly improve the retention characteristics.

BIBLIOGRAPHY

[1]. K. Kato, "Low Voltage Analog Circuit Design Techniques: A Review," IEICE Trans. Electron, Vol. E78, No. 4, pp. 414 - 423, April 1995.

[2]. C.G. Hutchens et al., "Proposed 16 bit 1mw 2KSPS ADC," Proposal to NRaD, San Diego, CA, April 1996.

[3]. O. Fujita, "A Floating - Gate Analog Memory Device for Neural Networks," IEEE Transactions on Electron Devices, Vol. 40, No. 11, pp. 2029 - 2035, November 1993.

[4]. D. A. Durfee, et al., "Low Programming Voltage Floating Gate Analog Memory Cells in Standard VLSI CMOS Technology," Electronics Letters, Vol. 28, No. 10, pp. 925 - 927, May 1992.

[5]. B.W. Lee, et al., "Analog Floating - Gate Synapses for General - Purpose VLSI Neural Computation," IEEE Transactions on Circuits and Systems, Vol. 38, No. 6, pp . 654 - 658, October 1986.

[6]. J. Miyamoto, et al., "An Experimental 5 - V - Only 256 - kbit CMOS EEPROM with a High Performance Single - Polysilicon Cell," IEEE Journal of Solid State Circuits, Vol. Sc - 21, No.5, pp. 852 - 859, October 1986.

[7]. C. K. Sin, et al., "EEPROM as an Analog Storage Device, with Particular Applications in Neural Networks," IEEE Transactions on Electron Devices, Vol. 39, No. 6, pp. 1410 - 1419, June 1992.

[8]. A. Thomson, et al., "Low Control Voltage Programming of Floating Gate MOSFETs and Applications," IEEE Transactions on Circuits and Systems, Vol. 41, No. 6, pp . 443 - 452, June 1994.

[9]. P. Manos, et al., "A Self Aligned EPROM Structure with Superior Data Retention," IEEE Electron Device Letters, Vol. 11, No.7, pp. 309 - 311, July 1990.

[10]. S. C. Gong, et al., "Evaluation of Q_{bd} for Electrons Tunneling from the Si/SiO_2 Interface Compared to Electron Tunneling from the Poly - Si/SiO_2 Interface ," IEEE Transactions on Electron Devices, Vol. 40, No. 7, pp. 1251 - 1257, July 1993.

[11]. A. Thomson, et al., "A Floating Gate MOSFET with Tunneling Injector Fabricated Using a Standard Double - Polysilicon CMOS Process, Vol. 12, No. 3, pp . 111 - 113, March 1993.

[12]. B. Fishbien, et al., "Measurement of Very Low Tunneling Current Density in SiO_2 Using the Floating Gate Technique," IEEE Electron Device Letters, Vol. 12, No. 12, pp . 713 - 715, December 1991.

[13]. K. Ohsaki, et al., "A Single Poly EEPROM Cell Structure for Use in Standard CMOS process," IEEE Journal of Solid State Circuits, Vol. 29, No.3, pp. 311 - 316, March 1994.

[14]. C. Fiegna, et al., "Oxide Field Dependance of Electron Injection from Silicon into Silicon Dioxide," IEEE Transactions on Electron Devices, Vol. 40, No. 11, pp. 2018 - 2022, November 1993.

[15]. A. Concannon, et al "Two Dimensional Numerical Analysis of Floating Gate EEPROM Devices," IEEE Transactions on Electron Devices, Vol. 40, No.7, pp. 1258 - 1262, July 1993.

[16]. M. Lanzoni, et al., "Experimental Characterization of Circuits for Controlled Programming of Floating Gate MOSFET's," IEEE Journal of Solid State Circuits, Vol. 30, No.6, pp. 706 - 709, June 1995.

[17]. L. Carley, et al, "Trimming Analog Circuits using Floating Gate Analog MOS Memory," IEEE Journal of Solid State Circuits, vol. 24, no.6, pp. 1569 - 1575, December 1989.

[18]. D. R. Walters, et al., "Fowler Nordhiem Tunneling in Implanted MOS Devices," Solid State Electronics, Vol. 30, No.8, pp. 835 - 839, January 1987.

[19]. B. Euzent, et al., "Reliability issues of Floating E^2PROM," IEEE Proc. IRPS 11, pp. 11 - 16.

[20]. S. Keeney, et al, "Complete Transient Simulation of FLASH EEPROM Devices," IEEE, IEDM 90-201, pp. 8.7.1 - 8.7.4.

[21]. Y.Y. Chai, et al, "A 2X2 Array Analog Memory Implemented with a Special Layout Injector," Ph.D Dissertation, Oklahoma State University, October 1994.

[22]. S. Gowder, et al, "A Proposed 10 Bit 1GhZ Analog to Digital Converter for Implementation in TFSOI," M.S. Thesis, Oklahoma State University, December 1994.

[23]. J. Tsrong, et al, "A 100 MhZ Pipelined CMOS Comparator." IEEE Journal Of Solid State Circuits, vol. 23, pp. 420-430, December 1988.

[24]. G.M. Yin, et al, "A High Speed CMOS Comparator with 8-b Resolution." IEEE Journal Of Solid State Circuits, vol. 27, pp. 208-211, February 1992.

[25]. Y.Horio, et al, "Artificial Neural Networks: Paradigms, Applications and Hardware Implementations," New York, NY, IEEE Press, 1992.

[26]. R.V.D. Plassche, et al, "Integrated Analog To Digital and Digital To Analog Converters," Kluwer Academic Press, 1994.

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