## FIRST ORDER QUASI STATIC MOSFET CHANNEL

## CAPACITANCE MODEL

By

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## LIST OF SYMBOLS

SYMBOLS		NAMES
$q_{c}$		channel charge per unit length
$q_{c0}$		zero order channel charge per unit length
$q_{c1}$		first order channel charge per unit length
$q_s$		source charge per unit length
$q_{d}$		drain charge per unit length
$q_g$		gate charge per unit length
L		channel length
W		channel width
$c_{ox}$		oxide capacitance per unit length
<sup>v</sup> fb		flat band voltage
$v_{t0}$		threshold voltage at zero source bias
v <sub>t</sub>		threshold voltage
$\phi$		fermi potential
$t_{ox}$		oxide thickness
<sup>v</sup> cb		channel terminal voltage
<sup>v</sup> gb		gate terminal voltage
vsb		source terminal voltage

SYMBOLS		NAMES
<sup>v</sup> db		drain terminal voltage
$k_1$		body effect coefficient
$k_2$		body effect coefficient
<i>I</i> <sub>c0</sub>		zero order (static) current
$I_D$		static drain current
IS		static source current
$I_{G}$		static gate current
I <sub>B</sub>		static substrate current
I(t)		total channel current
<sup>i</sup> d1		first order drain current
i <sub>s1</sub>		first order source current
i <sub>g1</sub>		first order gate current
i <sub>b1</sub>		first order substrate current
i d1,con	s	first order conserved drain current
i s1,cons	s	first order conserved source current
i d1, diss	5	first order dissipative drain current
i s1, diss		first order dissipative source current
$\overline{P_{c0}}$		average power
Р		total instantaneous power
P <sub>c</sub>		instantaneous channel power
$P_{c0}$		static power

SYME	BOLS	NAMES
P <sub>c1,dist</sub>	s	first order dissipative channel power
P <sub>c1,con</sub>		first order conserved channel power
P <sub>g1,cor</sub>	1.5	first order gate power
$C_L$		externally load capacitor
$C_{gb}$		gate to bulk capacitance
$C_{gs}$		gate to source capacitance
$C_{gd}$		gate to drain capacitance
C <sub>sb</sub>		source to bulk capacitance
C <sub>sg</sub>		source to gate capacitance
C <sub>sd</sub>		source to drain capacitance
$C_{db}$		drain to bulk capacitance
$C_{dg}$		drain to gate capacitance
$C_{ds}$		drain to drain capacitance
C <sub>csb</sub>		conserved source to bulk capacitance
C <sub>csg</sub>		conserved source to gate capacitance
C <sub>csd</sub>		conserved source to drain capacitance
C <sub>cdb</sub>		conserved drain to bulk capacitance
C <sub>cdg</sub>		conserved drain to gate capacitance
C <sub>cds</sub>		conserved drain to drain capacitance
C <sub>dsb</sub>		dissipative source to bulk capacitance

# SYMBOLS NAMES

$C_{dsg}$		dissipative source to gate capacitance
$C_{dsd}$		dissipative source to drain capacitance
C <sub>ddb</sub>		dissipative drain to bulk capacitance
$C_{ddg}$		dissipative drain to gate capacitance
$C_{dds}$		dissipative drain to drain capacitance
P <sub>c1, dis</sub>	s, B	BSIM first order dissipative channel power
P <sub>c1, con</sub>	ns, B	. BSIM first order conserved channel power
P g1,com	ns, B	. BSIM first order gate power
P g1,con	$s\Big _{Extra}$	. extra first order channel conserved power
P <sub>c1,diss</sub>	Extra	extra first order channel dissipative power
$P_{1,cons}$	Extra	extra first order conserved power

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## **CHAPTER I**

## **I. INTRODUCTION**

#### 1.1 MODELING PROCESS

Modeling is a process of accurately representing the behavior of a device to be used in a circuit simulator. Designers need these reliable and accurate models for circuit development. With the growth of CMOS technology, MOSFET modeling has taken a centre stage and the accurate modeling of MOS transistor channel capacitance has been an ongoing effort. First, Meyer's [1.1] reciprocal gate-capacitive model, then Ward's [1.2] charge-based, non-reciprocal capacitance model have been used. Many papers have also been written on the comparison of these models. Some [1.3-1.6] claim that Meyer's model fails due to charge non-conservation which justifies the usage of charge-based models while others claim [1.7-1.9] that the charge non-conservation is mainly due to the faulty mathematical modeling of the simulation software. As pointed out by Fossum [1.10], it is not clear whether we have explored all other possibilities. We may be able to achieve a better result with a different channel partition or may be with no partition at all. Recent papers on field-dependent mobility [1.33] and laterally asymmetrical doping [1.34] have now shown inconsistencies in Ward's model, which artificially partitions the channel charge into the source and the drain components. Many ideas have also been suggested for estimation of energy and power taking into consideration the input slew dependency [1.11], propagation delay [1.12], short circuit power [1.13] and supply current measurements [1.14-1.16].

One of the most popular and widely adapted, <u>Berkeley Short-Channel I</u>GFET (BSIM) Capacitive <u>Model</u> [1.17, 1.18] has tried to include many of the above mentioned modeling techniques to estimate the behavior of Insulated Gate Field Effect Transistors (IGFET). However, the BSIM

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capacitive model fails to include the first order trans-capacitive currents due to the charge redistribution in the channel that causes the actual output waveform and the delay to deviate from the BSIM stimulation results [1.19]. In reality, the MOS device is a highly nonlinear four terminal device and modeling it as a simple energy storage device leaves a lot to be desired. When the inversion layer is formed, the I-R drop from the resistive components and charge redistribution current causes power dissipation in the channel. This makes the assumption that the capacitive model does not contribute any net power dissipation in the channel inconsistent for use in energy prediction.

If the BSIM model is not consistent, one may ask as why it is still being used? The reason is: the BSIM quasi-static models are analog friendly, continuous and have good I-V characteristic. These I-V models are derived from the channel charge that is calculated correctly to the first order. Power is also derived from the channel charge. The problem, however, is that the power is derived only to zero order. In other words, the BSIM capacitive model calculates static power dissipation, which is nothing but the multiplication of zero order current and steady state voltage. Though the BSIM capacitive model includes first order corrections in dynamic power calculation, it leaves out some important terms. We can think the process of dynamic power calculation of the BSIM model as being nothing but an easy way of calculating the zero order power by using the change in the energy of the capacitors during charging and discharging. The BSIM capacitive model assumes that the first order terms are the energy storage terms (like capacitors and inductors) that do not dissipate energy, which in reality is not the case. Hence it is not appropriate to look at the change in the energy of the capacitors in the channel as there is no energy function for the channel. It causes an error and gives a different number for power from the supply power than the dissipated power from all the devices, clearly a violation of energy conservation principles. This effect is pointed out in Fig. 1.1 which is a plot of switching frequency and the energy imbalance for different width ratios of transistors in a inverter. As seen, for higher switching frequencies (small rise/fall times) the energy imbalance is more pronounced.

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In reality, it is very difficult to estimate the usefulness of SPICE simulation in the power estimation of a real circuit. In digital applications, it is well known that the glitches can contribute half the power, and how accurately we can predict the power spike depends on how accurately we can predict the glitches. Therefore, it did not make a whole lot of difference, as SPICE was not predicting the power accurately anyway. Even if it were able to predict the power, it is not possible to extrapolate to a real circuit with glitches that are not exactly the same as SPICE calculated. However, in the world of Pentiums [1.20], Core Duos [1.21] and Quanti-Speed Architecture processors [1.22], where the gates are switching around 300 billion times a second [1.23], it becomes essential to calculate the higher order transients to accurately predict the device power and switching dynamics.

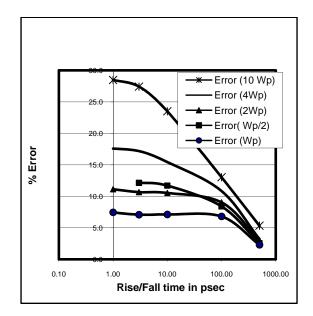


Figure 1.1: Energy Imbalance

It should also be pointed out that scholars working in the MOS device-modeling are aware of the transport current components flowing in the channel. Many papers [1.24 -1.27] and chapters [1.28-1.30] have been written about the charging and transport current components. However, all of them assume that it is not possible to separate the dissipative and energy storage components and have come up with many theories and models to envision the transient effects. One of the models by Lim-Fossum [1.31, 1.32] has the first order transient trans-capacitive current and

suggests the difference between non-reciprocal capacitive elements to be responsible for these transport currents. This however has some drawbacks. First, if these were the total trans-capacitive currents, its product with the drain to source voltage should have been the total dissipative power, which is not the case. Second, Lim-Fossum used Ward's charge partition model to find the source and drain charge components, which makes their model dependent on the accuracy of the charge partition.

#### 1.2 SCOPE

The object of the research is to realize the inconsistency in the current MOSFET modeling and develop efficient models for accurate intrinsic capacitance and power dissipation estimation. An ideal model would be to consider all non linear effects and solve a complete non-linear differential equation for the channel in three dimensions. In that case, we see a packet of charge traveling down the channel as a function of time. Although such models are valuable, from the simulation perspective, the process is ineffective as the simulation times are very long. To be computationally efficient, we need compact models that describe the electrical behavior analytically and are able to represent the non-linear channel in a reasonable time without sacrificing modeling accuracy. Furthermore, the fast scaling of frequency for semiconductor integrated circuits that was seen in the last few decades has been saturating. One of the reasons is the increase in power dissipation. Power limits the scaling. The high power dissipation due to small device geometry has thrown off course the roadmap of future development of semiconductor technologies. When the devices are switching rapidly, the power dissipation per unit area goes up causing excessive heating. Unless a sophisticated cooling system is implemented, the device may no longer be operational. The reality is: we have reached a power limited scaling regime. Scaling now is no longer determined by the device size, but by how much power the chip can dissipate at a particular working frequency. However, the lack of suitable device models to measure this power dissipation has provided a plethora of research avenues. The conventional MOSFET models have some inherent issues and are not consistent for power and energy prediction as they:

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- Fail to include the first order power dissipation due to channel charge redistribution
- Give a net non-zero power in the channel that has no physical basis from the terms that should be conserved

This makes the MOSFET modeling very important going forward into the nanometer regime. Given that the accuracy of the simulation depends on the physical representation of the device, it is very important that we have a reliable mathematical model that is able to represent the device behavior. Designers need these accurate models for circuit development.

#### 1.3 OUTLINE

The outline of the dissertation is as follows:

Chapter 2 describes the conventional MOSFET models used in transient analysis and computer simulation. The analysis of these models gives a general overview and a good background on device modeling. Some of these models are still being used for device simulation. The Meyer's model, Ward's charge partition model, Mehmet model and Trans-capacitance models and its effectiveness are considered. Some of the advantages and the shortcomings are also discussed.

Chapter 3 describes a one dimensional MOSFET current model with current continuity equations. These equations have been used to compute the channel currents and channel charges as well as currents at the source and the drain terminals for a charge conserving, quasi-static, channel capacitance model. The calculation of channel currents without charge partition allows the computation of the instantaneous channel power, which further helps in separating the dissipating and energy conserving current components.

Chapter 4 describes the details of power estimation. Zero and the first order instantaneous power is computed by integrating the power density over the entire channel. This leads to the derivation of closed-form analytical expressions for the conserved and dissipative current components from the first order drain and source currents. The energy function calculations from the first order conserved power components are also shown.

Chapter 5 describes the derivation of capacitances from the first order drain ( $i_{d1}$ ) and source ( $i_{s1}$ ) current components. These capacitances are then separated into conserved and dissipative components. An improved equivalent circuit is also developed by following the method used by Lim-Fossum.

The results are verified using the BSIM Capacitive and Lim-Fossum fully depleted SOI models for currents and charges in chapter 6. Even though these models used a charge partition instead of solving exactly as we have, all models predict the same source and drain currents, and hence the same terminal capacitances. However, we are able to separate out these capacitances into conserved and dissipative components.

Chapter 7 describes the inconsistencies of the BSIM capacitive model for energy and power prediction. We have shown that the dependence of the BSIM bulk charge parameter on the source potential causes extra power dissipation in the channel that has no physical basis. This leads to an inconsistent power model where energy supplied from the gate does not balance out with the energy generated at the channel.

### **CHAPTER II**

### **II. LITERATURE REVIEW**

This chapter describes some of the MOS models that have been used in circuit simulators to analyze the transient response. Historically, MOS devices have been modeled with capacitor and over the last few decades, many such capacitive models have been proposed to effectively represent the charges at the four terminals of a FET device. The problem however is the difficulty in representing the terminal charges by a single model. This is because; MOS transistors not only conduct current in a steady state but also conduct when the terminal voltages are varying. The time dependence of currents and voltages of a MOSFET makes representation using steady state (DC) conditions insufficient. A solution is possible by superimposing zero order steady state DC (I-V) representation over a capacitance (C-V) model to characterize the transients as

$$I(t) = I_{c0}(v) + i_{c1}(v, \frac{dv}{dt})$$

where  $I_{c0}(v)$  is the steady state (DC) current and depends only on the instantaneous terminal voltages.  $i_{c1}(t)$  is the transient transport component and is zero under steady state conditions. For simulation purposes, the capacitance (C-V) model is developed by expanding the transient current as

$$i_{c1}(t) = \frac{dq}{dt} = c\frac{dv}{dt}$$

In the subsequent sections, some of these models have been discussed in chronological order of the history of device modeling.

#### 2.1 MEYER'S MODEL

In 1971, Meyer [2.1] proposed the first large signal model for MOS transistors in terms of physical device parameters.

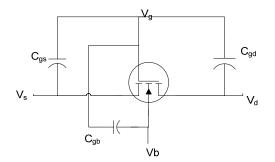


Figure 2.1: Meyer Capacitance Model

The model represents the charge storing property of MOS transistors using three nonlinear voltage dependent capacitors, as shown in Fig. [2.1]. These capacitors are defined in terms of the total gate charge  $Q_g$ . Meyer's model is a simple charge conservation model as it restricts the sum of the gate charge  $Q_g$  and channel charges  $Q_c$  o be zero, and is based on the following five assumptions.

- The total gate charge Q<sub>g</sub> is a function of the terminal voltage under steady state conditions.
- The gate capacitances are found as:

$$C_{gs} = \frac{\partial Q_g}{\partial v_{gs}} \qquad C_{gd} = \frac{\partial Q_g}{\partial v_{gd}} \qquad C_{gb} = \frac{\partial Q_g}{\partial v_{gb}}$$
(2.1)  
$$C_{gg} = C_{gs} + C_{gd} + C_{gb}$$

Where  $v_{gs}$ ,  $v_{gd}$  and  $v_{gb}$  are the gate to source, gate to drain and gate to bulk voltages.

• The drain to bulk, source to bulk and drain to source capacitances are assumed to be zero.

$$C_{ds} = C_{db} = C_{sb} = 0$$
$$C_{sd} = C_{bd} = C_{bs} = 0$$

 It is assumed that the capacitance matrix is symmetrical, which is necessary to conserve energy.

$$C_{gd} = C_{dg}$$
  $C_{gs} = C_{sg}$   $C_{gb} = C_{bg}$ 

• The total source, drain and bulk capacitances are calculated as:

$$C_{dd} = C_{ds} + C_{dg} + C_{db}$$
$$C_{ss} = C_{sg} + C_{sd} + C_{sb}$$
$$C_{bb} = C_{bs} + C_{bd} + C_{bg}$$

These five assumptions give the capacitance matrix as shown below;

$$\begin{bmatrix} C_{gd} + C_{gs} + C_{gb} & -C_{gd} & -C_{gs} & -C_{gb} \\ -C_{gd} & C_{gd} & 0 & 0 \\ -C_{gs} & 0 & C_{gs} & 0 \\ -C_{gb} & 0 & 0 & C_{gb} \end{bmatrix}$$

To calculate the total gate charge (  $\mathcal{Q}_{g}$  ), a gradual channel approximation is used. The charge

per unit area at any position x along the channel is given in by

$$Q(x) = C_{ox}(V_{gb} - V_t - V(x))$$

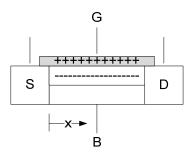


Figure 2.2: Channel Current Calculation

where  $V_{gb}$  is the gate voltage,  $V_t$  is the threshold voltage, V(x) is the potential at position x along the channel, and  $C_{ox}$  is the gate oxide capacitance per unit area. The steady state drain current  $I_{c0}$  is found using

$$I_{c0} = WQ(x)\mu \frac{dV(x)}{dx}$$

where W is the channel width and  $\mu$  is the mobility. Integrating from source (x=0) to drain (x=L);

$$I_{c0} = \mu C_{ox} \frac{W}{2L} (V_{gs}^2 - V_{gd}^2)$$
(2.2)

where *L* is the channel length. Gate charge is given by

$$Q_{g} = \frac{2}{3} WLC_{ox} \left[ \frac{(V_{gd} - V_{t})^{3}}{(V_{gd} - V_{t})^{2} - (V_{gs} - V_{t})^{2}} - \frac{(V_{gs} - V_{t})^{3}}{(V_{gd} - V_{t})^{2} - (V_{gs} - V_{t})^{2}} \right]$$
(2.3)

Using (2.1) and (2.2), capacitances are calculated as

$$C_{gs} = \frac{2}{3} WLC_{ox} \left[ 1 - \frac{(V_{gd} - V_t)^2}{(V_{gs} - V_t + V_{gd} - V_t)^2} \right]$$
(2.4)

$$C_{gd} = \frac{2}{3} WLC_{ox} \left[ 1 - \frac{(V_{gs} - V_t)^2}{(V_{gs} - V_t + V_{gd} - V_t)^2} \right]$$
(2.5)  
$$C_{gb} = 0$$

Finally, current through each capacitor is computed as

$$I_{gs} = C_{gs} \frac{dV}{dt} \qquad I_{gd} = C_{gd} \frac{dV_{gd}}{dt} \qquad I_{gb} = C_{gb} \frac{dV_{gb}}{dt}$$

Fig. 2.4 shows the current representation of Meyer's model. Currents I1 and I2 in the channel are assumed to be bidirectional, one being dependent on gate-to-source and other being dependent on gate-to-drain. This is also known as "Two-current-source MOS model".

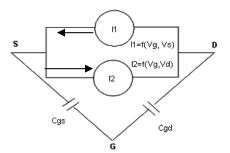


Figure 2.3: Current Representation in Meyer's model

The major drawback of Meyer's model is the exclusion of the source to bulk and drain to bulk capacitances resulting from substrate charges.

#### 2.2 CHARGE BASED MODELS

Ward [2.2-2.4] claimed that Meyer's model failed the charge conservation test for circuits that required charge storage. They identified the presence of nonlinear reciprocal capacitances and exclusion of the source to bulk and drain to bulk capacitances as being the source of charge non-conservation in the circuit simulation. They based their findings using current equation

$$i(t) = C(v) \frac{dV}{dt}$$
(2.6)

Here the capacitance term is dependent on the terminal voltages of the source, drain and the gate and has been evaluated at some appropriate voltage i.e. C(v) is not defined as a time dependent variable and can follow any path and as a result may lead to some arbitrary charge value. The best possible solution with average value of capacitor taken at two time intervals may also lead to an incomplete charge prediction. Integrating from the present time point  $t_0$  to the next time point  $t_1$  equation (2.6) can be written as

$$\int_{t_0}^{t_1} i(t)dt = \int_{v(t_0)}^{v(t_1)} C(v)dv$$
(2.7)

If C(v) is considered a constant, equation (2.7) reduces to

$$\int_{t_0}^{t_1} i(t)dt = C(v)[V(t_1) - V(t_0)]$$
(2.8)

The capacitance value for C(v) that's been used here is computed at time  $t_0$ . Ward assumes this being the reason for charge pumping, as there may be some residual charge at time  $t_0$ . He suggests that even if the capacitive values are calculated at time  $t_1$  or smaller time steps, it will not guarantee charge conservation. To overcome the assumed charge neutrality limitations, he suggested the charge-partition model [2.2].

The charge-partition model is based on the fixed charge distribution in the MOSFET terminals. The model tries to split the total channel charge  $Q_c$  into source ( $Q_s$ ) and drain ( $Q_d$ ) charges rather than splitting the total distributed capacitance into reciprocal gate-to-source and gate-to-drain capacitances. The current is then computed as the derivative of charge as

$$i(t) = \frac{dQ(t)}{dt}$$

Using similar integration approach as equation (2.7)

$$\int_{t_0}^{t_1} i(t)dt = Q(t_1) - Q(t_0)$$
(2.9)

Though  $Q(t_0)$  and  $Q(t_1)$  are complex functions of time, it can be obtained at any time by terminal voltage at that instant.

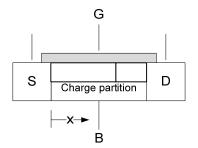


Figure 2.4: Channel Charge Approximation using Ward's model

The emphasis of the charge model was the use of charge as a state variable for the computation of charge at the MOSFET terminals. Ward was also able to put in perspective a current continuity

equation 
$$\frac{\partial I(y,t)}{\partial y} = -W \frac{\partial Q(y,t)}{\partial t}$$
 with the boundary conditions on  $V(y)$  as  $V(0) = V_s$  and  $V(L) = V_d$ 

to calculate the source and drain charges together with the source and drain currents, and the transport current. Using the current continuity equation, the current at any point y on the channel is evaluated as

$$I(y,t) - I_{s}(t) = -W \int_{0}^{y} \frac{\partial Q(y,t)}{\partial t} dy$$
(2.10)

where  $I_s(t) = I(0,t)$  is the source current, and L is the length of the channel. Considering only drift current for I(y,t) and solving for  $I_s(t)$ , equation (2.10) reduces to two current components

$$I(y,t) = -\mu WQ(y,t) \frac{\partial V(y,t)}{\partial y} \text{ and}$$
(2.11)

$$I_{s}(t) = -\frac{W}{L} \int_{0}^{L} \mu(y,t)Q(y,t)\frac{\partial V(y,t)}{\partial y}dy + \frac{d}{dt} \left[ W \int_{0}^{L} (1-\frac{y}{L})Q(y,t)dy \right]$$
(2.12)

Substituting y=L to obtain the drain current

$$I_{d}(t) = -\frac{W}{L} \int_{0}^{L} \mu(y,t)Q(y,t)\frac{\partial V(y,t)}{\partial y}dy + \frac{d}{dt} \left[ W \int_{0}^{L} (\frac{y}{L})Q(y,t)dy \right]$$
(2.13)

Since the drain and source current can be assumed to have transport and charge components, they can be represent using

$$I_{s}(t) = -I_{T}(t) + \frac{dQ_{s}(t)}{dt}$$
(2.14)

$$I_{d}(t) = I_{T}(t) + \frac{dQ_{d}(t)}{dt}$$
(2.15)

From equations (2.13) (2.14) and (2.15),

$$Q_s = W \int_0^L (1 - \frac{y}{L})Qdy$$
(2.16)

$$Q_d = W \int_0^L (\frac{y}{L}) Q dy$$
(2.17)

Many modifications have been made since Ward proposed the original charge model in 1981. Almost all these models consider "charge" as a state variable and use non-reciprocal capacitors. Some models have partitioned the channel charge into drain and source components in the ratio of 40/60 while others use a 50/50 model. However, none of these models addresses the actual cause of charge non-conservation. Yang, Berton and Chatterjee [2.5], while investigating the charge conservation problem, observed that the non-conservation of charge in circuit simulator SPICE is due to the integration problem independent of device physics. They think the error is due to the choice of voltage as a state variable for simulation, and also due to the nonlinearities in the MOS capacitances and its dependence on four different terminal voltages.

Sakallah, Yen and Greenberg [2.6] also support the view that the charge non-conservation in the Meyer capacitance model has nothing to do with the device physics or a faulty capacitive model, *"rather by the mathematical error of characterizing a multidimensional function by an incomplete subset of its partial derivatives."* They conclude that the charge non-conservation can be eliminated if circuit simulators are given non trivial models. They also followed modeling using Ward's approach and proceeded by splitting total channel charge into source and drain instead of splitting total distributed capacitance between the gate and the channel into reciprocal gate-to-source and gate-to-drain capacitances. As mentioned earlier, the charge splitting techniques have been revised many a time, and have been classified into two groups with respect to the bulk charges included in the model [2.7] for efficient MOSFET modeling. They are

I. Depletion Charge Model (DSM)

II. Simplified Charge Model (SCM)

In DCM, bulk charge is considered to be proportional to the square root of a voltage, while SCM is a more simplified DCM model, with slight compromise in bulk to drain and bulk to source capacitances.

Although charge-based models provided an alternate way to model MOSFET's, it was still not able to explain the charge non-conservation of the Meyer capacitance model. Roots and Hughes [2.8] in 1988 and Snider [2.9] in 1995 suggested a trans-capacitance model, which came close in identifying the conservation problem.

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#### 2.3 TRANS-CAPACITIVE MODEL

Roots and Hughes [2.8] in 1988 and later Snider [2.9] was able to explain the charge nonconservation of the Meyer capacitance model using the concept of trans-capacitance. According to them, a capacitive gate to source MOS elements that depends on both gate to source and gate to drain voltages would transport a non-zero charge. They predicted the violation of charge conservation due to the omission of recharging effect of capacitances and tried to compensate the charge by adding an extra element in the circuit and called it a trans-capacitance element. Their model concluded that:

1. Current equation  $I = C \frac{dV}{dt}$  alone does not account for all the currents in MOS transistors

as capacitances are controlled by more than one source.

2. These capacitances appear to dissipate energy if trans-capacitance terms are ignored.

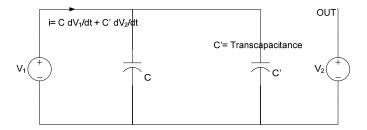


Figure 2.5: Trans-capacitance Approximation

#### 2.4 MEHMET MODEL

In 1989, Mehmet A. Cirit [2.10] was able to show the root cause of charge non-conservation in the gate-capacitance model proposed by Meyer. He points out that the "*Meyer model is a first-order inaccurate approximation to MOS capacitances.*" Since the MOS capacitance is dependent on several variables, faults in the modeling of such an element causes the SPICE simulator to neglect non-linear first order capacitive terms.

Considering the gate to source transient current equation

 $i_{gs} = C_{gs} \,\partial_t v_{gs}$ 

its partial derivative gives

$$i_{gs} = C_{gs} \delta^V_{gs} + \delta C_{gs} \delta^V_{gs} .$$
(2.20)

Since gate capacitance is dependent on gate to source, gate to drain and gate to bulk voltages, including these effects, equation (2.20) can be modified as

$$\delta i_{gs} = C_{gs} \delta^V_{gs} + V_{gs} \frac{\delta C_{gs}}{\delta V_{gs}} \delta V_{gs} + V_{gs} \frac{\delta C_{gs}}{\delta V_{gd}} \delta V_{gd} + V_{gs} \frac{\delta C_{gs}}{\delta V_{gb}} \delta V_{gb}$$
(2.21)

If  $\alpha$  is 1/h, where h is the time interval, and voltage varies by an amount  $\delta V$ , the corresponding change in its time derivative  $\overset{\bullet}{V}$  can be estimated as  $\delta \overset{\bullet}{V} = \alpha \delta V$ . Substituting these values in equation (2.21), equation (2.21) can be rewritten as

$$\delta i_{gs} = C_{gs} \alpha \delta V + V_{gs} \frac{\delta C}{\delta V_{gs}} \delta V_{gs} + V_{gs} \frac{\delta C}{\delta V_{gd}} \delta V_{gd} + V_{gs} \frac{\delta C}{\delta V_{gb}} \delta V_{gb}$$
(2.22)

Similarly, gate to drain and gate to substrate current can be written as

$$\delta i_{gd} = C_{gd} \alpha \delta V + V_{gd} \frac{\delta C_{gd}}{\delta V_{gs}} \delta V_{gs} + V_{gd} \frac{\delta C_{gd}}{\delta V_{gd}} \delta V_{gd} + V_{gd} \frac{\delta C_{gd}}{\delta V_{gb}} \delta V_{gb}$$
(2.23)

$$\delta i_{gb} = C_{gb} \alpha \delta V + V_{gb} \frac{\delta C_{gb}}{\delta V_{gs}} \delta V_{gs} + V_{gb} \frac{\delta C_{gb}}{\delta V_{gd}} \delta V_{gd} + V_{gb} \frac{\delta C_{gb}}{\delta V_{gb}} \delta V_{gb}$$
(2.24)

The first term in (2.22-2.24) is frequency dependent, while rests of the terms are due to non-linear capacitances and look like resistors in the channel. As circuit simulators only considered the frequency dependent terms for circuit evaluation, Mehmet assumed that this incomplete representation was the root cause of charge pumping in circuit simulators, and proposed a model to include ignored non-linear terms that caused an extra charge in the channel.

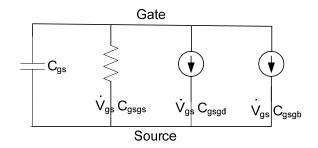


Figure 2.6: Small Signal Representation of Mehmet Model

Fig. 7 shows a small signal representation of Mehmet model for  $C_{gs}$  where

$$C_{gsgs} = \frac{\delta C_{gs}}{\delta V_{gs}} \qquad C_{gsgd} = \frac{\delta C_{gs}}{\delta V_{gd}} \qquad C_{gsgb} = \frac{\delta C_{gs}}{\delta V_{gb}}$$
(2.25)

$$C_{gdgs} = \frac{\delta C_{gd}}{\delta V_{gs}} \qquad C_{gdgd} = \frac{\delta C_{gd}}{\delta V_{gd}} \qquad C_{gdgb} = \frac{\delta C_{gd}}{\delta V_{gb}}$$
(2.26)

$$C_{gbgs} = \frac{\delta C_{gb}}{\delta V_{gs}} \qquad C_{gbgd} = \frac{\delta C_{gb}}{\delta V_{gd}} \qquad C_{gbgb} = \frac{\delta C_{gb}}{\delta V_{gb}}$$
(2.27)

Mehmet used this model in the circuit simulator Lspice and observed the charge conservation. He concluded that the Meyer gate capacitance model can be made to conserve charge by considering all first order terms. He also pointed out that the substrate charges might be easily included in the Meyer capacitance model to simulate the MOS devices more accurately.

It should be noted that in any MOSFET model, charge or capacitance, the charge neutrality condition is built into the derivation [2.11] and may seem unreasonable to come up with a charge non-conservation problem. Whichever modeling techniques are used, the main goal is to come up with an analytical description of MOS device behavior with emphasis on equations that are continuous in all regions of device operation.

### **CHAPTER III**

### **III. FIRST ORDER QUASI-STATIC CHANNEL CAPACITANCE MODEL**

This chapter describes the mathematical equations used to analyze the MOS transistor for the research work. The current continuity equations are presented without the channel charge partition to compute the steady state and dynamic current components. These currents then become the basis for I-V and C-V models to be used in the circuit simulators.

#### 3.1 STEADY STATE OPERATION

In the steady state, the gate and substrate are assumed to have no direct conductive path to the channel. Leakage through the gate oxide as well as recombination current between the substrate and the channel are neglected.

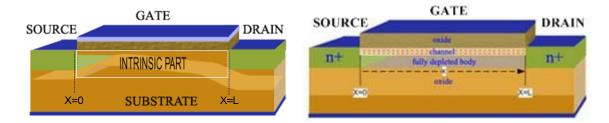


Figure 3.1: BULK and SOI CMOS Structures

It is very important that the body charges are properly modeled [3.1, 3.2, 3.3] and its effects are included for steady state and the transient simulations. These effects cause an uneven distribution of channel charge between the source and the drain regions, and the regions in between, which in turn causes uneven distribution of the gate and substrate charges. To model all these skewed distributions, it will be convenient to describe the charges by its density per unit length. Considering only the intrinsic part of the MOS transistor, which is responsible for all the transistor action, the zero order charge per unit length at the terminals can be written as

$$q_{jb0} = f(v_{gb}, v_{cb}) \text{ where } j = g, c$$
 (3.1)

In terms of drift current, current flow in the device can be seen due to the transport of electrons from the source to the drain terminal. Taking steady state values,

$$I_{c0} = I_D \tag{3.2}$$

$$I_S = -I_D \tag{3.3}$$

$$I_G = 0 \tag{3.4}$$

$$I_B = 0$$
 (3.5)

where  $I_{c0}$  is the steady state channel current, which becomes  $I_D$  at the drain end and  $-I_S$  at the source end. The steady state gate  $I_G$  and substrate currents  $I_B$  are zero as the transistors are assumed to be leakage free. These terminal currents can be expressed as some function of terminal voltages and can be written as

$$I_{c0} = f(v_D, v_G, v_S, v_B)$$
(3.6)

#### 3.2 QUASI-STATIC OPERATION

Equation (3.4) was calculated with the assumption that the terminal voltages were steady. In a real circuit, transistors operate under dynamic conditions where terminal voltages are varying. To calculate the charge under such conditions, quasi-static operations are assumed. The voltages are allowed to vary slowly in quasi-static operation. Though the gate, substrate and the channel charges are still the functions of instantaneous voltages and can be represented using equation (3.1), however, the currents can not be predicted using equation (3.6). With similar assumption of leakage free gate oxide and negligible recombination current, the first order gate ( $i_{g1}$ ) and substrate ( $i_{b1}$ ) currents are no longer zero. They are given at any location x along the channel by the gate ( $q_q$ ) and bulk ( $q_b$ ) charge densities as:

$$i_g(x,t) = \frac{d}{dt}q_g(x,t)$$
(3.7)

$$i_b(x,t) = \frac{d}{dt}q_b(x,t)$$
(3.8)

In the quasi-static operation, even though the charge distribution in the channel remains the same, there exists a conducting path between the source and the drain terminals. Charge enters from the source terminal and leaves the drain terminal, which makes channel partition schemes misleading to understand the device physics. It is also challenging to represent the channel charge and compute the first order source ( $i_{s1}$ ) and drain ( $i_{d1}$ ) terminal currents due to two reasons:

- It is unrealistic to consider the charges in the channel as being partitioned between source and drain and
- Charge redistribution causes extra dissipation in the channel.

The unrealistic partition can be resolved by solving for the total charge in the channel instead of separating it into source and drain charges.

Fig. 3.2 shows a voltage, charge magnitude and current waveforms. The current waveforms show a pair of first order components together with a steady state DC component. The origin of these first order components not predicted by DC operation can be explained using a test quasi-static voltage at the gate terminal.

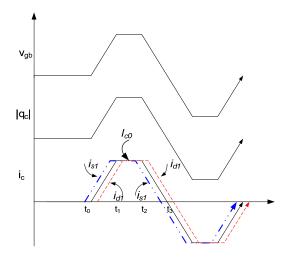


Figure 3.2: Voltage, Charge and Current Waveforms

A rising input at the gate terminal from time  $t_0$  to  $t_1$  causes the first order currents. Compared to first order drain current ( $i_{d1}$ ), first order source current ( $i_{s1}$ ) is more in this interval as more electrons are pumped from the source terminal and fewer electrons are removed from the drain. Between the intervals  $t_1$  to  $t_2$ , current settles into a steady state value of  $I_{c0}$ . On the other hand, for a falling waveform between the interval  $t_2$  to  $t_3$ , first order drain current becomes more than the first order source current as more electrons are sucked out from the drain terminal. These transients that show up during the switching are also responsible for the channel charge redistribution, which in turn also contributes to power dissipation. To properly analyze the MOS transistors and develop C-V models to be used in circuit simulators, we then need to consider these first order currents together with the steady state values. As mentioned above, the charge redistribution also contributes to the power dissipation, which suggests the presence of first order dissipative and conserved components. We have been able to identify and separate out these components. This is explained in detail in chapter 4 with derivations.

#### 3.3 MODELING EQUATIONS

In order to obtain an analytical solution, the current flow is considered in one dimension parallel to the surface of the device. The equations for both Bulk and SOI processes are developed with some assumptions. The body charge is assumed to have square root dependence for the Bulk process, while the charge expressions for SOI MOSFET assumes that the region under the channel is completely depleted of mobile charges. These simplified assumptions helps us to make use of a linear relationship between the body and the surface potential to compute the energy function without partitioning the channel charge. The linear body-surface relation also provides a simplified charge model and terminal currents. It should be noted that solving the model involves complicated algebraic calculations that are practically impossible without modern mathematics tools like "Mathematica" [3.4].

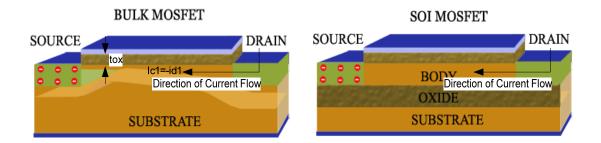


Figure 3.3: Four terminal (a) BULK NMOSFET and (b) SOI NMOSFET Structure

Fig. 3.3 shows NMOS BULK and SOI transistors. The charge per unit length  $(q_c)$  at a position x along the channel is given by

$$q_{c}(x) = -c_{ox}(v_{gb} - v_{fb} - v_{cb}(x) - \phi + q_{b}(x)/c_{ox})$$
(3.9)

Similarly, the bulk charge (back gate) per unit length (  $q_b$  ) at x can be written as

$$q_{b}(x) = \begin{cases} -c_{ox}(k_{1} + k_{2}v_{cb}(x)), & SOI \\ -c_{ox}(k_{1}\sqrt{\phi + v_{sb}} + (Abulk - 1)(v_{cb}(x) - v_{sb})), & BULK \end{cases}$$
(3.10)

where  $v_{fb}$ ,  $v_{gb}$  and  $v_{cb}$  are flat band, gate and channel voltages with respect to the body. *Abulk* [3.13] is the bulk charge coefficient,  $k_1$  and  $k_2$  are body effect coefficients.  $c_{ox} = w (c_{ox}/A)$  is the oxide capacitance per unit length and w is the channel width. The bulk charge is approximated using first two terms of Taylor's expansion around the source terminal  $v_{sb}$ . The linear dependence of back gate for a fully depleted SOI MOSFET is included in the  $k_1$  term. Charge conservation is insured by defining the gate charge per unit length  $q_g$  as

$$q_g = -(q_b + q_c) \tag{3.11}$$

It will be convenient to define the channel charge per unit length at the source (*x*=0)  $q_s$  and the drain (*x*=*L*)  $q_d$  and their time derivatives as

$$q_s = -c_{ox} v_{gst} \text{ and}$$
(3.12)

$$\frac{d}{dt}q_s = -c_{ox}\frac{d}{dt}v_{gst}$$
(3.13)

where 
$$v_{gst} = v_{gb} - v_t - v_{sb}$$
 (3.14)

In equation (3.14),  $v_t$  is the threshold voltage. The body effect parameters are included by considering the dependence of source terminal on the threshold voltage [3.5, 3.6] by defining

$$v_t(v_{sb}) = \begin{cases} v_{t0} + k_2 v_{sb}, & SOI \\ v_{t0} + k_1 (\sqrt{\phi + v_{sb}} - \sqrt{\phi}), & BULK \end{cases}$$
(3.15)

where

$$v_{t0} = \begin{cases} v_{fb} + k_1 + \phi, & SOI \\ v_{fb} + k_1 \sqrt{\phi} + \phi, & BULK \end{cases}$$
(3.16)

At the drain end,

$$q_d = -c_{ox} v_{gdt} \quad \text{and} \tag{3.17}$$

$$\frac{d}{dt}q_d = -c_{ox}\frac{d}{dt}v_{gdt} \qquad \text{where} \tag{3.18}$$

$$v_{gdt}(x) = \begin{cases} v_{gb} - v_t - v_{sb} - (1 + k_2)(v_{db} - v_{sb}), & SOI \\ v_{gb} - v_t - v_{sb} - Abulk(v_{db} - v_{sb}), & BULK \end{cases}$$
(3.19)

It is assumed that positive current flows into the drain and velocity saturation effects are neglected. The derivative of *Abulk* with  $v_{sb}$  is assumed to be negligible. These assumptions are necessary for energy conservation [3.7] and simplified capacitance equations [3.8]. Even though the equations are simplified, accuracy is not significantly compromised [3.8]. The results are expected to be accurate for a substrate referenced system [3.9]. Drift current at a distance x along the channel can be written as

$$i_{c}(x,t) = q_{c}(x,t)\mu \frac{d}{dx}v_{cb}(x)$$
 (3.20)

Charge conservation is assured using the continuity equation

$$\frac{d}{dx}i_{c}(x,t) = -\frac{d}{dt}q_{c}(x,t)$$
(3.21)

where  $q_c = q_{c0} + q_{c1}$ 

In equation (3.21),  $q_{c0}$  is a function of terminal voltages and  $q_{c1}$  is a function of first order time derivatives of terminal voltages. Using (3.20) in (3.21) gives

$$\frac{d}{dx}[q_c(x,t)\mu\frac{d}{dx}v_{cb}(x)] = -\frac{d}{dt}q_c(x,t)$$
(3.22)

Taking the spatial derivatives of charge per unit length as a function of potential along the channel, equation (3.9) and (3.10) reduces to

$$\frac{d}{dx}q_c(x,t) = C_c \frac{d}{dx}v_{cb}(x); \quad C_c = c_{ox}K; \quad K = \begin{cases} (1+k_2), & SOI\\ Abulk, & BULK \end{cases}$$
(3.23)

Substituting  $\frac{d}{dx}v_{cb}(x)$  in (3.22) and rearranging terms gives

$$\frac{d}{dx}[q_c(x,t)\frac{d}{dx}q_c(x,t)] = -\frac{C_c}{\mu}\frac{d}{dt}q_c(x,t)$$
(3.24)

Equation (3.24) can be solved iteratively to compute the current and the charge in the channel. In terms of the steady state (zero order) charge per unit length at any position x along the channel, equation (3.24) reduces to

$$\frac{d}{dx}(q_{c0}\frac{d}{dx}q_{c0}) = 0$$
(3.25)

Performing integration from source(x=0) to drain (x=L), zero order charge along the channel becomes

$$q_{c0} = -\sqrt{(q_s^2(1-x/L) + q_d^2 x/L)}$$
(3.26)

and the steady state drift current component simplifies to

$$I_{0} = \frac{\mu}{C_{c}} q_{c0} \frac{d}{dx} q_{c0}$$
(3.27)

Equation (3.27) gives the usual equation for static current neglecting velocity saturation, which is shown in Table 1. The first order current and charge can be found by keeping terms of first order in time derivatives in equation (3.24)

$$\frac{d}{dx}(q_{c0}\frac{d}{dx}q_{c1} + q_{c1}\frac{d}{dx}q_{c0}) = -\frac{C_c}{\mu}\frac{d}{dt}q_{c0}$$
(3.28)

Rearranging the terms, equation for the first order channel charge simplifies to

$$q_{c1} = -\frac{C_c}{\mu} \frac{1}{q_{c0}} (\frac{d}{dt} \int (\int q_{c0}[x]dx)dx) + c1x + c0$$
(3.29)

and the first order channel current reduces to

$$i_{c1} = \frac{\mu}{C_c} (q_{c0} \frac{d}{dx} q_{c1} + q_{c1} \frac{d}{dx} q_{c0})$$
(3.30)

Finally, equation (3.30) can be solved to compute the first order channel current at the source  $i_{s1} = i_{c1}$  (*x*=0) and the drain  $i_{d1} = -i_{s1}$  (*x*=L) ends in all regions of operation. We have assumed pinch-off saturation which occurs when  $q_d = 0$ . The drain voltage at saturation can now be estimated by

setting 
$$v_{gdt}(x) = 0$$
 to get  $v_{ds} \ge \frac{v_{gst}}{K}$  as a boundary between the linear and the saturation regions.

In the cut-off, it is assumed that the channel current is zero, which is made possible by setting both the charge densities  $q_d$  and  $q_s$  to zero. Table 1 summarizes the charge and current in all regions of operations. These results obtained without partitioning the channel charge are in agreement with Lim-Fossum [3.10] and the BSIM capacitive model [3.11, 3.12] which were obtained using Ward's [3.2] partition. Therefore, we have verified that Ward's partition is correct when the voltage dependence of Abulk is ignored.

	Linear	Saturation	Cut-Off
Conditions	$q_{c}$	$q_{c}^{} < 0$	$q_{_{\mathcal{C}}} = 0$
	$v_{gdt} > 0$ $v_{gst} > 0$	$v_{gdt} = 0$	$v_{gdt} = 0$
	$v_{gst} > 0$	$v_{gst} > 0$	$v_{gst} = 0$
$q_{s}$	$-c_{ox}v_{gst}$	$-c_{ox}v_{gst}$	0
$q_d$	$-c_{ox}v_{gdt}$	0	0

 Table 3.1: NMOS Zero and First Order Charges and Currents

I <sub>c0</sub>	$\frac{\mu c_{ox}}{2L(1+k_2)} (v_{gst}^2 - v_{gdt}^2)$	$\frac{\mu c_{ox}}{2L(1+k_2)}v_{gst}^2$	0
i <sub>s1</sub>	$\frac{2c_{ox}L}{15(v_{gdt}+v_{gst})^3} [2v_{gdt}(\frac{d}{dt}v_{gdt})(v_{gdt}^2+3v_{gdt}v_{gst}+v_{gst}^2) + v_{gst}(\frac{d}{dt}v_{gst})(8v_{gdt}^2+9v_{gdt}v_{gst}+3v_{gst}^2)]$	$\frac{2}{5}c_{ox}L\frac{d}{dt}v_{gst}$	0
<sup>i</sup> d1	$\frac{2c_{ax}L}{15(v_{gdt}+v_{gst})^3} [v_{gdt}(\frac{d}{dt}v_{gdt})(3v_{gdt}^2+9v_{gdt}v_{gst}+8v_{gst}^2) + 2v_{gst}(\frac{d}{dt}v_{gst})(v_{gdt}^2+3v_{gdt}v_{gst}+v_{gst}^2)]$	$\frac{4}{15}c_{ox}L\frac{d}{dt}v_{gst}$	0

# **CHAPTER IV**

# **IV. MOSFET POWER**

This chapter discusses the origin of MOS transistor leakage and describes the power computation techniques for conserved and dissipative components without the channel charge partition. The existence of an energy function is also validated. The conserved and dissipative power components then become the basis of conserved and dissipative current components in chapter 5.

The fast scaling of operation frequency for semiconductor integrated circuits that was seen in the last few decades cannot continue. One of the reasons is the increase in power dissipation. Power limits the scaling. The high power dissipation due to small device geometry has thrown off course the roadmap of future development of semiconductor technologies as predicted in the International Technology Roadmap for Semiconductors [4.1].

When the devices are switching rapidly, the power dissipation per unit area goes up causing excessive heating. Unless a sophisticated and expensive cooling system is implemented, the device may no longer be operational. The reality is: we have reached a power limited scaling regime. Scaling now is no longer determined by the device size, but by how much power the chip can dissipate at a particular working frequency. However, the lack of suitable device models to measure this power dissipation has provided a plethora of research avenues. The conventional MOSFET models have some inherent issues and are not consistent for power and energy prediction as they:

• Fail to include the first order power dissipation due to channel charge redistribution,

 Give a net non-zero power in the channel that has no physical basis from the terms that should be conserved.

This makes the MOSFET modeling very important going forward into the nanometer regime for low power design techniques and power-aware architectures [4.3]. Given that the accuracy of the simulation depends on the physical representation of the device, it is very important that we have a reliable mathematical model that is able to represent the device behavior. Designers need these accurate models for circuit development.

#### 4.1 SOURCES OF POWER DISSIPATION

There are three sources of power dissipation in the MOS transistor [4.3-4.6]. The first source of power dissipation is due to the transistor switching that is related to the charging and discharging of the external load capacitors. The second source is from the short-circuit power due to the current flow from the supply to the ground. These two dissipations are related to the transitions at the gate [4.7]. The third source is the leakage power. Transistor scaling has reduced the threshold voltage and increased the gate leakage resulting in higher static power. Fig. 4.1 shows all these leakage sources that are taking up the power budget. Some of these sources have dominant effects on the transistor performance in the nano-meter regime [4.7, 4.8].

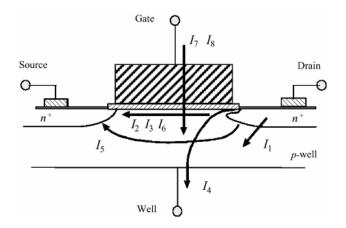


Figure 4.1: Leakage Current Components [4.5]

11	PN junctions reverse bias current
12	Subthreshold leakage
13	Drain Induced barrier lowering
14	Gate-Induced drain leakage
15	Punchthrough
16	Narrow width effect
17	Gate oxide tunneling
18	Hot carrier injection

#### 4.2 POWER AND ENERGY MODELING ISSUES

Meyer [4.9] was the first to present a capacitive model. Ward and Dutton [4.10] pointed out the assumed charge non conservation problems in Meyer's model. To solve these problems in transient simulation, they proposed a charge partitioning scheme with a charge conservation constraint. Sheu et al. [4.11] and Chung [4.12] made many improvements later to better derive I-V and C-V characteristics. One of the industry standards, the BSIM capacitive model includes many of these models to estimate the behavior of MOS transistors. The BSIM model assumes that the MOSFET capacitance is an energy storage device and uses the conserved charges (to first order) to predict the currents and voltages at different nodes. The same charge (to zero order) is also used to predict the channel power. This makes the BSIM capacitive a zero order, quasi-static power dissipation model. The model

- Assumes that the first order terms only contribute to energy storage
- Uses channel charge partition scheme and the bulk charge parameter has a non-linear dependence on the source potential.

Both these ideas leave a lot to be desired. First, the dissipative power has some higher order terms due to the charge redistribution. These higher order dissipative components become significant at higher frequencies and modify the total power dissipated in the channel [4.13]. This is explained later in section 4.5. Second, the non-linear dependence of *Abulk* on  $v_{sh}$  does not

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allow the derivation of energy function from all of the conserved components [Appendix A7.2]. These effects causes the BSIM capacitive model to predict a different number for instantaneous power measured from the supply than the power dissipated in the device, clearly a violation of energy conservation principles.

If an analytical closed form solution for the stored energy function is desired using non-reciprocal capacitors, the FET charge equation has to be solved for a linear source dependence of the bulk without the channel charge partition. These inconsistencies make the current BSIM capacitive model non-ideal for energy estimation.

#### 4.3 POWER MEASUREMENT TECHNIQUES

Many models have been suggested for the estimation of power, like using supply current measurements [4.14], input slew dependency [4.15], propagation delay [4.16], short circuit power [4.17] and non-conventional capacitor-based methods [4.18]

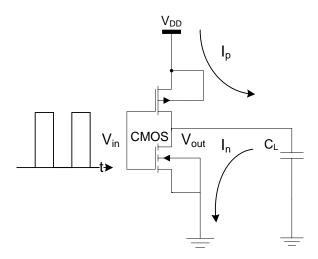


Figure 4.2: Dynamic Power

Fig 4.2 shows one of simplest techniques used to calculate the transistor power consumption. Power is consumed when the gate drives the output  $V_{out}$  to a new value. Assuming that the input  $V_{in}$  changes very fast, only one transistor turns on at a time. When the output goes high, the current flows through the PFET and goes only to the capacitor. The current component that goes down the NFET has been neglected. Similarly when the output settles to a low value, it is assumed that the current goes through the NFET. Though the PFET is not quite turned off yet, the current that is coming through the PFET is neglected.

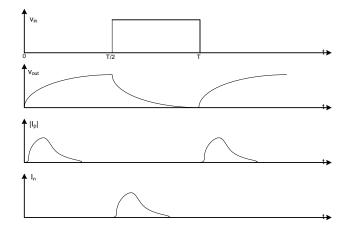


Figure 4.3: Transient Waveforms

Fig 4.3 shows the transient waveforms. The output looks more like a RC time constant due to the presence of the capacitance, charging up the output from 0 to T/2 and then discharging from T/2 to T. If we look at the corresponding current plots for falling input transient, it is only the PFET that is providing the capacitor current  $I_p$ . For the rising input transient, capacitor current  $I_n$  is through the NFET. It should be noted that the currents mentioned above are the magnitudes of the drain current. The instantaneous power dissipation is then calculated by solving for I and V and multiplying them together. It is also assumed that the capacitors are purely energy storage devices and does not contribute to net power dissipation. Hence, during the falling input transition, power dissipation is only in the PFET. Similarly during the rising input transition, power dissipation is only in the NFET.

Using these assumptions, the average power  $\overline{P_{c0}}$  for a complete cycle is computed using

$$\overline{P_{c0}} = \frac{1}{T} \begin{bmatrix} T/2 \\ \int U_p V_{DSp} dt + \int U_p V_{DSn} dt \end{bmatrix}$$
(4.1)

where  $V_{DSp}$  and  $V_{DSn}$  are the outputs at the PFET and NFET respectively. During the falling transition as PFET charges the capacitor, actual positive current flows from the device to the capacitor. This makes the PFET drain current  $I_p$  negative.

$$I_p = -(C_L \frac{dV_{out}}{dt})$$
(4.2)

where  $C_{L}$  is the output load. The corresponding output voltage at the PFET,  $V_{\rm DSp}$  becomes

$$V_{DSp} = V_{out} - V_{DD} = -(V_{DD} - V_{out})$$
(4.3)

where  $V_{DD}$  is the supply voltage. From (4.2) and (4.3), power dissipated in the PFET,  $P_{PFET}$  is computed using

$$P_{PFET} = \int_{0}^{T/2} I_p V_{DSp} dt$$
(4.4)

Similarly, the current through the NFET,  $I_n$  is negative of the capacitive current.

$$I_n = -(C_L \frac{dV_{out}}{dt})$$
(4.5)

and the corresponding output voltage,  $V_{\rm DSn}$  is

$$V_{DSn} = V_{out} \tag{4.6}$$

From (4.5) and (4.6), power dissipated in the NFET,  $P_{\rm NFET}$  is given by

$$P_{NFET} = \int_{T/2}^{T} I_n V_{DSn} dt$$
(4.7)

The average power,  $\overline{P_{c0}}$  for a complete cycle is estimated using equations (4.4) and (4.7) as

$$\overline{P_{c0}} = \frac{1}{T} [P_{PFET} + P_{NFET}]$$
(4.8)

Substituting  $I_n$ ,  $I_p$ ,  $V_{DSn}$  and  $V_{DSp}$  in equation (4.8), the average power equation reduces to

$$\overline{P_{c0}} = \frac{1}{T} \begin{bmatrix} T/2 \\ \int \\ 0 \end{bmatrix} C_L \frac{dV_{out}}{dt} (V_{DD} - V_{out}) dt + \int_{T/2}^{T} (-C_L \frac{dV_{out}}{dt}) V_{out} dt]$$
(4.9)

Because of the fact that the transistor currents are related to the charging and discharging of the currents of the capacitor, the power integrals can be replaced from integrals over dt to an integral over dv. This gives a closed form expression for the dynamic power independent of i(t) and v(t).

$$\overline{P_{c0}} = f C_L V_{DD}^2$$
(4.10)

There are, however, some issues in regards to the dynamic power equation (4.10). These issues are:

- The MOS channel is not purely an energy storage device and has no energy function.
   For an energy function to exist, second order partials have to be equal. This is shown in the Appendix [A4.5-A4.7].
- The MOS capacitors dissipate power and the trans-capacitive terms used in the charge model includes both dissipative and conserved components. Therefore, it is not appropriate to look at the change in the energy of the external load capacitor  $C_L$  in the channel as a true measure of power. Dynamic power predicted using equation (4.10) is in fact an easy way of computing the zero order power by looking at the change in energy during charging and discharging of external capacitors.

Fig. 4.4 shows another capacitor based technique used for power measurement. In this type of power measurement, switch S is closed and the load capacitor  $C_L$  is allowed to attain the supply voltage  $V_{DD}$ . The switch is then opened and the CMOS gate is allowed to undergo a transition. This causes some energy consumption in the circuit, which is captured by the measuring device as a decrease in supply voltage ( $\Delta v$ ). Energy dissipated in the circuit can now be estimated using

$$Energy = \frac{1}{2}C_L V_{DD}^2 - \frac{1}{2}C_L (V_{DD} - \Delta v)^2$$
(4.11)

where  $\frac{1}{2}C_L \Delta v^2$  is the energy consumed by the circuit. This method of energy prediction is very

accurate [4.18]. However, this energy prediction is not possible during the design phase. Hence,

there is a need for a verification tool that can simulate the real world behavior of the transistor during the design phase.

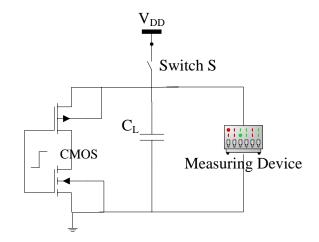


Figure 4.4: Capacitor based Power Measurement Technique

This makes the next and subsequent sections of power derivation one of the most important findings of our research, where the energy function is derived from a symmetrical charge conserving FET models. Before going through the derivation, it however, becomes important to discuss the extra source of transistor power dissipation that was not included in section 4.1. It also becomes important to check the validity of the quasi-static approximation in the model derivation.

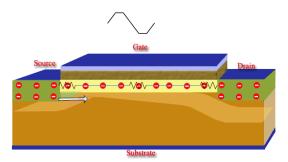


Figure 4.5: Power Dissipation in MOS Transistor

When the gate undergoes a transition, from  $v_{ss}$  to  $v_{dd}$  or  $v_{dd}$  to  $v_{ss}$ , the resistive drop (IR) and the charge redistribution cause the power dissipation in the channel. Usually, the zero order steady state current is used to determine the power dissipation. The additional power dissipation from

the channel charge redistribution is ignored. This is because, in the quasi-static model, charge redistribution is assumed to happen instantaneously with no propagation delays. However, the channel charge density still changes as an indirect function of time through the dependence on time varying terminal voltages. This allows the use of the quasi-static model to predict the charge redistribution and the associate power dissipation as long it satisfies  $t_R > 20 T_0$  [4.19] where  $t_R$  is the waveform rise time and  $T_0$  is the time taken by electrons to reach the drain from the source terminal (transit time). Moreover, the conventional charge model is based on the assumption that the MOSFET capacitors do not contribute any net power dissipation in the channel. But, as shown in Appendix [A4], it is not the case. The channel capacitances are not energy conserving. They do have some power dissipative terms due to the charge redistribution in the channel. These higher order dissipative terms become significant at higher frequencies, which make it necessary to include their effects on total power for efficient power dissipation prediction.

### 4.4 POWER EQUATIONS

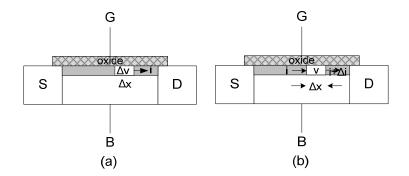


Fig: 4.6: MOSFET Channel Power Calculation

Fig 4.6 shows a MOS device. Considering a slice of thickness  $\Delta x$ , MOS channel can be thought of having two power components, due to:

• Fig. 4.6 a: The current i(x) flowing through the slice of thickness  $\Delta x$  having a potential  $\Delta v$ 

, which looks like a series resistance and results in the power dissipation of  $i\Delta v$ .

Fig. 4.6b: The rate of change of charge that is building in the slice due to the difference in current Δ*i*. This power change *v*Δ*i* is the energy stored in the charge at the potential *v*(*x*).

The instantaneous power going into the transistor channel  $P_c$  can then be estimated using

$$P_{c} = \int_{0}^{L} \frac{d}{dx} (i_{c}(x)v_{cb}(x)) dx = \int_{0}^{L} (\frac{d}{dx}i_{c}(x))v_{cb}(x)] dx + \int_{0}^{L} i_{c}(x)(\frac{d}{dx}v_{cb}(x))] dx$$
(4.12)

where the first integral represents change in stored energy and second term represents power dissipation. Keeping non-zero terms to first order in time derivatives, equation (4.13) can be expanded as:

$$P_c = P_{c0} + P_{c1,diss} + P_{c1,cons}$$

where

$$P_{c0} = \int_{0}^{L} I_{co}(\frac{d}{dx}v_{cb0}(x)) dx$$
 [Appendix 4.1] (4.13)

$$P_{c1,diss} = \int_{0}^{L} i_{c1} (\frac{d}{dx} v_{cb0}(x)) dx$$
 [Appendix 4.2] (4.14)

$$P_{c1, cons} = \int_{0}^{L} v_{cb0}(\frac{d}{dx}i_{c1}) dx$$
 [Appendix 4.3] (4.15)

The total instantaneous power P into the transistor is the sum of channel power  $P_c$  and gate

power 
$$P_{g1,cons}$$
.  
 $P = P_c + P_{g1,cons}$ 

where the gate power is

$$P_{g1,cons} = i_{g1}v_{gb} \tag{4.17}$$

(4.16)

where  $i_{g1}$  (Appendix: A3.3) is the first order gate current component.

Equation (4.13) represents the usual zero order power dissipation. Equation (4.14) represents the first order power dissipation due to the trans-capacitive transient current components and equation (4.15) represents the first order conserved power in the channel. Since the gate power estimated in equation (4.17) is assumed to be purely reactive and leakage free, it becomes necessary to add its contribution together with the conserved components from the channel to obtain a closed form solution for the stored energy function. Table 2 summarizes the power components and Appendix (A4) shows the derivation of these equations. We have used  $v_{gbt0} = v_{gb} - v_{t0}$ .

Power	Linear Region	Saturation	Cut-off
		Region	Region
<i>P</i> <sub>c0</sub>	$\frac{\mu c_{ox}}{2LK} v_{ds} (v_{gst}^2 - v_{gdt}^2)$	$\frac{\mu c_{ox}}{2LK} v_{ds} v^2_{gst}$	0
P <sub>c1,diss</sub>	$\frac{c_{ox}L}{30(v_{gdt}+v_{gst})^3}v_{ds}(v_{gst}-v_{gdt})[3v_{gdt}^2\frac{d}{dt}v_{gdt} + 3v_{gst}^2\frac{d}{dt}v_{gst} + 7v_{gdt}(\frac{d}{dt}v_{gdt} + \frac{d}{dt}v_{gst})v_{gst}]$	$\frac{\frac{c}{\partial x}L}{10} v_{ds} \frac{d}{dt} v_{gst}$	0
P <sub>c1,cons</sub>	$\frac{-\frac{c_{ox}L}{6K}[-3(v_{gdt}\frac{d}{dt}v_{gdt}+v_{gst}\frac{d}{dt}v_{gst})+}{4(v_{gdt}\frac{d}{dt}v_{gdt}(v_{gdt}+2v_{gst})+v_{gst}\frac{d}{dt}v_{gst}(2v_{gdt}+v_{gst}))(v_{gbt}0)}{(v_{gdt}+v_{gst})^2}]$	$-\frac{c_{ox}L}{6}\frac{d}{dt}v_{gst}$ $(v_{db}+3v_{sb})$	0

Table 4.	1: Power	Equations
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### 4.5 ENERGY FUNCTION CALCULATION

Energy is defined as *the capacity to do work*. In a MOSFET, work is done to transfer the charge from the source to the drain terminal. However, energy prediction is very tricky for MOS devices

as it is difficult to separate the charging (effective work) and the dissipative components of the electrons. This makes it difficult to predict how much energy is lost in the channel and how much energy is used as the effective work. To make the matter worse, the bias at the gate terminal forces these charge movements.

For the model derivation, the gate is assumed to be leakage free. It is also assumed that there is no net charge transfer from the gate to the channel. However, energy is still supplied from the gate to drive the channel charges. It then becomes necessary to add the contribution from the gate together with the channel charges. As these charges are conserved over a complete cycle, it is possible to derive a closed form analytical solution for an energy function from these conserved charges. The separation of conserved components make it possible to estimate total power dissipation by leaving out energy storage terms that do not contribute to power dissipation, making the solution simple, straightforward and computationally efficient.

The conserved component of channel power was given by equation (4.15). It can also be written as:

$$P_{c1,cons} = \frac{dE}{dt} = \sum_{V} \frac{\partial E}{\partial V} \frac{dV}{dt}$$
(4.18)

Equation (4.18) can be expanded to represent channel power in the form of energy as

$$P_{c1,cons} = \frac{\partial E_c}{\partial v_{gb}} \frac{dv_{gb}}{dt} + \frac{\partial E_c}{\partial v_{db}} \frac{dv_{db}}{dt} + \frac{\partial E_c}{\partial v_{sb}} \frac{dv_{sb}}{dt}$$
(4.19)

where  $E_c$  is some function of voltages  $v_{gb}$ ,  $v_{sb}$ ,  $v_{db}$ . Since the channel receives energy from the gate during switching transient, it can be shown [APPENDIX A4.5] that the energy from the channel alone is not conserved. Hence an energy function is not possible in equation (4.19).

Taking similar approach, gate power is represented using

$$P_{g1,cons} = \frac{\partial E_g}{\partial v_{gb}} \frac{dv_{gb}}{dt} + \frac{\partial E_g}{\partial v_{db}} \frac{dv_{db}}{dt} + \frac{\partial E_g}{\partial v_{sb}} \frac{dv_{sb}}{dt}$$
(4.20)

where  $E_g$  is also some function of  $v_{gb}$ ,  $v_{sb}$ ,  $v_{db}$ . Since gate is supplying the energy to the channel, it can also be shown that the gate alone has no energy function [APPENDIX A4.6]. An Energy function is possible only when the conserved components are combined [APPENDIX A4.7].

$$P_{cons} = P_{g1,cons} + P_{c1,cons}$$
(4.21)

Using equations (4.19), (4.20) and (4.21)

$$\frac{\partial E}{\partial v_{jb}}(v_{gb}, v_{sb}, v_{db}) = \frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_g}{\partial v_{jb}}; j = g, s, d$$
(4.22)

It can be shown that equation (4.22) can be solved [APPENDIX A4.7] to compute the energy function. Table 4.2 summarizes the energy function.

	ENERGY FUNCTION		
	Linear	Saturation	Cut-Off
Qg	$c_{ox}L(v_{gb} - v_{fb} - \phi - v_{sb} - \frac{v_{db} - v_{sb}}{2} + \frac{K(v_{db} - v_{sb})^{2}}{12(v_{gst} - K(v_{db} - v_{sb})/2)}$	$\phi - v_{sb} - \frac{v_{gst}}{3K})$	$c_{ox}L(v_{gb} - v_{fb} - \phi)$ $-\frac{v_{gbt0}}{K}$
E <sub>f</sub>	$\frac{1}{4}c_{ox}L\{(K-1)(v_{db}^{2}+v_{sb}^{2})+(v_{gbt}^{2}-v_{db}^{2})^{2}+(v_{gbt}^{2}-v_{sb}^{2})^{2}\}$ $+Q_{g}v_{t0}$	$\frac{\frac{1}{4}c_{ox}L\{(K-1)(\frac{v_{gbt0}^{2}}{K} + v_{sb}^{2}) + (v_{gbt0} - v_{sb})^{2}\}}{+Q_{g}v_{t0}}$	$\frac{\frac{c_{ox}L}{2}v_{gbt0}^{2}}{\frac{(K-1)}{K}}$ $+Q_{g}v_{t0}$

Table 4.2

## **CHAPTER V**

# V. FIRST ORDER CURRENT COMPONENTS AND CAPACITANCE CALCULATION

In this chapter, total capacitance equations are derived from the first order drain ( $i_{d1}$ ) and source ( $i_{s1}$ ) current components. These total capacitances are then separated into conserved and dissipative components. Finally, an equivalent circuit is developed by following the method used by Lim-Fossum [5.1] and results are verified for currents and charges.

# 5.1 FIRST ORDER CURRENT COMPONENTS

As seen in Table 3.1, first order currents are functions of voltages and their time derivatives (dv/dt). However, the coefficient of dv/dt instead of being purely storage capacitance is also responsible for some of the power dissipation in the channel. This suggests that the first order drain ( $i_{d1}$ ) and the source ( $i_{s1}$ ) currents consist of two separate components; one that contributes to power dissipation in the channel, and another that is responsible for the energy storage. Taking this approach, the first order drain and source currents obtained in chapter 3 can be expanded as

$$i_{d1} = i_{d1,cons} + i_{d1,diss}$$
 (5.1)

$$i_{s1} = i_{s1,cons} + i_{s1,diss}$$
(5.2)

where  $i_{d1,diss}$  and  $i_{s1,diss}$  are the dissipating, while  $i_{d1,cons}$  and  $i_{s1,cons}$  are the energy storing components of first order drain and source currents. Fig. 5.1 shows this concept where first order currents  $i_{d1}$  and  $i_{s1}$  are separated into two components. Since the gate and the substrate currents are non-dissipative in the absence of leakage, there is no need to separate them.

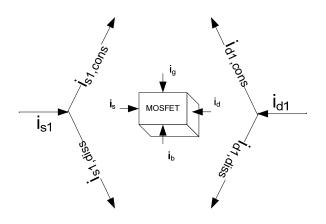


Figure 5.1: First order dissipative and conserved current components

The dissipative current components in equations (5.1) and (5.2) are due to the first order power dissipation in the channel from the charge redistribution. It is estimated by dividing the dissipative power obtained using equation (3.1) with the total channel potential as:

$$i_{d1,diss} = \frac{P_{c1,diss}}{v_{ds}} = -i_{s1,diss} = i_{tt,diss}$$
(5.3)

where  $i_{tt,diss}$  is the transient transport current that is responsible for the first order power dissipation in the channel, and is defined as positive going into the drain. The energy storage components are now easily computed by subtracting the dissipated component from the first order drain and source current components.

$$i_{d1,cons} = i_{d1} - i_{d1,diss}$$
 (5.4)

$$i_{s1,cons} = i_{s1} + i_{s1,diss}$$
 (5.5)

Equations (5.4) and (5.5) can also be verified by solving conserved channel power equation (4.16) obtained in chapter 4 as:

$$P_{c1,cons} = i_{d1,cons} v_{db} + i_{s1,cons} v_{sb}$$
(5.6)

Table 5.1 summarizes these first order, energy conserving and dissipative drain and source

current components in three regions of transistor operation.

	Linear	Saturation	Cut-Off
i d1, diss	$\frac{c_{ox}L(v_{gst} - v_{gdt})}{30(v_{gdt} + v_{gst})^3} [3(v_{gdt}^2 \frac{d}{dt}v_{gdt} + v_{gst}^2 \frac{d}{dt}v_{gst})$ $+7v_{gdt}v_{gst}(\frac{d}{dt}v_{gdt} + \frac{d}{dt}v_{gst})]$	$\frac{\frac{c_{ox}L}{10}}{10}\frac{d}{dt}v_{gst}$	0
<sup>i</sup> s1, diss	$-i_{d1,diss}$	$-i_{d1,diss}$	0
i <sub>d1, cons</sub>	$\frac{c_{ox}L}{6(v_{gdt} + v_{gst})^2} [v_{gdt} \frac{d}{dt} v_{gdt} (3v_{gdt} + 5v_{gst}) + v_{gst} \frac{d}{dt} v_{gst} (3v_{gdt} + v_{gst})]$	$\frac{\frac{c}{ox}L}{6}\frac{d}{dt}v_{gst}$	0
i s1, cons	$\frac{\frac{c_{ox}L}{6(v_{gdt} + v_{gst})^2} [v_{gdt} \frac{d}{dt} v_{gdt} (v_{gdt} + 3v_{gst}) + v_{gst} \frac{d}{dt} v_{gst} (5v_{gdt} + 3v_{gst})]$	$\frac{\frac{c}{ox}L}{2}\frac{d}{dt}v_{gst}$	0

# 5.2 CAPACITANCE DERIVATION

In the following section, capacitance equations are derived that are continuous and valid in all regions of transistor operation.

Conventional MOS transistor model assume the MOS channel is an energy storage device and ignores the dissipative components due to the channel charge redistribution and convection effects. It is shown [5.3] that the dissipative components have significant contributions at high

frequencies and energy conserving capacitance representation of MOSFET is misleading. However, MOS transistors can still be represented as an energy storage device if the dissipative components are separated from the total capacitances. Ours is a first step towards such a complete model, which is able to separate the total capacitance into the dissipative and conserved components.

Representing the first order current  $i_{i1}$  in terms of capacitance:

$$i_{i1} = C_{ii} \partial_t v_{ib} - \sum_{j \neq i,b} (C_{ij} \partial_t v_{jb}); \ i, j = g, d, s.$$
(5.9)

where  $C_{ii}$ ,  $C_{ij}$ 's are total capacitances and  $v_{ib}$ ,  $v_{jb}$  are the terminal voltages with respect to the body voltage. Table 5.3 summarizes these total capacitances, which are calculated by representing  $i_{d1}$  and  $i_{s1}$  in the above mentioned form. Table 5.4 and 5.5, on the other hand shows the independent energy storage and dissipative capacitances. This is one of the most important findings of our research, as all other capacitive models have mixed conserved and dissipative terms. However, in our model, the energy conserving capacitances are estimated simply from the conserved current components that were calculated using equations (5.4) and (5.5).

$$i_{i1,cons} = C_{cii} \partial_t v_{ib} - \sum_{j \neq i,b} (C_{cij} \partial_t v_{jb}); \ i, j = g, d, s.$$
(5.10)

where  $c_{cii}$ ,  $c_{cij}$  are the conserved components of the capacitor. In equation (5.9) and all the subsequent equations, the subscript notation 'c' or 'd' stands for conserved or dissipative components. Fig. 5.2 shows the normalized capacitance plots against different values of channel potential in 180 nm process parameters. The capacitance plot consists of total, conserved and dissipative capacitances that are calculated using respective currents.

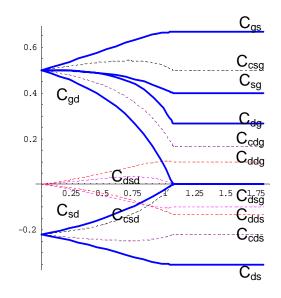


Figure 5.2 Total, Conserved and Dissipative Capacitances vs  $v_{\rm ds}$ 

	TOTAL CAPACITANCES		
	Linear	Saturation	Cut-Off
C <sub>gb</sub>	$\frac{k_2}{3(1+k_2)}c_{ox}L\frac{(v_{gdt} - v_{gst})^2}{(v_{gdt} + v_{gst})^2}$	$\frac{k_2}{3(1+k_2)}c_{ox}L$	$\frac{k_2 c_{ox} L}{(1+k_2)}$
C <sub>gd</sub>	$\frac{2}{3}c_{ox}Lv_{gdt}\frac{(v_{gdt}+2v_{gst})}{(v_{gdt}+v_{gst})^2}$	0	0
C <sub>gs</sub>	$\frac{2}{3}c_{ox}Lv_{gst}\frac{(2v_{gdt}+v_{gst})}{(v_{gdt}+v_{gst})^2}$	$\frac{2}{3}c_{ox}L$	0
	$\frac{c_{ox}L}{6} \frac{v_{gdt}^2 + 8v_{gst}v_{gdt} + 3v_{gst}^2}{(v_{gdt} + v_{gst})^2}$	$\frac{1}{2}c_{ox}L$	0
C <sub>sb</sub>	k <sub>2</sub> C <sub>csg</sub>	$k_2 C_{csg}$	0

Table 5.3:	Total	Capacitances
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C <sub>sd</sub>	$\frac{(1+k_{2})}{6}c_{ox}L\frac{v_{gdt}(v_{gdt}+3v_{gst})}{(v_{gdt}+v_{gst})^{2}}$	0	0
C <sub>dg</sub>	$\frac{c_{ox}L}{6} \frac{3v_{gdt}^2 + 8v_{gst}v_{gdt} + v_{gst}^2}{(v_{gdt} + v_{gst})^2}$	$\frac{1}{6}c_{ox}L$	0
C <sub>db</sub>	$k_2 C_{cdg}$	$k_2 C_{cdg}$	0
C <sub>ds</sub>	$-\frac{(1+k_{2})}{6}c_{ox}L\frac{v_{gst}(3v_{gdt}+v_{gst})}{(v_{gdt}+v_{gst})^{2}}$	$-\frac{1+k_2}{6}c_{ox}L$	0

Table 5.4: Conserved Ca	apacitances
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r				
	CONSERVED CAPACITANCES			
	Linear	Saturation	Cut-Off	
C <sub>gb</sub>	$\frac{k_2}{3(1+k_2)} c_{ox} L \frac{(v_{gdt} - v_{gst})^2}{(v_{gdt} + v_{gst})^2}$	$\frac{k_2}{3(1+k_2)}c_{ox}L$	$\frac{k_2 c_{ox} L}{(1+k_2)}$	
C <sub>gd</sub>	$\frac{2}{3}c_{ox}Lv_{gdt}\frac{(v_{gdt}+2v_{gst})}{(v_{gdt}+v_{gst})^2}$	0	0	
C <sub>gs</sub>	$\frac{2}{3}c_{ox}Lv_{gst}\frac{(2v_{gdt}+v_{gst})}{(v_{gdt}+v_{gst})^2}$	$\frac{2}{3}c_{ox}L$	0	
C <sub>csg</sub>	$\frac{\frac{c_{ox}L}{6}v_{gdt}^{2}+8v_{gst}v_{gdt}+3v_{gst}^{2}}{(v_{gdt}+v_{gst})^{2}}$	$\frac{1}{2}c_{ox}L$	0	
C <sub>csb</sub>	$k_2 C_{csg}$	$k_2 C_{csg}$	0	
C <sub>csd</sub>	$-\frac{(1+k_{2})}{6}c_{ox}L\frac{v_{gdt}(v_{gdt}+3v_{gst})}{(v_{gdt}+v_{gst})^{2}}$	0	0	

C <sub>cdg</sub>	$\frac{\frac{c_{ox}L}{6} \frac{3v_{gdt}^2 + 8v_{gst}v_{gdt} + v_{gst}^2}{(v_{gdt} + v_{gst})^2}}$	$\frac{1}{6}c_{ox}L$	0
	$k_2 C_{cdg}$	$k_2 C_{cdg}$	0
C <sub>cds</sub>	$-\frac{(1+k_{2})}{6}c_{ox}L\frac{v_{gst}(3v_{gdt}+v_{gst})}{(v_{gdt}+v_{gst})^{2}}$	$-\frac{1+k_2}{6}c_{ox}L$	0

# Table 5.5: Dissipative Capacitances

	DISSIPATIVE CAPACITANCES		
	Linear	Saturation	Cut-Off
C <sub>ddg</sub>	$\frac{c_{ox}L(v_{gst}-v_{gdt})(3v_{gdt}^2+14v_{gdt}v_{gst}+3v_{gst}^2)}{30\left(v_{gdt}+v_{gst}\right)^3}$	$\frac{1}{10}c_{ox}L$	0
C <sub>dds</sub>	$-\frac{(1+k_2)c_{ox}L(v_{gst}-v_{gdt})v_{gst}(7v_{gdt}+3v_{gst})}{30\left(v_{gdt}+v_{gst}\right)^3}$	$-\frac{1+k_2}{10}c_{ox}L$	0
C <sub>ddb</sub>	$-\frac{c_{ax}k_{2}L(v_{gst}-v_{gdt})(3v_{gdt}^{2}+14v_{gdt}v_{gst}+3v_{gst}^{2})}{30(v_{gdt}+v_{gst})^{3}}$	$-\frac{k_2}{10}c_{ox}L$	0
C <sub>dsg</sub>	$-C_{ddg}$	$-C_{ddg}$	0
C <sub>dsd</sub>	$\frac{\frac{(1+k_2)c_{ox}L(v_{gdt}-v_{gst})v_{gdt}(3v_{gdt}+7v_{gst})}{30(v_{gdt}+v_{gst})^3}$	0	0
C <sub>dsb</sub>	$-C_{ddb}$	$-C_{ddb}$	0

## 5.3 EQUIVALENT CIRCUIT

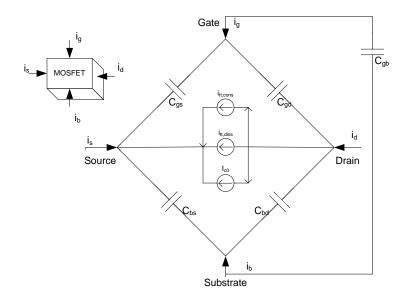


Figure 5.3: Equivalent Circuit

We have developed an equivalent circuit in this section by following the method used by Lim-Fossum [5.1]. Tables [5.3-5.5] showed that the capacitances are not reciprocal, which makes the capacitance representation using two terminal reciprocal capacitances impossible if these capacitances are made to represent the total first order drain current. However, equation (5.4) can be rewritten with reciprocal capacitors [Appendix A5.13] as

$$i_{d1,cons} = C_{gd} \partial_t v_{dg} + C_{bd} \partial_t v_{db} + i_{tt,cons}$$
(5.11)

where

$$i_{tt,cons} = (C_{gd} - C_{cdg})\partial_t v_{gb} + (C_{csd} - C_{cds})\partial_t v_{sb} + C_{csd}\partial_t v_{ds}$$
(5.12)

The dissipative component of current from equation (5.3) can also be written in terms of dissipative capacitances as

$$i_{d1,diss} = C_{ddd} \partial_t^v v_{db} - C_{ddg} \partial_t^v v_{gb} - C_{dds} \partial_t^v v_{sb} = i_{tt,diss} = -i_{s1,diss}$$
(5.13)

Fig.5.3 shows an equivalent circuit of a four terminal MOSFET. The circuit is equivalent to Lim-Fossum's, but we have broken the trans-capacitive transport current  $i_{tt}$  into conserved and dissipative components. There are three current components flowing from the drain to the source terminal.

The current component responsible for the first order power dissipation in the channel is represented by  $i_{tt,diss}$ . The conserved current component is represented by  $i_{tt,cons}$ .  $I_{c0}$  represents the steady state zero order current. Two terminal reciprocal capacitances  $C_{gd}$ ,  $C_{gs}$ ,  $C_{bd}$ ,  $C_{bs}$  and  $C_{gb}$  represents the conserved gate to drain, gate to source, substrate to source, substrate to drain and gate to substrate capacitances respectively. These reciprocal capacitances do not conserve energy by themselves; the conserved component of  $i_{tt}$  must be included.  $C_{ddd}$ ,  $C_{ddg}$ ,  $C_{dds}$  in equation (5.13) represents the dissipative drain to drain, drain to gate and drain to source capacitances respectively.

# **CHAPTER VI**

# VI. COMPARISON AND DISCUSSION

In this section we compare our results with Lim-Fossum's SOI model [6.1-6.3] and the BSIM Capacitive Model [6.4-6.5]. We also discuss the mechanism of net transfer of energy from the gate to the channel and show that the higher order dissipative terms modify the total power equation and have significant effects at higher frequencies.

#### 6.1 MODEL VERIFICATION AND ADVANTAGES

Our model verifies that Ward's [6.6] method of channel charge partitioning works correctly when the bulk charge has a linear dependence on the channel potential ( $v_{sb}$ ). Our model also verifies Lim-Fossum's equations for a fully depleted SOI MOSFET that uses Ward's partition scheme. It predicts the same source and drain currents, and hence the same terminal capacitances ( $C_{ij}$ ) as shown in Fig. 6.1. However, we are able to partition these total terminal capacitances into conserved ( $C_{cii}$ ) and dissipated ( $C_{dii}$ ) components.

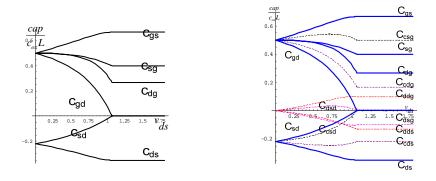
The partitioning approach to capacitances offers several advantages over conventional transcapacitances:

- The energy stored in the conserved capacitances can be predicted.
- They can be made to agree with Meyer's [6.7] capacitances if the body effect and body bias are ignored.

Fig 6.1 and Fig 6.2 shows the capacitances. The total capacitance shown in Fig 6.1 is separated into conserved and dissipative capacitances in Fig 6.2 and is written as

$$C_{ij} = C_{cij} + C_{dij}$$
 where  $i, j = g, s, d$ 

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**Figure 6.1:** Terminal capacitances vs v<sub>ds</sub> **Figure 6.2:** Capacitance vs v<sub>ds</sub>

Our other significant contribution has been in the power estimation. Our models have improved the device power estimation by implementing two important concepts:

- First order terms have to be included for power dissipation estimation as they become significant at higher frequencies.
- Stored components can be ignored for computationally efficient power dissipation estimation. The average device power computation is then possible by taking dissipative current times voltage and integrating them over time.

#### 6.2 ENERGY PUMPING

It is important to understand the pumping action of the gate to understand the power components from different sources. When the gate undergoes a rising (falling) transition, electrons (holes) are sucked out of the source terminal and stored in the channel. During the falling transition, these electrons (holes) are pushed out of the channel into the drain terminal. Even though the gate charge integrates out and there is no net charge transfer, there is transfer of energy from the gate to the channel. The gate acts as a energy source which allows the electrons (holes) to move in the channel, while the channel acts as a recipient of this energy.

Moreover, if power calculations are done using only the channel current components, it may appear that the MOS transistors are generating extra energy in the channel. In reality, power is pumped from the gate to the channel and when the gate contributions are added, the conserved terms cancel out. However, if the gate contributions are neglected, the channel ends up looking like an energy generator. Therefore it is not appropriate to integrate the channel currents alone for the power computation. Contributions from the gates need to be included. Fig. 6.3 shows the pumping action of the gate.

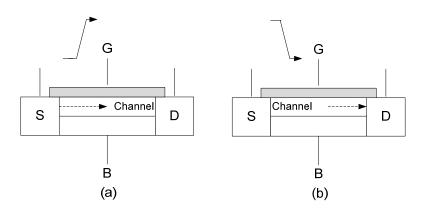


Figure 6.3: Gate pumping action

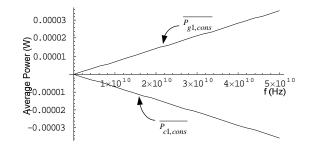


Figure 6.4: Average conserved gate and channel power vs. frequency

Fig. 6.4 shows the average conserved gate  $(\overline{P_{g1,cons}})$  and channel  $(\overline{P_{c1,cons}})$  power plots against frequency for 180 nm process parameters. The positive power from the gate shows that energy is flowing from the gate to the channel, while the negative channel power shows the energy generation at the channel. Since these average powers are equal and opposite, they cancel out over a complete cycle and contribute no net energy in the channel. This is all possible due to the existence of an energy function for the conserved components. The existence of

energy function validates the notion that the conserved terms do not contribute any net power dissipation in the channel. It also makes it possible to leave out power terms that do not contribute to net power dissipation in the total power equation, making the simulation simple and computationally efficient. This is explained in detail in the following section.

#### 6.3 TOTAL FIRST ORDER POWER

It is possible to derive the total first order MOS power by using the equation

$$P = i_{g1}v_{gb} + i_{d1}v_{db} + i_{s1}v_{sb}$$
(6.1)

The problem here is the complexity in the first order current terms. Other than the first order gate current, first order drain and source currents have both the conserved and dissipative terms, which are not separated. As mentioned in previous chapters, the gate and the conserved components of drain and source currents contribute no net power dissipation in the channel. Its presence just adds the extra complexity and slows down the simulation process. The separation of the first order terms into energy conserving and power dissipating terms on the other hand, simplifies the equation as energy conserving terms are taken out from the simulation. The total first order power then reduces to

$$P = i_{d1,diss} v_{db} + i_{s1,diss} v_{sb}$$
(6.2)

It should also be pointed out that leaving the gate component altogether and using the equation

$$P = i_{d1}v_{db} + i_{s1}v_{sb}$$
(6.3)

is not a very good option. In that case, as mentioned in section (6.1), the conserved channel power component acts as an independent source of energy. Equations using such models are inconsistent and should be avoided.

#### 6.4 SIMULATION EXAMPLE

A simple simulation is used to show the importance of first order power using only the dissipative components. Fig. 6.5 shows the idealized voltage waveforms for the drain and the gate terminals used to turn a transistor on then off.

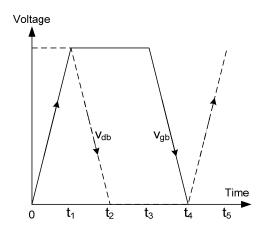


Figure 6.5: Idealized voltage waveforms

The average dissipative power from the first transition ( $v_{ds}=v_{dd}$ ) when  $v_{gb}$  goes from low at  $t_0$  to high at  $t_1$  is computed by

$$\overline{P_{c1}}_{(t_0 \to t_1)} = \frac{1}{(t_1 - t_0)} \int_{t_0}^{t_1} (i_{d1, diss} v_{db} + i_{s1, diss} v_{sb}) dt$$
(6.4)

If we assume the source and the substrate are at the same potential ( $v_{sb}=0$ ), equation (6.4) can be rewritten as

$$\overline{P_{c1}}_{(t_0 \to t_1)} = \frac{1}{(t_1 - t_0)} \int_{t_0}^{t_1} (i_{d1, diss} v_{db}) dt$$
(6.5)

In the second power dissipating transition, when the gate terminal is high, the drain swings from high at  $t_1$  to low at  $t_2$ . The dissipative power equation (6.4) reduces to

$$\overline{P_{c1}}_{(t_1 \to t_2)} = \frac{1}{(t_2 - t_2)} \int_{t_1}^{t_2} i_{d1,diss} dt_{dt} dt$$
(6.6)

During the interval  $t_2$  to  $t_4$ , there is no power dissipation in the channel ( $v_{db}=0$ ). Even though energy flows from the gate to the channel as  $v_{gb}$  changes, the energy is transferred to the channel carriers and is not dissipated. The final power transition occurs when the drain waveform swings from low at  $t_4$  to high at  $t_5$ . As the gate voltage has already reached a steady low value, the power equation becomes

$$\overline{P}_{c1(t_4 \to t_5)} = \frac{1}{(t_5 - t_4)} \int_{t_4}^{t_5} i_{d1,diss} v_{db} dt$$
(6.7)

The total dissipative power for a complete cycle is computed taking the sum of all these powers

$$\overline{P_{c1}} = \overline{P}(t_0 \to t_1) + \overline{P}(t_1 \to t_2) + \overline{P}(t_4 \to t_5)$$
(6.8)

For a complete cycle, energy is conserved. This allows us to leave out the conserved component from the power equation for computationally efficient power dissipation prediction. Nonetheless, the total dissipative powers predicted by equation (6.8) have first order terms. These first order dissipative components become significant at higher frequencies and modify the total power dissipated in the channel as shown in Fig 6.6. The total power is no longer constant, and at high frequencies becomes dependent on the switching frequencies.

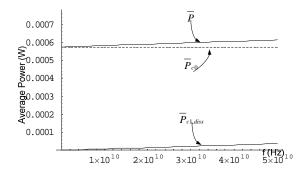


Fig 6.6: Total power vs. frequency

The result also shows that we need to be extra careful while doing the power measurements. It is not appropriate to look only at the channel dissipation; the first order power dissipation does have contributions from the gate. If the power dissipation is estimated by just considering the total channel power, there would be an extra negative component from the conserved energy. In that case, the channel would seem to act as an energy generator. Fig 6.7 and Fig 6.8 shows the current and the corresponding power plots.

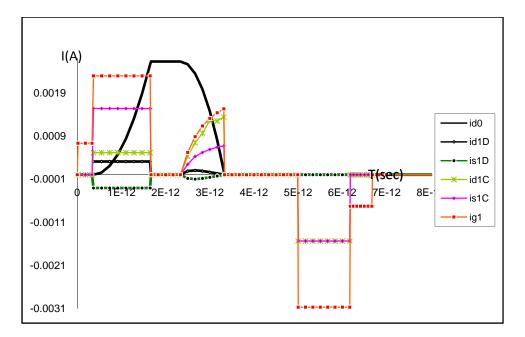


Figure 6.7: Current Plots

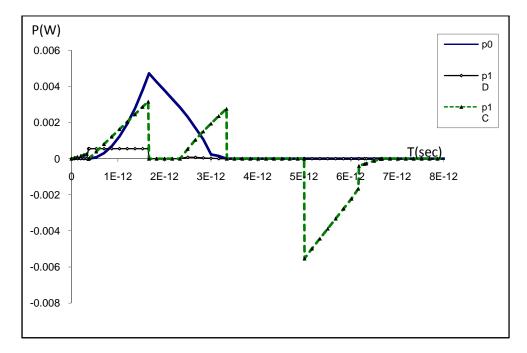


Figure 6.8: Power Plots

# **CHAPTER VII**

# VII. DEPENDENCE OF THE BSIM ABULK PARAMETER ON THE SOURCE POTENTIAL

In this chapter, the capacitive model is extended to include the source potential ( $v_{sb}$ ) dependence of the bulk charge coefficient *Abulk*. Until this chapter, the BSIM bulk parameter, *Abulk* [Appendix A7.1], was assumed to be constant with respect to the source potential, which made the derivation of the energy function possible. It also made the evaluation of the terminal capacitances straightforward, sacrificing very little accuracy. However for circuits where  $v_{sb}$  is not constant and bulk parameter dependence is included, unlike the Lim and Fossum model, the BSIM capacitive model fails to give an energy function for the conserved power components [Appendix A7.2]. The energy supplied from the gate does not balance with the energy generated in the channel and an extra power component shows up in the channel that has no physical basis. The term that gives energy storage in our model (equation (4.21)) does not give energy storage in BSIM, which makes the BSIM model inconsistent for power and energy prediction.

In general, when the conserved power components are integrated over a complete switching cycle and the transistor is returned to the original state, there is a non non-zero power contribution. This is where the inconsistency of the BSIM model is evident. The BSIM bulk charge coefficient has  $v_{sb}$  dependence and when this is included, the BSIM model:

- Generates extra current that has no physical basis
- Gives a net non-zero power that shows up in the channel from the terms that are supposed to be conserved,
- Fails to give an energy function from all of the conserved components

It should also be pointed out that we are not finding the energy function for the total transistor power, as not all the power components are conserving. It is also not true that the BSIM model has no energy function. It has a quasi-energy function; the same term that shows up in our model (Chapter 4) also show up in the BSIM model. Obviously for those terms there is an energy function. But, the BSIM model also has some extra terms due to the  $v_{sb}$  dependence that do not show up in our model, which makes it impossible to find an energy function for all of the conserved components. In other words, the quasi-conserving BSIM model is inconsistent. It generates extra power in the channel that has no physical basis.

Though the extra term has no physical rationale, it is thought to be from the incomplete mathematical representation of the square root dependence of the bulk charge on the channel potential  $v_{cb}$ , which the BSIM model tries to linearise using the first two terms of a Taylor's expansion. It can then be assumed that if the higher order terms are included that were left out in the Taylor's expansion, the BSIM model should provide the correct energy function.

Nonetheless, the good news is that we can still apply our model to BSIM by comparing the energy differences between the models. By doing so, we should be able to separate out the energy function from all the terms except for those that have  $v_{sb}$  dependence and also evaluate the physically inconsistent extra dissipating components.

#### 7.1 EVALUATION OF EXTRA CURRENT COMPONENTS

Our conserved components of the gate  $(i_{g1, cons})$ , source  $(i_{s1, cons})$  and the drain  $(i_{d1, cons})$ currents are given in Appendix (A3.3.5), and the respective BSIM components  $(i_{g1cons, B}, i_{s1cons, B})$  and  $i_{d1cons, B}$ ) can be evaluated including the source potential dependence on the bulk charge parameter using the equations given in Appendix (7.3). The difference in the first order gate current due to the source dependence of the BSIM bulk charge parameter is then given by

$$i_{g1,cons}\Big|_{Extra} = i_{g1cons,B} - i_{g1,cons}$$
(7.1)

Similarly, the difference in the conserved first order drain current is given by

$$i_{d1, cons}\Big|_{Extra} = i_{d1cons, B} - i_{d1cons}$$
(7.2)

and the difference in the first order source current is given by

$$i_{s1, cons}\Big|_{Extra} = i_{s1, cons, B} - i_{s1, cons}$$
(7.3)

These extra conserved first order gate, drain and the source currents predicted by equations (7.1-7.3) causes extra power in the channel that has no physical basis, and can be estimated using

$$P_{g1,cons}\Big|_{Extra} = P_{g1,cons,B} - P_{g1,cons}$$
(7.5)

$$P_{c1,cons}\Big|_{Extra} = P_{c1,cons,B} - P_{c1,cons}$$
(7.6)

$$P_{1,cons}\Big|_{Extra} = P_{g1,cons}\Big|_{Extra} + P_{c1,cons}\Big|_{Extra}$$
(7.7)

where

.

$$P_{g1, cons, B} = i_{g1, cons, B} v_{gb}$$
 and

 $P_{c1, cons, B} = i_{d1, cons, B} v_{db} + i_{s1, cons, B} v_{sb}$ 

#### 7.2 SIMULATION EXAMPLE

In this section, a simple simulation example is presented using a pass transistor logic. Though it is not straightforward to separate the conserved and the dissipative power components in the BSIM model (due to the channel charge partition), the example does show the existence of extra power due to  $v_{sb}$  dependence of *Abulk*. A pass transistor is chosen because they have a high  $v_{sb}$  swing which makes the BSIM models' unphysical effect (generation of extra power) more

pronounced. For the BSIM model to be consistent, it is assumed that the difference from the first order dissipative power should give the correction term. This correction term should then balance out the extra power component generated in the channel.

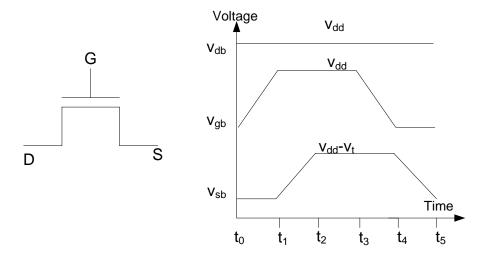


Figure 7.1: Pass transistor simulation - Voltage Waveforms (180nm process parameters)

Fig. 7.1 shows the idealized voltage waveforms for the drain, gate and the source terminals. The drain terminal is assumed to be high ( $v_{dd}$ ) during the entire simulation, while the gate and the source potentials are varied to calculate the extra power component.

In the first transition ( $t_0$  to  $t_1$ ), the gate terminal goes from low (0) at  $t_0$  to high ( $v_{dd}$ ) at  $t_1$ , while the source potential remains low (0). The transistor enters the saturation as soon as the gate to source potential  $v_{gb} - v_{sb}$  becomes greater than the threshold voltage  $v_t$ . The extra energy *Et*1, calculated from the extra power (eq. (7.7)) is then given by

$$Et1 = \int_{t0}^{t1} P_{1, cons} \Big|_{Extra} dt$$
(7.8)

During the second transition ( $t_1$  to  $t_2$ ), the gate terminal stays high ( $v_{dd}$ ) and the pass transistor remains in the saturation. The source terminal on the other hand, goes from low (0) to high ( $v_{dd} - v_t$ ) and the extra energy *Et*2 becomes

$$Et2 = \int_{t1}^{t2} P_{1, cons} \Big|_{Extra} dt$$
(7.9)

The transistor now enters cutoff (at  $t_2$ ) and remains there even though the gate and source terminals come back to their original states at  $t_4$  and  $t_5$ . The extra energies during these transitions are given by

$$Et3 = \int_{t2}^{t3} P_{1, cons} \Big|_{Extra} dt$$

$$Et4 = \int_{t3}^{t4} P_{1, cons} \Big|_{Extra} dt$$

$$Et5 = \int_{t4}^{t5} P_{1, cons} \Big|_{Extra} dt$$
(7.10)

Combining all, total energy difference (Et ) can be written as

$$Et = \sum_{i} Et_{i} \text{ where } i = 1 \text{ to } 5$$
(7.11)

For a complete cycle, energy should have been conserved and there should have been no contribution. But as shown by equation (7.11) and Fig 7.2, this is not the case. There is some extra power in the channel  $P_{1, cons}\Big|_{Extra}$ , which is more than the first order dissipative power

 $P_{c1,diss}$ . The correction term from the difference in first order dissipative power  $P_{c1,diss}\Big|_{Extra}$  that

we thought would negate the extra channel power was non-existent.

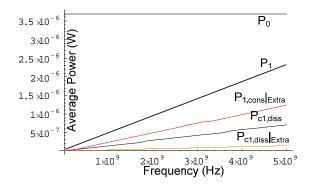


Figure 7.2: Extra power dissipation

Fig. 7.2 also shows that the frequency dependence of power components becomes significant at higher frequencies and also raises the first order power dissipation to a new value  $P_1$ , which includes the first order dissipative power ( $P_{cl,diss}$ ) and all other extra unphysical components (

 $P_{1,cons}\Big|_{Extra}$  and  $P_{c1,diss}\Big|_{Extra}$ ). It also proves that the energy pumped from the gate does not

balance out in the channel as was the case when *Abulk* was assumed to be a constant. In this particular case, the channel acts as an independent energy generator. This error, together with the non-inclusion of first order dissipative power makes the BSIM model inconsistent for energy and power prediction.

Fig. 7.3 compares the differences in the bulk charge parameters (*Abulk vs.*  $1+k_2$ ) and the threshold voltages ( $Vt_{,B}$  and Vt) between BSIM and our models, while Fig. 7.4 shows the zero order current plot for the simulation example mentioned above. From the plots 7.3 and 7.4, it is evident that our parameters match very well with the BSIM parameters when the zero order current is dominant.

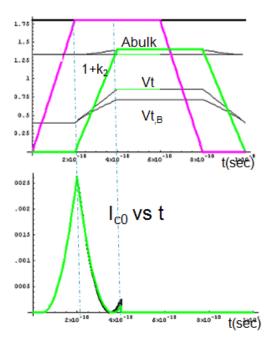


Figure 7.3: Abulk vs. (1+k2) and Vt's (Top)Figure 7.4: Zero order current plots (Bottom)

Fig 7.5 shows the instantaneous first order gate, drain and source current components. Here also, the plots matches very well and the difference is evident only in the first order source current, which as mentioned above, is due to the dependence of source potential and other extra components on the BSIM bulk charge parameter *Abulk* [Appendix 7].

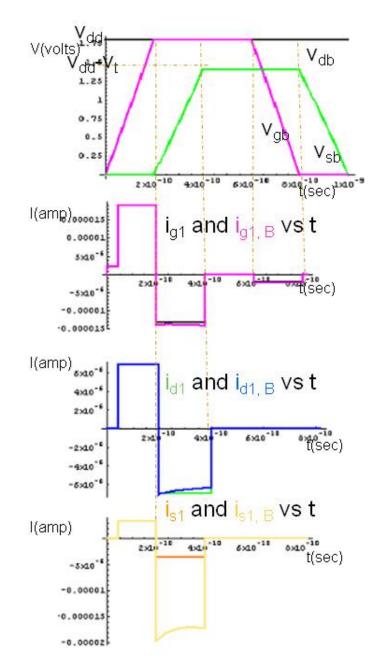


Figure 7.5: First order currents

### 7.3 CONCLUSION

Conventional MOS models for circuit simulation assume that the channel capacitances do not contribute to net power dissipation. Numerical integration of channel currents and instantaneous terminal voltages however shows the existence of first order dissipating terms. Given that the accuracy of the simulation depends on the physical representation of the device, it is very important that we have a reliable mathematical model that is able to represent the device behavior. Designers need these accurate models for circuit development.

To overcome the limitation of conventional charge based models, a self-consistent, first order, quasi-static, power dissipation model has been developed that is able to

- Predict the exact solution to first order 1-D channel equations for MOSFETs without a channel charge partition approximation provided that the charge has a linear dependence on the channel potential.
- Validate the terminal currents as being the same as Ward's channel charge partition approximation.
- Validate that Ward's partition scheme is correct as long as the charge has a linear dependence on the channel potential.
- Derive the first order channel charge (q<sub>c1</sub>) and current (i<sub>c1</sub>) as a function of position (x) inside the channel.
- Derive the first order power dissipation and conserved components.
- Estimate energy function.
- Separate the terminal current into conserved and dissipative components.
- Identify the inconsistencies in the BSIM power model.

In conclusion, there is a need to extend this work to include channel charge with a non-linear voltage dependence that does not generate extra power dissipation in the channel that has no physical basis.

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# APPENDICES

#### **APPENDIX 1: 180 NMOS SPICE model parameters**

### A1.1 180nm NMOS SPICE Parameters

.model NMOS NMOS +Level = 49+Lint = 4.e-08 Tox = 4.e-09+Vth0 = 0.3999 Rdsw = 250 +lmin=1.8e-7 lmax=1.8e-7 +Tref=27.0 version =3.1 +Xj= 6.000000E-08 +lln= 1.0000000 +wwn= 0.00 +lw = 0.00+w = 0.00+Mobmod= 1 +xw = 0+Dwg= 0.00 +K1= 0.5613000 +K3= 0.00 +Dvt2= 8.000000E-03 +Dvt2w= 0.00 +K3b= 0.00 +Vsat= 1.3800000E+05 +Uc= -5.250000E-11 +Prwg= 0.00 +A0= 1.1000000 +A2= 1.0000000 +B1 = 0.00+Voff= -0.12350000 +Cdsc= 0.00 +Eta0= 0.2200000 +PcIm= 5.000000E-02 +Pdiblcb= -1.3500E-02 +Pscbe2= 1.00000E-20 +Alpha0 = 0.00+kt1= -0.3700000 +Ute= -1.4800000 +Uc1 = 0.00 $+C_{j}=0.00365$ +Cjsw= 7.9E-10 +Cta=0+Ptp=0+N=1.0 +Caso=2.786E-10 +NQSMOD=0+Cgsl= 1.6E-10

Clc = 0.0000001Dwc= 0 wmin=1.8e-7 Cf= 1.069e-10 Nch= 5.950000E+17 lwn= 1.0000000 ||= 0.00|w| = 0.00ww= 0.00 binunit= 2 binflag=0Dwb= 0.00 K2= 1.000000E-02 Dvt0= 8.0000000 Dvt0w= 0.00 NIx= 1.650000E-07 Ngate= 5.000000E+20 Ua= -7.0000000E-10 Prwb = 0.00Wr= 1.0000000 Keta= 4.000000E-02 Ags= -1.000000E-02 NFactor= 0.9000000 Cdscb=0.00Etab= 0.00 Pdiblc1= 1.200000E-02 Drout= 1.7999999E-02 Pvag= -0.2800000 Beta0= 30,0000000 kt2= -4.000000E-02 Ua1= 9.5829000E-10 Kt1l= 4.000000E-09 Mj= 0.54 Mjsw= 0.31 Ctp=0JS=1.50E-08 Xti=3.0 Cabo=0.0E+00 Elm= 5 Cgdl= 1.6E-10

wmax=1.0e-4 DIc= 4E-08 wln= 0.00 wint= 0.00wwl = 0.00x = 0Dvt1= 0.7500000 Dvt1w = 0.00W0 = 0.00Ub= 3.500000E-18 U0= 3.500000E-02 A1 = 0.00B0= 0.00 Cit= 0.00 Cdscd=0.00Dsub= 0.8000000 Pdiblc2= 7.50000E-03 Pscbe1= 8.66000E+08 Delta= 1.000000E-02 At= 5.500000E+04 Ub1= -3.3473000E-19 Prt = 0.00Pb= 0.982 Php= 0.841 Pta=0JSW=2.50E-13 Cgdo=2.786E-10 Capmod=2Xpart= 1 Ckappa= 2.886

Cle=0.6

Vfbcv= -1

# A2.1 180nm PMOS SPICE Parameters

.model PMOS PMOS +Level = 49+Lint = 3.e-08 Tox = 4.2e-09 +Vth0 = -0.42 Rdsw = 450 +lmin=1.8e-7 +wmax=1.0e-4 +Xj= 7.000000E-08 +lln= 1.0000000 +wwn= 0.00 +lw = 0.00+wl = 0.00+Mobmod = 1+xw = 0.00+binflag= 0 +ACM=0+rsh=0+rsc=0+K1= 0.5560000 +K3 = 0.00+Dvt2= -1.000000E-02 +Dvt2w = 0.00+K3b=0.00+Vsat= 1.050000E+05 +Uc= -2.9999999E-11 +Prwg= 0.00 +A0= 2.1199999 +A2= 0.4000000 +B1 = 0.00+Voff= -6.4000000E-02 +Cdsc = 0.00+Eta0= 8.5000000 +Pclm= 2.0000000 +Pdiblcb= 0.1450000 +Pscbe2= 1.000000E-20 +Alpha0= 0.00 +kt1= -0.3700000 +Ute= -1.4800000 +Uc1 = 0.00+Cj= 0.00138 +Cjsw= 1.44E-09 +Cta= 0.00093 +Ptp=0+N=1.0 +Caso=2.786E-10 +NQSMOD=0+Cgsl= 1.6E-10 +Cf= 1.058e-10 +DIc= 3E-08

Imax=1.8e-7 Tref=27.0 version =3.1 Nch= 5.920000E+17 lwn= 1.0000000 ||= 0.00|w| = 0.00ww = 0.00binunit= 2 Dwg= 0.00 ldif=0.00 rd=0rdc=0K2= 0.00 Dvt0= 11.2000000 Dvt0w = 0.00NIx= 9.500000E-08 Ngate= 5.000000E+20 Ua= -1.200000E-10 Prwb = 0.00Wr= 1.0000000 Keta= 2.9999999E-02 Ags= -0.1000000 NFactor= 1.400000 Cdscb=0.00Etab = 0.00Pdiblc1= 0.1200000 Drout= 5.000000E-02 Pvag= -6.000000E-02 Beta0= 30.0000000 kt2= -4.000000E-02 Ua1= 9.5829000E-10 Kt1l= 4.000000E-09 Mj= 1.05 Mjsw = 0.43Ctp=0JS=1.50E-08  $X_{ti=3.0}$ Capo=0.0E+00 Elm= 5 Cgdl= 1.6E-10 Clc= 0.0000001 Dwc=0

wln= 0.00 wint= 0.00wwl = 0.00x = 0.00Dwb = 0.00hdif=0.00 rs=0Dvt1= 0.7200000 Dvt1w = 0.00W0 = 0.00Ub= 1.000000E-18 U0= 8.000000E-03 A1 = 0.00B0= 0.00 Cit= 0.00 Cdscd=0.00Dsub= 2.8000000 Pdiblc2= 8.000000E-05 Pscbe1= 1.000000E-20 Delta= 1.000000E-02 At= 5.500000E+04 Ub1= -3.3473000E-19 Prt= 0.00 Pb= 1.24 Php= 0.841 Pta= 0.00153 JSW=2.50E-13 Cgdo=2.786E-10 Capmod=2Xpart= 1 Ckappa= 2.886

Cle= 0.6

Vfbcv= -1

wmin=1.8e-7

### **APPENDIX 3: MOSFET CURRENT EQUATIONS**

The zero and first order channel charges as well as currents were used in chapter 3. However, the derivations were not shown, which is given in this appendix. It should also be pointed out that these derivations are very tedious and results would not have been possible without the help of sophisticated tools like Mathematica.

## A3.1 Zero Order Current Component

In equation (3.27), the zero order charge  $q_{c0}$  at a distance x along the channel is given by

$$q_{c0} = -\sqrt{(q_s^2(1 - x/L) + q_d^2 x/L)}$$

where L is the length of the channel.  $q_s$  and  $q_d$  are the source and the drain charges per unit length as given in (3.14) and (3.18). These charges can be substituted into the steady state current equation (3.28) to represent  $I_{c0}$  in terms of voltages.

$$I_{c0} = \frac{\mu}{2Lc_{ox}K} (q_d^2 - q_s^2) = \frac{\mu}{2LC_c} (v_{gst}^2 - v_{gdt}^2)$$
(A3.1)

In pinch-off saturation, the drain charge density ( $q_d$ ) is zero. This reduces the zero order current (A3.1) to

$$I_{c0} = \frac{\mu c_{ox}}{2LK} v_{gst}^2$$
(A3.2)

The corresponding drain to source potential in saturation ( $v_{dssat}$ ) can be estimated by setting

$$v_{gdt} = v_{gb} - v_t - v_{sb} - K(v_{db} - v_{sb}) = 0$$

so that

$$v_{dssat} = \frac{v_{gb} - v_t - v_{sb}}{K}$$
  
where  $K = \begin{cases} 1 + k_2 \rightarrow SOI \\ Abulk \rightarrow BULK \end{cases}$  as defined in (3.24).

In cut-off, it is assumed that there is no channel current, which is made possible by setting the source charge density  $q_{c}$  to zero.

$$I_{c0} = 0$$
 (A3.2)

(A3.1), (A3.2) and (A3.3) give the usual equations for the steady state current neglecting velocity saturation effects.

#### A3.2 First Order Channel Charge and Channel Current

The derivation of first order channel charge and current components are one of the most important findings of our research. The first order channel charge allows calculating the first order channel current without a charge partition, which can be used to calculate the first order drain and source currents. The first order channel current also makes it possible to derive the energy stored and dissipative power components. Since it is crucial component of our research, a detailed derivation is presented in this appendix.

Taking charge density as a function of potential along the channel, and keeping terms of first order in time derivatives, the current continuity equation (3.25) can be written as

$$\frac{d}{dx}(q_{c0}\frac{d}{dx}q_{c1} + q_{c1}\frac{d}{dx}q_{c0}) = -\frac{C_c}{\mu}\frac{d}{dt}q_{c0}$$
(A3.2.1)

Rearranging the terms, first order channel charge per unit length becomes

$$q_{c1} = -\frac{C_c}{\mu} \frac{1}{q_{c0}} \frac{d}{dt} \int \int q_{c0}[x] dx dx + c1x + c0$$
(A3.2.2)

where *c1* and *c0* are constants of integration, and can be calculated using the boundary condition  $q_{c1} = 0$  at x = 0 and x = L

$$c0 = \frac{C_c}{\mu} \frac{d}{dt} \int \left[ q_{c0}[x] dx dx \right]_{x \to 0}$$

$$= 4 \frac{C_c}{\mu} L^2 q_s^4 \frac{(4q_d q_s \frac{d}{dt} q_d - 5q_d^2 \frac{d}{dt} q_s + q_s^2 \frac{d}{dt} q_s)}{15(-q_d^2 + q_s^2)^3}$$
(A3.2.3)

$$c1 = \frac{C_c}{\mu} \frac{d}{dt} \int \int q_{c0}[x] dx dx \bigg|_{x \to L}$$

$$= 4 \frac{C_c}{\mu} L \frac{(-q_d \frac{d}{dt} q_d (q_d^{-5} - 5q_d^{-3} q_s^{-2} + 4q_s^{-5}) - q_s (4q_d^{-5} - 5q_d^{-2} q_s^{-3} + q_s^{-5}) \frac{d}{dt} q_s)}{15(-q_d^{-2} + q_s^{-2})^3}$$
(A3.2.4)

Substituting the values of *c0*, *c1* and  $q_{c0}$  in (A3.2.2), the first order charge at any point x along the channel becomes

$$\begin{split} q_{c1} &= -\frac{1}{15\sqrt{\frac{q_s^2(L-x)+q_d^2x}{L}\mu}} \{4C_c L(\frac{Lq_s^4(4q_dq_s\frac{d}{dt}q_d-5q_d^2\frac{d}{dt}q_s+q_s^2\frac{d}{dt}q_s)}{(-q_d^2+q_s^2)^3} + \\ &((q_d^5\frac{d}{dt}q_d-q_s^5\frac{d}{dt}q_s+4q_d^3q_s^2(-\frac{d}{dt}q_d+\frac{d}{dt}q_s)+4q_d^2q_s^3(-\frac{d}{dt}q_d+\frac{d}{dt}q_s) - \\ &q_dq_s^4(4\frac{d}{dt}q_d+\frac{d}{dt}q_s)+q_d^4q_s(\frac{d}{dt}q_d+4\frac{d}{dt}q_s))x)/(q_d-q_s)^2(q_d+q_s)^3) - \\ &\frac{1}{(q_d^2-q_s^2)^3} \left(\frac{q_s^2(L-x)+q_d^2x}{L}\right)^{3/2} (Lq_s(4q_dq_s\frac{d}{dt}q_d-5q_d^2\frac{d}{dt}q_s+q_s^2\frac{d}{dt}q_s) - \\ &(q_d^2-q_s)(q_d+q_s)(q_d\frac{d}{dt}q_d-q_s\frac{d}{dt}q_s)x))) \end{split}$$

The first order channel current at any position x along the channel can now be estimated using

$$i_{c1} = \frac{\mu}{C_c} (q_{c0} \frac{d}{dx} q_{c1} + q_{c1} \frac{d}{dx} q_{c0})$$
(A3.2.6)

Taking derivatives of  $q_{c0}$  and  $q_{c1}$ , and substituting the corresponding values, (A3.2.6) expands to

$$i_{c1} = \frac{L}{15(q_d - q_s)^2(q_d + q_s)^3} \{4(q_d \frac{d}{dt}q_d (q_d^4 + q_d^3 q_s - 4q_d^2 q_s^2 - 4q_d q_s^3 - 4q_s^4) + q_d \frac{d}{dt}q_s (4q_d^4 + 4q_d^3 q_s + 4q_d^2 q_s^2 - q_d q_s^3 - q_s^4)\}$$

$$(A3.2.7)$$

$$-10(q_d + q_s)(\sqrt{q_s^2(1 - \frac{x}{L}) + q_d^2 \frac{x}{L}}$$

$$\{q_s(2q_d \frac{d}{dt}q_d q_s - (3q_d^2 - q_s^2) \frac{d}{dt}q_s) - (q_d^2 - q_s^2)(q_d \frac{d}{dt}q_d - q_s \frac{d}{dt}q_s)x\}$$

As mentioned above, this is one of the most important findings of our research and can be solved to find the first order drain  $(-i_{c1} = i_{d1}, x \rightarrow L)$  and source  $(i_{c1} = i_{s1}, x \rightarrow 0)$  current components, which are shown in Table 3.1. These results obtained without partitioning the channel charge are in agreement with previous results (Lim-Fossum and BSIM) which were obtained using Ward's partition. Therefore we have verified that Ward's partition is correct when the voltage dependence of Abulk is ignored and the channel charge is linearly dependent on  $v_{cb}$ .

### A3.3 First Order Gate Current

We present here the derivation of the gate current. These derivations are not different than what have been done already and can be found in the literature.

The total gate charge ( $Q_g$ ) can be estimated by integrating the gate charge density from the source (x=0) to the drain terminals (x=L) as

$$Q_g = \int_0^L q_g dx \tag{A3.3.1}$$

where channel current equation  $i_c(x,t)\int dx = \mu \int_{v_{sb}}^{v_{ab}} q_c(x,t) dv_{cb}(x)$  can be solved to get

$$\int_{0}^{L} dx = \mu \int_{v_{sb}}^{v_{db}} \frac{q_c(x,t)}{i_c(x,t)} dv_{cb}(x)$$
(A3.3.2)

Replacing  $\int_{0}^{L} dx$  in (A3.3.1), it can be rewritten as

$$Q_{g} = \frac{\mu}{i_{c0}} \int_{v_{sb}}^{v_{db}} q_{g}(x,t) q_{c}(x,t) dv_{cb}(x)$$
(A3.3.3)

which can be solved to get the total gate charge.

/

$$Q_{g} = c_{ox}L\left(v_{gb} - v_{fb} - \phi - v_{sb} - \frac{v_{db} - v_{sb}}{2} + \frac{K(v_{db} - v_{sb})^{2}}{12(v_{gst} - \frac{K(v_{db} - v_{sb})}{2})}\right)$$
(A3.3.4)

The first order drift current flowing in the gate terminal can now be calculated from

$$i_{g1} = \frac{d}{dt}Q_g = \frac{dv_{gb}}{dt}\frac{dQ_g}{dv_{gb}} + \frac{dv_{db}}{dt}\frac{dQ_g}{dv_{db}} + \frac{dv_{sb}}{dt}\frac{dQ_g}{dv_{sb}}$$
(A3.3.5)

Taking the derivatives, the first order gate current in the linear region becomes

$$i_{g1} = c_{ox}L \frac{(3(K-1)\frac{d}{dt}v_{gb}(v_{gdt} + v_{gst})^2 + 2v_{gdt}\frac{d}{dt}v_{gdt}(v_{gdt} + 2v_{gst}) + 2v_{gst}(2v_{gdt} + v_{gst})\frac{d}{dt}v_{gst})}{3K(v_{gdt} + v_{gst})^2}$$
(A3.3.6)

In pinch-off saturation, when  $q_d = 0$  ,  $i_{g1}$  reduces to

$$i_{g1} = \frac{c_{ox}L}{3K} (3(K-1)\frac{d}{dt}v_{gb} + 2\frac{d}{dt}v_{gst})$$
(A3.3.7)

In cut-off, though the drift components of the drain and the source currents are zero, the gate still has some current, which can be estimated by setting  $q_s = 0$  in equation (A3.3.5)

$$i_{g1} = \frac{c_{ox}L}{K}(K-1)\frac{d}{dt}v_{gb}$$
 (A3.3.8)

### **APPENDIX 4: MOSFET POWER EQUATIONS**

This appendix describes the detailed derivations of MOS power components that were used in chapter 4. To avoid confusion with the general definition of the static and dynamic power terms, channel power components are defined as the zero and the first order powers in the dissertation. It should be pointed out that the zero order power defined in equation (4.14) is different than the static power. In general, static power is defined as being independent of time (time invariant). However, the zero order power that has been used in this research is time variant. Although there is no explicit time dependence, it depends on the terminal voltages that change in time. The first order power on the other hand, depends on the time derivatives of the terminal voltages, while the dynamic power that has been used in the literature depends on energy stored in external capacitances which is dissipated by both zero order and first order power in the transistor.

#### A4.1 Zero order power

The zero order power is given in equation (4.14) as

$$P_{c0} = \int_{0}^{L} [I_{c0}(\frac{d}{dx}v_{cb0}(x))] dx$$
(A4.1.2)

since  $I_{c0}$  is independent of the position along the channel x, equation (A4.1.1) reduces to  $I_{c0}v_{ds}$ where  $I_{c0}$  is given in equation (A4.1) as

$$I_{c0} = \frac{\mu}{2KL} c_{ox} (v_{gst}^2 - v_{gdt}^2)$$
(A4.1.2)

From (A4.1.2) and (A4.1.1)

$$P_{c0} = \frac{\mu}{2LK} c_{ox} v_{ds} (v_{gst}^2 - v_{gdt}^2)$$
(A4.13)

In pinch off saturation, the change density at the drain is assumed to be zero, which reduces (A4.1.3) to

$$P_{c0} = \frac{\mu}{2LK} c_{ox} v_{ds} v_{gst}^2$$
(A4.1.4)

In cut-off region, when the source charge density becomes zero, equation (A4.1.4) further reduces to 0.

### A4.2 First order dissipated power

In equation (4.15), the first order channel dissipated power is given by

$$P_{c1,diss} = \int_{0}^{L} [i_{c1}(\frac{d}{dx}v_{cb0}(x))] dx$$
(A4.2.1)

where  $i_{c1}$  is the first order channel current given by (A3.2.7). Solving the integral, (A4.2.1)

reduces to

$$P_{c1,diss} = \frac{L}{30C_c (q_d + q_s)^3} (q_d - q_s)^2 (3q_d^2 \frac{d}{dt}q_d + 3q_s^2 \frac{d}{dt}q_s$$

$$+7q_d (\frac{d}{dt}q_d + \frac{d}{dt}q_s)q_s)$$
(A4.2.2)

where  $q_d, q_s, \frac{d}{dt}q_d, \frac{d}{dt}q_s$  are defined in the List of Symbols. Substituting the values of

 $q_d, q_s, \frac{d}{dt}q_d, \frac{d}{dt}q_s$  in terms of v's and  $\frac{d}{dt}v$ 's as given in (3.14), (3.15), (3.18) and (3.19) into

(A4.2.2) gives

$$P_{c1,diss} = \frac{c_{ox}L}{30(v_{gdt} + v_{gst})^3} v_{ds} (v_{gst} - v_{gdt}) (3v_{gdt}^2 \frac{d}{dt} v_{gdt} + 3v_{gst}^2 \frac{d}{dt} v_{gst} + 7v_{gdt} (\frac{d}{dt} v_{gdt} + \frac{d}{dt} v_{gst}) v_{gst})$$
(A4.2.3)

In pinch-off saturation region, as  $q_d = 0$  equation (A4.2.3) reduces to

$$P_{c1,diss} = \frac{c_{ox}L}{10} v_{ds} \frac{d}{dt} v_{gst}$$
(A4.2.4)

and in cutoff, the first order dissipative power becomes

$$P_{c1,diss} = 0$$

### A4.3 FIRST ORDER CONSERVED POWER

The first order channel conserved power is given in (4.16) by

$$P_{c1,cons} = \int_{0}^{L} [v_{cb0}(\frac{d}{dx}i_{c1})] dx$$
(A4.3.1)

where  $i_{c1}$  is the first order channel current and  $v_{cb0}$  is the zero order channel potential. Integrating, equation (A4.3.1) expands to

 $P_{c1,cons} = -\frac{c_{ox}L}{6K} [-3(v_{gdt}\frac{d}{dt}v_{gdt} + v_{gst}\frac{d}{dt}v_{gst}) + \frac{4(v_{gdt}\frac{d}{dt}v_{gdt}(v_{gdt} + 2v_{gst}) + v_{gst}\frac{d}{dt}v_{gst}(2v_{gdt} + v_{gst}))(v_{gbt})}{(v_{gdt} + v_{gst})^{2}}]$ (A4.3.2)

In pinch-off saturation, with  $q_d = 0$ , equation (A4.3.3) reduces to

$$P_{c1,cons} = -\frac{c_{ox}L}{6}\frac{d}{dt}v_{gst}(v_{db} + 3v_{sb})$$
(A4.3.3)

and in cut-off, it becomes

 $P_{c1,cons} = 0$ 

#### A4.4 Energy function validation for the gate

Clairaut's theorem states that, "*If two second order partials are continuous, their derivatives will be equal*". The same theorem can be used to check the equality of second order partial and verify the existence of an energy function for the conserved power.

Using equation (4.18), the conserved first order gate power is given by

$$P_{g1,cons} = i_{g1}v_{gb} = v_{gb} \frac{c_{ox}L}{3K(v_{gdt} + v_{gst})^2} (3(K-1)\frac{d}{dt}v_{gb}(v_{gdt} + v_{gst})^2 + 2v_{gdt}\frac{d}{dt}v_{gdt}(v_{gdt} + 2v_{gst}) + 2v_{gst}(2v_{gdt} + v_{gst})\frac{d}{dt}v_{gst})$$
(A4.4.1)

In terms of energy, the conserved power can be written as

$$P_{g1,cons} = \frac{\partial E}{\partial v} \frac{dv}{dt} = \frac{\partial E_g}{\partial v_{gb}} \frac{dv_{gb}}{dt} + \frac{\partial E_g}{\partial v_{db}} \frac{dv_{db}}{dt} + \frac{\partial E_g}{\partial v_{sb}} \frac{dv_{sb}}{dt}$$
(A4.4.2)

Comparing (A4.4.1) and (A4.4.2), the derivatives of the gate energy with respect to voltages give

$$\frac{\partial E_g}{\partial v_{sb}} = \frac{-2c_{ox}Lv_{gbt}v_{gst}(2v_{gdt} + v_{gst})}{3(v_{gdt} + v_{gst})^2}$$
(A4.4.3)

$$\frac{\partial E_g}{\partial v_{db}} = \frac{-2c_{ox}Lv_{gbt}v_{gdt}(v_{gdt} + 2v_{gst})}{3(v_{gdt} + v_{gst})^2}$$
(A4.4.2)

$$\frac{\partial E_g}{\partial v_{gb}} = \frac{1}{6} c_{ox} L v_{gbt} \left( 6 - \frac{2(v_{gdt} - v_{gst})^2}{K(v_{gdt} + v_{gst})^2} \right)$$
(A4.4.3)

As mentioned earlier, an energy function exists if and only if the second order partials of (A4.4.3)-(A4.4.5) are equal. Comparing (A4.4.3)-(A4.4.5)

$$\frac{\partial}{\partial v_{sb}} (\frac{\partial E_g}{\partial v_{gb}}) \neq \frac{\partial}{\partial v_{gb}} (\frac{\partial E_g}{\partial v_{sb}})$$
$$\frac{\partial}{\partial v_{db}} (\frac{\partial E_g}{\partial v_{gb}}) \neq \frac{\partial}{\partial v_{gb}} (\frac{\partial E_g}{\partial v_{db}})$$

It is found that the partials are not equal, and hence an energy function does not exist for gate alone.

# A4.5 Energy function validation for the channel

In equation (A3.3), the conserved channel power is given by

$$P_{c1,cons} = -\frac{c_{ox}L}{6K} [-3(v_{gdt}\frac{d}{dt}v_{gdt} + v_{gst}\frac{d}{dt}v_{gst}) + \frac{4(v_{gdt}\frac{d}{dt}v_{gdt}(v_{gdt} + 2v_{gst}) + v_{gst}\frac{d}{dt}v_{gst}(2v_{gdt} + v_{gst}))(v_{gbt})}{(v_{gdt} + v_{gst})^{2}}]$$
(A4.5.1)

Taking a similar approach as in A4.4, the conserved power in terms of energy can be written as

$$P_{c1,cons} = \frac{\partial E_c}{\partial v_{gb}} \frac{dv_{gb}}{dt} + \frac{\partial E_c}{\partial v_{db}} \frac{dv_{db}}{dt} + \frac{\partial E_c}{\partial v_{sb}} \frac{dv_{sb}}{dt}$$
(A4.5.2)

From (A4.5.1) and (A4.5.2)  $\frac{\partial E}{\partial v}$ 's can be solved to get

$$\frac{\partial E_c}{\partial v_{sb}} = \frac{-c_{ox} L v_{gst} (3(v_{gdt} + v_{gst})^2 - 4v_{gbt} (2v_{gdt} + v_{gst}))}{6(v_{gdt} + v_{gst})^2}$$
(A4.5.3)

$$\frac{\partial E_c}{\partial v_{db}} = \frac{-c_{ox} L v_{gdt} (3(v_{gdt} + v_{gst})^2 - 4v_{gbt} (v_{gdt} + 2v_{gst}))}{6(v_{gdt} + v_{gst})^2}$$
(A4.5.4)

$$\frac{\partial E_c}{\partial v_{gb}} = \frac{c_{ox} L(3(v_{gdt} + v_{gst})^3 - 4v_{gbt}(v_{gdt}^2 + 4v_{gdt}v_{gst} + v_{gst}^2)}{6K(v_{gdt} + v_{gst})^2}$$
(A4.5.5)

Taking partials and comparing (A4.5.3)-(A4.5.5)

$$\frac{\partial}{\partial v_{sb}} (\frac{\partial E_c}{\partial v_{gb}}) \neq \frac{\partial}{\partial v_{gb}} (\frac{\partial E_c}{\partial v_{sb}})$$
$$\frac{\partial}{\partial v_{db}} (\frac{\partial E_c}{\partial v_{gb}}) \neq \frac{\partial}{\partial v_{gb}} (\frac{\partial E_c}{\partial v_{db}})$$

It is found that the partials are not equal. Hence an energy function does not exist for the channel alone.

### A4.6 Energy function validation for combination of the gate and the channel

In this appendix, an energy function is validated for the combination of the gate and the conserved component of the channel power. In equation (4.17), the total first order conserved power is given by

$$P_{cons} = P_{c1,cons} + P_{g1,cons}$$
(A4.6.1)

In terms of energy, the total power can be written as

$$P_{cons} = \left(\frac{\partial E_c}{\partial v_{gb}} + \frac{\partial E_g}{\partial v_{gb}}\right) \frac{dv_{gb}}{dt} + \left(\frac{\partial E_c}{\partial v_{db}} + \frac{\partial E_g}{\partial v_{db}}\right) \frac{dv_{db}}{dt} + \left(\frac{\partial E_c}{\partial v_{sb}} + \frac{\partial E_g}{\partial v_{sb}}\right) \frac{dv_{sb}}{dt}$$
(A4.6.2)

which can be solved to get  $\frac{dE}{dv}$ 's from the coefficients of  $\frac{dv_{jb}}{dt}$  as

$$\frac{\partial E}{\partial v_{jb}}(v_{gb}, v_{sb}, v_{db}) = \frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_g}{\partial v_{jb}}; j = g, s, d$$
(A4.6.3)

The second order partials are now compared for the validation of an energy function as done in previous sections.

$$\frac{\partial E}{\partial v_{sb}} = \frac{-c_{ox}Lv_{gst}(3(v_{gdt} + v_{gst})^2 - 4v_{gbt}(2v_{gdt} + v_{gst}))}{6(v_{gdt} + v_{gst})^2} + \frac{-2c_{ox}Lv_{gbt}v_{gst}(2v_{gdt} + v_{gst})}{3(v_{gdt} + v_{gst})^2}$$
(A4.6.4)

$$\frac{\partial E}{\partial v_{db}} = \frac{-c_{ox}Lv_{gdt}(3(v_{gdt} + v_{gst})^2 - 4v_{gbt}(v_{gdt} + 2v_{gst}))}{6(v_{gdt} + v_{gst})^2} + \frac{-2c_{ox}Lv_{gbt}v_{gdt}(v_{gdt} + 2v_{gst})}{3(v_{gdt} + v_{gst})^2}$$
(A4.6.5)

$$\frac{\partial E}{\partial v_{gb}} = \frac{1}{6} c_{ox} L v_{gbt} \left( 6 - \frac{2(v_{gdt} - v_{gst})^2}{K(v_{gdt} + v_{gst})^2} \right) + \frac{c_{ox} L (3(v_{gdt} + v_{gst})^3 - 4v_{gbt} (v_{gdt}^2 + 4v_{gdt} v_{gst} + v_{gst}^2)}{6K (v_{gdt} + v_{gst})^2}$$
(A4.6.6)

$$\frac{\partial}{\partial v_{sb}} \left(\frac{\partial E}{\partial v_{gb}}\right) = \frac{\partial}{\partial v_{gb}} \left(\frac{\partial E}{\partial v_{sb}}\right)$$
(A4.6.7)

$$\frac{\partial}{\partial v_{db}} \left(\frac{\partial E}{\partial v_{gb}}\right) = \frac{\partial}{\partial v_{gb}} \left(\frac{\partial E}{\partial v_{db}}\right)$$
(A4.6.8)

$$\frac{\partial}{\partial v_{sb}} \left(\frac{\partial E}{\partial v_{db}}\right) = \frac{\partial}{\partial v_{db}} \left(\frac{\partial E}{\partial v_{sb}}\right) \tag{A4.6.9}$$

The results (A4.6.7)-(A4.6.9) show that the partials are equal. It also confirms that an energy function exists and can be derived using the conserved components of the gate and the channel power.

## A4.7 Energy Function

It should be pointed out here again that an energy function is possible if and only if

- The dependence of *Abulk* on *v*<sub>sb</sub> is ignored
- The bulk charge has a linear dependence on v<sub>cb</sub> and
- The gate power is included with the conserved component of the channel power to compute the total conserved power.

The existence of an energy function was validated in appendix A4.6, which can be evaluated by solving the partial differentials using

$$\frac{\partial E}{\partial v_{jb}}(v_{gb}, v_{sb}, v_{db}) = \frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_g}{\partial v_{jb}}; j = g, s, d$$
(A4.7.1)

This method however, is a little cumbersome as it involves lots of algebra. A simple solution is possible by separating the gate power into two components.

$$P_{g1,cons} = i_{g1}v_{gb} = i_{g1}v_{gbt0} + i_{g1}v_{t0}$$
(A4.7.2)

where  $v_{gbt0} = v_{gb} - v_{t0}$  and  $i_{g1}v_{t0}$  can be considered as the threshold power. In terms of energy,

the gate power becomes

$$P_{g1,cons} = (\frac{dE_{gbt}}{dv_{gb}} + \frac{dE_{t0}}{dv_{gb}})\frac{dv_{gb}}{dt} + (\frac{dE_{gbt}}{dv_{db}} + \frac{dE_{t0}}{dv_{db}})\frac{dv_{db}}{dt} + (\frac{dE_{gbt}}{dv_{sb}} + \frac{dE_{t0}}{dv_{sb}})\frac{dv_{sb}}{dt}$$
(A4.7.3)

where  $E_{t0}$  is the threshold energy function and  $E_{gbt}$  is the rest of the energy. Equation (A4.7.1)

now can be rewritten as

$$\frac{\partial E}{\partial v_{jb}}(v_{gb}, v_{sb}, v_{db}) = \frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_{gbt}}{\partial v_{jb}} + \frac{\partial E_{t0}}{\partial v_{jb}}; j = g, s, d$$
(A4.7.4)

Though the total  $\frac{\partial E}{\partial v}$  is the same, the separation of the threshold component makes it possible to

derive two simple energy functions, one from the combination of  $\frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_{gbt}}{\partial v_{jb}}$ , and the other

from  $\frac{\partial E_{t0}}{\partial v_{ib}}$ . These two energy functions can then be combined to find the total energy function.

#### Threshold Energy Function (*E*<sub>t0</sub>) Calculation:

From (A7.2) and (A7.3), the threshold power can be written as

$$i_{g1}v_{t0} = \frac{\partial E_{t0}}{\partial v_{gb}} \frac{\partial v_{gb}}{\partial t} + \frac{\partial E_{t0}}{\partial v_{db}} \frac{\partial v_{db}}{\partial t} + \frac{\partial E_{t0}}{\partial v_{sb}} \frac{\partial v_{sb}}{\partial t}$$
(A4.7.5)

where  $i_{g1}$  is the gate current given by (A3.3.6). Since  $v_{t0}$  is constant, the threshold energy

function is given by

$$E_{t0} = \int i_{g1} v_{t0} dt = Q_g v_{t0}$$
(A4.7.6)

where  $Q_g$  is the gate charge and is given in the Table 4.2.

### Energy Function *E*<sub>cgbt</sub> Calculation:

Leaving the threshold terms, equation (A4.7.4) reduces to

$$\frac{\partial E_{cgbt}}{\partial v_{jb}}(v_{gb}, v_{sb}, v_{db}) = \frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_{gbt}}{\partial v_{jb}}; j = g, s, d$$
(A4.7.7)

which can be solved to find  $\frac{\partial E}{\partial v}$  's using A4.6.4 – A4.6.6

$$\frac{\partial E_{cgbt}}{\partial v_{gb}} = \frac{1}{2}c_{ox}L(2v_{gbt} - v_{db} - v_{sb})$$
(A4.7.8)

$$\frac{\partial E_{cgbt}}{\partial v_{sb}} = \frac{1}{2}c_{ox}L(Kv_{sb} - v_{gbt})$$
(A4.7.9)

$$\frac{\partial E_{cgbt}}{\partial v_{db}} = \frac{1}{2}c_{ox}L(Kv_{db} - v_{gbt})$$
(A4.7.10)

Taking partials of (A4.7.8)-(A4.7.10)

$$\frac{\partial}{\partial v_{sb}} \left( \frac{\partial E_{t0}}{\partial v_{gb}} \right) = \frac{\partial}{\partial v_{gb}} \left( \frac{\partial E_{t0}}{\partial v_{sb}} \right)$$
(A4.7.11)

$$\frac{\partial}{\partial v_{db}} \left(\frac{\partial E_{t0}}{\partial v_{gb}}\right) = \frac{\partial}{\partial v_{gb}} \left(\frac{\partial E_{t0}}{\partial v_{db}}\right)$$
(A4.7.12)

$$\frac{\partial}{\partial v_{sb}} \left( \frac{\partial E_{t0}}{\partial v_{db}} \right) = \frac{\partial}{\partial v_{db}} \left( \frac{\partial E_{t0}}{\partial v_{sb}} \right)$$
(A4.7.13)

The results (A4.7.11) - (A4.7.13) show that the partial derivatives are equal and an energy function also exist for the sum of the remaining gate and channel components. This energy function  $E_{cgbt}$  is then calculated solving the partial differentials with three independent variables

$$v_{gb}, v_{sb}, v_{db}$$
 respectively.

Solving with respect to the gate potential

$$E_{cgbt} = \int \frac{\partial E_{cgbt}}{\partial v_{gb}} dv_{gb} + E_1(v_{sb}, v_{db})$$

$$= \frac{1}{2} c_{ox} L(v_{gbt0}^2 - v_{gbt0}v_{db} - v_{gbt0}v_{sb}) + E_1(v_{sb}, v_{db})$$
(A4.7.14)

Solving with respect to the drain potential

$$E_{cgbt} = \int \frac{\partial E_{cgbt}}{\partial v_{db}} dv_{db} + E_2(v_{gb}, v_{sb})$$

$$= \frac{1}{4} c_{ox} L K v_{db}^2 - \frac{1}{2} c_{ox} L v_{gbt} v_{db} + E_2(v_{gb}, v_{db})$$
(A4.7.15)

Solving with respect to the source potential

$$E_{cgbt} = \int \frac{\partial E_{cgbt}}{\partial v_{sb}} dv_{sb} + E_3(v_{gb}, v_{db})$$

$$= \frac{1}{4} c_{ox} LK v_{sb}^2 - \frac{1}{2} c_{ox} L v_{gbt0} v_{sb} + E_3(v_{gb}, v_{db})$$
(A4.7.16)

Comparing and combining equations (A4.7.14)-(A4.7.16), the energy function reduces to

$$E_{cgbt} = \frac{1}{4}c_{ox}L((K-1)(v_{db}^2 + v_{sb}^2) + (v_{gbt0} - v_{db})^2 + (v_{gbt0} - v_{sb})^2)$$
(A4.7.17)

The total energy function can now be determined using

$$E = E_{cgbt} + E_{t0} \tag{A4.7.18}$$

$$E = \frac{1}{4}c_{ox}L\{(K-1)(v_{db}^2 + v_{sb}^2) + (v_{gbt0} - v_{db})^2 + (v_{gbt0} - v_{sb})^2\} + Q_g v_{t0}$$
(A4.7.19)

In pinch-off saturation region, as  $q_d = 0$  equation (A4.7.19) becomes

$$E = \frac{1}{4}c_{ox}L\{(K-1)(\frac{v_{gbt0}^{2}}{K} + v_{sb}^{2}) + (v_{gbt0} - v_{sb})^{2}\} + Q_{g,sat}v_{t0}$$
(A4.7.20)

where  $Q_{g,sat}$  is the gate charge at the saturation and is given by  $c_{ox}L(v_{gb} - v_{fb} - \phi - v_{sb} - \frac{v_{gst}}{3K})$ 

and in the cutoff, the energy function reduces to

$$E = \frac{1}{2}c_{ox}L(v_{gbt0})^2\frac{(K-1)}{K} + Q_{g,off}v_{t0}$$

where  $Q_{g,off}$  is the gate charge at the cutoff and is given by  $c_{ox}L(v_{gb} - v_{fb} - \phi - \frac{v_{gbt0}}{K})$ .

### **APPENDIX 5: CAPACITORS FOR EQUIVALENT CIRCUIT**

This appendix describes the derivation of a reciprocal capacitance plus some extra term that was used to represent the MOSFET using an equivalent circuit in section 5.3. Tables [5.3-5.5] showed that the MOSFET does not have reciprocal capacitances as  $C_{ji} \neq C_{ij}$ . However, these non-reciprocal capacitances can still be used to represent reciprocal capacitors plus the difference term using Lim-Fossum [6.1] terminal current equation as

$$i_{ij} = C_{ji} \frac{d}{dt} v_i - C_{ij} \frac{d}{dt} v_j$$
(A5.1)

where  $i_{ij}$  is the current at i<sup>th</sup> terminal due to the variation in j<sup>th</sup> terminal. Substituting equation (A5.1) to find the current at the drain terminal due to the variation at the gate

$$i_{dg} = C_{gd} \frac{d}{dt} v_{db} - C_{dg} \frac{d}{dt} v_{gb}$$
(A5.2)

where  $C_{gd}$  are  $C_{dg}$  are gate to drain and drain to gate capacitances. Equation (A5.2) can also be

written as

$$i_{dg} = C_{dg} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_d + C_{gd} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_g$$

$$= (C_{dg} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_g) + C_{gd} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_d$$

$$= (C_{dg} \frac{d}{dt} v_{dg}) + (C_{gd} - C_{dg}) \frac{d}{dt} v_d$$
(A5.3)

The current at the drain terminal due to the variation at the source is given by

$$i_{ds} = (C_{ds}\frac{d}{dt}v_{ds}) + (C_{sd} - C_{ds})\frac{d}{dt}v_d$$
(A5.4)

Similarly, drain current due to the variation at the substrate is given by

$$i_{db} = (C_{db}\frac{d}{dt}v_d) + (C_{bd} - C_{db})\frac{d}{dt}v_d$$
(A5.5)

Equations (A5.3 - A5.5) are combined to get the first order drain current as

$$i_{d1} = i_{dg} + i_{db} + i_{ds}$$
(A5.6)

$$i_{d1} = C_{dg} \frac{d}{dt} v_{dg} + C_{db} \frac{d}{dt} v_{db} + C_{ds} \frac{d}{dt} v_{ds} + (C_{gd} - C_{dg} + C_{bd} - C_{db} + C_{sd} - C_{ds}) \frac{d}{dt} v_{ds}$$
(A5.7)

The drain current can also be represented using

$$i_{d1} = C_{dd} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_g - C_{ds} \frac{d}{dt} v_s - C_{db} \frac{d}{dt} v_b$$
(A5.8)

which can be expanded as

$$i_{d1} = (C_{db} + C_{dg} + C_{ds})\frac{d}{dt}v_d - C_{dg}\frac{d}{dt}v_g - C_{ds}\frac{d}{dt}v_s - C_{db}\frac{d}{dt}v_b$$
$$= C_{db}\frac{d}{dt}v_{db} + C_{ds}\frac{d}{dt}v_{ds} + C_{dg}\frac{d}{dt}v_{gd}$$
(A5.9)

Equations (A5.7) and (A5.9) represents the same first order drain current, which is ture, if and only if

$$(C_{gd} - C_{dg}) + (C_{bd} - C_{db} + C_{sd} - C_{ds})\frac{d}{dt}v_d = 0$$
(A5.10)

Using capacitance table [5.3 - 5.5]

$$(C_{gd} - C_{dg}) = \frac{(C_{bd} - C_{db})}{k_2} = -\frac{(C_{sd} - C_{ds})}{1 + k_2}$$
(A5.11)

Substituting these values into equation (A5.10) and solving

$$-\frac{\binom{C_{sd} - C_{ds}}{1 + k_{2}} - k_{2} \frac{\binom{C_{sd} - C_{ds}}{1 + k_{2}} + \binom{C_{sd} - C_{ds}}{1 + k_{2}} + \binom{C_{sd} - C_{ds}}{1 + k_{2}} + \binom{C_{sd} - C_{ds}}{1 + k_{2}} = 0$$
(A5.12)

which shows that Lim-Fossum representation of the first order drain current with equation (A5.2) is correct as long as the condition (A5.10) is met. The first order drain current used in equation (A5.2) and highlighted in (A5.13)

$$i_{dg} = C_{gd} \frac{d}{dt} v_d + C_{dg} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_d - C_{dg} \frac{d}{dt} v_d + C_{dg} \frac{d}{dt} v_d + C_{dg} \frac{d}{dt} v_g$$
(A5.13)

can also be represented using

$$i_{dg} = C_{gd} \frac{d}{dt} v_d + C_{gd} \frac{d}{dt} v_g - C_{gd} \frac{d}{dt} v_g - C_{dg} \frac{d}{dt} v_g$$

$$= C_{gd} \frac{d}{dt} v_{dg} + (C_{gd} - C_{dg}) \frac{d}{dt} v_g$$
(A5.14)

$$i_{ds} = C_{sd} \frac{d}{dt} v_{ds} + (C_{sd} - C_{ds}) \frac{d}{dt} v_s$$
(A5.15)

$$i_{db} = C_{bd} \frac{d}{dt} v_{db} + (C_{bd} - C_{db}) \frac{d}{dt} v_{b}$$
(A5.16)

Equations (A5.14 – A5.16) can again be combined to find the total first order drain current as

$$i_{d1} = i_{dg} + i_{ds} + i_{db}$$
 (A5.17)

which is represented in section [5.3] in the form

$$i_{d1} = C_{bd} \frac{d}{dt} v_{db} + C_{sd} \frac{d}{dt} v_{ds} + C_{gd} \frac{d}{dt} v_{dg}$$

$$+ (C_{gd} - C_{dg}) \frac{d}{dt} v_g + (C_{sd} - C_{ds}) \frac{d}{dt} v_s + (C_{bd} - C_{db}) \frac{d}{dt} v_b$$
(A5.18)

# **APPENDIX 6**

# A6.1 Total dissipative power

The instantaneous MOS power can be estimated using

$$P = P_{c0} + P_{g1} + P_{d1} + P_{s1}$$
(A6.1)

where

$$P_{c0} = I_{c0}v_{ds}$$

$$P_{g1} = i_{g1}v_{db} = P_{g1,cons}$$

$$P_{d1} = i_{d1}v_{db} = P_{d1,cons} + P_{d1,diss}$$

$$P_{s1} = i_{s1}v_{db} = P_{s1,cons} + P_{s1,diss}$$
(A6.2)
(A6.3)

and the total conserved power is given by

$$P_{cons} = P_{c1, cons} + P_{g1, cons}$$

The derivation of the energy function from  $P_{cons}$  proves that there is no net energy loss from the conserved components. This is only possible when

$$\overline{P_{g1,cons}} = -\overline{P_{c1,cons}}$$
(A6.4)

From (A6.1), (A6.2), (A6.3) and (A6.4), it can be shown that the average MOS dissipative power can be written as

$$\overline{P} = \overline{P_{c0}} + \overline{P_{d1,diss}} + \overline{P_{s1,diss}}$$

#### **APPENDIX 7**

#### A7.1 BSIM Bulk Parameter (Abulk)

A non-zero drain to source potential makes the depletion width non-uniform along the channel. This non uniform depletion width which causes the threshold voltage to vary along the channel is known as the bulk charge effect, and is represented in the BSIM capacitive model using the bulk-charge coefficient *Abulk*. In order to account for the short-channel, narrow-width and many other effects, the *Abulk* parameter is more complicated than  $1 + \frac{K1}{2\sqrt{2\phi_f} + v_{sb}}$  that has been used in our

equations. In the BSIM model, the bulk charge coefficient is expressed as

$$Abulk = \left(1 + \frac{K1}{2\sqrt{2\phi_f - v_{bs}}} \left[\frac{A0.L_{eff}}{L_{eff} + 2\sqrt{XJ.X_{dep}}} (1 - AGS(v_{gs} - v_t)(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ.X_{dep}}})^2) + \frac{B0}{W_{eff} + B1}\right]\right)$$

$$\frac{1}{1 + KETA.v_{bs}}$$

#### A7.2 Energy function verification due to v<sub>sb</sub> dependence of Abulk

The existence of an energy function was validated in Appendix A4 ignoring the dependence of *Abulk* on  $v_{sb}$ . In this appendix, we present a proof that the dependence of the BSIM *Abulk* parameter on  $v_{sb}$  fails to give an energy function for all of the conserved components and leads to an absolute error in first order power. As mentioned in Chapter 7, though it is not straightforward to separate the conserved and the dissipative power components in the BSIM model due to the channel charge partition, it can still be shown that an energy function is never possible (from all of the conserved components) when *Abulk* has a non-linear dependence on the source potential.

Total first order conserved power  $P_{1,cons}$  is given by equation (4.21) as

$$P_{1,cons} = P_{c1,cons} + P_{g1,cons}$$
(A7.2.1)

where  $P_{c1,cons}$  is the first order conserved channel power, and  $P_{g1,cons}$  is the first order conserved gate power. For the energy function verification, instead of using solutions from equations (4.16) and (4.18), the conserved powers are recalculated by making the threshold voltage ( $v_t$ ) and bulk charge coefficient (*Abulk*) dependent on  $v_{sb}$ , such that the first order time derivatives for  $v_t$  becomes

$$\frac{d}{dt}v_t(v_{sb}) = (Abulk(v_{sb}) - 1)\frac{d}{dt}v_{sb}$$
(A7.2.2)

where 
$$v_t(v_{sb}) = v_{t0} + K1(\sqrt{2\phi_f + v_{sb}} - \sqrt{2\phi_f})$$
 and  $Abulk(v_{sb}) = 1 + \frac{K1}{2\sqrt{2\phi_f + v_{sb}}}$ 

and the first order time derivative for  $\textit{Abulk}(\textit{v}_{sb})$  expands to

$$\frac{d}{dt}Abulk(v_{sb}) = (Abulk(v_{sb}) - 1) \left( -\frac{\frac{d}{dt}v_{sb}}{2(2\phi_f + v_{sb})} \right)$$
(A7.2.3)

The conserved gate power can now be evaluated using equation (A4.4.1). The source potential dependence of *Abulk*, which was ignored initially to make *Abulk* = 1 + k2, however is included in the new conserved gate power estimation.

$$P_{g1,cons}\Big|_{Abulk(v_{sb})} = c_{ox}L(-(v_{gdt}^2 - v_{gst}^2)(2v_{gdt} + v_{gst})(\frac{d}{dt}v_{gb} - \frac{d}{dt}v_{gst}) + Abulk(v_{gdt}^2 - v_{gst}^2)(2v_{gdt} + v_{gst})(\frac{d}{dt}v_{gb} - \frac{d}{dt}v_{gst}) + 6Abulk^3\frac{d}{dt}v_{gb}(v_{gdt} + v_{gst})^2$$

$$(v_{gb} - v_{gst} - v_t + \phi) - 2Abulk^2(3\frac{d}{dt}v_{gb}(v_{gdt} + v_{gst})^2 - 2v_{gdt}\frac{d}{dt}v_{gdt}(v_{gdt} + 2v_{gst}) - 2v_{gst}\frac{d}{dt}v_{gst}(2v_{gdt} + v_{gst})(v_{gb} - v_{gst} - v_t + \phi))/6Abulk^3(v_{gdt} + v_{gst})^2(v_{gb} - v_{gst} - v_t + \phi)$$

$$(A7.2.4)$$

Similarly, including  $v_{sb}$  dependence of *Abulk* for the first order conserved channel power as in Appendix A4.3,  $P_{c1,cons}$  becomes

$$P_{c1,cons}\Big|_{Abulk(v_{sb})} = \frac{1}{6Abulk(v_{gdt} + v_{gst})^2} (c_{ox}((v_{gdt} - v_{gst}))(v_{gdt}\frac{d}{dt}v_{gdt}(3v_{gdt} + 5v_{gst})) + (a_{dt}v_{gdt}(3v_{gdt} + 5v_{$$

Equations (A7.2.4) and (A7.2.5) can now be combined to get the new first order conserved power

$$P_{1,cons}\Big|_{Abulk(v_{sb})}$$
 that includes the dependence of Abulk on  $v_{sb}$ . In terms of energy, the new

first order conserved power can be represented as:

$$P_{1,cons}\Big|_{Abulk(v_{sb})} = \left(\frac{\partial E_c}{\partial v_{gb}} + \frac{\partial E_g}{\partial v_{gb}}\right)\frac{dv_{gb}}{dt} + \left(\frac{\partial E_c}{\partial v_{db}} + \frac{\partial E_g}{\partial v_{db}}\right)\frac{dv_{db}}{dt} + \left(\frac{\partial E_c}{\partial v_{sb}} + \frac{\partial E_g}{\partial v_{sb}}\right)\frac{dv_{sb}}{dt}$$
(A7.2.6)

which can be solved to get  $\frac{\partial E}{\partial v_{jb}} \left(= \frac{\partial E_c}{\partial v_{jb}} + \frac{\partial E_g}{\partial v_{jb}} where \ j = g, d, s\right)$  from the coefficients of  $\frac{dv_{jb}}{dt}$ .

Finally the second order partials can be checked for the validation of energy function as done in previous sections.

$$\frac{\partial}{\partial v_{db}} \left(\frac{\partial E}{\partial v_{gb}}\right) = \frac{\partial}{\partial v_{gb}} \left(\frac{\partial E}{\partial v_{db}}\right)$$
(A7.2.7)

$$\frac{\partial}{\partial v_{sb}} \left(\frac{\partial E}{\partial v_{gb}}\right) \neq \frac{\partial}{\partial v_{gb}} \left(\frac{\partial E}{\partial v_{sb}}\right)$$
(A7.2.8)

$$\frac{\partial}{\partial v_{db}} \left(\frac{\partial E}{\partial v_{sb}}\right) = \frac{\partial}{\partial v_{sb}} \left(\frac{\partial E}{\partial v_{db}}\right)$$
(A7.2.9)

From (A7.2.7) to (A7.2.9), it can be seen that the second order partials are not equal due to  $v_{sb}$  dependence. This verifies that the BSIM capacitive model has no energy function for all of the conserved components. The difference results in extra dissipation in the channel that has no physical significance and is given by

$$P_{1,cons}\Big|_{Extra} = (P_{c1,cons} + P_{g1,cons})\Big|_{Abulk(v_{sb} \neq 0)} - (P_{c1,cons} + P_{g1,cons})\Big|_{Abulk(v_{sb} = 0)}$$

# A7.3 BSIM current and charge equations

The gate, bulk, drain and source charges are given by [6.4]

$$\begin{split} & \mathcal{Q}_{g} = Lc_{ox} \left( v_{gb} - v_{sb} - v_{fb} - \phi - \frac{(v_{db} - v_{sb})}{2} + \frac{Abulk(v_{db} - v_{sb})^{2}}{12 \left( v_{gst} - \frac{Abulk(v_{db} - v_{sb})}{2} \right)} \right) \\ & \mathcal{Q}_{b} = Lc_{ox} \left( v_{fb} - v_{t} + \phi - \frac{(1 - Abulk)(v_{db} - v_{sb})}{2} - \frac{(1 - Abulk)Abulk(v_{db} - v_{sb})^{2}}{12 \left( v_{gst} - \frac{Abulk(v_{db} - v_{sb})}{2} \right)} \right) \\ & \mathcal{Q}_{d} = -Lc_{ox} \left( \frac{\frac{v_{gst}}{2} - \frac{Abulk(v_{db} - v_{sb})}{2}}{4bulk(v_{db} - v_{sb}) \left( \frac{\frac{v_{gst}}{2} - \frac{Abulk(v_{db} - v_{sb})}{2}}{6} - \frac{Abulk v_{gst}(v_{db} - v_{sb})}{8} + \frac{Abulk^{2}(v_{db} - v_{sb})^{2}}{40} \right) \\ & + \frac{\left( v_{gst} - \frac{Abulk(v_{db} - v_{sb})}{2} \right)^{2}}{\left( v_{gst} - \frac{Abulk(v_{db} - v_{sb})}{2} \right)^{2}} \end{split}$$

The currents can then be derived from the time derivatives of the charges using

$$i_{gb,B} = \frac{d}{dt}Q_{g}$$
$$i_{db,B} = \frac{d}{dt}Q_{d}$$
$$i_{sb,B} = \frac{d}{dt}Q_{s}$$

where  $i_{gb,B}$ ,  $i_{db,B}$  and  $i_{sb,B}$  are first order BSIM gate, drain and source currents respectively. These current includes the extra components due to the source dependence of the BSIM bulk charge parameter.

### VITA

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Title of Study: FIRST ORDER QUASI-STATIC MOSFET CHANNEL CAPACITANCE MODEL

Pages in Study: 96 Candidate for the Degree of Doctor of Philosophy

Major Field: Electrical and Computer Engineering

Scope and Method of Study:

Conventional MOS models for circuit simulation assume that the channel capacitances do not contribute to net power dissipation. Numerical integration of channel currents and instantaneous terminal voltages however shows the existence of first order dissipating terms. To overcome these limitations, and given that the accuracy of the simulation depends on the physical representation of the device, it is very important that we have a reliable mathematical model that is able to represent the device behavior. Designers need these accurate models for circuit development.

Findings and Conclusions:

To overcome the limitation of conventional charge based models, a self-consistent, first order, quasi-static, power dissipation model has been developed that is able to

- Predict the exact solution to first order 1-D channel equations for MOSFETs without a channel charge partition approximation provided that the charge has a linear dependence on the channel potential.
- Validate the terminal currents as being the same as Ward's channel charge partition approximation.
- Validate that Ward's partition scheme is correct as long as the charge has a linear dependence on the channel potential.
- Derive the first order channel charge  $(q_{c1})$  and current  $(i_{c1})$  as a function of position (x) inside the channel.
- Derive the first order power dissipation and conserved components.
- Estimate energy function.
- Separate the terminal current into conserved and dissipative components.
- Identify the inconsistencies in the BSIM power model.

In conclusion, there is a need to extend this work to include channel charge with a non-linear voltage dependence that does not generate extra power dissipation in the channel that has no physical basis.

ADVISER'S APPROVAL: Dr. Louis G. Johnson