A LOW POWER LOW MODULATION INDEX ASK DEMODULATOR DESIGN FOR RFID APPLICATIONS

By

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Abstract: In the era of the Internet of Things (IoT) there is a tremendous increase in portable wireless devices utilized in our day to day working. One such example is the Radio Frequency Identification tag. The primary challenge in designing passive RFID tags is reliable functionality over extreme temperature and environmental conditions with low power operation. An important component of the RFID tag architecture is the demodulator which is tasked with interpreting the incoming data and extracting the reference clock for the Phase Locked Loop. A novel ASK demodulator architecture that functions across a temperature range of -25℃ to 125℃ is designed, analyzed and optimized for the worst and best case semiconductor process variations. The incoming RF frequency is selected as 900MHz based on the EPC GEN2 protocol and the baseband signal is set at 450 KHz with a modulation index of 5%. MOS transistor operation and variability in semiconductor processes is explored and a better understanding of how these concepts effect and shape our design decisions is established. A design objective is setup and steps to achieve these design objectives are presented. The design of the ASK demodulator is completed with the help of the Cadence Virtuoso tool, utilizing the IBM 0.18µm (CMOS 7RF) process. In order to test our design we have used the Monte Carlo analysis and all the significant DC parameters of the design have been tested for 10,000 samples owing to the high variability associated with modern semiconductor processes. On the other hand Monte Carlo simulations for the transient simulations have been done for 30 samples in accordance with the Central Limit Theorem. The results of the design are compared with other ASK RFID demodulator designs in the past and a comparison is made by utilizing a Figure of Merit from literature. The design is among the best ASK demodulator designs found in literature. Throughout this effort there is emphasis on MOS transistor operation and variations in semiconductor processes. The design takes all pertinent challenges such as extreme temperature, environment conditions and the reliability of the design. Through this work an attempt is made to try and simplify the work of the reader and expose them to the challenges associated with ASK demodulator design.

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CHAPTER I

INTRODUCTION

1.1 INTRODUCTION to IoT

The term IoT refers to the Internet of Things which is a term used to describe the advent of the innumerous wireless systems that are connected to the internet. The Internet of Things has a bright future and will be ubiquitous in the near future [6]. The growth of the internet of things is revolutionary and the number of devices connected to the internet grew to 12.5 Billion in the year of 2010 while the world population at that time was about 6.8 Billion, which implies that the number of connected devices per person was more than 1(≈2) at the time. In the future it is predicted that the number of devices connected to the internet should approach 50 Billion in the year 2020 while the population would be approximately 7.6 Billion[7]. This trend suggests that these IoT devices are going to not only outnumber the number of human beings but will be commonplace. One such example is the Apple watch which has instant internet connection on the go, other applications of such devices include[8]:

- Medical- monitoring, safety and quality control
- Personal wearables with real time medical assistance
- Industrial Robots and automation

- Supply Chain-Real time data analysis
- Infrastructure integrity monitoring systems-road and railway transportation
- Homes-Cameras, HVAC, lighting and security.

With so many devices simultaneously accessing the internet there is going to be a crunch in the spectrum available for these devices to communicate hence the communication would need some sort of data distribution network. With greater data rates and an with increase in distances of transmitted data the expenditure of power is going to be extremely high.

In designing IoT devices there is a great emphasis of low power consumption. Lower power consumption extends the battery life of these devices and their usable lifetime increases. These IoT devices have to function satisfactorily in extremes of temperature and environment conditions, as the temperature of the environment increases the semiconductor chips in these devices heat up leading to addition power loss. For the commercial IoT market, the devices have to be designed in order to function efficiently for a temperature range of 0℃ to 90℃ whereas wireless microsystems that find applications in the military or the automotive industry need to perform satisfactorily for a temperature range of -40℃ to 150℃.

1.2 INTRODUCTION TO RFIDs

The numerous IoT devices on the market includes the Radio Frequency Identification (RFID) tag. RFIDs find widespread applications such as object tracking, identification, inventory, data loggin, and supply chain management and data acquisition. RFIDs first found their bearings in the 1970s and since then have evolved to a great extent [9].

These RFID devices are classified into two categories

- Active RFID
- Passive RFID

Active RFID consist of on-chip integrated power source (battery). The luxury of an internal battery improves performance significantly. The drawback of having an internal battery is that these devices have a limited life time, cost more and are less bio compatible. The on-chip battery ensures that there is an abundance of power that can be utilized by the tag for its functioning. Due to the abundance of battery power the communication range for active RFIDs is >100m.

Just the opposite is true of their active counterpart, passive RFIDs have no internal battery and must harvest the power from an input RF signal, solar, acoustic or thermal source for the entire time that they are operational. This stipulation of not having an on-chip battery means that there is a scarcity of available power which the tag can utilize for not only function, i.e. data acquisition and/or storage but also for communicating. Passive RFIDs are smaller in size, have a greater life span and are safer for bio-implantation, and generally lower cost which tips the scales in its favor. However, passive RFIDs are generally limited to near field communication and may extend to a few meters. The drawbacks of using passive RFIDs is that there is greater emphasis on low power consumption, and near field operation. Hence each block in the circuit architecture must be optimized for low power consumption. This is often challenging. This work is limited to passive RFIDs and throughout this effort there will an emphasis on low power design techniques.

1.3 Ultra-Low Power Requirement Dictates Weak Inversion

The complete block diagram of a passive RFID is shown in Figure 1.1

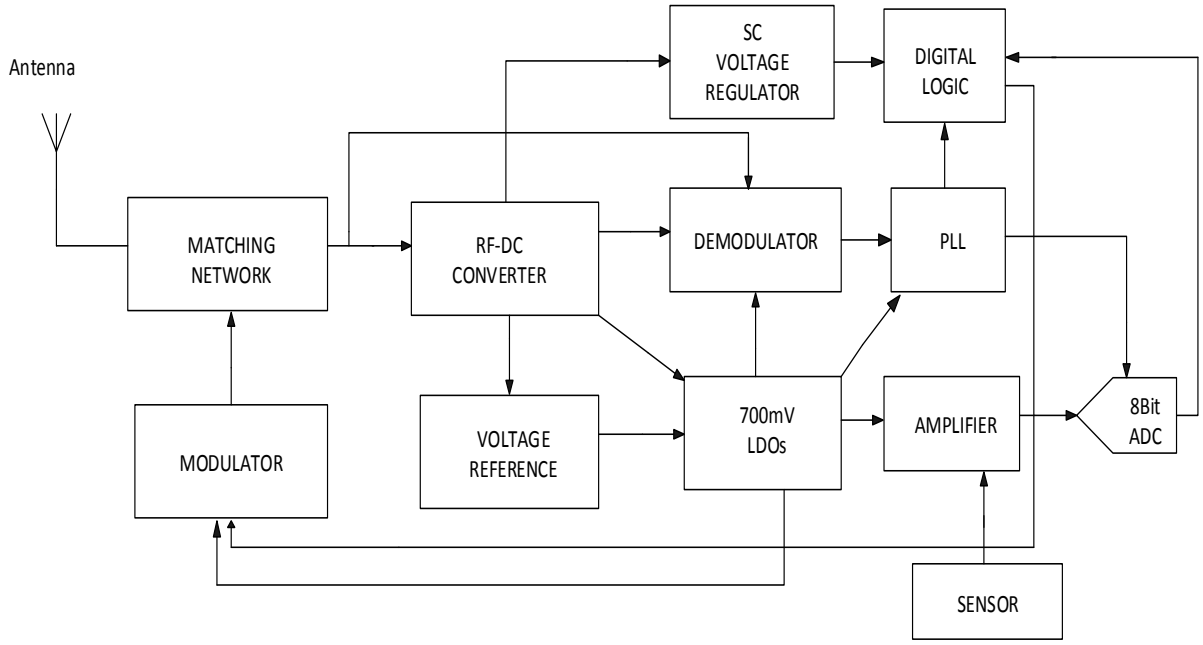

Figure 1.1 Complete Block Diagram of a "smart" RFID tag

As we can see there are many active blocks that may consume large amounts of power such as the Amplifier, Analog to Digital Converter, Voltage Reference, Demodulator, Phase Locked Loop, Low Dropout Regulator, etc. The greatest power offenders include the Low Dropout Regulators, Demodulator, Voltage Reference circuits, Analog-to-Digital converter and the amplifier. It is therefore imperative that each of these blocks are designed in such a manner that their overall power consumption is as efficient as possible. Such low power operation can be achieved by choice of circuit architectures and region of operation (weak inversion). Weak inversion operation benefits us by affording us greater bandwidth per watt compared to strong inversion. The time constraints on the RFID operation is relaxed as the bandwidth requirement of the physical world enables us to opt for weak inversion operation.

The concept of weak inversion and its low power capability is elaborated in Chapter 2. The average input power to an RFID is dependent on the modulation scheme used, for most passive RFIDs the most prevalent modulation scheme is the Pulse interval encoding scheme.

1.4 Pulse Interval Encoding

The protocol widely used for passive RFID tags that incorporate backscatter is EPC GEN 2, which is the protocol that was standardized by EPCglobal for passive RFIDs. All passive RFID devices that incorporate the EPC Gen 2 have to conform to a minimum set of rules or minimum standards. A detailed list of these requirements can be found in [10]. Pulse interval encoding is the encoding scheme preferred while communicating from the interrogator to a passive RFID tag in the EPC class-1 generation-2 UHF RFID protocol[10]. This is attributed to the fact the pulse interval encoding scheme maximizes the amount of power flow to the tag while communicating both binary 1's and 0's. The scheme is characterized by a long full power pulse for the binary 1 with a short power off pulse terminating it whereas the binary 0 starts with a short full power pulse and is terminated by the same short power off pulse[11]. The PIE baseband waveform is shown in Figure 1.2. The term Tari is an abbreviation of Type A Reference Interval. It is a unit of time duration that ranges from 6.35μs to 25μs and results in a communication bandwidth requirement approaching 1.5 MHz. The time duration for which the binary 1 and 0 experience a power off pulse is between 0.265 Tari and 0.525 Tari [4].

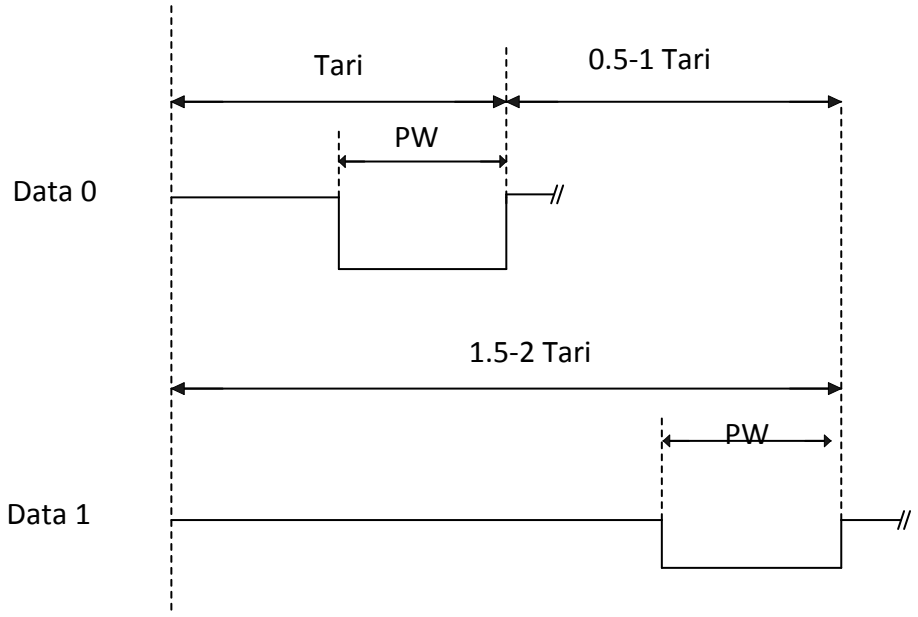

Figure 1.2. Baseband waveform of Pulse Interval Encoding[11]

One of the drawbacks of the scheme is that the data rate is data-dependent since the duration for binary 0 is shorter than the duration for a binary 1. The worst case in terms of power flow to the tag would be a series of binary 0s whereas the worst case data rate would be caused by a series of binary 1s. A series of 1s requires the greater bandwidth. To increase the average power to the RFID one possible solution is to reduce the modulation index of the incoming signal in order to increase the power levels for the binary 0s, this reduced modulation index imposes tighter specifications on the demodulator design which we would explore in detail in Chapter 4. Although the power at the input is increased, it is up to the matching and harvester circuits to make that input power available to the other parts of the RFID, we explore these circuits in the following sections.

1.5 Matching Network and Harvester Circuits

The front end circuit of the RFID is shown in Figure 1.2.

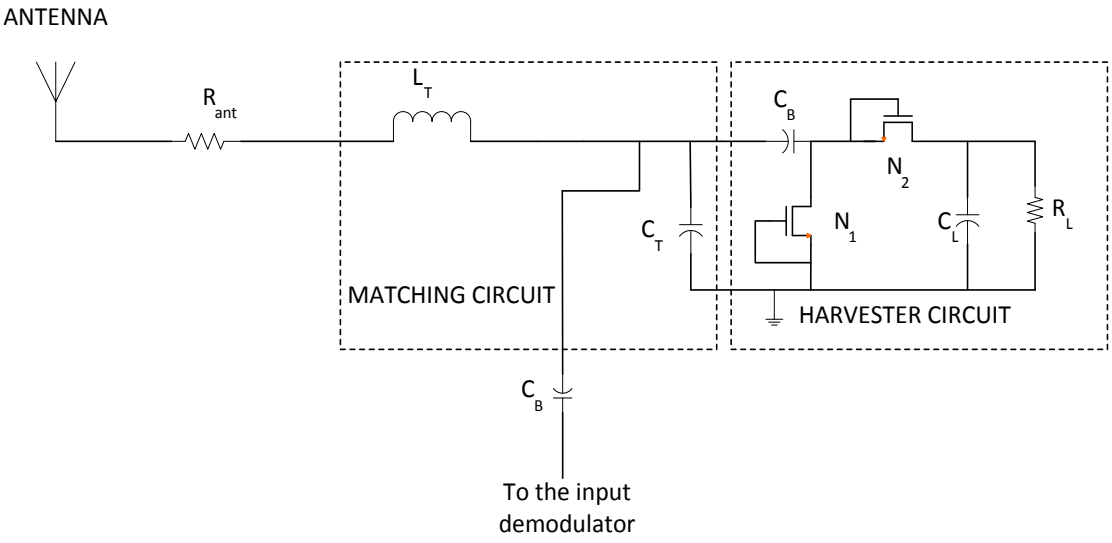

Figure 1.3 Front End Circuit of the RFID.

1.5.1 Matching Network

In order to maximizing harvesting of the power in the input RF signal we need to match the source impedance of the antenna to the input of the RFID in order to have maximum power transfer to the input of the harvester. Series matching is selected since it provides us with a voltage boost equal to the Q of the network [12]. This means that the incoming waveform voltage is multiplied by the Q of the matching circuit and the input to the harvester is now $V_{IN,HAR} = Q * V_{IN}$. The choice of series matching topologies is limited to the T, π and the L match networks to minimize complexity. The L match is the preferred choice since it offers greater efficiency compared to the T and the π [13] while presenting a voltage boost. The equivalent circuit for the matching network is shown in Figure 1.4.

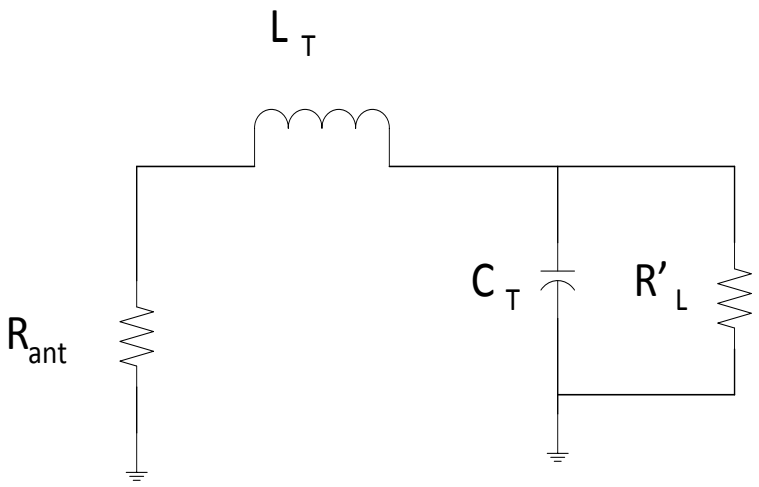

Figure 1.4 L match network

We need to match the R_{ant} in series with the inductor impedance X_L to the parallel impedance of R'_L and X_C.

$$R_{ant} + jX_L = \frac{1}{\frac{1}{R'_L} + \frac{1}{jX_C}}$$

$$Q_s = \frac{X_L}{R_{ant}} = \frac{{R'_L}^2 X_C}{R'_L X_C^2} = \frac{R'_L}{X_C} = Q_p = Q$$

Q_s is the quality factor of the inductor L_T whereas Q_p is the quality factor of the capacitor C_T

Solving Further

$$Q = \sqrt{\frac{R'_L}{R_{ant}} - 1} \approx \sqrt{\frac{R'_L}{R_{ant}}} \approx \sqrt{\frac{R_L}{R_{ant}}} = \sqrt{\frac{V_{Har}/I_{DC}}{R_{ant}}}$$

A higher Q is advantageous to the RFID operation yet the communication bandwidth limits the maximum applicable Q [12]. The values for V_{Har} and I_{DC} are known, as a result the R_{ant} value is adjusted in order to match the antenna to the load. For the EPC GEN 2 standard the

communication Q around 0.9 to 2.5 GHz approaches 30 to 80. This is effectively reduced to (25→66) by the process variation of +/- 20% in the tuning capacitance, C'_T

Resonant frequency is given by:

$$f_0 = \frac{1}{2\pi\sqrt{L_T C'_T}}$$

The choice of the load capacitor value is application dependent. The matching network design is not part of this effort hence we do not discuss it any further though a good reference can be found in [12]. As a result acceptable Qs may range between 6→25 at 900 MHz.

1.5.2 Harvester Circuit

The incoming RF wave has to be converted to DC power in order to power the entire RFID, for which there is a need for a rectifier. The overall power efficiency of the harvester circuit is critical as it directly impacts the performance of the entire RFID.

Harvester Working:

A more general/simplifed depiction of the harvester is shown in Fig 1.6.

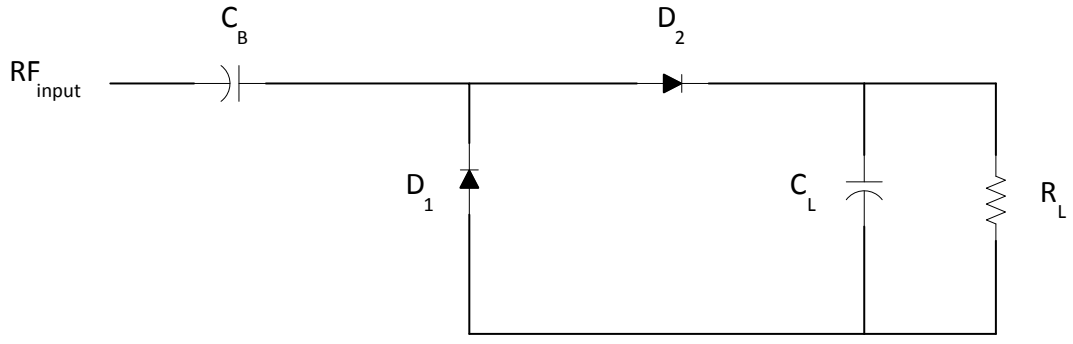

Fig 1.5 Basic Harvester Circuit

In the negative half cycle of the input waveform the diode D_1 becomes forward biased and conducts current which charges the capacitor C_B to V_{peak} (peak voltage value of the RF waveform), during this time the diode D_2 remains in the reverse biased mode and is off. This phenomenon is shown in Figure 1.6

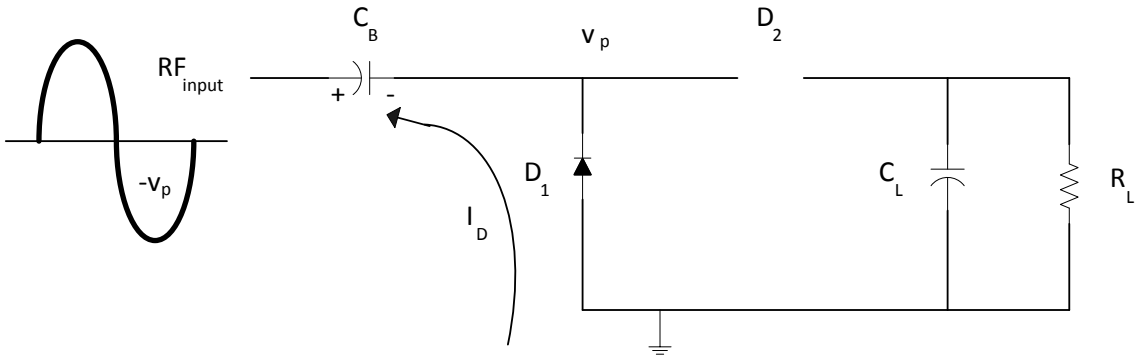

Figure 1.6 Negative half cycle of the input at the Harvester

On the positive half cycle of the input the reverse takes place where the diode D_2 is on and the diode D_1 shuts off. Diode D_2 would charge the load capacitor C_L to $2V_{peak}$, as the initial voltage at the capacitor was already V_{peak} at the moment the input waveform turned positive, it is added to the V_{peak} value of the incoming input to charge up to $2V_{peak}$. This occurrence is presented in Figure 1.7

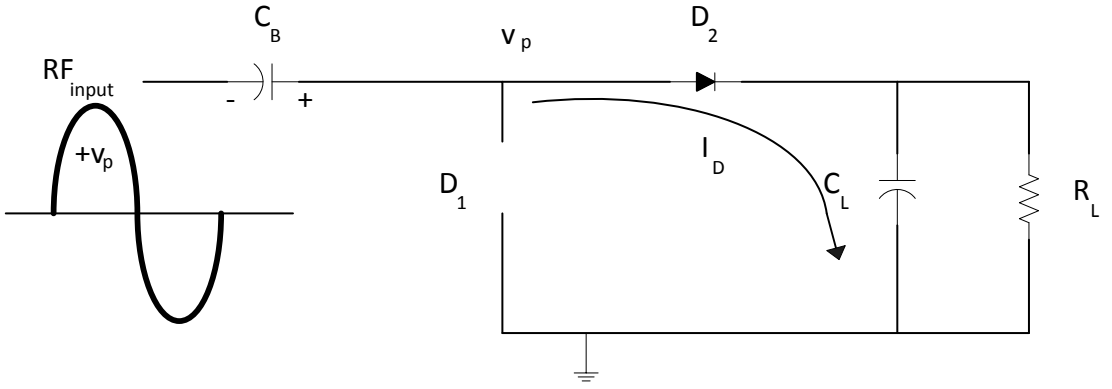

Figure 1.7 Positive half cycle of the input at the Harvester

The voltage output for N stage harvester circuit is given by

$$V_0 = 2N(V_P - V_d)$$

Where V_d is the total voltage drop due to the diode losses, LDO losses and parasitic losses at the carrier frequency and V_P is the peak amplitude of the incoming signal.

The design of the harvester circuit is not undertaken in this effort, complete design and optimization of the harvester can be found in [14], LDO loss numbers can be found at [15]. The output voltage of the harvester is assumed to be at 1V with a DC or average load current of 50µA hence the load resistor at the output of the harvester is given by

$$R_L = \frac{V_0}{I_L} = 20K\Omega$$

As seen in Figure 1.1 and 1.2 the demodulator and the harvester share the same input node which is the output node of the matching network, this implies that we need to ensure that the demodulator does not load the harvester output causing the output harvester voltage to reduce. A reduction in the harvester output voltage reduces the harvester power efficiency. It is important that the impedance looking into the demodulator is greater than approximately $20*R_L$ such that the demodulator has little or no effect on the performance of the harvester. Alternately stated dissipates insignificant power. This constraint has a direct impact on the design of the ASK demodulator effort presented in Chapter 4.

1.6 Research Objective

Demodulation is a process in which the digital baseband data is extracted from a modulated analog waveform which is at a higher frequency called the carrier frequency[11]. The demodulator is a vital cog in the circuit architecture of the RFID as it is responsible for faithfully reproducing the input signal RFID commands which control the RFID state machine. The

modulated input contains the clock embedded within it, and the demodulator has the task of decoding the data stream bit s(0 or 1) and in turn providing the embedded reference clock to the PLL. This effort is aimed at designing a power efficient low modulation index Amplitude Shift Keying (ASK) demodulator for RFID applications for a temperature range of -25℃ to 125℃ making use of a voltage supply of 700mV. For the design, the IBM CMOS7RF 0.18µm process is used and simulations are carried out using Cadence Virtuoso. Design objectives are presented and all design trade-offs and challenges are stated, steps to overcome them are demonstrated and an analytical approach to designing and optimizing the RFID Demodulator is presented. Throughout this effort there is emphasis on the operation of the MOS transistor in subthreshold region and the effects of change in temperature and process on transistor operation. The primary aim of this effort is to design a robust ASK demodulator for extreme of temperature conditions consuming minimum power. The designed ASK demodulator is compared with similar works by using a Figure of Merit[5].

1.7 Thesis Organization

In Chapter 1 the motivation for low power consumption was established, the circuits interacting with the ASK Demodulator were summarized along with their implications on the ASK demodulator design and finally the research objective of this effort was put forth.

Chapter 2 introduces subthreshold/weak inversion design and the effect of process and temperature variation on MOS operation. The chapter then goes on to describe supply voltage variation and concludes by establishing PVT (process, temperature and supply) corners for MOS transistors in weak and strong inversion regions of operation.

Chapter 3 will look at ASK demodulators for RFID applications implemented in the past and make a comparison table which would be used in Chapter 6 to put together a Figure of Merit.

Chapter 4 introduces the designed RFID demodulator and its working and goes on to establish a design objective and discusses the steps taken to achieve such an objective.

Chapter 5 will consist of the circuit simulations results and the DC Monte Carlo simulation results along with the transient working results of the circuit.

Chapter 6 will first look at possible parameters that should be considered towards establishing a Figure of Merit and will go on to establish such a Figure of Merit [5]. Concluding this effort the chapter will look at the Future Scope in an effort to identify best opportunities for improving efficient power usage on a block by block bases.

CHAPTER II

MOS TRANSISTOR CHARACTERISTICS AND VARIABILITY

This chapter is divided into three sections, the first section would introduce subthreshold operation of the MOS Transistor, and second section would explain in detail the origins of process variation and their consequences and the third section would explore temperature effects in subthreshold and velocity saturation on MOS operation.

2.1 Subthreshold/Near Threshold Designing

In our discussion of the MOS transistor we are going to be utilizing elements of both the EKV model and the BSIM3v3 model to understand the working of the transistor in various regions of operation. Conduction of current in MOS transistor takes places in two ways, one is through drift and the other through diffusion of charge carriers, the drift currents are dominant in the strong inversion regime while the diffusion current is associated with the weak inversion regime [16]. There are many models used to characterize the behavior of the MOS transistor such as the BSIM3[16] model which is a surface potential based model whereas the EKV model is a charge based models. In our discussion about subthreshold operation we are going to use the EKV model to illustrate subthreshold operation. The MOS transistor operation has three modes of operation when the channel is inverted i.e. weak, moderate and strong inversion operation.

The EKV model is a body referenced model which is useful in order to model the MOS transistor operation in weak inversion [16]. These modes of operation are classified based on the inversion coefficient which is defined by [17] as

$$IC = \max\left(i_f = {I_F}/{I_{spec}}, i_r = {I_R}/{I_{spec}}\right)$$

I_F is the forward current in the channel, I_R is the reverse current and I_{spec} is the specific current which is given by $I_{spec} = 2n\,\mu C_{ox}\frac{W}{L}\,U_T^2$ the current used to normalize I_F and I_R at the current level at which I_F or $I_R$changes from weak to strong inversion[17]

Weak inversion takes place for IC<<1, moderate for IC≅ 1 and strong inversion for IC>>1. Fig 2.1 shows the plot of log of the inversion charge vs the gate-to-body voltage in a two terminal MOS structure which establishes the notion of the threshold voltage[16]. Where V_{M0} is the extrapolated voltage that represents the onset of moderate inversion and V_{H0} the onset of strong inversion. V_{GB} is the gate-to-body voltage in a two terminal structure and Q_I is the inversion layer charge. The extrapolated threshold voltage V_{T0} (ignoring the body effect) is the voltage for which the MOS transistor is said to turn on based on the strong inversion model. Moderate inversion is not well modelled as both weak and strong inversion model fail as the current flowing through the transistor in moderate inversion constitutes both drift and diffusion currents. In a four terminal MOS device subthreshold operation is considered to take place when the gate-to-source bias on a MOSFET is lower than the extrapolated threshold voltage of that MOSFET. This means that any MOS transistor biased below its threshold voltage is said to operate in the subthreshold regime. In terms of regions of inversion subthreshold operation spans weak inversion and part of the moderate inversion regime of operation. A much simpler depiction is presented in Fig 2.2 which plots the ln of the drain current v/s the gate-to-source voltage of a MOS transistor for a source referenced model.

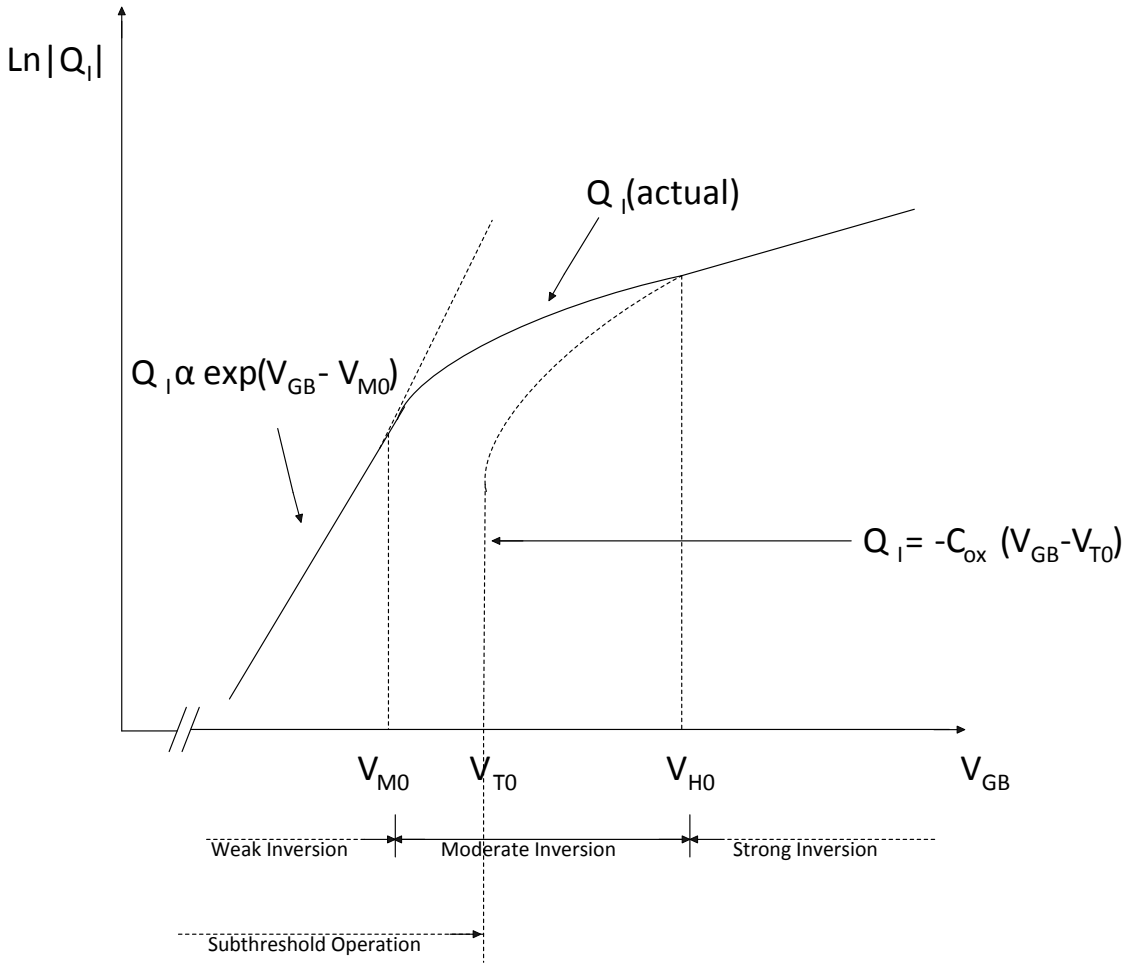

Fig 2.1. Log of inversion layer charge vs the gate-to-body voltage for a two terminal MOS device[16]

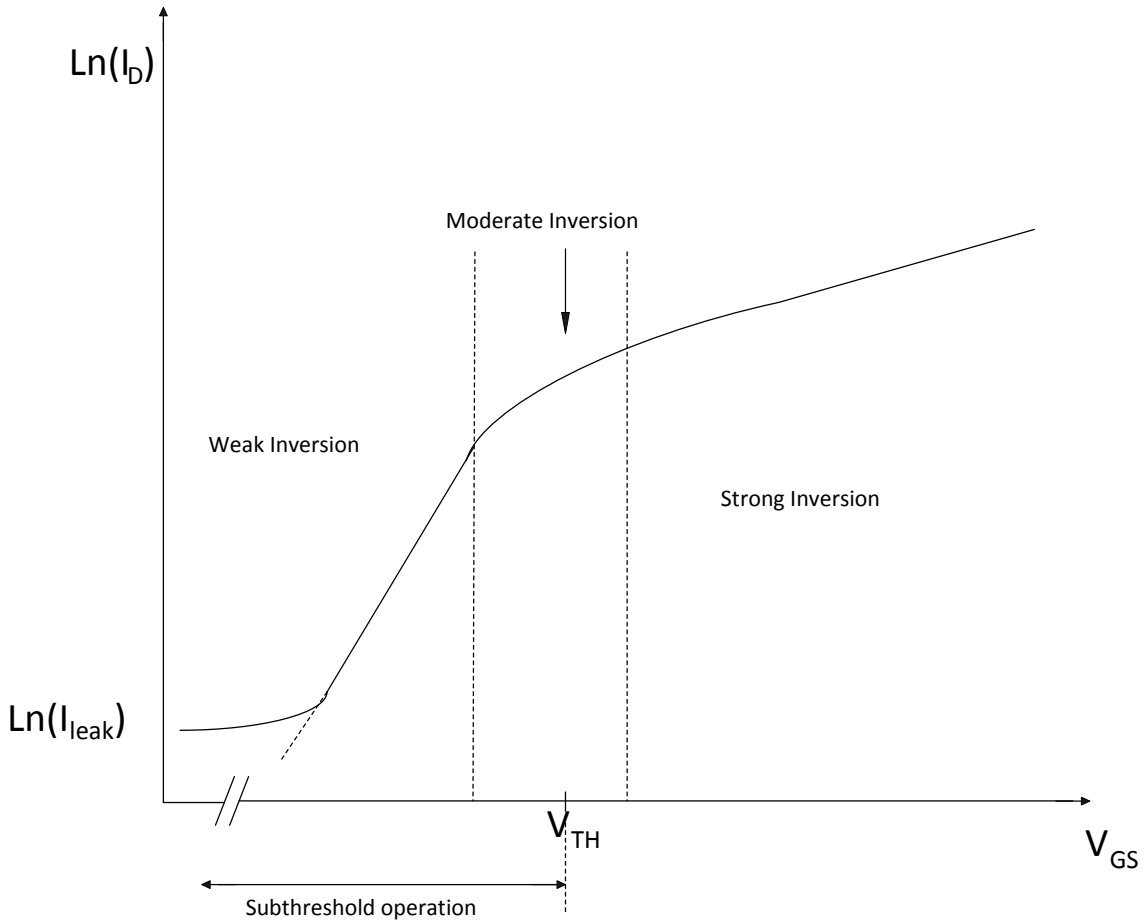

Fig 2.2 $\ln(I_D)$ $vs\ V_{GS}$ plot

The following sections will evaluate performance in the subthreshold regime by stating the advantages, disadvantages and limits of designing circuits in the subthreshold region.

The drain current equation in weak inversion is given by[17] as

$$I_D = I_S e^{\frac{V_G - V_{T0}}{nU_T}} \left(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right)$$

And can be approximated [11]as

$$I_D = I_{D0} e^{\frac{V_{GS} - V_T}{nU_T}} \left(1 - e^{\frac{-V_{DS}}{U_T}} \right)$$

2.1.1 Advantage of Operating in Subthreshold Region

High gm/ID efficiency: When the MOS transistor operates in the subthreshold region the $^{g_m}/_{I_D}$ is higher than that for above threshold operation where the $^{g_m}/_{I_D}$ saturates for high gate-to-source voltages. The gm/ID efficiency for a single finger minimum geometry diode connected NMOS device is shown in Fig 2.3. As seen in Fig 2.3 the gm/ID efficiency reduces as the gate-to-source voltage is increased above threshold. The threshold voltage of transistor is at 426mV at 27℃. Around the threshold voltage the gm/Id efficiency is about 18 while it reduces to 9 at 100mV above threshold and to 5 at 200mV above threshold. A higher gm/Id efficiency translates to a higher achievable gain for a lower drain current. The power consumed by an analog circuit is given by$Power = V_{DD} * I_D$, hence a lower drain current implies the power consumption would be lesser compared to above threshold design for the same gain.

Low Power Consumption: Considering digital circuits it is beneficial to operate circuits in the subthreshold or near subthreshold region for low power consumption while providing the required bandwidth. The latest technologies have ample bandwidth at their disposal and to incorporate subthreshold designs in order to reduce power consumption. This concept is explained through the equation for total power consumption.

The total power consumption is given by

$$P_{Total} = P_{static} + P_{static}$$

$$P_{Total} = V_{DD} * I_{leak} + C * V_{DD}^2 * f$$

$$P_{Total} \alpha I_{leak} + C * V_{DD} * f$$

Where f is the operating frequency and C is the capacitance that is charged or discharged. The term I_{leak} is the current flowing through the device when the device is said to be off. If we were to operate in subthreshold the contribution to the total power would be dominated by the static power which is a linear function of the supply voltage whereas the dynamic power is a quadratic function of the supply voltage, hence dynamic power makes a negligibly contribute to the overall power. Subthreshold design consumes low power for the required bandwidth, hence most passive RFIDs these days operate in the subthreshold region as the bandwidth achievable in weak inversion is feasible.

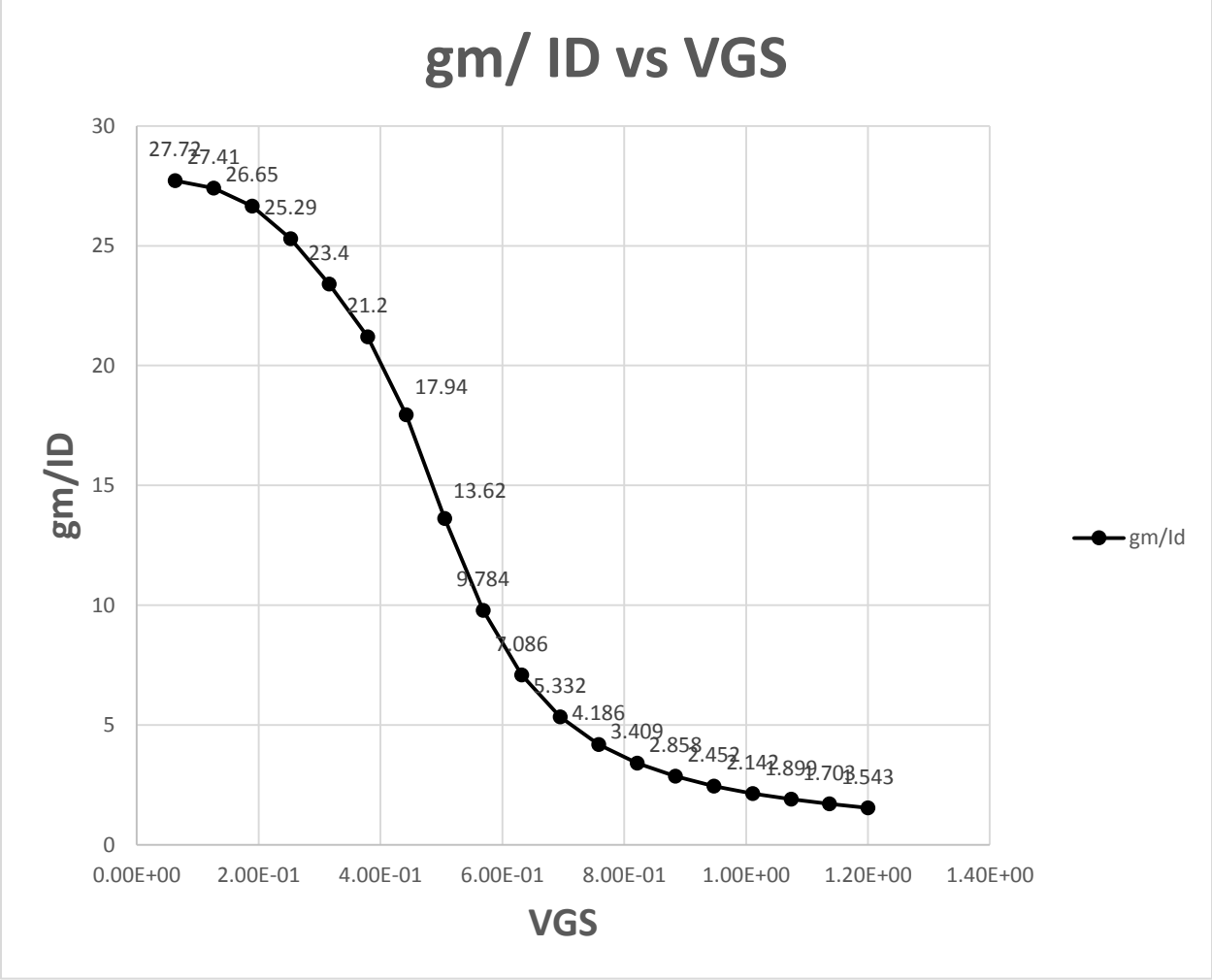

Figure 2.3. $^{gm}/_{I_D}$ vs V_{GS} plot

2.1.2 Drawbacks of Operating in Subthreshold Region

Low Bandwidth: Subthreshold operation is helpful in reducing the power consumption but the frequency of operation is drastically reduced compared to operating above threshold. The bandwidth achievable in the weak inversion regime is lower than that achievable in strong inversion as seen in Figure 2.4, although we are able to achieve a high gm/ID efficiency the magnitude of currents produced are fairly low causing the bandwidth of operation to be low. The transition frequency vs gate-to-source voltage for a minimum geometry diode connected NMOS is shown in Fig 2.4. The transition frequency rises rather abruptly as the gate-to-source voltage is increased beyond the threshold voltage. Since the bandwidth of operation required for passive RFID applications is fairly low, subthreshold operation is still a viable option.

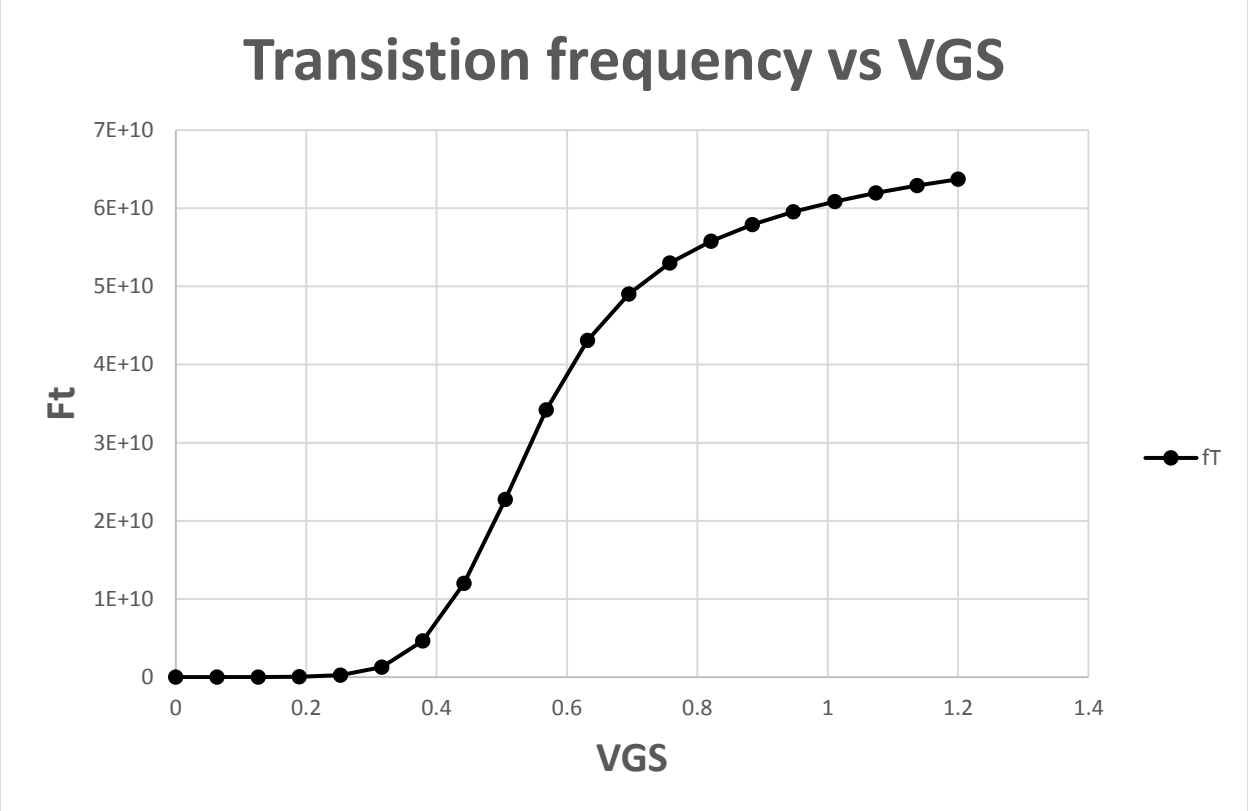

Fig 2.4. Transition frequency vs gate-to-source voltage for a diode connected NMOS transistor.

High Variability**:** The variability associated with the current is high due to the fact that the current is an exponential function of the threshold voltage in weak inversion. The threshold voltage of the device is highly variable and will be discussed in Section 2.2 in detail.

2.1.3 Subthreshold Operating Limits

When dealing with subthreshold design it is important to ensure that the I_{ON}/I_{OFF} ratio is high. This condition ensures that the active drain current used for circuit operation is much greater than the off state leakage current flowing through the device. If the off-state current is comparable to the on-state current, it could lead to a loss of state in a digital circuit and the circuit would not function as required. Also when operating in deep subthreshold ($V_{GS} << V_{TH}$) it is important to understand that as the gate-to-source voltage tends towards zero the model predicts that the drain current would also tend to zero yet the data provided by the IBM CMOS RF 7 0.18µm process shows that the leakage or off-state current is comparable to the drain current as shown in Fig 2.2. For the IBM 0.18µm process used for this effort the models incorporated in the simulator are BSIM3v3 or PSP intrinsic models. A designer needs to thoroughly understand the process and how it models the behavior of the MOS transistor in order to successfully predict and optimize any design effort.

2.2 PROCESS VARIATION

Every semiconductor chip applicaton (die) has specifications to achieve across extremes of temperature and environment conditions. Having said that a chip may be deemed a bad die if it is unable to meet the required specifications and the die may be destroyed or discarded. The semiconductor fabrication process is less than perfect, hence there is a standard deviation of the electrical parameters from their desired designed values. There are various sources of parametric variation associated with all semiconductor processes in general. These common sources of

variation are listed in Fig 2.5. The most important electric parameter of transistor in terms of variation is its threshold voltage, in this Sec we focus on transistor threshold variation caused by the process.

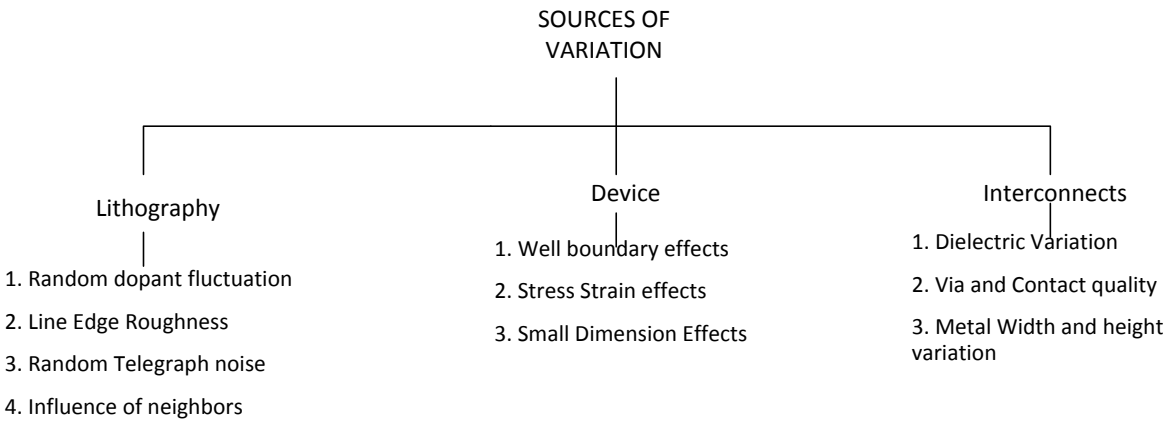

Fig 2.5. Sources of Variation[18]

2.2.1 Random Dopant Fluctuations

To get more performance out of transistors the industry has relentlessly followed Moore's Law by shrinking device dimensions every few years. The scaling of the device length and width causes a drastic reduction in the number of dopant atoms in the depletion region. For example considering W,L = 100nm for a device, the doping concentration is $N_A = 10^{18} cm^{-3}$ whereas the depletion width is 35nm, the number of acceptor atoms is given by $N = N_A * L * W_{Dom} = 350\ atoms$ [19]. At 32nm the number of dopant atoms is approximately 36. The extrapolated voltage expression for a two terminal device is given by[16].

$$V_{T0} = \emptyset_{ms} - \frac{Q_0}{C_{ox}} + \emptyset_0 + \frac{\sqrt{2q\epsilon_s N_A \emptyset_0}}{C_{ox}}$$

Where the gate to substrate work function is $\emptyset_{ms}$, Q_0 is the interface charge between the oxide and channel, q is the electron charge and $\emptyset_0$ is the surface potential. The number of dopants vary

from device to device and their standard deviation follows a Poisson's distribution due to its discrete statistical nature[19, 20]. Therefore the threshold voltage standard deviation due to random dopant fluctuations is given by[18] as

$$\sigma_{\Delta Vth} = \left(\sqrt[4]{2q^3\epsilon_{si}N_A\emptyset_0}\right) * \left(\frac{t_{ox}}{\varepsilon_{ox}}\right) * \frac{1}{\sqrt{3WL}} \cong \frac{A_{VT}}{\sqrt{WL}}$$

The threshold voltage is a continuous function and its standard deviation is modelled using a Normal distribution. The term A_{VT} is a constant referred to as the Pelgroms coefficient for the threshold voltage and is process technology dependent[21].

A small variation in this number can have substantial variation of electrical characteristics between devices which would ultimately lead to errors. Fig 2.6 shows the simulated RDF,LER by [19].

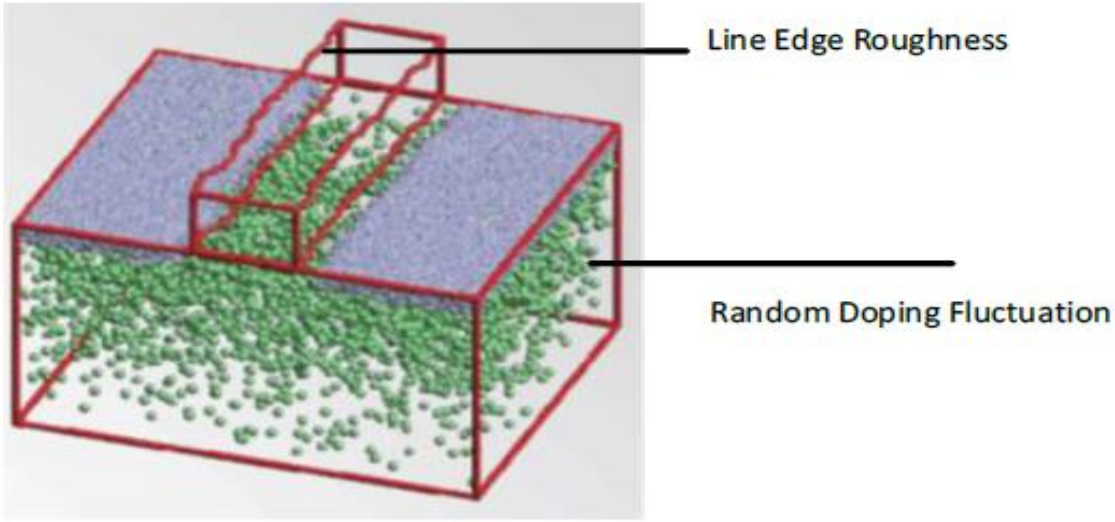

Fig 2.6. Atomistic simulation demonstrating RDF and LEF [18, 19]

The green spheres depict the dopant atoms. The effect of RDF on threshold voltage with change in device length is illustrated in Fig 2.7.

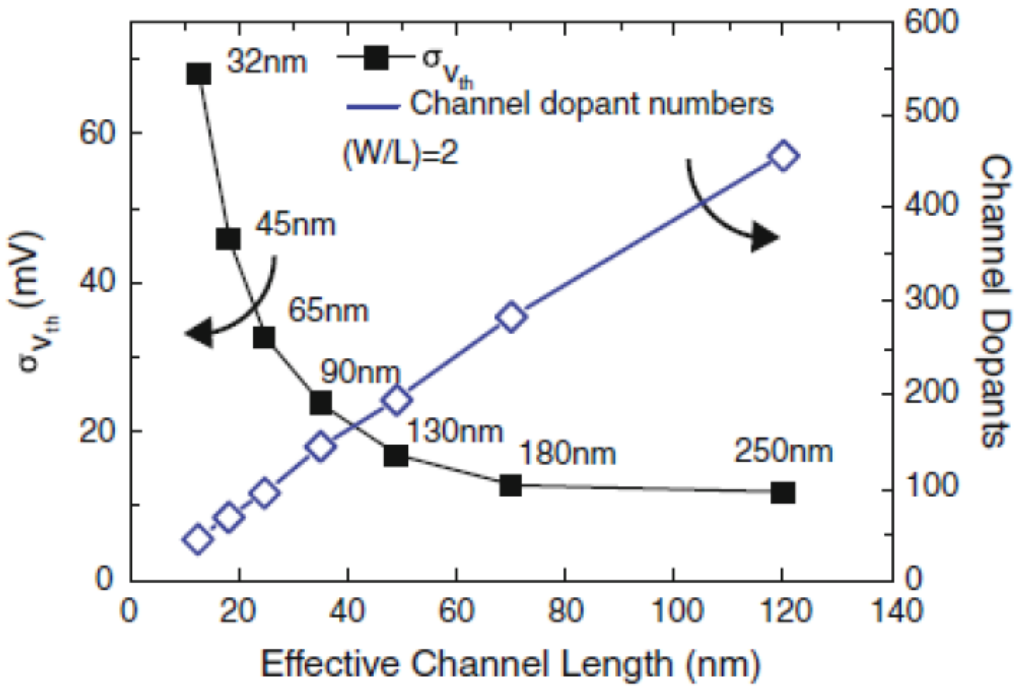

Fig 2.7. Impact of Random Dopant Fluctuation on σ_{VTH} with change in channel length [18, 19, 21-23]

2.2.2 Line Edge Roughness

Line edge roughness is caused due to improper patterning of the device dimensions such as the gate length. As the physical dimensions of the transistors is shrinking with every new process node the lithography wavelength has decreased from 500nm to 193nm for gate patterning. Optical lithography and enhancement techniques are used for process nodes 180nm and lower, these techniques employ aperture improvement using OPE (Optical Proximity effects) and immersion technology [18, 19, 24-26]. The optical proximity effects are major contributors to variation

which dictate the smallest feature size fabricated in a node generation. For process nodes below 50nm the LER is a significant contributor to the overall threshold variation [18, 19, 24-26]. Fig 2.8 shows the lithography wavelength for different process nodes.

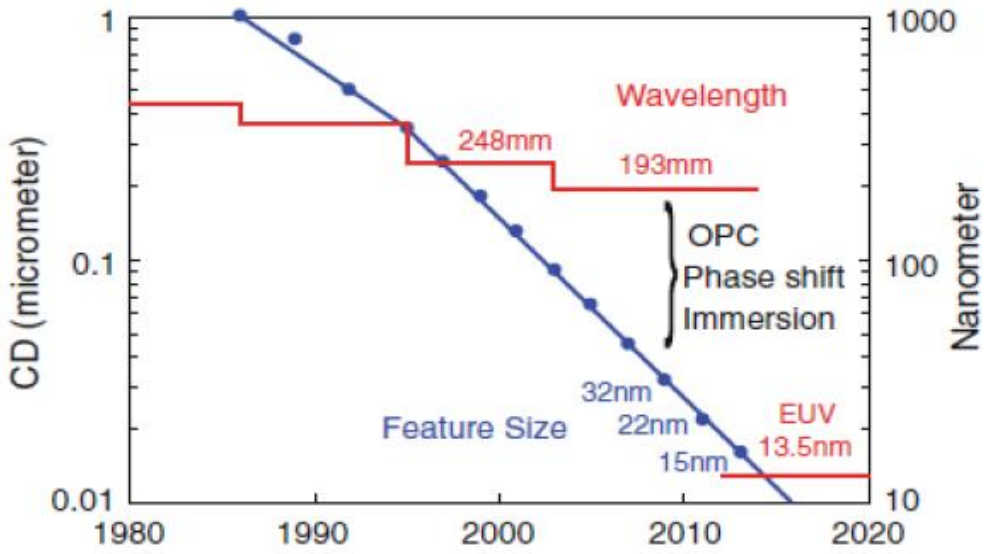

Fig 2.8. Lithography Wavelength for different process nodes[26]

2.2.3 Random Telegraph Noise (RTN)

Telegraph noise or flicker noise is not very well modelled, this noise or inaccuracy originates due to the scattering of the charge carriers in the channel. Since both the lateral and longitudinal fields effect the direction of carrier path, sometimes the carriers are trapped into the oxide region and accumulate there which reduces the overall channel charge effecting a higher threshold voltage. Once the amount of charge trapped in the oxide is extremely high, charge breaks free from the trap and all the previously trapped carriers are released leading to an increase in the surface potential causing a reduction in threshold voltage. This fluctuation of threshold voltage causes

many errors in the circuit and is modelled as a discrete statistical model. The impact of telegraphic or 1/f noise on the threshold voltage is given by [18, 27, 28]

$$\Delta V_{TH,1/f} = \frac{q}{W_{eff} * L_{eff} * C_{ox}}$$

RTN possesses a Gaussian long tail behavior which has critical implications beyond $\pm 3\sigma$ [19].

2.2.4 Influence of neighbors

Since Optical lithography is the primary method of lithography employed in the semiconductor industry there are many effects that are undesirable such as influence of the neighbors. In a die there may be many circuits designed that have their layouts in close proximity, the optical profile of one circuit can have an impact on the other adjacent circuit. Any variation in the lithography on one circuit can prove to be detrimental to the entire die. For this reason circuit layouts are isolated by either adequately spacing them apart or employing dummy circuits that are sacrificed in order to protect the circuits of requiring more significance[29] accuracy.

2.2.5 Small Dimension Effects

As we have seen the random doping is the prominent cause of variability when the dimensions of the width and the length of the transistors are small, there are other second order effects associated with the device dimensions that are process dependent and their effects vary from one process node to another. These effects include the Narrow Width, Inverse Narrow Width, Short Channel and Reverse Short Channel Effects.

- Narrow Width and Inverse Narrow Width Effect.

Modern CMOS sub-micron(below 0.25μm) processes often encounter the issues associated with the Narrow Width and the Inverse Narrow Width effects which are connected to the change of width of the device. When the width of the device has the same order of magnitude as the

depletion depth, that device is said to have a narrow width [30]. The Narrow Width Effect causes an increase in V_{TH} with a decrease in the width. This phenomenon is encountered often in processes that use non and semi recessed isolation such as the Local oxidization of silicon (LOCOS) CMOS process [30]. The LOCOS process was widely used for the processes having channel lengths of 0.25μm and greater [16]. For channel lengths 0.18µm and lower the processes usually use a Shallow-Trench Isolation (STI) which employs fully recessed isolation. The devices fabricated using the STI process encounter the Inverse Narrow Width effect wherein the V_{TH} decreases with the decrease in the channel width [31]. The IBM 0.18µm CMOS 7RF process is a CMOS STI process and encounters the Inverse Narrow Width effect[32]. To illustrate the same a plot of threshold voltage of a 1µm long NMOS transistor in the diode connected configuration vs change in width is shown in Fig 2.9.

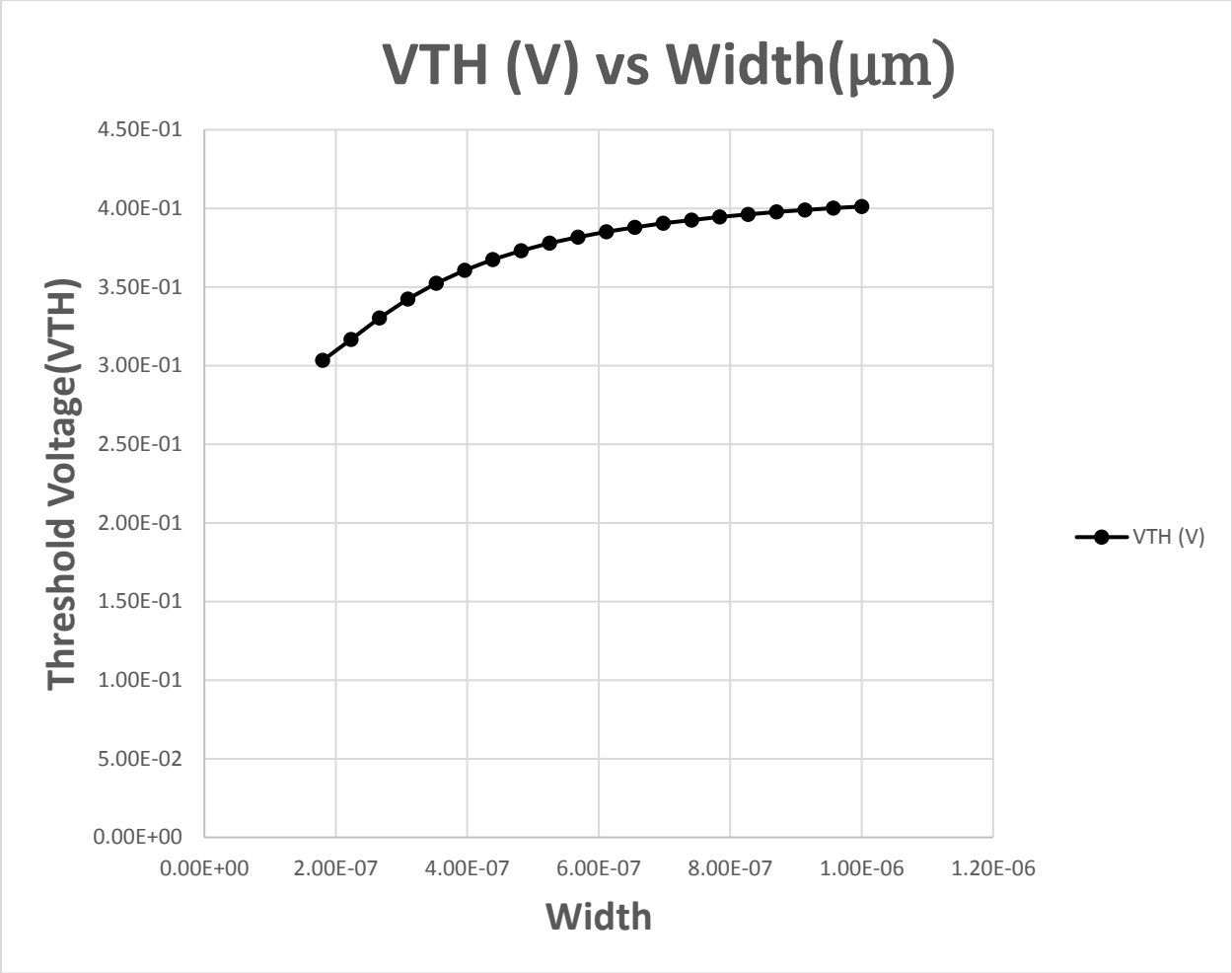

Fig 2.9. Threshold voltage vs Width of a 1µm long NMOS diode connected transistor

(V_{GS}= V_{DS} = 700mV)

The root cause of the inverse narrow width effect is the fringing fields originating at the gate and terminating at the sides of the channel. For a larger width these fringing fields are a small percentage of the total fields but at narrow widths these vertical fields deplete the region below the thin oxide increasing the surface potential. This increase in surface potential lowers the V_{GS} required for the onset of inversion which implies a reduction in the threshold voltage of the device [16]. These same fringing fields cause the narrow width effect in LOCOS processes, the fringe fields in LOCOS processes get wasted on the sides of the channel due to which the channel itself experiences a smaller field leading to an increase in threshold for narrow devices. In order

to negate the Narrow and Inverse Width Effects the unit width of a transistor should be kept higher than minimum geometry width (about 500nm at 180nm) and any increase in width should be realized through increasing the number of fingers, i.e. select a unit finger width of 260 to 300nm.

- Short Channel Effects and Reverse Short Channel Effects

Short channel effects are observed in processes where halo implants are absent (halo is a demarcation indicated for implant regions[16]), the resultant V_{TH} is decreased as the channel length is decreased. This is caused due to the S/D junction horizontal field penetrating into the channel and depletes the Si under the gate, hence a lesser gate-to-source voltage is required to achieve inversion effecting a reduction in the V_{TH} [32]. For processes that employ halo implants the scenario is just the opposite this is because the S/D halo regions are so close for short channel lengths that they overlap which increases the average channel doping and in turn increases the threshold voltage of the device with decreasing channel length [32]. The IBM CMOS7RF 0.18µm incorporates halo implants and follows the reverse short channel effect which can be seen in Fig 2.10 which plots the threshold voltage vs channel length for a 1µm wide NMOS device[32].

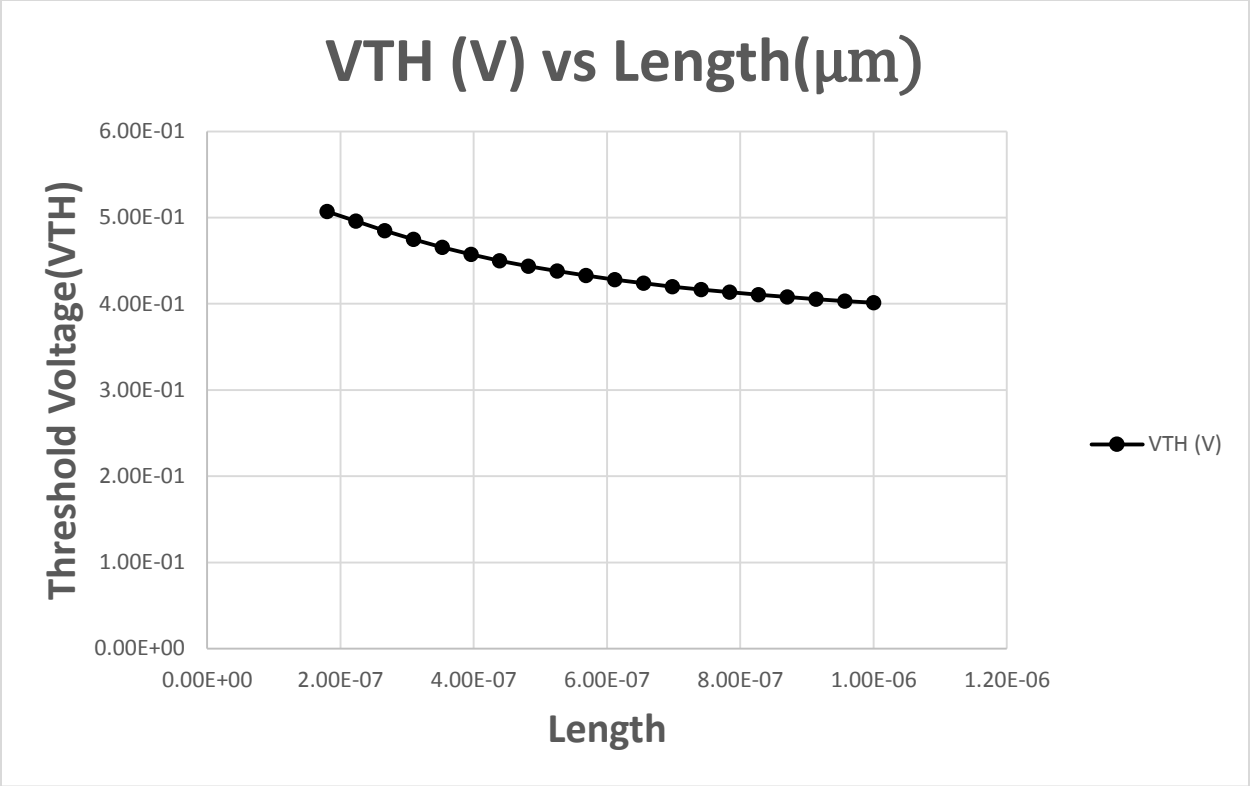

Fig 2.10 Threshold voltage vs Length of a 1µm wide NMOS diode connected transistor

(V_{GS}= V_{DS}= 700mV)

When considering non-fingered devices, the PMOS device experiences a lower impact from the INWE and RSCE compared to the NMOS [32]. Also the mobility of the PMOS is lower compared to the NMOS, in an attempt to match their mobility through change in transistor widths we can make use of both INWE and RSCE to our advantage.

- Drain Induced Barrier Lowering or DIBL

  As the drain voltage across a transistor is increased there is a phenomenon called drain induced barrier lowering which causes a decrease in threshold voltage. The drain induced barrier lowering or DIBL effect causes the current to increase and the channel inversion increases. This effect is observed mainly in short channel devices when the drain and source are in close proximity due to which their depletion regions approach each other,

there is a two-dimensional field on the carriers in the channel. Since there is a field from the source towards the drain and vice-versa the surface potential increases causing the carriers in the channel to move towards the drain for a lower gate-to-source voltage[16]. This phenomenon is extremely important when dealing with transistors operating in weak inversion since a reduction in threshold can causes an increase in inversion charge leading to moderate or strong inversion operation.

As all the sources effecting threshold voltage are uncorrelated, The total threshold voltage standard deviation is expressed by[19]

$$\sigma_{VTH} = \sqrt{\sigma^2{}_{VTH,RDF} + \sigma^2{}_{VTH,LER} + \sigma^2{}_{VTH,other}}$$

2.2.6 Effects of Process Variation

The effects of process variation are summarized in Fig 2.11.

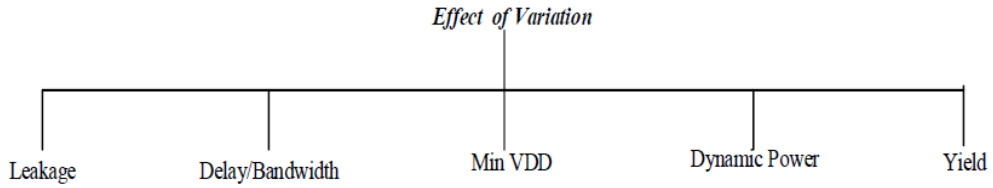

Fig 2.11. The effects of Variation[18]

Variation primarily effects Bandwidth, Dynamic Power, Leakage, Minimum supply voltage and the overall yield.

- Delay/Bandwidth: The current through a device can be represented as

$$I = C * \frac{dV}{dt} \cong C * \frac{\Delta V}{\Delta t};\ \Delta t = \frac{C}{I} * \Delta V$$

Where C is the parasitic capacitance and Δt is the time delay for the current to charge the capacitance C to ΔV voltage. As the current is dependent on the threshold voltage, any variation in threshold voltage causes variations in delay time which severely impacts performance.

- As stated in Sec 2.1.1 the total power dissipation is dependent on the leakage current and since the leakage current is a weak inversion current, variation in threshold brings about an exponential change in the leakage current which is one of the reasons weak inversion is characterized by high variability. This added leakage current can be detrimental in terms of power consumption when leakage from all devices is accounted for in a circuit.
- The minimum supply voltage for a stack of transistors will be decided primarily by the threshold voltages of the devices, for cold temperatures the threshold voltage of a device will increase which will put a limitation on the minimum supply voltage, this phenomenon of threshold change with temperature will be explored in Sec 2.3. This limitation on the supply voltage also effects the dynamic power dissipation as it is directly proportional to the square of the supply voltage.

2.2.7 Global Variation (Systematic/Process Variation)

The silicon wafer is circular in shape and many dies are placed on a single wafer, these dies are rectangular in shape. Misalignment in lenses and irregular lithography conditions causes die parameters to vary in dies that are placed closer to the circumference of the wafer compared to the center. The fabrication accuracy is high at the center of the wafer and all the dies in the center are efficient and faster compared to the remaining dies on the wafer. As die location moves towards the circumference of the wafer the dies are poorer in performance (higher threshold), this is attributed to the fact that the wafer is circular whereas the dies are rectangular in shape hence the dies close to the circumference do not experience the same process environment as at the center of the die. This variation of performance from the center of the die to its circumference is

modelled as a random probability function that has a spatial correlation and is referred to as process gradient or process variation. This radial variation is illustrated in Fig 2.12, as seen the center of the wafer is marked F which denotes that the performance of the dies in this region is faster (or superior) than the dies placed away from the center. The intermediate dies which are between the center and the circumference are marked T which denotes that they have a typical value which is the targeted performance and the dies close to the circumference are S which denote that these dies are slow and have poorer performance than desired. The process gradient affecting a single die is diagonal, left to right, bottom to top and vice versa. The process variation cannot be countered by any design techniques however the foundry provides test results that guide the designer to predict the process variation.

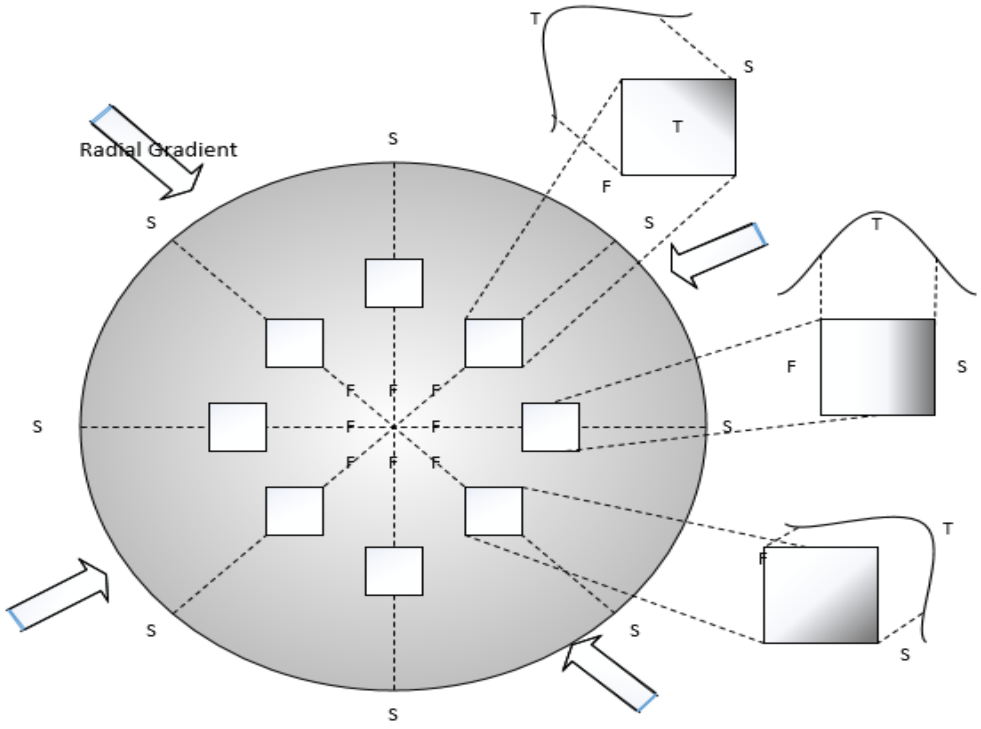

Fig 2.12. Radial gradient on wafer[18]

2.2.8 Local Variation

Apart from Global variation that plagues the wafer as a whole, semiconductor die are also affected by local variation that is variation in electric and chemical parameters within a limited or contained area within a die. This variation is caused due to the non-uniform doping illustrated in Sec 2.2.1, this variation is found between devices that are in close proximity to each other which is most commonly referred to as mismatch. Since the doping levels are random, one device may be doped with fewer or greater dopants than a device adjacent to it. This type of variation is detrimental to circuits which require uniform performance for devices that are kept close to one another such as differential amplifiers, current mirrors, comparators, etc. Within a fixed area the local mismatch is dominant over the global mismatch, this area is about 200µm X 200µm for the IBM CMOS 7 RF process[33]. The distribution of threshold voltage of a device due to local variation has a random distribution while its mean value varies with its position on the wafer (gradient), this phenomenon is illustrated in Fig 2.13. In a case where the size of a die is smaller than 200µm X 200µm, the parameter variations between dies will follow the local variation and this kind of variation is commonly referred to as Die-to-die variation. The RDF from Sec 2.2.1 causes a variation in the threshold voltage leading to DC voltage errors in the circuit, this type of error is commonly referred to as DC offset or offset. The offset is of great importance to this design effort since it limits the Signal to Noise ratio and dictates the transistor sizing and power consumption in order to achieve accuracy as well as robustness. Considering a minimum geometry NMOS device (220nm/180nm) and making use of the data indicated as $\pm 3\sigma$ provided by the semiconductor fabrication vendor we have

$$V_{osn} = \frac{A_{VTN}}{\sqrt{(W - K_{vtw})}(L - K_{vt})} = \frac{12mV.\mu m}{\sqrt{(0.22 + 0.58) * (0.18 - 0.58)}\,\mu m} = \pm 40mV$$

Where A_{VT} , K_{Vtw} , L_{Vtl} are process defined constants for the threshold voltage.

It is clear from the offset equation that the fix to reduce the offset is to increase the width and the length. Increasing the length will cost us bandwidth, hence the design technique used is to have maximum length that fulfils the bandwidth requirement and subsequently increase the width to reduce the offset such that it is tolerable. Increasing the width and length after a certain value $\approx 5-10$ ($W_{min} and L_{min}$) at that point the global variation is dominant over the local variation[32].

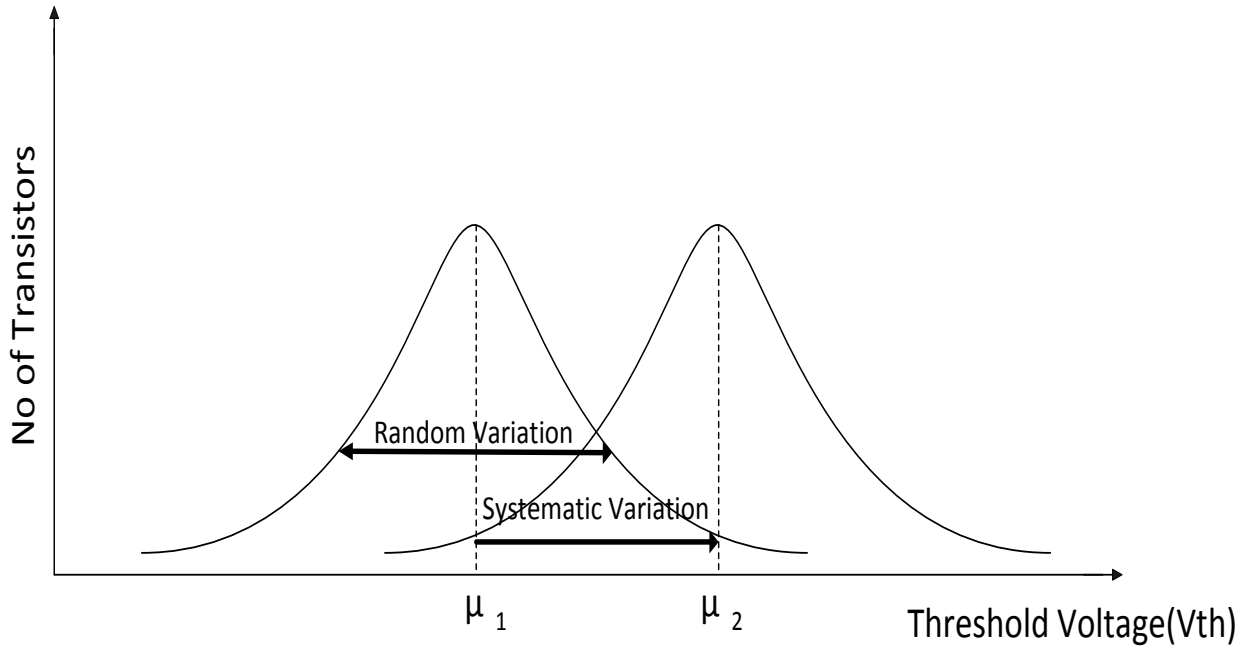

Fig 2.13. Stochastic perspective for Random and Systematic Variation of Threshold voltage of a device[18]

2.2.9 Monte Carlo

Monte Carlo is the technique used to sample the device parameters such as Length, Width, Threshold voltage, gate length, etc. These device parameters are assigned all the possible random values within the corner limits and the behavior of the entire circuit is analyzed based on the distributions of the circuit specifications such as gain, bandwidth, offset, etc. The design is

generally tested for $\pm 3\sigma$ from the target specification. Memory design on the other hand may require accuracy up to $\pm 6\sigma$ which is challenging to achieve. The tool used for this effort is Cadence Virtuoso which provides inbuilt Monte Carlo functionality which has been used to analyze the design performance for this effort. Through Monte Carlo simulations we are able to estimate the yield of a fabrication run. The yield of a fabrication run is the percentage of number of chips that meet the most relaxed specifications $(\pm 3\sigma - \pm 6\sigma)$ that deem a chip to be just about workable.

2.2.10 Process Corners

Process corners are certain conditions which demonstrate the limits of process, temperature and other design parameters that guide a designer to check the robustness of the design. The corners that are predominant when analyzing any design are SS (Slow NMOS, Slow PMOS), FF (Fast NMOS, Fast PMOS), TT (Typical NMOS, Typical PMOS), FS (Fast NMOS, Slow PMOS) and SF (Slow NMOS, Fast PMOS). For sophisticated processes there may be many more corners but these are the most widely used. The corner SS means that we randomly test a NMOS and PMOS within a die that is placed spatially at a location where the process is slow for a circuit specification for example clock rate. We then check if the clock rate meets our requirement, if not that die is either discarded or sold for less. The same is done for process corners FF and TT. All die specifications are tested for all these process corners to check robustness of the design. We do not demonstrate the process corners SF and FS, since it is not possible for one die to have a Fast NMOS and Slow PMOS no matter where that die is located on the wafer. Considering that there are many dies on the wafer and a spatial shift in the process variation it is impossible to practically explain the scenarios where the SF and FS corners become relevant. SF and FS corners are just checkpoints that guarantee that the design is robust even for a non-occurring event, hence any additional design effort to achieve performance to satisfy these design corners is

nothing but overdesigning. To avoid overdesigning in this effort we have neglected the SF and FS design corners and focused on the SS, TT and FF corners.

2.2.11 Lot-to-Lot and Wafer-to-Wafer Variation

Now that we have an understanding of what corners are we can explore the lot-to-lot and wafer-to-wafer variation. In a fabrication process multiple wafers are fabricated together and their collection is referred to as a lot. The variation between each lot is referred to as lot-to-lot variation which originates due to physical changes in mechanical and fabrication processes. Lot-to-Lot variation has a normal distribution such that the lots are segregated into Slow, Fast and Typical lots. Within each lot there would be a SS, TT and FF corners which implies that within that lot one wafer would be slow, typical and fast. This variation is referred to as wafer-to-wafer variation. Fig 2.14 shows the Lot-to-Lot variation while Fig 2.15 depicts Wafer-to-Wafer variation.

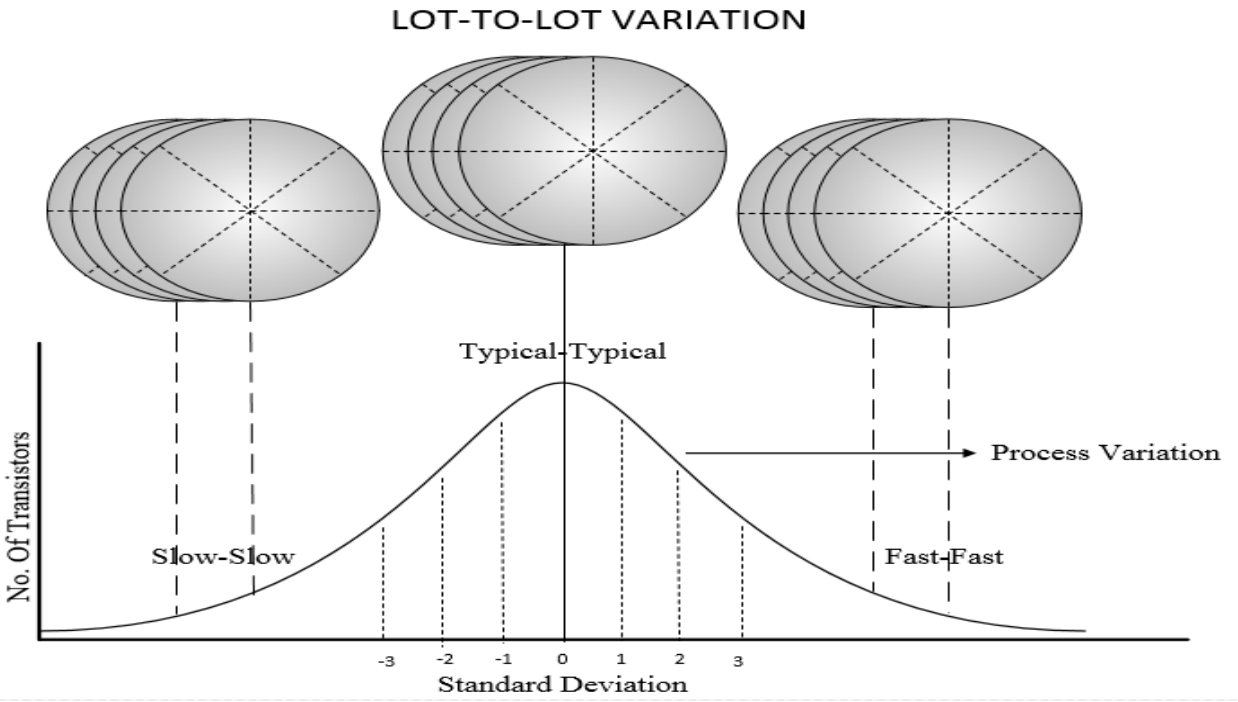

Fig 2.14 Lot-to-Lot Variation[18]

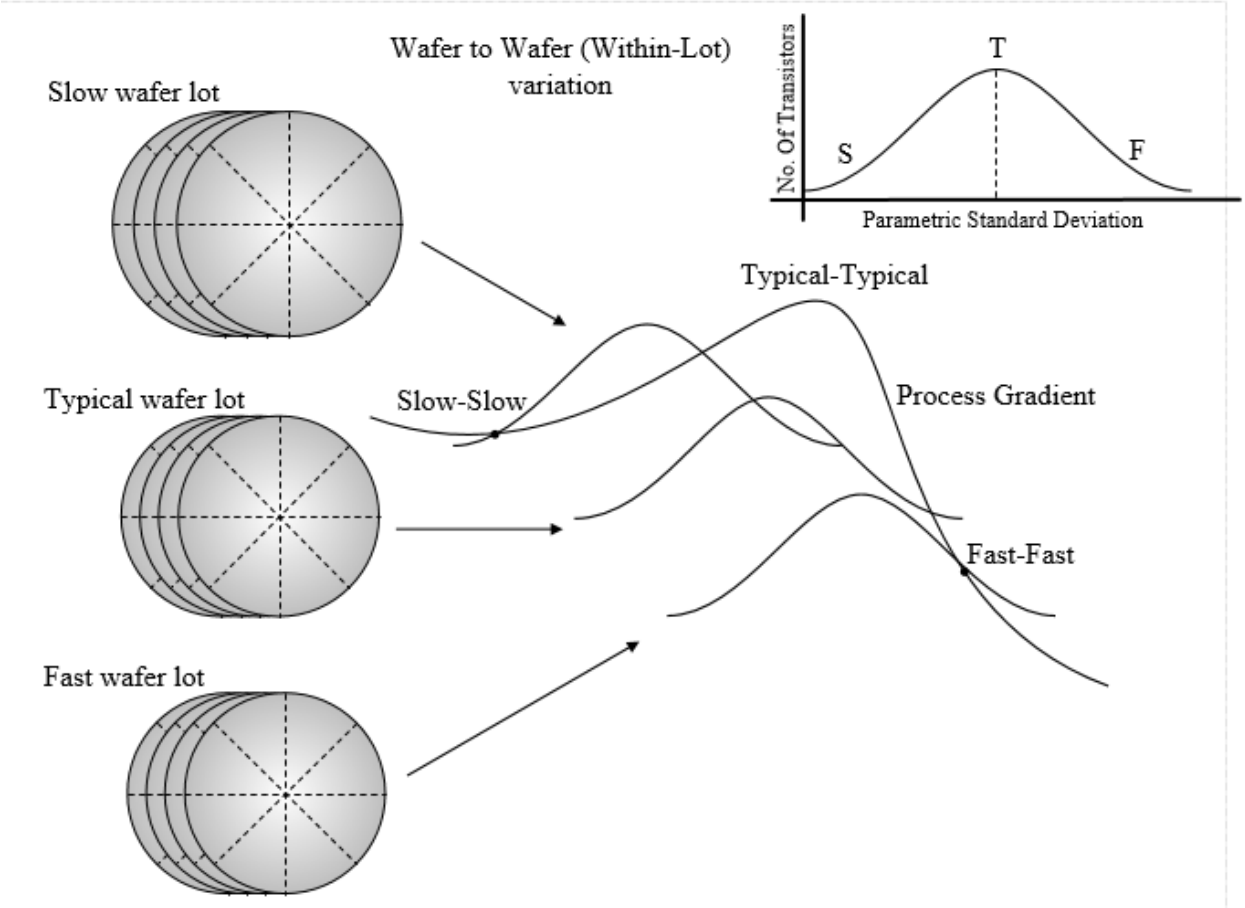

Fig 2.15. Wafer-to-Wafer Variation[18]

2.3 TEMPERATURE VARIATION

Temperature variation is a major factor when it comes to semiconductor chips. The environment condition temperatures can reach extremes and cause IC (Integrated chip) failures. Many a time when the cooling mechanism in the chip is not robust, the power generated by the chip itself can cause the internal temperature of the chip to rise to alarming levels as well as fluctuate over time.

This section will address the effects of temperature on the drain current in a circuit.

The mobility of electrons depends on the temperature as follows

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^m$$

Where T is the environmental temperature and T_0 is the reference temperature and m is the temperature coefficient of mobility. The coefficient m ranges from -1.2 to -2, often m=-1.5[11]. m is a process dependent parameter.

Threshold voltage of a MOS transistor is given by

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\emptyset_F} - \sqrt{2\emptyset_F}\right)$$

Where V_{SB} is the source-body voltage and $\emptyset_F$ is the Fermi potential which is given by

$$\emptyset_F = U_T \ln\left(\frac{N_A}{n_i}\right)$$

N_A is the acceptor atom doping and n_i is the concentration of intrinsic carriers in silicon. $\emptyset_F$ is a strong function of temperature hence the threshold voltage also varies with temperature. $V_T(T)$ decreases linearly with temperature as follows[16]

$$V_T(T) = V_T(T_0) + \alpha_{VT}(T - T_0)$$

Where $V_T(T_0)$ is the threshold voltage at temperature T and α_{VT} is the temperature coefficient of the threshold voltage. The typical value of the threshold voltage ranges from -0.5mV/℃ to -4mV/℃ [11].

Hence we observe that both the electron mobility and threshold voltage both decrease with increase in temperature though both have opposite effects on the current flowing through the transistor. When the threshold voltage of a transistor reduces the current flowing through it increases whereas for a decrease in the electron mobility the current reduces.

2.3.1 Effect of Temperature Change in Weak Inversion

Restating the weak inversion drain current equation

$$I_D = I_{D0} e^{\frac{V_{GS}-V_T}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{U_T}}\right)$$

$$I_{D0} = 2n\frac{W}{L}\mu_n C_{ox} U_T^2$$

n is the subthreshold slope and ranges from 1-2.

Since the threshold voltage is in the exponential term it has a stronger influence on the current when compared to the mobility of the electrons which only linearly effects the current. When the temperature of the transistor is increased the current flowing through it increases since the threshold has reduced. When the temperature of the transistor is reduced the threshold voltage is increased causing a lower drain current to flow even though electron mobility has increased. This implies that the best case scenario for a transistor biased in the weak inversion regime is maintaining a high temperature on the other hand a low temperature would be the worst case scenario to effect a high drain current.

2.3.2 Effect of Temperature Change in Strong Inversion

For the 0.18µm process the velocity of the carriers is saturated for their shorter channel lengths hence we are going to limit the strong inversion discussion to velocity saturation. When the longitudinal field in the channel is very high due to the small channel length the MOS transistor experiences carrier mobility degradation hence the slope of the carrier velocity decreases with increasing longitudinal field. Scatter effects in the channel close to the surface are the root cause of velocity saturation[16].

The drain current flowing through a transistor biased in strong inversion velocity saturation is given by[34]

$$I_D = \frac{\mu_n C_{ox}}{2\left(1 + \frac{V_{GS}-V_T}{\varepsilon_c L}\right)} \frac{W}{L} (V_{GS}-V_T)^2$$

Where ε_C is the critical field when the carrier mobility with a high horizontal field is half of the carrier mobility if the field applied was low according to [34]. The vertical field effect causes the mobility degradation due to the coulomb and phonon scattering effects[16]. The vertical and horizontal fields both contribute to the velocity saturation of the carriers, the assignment of the critical field ε_C is based on either fields horizontal or vertical as both have their critical limits. To avoid confusion, both the vertical and horizontal fields effect mobility and cause velocity saturation of the carriers as [16] associates the symbol ε_C as the critical field with the longitudinal field whereas [34] associates it to the horizontal field.

As both the carrier mobility and the threshold are linear terms of the current equation in such a case the dependence of the current would be a stronger function of carrier mobility than the threshold voltage w.r.t temperature change. Hence the current would reduce at higher temperatures as the mobility would go down dominating the effect of the reduced threshold voltage. Conversely at lower temperatures the current would be high in spite of an increased threshold voltage. The MOS transistor biased in the velocity saturated regime would therefore be slower at higher temperatures and faster at lower temperature which is completely opposite to what the MOS transistor experiences in the subthreshold region. The effect of temperature on the drain current in square-law operation is similar to the velocity saturated behavior.

2.3.3 Zero Temperature Coefficient Point (ZTC)

From sections 2.3.1 and 2.3.2 we have seen that the effect of temperature on the drain current through a MOS transistor is governed by the region of operation. The region of operation of a transistor is dependent on the gate-to-source voltage applied to the transistor. There exists a particular gate-to-source voltage for which the drain current is independent of temperature, where the effect of mobility and threshold voltage w.r.t temperature cancel each other. This value of V_{GS} for which the drain current is independent of temperature is termed as the Zero-Temperature-

Coefficient Bias Point or more commonly referred to as the ZTC point. In Fig 2.16 we investigate this ZTC point by sweeping the bias voltage of a single finger minimum geometry (220nm/180nm) NMOS in a diode configuration and varying the temperature from -25℃ to 125℃ while recording the drain current flowing through it. The same has been done for the PMOS transistor and is shown in Fig .17.

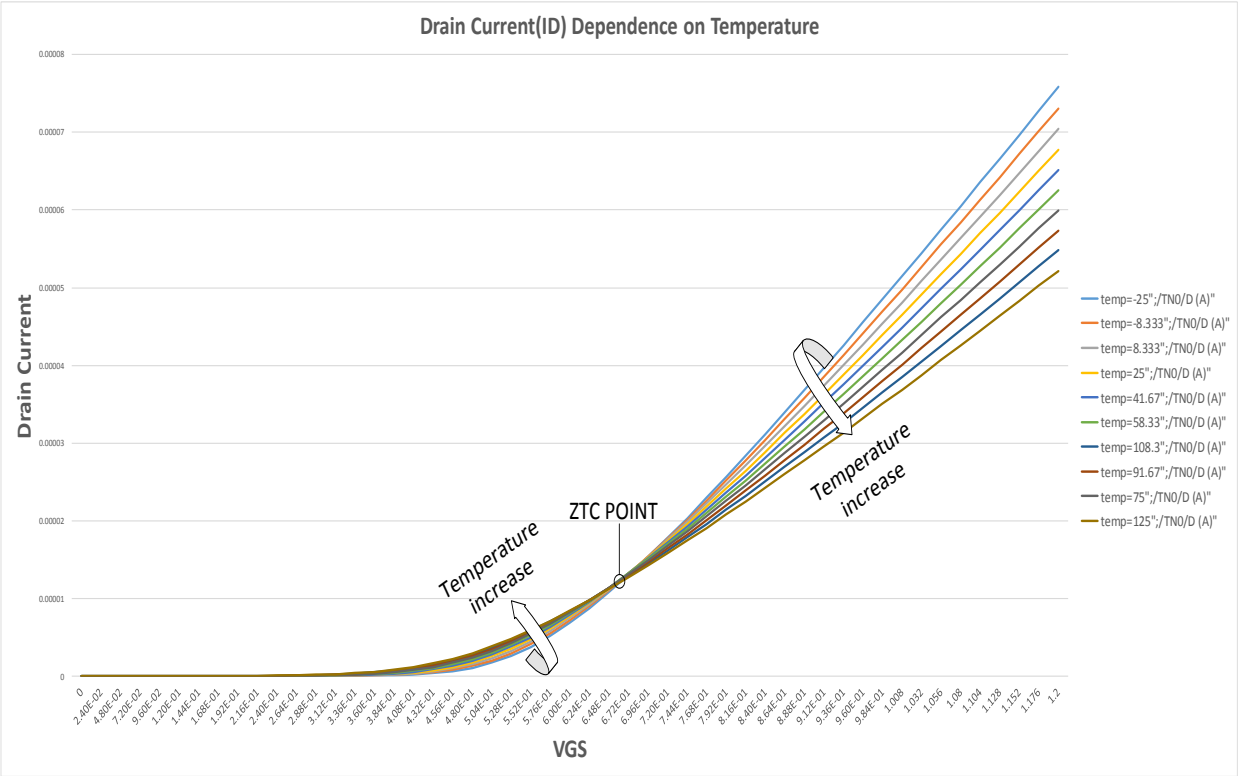

Fig 2.16. Drain Current Dependence on Temperature and the ZTC Point for a minimum geometry NMOS

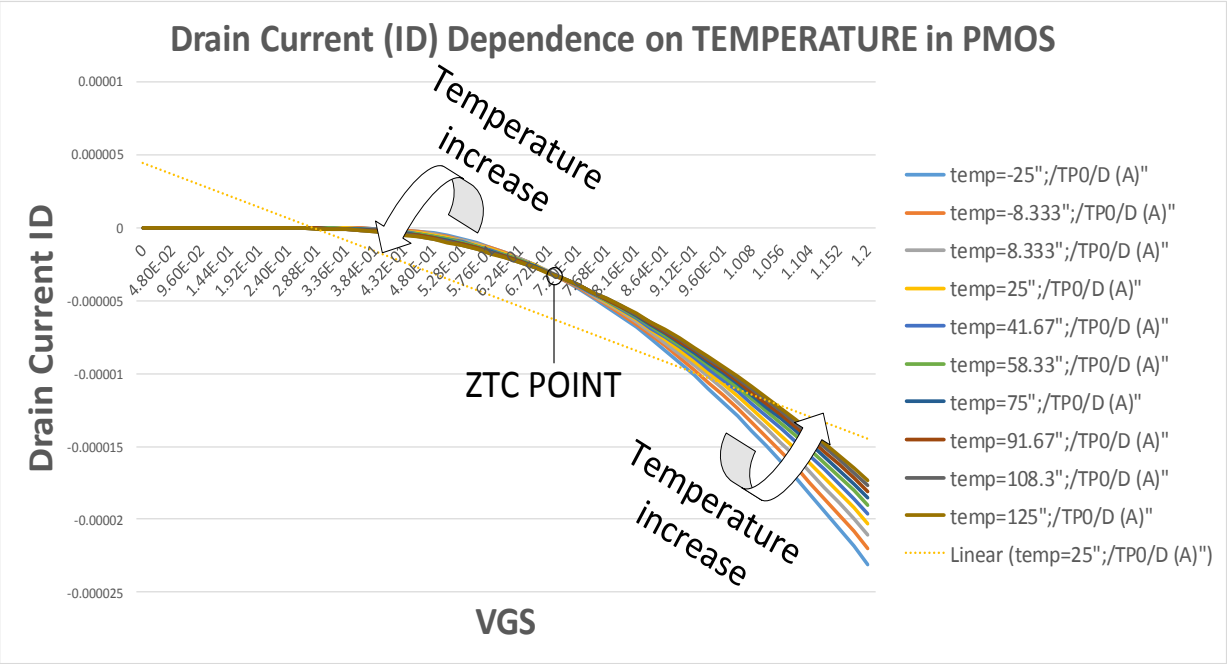

Fig2.17. Drain Current Dependence on Temperature and the ZTC Point for a minimum geometry PMOS

Fig 2.16,17 both show the contrasting effects of MOS operation in weak and strong inversion when the temperature is increased.

2.4 Supply Voltage Variation

The supply voltage to a die is variable which is due to many reasons such as power supply noise, crosstalk, IR drops, etc. The performance of the die is proportional to the supply voltage, hence a higher supply voltage facilitates a greater drain current which corresponds to higher speed. The supply voltage variation is modelled at about $\pm 10\%$ of the typical voltage value. Newer designs have a much tighter budget of $\pm 5\%$ [35] off the target supply voltage. The impact of variation in supply voltage is masked by the detrimental effects of process and temperature variation in IC designs.

2.5 PVT (Process, Voltage and Temperature) Corners

Form the discussions in Sec 2.2, 2.3 and 2.4 we have a good understanding of the impact of process, temperature and supply voltage variations on the operation of MOS transistors, now we take a look on how these three effects combine and their implications on the worst case and best case scenarios. The design of a circuit is tested for the worst case and best case PVT corners, given that the performance of that design is satisfactory for the best and worst cases it would be safe to say that the design will work for any other PVT corners within that range of operation.

2.5.1 Weak Inversion PVT corners

As seen in Sec 2.2.10 a die would have a poor performance at the SS corner, while Sec 2.3.1 established that a transistor slows down when the temperature is low when the device is biased in weak inversion. Putting these two conditions together and considering the proportional dependence of the voltage on the drain current we state that the transistor performance that would be the worst case PVT corners would be the SS @ -25℃ for 90% of the supply voltage. Conversely the best case would be FF@125℃ for 110% of the supply voltage.

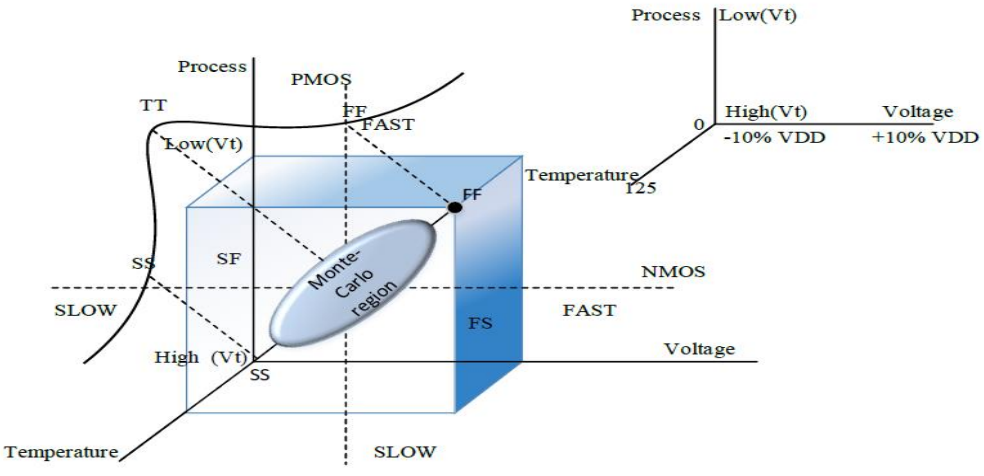

Fig 2.18. Weak inversion PVT corners[18]

Fig 2.18 represents the corners on three axis, process, temperature and voltage. The center of the graph represents the worst case whereas the best case is located in the 3-D plane and all other possible conditions are limited within these two extremes.

2.5.2 Strong Inversion PVT corners

The PVT corners for strong inversion is different from the weak inversion in terms of the temperature corner as seen in Sec 2.3. Hence the worst case PVT corner for the strongly inverted device would be SS@125℃ at 90% supply voltage whereas best case corner would be FF@-25℃ at 110% supply voltage. Fig 2.19 shows the corners for the strong inversion device.

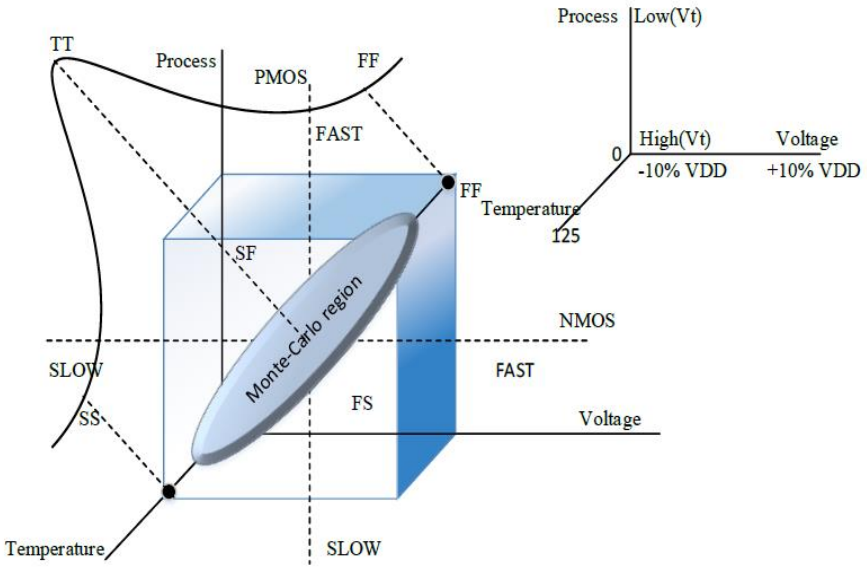

Fig 2.19. Strong inversion PVT corners[18]

CHAPTER III

ASK DEMODULATORS

3.1 Digital Modulation

The most prominent digital modulation schemes are Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK) and Phase Shift Keying (PSK). ASK modulation is the most widely used modulation schemes for passive wireless microsystems due to the fact that the modulator and demodulators are simple to configure and their power consumption[11]. In this work we focus on the ASK modulation, the FSK and PSK modulation schemes can be found in [11]. Figure 3.1 depicts the waveform of a binary ASK modulated bit stream[11].

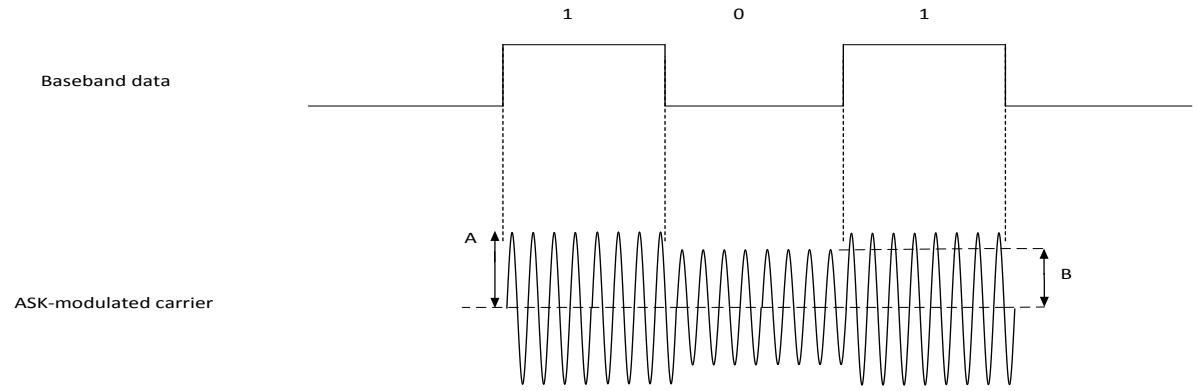

Figure 3.1 Binary ASK modulated bit stream [11]

Where A is the amplitude for binary 1 and B for binary 0. According to [36] there are two types of signaling suitable for passive RFID, Type A signaling and Type B signaling, not to confuse them with the amplitudes of the modulated waveforms presented in Figure 3.1. The Type A signaling utilizes 100% amplitude modulation which is the On-Off Keying (OOK) where the binary 1 data comprises of the full power pulse while the binary 0 is accompanied with a power off phase. Type B signaling on the other hand utilizes around 10% amplitude modulation.

The modulation index and modulation depth of a modulated waveform employing Type B signaling according to [36] is given by:

$$Modulation\ Index = \frac{A - B}{A + B} \tag{3.1}$$

$$Modulation\ Depth = \frac{B}{A} \tag{3.2}$$

From equations 3.1 and 3.2 we understand that the greater the modulation index the easier it is for demodulation whereas a smaller modulation index means that the amplitude difference between the binary 1 and binary 0 is small adding additional constraints on the demodulator circuit. The drawback of having a small modulation index is that the signal is prone to noise and disturbances. Hence the noise from the demodulator circuit itself should not harm the incoming signal. The advantage of having a low modulation index is that it provides a more even power flow to the RFID harvester. This even power flow to the harvester ensures that the RFID operates optimally for both logic 1 and logic 0 cycles.

3.2 ASK Demodulators

The basic principle of the RFID ASK demodulator is depicted in Figure 3.2

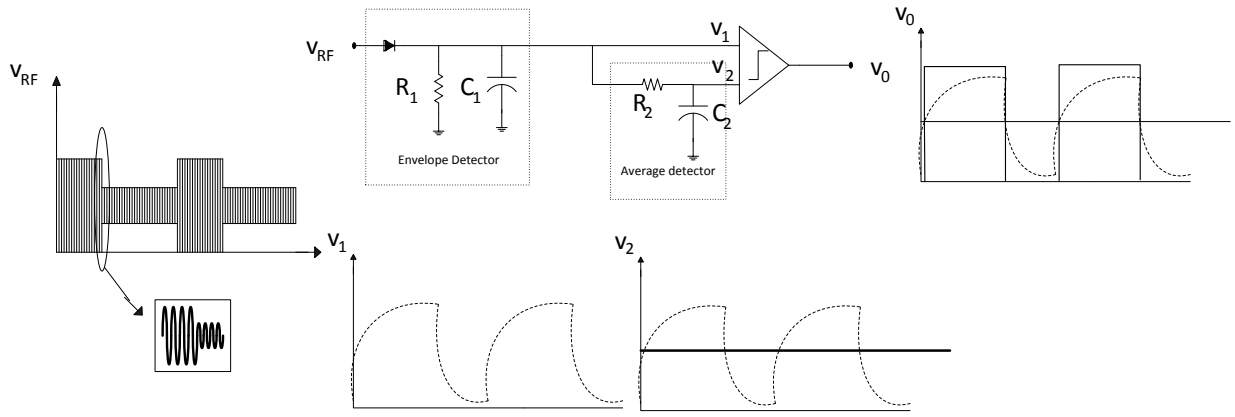

Figure 3.2. Basic implementation of a demodulator[11]

The basic ASK demodulator consists of a passive envelope detector and an average detector and a hysteresis comparator. The diode in combination with the low pass network of R_1 and C_1 constitute the envelope detector. During the positive cycle, the diode is forward biased and the capacitor C_1 is charged to the peak of the input, on the negative cycle the diode is reversed biased and is off due to which the capacitor C_1 discharges across the resistor R_1 as shown in Fig13. The average detector on the other hand consists of a low pass filter consisting of resistor R_2 and capacitor C_2 .The average detector produces the DC component of the input signal. The comparator compares the envelope (v_1) and the DC component (v_2) of the input to produce the output which represents the demodulated version of the input. The choice of the time constants of the filters is critical. Time constant of the envelope detector is given as$\tau_1 = R_1 C_1$. This time constant (τ_1) should be sufficiently large enough such that the voltage v_1 does not contain significant amount of ripples, on the other hand it should be small enough to follow the input RF waveform envelope[11]. The time constant of the average detector should be large enough to filter out the high frequency components of the voltage v_1. Typically $\tau_2 \approx 10 * \tau_1$ [11]. The drawback of having a high time constant for the average detector is the area penalty as the area associated with the passive components as to increase the resistance and/or capacitance the area associated with these elements has to be increased.

ASK Demodulators are classified into three categories:

- Voltage-Mode ASK Demodulators
- Current-Mode ASK Demodulators
- Mixed-Mode ASK Demodulators

This classification is based on whether the nodal voltages or nodal currents of the modulated input are utilized in order to process the information [11]. In Voltage-Mode ASK Demodulator the nodal voltages are represented by voltages whereas Current-Mode by currents and Mixed-Mode use both voltage and currents in order to process the information. The following sections will present a few of the more significant RFID designs implemented in the recent past representing each of the three types of demodulators.

3.2.1 Voltage-Mode ASK Demodulators

Bouvier et al[37] implemented a voltage mode demodulator by substituting the resistors and capacitors with MOSFETs and made use of a two stage amplifier in order to compare the envelope and the average voltages, resulting in a significant area savingsThe circuit diagram for the same is given in Figure 3.3.

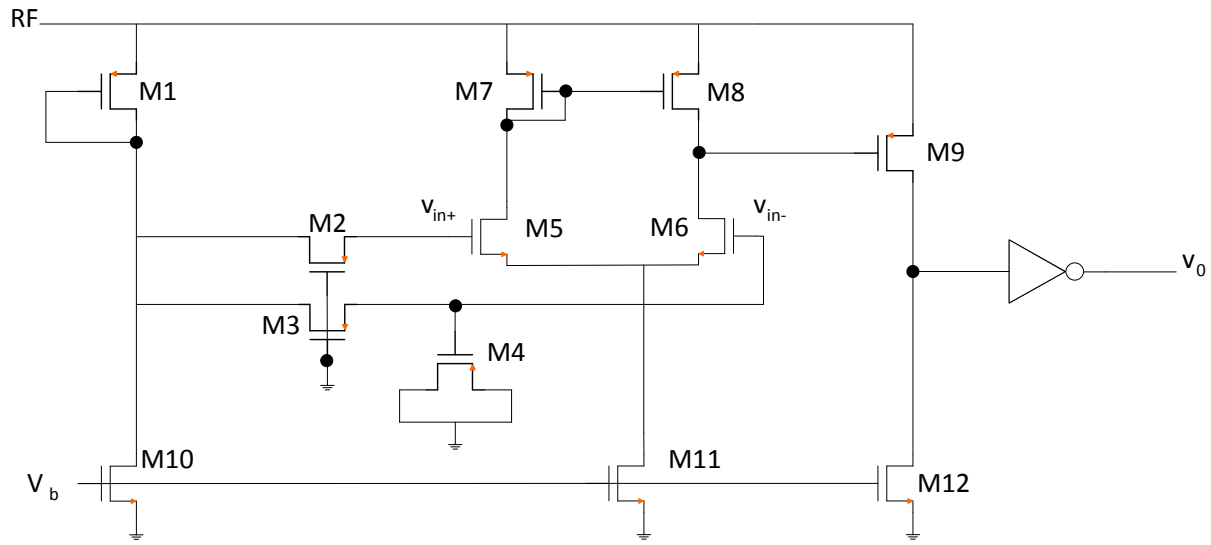

Figure 3.3. Bouvier et al Circuit Diagram[37]

When the RF signal exceeds the V_T of transistor M1, transistors M2 and M3 are on which are biased in the triode region whereas when the RF input is lower than the V_T of "MOS diode" transistor M1, transistors M2 and M3 are off. Transistor M2 and M3 acts as a resistors. M2 along with the C_{gs} of transistor M5 make up the envelope detector. Transistor M3 along MOS capacitor M4 constitute the average detector. M10 provides the discharge path of both envelope and average detector. The voltage amplifier composed of transistors M5-M8 has a single ended output which is followed by a common source amplifier stage composed of M9 and M12 has a gain approaching $\mu^2/_2$, where μ represents the self-gain of transistor M9 and M6. Finally an inverter is used to restore the full swing of the demodulated output. The use of MOS transistors in place of the passive resistors and capacitors reduces the area as the area taken by the MOS resistor and MOS capacitor are reduced compared to their passive counterparts. The voltage amplifier, the transistor M1 branch and the common source amplifier all continuously sink current which is a potential drawback since this current would increase power consumption($P_{Loss} = V_{DD}I_D$). Mendizabel et al[1] realize an ASK voltage mode demodulator employing the ASK-PWM

modulation scheme, selecting the region of operation as the weak inversion region in order to reduce the overall power consumption although at a lower data rate and 100 % modulation index. The architecture employs an envelope detector circuit as shown in Figure 3.4 (a) and a Doki Schmitt trigger [2] for the average detector shown in Figure 3.4 (b). The output from the envelope detector goes to an integrator shown in Figure 3.4 (c) and a comparator in order to measure each pulse duration to decide whether it is a logic 1 or logic 0[1]. The design achieves a low power although the variability of MOS transistor operation in weak inversion is not addressed. Another drawback is that the design fails below 5℃ and may not be suitable for use in military or automotive applications.

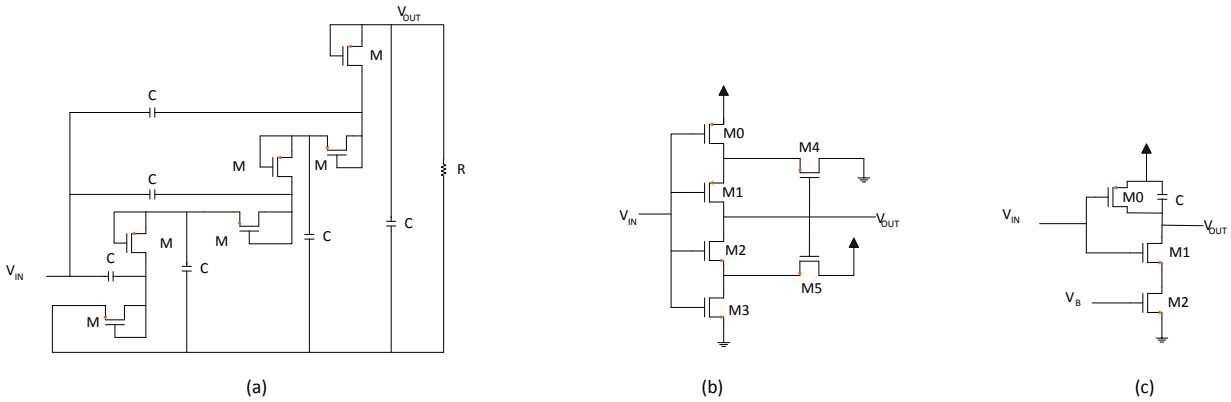

Figure 3.4 (a) Envelope Detector circuit by [1] (b) Doki Schmitt Trigger circuit[2] (c) Integrator Circuit[1]

3.2.2 Current Mode ASK Demodulator

Liu et al[3] designed a current mode demodulator for modulation index of 10% which employs a state machine to power off the remaining circuits while the current and voltage comparators are comparing the envelope and the average values of the input, this ensures low power consumption, on the other hand we have to invest in a state machine which adds complexity to the design but with the benefit of low power and low voltage operation[3]. The simplified equivalent block diagram of the design is shown in Figure 3.5. The drawback of the design is that it requires 5

voltage and 5 current comparators which involves significant design effort to realize the architecture. More significantly the design requires over 15 legs of current at demodulator bandwidth as shown in Figure 3.6. Although this design achieves low power consumption it takes a modest amount of area to realize the design. Another approach is presented by Gudnason et al [4] and the block diagram is shown in Figure 3.7 (a) which consists of a passive RC network which generates the input RF signal current, it is then rectified by a squarer as shown in Figure 3.7 (b), a third-order Gm-C low-pass stage is employed in order to extract the envelope of the output of the squarer as shown in Figure 3.7 (c) and finally a level detector shown in Figure 3.7 (d) is used to eliminate the long synchronization sequence necessary to establish the voltage reference used for data recovery[11]. Figure 3.7 (e) shows the Gm stage used in the low-pass stage. The design involves many stages and takes a fair amount of area to realize the whole design. The drawbacks of the design include the high power of the design given the total number of current legs at bandwidth is about 20 and the complexity involved in realizing such a design. Another important drawback of the design is that when we scale to the latest CMOS technologies there is a limitation on the unit width and length of a transistor and width increments cannot be made by increasing the number of fingers of the transistor. The only way to increase the width of the transistor is to manually place more transistors in parallel and in series in order to increase their lengths in the schematic view, in such a scenario this design would prove cumbersome due to the number of transistors in the design. Hence this design would not only prove complex but will also be time consuming for the designer for the latest technologies.

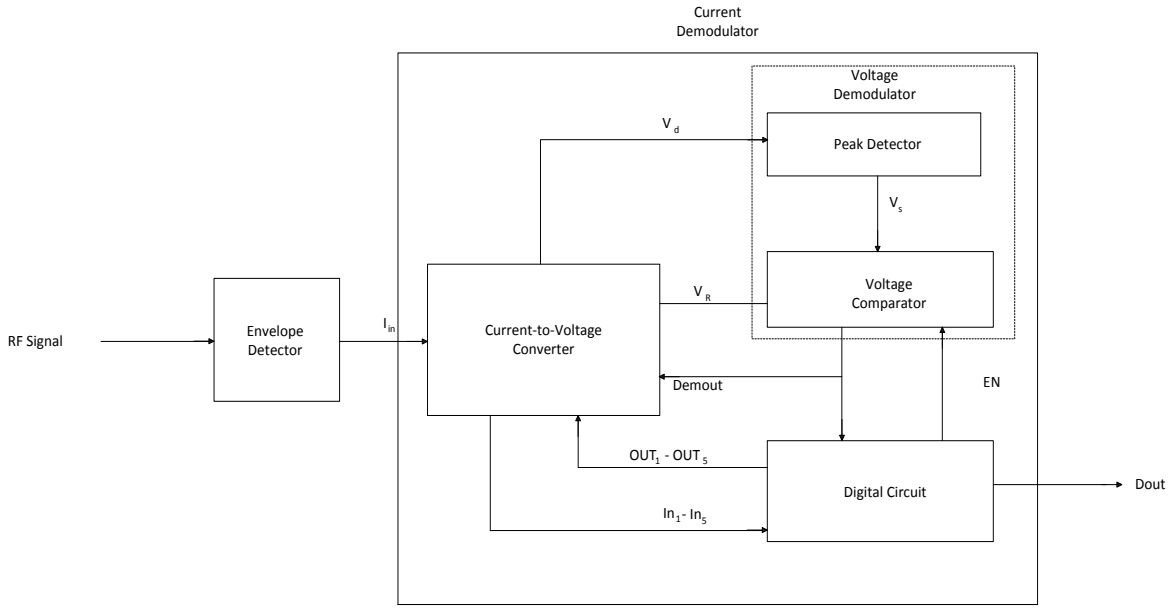

Figure 3.5 Block Diagram of LIU et al[3]

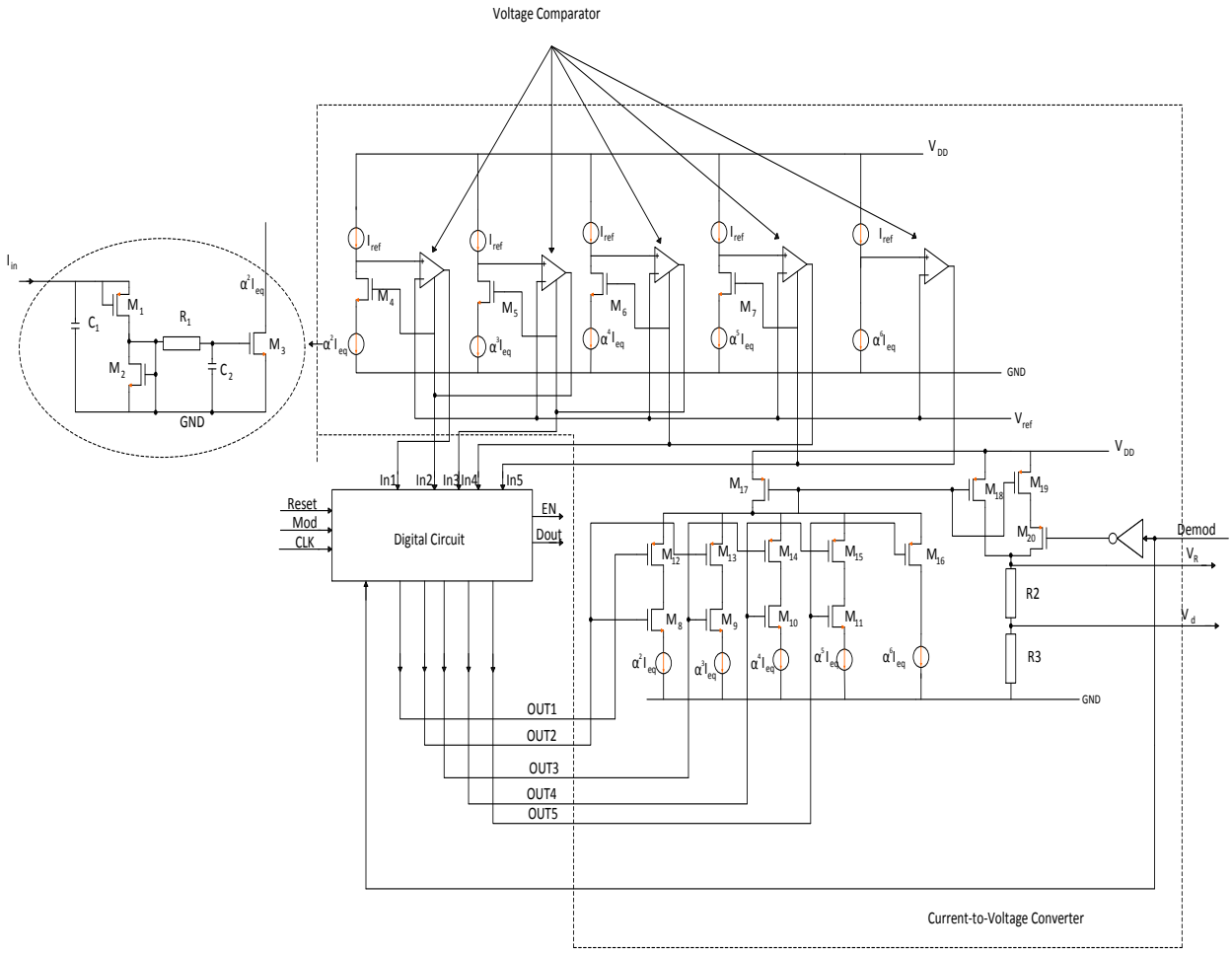

Figure 3.6 Current to voltage Converter[3]

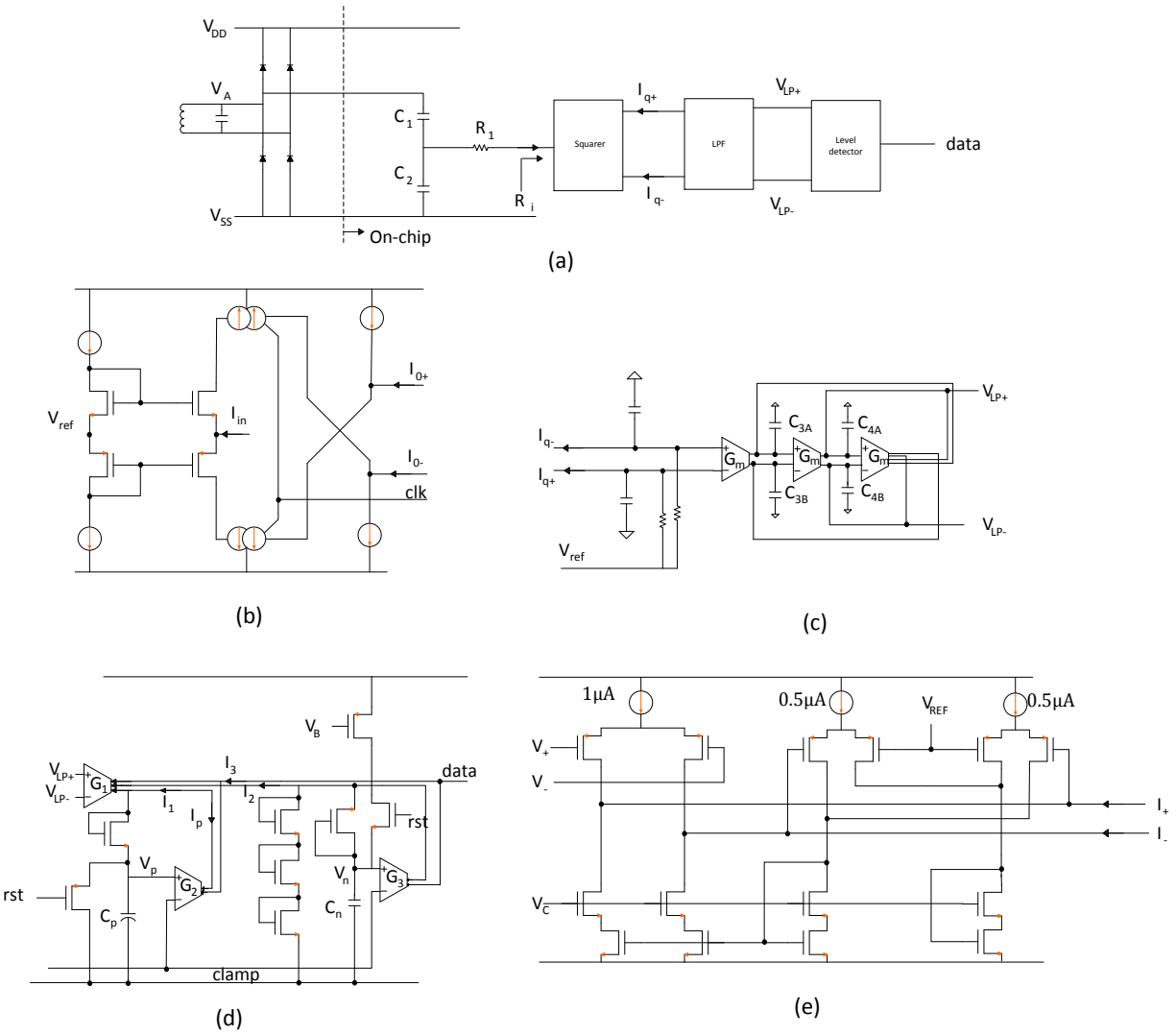

Figure 3.7 (a) Block Diagram of GUDNASON[4] (b) Squarer circuit[4] (c) The differential LPF implementation [4](d) The peak detector and data signal extraction circuit[4] (e) A single-output filter transconductor, with CMFB circuit[4]

3.2.3 Mixed-Mode ASK Demodulators

Mousavi et al[5] makes use of the conventional envelope detector but opts for a faster average detector to reduce the high Bit error rates(BER). The premise on which this solution is based is that if the time constant of the average detector is more than a bit interval T_b, this causes a problem for the detector (e.g. comparator). This effect greatly influences the performance of the

demodulation process by deteriorating BER[5]. To ensure that the BER is not effected by the circuit time constant limitations, the data rate $R_b = 1/T_b$ should be much smaller than the inverse of the time constant of the average detector ($R_b < (5\tau_2)^{-1}$). Having a fast average detector would mean that the time constant is small, making its inverse greater than the data rate. This faster average detector is realized by substituting the passive resistor and capacitors with MOS transistors and making use of diode connected MOS transistors in order to level shift the average value of the input signal to a lower value than the voltage envelope of the input signal. The circuit diagram for the same is shown in Figure 3.8 (a) and its simplified equivalent is shown in Figure 3.8 (b). To satisfy the BER condition the following condition must be satisfied.

$$Data\ Rate < \frac{1}{5C_4\left(1/gm_2\right)} = \frac{gm_2}{5C_4}$$

Hence the sizing of transistors M_2 and M4 are done such that the above condition is met. The averaging circuit then drives a gm stage (Transistor M_5) which works in the following manner

$$i_{D5} = \begin{cases} g_{m5}(V_{SG5} - V_{TH}) & for\ \left(V_{env} - V_{avg}\right) > V_{TH} \\ 0 & for\ \left(V_{env} - V_{avg}\right) < V_{TH} \end{cases}$$

Transistor M_5 then copies the current to transistor M9 with the help of transistors M6-M8 and finally using transistors M10-M13 this current is converted to a voltage which is fed to a decision circuit that gives the demodulated output. The advantage of such a design is that the transistor M_5 shuts off when the average value of the input is greater than the voltage envelope, hence the current flowing through the transistor M_5 is zero saving power during the off phase. The design uses high-voltage 3.3V transistors using the 0.18µm high voltage process. A possible drawback of this architecture is that for low voltage operation the transistors would leak and the advantage of power saving would not make much sense since the transistor M_5 would not be off irrespective of $V_{env} < V_{avg}$ as it would continue to operate in the subthreshold region. Another drawback of this

circuit is the need to generate a bias current I_{bias}. Though this design does not utilize a current envelope detector it does warrant inclusion in the Mixed Mode demodulator section since both voltage and current quantities are manipulated to achieve demodulation. Mousavi et al[5] presents a Figure of Merit for the design which we would analyze in detail in Chapter 6.

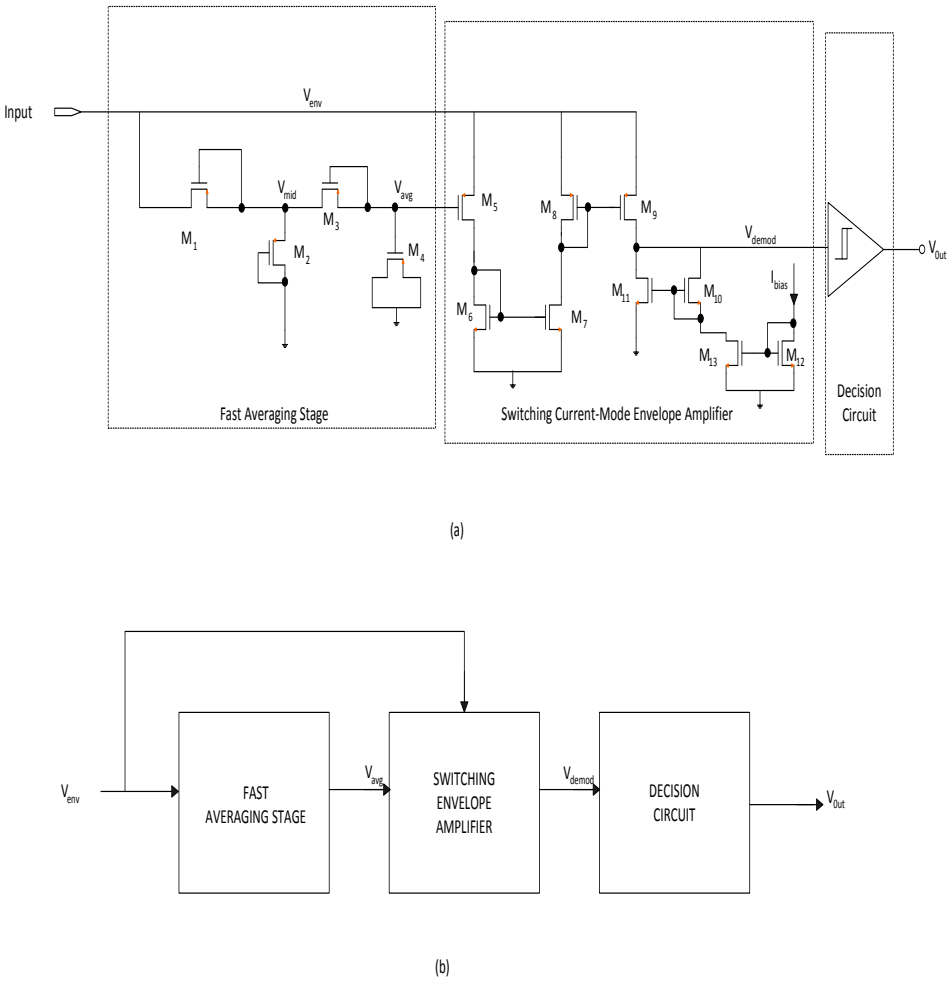

Figure 3.8 (a): Mousavi et al circuit diagram (b) equivalent block diagram [5].

3.3 Tabular Comparison of ASK demodulators in the past

This section mentions relevant RFIDs designed in the past and notes all the important design specifications that would be useful in comparison using a Figure of Merit in Chapter 6. The

important design specifications of supply voltage, data rate, and power consumed at room temperature, modulation index, carrier frequency, process node and area are presented in Table 3.1.

Table 3.1 Design Parameters of ASK Demodulators designed in the Past

REFERENCE	SUPPLY VOLTAGE (V)	Data rate (kbits/s)	POWER CONSUMED AT RTM (27℃) (μW)	MODULATION INDEX (%)	CARRIE FREQUENCY (MHz)	Process (nm)	Area (mm^2)
GANESH[38]	1.25	160	>0.2	≈11	860-960	130	-
Huang[39]	1.8	-	0.9	-	-	180	-
ASHRY[40]	1.2	-	0.2	-	-	130	-
KAO[41]	1.8	1000	396	2.86-38.64	2	180	0.0036
CHOI [42]	1	-	7.065	-	900	200	-
ZONG[43]	0.95	20	0.23	100	915	90	0.015
MARYAM[44]	1.2	125-250	>>0.248	-	2400	180	-
REHAN[14]	0.7	320	0.1	50	900	180	-
DJEMOUAI[45]	1.8	500	8	-	-	180	-
LIU[3]	1.5	4000	3.95	10	860-960	180	0.057
HARJANI[46]	1-2	1000	3000	-	10	500	-
GUDNASON[4]	3	200	60	10-100	1-15	500	0.22
WANG[47]	3.3	10	1000-23900	10-17	2	350	0.0127
WANG[48]	3	1200	306	-	13.56	350	0.0033
MOUSAVI[5]	1.8	Up to 2000	35	7	13.56	180	0.003
MENDIZABEL[1]	0.3	≈125	0.015	100	900	90	0.000462

GONG[49]	1.8	Up to 1000	336	>5.5	2	180	0.00047
LEE[50]	1.8 and 3.3	6780	348750	2.56	13.56	180	0.08

CHAPTER IV

DESIGN IMPLEMENTATION

In this chapter we would introduce the implementation of the ASK demodulator designed in this effort. The chapter starts with the input waveform characteristics and goes on to present the circuit and works of the entire design. The design objective and steps to achieve such a design objective are presented latter in the chapter.

4.1 Input to the ASK Demodulator

The input to the RFID is a Double Sideband suppressed carrier signal as shown in Figure 4.1.

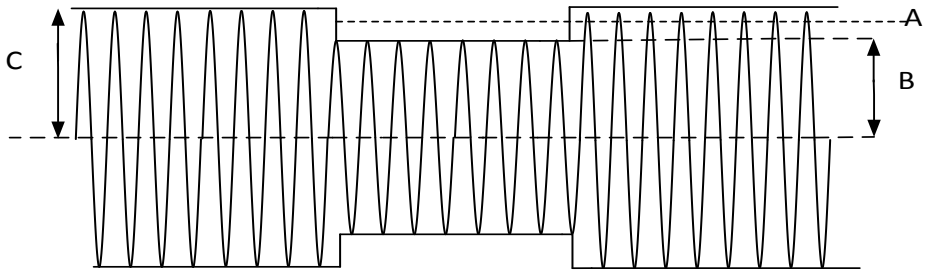

Fig 4.1 DSB-AM Waveform

The modulation schemes used in the RFID tags that employ amplitude shift keying include the double side band-amplitude shift keying (DSB-ASK), Phase Reversal Amplitude shift keying(PR-ASK) and Single Side band ASK(SSB-ASK) modulation schemes[51].

In this effort we use the double side band-amplitude shift keying (DSB-ASK) waveform as the incoming RF input to the tag. DSB-ASK modulation scheme modulates the carrier waveform by a baseband data signal which is obtained from the data encoding scheme[51]. The input voltage waveform at the input of the demodulator is dependent on the nature of the DSB-ASK waveform received at the input of the RFID.

The calculations for the waveform at the input of the demodulator are as follows:

Assuming a Modulation index of 0.05,

$$\frac{A-B}{A+B} = 0.05$$

$$\frac{1-\frac{B}{A}}{1+\frac{B}{A}} = 0.05$$

$$\frac{B}{A} = \frac{0.95}{1.05} = 90.47\%$$

- Modulation index = 5% and Modulation depth = 90.47%

Assuming minimum input power P_{IN} for the RFID functioning is -3dBm, only half that power is available at the input of the RFID which is -6dBm. Hence the magnitude of $P_{IN,Demod}$ from [52]

$$P_{sig|dBm} = 10\ log\left(\frac{P_{in}}{1mW}\right)$$

Therefore, we have

$$-6dBm = 10\ log\left(\frac{P_{in}}{1mW}\right)$$

Solving further we get,

$$P_{in} = 250\mu W$$

Assuming Matching is perfect we calculate the V_{pp} voltage as follows:

$$P_{in} = \frac{{V_{rms}}^2}{R_{antenna}}$$

For $R_{antenna} = 50\Omega$ and using

$$V_{rms} = \frac{V_{pp}}{2\sqrt{2}}$$

$$250\mu = \frac{{V_{pp}}^2}{\left(2\sqrt{2}\right)^2 * 50}$$

$${V_{pp}}^2 = 8 * 50 * 250 * 10^{-6} = 100m$$

$$V_{INp} = \frac{316mV}{2} = 158mV$$

For a Quality factor of 6 to 8 for the series matching network shown in Figure 1.2, we achieve a voltage boost given by

$$V_{IN\_RF} = Q * V_P = (6\ to\ 8) * 158mV \approx 900mV\ to\ 1.2V$$

From the Modulation index of 0.05

$$V_{min} = V_{IN\_RF} - 0.05 * V_{IN_{RF}} \approx 0.9 - 0.9 * 0.05 = 0.99 = 855mV$$

$$V_{sig} = V_{max} - V_{min} \approx 900 - 855 \approx 45\text{mV}.$$

The input of the demodulator is approximately 45mV input

4.2 Block Diagram of Front End of the RFID

The block diagram of the designed demodulator is shown in Figure 4.2.

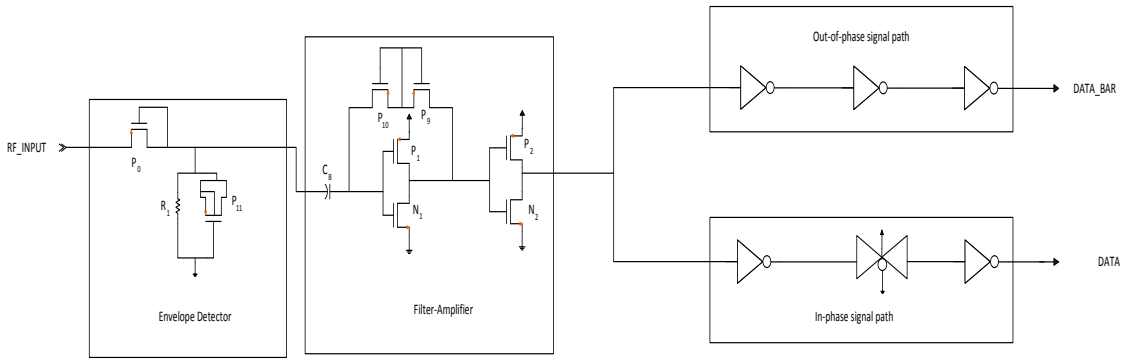

Figure 4.2 Block Diagram of the Designed ASK Demodulator

The designed demodulator design consists of the envelope detector block, amplifier block and the In-phase and Out-of-phase signal path blocks. The outputs of the demodulator include the DATA and DATA_BAR signals.

4.3 The Envelope Detector

The envelope detector is the first block in the demodulator and consists of a MOS diode P_0 along with resistor R_1 and a MOS capacitor P_{11} which is a strong inversion PMOS capacitor. The envelope detector ensures that the condition of input impedance looking into the demodulator$R_{IN} \gg R_L$, this is achieved by using a high value resistor R_1 such that $R_{IN} \approx 10 * R_L$. Since the load of the harvester R_L from Figure 1.2 is 20KΩ, R_1 is selected as 188KΩ and is realized using a RR polysilicon, 8 unit resistors in series having 320nm in width by 5µm in length. The RR polysilicon resistor was selected as it has the highest resistance per unit area. The characteristics of the resistor R_1 is given in table 4.1. The MOS capacitor is made of transistor P_{11} which is a MOS capacitor in strong inversion as its gate is connected to a negative bias compared to its source and drain terminals which are tied together to a higher potential [29]. The

combination of the resistor R_1 and MOS capacitor P_{11} is shown in Figure 4.3 comprise a pre demodulator low pass filter.

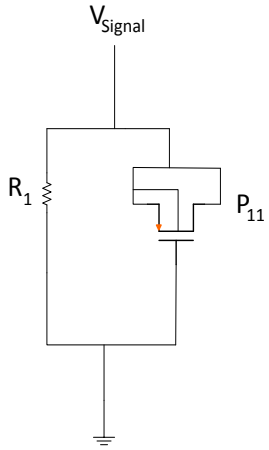

Figure 4.3 Combination of the Resistor R_1 and the MOS capacitor P_{11}

The length and width of the MOS capacitor P_{11} is set at 1µm. Another option is to use zero threshold NMOS devices to realize the MOS capacitor, although in this effort we have selected the PMOS strong inversion MOS capacitor. The total capacitance presented by the MOS capacitor P_{11} is equal to 5fF. The total capacitance presented by the polysilicon resistor R_1 and the MOS capacitor P_{11}, the total capacitance$C_{Total} \approx 100fF$.The time constant($\tau = R_1 C_{Total}$) of this low pass filter is critical and must be selected such that it follows the input envelope yet it should not limit the demodulation bandwidth. The combination of the resistor R_1 and MOS capacitor P_{11} contribute a pole at the location of $\frac{1}{2\pi.R_1 C_{Total}}$.

$$f_{pole} = \frac{1}{2\pi.20x10^{-9}} = 7.95MHz$$

The temperature variations can cause an increase in the Resistance in the resistor, every resistor type available in the process possesses a unique temperature coefficient which is a function of the material used to realize that resistor[29]. To ensure that the envelope detector does not limit the bandwidth of the demodulator f_{pole} is set such that it is much greater than the bandwidth of

operation of the demodulator, this is further discussed in Section 4.6. An important criteria for the time constant is given by as

$$1/f_{RF} \ll \tau \ll 1/f_{DATA}$$

Where f_{RF} is the frequency of the carrier wave and f_{DATA} is the digital data rate.

For $R_1 \approx 200K\Omega \; and \; C_{Total} \approx 100fF.\; \tau \approx 200x10^3x100x10^{-15} \approx 20ns$, $1/f_{RF} = \frac{1}{900MHz} = 1.11ns$ and $1/f_{DATA} = \frac{1}{450KHz/2} = 1.11\mu s$

Table 4.1 Characteristics of RR Polysilicon Resistor R_1

Characteristics	RR Polysilicon Resistor
Drawn Dimensions	Length = 5µm; Width = 0.32µm Number of bars in series =8; Number of bars in parallel =1
Resistance Calculated	24.028KΩ@25℃
Error	1.88Ω@-50℃;0.11Ω@25℃;0.49Ω@125℃ Tolerance = 22%
Resistor Mis-match %	Model Mismatch = 7.16%; Data Mismatch = 5.94%
Parasitic Capacitance	Capacitance from PDK Plots $\approx 10fF$, Total Parasitic capacitance≈80fF

Error denotes the difference between the measured and the model data.

Data Mismatch represents the calculated mismatch based on 20 sites from each of 3 wafers from 3 lots[33].

4.4 The Filter-Amplifier

The filter-amplifier consists of a blocking capacitor C_B, first stage amplifier and a second stage amplifier as shown in Figure 4.3, this structure is similar to the one used in [53]. The amplifier consists of a complementary common-source amplifier with a feedback resistor realized using PMOS transistors P_9 and P_{10} as shown in Figure 4.4.

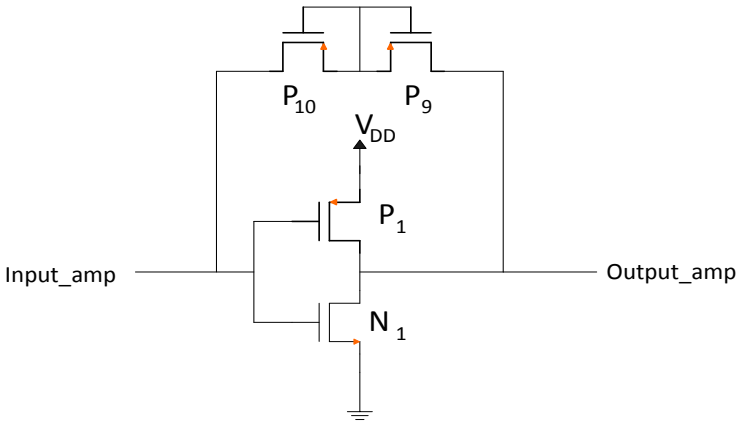

Figure 4.4 Complementary Common Source amplifier with feedback resistor

4.4.1 Feedback Resistor

In order to understand the working of the complementary C-S amplifier we need to first understand the working of the feedback network consisting of the transistors P_9 and P_{10}. This arrangement is shown in detail in Figure 4.6. This feedback arrangement ensures that the dc voltage of the input and the output voltage of the amplifier is equal and at $V_{DD}/2$ or the trip point. The small signal equivalent of the feedback network is depicted in Figure 4.7.

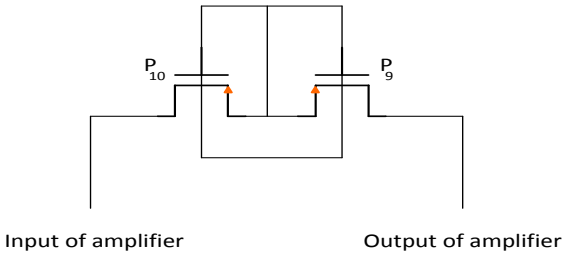

Figure 4.5 Feedback resistor network

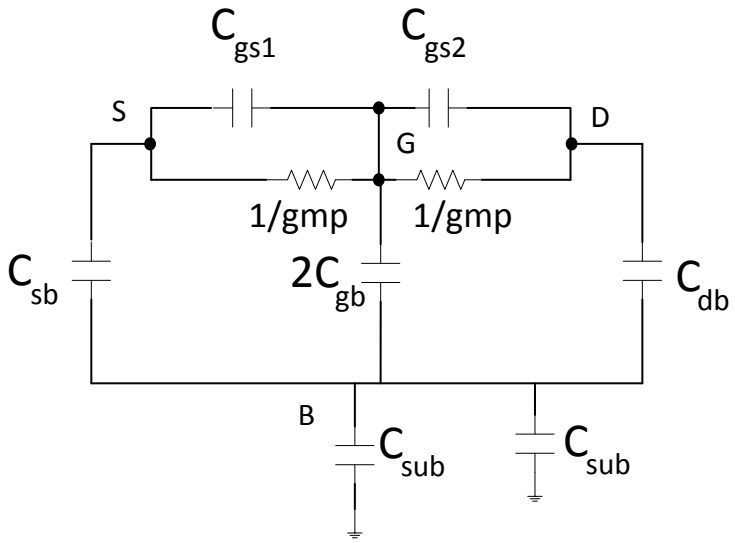

Figure 4.6 Small signal equivalent of the feedback network

Both the transistors P_9 and P_{10} are operating in the weak inversion regime and the gate-to-source voltage for both of these transistors is approximately zero. In such a scenario both transistors are considered off, although one of the two transistor is slightly more on than the other due to offset voltage at the gates of these devices. These off-state PMOS transistors are set at minimum geometry of 220nm/180nm which possess a threshold voltage of -384mV.As the devices are off, and operate in the accumulation mode we approximate the current through these devices with the weak inversion model $g_m = \frac{I_D}{nU_T}$

In the case of an off-state device$I_D \approx I_{OFF}$, the gm expression for the off-state PMOS with V_{GS} = 0 and assuming an offset voltage of 5mV, $V_{DS} = 5mV$

$\mu_p C_{ox} \approx 70\mu A$

$$1/gm_p = \frac{nU_T}{I_{OFF}} = \frac{nU_T}{2nU_T^2 \frac{W}{L}\mu_p C_{ox} e^{-|V_{TP}|/nU_T}\left(1 - e^{-V_{DS}/U_T}\right)}$$

$$1/gm_p = \frac{1}{2 * 25 * 10^{-3} * 70 * 10^{-6} * \frac{220}{180} * e^{-384/50mV}(1 - e^{-5/50})} \approx 5.25G\Omega$$

The equivalent resistance of the feedback network $R_F = 1/gm_p + 1/gm_p = 2/gm_p$ at low frequencies

$R_F \approx 2 * 5.25G\Omega = 10.5G\Omega$ At low frequencies.

The parasitic capacitors associated with the off-state transistors include the gate-to-source capacitance $C_{gsp1\&2}$ of transistors P_9 and P_{10}. Increasing the width of the feedback transistors would reduce the resistance whereas the parasitic capacitance would increase which would reduce the effective impedance presented by these off-state transistors. From Figure 4.7 we see that the parasitic capacitances C_{sb}, 2*C_{gb}, C_{db} along with the C_{sub} capacitance form a ground path giving rise to a pole whereas the series combination of C_{gs1} and C_{gs2} ($C_{gs1/2}$ = 35aF from simulation) contributes to a zero as the signal feeds directly to the output in this case. Calculating the locations of the poles and zeros:

$$f_{zero} = \frac{1}{2\pi\, R_F(C_{gs1}||C_{gs2})} = \frac{1}{2\pi * 10.5G\Omega * (35 * 10^{-18}||35 * 10^{-18})}$$

$$f_{zero} = \frac{1}{2\pi * 10.5 * 10^9 * 17.5 * 10^{-18}} = 866KHz$$

C_{bb} capacitance for each transistor is 171.9aF≈172aF whereas the parallel combination of C_{gb} , C_{sb} and C_{db} are given as $C_{eq} = C_{gb} + C_{sb} + C_{db}$ = (111 + 60 + 60) aF = 230aF. Hence 2* C_{sub}> C_{eq} we ignore C_{sub} in the expression.

$$f_{pole} = \frac{1}{2\pi R_F * C_{eq}} = \frac{1}{2\pi R_F(2\,C_{gb} + C_{sb} + C_{db})} = \frac{1}{2\pi * 10.5G\Omega * (230 * 10^{-18})} = 65KHz$$

In order to verify the locations of the pole and the zero we need to setup a test bench for the feedback network and pass an alternating current through it and observe the voltage across the feedback network. Figure 4.8 shows the test bench used to characterize the frequency response of the feedback arrangement.

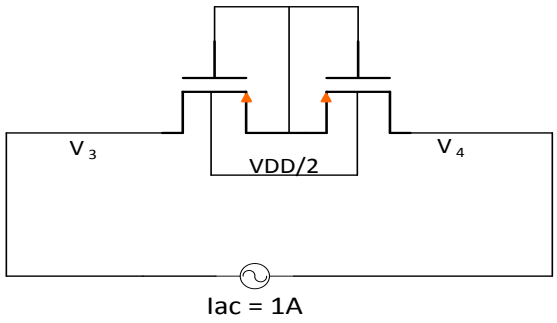

Figure 4.7 Test setup to observe the frequency response of the feedback network

The simulated values of V_3 and V_4 across a frequency range of 1Hz to 1GHz is shown in Figure 4.9. Since the ac current in the test setup is at 1A, the resistance offered by the feedback network would be the same value of the voltage but would have the units of Ωs. V=IR, if I = 1A then the V(V) = R(Ω). From Figure 4.9 it is evident that the ac resistance offered by the feedback network rolls off at placement of the pole and recovers some when the zero frequency is reached. The following section will look at the amplifier working and how this high feedback resistance assists the working of the amplifier.

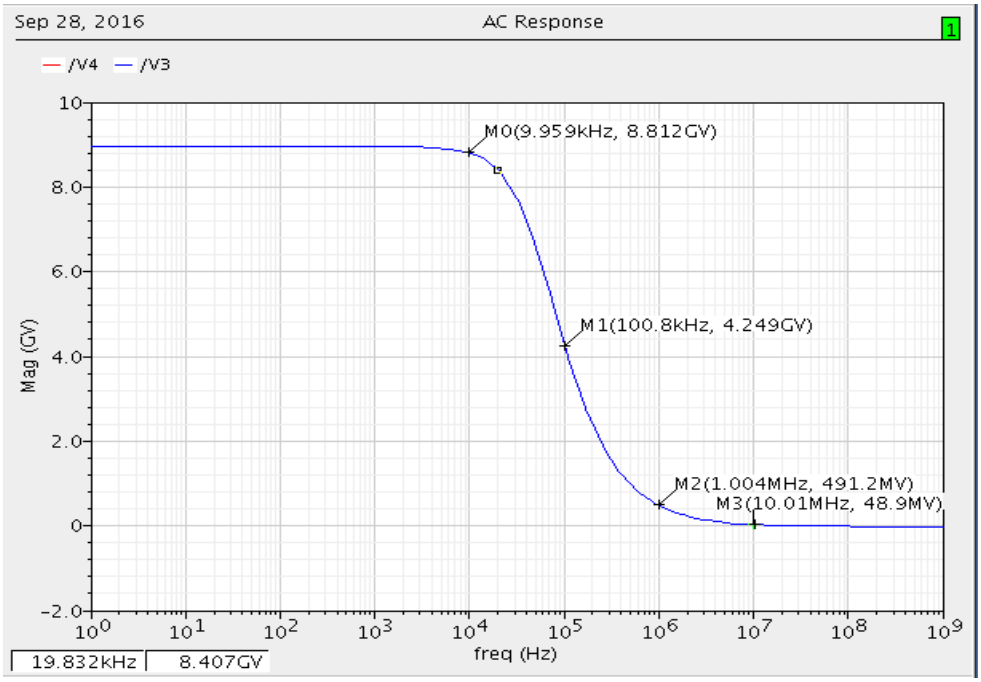

Figure 4.8 Frequency response of the feedback resistor network

4.4.2 First Stage amplifier Working

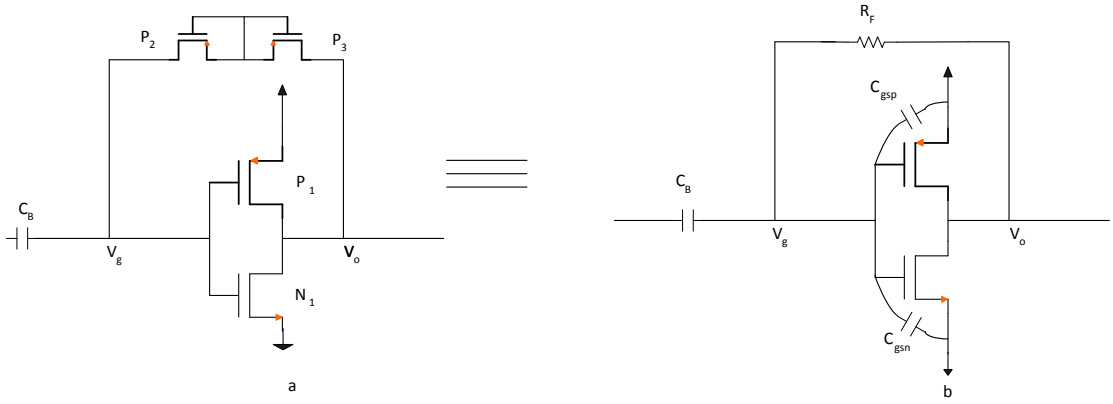

Figure 4.9 (a) shows the amplifier circuit and (b) Depicts its equivalent circuit.

The trip point of the amplifier is set nearly at $\frac{V_{DD}}{2}$ = 350mV. The threshold voltage of the NMOS and the PMOS transistors comprising of the amplifier are greater than 350mV (-406.7mV for the PMOS and 415mV for the NMOS, elaborated in Chapter 5). This implies that the amplifier operation takes place in the subthreshold (moderate inversion) region. For the worst case i.e. -

25℃ at the slow-slow corner the amplifier would be operating in the weak inversion region with a reduction in the operating bandwidth as observed in Chapter 2. In order to ensure that the amplifier is fast enough we model the transistor in weak inversion as follows[34]:

$$f_T \alpha \frac{\mu_n U_T I_D}{L^2 I_M} \alpha \frac{1}{L^2}$$

Where $f_T$the transition frequency, I_M is the maximum drain current that flows in weak inversion, L is the length of the device and μ_n is the mobility of the carriers in the channel. When considering the transition frequency of transistors operating in strong inversion velocity saturation the transition frequency is given as follows[34]

$$f_T \alpha \frac{1}{2\pi} \frac{g_m}{C_{gs}} \alpha \frac{W C_{ox} v_{scl}}{W L C_{ox}} \alpha \frac{v_{scl}}{L}$$

Where v_{scl} represents the scattering limit velocity of the minority charge carriers in the channel. In the case of moderate inversion the channel current is a combination of both drift and diffusion current there is a need to sweep the length of the transistors such that we are able to support the bandwidth of interest. Increased device length ensures a lower static current I_D and a lower static power dissipation $(V_{DD} * I_D)$ follows. It is therefore beneficial to operate with the largest possible device length that affords us the bandwidth of interest. The choice of length and width are addressed in Section 4.6.

From Figure 4.10, the voltage at the node V_g is given by

$$v_g = v_{in} \frac{C_B}{C_B + (C_{ggn} + C_{ggp})}$$

Hence if we set sizing of the capacitor C_B such that $C_B >> (C_{ggn} + C_{ggp})$, $v_g \approx v_{in}$. C_B is a selected as a MIM capacitor with a value of 1.281pF. The total input capacitance $(C_{ggn} + C_{ggp}) = 16fF$ for the geometries discussed in Section 4.6. The role of the blocking capacitor is to allow the ac

content of the signal to pass at the input of the amplifier. From section 4.4.1 it is was found that the feedback resistor provided a resistance of 10.5GΩ at low frequencies, which is a very high value, in such a case the signal at the input of the amplifier will flow through the amplifier and the amplifier would operate in its open-loop configuration and we would assume the feedback resistor will look like an open circuit to any incoming ac signal. Hence the complementary C-S amplifier works in the open-loop configuration and the feedback resistor R_F much greater than the output impedance provided by the complementary C-S amplifier such that we can neglect it when solving for the small signal model of the amplifier. The small signal equivalent of the amplifier is shown in Figure 4.10.

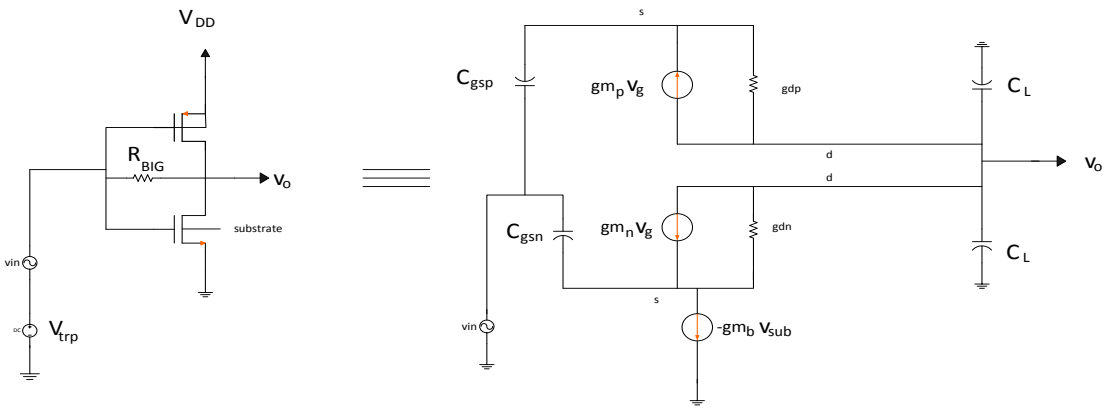

Figure 4.10 Small signal equivalent of the amplifier

Writing KCL equation for the drain node

$$v_{in}\left(gm_n + gm_p + v_o\left(g_{dn} + g_{dp} + 2.s.C_L\right)\right) = 0$$

$$\frac{v_0}{v_{in}} = -\frac{(gm_n + gm_p)}{gd_n + gd_p + 2.s.C_L}$$

The expression for the f_{3dB} is given by:

$$\mu_{eff} = \frac{gm_n + gm_p}{gd_n + gd_p} = (gm_n + gm_p)(r_{on}||r_{op}) \; and \; f_{Teff} = \frac{1}{2\pi}\frac{gm_n + gm_p}{Cgg_n + Cgg_p}$$

$$f_{3dBeff} = \frac{\mu_{eff}}{f_{Teff}}$$

Assuming that the PMOS and NMOS are beta matched we get $gm_n \approx gm_p \approx gm$

$$\frac{v_o}{v_{in}} = \frac{-2.gm}{2gd + 2.s.C_L} = \frac{-\mu}{(1 + s\,C_L/gd)}$$

The above equation shows that there is a pole at $-gd/C_L = \frac{-1}{C_L.(r_{dsn}||r_{dsnp})}$ and the DC gain = μ= gm •r_0. Here the symbol μ has been used as the self-gain of the transistor and not to confuse this symbol for the mobility of the electrons or holes that is more frequently associated with the symbol μ. In the following text unless mentioned explicitly μ will represent the self-gain of the associated transistor. The C_L for the amplifier is the C_{gg} (Cgs+Cgd) of the inverter following the amplifier. If the second stage of the complementary C-S amplifier has the same geometry as the first stage, the C_L for the first stage of the amplifier would equal its own C_{gg}. For the amplifier the C_{gg} at 27℃ for TT process corner we get 16fF.The value of $g_{dsp} \approx 750nS$ and $g_{dsn} \approx 900nS$ at 27℃ for TT process corner, for a worst case scenario where the pole is dependent on the lowerg_{ds} among the PMOS and NMOS, we consider that the PMOS g_{ds} lowers the pole value since it has the lower value. Computing the location of the pole of the amplifier as follows

$$\omega_{pole} = \frac{750*10^{-9}}{16*10^{-15}} \equiv f_{pole} = \frac{750*10^{-9}}{2\pi*16*10^{-15}} = 7.46MHz$$

The bode plot of the AC response of the amplifier from simulation is shown in Figure 4.11. From the plot we can see that the f_{3dB} for the amplifier is at 7.37MHz.

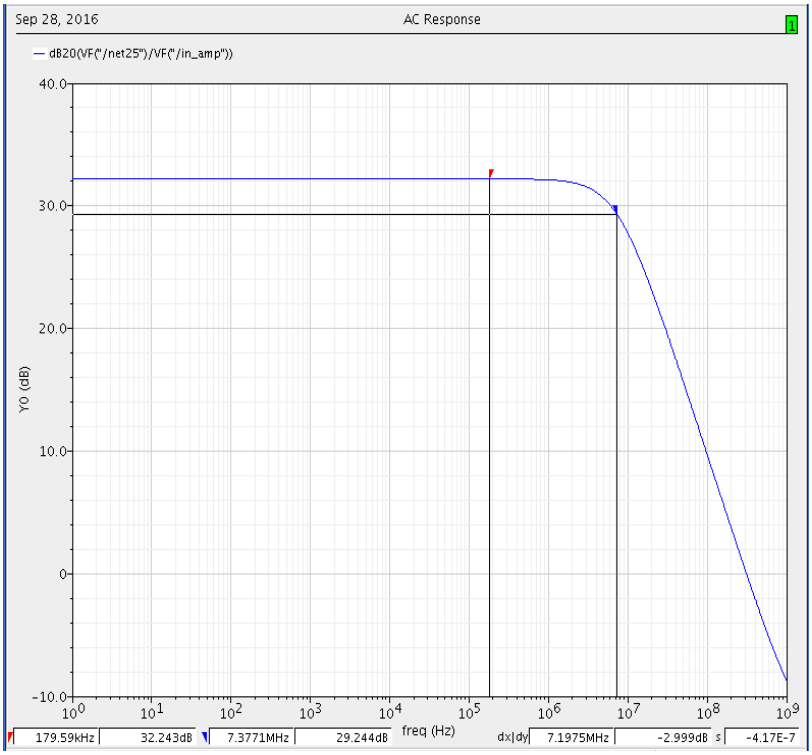

Figure 4.11 Bode plot of the AC response of the Complementary C-S amplifier

To ensure that the complementary C-S amplifier operates in the open-loop configuration which is its intended configuration we need to ensure that the feedback resistance R_F is much greater than the effective output impedance of the complementary amplifier r_{0eff}. In such a case ($R_F >> r_{0eff}$) the gain of the amplifier is the effective intrinsic gain μ_{eff}. The width of the transistors constituting the complementary C-S amplifier are set according to the offset requirement which is explained in detail in Section 4.6.

4.4.3 Second Stage amplifier

The second stage of the amplifier is another complementary C-S amplifier without the feedback network acting as both an amplifier and a logic inverter/comparator, since the input of this second stage is biased at $V_{DD}/2$ by the output of the first stage it acts as an amplifier providing gain whereas its output node is connected to logic gates which causes its output to swing thereby

partially acting as a logic inverter. The design of this second stage is based on the need for additional gain. The sizing of the second stage of the amplifier is identical to the first stage in order to reduce the mismatch between the first and the second amplifier stages. In order to limit the mismatch we keep the same geometries for the first and second stages. Table 4.2 gives a summary of all the poles and zeros of the various blocks in the design and compares the calculated values and the simulated results, these poles and zeros are important in terms of understanding the behavior of each block across the frequency spectrum.

Table 4.2 Demodulator block Characteristics

Block	Calculated	Simulated Result
Envelope Detector	$f_{pole} = 7.95MHz$	-
Feedback Resistor	1) $R_F \approx 10.5G\Omega$ 2) $f_{pole} = 65KHz$ 3) $f_{zero} = 866KHz$ 4) -	1) $R_F \approx 8.8G\Omega$ 2) $f_{pole} \approx 10KHz$ 3) $f_{zero} \approx 1MHz$ 4) $R_F \approx 50m\Omega$ @$10MHz$
C-S Amplifier	1) $f_{3dB} = 7.46MHz$	1) $f_{3dB} = 7.37MHz$

In the feedback resistor analysis we have not taken into account the parasitic capacitance involved in the layout which would give us a closer value to the simulated result of 10 KHz.

4.5 Phase Splitter

The block diagram of the phase splitter is shown in Figure 4.12.

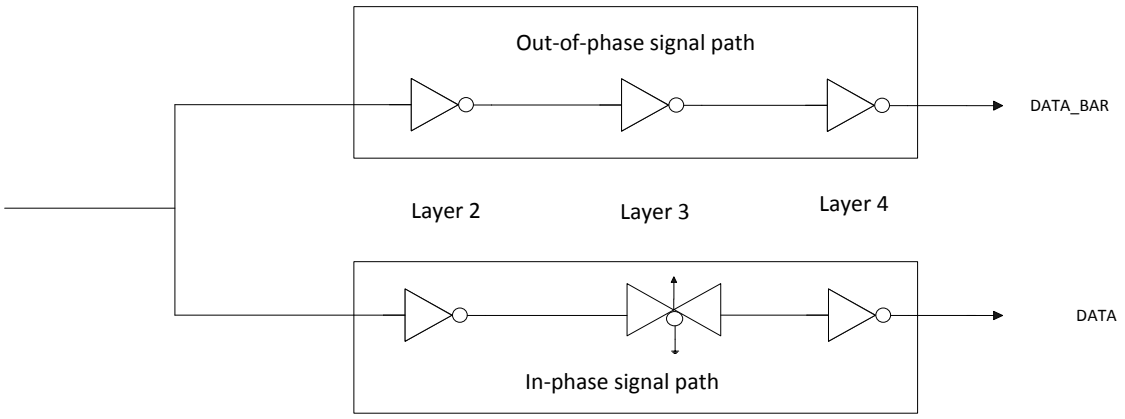

Figure 4.12 Phase splitter block diagram

The phase splitter consists of two branches, the In-phase signal path which gives the demodulated representation of the baseband signal as the output DATA and the Out-of-phase signal path gives the complement of the baseband signal as the output DATA_BAR. The In-phase path consists of an inverter, followed by a transmission gate and another inverter. The out-of-phase path consists of three inverters back to back. The transistors constituting the entire chain (both in-phase and out-of-phase) have their lengths set to minimum geometry i.e. 180nm in order to reduce the rise and fall times in the logic waveforms. The voltage waveforms at the output of the inverters in layer 2 are a logic level, also as the gains in the amplifier and the inverter following it are fairly high (>>1) the offset produced by the inverter layers 2-4 do not contribute significantly to the effective offset at the input of the amplifier as their offset contribution is divided by the gain of both the both stages of the amplifier when referred to the input of the first stage. . The offset of the inverters in layer 2, 3 and 4 can however effect the voltage at the output of the second stage of the amplifier, for that reason the geometric width of these inverters is kept at $\frac{W_{amp}}{2}$ while at the same time as they are logic devices their power contributions are insignificant, increasing the geometry further does not achieve any significant improvement. In this design the inverter chain is not designed such that the delay is minimized, [54] has a discussion on how to optimize the

delay while driving higher and lower loads in an inverter chain. Another important detail that may be an issue for optimized and synchronized DATA and DATA_bar signals is that the In-phase signal path yielding the data signal contains a transmission gate whereas the DATA_bar chain contains an inverter in layer3. The rise and fall times for the inverter and the transmission gate would differ.

4.6 Design Objective

The design objective is to obtain reasonable functioning of the Demodulator for a temperature range of -25℃ to 125℃ across process corners of Slow-Slow (ss), Typical-Typical (tt) and Fast-Fast (ff). The design is carried out for $\pm 3\sigma$ accuracy.

The major parameters involved in optimization are:

1. Bandwidth of the first and second stages of the filter amplifier:
   f_{3dB1} and f_{3dB2} respectively
2. The Offset of the first and second stages of the filter amplifier: V_{os1} and V_{os2}
3. Gain of the first and second stages of the filter amplifier: μ_1, μ_2
4. Total Power Consumption of the Demodulator

4.6.1 Bandwidth of the first and second stage amplifier:

The bandwidth of the first and second stages of the amplifier needs to be such that it supports enough harmonics of the baseband signal for successful demodulation. Baseband signal = 450 KHz, in order to demodulate the signal efficiently we need to demodulate 5 to 9 harmonics of the baseband signal. To understand the relationship of the number of harmonics with the signal content we need to examine a baseband square wave signal and its Fourier series. Assuming that the square is represented by f(x) where x represents the time axis, then its Fourier series expression is as follows:

$$f(x) = \frac{4}{\pi}\sum_{n=1,3,5....}^{\infty}\frac{1}{n}\sin\left(\frac{n\pi x}{L}\right) \equiv f(x) = \frac{4}{n\pi}\begin{cases}0 & n\ even\\ 1 & n\ odd\end{cases}$$

Where 2*L denotes the length of the square wave in the x direction.The greater the number of harmonics demodulated, the higher the frequency content as each odd harmonic contains 4/nπ signal content. After a certain number of harmonics, we would reach the point of marginal returns when the higher harmonics demodulated do not contain enough signal content, although designing steps taken to demodulate all these higher harmonics would decrease the demodulator efficiency. In this design we demodulate up to the 9th harmonics of the baseband signal. Location of the 9th Harmonic = 9 x 450 KHz = 4.05 MHz = f_{9th}.The requirement for efficient demodulation can be expressed as $f_{3dB} > f_{9th}$ where f_{3dB} is the bandwidth of the amplifier and f_{9th} is the ninth harmonic of the baseband signal. For a single stage, demodulating 9 harmonics v/s 5 harmonics proves to be less power efficient. Since we have two stages we need to demodulate a greater number of harmonics to ensure satisfactory operation as the effective bandwidth of a cascade of amplifier stages reduces with increase in number of stages[55]. Hand calculations for f_{3dBeff} are cumbersome and laborious hence we invoke the use of a parametric sweep of L to get the same equal PMOS and NMOS bandwidth. As we have seen the transition frequency is a function of length, we are operating in moderate inversion@27℃ it would be more efficient to take more Monte Carlo samples while sampling the various DC parameters, 1000-10,000 would be a more meaningful than 200 samples that were common place for earlier designs. From Chapter 2 we established that the threshold voltage of the transistors varies on account of process variations and temperature variations, considering worst case scenarios the threshold would vary about ±100mV(@1mV/℃) due to temperature and ±50mV due to process variation. This means we are anticipating a variation of ±150mV variation of the threshold, such high variation can cause the transistors to either operate in weak inversion or in strong inversion velocity saturation. In weak inversion the variation in threshold is very high and the bandwidth is low, in such a scenario the design may fail and to ensure that such a situation is not encountered

we need to take more Monte Carlo sample. Moderate Inversion operation is not well modelled and weak inversion operation is associated with high variability. The operating point of the amplifier in the design is critical, hence through a high number of samples we intend to ascertain this operating point to a better extend under worst case threshold variations. For the required bandwidth we set the length of the NMOS transistor in the first and second stages of the filter amplifier to 500nm. The Monte Carlo data for $f_{3dB}$of the NMOS transistor in the first stage suggests that the worst case is 4.88 MHz for 10,000 runs for process and mismatch, with a mean of 12.73MHz and $\sigma = \pm$ 2.885MHz which is shown in Figure 4.13, the worst case f_{3dB} of the NMOS device in the amplifier is higher than the f_{9th}. Similarly for the PMOS transistor we have Figure 4.14 which shows the $f_{3dB}$of the PMOS transistor in the first stage. The worst case f_{3dB} for the PMOS in the first stage is 4.58MHz having a mean of 12.91MHz and $\sigma = \pm 3.527MHz$ for a length of 200nm. The length of the devices is limited to a minimum of 180nm and any increments can be made in additions of 10nm for the IBM CMOS7RF 0.18µm process, hence a reduction of the length to 190nm would reduce the worst case f_{3dB} below the f_{9th} harmonic of the baseband signal.

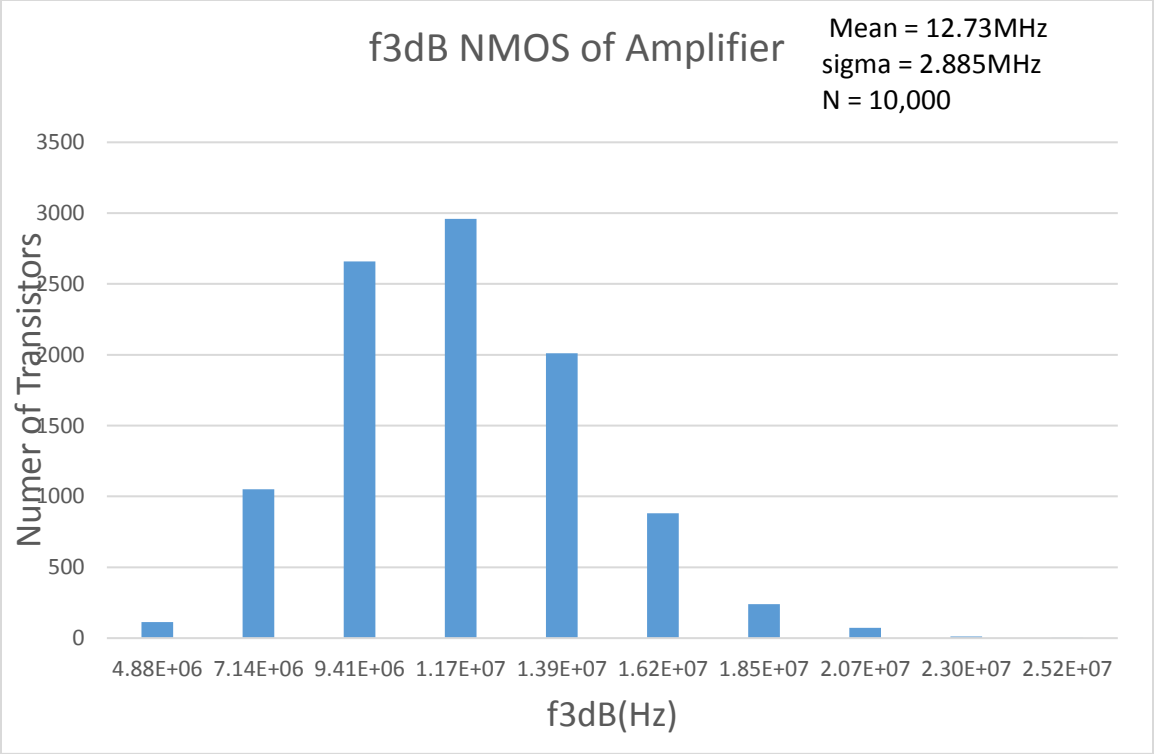

Figure 4.13 Monte Carlo data for f3dB of the NMOS transistor in the Complementary C-S amplifier

It can be argued that the effective f_{3dB} of the amplifier is higher than the f3dB of a single transistor, yet we are taking a conservative approach in order to identify the limiting transistor and designing accordingly such that any effective f3dB would satisfy the bandwidth requirements.

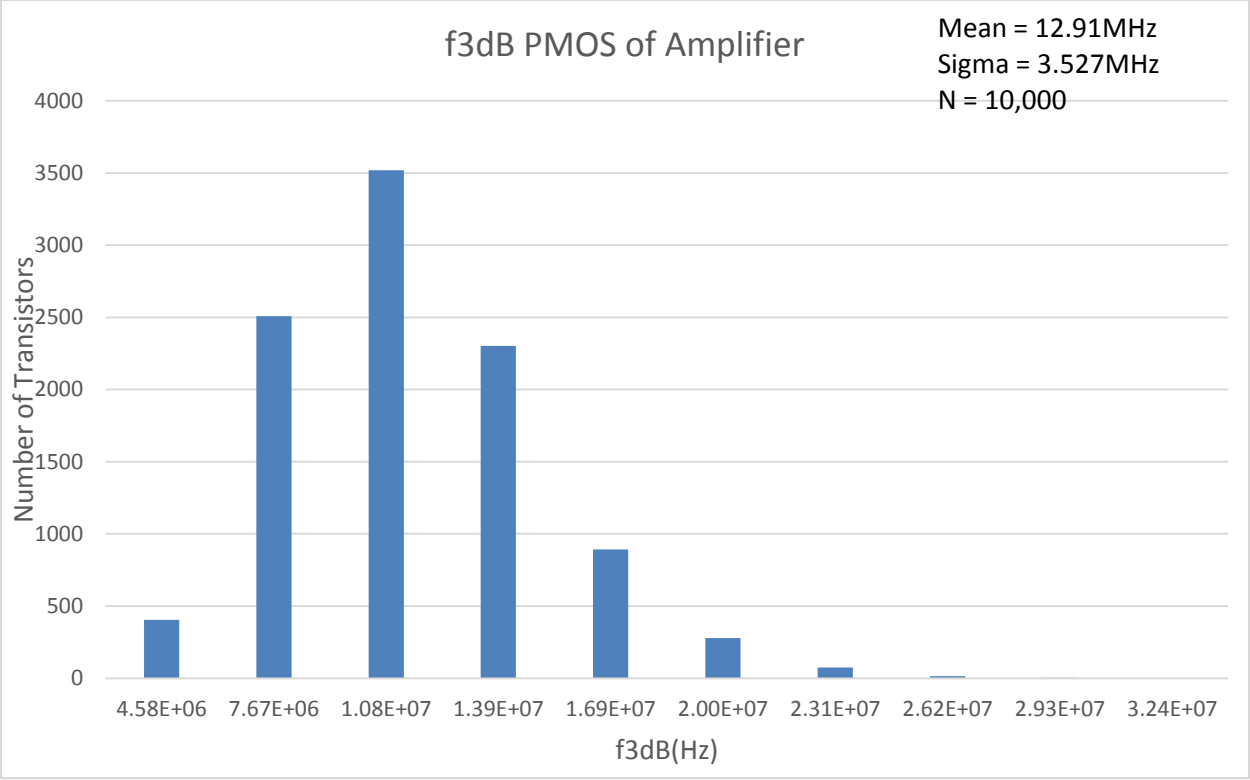

Figure 4.14: Monte Carlo data for f3dB of the PMOS transistor in the Complementary C-S amplifier

4.6.2 The Offset of the first and second stage amplifier: $V_{os1}\ and\ V_{os2}$:

The offset of the first and second stage of the complementary C-S amplifier is caused due to the variability of the PMOS and NMOS devices constituting them. The offset voltage at the input of the amplifier must be negligible compared to the input signal.

$$\frac{V_{signal}}{4} \gg V_{OS(amp)}$$

$$\frac{45mV}{4} \gg V_{OS(amp)} \equiv V_{OS(amp)} \ll 11.25mV$$

The mobility of the carriers in the channel of the PMOS and the NMOS differ, there is a need to match their mobility to effect equal currents flowing through them. This matching of mobility of the NMOS and PMOS known as beta matching and is completed by weighting the NMOS and

PMOS geometries such that the current flowing through them is the same and independent of VT and L. The matching of the NMOS and PMOS for the weak inversion model can be done as follows:

$$I_P = I_N$$

Using the notation of μ_n ,μ_p for the mobility of electrons and holes respectively for the rest of this section.

$$2n.\mu_p.C_{ox}\left(\frac{W}{L}\right)_p {U_T}^2\, e^{\left(\frac{V_{GSP}-V_{THP}}{nU_T}\right)} = 2n.\mu_n.C_{ox}\left(\frac{W}{L}\right)_n {U_T}^2\, e^{\left(\frac{V_{GSN}-V_{THN}}{nU_T}\right)}$$

$$V_{THN} = 415mV\ ;\ V_{THP} = -405mV\ ;\ V_{trip} = 350mV$$

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n e^{\left(\frac{350-415}{2*26}\right)}}{\mu_p e^{\left(\frac{350-406}{2*26}\right)}}$$

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = 0.84\ \frac{\mu_n}{\mu_p}$$

The mobility of the electrons is about 3-4 times the mobility of the holes in the 180 nm process[16]

Assuming $\mu_n \approx 4\ \mu_p$

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} \approx 3.36$$

The matching of the NMOS and PMOS in strong inversion velocity saturation can be done as follows:

$$I_P = I_N$$

$$W_p C_{ox} v_{scl_p}(V_{GSp} - V_{thp}) = W_n C_{ox} v_{scl_n}(V_{GSn} - V_{thn})$$

$$\frac{W_p}{W_n} = \frac{v_{scl_n}(V_{GSn} - V_{thn})}{v_{scl_p}(V_{GSp} - V_{thp})}$$

Since the operation of both the PMOS and the NMOS transistors constituting the complementary C-S amplifier operate in moderate inversion the current flowing through both transistor have to be equal at the trip point of $V_{DD}/2$, in such a case it is not possible to obtain $gm_n = gm_p$, since both the NMOS and PMOS transistors have different threshold voltages, although we can aim to design for $gm_n \approx gm_p$. As the matching condition for weak and strong inversion is different, it is difficult to current match these transistors. For transistors operating in moderate inversion the current has two components one that follows weak inversion approximation (diffusion current) and the other follows the strong inversion approximation (drift current), making matching a difficult task. The process variation is going to be uniform for the entire design as the area of the demodulator would be less than 200µm X 200µm, as seen in Chapter 2 such a scenario implies that the local variation is dominant over the global variation. The first stage does not contribute to the offset at its output due to the feedback resistor which ensures that the input and output of the first stage are at the same dc potential. For this to be true the leakage current flowing in the feedback resistor has to be negligible such that the voltage drop across the feedback resistor is given by $I_{leak} * R_F$ is negligible. The offset in the system is due to the mismatch in the PMOS devices of the first and second stage and the NMOS devices in the first and second stage amplifiers. The expression for the mismatch between the first and the second stage is given by

$$V_{OS} = \sqrt{\frac{{A_{VTP}}^2}{(W * L)_{PMOS}} + \frac{{A_{VTN}}^2}{(W * L)_{NMOS}}}$$

Since the Length of the devices is selected by the bandwidth requirements, this gives us the freedom to increase the width of the devices in order to achieve the desired offset. At this point we need to ascertain how to increase the width, either increase the width by increasing the unit width and keeping one finger or keeping a smaller unit width and increasing the number of fingers to achieve the offset requirement. As seen from Chapter 2, for a small minimum unit width PMOS device experiences the inverse narrow width effect more strongly. Hence we select the unit width of the PMOS and NMOS transistors at 500nm where the effect of inverse narrow width effect on either transistors is reduced. The increase in the width after that point is done by increasing the number of fingers of the transistors. The geometries of the NMOS and PMOS transistors that make up the complementary C-S amplifier are set such that the offset is driven down and the currents in the PMOS and the NMOS are equal at the trip point. Table 4.3 shows the geometry selection of the PMOS and the NMOS transistors on the first and second stage of the filter amplifier. The DC Monte Carlo simulation results for the GBP and threshold voltage are presented in Chapter 5.

Table 4.3 Demodulator transistor geometries

DEVICE	UNIT WIDTH	UNIT LENGTH	FINGERS	MULTIPLICITY	TOTAL WIDTH	TOTAL LENGTH
P1(PMOS first stage)	500nm	200nm	18	1	9µm	200nm
N1(NMOS first stage)	500nm	500nm	10	1	5µm	500nm
P2(PMOS second stage)	500nm	200nm	18	1	9µm	200nm

N2(NMOS second stage)	500nm	500nm	10	1	5µm	500nm
P3-P8(PMOS of inverters from layers 2-4)	500nm	180nm	9	1	4.5µm	180nm
N3-N8(NMOS of inverters from layers 2-4)	500nm	180nm	5	1	2.5µm	180nm

Calculating the resulting offset due to variability

$$V_{OS}(amplifier/inverter) = \pm\sqrt{\frac{(7mV-\mu m)^2}{9\mu m x 0.2\mu m}+\frac{(12mV-\mu m)^2}{5\mu m x 0.5\mu m}}$$

$$\pm 3\sigma\, V_{OS} = . \pm\sigma = 3.066mV$$

A_{VTP} = 7mV-µm and A_{VTN} = 12mV-um[33].

The mismatch observed at the output of the first stage (input of the second stage), although the effective mismatch at this node can be more accurately found by referring the voltage at the output of the second stage amplifier to its input. The voltage at the output of the second stage is shown in Figure 4.15. The σ represents $V_{IN2\sigma} * A_{stage\,2}$, the gain of the NMOS and PMOS devices constituting the second stage is shown in Figure 4.15. The gain for the PMOS device has a mean of 36 whereas the NMOS gain has a mean of 45.6, considering the worst case scenario when the gain of the second stage is 30

$$V_{Out2\sigma} = \pm 101mV$$

$$V_{OSeff} = \frac{V_{Out2\sigma}}{A_{stage\,2}} = \frac{101mV}{30} = \pm 3.366mV$$

The Monte Carlo results for the mismatch at the input of the amplifier is given in Figure 4.15

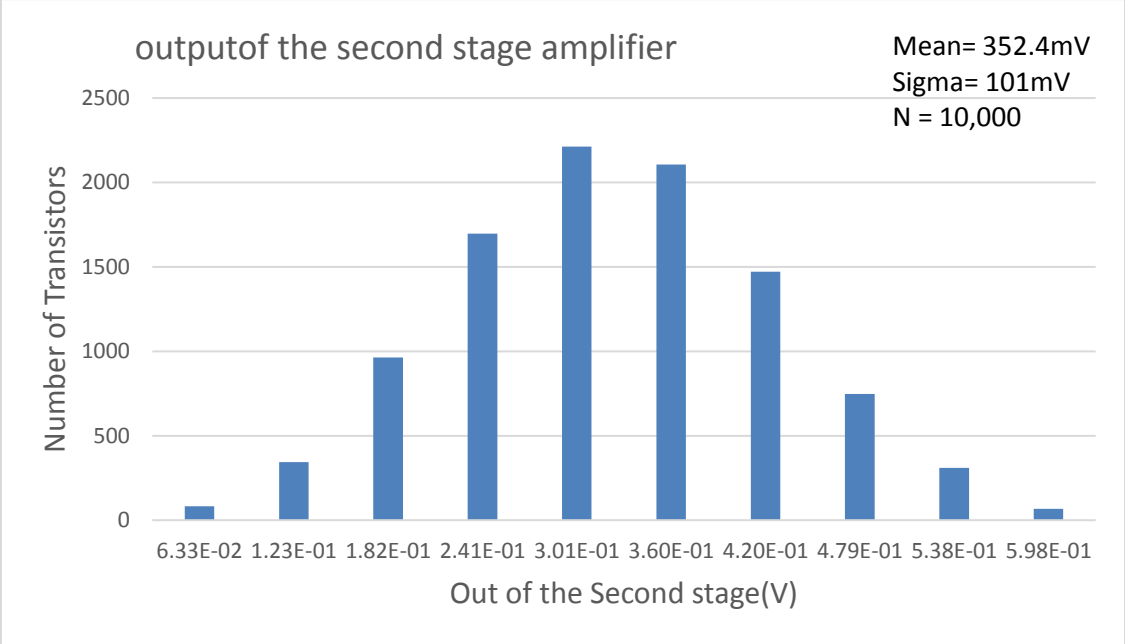

Figure 4.15 Monte Carlo results for the output of the second stage.

Comparing the offset to the KT/C noise we get

$$V_{\frac{KT}{C}}\ \alpha\ \pm\sqrt{\frac{K*T}{C_L}} = \pm\sqrt{\frac{1.38*10^{-23}*300}{16*10^{-15}}} = \pm 508\mu V$$

Since the offset voltage value of 6.5123mV is much greater than the KT/C noise we ignore its contribution in the design objective. An important detail is that when the temperature is at -25℃, the r_{ds} of the amplifier increases to a high value, in order to maintain the condition of $R_F \gg r_{ds}$ the widths of the amplifier transistors may have to be increased. For the SS@-25℃, the values of $gd_n\ and\ gd_p$ are 81.87nS and 96.02nS.

$$rds_{(amp)eff} = \frac{1}{gd_p + gd_n} = \frac{1}{(81.87 + 96.02)10^{-9}} = 5.62145M\Omega$$

The change in the resistance R_F is comparatively lower than the change in the r_{ds} with change in temperature. For a lower temperature and a higher baseband frequency this may be a potential problem..

4.6.3 Gain of the first and second stage amplifier

In order to get a high Signal-to-Noise ratio (SNR) we need enough gain to amplify the signal such that we can make a valid logic decision and the amplified noise does not cause any errors. The noise in system is dominated by the off-set of the devices i.e. the first and second stages. Hence the gain has to be adequate to fulfil the following requirement:

$$\mu_{amp} V_{sig}/4 \gg V_{OS(Total)}$$

The Monte Carlo results for the self-gain of NMOS of the first stage of the filter-amplifier are given in Figure 4.16. The self-gain noted from the Monte Carlo data has a mean of 46.62 and a 1σ deviation of 1.268. Similarly for the PMOS of the first stage of the filter-amplifier the mean is 36.51 with a 1σ deviation of 2.908. The Monte Carlo results for the self-gain of PMOS of the first stage of the filter-amplifier are given in Figure 4.17. For a certain geometry we get a fixed self-gain from the transistor. As we have set the length of the devices to accommodate the bandwidth and the width to drive down the offset, we have no means of changing the self-gain of the amplifier. We have no control over the self-gain of the amplifier, although we need to ensure that the gain is sufficient in order to give us a high Signal-to-Noise ratio. If the geometries selected do not afford us the required gain then there would be a need for addition gain stages in order to increase the gain further.

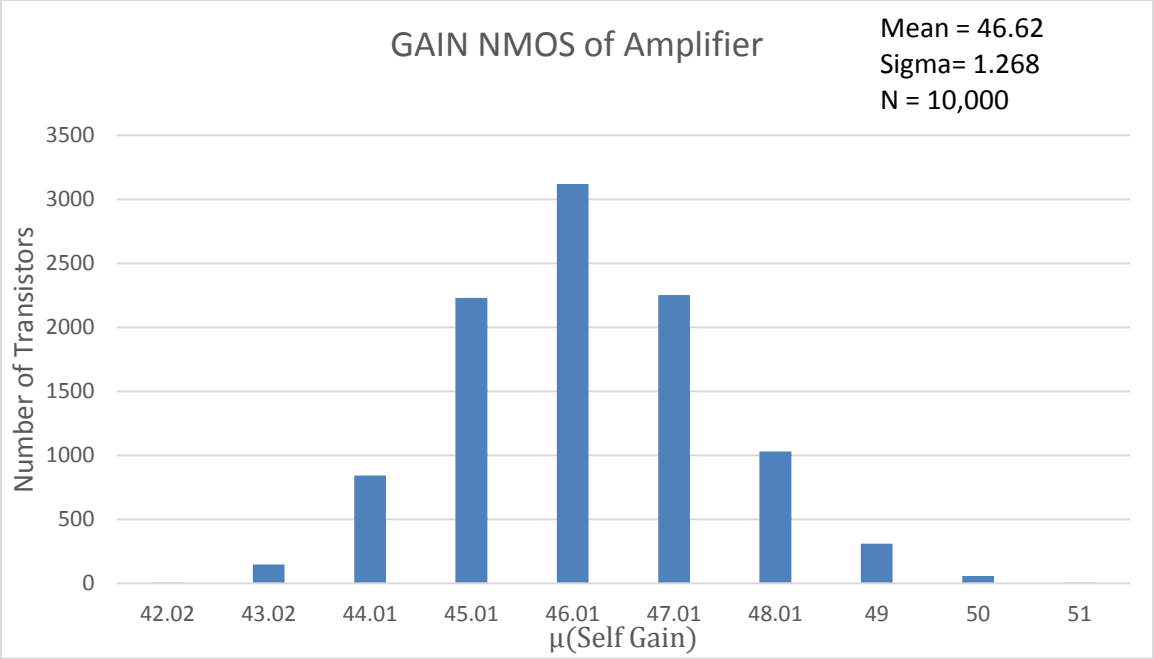

Figure 4.16 Monte Carlo results for self-gain of the NMOS transistor in the Complementary C-S amplifier

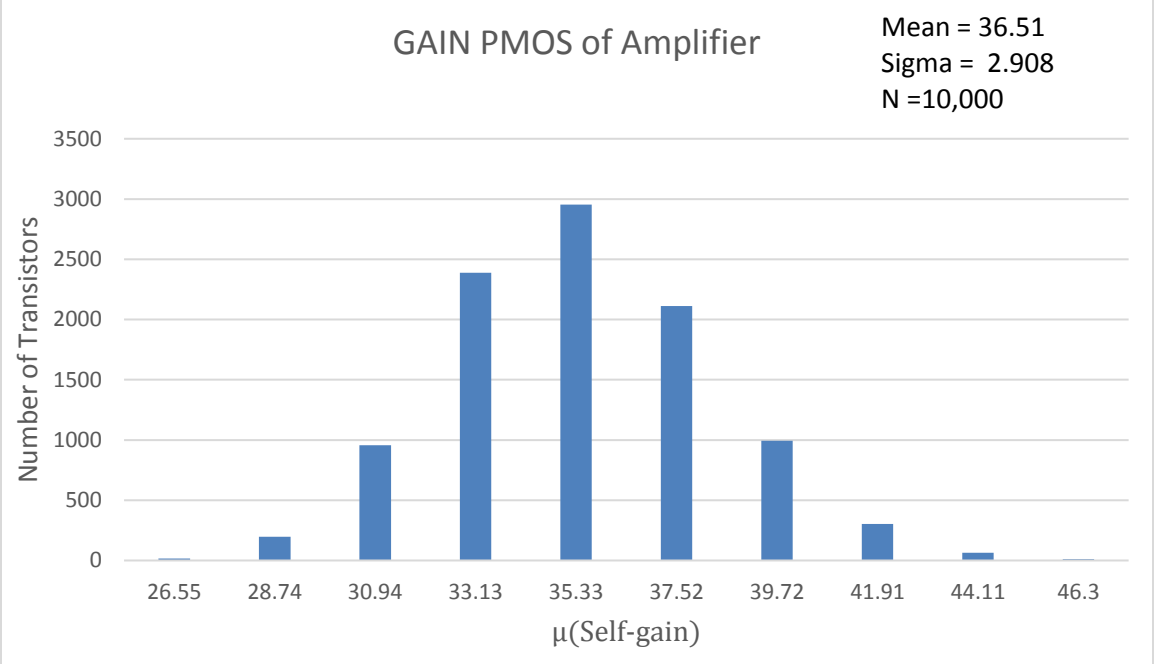

Figure 4.17 Monte Carlo results for self-gain of the PMOS transistor in the Complementary C-S amplifier

To summarize the selection geometry:

- Length: The bandwidth of the baseband signal sets the device length.
- Width: The minimum unit length is dictated by the inverse width effect. The total width is set according to the offset to be achieved, also in a situation of extremely low temperatures the width may be dictated by the r_{ds} of the amplifier.
- The power dissipation in the amplifier and the inverter is set by the geometry of the devices, since the current flowing through the amplifier and the inverter following the amplifier is dependent on the W/L ratio of the devices constituting them. The total average power dissipation is discussed in the following section.

4.6.4 Total Power:

The total power is the average power contributed by the amplifier, the inverter following the amplifier and the inverters consisting of layer2. The power dissipation due to the inverters of layers 3 and 4 only contribute switching power which is negligible to the power of the preceding stages. The expression for the total average power dissipation is given by

$$P_{Total} = V_{DD}\left(I_{D(amp)} + I_{D(inverter1)} + 2.I_{D(inverter2)}\right)$$

$$P_{Total} = 0.7V * (1.219 + 1.219 + 2 * 0.617)\mu A = 2.5\mu W$$

The total power Monte Carlo results for 10,000 samples is shown in Figure 4.18. The total power has a mean of 2.106µW with a 1σ deviation of 689.6nW.

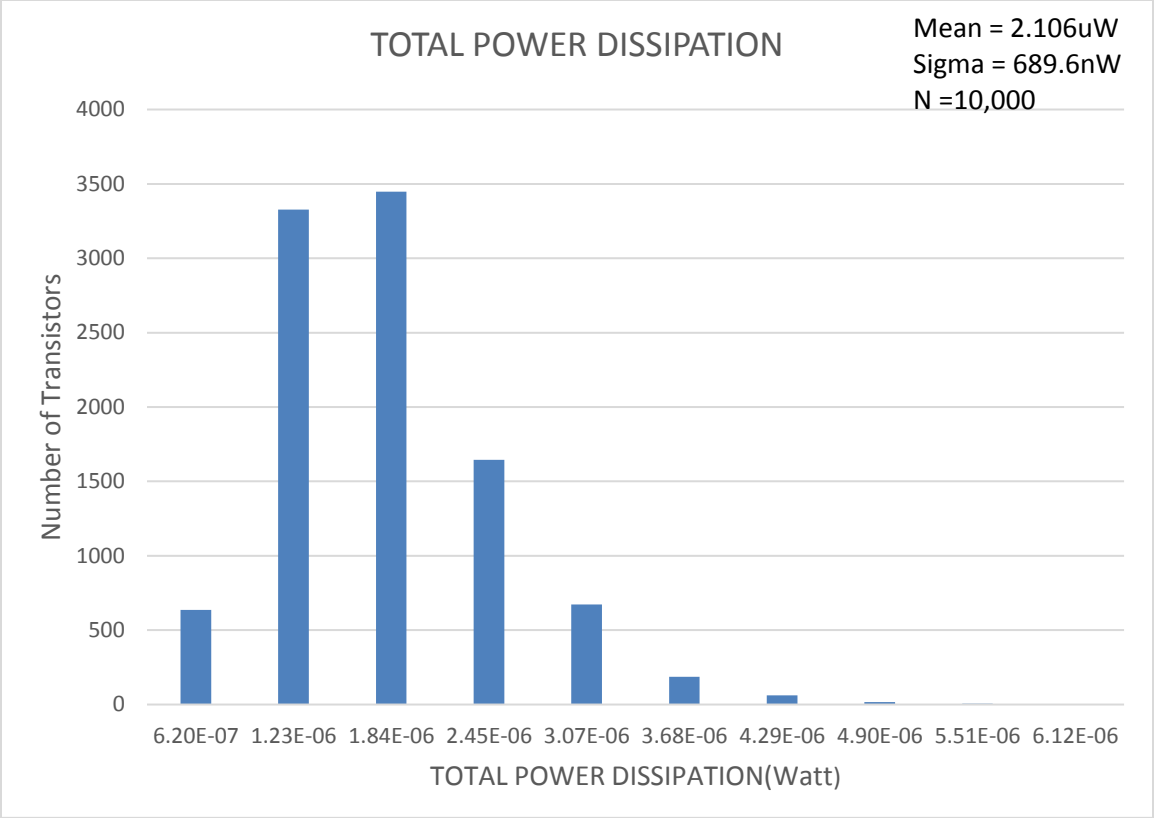

Figure 4.18 Monte Carlo results for Total Power Consumption

As the length and width are set as per the bandwidth and the offset requirements respectively, the total power of the design is only a consequence while fulfilling other design objectives. It may appear that the only lever we have in regard to the total power dissipation is the operating region of the first and second stage of the filter-amplifier. In order to reduce power dissipation we could operate in deep weak inversion, although it may not be possible to achieve the bandwidth objective as weak inversion may not afford us the required bandwidth, also no reduction of device length is permissible below 180nm. There may be no benefit in trying to operate the devices in weak inversion compared to moderate inversion, this is due to the fact that in order to achieve the bandwidth objective there would be a need to reduce device lengths, which would increase the flow of current through the devices, hence any possible improvement for seen by lowering the

operating point to weak inversion may effectively not amount to anything substantial. The performance of the demodulator designed in this effort is tabulated in Table 4.4.

Table 4.4 Performance of the Designed ASK Demodulator

Supply Voltage	Data rate (kbits/s)	Power Consumed at RTM	Modulation Index	Carrier Frequency	Process
700mV	900	2.1µW	5%	900MHz	180nm

4.6.5 Demodulator design specifications

- Input Carrier frequency = 900MHz
- Input Baseband Signal = 450KHz
- Modulation Index = 5%
- Amplifier Gain >30
- Amplifier Bandwidth > 4.05MHz
- Input Power to demodulator = -6dBm
- Total Power Consumed = 2.1µW
- Supply Voltage = 700mV

CHAPTER V

SIMULATION RESULTS

In this chapter we look at the results of the transient simulations for PVT conditions of Typical-Typical @ 27℃, Slow-Slow @ -25℃ and Fast-Fast @ 125℃. The Monte Carlo Simulations results for other circuit parameters not listed in Chapter 4 are also presented. The chapter concludes with the Monte Carlo simulations for the transient conditions for 30 samples. The notations for the various labels in the waveform outputs are listed at the end in the Appendix section. This chapter documents the transient simulation results of voltage waveforms at different nodes in the designed demodulator and DC Monte Carlo results of the Filter-Amplifier constituting the demodulator presented in Chapter 4. These Monte Carlo results are documented for the $\pm 3\sigma$ variation, as mentioned in the design objective in Chapter 4.

5.1 Transient Simulations

The transient simulation results for the voltage waveforms at various nodes of the circuit are given in Figure 5.1 for the typical-typical@27℃ PVT corner for 700mV supply, Figure 5.2 for the slow-slow@-25℃ PVT corner for 700mV supply and Figure 5.3 for the fast-fast@125℃ PVT corner for 700mV supply. For any square wave the ideal duty cycle is 50% for both the logic 1 and logic 0.

$$Duty\ Cycle = \frac{PW}{T}\ x100\%$$

Where PW stands for the pulse width and T for the Time period, the time period of the input waveform is 2.2222µs. The duty cycle for the logic 1 of the output of the demodulator presents a duty cycle of 49.98% whereas the duty cycle for the logic 0 is 50.01% for the fast-fast@125℃ as it is the best case as explained in Chapter 2, similarly the worst case scenario is the slow-slow@-25℃ which has a duty cycle of 56.25% for the logic 1 and 43.75% for the logic 0. In the case of the typical-typical@27℃ the duty cycle for the logic 1 is 53.6% while the logic 0 has a 46.4% duty cycle. We assume that the difference of the duty cycles of the logic 1 and logic 0 from 50% is taken care of by the PLL following the demodulator and that our results are acceptable.

Transient simulation results for TT@27℃

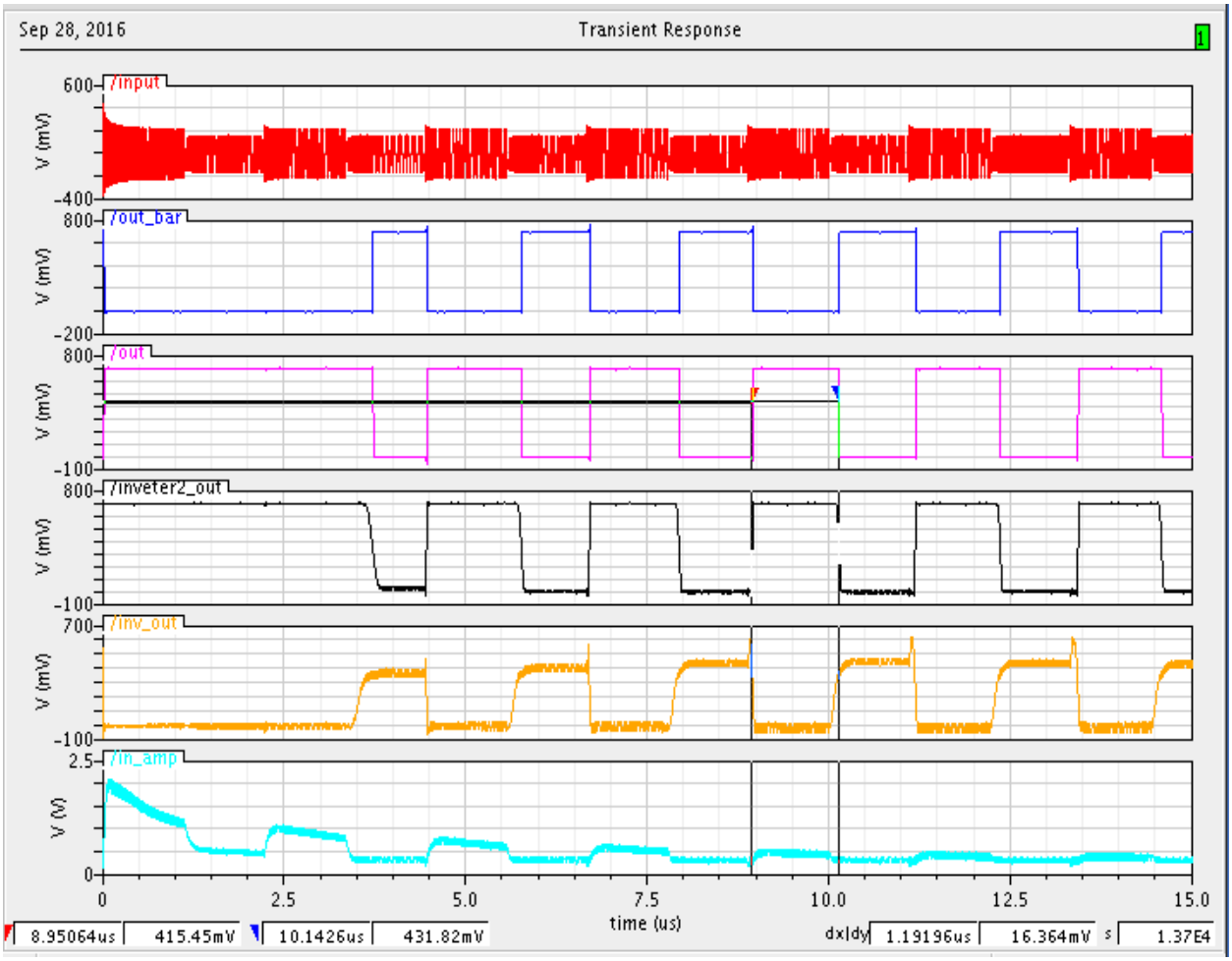

Figure 5.1 Transient simulations for typical-typical process @ 27℃

Transient simulation results for SS@-25℃

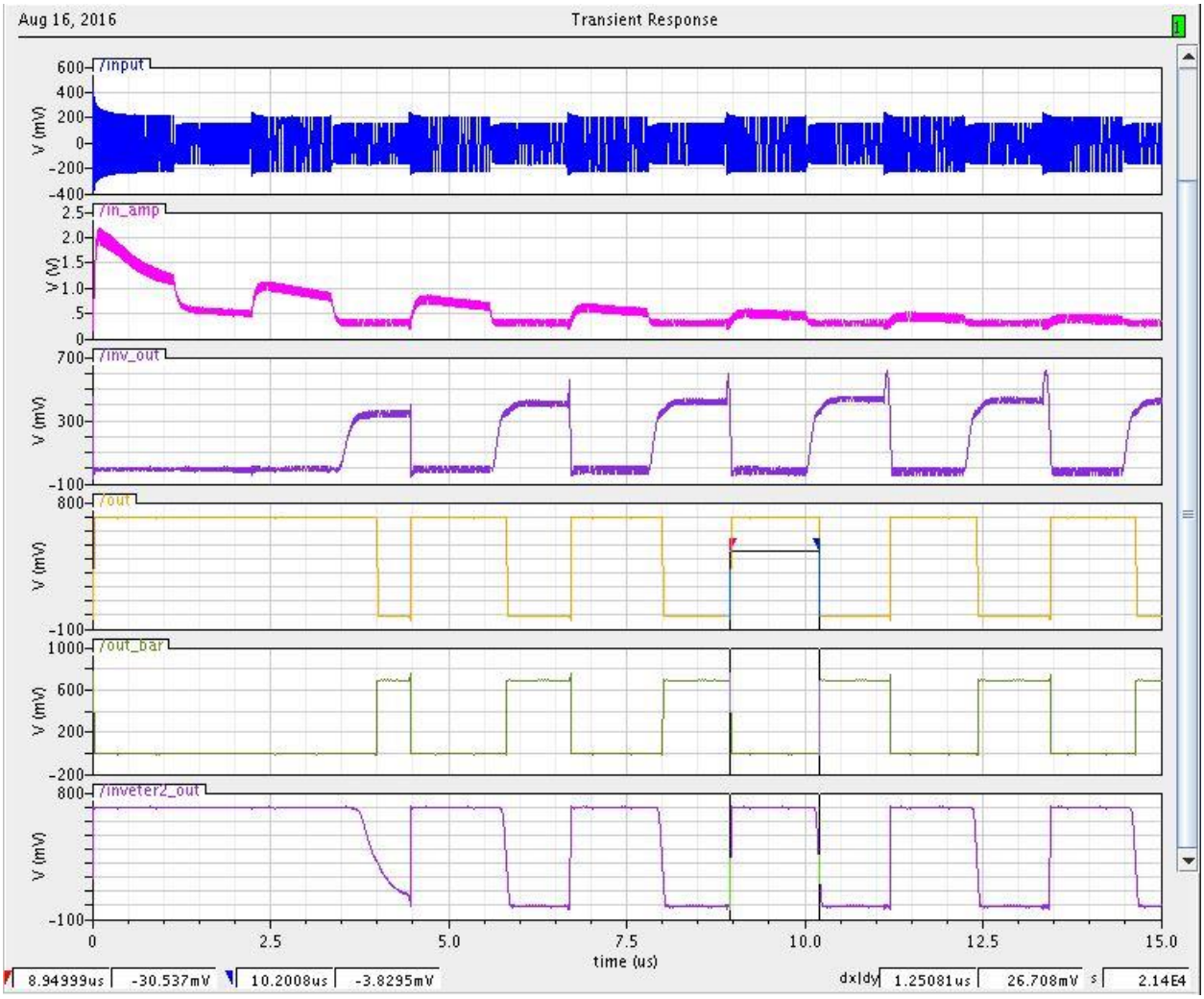

Figure 5.2 Transient simulations for slow-slow process @- 25℃

Transient simulation results for FF@125℃

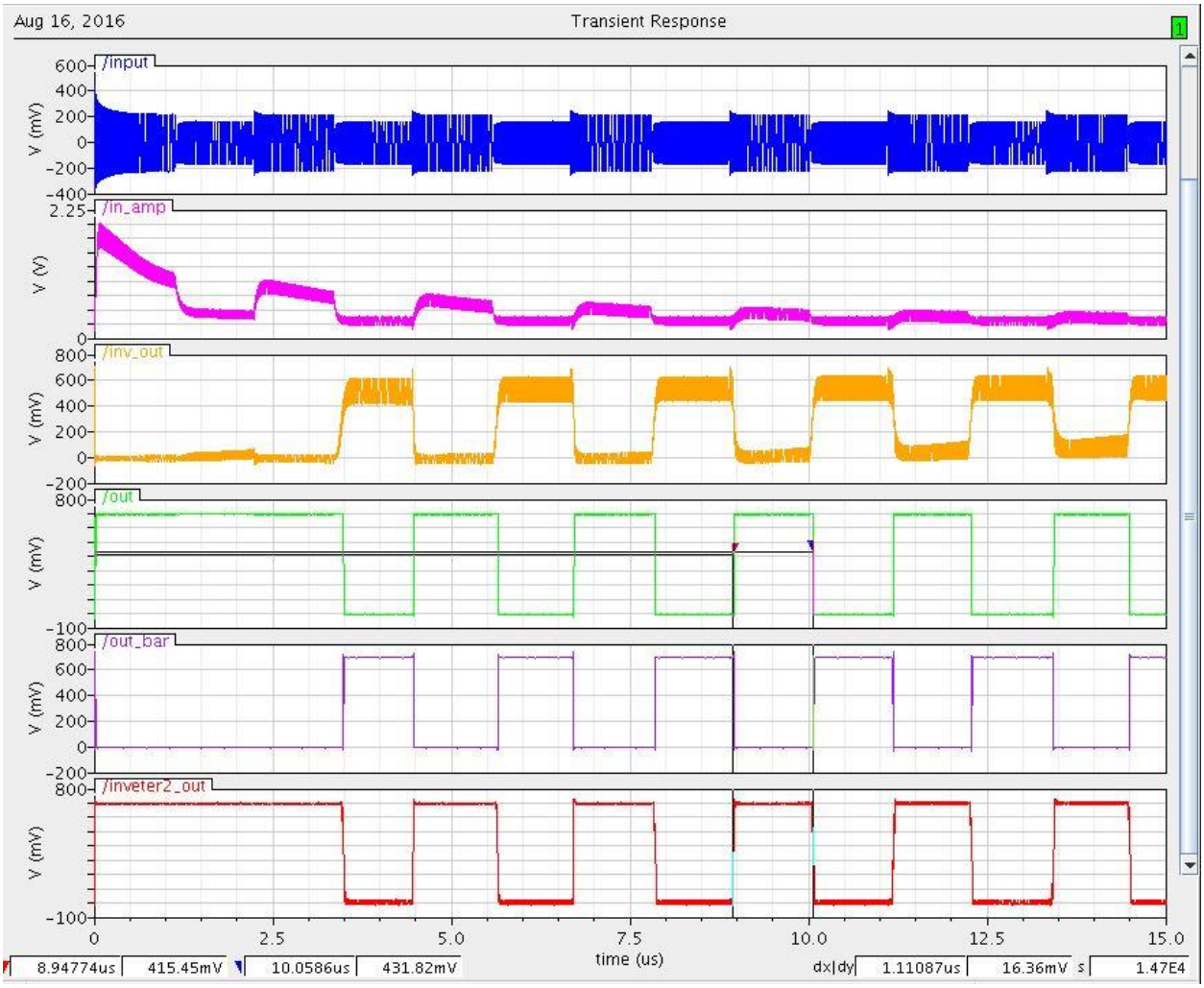

Figure 5.3 Transient simulations for fast-fast process @125℃

5.2 DC Monte Carlo Results:

In this section we present the DC Monte Carlo results for the circuit parameters of the Filter-amplifier which were not discussed in Chapter 4. These parameters include the Gain-Bandwidth-Products and threshold voltages of the individual transistors that make up the first stage Complementary C-S amplifier. The GBPs of the transistors are reviewed in order to check how

closely the NMOS and PMOS of the complementary C-S amplifier are matched in terms of both the gain and the bandwidth whereas the threshold voltage gives us more insight as to the operating regions of each individual transistor and how to design them for equal currents. The matching of the complementary C-S amplifier in Chapter 4 was based on the results of the threshold voltages presented in this section.

5.2.1 First stage of the complementary C-S amplifier DC Monte Carlo results

The GBP of the NMOS and PMOS in the first stage of the filter-amplifier (shown in Figure 4.10(a)) are shown in Figure 5.4 and Figure 5.5.

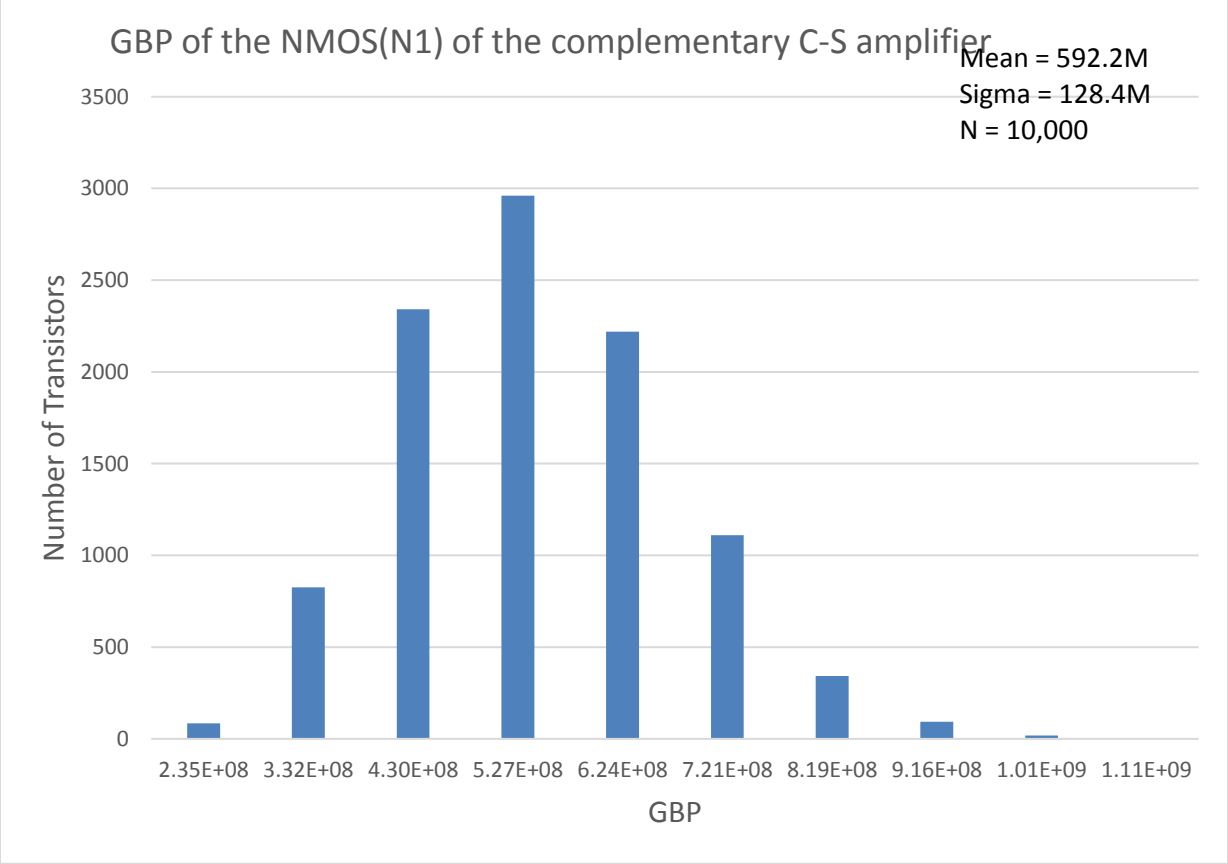

Figure 5.4 GBP of NMOS (N1) in the first stage (complementary C-S amplifier)

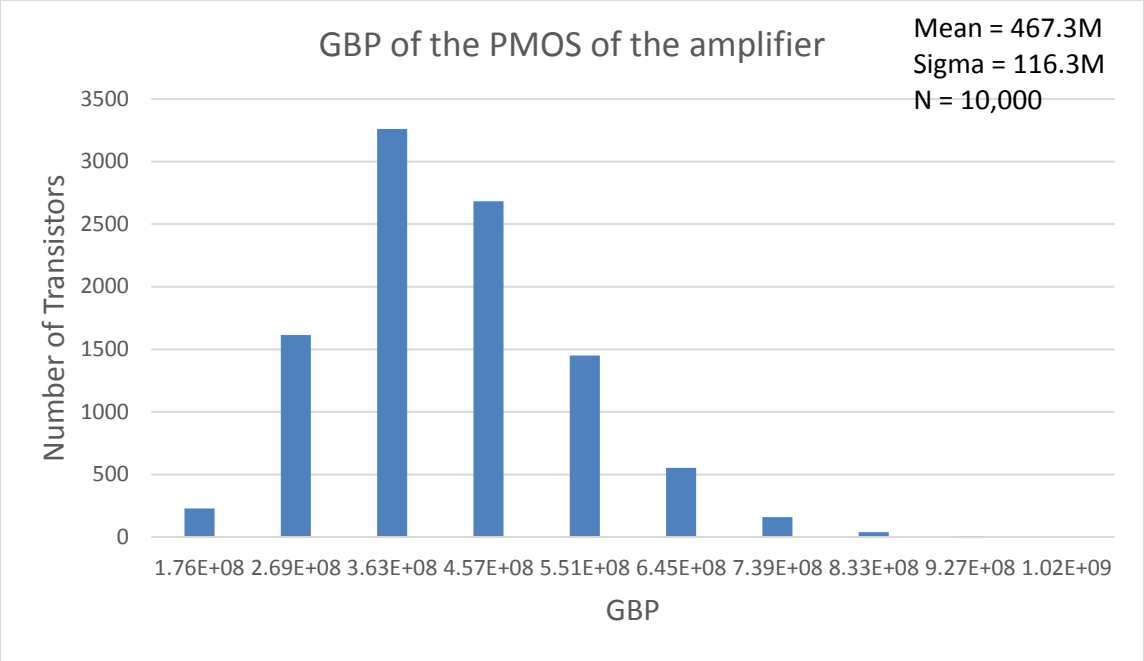

Figure 5.5 GBP of PMOS in the first stage (complementary C-S amplifier)

The Monte Carlo results show that the mean of the GBP of the NMOS device in the first stage (complementary C-S amplifier) is 592.2M with $\sigma = \pm 128.4M$ whereas the mean of the GBP of the PMOS device constituting the first stage (complementary C-S amplifier) is 467.3M with $\sigma = \pm 116.3M$ for N=10,000. As both the NMOS and PMOS transistors are designed in such a way that they individually satisfy all the design objectives, their GBP is a byproduct, although the GBP gives us insight as to how the performance of the NMOS and PMOS compare with each other. The threshold voltage on the other hand has greater importance as the region of operation is a function of the threshold voltage since the gate-to-source voltages on both the transistors is approximately $V_{DD}/2$. The NMOS transistor in the first stage has a mean threshold of 415mV with $\sigma = \pm 17.09mV$ for N =10,000 and the PMOS transistor in the first stage has a mean of -406.7mV and $\sigma = \pm 16.55mV$ for N = 10,000. The threshold voltage of the devices can be modelled by the designer by changing the unit width of the devices and this resultant threshold after the unit width allocation will determine the region of operation. As length is limited by the bandwidth any effect of reverse short channel effects on the threshold have to be endured and

their effects can be reduced by using the appropriate unit widths of the devices utilizing the inverse narrow width effect.

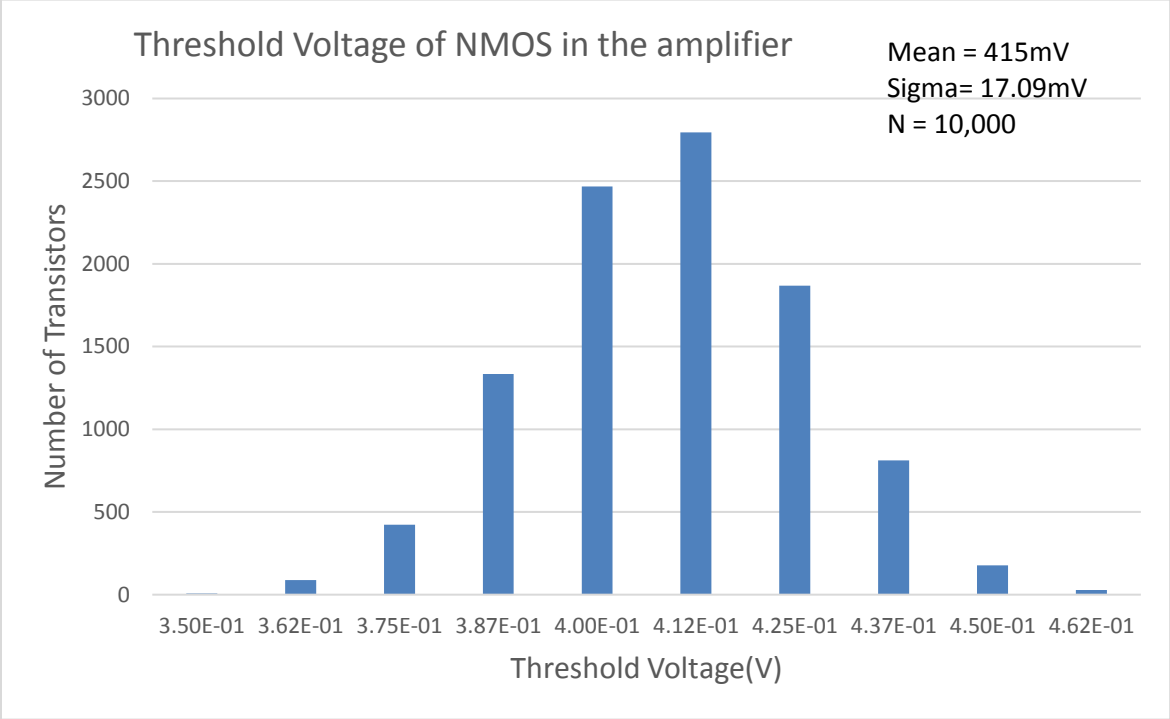

Figure 5.6 Threshold Voltage of the NMOS transistor in the first stage (complementary C-S amplifier)

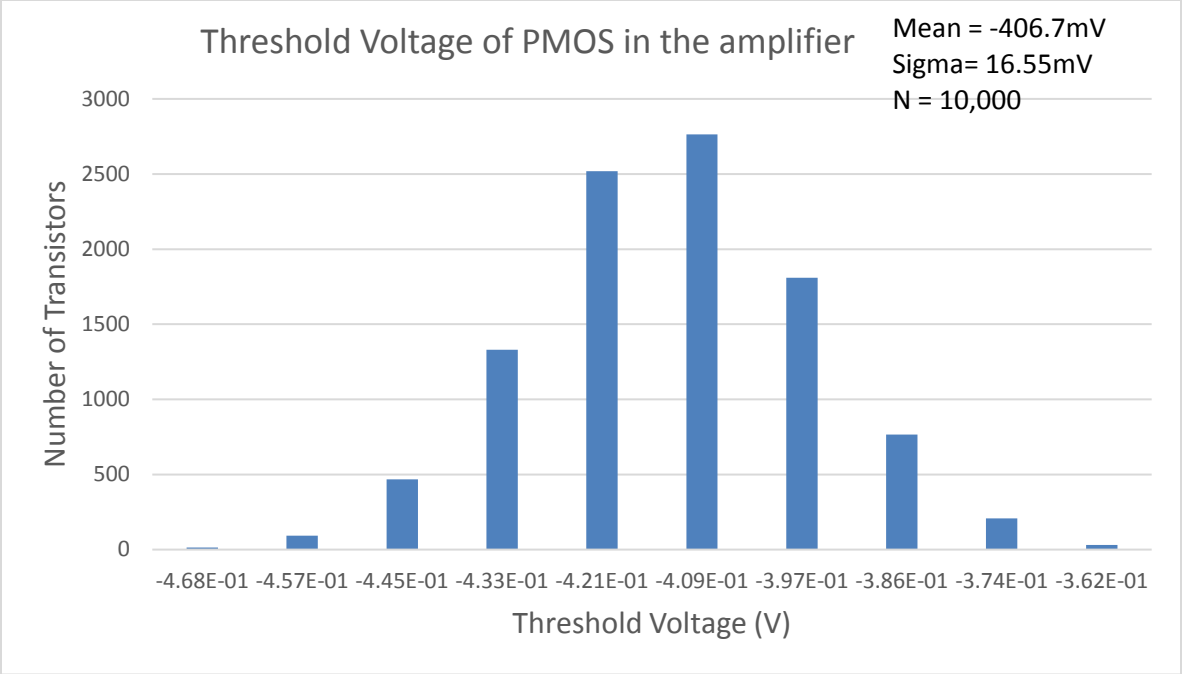

Figure 5.7 Threshold Voltage of the PMOS transistor in the first stage (complementary C-S amplifier)

5.2.2 Monte Carlo results for the second stage of the complementary C-S amplifier

Figure 5.8 shows the first and second stage Complementary C-S amplifier with the second stage in the dashed ellipse.

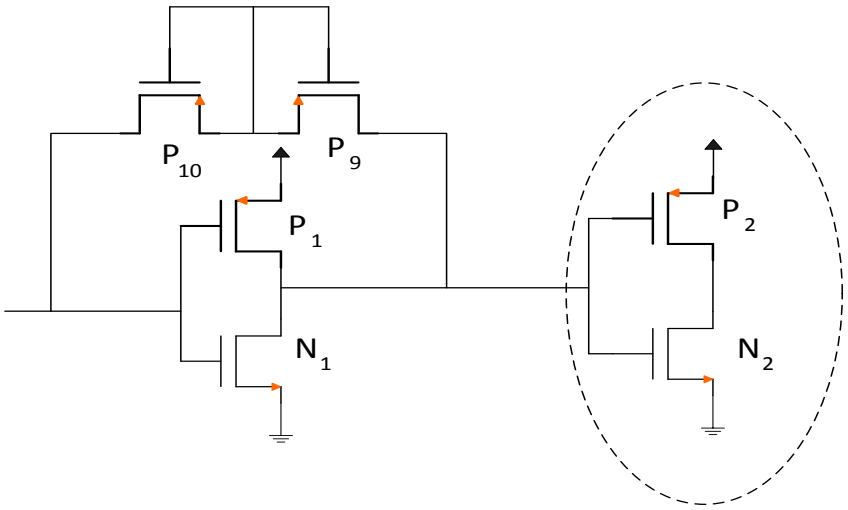

Figure 5.8 second stage Complementary C-S amplifier in the dashed Ellipse

In this section we present the DC Monte Carlo results of parameters such as the f_{3dB}, gain of the transistors constituting the second stage of the filter-amplifier along with its output voltage. The f_{3dB} of the second stage has to meet the bandwidth objective presented in Chapter 4, hence we need to verify the f_{3dB} of the transistors constituting it. The gain is a function of the geometries and since the geometry of the second stage is the same as the first stage we expect to have similar gain as the first stage, although we need to verify that. The threshold voltage of the transistors in the second stage would be identical to the first stage as the unit length and width of the transistors in both stages is the same, hence we do not present them once again. The DC Monte Carlo results for the NMOS and PMOS of the second stage are given in Fig X and Y respectively.

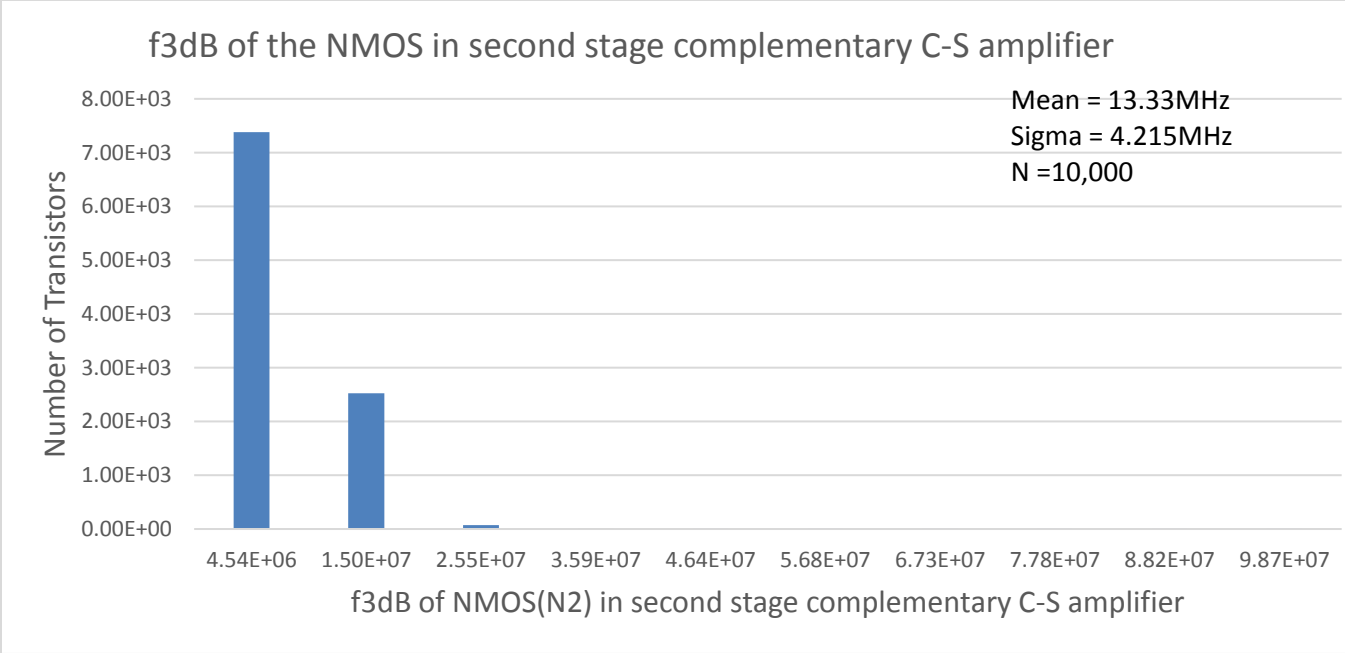

Figure 5.9 f3dB of the NMOS (N2) in the second stage complementary C-S Amplifier

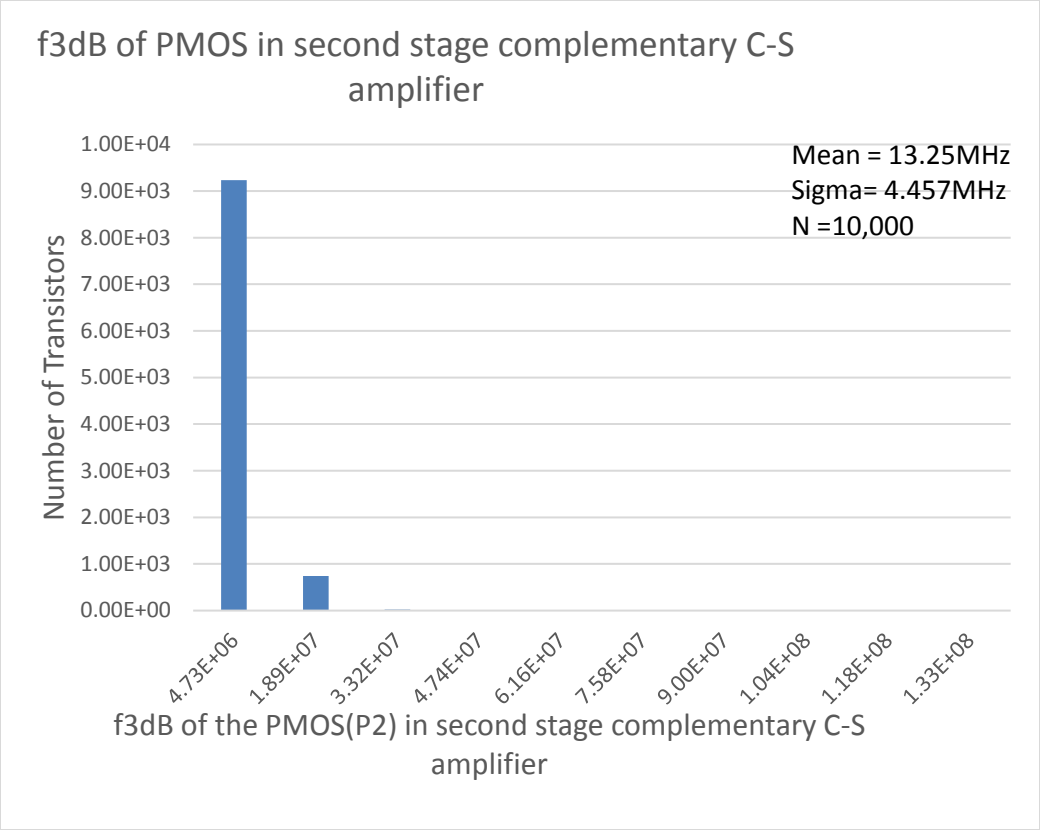

Figure 5.10 f3dB of the PMOS (P2) in the second stage complementary C-S Amplifier

The mean of the f_{3dB} of the NMOS in the amplifier is 13.33MHz with a $\pm\sigma = 4.215MHz$ while the mean for the PMOS device is 13.25MHZ with$\pm\sigma = 4.4575MHz$. As seen from Figures 5.9 and 5.10 that the f_{3dB} of the transistors constituting the inverter following the amplifier have a greater number of samples in the range of 4.5-5MHz, hence any increase in lengths of these devices will adversely affect our bandwidth objective discussed in Chapter 4. The gain of the inverter for the NMOS and the PMOS devices are shown in Figures 5.11 and 5.12 respectively. The NMOS gain has a mean of 45.6 with $\pm\sigma = 6.482$ and the PMOS has a mean of 36 with a $\pm\sigma = 4.183$. The mean gain and bandwidth in the PMOS and the NMOS of the first stage and second stage amplifier are approximately the same although the variation in the gain and bandwidth for the second stage is much greater than that of the first stage. Hence care needs to be taken when designing the cascade such that none of the stages individually impact performance.

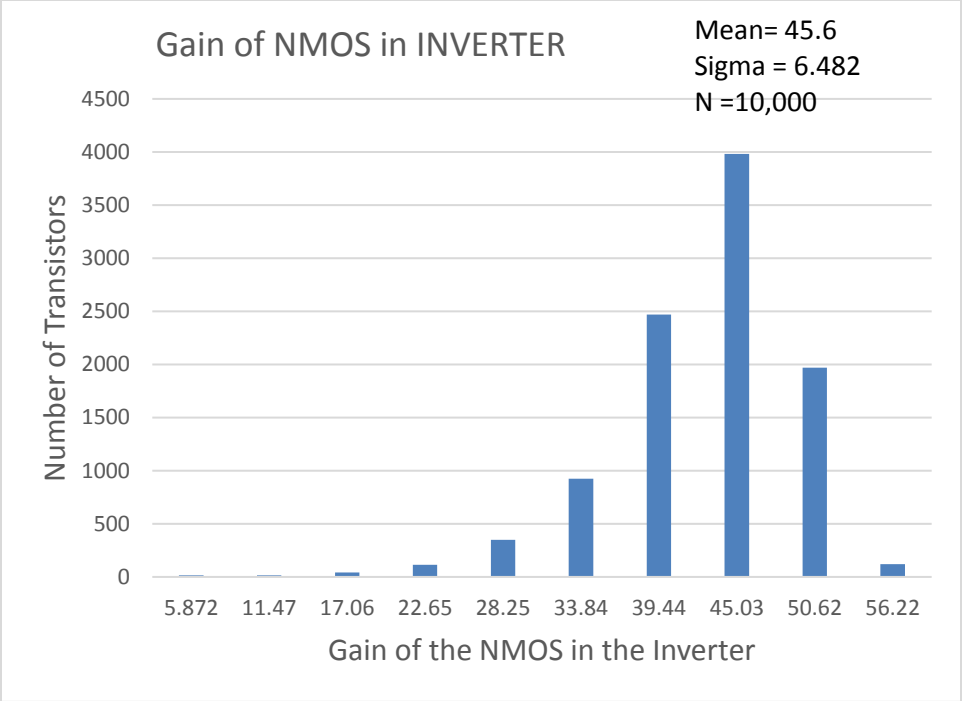

Figure 5.11 Gain of the NMOS in the Second stage of the Complementary C-S amplifier

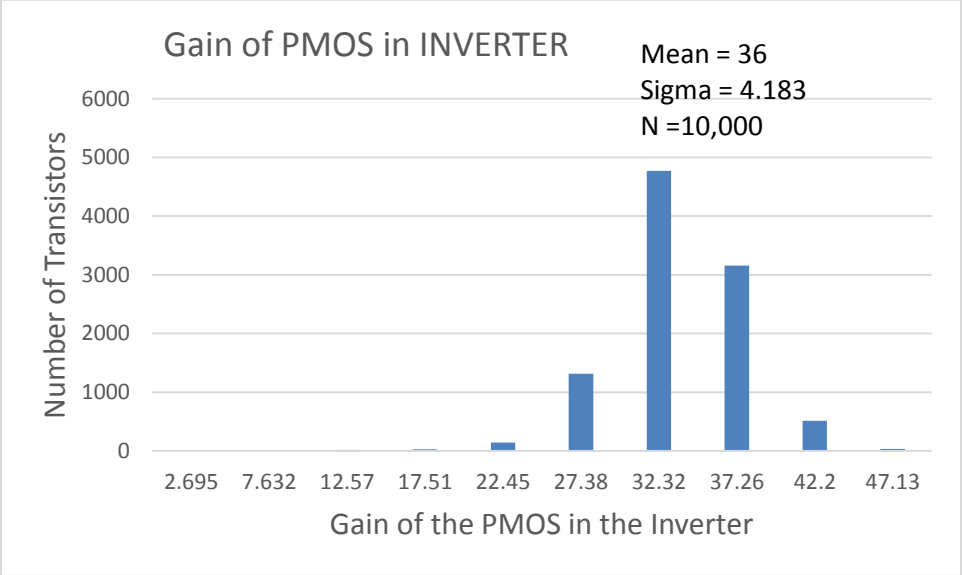

Figure 5.12 Gain of PMOS in the Second stage of the Complementary C-S amplifier

5.3 Monte Carlo Transient Simulations for N = 30

In this section we present the Monte Carlo results for the transient simulations of 30 samples. Figure 5.14 shows the node voltages that are plotted in the simulation

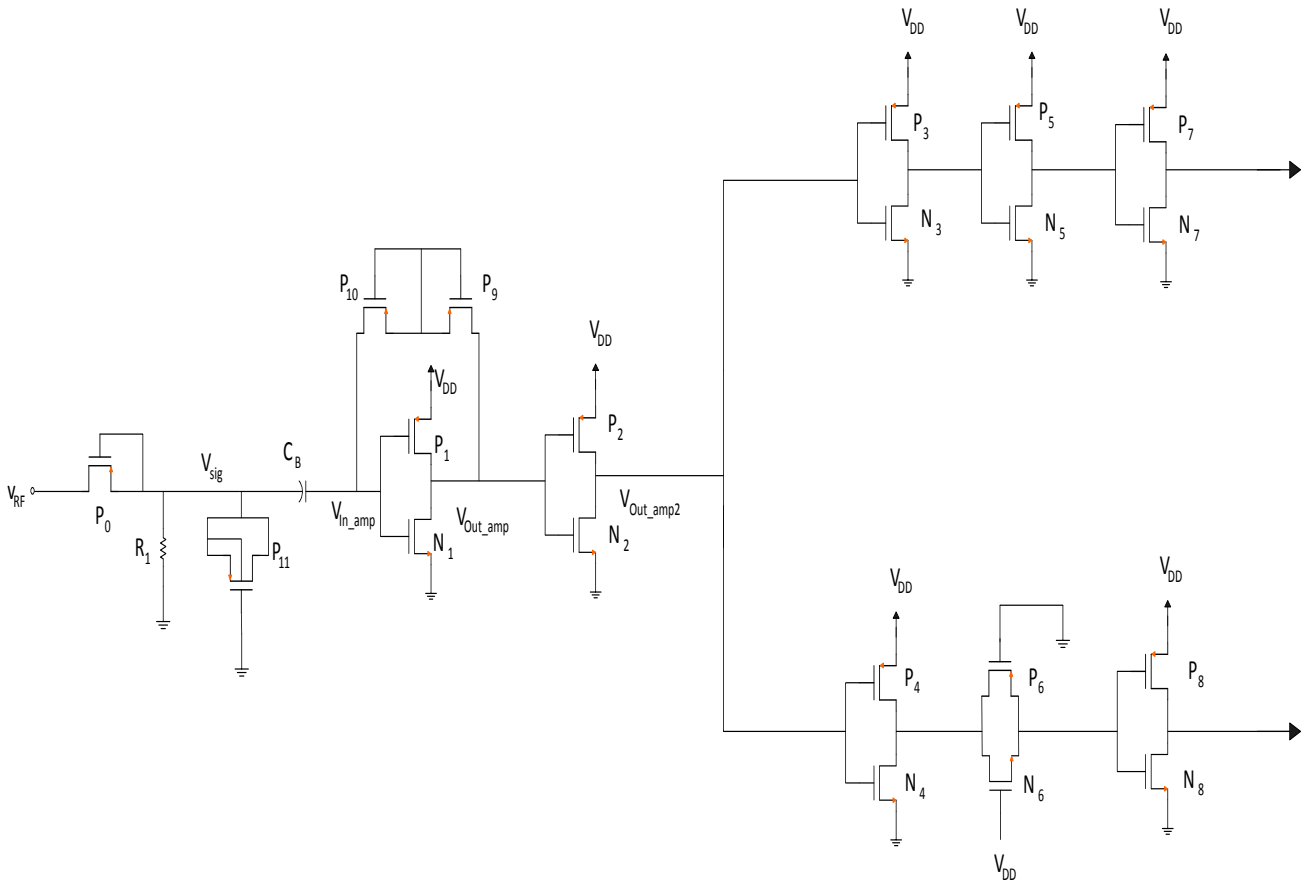

Figure 5.13 Demodulator circuit diagram

We plot the voltage waveforms at nodes $V_{sig}, V_{In\_amp}, V_{Out\_amp}, V_{Out\_amp2}, DATA\ and\ \overline{DATA}$ as seen in Figure 5.13 for the Monte Carlo transient simulations. The Monte Carlo transient simulation result is shown in Figure 5.14

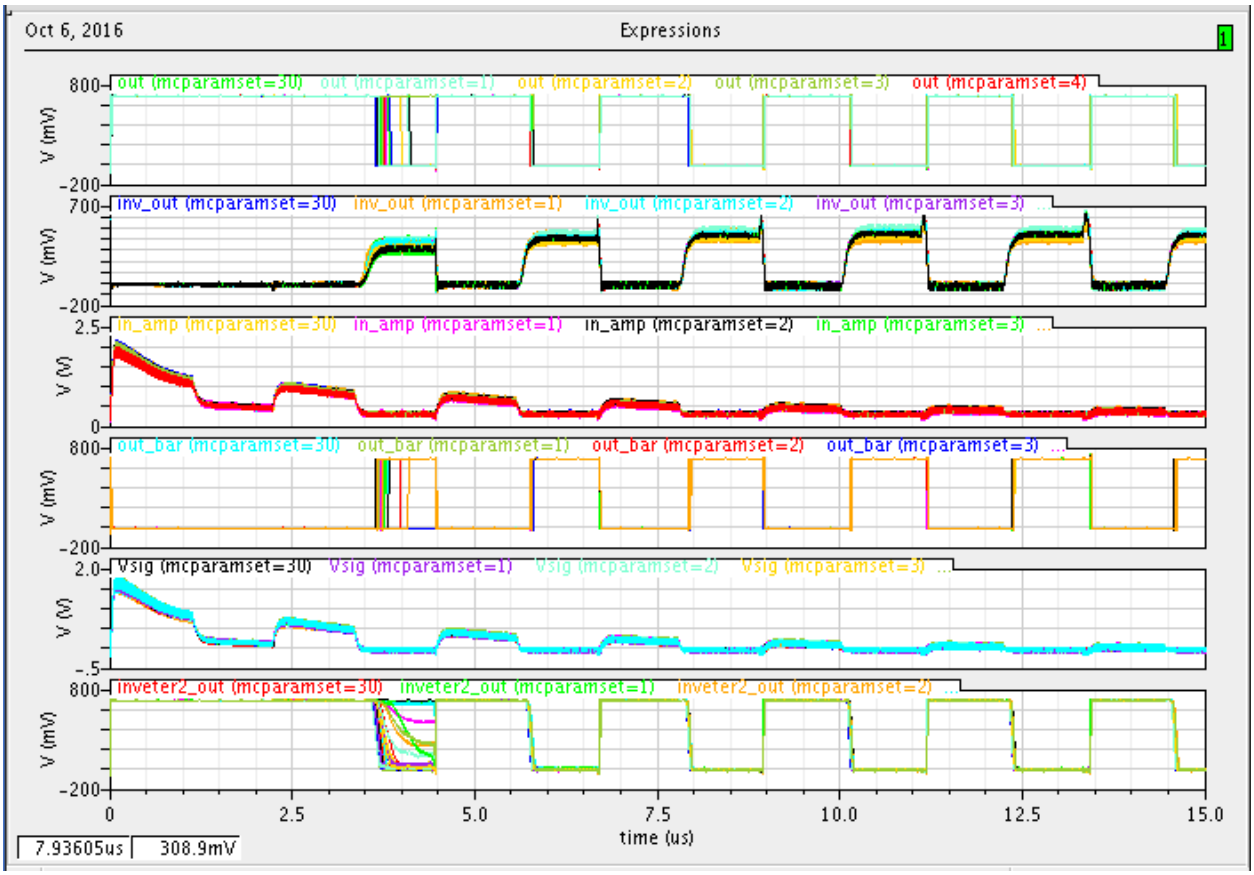

Figure 5.14 Monte Carlo Simulations for 30 samples

As seen from Figure 5.14 it is evident that the waveforms take 1-2 cycles to reach their intended functioning, hence for individual waveform results we would be presenting the data from 8.5µs to 10.5µs with a sampling rate of 0.5ns between each sample such that the variations in the waveforms are fully captured.

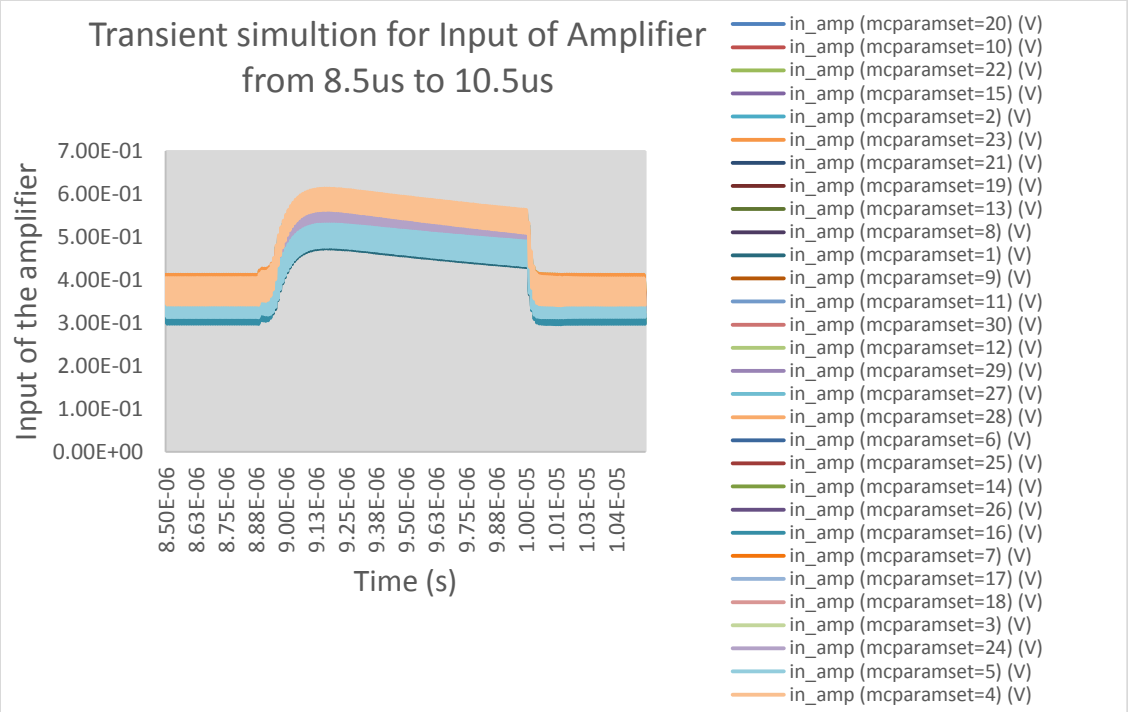

Figure 5.15 Transient Simulation of Input of the Amplifier from 8.5µs to 10.5µs

The input of the amplifier is at biased at the VDD/2 = 350mV. The transient simulation for the output of the first stage amplifier is shown in Fig 5.15. In order to capture the variation in the output of the amplifier we present the data for time from 7.5µs to 10µs as shown in Figure 5.16. The output of the demodulator DATA and DATA_bar are shown in Figure 5.17 and 5.18 respectively, also the output of the envelope detector is shown in Figure 5.19 for the time 8.5-10.5µ. As seen from all these waveforms that there is no failure in 30 samples, we assume the design is robust although to be more assured of robustness the number of transient Monte Carlo simulations usually is completed on 200 or more samples. In this effort we have limited the Monte Carlo simulations to 30 since the time and effort taken for 200-10,000 samples is very high.

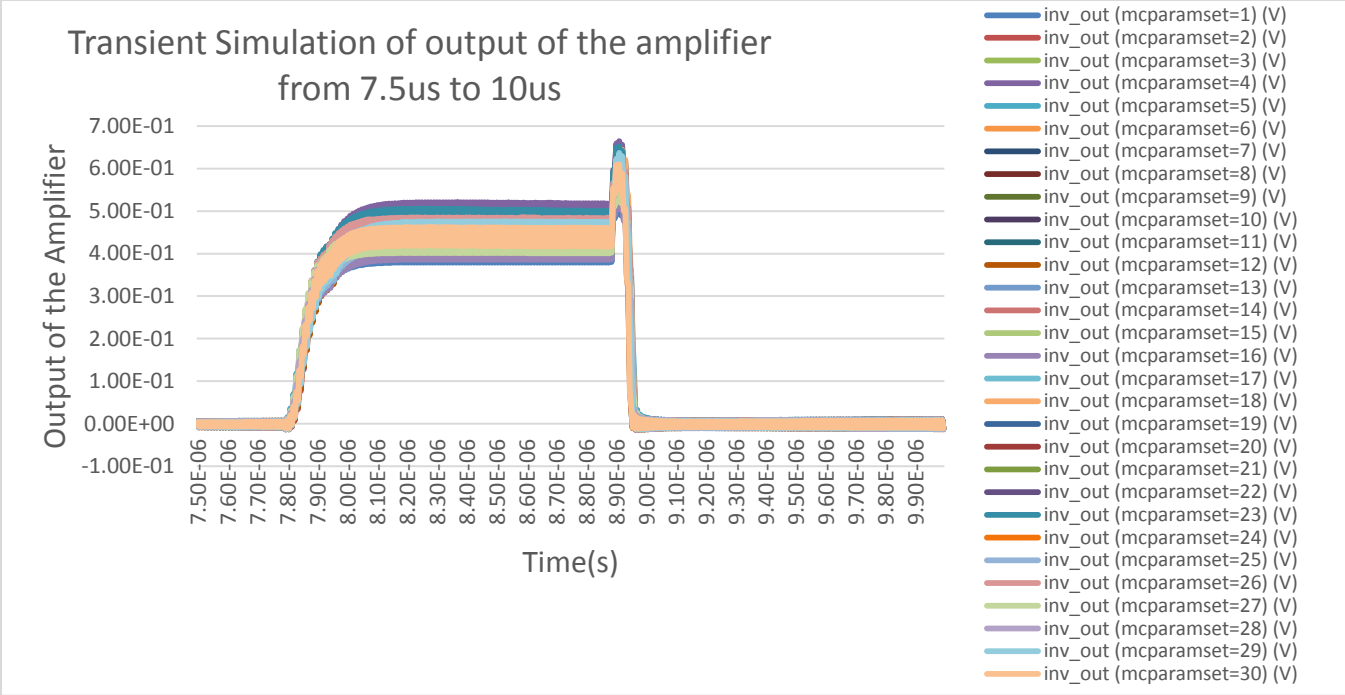

Figure 5.16 Transient Simulation of Output of the first stage of the Amplifier from 7.5µs to 10µs

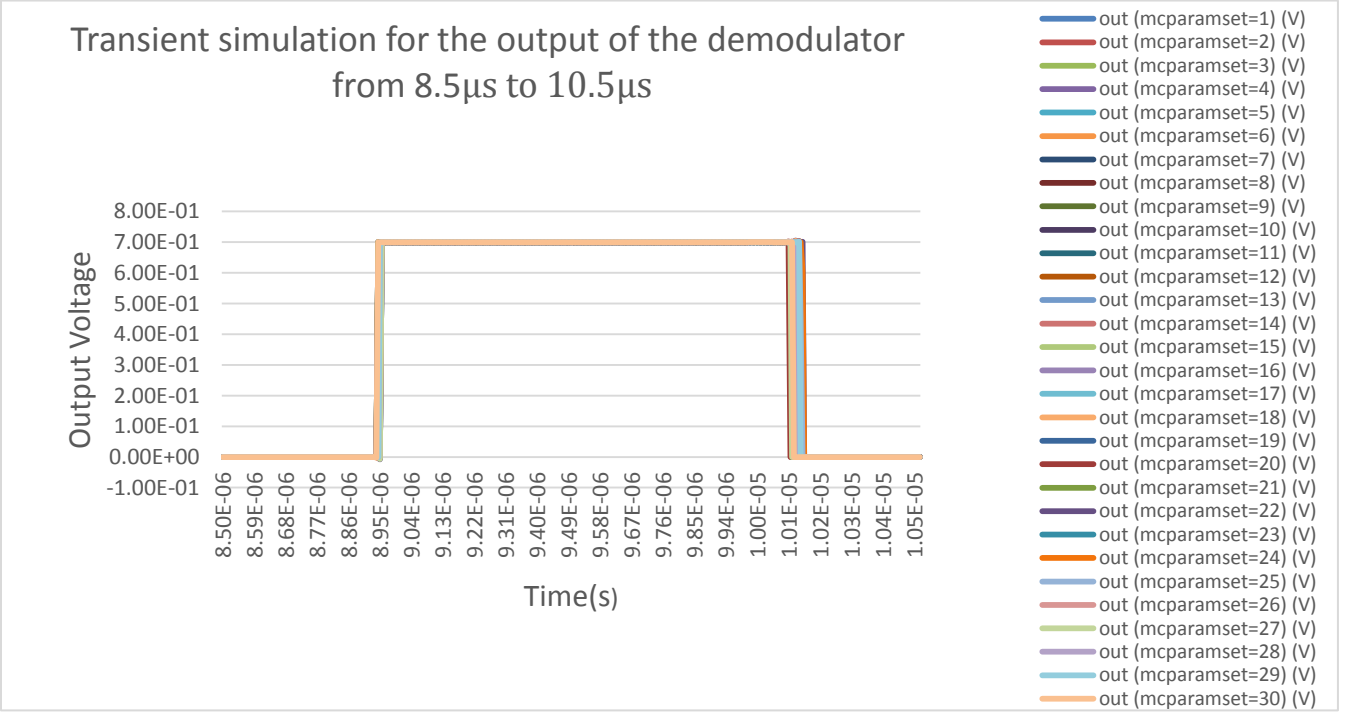

Figure 5.17 Transient Simulation of Output of the Demodulator from 8.5µs to 10.5µs

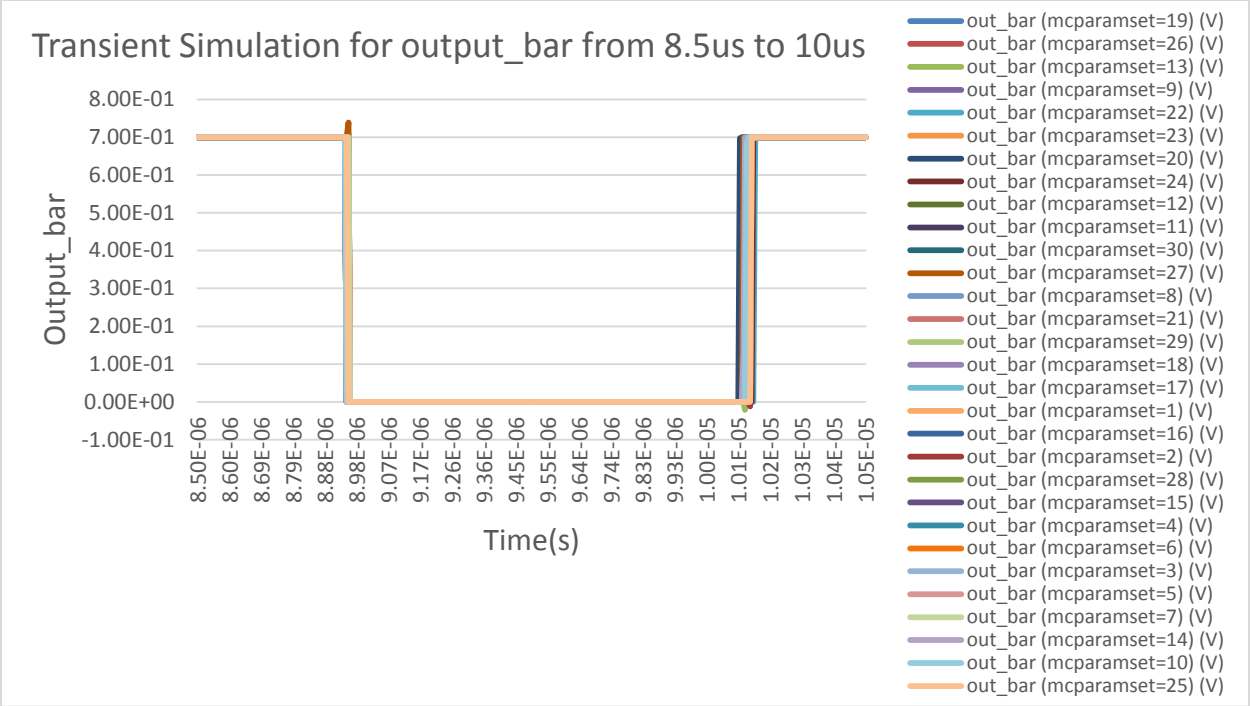

Figure 5.18 Transient Simulation of Inverse of the Output of the Demodulator (8.5µs to 10.5µs)

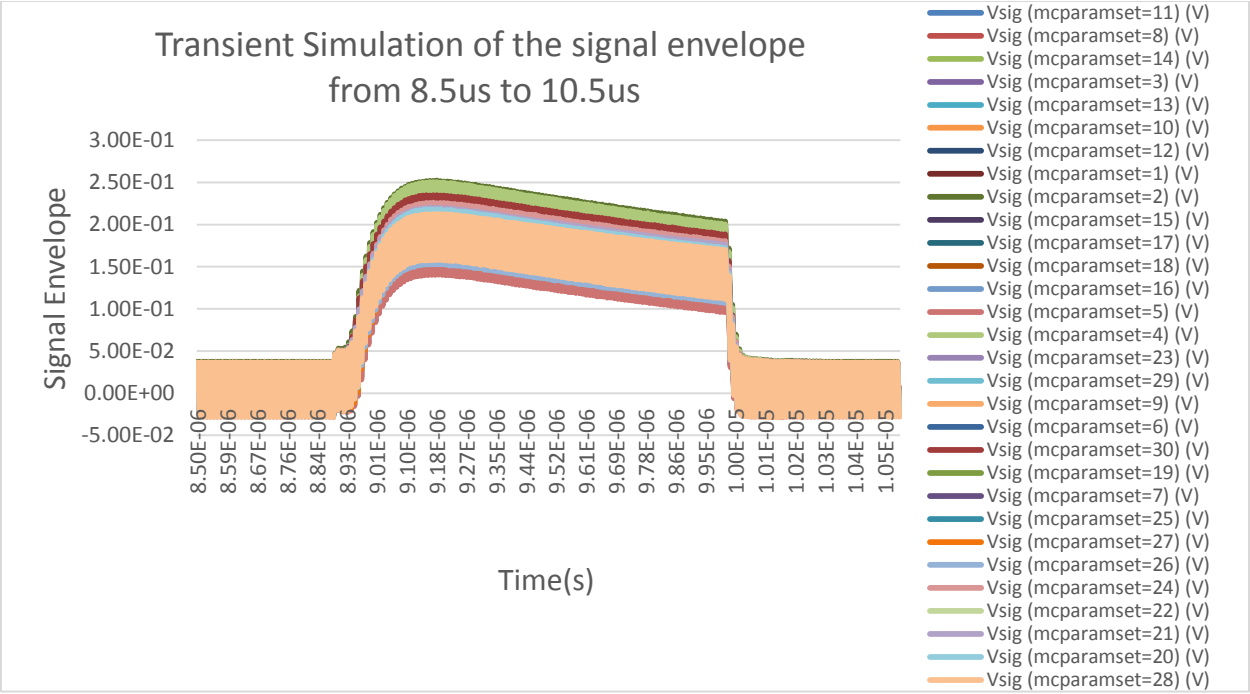

Figure 5.19 Transient Simulation of Voltage at the output of the Envelope Detector from 8.5µs to 10.5µs

CHAPTER VI

CONCLUSION

In this Chapter we first discuss the important parameters required to formulate the Figure of Merit for this effort and using this Figure of Merit we compare our design with the designs implemented in the past. The chapter concludes with the future scope and the entire effort will conclude my summarizing the outcome of this work.

6.1 Important parameters in Formulating the Figure of Merit.

- Data rate: The amount of information the demodulator is able to demodulate in a certain period is of great significance. A higher data rate requires that the length of the MOS devices constituting the demodulator need to be lower which results in greater power consumption.
- Modulation Index: The modulation index of the demodulator is an important circuit specification as the input voltage of the demodulator is set by the modulation index. A lower modulation index makes the design more challenging as the offset voltage requirement reduces which necessitates greater area in order to lower this offset.

- Power Consumption: As explained in Chapter 1 the power consumption of the demodulator is critical and the lower the power consumed by the demodulator the greater its utility.
- Carrier frequency: The greater the difference between the carrier frequency and the baseband frequency the easier the design is as the requirement on the low-pass filter at the input of the demodulator is relaxed.

6.2 Figure of Merits in the past

The Figure of Merit (FOM) is an expression that fully incorporates the important performance results of a design such that all designs can be compared with each other. One of the FOM presented in the past by [47] is as follows:

$$\text{FOM[47]} = \frac{Data\ Rate}{Gate\ Count\ X\ Power\ Consumed\ X\ Core\ Area}$$

The Figure of Merit established by [47] does not take into account the carrier frequency and the modulation index, these two parameters add additional constraints to the design. A design for a lower modulation index would result in greater power consumption since the geometry of the devices would need to be large enough to reduce the offset, yet a higher carrier frequency would be easier to design as the time constant of the envelope filter will have a relaxed constraint. The FOM explored by [47] does take into account the low modulation index complexity although indirectly through total power consumption, it does not incorporate the constraint imposed by the carrier frequency on the design.

Another Figure of Merit is presented by Mousavi et al[5]

$$\text{FOM[5]} = \frac{Data\ rate}{Power\ Consumed\ X\ Modulation\ Index\ X\ Carrier\ Frequency}$$

This Figure of Merit takes into consideration all the important factors that affect the performance of the design. Low power consumption, low modulation index and a lower carrier frequency

increase the complexity of design hence they are included in the denominator of the Figure of Merit whereas the data rate is in the numerator. The only problem with this Figure of Merit is that the carrier frequency in most cases is set by the protocol and any design which is intended for a particular protocol which has a high carrier frequency may lose out compared to a protocol incorporating a low carrier frequency. The carrier frequency is not a good estimator of the utility of the demodulator architecture incorporated as in most cases the designer has no control over the choice of the carrier frequency.

Table 6.1 Performance Comparison Table:

REFERENCE	Data Rate (kbits/s)	Power Consumed (μW)	Modulation Index (%)	Carrier Frequency (MHz)	Figure of Merit (FOM)
WANG[47]	10	10000-23900	10-17	2	0.05
MOUSAVI[5]	Up to 2000	35	7	13.56	602
GANESH[38]	160	>0.2	≈11	860-960	84.56
LIU[3]	4000	3.95	10	860-960	117.4
MENDIZABEL[1]	≈125	0.015	100	900	92.59
REHAN[14]	320	0.1	50	900	71.11
GUDNASON[4]	200	60	10-100	5	66.667
GONG[49]	Up to 1000	336	>5.5	2	270.56
LEE[50]	6780	348750	2.56	13.56	0.56
KAO[41]	1000	396	2.86-38.64	2	441.47*
This Work	**900**	**2**	**5**	**900**	**100**

"*" – FOM achieved from post layout simulations

As discussed in the previous section that the skew in the Figure of Merit is based on the carrier frequency, on comparing our work with similar works that incorporate carrier frequencies in the range of 900MHz the design is comparable to most of the designs in that category. The only design that has a Figure of Merit greater than out design with its carrier frequency close to 900MHz is LIU[3], as illustrated in Chapter 3 the complexity and labor involved in this design is far greater than our design which is simple and easy to realize.

6.3 Future Scope

The RFID is and will remain a vital element in the IoT, as long as the demand for RFID is there in the market, demodulator design for RFID applications would require some thought and effort. With the advent of the Internet of Things there is a need to keep the communication between the base station and the RFID tag to be secure which would require an encryption and decryption block in the block diagram of the passive RFID shown in Figure 1.1. These encryption and decryption protocol will have to be incorporated in the entire RFID which would also have to be low power. When considering the block diagram in Figure 1.1, the only clear avenue for power optimization is presented by the Low Dropout regulator as the efficiency of the LDO has been a challenge in the past and still remains a challenge. Other blocks such as the Phase Locked Loop, Harvesters have been optimized in the past[14], whereas digital circuits take up negligible power compared to other analog architectures. The Analog-to-Digital converter can also be a candidate for power optimization. Process Variation compensation methodologies to effect low power dissipation need to be explored to improve reliability and life span of the RFID.

6.4 Conclusion

In this effort we designed and optimized a ASK demodulator for RFID applications. This effort started with making the reader aware of the various challenges in terms of low power consumption in regards to passive RFID applications. Then introduced the concepts of Process,

Temperature and Voltage variation in semiconductor fabrication and their effects on the operation of a MOS transistor. A brief overview of past demodulator designs implemented was presented, after which the designed demodulator was introduced and various circuit design techniques were considered. A design objective was stated and steps to achieve them were shown and incorporated in the design. The simulation results in regard to the design were presented and finally a figure of merit was referenced in order to compare our design with the designs reviewed earlier. Through this work an attempt was made to try and simplify the work of the reader and expose them to the challenges associated with ASK demodulator design.

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APPENDICES

In the section we note down the legends in the transient simulation outputs

/input: Voltage at the input of the RFID

/in_amp: Voltage at the gate of the amplifier in the demodulator circuit presented in Chapter 4. /in_out: Voltage at the output of the amplifier

/out: Voltage at the output of the demodulator which represents the demodulated output

/out_bar: Voltage at the output of the demodulator which represents the inverse of the demodulated output.

/inverter2_out: Voltage at the output of the inverter following the amplifier.

/Vsig: Waveform representing the voltage of the envelope detector

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