EXTREME TEMPERATURE MEMORY DESIGN

WITH THE REDUCED DESIGN TIME USING SILICON

ON SAPPHIRE TECHNOLOGY

By

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I want to thank for my parents for their constant encouragement, love and support. To all of them I dedicate this work.

GLOSSARY

SRAM	Static Random-access Memory
ROM	Read-only Memory
NMOS	n-channel Metal-Oxide-Semiconductor
PMOS	p-channel Metal-Oxide-Semiconductor
I_D	Dain Current
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
KP	μC_{ox}
KP_P	KP of PMOS
KP_N	KP of NMOS
μ	Mobility
C_{ox}	Oxide Capacitance
I_{ON}	On-state Current
I_{OFF}	Off-state Current
V_{TH}	Threshold Voltage
ASIC	Application Specific Integrated Circuit
IC	Integrated Circuit
LVS	Layout Versus Schematic
LEF	Library Exchange Format

VHDL	VHSIC (Very High Speed Integrated Circuits) Hardware Description Language
Verilog	Hardware Description Language
VDD	Supply Voltage
GND	Ground
VSS	Ground
VTC	Voltage Transfer Characteristic
DRC	Design Rule Check
I/O	Input/Output
ALF	Advanced Library Format
TLF	Timing Library Format
RTL	Register Transfer Level
OSU	Oklahoma State University
MSVLSI	mixed signal circuit design group of OSU
U_T	Thermal Voltage
V_{SB}	Source to Body Voltage
V_{TH0}	Threshold Voltage with V_{SB} =0
RTL	Register transfer level

TABLE OF CONTENTS

Chapter Page

LIST OF TABLES

TABLE Page

LIST OF FIGURES

Figure Page

CHAPTER I

INTRODUCTION

1.1 Research Objective

High temperature integrated circuit design is a challenge for conventional bulk-silicon integrated circuit technology. Bulk technologies are used to 150 ℃ for the automotive market but are generally unavailable due to increased leakage current at higher temperatures [46][47] and limited market demand. The increased leakage current is caused by substrate and well diodes, and threshold voltage roll-off at elevated temperatures. To address these issues, the 0.5um Peregrine Silicon-on-Sapphire (SOS) technology is selected to minimize the drain/source to body diode leakage. The detailed advantages and disadvantages are discussed in Section 1.3.

This dissertation describes high temperature memories for microcontroller design using 0.5 um Peregrine SOS CMOS technology, which are suitable for aerospace, well logging, solar controllers, and automotive applications. The designed memories are as part of the design for 275 ℃ HC11 microcontroller and 200 ℃ LEON3 processor [9]. For the HC11, the design simulations are over the -55 ℃ to 295 ℃ range with testing completed over the room to 295 ℃ range. For the LEON3, the design simulations are over the -55 ℃ to 200 ℃ range with testing completed over the room to 200 ℃ range. The detailed testing is discussed in CHAPTER IV.

The memories having been designed include: a 4K on-chip SRAM, 512byte on-chip ROM, 4K SPI-SRAM, 2K SPI-ROM , 2K x16 off-chip SRAM, 128 x 32 cache , 32 x 32 cache, and SRAM design with Encounter support. The on-chip 4K SRAM is used to store the data and instructions executed by the HC11 microcontroller. The on-chip 512byte ROM is able to perform a sequence of the HC11 peripherals and registers self-test process; and it control the bootstrap process to boot from either SCI

or SPI interface. The 4K SPI-SRAM is used for off-chip storage of data and software routines to be uploaded and executed by the HC11. The 2K SPI-ROM is used to store a small monitor program, 68MON which is a monitor/debugger program for the HC11. Both on-chip and off-chip ROMs are the customer mask designs. The masking operation was completed separately from the other structures and programmed using a combination of Matlab and Cadence SKILL language. The off-chip 2K x 16 SRAMs are used for program and data storage, and they communicate with the LEON3 using a memory controller bridge. The 128 x 32 caches are used in LEON3 for high speed data and instruction storage. The 32x32 cache is used for the register file in the LEON3. The on-chip memories were designed using hand-layout, then instantiated as cells and placed and routed with HC11 and LEON3, respectively. The SRAM design with Encounter support basically uses the Encounter tool to Place & Route SRAM, which reduces the design time from 11 weeks to 6 weeks. The HC11 microcontroller along with SPI SRAM and ROM was developed to produce a down-hole microcomputer system (DMS) for Department of Energy/National Energy Technology Laboratory (DOE/NETL). The LEON3 processor with on-chip caches was developed for the use in jet engine sensor data acquisition for NAVAIR. The detailed designs of these memories are discussed in CHAPTER III. The specifications of SPI SRAM and ROM are described in Appendix B and C.

1.2 OSU cell library, HC11 and LEON3

The HC11 (operating at 275 °C, 3.3V and 3 MHz) consists of a microprocessor, arithmetic logic unit (ALU), a small boot ROM (512 bytes), 4K byte data RAM, counter/timer unit, serial peripheral interface (SPI), asynchronous serial interface (SCI), and the A, B, C, and D parallel ports (except port E). The LEON3 (operating at 200 °C, 3.3V and 18 MHz) is configured with a 128 x 16 instruction cache, a 128 x 16 data cache with tag, a 32 x 32 register file, JTAG, generic APB UART, CAN controller, interrupt controller, timer, LEON3 memory controller, an AHB controller, AHB/APB bridge, LEON3 debug support unit, general input/output ports, and analog can-driver.

HC11 and LEON3 circuit blocks along with the standard cell libraries were designed by OSU's MSVLSI design group [9] with the assistance from Aeroflex Gaisler which maintained the LEON3 code [41]. The standard cell libraries with the timing file and abstraction file were generated using the Cadence Characterization tool; the on-chip memories were designed using hand-layout, then instantiate as cells with the timing file and abstraction file; the Cadence Ambit synthesizer took the HC11 or LEON3 code (VHDL or Verilog RTL code) and generated a netlist of the circuit implementation using the characterized cell libraries and memories. LEON3 and HC11 have gate counts of 128,839 and 50,449, respectively. Without a standard cell library based Place & Route, the designer could spend years to produce hand-layout while experience many layout errors. The SRAM design with Encounter support was also synthesized, placed and routed using the characterized standard cell library and SRAM bank. As in Fig. 1.1, the design procedures of a standard cell library are described below:

1) The transistor width and length are chosen as discussed in Chapter II. The geometries of the transistors in the cell library can be determined to satisfy the worst case corners. The designed library cells have sufficient I_{ON}/I_{OFF} ratio to avoid design errors which may be caused by inaccurate Peregrine model. Furthermore, the cell designs satisfy a beta-matched requirement providing more robust behavior.
2) All the schematics in the cell library are simulated using Cadence Spectre.
3) Layouts in the cell library are generated as dense as possible and DRC/LVS is used to verify if the layout has correct connection and correct transistor size.
4) The cells are characterized using Cadence Characterization tool. The generated .lib file has functionality, timing and power information. The .lib file is a standard format required for integrating the standard cells into digital logic. The generated .lef file is a standard format to be used in Place & Route which defines blockages of routing layers and blockages of pins.

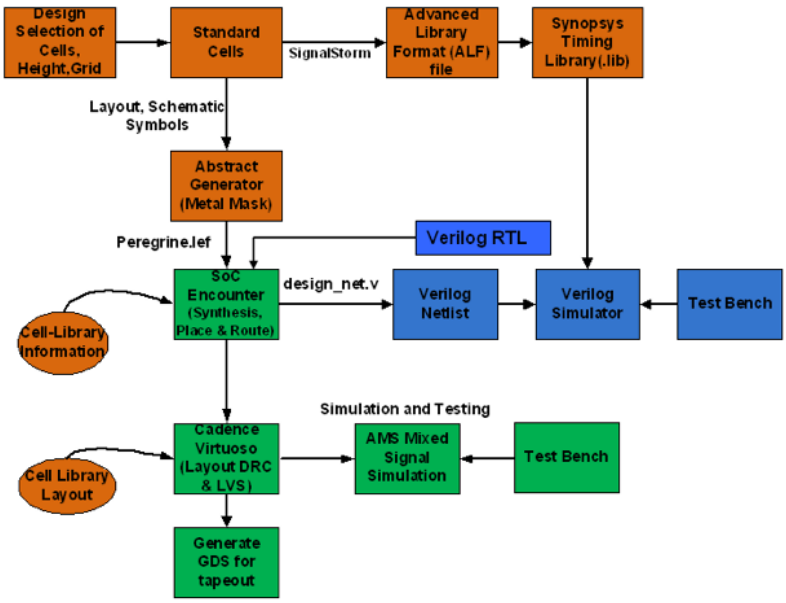


Fig. 1.1 General flow for creating a standard cell [40].

The standard cell library based ASIC design flow, Fig. 1.2 [40], categorizes the entire design procedure of HC11 and LEON3.

1) Cell libraries with .lib and .lef files are generated using Cadence Characterization tool. The memory cell is not able to be characterized using Cadence Characterization tool because of its complexity. However, the memory blocks can be simulated in Cadence and a .lib file can be generated manually. The input and output timings with the specified input and output capacitances are filled in the memory library file. The .lef file is generated the same as the cell library. The .v file with timing of the memory is generated with input and output timings and later used in step 3) and 4).
2) HC11 and LEON3 codes are finished using Verilog or VHDL at RTL level.
3) HC11 and LEON3 are synthesized with the cell library and the memory .v file.
4) Functional simulation and timing analysis are performed using the synthesized HC11 and LEON3 codes, the cell library and memory .v file.

5) Place & Route is performed using synthesized code, .lib file, and .lef file. Layouts and schematics are generated and timing constraints are satisfied.

6) Post layout simulation of HC11 and LEON3 are performed to verify the functionality of the design over all extreme process, voltage and temperature corners.

7) Physical verifications (DRC, LVS, antenna check) are performed before sent the HC11 and LEON3 to semiconductor foundry for fabrication.

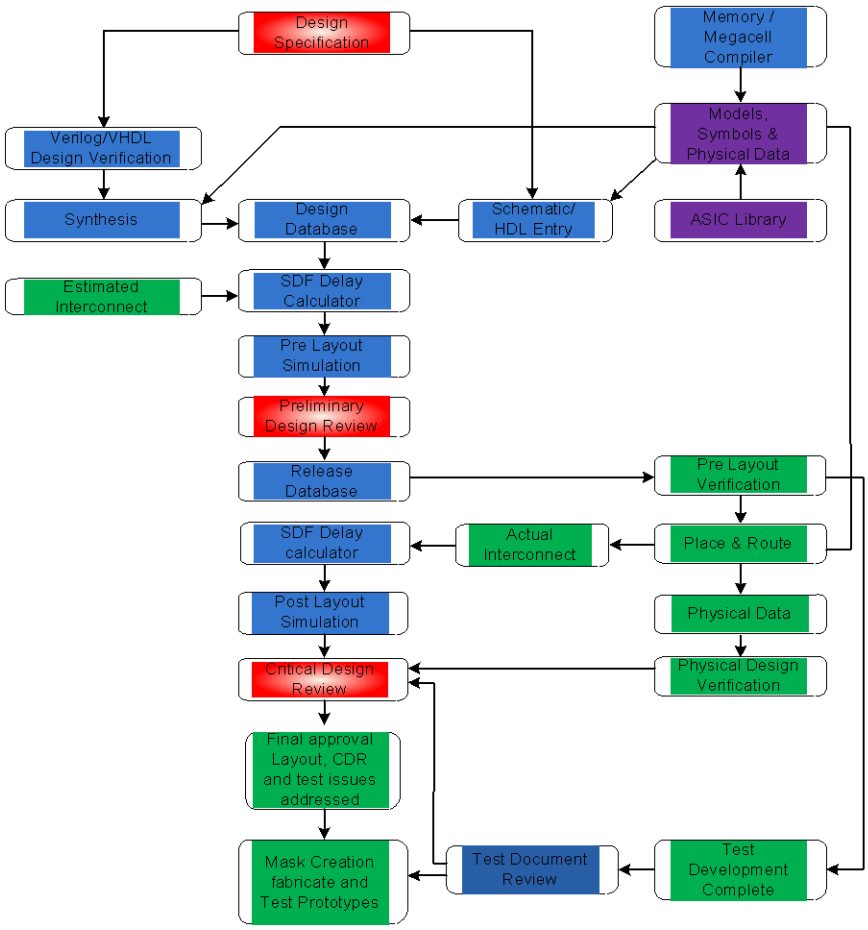


Fig. 1.2 Standard cell based ASIC design flow [40].

The layout and the abstraction of the cell are required for the standard cell library design. Fig. 1.3 shows the layout format of the standard cell library of Peregrine 0.5um process [49]. The layout horizontal grid and vertical grid sizes are 2.2um; the cell height used is 22um, and 22 um is exactly 10

times the grid size; 2.2um is chosen because it is the minimum distance of two contacts and 22um is used because the Encounter place & route can place the maximum contacts possible within the 22um. The required safety zones are 0.9um on the nlocos side and 0.4 um on the plocos side, the left and right sides also have safety zone of 0.4 um. The safety zones are required to avoid any DRC error when the cells are abutted to each other during the placing process.

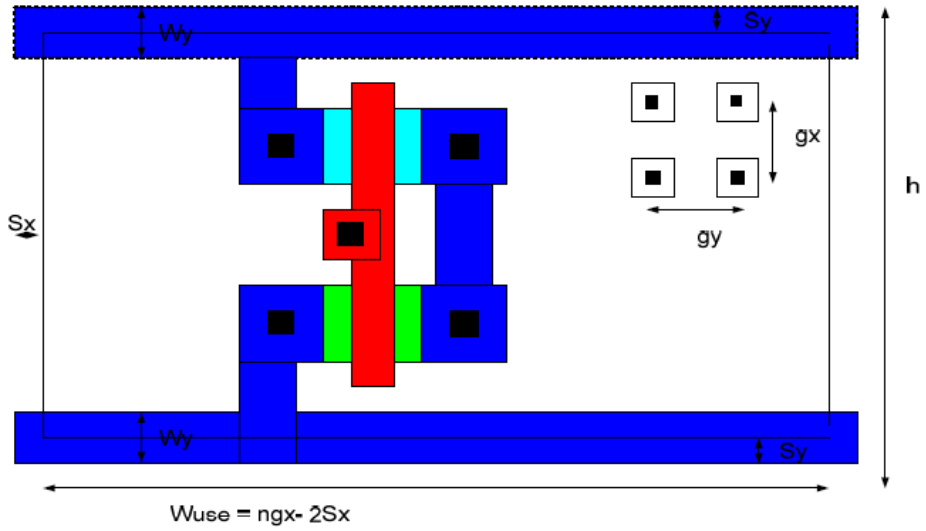
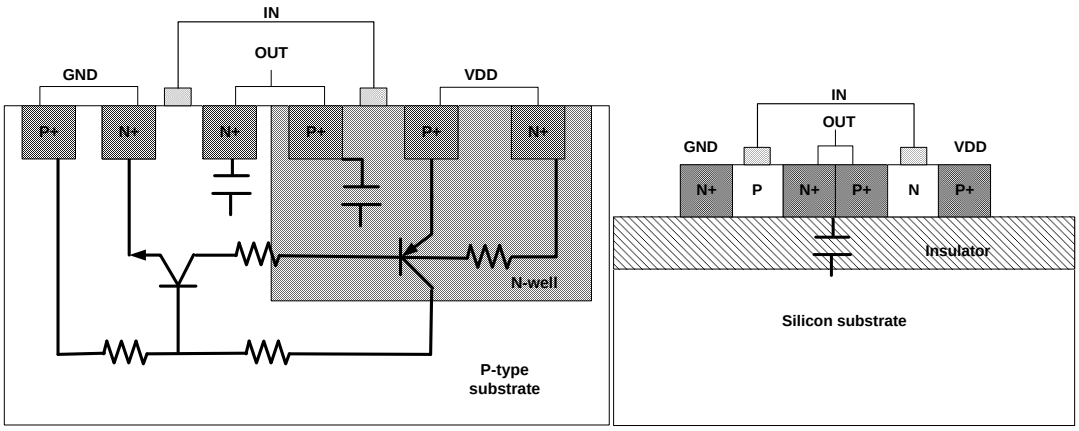


Fig. 1.3 The layout format of the standard cell library [49].

1.3 SOI and Bulk Comparison

Fig 1.4 shows the cross section of bulk CMOS inverter and SOI CMOS inverter. For bulk CMOS, PMOS or NMOS is fabricated in the well or substrate. Because of the lack of isolation to the substrate, the latch-up happens to the bulk CMOS inverter. However, for the SOI CMOS inverter, the substrate is isolated by the insulator. This insulator layer brings several advantages for SOI CMOS over bulk CMOS: high speed, low power and high device density, low leakage and no latch-up. The Peregrine SOS 0.5um process is partially depleted SOI process which uses Al_2O_3 as the insulator. The floating body effect in partially depleted SOI is well-known documented [1].



(a) (b)

Fig. 1.4 (a). Cross section showing the latch-up path in a bulk CMOS inverter. (b). Cross section of an SOI CMOS inverter. The drain parasitic capacitances are also presented [3].

1.3.1 High Speed, Low Power and High Device Density

As in Fig 1.4, bulk CMOS has a capacitance from drain/ source to the P-type substrate while SOI CMOS has a capacitance from drain/source to the silicon substrate. The Al_2O_3 insulator has relatively lower permittivity and much greater capacitance thickness compared with the bulk capacitance. This results in reduced capacitance, smaller RC delay and smaller dynamic power for modern VLSI design. This is significant in SRAM circuit design, as the column capacitances are significantly reduced resulting in higher speed and lower power design. SOI has the advantage of higher device density as well, due to well elimination. As shown in Fig.1.4, SOI has no N-well or P-well, and no contact is required for the well.

1.3.2 Low Leakage

SOI has less leakage current at elevated temperatures compared with bulk CMOS because the excessive junction leakage current occurs in bulk at elevated temperatures; insulator isolation eliminates this junction leakage current in SOI. As a result, it is very difficult to use conventional bulk CMOS technology at temperatures above 150 ℃ [46][47].The significantly reduced leakage in

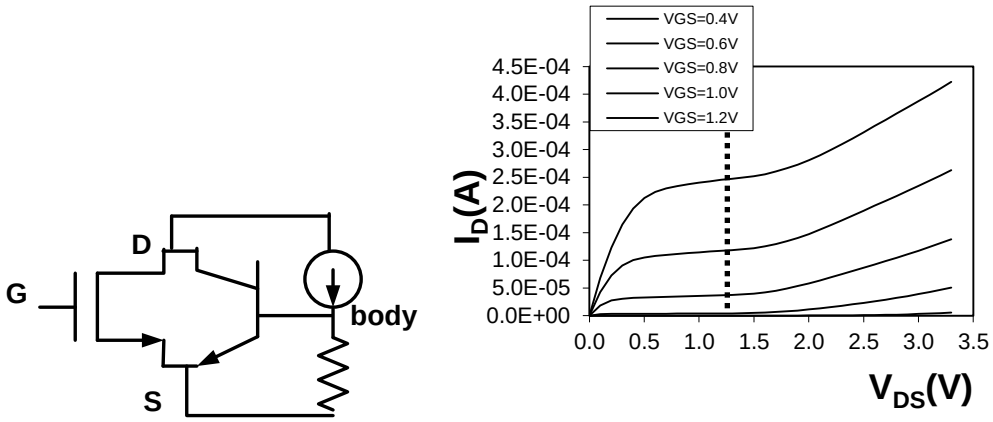
SOI results in sufficient I_{ON}/I_{OFF} ratio and less leakage power for valid digital designs at elevated temperatures [9][47]. These issues will be discussed in greater detail in CHAPTER II and III.

1.3.3 No Latch-Up

Fig. 1.4 shows the latch-up path in bulk which is eliminated in SOI. Latch-up happens in bulk CMOS which creates the thyristor structure [3]. Fig. 1.4(a) shows the formation of a thyristor like PNPN structure with a PNP transistor and a NPN transistor connected back to back which results in latch-up. Once the thyristor is triggered both transistors start to conduct and large amount of current flows through the transistors until the transistors are switched off. SOI CMOS eliminates the latch-up by insulator isolation [Fig. 1.4(b)].

1.3.4 Floating Body Effect

The insulator SOI structure offers several advantages but also brings disadvantage. The floating body results in a parasitic BJT which in turn results in increased I_D-V_{DS} characteristics currents referred to as the kink effect [43]. In a bulk CMOS device, the base of this BJT is connected to ground through the substrate or the well contact. For the SOI device, the base of the transistor is usually floating referred as the 'floating body effect'. Fig. 1.5(a) shows the parasitic BJT structure at the body of SOI NMOS. The small signal model current is to model the BJT current which results in reduced NMOS effective output resistance. In Fig. 1.5(b), the kink effect is no existent for V_{DS} less than approximately 1.45V [27]. This late turn-on of BJT is the result of insufficient energetic carriers in the channel which is required to produce other electron-hole pairs or cause impact ionization. The kink effect is not observable until V_{DS} exceeds approximately 2V for PMOS. This effect is smaller in PMOS devices because of the lower impact ionization of holes [27]. The kink effect can be harmful to SRAM cell stability, sense amp sensing, and digital circuit delay. This issue is fully discussed in CHAPTER IV along with robust design of SRAM cell, sense amp and digital circuits in the presents of transistor kink.



(a) (b)

Fig. 1.5 (a) Parasitic BJT inside a PD SOS NMOS transistor [27]. (b) I_D-V_{DS} characteristics of High V_{TH} NMOS with width equals 16@3.6 um, length equals 2 um. Measured I_D at V_{DS} equals 0.2V,0.4V,0.6V,0.8V,V_{GS} equals 0~3.6V at 195 ℃.

In conclusion, SOI has several advantages over bulk CMOS as in Table 1.1.The disadvantages of floating body effect requires robust design to overcome the issue.

Table 1.1
Comparison of SOI and Bulk CMOS advantages and disadvantages

	SOI CMOS	Bulk CMOS
Speed, drain/source capacitance	Lower S/D to body capacitances and as a result increases the circuit speed	Higher S/D to body capacitances
Latch up	No latch up	Latch-up problems due to the parasitic thyristors
Device density	Higher device density due to well elimination	Lower device density due to well
Leakage current	smaller leakage at elevated temperatures due to insulator isolation	No bulk technology available for applications above 150 ℃ due to large junction leakage
Kink effect	Kink effect happens due to no body tie	No kink effect because the body tie avoid the parasitic BJT to turn on

1.3 Design Methodologies

In this dissertation, the design methodologies are developed for high temperature memories, cell library and the top module (HC11, LEON3, and SRAM design with Encounter support). The methodologies are highly dependent on elevated temperature data and summarized below:

1) The Peregrine simulation models are only characterized up to 150 ℃ by the vendor and as a result can be of questionable value at elevated temperatures. Device data is taken to address the issues of elevated temperature behavior in SOS. The measured data is used as an important source to support cell library and memory circuit development, design and simulation. Measured data includes I_{ON} and I_{OFF}, threshold, and mobility. With the measured data, the kink effect is observed and its effect is documented. I_{ONP}/I_{OFFN} is found to be worse than I_{ONN}/I_{OFFP}.

2) The standard cell library is then designed based on the measured data. A CMOS gate performance equation model is developed to determine the cell geometries and ensure circuit robustness to I_{ON}/I_{OFF} to cell variability, ensuring an adequate noise margin.

3) The memory designs are developed with the aid from the measured data to address write and read stability in the context of floating body effect, kink effect, and shrinking I_{ON}/I_{OFF} currents with temperatures.

4) Each top module can be designed with the specific standard cell library and the required memories. The on-chip memories are designed using hand-layout, then instantiated as cells with timing and abstraction files; the top module is then synthesized and placed & routed with the satisfied timing.

1.4 Dissertation Organization

This dissertation describes high temperature memories as part of the design for 275 ℃ HC11 microcontroller and 200 ℃ LEON3 processor [9] using SOS technology. CHAPTER II presents the accurately measured data including I_{ON}/I_{OFF} ratio, threshold, and mobility. The kink effect is also observed from the I_D vs. V_{DS} curve. CHAPTER III presents the standard cell library design and the

memory design. The design issues of the standard cells are: functional design/able to switch, rise and fall time, I_{ON}/I_{OFF} ratio, variability, and beta-match requirement. The design issues for SOS SRAM and sense amp are: I_{ON}/I_{OFF}, floating body effect, mid-rail read, V_{TH} of the SRAM cell, and mobility. The memory device test result is presented in CHAPTER IV along with functionality across temperature corners. The testing analysis found the possible error sources, which can be useful for future SRAM design. CHAPER V discusses the SRAM layout with Encounter support to reduce the SRAM design time. And finally CHAPTER VI concludes this dissertation.

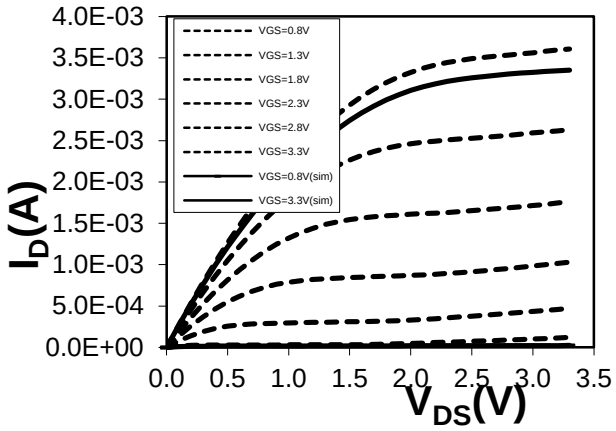
CHAPTER II

ACCURATE DATA FOR CELL LIBRARY AND MEMORY

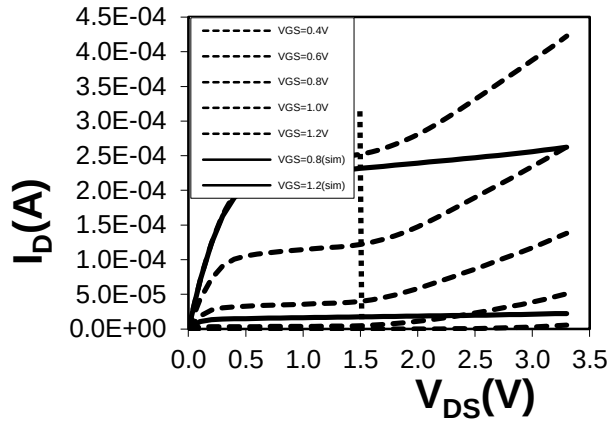
2.1 Measured ION/IOFF, Threshold and Mobility

Accurate knowledge of ION/IOFF ratio, threshold (VTH) and mobility of the SOS devices versus temperature is a key to the successful design of the cell libraries and the memories for extreme temperatures. The Peregrine simulation model, characterized for below 150 ℃ by the vendor, can be of questionable value at elevated temperatures by observing comparison with the measured data [45]. Furthermore, the kink effect is not included in the model as well. Fig. 2.1 shows a plot of the Peregrine model versus the measured data at room temperature and the increased current is well observed from the measured data. Cell library designs for elevated temperatures (200 ℃ and 275 ℃) characterized with the Peregrine model require further consideration to avoid design failures and/or low yield.

The kink effect as observed in Fig. 2.1(b) increases the current compared to the model; this effect happens especially at low V_{GS}. The kink effect is nonexistent for V_{DS} less than approximately 1.45V for NMOS. This late turn-on of the BJT is the result of insufficient energetic carriers in the channel and these carriers are required to produce electron-hole pairs resulting from impact ionization [27]. The kink effect occurs around V_{DS} equals 2V for PMOS. This effect is smaller in PMOS devices because of the lower impact ionization energy of holes [27].



(a)



(b)

Fig. 2.1 (a)I_D vs V_{DS} for 20 x 1.4um/1.4um high V_{TH} NMOS, V_{DS}=0 to 3.3V, V_{GS}=0.8V to 3.3V in 6 steps at room temperature. (b) I_D vs V_{DS} of the same device at low V_{GS}, V_{GS}=0.4V to 1.2V in 5 steps. Note solid data is simulated and dashed is measured.

I_{ON}/I_{OFF} data is used to develop the cell library sizing rules and verify the Encounter Library Characterization tool rise/fall results with elevated temperature functional designs in mind. These data is equally important for the memory design and is the basis for validating Cadence Spectre simulation of delay, leakage current and power. The measurement equipment used is Keithley 2400 and Cascade Alessi REI-6100 semi-automatic probe station. These data is discussed in detail below.

Fig. 2.2 **Error! Reference source not found.**shows the I_{ON}/I_{OFF} ratio versus temperature for high V_{TH} PMOS and NMOS, where W equals 20 x 1.4um and L equals 0.8um for PMOS, and W equals 1 x 20um and L equals 1.6um for NMOS. These high V_{TH} PMOS and NMOS are known

as 'RP' and 'RN' in the Peregrine model. I_{ON} was measured at V_{DS} equals 50mV, V_{GS} equals 3.6V and I_{OFF} was measured at V_{DS} equals 3.6V, V_{GS} equals 0V. The "EXP_PMOS" and "EXP_NMOS" lines are an averaged exponential fit to find the I_{ON}/I_{OFF} ratio for 10 RP and RN, respectively. The error bars are the 1-sigma standard error points. As shown in Fig. 2.2, I_{ON}/I_{OFF} ratio is degrading with temperatures. The other test results with different geometries are shown in Table 2.1; RP and RN have the lengths of 0.6um and 0.7um and 1.1um, 1.3um and 1.4um, respectively. Each data point is the average of 10 different die where each transistor is composed of 20 fingers each 1.4um in width except that RN with 1.6um length has 20um width. Typically I_{ON} and I_{OFF} can be calculated in Equation (2.1) and (2.2) [54], respectively.

$$I_D = KP \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{{V_{DS}}^2}{2} \right] \tag{2.1}$$

$$I_D = I_{D0} \cdot \exp\left(\frac{V_G - n \cdot V_S}{n \cdot U_T} \right) \left[1 - \exp\left(-\frac{V_D - V_S}{U_T} \right) \right] \tag{2.2}$$

$$I_{D0} = I_S \cdot 2 \cdot n \cdot KP \cdot \frac{W}{L} \cdot U_T^2 \cdot \exp\left(\frac{-V_{TH0}}{n \cdot U_T} \right)$$

where KP = μC_{ox}, V_{GS}, V_{TH}, V_G, V_D, V_S , I_S, n take on their usual values. W is the width of the transistor. L is the length of the transistor. U_T is the thermal voltage. V_{TH0} is threshold voltage for zero substrate bias. μ is the mobility. C_{ox} is the oxide capacitance.

Fig. 2.3 shows the average I_{OFF} current from the measurement and the Peregrine model using the same test condition as Fig. 2.2; the measured devices are: RN with L equal 1.1um, 1.3um and 1.4um; all widths are 20 x 1.4um and the plot uses 1.4um width for convenience; I_{OFF} as observed is increased with temperature; the model data follows Equation (2.2) while the measured data has larger value than the model data because it includes both Equation (2.2) and the kink current. It is also interesting to observe from Fig. 2.1, the measured I_{ON} is consistent with the model at V_{DS} equals 50mV, V_{GS} equals 3.6V.

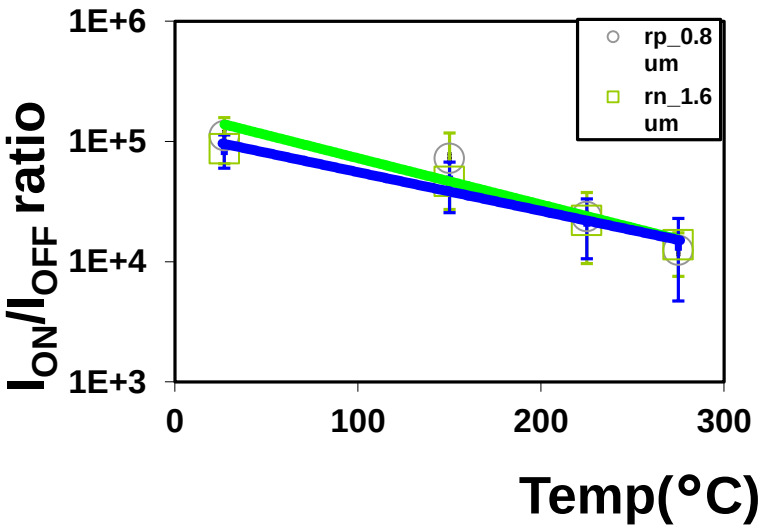


Fig. 2.2 I_{ON}/I_{OFF} ratio over (room to 275 ℃) for RP W equals 20 x 1.4um, L equals 0.8um, and RN W equals 20 x 1.4um, L equals 1.6um. Measured I_{ON} at V_{DS} equals 50mV, V_{GS} equals 3.6Vand I_{OFF} at V_{DS} equals 3.6V, V_{GS} equals 0V.

Table 2.1
I_{ON}/ I_{OFF} ratio and the variations of I_{ON}/ I_{OFF} ratio

Device (W/L)	I_{ON}/I_{OFF} (27 ℃)	1σ I_{ON}/I_{OFF} (27 ℃)	I_{ON}/I_{OFF} (150 ℃)	1σ I_{ON}/I_{OFF} (150 ℃)	I_{ON}/I_{OFF} (225 ℃)	1σ I_{ON}/I_{OFF} (225 ℃)	I_{ON}/I_{OFF} (275 ℃)	1σ I_{ON}/I_{OFF} (275 ℃)
RP 20 x 1.4/0.6 um	1.26E5	4.06E4	2.08E4	3.13E4	3.33E4	1.18E4	4.52E4	1.37E4
RP 20 x 1.4/0.7 um	2.04E5	1.02E4	1.03E5	2.57E4	2.72E4	1.31E4	1.34E4	4.54E3
RP 20 x 1.4/0.8 um	1.11E5	4.60E4	7.04E4	4.51E4	2.36E4	1.40E4	0.26E4	4.89E3
RN 20 x 1.4/1.1 um	353	262	67.5	49.3	35.5	14.2	29.9	9.87
RN 20 x 1.4/1.3 um	138	88.7	93.1	64.1	48.1	23.6	30.1	12.5
RN 20 x 1.4/1.4 um	8.49E3	5.47E3	401	319	68.9	30.7	100	55.3
RN 1 x 20/1.6 um	8.66E4	2.30E4	4.64E4	1.83E4	2.19E4	1.14E4	1.38E4	9.16E3

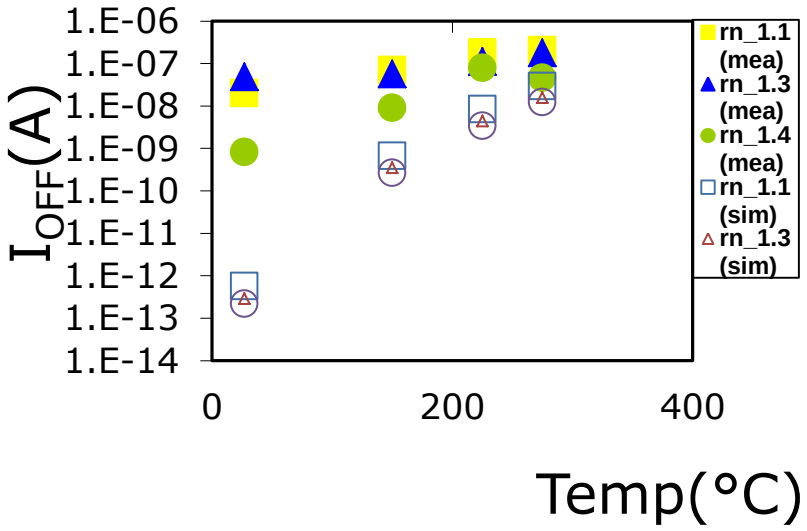


Fig 2.3 I_{OFF} over (room to 275 ℃) for NMOS L equal 1.1um, 1.3um and 1.4um. All widths are 1.4um.Measured and simulated at V_{GS} equal 0V, V_{DS} equal 3.6V.

V_{TH0} versus temperature is plotted in Fig. 2.4, where W equals 20 x 1.4um and L equals 0.8um for RP, and W equals 1 x 20um and L equals 1.6um for RN. The threshold voltage temperature coefficients are found to be 0.52mV/ ℃ and 0.43mV/ ℃ for RN and RP, respectively with V_{SB} equals zero. V_{TH0} was measured at V_{DS} equals 50mV and V_{GS} swept from 0 to 3.3V in 50mV steps [20]. The error bar indicates the 1-sigma V_{TH0} error. KP versus temperature for both RN and RP is presented in Fig. 2.5, where W equals 20 x 1.4um and L equals 0.8um for RP, and W equals 1 x 20um and L equals 1.6um for RN. KP is degrading at an exponential rate of -0.80 and -0.98 for both RN and RP, respectively. The "EXP_NMOS" and "EXP_PMOS" lines again are an averaged exponential fit to find the KP values for RN and RP, respectively. Equation (2.1) is used to calculate KP [31] [32]. The mobility variation is ignored in Equation due to the dominancy of V_{TH} variation [4] [30]. The other test results are shown in Table 2.2 and 2.3.

The measured I_{OFF} is more accurate as it includes both the kink effect and I_{OFF} calculation in Equation (2.2) while the vendor supplied model does not include the kink current. Moreover, the measured I_{ON} and I_{OFF} variations observed in this dissertation are larger than the I_{ON} and I_{OFF} variations projected from previously determined Pelgrom coefficients [8] as well as the vendor

model; the measured V_{TH} and KP variations are also different than the previous determined for the following reasons:

1) Current variations due to kink effect were not included in the previous measurement work [8].
2) Our smaller sample size of 10 leads to less accurate estimates.
3) Die to die variations were not considered and devices were laid out for analog matching in the previous work [8]. No common centroid geometries or dummies were included for this measurement setup. The Pelgrom coefficient previously found in [8] considered only the analog layout for improved circuit matching with the expectation that V_{DS} would be less than 1V.

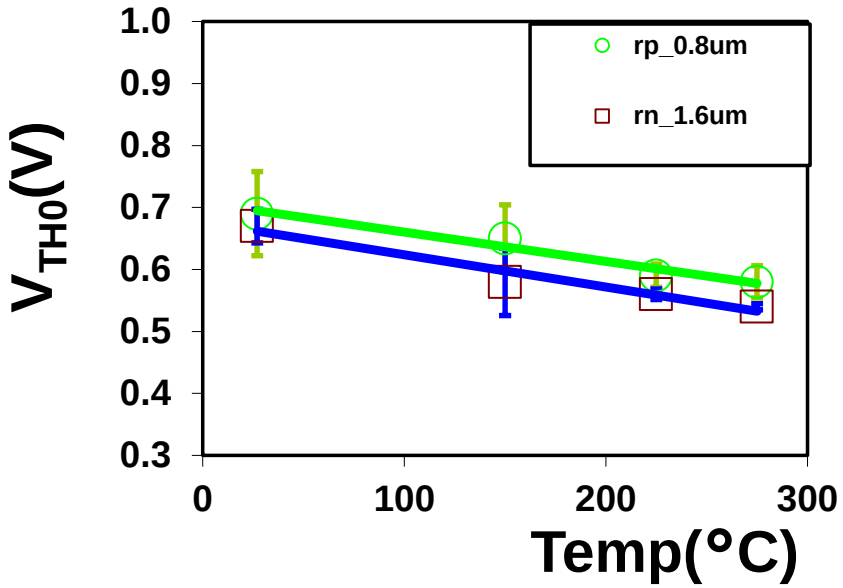


Fig. 2.4 V_{TH0} over (room to 275 ℃) for RP W equals 20 x 1.4um, L equals 0.8um, and RN W equals 20 x 1.4um, L equals 1.6um. Calculated at V_{DS} equals 50mV, V_{GS} equals 0 ~3.3V at 50mV each step. (Only the absolute value of V_{THP} is used in this dissertation.)

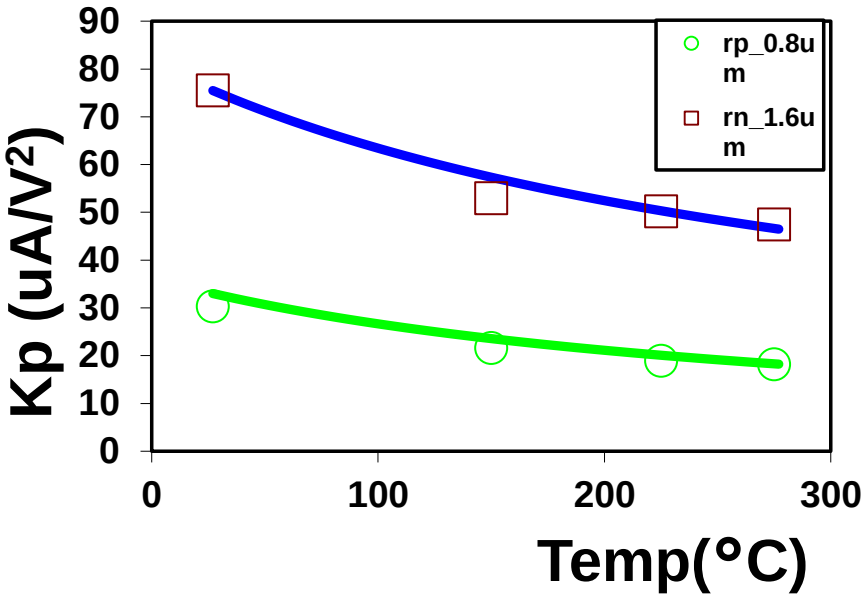


Fig. 2.5 KP over (room to 275 ℃) for RP W equals 20 x 1.4um, L equals 0.8um, and RN W equals 20um x 1.4um, L equals 1.6um. Measured at V_{GS} equals 1V, V_{DS} equals 50mV.

Table 2.2
V_{TH} and the variations of V_{TH} at different temperatures

Device(W/L)	V_{TH} (27 ℃)	1σ-V_{TH} (27 ℃)	V_{TH} (150 ℃)	1σ-V_{TH} (150 ℃)	V_{TH} (225 ℃)	1σ-V_{TH} (225 ℃)	V_{TH} (275 ℃)	1σ-V_{TH} (25 ℃)
	(V)	(V)	(V)	(V)	(V)	(V)	(V)	(V)
RP 20@1.4/0.6 um	0.71	0.12	0.64	0.11	0.60	0.04	0.59	0.05
RP 20@1.4/0.7um	0.70	0.23	0.62	0.14	0.59	0.22	0.58	0.22
RP 20@1.4/0.8 um	0.69	0.21	0.65	0.05	0.59	0.02	0.58	0.03
RN 20@1.4/1.1 um	0.58	0.16	0.55	0.18	0.49	0.02	0.47	0.01
RN 20@1.4/1.3 um	0.56	0.16	0.51	0.15	0.48	0.13	0.46	0.01
RN 20@1.4/1.4 um	0.60	0.09	0.55	0.26	0.5	0.02	0.47	0.01
RN 1@20/1.6 um	0.67	0.03	0.58	0.06	0.56	0.01	0.54	0.01

Table 2.3
KP at different temperatures

Device(W/L)	KP (27 ℃) ($\mu A/V^2$)	KP (150 ℃) ($\mu A/V^2$)	KP (225 ℃) ($\mu A/V^2$)	KP (275 ℃) ($\mu A/V^2$)
RP 20@1.4/0.6 um	34.5	22.2	21.5	21.3
RP 20@1 4/0.7 um	33.5	21.1	17.2	15.4
RP 20@1.4/0.8 um	30.3	21.6	18.9	18.1
RN 20@1.4/1.1 um	53.1	46.8	42.0	39.9
RN 20@1.4/1.3 um	58.6	43.3	40.6	39.2
RN 20@1.4/1.4 um	63.8	39.4	44.6	37.0
RN 1@20/1.6 um	75.5	52.9	50.2	47.4

2.2 Summery

The measured I_{ON} and I_{OFF}, threshold, and mobility are used as the basis for cell library and memory designs. With these data, the kink effect is noted as being significant; I_{ONP}/I_{OFFN} (PMOS I_{ON} NMOS I_{OFF} ratio) is found to be much worse than I_{ONN}/I_{OFFP}; measured I_{ON} is found to be consistent with the Peregrine model at 200 ℃ while the measured I_{OFF} is found to be greater than the model due to the kink effect. (200 ℃ is the LEON3 temperature corner). The worst case temperature and process variations of I_{ON} and I_{OFF} for single P and N devices for lengths of potential interest are summarized in Table 2.4. The worst case I_{ON} is at lowest I_{ON} and the worst case I_{OFF} is at largest I_{OFF} [34], or low VDD, slow process, and highest temperature. From the measured data, I_{ON} decreases with temperature and I_{OFF} increases with temperature. Frequently 2-3 sigma is defined as the process corner [25][42]. So Table 2.4 used $\mu I_{ON} - 3\sigma I_{ON}$ and $\mu I_{OFF} + 3\sigma$-I_{OFF} as the process corner.

As shown in Table 2.4, the "minimum" geometry inverter '1X INV' and 3-input NOR 'NOR3' I_{ON}/I_{OFF} ratios in Table 2.4 show L greater than or equal 1.6um is adequate for designing with the NMOS in conjunction with an L equal 0.8um PMOS. The choice of PMOS L equals 0.8um is to maximize the noise margin and will be discussed in CHAPTER III. Other NMOS geometries

have insufficient I_{ON}/I_{OFF} which can result in slow or fail digital logic. The similar worst case corners are summarized in Table 2.5 for the HC11 at 275 ℃ temperature corner. The detailed implementation for logic gates and memories are discussed in CHAPTER III and IV.

Table 2.4
I_{ON} and I_{OFF} and the variations of I_{ON} and I_{OFF} at 200 ℃

Device(W/L)	μI_{OFF}	1σ-I_{OFF}	I_{OFF} Worst Case $\mu I_{OFF} + 3\sigma$-I_{OFF}	μI_{ON}	1σ-I_{ON}	I_{ON} Worst Case $\mu I_{ON} - 3\sigma$-I_{ON}	1X INV $I_{ON\_RP\_0.8um}/I_{OFF}$ ratio	NOR3 $I_{ON\_RP\_0.8um}/I_{OFF}$ ratio
	(nA)	(nA)	(nA)	(uA)	(uA)	(uA)		
RP 1.4/0.6 um	0.174	0.380	1.31	5.81	0.986	2.85		
RP 1.4/0.7 um	0.152	0.401	1.36	4.85	1.14	1.43		
RP 1.4/0.8 um	0.184	0.113	0.523	4.35	0.628	2.47		
RN 1.4/1.1 um	158	338	1170	6.64	1.15	2.94	2.11	1.67
RN 1.4/1.3 um	220	366	1210	5.84	1.44	1.52	2.04	1.66
RN 1.4/1.4 um	78.5	255	843	5.41	1.07	2.20	2.93	1.97
RN 1.4/1.6 um	0.176	0.830	2.67	3.87	0.264	3.08	925	769

Table 2.5
I_{ON} and I_{OFF} and the variations of I_{ON} and I_{OFF} at 275 ℃

Device(W/L)	μI_{OFF}	1σ-I_{OFF}	I_{OFF} worst case $\mu I_{OFF} + 3\sigma$-I_{OFF}	μI_{ON}	1σ-I_{ON}	I_{ON} worst case $\mu I_{ON} - 3\sigma$-I_{ON}	1X INV $I_{ON\_RP\_0.8um}/I_{OFF}$ ratio	NOR3 $I_{ON\_RP\_0.8um}/I_{OFF}$ ratio
	(nA)	(nA)	(nA)	(uA)	(uA)	(uA)		
RP 1.4/0.6 um	0.126	0.178	0.660	5.84	0.648	3.90		
RP 1.4/0.7 um	0.299	0.489	1.77	4.80	0.453	3.44		
RP 1.4/0.8 um	0.328	0.839	2.85	4.08	0.584	2.33		
RN 1.4/1.1 um	205	409	1430	6.15	0.853	3.59	1.63	1.28
RN 1.4/1.3 um	179	543	1810	5.40	0.477	3.97	1.29	1.04
RN 1.4/1.4 um	46.1	201	649	4.36	0.758	2.09	3.59	2.96
RN 1.4/1.6 um	0.289	2.53	7.79	3.98	0.171	3.47	1020	809

CHAPTER III

CELL LIBRARY AND MEMORY DESIGN

3.1 Introduction

CHAPTER II discusses the accurate data for the cell library and memory design. The measured data is used to develop the cell library and verify the Encounter Library Characterization tool rise/fall results, and cell size with functional high temperature designs in mind. These data is important for the memory design for identical reasons and are the basis for calculating delay, leakage current and power. This CHAPTER discusses the cell library design and the memory design in details.

3.2 Cell Library Design

The existence of high temperature cell library allows for fast design of the complex digital devices. The top modules (HC11, LEON3 and SRAM layout with Encounter support) are designed based on the cell libraries, and later placed & routed with the required timing. The design procedures of a standard cell library includes creating cells, extracting timing for each cell, and abstracting the cell for place and route; these are discussed in CHAPTER I. The vendor supplied model is not accuracy on I_{OFF}, which can cause characterization errors by using Cadence Characterization tool if the cells are not carefully designed. Here a methodology is developed to design the cells, which makes the characterization valid for all the cells. Sufficient I_{ON}/I_{OFF} ratio is important for cell functionality, this ratio is affected by the cell variability as well; with sufficient I_{ON}/I_{OFF} ratio assured from Table 2.4 and 2.5, switching of a cell under the worst case corner is known, and rise/fall times of a cell can also be assured resulting in robust

designs. Furthermore, to optimize the noise margin of a cell, the geometries need to ensure the switching threshold at VDD/2 (beta-match requirement) [18]. Equation (3.1) and (3.2) are developed to ensure sufficient I_{ON}/I_{OFF} ratio while maximizing the noise margin [18] across process:

$$\begin{aligned}
\mu N \cdot \left(\frac{W_N}{L_N}\right)_{INV} &= \mu P \cdot \left(\frac{W_P}{L_P}\right)_{INV} \\
\mu N \cdot \left(\frac{W_N}{L_N}\right)_{INV} &= \mu P \cdot \left(\frac{W_P}{L_P}\right)_{INV} \cdot \left(\frac{S_{NOR}}{m_{NOR}}\right) \\
\mu N \cdot \left(\frac{W_N}{L_N}\right)_{INV} \cdot \left(\frac{S_{NAND}}{m_{NAND}}\right) &= \mu P \cdot \left(\frac{W_P}{L_P}\right)_{INV}
\end{aligned} \tag{3.1}$$

$$\begin{aligned}
k_G(INV) &= \frac{\mu I_{ON} - 3 \cdot \sigma I_{ON}}{\mu I_{OFF} + 3 \cdot \sigma I_{OFF}} \\
k_G(NOR) &= \frac{\mu I_{ON} - 3 \cdot \sigma I_{ON} \big/ \sqrt{S_{NOR} \cdot m}}{m \cdot \left(\mu I_{OFF} + 3 \cdot \sigma I_{OFF} \big/ \sqrt{m}\right)} \\
k_G(NAND) &= \frac{\mu I_{ON} - 3 \cdot \sigma I_{ON}}{S_{NAND} \cdot \mu I_{OFF} + \sqrt{S_{NAND}} \cdot 3 \cdot \sigma I_{OFF}}
\end{aligned} \tag{3.2}$$

where "m_{NOR}" and "m_{NAND}" are the numbers of the PMOS/NMOS inputs. "μP" and "μN" are the mobility of PMOS and NMOS, respectively. "W_P/L_P" and "W_N/L_N" are the 1X INV geometries for the designed PMOS and NMOS, respectively. "S_{NOR}" and "S_{NAND}" are the scaling factors for NOR and NAND, respectively. Equation (3.1) is developed based on the ratio r equals 1 when V_{TP} and V_{TN} are equal [18]. "μI_{ON}" and "σ-I_{ON}" are the mean and variation of single transistor I_{ON}, respectively. "μI_{OFF}" and "σ-I_{OFF}" are the mean and variation of single transistor I_{OFF}, respectively. "k_G(INV)", "k_G(NOR)", and "k_G(NAND)" are the worst case I_{ON}/I_{OFF} ratios for INV, NOR and NAND gates, respectively and evaluated by substituting S_{NOR} and S_{NAND} from Equation (3.2). k_G(INV), k_G(NOR) and k_G(NAND) should be ≥ 100 for the delay error to be independent of the leakage current. The modeled I_{ON} is consistent with the data and the modeled I_{OFF} is smaller than the measured I_{OFF}, as observed from CHAPTER II. As the result, characterizations via Cadence timing tools can be considered valid. With Table 2.4 and 2.5, Equation (3.1) and (3.2), W_P/L_P and

W_N/L_N are such that the 1X INV which ensure $k_G > 500$ and maximize the noise margin. As in Table 2.4 and 2.5, only NMOS length of 1.6um results in $k_G > 500$ while shorter measured geometries have insufficient k_G. Note that Table 2.4 and 2.5 are the worst case I_{ON} and I_{OFF} for LEON3 (200 ℃) and HC11 (275 ℃) designs, respectively. Acceptable W_P/L_P and W_N/L_N were found to be 1.4/0.8um and 1.4/1.6um, respectively. Then NOR or NAND geometries can be found from Equation (3.1) and (3.2). Here LEON3 NOR3 is used as an example; S_{NOR} of NOR3 is found to be 3 using Equation (3.1) and (3.2); and as a result $k_G > 500$. NOR3 has the smallest k_G of all the cells as a result of the weak pull-up [35]. k_G of NOR3 is smaller than the 1X INV, note Table 2.4; also a 2-input NOR has a larger k_G than NOR3 using Table 2.4 data and Equation (3.2). The designed NOR3 geometries are shown in Fig. 3.1. It should be noted that from Table 2.4 NMOS 1.4um/1.5um may be valid. However, these test cells were not included on the mask and for this reason are not considered.

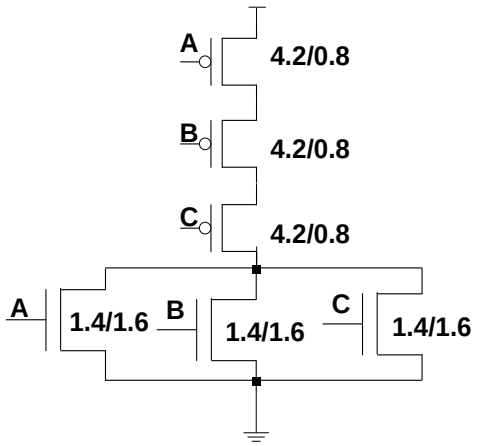


Fig. 3.1 NOR3 schematic with geometries used.

With W_P/L_P and W_N/L_N, all the cell geometries in the standard cell library are determined by solving S_{NOR} or S_{NAND} from Equation (3.1) as in Fig. 3.1. The worst case I_{ON}/I_{OFF} ratios for all cells > 500 are assured using Equation (3.2). All cells are functional designs which rise/fall times are accurately evaluated after post extraction for LEON3 and HC11 designs, respectively. Furthermore, the cell geometries maximize the noise margin. By example, a 3-input NAND uses

the following geometries where PMOS and NMOS sizes equal 1.4/0.8um and 4.2/1.6um, respectively. All the cells designed are listed in Appendix A.

3.3 Memory Design

In this section, memory designs are discussed in detail. The memories designed for HC11 and LEON3 include: a 4K on-chip SRAM, 512byte on-chip ROM, 4K SPI-SRAM, 2K SPI-ROM , 2K x16 off-chip SRAM, 128 x 32 cache, and 32 x 32 cache. The on-chip 4K SRAM is used to store the data and instructions executed by the HC11. The on-chip 512byte ROM is able to perform a sequence of the HC11 peripheral and register self-test process where the ROM code controls the bootstrap process and is able to boot from either SCI or SPI interface. The 4K SPI-SRAM is used for off-chip storage of data and software routines to be uploaded and executed by the HC11. The 2K SPI-ROM is used to store a small monitor program, 68MON which is a monitor/debugger program for the HC11. Both on-chip and off-chip ROMs are customer mask designs. The masking operation was completed separately from the other structures and programmed using a combination of Matlab and Cadence SKILL language. The off-chip 2K x 16 SRAMs are used for program and data storage, and they communicate with the LEON3 using a memory controller bridge. The 128 x 32 caches are used in LEON3 for high speed data and instruction storage. The 32x32 cache is used for the register file in the LEON3.

3.3.1 The Architecture of the Memories

The off-chip 2K x 16 SRAM, Fig. 3.2, is constructed using a compare circuit, a control circuitry, pre-decoders, decoder drivers, latches and I/O buffers, and 8 SRAM banks. Each SRAM bank includes: RAM cells, sense amps, write circuitry all arrayed in a 256 x 16 arrangement. The SRAM is designed for low power high temperature applications up to 275 ℃ operating at 18MHz for LEON3. LEON3 standard write and read are shown in Fig. 3.3(a) and (b), respectively [22]. Write access to SRAM has a lead-in, data and lead-out cycle, while a write starts at the falling

edge of “rwen”, as in Fig. 3.3(a). A read access to SRAM consists of two data cycles and 1 lead-out cycle. Read data is latched on the rising edge of the clock on the lead-out cycle.

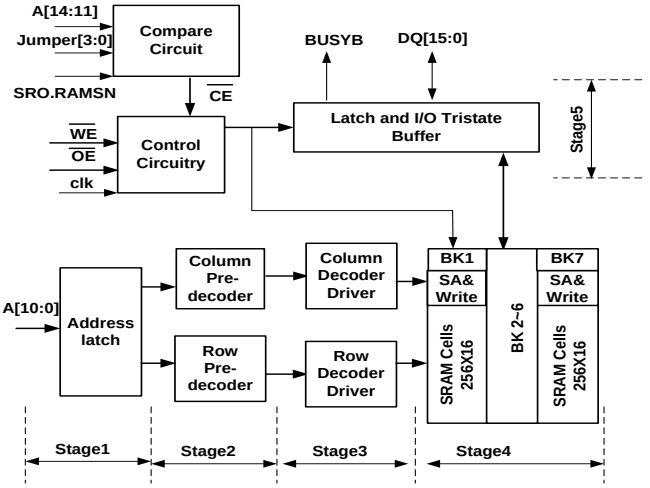
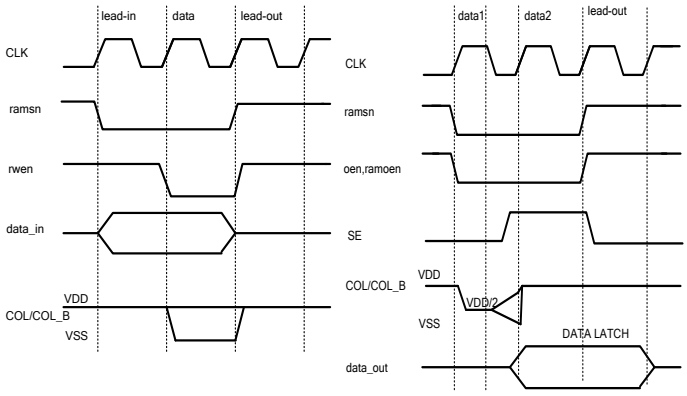


Fig. 3.2 The 2K x16 SRAM block diagram for LEON3.



(a) write timing (b) read timing

Fig. 3.3 LEON3 write and read timing.

An identical architecture is used for the other memories. The SPI 4K-SRAM for HC11 has the same architecture as the LEON SRAM, and it is specified in Appendix B. The difference being on-chip cache has no sense amp, and no complex control circuitry required as results of 8T cell usage. For the ROM, write circuitry is removed and no sense amp is required; the 2K SPI-ROM is specified in Appendix C. In this CHAPTER, 2K x 16 SRAM for 200 ℃ LEON3 is discussed in

detail including: critical delay path, SRAM design issues, 6T PMOS SRAM cell design and sense amp design.

3.3.2 Critical Delay Path

As in Fig. 3.2, read access time for the SRAM is limited by the delay times from five stages; address latch(stage 1), row pre-decoder(stage 2), row decoder driver(stage 3), SRAM cell and sense amp(stage 4), and latch and I/O tri-state buffer(stage 5). The latch delays of stage 1 and stage 5 are calculated as in Equation (3.3) [24]. A predecoding technique [14] is used in pre-decoder providing an efficient mechanism to trade off speed and power. Pre-decoder delay is calculated from Equation (3.4) [26]:

$$\tau_{rise\_o} = \tau_{rise}(NOR2) + \tau_{fall}(NOR2) \tag{3.3}$$

$$\tau_o = 2.72 \cdot \tau_i \cdot n \tag{3.4}$$

where τ_{rise_o} is the output rise time of SR-latch. τ_{rise}(NOR2) and τ_{fall}(NOR2) are the rise time and fall time of the 2-input NOR gate, respectively. τ_o is the output delay. n is the number of stages. The logic-level time constant is $\tau_i = C_i/g$. C_i is the logic-level capacitance. g is the logic-level conductance.

Row decoder buffer and column decoder buffer delays are also calculated from Equation (3.4). In the 2K-SRAM implementation, the row pre-decoder has the greater delay. The stage 4 delay is discussed in Section 3.4.3 and all other stages can be designed for optimal delays equivalent to an optimal buffer design [51][52].

3.3.3 General SRAM Design Issues

The design issues for SOS SRAM and sense amp are: I_{ON}/I_{OFF}, floating body effect, mid-rail read, V_{TH} of the SRAM cell, and mobility. As discussed in CHAPTER II, the worst case I_{ON} and I_{OFF}

for a single device are at 200 ℃. For the SRAM columns, the worst case leakage is defined by the leakage current when "reading a 1" from polarized cells of all 0's or 255 leakage paths at 200 ℃. $I_{ON} - 255I_{OFF}$ needs to be sufficient large to assure a valid read with an acceptable delay. Also I_{ONP}/I_{OFFN} is required to be sufficient to assure read stability. The floating body effect can affect SRAM cell write stability, read stability, and total SRAM delay if the SRAM cell and sense amp are not properly addressed. PMOS pass gates are used to eliminate/minimize the kink effect resulting from the floating body because PMOS kink is less than NMOS kink and occurs at a higher voltage, as discussed in CHAPTER II. SRAM columns are pulled to VDD when not in use and read or sensed at mid-rail. This has the effect of biasing the floating PMOS pass gate body to maximize V_{TH}. A stacked NMOS structure is used for the sense amp to eliminate the kink effect [8]. The worst case V_{TH} occurs at 200 ℃ due to the reduced V_{TH} effect on SRAM read stability [29]; the V_{TH} decreases with increasing temperature, note Fig. 2.4. The detailed calculation of SRAM V_{TH} is required to assure reliable SRAM cell write and read. The mobility is used for calculation of write and read stability; however, mobility variation is ignored, note CHAPTER II. In summary, SRAM design methodologies developed for kinked SOS CMOS are: 1) use PMOS pass gates, 2) hold SRAM columns at VDD when not in use, 3) apply a mid-rail read, and 4) use stacked NMOS for sense amp. These are addressed in Section 3.3.4 in detail.

3.3.4 PMOS SRAM Cell Design

Fig. 3.4 shows the PMOS SRAM cell schematic. SRAM write operation is shown in Fig. 3.3(a): hold SRAM columns at VDD, write to SRAM cell at "data" cycle, and drive the columns back to VDD after a write. SRAM read operation is shown in Fig. 3.3(b): the SRAM columns are precharged to VDD/2, precharge is then turned off, and the SRAM cell row is enabled. This drives the differential column voltage to ΔV_{SA}, and with ΔV_{SA} established the sense amp is enabled, and the column voltage is evaluated. The sense amp regenerates driving the sense amp

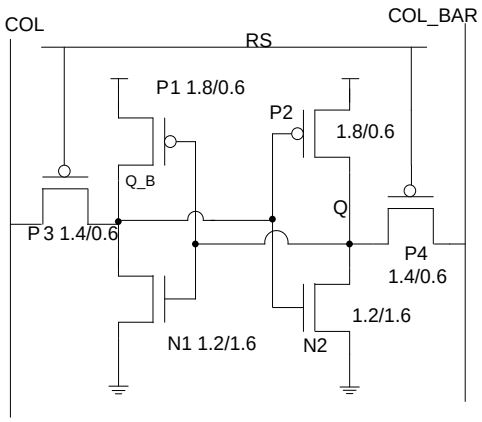


Fig. 3.4 6T PMOS SRAM cell schematic.

Table 3.1
SRAM cell worst case V_{TH} at 200 ℃

	μV_{TH}	1σ-V_{TH}	V_{TH} Wors Case
	(V)	(mV)	(V)
P3,P4 at write	0.530	11.0	0.530+3*0.011=0.563
P3,P4 at read	0.530	11.0	0.530-3*0.011=0.497
P1,P2 at write	0.630	13.0	0.630-3*0.013=0.591
P1,P2 at read	0.630	13.0	0.630+3*0.013=0.669
N1,N2 at write	0.560	84.0	0.560-3*0.084=0.308
N1,N2 at read	0.560	8.00	0.560-3*0.008=0.536

outputs to logic levels. Then the outputs of sense amp force the columns back to VDD. As results, SRAM columns are held to VDD for 2/3 of the write cycle and 1/2 of the read cycle. This has the effect of biasing the PMOS pass gate bodies or column voltages at an average ≥ 2/3 of VDD as a worst case scenario or V_{SB} then averages 1/3 VDD. Equation (3.5) [3] is used to calculate the effect if V_{SB} on.

$$V_{THP} = V_{TH0} + \gamma \cdot \left(\sqrt{\left| 2\phi_F \right| + V_{SB}} - \sqrt{\left| 2\phi_F \right|} \right) \tag{3.5}$$

where V_{THP} is the PMOS threshold voltage when substrate bias is presented. V_{SB} is the source-to-body substrate bias. Φ_F is the surface potential. γ is the body effect parameter. $\Phi_F = 0.42$, $\gamma = 0.14$ in this dissertation [8]. As discussed in CHAPTER II, the transistors are measured in the kink

region in this work and their threshold should be calculated from this work; the transistors which are not in kink use the previous work data [8]. The ±3 sigma V_{TH} is decided from the worst case corner to assure write and read stability [25]. SRAM cell V_{TH} is calculated from Equation (3.5) and summarized in Table 3.1.

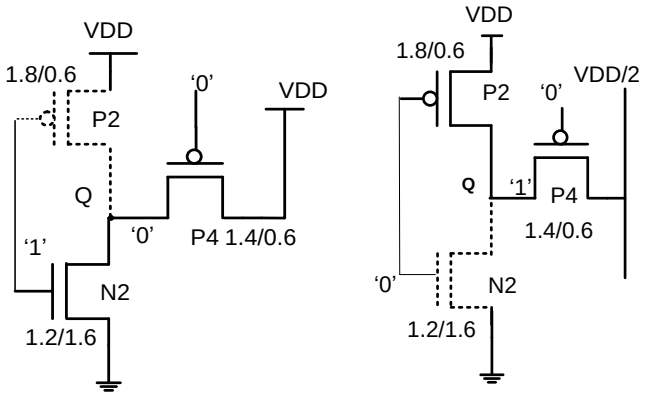


Fig. 3.5 SRAM simplified model for write operation and read operation.

Fig. 3.5(a) shows the simplified model used during write operation. It is reasonable to assume the gate of P4 is stay at GND while V_{GSN} of N2 is around 2.5V. P4 needs to be sufficiently strong to pull "Q" to VDD-V_{THN} to assure a correct write [18]. The I_{OFF} of P2 is negligible, note Table 2.4. N2 is in the kink region and P4 is not in kink as "Q" is approximately VDD-V_{THP1}. V_{THP1} equals 0.59V at write. Equation (3.6) is developed from the write current path [18]:

$$KP_{P4} \cdot \frac{W_{P4}}{L_{P4}} \cdot \left(\left(VDD - |V_{THP4}|\right) \cdot \left(VDD - V_Q\right) - \frac{\left(VDD - V_Q\right)^2}{2} \right) = \frac{1}{2} K_{kink} \cdot KP_{N2} \cdot \frac{W_{N2}}{L_{N2}} \cdot \left(V_{GSN} - V_{THN2}\right)^2 \tag{3.6}$$

$$V_Q = \mu_{P2} \cdot |V_{THP2}| - VDD \cdot (\mu_{P2} - 1) + \sqrt{(-2\mu_{P2}{}^2 \cdot VDD \cdot |V_{THP2}| - CR \cdot \mu_{N2} \cdot K_{kink} \cdot (V_{GSN} - V_{THN2})^2 + \mu_{P2}{}^2 \cdot (V_{THP2}^2 + VDD^2)} \tag{3.7}$$

$$CR = \frac{W_N / L_N}{W_{PPASS} / L_{PPASS}}$$

where V_Q is the voltage drop at node "Q". V_{GSN} is the V_{GS} of N2. V_{THP4} and V_{THN2} are the threshold voltages of P4 and N2, respectively. Using Table 3.1, V_{THP4} and V_{THN2} are 0.57V and 0.31V, respectively. KP_{P4} and KP_{N2} are the μCox of P4 and N2, respectively; the mobility data at 200 ℃ is used, note CHAPTER II. K_{kink} is the kink factor, which is defined as the increased current due to the kink; K_{kink} is calculated from the measured current divided the calculated current, note CHAPTER II. K_{kink} is listed in Table 3.2.

Solving for V_Q from Equation (3.6) leads to Equation (3.7) using Derive 6. CR, cell ratio, is defined as the size ratio between NMOS access transistor and PMOS pass transistor. The dependence of V_Q on CR is plotted in Fig. 3.6. CR≤0.32 is required to assure V_Q > 2.71V or V_Q>VDD-V_{TP}. Using Equation (3.7) and accurate data, CR is found to be ≤0.32 cross temperature and process corners.

Table 3.2
K_{kink} values for different lengths NMOS

	L=1.1um	L=1.3um	L=1.4um	L=1.6um
K_{kink}	1.10	1.06	1.14	1.06

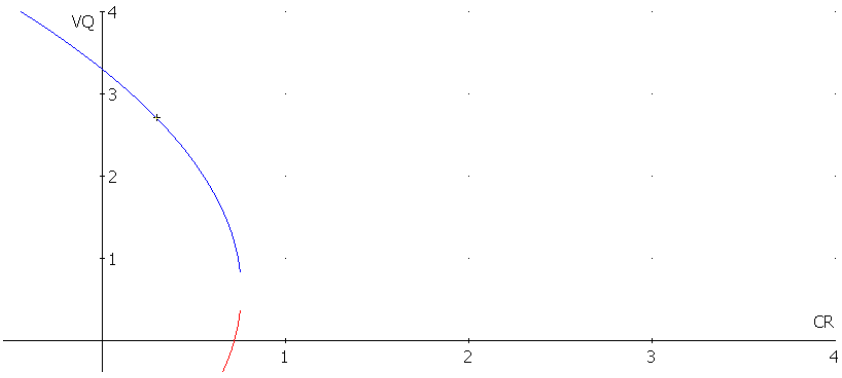


Fig. 3.6 V_Q vs CR.

Fig. 3.5(b) shows the simplified model used for read operation where both P2 and P4 are not kinked. It is reasonable to assume both the gates of transistors P2 are held at less than 0.4V and P4 stay at GND. "Q" needs to preserve "1" and ensures "Q" cannot drop below VDD-V_{THP1} [18].

V_{THP1} equals 0.67V at read. The I_{OFF} of N2 needs to be much smaller than the PMOS I_{ON} otherwise the cell can be flipped by the large I_{OFF}. An L of 1.6um is chosen to ensure I_{OFF} is less than 0.1% of I_{ON}, note Table 2.4. Equation (3.8) is developed from the read current path [18]:

$$KP_{P4}\cdot\frac{W_{P4}}{L_{P4}}\cdot\left((VDD-\Delta V-V_{THP4})\cdot(VDD-V_{COL}-\Delta V)-\frac{(VDD-V_{COL}-\Delta V)^2}{2}\right)$$
$$=KP_{P2}\cdot\frac{W_{P2}}{L_{P2}}\cdot\left((VDD-V_{THP2})\cdot\Delta V-\frac{\Delta V^2}{2}\right) \tag{3.8}$$

where V_{COL} is column voltage. ΔV is the voltage drop at node "Q". Using Table 3.1, V_{THP2} and V_{THP4} are equal to 0.67V and 0.50V, respectively. KP_{P4} and KP_{P2} are equal.

Solving Equation (3.8) leads to

$$\Delta V=\frac{\sqrt{PR^2(V_{THP2}-VDD)^2+PR(V_{COL}{}^2-2V_{COL}V_{THP4}+2V_{THP2}(V_{THP4}-VDD)+VDD^2)+V_{COL}{}^2-2V_{COL}V_{THP4}+V_{THP4}{}^2}}{PR+1}$$
$$+\frac{PR(VDD-V_{THP2})-VTHP4+VDD}{PR+1} \tag{3.9}$$
$$PR=\frac{W_{PPULL}/L_{PPULL}}{W_{PPASS}/L_{PPASS}}$$

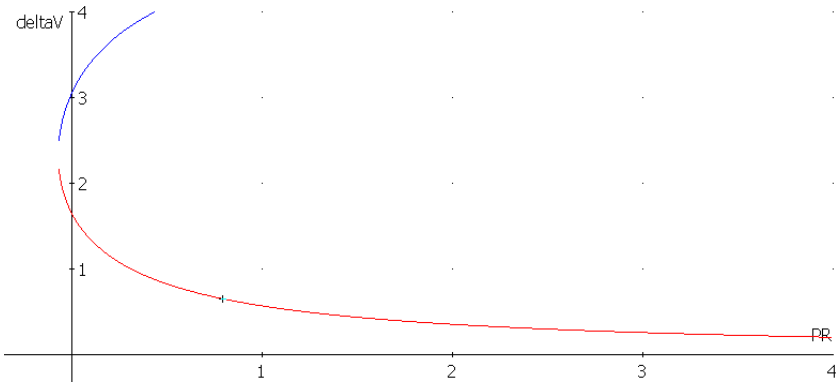


Fig. 3.7 ΔV vs PR.

PR, pull-up ratio, is defined as the size ratio between PMOS access transistor and PMOS pass transistor. The dependence of ΔV on PR is plotted in Fig. 3.7. PR≥0.8 is required to assure $\Delta V<0.67V$ or $<V_{THP}$. Using Equation (3.9) and accurate data, PR is found to be ≥0.8 cross temperature and process corners.

With Equation (3.6)~(3.9), SRAM cell size should be designed to be small, while assuring robust write and read stability [18]. SRAM cell size is shown in Fig. 3.4 and compact SRAM cell layout is shown in Fig. 3.8. With the length of NMOS chosen to be 1.6um, the SRAM CR and PR are found from Equation (3.7) and Equation (3.9). The SRAM cell designed in 2008 has 1.4um length. Table 2.4 shows NMOS of 1.4um length has 843.5nA leakage while NMOS of 1.6um has only 2.67nA leakage. As shown in Equation (3.8), this large I_{OFF} can increase ΔV significantly and the read stability requirement cannot be satisfied; this large I_{OFF} can flip the cell and cause a read error. This results in reducing SRAM yield; the detailed SRAM testing is discussed in CHAPTER IV.

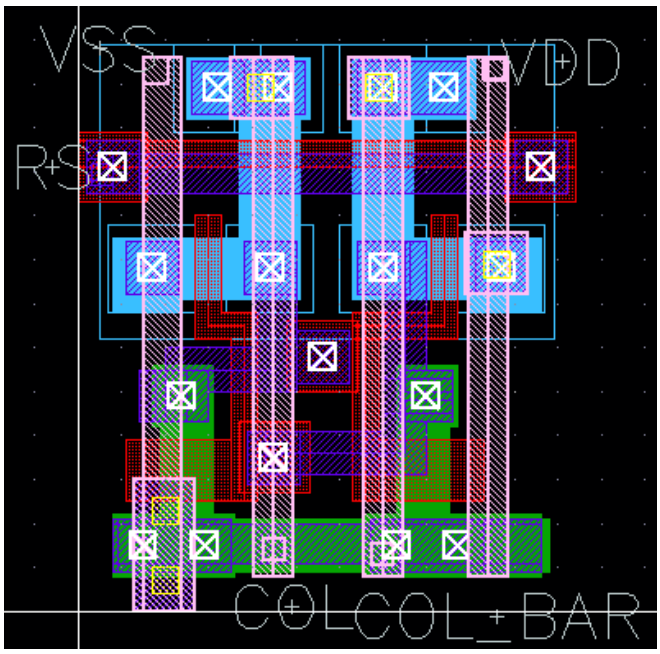


Fig. 3.8 6T SRAM layout (x=9.8um, y=11.8um).

The SRAM cell size is designed using Rabaey's method [18]. The Static Noise Margin (SNM) is also calculated to show the adequate design [29] [30] using the same parameters as applied to Equation (3.6) and (3.8). For our PMOS SRAM cell, the worst case read stability situation is when the PMOS pass gates are selected and column voltages are at VDD/2. I_{OFFN} is negligible

since it is only 0.1% of the I_{ONP}, note Table 2.4. Using the approximations in [30], the current equations are:

$$\begin{aligned} I_{P2} &= I_{P4} \\ I_{P3} &= I_{N1} \end{aligned} \tag{3.10}$$

P2, P4, P3 and N1 are not in kink region. Similar to Equation (3.6) and (3.8), the voltages at Q and Q_B can be found from Equation (3.11):

$$\begin{aligned} & KP_{P2} \cdot \frac{W_{P2}}{L_{P2}} \cdot \left((VDD - V_{Q\_B} - V_{THP2}) \cdot (VDD - V_Q) - \frac{(VDD - V_Q)^2}{2} \right) \\ &= KP_{P4} \cdot \frac{W_{P4}}{L_{P4}} \cdot \left((V_Q - V_{THP4}) \cdot \left(V_Q - \frac{VDD}{2} \right) - \frac{\left(V_Q - \frac{VDD}{2} \right)^2}{2} \right) \\ & \frac{1}{2} KP_{P3} \cdot \frac{W_{P3}}{L_{P3}} \cdot \left(\frac{VDD}{2} - V_{THP3} \right)^2 = KP_{N1} \cdot \frac{W_{N1}}{L_{N1}} \cdot \left((V_Q - V_{THN1}) \cdot V_{Q\_B} - \frac{{V_{Q\_B}}^2}{2} \right) \end{aligned} \tag{3.11}$$

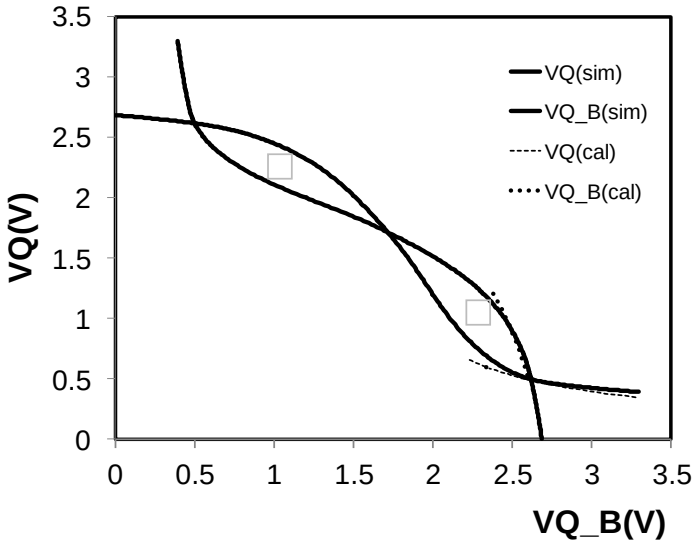


Fig. 3.9 The simulation static voltage transfer characteristics (VTCs) of the two cross-coupled inverters during read access of the cell are represented by the solid curves. The same VTCs from calculation are represented by the dash curves.

The above approximations are plotted in Fig. 3.9 and compared with the static transfer characteristics generated from SPICE simulations. Both the calculations and simulations are under the same test set up when the PMOS pass gates are selected and column voltages are at

VDD/2 and at 200 ℃. The maximum square is drawn in Fig. 3.9 and results in 0.18V. The SNM of 0.18V is found at the worst case corner.

After the PMOS SRAM cell is designed, the SRAM column delay is calculated using SRAM cell geometries. The minimum SRAM column delay, t_{cell}, is required to generate the minimum SRAM column delta (ΔV_{SA}). t_{cell} is related to column capacitance (C_{COL}), cell current (I_{cell}) and leakage current (I_{leak}) and is written as:

$$t_{cell} = \frac{C_{COL} \cdot \Delta V_{SA}}{I_{cell} - I_{leak}} \tag{3.12}$$

where C_{COL} is extracted using Cadence Diva Extractor as 800fF. I_{cell} varies as results of process and temperature variations and is considered as Gaussian distribution [4] biased by temperature. I_{leak} is defined by the leakage current when "reading a 1" to polarized cells of all 0's or 255 leakage paths. During read, PMOS transistors (P2 and P4) form a read path to pull up the columns from VDD/2 to VDD/2 ± ΔV_{SA}. The series PMOS P2 and P4 are in triode region and can be considered as a composite PMOS where L equals 1.2um. I_{ON} and 255 I_{OFF} are calculated to be 61.4uA and 28.7nA, respectively, as in Table 3.3. For C_{COL} equals 800fF, ΔV_{SA} equals 50mV ± 3σ-Vos; the mean and the 3σ variation of t_{cell} is 0.42ns ± 0.36ns.

Table 3.3
I_{ON} and I_{OFF} and their variations of SRAM pass transistors at 200 ℃

	μI_{OFF} of 255 cells	σ-I_{OFF} of 255 cells	worst case I_{OFF}	μI_{ON} at V_{DS} =1.65V	σ-I_{ON} at V_{DS} =1.65V	worst case I_{ON}
	(nA)	(nA)	(nA)	(uA)	(uA)	(uA)
PMOS 1.4/0.6um at read	44.4	6.07	62.6	192	32.5	94.2
PMOS 1.4/1.2um at read	22.2	2.15	28.7	95.9	11.5	61.4
PMOS 2/0.6um	28.5	3.78	39.9	274	38.8	157

Fig. 3.10 shows the "Delay Circuit" which is used to ensure a successful read; this requires the Delay Circuit delay to be greater than t_{cell} delay. The Delay Circuit uses 4 1X INVs in series.

With the data in CHAPTER II, the mean and 3-sigma delay of the 4 INVs is calculated to be 2.24ns and 61.9ps, respectively. Using the Monte Carlo simulations, the Delay Circuit has a mean and 3-sigma variation of 2.18ns $\pm$ 19.5ps and is sufficient to meet the requirement for t_{cell}. Timing based on measured data and Monte Carlo simulations show the designed Delay Circuit satisfied the 3-sigma delay requirement.

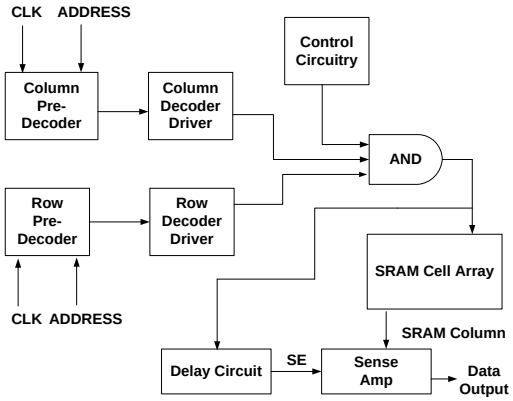


Fig. 3.10 SRAM's read circuitry block diagram.

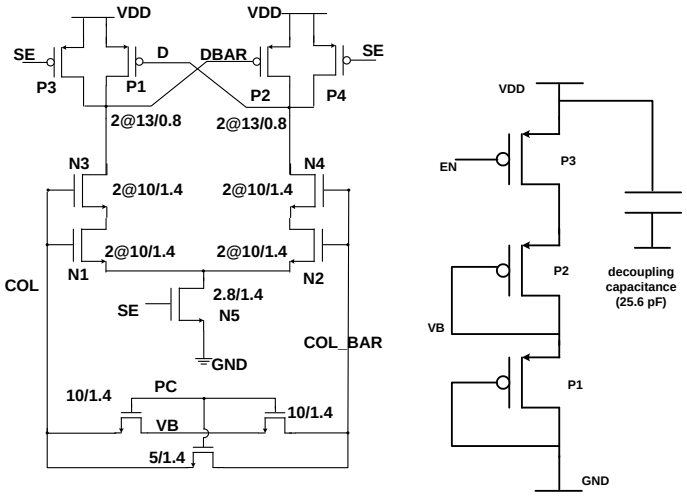
3.3.5 Stacked-NMOS Sense Amp Design

The current-mode latch sense amp is shown in Fig. 3.11(a) [16]. The sense enable signal, "SE", allows sense amp to be switched off to save power when not in use. As SE is turned on, the sense amp starts to regenerate following a short intrinsic delay of N1~N4.The sense amp regenerates driving D and DBAR to their valid logic levels. The sense amp read delay is approximated by:

$$t_{sense} \approx 2 \cdot C_{gdop} \cdot V_{THP} / I_{SA} + \frac{C_{gsp}}{gm_n - g_o} \ln \frac{V_{final}}{V_{OD}} \tag{3.13}$$

where C_{gsp} and C_{gdop} are the gate to source capacitance and overlap capacitance of the PMOS pair [Fig. Fig. 3.11(a)], respectively; C_{gsp} is much greater than the loading of the follow on logic. The transconductance, $gm_{P,}$ of the PMOS pair is set by I_{SA}, the tail current of sense amp. g_o is the output conductance at node D and DBAR. V_{final} equals 0.8 VDD. V_{OD} is a sufficient overdrive voltage to timely settle the sense amp. V_{OD} equals $|\Delta V_{SA}|$ minus $|V_{OS\_SA}|$. As in Fig. 3.11(b), a

PMOS diode divider is used to bias COL and COL_BAR to VDD/2 during bank select ensuring N1~N4 operate in saturation during read. The enable signal "EN" also switches off all PMOS diode bank bias circuit when not in use. A local decoupling capacitance [Fig. 3.11(b)] of 25.6pF is used across VB to reduce the power and ground fluctuations. Spectre simulation shows power fluctuation is only 0.3V and settles within 7ns.



(a) (b)

Fig. 3.11 Current-mode latch sense amp with precharge and PMOS diode bank bias circuit [16].

To reduce sense amp delay, I_{SA} can be increased reducing regeneration time, as in Equation (3.14). The V_{OS} of the sense amp is determined by the P and N transistor pair geometries [28]. Increasing the transistor size can reduce V_{OS} which results in reducing required ΔV_{SA} and SRAM cell delay. Practically transistor size is limited by the SRAM column pitch. The elected sense amp layout height is 4% of total SRAM memory array height. Moreover, reducing V_{OS} by a factor of two requires a 4 times increasing in power and area if sense amp bandwidth remains constant.

Kink effect is the final issue in sense amp design. Kink significantly reduces the output drain resistance, rds, and differential pair gm, reducing bandwidth and increasing mismatch. Stacked-NMOS (N1~N4) are used in Fig. 3.11(a), to maintain V_{DS} of N1 and N2 less than the kink voltage [8].

With gate logic, SRAM cell and sense amp design issues having been addressed, and functional 2K x 16 SRAM design simulations checked by measured data suggests 18 MHz operation over

the -55 °C to 200 ℃ is attainable. Test results confirm this valid over the room to 275 ℃ range. The SRAM kink and leakage issues are solved by: 1) the use of PMOS pass gates, 2) holding SRAM columns at VDD when not in use, 3) using a mid-rail read, and 4) using stacked-NMOS for sense amp. The total delay of an SRAM cell and sense amp is read approximated by:

$$t_{total\_delay} \approx \frac{C_{COL} \cdot \Delta V_{SA}}{I_{cell} - I_{leak}} + 2 \cdot C_{gdop} \cdot V_{THP} / I_{SA} + \frac{Cgsp}{gm_p - go} \ln \frac{V_{final}}{V_{OD}} \tag{3.14}$$

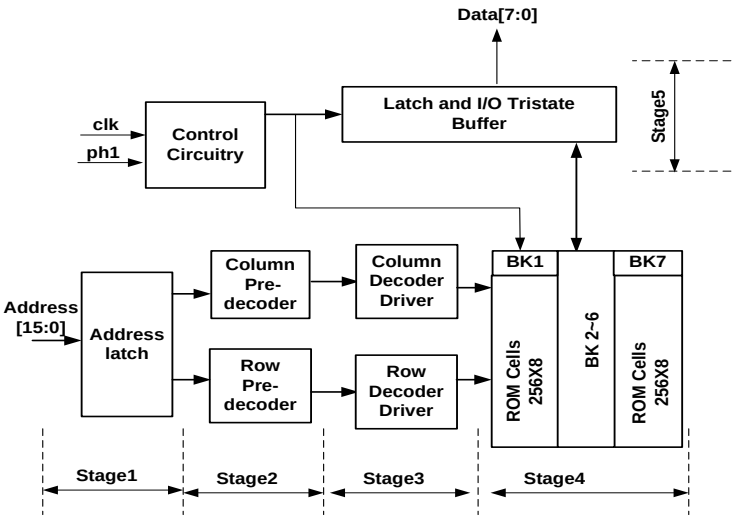


Fig 3.12 2K ROM structure.

3.3.6 ROM Design

The ROMs designed for HC11 include: the 2K SPI-ROM, and the 512byte on-chip ROM. The 2K ROM structure is shown in Fig. 3.12. Similar to SRAM, access time for the ROM consists of the sum of the delay times of five circuit stages: address latch (stage 1), pre-decoder (stage 2), decoder driver (stage 3), ROM cell (stage 4), and latch with I/O tri-state buffer (stage 5). As shown in Fig. 3.13, the ROM cells are connected to either VDD or VSS depending on the value of the bits stored and are read from columns. After the ROM layout without the "data" connection to VDD/VSS finished, the resulting layout was completed with metal lines placed on the original layout by using SKILL code written to instantiate the desired logic bit. The ROM kink and

leakage current issues are solved by using PMOS as the ROM cell. Using Table 3.3, the worst case column leakage is 63.5nA for 255 cells. Compared with worst case I_{ON} of 157.3uA, the leakage is small enough to be ignored.

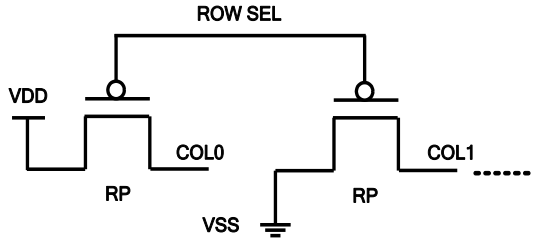


Fig. 3.13 ROM cell structure.

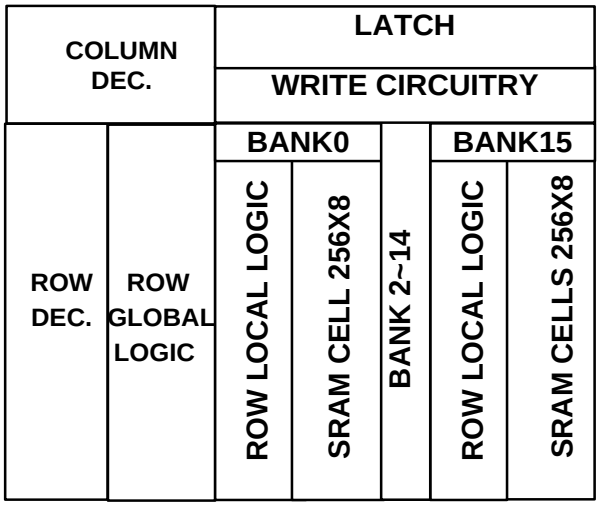


Fig 3.14 128 x 32 cache structure.

3.3.7 Cache Design

The caches designed for LEON3 include: the 128 x 32 cache, and the 32 x 32 cache. The 128 x32 cache structure is shown in Fig. 3.14. The On-chip caches have similar structures as the off-chip 2K x 16 SRAM. However, the cache size, is only 1/32nd the off-chip SRAM, makes the 8T SRAM cell suitable for the cache usage. As shown in Fig. 3.15, the 8T SRAM cell provides significantly larger SNM compared with 6T SRAM with only a 30% area penalty [21]. The small memory size made the 30% increase of the layout area reasonable because the cache is only 4%

of LEON3 in area. Furthermore, the small column capacitance and the strong drive of the 8T SRAM ensure the cache fast enough and with an adequate logic level for use without need of a sense amp. The precharge technique is used to pull down the SRAM columns before a read because this 8T SRAM cell cannot pull down by itself. The SRAM kink and leakage issues are solved by: PMOS pass gates, and sufficient NMOS length. Read and write times are equal and 21.25ns at 200 ℃. Using Table 3.3, the worst case I_{OFF} of 255 cells on COLR is 28.7nA and the worst case I_{ON} on COLR is 84.1uA. The 128 x 32 cache is instantiated as a cell using its timing and abstraction files. Later LEON3 is placed and routed using the cell library and the instantiated caches.

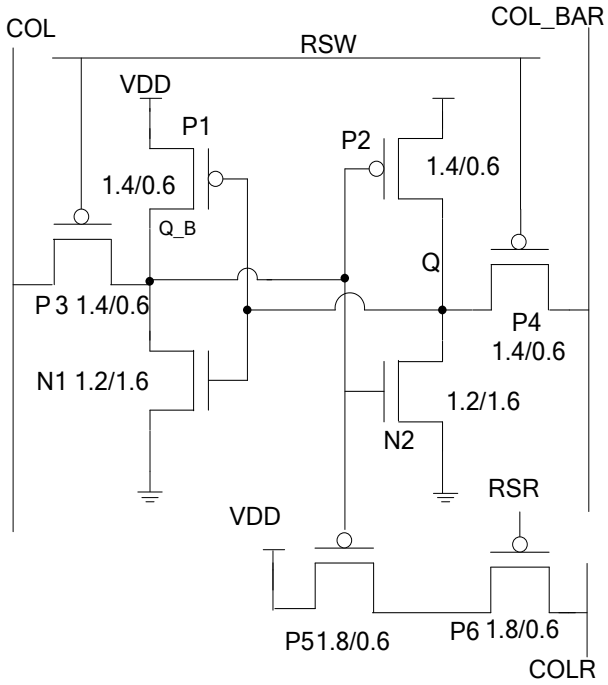


Fig.3.15 8T SRAM cell schematic.

3.4 Summary

This chapter discusses the design methodologies of cell libraries and memories. Equation (3.1) and (3.2) are developed for easy design of cell libraries based on the measured data from CHAPTER II. All cells are functional designs which rise/fall times are accurately evaluated for

LEON3 and HC11 designs, respectively. The 2K x 16 off-chip SRAM is used as an example of 6T PMOS SRAM design; write stability, and read stability of the SRAM are assured at worst case temperature and process corners; the SRAM column delay and sense amp delay are discussed as well. Finally, ROM design and cache design are discussed briefly as they have easier design issues compared with 2K x 16 off-chip SRAM.

CHAPTER IV

MEMORY TESTING

4.1 Introduction

CHAPTER III discusses 2K x 16 off-chip SRAM for LEON3, ROMs for HC11 and caches for LEON3. The 4K on-chip SRAM and 4K SPI-SRAM for HC11 were tested which have identical structures and are discussed in this chapter. The 2K x 16 off-chip SRAM for LEON3 was not tested but has a structure identical with the HC11 SRAMs. The caches for LEON3 and ROMs for HC11 are also discussed in this chapter. Full working die were found for all these designs. Testing faults are also found as usual in memory testing. Shorted circuit die were found to be a significant process issue for 2007 and 2008 fabrication runs. The row, cell, and column errors were observed for 4K SPI-SRAM and 2K SPI-ROM. It is believed that row and cell errors are predominantly caused by physical defects and/or strong (leaky NMOS) transistors in the row decoding logic and memory cells. It is believed column errors are mainly caused by Metal2 shorts. The strong(leaky NMOS) transistors is assumed to be a great source of error, as can be noted from Table 2.4 and 2.5; designs using NMOS lengths of 1.0um~1.4um result in poor I_{ON}/I_{OFF} ratios for gate logic and memory cell. The original LEON3 cell library used NMOS lengths of 1.0um and all memories used 1.4um versus the desired 1.6um are found post evaluation. The newest generation of 6T SRAM, ROM and cache was summarized in CHAPTER III.

4.2 SRAM Testing

4.2.1 SRAM Testing Condition

The 4K SPI-SRAMs were fabricated on Peregrine 0.5um SOS process in 2007 and 2008, respectively. The 6T SRAM structure is shown in Fig. 3.4 and the 4K SPI-SRAM is 16.5mm^2 in area. The reason for the second fabrication in 2008 was to improve the SRAM yield. The detailed

testing results are discussed in Section 4.1~4.3. The definition of successful write/read for SRAM is as follows: a write followed by 2 successful reads of FF's, 00's, 55's, and 255-through-0's of each byte in the die. The 4K SPI-SRAM must also pass the frequency, temperature, and voltage corners of 2MHz, 4MHz, and 8MHz, 27 ℃, 200 ℃, 275 ℃, and 295 ℃, and 2.5V, 3V, 3.3V, and 3.6V, respectively on the alessi rel 6100 probe station. Furthermore, a 16 hour test at 300 ℃ along with a 1 week test of packaged SPI SRAM on Roger board at 200 ℃ was completed to assure SRAM long time viability. The output was checked by automatic test bench code in Matlab. The Tektronix TLA 720 logic analyzer was used to provide the input pattern and observe the outputs, where the logic analyzer's switching threshold voltage was set to VDD/2. Failures were independent of temperature.

The original testing idea is from March C- test [23]. The algorithm is shown below by order:

1. Write '0' to all locations, write order is irrelevant. (Either from address n-1 down to 0 or from address 0 up to address n-1.
2. Read '0' from address 0 up to address n-1. Then write '1' from address 0 up to address n-1.
3. Read '1' from address 0 up to address n-1. Then write '0' from address 0 up to address n-1.
4. Read '0' from address n-1 down to 0. Then write '1' from address n-1 down to 0.
5. Read '1' from address n-1 down to 0. Then write '0' from address n-1 down to 0.Then read '0' and the read order is irrelevant.

March C- test covers stuck-at faults, stuck-open faults, transition faults, state coupling faults, and idempotent coupling faults. Here are the definitions of the faults [23]:

1. Stuck-at faults: The logic value of a stuck-at cell or line is always '0' or always '1'.
2. Stuck-open faults: A cell cannot be accessed, perhaps because of an open word line.

3. Transition faults: a cell fails to undergo a ‘0’ to ‘1’ transition or ‘1’ to’ 0’ transition.
4. State coupling faults: a coupled cell or column is forced to a certain value only if the coupling cell or column in given ‘1’ or ‘0’.
5. Idempotent coupling faults: the fault is sensitized by a transition write operation to a cell, which forces the contents of another cell to a fixed value (‘1’ or ‘0’).
6. Data retention faults (DRF): this occurs when a cell fails to retain its logical value after some period of time.

The March C- test algorithm was used for testing SRAM initially, and it has almost 100% fault coverage [23] but fault masking may occur; for example, a coupling fault may not be detected when the coupled cell also has a DRF because the DRF may mask the coupling fault. Stuck-at faults and stuck-open faults are discussed in Section 4.1.3. Stuck-open faults can mask stuck-at faults [23]; when a cell cannot be accessed, the columns stay at VDD/2 and the sense amp offset decides the read out data and shows stuck-at ‘1’ or ‘0’. Transition faults are not found; all the error cells suffer stuck-at ‘1’ or ‘0’, not the transition faults. State coupling fault and idempotent coupling fault are not found because no cell or column is found as the coupling fault. The cell and column errors found are only stuck-at ‘1’ or ‘0’ which are independent of adjacent cell or column [23]. Type 6) faults are not observed from the testing results. A DRF may be caused by a broken (open) pull-up transistor of a 6T SRAM. Leakage currents then will cause the node with the broken pull-up transistors to lose its charge and flip the data [23].

Currently, testing accounts for about half the cost of memory chip, so tests should only be performed to detect those faults which are reasonably likely to occur [23]. Since type 3) ~6) errors are not found, the SRAM testing patterns are simplified as SRAM testing conditions above which save half of the testing time.

4.2.2 SRAM Testing Analysis

Fig. 4.1 defines the 3 types of common errors occurring in the SRAM/ROM: cell errors, row errors and column errors. Cell errors are ≤8 cell errors for a byte oriented SRAM/ROM. However, in our case also includes many adjacent or clustered cell errors distributed in random locations. Column errors are usually one or more column errors; more specifically a column failure is the whole column or 256 bit errors; this type of error may mask a few cell errors. Row failure is usually the 1 or more row read failures; more specifically one row is the whole row of memory or 16 bytes; this type of error may also mask a few cell errors.

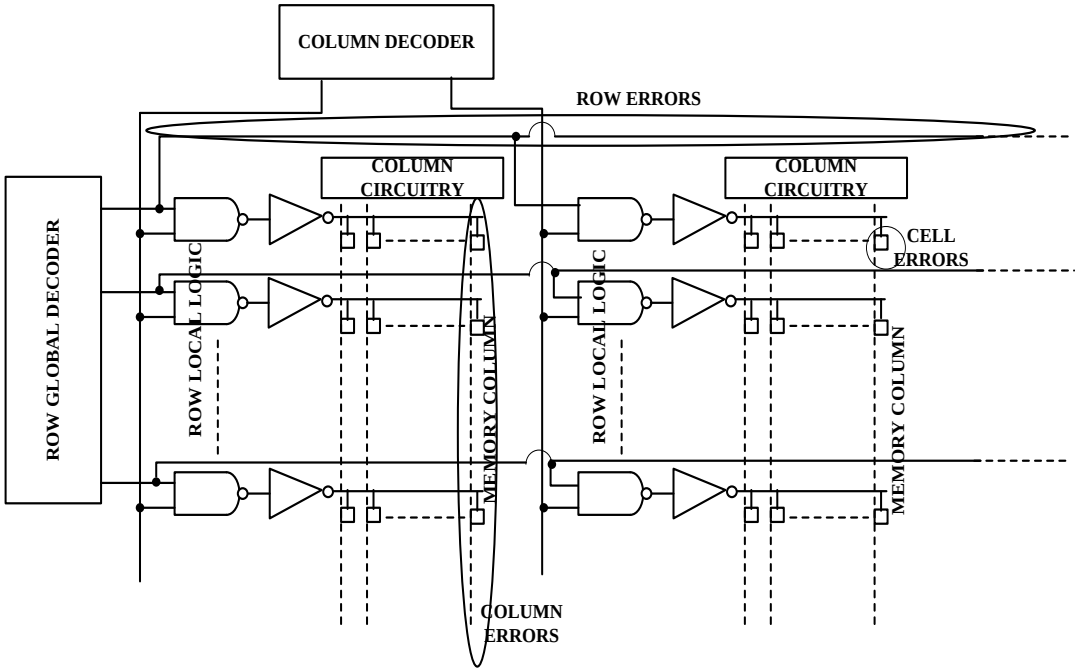


Fig. 4.1 SRAM/ROM failure types.

Table 4.1 shows the comparison of the SPI SRAM testing results in 2008 with the results in 2007. (1) In 2007 and 2008, 15.3% and 25.6% of the die read out successfully, respectively. The yield improvement is 67.3%. (2) In 2007 and 2008, 18.9% and 11.6% of the die had cell errors, respectively. This may be the benefit of improving power connections. In 2007, power connections run only horizontally. As shown in Fig. 4.3, the power connections run both vertically and horizontally in 2008 which reduce power supply drops [57]. (3) In 2007 and 2008,

34.2% and 34.7% of the die had column errors, respectively. The column errors showed no improvement. (4) In 2007 and 2008, 2.7% and 0.8% of the die had row errors, respectively. (5) In 2007 and 2008, 28.8% and 27.3% of the die were shorted, respectively. The shorted-circuit die are shorted from VDD to GND. When I_{DD} measured >30mA, die were classified as shorted. No correct data is read from the shorted-circuit die and this error is due to some process limitation.

Table 4.1
4K SRAM testing error die of 2008 and 2007

	4K SRAM in 2008	The distribution of 4K SRAM in 2008	4K SRAM in 2007	The distribution of 4K SRAM in 2007
Fully working die	31	25.6%	17	15.3%
Partially working die	57	47.1%	63	56.8%
Cell errors	14	11.6%	21	18.9%
Row errors	1	0.8%	3	2.7%
Column errors	42	34.7%	38	34.2%
Shorted-circuit die	33	27.3%	32	28.8%
Full working and partially working	88	72.7%	79	71.2%
Total	121	100%	111	100%

4.2.3 SRAM Testing Diagnosis

From the error analysis above, the column errors have no significant improvement from 2007 to 2008; 34.7% of the 4K SRAMs have these errors which reduced the SRAM yield significantly. So a detailed diagnosis is required to find the column error sources. This would be extremely useful for future memory designs. Fig. 4.2 shows the 4K SRAM structure with different error locations. These error sources are used for ROM testing diagnosis as well due to the similar structure of SRAM and ROM. There are three different error sources found from the SRAM/ROM testing:

1) Error source A: spot defect. The spot defects include 4 different types at layout level [55]: broken wires (unconnected), shorts between wires, missing contact, and poorly created transistors. Metal2 shorts may be a cause of SRAM/ROM column errors and will be discussed. Fig 4.3 shows the 6T-SRAM cell layout with possible shorts. The presents of spot defect may result in the following errors: 1) a memory cell stuck-at '0' or '1', 2) a memory cell stuck-open, 3) decoder errors, and 4) column errors [55].

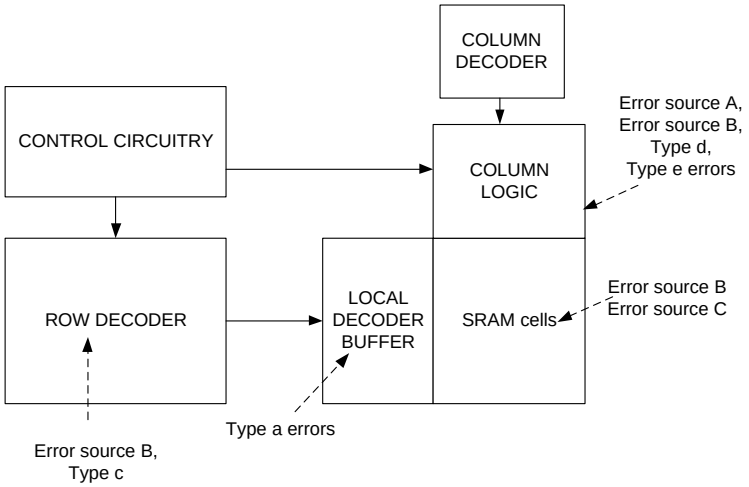


Fig. 4.2 4K SRAM structure with the error locations

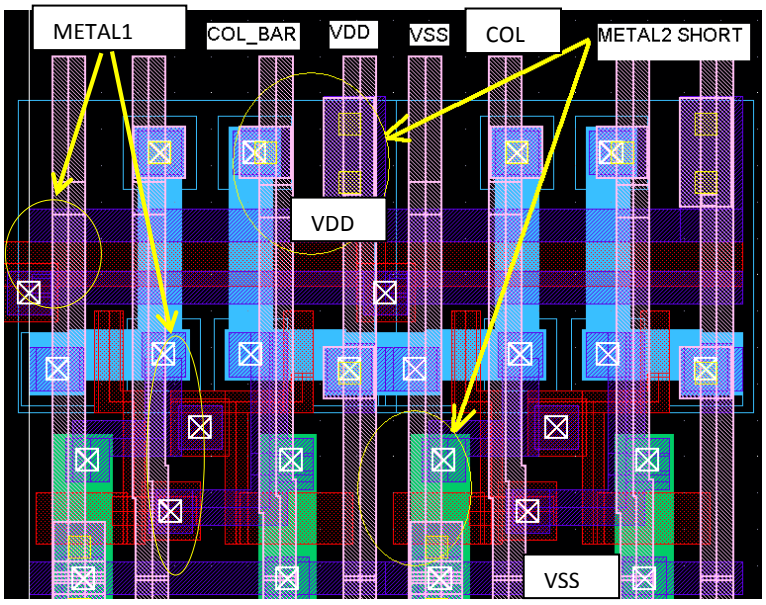


Fig. 4.3 6T-SRAM cell layout in 2008 with possible shorts.

2) Error source B: Silicon defect resulting in strong (leaky NMOS) transistors. The silicon defect is defined as excessive thick silicon in a small area of the die, which may cause lower V_{TH} for the transistor. As discussed in [56], excessive thick silicon causes high electric field at drain of SOI NMOS as well as the potential well; holes are accumulated at the subtracted and V_{BS} is increased; as a result, V_{TH} of the NMOS is reduced, note CHAPTER III. However, for thin silicon (10nm), the drain electric field is much lower and no potential well is formed, as a result kink effect is eliminated [56]. As discussed in CHAPTER III, the effective NMOS transistor V_{TH} reduced significantly at V_{DS} >1.45V due to the kink effect; excessive thick silicon is the identical reason for kink effect. NMOS with lengths ≤1.4um has excessively high leakage kink current resulting in I_{ON}/I_{OFF} <4. The logic gates with length ≤1.4um will result in a slow and/or a failed design; a typical error is a stuck-at-0 due to the strong NMOS leakage. Similar to SRAM cell, if a NMOS access transistor is strong and I_{ON}/I_{OFF} <4, the drain node of the NMOS may be stuck-at '0'; this is observed as stuck-at faults.
3) Error source C: improper testing setup caused errors of unknown origin. Several die were found with such errors. Initially an "error die" was found with errors from several locations; then when measuring the data with same testing condition but with different landing of probes, the retested error die data read out correctly for all locations. Some die were not re-measured again due to lack of understanding of source of memory errors initially. Die with this type of error were eliminated from consideration in the analysis of this work.

The detailed SRAM/ROM error classification is shown in Table 4.2 and detailed the error locations of the SRAM/ROM are defined as follows.

Type a: local decoder buffer. As shown in Fig. 4.4, the local decoder buffers for SRAM and ROM have identical structure, which include a 1X NAND, 1X inverter and 3X

inverter. As discussed above, NMOS with length ≤1.4um may be the cause of a failed design. A 1X inverter is more likely the error source than the 1X NAND or 3X inverter as a result of its greater variability. Using Equation (3.1) and (3.2) in CHAPTER III, the 1X inverter has larger cell variability and lower worst case I_{ON}/I_{OFF} ratio, compared with the 1X NAND or 3X inverter. The I_{ON}/I_{OFF} ratios of 1X inverter, 1X NAND and 3X inverter are 2.93, 3.95, and 14.5, respectively. This type of error may cause 1X inverter stuck-at-0 and disable 1byte SRAM cell row selection "RS" (Fig. 3.6) and the SRAM may read out random data.

Type b: disabled output of row global decoder stage 1. Fig. 4.6 shows the stage 1 and stage 2 of the row global decoder. The stage 1 is a small 4-to-16 decoder. As discussed above, an NMOS of 1.4um length is used in the decoder. If the 1X inverter or the 9X inverter of the stage 1 suffer a stuck-at '0', this disables the row global decoder stage 1 and as a result 1/16 of decoder outputs will fail; this will cause 1/16 of all memory locations read out incorrectly. A 1X inverter is more likely to fail due to its reduced area and greater cell variability compared with the 3X inverter or the 9X; the worst case I_{ON}/I_{OFF} ratios of the 1X, 3X and 9X are 2.93, 14.5, and 25.3, respectively, as noted from Table 2.4.

Type c: disabled output of global row decoder stage 2. As in Fig. 4.6, this type error may be caused by 1X inverter and 9X inverter stuck-at-0, respectively, and results in stuck-at-0 for the output of the row decoder.

Type d: precharge circuit short. As in Fig. 3.11, the precharge circuit short may cause an SRAM COL-COL_BAR short and result in memory stuck-at '1' or '0' for a whole column.

Type e: minimum SRAM column delay. As discussed in CHAPTER III, the minimum SRAM column delay is required to generate the minimum SRAM column delta (ΔV_{SA}). If the minimum SRAM column delay is not sufficient, the whole column of data is decided by sense amp V_{OS} and results in stuck-at '1' or '0' at whole column.

Table 4.2
SRAM testing error classification for 2008

	SRAM category	SRAM sub-category	Error source
Cell errors	Adjacent to each other	2 bytes 101010101 flipped to 01010101 at adjacent column locations= 1 die 8bits or 1 byte location errors =3 die 24 bytes 10101010 flipped to 0101010 at adjacent column locations = 1 die	Error source B Error source C Type a
		Stuck-at '1' or '0' 2-cell errors=3 die 3-cell errors=1 die 4-cell errors=1 die	Error source B
	Non-adjacent	None	N/A
	Single error	Stuck-at '1' or '0' = 4 die	Error source B
Row errors	Adjacent row	2 adjacent row location error =1 die	Error source B Type c
	Non-adjacent row	none	N/A
Column errors	Adjacent column	none	N/A
	Non-adjacent column	Stuck-at '1' or '0' 1-clumn-error die=32 die 2-column-error die=9 die 3-column-error die=1 die	Error source A Error source B Type d Type e

With the error sources and the error locations defined above, Table 4.2 provides the detailed classification of the SRAM testing. The SRAM cell errors are identified as adjacent cell errors, non-adjacent cell errors, and single-cell error. Table 4.2 shows the adjacent cell errors; one die was found with 10101010 to 01010101 pattern flip for 2 adjacent byte locations. Three die were found with an incorrect pattern at a single byte location. The patterns are 10101010(correct) -> 00000000(incorrect), 01010101(correct) -> 11111111(incorrect), and 10101010(correct) -> 01010101(incorrect). The 2-bytes adjacent location error and 1-byte location error may have the same error source, the silicon defeat (Error source B) on 1 or 2 local decoder buffers. Fig. 4.4

shows the local decoder buffer, and the NMOS transistors in the 2 adjacent locations which mean NMOS are next to each other and share the same GND. A silicon defect may cause low V_{TH} for the adjacent NMOS and as a result the NMOS transistors suffer stuck-at '0'. The reason for pattern 10101010->00000000, 01010101-> 11111111, and 10101010-> 01010101 is unknown; the expected error read should be random data where read decisions are made by sense amp Vos. As in Table 4.2, 1 die was found 10101010 flipped to 01010101 for 24 bytes adjacent locations; this is the unknown errors (Error source C).

As in Table 4.2, four die had single-cell error, three die had 2-cell-errors, one die had 3-cell-errors, and one die had 4-cell-errors; all these errors are found at adjacent or single locations, and may be caused by Error source B, the silicon defect. Single-cell errors along with 2-to-4-cell errors are stuck-at-1 and stuck-at-0 approximately 50%, and 50%, respectively. As in Table 4.1, there are 88 partially working and fully working die. The probability of 1-cell-error die out of 88 die is 4.4%. Based on this, the probability of 2-cell-errors die out of partially functional die should be 0.2% if the cell errors are independent from each other; but this is not consistent with the tested die. All these 2-to-4 cell errors are adjacent to each other, which strongly suggest the cell errors are correlated to a silicon defect; also there are no non-adjacent cell errors observed, as in Table 4.2. This result further proves 1-to-4 cell errors are due to the silicon defect.

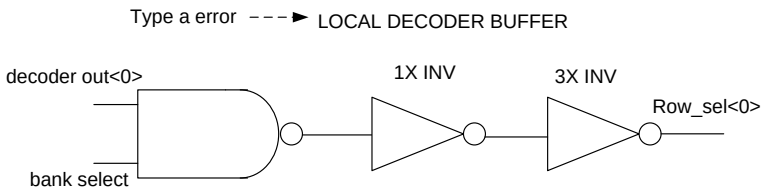


Fig. 4.4 Local decoder buffer.

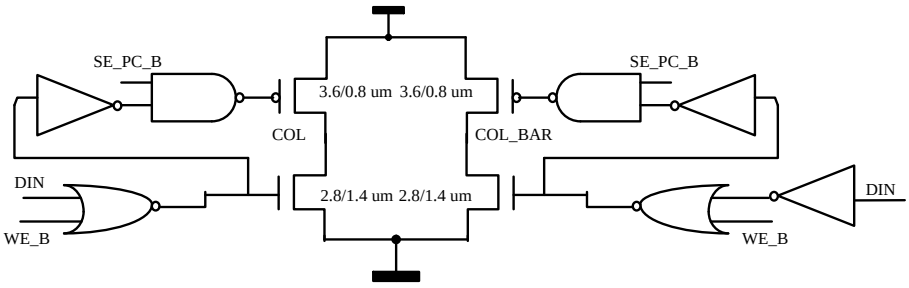


Fig. 4.5 SRAM write circuitry.

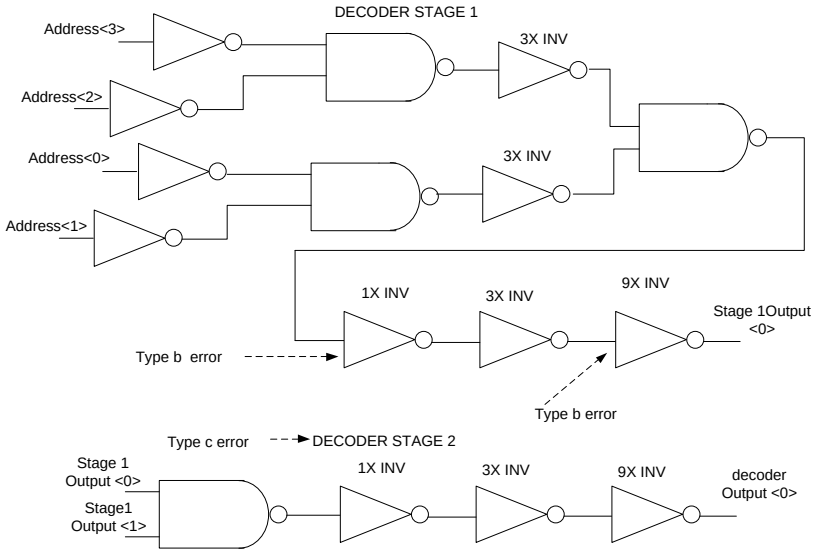


Fig. 4.6 Main decoding path of global row decoder.

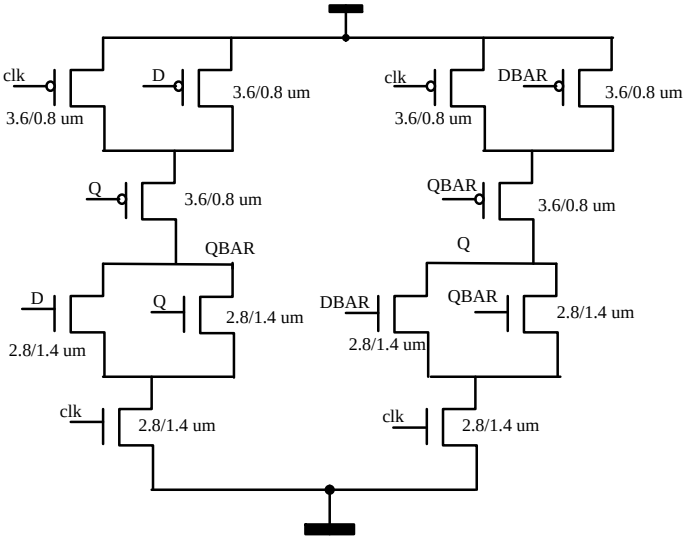


Fig. 4.7 SRAM/ROM latch for column read.

Table 4.2 shows 1 die has row errors. These errors occur at disabled output of global row decoder stage 2 (Type c) and may be caused by Error source B, the silicon defect as well. As in Fig. 4.6, the silicon defect may cause 2 adjacent NMOS stuck-at-0 and these 2 adjacent NMOS may disable the 2 row of global row decoder stage 2. As a result, the whole row reads out error data.

Table 4.2 shows the column errors which are categorized as adjacent location die and non-adjacent location die. The numbers of die are 0 and 42, for adjacent location die and non-adjacent location die, respectively. Of the 42 die with column errors, 32 die have 1-column error, 9 die have 2-column errors, and 1 die have 3-column errors. The stuck-at '1' and '0' are approximately 50% and 50%, respectively. Out of 88 die, there are 32 1-column-error die and the probability of 1-column-error die is 36.4%; based on the calculation, the probabilities of 2-column-error die and 3-column-error die are 13.2% and 4.8%, respectively, under the condition that column errors are independent from each other. The probabilities of 1-column-error die, 2-column-errors die, and 3-column-errors die are 36.4%, 10.2% and 1.1%, respectively, which is considered consistent with the calculation.

The minimum SRAM column delay (Type e) may be a cause of column error, but does not appear likely. The minimum SRAM column delay and sense amp designs are correct using Spectre simulations; the sense amp is designed with large geometry transistors with a monte carlo simulation and 1-sigma V_{OS} equals 1.71mV; the minimum SRAM column delay designed is sufficient enough to overcome a 6-sigma sense amp offset. However, it is worth noting that the present of a silicon defect may strongly alter this behavior.

A hypothesis can be made; row errors and column errors are only caused by Metal1 and Metal2 shorts (spot defects); Metal1 run mostly horizontal and Metal2 run mostly vertically; The total Metal1 and Metal2 runs are 0.45mm^2 and 0.86 mm^2, respectively [55]; this suggest error probability ratio of Metal1 vs. Metal2 shorts is expected to be greater than 1:1.9. However, the

tested die show the row errors and column errors are 0.8% and 34.7%, respectively. This clearly suggests Metal1 shorts are most likely not the problem. As a result, it is suggested that Metal2 shorts may be occurring in the SRAM columns.

Another hypothesis can be made, row errors, cell errors and column errors are only caused by the silicon defect and/or strong (leaky NMOS) transistors. Fig. 4.2 shows the SRAM column logic which includes: write circuitry, sense amp with precharge, latch, and tri-state buffer. All column logic circuits use NMOS 1.4um. Fig. 4.5 shows the SRAM write circuitry and the NMOS devices connected to the columns may cause a stuck-at-0 as well; fig. 4.7 shows the latch and may also have the stuck-at faults; the sense amp and precharge circuit may suffer stuck-at '0', respectively, due to the excessive thick silicon. The worst case I_{ON}/I_{OFF} ratios of the write circuitry, latch, and tri-state buffer are 5.12, 3.95, and 7.39, respectively. The total silicon defects from row errors and cell errors are 15 out of 88 die; the total row layout area and SRAM array area are 5.78mm^2; so the defect rate is 0.0295/mm^2. Column logic has 40.0mm^2 out of 88 die; so the column defect is only 1 out of 88 die. This suggests silicon defect is not the dominant error of the column errors. As a result, Metal2 shorts may be the main error source of SRAM column errors. As shown in Fig. 4.3, Metal2 shorts may occur for 6T SRAM cell. Column logic may also have the Metal2 shorts, which include write circuitry, sense amp with precharge, latch and tri-state buffer. Precharge circuit shorts (Type d) may occur. Monte carlo simulations demonstrate when both COL and COL_BAR are at VDD/2 and shorted, sense amp with latch settles in 2.73ns±30ps, which is much less than SRAM read delay time of 80ns; so the precharge circuit shorts may result in whole column stuck-at '1' or '0'. Metal2 shorts are observed for 2K ROM and discussed in Section 4.3.

The cell errors, row errors and column errors are observed for 4K SPI SRAM. It is interesting to observe there is only 1 row error observed out of 88 die so the row-error rate is only 0.004%; furthermore, the observed row-error die has adjacent row errors so this is probably not open wires

or missing contacts; the global row decoder and local decoder buffers are both laid out using ≥2 contacts at each node, and the same metal widths. As discussed above, Metal1 shorts are most likely not the problem. As results, both global row decoder and local decoder buffers are not likely to have spot defects, but more likely have silicon defect. The adjacent SRAM cell errors are observed which are not likely the spot defects as well as the row errors. As a result, SRAM cell is less likely to have spot defects, but more likely to have silicon defects. In conclusion, the cell errors are believed to be mainly caused by the silicon defect in the memory cells, and cell byte errors are a result of the silicon defect in the local decoder buffers; column errors are believed mainly to be caused by Metal2 shorts; row errors again are caused by the silicon defect in the row global decoder. A comparison of SRAM and ROM errors are discussed in Section 4.2.

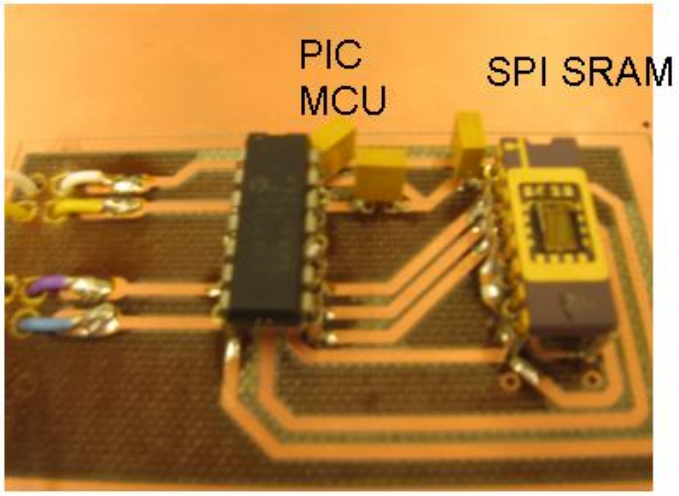


Fig. 4.8 PIC and SRAM chips on PCB.

4.2.4 SRAM Testing on PCB

Fig.4.8 shows the testing set up of the PIC and SRAM chips on PCB. The code residing in the PIC is to present a GUI, to allow the user to type command to trigger the PIC to write and read to/from SPI-SRAM up to 512 bytes. When command ‘S’ is entered, the PIC will get a byte of data from its on-chip EEPROM and then write a byte to SPI-SRAM starting at address 0000h.

After writing a byte, the PIC will read back a byte from SPI-SRAM and echo the data byte to the HyperTerminal window. As shown in Fig. 4.9, the testing is to write a byte and read back a byte to/from SPI SRAM. The output byte from SPI SRAM will be read by PIC via SPI interface.

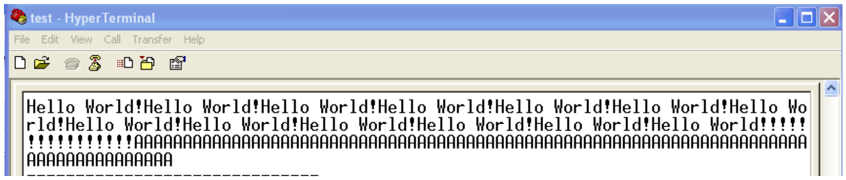


Fig. 4.9 HyperTerminal output for PIC.

4.3 ROM Testing

4.3.1 ROM Testing Condition

The 2K SPI-ROMs were fabricated on Peregrine 0.5um SOS process in 2007 and 2008, respectively. The total area of 2K SPI-ROMs in 2008 is 5.0mm^2. The 2K SPI-ROM passes the frequency, temperature and voltage corners of 2MHz, 4MHz and 8MHz and 27 ℃, 200 ℃, 275 ℃, and 295 ℃, and 2.5V, 3V, 3.3V, and 3.6V, respectively (alessi rel 6100). The ROM cell structure is shown in Fig. 3.12. The test consisted of confirming the customer code or modified version 68MON monitor code by using the Tektronix TLA 720 logic analyzer to capture the output data, and then compared it with the original memory file used to form the ROM contents by running an automatic Matlab testbench. The settings of the Tektronix TLA 720 instrument are the same as SPI-SRAM testing.

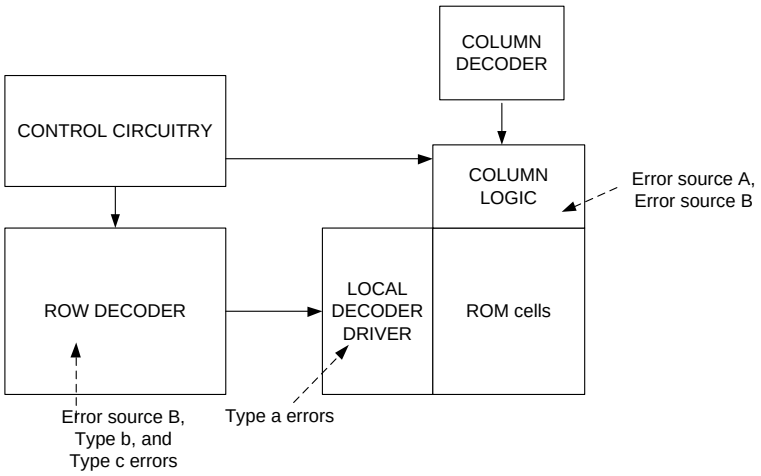


Fig. 4.10 ROM structure with error sources.

Table 4.3
2K ROM testing error die of 2008 and 2007

	2K ROM in 2008	The distribution of 2K ROM in 2008	2K ROM in 2007	The distribution of 2K ROM in 2007
Fully working die	53	71.6%	31	44.9%
Partially working die	15	20.3%	29	42.0%
Cell errors	4	5.4%	12	17.3%
Row errors	5	6.8%	4	5.8%
Column errors	6	8.1%	13	18.8%
Shorted-circuit die	6	8.1%	9	13.0%
Full working and partially working die	67	90.5%	60	87.0%
Total	74	100%	69	100%

4.3.2 ROM Testing Analysis

As in Fig. 4.1, the ROM has 3 types of common errors: row, cell, and column errors. Table 4.3 show the comparison of the SPI 2K-ROM testing results in 2008 with the results in 2007. In 2007 and 2008, 44.9% and 71.6% of the die read out successfully, respectively. The yield improvement is 59.5%. In 2007 and 2008, 5.4% and 17.3% of the die had cell errors, respectively. The cell errors reduced 53.1% from 2007 to 2008. This is believed due to the 2008 ROM cell having a

larger cell pull-up transistor by 90.5%; also the number of PMOS gate contacts was increased from 1 to 2, compared with the 2007 ROM. In 2008 and 2007, 8.1% and 18.8% of the die had column errors, respectively. The column errors reduced 53.1% from 2007 to 2008. In 2008 and 2007, 6.8% and 5.8% of the die had row errors, respectively. In 2008 and 2007, 8.1% and 13.0% of the die were shorted, respectively.

Table 4.4
ROM testing error classification for 2008

	ROM	ROM Notes	Error source
Cell errors	Adjacent cells =2 die	4-cell-errors = 1 die 6-cell-errors = 1 die	Error Source B Type a
	Non-adjacent cells	0	NA
	Single error=2 die	Single error = 2 die	Error Source B
Row errors	Adjacent row	2 adjacent row location die = 2 die single row location die = 1 die	Error Source B Type c
	Non-adjacent row	128 bytes out of 2048 bytes = 2 die	Error Source B Type b
Column errors	Adjacent column Die=2	2-column-error die= 2 die	Error Source C
	Non-adjacent column =4	1-column-error= 4 die	Error Source B Error Source A

4.3.3 ROM Testing Diagnosis

Table 4.4 shows common errors including cell, row, and column errors. The error classification of ROM is shown in Table 4.4 and specified Fig. 4.10. Cell errors are categorized as the adjacent-cell errors, single-cell errors, and non-adjacent cell errors. For the adjacent-cell errors, one die had 4-cell-errors in adjacent locations; one die had 6-cell-errors in adjacent locations; this may be local decoder buffer (Type a) errors. Two die had single-cell error; single-cell error may be Type a errors as well. ROM testing is to read first address to last address by orders; these error data is

found the same as the adjacent location data. This indicates the error bytes are not selected during a read and ROM reads the previously stored information from the ROM columns. This is believed to be the local decoder buffer error, and similar to the SRAM, SRAM has 1-byte cell errors which are caused by local decoder buffer as well. As a result, no ROM cell is observed as the cell errors.

Table 4.4 also shows the row errors. The row errors are categorized as adjacent and non-adjacent errors; two die had row errors at 2 adjacent row locations; one die had row errors at a single row location. This is disabled output of global row decoder stage 2 (Type c) errors and may be caused by Error source B, the silicon defect. As in Fig. 4.6, the silicon defect may cause single or 2-adjacent NMOS stuck-at-0 and these single or 2-adjacent NMOS may disable the single or 2 rows of global row decoder stage 2. As a result, the whole row reads out error data. The Type c errors are observed in both SRAM and ROM. As in Table 4.4, 2 die had non-adjacent errors; they had 128-bytes errors out of 2K bytes ROM. It is disabled output of global row decoder stage 1 (Type b) errors because the observed errors are occurred at all ROM columns and at the same row addresses of 6, 22, 38 …246 for each column; the expected error rows have to be 16 addresses separated to each other, which is the same as the observed; as in Fig 4.6, if a single output of global row decoder stage 1 has a disable error, $1/16^{th}$ of the ROM bytes are not able to select and not able to read out correctly. It is believed these errors are only caused by row global decoder stage 1 error.

As discussed above, the cell errors and row errors are caused only by the global row decoder and the local decoder buffers; more specifically the silicon defect. There are 9 defects observed out of 67 die which include the fully working and partially working die. The total area of row global decoder and local decoder buffers are 59.0 mm^2 out of 67 die; the silicon defect rate is 0.15 defect/mm^2. Furthermore, no silicon defects are found in the PMOS ROM cells. This is because PMOS threshold variations are much smaller compared with NMOS, as discussed in Error source B.

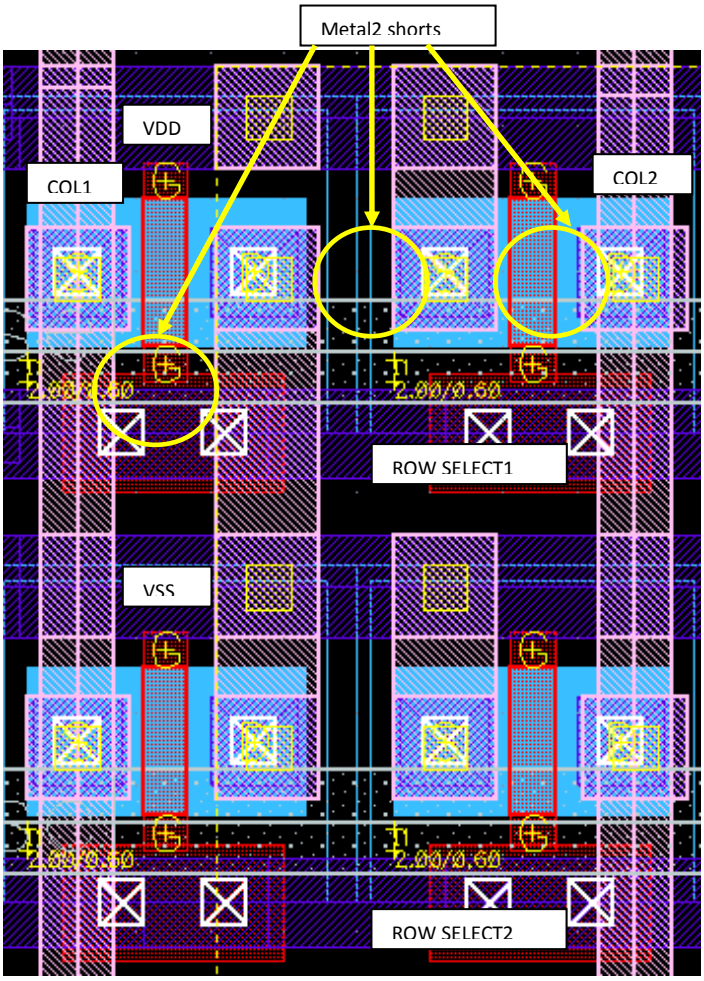


Fig. 4.11 ROM cell layout in 2008 with possible shorts.

No spot defect (Error source a) are found for the 2K ROM cells in the 67 die. This most likely because 2 contacts are used in the ROM cell gate, PMOS drive strength increases 90.5%, and Metal1 width for the ROM cell is 1.6 times the minimum Metal1 width. This indicates no cell errors are caused by Metal1 shorts, missing contacts or broken wires. Both 6T SRAM and ROM run Metal1 horizontally using the same widths, and only 1 PMOS drain/source contact is used for both. This further proves that SRAM cells are not likely caused by spot defects such as Metal1 shorts, missing contact or broken wires.

Four die had non-adjacent 1-column errors, as in Table 4.4. The error die are stuck-at ‘1’ or ‘0’ for approximately 50% and 50%, respectively. Four 1-column-error die are found out of 67 die,

so the probability of 1-column-error die is 6.0%. This may be caused by Error source A and/or Error source B. Two die had adjacent 2-column errors; the error die suffer stuck-at '1' or '0' for 50:50, respectively. If the 2-column errors are independent errors, the 2-column-error die out of fully and partially working die should be 0.06 squared, or 0.3%, which is not consistent with the tested die. However, the 2-column errors are adjacent column locations; this suggests the correlated errors; ROM adjacent columns are 1.4um apart which are the duplicates of the columns shown in Fig. 4.11; as a result adjacent column shorts may be the cause for 2-column errors.

Another cause of column error may be the silicon defect, but this does not appear likely. As shown in Fig. 4.10, the tri-state buffer uses 1.4um NMOS and may be caused by the silicon defect. The 1X NAND and 1X inverter used have 1.6um and have >500 I_{ON}/I_{OFF} ratio. The silicon defect rate is 0.15/mm^2 and the total tri-state buffer layout area out of 67 die is 1.29mm^2; so ≤1 column error die is believed to be caused by the silicon defect. Similar to 4K SRAM, Metal2 shorts (Error source A) may be occurring at ROM columns as well.

Fig. 4.7 and Fig. 4.12 show the difference of 2008 and 2007 ROM column logic. The 1X NAND and 1X inverter used in 2008 has NMOS of 1.6um length and the I_{ON}/I_{OFF} ratios of 500 are assured; the latch used in 2007 ROM has NMOS of 1.4um length, and the I_{ON}/I_{OFF} ratio is <4; this may cause the column errors. In 2007, the total column logic layout area out of 60 die is 3.47mm^2. As a result ≤1 column error die is believed to be caused by the silicon defect, and the reason for reduced column errors from 2007 to 2008 is unknown.

In conclusion, PMOS ROM cell has no spot defects observed; this suggests ROM and 6T SRAM are not likely to have Metal1 shorts, missing contact or broken wires. Both SRAM and ROM row errors and cell errors are mainly caused by the silicon defects and/or strong (leaky NMOS) transistors. Both SRAM and ROM column errors are believed to be mainly caused by Metal2 shorts.

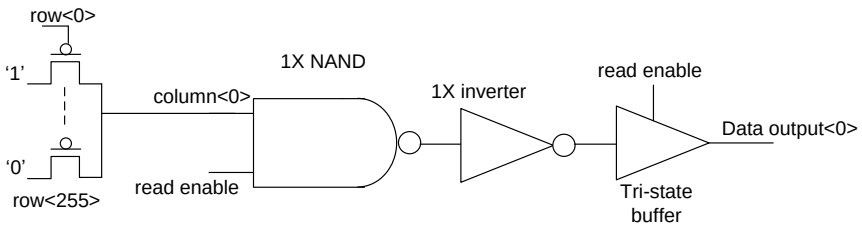


Fig. 4.12 ROM read circuitry in 2008 design.

4.4 Cache Testing

128 x 32 and 32 x32 caches were used as the on-chip caches for 200 ℃ LEON3 and were fabricated in 2007. The total cache area is 2.74mm^2. The 8T SRAM cell structure is shown in Fig. 3.13. A test fixture was built to verify the functionality of the LEON3, where the heater was placed in direct contact with the top of the ceramic package for high temperature testing from room to 200 °C. The GRMON debug monitor software [54] was then used to communicate with the LEON3 via JTAG. GRMON tests and debugs LEON3 by downloading and executing of LEON3 applications. Both the LEON3 and caches were tested by writing and reading all caches. An external EEPROM with the user application code was read via GPIO port and hexadecimal strings were in turn written to the terminal window via RS232 connected to the LEON3. The LEON3 IC successfully fetches the user code from EEPROM at boot up, uses a GRMON "run" or "go" to start execution of a system self-test and finished the terminal test demonstration program. The GRMON stored in an off-chip EEPROM was provided by Jiri Gaisler [33]. The successful completion of the test routine proved the successful fabrication of the 200 ℃ LEON3. The LEON3 achieved functional design across corners; temperature - 27 ℃, 80 ℃, 150 ℃, and 200 ℃, frequency -1MHz, 4MHz, 8MHz, 16MHz, and 18MHz and voltage of - 3.0V, 3.3V, and 3.6V. Fig. 4.13 shows the Percentage Distribution of Testing 39 LEON3 die. Of the 39 tested LEON3 die, 10% are fully functional, 13% are short-circuit die, 23% have a register or hardware failure, and 54% have cache errors. Short circuit die were again observed, the same as 4K SPI-SRAMs; cache errors including cell errors and column errors were observed during reading the

caches. The testing results show the cache errors may be influenced by shorted metals, physical defect, and strong (leaky NMOS) transistors. Similar to the 6T SRAM errors, NMOS devices with 1um length are used as the cells and digital logic which can cause cell errors, row errors and column errors.

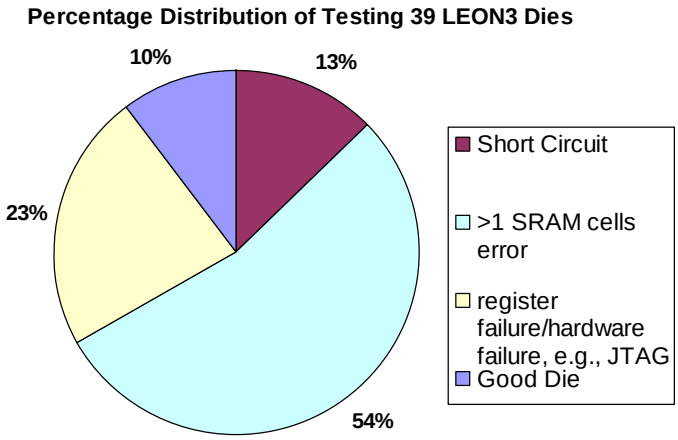


Fig. 4.13 Percentage Distribution of Testing 39 LEON3 Die.

As discussed in Section 4.3, both 4K SRAM and 2K ROM column errors are mainly caused by Metal2 shorts. One possible hypothesis can be made, Metal2 shorts may result in a short-circuit die in each of the ROM, SRAM, and LEON3 cache, as shown in Table 4.5. In ROM, SRAM and LEON3 cache layouts, Metal2 VDD and VSS are next to each other, respectively. If column and shorted-circuit are both the short errors, the probability of occurrence is proportional to the length of Metal2 at the same separation [55]. The tested 4K SRAM column errors vs. shorted-circuits are 1.27:1; the total length of column shorts vs. VDD-to-VSS shorts is 1.6:1. The tested 2K ROM column errors vs. shorted-circuits are 1:1; the total length of column shorts vs. VDD-to-VSS shorts is 1.8:1. These suggest SRAM/ROM column errors and shorted-circuits may have similar causes of error which is Metal2 shorts.

The tested ROM, SRAM, LEON3, and HC11 have 8.1%, 27.3%, 13%, 33% shorted-circuits,

respectively; the shorted-circuit probability of ROM, LEON3 cache, LEON3, HC11 normalized to SRAM are 0.30, <0.48, 0.48 and 1.21, respectively, as shown in Table 4.5. If shorted-circuit is only proportional to the layout area, ROM, LEON3 caches, LEON3, and HC11 normalized to SRAM are 0.29, 0.17, 3.78 and 2.56, respectively. LEON3 has 2.78 times larger area but only 48% shorts of the SRAM; this suggests shorted-circuit appears to strongly correlate with memory layout and more specifically Metal2 shorts.

Table 4.5
Possible shorted-circuit summery

	4K SPI-SRAM	2K SPI-ROM	LEON3 caches	LEON3 [9]	HC11 [9]
Shorted-circuit percentage	27.3%	8.1%	<13%	13%	33%
area	16.5mm^2	5.0mm^2	2.74mm^2	62.4mm^2	42.25mm^2
Shorted-circuit /unit area	1	0.30	0.17	3.78	2.56
Total M2 run	480mm	80mm	182mm	>182mm	>480mm
Shorted-circuit /unit length	1	0.17	0.38	>1	>1

Assuming the Metal2 is the only cause of shorted-circuit or VDD-VSS shorts. As shown in Table 4.5, the total lengths of Metal2 for SRAM, ROM and LEON3 cache are 431mm, 112mm, and 146mm, respectively. The Metal2 separations for SRAM, ROM and LEON3 cache are 0.9um, 1.4 um and 0.8um, respectively. The probability of a fault is caused by the separation distance and the total length of the metals [55]; as a result shorted-circuit probabilities of ROM, LEON3 cache normalized to SRAM are 0.17 and 0.38, respectively. Based on the tested die, the shorted-circuit probabilities of ROM, LEON3 cache normalized to SRAM are 0.30 and <0.48, respectively. These suggest memory shorts are correlated to Metal2 column shorts. In conclusion, the shorted-

circuit is believed to be mainly the Metal2 shorts in the memory cells and column logic.

4.5 Testing Summary

The 4K SPI-SRAM testing and 2K SPI-ROM confirmed operations across room to 295 ℃, making the memories suitable for 275 ℃ HC11 design. The HC11 testing proved 4K on-chip SRAM and 512byte on-chip ROM were functional [9] across room to 295 ℃. The LEON3 testing confirmed operations across room to 200 ℃ including 128 x 32 cache and 32 x 32 cache. The 2K x 16 off-chip SRAM is identical to 4K SPI-SRAM and is proved suitable for LEON3 design.

The cell errors, column errors, and shorted-circuit die are the most common errors for the 3 different memory cell structures including 6T SRAM, ROM and cache. Both SRAM and ROM row errors and cell errors are believed to be mainly caused by the silicon defects and/or strong (leaky NMOS) transistors. SRAM and ROM column errors are believed to be mainly caused by Metal2 shorts. Shorted-circuits of 6T SRAM, ROM and cache are believed to be mainly caused by Metal2 shorts as well. Row errors and cell errors can be reduced by fixing digital logic design and memory cell design, as discussed in CHAPTER III. Column errors and shorted-circuit may be reduced by increasing the separation of Metal2. However, the silicon defect and Metal2 shorts are the process limitation and as a result memory design on Peregrine 0.5um SOS process is not suitable for large memories. The memory design using this process is suitable for <4K bytes memory and for small production designs.

CHAPTER V

MEMORY DESIGN WITH ENCOUNTER SUPPORT

5.1 Introduction

The increase of performance in microprocessors and digital signal processors requires high-speed and high-density memories. When considering efficiency, it is not practical to design different memories from scratch for every unique application. From 1986, several groups have designed memory compilers to achieve handling different memory designs and migrating memories between technology kits [36]-[39]. The fastest reported memory development is 1 week [36]. This work uses memory layout with Encounter support to achieve handling different memory designs using Peregrine 0.5 um SOS process. Compared with the other memory compilers, this work spends more time (6 weeks), but this work is specialized for Peregrine SOS 0.5um technology and is a lower cost solution. This time is expected to shorten with experience.

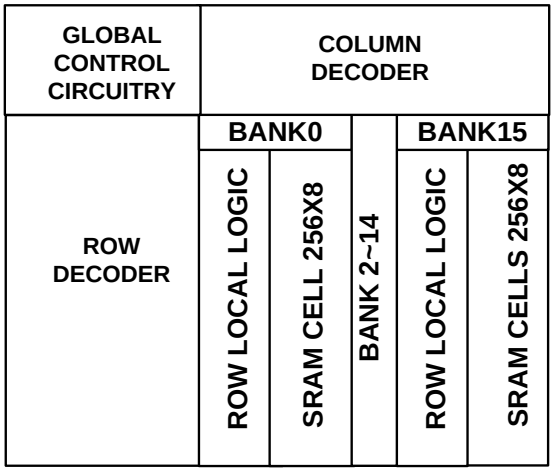


Fig. 5.1 Basic SRAM structure.

5.2 Memory Design with Encounter Support

Figure 5.1 shows the SRAM basic structure which includes global control circuitry, column decoder, row decoder, and SRAM bank. The SRAM bank includes SRAM cells, sense amps and local logic.

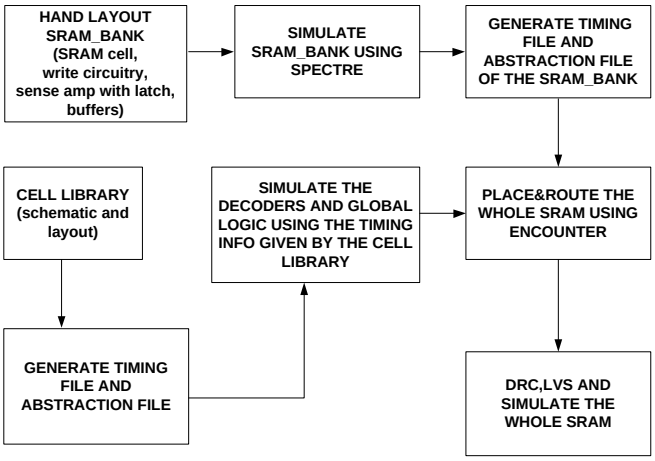


Fig 5.2 SRAM design with Encounter support.

The cell library is predesigned as discussed in CHAPTER III. The global control circuitry, column decoder and row decoder can be implemented using Verilog or VHDL and characterized using the cell libraries. The SRAM bank is also designed as discussed in CHAPTER III; after the "SRAM_BANK" schematic, layout and Spectre simulation finished, timing file of the SRAM bank is generated by filing out the timing information using the same format as the cell library timing; abstraction file is generated using Cadence Abstraction tool. Using Encounter the abstracted SRAM bank cell is placed and routed with all the digital logic ensuring the timing requirements are meet. Fig. 5.2 shows the SRAM design using Encounter place and route design flow, as specified below:

1) Memory cell and memory column are designed, verified across process corners, resulting layout abstracted establishing critical read timings, cell geometries and write drive.

2) SRAM_BANK schematic and layout of a variety dimensions are generated using the verified column from 1) above.
3) SRAM_BANK is simulated using Cadence Spectre. Timing information such as column delay, row delay, and signal delays are found. The loading capacitance of each delay is found as well.
4) Timing file and abstraction file of SRAM_BANK are generated (See Appendix B). The SRAM_BANK timing file is manually filed out with the timing found from 3).
5) The schematic and layout of the cell library are generated.
6) Timing file and abstraction file of the cell library are generated.
7) Decoders and global control circuitry are simulated using Simvision.
8) SRAM_BANK, decoders and global control circuitry are placed and routed using Encounter.
9) The whole SRAM is DRCed and LVSed. Then post-layout simulation is completed for final verification.

The basic steps of Encounter place and route include [58]:

1) Importing Design: import Verilog files, timing libraries, LEF files.
2) Floor planning: decide the chip area, add power net and place the power blocks (Fig.5.3).
3) Power planning: place the power distribution network which includes power pads, power rings, power strips, and power rails forming the power grid.
4) Special route: the block pins are connected, power rings are connected and standard cell pins are generated and connected.
5) Trial route: route the remaining nets of the blocks.

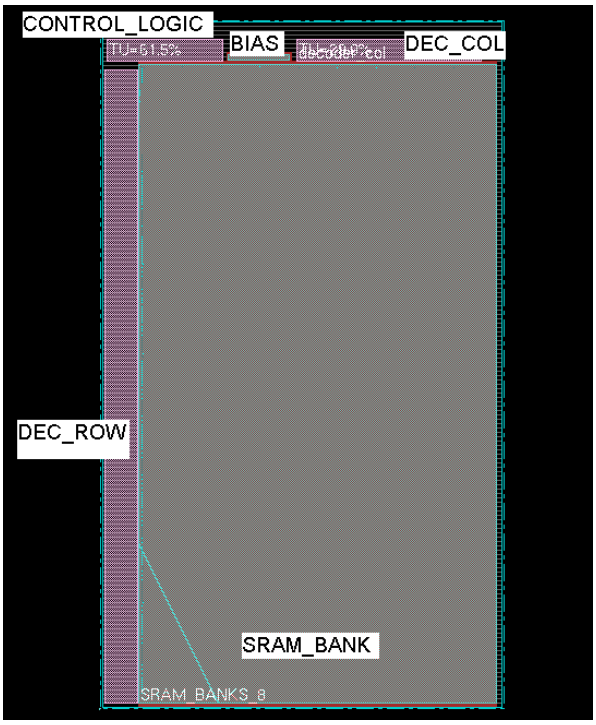


Fig 5.3 Floor plan of the SRAM.

6) Timing analysis: find out if there is timing violations and add buffers/inverters for timing optimization.
7) Clock tree synthesis: add buffers and inverters.
8) Hold Timing Analysis: fix the hold timing violation after Clock Tree Synthesis.
9) Nano-route: global and detail routing to prevent crosstalk. (Fig.5.4).
10) Post-route with timing optimization: optimize the timing by adding buffers/inverters, remapping logic, swapping pins.
11) Fillers insertion: add decoupling capacitance.

Table 5.1 summarizes the comparison of SRAM design with Encounter support and hand-layout SRAM. SRAM design with Encounter Support reuses the previous SRAM design in HC11 or LEON3 and shortens the SRAM design time from 11 weeks to 6 weeks. SRAM layout with Encounter support required less decoder and global logic design time due to simulation time of the tools; automatic place and route typically has only a few errors needed to be cleaned up manually, and layout time is reduced significantly compared with hand layout. Compared with

the memory compilers [36]-[39], SRAM layout with Encounter support requires 50% more design time. However, it is timing consuming to develop a memory compiler which requires developing SKILL script and/or Perl script; these memory compilers are on market and costly. A memory compiler [35] is suitable for technology migration, but there are 2 design problems: the memory compiler uses the same layout area for each standard cells for different design kits, such as inverters, NAND gates, and SRAM cells, but designers desire to compact layout sizes from one design kit to another, especially SRAM cell; there are often very large and unexpected DRC rule changes from one design kit to another. This work is specialized for Peregrine SOS 0.5um technology and SRAM cell was manually laid out to be compact, as discussed in CHAPTER III; also Encounter is an easier tool provided by Cadence so the memory design using Encounter support is a lower cost solution.

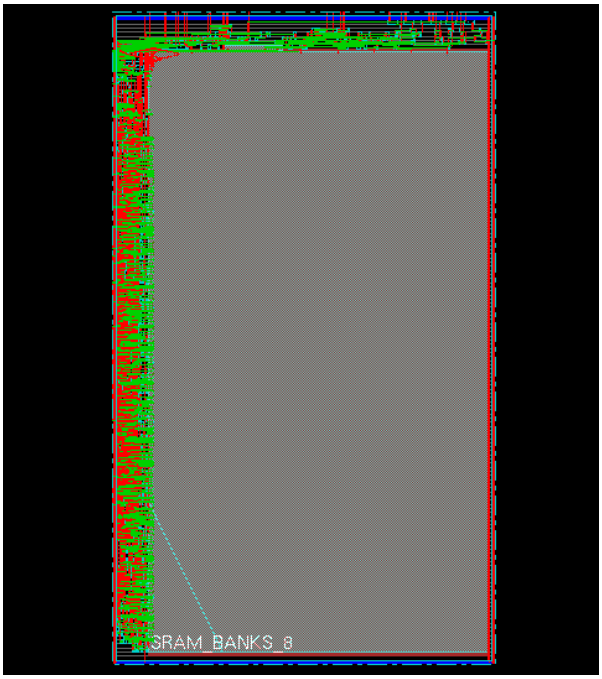


Fig 5.4 Nanorout of the SRAM.

Table 5.1
Comparison of SRAM design with Encounter support and hand-layout SRAM

	Hand-layout SRAM	SRAM layout with Encounter support
area	2.2x3.8 mm^2	2.2x3.8 mm^2
SRAM column including sense amp, write circuitry and SRAM cell	3 weeks (schematic Spectre simulation)	3 weeks (schematic Spectre simulation)
Decoder and global logic	2 weeks (schematic Spectre simulation)	1 week (Verilog Simvision simulation)
Layout	5 weeks (hand layout)	1 weeks (hand layout and Encounter place & route)
Post layout simulation	1 week	1 week
Total design time	11 weeks	6 weeks

CHAPTER VI

CONCLUTIONS

In this dissertation, we have demonstrated the high temperature memories for microprocessor designs using 0.5um Peregrine SOS CMOS technology, which can be useful for aerospace, well logging, solar controllers, automobile and other high temperature environment applications. The designed memories are as part of the design for 275 ℃ HC11 microcontroller and 200 ℃ LEON3 processor. The memories having been designed include: a 4K on-chip SRAM, 512byte on-chip ROM, 4K SPI-SRAM, 2K SPI-ROM , 2K x16 off-chip SRAM, 128 x 32 cache , 32 x 32 cache, and SRAM design with Encounter support. For the HC11, the design simulations are over the -55 ℃ to 295 ℃ range with testing completed over the room to 295 ℃ range. For the LEON3, the design simulations are over the -55 ℃ to 200 ℃ range with testing completed over the room to 200 ℃ range. The 4K SPI-SRAM and 2K SPI-ROM testing confirmed operations across room to 295 ℃, making the memories suitable for 275 ℃ HC11 design. The HC11 testing proved 4K on-chip SRAM and 512byte on-chip ROM were functional. The LEON3 testing confirmed operations across room to 200 ℃ including 128 x 32 cache and 32 x 32 cache. The 2K x 16 off-chip SRAM is identical to 4K SPI-SRAM and is proved suitable for the LEON3 design. With testing analysis, good candidates for error sources of memory failure were found and memory yield can be improved for future memory designs; the memory row errors and cell errors are believed to be mainly caused by the silicon defects and/or strong (leaky NMOS) transistors; the memory column errors are believed to be mainly caused by Metal2 shorts; shorted-circuits of the memories are believed to be mainly caused by Metal2 shorts as well. The row errors and cell errors can be reduced by fixing the leaky NMOS transistor designs. The developed methodologies presented can be useful to the LEON3/HC11 design and supporting memories across process corners. Accurate data of I_{ON} and I_{OFF}, threshold and mobility was developed; which resulted in

high temperature 3.3V cell libraries for the LEON3and HC11, respectively. The memories are designed with aid from the measured data to address write and read stability in the context of floating body effect, kink effect, shrinking I_{ON}/I_{OFF} currents; the LEON3/HC11 is then designed with the standard cell library and characterized memories. Finally, SRAM design with Encounter support proved reducing design time from 11 weeks to 6 weeks, compared with hand-layout SRAM. Compared with other memory compilers, this work has 50% more design time but it is specialized for Peregrine SOS 0.5um technology and is a lower cost solution.

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APPPENDICES

APPPENDICE A

The list of the cells used in the cell library

And2_1	And2_2	And_2_3	And_2_4	Ao21_1	Ao21_2	Ao21_3
Ao21_4	Ao22_1	Ao22_2	Ao22_3	Ao22_4	Ao32_1	Ao32_2
Ao32_3	Ao32_4	Ao33_1	Ao33_2	Ao33_3	Ao33_4	Ao331_1
Ao331_2	Ao331_3	Ao332_1	Ao332_2	Ao332_3	Ao332_4	Ao333_1
Ao333_2	Ao333_3	Ao333_4	Aoi21_1	Aoi21_2	Aoi21_3	Aoi21_4
Aoi22_1	Aoi22_2	Aoi22_3	Aoi22_4	Aoi31_1	Aoi31_2	Aoi31_3
Aoi31_4	Aoi32_1	Aoi32_2	Aoi32_3	Aoi32_4	Aoi33_1	Aoi33_2
aoi33_3	aoi33_4	aoi331_1	aoi331_2	aoi331_3	aoi331_4	aoi332_1
Aoi332_2	Aoi332_3	Aoi332_4	Aoi333_1	Aoi333_2	Aoi333_3	Aoi333_4
Buf_1	Buf_2	Buf_3	Buf_4	Buf_5	Buf_6	Buf_8
Buf_9	Buf_11	Buf_12	Buf_14	Buf_15	Buf_18	Buf_20
Buf_22	Buf_24	Fulladd	Fulladd_4	Halfadd	Halfadd_4	Halfsub
Halfsub_4	Inv_1	Inv_2	Inv_3	Inv_4	Inv_5	Inv_6
Inv_8	Inv_9	Inv_12	Inv_15	Latch_1	Latch_2	Latch_3
Latch_4	Latchn_1	Latchn_2	Latchn_3	Latchn_4	Latchnnr_1	Latchnnr_2
Latchnnr_3	Latchnnr_4	Latchnns_1	Latchnns_2	Latchnns_3	Latchnn_4	Latchnnsnr_1
Latchnnsnr_2	Latchnnsnr_3	Latchnnsnr_4	Latchnr_1	Latchnr_2	Latchnr_3	Latchnr_4
Latchns_1	Latchns_2	Latchns_3	Latchns_4	Latchnsnr_1	Latchnsnr_2	Latchnsnr_3
Latchnsnr_4	Msdff_1	Msdff_2	Msdff_3	Msddf_4	Msdffn_1	Msdffn_2
Msdffn_3	Msdffn_4	Msdffnnr_1	Msdffnnr_2	Msdffnnr_3	Msdffnnr_4	Msdffnnsnr_1
Msdffnnsnr_2	Msdffnnsnr_3	Msdffnnsn_4	Msdffnr_1	Msdffnr_2	Msdffnr_3	Msdffnns_4
Msdffnns_1	Msdffnns_2	Msdffnns_3	Msdffnns_4	Msdffnnsnr_1	Msdffnnsnr_2	Msdffnnsnr_3
Msdffnnsnr_4	Msdffnr_1	Msdffnr_2	Msdffnr_3	Msdffnr_4	Msdffns_1	Msddfns_2
Msddfns_3	Msddfns_4	Msdffnsnr_1	Msdffnsnr_2	Msdffnsnr_3	Msdffnsnr_4	Mux21_1
Mux21_2	Mux21_3	Mux21_4	Mux41_1	Mux41_2	Mux41_3	Mux41_4
Nand2_1	Nand2_2	Nand2_3	Nand2_4	Nand3_1	Nand3_2	Nand3_3
Nand3_4	Nand4_1	Nand4_2	Nand4_3	Nand4_4	Nor2_1	Nor2_2
Nor2_3	Nor2_4	Nor3_1	Nor3_2	Nor3_3	Nor3_4	Nor4_1
Nor4_2	Nor4_3	Nor4_4	Oa21_1	Oa21_2	Oa21_3	Oa21_4
Oa22_1	Oa22_2	Oa22_3	Oa31_1	Oa31_2	Oa31_3	Oa31_4
Oa211_1	Oa211_2	Oa211_3	Oa211_4	Oa221_1	Oa221_2	Oa221_3
Oa221_4	Oa222_1	Oa222_2	Oa222_3	Oa222_4	Oa311_1	Oa311_2
Oa311_3	Oa311_4	Oa321_1	Oai21_1	Oai21_2	Oai21_3	Oai21_4
Oai31_1	Oai31_2	Oai31_3	Oai31_4	Oai31_1	Oai31_2	Oai31_3
Oai31_4	Oai32_1	Oai32_2	Oai32_3	Oai33_3	Oai33_4	Oai211_1
Oai211_2	Oai211_3	Oai211_4	Oai221_1	Oai221_2	Oai221_3	Oai221_4
Oai222_1	Oai222_2	Oai222_3	Oai311_1	Oai311_2	Oai311_3	Oai311_4
Oai321_1	Oai321_2	Oai321_3	Oai321_4	Oai322_1	Oai322_2	Oai322_3
Oai331_1	Oai331_2	Oai331_3	Oai332_1	Oai332_2	Oai332_3	Oai332_4
Oai333_1	Oai333_2	Oai333_3	Oai333_4	Or2_1	Or2_2	Or2_3
Or2_4	Or3_1	Or3_2	Or3_3	Or3_4	Or4_1	Or4_2
Or4_3	Or4_4	Scanmsdff_1	Scanmsdff_2	Scanmsdff_3	Scanmsdff_4	Scanmsdffn_1
Scanmsdffn_2	Scanmsdffn_3	Scanmsdffn_4	Scanmsdffnnsnr_1	Scanmsdffnnsnr_2	Scanmsdffnnsnr_3	Scanmsdffnnsnr_4
Scanmsdffnr_1	Scanmsdffnr_2	Scanmsdffnr_3	Scanmsdffnr_4	Scanmsdffns_1	Scanmsdffns_2	Scanmsdffns_3
Scanmsdffns_4	Scanmsdffnsnr_1	Scanmsdffnsnr_2	Scanmsdffnsnr_3	Scanmsdffnsnr_4		

APPPENDICE B

4K SPI BUS SERIAL SRAM DOCUMENTS

TABLE OF CONTENTS

DOCUMENT Page

1. Description

The SPI serial bus SRAM is 4Kbyte memory device (Fig. 2). The memory is accessed through a simple serial peripheral interface (SPI) compatible serial bus. The SPI is a serial synchronous communication protocol that requires minimum of three wires, which are the SPI clock input (**sck**), data in (**di**) and data out (**do**) bus lines. The device is enabled through the chip select enable pin ($\overline{csn}$).The device is enabled by setting the $\overline{csn}$ low (Fig. 1).

The device has to be reset via reset ($\overline{rst}$) pin, a toggle of low to high transition complete the reset cycle. Since the device does not have an on-chip crystal/clock oscillator, the external clock source is required to supply through clock input line (**mclk**). The device supports two operating modes with cpol = 0, cpha = 0 and cpol = 1 and cpha = 0. The read operation is shown in Fig. 3.The byte write sequence is shown in Fig. 4.The burst write mode is not implemented.

To help in debug, pins **ld**, **ce** and **clk_sram** are used for debugging purpose via an internal scan chain. For receiving every 8-bit, **ld** will be asserted and back to low state. A pulse can be observed at pin **ce** as a toggle of transferring data from SRAM to SPI data buffer. Pin **E_ram** is the clock pulse that is supplied to the SRAM to shift out the data from SRAM to SPI data buffer.

1.1 Features

Max clock 8MHz

3.3V low-power CMOS technology

4K x 8bit organization

Sequential read (Page Read/Burst mode) not supported

Max. read cycle time: 425ns max.

Max. Write cycle time: 375ns max.

Internal read time (4K SRAM): 80 ns

Internal write time (4K SRAM): 76ns

Temperature range supported: -25 ^{o}C to +275 ^{o}C

Table I.
Instruction Set

Instruction Name	**Instruction format**	**Description**
READ	0000 0011	Read data from memory array at the selected address
WRITE	0000 0010	Write data to memory array at the selected address

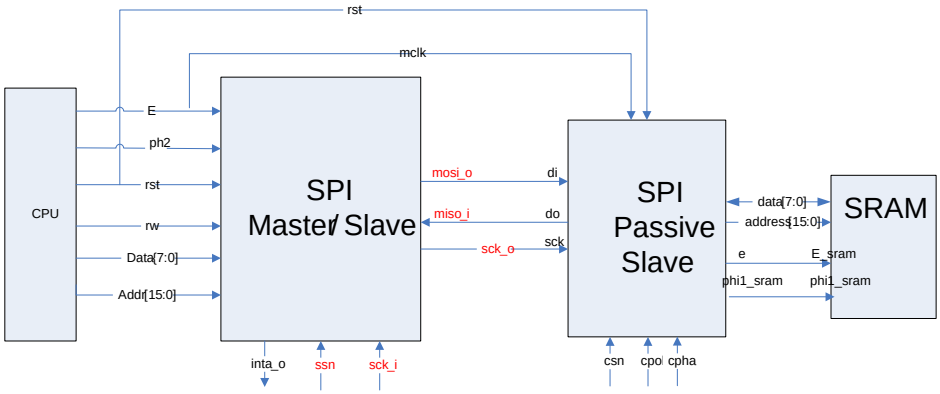

Fig. 1 Master and Slave SPI devices communication diagram.

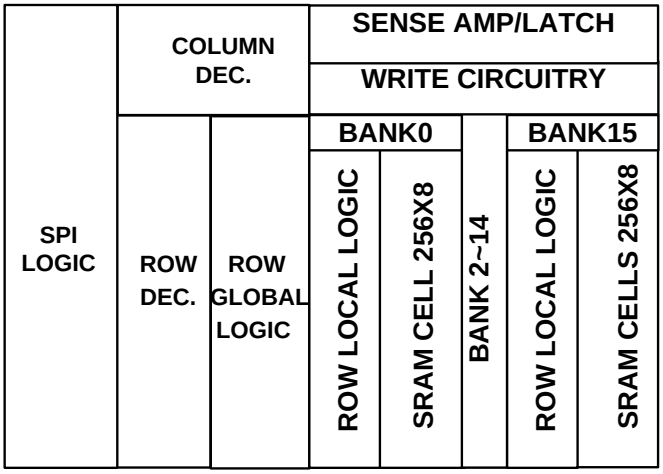

Fig. 2 SRAM architecture diagram.

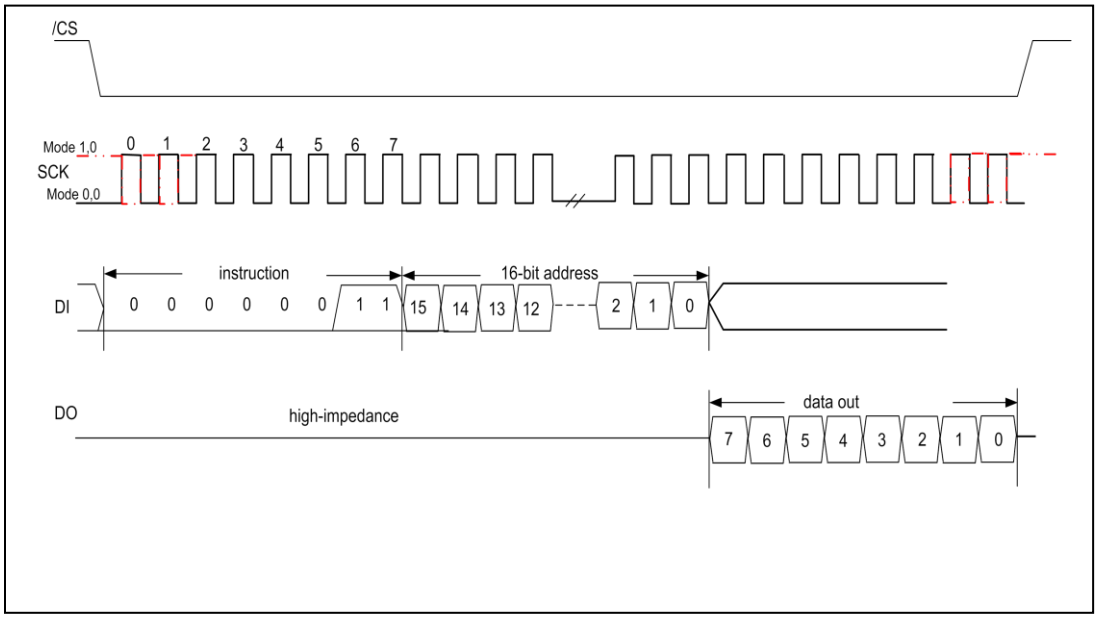

Fig. 3 Serial read sequence timing.

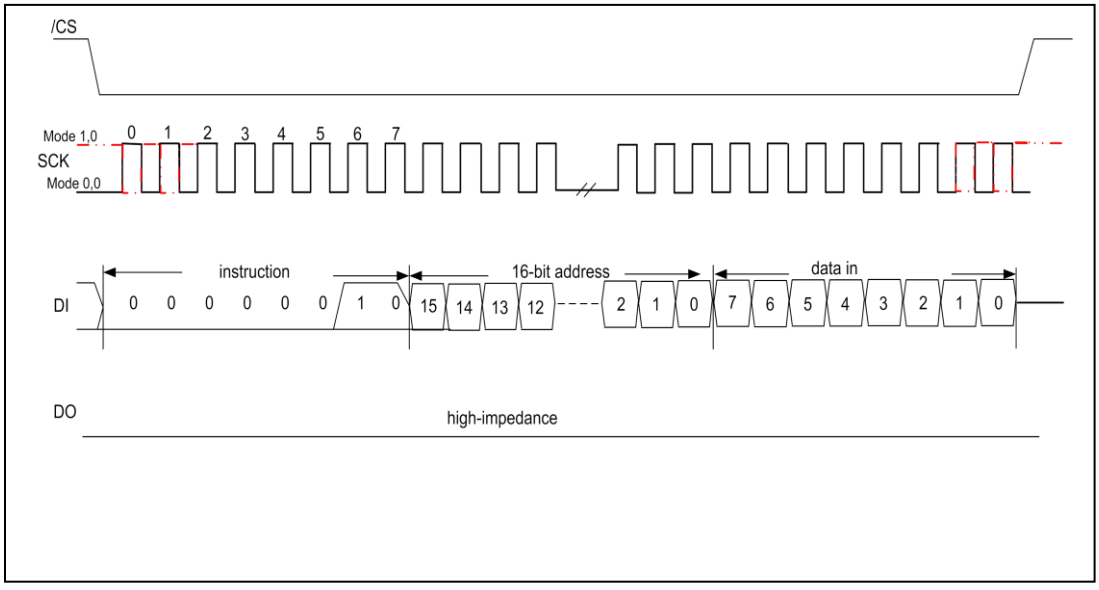

Fig. 4 Serial write sequence timing.

2. Pins

TABLE II
Package pins

Port	Package pin number	Width	Direction	Description
di	1	1	input	Slave data in
sck	2	1	output	SPI input clock (1/8 frequency of mclk)
$\overline{csn}$	3	1	input	Chip select/enable active low
vdd	4	1	input/output	Power digital
vss	5	1	input/output	Power digital
$\overline{rst}$	6	1	input	System reset ,active low reset
cpol	7	1	input	Mode 0 or 1
cpha	8	1	input	Mode 0
vdd	9	1	input /output	Power digital
ctrl_en	10	1	input	Scan chain control enable, must tie to ground to disable scan chain (debugging purpose).
NC	11	1		
NC	12	1		
NC	13	1		
vss	14	1	input/output	Power digital
do	15	1	output	Slave data out
mclk	16	1	input	Main clock

Note: NC= Not connection needed.

TABLE III
SPI Slave and SRAM Circutry Interface Connections

Port	Width	Direction	Description
D	8	input/output	Data input/output
address	16	input	The memory location the CPU wants to write or read
RW	1	input	RW given by SPI
E_sram	1	input	E-clock input
phi1_sram	1	Input	¼ cycle delayed from E
CE	1	input	Read enable signal, active high.
vdd	1	input/output	Power digital
vss	1	input/output	Power digital

3. Layout

SPI SRAM Description:
Total Memory Size: 4K bytes
Number of banks: 16
One bank size: 256 rows by 8 columns
Module area (4K): 16.5mm^2
Switch and standby Power: 9.2mW (at 275 C and 8MHz)
Standby Power: 2.1mW (at 275 C)
Read Access Time : 238ns
Write Access time : 190ns
Decoder Delay : 10ns
Bit Line Delay : 30ns
Useful read time : 80ns
Useful Write time : 76ns

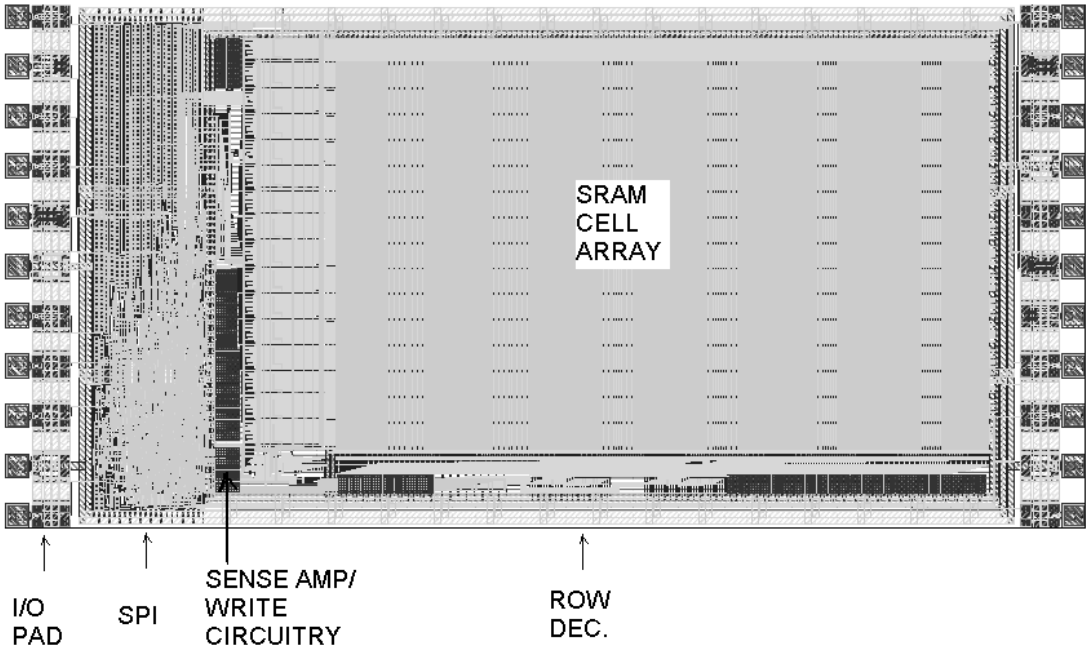

Fig. 5 The layout of 4k SPI SRAM.

4. Testing and Simulation

Simulator: Cadence Spectre

The timing and functional test with parasitic capacitance is tested on the cadence simulation tool.

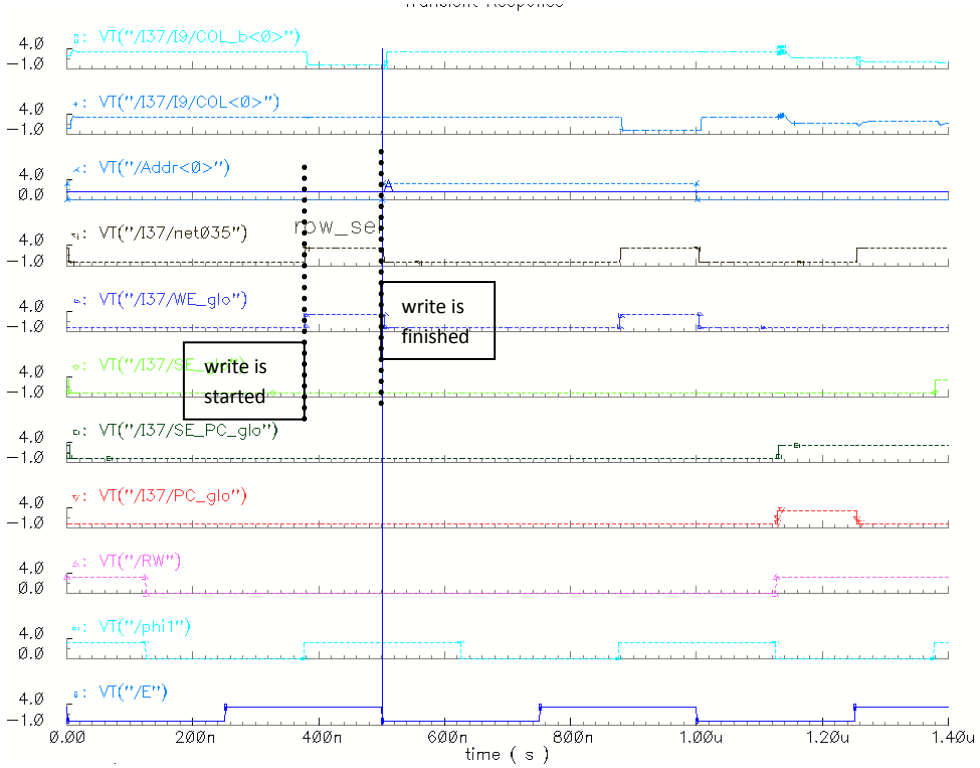

Fig. 6 SRAM internal write cycle.

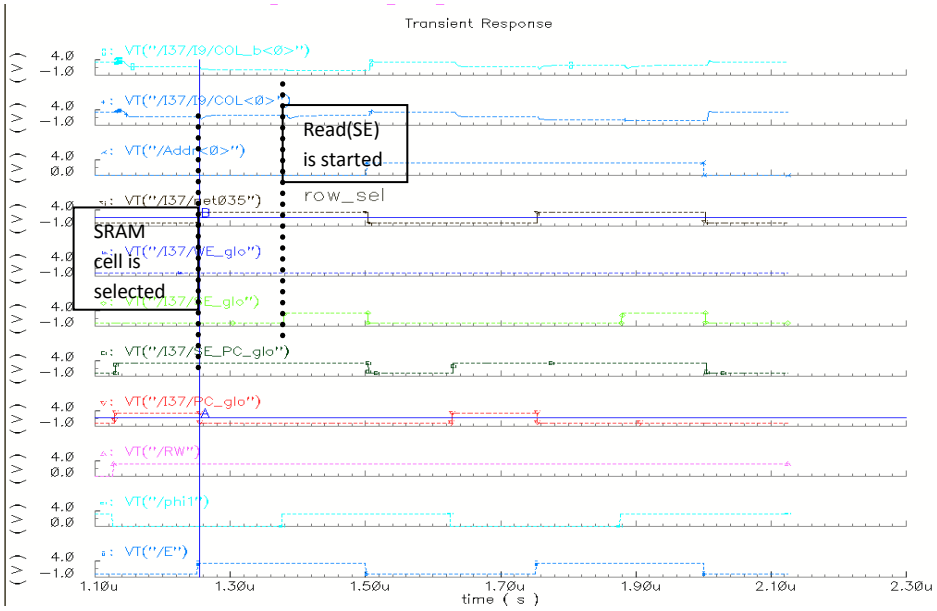

Fig. 7 SRAM internal read cycle.

5. Electrical Characteristics

Maximum Ratings

Vcc…….….3.3V
All input and outputs w.r.t. Vss……..3.3V
Storage temperature…….....-55 ℃ to 275 ℃
Ambient temperature under bias....-55 ℃ to 275 ℃

Table IV

DC Characteristics

T_A = -65 ℃ to 275 ℃ Vcc = 2.0V to 3.3V					
Parameter	Symbol	Min	Max	Units	Test conditions
High level input voltage	V_{IH}	2.0	Vcc+0.7	V	
Low level input voltage	V_{IL}	-0.5	0.8	V	
Low level output voltage	V_{OL}	-	0.4	V	I_{OL} =
High level output voltage	V_{OH}	V_{CC}-0.6	-	V	I_{OH} =
Input leakage current	I_{LI}	-100	100	nA	$\overline{CS}$ = V_{CC}, V_{IN}=GND to V_{CC}
Output leakage current	I_{LO}	-5.4	5.4	uA	$\overline{CS}$ = V_{CC}, V_{OUT}=GND to V_{CC}
Internal capacitance (all inputs and outputs)	C_{INT}	-	0.2	pF	
Operating Current	$I_{CC\ write}$	-	1.58	mA	V_{CC}=3.3V;SO =Open, F_e= 8MHz (Note)
	$I_{CC\ read}$	-	2.00	mA	V_{CC}=3.3V;SO =Open, F_e= 8MHz (Note)
Standby Current	I_{CCS}	-	0.31	mA	$\overline{CS}$ = V_{CC}

Note: This parameter is periodically sampled and not 100% tested.

Table V

AC Characteristics

T_A = -65 ℃ to 275 ℃ Vcc = 2.0V to 3.3V						
Param. No.	Symbol	Parameter	Min	Max	Units	Test conditions
1	F_e	E Clock Frequency	-	8	MHz	$2.0V \leq V_{CC} \leq 3.3V$
2	F_{SCK}	SPI Clock Frequency	-	4	MHz	$2.0V \leq V_{CC} \leq 3.3V$
3	T_{CSS}	$\overline{CS}$ Setup Time	125	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
4	T_{CSH}	$\overline{CS}$ Hold Time	250	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
5	T_{CSD}	$\overline{CS}$ Disable Time	125	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
6	T_{SU}	Data Setup Time	4	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
7	T_{HD}	Data Hold Time	16	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
8	T_R	SCK Clock Rise Time	-	2	µs	(Note)
9	T_F	SCK Clock Fall Time	-	2	µs	(Note)
10	T_{HI}	SCK Clock High Time	0.125	-	µs	$2.0V \leq V_{CC} \leq 3.3V$
11	T_{LO}	SCK Clock Low Time	0.125	-	µs	$2.0V \leq V_{CC} \leq 3.3V$
12	T_{CLD}	SCK Clock Delay Time	62.5	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
13	T_V	Output Valid from SCK Clock Low (mode cpol = 0, cpha = 0) Output Valid from SCK Clock High (mode cpol = 1, cpha = 0)	- -	125 125	ns ns	$2.0V \leq V_{CC} \leq 3.3V$
14	T_{HO}	Output Hold Time	16	-	ns	
15	T_{DIS}	Output Disable Time	-	80	ns	(Note)
16	T_{WC}	Internal Write Cycle Time (byte)	-	½ Te +30	ns	$2.0V \leq V_{CC} \leq 3.3V$

Note: This parameter is periodically sampled and not 100% tested. Refer to Fig. 8 and Fig. 9

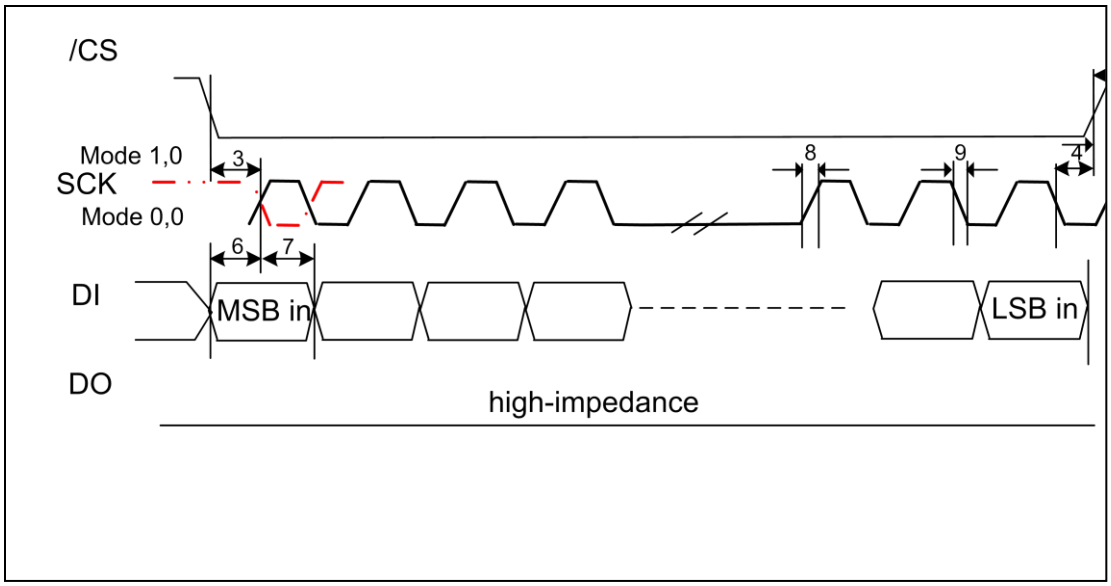

Fig. 8 Serial input timing.

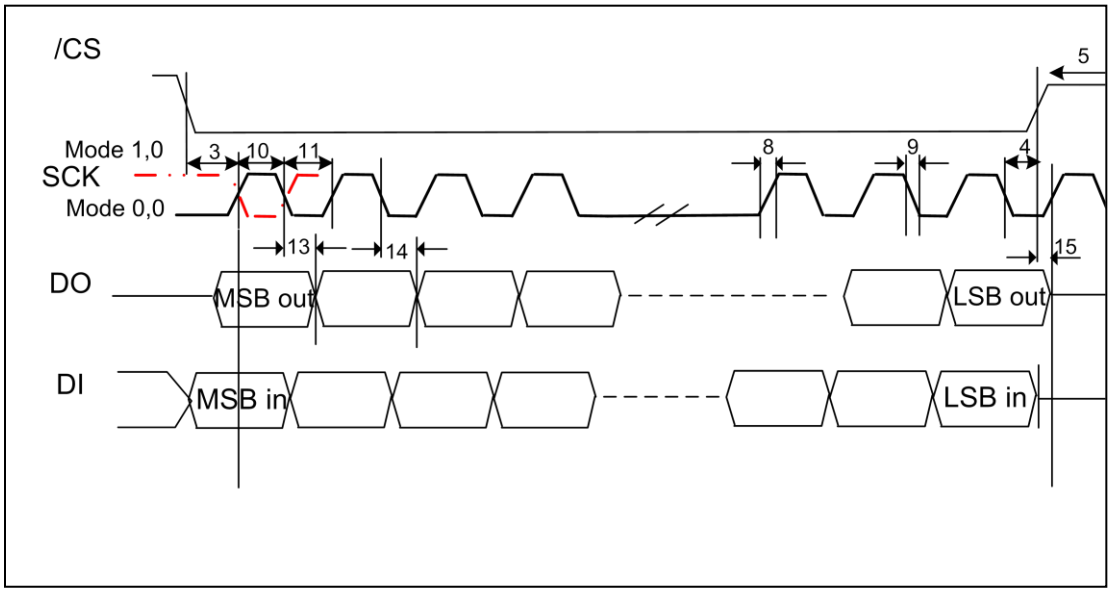

Fig. 9 Serial output timing.

APPPENDICE C

2k SPI BUS SERIAL ROM DOCUMENTS

TABLE OF CONTENTS

DOCUMENT Page

1.Description

The SPI serial bus ROM is 2Kbyte memory device. The memory is accessed through a simple serial peripheral interface (SPI) compatible serial bus. The SPI is a serial synchronous communication protocol that requires minimum of 3 wires, which are a clock input (sck), data in (di) and data out (do) bus lines. The device is enabled through the chip select enable pin (csn).

The device has to be reset via reset (rst) pin, a toggle of low to high transition complete the reset cycle. Since the device does not have an on-chip crystal/ clock oscillator, the external clock source is required to supply through clock input line (clk_i). The device support two operating modes with cpol = 0, cpha = 0 and cpol = 1 and cpha = 0.

To help in debug, pins ld, ce and clk_sram are used for debugging purpose. For receiving every 8-bit, ld will be asserted and back to low state. A pulse can be observed at pin ce as a toggle of transferring data from ROM to SPI data buffer. Pin clk_ram is the clock pulse that is supplied to the ROM to shift out the data from ROM to SPI data buffer.

1.1 Features

Max clock 8MHz

3.3V low-power CMOS technology

4K x 8bit organization

Sequential read (Page Read/Burst mode) not supported

Read cycle time: 280ns max.

Temperature range supported: -125 ^{o}C to +275 ^{o}C

Table 1. Instruction Set

Instruction Name	**Instruction format**	**Description**
READ	0000 0011	Read data from memory array at the selected address

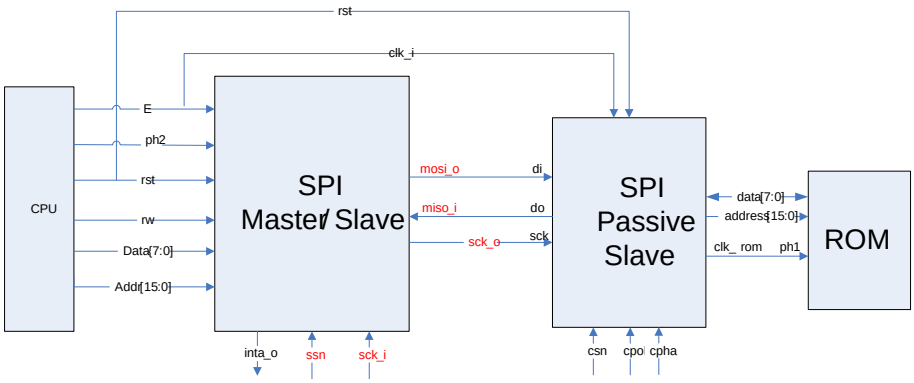

Fig. 1 Master and Slave SPI devices communication diagram.

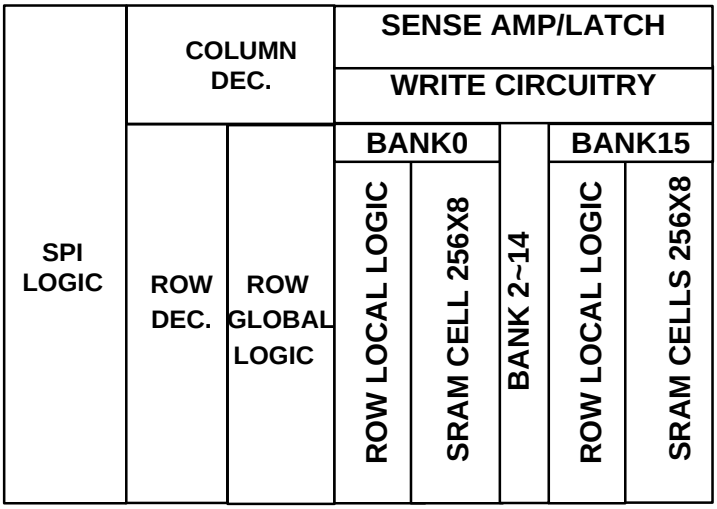

Fig. 2 ROM architecture diagram.

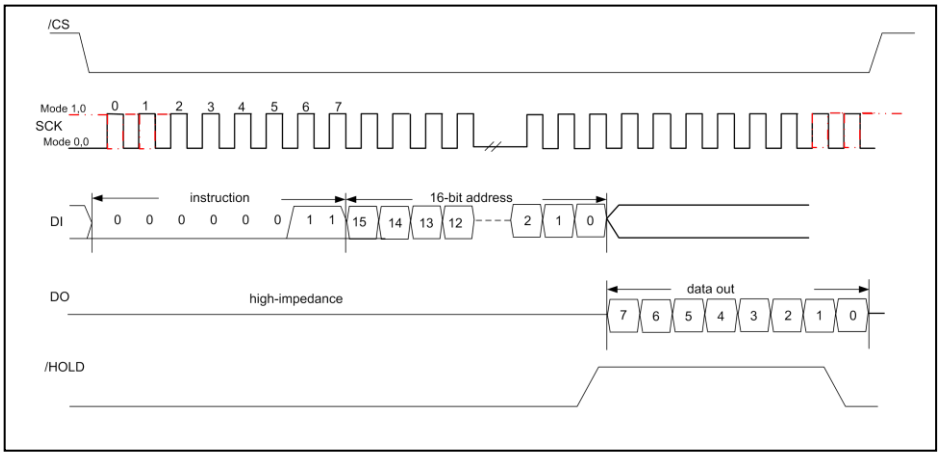

Fig. 3 Seiral read sequence timing.

2.Pins

TABLE I
Pads Out(External Connections)

Port	Width	Direction	Description
ctrl_en	1	input	Control enable
lrw	1	output	Scan chain enable
clk_rom	1	output	Debug pin. Clock pulse supplys by SPI slave to the ROM memory circuitry.
vss	1	input/output	Power pin
ce	1	output	Debug pin. Toggle bit to start the transferring of data from ROM to SPI data buffer
sck	1	output	SPI input clock
di	1	input	Slave data in
do	1	input/output	Slave data out
csn	1	input	chip select/enable active low
e	1	input	E-clock
rst	1	input	System rest
cpol	1	input	Mode select: CPHA,CPOL: 00 or 11
cpha	1	input	Mode select: CPHA,CPOL: 00 or 11
ld	1	output	Debug pin. ld will be asserted after receiving every 8-bit.
scanin	1	input	Scan input
scanout	1	output	Scan output
scanclk	1	input	Scan clock
Eclki	1	input	E clock
sck	1	output	SPI input clock
csn	1	input	Chip select/enable active low

TABLE II
SPI Slave and ROM Circutry Interface Connections

Port	Width	Direction	Description
data	8	input/output	Data input
address	16	input	The memory location the CPU wants to write or read
clk_rom	1	input	Memory internal clock
rw	1	input	rw given by SPI
e	1	input	E-clock input
CE	1	input	Read enable signal, active high.

3. Layout

SPI ROM Description:
Size: 2K bytes
Number of banks: 8
One bank size: 256 rows by 8 columns
Module Area: 5.0mm^2
Standby Leakage power: 0.66mW (at 275 C)
Switch and standby Power: 1.3mW (at 275 C and 8MHz)
Decoder Delay : 10ns
Read Access Time: 280 ns
Useful Read Time: 30ns

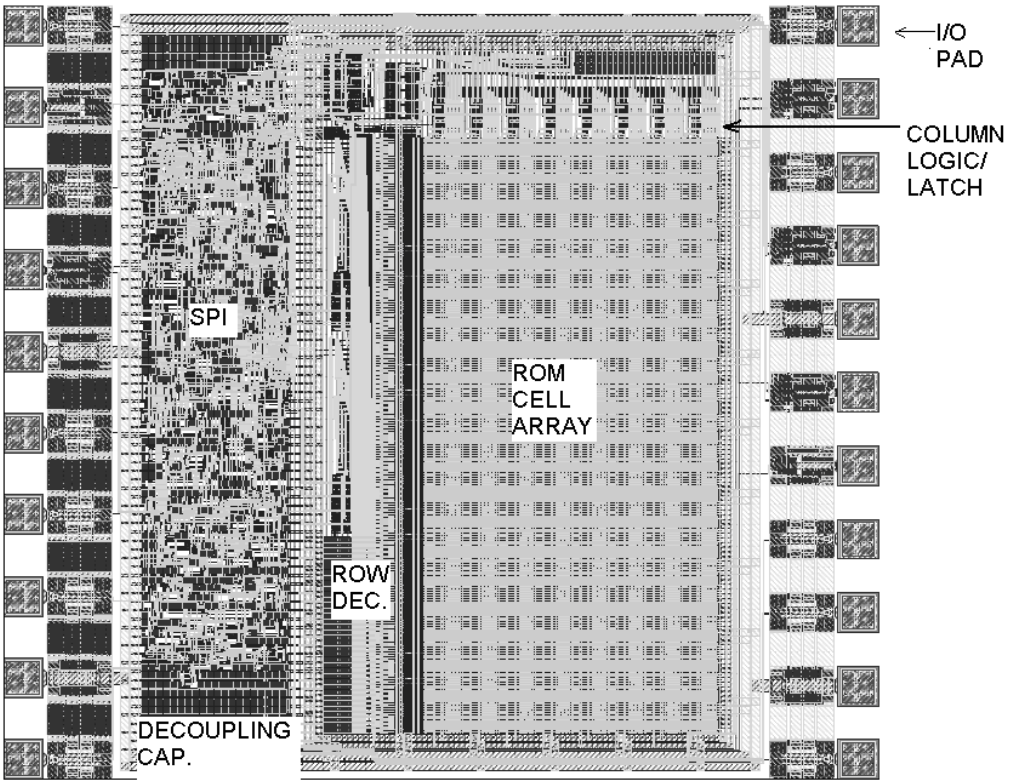

Fig.4 The layout of 2k SPI ROM.

4. Testing and Simulation

Simulator: Cadence Spectre

The timing and functional test with parasitic capacitance is tested on the cadence simulation tool.

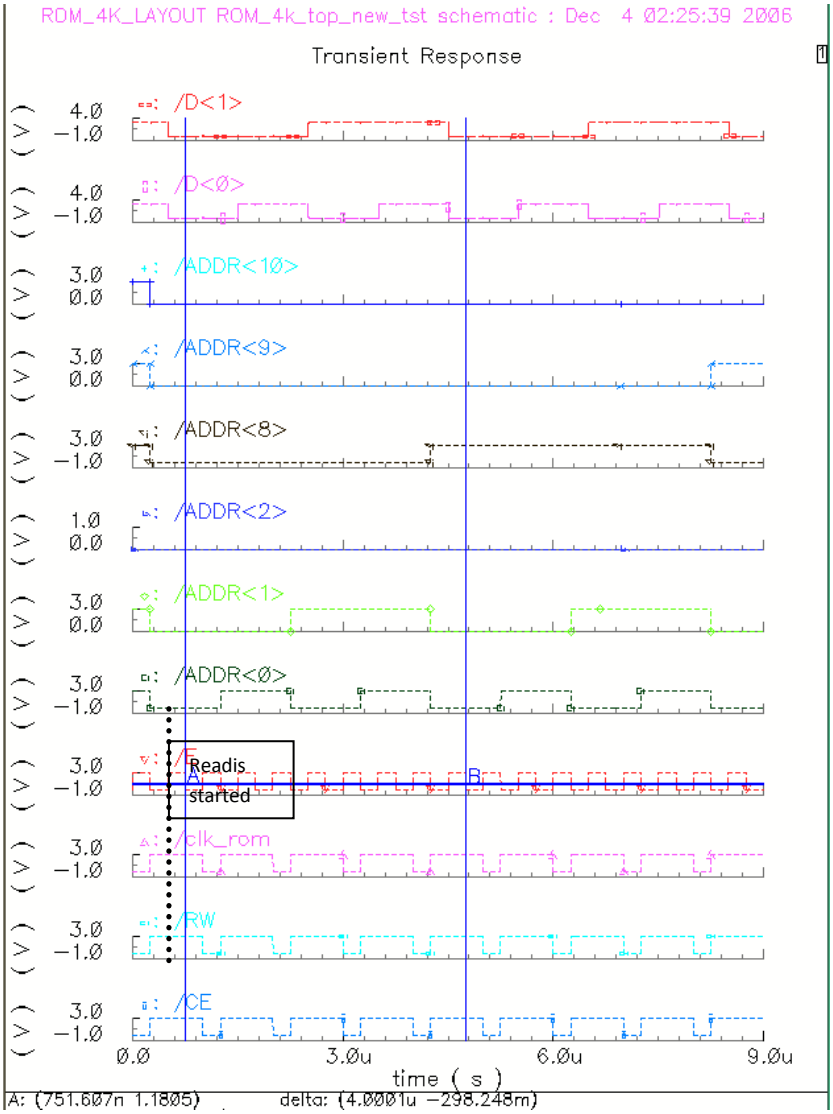

Fig. 5 internal ROM read timing.

5. Electrical Characteristics

Maximum Ratings

Vcc…….….3.6V
All input and outputs w.r.t. Vss……..3.6V
Storage temperature…….....-55 ℃ to 275 ℃
Ambient temperature under bias....-55 ℃ to 275 ℃

Table III
DC Characteristics

T_A = -65 ℃ to 275 ℃ Vcc = 2.0V to 3.3V

Parameter	Symbol	Min	Max	Units	Test conditions
High level input voltage	V_{IH}	2.0	Vcc+0.7	V	
Low level input voltage	V_{IL}	-0.5	0.8	V	
Low level output voltage	V_{OL}	-	0.4	V	I_{OL} =
High level output voltage	V_{OH}	V_{CC}-0.6	-	V	I_{OH} =
Input leakage current	I_{LI}	-44	44	nA	$\overline{CS}$ = V_{CC}, V_{IN}=GND to V_{CC}
Output leakage current	I_{LO}	-44	44	nA	$\overline{CS}$ = V_{CC}, V_{OUT}=GND to V_{CC}
Internal capacitance (all inputs and outputs)	C_{INT}			pF	
Operating Current	$I_{CC\ read}$	-	1.78	mA	V_{CC}=3.3V;SO= Open, F_e= 8MHz (Note)
Standby Current	I_{CCS}	-	1.30	mA	$\overline{CS}$ = V_{CC}

Note: This parameter is periodically sampled and not 100% tested.

Table IV
AC Characteristics

T_A = -65 ℃ to 275 ℃ Vcc = 2.0V to 3.3V						
Param. No.	Symbol	Parameter	Min	Max	Units	Test conditions
1	F_e	E Clock Frequency	-	8	MHz	$2.0V \leq V_{CC} \leq 3.3V$
2	F_{SCK}	SPI Clock Frequency	-	4	MHz	$2.0V \leq V_{CC} \leq 3.3V$
3	T_{CSS}	$\overline{CS}$ Setup Time	125	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
4	T_{CSH}	$\overline{CS}$ Hold Time	250	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
5	T_{CSD}	$\overline{CS}$ Disable Time	125	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
6	T_{SU}	Data Setup Time	4	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
7	T_{HD}	Data Hold Time	16	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
8	T_R	SCK Clock Rise Time	-	2	µs	(Note)
9	T_F	SCK Clock Fall Time	-	2	µs	(Note)
10	T_{HI}	SCK Clock High Time	0.125	-	µs	$2.0V \leq V_{CC} \leq 3.3V$
11	T_{LO}	SCK Clock Low Time	0.125	-	µs	$2.0V \leq V_{CC} \leq 3.3V$
12	T_{CLD}	SCK Clock Delay Time	62.5	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
13	T_V	Output Valid from SCK Clock Low (mode cpol = 0, cpha = 0) Output Valid from SCK Clock High (mode cpol = 1, cpha = 0)	- -	125 125	ns ns	$2.0V \leq V_{CC} \leq 3.3V$
14	T_{HO}	Output Hold Time	16	-	ns	
15	T_{DIS}	Output Disable Time		80	ns	(Note)
16	T_{HS}	$\overline{HOLD}$ Setup Time	125	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
17	T_{HH}	$\overline{HOLD}$ Hold Time	250	-	ns	$2.0V \leq V_{CC} \leq 3.3V$
18	T_{RC}	Internal Read Cycle Time (byte)	-	½ Te +30	ns	$2.0V \leq V_{CC} \leq 3.3V$

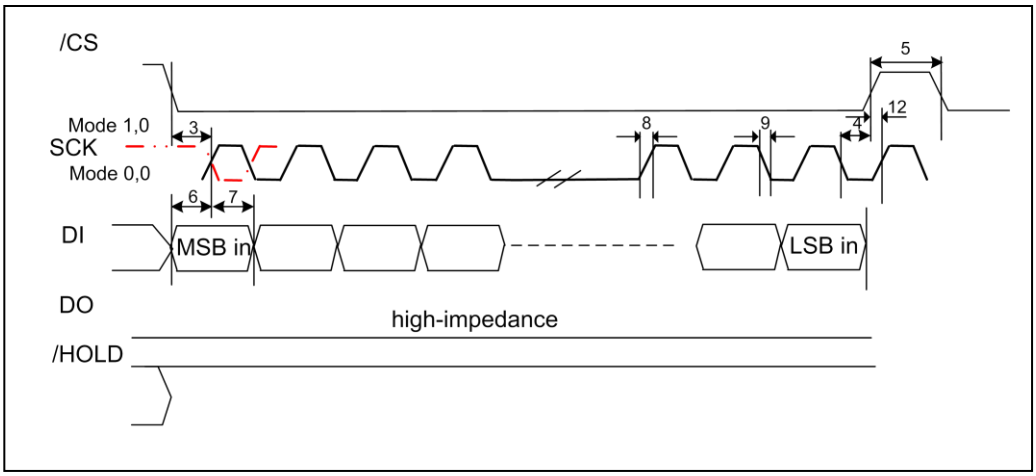

Fig. 6 Serial input timing.

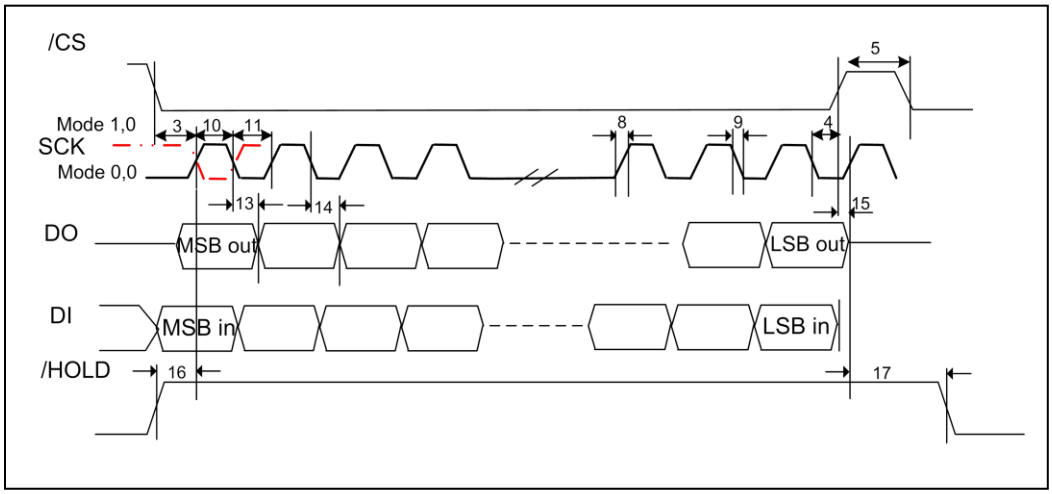

Fig. 7 Serial output timing.

APPPENDICE C

The timing library of SRAM banks for Encounter place and route

```
library(sram_lib){
        technology(cmos)
        delay_model:generic_cmos;
        in_place_swap_mode:match_footproint;
        revision:1.0;
        data: "2010-01-01 01:05:12z";

        default_inout_pin_cap:0.03;
        default_inout_pin_fall_res:0.0;
        default_inout_pin_rise_res:0.0;
        default_input_pin_cap:0.03;
        default_intrisic_fall:1.0;
        default_intrisic_rise:1.0;
        default_output_pin_cap:0.03;
        default_output_pin_fall_res:0.0;
        default_slope_fall:0.0;
        default_slope_rise:0.0;
        default_fanout_load:1.0;
        default_cell_leakage_power:0.0;
        default_leakage_power_density:.0;

        slew_lower_threshold_pct_rise:10.00;
        slew_upper_threshold_pct_rise:90.00;
        slew_lower_threshold_pct_fall:10.00;
        slew_upper_threshold_pct_fall:90.00;
        slew_derate_from_library:1.00;
        input_threshold_pct_rise:50.0;
        input_threshold_pct_fall:50.0;
        output_threshold_pct_rise:50.0;
        output_threshold_pct_fall:50.0;

time_unit:"1ns";
voltage_unit:"1V";
current_unit:"1uA";
leakage_power_unit:"1mW";
pulling_resistance_unit:"1ohm";
capacitive_load_unit(1,pf);

nom_process:1;
nom_temperature:25.0;
nom_voltage:3.3;
opeatiing_conditions(slow){
```

```
process:1;
temperature:150;
voltage:3.0;
tree_type:"worst_case_tree";
}

default_operating_conditions:slow;
       input_voltage(CMOSIN) {
       vil    :0.3*VDD;
       vih    :0.7*VDD;
       vimin  :-0.5;
       vimax  :VDD + 0.5;
}

       output_voltage(CMOSOUT){

       vol    :0.3*VDD;
       voh    :0.7*VDD;
       vomin  :0.0;
       vomax  :VDD;
}

       power_lut_template(ram_energy_template) {
       variable_1:input_transition_time;
       index_1 ("1000,1001");
}


type(ram_row_ADDRESS) {
       base_type:array;
       data_type:bit;
       bit_width:256;
       bit_from:255;
       bit_to:0;
       downto:true;
}

type(ram_col_ADDRESS) {
       base_type:array;
       data_type:bit;
       bit_width:9;
       bit_from:8;
       bit_to:0;
       downto:true;
}

type(ram_DATA) {
```

```
        base_type:array;
        data_type:bit;
        bit_width:16;
        bit_from:15;
        bit_to:0;
        downto:true;
}



cell(SRAM_8banks) {
        dont_use:TRUE;
        dont_touch:TRUE;
        interface_timing:TRUE;


pin(vb)
{
        direction:input;
        capacitance:0.026;
        input_voltage:CMOSIN;
}


pin(E_glo)
{
        direction:input;
        capacitance:0.2;
        input_voltage:CMOSIN;
        clock:true;
        min_pulse_width_low:24; /*cycle 50ns */
        min_pulse_width_high:24;
        min_period:48;
        max_trasition:5;
        internal_power() {
        rise_power(ram_energy_template){
        index_1 ("0.0 1.0");
        values ("89.776,89.776")
}
        fall_power(ram_energy_template){
        index_1 ("0.0 1.0");
        values ("89.776,89.776")

}
}
}
```

```
pin(PC_glo)
{
       direction:input;
       capacitance:0.2;
       input_voltage:CMOSIN;
       clock:true;
       min_pulse_width_low:24; /*cycle 50ns */
       min_pulse_width_high:24;
       min_period:48;
       max_trasition:5;
}


pin(SE_PC_glo)
{
       direction:input;
       capacitance:0.2;
       input_voltage:CMOSIN;
       clock:true;
       min_pulse_width_low:24; /*cycle 50ns */
       min_pulse_width_high:24;
       min_period:48;
       max_trasition:5;
}



pin(WE_glo)
{
       direction:input;
       capacitance:0.2;
       input_voltage:CMOSIN;
       clock:true;
       min_pulse_width_low:24; /*cycle 50ns */
       min_pulse_width_high:24;
       min_period:48;
       max_trasition:5;
}

pin(SE_glo)
{
       direction:input;
       capacitance:0.2;
       input_voltage:CMOSIN;
       clock:true;
       min_pulse_width_low:24; /*cycle 50ns */
```

```
        min_pulse_width_high:24;
        min_period:48;
        max_trasition:5;
}

pin(rowsel_glo)
{
        direction:input;
        capacitance:0.2;
        input_voltage:CMOSIN;
        clcok:true;
        min_pulse_width_low:24; /*cycle 50ns */
        min_pulse_width_high:24;
        min_period:48;
        max_trasition:5;
}

pin(OE_glo)
{
        direction:input;
        capacitance:0.2;
        input_voltage:CMOSIN;
        clcok:true;
        min_pulse_width_low:24; /*cycle 50ns */
        min_pulse_width_high:24;
        min_period:48;
        max_trasition:5;
}


bus(RS_b[255:0])
{
        bus_type:ram_row_ADDRESS;
        direction:input;
        capacitance:0.026;
        input_voltage:CMOSIN;
        timing(){
        related_pin:"E_glo";
        timing_type:setup_rising;
        intrisic_rise:70;
        intrisic_fall:70;
        }
        timing(){
        related_pin:"E_glo";
        timing_type:hold_falling;
        intrisic_rise:5;
        intrisic_fall:5;
```

```
        }
}

bus(BS[8:0])
{
        bus_type:ram_col_ADDRESS;
        direction:input;
        capacitance:1.4;
        input_voltage:CMOSIN;
        timing(){
        related_pin:"E_glo"
        timing_type:setup_rising;
        intrisic_rise:70;
        intrisic_fall:70;
        }
        timing(){
        related_pin:"E_glo"
        timing_type:hold_falling;
        intrisic_rise:5;
        intrisic_fall:5;
        }
}

bus(Di_buf[15:0])
{
        bus_type:ram_DATA;
        direction:input;
        capacitance:0.316;
        input_voltage:CMOSIN;
        timing(){
        related_pin:"E_glo"
        timing_type:setup_rising;
        intrisic_rise:80;
        intrisic_fall:80;
        }
        timing(){
        related_pin:"E_glo"
        timing_type:hold_falling;
        intrisic_rise:5;
        intrisic_fall:5;
        }
}

bus(Dout[15:0])
{
        bus_type:ram_DATA;
        direction:output;
```

```
        max_capacitance:3.418;
        output_voltage:CMOSOUT;
        timing(){
        related_pin:"OE_glo"
        timing_type:setup_rising;
        intrisic_rise:110;
        intrisic_fall:110;
        }
        timing(){
        related_pin:"OE_glo"
        timing_type:hold_falling;
        intrisic_rise:5;
        intrisic_fall:5;
        }
}
}

}
```

VITA

ZHE YUAN

Candidate for the Degree of

Doctor of Philosophy/Education

Dissertation: EXTREME TEMPERATURE MEMORY DESIGN WITH THE REDUCED DESIGN TIME USING SILICON ON SAPPHIRE TECHNOLOGY

Major Field: Digital and Mixed-signal Circuit Design

Biographical:

Education:

Completed the requirements for the Doctor of Philosophy in Electrical Engineering major at Oklahoma State University, Stillwater, Oklahoma in July, 2011.

Completed the requirements for the Master of Sciences in Electrical Engineering at Syracuse University, Syracuse, NY,USA in 2004

Completed the requirements for the Bachelor of Science in Electrical Engineering major at Sichuan Institute of Technology, Chengdu, Sichuan, China in 2002.

Experience:

Professional Memberships:
Electrical Engineer, 2011~now, worked on Nanowire Thermoelectric Infrared Detector Arrays project for Amethyst Research Inc.

Graduate Research Assistant, 2005~2010, worked in Mixed-Signal VLSI lab at School of Electrical and Computer Engineering, Oklahoma State University

Graduate Teaching Assistant, fall 2005, Digital Integrated Circuit Design (ECEN 4303) at School of Electrical and Computer Engineering, Oklahoma State University.

Electrical Engineer in Eastern Electronics, MA 2004~2005, Repair desktop and laptop, TV, printer, board level troubleshooting

Institution: Oklahoma State University Location: Stillwater, Oklahoma

Title of Study: EXTREME TEMPERATURE MEMORY DESIGN WITH THE REDUCED DESIGN TIME USING SILICON ON SAPPHIRE TECHNOLOGY

Pages in Study: 117 Candidate for the Degree of Doctor of Philosophy/Education

Major Field: Electrical Engineering

Scope and Method of Study:

This dissertation describes the high temperature memories as part of the design for 275 ℃ HC11 microcontroller and 200 ℃ LEON3 processor using the 0.5 um Peregrine SOS CMOS technology, which are suitable for aerospace, well logging, solar controllers, and automotive applications. Data for I_{ON} and I_{OFF}, threshold and mobility versus temperature was extracted. High temperature 3.3V digital cell libraries were developed for the LEON3and HC11. The memories were designed with aid from the measured data, addressing write and read stability in the context of floating body effect, kink effect, and shrinking I_{ON}/I_{OFF} currents with temperature. The LEON3/HC11 was placed & routed with the standard cell library and characterized memories. Memory testing demonstrated functional memory designs and with testing analysis, the error sources of the memories are found such that memory yield will be improved in future designs.

Findings and Conclusions:

In this dissertation, we have demonstrated high temperature memories for microprocessor designs using the 0.5um Peregrine SOS CMOS technology, which can be useful for aerospace, well logging, solar controllers, automobile and other high temperature environment applications. The designed memories are as part of the design for 275 ℃ HC11 microcontroller and 200 ℃ LEON3 processor. The memories designed include: a 4K on-chip SRAM, 512byte on-chip ROM, 4K SPI-SRAM, 2K SPI-ROM , 2K x16 off-chip SRAM, 128 x 32 cache , 32 x 32 cache, and SRAM design with Encounter support. For the HC11, the design simulations are over the -55 ℃ to 295 ℃ range with testing completed over the room to 295 ℃ range. For the LEON3, the design simulations are over the -55 ℃ to 200 ℃ range with testing completed over the room to 200 ℃ range. The 4K SPI-SRAM and 2K SPI-ROM testing confirmed operation across room to 295 ℃, making the memories suitable for 275 ℃ HC11 design. The HC11 testing proved 4K on-chip SRAM and 512byte on-chip ROM were functional. The LEON3 testing confirmed operations across room to 200 ℃ including 128 x 32 cache and 32 x 32 cache. The 2K x 16 off-chip SRAM is identical to 4K SPI-SRAM and proved suitable for LEON3 usage. The memory row errors and cell errors are believed to be mainly caused by the silicon defects resulting in strong (leaky

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NMOS) transistors. The memory column errors are believed to be mainly caused by Metal2 shorts. Shorted-circuits of the memories are believed to be mainly caused by Metal2 shorts as well. The row errors and cell errors can be reduced by redesign of digital logic and the memory cell. The column errors can be reduced by increasing the separation of Metal2. A novel 6T PMOS SRAM cell and a stacked-NMOS sense amp were designed to solve these issues. The LEON3/HC11 was placed and routed with the standard cell library and characterized memories. Finally, SRAM design with Encounter support has been demonstrated to be a fast time to market memory design solution.

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ABSTRACT

This dissertation describes high temperature memories as part of the design for 275 ℃ HC11 microcontroller and 200 ℃ LEON3 processor using the 0.5um Peregrine SOS CMOS technology. The memories having been designed include: a 4K on-chip SRAM, 512byte on-chip ROM, 4K SPI-SRAM, 2K SPI-ROM , 2K x16 off-chip SRAM, 128 x 32 cache , 32 x 32 cache, and SRAM design with Encounter support. The 4K SPI-SRAM testing and 2K SPI-ROM confirmed operations across room to 275 ℃. The LEON3 testing confirmed operations across room to 200 ℃ including 128 x 32 cache and 32 x 32 cache. With testing analysis, good candidates for error sources of memory failure were found and memory yield can be improved for future memory designs. The error sources are believed to be mainly the silicon defects and/or strong (leaky NMOS) transistors, and Metal2 shorts. The developed methodologies presented are essential for the microprocessor and memory designs across process and temperature corners. Data for I_{ON} and I_{OFF}, threshold and mobility was developed with temperature. High temperature 3.3V cell libraries were developed for the LEON3 and HC11. The memories were designed with aid from the measured data, addressing write and read stability in the context of floating body effect, kink effect, shrinking I_{ON}/I_{OFF} currents. Especially a novel 6T PMOS SRAM cell and a stacked-NMOS sense amp were designed to solve these issues. The LEON3/HC11 was placed and routed with the standard cell library and characterized memories. Finally, SRAM design with Encounter support has been demonstrated to be a fast time to market memory design solution.

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