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This dissertation is dedicated to my dear wife.
None of this would have been possible without her
sacrifices, unconditional love, and support.

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Abstract

The method in which the frequency spectrum is currently allocated is unsustainable. An increasing number of devices are becoming wireless, overcrowding an already crowded spectrum (e.g., the ISM band). Therefore, future systems will be forced to move to higher frequencies in order to be allocated an unused slice of the spectrum and accumulate the desired/required bandwidth. Furthermore, with the continued desire to implement a multitude of sensors on unmanned aerial vehicles (UAVs), as well as the need for conformal small-cell repeaters for 5G communications, next generation systems will have to achieve unprecedented reductions in size, weight, power, and cost (SWaP-C).

In order for future systems to become practical, several fundamental technological hurdles must be overcome including the development of low loss and highly integrated components used to build next generation systems. The RF/microwave filter is of particular interest, as it is not only crucial for conditioning the signal for transmission and/or digitization, but can also affect critical system parameters based on it's placement in the system. Due to the increased attenuative nature of the environment at microwave frequencies, the systems dynamic range will have to be maximized requiring an exceptionally low loss filter if placed close to the antenna in the receiver (Rx) chain, which is necessary for defense and adaptive/re-configurable systems. While low loss microwave filtering can be easily achieved using waveguide design techniques,

it is much more difficult in a highly integrated planar design due to increased radiation and dielectric losses. A promising solution which minimizes these losses and offers a planar solution is the suspended integrated stripline (SISL) filter.

In this research, a low loss fully-board integrated lowpass and highpass filter, using the suspended integrated stripline technology, are designed and studied, pushing the stat-of-the-art in planar filtering technologies. A multi-layer board stack-up, with internally buried hollowed cavities, is used to create the suspended stripline. The embedded filter is accessed through a co-planar waveguide-to-stripline vertical via transition and vice-versa. Simulated and measured results show that insertion losses of less than 1 dB are obtainable including the vertical via transition and associated trace losses. Compared to it's suspended substrate stripline (SSS) predecessor, the SISL filter is one order of magnitude smaller and lighter while achieving identical performance. Beyond the proposed filters, this technological solution can be applied to several other passive microwave components such as couplers, power dividers, and gain equalizers. The capabilities demonstrated in this research will be crucial to the design and integration of modern and next generation systems as it requires no mechanical housing, connectors, or assembly, resulting in a light weight, compact size, and low cost solution.

Chapter 1

Introduction

1.1 Motivation

The recent trend in modern wireless and radio frequency (RF) system design has been to integrate several subsystems onto a single printed circuit board (PCB) through the use of multi-chip modules (MCM) [1], [2] or system on chip (SoC) [3]–[5] techniques. While a single custom designed application specific integrated circuit (ASIC) that could perform all the tasks required for a specific system is ideal, it is currently unrealistic due to cost and performance restrictions. Therefore, a more realistic approach is to integrate several amplifiers, switches, and attenuators onto a single ASIC and utilize an underlying multi-layer substrate stack-up to integrate and design the needed passive components (i.e. filters and antennas) [6]. This thrust area has been crucially influenced over the last decade to meet the reduced size, weight, power, and cost (SWaP-C) demands for wireless communication (5G) [7], [8] as well as automotive radar and un-manned aerial vehicle (UAV) sensors [9]. Furthermore, beyond the commercial market, the science and defense communities have also benefited from these higher forms of integration; specifically, in the areas of weather [10], remote sensing [11], and airborne electronic warfare [12].

This is in large part due to advances in active electronically scanned arrays (AESAs), which have been made more feasible over the last decade thanks to miniaturized transceiver modules that can be placed behind each element of a phased array antenna.

Another recent trend has been to design systems that are continuously shifting to higher frequencies of operation. An increasing number of devices are becoming wireless, overcrowding an already crowded spectrum. Therefore, it is becoming exceedingly difficult to get the desired/required bandwidths at these lower frequency bands (e.g. UHF, L, S, C). By moving to millimeter wave (mmWave) frequencies, an abundance of unallocated spectrum is available, allowing system designers to not be bandwidth constrained. However, several fundamental technological hurdles will need to be overcome such as the increased attenuative nature of the atmosphere [13], electromagnetic compatibility issues, and highly integrated low loss microwave components to support the system design. All of these hurdles will need to be addressed in order to advance next generation systems without sacrificing critical system parameters and data quality.

Among the multitude of microwave components, the filter is of particular interest in the design of next generation systems. Filters are used extensively throughout the design to suppress multiplicative harmonics and/or spurious signals that are generated by up-conversion mixer processes. Until digital-to-analog (DAC) converters can directly produce the high frequency signals needed for transmission, these up-conversion processes are needed to operate at higher frequencies. Filters are also used in the RF front-end of the system to precondition the waveform prior to transmission out of the transmitter (Tx) antenna and after being captured by the receiver (Rx) antenna right before

down-converting the waveform to an intermediate frequency (IF). An ideal front-end filter will have a passband bandwidth equal to that of the generated waveform and display very low passband insertion loss with large stopband attenuation. On transmit, these filter characteristics are important to ensure minimal power loss and greatly attenuate any spurious signals to avoid transmitting multiple out-of-band signals. On receive, these same characteristics are desirable to minimize noise figure (NF) contribution and attenuate any unintentional or intentional jammers to avoid saturation of the Rx chain. For communication and radar systems, it is also important that the filter display linear phase to maximize communications throughput and minimize degradation of the resolution cell in radar. Moreover, filter designs to meet next generation system demands will also have to be highly integrated, ideally in some planar fashion, to reduce SWaP-C. While easy in theory, there are several trade-offs between packaged and integrated filters. One primary trade-off is going to higher forms of integration commonly results in increased passband insertion loss, which can drastically affect system performance and is the topic of discussion in the next section.

1.2 Filter Impact on Systems: SWaP vs. Sensitivity

The performance quality of any system depends on the design of the RF front-end; specifically, the design of the Rx chain. A block diagram of a simple RF front-end is shown in Fig. 1.1 with the Tx and Rx chains clearly labeled. A common debate amongst many system designers is should the filter or low noise amplifier (LNA) be placed first in the receiver chain. These components are labeled and circled in red in Fig. 1.1.

By placing the LNA first in the Rx chain, the NF can be greatly limited due

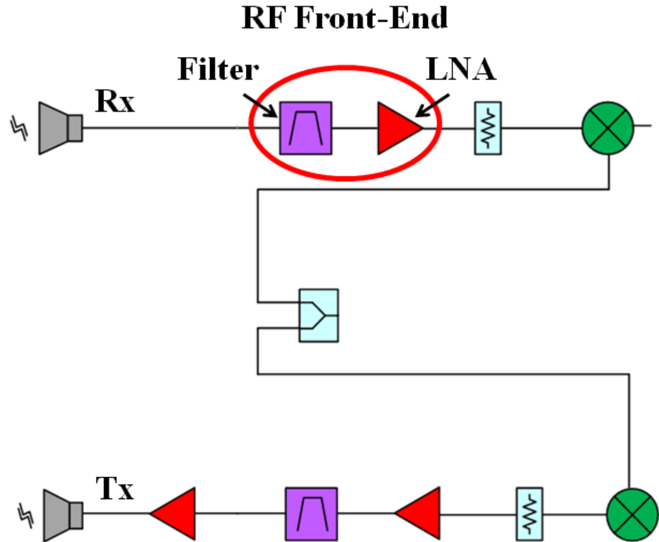


Figure 1.1: Block diagram of a simple RF front-end.

to the high-gain (G_1)/low-noise (F_1) benefits of the LNA. The NF is calculated as

$$NF_{system} = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_N - 1}{G_1 G_2 \cdots G_{N-1}} \tag{1.1}$$

where F_2 and G_2 are the NF and gain of the filter [14]. This mathematically verifies the previous statement. Keeping the NF as small as possible lowers the minimum detectable signal (MDS) and thus improves the overall system dynamic range. A drawback of placing the LNA first in the Rx chain is the front-end is left open to being saturated by out-of-band or near-band signals. These out of band signals can cause inter-modulation issues due to nonlinearities of the LNA especially if the signal is large enough to drive the LNA deep into saturation. In the case of high power jammers, which is a major concern for military systems, the near-band signal could drive the entire Rx chain to the point of burning out the amplifiers rendering the system inoperable.

The alternative option is to place the filter first in the Rx chain. Ideally,

the filter will attenuate these out-of-band signals enough so that they have zero effect on the system performance. However, the NF of a passive component is directly related to its insertion loss. Therefore, the higher the insertion loss, the higher the NF. Looking at (1.1), F_1 will increase with insertion loss and G_1 for a passive component is always less than one. This degradation of the NF limits how small of a signal the receiver can detect (sensitivity) before the signal falls below the noise floor, and therefore degrades the overall system dynamic range. If the filter is to be placed first in the Rx chain, it is imperative for the filter to be low loss (i.e. < 1 dB) to have minimum impact on system performance.

In the past, RF front-end designs that required the filter to be placed first, utilized packaged filters due to their low insertion loss attributes [15]–[17]. However, as mentioned earlier, systems are continuously moving towards higher forms of integration and these packaged filters, with their required connectors, will no longer meet SWaP-C demands. Planar filters such as microstrip and stripline are a traditional method for integrating the filter directly onto/into the printed circuit board, offering a more integrated solution. While these filters are a good solution at lower frequencies, they can become very lossy ($\approx$ 3-5 dB) at higher frequencies due to inherent radiated and dielectric losses.

The microstrip structure [18]–[20] is a planar transmission line technology for realizing LC equivalent or resonator based filters integrated onto the top copper of a two copper-sided dielectric substrate. Fig. 1.2 shows the geometry for a micostrip transmission line. Given the substrate thickness (d) and material properties (dielectric constant: [ϵ_r] & loss tangent: [$\tan\delta$]), the characteristic impedance (Z_0) of the trace can be tuned by changing the width

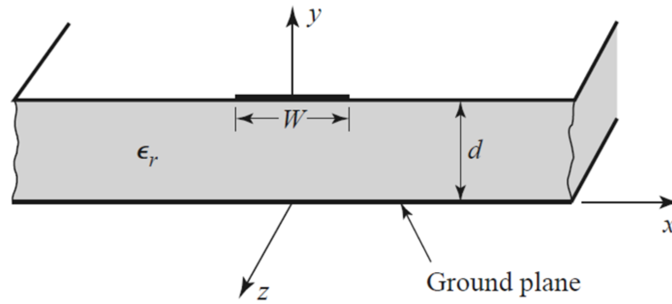
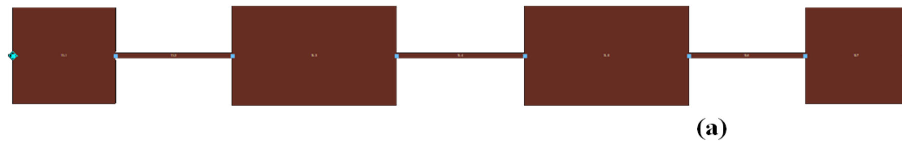


Figure 1.2: Microstrip transmission line geometry [18].

(W) of the trace. Individual microstrip traces are then cascaded in a particular order to provide different filter characteristics as illustrated in the stepped impedance lowpass filter (LPF) example shown in Fig. 1.3. One drawback of the microstrip filter is the added loss due to radiation. The field distribution for a microstrip line is shown in Fig. 1.4. It is apparent that part of the fields are captured within the substrate material itself, but part of the fields are distributed within the air above the substrate. A portion of the fields within the air will radiate away from the circuit and will contribute to the



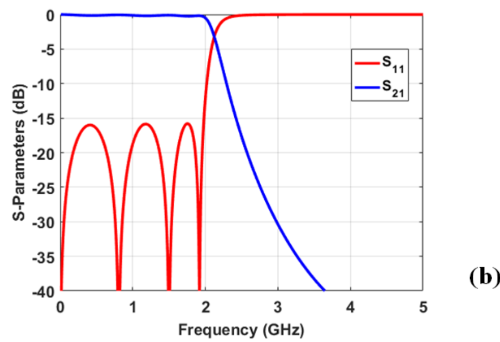


Figure 1.3: Stepped impedance LPF (a) layout and (b) S-parameters.

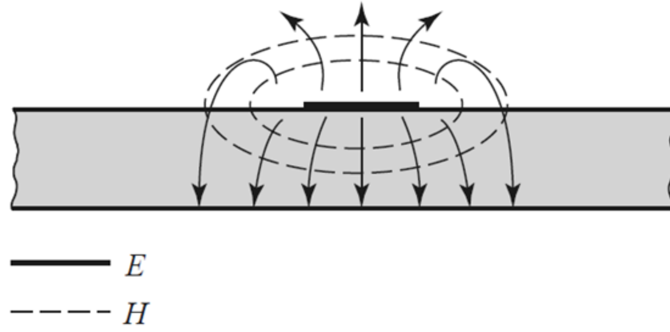


Figure 1.4: Microstrip transmission line field distribution [18].

overall loss (filter passband insertion loss + radiated loss). This radiated loss will worsen with an increase in operating frequency and can cause additional concerns such as undesired coupling into nearby circuits reducing the electromagnetic compatibility (EMC). To minimize this radiated loss and associated EMC concerns, the stripline technology can be used instead.

The stripline structure [18], [20] is another planar transmission line technology ideal for realizing integrated filters. The stripline geometry is shown in Fig. 1.5. Similar to the microstrip trace, the width (W) of the stripline trace can be tuned to yield the desired characteristic impedance, but the trace is embedded within the substrate between two ground planes separated by distance (b). Fig. 1.6 shows the stripline field distribution. Because the field

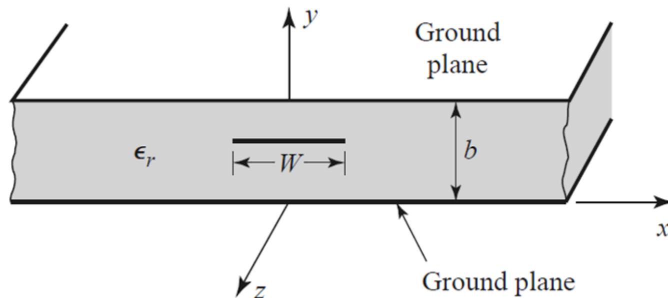


Figure 1.5: Stripline transmission line geometry [18].

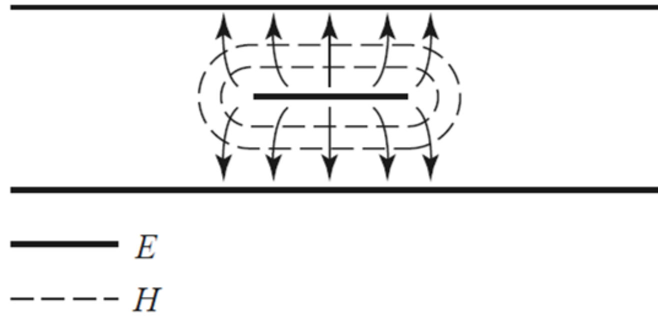


Figure 1.6: Stripline transmission line field distribution [18].

distribution is entirely contained within the two ground planes, a TEM-mode wave propagation is excited with none of the total energy loss due to radiated fields. This is highly beneficial as the radiated loss has been minimized as well as reducing EMC issues. However, stripline designs are very dependent on the substrate and its material properties. If the dielectric loss tangent becomes too large, a significant amount of energy can be lost due to heat as the signal signal propagates through the stripline design. The loss tangent of most materials gets worse as a function of frequency [21] and can add to the overall loss of the design (filter passband insertion loss + dielectric loss). While there are several materials specifically designed to have a small loss tangent, another drawback of the stripline technology is the variation in material property values as a function of frequency and temperature.

The field's velocity of propagation (v_p) within the substrate is

$$v_p = \frac{c}{\sqrt{\epsilon_r}} \tag{1.2}$$

where c is the speed of light (3x10^8 m/s). The relative permittivity (ϵ_r) of the material is a function of both frequency (f) and temperature (T) and should be written as $\epsilon_r(f, T)$. This variability is critical for the design of wideband

filters, especially for large bandwidth radar systems, as measured performance could vary drastically from simulated results. This is because most electromagnetic solvers do not take these frequency or temperature variations into account for the material settings. When designing filters for a 50 ohm characteristic impedance match, any change to the dielectric constant will result in a deviation from the intended 50 ohm impedance resulting in unwanted losses due to reflections at the filter interface. Therefore, stripline filters also have issues achieving wideband low loss designs.

Regardless of which transmission line technology is chosen, they both have a fundamental trade-off of a more integrated design at the risk of increased loss that gets worse with an increase in frequency. Furthermore, with the desire of moving to higher frequencies, to gather more bandwidth, adding additional reflective losses due to the material variation compounds the issue. If the filter is intended to be used as the first component in the Rx front-end, this increased loss has a direct negative impact on the system's sensitivity. As a system designer, this SWaP vs. sensitivity trade-off must be carefully analyzed and will ultimately need to satisfy the link budget requirements.

For example, small cell repeaters will be needed to boost 5G wireless signal power levels as the signal propagates from the multi-input and multi-output (MIMO) phased array antenna to the user's cellphone and vice-versa. Due to the increased attenuative nature of the atmosphere at mmWave frequencies, these small cell repeaters will need to be placed densely throughout large cities. The density of these small cell repeaters will depend on the sensitivity of the device (link budget), which is dependent on the Rx front-end. One proposal is to integrate these repeaters into currently existing light poles to reduce infrastructure cost. While promising, these repeater systems will need

to be small in form factor, and sometimes conformal, in order for successful implementation. This means the filter will need to be fully integrated into the PCB. Given the congested environment of the future, the filter will need to be the first component in the Rx front-end; therefore, its associated insertion loss will directly affect the separation between small cell repeaters. Large passband insertion loss will result in degraded sensitivity and will require the repeaters to be placed closer together. This will inherently increase implementation costs. The ideal solution is to offer a highly integrated and wideband low loss filter solution to maximize repeater separation and minimize costs.

Another example is related to the needs of the defense community where there is a major push to implement sensors on UAVs, which offers human involvement from a distance to enable safer execution of operations. This is a highly beneficial approach when working in hostile environments. Sacrificing sensitivity or any critical system parameter is non-negotiable in warfare operations. But integrating complete systems on tiny platforms requires extreme reductions in SWaP which can lead to non-ideal reductions in system quality due to increased insertion losses. Similar to the commercial application previously mentioned, a highly integrated and wideband low loss filter that can allow unprecedented reductions in SWaP, without sacrificing sensitivity would be ideal for future system designs.

Over the last few decades, there has been an incredible amount of work that has gone into designing such a filter that could offer exceptionally low loss characteristics in a highly integrated form factor. With advances in electromagnetic solvers, complex circuit models, and manufacturing capabilities, filter designers have been able to continuously push the limit in the state-of-the-art. The next section will discuss several filter technologies along with

their advantages and disadvantages. This chapter will also heavily focus on the suspended substrate stripline (SSS) design, which is known for its wideband and low loss capabilities, and discusses several integration techniques that have been investigated along with their successes and limitations.

1.3 History of Low Loss Filter Integration

Next generation radar and communication systems will continue to demand larger dynamic range with increased bandwidth. With improvements to digital back-end hardware and processing power, the ability to independently excite each element of a phased array radar for digital beam-forming and MIMO operation has become more feasible. Element-level control requires individual transmit and receive functionality. To minimize loss and phase imbalance, miniaturized transceivers should be placed directly behind each element. To achieve this at high frequencies, where the wavelength spacing requirements becomes very small, highly integrated front-ends will be necessary, containing both active and passive components. Therefore, filters will need to exhibit low loss, linear phase, and wideband capabilities while simultaneously achieving highly integrated form factors. In addition, as subsystems move closer together due to a decrease in packaging size, increasing the electromagnetic shielding effectiveness will become crucial to avoid EMC issues. Any unintentional coupling could lead to non-ideal system performance, saturation of active components, and/or misrepresentation of data.

Over the last several decades, the resonating waveguide topology has been the leader in low loss filtering at RF/microwave frequencies. These filters offer high quality factors (Q-factors) around $1,000 - 12,000$, but are limited in many applications due to their increased weight, size, and cost. A much

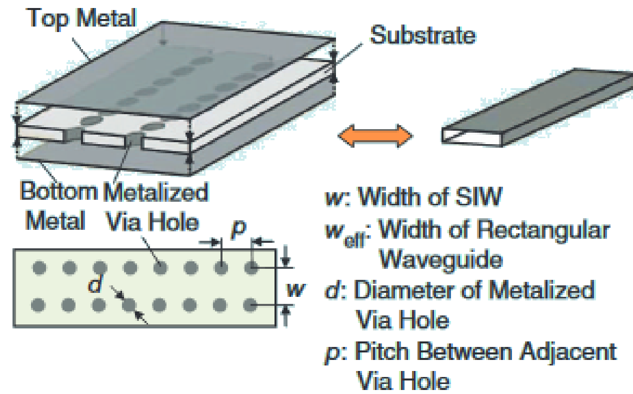


Figure 1.7: SIW technology [22].

more cost-effective design with larger integrability is the substrate integrated waveguide (SIW) shown in Fig. 1.7. In this design, the traditional waveguide is implemented within the substrate of a PCB board or material stack-up. Therefore, the size benefit comes from the waveguide being loaded with a dielectric material. While the electromagnetic fields are completely contained in the SIW design resulting in minimal radiation loss, the majority of the loss contribution comes from the dielectric loss. In general, the loss of an SIW filter is slightly larger than a traditional waveguide, and the Q-factor is smaller with typical values between $150 - 1000$.

The dielectric resonator (DR) offers a compromise between the SIW and waveguide technologies. The Q-factor range associated with the DR is between $200 - 300$. The dielectric resonator is smaller than the waveguide due to the increased permittivity, but has additional dielectric losses contributing to the overall insertion loss. On the other hand, the DR has lower insertion loss than the SIW at the trade-off of being slightly larger and more costly.

All of the above mentioned technologies generate a bandpass filter response through resonating structures. These filters inherently have limited bandwidth

capabilities as the cavity structures are designed specifically to resonate at one frequency. Moreover, the frequency variation and temperature dependency of the dielectric material can further limit the bandwidth limiting their uses in wideband radar applications. Therefore, the remainder of this chapter will focus on low loss implementations of wideband planar filter technologies.

A common technology available today for creating wideband, low loss filters is the SSS filter [23]–[30]. The original SSS concept was first investigated in 1979 [31], shortly after the idea of integrating microwave filters onto a PCB was conceived [32]. Since then, this technology has been used to develop high performance LPFs [33], [34], highpass filters (HPFs) [35], [36], bandpass filters (BPFs) [37], [38], tunable filters [39], and ultrawide band (UWB) filters using traditional methods such as capacitive coupling [40], multiple resonances resonators (MRR) [41], defected ground structures [42], broadside coupling [43], and cascaded LPF/HPF designs [44], [45]. The basic idea is to take the stripline design and replace the dielectric with air. A cross-section of the SSS design is shown in Fig. 1.8. As can be seen in the figure, a thin substrate of thickness (h) is suspended within a metal enclosure of height (H), which creates the air cavities above and below the substrate. The copper clad

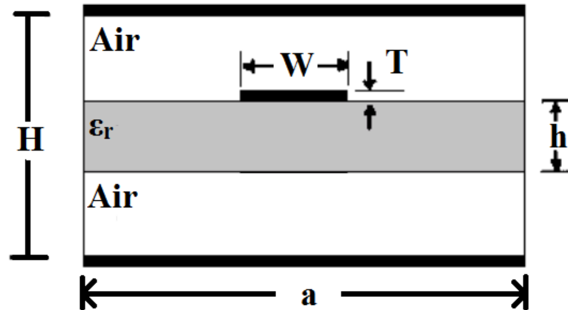


Figure 1.8: Cross-sectional view of the suspended substrate stripline design.

substrate can be etched using photo-lithography to create the filter and then suspended within the air cavity by extending the substrate and securing the additional material between the metal housing. If a symmetrical configuration is used, a TEM-mode wave propagation is excited with the majority of the electric and magnetic fields captured within the uniform air dielectric.

There are several benefits the SSS design offers due to the TEM-mode propagation inside of the air dielectric. Because the relative permittivity of air ($\epsilon_r = 1.0006$) is constant as a function of frequency and readily stable as a function of temperature, it is ideal to use as the propagating medium for microwave design as it minimizes dispersion. This allows for accurate wide-band design and incredibly linear phase. Furthermore, an added benefit of the relative permittivity being LOW, crucial circuit dimensions can be increased making them physically realizable with larger fabrication tolerances. Circuit dimensions and tight tolerances can be a major limiting factor in wideband component design [29].

Another benefit of the SSS design is that the loss tangent ($\tan \delta$) is essentially zero. If a very thin substrate is used inside of a larger cavity, then the volumetric loading will be very small. Therefore, a majority of the fields will be captured within the air medium, which has a loss tangent of zero. This characteristic is also ideal for microwave design. If the loss tangent is zero, there is no additional attenuation due to the wave propagation through the material, which is a drawback of the traditional stripline design. Moreover, due the the minimized loss, high Q-factor resonating filters can be achieved.

Lastly, since the fields are entirely contained within the metal cavity, the SSS design has a large electromagnetic shielding effectiveness. Any radiated fields from the substrate is terminated at the cavity interface. This keeps the

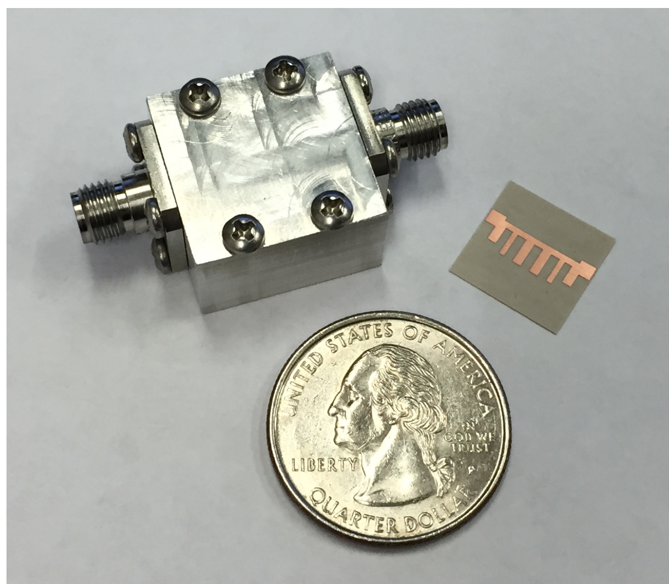


Figure 1.9: Photograph of a suspended substrate stripline lowpass filter [46].

field from coupling onto other structures on the same PCB resulting in non-ideal performance. Fig. 1.9 is a photograph of an eleventh-order generalized Chebyshev SSS LPF (right) and cavity with field-replaceable SMA connectors (left) [46]. A quarter is included for size reference.

One drawback of the SSS design is the increased size and weight due to the required cavity and associated connectors. In order to execute the air cavity concept, the air cavity itself has to be created by some physical means. As seen in Fig. 1.9, this is accomplished via a metal structure which has been machined to create the internal air cavity when the two halves are brought together. Using a light weight material such as aluminum can help reduce weight, but SSS designs tend to be heavier due to the non-zero thick walls adding weight and size. Furthermore, to access the internal filter design, a transition from the filter feed point to the rest of the system must occur. This is traditionally accomplished by using a Teflon protected feed-through pin [47] that is soldered to the filter feed line on one end and mates with a

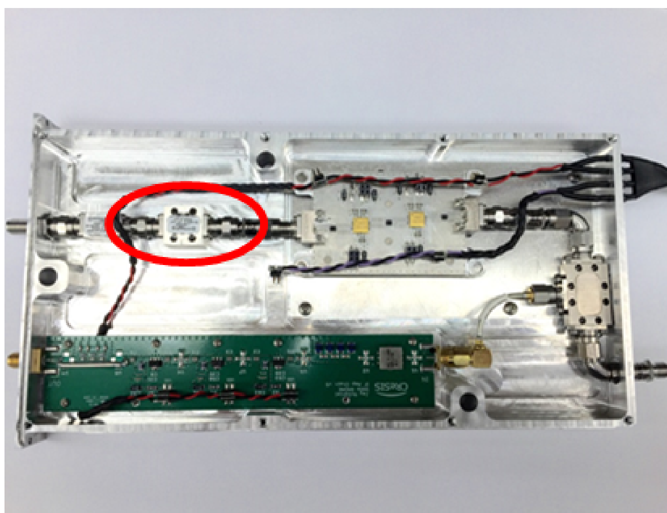


Figure 1.10: Photograph of a connectorized radar receiver with SSS front-end filter [49].

field-replaceable [48] connector on the other end. The connector can then be attached to other components through coaxial cables or RF adapters making it easy to integrate with the rest of the system as shown in Fig. 1.10. The only downside to this approach is that the connectors further increase the size and weight of the overall SSS design.

Another drawback of the SSS design is the parasitic waveguide modes that can be excited within the cavity if not carefully designed. If the cavity width, denoted as a in Fig. 1.8, becomes too wide, a parasitic waveguide mode will propagate, ultimately degrading the performance. The first waveguide mode (TE_{10}) can therefore be thought of as an effective cutoff frequency. This cutoff frequency can be calculated from a first order approximation using (1.3) [50]

$$f_c = \frac{c}{2a} \tag{1.3}$$

where c is the speed of light. The frequency of this waveguide mode should be placed beyond the passband of the filter in order to ensure that it will not

alter the response of the SSS design.

It is apparent that as long as the SSS cavity is designed correctly, the SSS concept is near-ideal for low loss and wideband filter design. The primary drawback is the increased size and weight due to the required cavity and associated connectors. However, there have been other approaches to rid the SSS design of the need for connectors, and also push for higher orders of integration of the air cavities.

Initially, a majority of the integration efforts focused on implementation in integrated circuits (ICs). This is likely due to the ease of integration that multi-layer integrated circuits offered at the time paralleled with a concurrent research focus on micro-machining. The microshield line [52]–[54] was one of the original approaches to integrate air cavities within an IC. The internal air cavities were achieved by micromachining small pyramidal cavities into a silicon wafer stack-up, which contains two silicon wafers with a dielectric membrane in between. After micromaching the air cavities, the stack-up was attached to a carrier wafer finalizing the bottom air cavity, and a top shielding wafer was placed to finalize the top air cavity. A cross-sectional view of the microshield structure is shown in Fig. 1.11. Comparing Figs. 1.11 and 1.8, it should be apparent that the microshield line will have the same ideal qualities

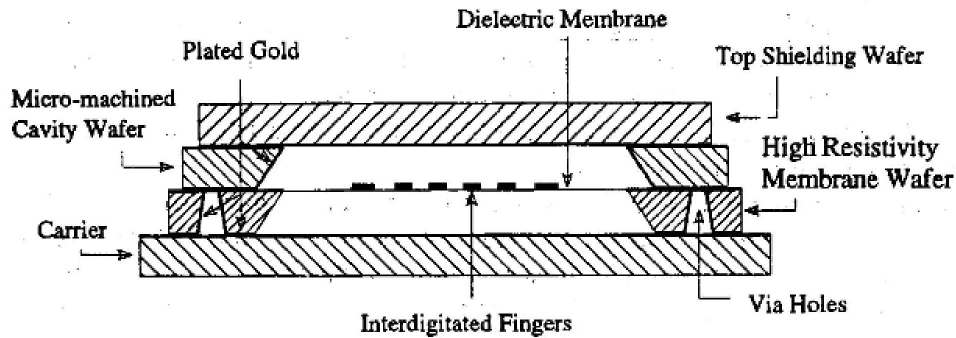


Figure 1.11: Cross-sectional view of the microshield structure [51].

as the SSS design with an added benefit of the higher form of integration. Shortly after the advent of the microshield line concept, it was used to implement lumped element and coupled line structures to design highly integrated and low loss filters (< 2 dB) at Ku-band [55]. While the microshield line is ideal for IC designs, the additional cost and long lead times for custom IC designs limits the wide use of this technology.

In order to offer a more cost effective and easily implemented solution, similar research has been conducted to implement the SSS design into a multi-layer planar PCB. This has become more economical with advancements in PCB manufacturing and material development. Initial work was done by placing the PCB on a metal backplate with cavities drilled out in the areas where the SSS design was intended, and then placing metal caps on top of the PCB completing the SSS cavity structure [56]. A picture of this implementation can be seen in Fig. 1.12. The benefit of this design was the elimination of the connectors by carefully designing the SSS to microstrip transition. The microstrip transmission line could then be extended beyond the SSS design to other components in the microwave circuit. This was the first demonstration

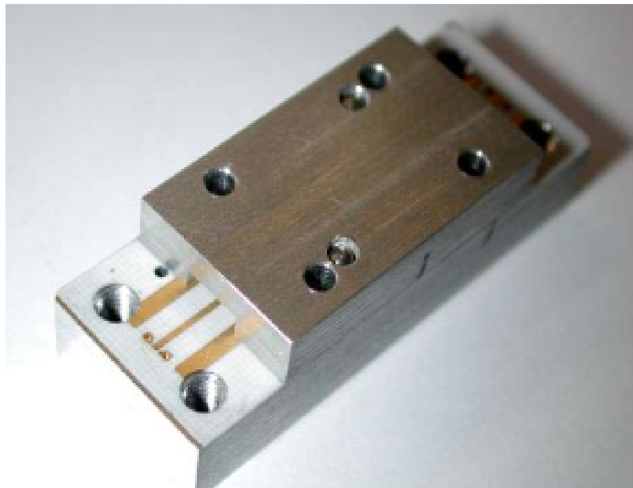


Figure 1.12: Cross-sectional view of the suspended stripline structure [56].

of an SSS filter that could be integrated into complex circuits rather than being used as a discrete component. Moreover, a slight name change happened and this approach quickly became known as suspended stripline (SSL). The downside of this design was that the bulky backplate, used to create the bottom cavity and support the PCB, had to be as thick as the cavity required. This resulted in an overly heavy backplate that increased the weight of the overall design. While the backplate technically only had to be present in the SSS design area, in reality, this backplate would need to be the size of the circuit board to provide mechanical rigidity as well as provide proper thermal dissipation.

Instead of using a metal backplate to support thin substrates, it is common to attach a thin microwave substrate to a thicker and cheaper substrate such as FR4 to provide mechanical rigidity. This provides a lighter weight and cheaper solution when compared to using a metal backplate. A metal cap could then be placed on top of this stack-up to create a quasi-SSL structure. Because of this newly adopted multi-layer approach, more research was conducted to implement SSL filters in this stack-up [57]. A cross-sectional view of the multi-layer stack-up with metal cap is shown in Fig. 1.13. The results presented in

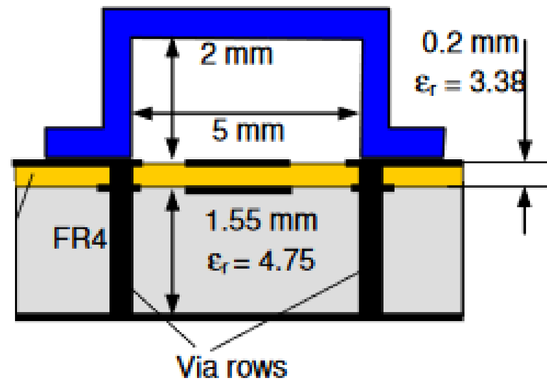


Figure 1.13: Cross-sectional view of the quasi-SSL structure [57].

[57] show that decent filter performance can be achieved using this technique. A clear advantage is the reduced weight and mechanical fabrication. Moreover, physical circuit size can be reduced because of the higher effective permittivity, due to the large dielectric constant of FR4. However, this higher dielectric constant reduces the first parasitic waveguide mode reducing the stopband bandwidth. Also, dispersion and dielectric losses increase due to the larger volume of substrate to air ratio within the cavity.

Recently, a novel transition from substrate integrated suspended line (SISL) to conductor backed coplanar waveguide (CPWG) was developed to further push the state-of-the-art of suspended circuits [58]. A 3-D view of the SISL stack-up is shown in Fig. 1.14. Compared to its predecessors [59]–[61], the SISL transition uses no mechanical housing reducing the need for mechanical processing along with size and weight. This new transition utilizes PCB technology to offer a self-packaged multi-layer structure, which has advantages such as small size, low cost, and minimized weight. This technology has been widely used and proven to be an excellent transmission line to realize ampli-

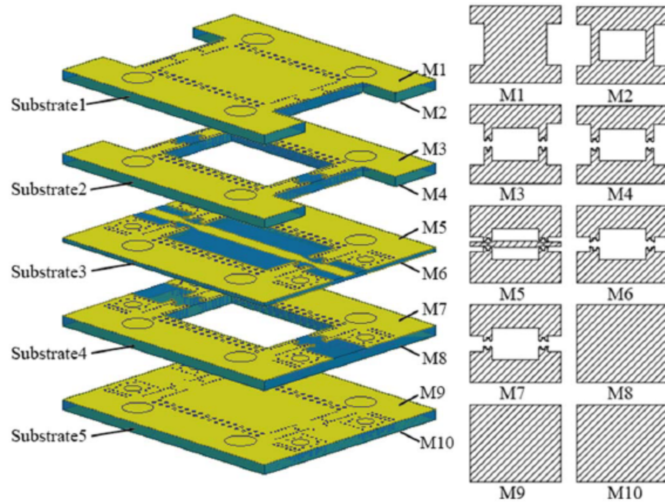


Figure 1.14: 3-D view of the SISL stack-up [58].

fiers [62], antennas [63]–[65], couplers [66]–[69], and filters [70]–[75]. However, the reported SISL transition does have some inherent drawbacks. There are three drawbacks in particular, which are the need for PCB caps, increased optimization time, and limited frequency scalability. Each one of these topics is further discussed below.

As previously mentioned, in [58], the authors proposed a novel SISL transition that rids the original SSS design of connectors and mechanical assembly. Yet, compared to the design in [56], the metallic lid has simply been replaced with a PCB lid and therefore the SISL thru-line is technically on metal layer 5 (M5). Because the PCB cap has to be larger than the SISL design itself, additional board real-estate is used forcing greater separation between components and increasing the overall circuit size. Furthermore, if metal shielding is required as part of the packaging process to meet FCC regulations, additional mechanical processing will be needed for each PCB cap which increase costs and overall design complexity.

Another concern with the current SISL transition design is the increased optimization time to minimize reflections at the CPWG-Stripline-SISL boundaries. A discontinuity exists at each one of these boundaries in terms of both material properties and wave propagation. A quasi-TEM-mode propagation exists on the coplanar waveguide trace with an effective permittivity somewhere between 1 (air) and whatever the permititty is of Substrate 3. The effective permittivity can be accurately calculated using design equations in [76], which are the same equations used in Keysight's Advanced Design System (ADS) tool LineCalc. A TEM-mode propagation exists within the stripline section of the transition with an effective permittivity determined by Substrates 2 and 4 if Substrate 3 is kept thin. In the suspended stripline, a

TEM-mode propagation also exists with an effective permittivity close to 1 due to the air cavity. At each one of these discontinuities, it is important to have a gradual field match to minimize these reflections, which can be accomplished by smoothly transitioning from one mode of propagation in one medium to another mode of propagation into a second medium [77]. In [58], the authors taper the transmission line and place vias near the taper to help with this gradual field match. However, the amount of taper and via placement is arbitrarily done and then optimized in ANSYS High Frequency Structure Simulator (HFSS). This transition technique greatly increases the optimization time needed to achieve a successful design.

In addition to the increased optimization time, this complex transition design also limits the frequency scalability of the SISL design. Because no theory, math, or design guidelines are given for the transition section, a designer who wants to use this technology has limited knowledge to frequency scale the design other than use an optimizer. An optimizer can lead to non-ideal results or fail to converge if not set up correctly or given a reasonable design to start off with. This makes the current SISL technology less attractive and more difficult to implement at higher frequencies. In order to make the current design more applicable, a set of design guidelines should be provided to give a good first order approximation based on the desired frequency of operation.

All of the filter technologies discussed in this section along with their advantages and disadvantages are summarized in Table 1.1. The substrate integrated suspended line offers the best performance along with low SWaP capabilities. However, no design currently meets all of the criteria to effectively design low loss, wideband, and highly integrated filters scalable to mmWave frequencies for next generation systems.

Table 1.1: Comparison of filter technologies.

Techn.	Integ.	Low Loss	Wideband	Scalable	Low Cost
Microstrip	✓	x	x	✓	✓
Stripline	✓	x	x	✓	✓
SIW	✓	x	x	✓	✓
DR	x	✓	x	✓	x
Waveguide	x	✓	x	✓	x
SSS	x	✓	✓	✓	x
SISL	✓	✓	✓	x	✓

1.4 Research Objective

In this dissertation, a novel fully-board embedded and self-packaged suspended integrated stripline technology (SISL) is proposed. The proposed SISL design takes advantages of the original suspended line structure and utilizes modern day PCB processing to form a new self-packaged design that also has advantages of low loss, compact size, and reduced cost. Several design guidelines are provided for this innovative approach allowing for quick design times with minimal tuning and frequency scalability. A DC-20 GHz SISL thru-line is designed, fabricated, and measured to verify the technology and offer a first time demonstration of a fully-board embedded SISL design.

The SISL technology is very promising and is extended in this work to design highly integrated and low loss filters. The inherent TEM-mode propagation and air cavity design allows for low loss implementation of microwave distributed filters, such as the stub-based generalized Chebyshev filters demonstrated in this dissertation. An eleventh-order generalized Chebyshev DC-18 GHz LPF is designed to demonstrate the usability of this technology. The

design goals for the LPF are less than 1.0 dB of insertion loss with a return loss greater than 10.0 dB across the entire 18 GHz passband, and greater than 30 dB of stopband attenuation up to 1.5 times the cutoff frequency. Additionally, an eleventh order generalized Chebyshev HPF with cutoff frequency of 2 GHz is designed to demonstrate UWB capabilities of broadside coupled structures in the SISL technology. Both the LPF and HPF are first time demonstrations of fully-board embedded SISL filters.

Another task of this work is to demonstrate the frequency scalability of the proposed SISL technology. This is accomplished by scaling the LPF and HPF designs to Ka-band ($\approx$ 30 GHz). Several design guidelines and considerations are provided to help with the scaling process. Simulated performance in HFSS verifies frequency scalability along with the high frequency capabilities of the proposed SISL technology.

1.5 Outline of the Dissertation

This dissertation is devoted to the suspended integrated stripline technology and filter implementation. Therefore, the primary focus of this dissertation will be on the design, synthesis, and fabrication of the SISL thru-line and generalized Chebyshev filters. Following the introduction, Chapter 2 introduces the design and implementation of the proposed fully-board embedded SISL technology. Several design guidelines, considerations, and trade-offs will be provided to aid in the realization of low loss designs in the SISL platform. This includes the design and simulation of the CPWG and stripline transmission lines, modeling of the Southwest Microwave edge launch connector, material stack-up, CPWG-to-stripline vertical via transition, electromagnetic wave propagation, parasitic waveguide modes, and finally the design, fabrica-

tion, and measurement of a DC-20 GHz SISL thru-line.

Chapter 3 is focused on the design and implementation of a generalized Chebyshev LPF. This chapter starts with the generalized Chebyshev LPF prototype and simulations of the ideal LC model. Next, distributed design equations are derived taking into account packaging effects. HFSS is used to extract the effective permittivity of the air cavity to more accurately calculate distributed line lengths and widths. Next, a quick discussion is given on modifications made to ADS stripline model in order to utilize the plethora of transmission line models in the stripline library. An eleventh-order DC-18 GHz LPF is designed and simulated in ADS to verify design equations. The SISL LPF is modeled in HFSS and simulated to verify ADS model and overall LPF performance. Discussion is provided on fabrication of the LPF and measured results are compared to simulated results.

Chapter 4 is similar to Chapter 3 but is focused on the design and implementation of a generalized Chebyshev HPF. The ideal LC model is simulated in ADS and distributed design equations are again derived. Special attention to broadside coupled structures are given in this chapter to realize UWB HPF performance with manufacture-able lengths and widths. An eleventh order generalized Chebyshev HPF with a 2 GHz cutoff frequency is designed and simulated in HFSS to verify performance and measured results are provided.

Chapter 5 studies the ability to internally cascade the LPF and HPF design to realize super UWB bandpass filters. The modular design approach used to design the cascade reduces the number of vertical via transitions thereby minimizing the insertion loss. To demonstrate the concept, a 2-18 GHz bandpass filter with insertion loss less than 1.0 dB and return loss greater than 15 dB is shown, and measured results are compared to simulated results.

Chapter 6 investigates the ability to frequency scale the SISL technology. To make the technology work at higher frequencies, a few modifications to the design have to be made such as minimizing the air cavity height, movement of SISL structure from copper layer 5 to copper layer 6, and minimizing via separation to avoid excitation of parasitic waveguide modes. Each of the modifications will be discussed in detail. To verify high frequency operation, a DC-40 GHz thru-line is designed and simulated. Next, simulated results are provided for a 28 GHz HPF, 32 GHz LPF, and 28-32 GHz cascaded BPF.

Chapter 7 concludes the dissertation by providing a summary of the work. The significance and technical contributions of this work is listed in this chapter. Topics for future research related to this dissertation are also provided.

The required fabrication steps of the suspended integrated stripline filters will be covered in Appendix A. Appendix B presents the list of acronyms used throughout the dissertation.

Whereas the majority of the research presented here is attributed to the author, some of the fabrications techniques aspects were contributed by Christopher Walker, Paul Boydstun, Dr. Shahrokh Saeedi, and Dr. Hjalti H. Sigmarsson.

Chapter 2

Fully-Board Embedded SISL Technology

The purpose of this chapter is to introduce the proposed fully-board embedded SISL design and provide a highly detailed design procedure of the SISL technology. This chapter will also offer several design guidelines, considerations, and trade-offs for each part of the design process to aid in the realization of RF and microwave designs in the SISL platform. A DC-20 GHz SISL thru-line is used as the design example throughout the chapter. This design example is chosen to verify proof-of-concept and high frequency operation capability. The end result is a first time demonstration of a fully-board embedded SISL design and first time demonstration of a self-packaged suspended line design with frequency capability up to 20 GHz.

2.1 SISL Design and Implementation

Fig. 2.1 shows the exploded 3-D view of the proposed SISL technology. The air cavities and suspended line shown in Fig. 1.8 are fully-embedded within a multilayer PCB stack-up. The stack-up consists of five individual laminate substrate layers. It should be noted that metal layers 3, 4, 7, and 8 (M3, M4, M7, and M8) are completely etched prior to fabrication and are actually implemented on metal layers 2, 5, 6, and 9 (M2, M5, M6, and M9). They are

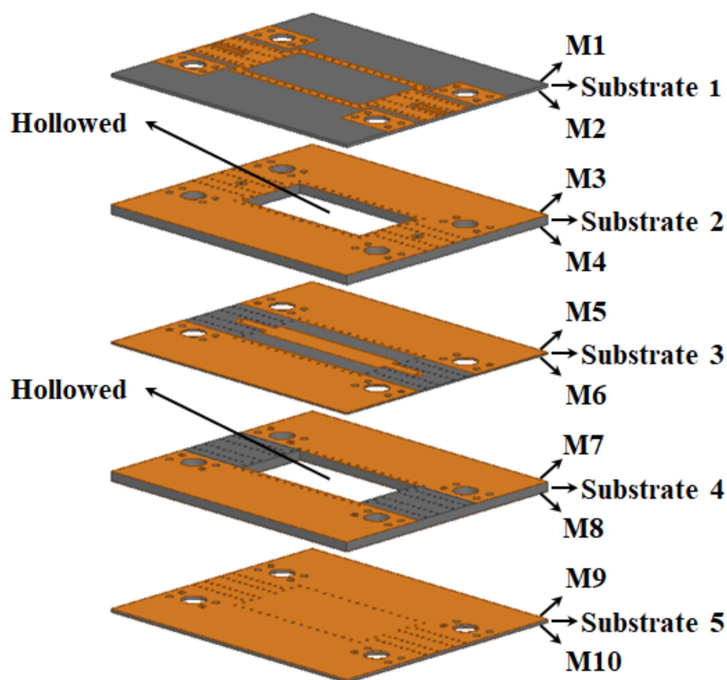


Figure 2.1: 3-D exploded view of the proposed SISL technology.

shown in Fig. 2.1 for visual purposes only. Substrate 2 and Substrate 4 are hollowed around the SISL design, which form the required air cavities. Metal layers 2 and 9 (M2 and M9) are ground planes that create the top and bottom metal walls, respectively. Plated through-vias are arranged around the air cavity to create the metalized side-walls. This is illustrated in Fig. 2.2. The via spacing (s) is less than $\lambda/10$ to ensure an effective constant side-wall and reduce the leakage loss [78].

The SISL air cavity is accessed through a CPWG-to-stripline vertical via transition. This transition is illustrated in Fig. 2.3. The CPWG trace is located on metal layer 1 (M1), which is the top copper of Substrate 1. The internal stripline trace can be placed on either M5 or M6, which is the top or bottom copper of Substrate 3, respectively. Placement of the stripline is dependent on the design and frequency of operation and will be discussed later.

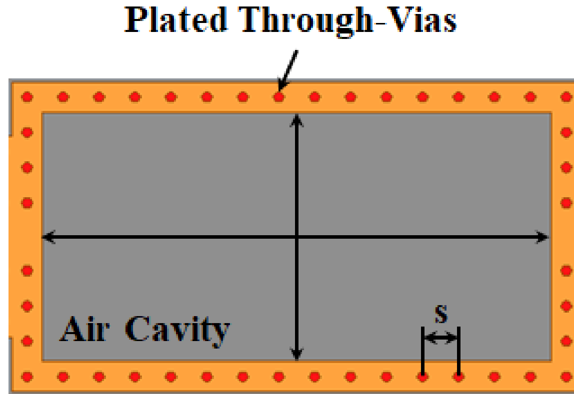


Figure 2.2: Top-down view of the proposed SISL design to illustrate the plated through-vias creating the metal side walls.

Due to the design, a stripline-to-SISL transition must also occur. The wave propagation is TEM-mode in both the stripline and SISL air cavity. Figs. 2.4 and 2.5 show the electric and magnetic field distributions, respectively, in both the stripline and SISL air cavity. If the material chosen for substrates 2-4 have a small relative permittivity, then a very good match at the transition is achieved. This is done by designing both the stripline and SISL design to have

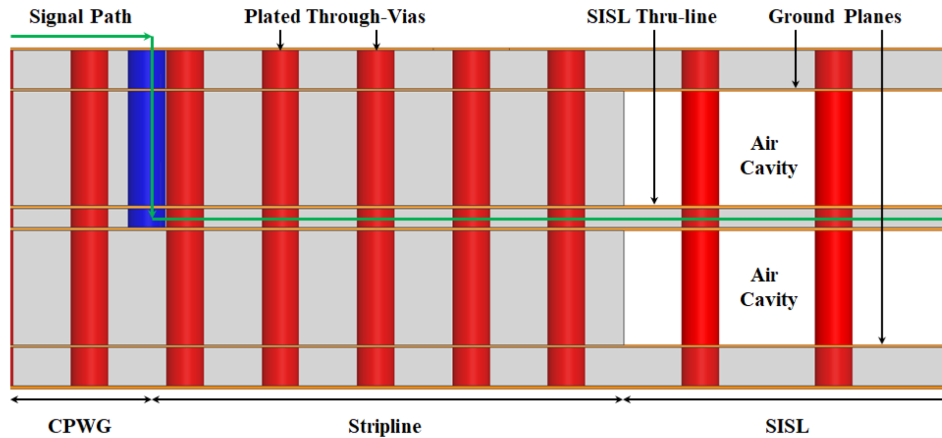


Figure 2.3: Side-view of the proposed SISL design to illustrate the CPWG-to-stripline vertical via transition.

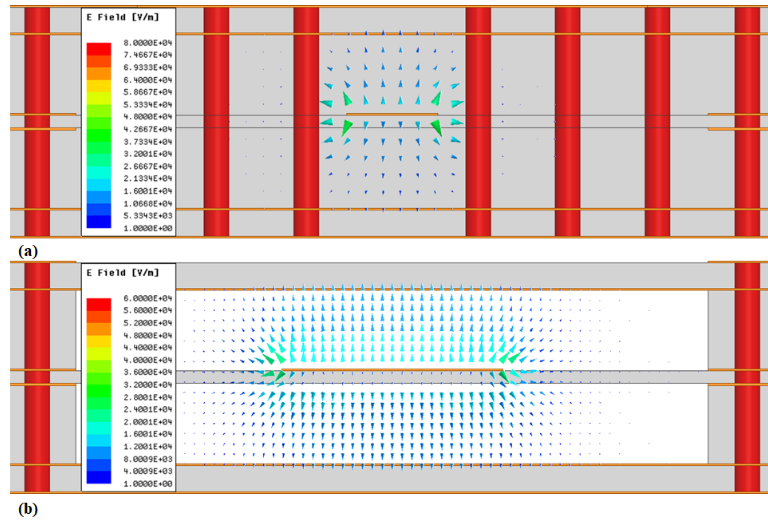


Figure 2.4: Vector plot of the E-field in the (a) stripline and (b) suspended integrated stripline medium.

a characteristic impedance (Z_o) of 50 ohms and connecting them together at the discontinuity. This eliminates the need for an optimized taper and special via placement that was required in [58] and reduces the optimization time needed to minimize reflections.

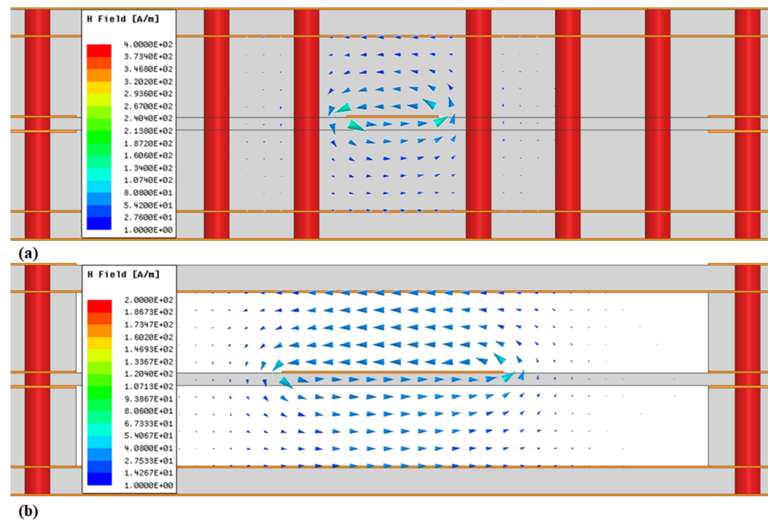


Figure 2.5: Vector plot of the H-field in the (a) stripline and (b) suspended integrated stripline medium.

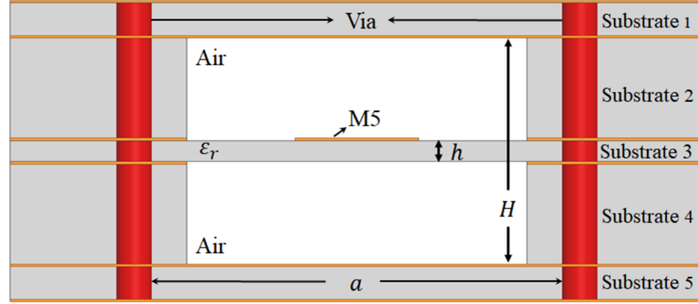


Figure 2.6: Cross-sectional view of the proposed SISL design to further illustrate the waveguide-like structure.

The wave will go through another SISL-to-stripline transition before propagating back up a redundant vertical via transition to the top copper CPWG trace. In an extended circuit, the input/output CPWG traces of the embedded SISL component would connect to the previous/next component in the system.

As with any suspended line design, if not designed correctly, a parasitic waveguide mode can be excited because of the metalized cavity. Fig. 2.6 is a cross-sectional view of the SISL air cavity, which gives a better view to visualize the waveguide-like nature of the design. If the cavity width (a) becomes too wide, parasitic waveguide modes will propagate and create notches within the passband, ultimately degrading the device performance. The first waveguide mode (TE_{01}) can be thought of as an effective cutoff frequency and can be calculated using (2.1) [79]

$$f_c = \frac{c}{2a}\sqrt{1 - \frac{h}{H}\left(\frac{\epsilon_r - 1}{\epsilon_r}\right)} \tag{2.1}$$

where h is the thickness of Substrate 3, H is the air cavity height, ϵ_r is the dielectric constant of Substrate 3, and c is the speed of light. The width should

minimized to push this mode beyond the maximum operating frequency to ensure it will not alter desired performance.

As previously mentioned, as long as the stripline and the input/output port of the SISL design are matched to 50 ohms, each section can be designed independently and then brought together later on to form the final design. Because of this ideal property, the vertical via transition and the SISL air cavity component can be thought of as two sub-designs. This drastically decreases the complexity of the overall design and allows for a more step-by-step design procedure to occur. A typical design procedure is completed as follows:

1. Gather the necessary material stack-up if integrating into a currently existing design, or choose an initial design stack-up if starting with a new design.

2. Design the CPWG transmission line given the material properties and thickness of Substrate 1.

3. (Optional step) Tune the CPWG transmission lines input/output if a edge-launch connector will be used for testing or connecting purposes.

4. Design the stripline transmission line given the material properties and thicknesses of substrates 2-4.

5. Design the CPWG-to-stripline vertical via transition using the CPWG and stripline designs from step (2) and (4).

6. Model the SISL air cavity and extract the effective relative permittivity using HFSS.

7. Design the SISL component (thru-line, filter, etc...) using the permittivity extracted from (6) for a more accurate first-order approximation, and

place between two vertical via transitions to form the final SISL design.

8. Tune the cavity dimensions to ensure that the excitation of parasitic waveguide modes occurs above the maximum operating frequency (might require fine-tuning of the SISL component design).

9. Simulate the final design and make sure the vertical via transition has minimum effect on the final design and verify that any internal resonances do not affect the overall performance.

10. Generate layout files from the HFSS model.

After the design procedure and final simulations are completed, the device is ready for fabrication. Appendix A contains an in-depth fabrication procedure flow that is used to make several of the designs discussed in this dissertation. A quick discussion on the fabrication procedure will be given in this Chapter, but a more detailed description is provided in Appendix A if needed. For standalone SISL devices, after fabrication, the designs are connectorized using Southwest Microwave edge-launch connectors [80] and connected to a calibrated performance network analyzer (PNA) for scattering parameter (S-parameter) measurements.

The next several subsections will go into fine details for each given step of the design procedure listed above. This will be done for the design of a DC-20 GHz SISL thru-line. The thru-line is an ideal component to use as a proof-of-concept as it is easy to design, will provide wide bandwidth performance, and indicates the low loss capabilities that can be achieved with the SISL technology. The following design procedure is accomplished using Keysight ADS and ANSYS HFSS software.

2.1.1 Material Stack-up

Determination of the material stack-up is one the most important steps of the SISL design procedure. The material that is used for Substrate 1 and its thickness will determine the trace and gap width for the top copper CPWG transmission line. Substrates 5 is not as important because it is simply used to provide symmetry for the entire stack-up. This is done to keep the board from bowing during the PCB fabrication process. Substrates 2-4 are the most critical layers to determine as they affect several design parameters. It is suggested to choose the same material for all 3 internal layers which ideally have a relative permittivity close to that of air, and with as small of a dielectric loss tangent as possible. Furthermore, it is recommended to make Substrates 2 and 4 to be the same thickness and Substrate 3 as thin as possible to provide symmetry.

It is important for all three layers to be the same material that provides symmetry so that a homogeneous medium is present to excite a pure TEM-mode wave propagation in the stripline section of the design. The relative permittivity of these layers and thicknesses will determine the trace width of the internal stripline. If the loss tangent is small, then very little attenuation, due to the dielectric, will occur minimizing insertion loss. Another reason to keep Substrates 2 and 4 identical is to provide identical air cavities above and below Substrate 3. Substrate 3 will slightly alter the effective permittivity inside of the cavity as it does volumetrically load said cavity; however, because Substrate 3 is normally kept very thin and ideally has a relative permittivity close to that of air, it has minimal effect. Keeping the dielectric thin with a permittivity close to that of air is also ideal to minimize dispersion, dielectric loss, and effects from temperature variation.

It should also be noted that the thickness of Substrates 2 and 4 determine the maximum frequency of operation, which will be discussed further during the design of the vertical via transition. For now, the key take-away is that the cavity height (H) is maximized to increase power handling capability and decrease temperature variability, but simultaneously minimized to increase the maximum operating frequency.

The material composition itself is important when deciding the material stack-up. There are several different materials to choose from such as the standard epoxy/glass (FR-4), hydrocarbon ceramic laminates, and teflon-filled. All of these different materials have their advantages and disadvantages depending on the application. For this dissertation, a ceramic-filled, teflon-based substrate is used for all substrate layers. The specific material chosen is the RT/duroid® laminates provided by the Rogers Corporation [81]. These laminates offer exceptionally low electrical loss and extremely stable relative permittivity over frequency (up to 40 GHz) and temperature. They are ideal for use in planar multi-layer circuits including the design of filters, oscillators, and delay lines. To bond multiple laminate layers together, the DuPont Pyralux LF sheet adhesive is used, which has an identical relative permittivity as the Rogers 6000 series materials at RF/microwave frequencies.

For the DC-20 GHz thru-line design, the laminate substrates shown in Fig. 2.1 are chosen as follows: Substrates 1 and 5 are 10-mil-thick Rogers RT/duroid 6006® [82] microwave laminate substrates ($\epsilon_r = 6.15$ and $tan\delta = 0.0027$). Substrates 2 and 4 are 30-mil-thick Rogers RT/duroid® 6002 ($\epsilon_r = 2.94$ and $tan\delta = 0.0012$) and Substrate 3 is 5-mil-thick Rogers RT/duroid® 6002 [83]. All copper claddings are electro-deposited with a weight of 1/2 oz. corresponding to a thickness of 18 μm.

2.1.2 CPWG Design

The CPWG design is chosen as the top copper transmission line due to its wide bandwidth and low dispersion capabilities. The characteristic impedance of the CPWG trace is determined by the ratio of the center strip (W) to the gap width (S), as shown in Fig. 2.7, given a specific substrate thickness (h) [76]. If a high dielectric constant substrate is used, the field above the CPWG trace is kept from radiating by concentrating a majority of the field within the substrate between the trace and the lower ground plane. This minimizes radiated loss and helps with electromagnetic compatibility as the circuits are moved closer together. Radiation can be further reduced by placing plated through-hole stitching vias along the CPWG trace. This via stitching will also prevent higher order modes and surface modes internal to the substrate from being excited as long as they are placed correctly. In general, the spacing between vias, shown as (s_1) in Fig. 2.8, should be less than a quarter of a wavelength ($\lambda/4$) of the highest desired operating frequency [85]. To ensure no signal couples onto the extended ground plane, a more industry standard is one-twentieth of a wavelength ($\lambda/20$). It is also important to keep the via spacing (d_1) kept to a minimum to push parallel plate modes above the pass-band. However, the edge of the vias should be placed at least one via diameter

Figure 2.7: Ground-Backed Coplanar Waveguide geometry [84].

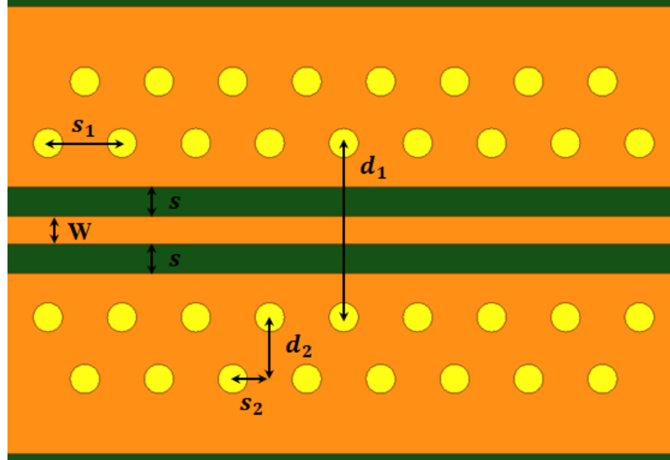


Figure 2.8: Top-down view of the CPWG trace to illustrate design dimensions.

away from the edge of the copper. Finally, a second row of stitching vias can be placed with a spacing of (d_2) and offset of (s_2) to more effectively suppress parallel plate modes [86]. If these design rules are followed, the effective cutoff frequency of the CPWG trace can be pushed as high in frequency as needed and a low loss and low dispersion wave propagation is achieved.

Given the material properties and thickness of Substrate 1, the CPWG transmission line is designed. Using Keysight's ADS tool LineCalc, initial dimensions for the CPWG trace are s = 10 mil and W = 12.9 mil. The CPWG trace is modeled in HFSS to fine-tune the dimensions. An image of the HFSS model is shown in Fig. 2.9. Stitching vias with a diameter of 0.3 mm are placed alongside the CPWG trace with a spacing of $s_1 = 30$ mil, which is a $\lambda/20$ spacing assuming a max frequency of 20 GHz. To avoid any half-wave ($\lambda/2$) resonances from occurring in the passband, the spacing between vias (d_1) has to be less than 155 mil. The via spacing is $d_1 = 70$ mil because the CPWG circuit dimensions are so small. An extra row of vias with a diameter of 0.3 mm are placed with a spacing of $d_2 = 25$ mil and an offset of $s_2 = 15$

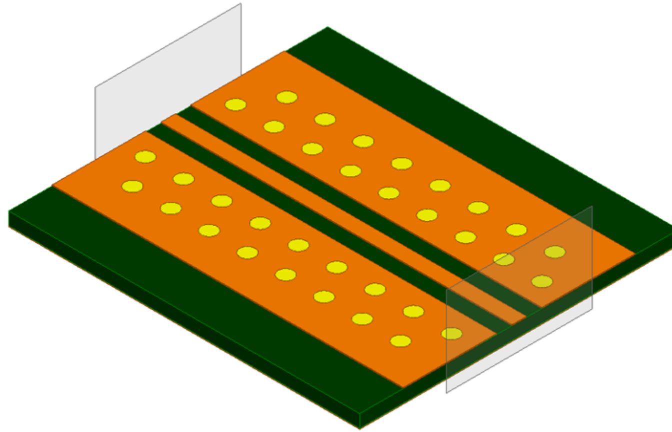


Figure 2.9: HFSS model of the CPWG transmission line.

mil. To improve the 50 Ω match, the trace and gap width are tuned. A return loss better than 20 dB is achieved with trace dimensions of $W = 11.4$ mil and $s = 12$ mil. The simulated S-parameters of the CPWG trace after tuning the circuit dimensions are plotted in Fig. 2.10.

In order to test the individual SISL components, an edge-launch connector is used to excite the mode on the CPWG trace. A signal from the PNA is

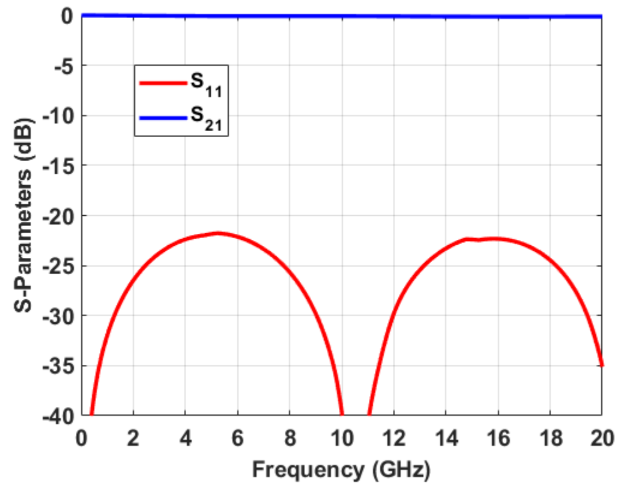


Figure 2.10: Simulated S-parameters of the tuned CPWG transmission line.

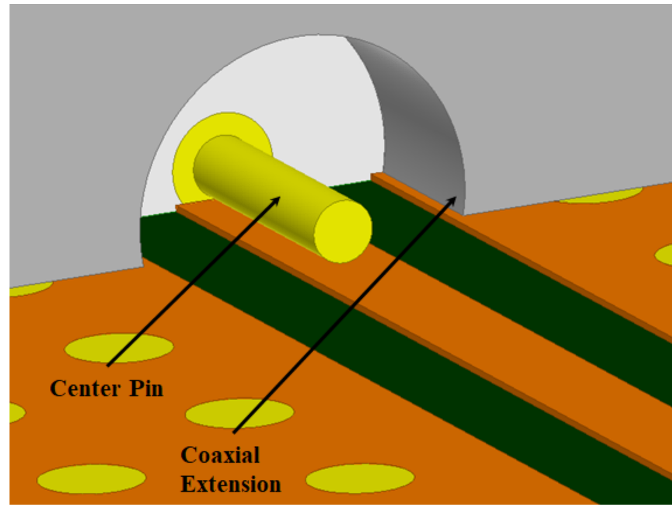


Figure 2.11: Zoom-in on the edge-launch connector transition.

brought to the edge-launch connector through an RF cable. At the edge of the board where the transition from coaxial line to the CPWG transmission line occurs, there is a center pin that extends from the edge-launch connector that sits on top of the board. This center pin increases the capacitance and must be compensated for to achieve a good 50 Ω match. Moreover, there is a slight protrusion of the coaxial line shield that extends from the connector to allow excellent mating to the CPWG ground planes. This also adds additional capacitance and must be compensated for in the design. Both the center pin transition and the coaxial extension are shown in Fig. 2.11. If the CPWG ground planes extend wider than the coaxial extension, different connector models are available to meet design demands. However, the connector model in HFSS should be modified to account for the dimension changes to ensure that the capacitance is correctly compensated. For this research, the Southwest Microwave connector used is model number 292-06A-5. The dimensions can be found in [87] and were used to model the connector in HFSS.

The easiest way to compensate for this additional capacitance is to add

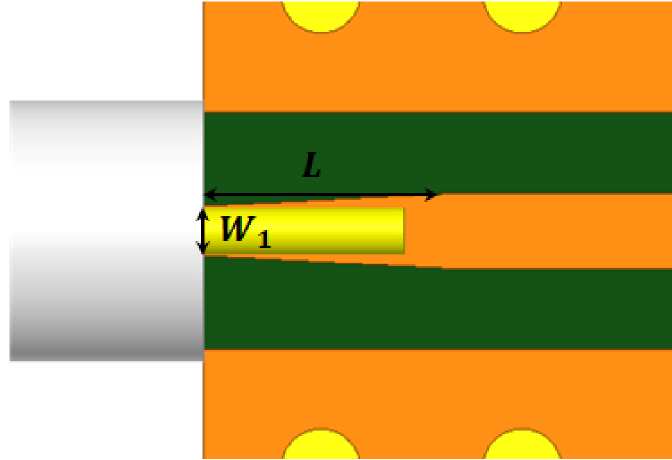


Figure 2.12: Top-down view of the CPWG taper to illustrate taper dimensions.

inductance to the design. For CPWG traces, this can be achieved by tapering the CPWG center trace along the length of the center pin [88]. Traditionally, the taper starts at the edge of the board with a width equal to the coax launch pin and then tapers out to the width of the CPWG center trace over the length of the center pin. However, to achieve the correct compensation inductance for this design, the taper would have to become narrower than the center pin. This is non-ideal as any misalignment of the center pin to the CPWG center trace could load one side of the transmission line and degrade performance. Therefore, the taper is kept slightly larger than the center pin at the edge of the board and extended beyond the length of the center pin. This provided the additional inductance necessary to completely compensate for the parasitic capacitances. Fig. 2.12 shows a zoom-in on the HFSS model around the taper. The width of the taper at the edge of the board is $W_1 = 7.4$ mil and the length of the taper is $L = 39$ mil.

Fig. 2.13 shows the HFSS model of the CPWG transmission line with the Southwest Microwave edge-launch connector. For the proposed SISL design,

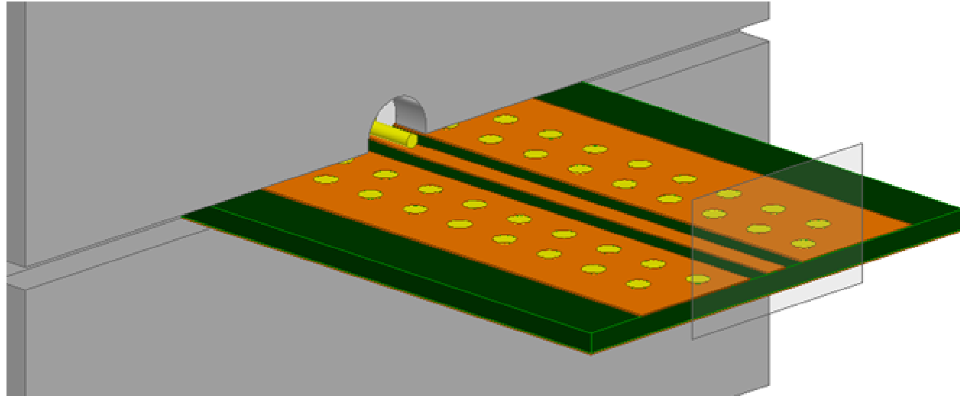


Figure 2.13: HFSS model of the CPWG transmission line with Southwest Microwave edge-launch connector.

the connector only needs to be included on one side of the transmission line. This is because one side of the board will have a connector and the other side will terminate into the vertical via transition. Assuming that the vertical via is designed to 50 ohms, a 50 ohm wave port can be placed on this end for simulation purposes. The simulated S-parameters of the CPWG transmission line with edge-launch connector are shown in Fig. 2.14.

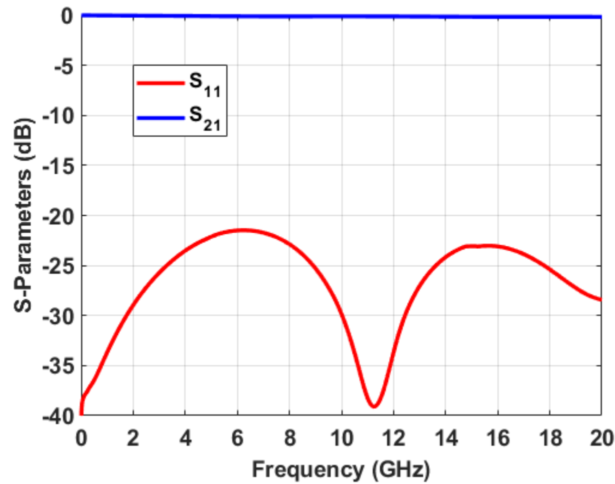


Figure 2.14: Simulated S-parameters of the CPWG transmission line with edge-launch connector and taper compensation.

2.1.3 Stripline Design

The stripline transmission line was briefly discussed in Chapter 1 and the geometry was provided in Fig. 1.5. The characteristic impedance of the stripline trace is determined by the trace width (W) and the spacing between ground planes (b). Exact design equations can be found in [18]. For the proposed SISL design, the ground plane spacing is determined by the thicknesses of substrates 2-4. Given the thicknesses in section 2.1.1, the ground plane spacing is $b = 65$ mil. The actual spacing is slightly larger due to the non-zero thickness of the pre-preg material, but is close enough for first order approximations. Similar to the CPWG transmission line, stitching vias are used to suppress parallel plate modes, which can propagate wherever the two ground planes exist. As can be seen in Fig. 2.15, a similar via stitching approach is used to suppress undesired modes. A major difference between the CPWG and stripline trace is that all of the fields are captured within the substrate material for the stripline configuration. While this minimizes radiated loss, it is crucial for the chosen

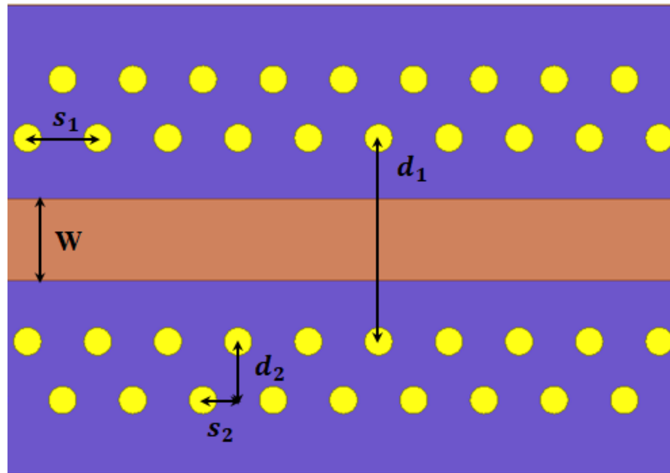


Figure 2.15: Top-down view of the stripline trace to illustrate design dimensions.

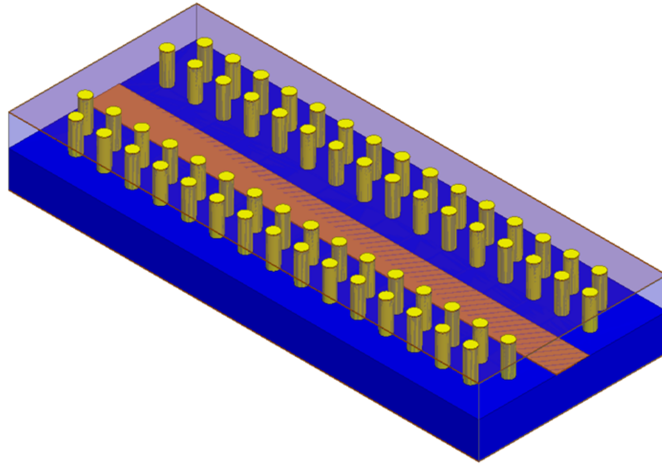


Figure 2.16: HFSS model of the stripline transmission line.

substrate to have a very small dielectric loss tangent to minimize dielectric losses. If these design rules are followed, the effective cutoff frequency can be pushed beyond the passband and a low loss and dispersion-less TEM-mode wave propagation can be achieved.

Given the material properties and thicknesses for Substrates 2-4, the stripline trace is designed. Using Keysight's ADS tool LineCalc, the width of the stripline trace is calculated to be $W = 40$ mil. The stripline trace is modeled in HFSS to fine-tune the stripline width. An image of the HFSS model is shown in Fig. 2.16. Stitching vias with a diameter of 0.3 mm are placed alongside the stripline trace with a spacing of $s_1 = 30$ mil. To avoid any half-wave resonances from occurring in the passband, the spacing between vias d_1 has to be less than 172 mil. The via spacing is $d_1 = 100$ mil. A redundant row of vias with a diameter of 0.3 mm are placed with a spacing of $d_2 = 25$ mil and an offset of $s_2 = 15$ mil. The simulated S-parameters of the stripline trace are plotted in Fig. 2.17.

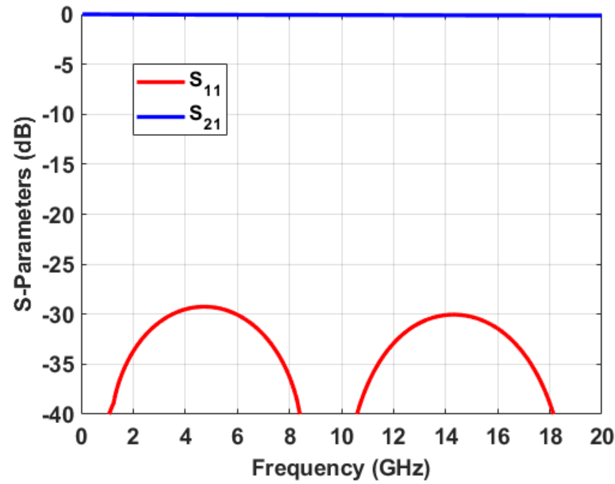


Figure 2.17: Simulated S-parameters of the stripline transmission line.

2.1.4 Vertical Via Transition Design

The CPWG-to-stripline vertical via transition is a critical part of the proposed SISL design as it provides access to the embedded SISL air cavities. Fig. 2.18 shows the HFSS model of the vertical via transition. The edge-launch connectors are included in the model, but not shown here to more clearly show the via transitions. This transition must be carefully designed to ensure a proper match is achieved across the entire passband of interest. While the CPWG

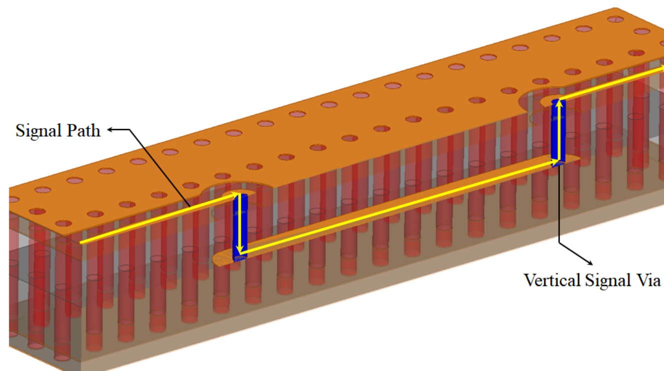


Figure 2.18: 3-D view of the CPWG-to-stripline vertical via transition.

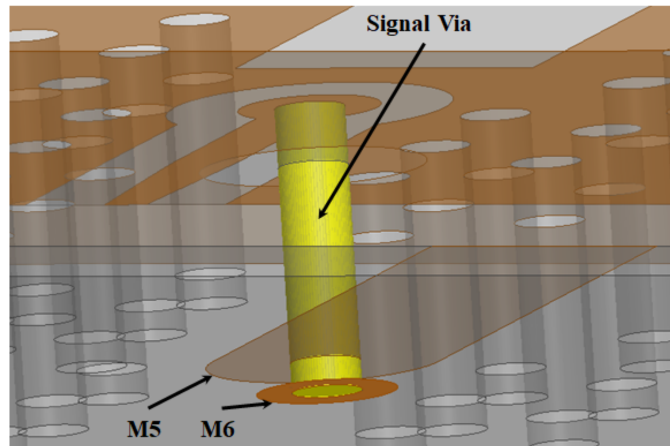


Figure 2.19: Bottom view of vertical via transition to illustrate stripline on M3 and via pad on M4.

and stripline traces have already been designed, the via pads, anti-pads, via length, and diameter must be tuned appropriately.

Before modeling the transition, the metal layer that the stripline will be implemented on needs to be decided. There are two options for the proposed SISL design, which are metal layer 5 or metal layer 6. The initial designs had the stripline on metal layer 5. Because the signal via is implemented as a blind via to avoid resonating in the passband, the signal via is drilled and plated after substrates 1-3 are laminated together. In order to make sure the via is plated properly, a via pad needs to be added on metal layer 6. This is shown in Fig. 2.19. The via pad on metal layer 6 has to be large enough to surround the signal via plus some margin for alignment error during the fabrication process. The larger this via pad becomes, the greater the parallel plate capacitance between this via pad and the stripline on metal layer 5 becomes. This additional capacitance quickly degrades the performance of the transition at higher frequencies. While the via pad could be mechanically scraped off following the via plating, concerns of cracking the via and disconnecting

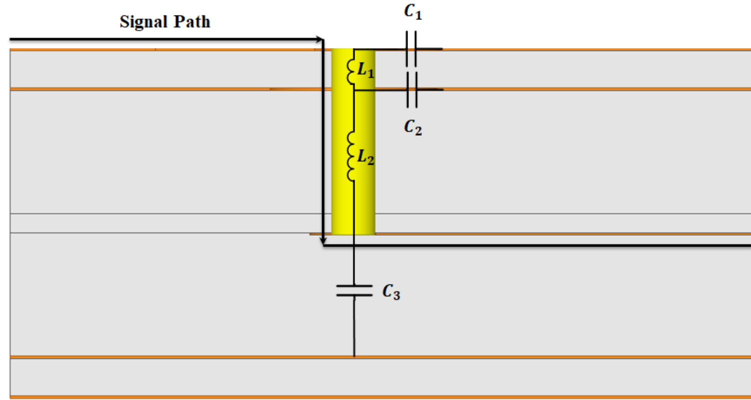


Figure 2.20: Side-view of the CPWG-to-stripline vertical via transition to illustrate the associated inductances and capacitances.

from the stripline trace made this an undesirable option. To eliminate this issue, the stripline trace is moved to metal layer 6. This approach is what will be used for the remainder of this discussion.

The vertical via transition can effectively be thought of as a lowpass filter. This is illustrated in Fig. 2.20. There is a small capacitance to ground between the via pad on metal layer 1 and the surrounding cylindrical ground plane (C_1). There is also a small capacitance between the via and the cylindrical anti-pad ground plane on metal layer 2 (C_2). The anti-pad is needed to ensure that the signal via is not shorted to the M2 ground plane. Lastly, there is a parallel plate capacitance between the bottom of the via and metal layer 9 (C_3). Moreover, the via itself can be modeled as two series inductances (L_1 & L_2). The equivalent circuit model is shown in Fig. 2.21, which is the ideal LC circuit model for a LPF. Capacitances C_1 and C_2 are calculated using [89]

$$C_i \approxeq \frac{1.41\epsilon_r T_i D_1}{D_2 - D_1}, \qquad i = 1, 2 \tag{2.2}$$

where C is the capacitance in picoFarads (pF), ϵ_r is the relative dielectric

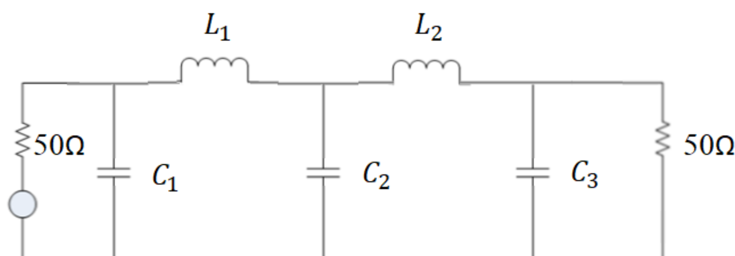


Figure 2.21: Equivalent circuit model of the vertical via transition.

constant, T is the PCB board thickness (inches), D_1 is the diameter of the via pad (inches), and D_2 is the diameter of clearance hole (inches). For the capacitance on metal layer 2, D_1 is zero since there is no via pad. C_3 is calculated using [90]

$$C_3 = \frac{\epsilon_o \epsilon_r A}{d} \tag{2.3}$$

where ϵ_o is the permittivity of free space ($8.854x10^{-12}$ F/m), ϵ_r is the relative permittivity of Substrate 4, A is the area, and d is the thickness of Substrate 4. A first order approximation for the area in (2.3) is the circular area of the via pad on metal layer 6. The series inductances of the via is calculated using [89]

$$L_i \approxeq 5.08 h_i \left[\ln \frac{4h_i}{d} + 1 \right], \qquad i = 1, 2 \tag{2.4}$$

where L is the inductance in nanoHenries (nH), h is the via length (inches), and d is the via diameter (inches).

Looking through the model libraries in Keysight's ADS, a library exists that allows for a multilayer vertical via transition to be modeled. The next step is to use this model for the vertical via transition with initial values for the pad sizes etc., and compare to the equivalent LC model. If the simulated results show good agreement, then a solution to achieve a better match can quickly be determined since the calculated inductance and capacitance values

Table 2.1: Calculated inductance and capacitance values for the vertical via transition equivalent LPF circuit model.

Capacitor	Value (pF)	Inductor	Value (nH)
C_1	0.0867	L_1	0.1212
C_2	0.0310	L_2	0.6470
C_3	0.0277		

are directly associated with a physical representation in the model. As a first attempt at the design, the signal via diameter is chosen to be 10 mil. The via pad diameter on metal layer 1 is 24 mil with a clearance of 12 mil to the cylindrical ground plane. The via anti-pad diameter on metal layer 2 is 38 mil, and the via pad diameter on metal layer 6 is 40 mil. These values along with the substrate thicknesses are used in the predefined ADS model. The calculated inductances and capacitances are provided in Table 2.1. Both the built-in multilayer vertical via transition and equivalent LC model are simulated in ADS and the simulated S-parameters are shown together in Fig. 2.22. The models show excellent agreement up to 20 GHz.

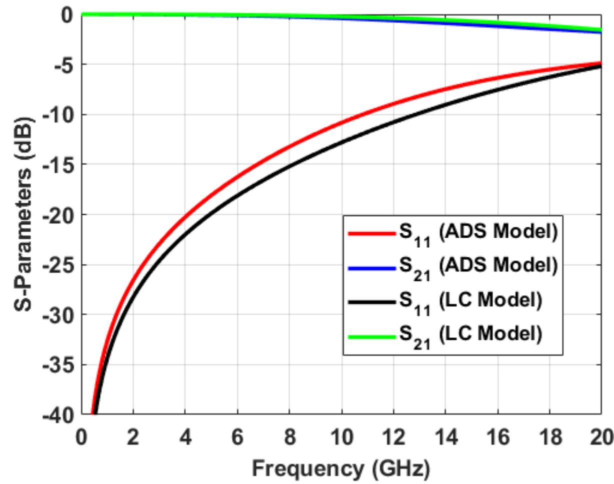


Figure 2.22: ADS simulated S-parameters comparing the ADS multilayer vertical via transition model and the LC equivalent circuit model.

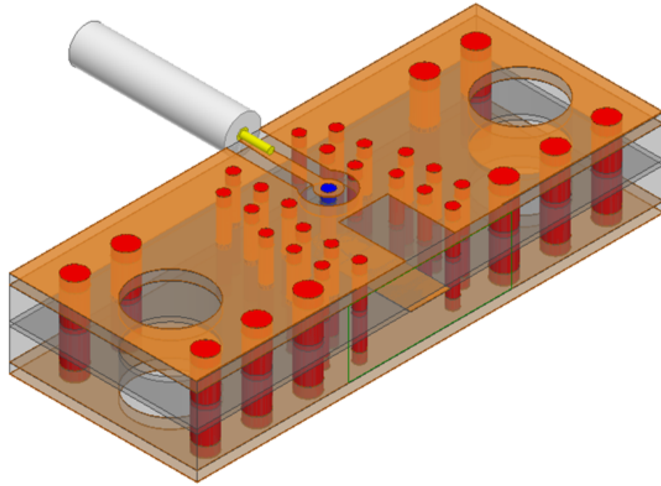


Figure 2.23: 3-D view of a single CPWG-to-stripline vertical transition modeled in HFSS.

The next step is to add the CPWG and stripline traces to the equivalent LC model and simulate the entire vertical via transition. Furthermore, the vertical via transition is modeled and simulated in HFSS to see how accurately the LC model compares to a full finite-element method electromagnetic simulation. The HFSS model of the single vertical via transition in shown in Fig. 2.23. The edge-launch connector is hidden to better show the transition. Fig. 2.24 shows the ADS LC model and HFSS simulated S-parameters plotted together. The ADS and HFSS simulations show good agreement across the 20 GHz passband. The HFSS simulation ran to a maximum delta S of 0.02 with 3 consecutive convergences for each setup. There are 5 setups each covering 4 GHz of bandwidth. The total time to simulate all 20 GHz of bandwidth and produce the plot in Fig. 2.24 is 40 minutes. The ADS simulation runs in roughly 4 seconds. This allows an incredible time savings when tuning the vertical via transition design parameters to achieve an excellent 50 ohm match.

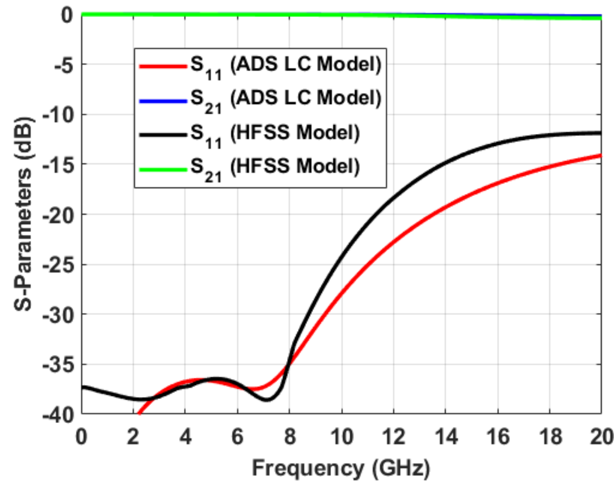


Figure 2.24: Simulated S-parameters comparing the HFSS multilayer vertical via transition model and the ADS LC equivalent circuit model with CPWG and stripline traces.

Using the ADS tuning function, the return loss is made better than 20 dB across the entire 20 GHz passband. This is accomplished by slightly decreasing the series inductance and reducing C_1 and C_2. Reducing the series inductance can be achieved by increasing the signal via diameter according to (2.4). C_1 and C_2 can be reduced by either decreasing the via pad or by increasing the clearance ring according to (2.2). The HFSS model is updated based on the ADS simulations results and then fine-tuned using a parametric sweep in the HFSS optimetrics suite. The signal via diameter is increased to 0.3 mm and the via anti-pad diameter on metal layer 2 is increased to 45 mil. The tuned ADS LC model and HFSS simulated S-parameters are shown together in Fig. 2.25. Again, the ADS and HFSS simulated S-parameters show good agreement. The S_{21} is plotted separately in Fig. 2.26 and zoomed-in to show the simulated loss across the 20 GHz passband. The greatest loss occurs at 20 GHz with a simulated insertion loss of 0.12 dB. Assuming the loss is doubled for the second via transition in the final SISL design, the insertion loss due to the

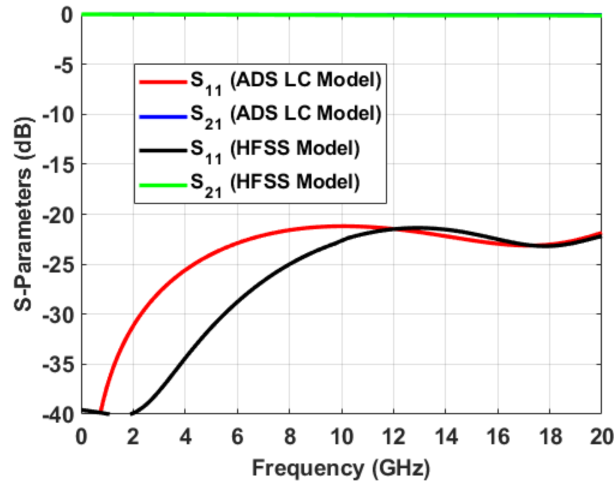


Figure 2.25: Simulated S-parameters comparing the tuned HFSS multilayer vertical via transition model and the tuned ADS LC equivalent circuit model.

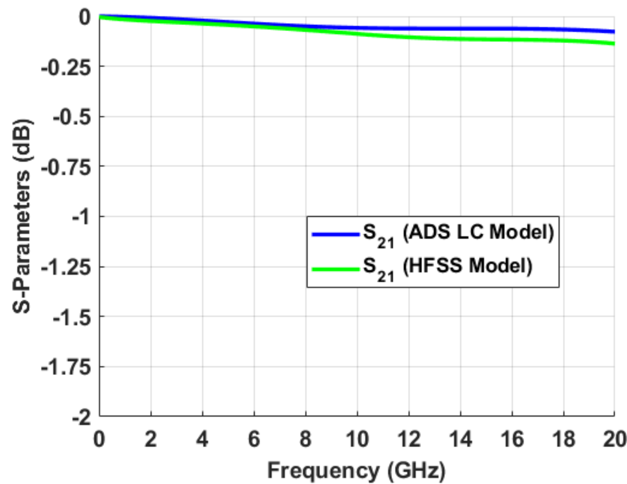


Figure 2.26: Zoomed-in view of the simulated S_{21} plots.

via transitions will be less than 0.25 dB. This is ideal since the goal of the proposed SISL design is to achieve low loss and highly integrated components designs. The vertical via transition designed in this section will be used for the DC-20 GHz SISL thru-line. Note that if the vertical via must be made shorter to reduce the series inductance, the material stack-up should be updated and the CPWG and/or stripline should be redesigned accordingly.

2.1.5 Effective Relative Permittivity & ADS Model

It is important to have a solid understanding of the SISL air cavities effective permittivity (ϵ_{eff}) when designing distributed RF/microwave components. All of the distributed length and width calculations are going to be dependent on the effective permittivity inside of the SISL air cavity. If the permittivity assumption inside of the cavity is off, the calculated dimensions will be incorrect resulting in poor component performance. For example, if the lengths of the shunt open-ended capacitor equivalent stubs are incorrect for a LPF design, the cutoff frequency will be shifted. While this issue can be corrected after modeling the design in an electromagnetic solver, the associated tuning and/or optimization process can take a long time and sometimes will not converge if a poor first order approximation is given. This is a non-ideal approach that can waste a rather significant amount of design time and should be avoided.

For the proposed SISL design, it is also important to know the effective permittivity in order to accurately model the transmission lines in ADS. There is an extremely limited number of suspended substrate models in ADS greatly limiting the ability to model complex designs and accurately simulate microwave components. However, if the effective permittivity of the entire cavity can be extracted, the stripline model in ADS can be used, which has a plethora of models. This is accomplished by setting the ground plane spacing to the same thickness as Substrates 2-4 and setting the relative dielectric constant as the effective permittivity of the cavity. The ability to model and simulate in ADS allows for rapid design verification and quick tuning abilities greatly reducing the time to design microwave components in the proposed SISL technology. Therefore, a method for extracting the effective permittivity is developed.

Initial work on calculating the effective permittivity was done shortly after the suspended stripline technology was developed. Original papers offered several numerical approaches but required solving very complicated mathematics [91]–[95]. A half a decade later, analysis equations were developed but only satisfied open SSS structures [96], [97]. In [98], closed-form equations were derived using a least-squares curve fitting method for a shielded suspended substrate microstrip line. The equations were found to be accurate within $\pm$ 2% compared to values obtained with a finite-differential method. However, there are several limitations that render this approach non-ideal for the proposed SISL design. First off, these equations were derived over 30 years ago and since then an incredible amount of research has gone into material development and PCB fabrication allowing for a wide range of dielectric constant and material thicknesses. The equations in [98] greatly limit the materials of use and therefore should be used with caution. The derived equations also assume that the suspended line is encapsulated entirely by a metal structure and therefore the fields terminate immediately at the cavity edge. The LineCalc tool in ADS will solve for k_{eff} in the suspended substrate model, but assumes the same metal cavity scheme. For the proposed SISL design, the side-wall metalization is achieved using closely spaced vias that are located slightly within the substrate. This additional substrate within the cavity will dielectrically load the cavity and increase the overall effective permittivity. Therefore, a more sophisticated approach must be taken to account for all of these nuances.

The approach used in this dissertation utilizes ADS and HFSS to extract the effective permittivity. The first step is to use ADS and simulate a basic thru-line using the available model. The ADS schematic is shown in Fig. 2.27.

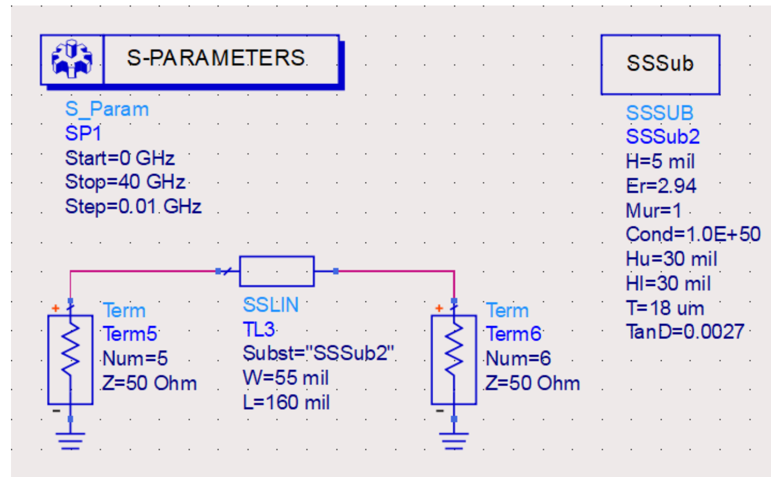


Figure 2.27: Image of the ADS suspended stripline model.

An arbitrary length and width of 160 mil and 55 mil, respectively, are chosen and modeled in ADS. Next, the simulation is ran over a frequency range from DC to 40 GHz. The simulated results are shown in Fig. 2.28. From this figure, the first deep null in the return loss happens at 34.54 GHz, which indicates that the 160 mil long thru-line is a half-wavelength at 34.54 GHz. This gives a good indication of what to expect in HFSS and limits the frequency range

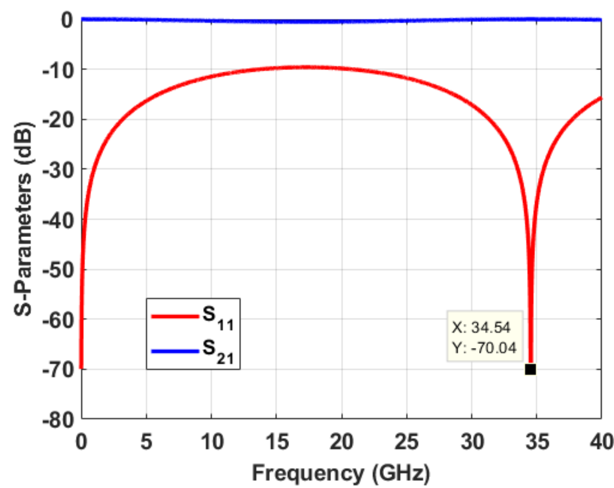


Figure 2.28: ADS simulated S-parameters of the suspended thru-line.

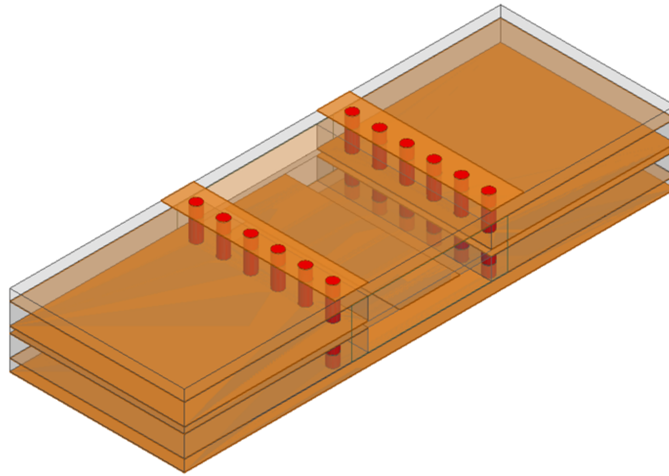


Figure 2.29: Image of the HFSS suspended stripline model.

that must be simulated in HFSS. The next step is to model the entire SISL stack-up in HFSS with a 160 mil long and 55 mil wide thru-line. An image of the HFSS model is shown in Fig. 2.29. The HFSS model is simulated over a 26 to 40 GHz frequency range. The HFSS simulated S-parameters are plotted along with the ADS simulated S-parameters in Fig. 2.30. There is a

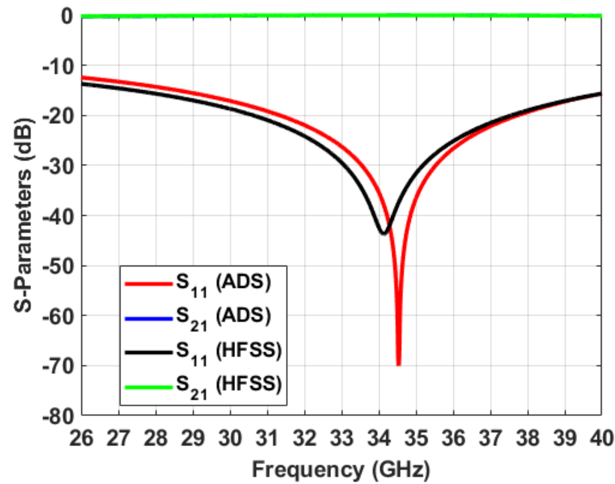


Figure 2.30: ADS and HFSS simulated S-parameters of the suspended thru-line.

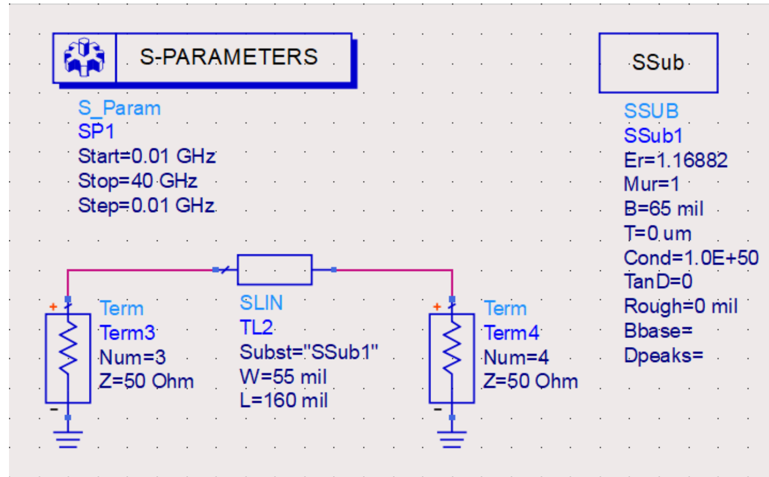


Figure 2.31: Image of the ADS stripline model.

slight shift in the return loss null indicating that the effective permittivity has changed. This result is expected since the cavity has more substrate within the air cavity due to the side-wall via design. Now, the effective permittivity of the SISL air cavity can be calculated using

$$\epsilon_{eff} = \left(\frac{c}{2 f_{\lambda/2} L} \right)^2 \tag{2.5}$$

where c is the speed of light, L is thru-line length, and $f_{\lambda/2}$ is the half-wavelength frequency determined by the HFSS simulation. The half-wavelength frequency from the HFSS simulation is 34.14 GHz. Solving (2.5) yields an effective permittivity of $\epsilon_{eff} = 1.16882$.

To verify the calculated permittivity and the modified ADS stripline model technique, the stripline model is used in ADS with the ground plane spacing set to 65 mil and the effective permittivity set to 1.16882. The ADS model is shown in Fig. 2.31. The simulated ADS stripline S-parameters are plotted with the HFSS simulated S-parameters in Fig. 2.32. As seen in Fig. 2.32, the

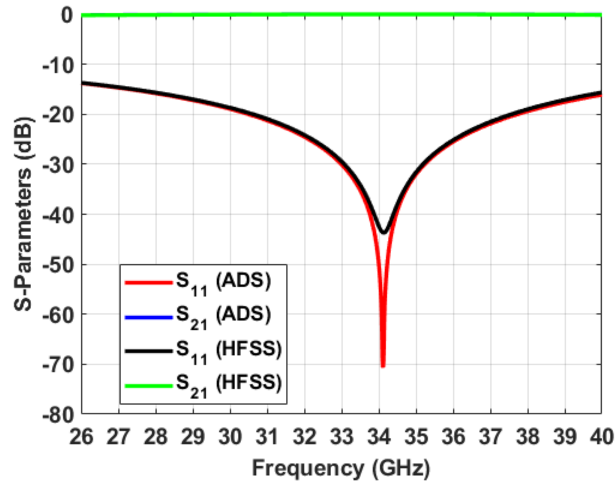


Figure 2.32: Modified ADS stripline model and HFSS simulated S-parameters.

simulated S-parameters for both the ADS and HFSS simulations align almost perfectly. This indicates that the effective permittivity extraction technique proposed if fully verified. Also, this verifies that the modified ADS stripline model can be used to model the proposed SISL design in ADS. Using the tuning feature in ADS, the width is optimized to 85 mil. The tuned ADS and HFSS simulated S-parameters are plotted together in Fig. 2.33.

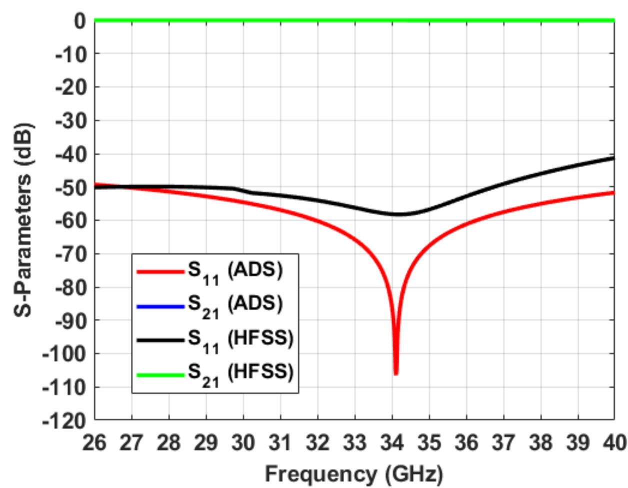


Figure 2.33: Modified ADS stripline model and HFSS S-parameters (tuned).

2.1.6 DC-20 GHz SISL Thru-Line Design

The fully-board embedded DC-20 GHz SISL thru-line can now be designed and modeled. First off, the length of the SISL thru-line is increased to 500 mil. Then, using the modified ADS stripline model for SISL, the width of the thru-line is optimized to 85 mil over the DC-20 GHz passband. Finally, the thru-line (similar to Fig. 2.29) and two vertical via transition sections (Fig. 2.23) are modeled together to form the final proposed SISL thru-line design. The exploded 3-D view of the thru-line is shown in Fig. 2.1 and a 3-D view of the final HFSS model is shown in Fig 2.34.

During this phase of the design, some thought should be given to how the final design will be built. Since this is a multi-layer PCB, pre-preg material will be used to laminate the boards together. This will inherently increase the cavity height and slightly change the effective permittivity. The DuPont Pyralux pre-preg material used has a thickness of 0.5 mil resulting in a 2.0 mil increase in the air cavity. The width is further optimized to 89 mil.

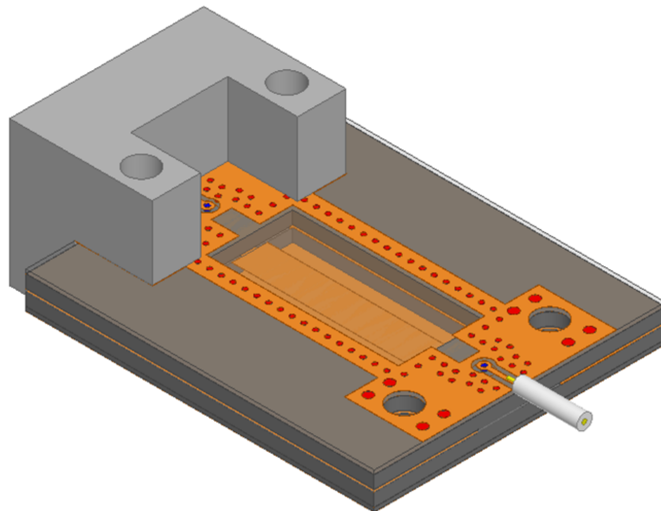


Figure 2.34: 3-D view of the proposed DC-20 GHz SISL thru-line.

2.1.7 SISL Air Cavity Tuning

The next step is to make sure that the cavity dimensions are appropriately designed to push parasitic waveguide modes beyond the passband frequency range. Analyzing the SISL air cavity, a rectangular waveguide is created by the upper and lower ground planes and the side-wall vias. Furthermore, because of the vias at the input and output of the cavity, a rectangular cavity resonance will also be excited. These concepts are illustrated in Figs. 2.35 and 2.36. In the first figure, the length and width of the cavity are defined by the center-to-center via spacing indicated as c and a, respectively. The second figure illustrates the cavity height b and a cross-hatch overlay is added to further show the waveguide cavity. These dimensions need to be kept to a minimum in order to ensure that parasitic waveguide modes can only be excited beyond the passband. If excited in the passband of interest, deep notches in the S_{21} will occur ultimately degrading performance. The goal of the proposed SISL design in to ensure only a TEM-mode propagation through the SISL air cavity.

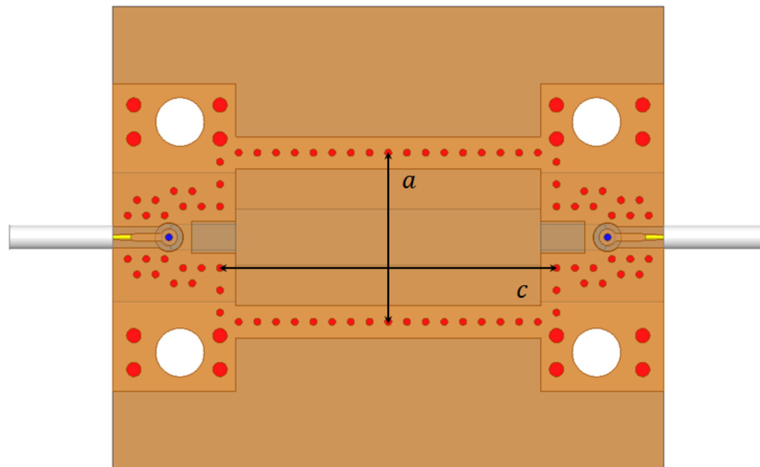


Figure 2.35: Top-down view of the proposed SISL design showing the effective rectangular waveguide structure.

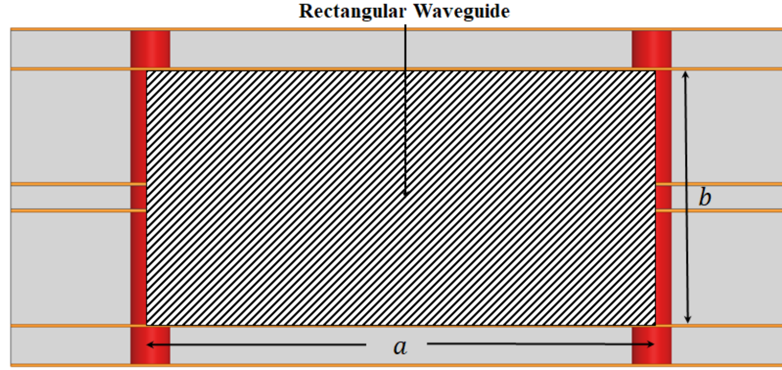


Figure 2.36: Cross-sectional view of the proposed SISL design showing the effective rectangular waveguide structure.

For most designs, the width of the cavity will become larger than the cavity height; therefore, the first parasitic waveguide mode is TE_{01}. As previously mentioned, this can be calculated using (2.1) or

$$f_c = \frac{c}{2a\sqrt{\epsilon_{eff}}} \tag{2.6}$$

where c is the speed of light and ϵ_{eff} is the effective permittivity extracted in Section 2.1.5. Using the above equation is more conservative since the effective permittivity is larger resulting in a smaller cutoff frequency. The via spacing a in the thru-line design is 250 mil, which places the waveguide cutoff frequency at 21.85 GHz. This is above the 20 GHz passband upper frequency and satisfies the design.

It is also important to make sure that the rectangular waveguide does not become a cavity resonator in the passband. In [50], if $c > a > b$, the mode with the lowest order is TE_{101} and will resonate at

$$f_{r_{101}} = \frac{c}{2\sqrt{\epsilon_{eff}}}\sqrt{\left(\frac{1}{a}\right)^2 + \left(\frac{1}{c}\right)^2} \;. \tag{2.7}$$

The via spacing along the cavity length c is 550 mil. Solving the above equation yields a resonant frequency at 23.2 GHz. Again, this is above the 20 GHz maximum passband frequency and satisfies the design.

For the given thru-line design, the via spacing a is small enough to avoid excitation of a waveguide mode in the passband, but large enough so that the field strength at the side-wall is small. Therefore, only a single row of termination vias is needed. If the spacing is reduced, a second row of vias might be necessary to terminate the fields. This can be accomplished by adding a redundant row of vias without or with an offset identical to what is done for the CPWG and stripline traces. If the fields are not appropriately terminated at the via side-wall, some of the field will couple onto the extended ground plane. This can cause two problems. The first problem is that the coupled fields will resonate on the extended ground plane with a resonant frequency determined by the board width. Second, if the design is part of an extended circuit, these coupled fields will propagate wherever the ground planes exist and can further couple into nearby circuits.

Finally, if the SISL air cavity dimensions are too large and need to be reduced, the SISL component design might need to modified to fit the new cavity size. If the cavity is significantly reduced, the new effective permittivity needs to be extracted and the modifications to the SISL design can occur. Oftentimes, the SISL component and cavity are co-designed to make sure all design criteria are met simultaneously to avoid re-designs. It is also noted that sufficient buffer should be built into the design, especially for the waveguide dimensions, to allow for fabrication tolerances. It is recommended to design with a $\pm$ 5 mil fabrication tolerance in mind.

2.2 DC-20 GHz SISL Thru-line Simulations

Now that the design has been modeled in HFSS and verification of the cavity dimensions has been completed, the HFSS model is simulated. The model uses two wave port excitations renormalized to 50 ohms since the design is intended to be used in a 50 ohm system. The 20 GHz bandwidth is broken up into 5 simulations each covering 4 GHz of bandwidth. The driven solution setup is set with a maximum delta S of 0.01 and 5 minimum converged passes. The simulated S-parameters are shown in Fig. 2.37. The simulated insertion loss is less than 0.25 dB across the entire 20 GHz passband including the connectors, vertical via transitions, and 500 mil thru-line. The return loss is better than 20 dB across the passband indicating a very good match. This match is achieved without the need for optimization because the thru-line and the vertical via transition are both designed to a 50 ohm characteristic impedance.

For direct use in microwave radar and communications applications, it is imperative for the proposed SISL technology to display linear phase, which is

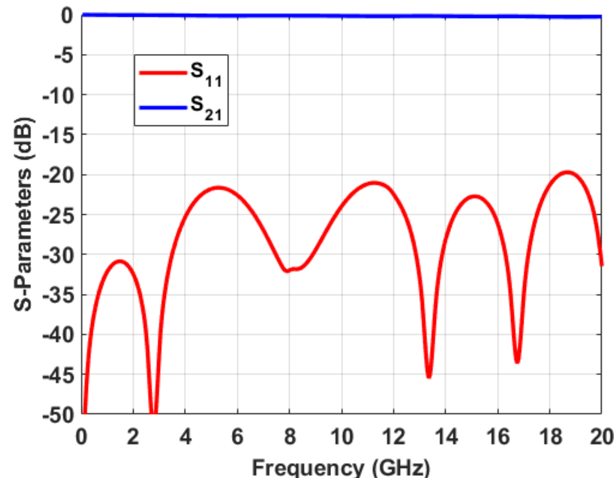


Figure 2.37: HFSS simulated S-parameters of the proposed DC-20 GHz SISL thru-line.

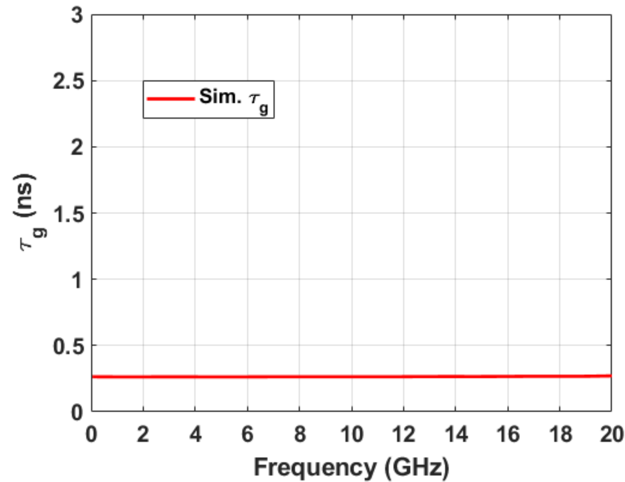


Figure 2.38: HFSS simulated group delay of the proposed DC-20 GHz SISL thru-line.

the same as having a constant group delay (τ_g). For example, in a radar system, a significant group delay that drastically varies with frequency will have a dispersive effect on the signal, which will ultimately degrade the resolution cell as well as give a false indication of the actual range to the target [99]. Fig. 2.38 plots the simulated group delay. The group delay displays very flat response with a maximum delay of 0.272 ns at 20 GHz, and an average delay of 0.265 ns.

2.3 Layout File Generation

After the design has been simulated and desired performance is achieved, the layout files are generated to fabricate the proposed SISL design. In this research, a Gerber file format is used. This is accomplished by creating a new project with the same design, but deleting the connectors, wave ports, and radiation boundaries. The model is then exported as a GDSII file. This will export all of the metal layers which are needed to generate the Gerber files.

The GDSII file is then imported into Keysight's ADS layout view and modified to its final layout. Finally the individual layers are exported as Gerber files. These Gerber files are then used to plot the photo-masks needed during the photolithography process. The Gerber files are also used by the LPKF ProtoMat S103 rapid PCB prototyping machine for drilling and milling the PCB stack-up.

2.4 Device Fabrication Procedure

Based on the final design, the proposed SISL thru-line is fabricated using a standard PCB processing procedure. To this end, Substrates 2 and 4 are first patterned using a LPKF ProtoMat S103 rapid PCB prototyping machine, to create the air cavities. Then, both of the copper layers on these two laminate substrates are completely etched off. In the next step, M1, M2, M5, and M6 are patterned using photolithography followed by an etching process. Then, substrates 1 through 3 are laminated together using a DuPont Pyralux LF-1500 acrylic adhesive pre-preg, which is ideal for bonding PTFE composite materials such as the RT/duroid® 6000 series laminate substrates. This makes sub-assembly 1 in the final stack-up.

At this point, the vertical signal via is drilled into sub-assembly 1, followed by a copper plating process. Therefore, the vertical via transition between the CPWG and stripline is formed. Even though the signal via is a blind via in its final form, it can be implemented as a through-via to alleviate aspect ratio limitations of traditionally processed blind vias. Since the copper plating process covers all of the external surfaces, M1 and M6 need to be patterned again using an etching process, unless a selective plating process is utilized. After this step, Substrates 4 and 5 are laminated to sub-assembly 1 using the

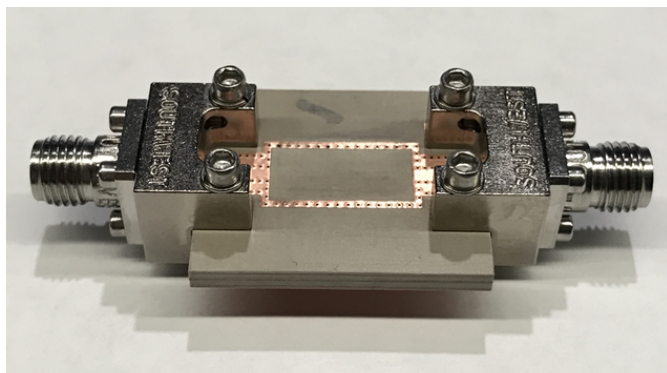


Figure 2.39: Photograph of the fabricated DC-20 GHz SISL thru-line.

same DuPont Pyralux LF-1500 adhesive. The full assembly is then drilled and copper plated to form the ground vias. At the end, M1 is etched again to create the CPWG lines. This process is followed by a cutting process, accomplished using the LPKF ProtoMat S103. Multiples of the thru-line are populated on the microwave laminate substrate stack-up to be fabricated simultaneously. Fig. 2.39 is a photograph of the fabricated fully-board embedded SISL DC-20 GHz thru-line. The overall size of the fabricated component is 2.53 x 2.16 x 0.23 cm^3. The SISL thru line itself is only 1.27 x 0.62 x 0.22 cm^3.

2.5 Measured Results

The fabricated DC-20 GHz SISL thru-line is measured using an Agilent Technologies N5225A PNA that has been calibrated to the reference plane of the edge-launch connectors using an Agilent N4691-60006 electronic calibration module. The simulated and measured S-parameters are plotted in Fig. 2.40. This is the first time demonstration of a fully-board embedded suspended integrated stripline design. Looking at the figure, the simulated and measured results show good agreement.The measured insertion loss is less than 1.1 dB

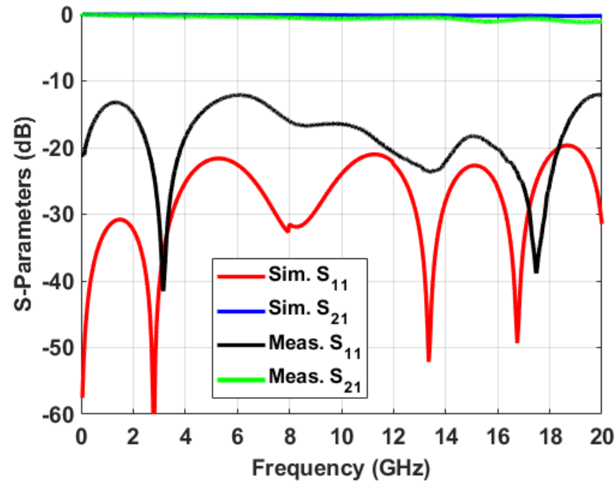


Figure 2.40: Simulated and measured S-parameters of the proposed SISL thru-line.

across the 20 GHz passband, and the measured return loss is greater than 12 dB across the passband. There is roughly 0.75 dB of additional loss compared to simulated results. In [100] and [101], it is shown that ohmic losses in the vias, reduced copper conductivity, and surface roughness can result in greater insertion loss. In HFSS, the conductivity is set to the ideal value for copper, the surface roughness it set to zero, and all of the vias are plated uniformly. The above measured thru-line is completely fabricated at the University of Oklahoma in a PCB fabrication laboratory. In [102], it is shown that the copper conductivity of the in-house plated copper is half of the ideal value. Furthermore, initial cross-sections showed some plating issues, which will increase ohmic losses. Therefore, all of the above mentioned issues are present and add to the additional loss. As far as the return loss, the overall shape and reflection zeros align very well. The degraded performance is due to the fabrication process used for the initial builds. A triple photolithography process had to be performed since a selective plating process was not used. Since this was done in-house, without a contactless photomask aligner, the alignment

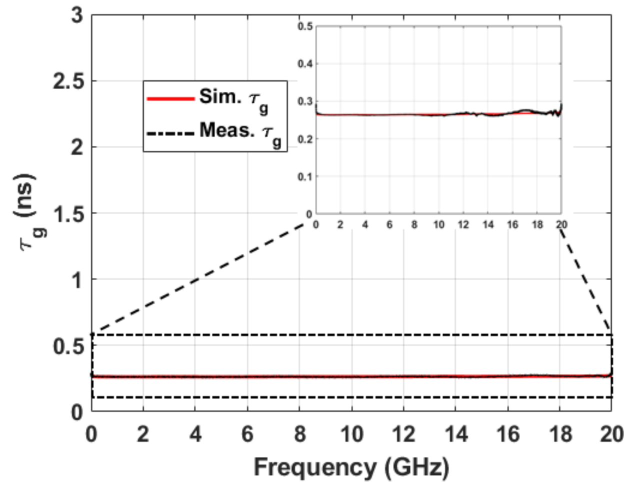


Figure 2.41: Simulated and measured group delay of the proposed SISL thru-line.

had to be done by hand. If the mask is not perfectly aligned, the CPWG trace and gap width will be wider and narrower, respectively, than designed. This causes a shift in the characteristic impedance of the line and ultimately degrades the return loss. These additional losses and degraded match can be alleviated in future builds by outsourcing the circuit fabrication.

The group delay through the thru-line is also measured and plotted with the simulated group delay in Fig. 2.41. Again, these results show very good agreement. The measured group delay is exceptionally small across the entire passband reaching a maximum of only 0.3 ns at 20 GHz. The group delay is also extremely flat with an average delay of 0.265 ns.

For this research, the edge-launch connectors are used simply for testing purposes. In an extended circuit board, the input/output CPWG traces will connect to the previous/next component in the design. Therefore, the connectors will not be needed and the additional associated losses can be ignored. Additionally, the CPWG traces will not need to be tapered and testing can be accomplished with a ground-signal-ground RF probing station.

Chapter 3

Suspended Integrated Stripline Lowpass Filter

The purpose of this chapter is to apply the fully-board embedded SISL technology to the design of microwave distributed lowpass filters. This chapter will derive necessary design equations and offer several design guidelines to realize wideband lowpass filters in the SISL technology. An eleventh-order generalized Chebyshev DC-18 GHz LPF is used as a technology demonstrator. This design example is chosen to demonstrate low loss, wide band, and high frequency capabilities of the SISL technology for filter applications. The end result is a first time demonstration of a fully-board embedded SISL lowpass filter design and first time demonstration of a self-packaged suspended line filter design with frequency capability up to Ku-band.

3.1 SISL LPF Design

Fig. 3.1 shows the exploded view of the proposed LPF using the fully-board embedded SISL technology. The PCB stack-up is identical to the one used for the DC-20 GHz thru-line in Section 2.1.1. Because the passband of the LPF is less than the thru-line, the same stack-up can be used with no modifications to the vertical via transitions; therefore, the SISL thru-line section can be replaced by the SISL LPF. Another reason the same stack-up is used is to

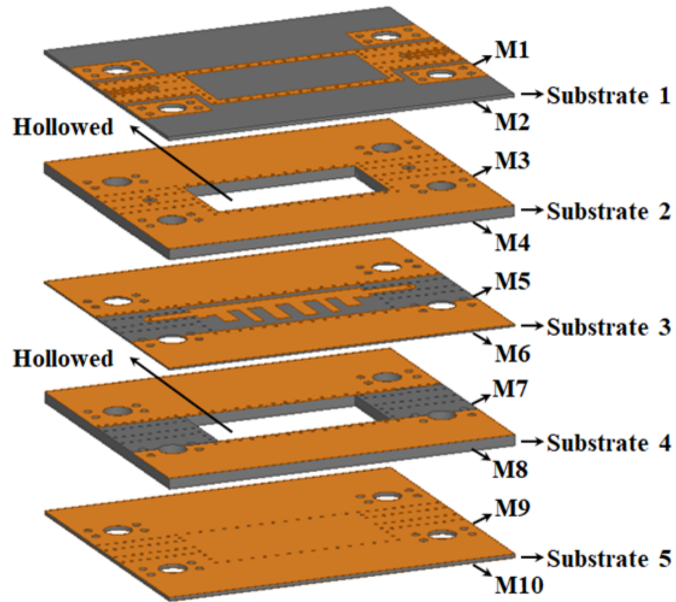


Figure 3.1: 3-D exploded view of the proposed SISL generalized Chebyshev LPF.

allow for multiple designs to be arrayed on the same PCB panel and fabricated at the same time.

Assuming the vertical via transitions are already designed, the remaining design procedure is completed as follows:

1. Choose the cutoff frequency, filter type, and filter order.

2. Model and simulate the ideal LC circuit model to verify filter performance.

3. Model the SISL air cavity and extract the effective permittivity using HFSS (discussed in Section 2.1.5).

4. Calculate the distributed lengths and widths for the LC equivalent transmission line components using the extracted effective permittivity.

5. Using the modified ADS stripline configuration from Section 2.1.5, model the filter and simulate to verify the distributed filter performance.

6. Model the filter design in an electromagnetic simulator and compare simulated results to the modified ADS model.

7. Fine-tune for optimal filter performance in ADS and then update electromagnetic simulator model and simulate to verify performance.

8. Place the design between two vertical via transitions and tune the cavity dimensions to ensure excitation of parasitic waveguide modes occurs above the filter cutoff frequency (might require fine-tuning of the SISL component design).

9. Simulate the final SISL design to make sure the via transitions have minimum affect on the final design.

10. Generate layout files from HFSS model.

After the design procedure is completed and final simulations are ran, the device is ready for fabrication. The same fabrication procedure used for the SISL thru-line, discussed in Appendix A, is used for fabrication of the SISL LPF. The filters are then connectorized and connected to a calibrated PNA for S-parameter measurements.

The next several subsections will go into fine details for each given step of the design procedure above except for step 3, which has already been discussed in detail. This will be done for the design of a DC-18 GHz SISL LPF. This LPF design in chosen to illustrate the wide bandwidth and low loss capabilities of the SISL technology. Furthermore, the end goal is to develop a 2-18 GHz cascaded BPF, which requires the above mentioned filter. The following design procdure is accomplished using Keysight ADS and ANSYS HFSS software.

3.1.1 Filter Characteristics

The cutoff frequency (f_c) of choice is dependent on the design application. The end goal of this dissertation is to design a 2-18 GHz BPF to be used in the next generation 2-18 GHz FMCW radar discussed in [11], [46], [49], [103]. Because of the 16 GHz bandwidth, a cascaded BPF is required to meet the design criteria, which is why the cutoff frequency for the LPF designed in this chapter is $f_c = 18$ GHz. The new system will be integrated onto a single PCB that can be placed directly behind each antenna element. This requires the previously designed SSS filters to be replaced with the proposed SISL filters to meet SWaP requirements.

The filter type is also dependent on the design application. For any radar or communications application, it is necessary for the filter type to have excellent selectivity, be capable of broadband performance, and achieve linear phase. The selectivity is needed to ensure that the frequency band of interest is passed while greatly attenuating near band signals. The generalized Chebyshev lowpass prototype developed in [23] satisfies a generalized Chebyshev response with an equiripple passband, three transmission zeros at infinity, and the remainder at a finite frequency close to the cutoff frequency. The generalized Chebyshev lowpass prototype filter is shown in Fig. 3.2. This prototype

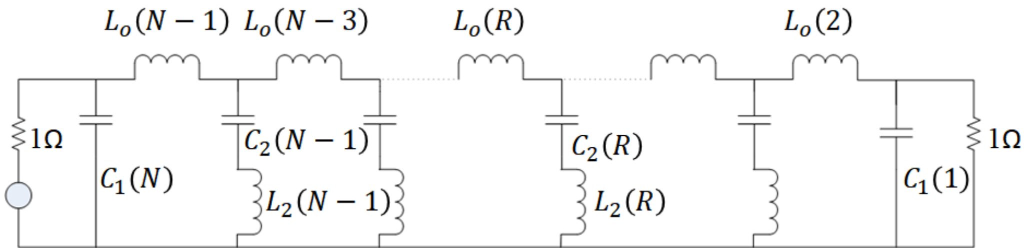


Figure 3.2: Generalized Chebyshev LPF prototype filter having 3 transmission zeros at infinity and (N-3) at a finite frequency.

produces a highly selective filter compared to other prototypes with only a single transmission zero at infinity [104]. Its selectivity is very close to that of an elliptic filter, but can achieve very flat group delay in the passband due to its inherent Chebyshev response. Furthermore, it is easier to realize and fabricate since it has an impedance variation of 2:1 versus 10:1 of a more traditional elliptic filter. This is ideal as impedance variations increase with bandwidth, which is large for the current design.

The generalized Chebyshev element values for different order (N) filters are solved for using the alternating-pole technique [23]. Furthermore, the normalized frequency where ($N-3$) transmission zeros occur (ω_o) and the normalized bandedge frequency (ω_1) are solved for using a Newton-Raphson technique and are also provided for different N. The former frequency is used when calculating the distributed line lengths and the latter frequency is used to determine the filter order. A design chart is provided to help determine the filter order needed to achieve the desired filter performance. The design criteria for the 18 GHz LPF is to have 20 dB of return loss across the entire passband and 50 dB of insertion loss by 20 GHz. Given these design parameters, an eleventh-order ($N = 11$) filter is needed to meet the design goals. A LPF prototype with corresponding elements for an eleventh-order filter is shown in Fig. 3.3. The element values and normalized frequencies for the eleventh-order generalized

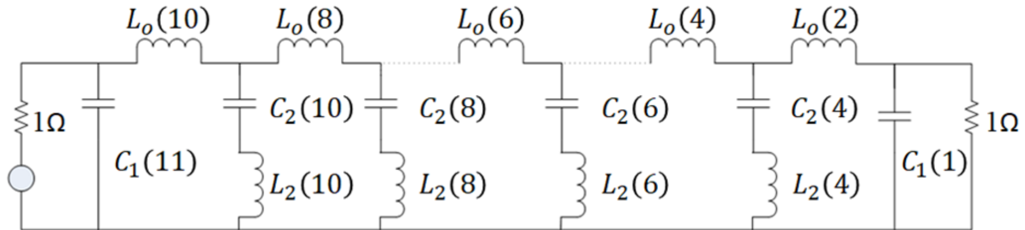


Figure 3.3: Generalized Chebyshev LPF prototype for an eleventh-order filter.

Table 3.1: Calculated element values for an eleventh-order generalized Chebyshev LPF prototype using an alternating-pole technique [23].

N = 11		**R.L. > 20 (dB)**
R	**Element**	**I.L. > 50 (dB)**
11	$C_1(11)$	1.04297
10	$L_0(10)$	0.935065
	$L_2(10)$	0.984313
	$C_2(10)$	0.787121
8	$L_0(8)$	0.786767
	$L_2(8)$	0.794605
	$C_2(8)$	0.975041
6	$L_0(6)$	0.807267
	$L_2(6)$	0.794605
	$C_2(6)$	0.975041
4	$L_0(4)$	0.786767
	$L_2(4)$	0.984313
	$C_2(4)$	0.787121
2	$L_0(2)$	0.935065
1	$C_1(1)$	1.04297

Chebyshev LPF prototype are shown in Table 3.1 and Table 3.2, respectively. Note that the LPF prototype is symmetrical about the center inductor $L_0(6)$. For any odd order generalized Chebyshev prototype, the design will be symmetrical about the center inductor. The element values and ω_o are used in Sections 3.1.2 and 3.1.3 to develop the ideal LC circuit model and calculate the distributed lengths and widths, respectively.

Table 3.2: Calculated normalized frequencies using an iterative Newton-Raphson technique [23].

		R.L. > 20 (dB)
Order	**Frequency**	**I.L. > 50 (dB)**
11	ω_o	1.13609
	ω_1	1.06853

3.1.2 Ideal LC Model

The ideal LC model can be built in ADS after a frequency and impedance scaling is performed using the element values and the cutoff frequency from Section 3.1.1. The capacitor values are calculated using

$$C = \frac{C_n(R)}{R_o \omega_c} \tag{3.1}$$

where R_o is the impedance of the system, $C_n(R)$ are the element values from Table 3.1, and ω_c is the cutoff frequency in rad/sec. The cutoff frequency (ω_c) is solved for using

$$\omega_c = 2\pi f_c \tag{3.2}$$

where f_c is the cutoff frequency in Hz. The inductor values are calculated using

$$L = \frac{R_o L_n(R)}{\omega_c} \tag{3.3}$$

Table 3.3: Calculated inductance (nH) and capacitance (pF) values for the ideal LC circuit model.

N = 11	**R.L. > 20 (dB)**		**I.L. > 50 (dB)**	
R	**Capacitor**	**(pF)**	**Inductor**	**(nH)**
11	$C_1(11)$	0.184438		
10	$C_2(10)$	0.139194	$L_0(10)$	0.413389
			$L_2(10)$	0.435162
8	$C_2(8)$	0.172425	$L_0(8)$	0.347827
			$L_2(8)$	0.351293
6	$C_2(6)$	0.172425	$L_0(6)$	0.356890
			$L_2(6)$	0.351293
4	$C_2(4)$	0.139194	$L_0(4)$	0.347827
			$L_2(4)$	0.435162
2			$L_0(2)$	0.413389
1	$C_1(1)$	0.184438		

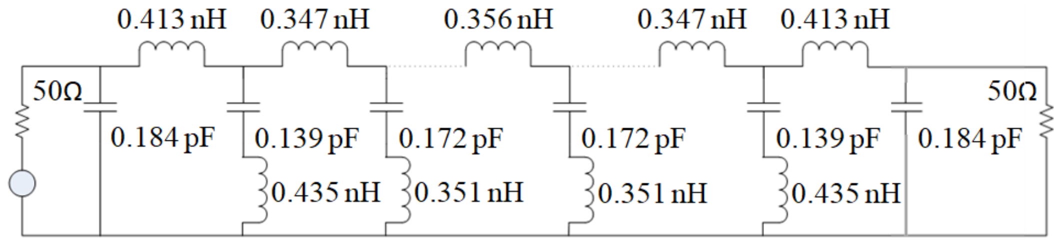


Figure 3.4: Generalized Chebyshev LPF prototype for an eleventh-order filter with calculated inductance and capacitance values.

where $L_n(R)$ are the element values form Table 3.1. Using these equations, the inductance and capacitance values for the ideal LC circuit model can be calculated and are shown in Table 3.3. The eleventh-order generalized Chebyshev prototype with calculated values is provided in Fig. 3.4. This LC circuit model is built in ADS and simulated to verify the calculated values and the filter performance. The simulated S-parameters are shown in Fig. 3.5. The cutoff frequency is right at 18 GHz with a return loss greater than 20 dB across the passband and greater than 50 dB of insertion loss at 20 GHz.

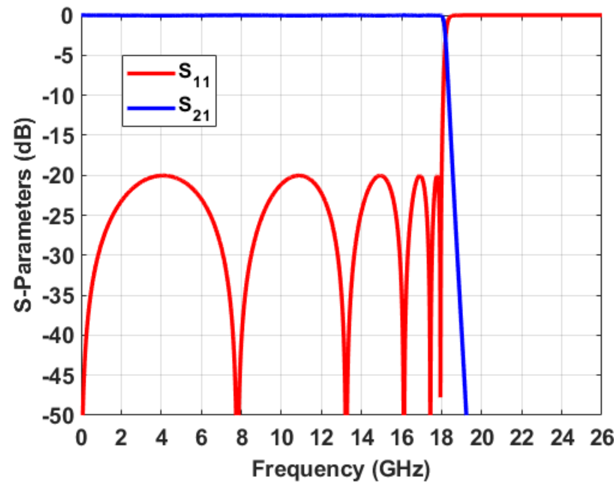


Figure 3.5: ADS simulated S-parameters of the eleventh-order Generalized Chebyshev ideal LC circuit model.

3.1.3 Distributed LPF Design Equations

Now that the ideal LC circuit model is verified, it is time to realize the filter. Unfortunately, no available inductors or capacitors exist with these small of values with self-resonant frequencies beyond the cutoff frequency. Therefore, the filter will need to be converted from its current lumped element design to a distributed design using LC equivalent transmission lines. This is accomplished using basic circuit theory and Richard's Transformation expressed as [18]

$$\begin{aligned} s &= j\omega_o \tan(a\omega) \\ &= \omega_o \tanh(sa) \end{aligned} \tag{3.4}$$

where s is the complex frequency variable and a is a constant.

The equivalent transmission line model for the shunt LC circuit is derived first. The input admittance (Y_{in}) of the shunt section is solved for as

$$Y_{in} = \frac{sC_2(R)}{s^2 L_2(R) C_2(R) + 1} \tag{3.5}$$

where $C_2(R)$ and $L_2(R)$ are the capacitance and inductance values, respectively, from Table 3.1. The input admittance can be written as

$$Y_{in} = \frac{sC_2(R)}{1 + s^2/\omega_o^2} \tag{3.6}$$

where ω_o is the resonant frequency of the shunt section

$$L_2(R)C_2(R) = \frac{1}{\omega_o^2} \quad . \tag{3.7}$$

Applying Richard's Transformation, the input admittance is re-written as

$$\begin{aligned} Y_{in} &= \frac{C_2(R)\omega_o \tanh(sa)}{1 + \frac{(\omega_o \tanh(sa))^2}{\omega_o^2}} \\ &= \frac{C_2(R)\omega_o \tanh(sa)}{1 + \frac{\omega_o^2 \tanh^2(sa)}{\omega_o^2}} \\ &= \frac{C_2(R)\omega_o \tanh(sa)}{1 + \tanh^2(sa)} \\ &= \frac{C_2(R)\omega_o \tanh(2sa)}{2} \\ &= \frac{jC_2(R)\omega_o \tan(2\omega a)}{2} \quad . \end{aligned} \tag{3.8}$$

The admittance for a shunt open-circuit stub is

$$\begin{aligned} Y &= jY_o \tan(\beta l) \\ &= jY_o \tan\left(\frac{\omega l}{v}\right) \end{aligned} \tag{3.9}$$

where l is the length of the shunt open-circuit stub and v is the velocity of propagation. Equations (3.8) and (3.9) are equated together to obtain

$$Y_o \tan\left(\frac{\omega l}{v}\right) = C_2(R)\omega_o \cdot \frac{\tan(2\omega a)}{2} \tag{3.10}$$

which indicates that the shunt LC circuit can be realized as a distributed shunt open-circuit stub. The characteristic impedance of the Rth stub is

$$Z_o = \frac{2}{\omega_o \cdot C_2(R)} \tag{3.11}$$

which is extracted from (3.10). Equating the tangent arguments results in

$$a = \frac{l}{2v} \quad . \tag{3.12}$$

Equation (3.4) can be rearranged to yield

$$\Omega = \frac{\omega}{\omega_o} = \tan(a\omega) = \tan(2\pi f a) \tag{3.13}$$

and is further simplified to

$$\Omega = \frac{1}{\omega_o} = \tan(2\pi f_c a) \tag{3.14}$$

when evaluated at the cutoff frequency. Inserting (3.12) into (3.14), the physical length of each stub can be solved for as

$$\begin{aligned} \arctan\left(\frac{1}{\omega_o}\right) &= 2\pi f_c \cdot \left(\frac{l}{2v}\right) \\ l &= \frac{v}{\pi f_c} \arctan\left(\frac{1}{\omega_o}\right) \end{aligned} \tag{3.15}$$

hence

$$l_{shunt\ inner\ stub} = \frac{c}{\pi f_c \sqrt{\epsilon_{eff}}} \arctan\left(\frac{1}{\omega_o}\right) \tag{3.16}$$

where c is the speed of light and ϵ_{eff} is the effective relative permittivity. For the proposed SISL design, the effective permittivity is determined by the air cavity and the extraction technique is discussed in Section 2.1.5. The ω_o variable is from Table 3.2 to ensure that the transmission zeros occur near the bandedge to provide excellent selectivity.

Now that the length of the shunt open-circuit stub is known, the next step is to derive a solution to calculate the width. Because the proposed SISL design is based on the stripline technology, stripline design equations can be modified to fit our needs. From microwave engineering, it is known that the characteristic impedance of a lossless TEM-mode stripline transmission line is

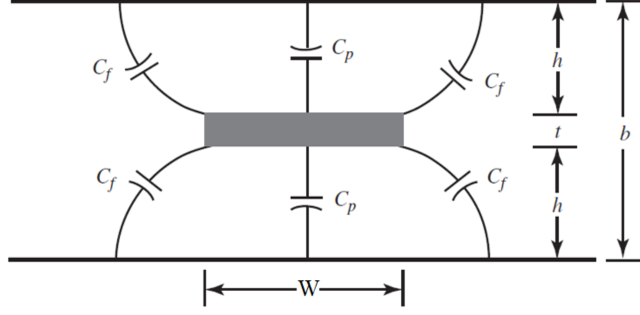


Figure 3.6: Capacitance model for the proposed SISL transmission line [50].

related to the static capacitance to ground as

$$Z_o\sqrt{\epsilon_r} = \frac{\eta_o}{(C_t/\epsilon)} \tag{3.17}$$

where $\eta_o = 120\pi$ and the total capacitance C_t/ϵ is composed of the parallel plate capacitance C_p/ϵ and the fringing capacitance C_f/ϵ all per unit length. For the proposed SISL design, this can be rewritten as

$$Z_o\sqrt{\epsilon_{eff}} = \frac{\eta_o}{(C_t/\epsilon)} \tag{3.18}$$

where the permittivity is the effective permittivity of the air cavity.

Fig. 3.6 shows the capacitance model of the proposed SISL transmission line. The total capacitance can then be calculated as

$$\frac{C_t}{\epsilon} = \frac{2C_p}{\epsilon} + \frac{4C_f}{\epsilon} \tag{3.19}$$

since all of the capacitances are in parallel. The parallel plate capacitance can be calculated using

$$\frac{C_p}{\epsilon} = 2 \cdot \frac{W/b}{1 - t/b} \tag{3.20}$$

where W and t are the width and thickness of the transmission line, respectively, and b is total SISL air cavity height. The fringing capacitance for an isolated bar was originally published in [105] and later confirmed with and even- and odd-mode analysis in [106]. The approximation for the fringing capacitance can be calculated using

$$\frac{C_f}{\epsilon} \approx \frac{1}{\pi}\left\{\frac{2}{1-t/b}\ln\left(1+\frac{1}{1-t/b}\right)-\left(\frac{1}{1-t/b}-1\right)\ln\left[\frac{1}{\left(1-t/b\right)^2}-1\right]\right\} \tag{3.21}$$

which reduces to

$$\frac{C_f}{\epsilon} \approx \frac{1}{\pi}[2\ln(2)] = 0.4413 \tag{3.22}$$

for zero-thickness center conductor ($t = 0$). Inserting (3.19) into (3.20) yields

$$\frac{C_t}{\epsilon} = \frac{4W}{b-t} + \frac{4C_f}{\epsilon} \quad . \tag{3.23}$$

Substituting (3.23) into (3.18), the relationship between the characteristic impedance and the width is obtained. Solving for the width gives

$$W = \frac{b-t}{4}\left(\frac{\eta_o}{Z_o\sqrt{\epsilon_{eff}}} - 4\cdot\frac{C_f}{\epsilon}\right) \quad . \tag{3.24}$$

Impedance scaling the expression in (**??**) to 50 ohms terminations, then substituting into (3.24), the physical width of each stub can be solved for as

$$W = \frac{b-t}{4}\left(\frac{1.2\pi\omega_o C_2(R)}{\sqrt{\epsilon_{eff}}} - 4\cdot\frac{C_f}{\epsilon}\right) \tag{3.25}$$

where $C_2(R)$ and ω_o come from Tables 3.1 and 3.2, respectively.

The shunt capacitive stubs are responsible for two of the three transmission

zeros at infinity. From [23], the length of the shunt outer stubs are half the length of the shunt inner stubs. This is simply calculated as

$$l_{shunt\ outer\ stub} = \frac{l_{shunt\ inner\ stub}}{2} \quad . \tag{3.26}$$

The width of the shunt outer stubs is calculated the same way as the inner stubs, but $C_2(R)$ is replaced with $C_1(R)$. Therefore, using equations (3.16), (3.26), and (3.25), the physical length and widths of the shunt open-circuit stubs can be calculated.

The last part of the LPF prototype to solve is the series lumped inductors. The distributed network for the series inductors is a series short circuit stub. The equivalent circuit for a length of transmission line is a π-network. Dimensions for the series line can be derived by equating the series impedance of the π-network with the series short circuit stub. The impedance of the short circuit stub is solved for using a Richards Transformation and given as

$$Z = jL_o(R)\omega_o \cdot \tan\left(\frac{\omega_c l_s}{v}\right) \tag{3.27}$$

where $L_o(R)$ is from Table 3.1 and l_s is the length of the short circuit stub. For a quarter-wavelength line, l_s equates to one-half the length described in (3.16) and simplifies the above equation to

$$\begin{aligned} Z &= jL_o(R)\omega_o \cdot \tan\left(\frac{2\pi f_c}{v} \cdot \frac{v}{2\pi f_c} \cdot \arctan\left(\frac{1}{\omega_o}\right)\right) \\ &= jL_o(R) \quad . \end{aligned} \tag{3.28}$$

The series impedance of the π-network is

$$Z = jZ_L \sin\left(\frac{\omega_c l_L}{v}\right) \tag{3.29}$$

which can be be simplified using the small angle approximation to

$$Z \approxeq jZ_L \cdot \frac{2\pi f_c l_L}{v} \tag{3.30}$$

where Z_L is the normalized characteristic impedance of the series element and l_L is the physical length of the inductive line. Equations (3.28) and (3.30) are equated together to derive the length equation as

$$l_L = \frac{L_o(R)}{Z_L} \cdot \frac{c}{2\pi f_c \sqrt{\epsilon_{eff}}} \quad . \tag{3.31}$$

Z_L must be known prior to solving for the length, which can be calculated by substituting $Z_o = Z_t erm \cdot Z_L$ into (3.24), where Z_{term} is the termination impedance, and rearrange to get

$$Z_L = \frac{120\pi}{4 \cdot Z_{term}\sqrt{\epsilon_{eff}}\left(\frac{W_L}{b-t} + 4 \cdot \frac{C_f}{\epsilon}\right)} \tag{3.32}$$

where W_L is the width of the inductive line. Lastly, the width must be known prior to solving (3.32). This width can arbitrarily be chosen but is approximated using the characteristic impedance equation of a 50 ohm stripline trace to minimize both capacitance error and filter size. The stripline equation in [107] is modified substituting the extracted effective relative permittivity from

HFSS and ignoring trace thickness to yield

$$W_L = \frac{1.9 \cdot b}{0.8e^{\frac{5\sqrt{\epsilon_{eff}}}{6}}} \tag{3.33}$$

where b is the total SISL air cavity height. Equation (3.33) should be solved separately to find the width of the inductive line. However, a single equation is compiled to solve for the length of the inductive line by combining equations (3.31), (3.32), and (3.33) and is expressed as

$$l_L = \frac{Z_{term} \cdot L_o(R)}{30\pi} \cdot \left[\frac{2.375 \cdot b \cdot e^{\frac{-5\sqrt{\epsilon_{eff}}}{6}}}{b - t} + \frac{C_f}{\epsilon} \right] \cdot \frac{c}{2\pi f_c} \quad . \tag{3.34}$$

Therefore, using equations (3.33) and (3.34), the physical length and widths of the series short circuit stubs can be calculated.

All of the design equations needed to fully-realize a distributed LPF [(3.16), (3.25), (3.33), and (3.34)] are derived and can now be used to calculate the physical lengths and widths. Step 3 of the LPF design process is skipped since it was already done for the SISL thru-line, but recall that the effective permittivity is 1.16882 for the given material stack-up. Moreover, all material layers contain 1/2 oz. copper making the thickness variable $t = 0.708661$ mil. Lastly, the filter is designed for a 50 ohm system; therefore, $Z_{term} = 50$ ohms. The LPF layout representation and calculated distributed parameters are shown in Fig. 3.7 and Table 3.4, respectively.

In Fig. 3.7, notice the symmetry about the center trace. This symmetry is convenient as it halves the number of variables during the tuning process. For the eleventh-order filter, the width of all the series inductors is the same greatly reducing the number of variables and tuning complexity. Therefore, the entire design can be tuned with just 9 variables ignoring l_0. The feed

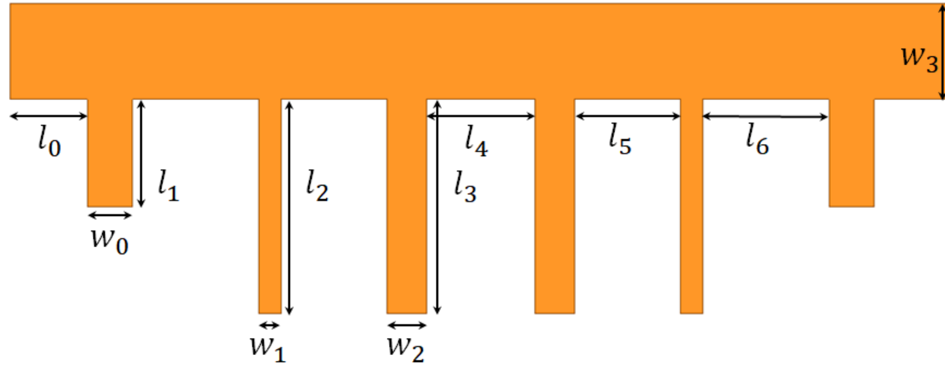


Figure 3.7: Layout representation of the distributed generalized Chebyshev LPF.

Table 3.4: LPF calculated distributed prototype parameters.

Variable	Length (mil)	Variable	Length (mil)
w_0	36.64	w_1	20.35
w_2	32.32	w_3	62.71
l_0	40	l_1	69.72
l_2	139.44	l_3	139.44
l_4	64.33	l_5	62.70
l_6	74.52		

line length designated as l_0 is ideally zero. However, some length needs to be added to the input and output to make sure the filter is not shorted to the surrounding ground plane in the final SISL design.

3.1.4 ADS and HFSS Simulations of the SISL LPF

The eleventh-order generalized Chebyshev LPF is built in ADS, using the modified stripline model, and simulated to verify the design equations and distributed filter performance. The first ADS simulation uses the stripline open-circuited stub (SLOC) model for the shunt stubs; thereby, ignoring the open-ended edge effect. The ADS simulated S-parameters are shown in Fig. 3.8.

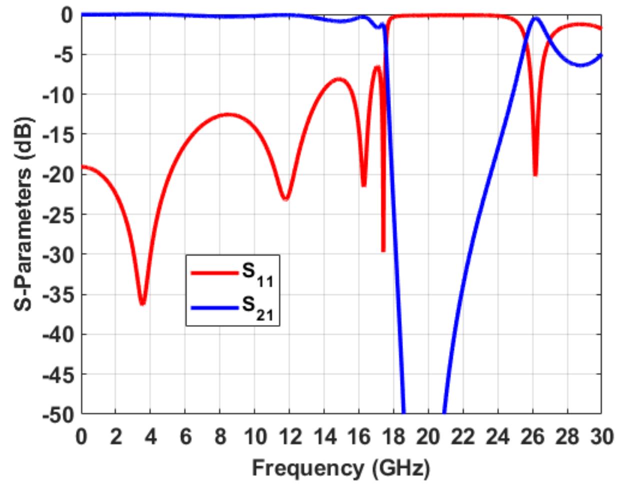


Figure 3.8: ADS simulated S-parameters of the Chebyshev LPF ignoring open-circuit edge effects (calculated values).

The cut-off frequency is very close to the desired 18 GHz cutoff and the match of the LPF is less than 10 dB up to 14 GHz, but then quickly degrades. This degradation in the match for super wideband filters is due to the length of the shunt outer stubs. Before the LPF is tuned, it is modeled in HFSS, shown in Fig. 3.9, and simulated to compare with the ADS simulation.

Fig. 3.10 plots the ADS and HFSS simulated S-parameters of the Cheby-

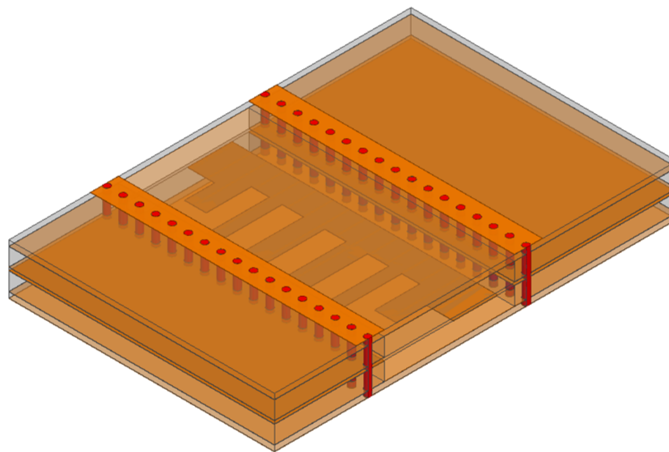


Figure 3.9: 3-D view of the LPF HFSS model.

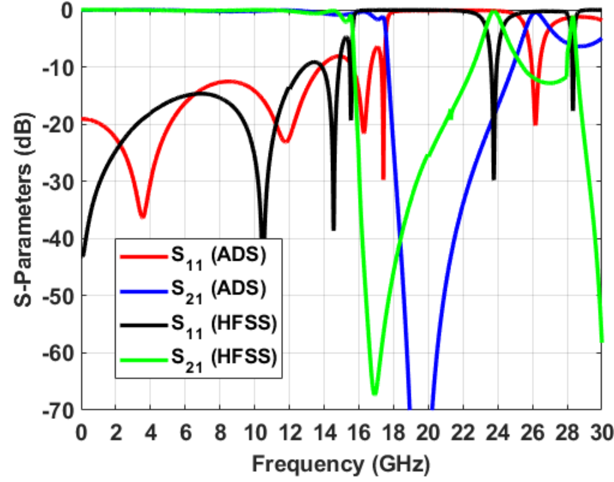


Figure 3.10: ADS and HFSS simulated S-parameters of the Chebyshev LPF (calculated values).

shev LPF using calculated values. It is seen that the simulations are very similar, but the cutoff of the HFSS simulation is shifted to the left (lower in frequency). This is expected as the HFSS simulation will account for edge effects due to the open-circuit stubs. This edge effect can ultimately be thought of as a small parasitic capacitance to ground, which effectively increases the length of the shunt open-circuit stubs. Analyzing (3.16), an increase in the stub length will lower the cutoff frequency. Fortunately, the effective length associated with this edge effect capacitance can be calculated using [108]

$$d_{edge\ effect} = \frac{1}{k} \cot^{-1}\left[\frac{4c + 2w}{c + 2w} \cot(kc)\right], \qquad k = \frac{2\pi}{\lambda} \tag{3.35}$$

and

$$c = \frac{b \ln(2)}{\pi} \tag{3.36}$$

where b is the height of the SISL air cavity, and w is the width of the shunt

Table 3.5: Calculated edge effect lengths.

Variable	**Length (mil)**
d_1	19.24
d_2	16.10
d_3	18.56

open-circuit stub. Equation (3.35) simplifies to

$$d_{edge\ effect} = c\left(\frac{c+2w}{4c+2w}\right) \tag{3.37}$$

for $kc < 0.3$ and is accurate within 3%. This edge effect length equation above is only due to one-half of the parasitic capacitance and must be multiplied by two for the proposed SISL technology. The calculated lengths are provided in Table 3.5. Length d_1 is the additional length to l_1 in Fig. 3.7 and so on. The additional lengths are added to the ADS LPF model and the simulated results are shown in Fig. 3.11. With the additional length added, the S-parameters

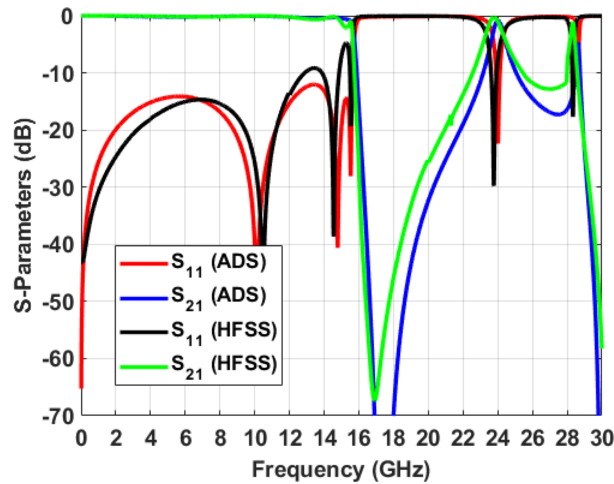


Figure 3.11: ADS and HFSS simulated S-parameters of the Chebyshev LPF with additional edge effect length added to ADS LPF model.

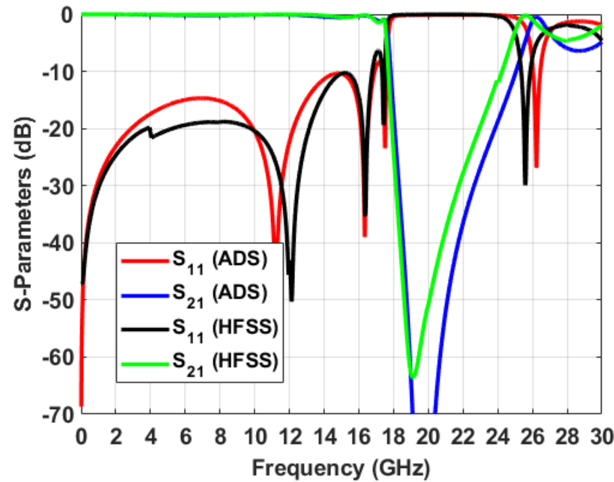


Figure 3.12: ADS and HFSS simulated S-parameters of the Chebyshev LPF with edge effect compensation added to the HFSS model.

of the ADS LPF model and HFSS model are almost identical. The reflection zeros of the return loss align very well as well as the cutoff frequency and stopband performance.

Since the lowered cutoff frequency is directly correlated to the additional parasitic capacitance length, this can be compensated for in the design. All that is needed is to subtract the lengths calculated using (3.35) from (3.16). The HFSS model is modified reducing the stub lengths based on the calculated lengths provided in Table 3.5. The simulated S-parameters of the ADS LPF and the newly edge effect compensated HFSS model are shown together in Fig. 3.12. The simulated results verify the edge effect compensation resulting in a very good agreement between the ADS and HFSS simulation. At this point, the distributed equations with compensation and the modified ADS stripline model are fully-verified and confirmed with HFSS simulations.

Now that there is an ADS model that accurately mimics the electromagnetic response, the LPF can be quickly tuned in ADS greatly reducing the time needed to generate the desired performance. In [46], it is shown that

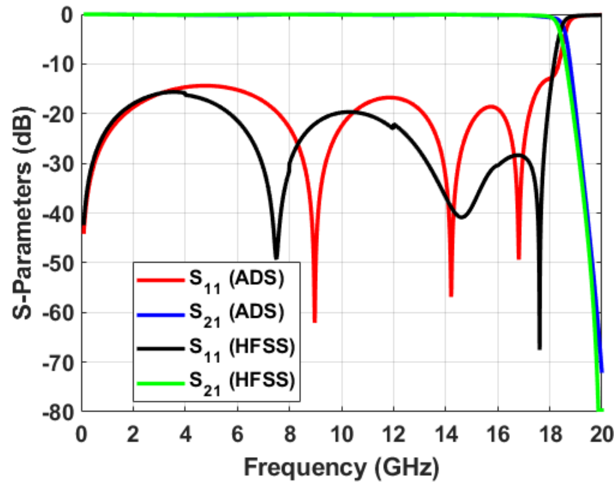


Figure 3.13: ADS and HFSS simulated S-parameters of the Chebyshev LPF (tuned values).

the shunt outer stubs can be made longer to increase the passband and stopband bandwidth and eliminate ripples near the cutoff frequency; therefore, l_1 is increased to 84 mil to improve the high frequency match. Moreover, stub lengths l_2 and l_3 are decreased slightly to 112 and 113 mil, respectively, to get the correct 18 GHz cutoff frequency. Lastly, w_3 is increased to 72 mil to improve the match across the entire passband. The simulated S-parameters of the tuned ADS LPF and HFSS model are shown in Fig. 3.13. The return loss is made better than 15 dB across the passband with a cutoff frequency of 18 GHz and 50 dB of stopband suppression by 20 GHz.

Recall that the ideal LC prototype in Fig. 3.5 had 6 reflection zeros in the passband located at 0, 8, 13, 16, 17.4, and 18 GHz. However, there is a slight discrepancy in the number of reflection zeros in Fig. 3.13 if compared to the ideal LC model. When simulating distributed filters, it is common for the reflection zeros to merge, especially for large passband filter designs. Comparing the ideal LC model to the HFSS simulated results, the reflection zeros at 13 and 16 GHz have merged resulting in a broader and shallower null

at 14.5 GHz. Moreover, the reflection zeros at 17.4 and 18 GHz have almost perfectly merged at 17.6 GHz yielding a very deep and narrow notch.

3.1.5 DC-18 GHz SISL LPF and Air Cavity Tuning

The design of the DC-18 GHz SISL LPF can now be completed. First off, the LPF design is placed between two vertical via transitions and the pre-preg is added to the model to accurately model the cavity height. The proposed SISL LPF is shown in Fig. 3.14. Slight tuning of the filter dimensions is required due to the addition of the via transitions and cavity height change. The final LPF layout and tuned dimensions are provided in Fig. 3.15 and Table 3.6, respectively. The only significant change is the length and width of the series short-circuit stubs (l_4, l_5, and l_6). The width is intentionally made narrower in order to reduce the length of the stub. If the width W_L in (3.32) is reduced, Z_L gets larger, which decreases the length l_L as seen in (3.31). This is done to improve the stopband performance by pushing out half-wave resonances.

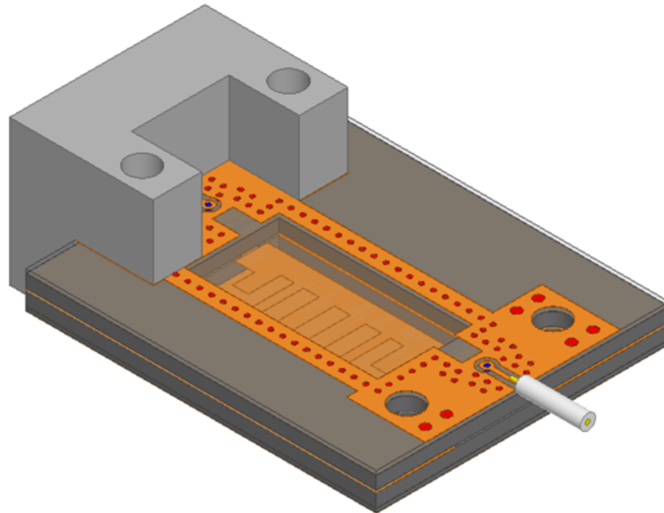


Figure 3.14: 3-D view of the proposed DC-18 GHz SISL LPF.

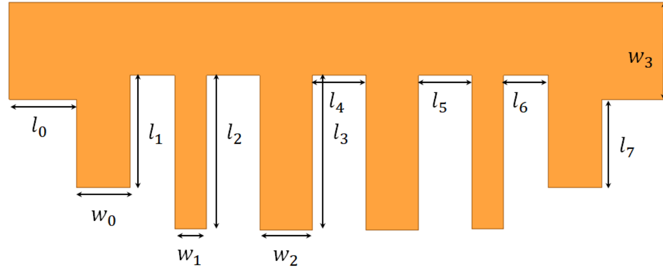


Figure 3.15: Layout representation for the tuned SISL Chebyshev LPF.

Table 3.6: Final LPF distributed parameters.

Variable	Length (mil)	Variable	Length (mil)
w_0	40.42	w_1	23.86
w_2	39.48	w_3	73.00
l_0	50.31	l_1	84.19
l_2	115.34	l_3	116.23
l_4	40.18	l_5	39.99
l_6	33.59	l_7	66.09

Similar to the SISL thru-line, the dimensions of the air cavity surrounding the SISL LPF must be carefully chosen to ensure no parasitic waveguide modes are excited. Fig. 3.16 shows the top-down view of the SISL LPF and the cross-sectional view is identical to Fig. 2.36. The cavity width a for the SISL LPF design is wider than the cavity is tall, so the first parasitic waveguide mode will be TE_{01}, which can be calculated using (2.6). Furthermore, $c > a > b$, so a TE_{101} cavity resonance will occur and can be calculated using (2.7).

For the 18 GHz LPF, the cavity width must be less than 303 mil in order to make sure the TE_{01} waveguide mode will excite above 18 GHz. The total width of the final SISL LPF design is $w_3 + l_3 = 73 + 66 = 139$ mil. Therefore, the cavity width can be reduced to push this mode even higher in frequency. The cavity width was initially chosen to be 260 mils prior to the final design yielding an effective cutoff frequency of 21 GHz. For the final design, the

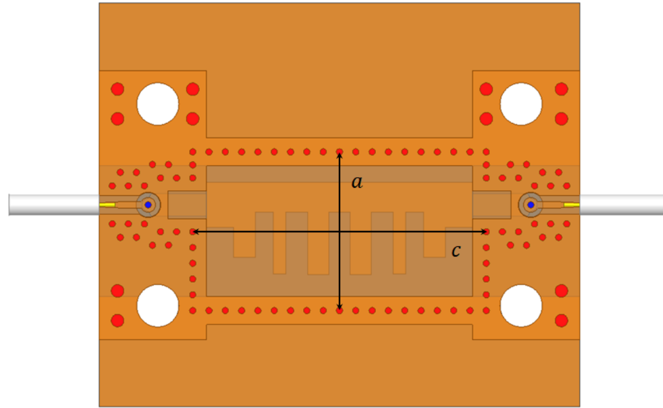


Figure 3.16: Top-down view of the proposed SISL LPF design showing the effective rectangular waveguide structure dimensions.

cavity width had to be widened to 283 mil, which pushes the effective cutoff to 19.3 GHz. This is well above the 18 GHz cutoff frequency of the proposed SISL LPF and will have no effect on the filter's passband performance.

The length of the air cavity denoted as c in Fig. 3.16 is roughly 535 mil. Using (2.7), the resonance frequency of the air cavity is 21.8 GHz. Again, this is above the 18 GHz cutoff frequency of the SISL LPF and will not affect the filter's passband performance. However, this cavity resonance can have an affect on the stopband performance, but can be compensated for by designing a ground defected structure at the resonance frequency if needed. This concept is left to future work and will not be covered in this dissertation.

3.2 DC-18 GHz SISL LPF Simulations

Once the design has been modeled in HFSS and verification of the cavity dimensions has been completed, the HFSS model is simulated. The SISL LPF model uses two wave port excitations renormalized to 50 ohms since the design is intended to be used in a 50 ohm system. The 26 GHz bandwidth is broken

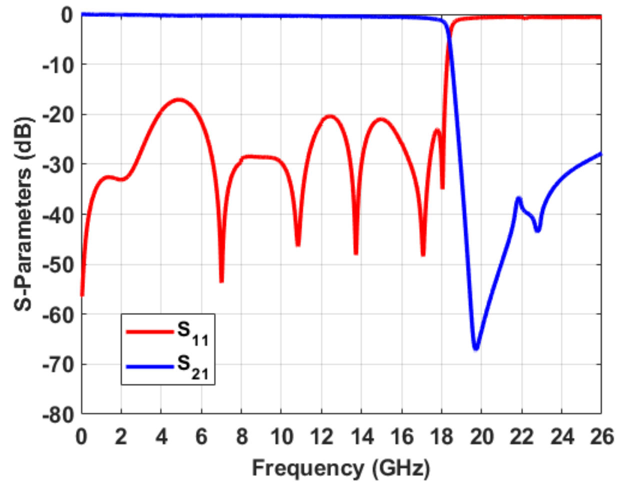


Figure 3.17: HFSS simulated S-parameters of the proposed DC-18 GHz SISL LPF.

up into 7 simulations, with the first 6 each covering 4 GHz of bandwidth and the last covering 2 GHz. The driven solution is set with a maximum delta S of 0.01 and 5 minimum converged passes. The plots are shown up to 26 GHz since calibration of the measured results are only good up to 26 GHz. The simulated S-parameters are shown in Fig. 3.17.

The simulated insertion loss is 0.6546 dB at the 18 GHz cutoff frequency. This agrees very well with the expected insertion loss of 0.6469 dB, which is calculated by adding the simulated insertion loss of each individual section. The breakdown of this 0.6469 dB loss is as follows:

1. 0.1156 dB is due to the CPWG traces,
2. 0.0630 dB is due to the stripline traces,
3. 0.0142 dB is due to the connectors,
4. 0.0167 dB is due to the via transitions,
5. 0.4374 dB is due to the SISL LPF.

The slight difference between the expected S_{21} (0.6469 dB) and full-model simulated S_{21} (0.6546 dB) is more than likely due to a minor mismatch from the stripline to SISL transition, which is only captured in the full filter model.

In Fig. 3.17, it is noted that the number of reflection zeros has increased to seven. The additional reflection zero at approximately 2 GHz is a result of the additional length of the connector. This was proven by simulating the proposed filter in HFSS with and without the connector and changing the length of the connector using the de-embedding feature in HFSS. When the connectors are removed, the additional reflection zero is eliminated and only the six reflection zeros of the filter are present. Moreover, by changing the length of the connector, the reflection zero shifts in frequency. In practice, there will be no need for the connectors as the CPWG traces will be routed to the adjacent component of the extended circuit.

The HFSS simulated group delay of the proposed SISL LPF is shown in Fig. 3.18. The maximum delay in the passband is 0.558 ns at 18 GHz with an average delay of 0.331 ns across the DC-18 GHz passband.

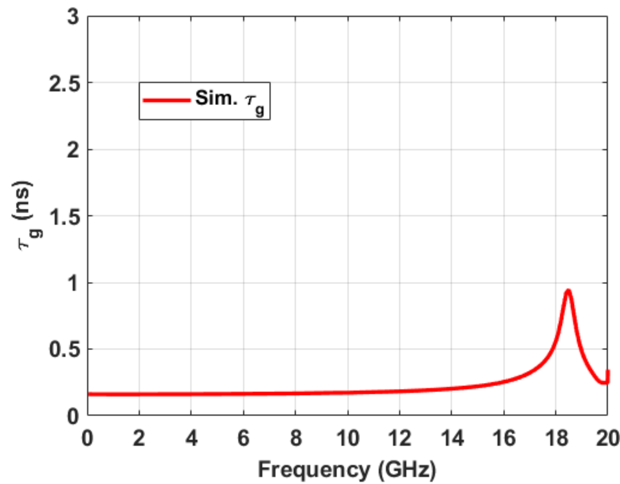


Figure 3.18: HFSS simulated group delay of the proposed SISL LPF.

3.3 Layout File Generation and Device Fabrication

The Gerber files are generated exactly the same as the SISL thru-line discussed in Section 2.3. Furthermore, the LPF device fabrication is completed using the same procedure as the thru-line, which is explained in-depth in Appendix A. Fig. 3.19 is a photograph of the in-house fabricated fully-board embedded DC-18 GHz SISL LPF. The LPF devices are also fabricated by Accurate Circuit Engineering (ACE) [109]. The overall size of the fabricated component is 2.28 x 1.91 x 0.23 cm^3. The SISL LPF itself is only 1.25 x 0.62 x 0.22 cm^3. To make sure all of the fabrication steps were done properly, one of the fabricated prototypes is cross-sectioned to investigate the structures of layers as well as the quality of plating. Fig. 3.20 shows a longitudinal cross-section of a sample LPF. The air cavities and the plated ground vias are observed.

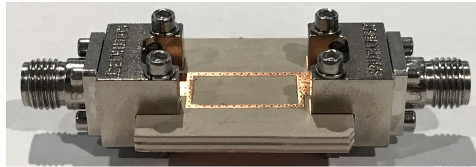


Figure 3.19: Photograph of the fabricated DC-18 GHz SISL LPF.

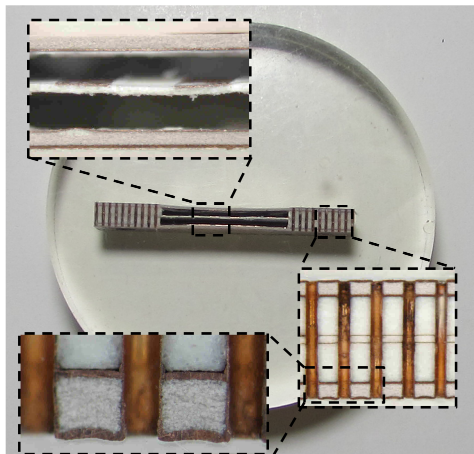


Figure 3.20: Cross-section of a fabricated SISL LPF with inset showing both the air cavity and plated thru-hole vias (dark areas are due to oxidation).

3.4 Measured Results

Both the in-house and professionally fabricated DC-18 GHz SISL LPFs are measured using an Agilent Technologies N5225A PNA that has been calibrated using an Agilent N4691-60006 electronic calibration module. The in-house filters had considerably more passband insertion and mismatch loss due to registration and lamination issues. Therefore, only the measured results of the the ACE LPF is shown. Fig. 3.21 plots the simulated and measured S-parameters. The simulated and measured results show good agreement up to 26 GHz in both the passband and stopband. The measured insertion loss is less than 0.9266 dB up to 18 GHz with greater than 10.5 dB of return loss across the filter's passband. The filter portrays great stopband performance providing greater than 30 dB of attenuation up to 26 GHz. Notice there is a small resonance right at 21.8 GHz. This is due to the cavity resonance discussed in Section 3.1.5.

There is some degradation in the return loss for the measured filter that is most likely due to the air cavity dimensions (slight bowing of the material

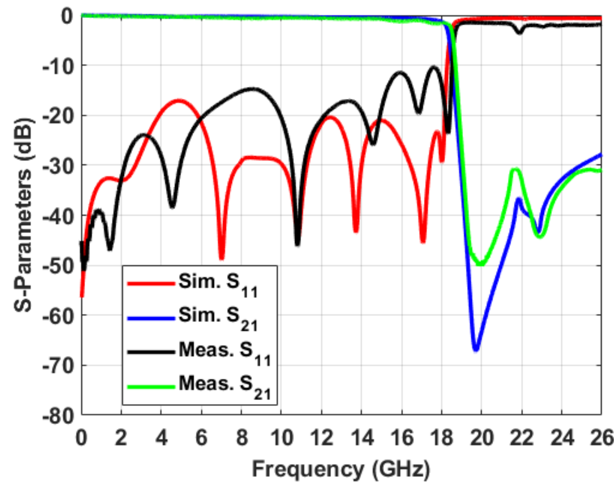


Figure 3.21: Simulated and measured S-parameters of the proposed SISL LPF.

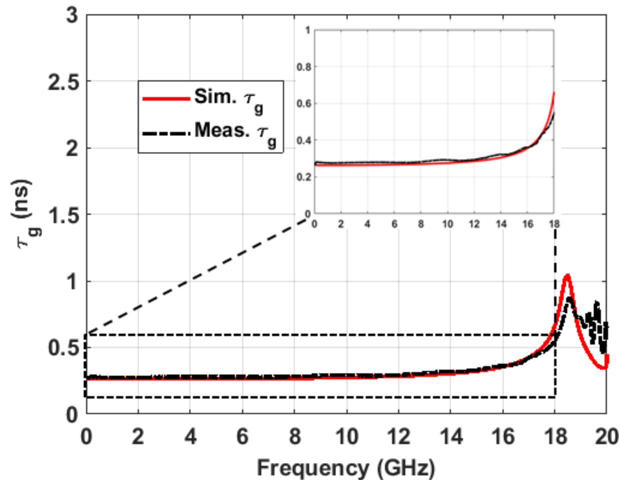


Figure 3.22: Simulated and measured group delay of the proposed SISL LPF.

around the air cavity) and the suspended dielectric layer. The return loss is very sensitive to the air cavity height. Analyzing the plots at 18 GHz, which is the frequency of highest passband loss, there is an additional 0.1934 dB of mismatch loss. This mismatch loss can be added to the 0.6546 dB of simulated loss resulting in an expected insertion loss of 0.8479 dB due to mismatch, which agrees very well with the measured insertion loss. The additional 0.0786 of loss is likely due to conductivity loss since the HFSS model assumes perfect copper conductivity. Therefore, a detailed loss analysis has been completed and fully captures all the losses contributing to the difference between simulated and measured results.

The group delay of the SISL LPF is also measured and plotted with the simulated group delay in Fig. 3.22. Again, these results show good agreement. The measured group delay is exceptionally small across the entire passband reaching a maximum of only 0.548 ns at the 18 GHz cutoff frequency. The group delay is also extremely flat with an average delay of 0.366 ns.

The proposed SISL LPF is compared in regards to volumetric size and per-

Table 3.7: Comparison of commercially available and academically researched LPFs to the proposed SISL LPF.

Reference	**Techn.**	**f_c (GHz)**	**Volume (cm^3)**	**I.L. (dB)**	**R.L. (dB)**
[110]	Micro-strip[1]	1.0	0.21	< 3.0	> 15.0
[74]	SISL	1.0	7.20[3]	< 1.0[4]	> 25.0[4]
[15]	Lumped LC	18.0	49.16	< 1.0	> 10.0
[16]	Micro-strip[2]	18.0	5.46	< 1.2	> 20.0
[17]	SSS	18.0	17.95	< 1.0	> 10.0
(sim.)*	SISL	18.0	0.17[3]	< 1.0[4]	> 20.0[4]
(meas.)*+	SISL	18.0	0.17[3]	< 1.0[4]	> 12.0[4]

[1] un-packaged micro-strip filter
[2] packaged micro-strip filter
[3] without edge-launch connectors
[4] with edge-launch connectors
* simulated and measured values from this work
+ measured results after loss compensation

formance to other commercially available and academically studied LPFs, as shown in Table 3.7. It should be noted that the filter in [74] and the proposed SISL filter both include the edge-launch connector for measured performance, but do not consider the connectors for the volume calculation. Because the proposed filter is a distributed LC equivalent filter, which does not rely on the cavity resonance or the cavity's quality factor, the air cavity can be significantly reduced to minimize size with minimal impact to the insertion loss. The proposed SISL LPF is approximately 290 times volumetrically smaller than the lumped element LC filter in [15], and can be made cheaper due to the elimination of assembly and component cost. Compared to the SSS filter, the SISL filter is two orders of magnitude volumetrically smaller and requires no mechanical housing, connectors, or assembly, resulting in a lighter weight,

compact size, and low cost filter. In general, the microstrip filter in [16] does not need to be packaged, but the packaging is needed to minimize radiation losses and maintain a low passband insertion loss. Moreover, the SISL LPF is self-packaged yielding a high electromagnetic shielding effectiveness. A key take-away from Table 3.7 is that the proposed SISL LPF has the same small form factor as seen in traditional integrated micro-strip filters [110], but also emulates the SSS filter structure in [17] allowing for the low passband insertion loss that the SSS filter technology is known for.

Chapter 4

Suspended Integrated Stripline Highpass Filter

The purpose of this chapter is to apply the fully-board embedded SISL technology to the design of microwave distributed highpass filters. This chapter will derive necessary design equations and offer several guidelines to realize wideband highpass filters in the SISL technology. An eleventh-order generalized Chebyshev HPF with a cutoff frequency of 2 GHz is used as a technology demonstrator. A broadside coupling method is used to achieve wide passband performance up to 18 GHz. The end result is a first time demonstration of a fully-board embedded SISL highpass filter design and first time demonstration of a self-packaged suspended line filter with octo-octave passband performance up to Ku-band.

4.1 SISL HPF Design

Fig. 4.1 shows the exploded view of the proposed HPF using the fully-board embedded SISL technology. A bottom looking view of the exploded stack-up is shown in Fig. 4.2 since the HPF uses broadside coupling to achieve wideband performance. The broadside coupling is implemented on metal layers 5 (M5) and 6 (M6). The PCB stack-up is identical to the one used for both the SISL thru-line and LPF discussed in Section 2.1.1. The HPF passband will extend

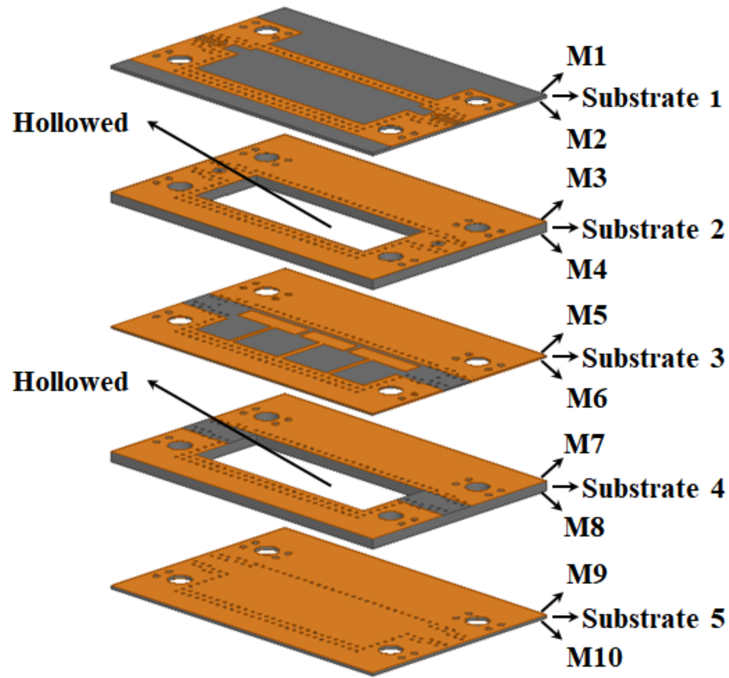


Figure 4.1: 3-D exploded view of the proposed SISL generalized Chebyshev HPF.

from 2 GHz up to 18 GHz. Because the passband of the HPF is less than the thru-line, the same stack-up can be used with no modifications to the vertical via transitions; therefore, the SISL thru-line section can be replaced by the SISL HPF.

Assuming the vertical via transitions are already designed, the remaining design procedure is completed as follows:

1. Choose the cutoff frequency, filter type, and filter order.

2. Model and simulate the ideal LC circuit model to verify filter performance.

3. Model the SISL air cavity and extract the effective permittivity using HFSS (discussed in Section 2.1.5).

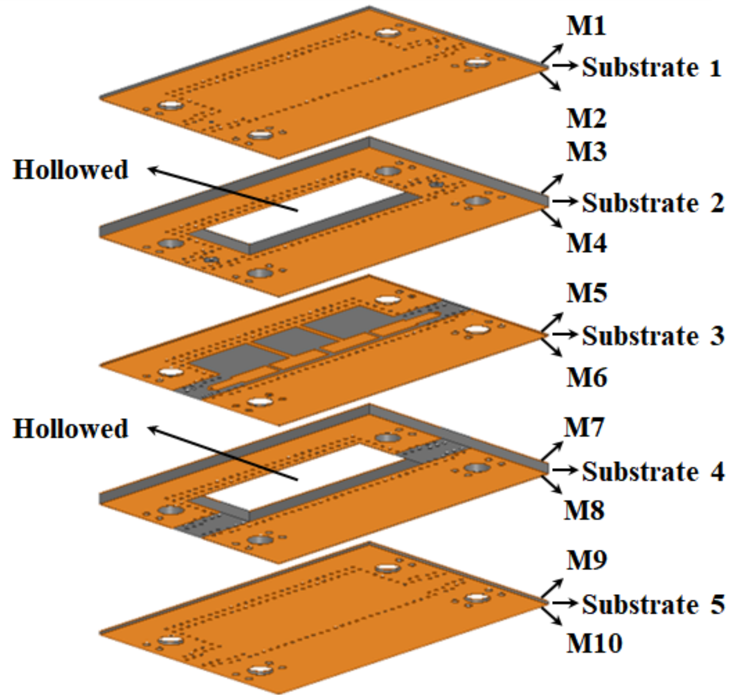


Figure 4.2: Bottom 3-D exploded view of the proposed SISL generalized Chebyshev HPF.

4. Calculate the distributed lengths and widths for the LC equivalent transmission line models using the extracted effective permittivity.

5. Using the modified ADS stripline model, modify the LC filter with distributed shunt short-circuit stubs and tune for correct passband response.

6. Model the filter design in an electromagnetic simulator with distributed capacitors and resonators and simulate.

7. Fine-tune for optimal filter performance in ADS and then update electromagnetic simulator model and simulate to verify performance.

8. Place the design between two vertical via transitions and tune the cavity dimensions to ensure excitation of parasitic waveguide modes occurs above the filter cutoff frequency (might require fine-tuning of the SISL

component design).

9. Simulate the final SISL design to make sure the via transitions have minimum affect on the final design.

10. Generate layout files from HFSS model.

After the design procedure is completed and final simulations are ran, the device is ready for fabrication. The fabrication procedure used for the SISL LPF, discussed in Appendix A, is used for fabrication of the SISL HPF. The filters are then connectorized and connected to a calibrated PNA for S-parameters measurements.

The next several subsections will go into fine details for several steps of the design procedure above. Some of the sections are skipped since they have been shown and verified in previous chapters. This will be done for the design of a 2 GHz SISL HPF. The following design procedure is accomplished using Keysight ADS and ANSYS HFSS software.

4.1.1 Filter Characteristics

As previously mentioned, the final filter design is a 2-18 GHz cascaded BPF. The cutoff frequency of the HPF for this design needs to be 2 GHz. The same generalized Chebyshev [23] filter type is used, which has an equiripple passband, three transmission zeros at infinity, and the remainder at a finite frequency near the cutoff frequency. The generalized Chebyshev LPF prototype is shown in Fig. 3.2. The dual of the LPF prototype, shown in Fig. 4.3, is used in this section. The element values, normalized frequencies, and filter order design chart in [23] are still valid, but careful attention to detail is required due to the variable changes in the prototype. The design criteria for the

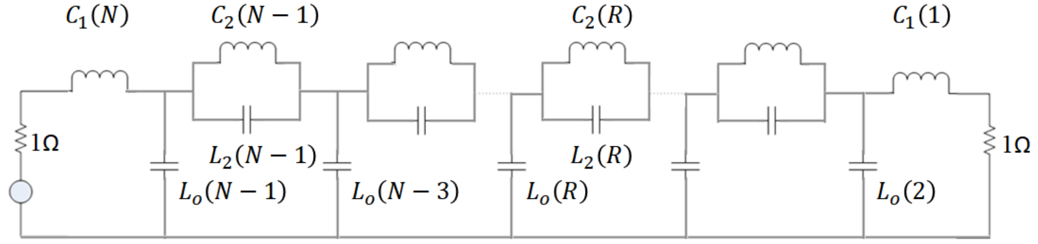


Figure 4.3: Generalized Chebyshev LPF prototype (dual) having 3 transmission zeros at infinity and (N-3) at a finite frequency.

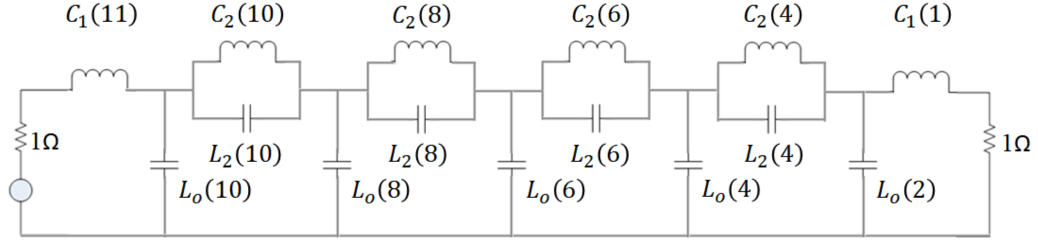


Figure 4.4: Generalized Chebyshev LPF prototype (dual) for an eleventh-order filter.

2 GHz HPF is to have 20 dB of return loss across the entire passband and 50 dB of insertion loss by 1.5 GHz. Given these design parameters, a ninth-order ($N = 9$) filter is needed to meet design goals. However, an eleventh-order filter is chosen since all of the information needed has already been used. A LPF prototype with corresponding elements for an eleventh-order filter is shown in Fig. 4.4.

The LPF prototype must be transformed into a HPF prototype. The frequency substitution

$$\omega \rightarrow -\frac{\omega_c}{\omega} \tag{4.1}$$

is used to convert from a lowpass to a highpass response [18]. The negative sign is needed to convert to physically realizable inductors and capacitors. The transform mathematically indicates that the lumped element inductors are replaced with capacitors and lumped element capacitors are replaced with

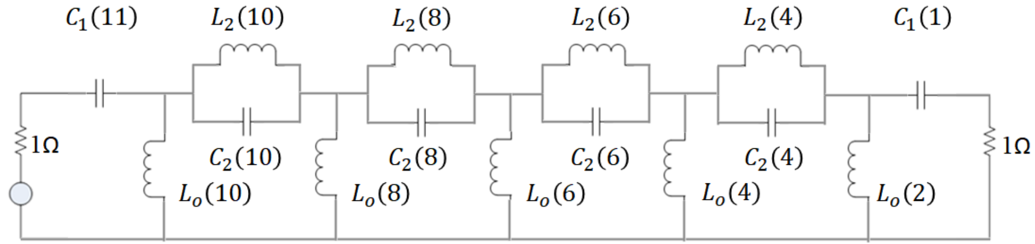


Figure 4.5: Generalized Chebyshev HPF prototype for an eleventh-order filter.

inductors. Making these lumped element substitutions, the HPF prototype is shown in Fig. 4.5. The element values and normalized frequencies for the eleventh-order generalized Chebyshev HPF prototype are shown again for convenience in Table 4.1 and Table 4.2, respectively.

Table 4.1: Calculated element values for an eleventh-order generalized Chebyshev HPF prototype using an alternating-pole technique [23].

N = 11		**R.L. > 20 (dB)**
R	**Element**	**I.L. > 50 (dB)**
11	$C_1(11)$	1.04297
10	$L_0(10)$	0.935065
	$L_2(10)$	0.984313
	$C_2(10)$	0.787121
8	$L_0(8)$	0.786767
	$L_2(8)$	0.794605
	$C_2(8)$	0.975041
6	$L_0(6)$	0.807267
	$L_2(6)$	0.794605
	$C_2(6)$	0.975041
4	$L_0(4)$	0.786767
	$L_2(4)$	0.984313
	$C_2(4)$	0.787121
2	$L_0(2)$	0.935065
1	$C_1(1)$	1.04297

Table 4.2: Calculated normalized frequencies [23].

		R.L. > 20 (dB)
Order	**Frequency**	**I.L. > 50 (dB)**
11	ω_o	1.13609
	ω_1	1.06853

4.1.2 Ideal LC Model

The ideal LC model can be built in ADS after a frequency and impedance scaling is performed using the element values and cutoff frequency from Section 4.1.1. The capacitor values are calculated using

$$C = \frac{1}{R_o \omega_c C_n(R)} \tag{4.2}$$

where R_o is the impedance of the system, $C_n(R)$ are the element values from Table 4.1, and ω_c is the cutoff frequency in rad/sec. The inductor values are calculated using

$$L = \frac{R_o}{\omega_c L_n(R)} \tag{4.3}$$

where $L_n(R)$ are the element values from Table 4.1. Using these equations, the inductance and capacitance values for the ideal LC circuit model can be calculated and are shown in Table 4.3. The eleventh-order generalized

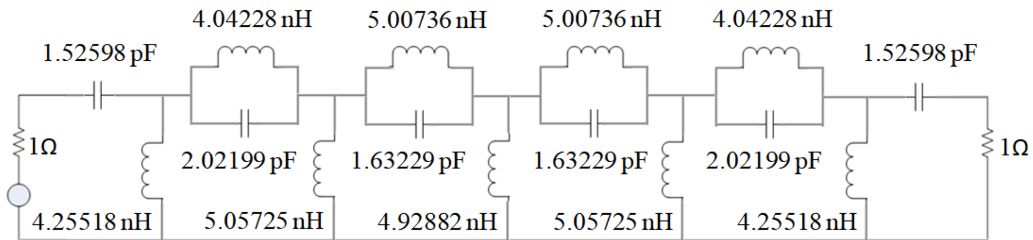


Figure 4.6: Generalized Chebyshev HPF prototype for an eleventh-order filter with calculated inductance and capacitance values.

Table 4.3: Calculated inductance (nH) and capacitance (pF) values for the ideal LC circuit model.

N = 11	**R.L. > 20 (dB)**		**I.L. > 50 (dB)**	
R	**Capacitor**	**(pF)**	**Inductor**	**(nH)**
11	$C_1(11)$	1.52598		
10	$C_2(10)$	2.02199	$L_0(10)$ $L_2(10)$	4.25518 4.04228
8	$C_2(8)$	1.63229	$L_0(8)$ $L_2(8)$	5.05725 5.00736
6	$C_2(6)$	1.63229	$L_0(6)$ $L_2(6)$	4.92882 5.00736
4	$C_2(4)$	2.02199	$L_0(4)$ $L_2(4)$	5.05725 4.04228
2			$L_0(2)$	4.25518
1	$C_1(1)$	1.52598		

Chebyshev prototype with calculated values is provided in Fig. 4.6. The simulated ADS LC circuit model S-parameters are shown in Fig. 4.7. The cutoff frequency is right at 2 GHz with a return loss greater than 20 dB across the passband and greater than 50 dB of insertion loss at 1.5 GHz.

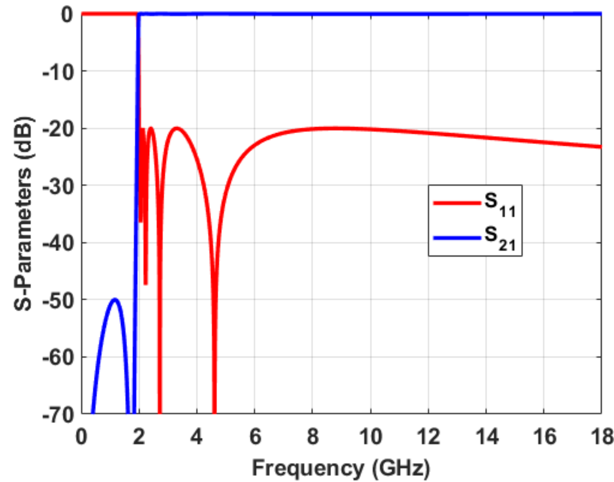


Figure 4.7: Generalized Chebyshev HPF prototype for an eleventh-order filter with calculated inductance and capacitance values.

4.1.3 Distributed HPF Design Equations

Now that the ideal LC model is verified, it is time to realize the filter. While there are capacitors available at the calculated values, they should be used with caution as capacitor tolerances can become an issue. Even using a tight tolerance capacitor of $\pm$ 0.05 pF is difficult because pad size, placement, and soldering can all affect the final capacitance value. As far as inductors, there are no currently available inductors at the values needed that have a self-resonance frequency (SRF) above 18 GHz. Therefore, the filter will need to be converted from its current lumped element design to a distributed design using LC equivalent transmission lines.

The input impedance of a Richards transformed short-circuit stub is

$$Z_{in} = jZ_o \tan(\beta l) \tag{4.4}$$

where Z_o and l are the characteristic impedance and length of the stub, respectively. Recall that the reactance of an inductor is

$$Z_L = jX_L = j\omega L \tag{4.5}$$

where L is the lumped element inductance. Equating these two equations together

$$\begin{aligned} j\omega L &= jZ_o \tan(\beta l) \\ \omega L &= Z_o \tan(\beta l) \end{aligned} \tag{4.6}$$

shows that for a given Z_o and length l, the inductance can be represented as a short-circuit stub at one specific frequency. For filter designs, this should

occur at the cutoff frequency f_c and (4.6) is modified to

$$2\pi f_c L = Z_o \tan(\beta l). \tag{4.7}$$

Moreover, if the length of the short-circuit stub is set to $\lambda/8$, this equation further simplifies to

$$\begin{aligned} 2\pi f_c L &= Z_o \tan\left(\frac{2\pi}{\lambda} \cdot \frac{\lambda}{8}\right) \\ 2\pi f_c L &= Z_o \tan\left(\frac{\pi}{4}\right) \\ Z_o &= 2\pi f_c L \end{aligned} \tag{4.8}$$

since the tangent of $\pi/4$ is equal to 1. Substituting in (4.3) for L, the characteristic impedance of the R_{th} stub is

$$\begin{aligned} Z_o &= 2\pi f_c \cdot \frac{R_o}{2\pi f_c L_o(R)} \\ Z_o &= \frac{R_o}{L_o(R)} \end{aligned} \tag{4.9}$$

where $L_o(R)$ are the element values from Table 4.1. Because the shunt short-circuit stub is geometrically identical to the shunt open-circuit stub in the LPF, the derivation relating the width of the stub to the characteristic impedance is the same. Therefore, (4.9) is substituted into (3.24) and scaled to 50 ohm terminations to yield

$$W = \frac{b-t}{4}\left(\frac{2.4\pi L_o(R)}{\sqrt{\epsilon_{eff}}} - 4 \cdot \frac{C_f}{\epsilon}\right) \tag{4.10}$$

where b and ϵ_{eff} are the height and the effective relative permittivity of the SISL air cavity, t is the copper thickness, and the fringing capacitance (C_f/ϵ) is calculated using (3.21).

As previously mentioned, the length shunt short-circuit stubs are an eighth of a wavelength. This is calculated as

$$l_{shunt\ stub} = \frac{c}{8f_c\sqrt{\epsilon_{eff}}} \tag{4.11}$$

where c is the speed of light. In summary, (4.10) and (4.11) are used to calculate the physical widths and lengths of the shunt short-circuit stubs.

In order to realize the highpass filter, the series capacitors and resonators are approximated by a inhomogeneous coupled line structures [36]. Due to the suspended substrate, this is achieved by overlapping M5 and M6 and coupling through Substrate 3 using broadside coupling as shown in Fig. 4.8. The broadside coupling structure (BCS) is chosen because of its ability to realize incredibly large impedance values. For large bandwidths, where impedance variations can get drastically large and therefore large capacitance values, the line separation for end-coupled and edge-coupled structures becomes too small to physically fabricate. Since Substrate 3 is thin for the proposed SISL design, tight coupling between M5 and M6 is achieved.

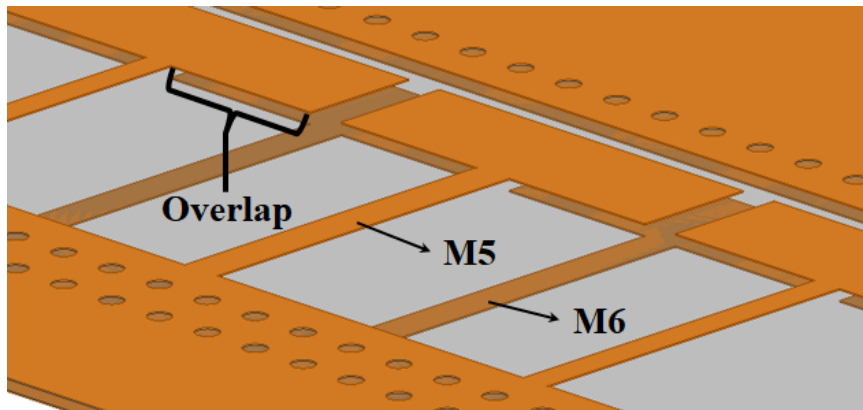


Figure 4.8: 3-D view of the overlap section to further illustrate the broadside coupling structure.

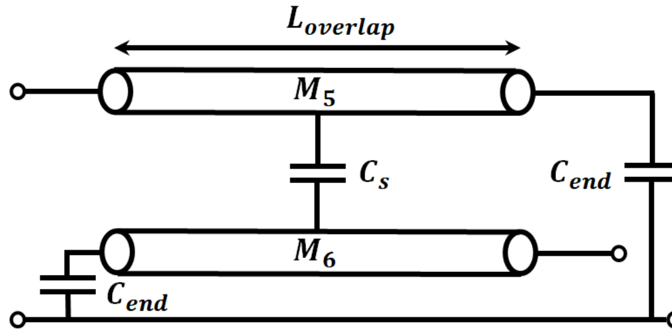


Figure 4.9: Side view of the broadside coupled structures equivalent model.

The next step is to derive a set of equations that can be used to solve for the distributed length and width of the BCS. An equivalent model of the broadside coupled structure is shown in Fig 4.9. The coupled lines will create a coupling capacitance (C_s) across the overlap length ($L_{overlap}$) that is equivalent to the series capacitance calculated in Table 4.3. The parasitic end capacitances (C_{end}) will add some additional length and can be compensated for using (3.36) and (3.37) and will be built into the final equation.

As with any coupled line structure, an even and odd mode propagation will occur. The odd-mode propagation is responsible for the coupling between M5 and M6 and the electric field lines are shown in Fig. 4.10. For the odd mode

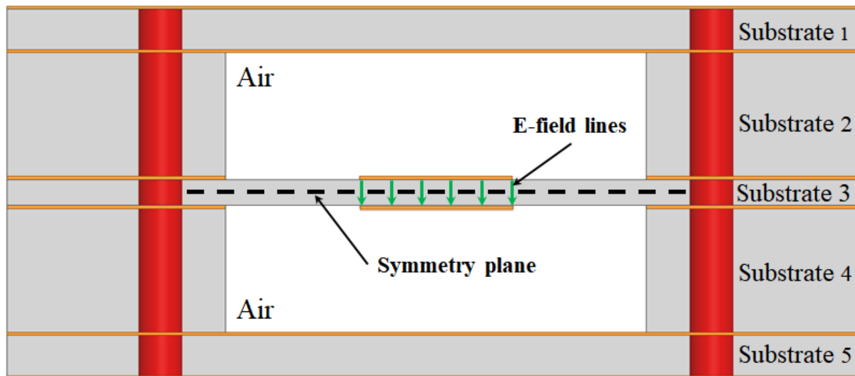


Figure 4.10: Side view of the broadside coupled structures equivalent model.

analysis, a PEC boundary is placed at the symmetry plane. It is apparent that the top and bottom half are now simply shielded microstrip tranmission lines, so it appears that the odd mode impedance is equal to the microstrip impedance. In [25], it is shown that this approximation is very precise for relatively short line lengths. This result is useful as the characteristic impedance of mictostrip transmission lines has been heavily studied and empirical closed-form equations exist as [18]

$$Z_o = \frac{120\pi}{\sqrt{\epsilon_e}[W/d + 1.393 + 0.667\ln(W/d + 1.444)]} \qquad for\ W/d < 1 \tag{4.12}$$

where

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + 12d/W}} \tag{4.13}$$

and all the variables are defined in Fig. 1.2. In the design equations above, the height (d) should be divided by 2 in order to find the odd mode characteristic impedance (Z_{oo}). Of course, this equation requires previous knowledge of the width of the transmission line. Because the overall structure is still a suspended stripline with TEM-mode propagation, (3.33) can be used to solve for an initial W. However, if the width is too narrow, the overlap length can become large enough to resonate in the passband. If this happens, the width should be increased to shorten the overlap length and push the resonant frequency above the upper passband frequency.

Now, for the series resonator sections, the odd mode characteristic impedance is directly related to the odd mode capacitance C_s as

$$\frac{C_s}{L_{overlap}} = \frac{\sqrt{\mu_o \epsilon_o \epsilon_e}}{Z_{oo}} \quad . \tag{4.14}$$

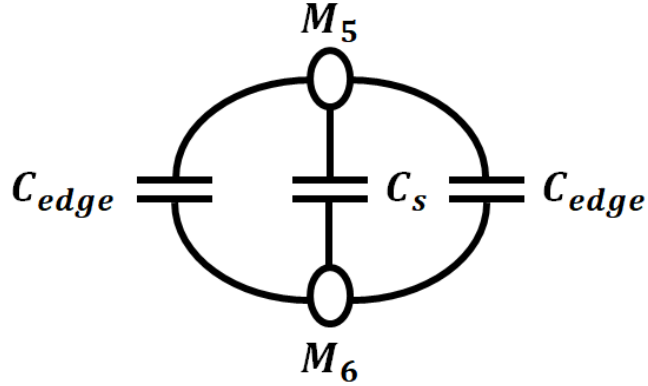


Figure 4.11: End view of the broadside coupled structures equivalent model.

Rearranging this equations and simplifying yields

$$L_{overlap} = \frac{c \cdot Z_{oo} \cdot C_s}{\sqrt{\epsilon_e}} \tag{4.15}$$

where c is the speed of light and all fringing field effects are ignored. Beyond the open end capacitance, there is an additional capacitance that occurs along the length of the overlap section. This is shown in Fig. 4.11. This edge capacitance (C_{edge}) is small for short overlap lengths and is commonly ignored since it is small relative to C_s and C_{end}. However, exact design equations exist and are found in [111]. Taking into account the end capacitances, the final expression is

$$L_{overlap} = \frac{c \cdot Z_{oo} \cdot C_s}{\sqrt{\epsilon_e}} - \frac{b\ln(2)}{2\pi}\left(\frac{b\ln(2) + 2\pi W}{2b\ln(2) + \pi W}\right) \tag{4.16}$$

where b is the SISL air cavity height and W is the width of the transmission line. For the series capacitors, the capacitance can also be represented by a

length of overlapping lines and can be calculated using [36]

$$L_{overlap} = \frac{1.8 \cdot c \cdot Z_{oo} \cdot C_s}{\sqrt{\epsilon_e}} - \frac{b \ln(2)}{2\pi} \left(\frac{b \ln(2) + 2\pi W}{2b \ln(2) + \pi W} \right) \quad . \tag{4.17}$$

In summary, (3.33), (4.16), (4.17) are used to calculate the physical widths and lengths of the series resonators and capacitances.

All of the design equations needed to fully-realize a distributed HPF [(4.10), (4.11), (3.33), (4.16), and (4.17)] are derived and can now be used to calculate the physical lengths and widths. Again, step 3 of the HPF design is skipped since it has already been done for the SISL thru-line, but recall that the effective relative permittivity is 1.16882. Moreover, all material layers and the stack-up are identical to the thru-line and LPF, and the HPF is designed for a 50 ohm system. The HPF layout representation and calculated distributed parameters are shown in Fig. 4.12 and Table 4.4, respectively.

In Fig. 4.12, notice the symmetry about the center shunt short-circuit stub. This symmetery is convenient as it halves the number of variables during the tuning process. Moreover, the length of all the shunt short-circuit stubs are the same $\lambda/8$ length further reducing the tuning complexity. Therefore, the entire design can be tuned with just 8 variables. However, the design process for the HPF is much more involved for wide passband applications since the calculated lengths will commonly start to resonate within the passband. This

Table 4.4: HPF calculated distributed prototype parameters.

Variable	**Length (mil)**	**Variable**	**Length (mil)**
w_0	75.24	w_1	58.62
w_2	60.91	w_3	62.71
l_0	144.46	l_1	682.80
l_2	103.79	l_3	81.90

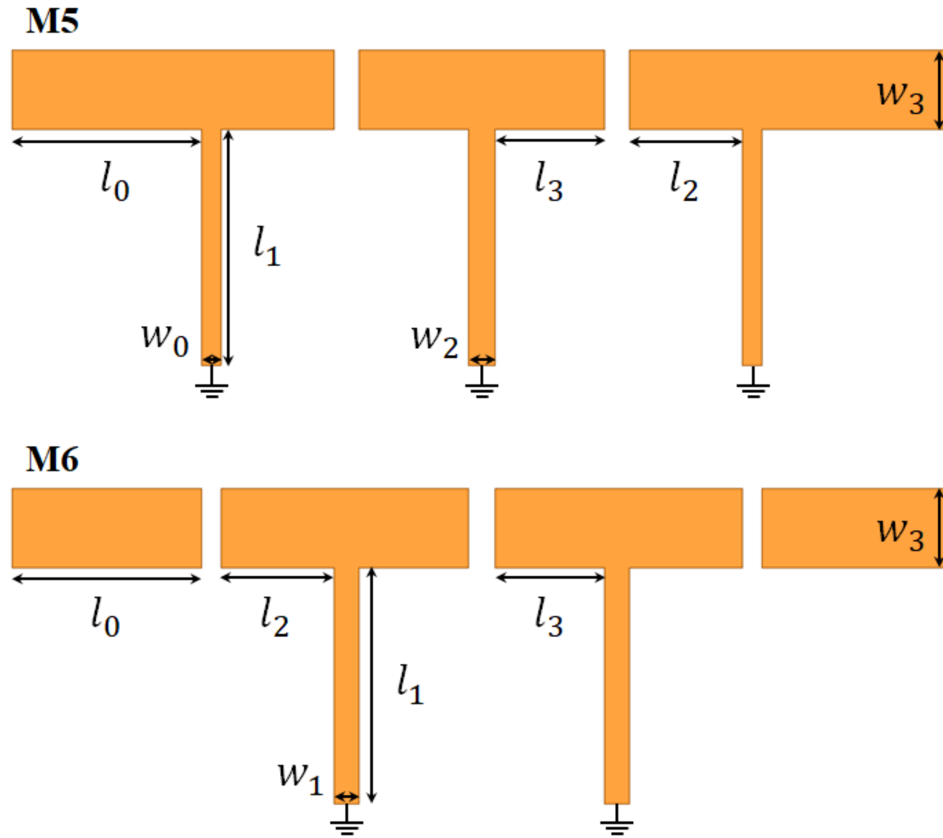


Figure 4.12: Layout representation of the distributed generalized Chebyshev HPF.

requires the lengths to be reduced, which inherently requires the widths to be tuned. This will be discussed further in the next section.

4.1.4 ADS and HFSS Simulations of the SISL HPF

The ideal LC model of the HPF from Section 4.1.2 is copied into a new ADS schematic. The ideal shunt inductors are replaced with the distributed shunt short-circuit stubs using the calculated length and widths. Fig. 4.13 is a plot of the ADS simulated S-parameters. The cutoff frequency is right at 2 GHz with great stopband performance, but the response quickly degrades above roughly

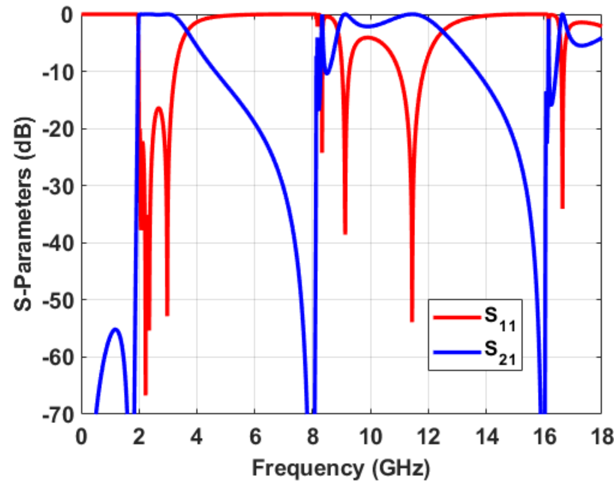


Figure 4.13: ADS simulated S-parameters of the Chebyshev LC model HPF with distributed shunt short-circuit stubs.

3 GHz. This poor response is due to the length of the shunt short-circuit stubs. Given a length of 682.80 mil and an effective permittivity of 1.16882, the half-wave resonance of the stub occurs at 8.0 GHz, which is clearly seen in the simulated response. Therefore, the length of the stub must be shortened to push the resonance above the 18 GHz upper passband frequency. Quick calculations show that the length of the stub must be shorter than 303 mil for this criteria to be satisfied. The length of the stubs are reduced to 190 mil to push the resonance significantly above the 18 GHz frequency. The widths of the stubs are changed to compensate for the change in length. Recall (4.7) which relates the inductance to the characteristic impedance of the stub. If the length of the stub is reduced, the characteristic impedance of the stub must be increased to achieve the same inductance. The characteristic impedance can be made larger by making the stub narrower. Quick tuning of the shunt stubs offers a much more acceptable wideband HPF response shown in Fig. 4.14. Significant tuning to achieve optimal filter response should not be done at this time, and should be postponed until after the distributed capacitances

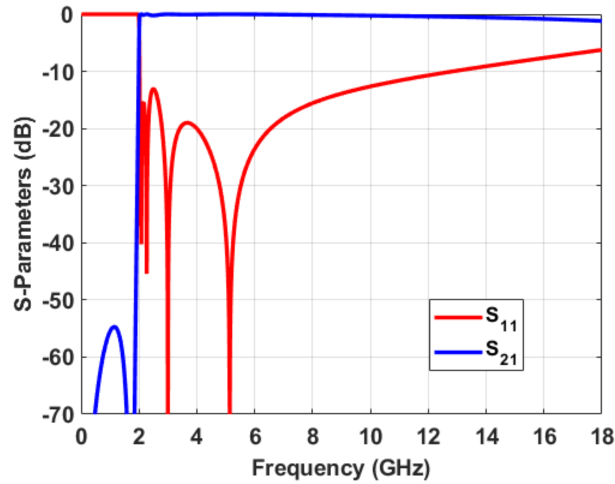


Figure 4.14: ADS simulated S-parameters of the Chebyshev LC model HPF with tuned shunt short-circuit stubs.

and resonators are included in the ADS model. For now, the only goal is to reduce the length and width of the shunt stubs to achieve the desired passband bandwidth.

Next, the series capacitors and resonators are replaced with the distributed broadside coupled structures and simulated. The S-parameters are plotted and shown in Fig. 4.15. The cutoff frequency is right at the desired 2 GHz

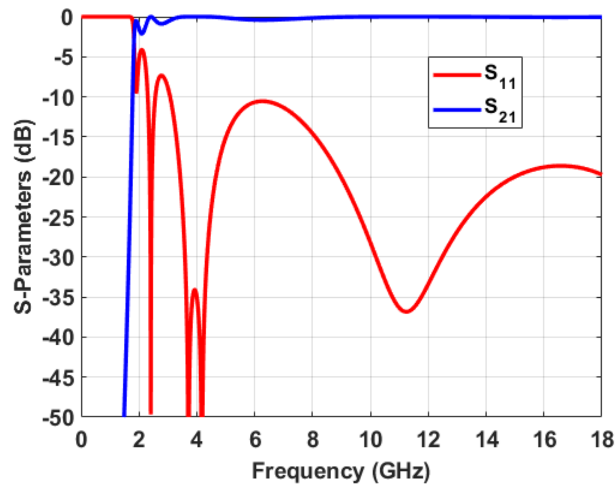


Figure 4.15: ADS simulated S-parameters of the distributed Chebyshev HPF.

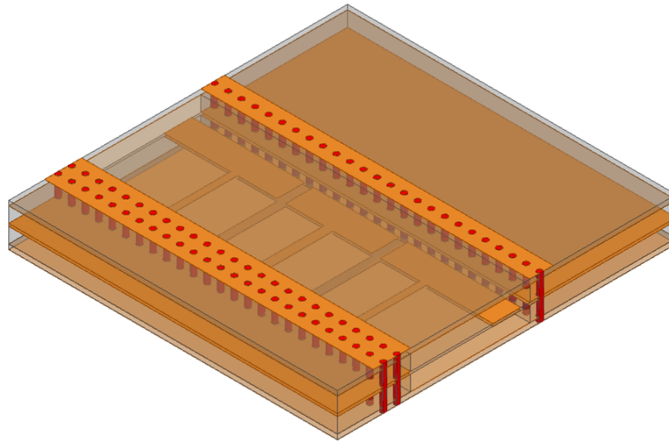


Figure 4.16: 3-D view of the HPF HFSS model.

cutoff. The match is decent beyond 3 GHz but is degraded right near the cutoff frequency. These reflection zeros are due to the series capacitances and resonators and will be tuned next. Before the HPF is tuned, it is modeled in HFSS, shown in Fig. 4.16, and simulated to compare with the ADS simulation.

Fig. 4.17 plots the ADS and HFSS simulated S-parameters of the Chebyshev HPF using calculated values. The ADS and HFSS simulated results show good

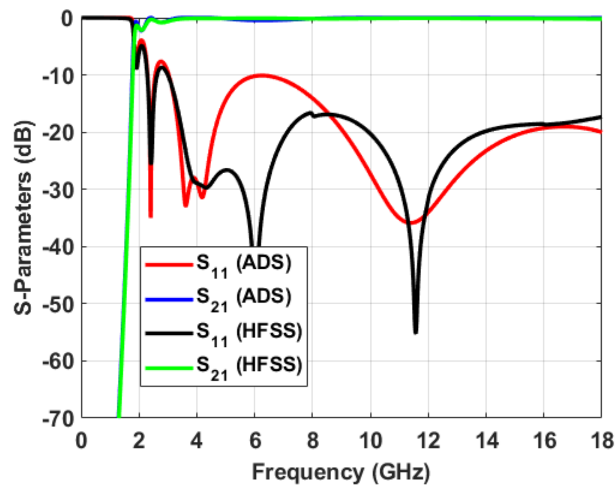


Figure 4.17: ADS and HFSS simulated S-parameters of the Chebyshev HPF (calculated values).

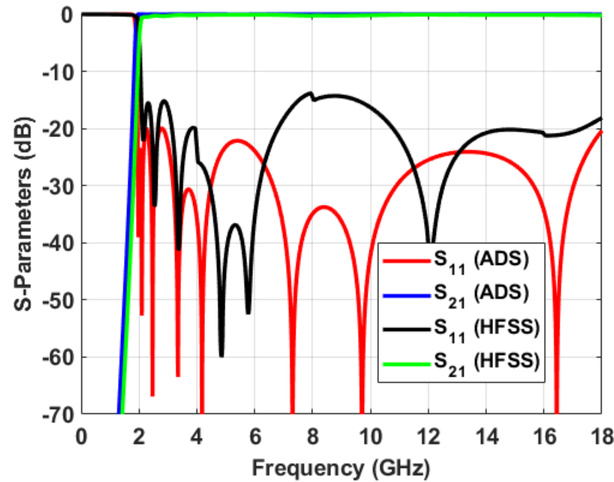


Figure 4.18: ADS and HFSS simulated S-parameters of the Chebyshev HPF (tuned values).

agreement; therefore, the HPF can be tuned quickly in ADS. The match near the cutoff is improved by tuning the lengths of the series BCSs. Tuning the series lengths causes a slight shift in the cutoff frequency so the length of the shunt short-circuit stubs are tuned to compensate. Finally, the widths of the shunt stubs are tuned to provide good match over the entire HPF passband. The HFSS model is updated with the new distributed dimensions, simulated, and compared to simulated ADS results. The tuned ADS and HFSS simulated S-parameters are plotted in Fig. 4.18. Again, the results show overall good agreement.

There is some disagreement around the 8-10 GHz region and the cutoff frequency is slightly off. Both of these issues are due to the shunt short-circuit stubs. In the ADS model, the shunt stub are terminated directly at the end of the stub length. For the fully-board embedded SISL HPF, the grounding of the shunt stubs is more complicated. A top-down view of the HPF HFSS model is shown in Fig. 4.19. The highlighted region shows how the shunt stubs are grounded. Notice that there is some additional length beyond the

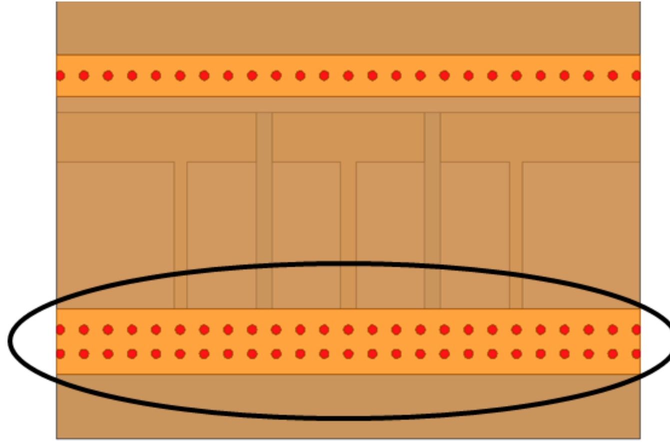


Figure 4.19: Top-down view of the HPF HFSS model.

end of the stub and the effective metalized side-wall created by the stitched vias. This short length is required since the vias must be pulled back at least one via diameter from the edge of the cavity. Furthermore, the copper must extend to the edge of the cavity in order to make sure no leakage into the cavity occurs during the plating process of the through-vias. Because the effective width of the shunt stub is larger between the edge of the cavity and the vias, the characteristic impedance of the stub is reduced. In order to keep the same inductance, the length of the shunt stub must be increased. The ADS and HFSS simulated S-parameters after adjusting the shunt stub lengths are shown in Fig. 4.20. After compensating for the length, the cutoff frequencies align very well and the return loss at 9 GHz is improved by about 5 dB.

Recall that the ideal LC prototype had 6 reflection zeros in the passband located at 2 GHz, 2.1 GHz, 2.25 GHz, 2.7 GHz, 4.6 GHz, and infinity. In Fig. 4.20, the same reflection zeros are present with a few more above 6 GHz. All of the reflection zeros above 6 GHz are due to making the distributed lengths of the series capacitances and resonators shorter to push any half-wave resonances above the 18 GHz upper passband frequency.

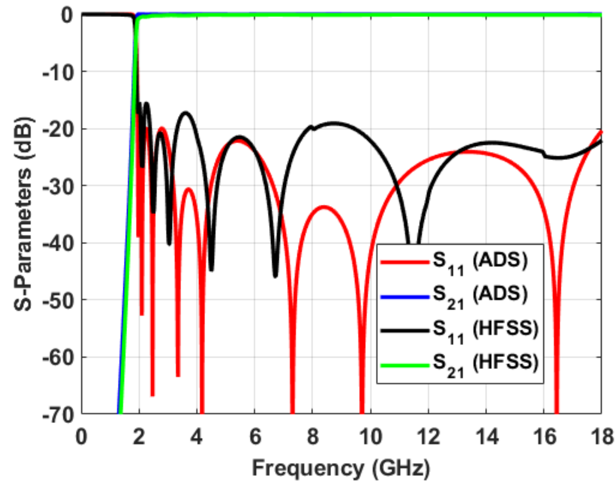


Figure 4.20: ADS and HFSS simulated S-parameters of the Chebyshev HPF.

4.1.5 2 GHz SISL HPF and Air Cavity Tuning

The design of the 2 GHz SISL HPF is accomplished by placing the previously designed HPF between two vertical via transitions. The proposed SISL HPF is shown in Fig. 4.21. The final HPF layout and tuned dimensions are provided in Fig. 4.22 and Table 4.5, respectively. The only significant change is the

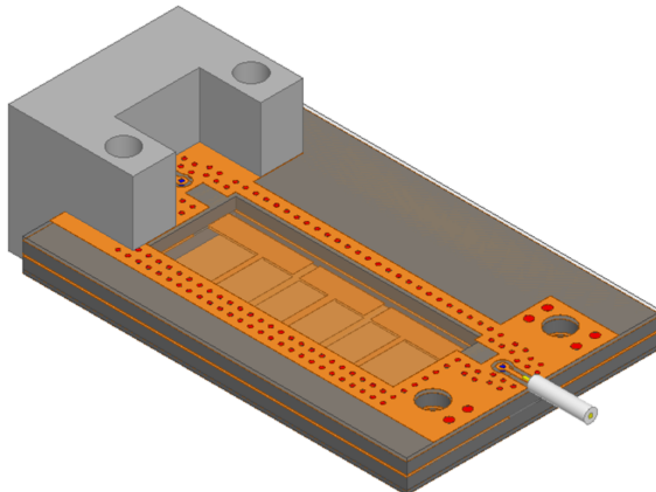


Figure 4.21: 3-D view of the proposed 2 GHz SISL HPF.

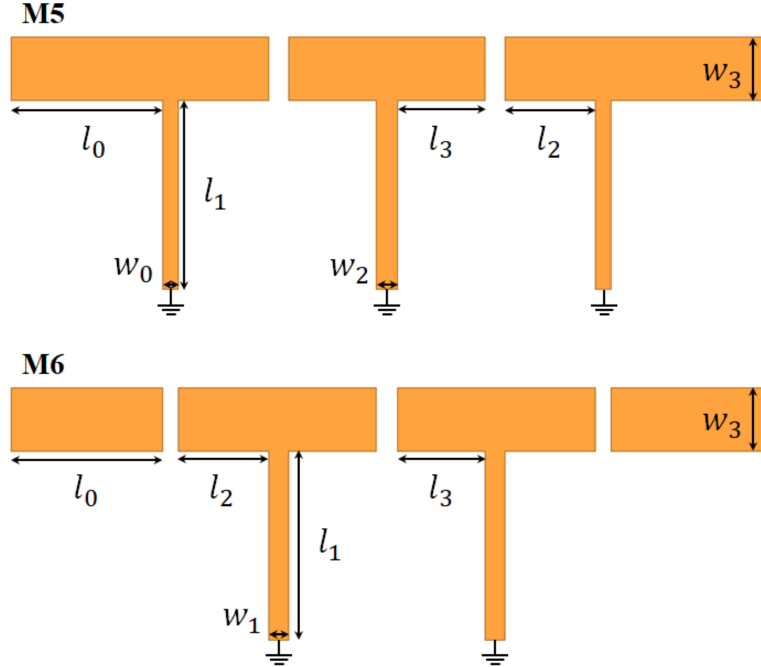


Figure 4.22: Layout representation for the tuned SISL Chebyshev HPF.

Table 4.5: Final HPF distributed parameters.

Variable	Length (mil)	Variable	Length (mil)
w_0	15.24	w_1	19.13
w_2	20.45	w_3	61.47
l_0	146.88	l_1	202.86
l_2	87.50	l_3	84.93

length of the shunt short-circuit stubs and the corresponding widths. The reason behind this is discussed in detail in the previous section.

Just like the SISL thru-line and LPF, the dimensions of the air cavity surrounding the SISL HPF are analyzed to ensure no parasitic waveguide modes are excited. Fig. 4.23 shows the top-down view of the SISL HPF and the cross-sectional view is identical to Fig. 2.36. For the 2 GHz HPF, the cavity width (a) must be less than 303 mil in order to make sure the TE_{01} waveguide mode will excite above the 18 GHz upper passband frequency. The

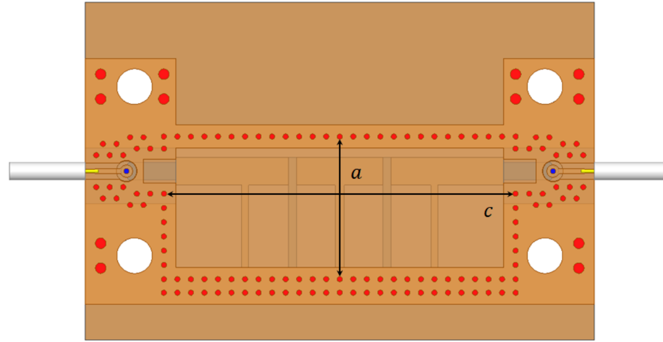


Figure 4.23: Top-down view of the proposed SISL HPF design showing the effective rectangular waveguide structure dimensions.

final cavity width is just barely under this value at 290 mils. The cavity could not be narrowed any further due to the physical size of the HPF itself along with some clearance to the ground plane. The calculated effective cutoff frequency is 18.84 GHz. The length of the air cavity (c) is 768 mil. Using (2.7), the resonance frequency of the SISL HPF is 20.13 GHz. Both of these frequencies are above the 18 GHz upper passband frequency and will have no affect on the filter's passband performance.

In Fig. 4.23, notice that there are two rows of stitching vias right after the shunt short-circuit stubs. Initial simulations showed a resonance occurring around 10 GHz that caused a narrow notch in S_{21}. The simulated S-parameters around 10 GHz are shown in Fig. 4.24. Because the cavity dimensions had already been verified, the resonance has to be occurring internally on the extended ground plane. To verify, the current density is plotted on each metal layer and analyzed to look for any ”hot-spots” that could be associated with the resonance. The current density on M5 and M6, shown in Fig. 4.25, clearly shows an issue beyond the shorting vias. The length of the hot-spot (d) is measured in HFSS and is about 335 mils wide. This resonance occurs within Substrate layer 2 which has a dielectric constant of 2.94. Inserting these val-

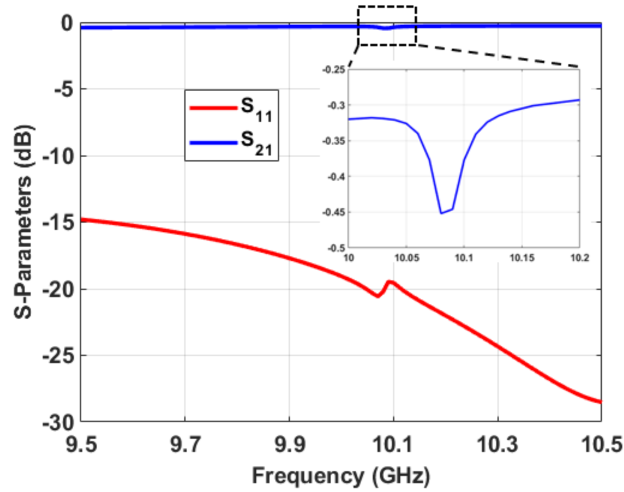


Figure 4.24: Simulated S-parameters showing the resonance around 10 GHz.

ues into (2.6), the resonance frequency is at 10.28 GHz. This agrees very well with the location of the simulated resonance. Therefore, the resonance can be associated with this hot-spot. Fortunately, this is easily fixed by placing a second row of stitching vias to properly terminate the resonance on the extended ground plane. Another approach is to narrow the width of the extended ground plane, but this is limited by the edge-launch connectors. The HFSS simulation is ran again after adding the second row of stitching vias and the

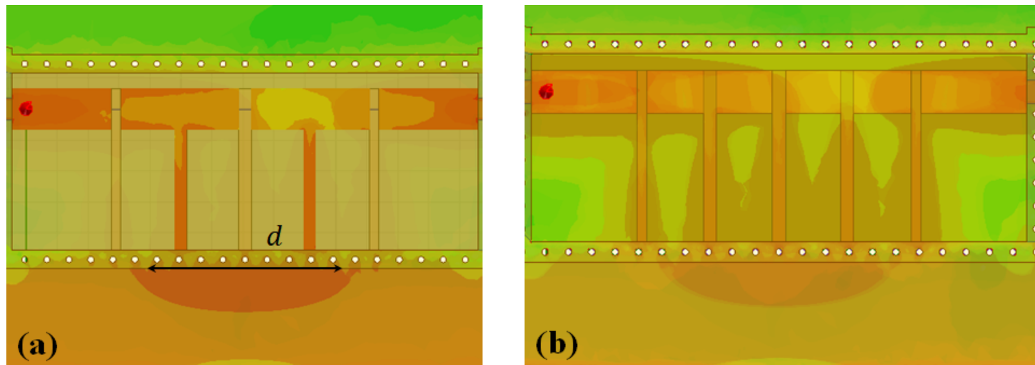


Figure 4.25: Top-down view of the proposed SISL HPF design showing the internal resonance on (a) M5 and (b) M6.

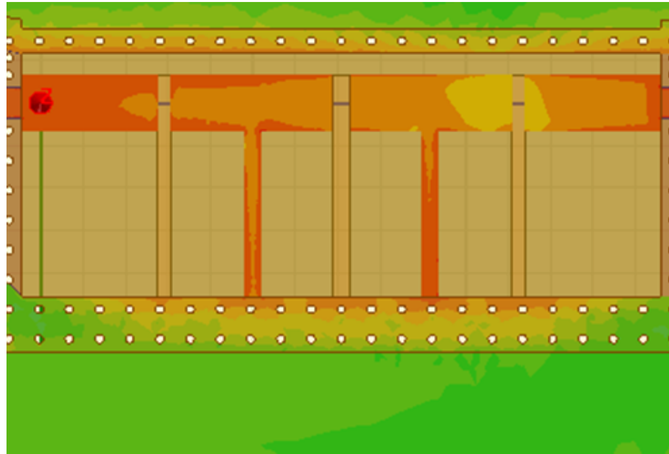


Figure 4.26: Top-down view of the proposed SISL HPF design showing the current density on M5 after adding the second row of grounding vias.

current density on M5 is shown in Fig. 4.26. Notice how the extended ground plane is clear of any hot-spots; therefore, the associated resonance at 10 GHz should be fixed. The simulated S-parameters for the double via stitched design are shown in Fig. 4.27 and the 10 GHz resonance has been eliminated.

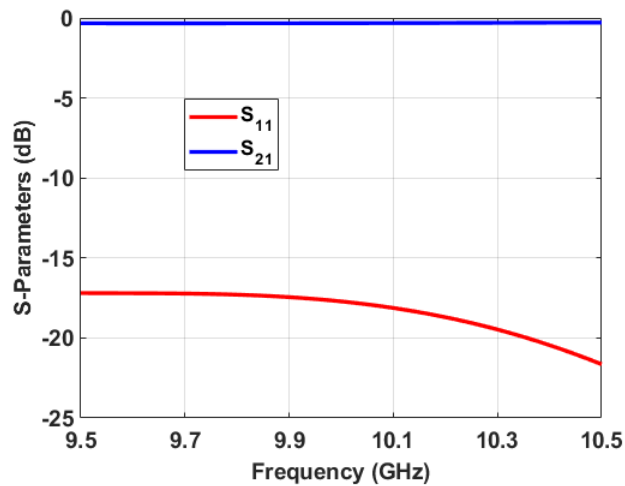


Figure 4.27: Simulated S-parameters after adding the second row of stitching vias.

4.2 2 GHz SISL HPF Simulations

Once the design has been modeled in HFSS and verification of the cavity dimensions has been completed, the final HFSS model is simulated. The SISL HPF model uses two wave port excitations renormalized to 50 ohms. The 20 GHz bandwidth is is broken up into 5 simulations each covering 4 GHz of bandwidth. The driven solution is set with a maximum delta S of 0.01 and 5 minimum converged passes. The plots are only shown up to 18 GHz since that is the highest frequency of interest. The simulated S-parameters are shown in Fig. 4.28.

The simulated loss is 0.7766 dB at the 2 GHz cutoff frequency. This agrees very well with the expected insertion loss of 0.7494 dB, which is calculated adding the simulated insertion loss of each individual section. The breakdown of this 0.7494 dB loss is as follows:

1. 0.1156 dB is due to the CPWG traces,

2. 0.0630 dB is due to the stripline traces,

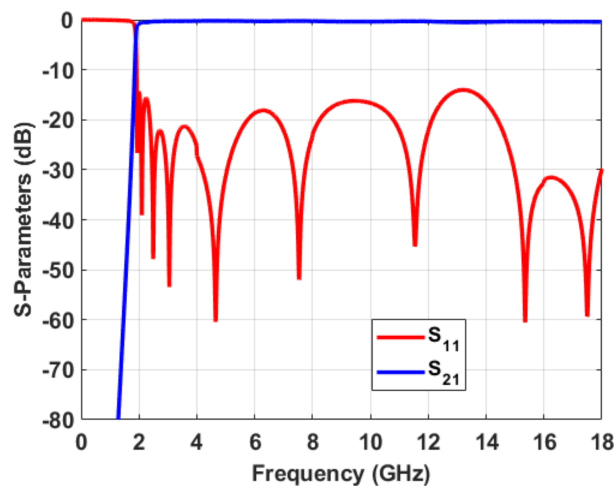


Figure 4.28: HFSS simulated S-parameters of the proposed 2 GHz SISL HPF.

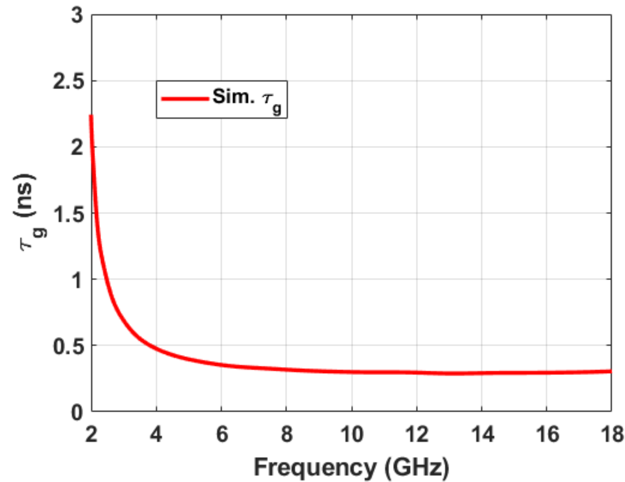


Figure 4.29: HFSS simulated group delay of the proposed SISL HPF.

3. 0.0142 dB is due to the connectors,

4. 0.0167 dB is due to the via transitions,

5. 0.5399 dB is due to the SISL HPF.

The slight difference between the expected S_{21} (0.7494 dB) and the full-model simulated S_{21} (0.7766 dB) is more than likely due to a minor mismatch from the stripline and SISL transition.

The HFSS simulated group delay of the proposed SISL HPF is shown in Fig. 4.29. The maximum delay is 2.22 ns at 2 GHz with an average delay of 0.304 ns beyond 3 GHz.

4.3 Layout File Generation and Device Fabrication

The layout files are generated the same way as the thru-line and LPF discussed in Section 2.3. The HPF devices are fabricated by ACE (Accurate Circuit Engineering) [109]. The primary difference between the in-house and professional circuit fabrication is the silver immersion process to prevent the copper from

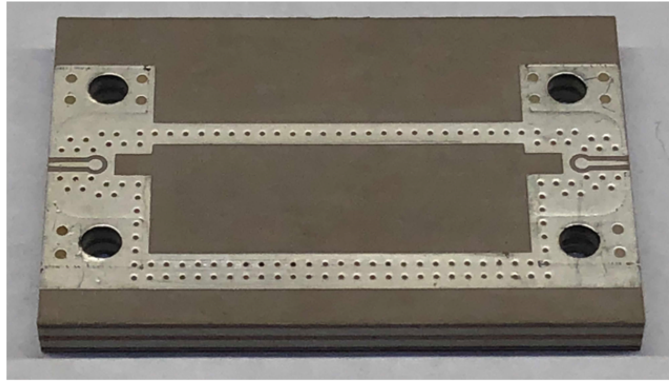


Figure 4.30: Photograph of the fabricated 2 GHz SISL HPF.

oxidizing. Fig. 4.30 is a photograph of the of the fabricated fully-board embedded 2 GHz SISL HPF. The overall size of the of the fabricated component is 2.88 x 1.91 x 0.23 cm^3. The SISL HPF itself is only 1.85 x 0.62 x 0.22 cm^3.

4.4 Measured Results

The fabricated 2 GHz SISL HPF is measured using an Agilent Technologies N5225A PNA that has been calibrated using an Agilent Technologies N4691-60006 electronic calibration module. Fig. 4.31 plots the simulated and measured S-parameters. The simulated and measured results show good agreement all the way up to 18 GHz. The measured insertion loss is less than 0.86 dB at 2 GHz with greater than 10.25 dB of return loss across the entire passband. The filter portrays phenomenal stopband performance achieving greater than 55 dB of stopband suppression by 1.5 GHz. Analyzing the return loss at the cutoff frequency, there is an additional 0.0787 dB of mismatch loss. This mismatch loss can be added to the 0.7766 dB of simulated loss resulting in an expected insertion loss of 0.8553 dB, which agrees well with the measured insertion loss.

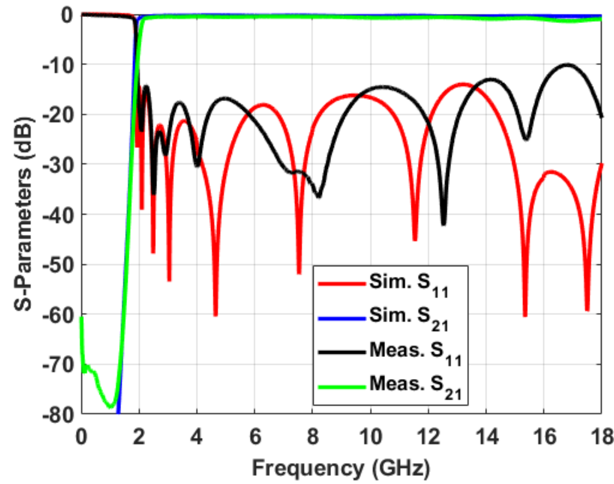


Figure 4.31: Simulated and measured S-parameters of the proposed SISL HPF.

The group delay of the SISL HPF is also measured and plotted with the simulated group delay in Fig. 4.32. The group delays shows excellent agreement. The measured group delay is very small across the passband, but reaches 2.624 ns at the 2 GHz cutoff frequency. This is due to the incredibly sharp roll-off of the HPF. Beyond 3 GHz, the group delay is exceptionally flat with an average delay of 0.318 ns.

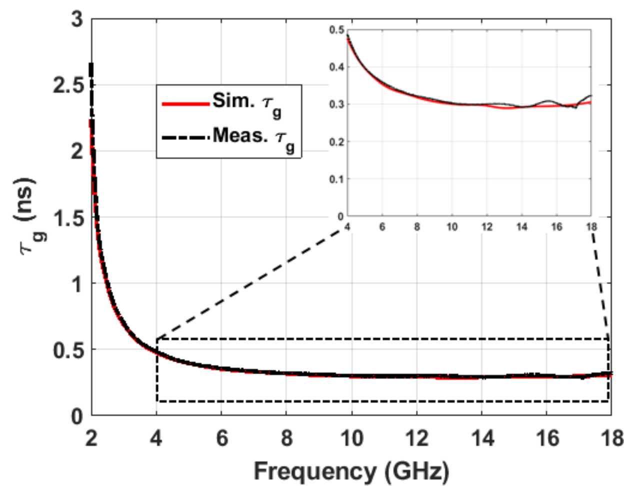


Figure 4.32: Simulated and measured group delay of the proposed SISL HPF.

Chapter 5

SISL Cascaded Bandpass Filter Design

The purpose of Chapter 5 is to apply the fully-board embedded SISL technology to the design of microwave cascaded bandpass filters. This chapter will offer design guidelines to internally cascade a LPF and HPF to minimize size while achieving wideband performance. As a design example, the previously designed eleventh-order generalized Chebyshev DC-18 GHz LPF and 2 GHz HPF are cascaded to develop a 2-18 GHz BPF. The end result is a first time demonstration of a fully-board embedded SISL cascaded bandpass filter design and first time demonstration of a self-packaged suspended line octo-octave BPF.

5.1 SISL BPF Design

Fig. 5.1 shows the exploded view of the proposed cascaded BPF using the fully-board embedded SISL technology. A bottom looking view of the exploded stack-up is shown in Fig. 5.2 to show the BCS of the HPF. The PCB stack-up is identical to the one used for the thru-line, LPF, and HPF discussed in Section 2.1.1. This allows for the LPF and HPF to be cascaded with no modifications to the filter designs. Therefore, the LPF and HPF can be internally cascaded with a stripline trace and then the effective BPF can be placed between two

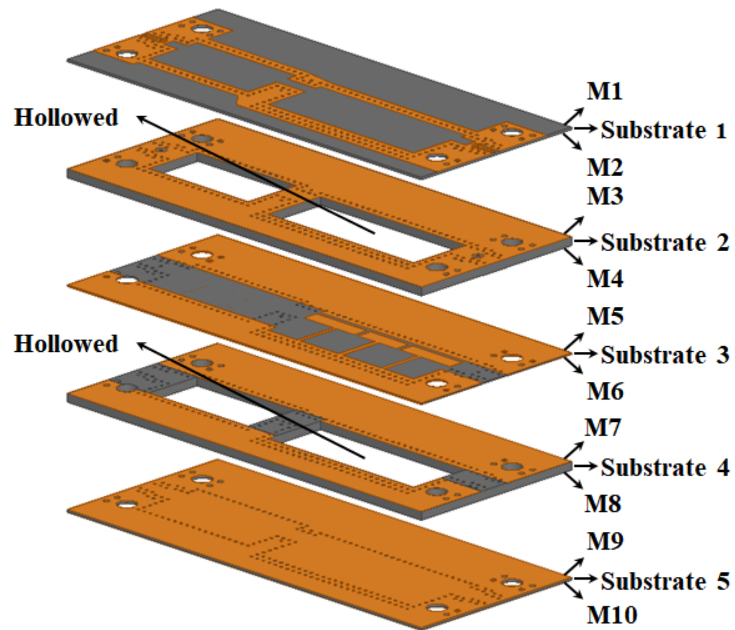


Figure 5.1: 3-D exploded view of the proposed cascaded Chebyshev SISL BPF.

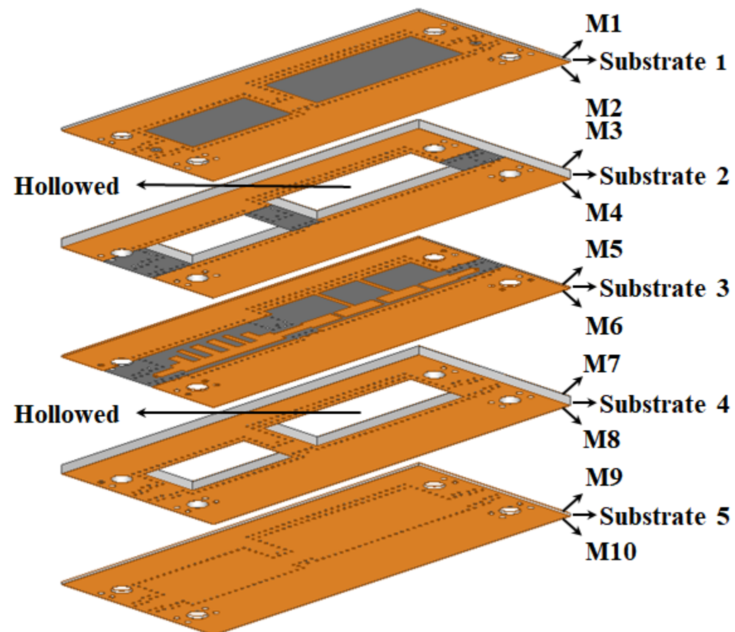


Figure 5.2: Bottom 3-D exploded view of the proposed cascaded Chebyshev SISL BPF.

vertical via transitions.

Assuming the vertical via transitions, LPF, and HPF are already designed, the design procedure is completed as follows:

1. Cascade the LPF and HPF with a stripline trace.

2. Place the cascaded BPF design between two vertical via transitions.

3. Simulate the final SISL design.

4. Generate Gerber files from HFSS model.

After the design procedure is completed, the device is ready for fabrication using the fabrication procedure in Appendix A. The filters are then connectorized and connected to a calibrated PNA for S-parameter measurements.

5.1.1 Stripline Trace for Internal Cascade

Traditionally, filters are cascaded by using a connectorized adapter between them. But this inherently increases SWaP and not ideal for the current SISL implementation. Using the previous SISL technology [58], the filters could be cascaded by connecting the filters with the microstrip trace in between PCB caps. This approach could be used for the fully-board embedded design by bringing the signal back to M1 after the LPF and then repeat the process for the HPF. However, adding vertical via transitions not only increases the size and complexity of the cascaded BPF, but also adds additional unnecessary loss by transitioning two more times than needed. The ideal approach is to internally cascade the LPF and HPF with a stripline trace. Therefore, the output of the LPF goes straight into the HPF minimizing loss and reducing overall complexity.

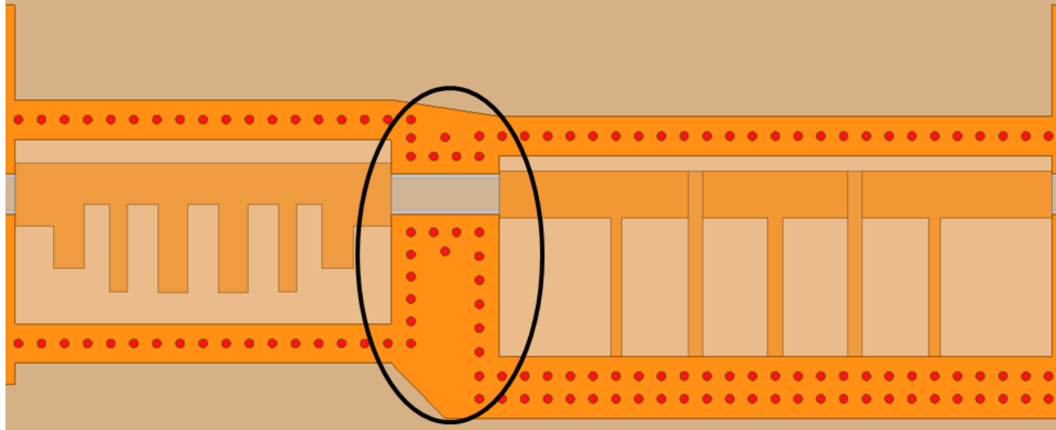


Figure 5.3: Top-down and zoomed-in view of the proposed cascaded SISL BPF.

Because the stack-up is the same throughout the entire BPF design, the same stripline trace designed in Section 2.1.3 can be used. A top-down zoomed-in view of the internal cascade section is shown in Fig. 5.3. It is important to use the same via spacing and arrangement that is used for the vertical via transition to make sure parallel-plate modes are not excited in this cascade region. Ideally, the length of the stripine trace is zero, but directly cascading the filters would create a very large cavity with no support and would cause bowing issues. The next best length is $\lambda/2$ at the center frequency of the BPF to place a deep null in the return loss and maximize the match. However, this technique for wideband filters is not very effective and increases the length of the stripline trace. For this design, the stripline trace is 155 mils, which provides the same overall passband return loss but slightly shifts the nulls in frequency.

5.2 2-18 GHz SISL BPF Simulations

The design of the 2-18 GHz cascaded SISL BPF is finished by placing the cascaded filters between two vertical via transitions. The proposed SISL BPF is shown in Fig. 5.4. At this point, there is no need to tune the air cavities since this has already been done during the design of the individual LPF and HPF. Also, since the filters are designed for 50 ohm terminations, and the internal stripline is designed for 50 ohms, there are no modifications to the filter designs in the final cascaded design.

The cascaded SISL BPF model uses two wave port excitations renormalized to 50 ohms located at the reference plane of the edge-launch connectors. The 26 GHz bandwidth is broken up into 7 simulations with the first six each covering 4 GHz of bandwidth and the last simulation covering 2 GHz of bandwidth. The driven solution is set with a maximum delta of 0.01 and 5 minimum converged passed. The simulated S-parameters and group delay are shown in Figs. 5.5 and 5.6, respectively. The simulated insertion loss is less than 0.85 dB and the simulated return loss is greater than 15.5 dB across the 2-18 GHz passband. The average group delay is 0.429 ns across the 2-18 GHz passband.

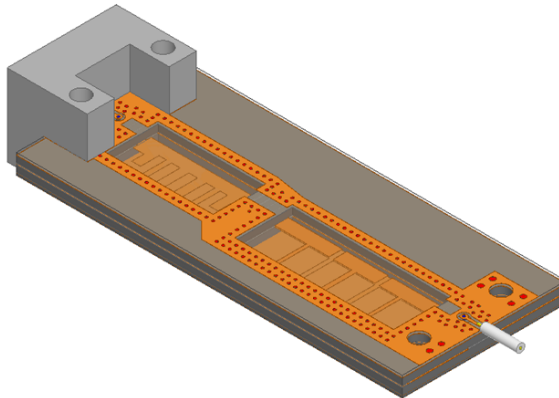


Figure 5.4: 3-D view of the proposed 2-18 GHz cascaded SISL BPF.

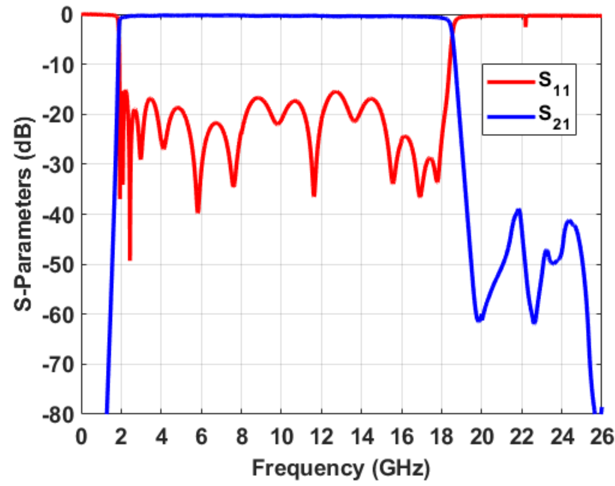


Figure 5.5: HFSS simulated S-parameters of the proposed 2-18 GHz cascaded SISL BPF.

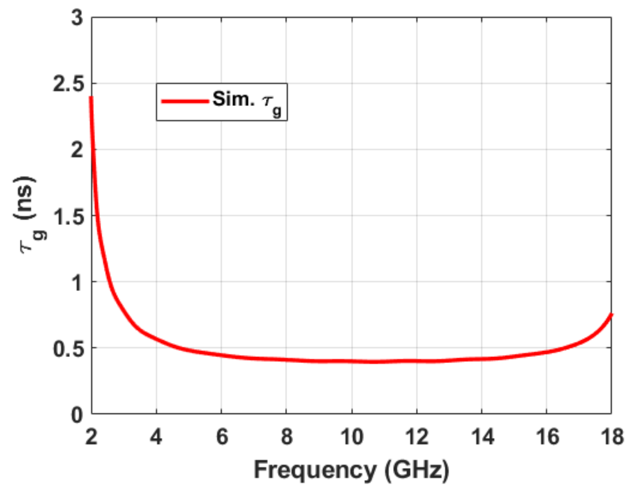


Figure 5.6: HFSS simulated group delay of the proposed 2-18 GHz cascaded SISL BPF.

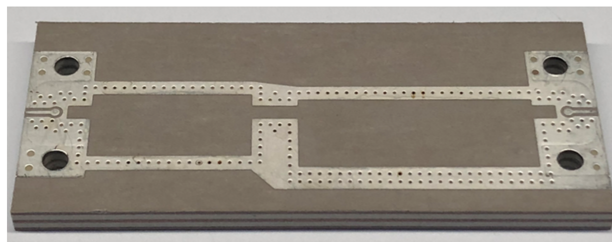


Figure 5.7: Photograph of the fabricated 2-18 GHz cascaded SISL BPF.

5.3 Layout File Generation and Device Fabrication

The layout files are generated the same way as the thru-line, LPF, and HPF discussed in Section 2.3. The BPF devices are fabricated by ACE (Accurate Circuit Engineering) [109]. Fig. 5.7 is a photograph of the of the fabricated fully-board embedded 2-18 GHz cascaded SISL BPF. The overall size of the of the fabricated component is 4.49 x 1.91 x 0.23 cm^3. The SISL BPF section, including the internal stripline trace to cascade the LPF and HPF, is only 3.47 x 0.73 x 0.22 cm^3.

5.4 Measured Results

The fabricated 2-18 GHz cascaded SISL BPF is measured using an Agilent Technologies N5225A PNA that has been calibrated using an Agilent Technologies N4691-60006 electronic calibration module. Fig. 5.8 plots the simulated and measured S-parameters. The simulated and measured results show good agreement. The measured insertion loss is less than 1.1 dB with greater

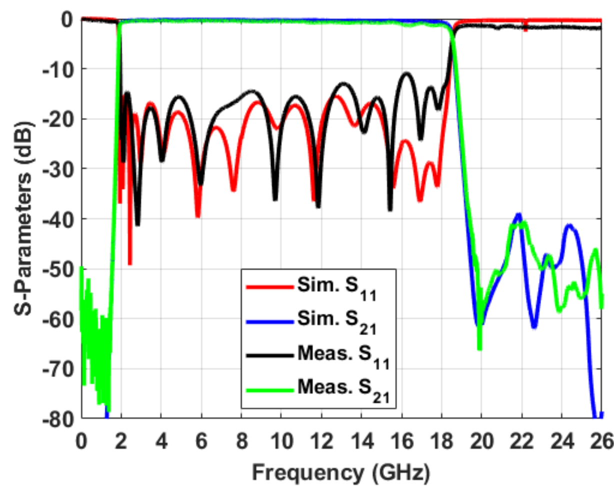


Figure 5.8: Simulated and measured S-parameters of the proposed cascaded SISL BPF.

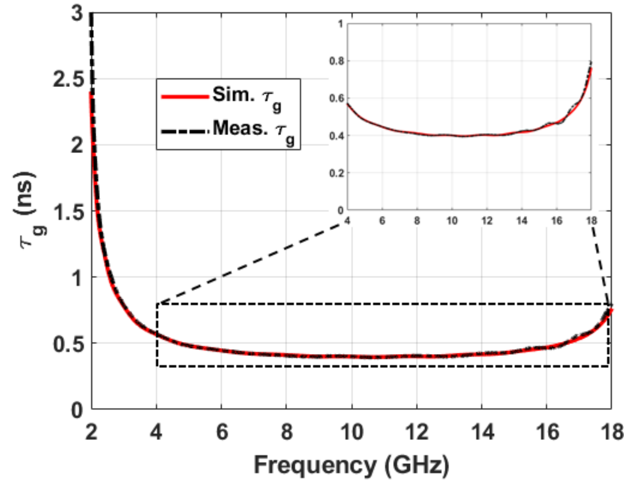


Figure 5.9: Simulated and measured group delay of the proposed cascaded SISL BPF.

than 11 dB of return loss across the entire 2-18 GHz passband. The filter's stopband performance has greater than 55 dB of stopband suppression by 1.5 GHz and 40 dB of attenuation from 19-26 GHz. Analyzing the return loss at the cutoff frequency, there is an additional 0.2098 dB of mismatch loss. This mismatch loss can be added to the 0.85 dB of simulated loss resulting in an expected insertion loss of 1.059 dB, which agrees well with the measured insertion loss.

The group delay of the cascaded SISL BPF is also measured and plotted with the simulated group delay in Fig. 5.9. The group delays show excellent agreement. The measured group delay is very small across the passband reaching 2.977 ns at 2 GHz and 0.795 ns at 18 GHz. From 2 GHz to 18 GHz, the group delay is exceptionally flat with an average delay of 0.462 ns.

Chapter 6

Frequency Scaling of SISL Design to Ka-band

The purpose of Chapter 6 is to evaluate the frequency scalability of the proposed SISL technology. As a demonstrator, a DC-40 GHz thru-line and a series of Ka-band filters are designed including a 28 GHz HPF, 32 GHz LPF, and cascaded 28-32 GHz bandpass filter. This frequency range is chosen due to its attractiveness for remote sensing, weather radar, and next generation 5G telecommunications. The end result is a first time demonstration of a self-packaged suspended line technology up to Ka-band and first time demonstration of a fully-board embedded Ka-band LPF, HPF, and BPF.

6.1 Ka-Band SISL Thru-line and Filter Design

Fig. 6.1 shows the exploded 3-D view of the proposed Ka-band thru-line using the integrated SISL technology. Note that the metal layers are labeled with an L instead of an M. This is purposefully done to avoid confusion between the Ku- and Ka-band designs. There are five individual laminate substrate layers that comprise the multi-layer PCB stack-up. The air cavities of the SISL structure are created by hollowing out Substrate 2 and Substrate 4 around the SISL thru-line and filters similar to the Ku-band design. The laminate substrates shown in Fig. 6.1 are chosen as follows: Substrate 1 and Substrate

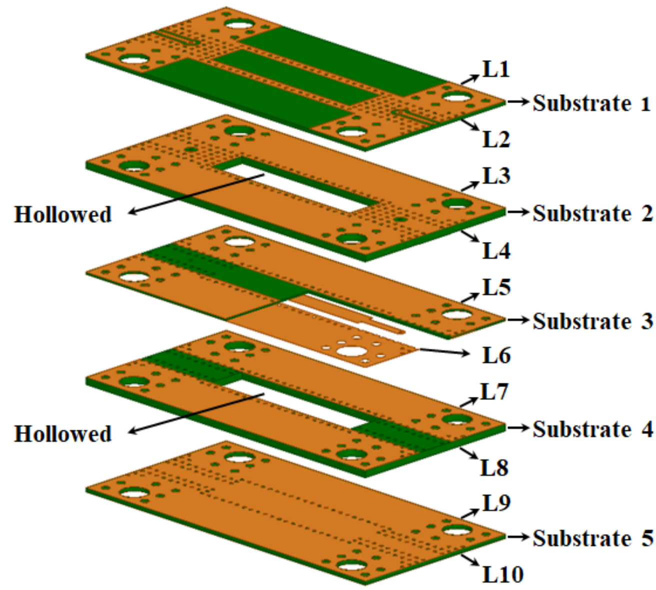


Figure 6.1: 3-D exploded view of the proposed Ka-band SISL technology.

5 are 10-mil-thick Rogers RT/duroid® 6006 microwave laminate substrates ($\epsilon_r = 6.15$ and $\tan\delta = 0.0027$). Substrate 2 and Substrate 4 are 15-mil-thick Rogers RT/duroid® 6002 ($\epsilon_r = 2.94$ and $\tan\delta = 0.0012$), and Substrate 3 is 5-mil-thick Rogers RT/duroid® 6002. Substrates 2 and 4 are thinner in order to increase the cutoff frequency of the vertical via transition, which will be further discussed in Section 6.1.1. The two SISL cavities have an individual height of 15 mil, which is the corresponding thickness of Substrates 2 and 4. The metalized side-walls are still created by arranging plated through vias

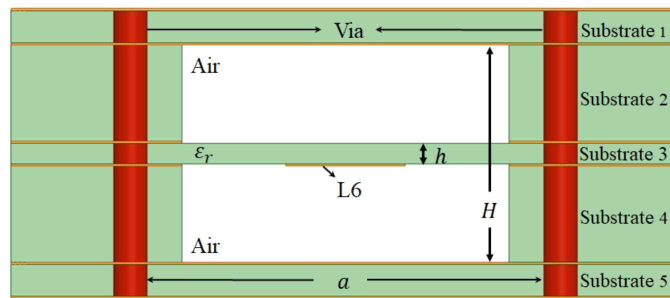


Figure 6.2: Cross-sectional view of the proposed Ka-band SISL technology.

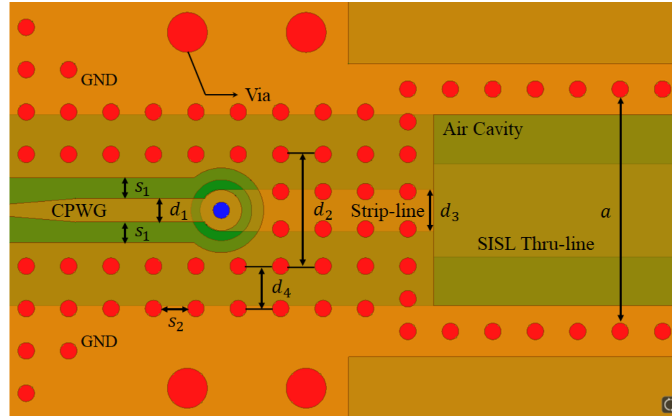


Figure 6.3: Top-view of the proposed SISL technology to illustrate L1.

around the air cavity. The center-to-center via spacing is minimized to ensure an effectively constant side-wall and reduce the loss due to leakage [78]. Fig. 2 shows the cross-sectional view of the proposed SISL thru-line to further illustrate the substrate and metal layers as well as the air cavities.

L10 is a metal layer, and L2 and L9 are the ground layers for both the suspended stripline and stripline. Both the thru-line and filters are designed on metal layer L6 inside of the air cavity. A section of L5 and Substrate 3 have been removed in Fig. 6.1 to reveal L6. L1 is the top metal layer, shown with more detail in Fig. 6.3, which contains the CPWG microwave trace. The CPWG trace provides signal routing from the vertical via transition to other microwave components in an extended circuit. Because an edge launch connector is used for testing purposes, the CPWG trace is tapered at the input and output to compensate for the capacitive loading of the center pin as discussed in Section 2.1.2.

In the following subsections, discussion on the vertical via transition, thru-line, and each filter (LPF, HPF, and BPF) are given. Some design guidelines and integration techniques will be discussed to frequency scale the integrated SISL design for Ka-band operation. It should be noted that the thru-line and

filters are designed separately from the via transition and then brought together for the individual final designs. Recall, the waves in the stripline and suspended stripline are both propagating in TEM-mode; therefore, there is no need for special via placement or tapering at the stripline to SISL boundary. Therefore, if the vertical via transition is designed to a characteristic impedance of 50 ohms, as well as the input and output ports of the thru-line and filters, the designs will be appropriately matched and can be attached together with minimum alterations to the overall design.

6.1.1 Ka-band Vertical Via Transition

Fig. 6.4 shows the ANSYS HFSS model of the Ka-band vertical via transition. In order to achieve up to 40 GHz of operation, a few modifications to the original design in [112] had to be made as follows: reduction in the air cavity height, movement of SISL structure from L5 to L6, minimize both the stripline via spacing (d_2) and SISL via spacing (a), and either add blind vias between L1 and L2 or remove sections of L1 for Substrate 1 waveguide-mode cancellation.

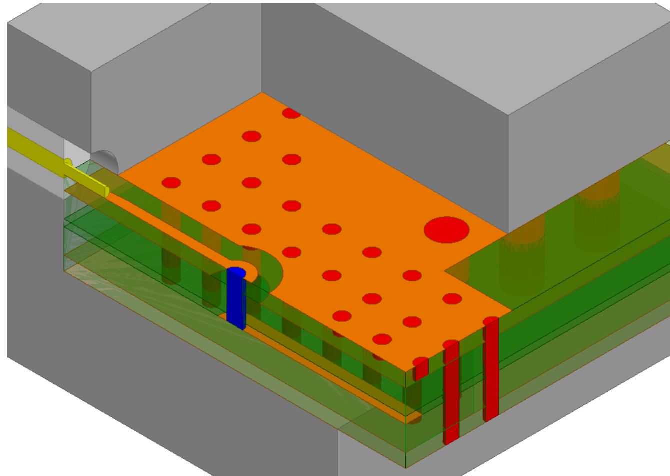


Figure 6.4: 3-D view of the vertical via transition including edge-launch connector.

Furthermore, a second row of plated through vias around the SISL air cavity and extra ground plane vias are added to suppress resonances on the extended ground plane. Each of these topics are further discussed below.

The vertical via transition in Fig. 6.4 can effectively be modeled as a low pass filter, which was discussed in Section 2.1.4. The series inductance is attributed to the inductive reactance of the via, which becomes increasingly large with higher operating frequencies. Special consideration of the via length must be taken into account to make sure the cut-off frequency of the transition is higher than the intended operating frequency. By shortening the via length, the inductance of the via can be reduced. Therefore, the air cavity height must be minimized to increase the cut-off frequency, but simultaneously maximized to ensure TEM-mode propagation in the suspended line. Simulations in Keysight's ADS showed that the standard 15-mil-thick Rogers 6002 laminate would be sufficient for Substrates 2 and 4 given a 12 mil via diameter.

If a high dielectric constant material is used for the entire material stack-up, the via length might needed to be further reduced to avoid resonating at its $\lambda/2$ length. As the dielectric constant increases, the half-wave resonance decreases for the same given length. Therefore, the via length should be short enough that the half-wave resonance occurs beyond the intended operating frequency, and does not degrade the passband performance of the SISL component.

The next modification is moving the stripline and SISL design to L6. For the Ku-band builds, the strip line and SISL designs could be placed on either M5 or M6, but for Ka-band they are required to be placed on L6. To achieve the design in [112], a sequential lamination process was performed. After patterning L2, L5, and L6 using photolithography, substrates 1 to 3 are laminated together creating the first sub-assembly. At this point, the blind

signal via connecting the CPWG trace to the internal stripline is drilled and followed by a copper plating process. Because the blind via extends all the way through the first sub-assembly, a copper annulus on L6 is required to successfully plate the blind via. This annulus acts as a shunt parasitic capacitance, which just like the via inductance, can be thought of as a low pass filter with some cut-off frequency. At Ka-band, the annulus had to have essentially the same diameter as the blind via in order to operate up to 40 GHz. To overcome this constraint, the stripline and SISL design were moved to L6, and the end of the stripline trace is rounded off to create the copper annulus for via plating. This technique eliminates the parasitic shunt capacitance and extends the frequency range.

While designing the stripline trace and the SISL air cavity, special attention must be given to the stripline via-stitching separation (d_2) and SISL cavity width (a), both shown in Fig. 6.3, to ensure no parasitic waveguide modes will be excited. For the stripline trace, via-stitching is used to suppress parallel-plates modes and increase bandwidth. The via separation should be maximized to ensure that the characteristic impedance is not perturbed; however, the spacing should be minimized so that a rectangular TE_{10} mode will not be excited and propagate. Given a maximum frequency of operation (f_c), the maximum via separation can be calculated as [50]

$$d_{2,max} = \frac{c}{2f_c\sqrt{\epsilon_r}} \tag{6.1}$$

where c is the speed of light and ϵ_r is the relative permittivity of Substrates 2 to 4. An identical phenomena will occur inside the SISL air cavity due to the metalized side-wall vias as discussed in Section 2.1.7. During the design of the thru-line, a resonance at roughly 38.75 GHz was observed affecting the

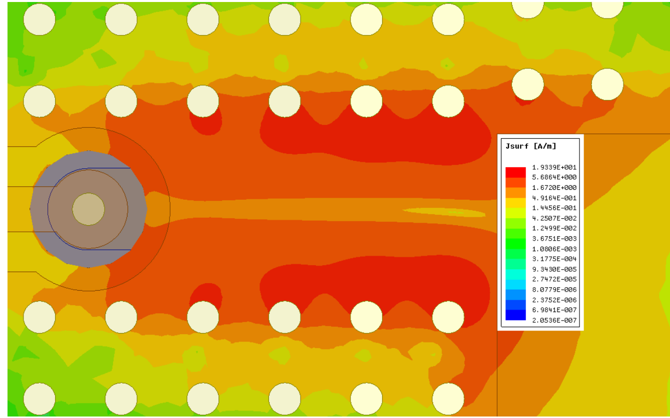


Figure 6.5: Current density plot on L2 without blind vias or modified L1.

desired 40 GHz performance. After analyzing the ANSYS HFSS model at the resonant frequency, a strong current density on L2 between the via stitching was noticed as shown in Fig. 6.5. This resonance is caused by the fields coupling into Substrate 1 as the signal propagates down the vertical signal via, and resonating between the plated through-vias used for via-stitching the stripline. Since the relative permittivity of Substrate 1 is much higher than that of Substrates 2 to 4, the resonance according to (6.1) will occur much lower in frequency. In this case, the calculated resonant frequency is 38.8 GHz; therefore, the expected issue on L2 is confirmed mathematically. The plated though-vias along this section can not be brought closer together as that will short the internal stripline. However, additional blind vias from L1 to L2 can be added between the plated-through vias, which will reduce the overall via separation in Substrate 1 (d_3) and push the parasitic mode out of the passband. Fig. 6.6 shows the current density at the original resonant frequency with the introduction of blind vias.

Although the blind vias connecting L1 and L2 fix the issue in Substrate 1, they add another processing step and greatly increases the fabrication cost and complexity. Another solution, which is much easier to implement and

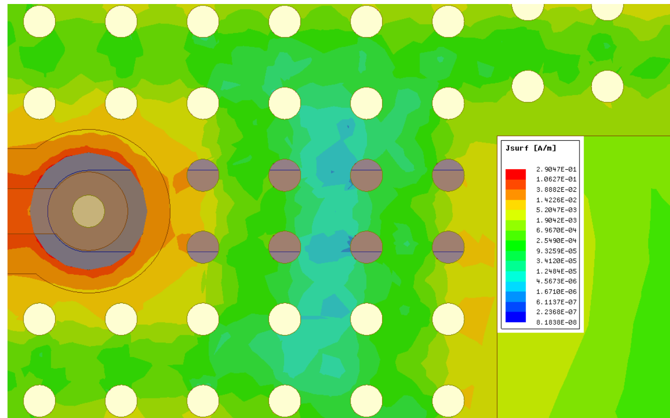


Figure 6.6: Current density plot on L2 with blind vias.

cheaper, is to simply remove some copper from L1 in the problem area. This modification is highlighted in Fig. 6.7. The HFSS model with L1 modifications is re-simulated and the current density on L2 is plotted to verify that the resonance is gone. The current density is shown in Fig. 6.8. By removing the copper from L1, the upper boundary condition is removed and the waveguide resonance is suppressed.

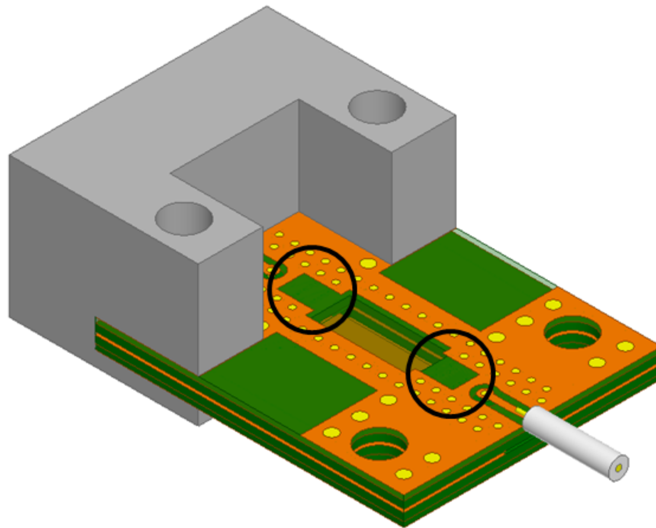


Figure 6.7: 3-D view of the SISL technology with L1 modifications to avoid waveguide resonance in Substrate 1.

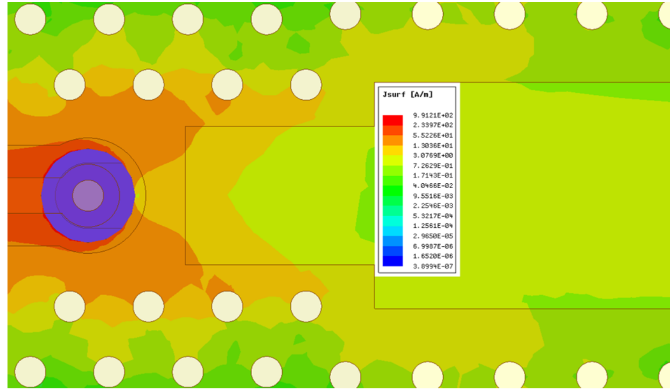


Figure 6.8: Current density plot on L2 with modification to L1.

In the HPF design, a second row of stitching vias had to be placed around the SISL air cavity where the shunt short-circuit stubs attached to the ground plane. This was done to ground any fields that coupled onto the ground plane that could was unwanted resonances. For the Ka-band filter designs, the SISL components are very close to the ground plane since the air cavity width has to be significantly reduced to avoid parasitic waveguide modes. Moreover, parasitic coupling at these frequencies is more prevalent further compounding the issue. Therefore, a second row of vias were used to ensure a more constant and effective side-wall. Lastly, a few 1.6 mm diameter plated through-vias are placed along the extended ground plane to ensure any remaining electromagnetic fields are sufficiently grounded.

Given all of the design constraints, guidelines, and techniques listed above, the vertical via transition is designed for up to 40 GHz operation. The CPWG and stripline traces are designed separately each with a characteristic impedance of 50 ohms. The CPWG trace dimensions, shown in Fig. 6.3 as d_1 and s_1, are tuned to 13.7 and 12.3 mils, respectively. To ensure equi-potential up to 40 GHz along the CPWG trace, via-stitching parallel to the trace is implemented. The vias are 0.3 mm in diameter with $s_2 = 15$ mils of edge to edge

via spacing. Moreover, the width between the stitching vias is $d_2 = 56$ mils. A second row of vias are placed $d_4 = 25$ mils apart to suppress any parallel plate mode coupling on the extended ground plane. The same via configuration is used for the stripline stitching vias placing the first parasitic waveguide mode at roughly 61.5 GHz, which is significantly higher than the required 40 GHz. Including the effects of the stitching vias, the stripline width is tuned to $d_3 =$ 25 mils. Finally, all metal layers are set as 1/2 oz. copper with a conductivity of $5.8\text{x}10^7$ S/m.

6.1.2 Ka-band SISL Thru-line Design

Fig. 6.9 shows the ANSYS HFSS model of the Ka-band thru-line. Given a cavity height of $H = 35$ mils, the effective relative permittivity is found to be 1.279. Using the technique discussed in Section 2.1.5, the width is tuned in Keysight's ADS to 45 mils. The total length of the thru-line is 500 mils long. The side-wall vias were placed with a separation of $a = 115$ mils. Using

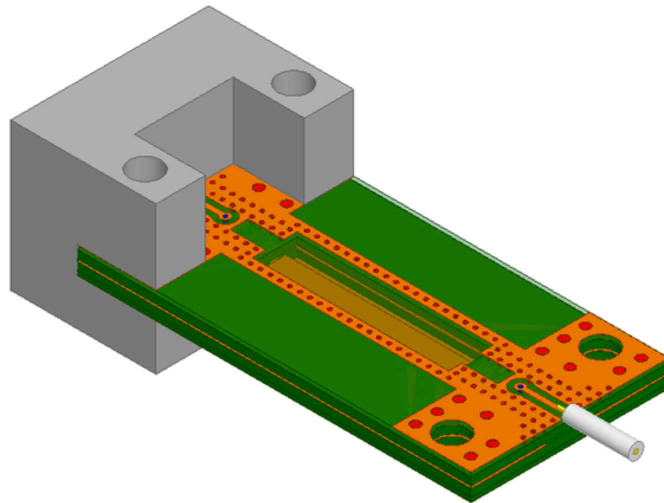


Figure 6.9: 3-D view of the HFSS Ka-band SISL thru-line model.

(2.6) and (2.7), the waveguide cutoff and resonant frequency are calculated to be 45.4 and 46.6 GHz, respectively, both well above the 40 GHz passband. The SISL thru-line section was attached to the vertical via transitions with minimum design modifications.

6.1.3 Ka-band SISL Chebyshev LPF Design

Fig. 6.10 shows the ANSYS HFSS model of the Ka-band Chebyshev LPF. An eleventh-order generalized Chebyshev LPF, with a 32 GHz cutoff frequency, is designed using the same design procedure discussed in Chapter 3. The filter is tuned to provide optimal performance over the 28-32 GHz passband frequency range since that is the frequency passband of interest. The LPF layout representation with variables is provided in Fig. 6.11 and the corresponding distributed filter parameters are shown in Table 6.1.

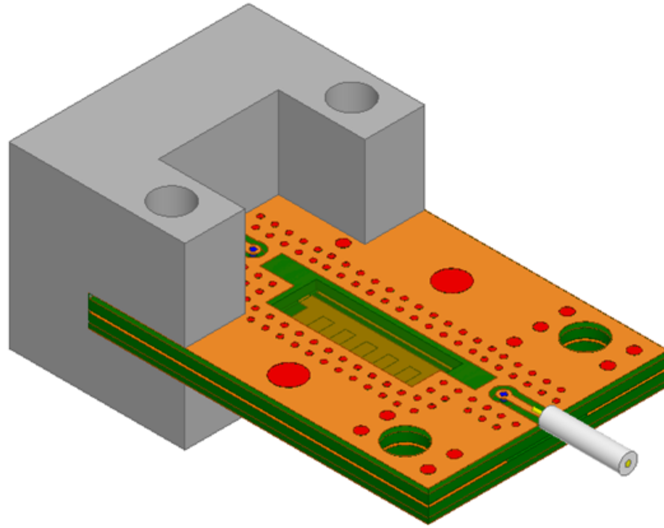


Figure 6.10: 3-D view of the HFSS Ka-band SISL Chebyshev LPF model.

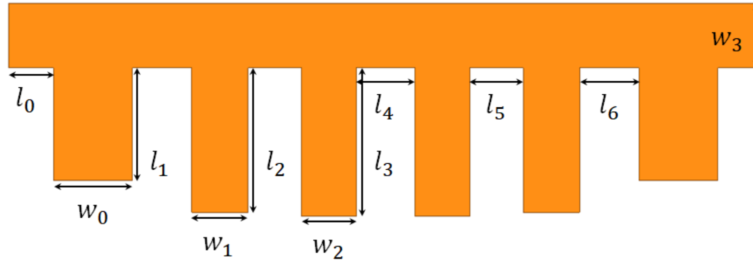


Figure 6.11: Layout representation of the distributed generalized Chebyshev LPF.

Table 6.1: Final LPF distributed parameters.

Variable	Length (mil)	Variable	Length (mil)
w_0	33.71	w_1	22.80
w_2	22.15	w_3	26.18
l_0	18.05	l_1	45.59
l_2	58.39	l_3	60.05
l_4	23.81	l_5	22.68
l_6	23.97		

6.1.4 Ka-band SISL Chebyshev HPF Design

Fig. 6.12 shows the ANSYS HFSS model of the Ka-band Chebyshev HPF. An eleventh-order generalized Chebyshev HPF, with a 28 GHz cutoff frequency, is designed using a similar design procedure discussed in Chapter 4. The HPF is also tuned to provide optimal performance over the 28-32 GHz passband frequency range. The HPF layout representation with variables is provided in Fig. 6.13 and the corresponding distributed filter parameters are shown in Table 6.2. Lastly, because the width of the SISL air cavity is so narrow, a decent amount of the fields couple onto the extended ground plane. Although a double row of grounding vias are used, larger grounding vias are placed beyond to ensure equipotential grounding.

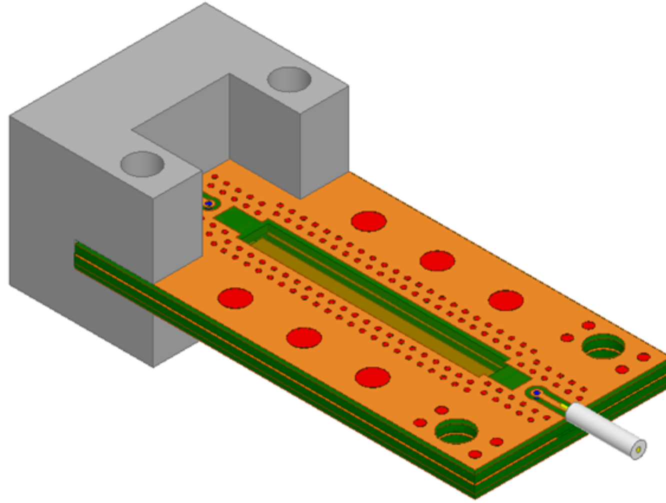


Figure 6.12: 3-D view of the HFSS Ka-band SISL Chebyshev HPF model.

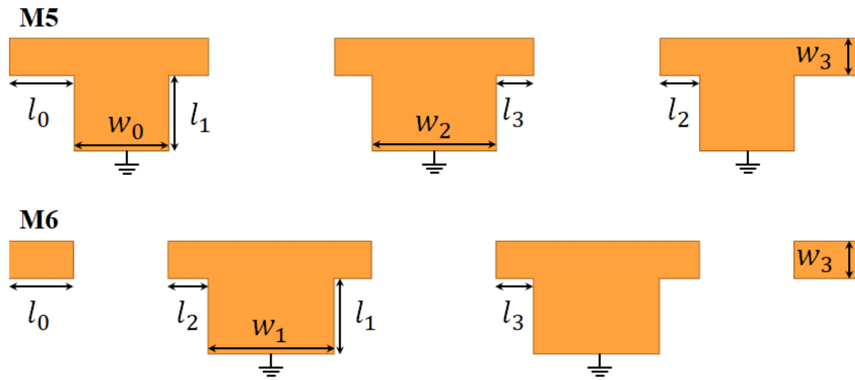


Figure 6.13: Layout representation of the distributed generalized Chebyshev HPF.

Table 6.2: Final HPF distributed parameters.

Variable	Length (mil)	Variable	Length (mil)
w_0	35.42	w_1	47.40
w_2	46.76	w_3	15.00
l_0	24.33	l_1	28.44
l_2	14.97	l_3	14.05

6.1.5 Ka-band SISL Chebyshev BPF Design

Fig. 6.14 shows the ANSYS HFSS model of the Ka-band Chebyshev BPF. The LPF and HPF are cascaded and connected by a $L = 155$ mil long stripline trace with a width of $W = 25$ mil, which is identical to the input and output stripline trace. This length of stripline is approximately $3\lambda/2$ creating an excellent match at 30 GHz. Because the LPF and HPF are designed for 50 ohm terminations, the filter dimensions are unchanged. The BPF layout representation with variables is provided in Fig. 6.15.

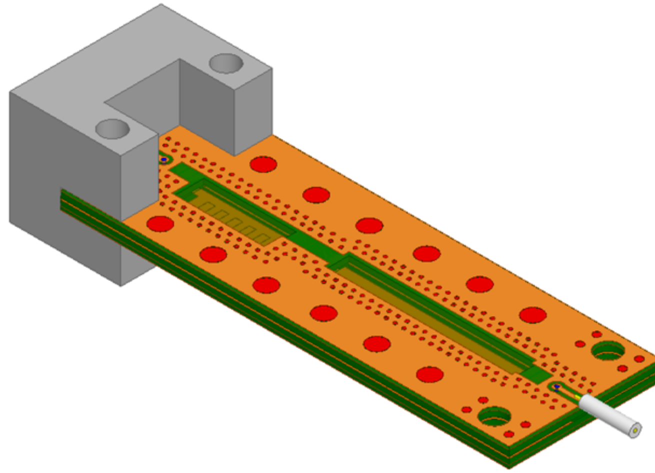


Figure 6.14: 3-D view of the HFSS Ka-band SISL Chebyshev BPF model.

Figure 6.15: Layout representation of the distributed generalized Chebyshev BPF.

6.2 Simulated Results

All of the Ka-band designs are simulated in HFSS. The models use two wave port excitations renormalized to 50 ohms placed at the reference plane of the edge-launch connectors. Each solution setup is set with a maximum delta of 0.01 and 5 minimum converged passes.

6.2.1 Ka-band SISL Thru-line

The fully-board embedded Ka-band SISL thru-line S-parameters are shown in Fig. 6.16 The simulated insertion loss is less than 1.20 dB and the simulated return loss is greater than 9.5 dB across the entire 40 GHz passband, including the vertical via transition and edge-launch connectors. These simulated results are promising and indicate that resonant-free passbands up to 40 GHz are achievable with good performance.

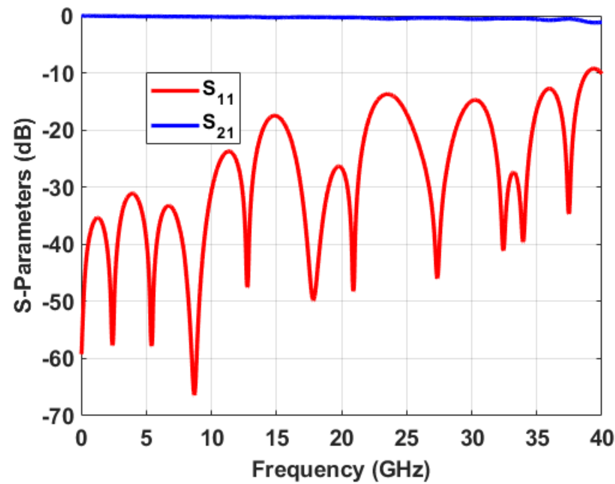


Figure 6.16: Simulated S-parameters of the proposed Ka-band SISL thru-line.

6.2.2 Ka-band SISL Chebyshev LPF

The fully-board embedded Ka-band SISL Chebyshev LPF S-parameters and group delay are shown in Figs. 6.17 and 6.18, respectively. The simulated insertion loss is less than 0.9 dB and the simulated return loss is greater than 17.0 dB across the 28-32 GHz passband, including the vertical via transition and edge-launch connectors. The passband provides greater than 35 dB of

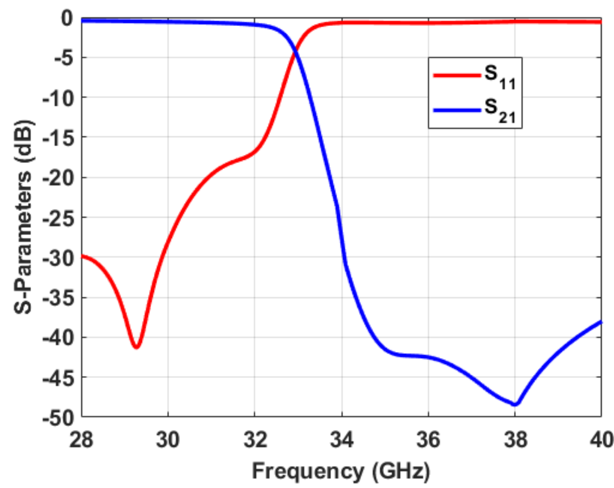


Figure 6.17: Simulated S-parameters of the proposed Ka-band SISL Chebyshev LPF.

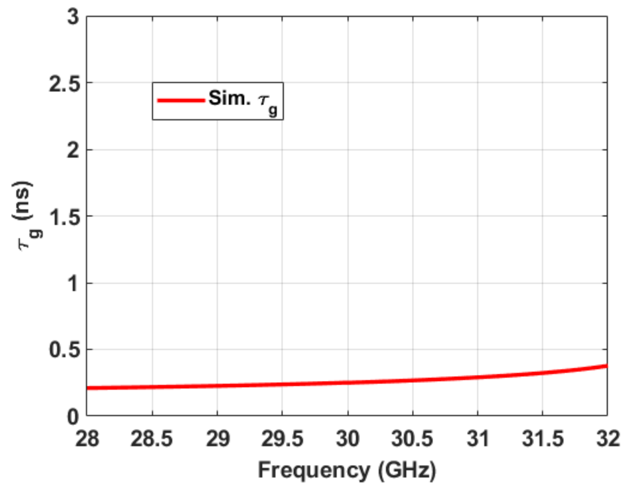


Figure 6.18: Simulated group delay of the proposed Ka-band Chebyshev LPF.

attenuation up to 40 GHz, which can be extended further by incorporating a defected ground structure at the resonant frequency of the cavity. Fig. 6.18 shows the simulated group delay over the 28-32 GHz passband. The simulated group delay is small across the entire 28-32 GHz passband reaching a maximum delay of only 0.377 ns at the 32 GHz cutoff frequency. The group delay is very flat with an average delay of 0.264 ns.

6.2.3 Ka-band SISL Chebyshev HPF

The fully-board embedded Ka-band SISL Chebyshev HPF S-parameters are shown in Fig. 6.19. The simulated insertion loss is less than 0.5 dB and the simulated return loss is greater than 22.0 dB across the 28-32 GHz passband, including the vertical via transition and edge-launch connectors. The passband provides greater than 40 dB of attenuation by 20 GHz, which continues to increase as the frequency approaches DC. Fig. 6.20 shows the simulated group delay over the 28-32 GHz passband. The simulated group delay is small across

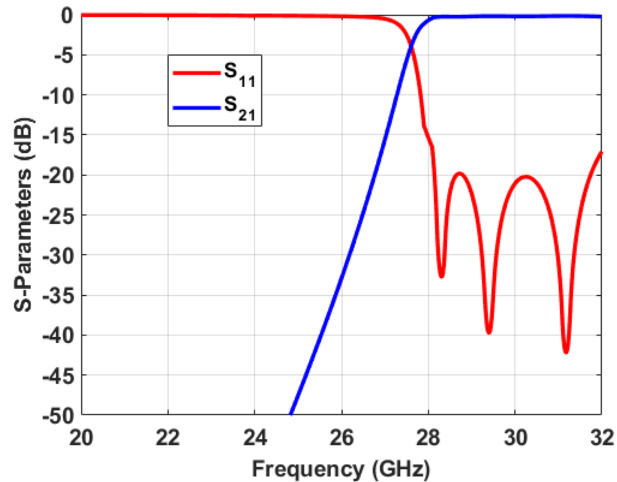


Figure 6.19: Simulated S-parameters of the proposed Ka-band SISL Chebyshev HPF.

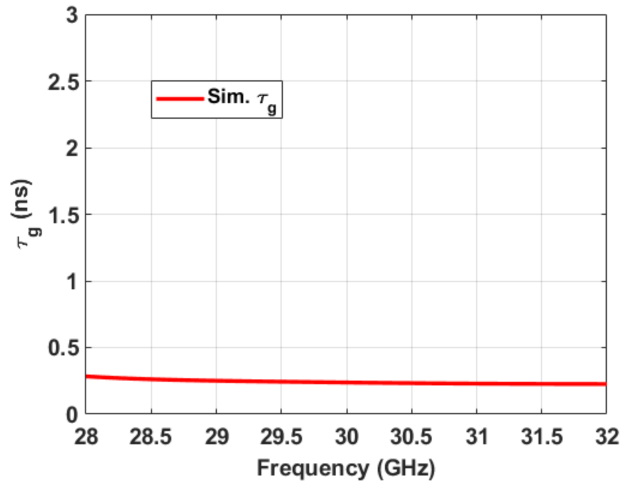


Figure 6.20: Simulated group delay of the proposed Ka-band Chebyshev HPF.

the entire passband reaching a maximum delay of only 0.284 ns at the 28 GHz cutoff frequency. The group delay is flat with an average delay of 0.242 ns.

6.2.4 Ka-band SISL Chebyshev BPF

The fully-board embedded Ka-band SISL Chebyshev BPF S-parameters are shown in Fig. 6.21. The simulated insertion loss is less than 1.0 dB and the

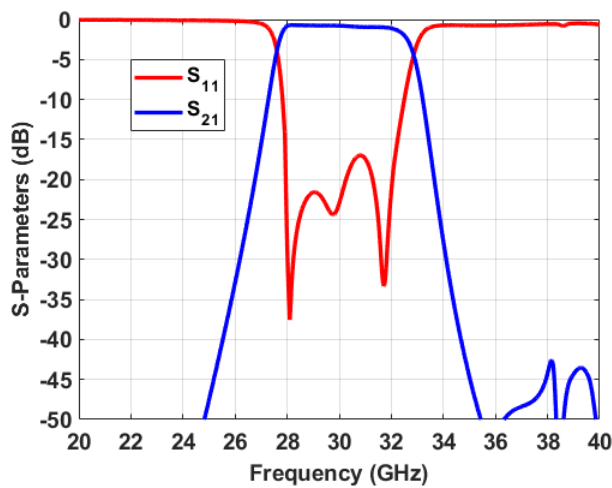


Figure 6.21: Simulated S-parameters of the proposed Ka-band SISL Chebyshev BPF.

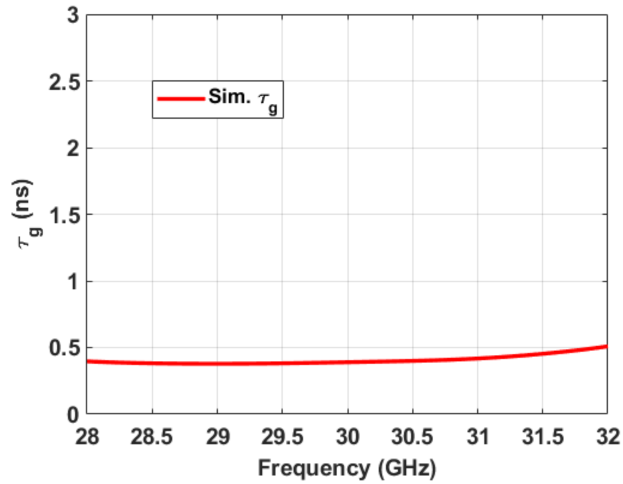


Figure 6.22: Simulated group delay of the proposed Ka-band Chebyshev BPF.

simulated return loss is greater than 17.0 dB across the 28-32 GHz passband, including the vertical via transition and edge-launch connectors. The passband provides greater than 40 dB of attenuation by 20 GHz and from 35 to 40 GHz. Fig. 6.22 shows the simulated group delay over the 28-32 GHz passband. The simulated group delay is small across the entire passband reaching only 0.396 ns at 28 GHz and 0.508 ns at 32 GHz. The group delay is very flat with an average delay of 0.406 ns. Given the good agreement between simulated and measured results at Ku-band, there is high confidence that the simulated cascaded BPF will produce good measured results.

Chapter 7

Summary and Future Work

7.1 Summary

The purpose of this research was to develop state-of-the-art suspended line filters for next generation telecommunications and radar systems. Future systems will require unprecedented reductions in size, weight, power, and cost forcing the supporting RF/microwave filters to achieve very small and highly integrated form factors that can also deliver very low loss in the filter's passband. In this work, fully-board embedded suspended integrated stripline filters have been designed and implemented to satisfy such requirements.

First, a DC-20 GHz SISL thru-line is designed as a proof-of-concept of the fully-board embedded SISL technology. The goal was to demonstrate the wideband and low loss capabilities desired. During the design phase, attention to fabrication was kept in mind to ensure that the device could be physically realized with modern day fabrication techniques. Measured results of the professionally fabricated DC-20 GHz thru-lines resulted in insertion losses less than 1 dB, and opens the door for filter designers to realize wideband and low loss filters for next generation systems.

The fully-board embedded SISL technology was used to design an eleventh-

order generalized Chebyshev LPF with a cutoff frequency of 18 GHz and an eleventh-order generalized Chebyshev HPF with a cutoff frequency of 2 GHz. The filters were then internally cascaded using a stripline trace to develop a 2-18 GHz BPF that will be used as the front-end filter for a 16 GHz bandwidth FMCW radar. The measured LPF insertion loss is less than 0.927 dB and measured return loss is greater than 10.5 dB across the 18 GHz passband. The measured HPF insertion loss is less than 0.86 dB and measured return loss is greater than 10.25 dB across the passband. By using broadside coupled structures, the length of the coupled lines length could be reduced to push resonances above the 18 GHz upper passband frequency while still achieving the required element-level capacitance. The cascaded BPF achieved a measured insertion loss less than 1.1 dB and measured return loss greater than 11.0 dB across the 2-18 GHz passband, with excellent stopband rejection. All of the measured results agreed very well with simulated results indicating the developed mathematics and HFSS models are accurate.

Next, the SISL technology was evaluated to determine the frequency scalability. Several design guidelines were provided and applied to the design of a DC-40 GHz thru-line as a technology demonstrator. Simulated results showed an insertion loss less than 1.2 dB and a return loss greater than 9.5 dB could be achieved. The frequency can be scaled even higher in frequency as long as substrates thin enough can be sourced to minimize the signal via length and push the cutoff frequency above the desired frequency of operation. Given the good agreement between simulated and measured results at Ku-band, there is high confidence that measured results of the Ka-band thru-line will agree well with the simulated results

Finally, an eleventh-order generalized Chebysehv LPF with cutoff frequency

of 32 GHz and an eleventh-order generalized Chebyshev HPF with cutoff frequency of 28 GHz are designed and implemented to demonstrate low loss and wideband performance at Ka-band. The filters are then internally cascaded to develop a 28-32 GHz BPF. The simulated LPF insertion loss is less than 0.9 dB and simulated return loss is greater than 17.0 dB across the 28-32 GHz passband. The simulated HPF insertion loss is less than 0.5 dB and measured return loss is greater than 22.0 dB across the passband. The cascaded BPF achieved a simulated insertion loss less than 1.0 dB and measured return loss greater than 17.0 dB across the 28-32 GHz passband, with good stopband rejection. The benefit of the proposed SISL design is that the low loss performance of waveguide filters are possible while simultaneously achieving the small form factors and sharp roll-offs of integrated stub-based filters.

In conclusion, the work presented here represents the current stat-of-the-art in highly integrated suspended line filters. The proposed SISL designs have advantages of low loss and wideband performance, compact size, and low cost to meet the needs of next generation telecommunications and radar systems.

7.2 Contributions

- First time demonstration of a fully-board embedded SISL design.
- First time demonstration of a self-packaged suspended line design with frequency capability up through Ku-band.
- First time demonstration of a fully-board embedded SISL lowpass filter design.
- First time demonstration of a suspended line filter design with a cutoff frequency at Ku-band frequencies.

- First time demonstration of a fully-board embedded SISL highpass filter design.
- First demonstration of a self-packaged suspended line HPF with octo-octave passband performance.
- First time demonstration of a fully-board embedded SISL cascaded bandpass filter design.
- First time demonstration of a self-packaged suspended line bandpass filter with 160% passband percent bandwidth.
- First time demonstration of a TEM-mode fully-board embedded SISL design at Ka-band frequencies.
- First time demonstration of a fully-board embedded Ka-band LPF, HPF, and BPF.

7.3 Future Work

The fully-board embedded SISL filters demonstrated in this dissertation offer a viable low loss and highly integrated solution for high frequency applications such as 5G telecommunications, cloud weather radar, and automotive radar. All of these applications require excellent front-end sensitivity, and most will require filtering right behind the antenna to suppress near band signals. For now, substrate integrated waveguide (SIW) filters are commonly used, but suffer from high dielectric losses at V-band and above. Another approach is to use CMOS based filters, but these are lossy in the passband due to the poor resistivity silicon and are much more expensive to fabricate. The fully-board embedded SISL filters are only limited by the thickness of the substrate

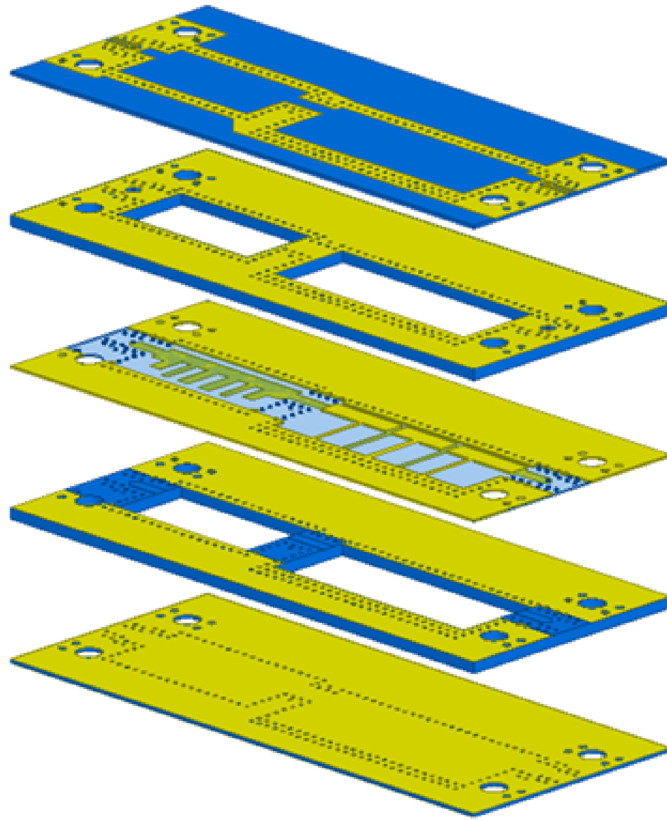


Figure 7.1: 3-D exploded view of the proposed LTCC SISL BPF.

stack-up. Given the advanced materials available today such as liquid crystal polymer (LCP) [113], LTCC [114], and glass [115], substrate thicknesses on the order of 0.5 to 4 mil thick are possible. This would allow for SISL filter designs up to 100 GHz [116]. Fig. 7.1 shows the exploded view of a LTCC fully-board embedded SISL BPF using gold thick-film metal layers. Using 4-mil layers, a 76-77 GHz BPF for automotive radar is designed and simulated results are shown in Fig. 7.2. This design example illustrates that incredibly low loss and wideband filters can be achieved at V-band and above to satisfy the low SWaP and high sensitivity requirements of next generation systems.

Another area of research is to investigate how narrow of a bandwidth can be achieved in the SISL technology and still maintain low loss capabilities.

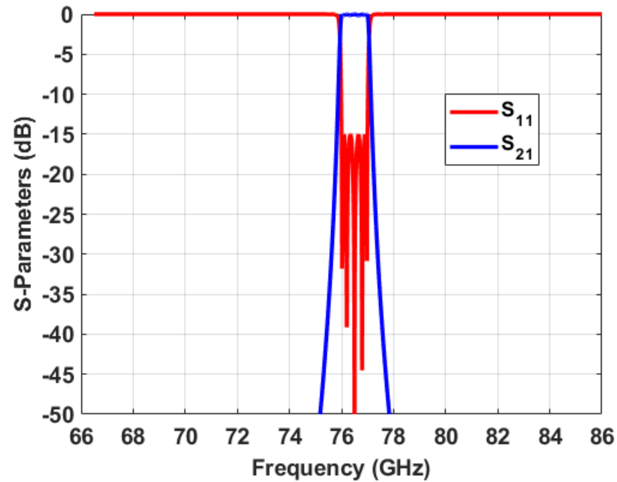


Figure 7.2: Simulated S-parameters of the proposed LTCC SISL BPF.

Traditionally, for low-order cascaded filters, as the cutoff frequencies of the LPF and HPF are brought closer together, the insertion loss increases as the roll-offs begin to overlap. For higher order filters with sharp rejection like the proposed SISL filters, the cutoff frequencies can be brought very close together without affecting the insertion loss. While this is a non-traditional approach, it offers a highly integrated and low loss solution that other filter topologies can not achieve simultaneously.

Beyond just high frequency operation, there is a significant amount of research potential for the implementation of other filter topologies. Another area of interest, as previously mentioned in Section 3.1.5, is the design of defected ground structures to suppress the cavity resonance and extend the lowpass filter stopband. The cavity resonance causes a spike in S_{21} at the resonant frequency and degrades the stopband. Due to the convenient stack-up of the fully-board embedded SISL design, a defected ground structure can be implemented below the input and output CPWG traces, which will ultimately act as a bandstop filter. If designed correctly at the cavity resonance frequency, the bandstop filter will counteract the cavity resonance and allow for

an extended stopband with better attenuation [117]. Lastly, having to use a multilayer PCB approach to implement the fully-board embedded SISL technology might be too expensive for some designs. Therefore, slight changes to the input and output traces cab be investigated to make the filter a surface mountable planar filter that can be soldered on top of a single layer board using a re-flow process. Therefore, the same benefits of the SISL filter can be achieved while not requiring the entire subsystem/system PCB to be multilayer. This would be highly beneficial for low budget applications where such forms of integration are not needed.

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Appendix A

Fabrication Process

The step by step fabrication process used throughout this research is presented in this appendix. All of the drilling steps are completed using a LPKF ProtoMat S103 milling machine [118]. The patterning fabrication steps are completed using a photolithography process due to the fine lines and spaces.

For the Ku-band build, there are 13 Gerber files generated that are needed to fabricate the designs. The required Gerber files are as follows:

1. Copper_Layer_1 - metal layer 1 (M1).
2. Copper_Layer_2 - metal layer 2 (M2) between substrates 1 and 2.
3. Copper_Layer_3 - metal layer 5 (M5) between substrates 2 and 3
4. Copper_Layer_4 - metal layer 6 (M6) between substrates 3 and 4.
5. Copper_Layer_5 - metal layer 9 (M9) between substrates 4 and 5.
6. Copper_Layer_6 - metal layer 10 (M10).
7. Thru_Via - 0.3 mm diameter plated via through substrates 1-5.
8. Signal_Via - 0.3 mm diameter plated blind via through substrates 1-3.

9. Mounting_Hole - 2 mm diameter drill hole needed to mount the Southwest Microwave edge launch connectors.

10. Ground_Pad_Via_0.6mm - 0.6 mm diameter plated via through substrates 1-5 to ground edge launch connectors.

11. Outline - individual board outlines used for individual routing of the SISL components (used if multiple parts arrayed on a single stack-up).

12. Substrate_Cutout - drill file used to mil out the air cavities in substrates 2 and 4.

13. Board_Outline - outline of the 5x5 board stack-up that contains the entire component array (9x12 for the ACE fabricated parts).

The Ka-band build has one additional Gerber file as follows:

14. Ground_Pad_Via_1.6mm - 1.6 mm diameter plated via through substrates 1-5.

A.1 Detailed Fabrication Process

The fabrication process is broken down into 7 steps as follows:

1. Preparation.

2. Laminate substrates 1-3.

3. Drill and plate signal via.

4. Laminate substrates 1-5.

5. Etch M1.

6. Drill and plate grounding through vias.

7. Individual route.

A.1.1 Preparation

All of the substrate layers (1-5) are cut to a 5x5 inch square using a shear. Each laminate substrate layer goes through some preparation prior to lamination. The preparation steps for each individual layer is discussed below.

A.1.1.1 Substrate Layer 1

First, the fiducial and mask alignment holes are drilled to ensure proper registration is achieved throughout the fabrication process. Next, M1 of substrate layer 1 is exposed to protect all of the copper during the photolithography process. Lastly, M2 on substrate layer 1 is etched using the Copper_Layer_2 masks, which creates the anti-via pad for the signal via.

A.1.1.2 Substrate Layer 2

First, the fiducial and mask alignment holes are drilled to ensure proper registration is achieved throughout the fabrication process. Next, the SISL air cavity is cut out with the LPKF S103 using the Gerber file name Substrate_Cutout. Finally, the copper is etched off of both sides of substrate layer 2.

A.1.1.3 Substrate Layer 3

First, the fiducial and mask alignment holes are drilled to ensure proper registration is achieved throughout the fabrication process. This is done by clamping the board between two thicker substrates to ensure proper drill holes (substrate layer 3 is too thin to drill by itself). Next, M5 and M6 are etched using

the Copper_Layer_3 and Copper_Layer_4 masks, respectively. It is critical to have great alignment during this step in order to make sure the broadside coupled lines overlap correctly.

A.1.1.4 Substrate Layer 4

First, the fiducial and mask alignment holes are drilled to ensure proper registration is achieved throughout the fabrication process. Next, the SISL air cavity is cut out with the LPKF S103 using the Gerber file name Substrate_Cutout. Finally, the copper is etched off of both sides of substrate layer 4.

A.1.1.5 Substrate Layer 5

The only step needed for substrate layer 5 is to drill the fiducial and mask alignment holes to ensure proper registration is achieved throughout the fabrication process.

A.1.1.6 Pre-preg and Teflon Layers

Using the shear, six layers of the Pyralux LF-1500 adhesive material are cut to 5x5 inches. These pre-preg layers are then stacked and the SISL air cavities are cut using the Substrate_Cutout Gerber file. The pre-preg needs to be cut in the cavity area so that there is no material covering up the M2 and M9 ground planes.

Eight sheets of Teflon also need to be cut to 5x5 inches using the shear. These Teflons pieces are used during the lamination process.

A.1.2 Laminate Layers 1-3

The lamination process starts by tacking the Pyralux pre-preg onto substrate layers 2 and 4. The pre-preg comes with one side exposed and the other side has a thin plastic film on it. This tacking process allows for the non-plastic covered side to adhere to the substrate. The plastic film can be then removed from the other side. Substrate layer 1 and 3 are now aligned and laminated to substrate layer 2 forming sub-assembly 1. The substrate layers and pre-preg are aligned by using an in-house made fixture with built-in alignment pins. The mask alignment holes previously drilled slide over these pins to perfectly align all the layers prior to lamination.

A.1.3 Signal Via

After sub-assembly 1 is complete, the signal via can now be processed. The blind signal via is processed at this point due to the limited plating abilities of a true blind via. For successful via formation, an aspect ratio of 2:1 maximum should not be exceeded. Given a 12 mil diameter via, the length of the via should not exceed 24 mil if processed as a blind via. The singal via in the Ku-band design is a little over 45 mil and must be processed as a plated through via at this point in the process. Then, after substrates 4 and 5 are laminated to sub-assembly 1, it will be a blind via. Using the LPKF S103, the signal vias are drilled using the Signal_Via Gerber drill file. After drilling, the signal via is plated to form the blind signal via.

A.1.4 Laminate Layers 1-5

The first step is to tack the pre-preg to both sides of substrate layer 4 identical to what was done earlier with substrate layer 2. Substrate layer 4 is aligned in

the fixture with substrate layer 5 and sub assembly 1 and laminated to form the final board stack-up.

A.1.5 Etch Copper Layer 1

After the final PCB stack-up is complete, M1 is etched using the Copper_Layer_1 mask. All of M10 should be exposed prior to etching in order to keep the copper protected during the etching process.

A.1.6 Ground Vias

All of the plated through-vias are now drilled using the LPKF S103 and the Thru_Via Gerber drill file. After drilling, the through-vias are selectively plated to provide ground connection between all the ground planes. This step uses a selective plating process in order to not plate over CPWG traces etched in the previous fabrication step.

A.1.7 Individual Route

At this point, all of the fabrication steps have been completed except for individually cutting out all of the components arrayed onto the PCB stack-up. The individual parts are cut out using the LPKF S103 and the Outline Gerber file. The components can now be connectorized and tested.

A.2 Fabrication Procedure

This section provides a listed procedure that should be followed and used as a checklist to fabricate the microwave components in the proposed SISL technology. The individual components are arrayed onto a larger board stack-up in order to fabricate several parts in one fabrication. The fiducial and alignment holes are drilled into the larger board for this reason.

1. Preparation:
   (a) Size all the substrates 1-5 to 5x5 inches using the shear.
   (b) Substrate Layer 1:
      i. Drill fiducial and alignment holes.
      ii. Expose M1 to keep all copper on this side.
      iii. Use mask Copper_Layer_2 to etch away the copper around the signal vias on copper layer 2.
   (c) Substrate Layer 2:
      i. Drill fiducial and alignment holes.
      ii. Cut out the cavity before etching using the Substrate_Cutout Gerber file.
      iii. Etch away M3 and M4.
   (d) Substrate Layer 3:
      i. Drill fiducial and alignment holes using the sandwich method (board is very thin).
      ii. Etch M5 and M6 with masks Copper_Layer_3 and Copper_Layer_4, respectively.
   (e) Substrate Layer 4:

i. Drill fiducial and alignment holes.

ii. Cut out the cavity before etching using the Substrate_Cutout Gerber file.

iii. Etch away M7 and M8.

(f) Substrate Layer 5:

i. Drill fiducial and alignment holes.

(g) Pre-preg Patterning:

i. Size six layers of pre-preg to 5x5 inches using the shear (make sure half of the pre-preg layers are face down and the rest face up to allowing for tacking procedure).

ii. Size eight sheets of Teflon to 5x5 inches using the shear.

2. Laminate Layers 1-3:

(a) Tack the pre-preg onto substrate layers 2 and 4 using the temperature profile in the datasheet.

i. This transfers the adhesive layer to substrates 2 and 4 to get rid of the plastic film that is on the pre-preg from the manufacturer.

ii. An in-house fixture is made with pins that align with the alignment holes in the substrates. This fixture is used to stack materials for tacking and lamination.

(b) Using the fixture, make a stack-up as shown below in Fig. A.1 for tacking.

(c) Using the fixture, make a stack-up as shown below in Fig. A.2 to laminate substrates 1-3 and create sub-assembly 1.

   (d) Laminate substrates 1-3 using the heating and pressure profile per the pre-preg datasheet.

3. Drill and Plate the Signal Vias:

   (a) Use the LPKF S103 and the Signal_Via Gerber file to drill the signal via.

   (b) Selectively plate the signal via to connect M1 to M6.

4. Laminate Layers 1-5:

   (a) Tacking: use the same procedure as 2.b. to tack the pre-preg to substrate layer 4.

   (b) Using the fixture, make a stack-up as shown below in Fig. A.3 to laminate substrates 1-5 and create the final assembly.

   (c) Laminate substrates 1-5 using the heating and pressure profile per the pre-preg datasheet.

5. Etch Copper Layer 1:

   (a) Using the mask titled Copper_Layer_1, etch M1 keeping all copper on M10.

6. Drill and Plate Ground/Thru Vias

   (a) Use the LPKF S103 and the Thru_Via Gerber file to drill the ground/thru vias.

   (b) Selectively plate the ground/thru vias to connect all metal layers.

7. Individual Route:

(a) Use the LPKF S103 and the Outline Gerber file to individually route each component of the array.

Fixture Top Layer
Teflon (not patterned)
Prepreg with adhesive face down
Substrate Layer 2/4
Prepreg with adhesive face up (toward substrate)
Teflon (not patterned)
Fixture Bottom Layer

Figure A.1: Material stack-up for tacking process.

Fixture Top Layer
Teflon (patterned and placed with correct orientation) 1 or 2 layers
Substrate Layer 1
Substrate Layer 2 (ALREADY TACKED)
Substrate Layer 3
Teflon (patterned and placed with correct orientation) 1 or 2 layers
Fixture Bottom Layer

Figure A.2: Material stack-up for lamination of substrate layers 1-3.

Fixture Top Layer
Teflon (patterned and placed with correct orientation) 1 or 2 layers
Substrate Layers 1-3
Substrate Layer 4 (ALREADY TACKED)
Substrate Layer 5
Teflon (patterned and placed with correct orientation) 1 or 2 layers
Fixture Bottom Layer

Figure A.3: Material stack-up for lamination of substrate layers 1-5.

Fig. A.4 shows an overview of the fabrication flow and Fig. A.5 shows a cross-sectional view of the fabrication flow.

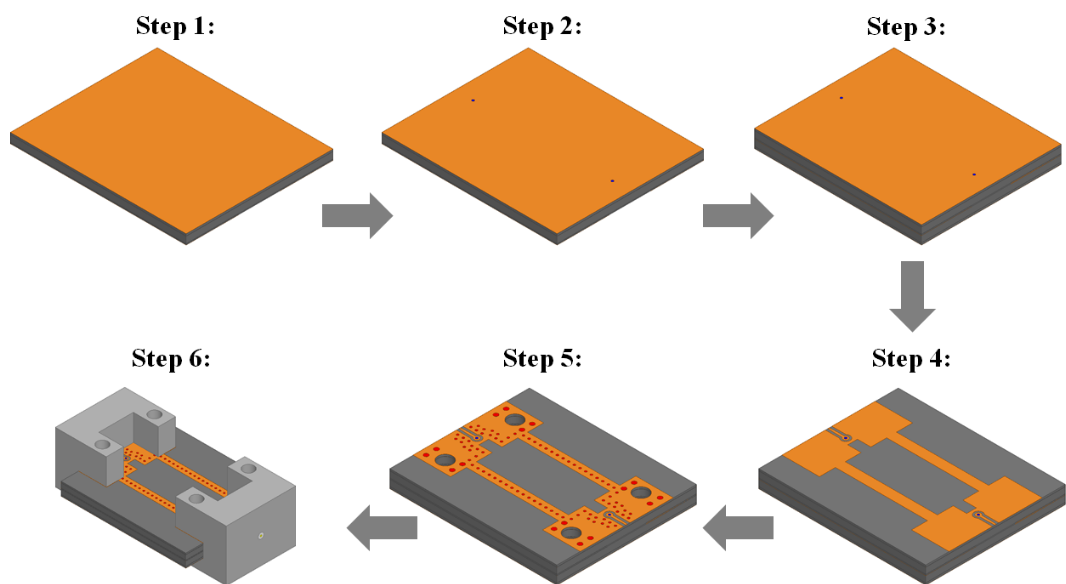

Figure A.4: Fully-board embedded suspended integrated stripline component step by step fabrication procedure.

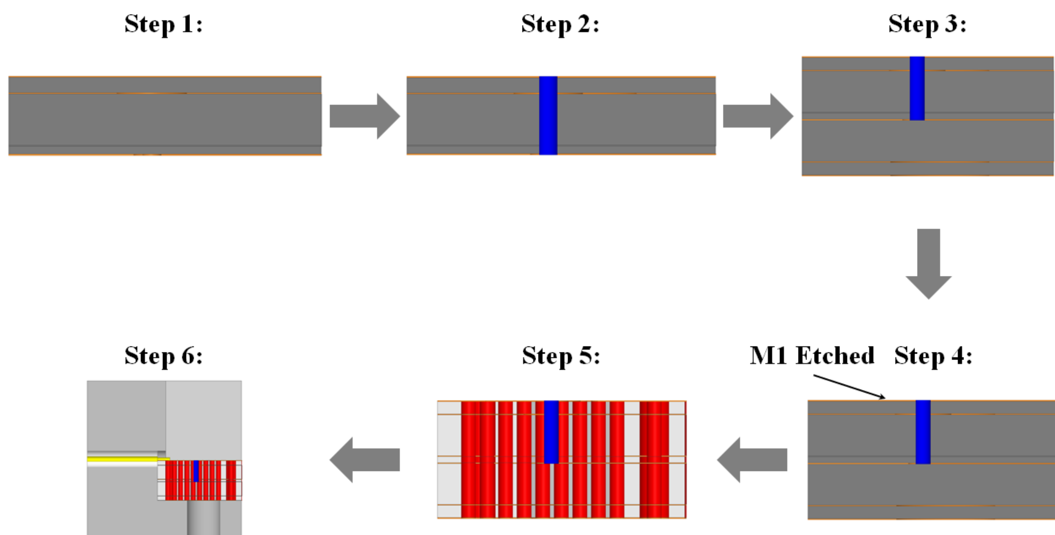

Figure A.5: Cross-sectional view of the step by step fabrication procedure.

Appendix B

List of Acronyms and Abbreviations

ACE Accurate Circuit Engineering

ADS Advanced Design System

AESA Active Electronically Scanned Arrays

ASIC Application Specific Integrated Circuit

BCS Broadside Coupling Structure

BPF Bandpass Filter

CPW Coplanar Waveguide

DAC Digital-to-Analog Converter

EMC Electromagnetic Compatibility

HFSS High Frequency Structure Simulator

HPF Highpass Filter

IC Integrated Circuit

IF Intermediate Frequency

LCP Liquid Crystal Polymer

LNA Low Noise Amplifier

LPF Lowpass Filter

$LTCC$ Low Temperature Co-fired Ceramic

MCM Multi-chip Module

MDS Minimum Detectable Signal

$MIMO$ Multi-Input and Multi-Ouput

$mmWave$ Millimeter Wave

MRR Multiple Resonances Resonator

NF Noise Figure

nH Nanohenries

PCB Printed Circuit Board

pF Picofarads

PNA Performance Network Analyzer

RF Radio Frequency

Rx Receiver

$S-Parameters$ Scattering Parameters

SAR Synthetic Aperture Radar

$SFCW$ Stepped Frequency Continuous Wave

$SISL$ Substrate Integrated Suspended Line

$SISL$ Suspended Integrated Stripline

SIW Substrate Integrated Waveguide

$SLOC$ Stripline Open-Circuited

SoC System on Chip

SSL Suspended Stripline

SSS Suspended Substrate Stripline

$SWaP-C$ Size, Weight, Power, and Cost

Tx Transmitter

UAV Unmanned Aerial Vehicle

UWB Ultrawide Band