A MODULAR GENERAL PURPOSE APPROACH TO THE

SIMULATION OF CONSTANT SPEED DISCRETELY

SPACED RECIRCULATING

CONVEYOR SYSTEMS

Thesis Approved:

M. Palmer Terrell
Thesis Adviser

G. T. Stevens, Jr.

Fred Black

James E. Shamblin

N N Durham
Dean of the Graduate College

PREFACE

This dissertation includes a feasibility study and partial development of a general purpose simulation model that can be used to study the operational aspects of constant speed discretely spaced recirculating complex conveyor systems. The study includes both a general and a detailed description and explanation of the model development which utilizes a modular format. These modules are stacked together like building blocks to construct the entire conveyor system. In order to test the feasibility of the approach and validate the model, the simulation modules are used to simulate the operation of two large manufacturing companies' recirculating conveyor systems. The simulation modules are written in General Purpose Simulation System language for the IBM 360 Model 65 computer. Source listings, flowcharts, and simulation outputs are included in this research.

The author wishes to express his appreciation to his major adviser, Dr. M. Palmer Terrell, for his guidance and assistance throughout this research. Appreciation is also expressed to the other committee members, Dr. G. T. Stevens who served as committee chairman, Prof. Frederick M. Black who stimulated the author's interest in simulation, and Dr. James E. Shamblin for his invaluable support and encouragement.

Sincere appreciation is expressed to my wife, Lana, for typing the initial and final drafts of the manuscript.

Finally, special gratitude is expressed to my wife and our children, Robin and Jonathan, for their understanding, encouragement, and many sacrifices.

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CHAPTER I

INTRODUCTION

The principle objective of this research is to demonstrate the feasibility of a general purpose simulation model which can be used to study and develop an understanding of the operational aspects of constant speed discretely spaced recirculating complex conveyor systems. It is <u>not</u> the purpose of this research to develop that all-encompassing model, but only to demonstrate the feasibility of the approach.

Many industrial manufacturers use recirculating conveyor systems not only for transporting goods to various locations in the plant but also for storing goods and for smoothing out irregularities in the flow of goods to loading and unloading stations. There are many types of recirculating conveyor systems, such as: drag line or tow line conveyors, bucket conveyors, overhead monorails, suspended tray conveyors, trolley conveyors, carrousels, and towveyors. Regardless of the basic type, all are typified by running at a constant speed, having discretely spaced hooks or dogs, and recirculating or forming a closed loop. All are often referred to as powered line conveyors.

The conveyor system in a manufacturing plant is merely a subsystem of the entire integrated system. The design of the conveyor subsystem must be carefully considered since the conveyor interacts with a great many other subsystems of the plant. Both the mechanical and the performance aspects of its design must be dealt with. The mechanical aspects of the design problem such as conveyor dimensions, conveyor strength, frame structure, installation factors, size of the drive unit, starting loads, maximum imposed loads, and method of lubrication appear to be well understood. Solutions to these types of problems can be found with existing scientific and mathematical techniques. The performance aspects of the design problem such as capacity and utilization of the conveyor as an in-process storage device, traffic density, potential bottlenecks in the system, utilization of load and unload stations, and average queues that form at the various points are not well understood. Solutions to these types of problems can not readily be found. The combinatorial aspects of these types of problems are so large that the solution defies analytical techniques such as the direct application of numerical analysis or classical queueing theory.

Many of the performance aspects of recirculating conveyor systems are a result of relationships between and among other characteristics and parameters that are not presently understood. A search of the literature indicates that there is neither the data nor the methodology available to define these relationships or study the performance characteristics.

Research Objectives

In order to demonstrate the feasibility of a general purpose simulation model which can be used to study recirculating conveyor systems, five subobjectives were undertaken sequentially:

1. The examination and analysis of the functional components of a particular complex integrated conveyor system, with the objective of identifying the functional components and parameters of the system.
2. The identification and description of the components and parameters of the types of interfaces that do occur between the functional components of the complex recirculating conveyor system.
3. The development and encoding of a computer simulation model using a modular format to represent the functioning of the components identified in 1. and 2. above.
4. The demonstration that the "plug-in" simulation modules provide a feasible approach for building a general purpose simulation model.
5. The use of the "plug-in" simulation components to simulate the recirculating conveyor system referenced in 1., 2., and 3. above to validate the model logical construction, and further validate the simulation modules and demonstrate the feasibility of the approach by using the modules to simulate another unrelated recirculating conveyor system.

Stages of the Investigation

The investigation took place in four distinct stages. The first stage consisted of selection and study of a particular complex conveyor system. The system chosen for analysis was the warehouse distribution system of a large manufacturing company. This researcher was required to refrain from identifying the company.

The company had kindly consented to cooperate in this research, and several personal visits to the company were necessary to study the system and obtain the data about the system that was available.

The model construction and validation, the second stage, was the most time consuming. The model was encoded in General Purpose Simulation System (GPSS), simulated, and validated in the Oklahoma State University IBM 360 Model 65 Computer.

The third stage was a simulation of the manufacturing company's conveyor system and a validation of the model by evaluating the results of the simulation.

The fourth stage was a simulation of another recirculating conveyor system of a manufacturing company which also wishes to be unnamed.

Before proceeding into a description of the first conveyor system chosen for study, a brief review of the literature will be presented.

CHAPTER II

LITERATURE REVIEW

This chapter summarizes the present state of knowledge applicable to this research by a summary of the published work that has been accomplished in the past fifteen years. Before proceeding to the literature review, a framework must be established to classify the prior research.

Classification of Conveyor Research

The type of conveyor system that has been used for study in this research is the constant speed discretely spaced recirculating conveyor system. This type of conveyor system was selected because it was believed that a general purpose simulation model could be developed to study the performance aspects of any particular constant speed discretely spaced recirculating conveyor system. The primary objective of this research is to demonstrate the feasibility of a general purpose simulation model. The three characteristics of conveyor systems studied in this dissertation will be used as a framework within which to classify prior research. Regardless of the actual form it may take such as overhead trolley, suspended tray, tow line, etc., the conveyor system must possess these three characteristics: (1) it must run or move at a constant speed, (2) it must have discretely spaced hooks or dogs which may or may not be loaded with goods, and (3) it must be a recirculating system or it must form one or more closed loops in which goods placed on the conveyor can pass a given point in the system more than once. If a particular conveyor system lacks one or more of these characteristics, it can not be analyzed or studied by the research approach presented in this study.

The first necessary characteristic that a conveyor system must possess is it must run at a constant speed. The so called "power and free" type conveyors do not meet this requirement because the hooks or dogs may be stopped at locations along the conveyor for random periods of time. Also large systems which consist of many subsystems that move at different speeds do not meet this requirement.

The second necessary characteristic is the conveyor must consist of discretely spaced hooks or dogs which may or may not be loaded. This means that the distance between adjacent hooks of the conveyor is a constant. Let k be the constant distance between adjacent hooks. Then the loads on the hooks would occur at spacings of nk where n is an integer random variable ($n = 1, 2, 3, 4, \cdots$). Most endless belt conveyors do not meet this requirement. A belt load such as sand, grain, or ore would obviously not be spaced discretely but is spaced continuously along the belt. Even unit loads on an endless belt do not meet the requirement since the distance between adjacent loads is a continuous random variable. Some types of endless belt conveyors are fitted with discretely spaced dividers which means that the belt has "hooks" or load positions which are uniformly spaced but not necessarily uniformly occupied.

The third necessary characteristic is the conveyor must recirculate or form one or more closed loops. Many types of short feeder conveyors such as endless belts, rollers, or powered rollers do not recirculate goods which fail to be removed from the conveyor but simply dump them off at the end. Large complex conveyors especially the tow line type may be used for delivery of goods to a great number of locations in a plant or a warehouse. Often these types of systems form several closed loops. In these conveyors, loaded or unloaded carts can take a variety of routes to pass a given point in the system more than once. Simple systems such as carrousels and single loop overhead trolley type continuous chain conveyors frequently form an easily recognizable single closed loop.

Prior Research

After an extensive literature review, it was evident that no researcher has attempted to study or develop the model proposed by this dissertation. The prior investigations summarized below do not in most cases relate directly to the particular conveyor system that is the subject of this study; however, all of them deal with materials handling or the various aspects of conveyor theory or application.

Probably the first to study some of the performance aspects and mechanical principles of conveyor systems was Kwo (14). The system that he studied was a recirculating overhead suspended hook type conveyor which was fed by a single load station and unloaded by an unload station. The mathematical equations that he developed showed how to calculate limiting values of conveyor speed, capacity, and uniformity of loading. In a later study by Kwo (15), he crystallized the design problem of overhead recirculating conveyor systems and presented a method of arriving at feasible conveyor designs. He lists twelve steps in the design process which include solving mathematical equations developed by Kwo as design criteria. At about the same time Helgeson (12) was also working on the design problem of overhead recirculating conveyor systems. He developed a theory useful in the study of these conveyors which link a production system with uncertain production rate with a using system with uncertain consumption. These production and using systems were subject to severe mechanical limitations imposed by such a conveyor. He also developed a practical planning technique including the use of a nomograph to assist the conveyor systems planner in achieving a better solution to the conveyor systems design problem than by the "rule of thumb" techniques that were commonly in use.

Palm (20) and Khinchine (13) were two of the early researchers in the area of randomly spaced nonrecirculating waiting line systems who through the use of queueing theory studied the overflow problem. Their solution techniques were applied to conveyor systems by Disney (9, 10) who studied randomly spaced nonrecirculating conveyor systems as a delivery device for one and two channel unloading stations. His solution technique utilizes multichannel ordered entry queueing theory, and he also develops system performance equations for local storages positioned between the conveyor and the unload station. In a later continuation of his work in these types of conveyor systems, Cinlar and Disney (7) study the overflow problem first examined by Palm (20) and Khinchine (13). Cinlar and Disney (7) develop a distribution of a stream of overflows from a finite queue from randomly spaced nonrecirculating conveyor systems in which the processes are Markovian. In an extension of the work of Disney (9, 10), Gupta (11) researched the use of generating functions to produce a new solution technique to the two channel queueing problem with ordered entry.

Among the first researchers to study how a conveyor affects an unload station, if the unload station is a work station, were Reis and Hatcher (24) and Reis, Dunlap, and Schneider (25). This early work was extended by Reis, Brennan, and Crisp (26) who used a Markovian type analysis for the delay at the conveyor supplied work stations. They also developed a set of work rules for the operation of the work station. In another extension of this research by Beightler and Crisp (2) the work station problem was formulated as a discrete time queueing process to improve the work rules. Crisp, Skeith, and Barnes (8) continued the work on conveyor supplied work stations using simulation.

In a more general context, Morgan (16) examines a two-link materials handling system exemplified by a set of shovels in the first link dumping material into a hopper. The hopper is emptied into a fleet of trucks that transport the material in the second link. The solution technique involves the solution of a set of simultaneous equations dealing with system parameters.

Pritsker (16) uses both simulation and ordered entry queueing theory to examine both recirculating and nonrecirculating conveyor systems which supply more than one work station. The work stations may or may not have a local storage capacity. With respect to his work in recirculating conveyor systems, he found through simulation that when the rate of recirculation became significant, the multichannel queueing theory no longer accurately predicts the probabilities associated with system performance parameters. In an extension of Pritsker's work, Phillips (21) and Phillips and Skeith (22) also used simulation to study randomly spaced recirculating conveyor systems. These simulation models considered the recirculation aspects of conveyor systems differently. Pritsker (16) worked with a constant delay for goods which are recirculating. Phillips and Skeith (22) force a queue to form if the recirculating conveyor is occupied which caused the recirculation delay to be a random variable rather than a constant. The remainder of this chapter includes the more recent developments in conveyor research.

Burbridge (4) used GERT to analyze a particular conveyor system which has both primary and recirculating arrivals. The conveyor system of interest has one unloading station which has a local storage. Units arrive at the loading station from an outside source or from the conveyor. If the local storage is full, the units arriving from the conveyor must recirculate and arrive again at a later time.

Agee and Cullinane (1) present a methodology for determining the transient response of a two link materials handling system. A straight line gravity feed conveyor connecting two production centers is an example of such a system. The system is modeled as a non-recirculating, multiple source, multiple server, limited waiting space queueing process.

Brady (3) examines the effect of operator work time variability in fixed transfer and in free transfer conveyor systems. The comparisons made indicate the superiority of the free transfer system in terms of output efficiency and jig requirements under specified conditions.

The early work of Muth (17) dealt with continuous flow conveyors. He studied recirculating conveyors that were used both as a delivery and a storage device. Later work by Muth (18, 19) examined closed loop conveyor systems with discrete material flow. This work extended a previous solution to the problem of conveyor design for arbitrary loading and unloading patterns. Solutions to difference equations representing material flow were obtained numerically by generalized matrix inverses. Several specific cases were presented graphically.

The most significant contribution to the research of constant speed discretely spaced recirculating conveyor systems was that of Bussey and Terrell (5, 6). They used simulation to study a single loop constant speed discretely spaced recirculating conveyor. The conveyor was supplied by a single server and unloaded at n unload stations.

The simple single loop model of Bussey and Terrell is a starting point and provides a spring board for this research.

CHAPTER III

CONVEYOR SYSTEM DESCRIPTION

The recirculating conveyor system of the first manufacturing company was chosen for study because it is sufficiently large and complex to adequately accomplish the research objectives set forth earlier in this dissertation. The conveyor system moves finished goods through a 500,000 square-foot warehouse via a sub-floor towline conveyor. The towline looks like a chain running in the floor with "hooks" spaced every twenty one feet along the chain. Each of these hooks may or may not be pulling a cart along with it. There are 380 carts in the system at all times.

A floor plan diagram of the conveyor system is shown in Figure 1. Among its functions are delivery of finished goods from manufacturing to storage or from storage to the rail and truck docks and delivery of incoming goods from the rail and truck docks to storage. The main loop shown in Figure 1 by a dashed line is 5600 feet long, and the towline travels at 70 feet per minute. However, each cart may not be required to travel the entire length of the main loop. Carts may be programmed manually for any of 20 destinations around the loop, and they will always travel the shortest distance to arrive at their destinations. The destinations are any one of the non-powered spurs at the ends of storage aisles. The following carts push the carts into the spur. After unloading and or loading it is manually brought back to the powered towline and programmed for a new destination. Carts are programmed manually by moving magnet-tipped probes at the front of each cart. As the cart moves along the loop, the probes activate reed switches embedded in the floor, causing switches to open which send the cart to its proper destination.

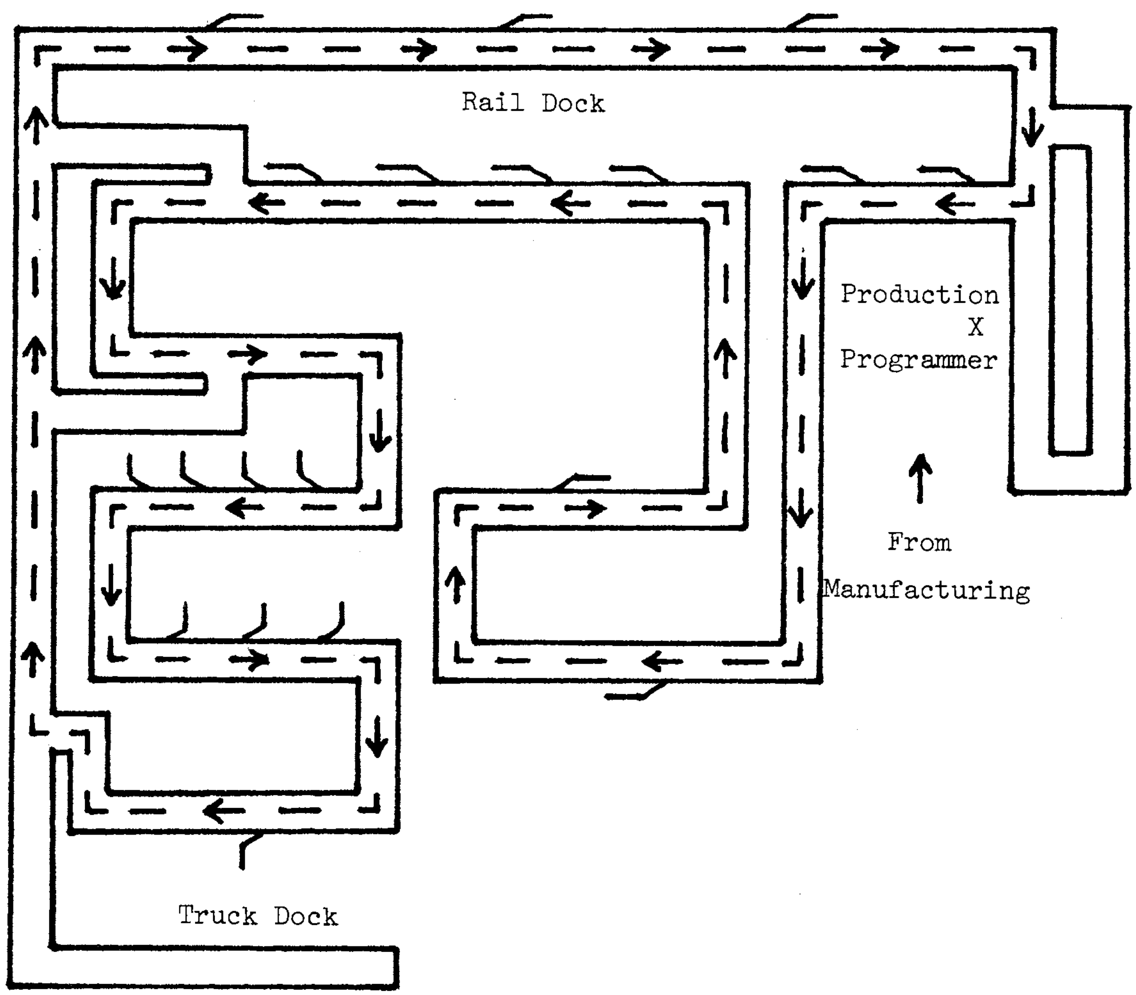

Figure 1. Conveyor Diagram

Each cart weighs 500 pounds, and it may be traveling loaded or unloaded. The carts are loaded and unloaded by fork lift trucks which either place or remove pallets of finished goods on or off the carts. The cart is then programmed for a destination by the fork lift truck operator and placed back on line. Finished goods which enter the warehouse from the manufacturing area via fork lift trucks are loaded on empty carts. The carts are then programmed for a destination in the warehouse by the production programming dispatcher. Computer punch cards are supplied to him daily or sometimes even hourly to tell him the proper destination for each load. If the destination or spur for which the cart is programmed is full, the cart will recirculate on the portion of the conveyor which forms the shortest closed loop past its assigned destination rather than recirculating the entire loop. Transfer sections allow carts to take a short-cut between sections of the loop so that they can reach their destination without traversing the entire 5600 foot main loop. They can travel around one segment of the loop in less than 30 minutes compared to 80 minutes for the entire loop. Empty carts can also recirculate and be removed as required to be loaded with complete orders for delivery to either the truck or rail docks, or with incoming shipments for storage.

As shown in Figure 1, there are decision points along the route at which logical considerations must be undertaken. For example, when a loaded cart from the manufacturing area and production programming dispatcher attempts to go on the main line, it may have to compete for a hook with a cart that is recirculating.

Since the cart on the main line has the right-of-way, the loaded cart from the production programming dispatcher must wait until an empty hook on the main line appears. It can then seize the hook and start to move on the main line. Figure 2 shows two carts moving from left to right and arriving at one of these decision points after having passed the truck dock.

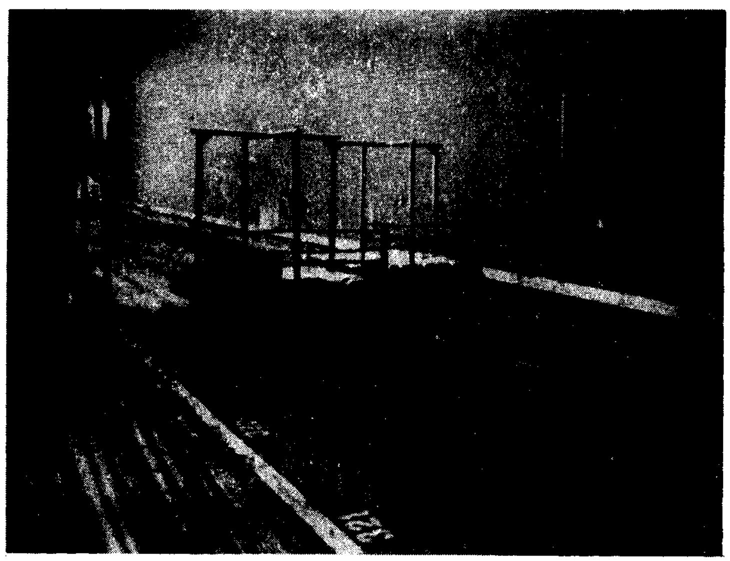

Figure 2. Merge Interface

The cart on the left is on the main line, is loaded, and has the right-of-way. The cart on the right has just been unloaded at the truck dock and placed on the powered spur empty. The empty car must wait and seize the hook directly behind the loaded cart to proceed along the main line. This decision point or interface occurs between functional components of the conveyor at four different locations along the line. For modeling purposes it will be identified as a MERGE module.

Another decision point occurs at each of the destination spurs that a cart passes. As the cart encounters each spur, it must decide if this is its destination or not, and if it is the proper destination, it must decide if the spur is full or not. Figure 3 shows carts moving from left to right.

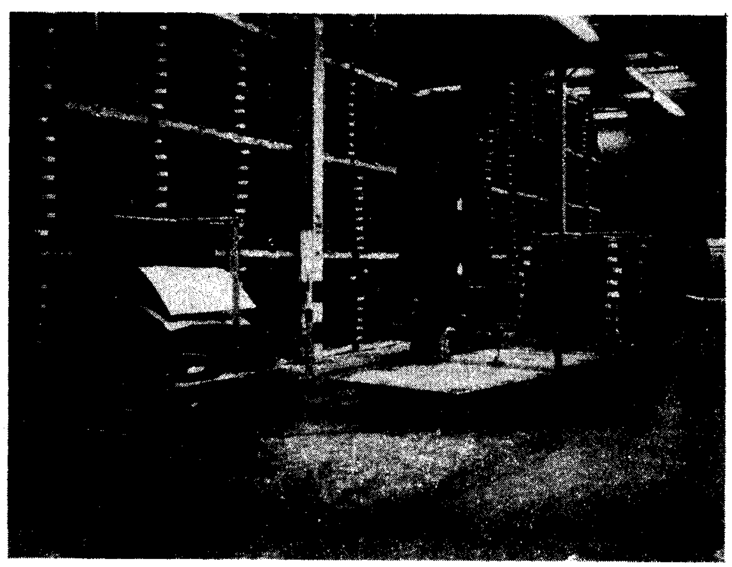

Figure 3. Unload and Load Station Interface

The four carts in the foreground (two empty and two loaded) which are bumper-to-bumper have been automatically side-tracked and stopped at their assigned destination spur. Each of these carts has been pushed further up the spur and out of the way by the following cart. Another loaded cart to the left of these four carts has just passed that destination spur, and since that spur is either full or is not its assigned destination, it is continuing on along the main line. There are nineteen destination spurs of this type along the conveyor. These spurs will be identified as an UNLOAD AND LOAD STATION module for modeling purposes.

There are also four points along the towline at which the cart has the option of taking a powered towline to the right or taking another powered towline to the left. There are several towlines in the system which disappear under the floor and reappear at other points. Figure 4 shows two carts moving from bottom to top. The cart on the right has selected the powered towline to the right since its destination lies in that direction. The cart on the left has selected the powered towline to the left since its destination lies in that direction. For modeling purposes, this interface or decision point will be identified as a SPLIT module.

The powered spur on which empty carts are loaded with finished goods from the manufacturing area is the final interface necessary to completely describe the conveyor system. There is only one of these spurs along the conveyor. The empty carts with this destination form a queue as shown in Figure 5. The carts are

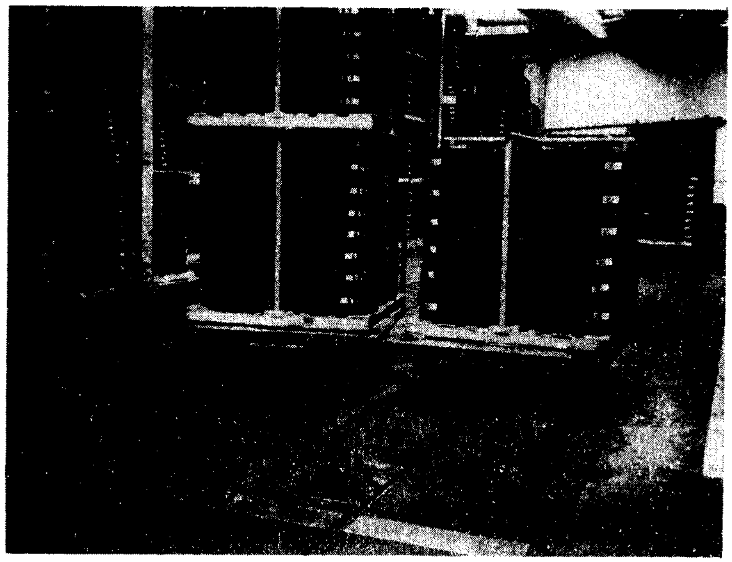

Figure 4. Split Interface

moving from bottom to top around the U-turn area and then toward the bottom. The first cart in the queue has been loaded and is waiting for the dispatcher to program and release it. In the model this spur will be identified as the PRODUCTION PROGRAMMING LOAD STATION module.

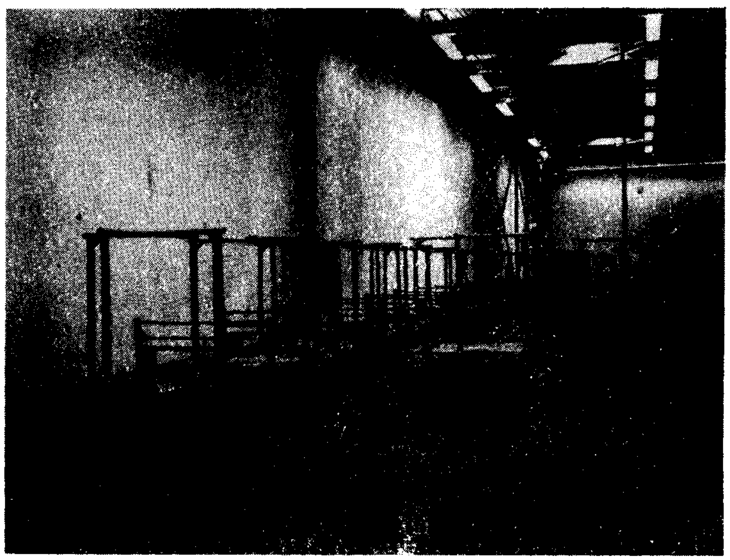

Figure 5. Production Programming Load Station Interface

CHAPTER IV

MODEL CONSTRUCTION AND VALIDATION

One of the most used general purpose techniques in modeling is the modular format. After the interfaces or decision points in the system had been identified and categorized, they were encoded as general purpose modules. These modules were then stacked together like building blocks to construct the entire conveyor system. The remainder of this chapter is a logical description of each of those modules and an argument for their validation.

Preliminary Considerations

Early in the research, it was decided to use GPSS/360 as the simulation language. This was done primarily for three reasons: (1) it is a discrete event oriented language in which one can easily encode and debug rather complex discrete event oriented systems, (2) it provides easily obtainable output statistics, and (3) the use of GPSS/360 MACRO statements lend themselves to a general purpose modular approach. The modules which had to be used several times in building the system were encoded in general purpose macros which could be used over and over by changing the various MACRO arguments.

The units of traffic that are created and move through a system encoded in GPSS/360 are called transactions. In this conveyor system a transaction represents either a hook or a cart. Each transaction possesses parameters as its key attributes. Only three parameters were necessary to describe the conveyor system transactions. The convention used in this model is: (1) P1 = 0 implies the transaction is a hook, P1 = 1 implies the transaction is a cart, (2) P2 = 0 implies the transaction is an empty cart, P2 = 1 implies the transaction is a loaded cart, and (3) P3 = 0,1,2,...19 implies the cart has been assigned any one of twenty possible destinations around the loop. All the transactions were given a Priority = 1 initially. This was necessary for timing and logical considerations in the MERGE module which will be discussed later. Three savevalues, X1, X2, and X3, were used and will be described in the next section.

Since GPSS/360 is oriented toward integer-valued variables, the unit of time used in the model is milliminutes, or the clock time is scaled by a factor of 1000.

Near the end of each of the general purpose modules is an ADVANCE block which delays each transaction the specific clock time that it would take that transaction to move on the conveyor to the next sequential module. The transactions are evenly spaced in time around the conveyor since the conveyor is a constant speed discretely spaced recirculating system.

Cart and Hook Generator Module

The CART AND HOOK GENERATOR module actually builds the conveyor system by filling it with hooks and carts. Once the system becomes full of hooks and all the carts are placed somewhere in the system, this module becomes inoperative. There is only one CART AND HOOK GENERATOR (CAHG) module in the system, and it is designed to be placed directly before the PRODUCTION PROGRAMMING LOAD STATION (PPLS) module.

General Description

The CAHG module may be represented as a box shown in Figure 6. The entrance to the module is labelled NTR. There is only one exit from the module.

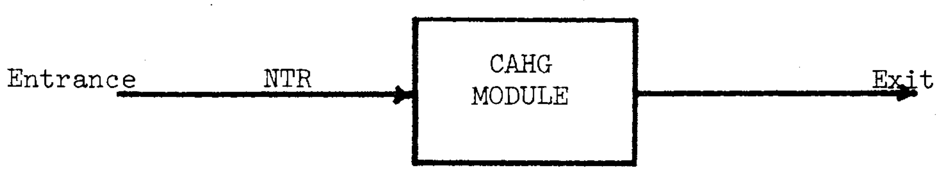

Figure 6. Cart and Hook Generator Module

The module generates empty carts until some user specified upper limit is reached. It also generates hooks until the first transaction which enters the module at NTR shuts off the hook generator.

This module also has the capability to assist the system in reaching steady state very rapidly by channelling empty carts into the system when the PPLS spur becomes full and queue CARS is not empty.

Detailed Description

The first part of this module is the cart generator. A variable is used to calculate the delay time between succeeding hooks on the powered towline. X2 is initialized at the hook spacing and X3 at the conveyor speed.

```
1 VARIABLE          (X2*1000)/X3
```

The formula used to calculate this delay time in milliminutes is given below.

(Hook spacing)*(1000)/(Conveyor Speed)

The empty carts are created by the next sequential block.

```
GENERATE            V1,,,X1,,3
```

The carts are generated at the same interval as the hook spacing and only X1 (initialized at the number of carts in the system) carts are generated.

The empty carts then enter a queue of empty carts and attempt to seize the facility which allows them to capture a hook and begin to move on the towline.

```
QUEUE               CARS
SEIZE               CAR
```

The facility consists of a logic gate which is opened by an empty hook later in this module.

```
GATE LS             20
```

The empty cart which has just passed through this gate then closes the gate behind it before departing the queue, releasing the facility and destroying itself.

```
      LOGIC R        20
      DEPART         CARS
      RELEASE        CAR
TERM  TERMINATE
```

The empty cart is destroyed because the hook which it captured has now been transformed into the empty cart as will be shown later in this module.

The hooks are created by the next sequential block in this module.

```
      GENERATE       V1,,,,1,3
```

These hooks have a priority equal to one and three parameters. They are created at the hook spacing defined by the user in variable number one.

The hooks then enter a logic gate which allows them to proceed to the next sequential block unless a transaction has set logic switch 19. If logic switch 19 has been set, the hooks are then sent to the alternate exit which directs them to the TERMINATE block.

```
      GATE LR        19,TERM
```

The purpose of this block is to shut off the hook generator once the closed loop which contains this module becomes full of hooks. This means the powered towline has been completely constructed and the hook generator is no longer needed.

The newly created hook is then transfered around the entrance to this module to location BEGN.

```
      TRANSFER       ,BEGN
```

The entrance to this module is labelled NTR and the first transaction which completes the closed loop and enters this module at NTR shuts off the hook generator by setting logic switch 19 as has been discussed previously.

```
NTR  LOGIC S          19
```

The transaction which proceeds to the next sequential block may be either a hook or a cart. It is first tested to determine what it is.

```
BEGN TEST E           P1,0,SKIP
```

If it is a hook (P1 = 0), it proceeds to the next sequential block. If it is a cart (P1 = 1), it takes the alternate exit and is directed to location SKIP.

A hook then encounters another TEST block which determines if there are any empty carts in the queue called CARS waiting to capture a hook. If queue CARS is zero, the hook takes the alternate exit and is directed to location SKIP.

```
     TEST G           Q$CARS,0,SKIP
```

If there are carts waiting in the queue, the hook proceeds to the next sequential block.

In the next block, the hook determines if the powered spur which feeds the PPLS module is full of carts or not. The maximum capacity of this spur is determined by the user and in this case it is 35 cars.

```
     TEST LE          Q$LCR1,35,BYPS
```

If the spur is not full, the hook proceeds to the next sequential block. If the spur is full, the hook takes the alternate exit and is directed to location BYPS.

A hook continuing to the next sequential block sets logic switch 20 which opens the gate for an empty cart as discussed earlier in this module.

LOGIC S 20

The empty cart is terminated and the hook is now transformed into an empty cart by placing a one in parameter one.

ASSIGN 1,1

All the transactions which were directed to location SKIP from various places in the module and the newly formed empty carts are transfered to the entrance to the PPLS module.

SKIP TRANSFER ,LST1

The last section of this module is a technique to assist the conveyor model to reach steady state very rapidly. When the PPLS powered spur is full of empty carts waiting to be loaded and there is a pool of empty carts waiting in queue CARS to enter the model also, the carts in queue CARS are short-circuited into the model empty just to get them into the system. The first block that a hook going through this section of the model encounters sets logic switch 20 to open the gate for an empty cart as discussed earlier.

BYPS LOGIC S 20

Another hook is created and sent to location LH01 in the PPLS module. This is done to preserve the timing and logic of the conveyor system.

SPLIT 1,LH01

The hook which proceeds to the next sequential block is transformed into an empty cart by changing parameter one to a one.

ASSIGN 1,1

The empty cart is then given a destination by a function which is defined by the user.

ASSIGN 3,FN$DECP

The cart is then transferred into the PPLS module at a point where it can capture a hook and go on line without having to wait to be loaded.

TRANSFER ,LSZ1

A source listing of the CAHG module is given in Figure 7 and the module flow chart is given in Figure 8.

```
   1 VARIABLE     (X2*1000)/X3
     GENERATE     V1,,,X1,,3
     QUEUE        CARS
     SEIZE        CAR
     GATE LS      20
     LOGIC R      20
     DEPART       CARS
     RELEASE      CAR
TERM TERMINATE
     GENERATE     V1,,,,1,3
     GATE LR      19,TERM
     TRANSFER     ,BEGN
 NTR LOGIC S      19
BEGN TEST E       P1,0,SKIP
     TEST G       Q$CARS,0,SKIP
     TEST LE      Q$LCR1,35,BYPS
     LOGIC S      20
     ASSIGN       1,1
SKIP TRANSFER     ,LST1
BYPS LOGIC S      20
     SPLIT        1,LH01
     ASSIGN       1,1
     ASSIGN       3,FN$DECP
     TRANSFER     ,LSZ1
```

Figure 7. Source Listing of CAHG Module

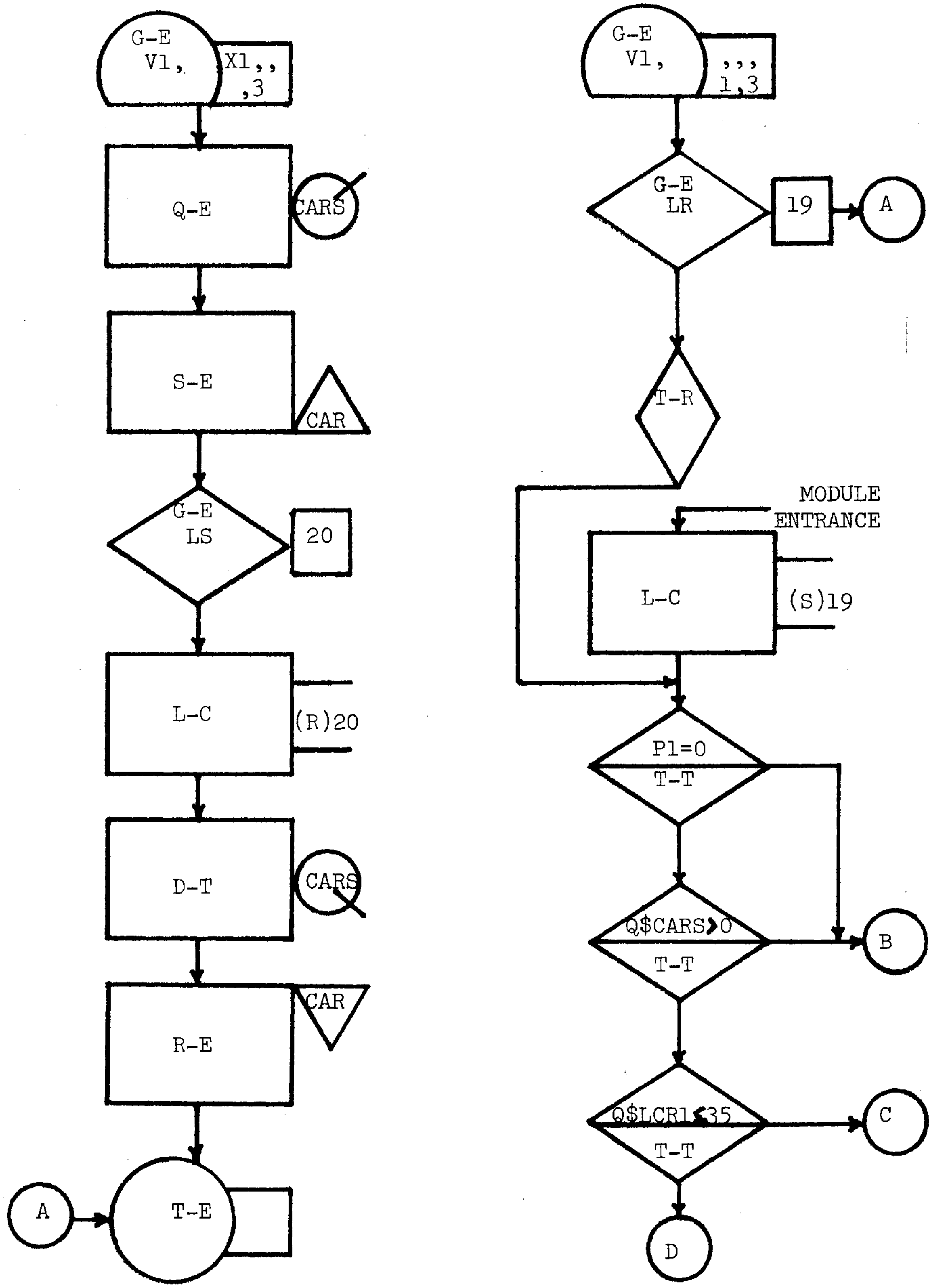

Figure 8. Flow Chart of CAHG Module

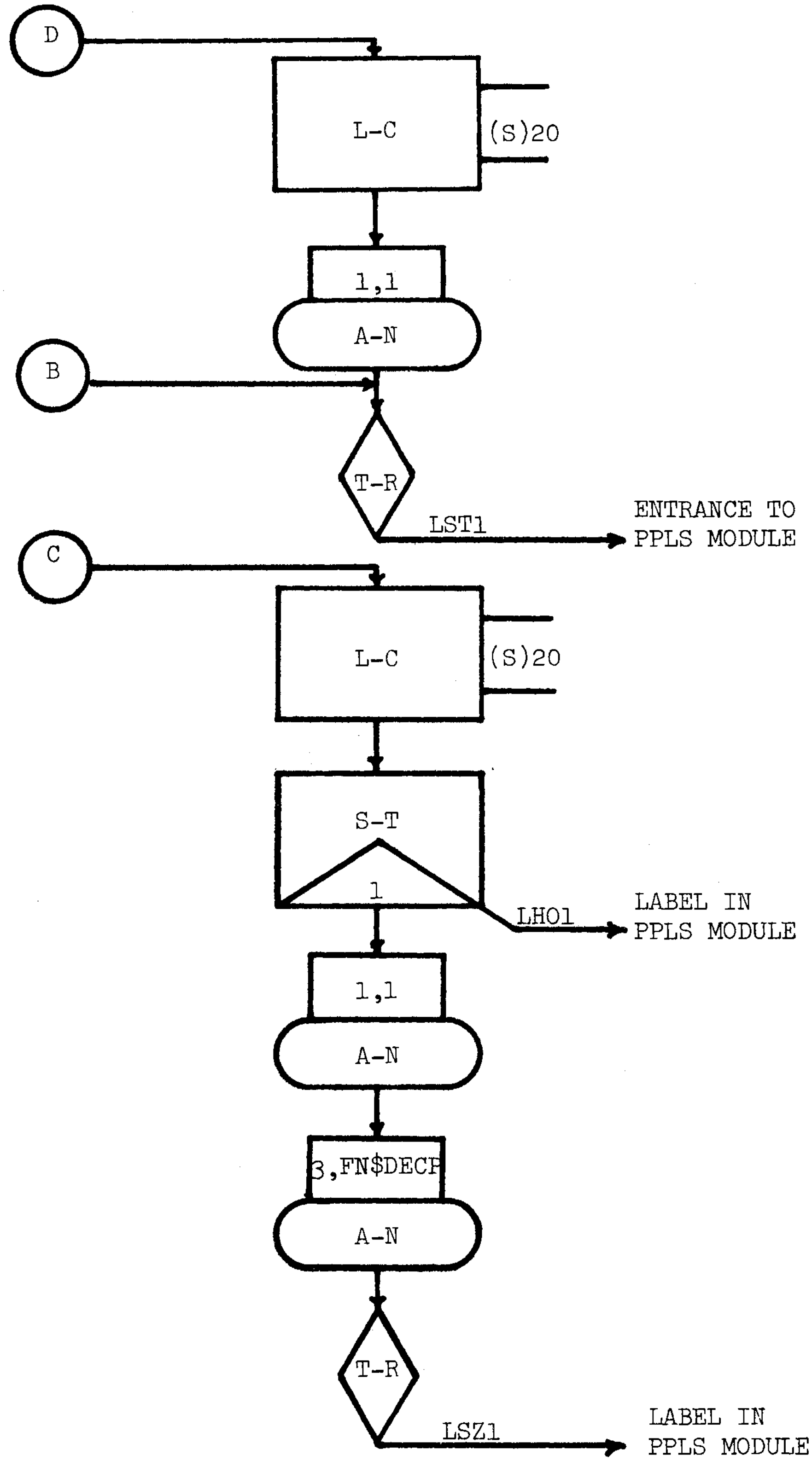

Figure 8. (Continued)

Production Programming Load Station Module

The module which must immediately follow the CAHG module is the PRODUCTION PROGRAMMING LOAD STATION (PPLS) module. This module is an interface in the system at which empty carts are loaded with finished goods from the manufacturing area. The carts are given a destination and placed on the conveyor by the dispatcher.

General Description

The PPLS module may be represented as a box shown in Figure 9. The entrance to the module is labelled LST1, and there is only one exit from the module. In this module empty carts are delayed by a user specified load time and are given a destination by a user specified function. The user must also specify the distance to the next module entrance. The logic in this module maintains the integrety and timing of the powered towline as hooks and carts pass through it.

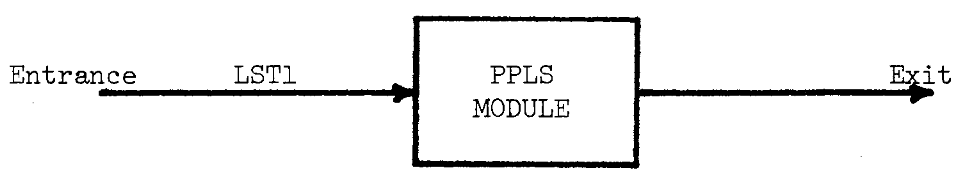

Figure 9. Production Programming Load Station Module

Detailed Description

The entrance to the module is labelled LST1, and the first block in the module determines if the entering transaction is a cart or a hook.

```
LST1 TEST E             P1,1,LHK1
```

A hook takes the alternate exit and is transferred to location LHK1. A cart proceeds to the next block.

The cart then causes a new transaction to be created, and the cart

```
     SPLIT              1,LEC1
```

is transferred to location LEC1.

The newly created transaction is transformed into a hook.

```
LHO1 ASSIGN             1,0
     ASSIGN             2,0
     ASSIGN             3,0
```

The hook then passes through a logic gate which either allows the hook to proceed to the next sequential block or transfers it to location LTH1.

```
LHK1 GATE LR            3,LTH1
```

If the hook proceeds to the next sequential block, it is transferred to the end of this module.

```
     TRANSFER           ,LSO1
```

If the hook transfers to LTH1, then a cart has captured it and will be taking its place on the conveyor.

The cart which was transferred to location LEC1 joins the queue of carts waiting to be loaded at the PPLS module.

```
LEC1 QUEUE           LCR1
```

To save CPU time these carts are linked onto user chain LCH on a FIFO basis.

```
     LINK            LCH,FIFO,LFA1
```

A cart may then seize the loading facility and depart the queue.

```
LFA1 SEIZE           LCR1
     DEPART          LCR1
```

If the cart is already loaded it is transferred around the loader to location LDC1.

```
     TEST E          P2,0,LDC1
```

An empty cart proceeds and enters into the in process storage.

```
     ENTER           IPS
```

It is then delayed while being loaded. The mean and spread modifier are specified by the user. In this case the load time is a normally distributed random variable with a mean of two minutes and a standard deviation of .4 minutes.

```
LVB1 VARIABLE        FN$NORM*400
     ADVANCE         2000,V$LVB1
```

The function NORM is the standard normal function which uses random number generator number one.

The empty cart is transformed into a loaded cart by changing parameter two to a one.

```
     ASSIGN          2,1
```

And the loaded cart is given a destination by a user defined function. In this case the function is called DLCP.

```
     ASSIGN          3,FN$DLCP
```

The loaded cart releases the loading facility and unlinks the next cart from the user chain.

```
LDC1 RELEASE          LCR1
     UNLINK           LCH,LFA1,1
```

The cart then attempts to seize a facility that consists of the logic necessary to capture a hook and proceed on line.

```
LSZ1 SEIZE            LCH1
```

After seizing the facility the cart sets logic switch three which indicates to the next available hook that a cart is waiting to capture it.

```
     LOGIC S          3
```

The cart then stops at the logic gate to wait for a hook to open it.

```
     GATE LR          3
```

Once the gate is opened by a hook, the cart releases the facility to go on line and transfers to the end of the PPLS module.

```
     RELEASE          LCH1
     TRANSFER         ,LS01
```

A hook which has been destined to be captured by a waiting cart opens the cart's logic gate by resetting logic switch three and the hook is destroyed.

```
LTH1 LOGIC R          3
     TERMINATE
```

The end of the module is of course an ADVANCE block which delays a transaction the length of time it takes it to travel on the towline to the next sequential module. The delay time is calculated in a variable which is defined by the user. The formula used to calculate the delay time in milliminutes in this case is shown below.

((Distance to next module)/(Conveyor Speed))*(1000)

The transaction is finally transferred to the next sequential module or module entrance.

```
LAV1 FVARIABLE          (55/X3)(1000)

LS01 ADVANCE            V$LAV1

     TRANSFER           ,MA0
```

A source listing of the PPLS module is given in Figure 10 and a flow chart of the module is shown in Figure 11.

```
LST1 TEST E         P1,1,LHK1
     SPLIT          1,LEC1
LH01 ASSIGN         1,0
     ASSIGN         2,0
     ASSIGN         3,0
LHK1 GATE LR        3,LTH1
     TRANSFER       ,LS01
LEC1 QUEUE          LCR1
     LINK           LCH,FIFO,LFA1
LFA1 SEIZE          LCR1
     DEPART         LCR1
     TEST E         P2,0,LDC1
     ENTER          IPS
LVB1 VARIABLE       FN$NORM*400
     ADVANCE        2000,V$LVB1
     ASSIGN         2,1
     ASSIGN         3,FN$DLCP
LDC1 RELEASE        LCR1
     UNLINK         LCH,LFA1,1
LSZ1 SEIZE          LCH1
     LOGIC S        3
     GATE LR        3
     RELEASE        LCH1
     TRANSFER       ,LS01
LTH1 LOGIC R        3
     TERMINATE
LAV1 FVARIABLE      (55/X3)(1000)
LS01 ADVANCE        V$LAV1
     TRANSFER       ,MA0
```

Figure 10. Source Listing of PPLS Module

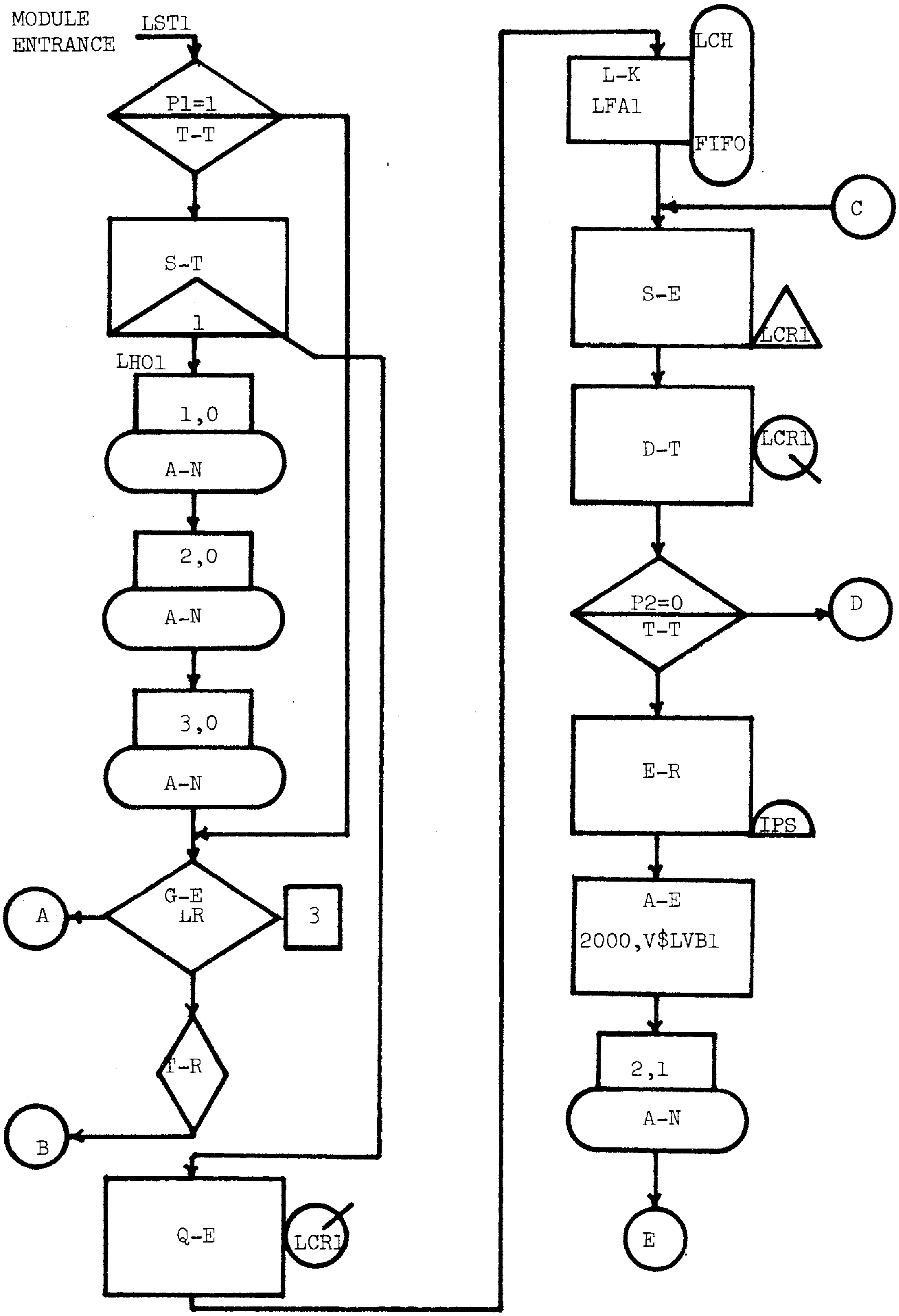

Figure 11. Flow Chart of PPLS Module

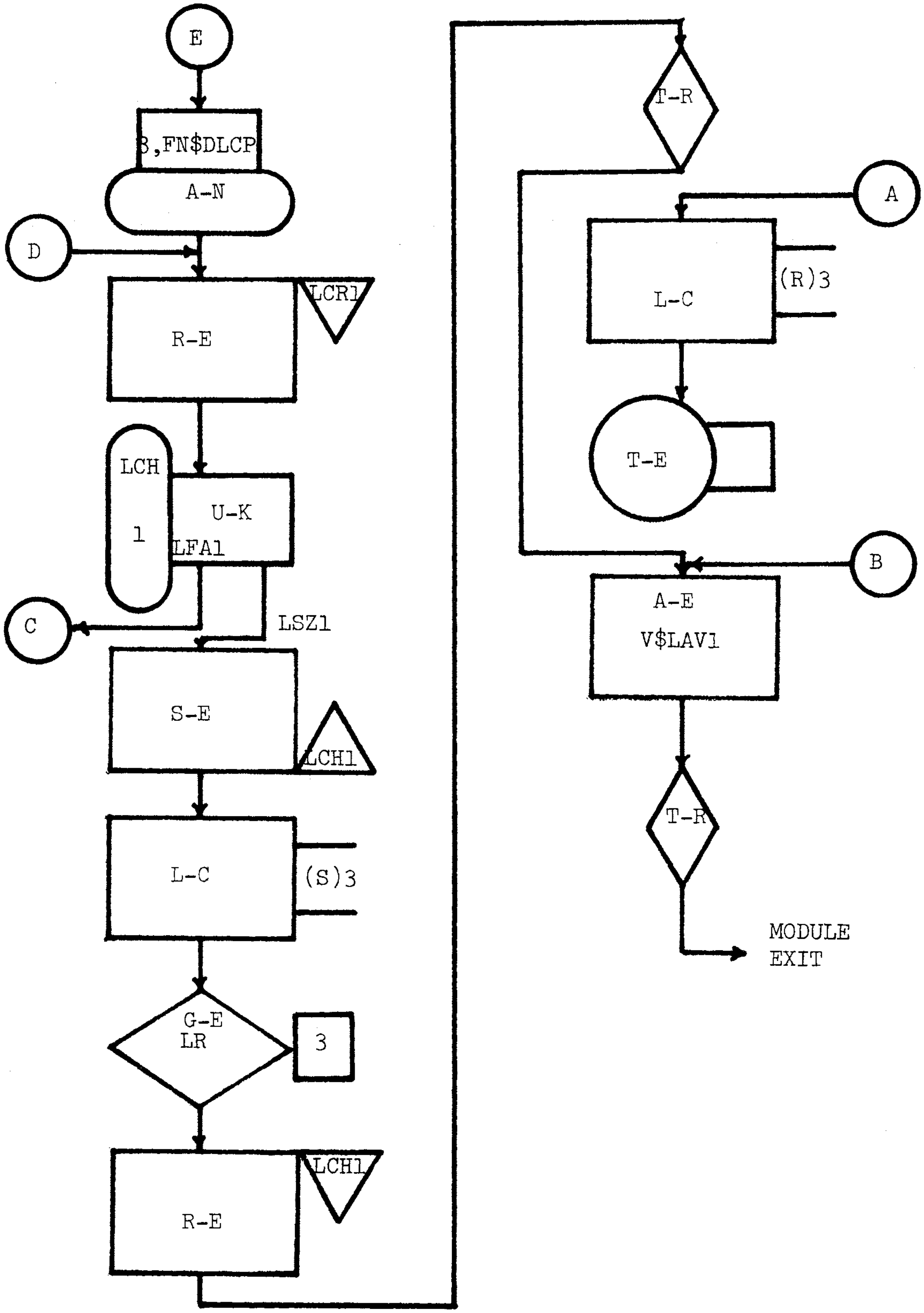

Figure 11. (Continued)

Split Module

The SPLIT module which has been described in Chapter III is a decision point in the system at which a cart must decide to take either the right or left powered towline.

General Description

The SPLIT module may be represented as a box shown in Figure 12 which has one entrance and two exits. A transaction which enters this module can not be delayed since there are no blocks in this module which can deny entry to a transaction.

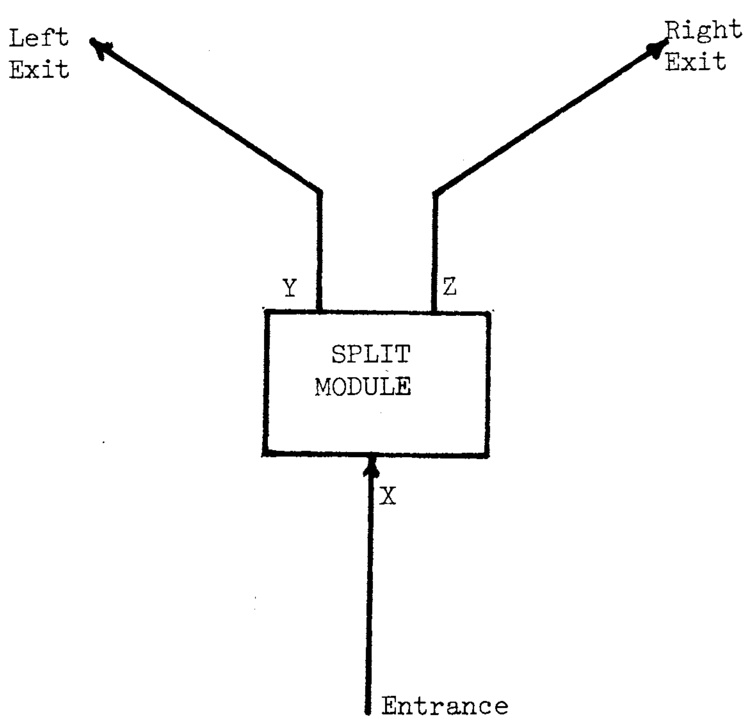

Figure 12. Split Module

There are three types of transactions which enter this module. The logic is designed to process each of these three types as separate cases.

Case 1. (X = hook) If a hook enters the SPLIT module, then another hook will be created in the module, and a hook will be sent to each exit. (Y = hook and Z = hook)

Case 2. (X = cart whose destination lies to the left) If a cart which desires to go to the left enters, then a hook will be created and sent to the right. (Y = cart and Z = hook)

Case 3. (X = cart whose destination lies to the right) If a cart which desires to go to the right enters, then a hook will be created and sent to the left. (Y = hook and Z = cart)

Detailed Description

The first statement that an entering transaction encounters in this module determines if the transaction is a hook or a cart.

```
     TEST  E          P1,1,HOOK
```

A cart continues on to the next sequential block or a hook takes the alternate exit and is transferred to location HOOK.

A cart which continues to the next sequential block is tested to see if its destination lies to the right or to the left. This is done by means of a boolean variable and a TEST block.

```
   1 BVARIABLE        P3'GE'9*P3'L'17
     TEST  E          BV1,1,CRGHT
```

If the value of the boolean variable is one, the cart's destination is to the left and it proceeds to the next sequential block. If the value of the boolean variable is zero, the cart's destination is to the right and the cart takes the alternate exit and is transferred to location CRGHT. The boolean variables are defined by the user and may vary in form in different SPLIT mdoules.

The cart whose destination is left proceeds to the next sequential block.

TEST LE Q$LCR1,999,CRGHT

The arguments of this block are defined by the user and the condition must be true for a cart to proceed to the left. In the case shown, the queue of cars waiting to be loaded at the PPLS module must be less than or equal to 999. Since there are only 380 carts in the system, this block has no effect on the system. If the 999 were changed to 36 in one of the SPLIT modules and the queue of empty carts at the PPLS module was greater than 36, then a cart whose destination lies to the left would be sent to the right to recirculate in the system by taking the alternate exit CRGHT.

A car proceeding to the left encounters the next block.

SPLIT 1,HRGHT

Since the timing and integrety of both powered towlines must be maintained, a hook is created and sent to location HRGHT which sends it to the right.

The cart is then transfered to the ADVANCE block which delays the cart for the time it takes it to reach the next module to the left.

TRANSFER ,ALEFT

The hook that has been created and sent to the right is first made into a hook by setting all three parameters

```
HRGHT ASSIGN            1,0
      ASSIGN            2,0
      ASSIGN            3,0
```

equal to zero.

The hook is then transfered to the ADVANCE block which delays the hook for the time it takes it to reach the next module to the right.

```
      TRANSFER          ,ARGHT
```

A car proceeding to the right encounters the next block.

```
CRGHT SPLIT             1,HLEFT
```

A hook is created and sent to location HLEFT which sends it to the left to maintain the timing and integrety of both powered towlines.

The cart is then transfered to the ADVANCE block which delays the cart for the time it takes it to reach the next module to the right.

```
      TRANSFER          ,ARGHT
```

The hook that has been created and sent to the left is first made into a hook by setting all three parameters equal to zero.

```
HLEFT ASSIGN            1,0
      ASSIGN            2,0
      ASSIGN            3,0
```

The hook is then transfered to the ADVANCE block which delays the hook for the time it takes it to reach the next module to the left.

```
     TRANSFER          ,ALEFT
```

A hook which enters this module at the entrance is split into two hooks so that a hook can leave at each of the two exits. The following two blocks perform this function.

```
HOOK SPLIT             1,ALEFT
     TRANSFER          ,ARGHT
```

The delay time to the next module is calculated using variables and the time is in milliminutes. The formula used is given by:

(Distance to next module)*(1000)/(Conveyor Speed).

The last blocks in this module are the ADVANCE block and exits of the module which have been previously discussed.

```
    1 VARIABLE         236*1000/X3
ALEFT ADVANCE          V1
      TRANSFER         ,MODULE TO LEFT
    2 VARIABLE         60*1000/X3
ARGHT ADVANCE          V2
      TRANSFER         ,MODULE TO RIGHT
```

A source listing of the SPLIT module is given in Figure 13 and a flow chart of the module is shown in Figure 14.

Unload and Load Station Module

The UNLOAD AND LOAD STATION (UALS) module is a general purpose module that occurs in the conveyor system at points where a cart may or may not decide to sidetrack itself at one of the unpowered spurs. Here the cart is unloaded and or loaded, and then placed back on the towline.

```
      TEST E         P1,1,HOOK
    1 BVARIABLE      P3'GE'9*P3'L'17
      TEST E         BV1,1,CRGHT
      TEST LE        Q$LCR1,999,CRGHT
      SPLIT          1,HRGHT
      TRANSFER       ,ALEFT
HRGHT ASSIGN         1,0
      ASSIGN         2,0
      ASSIGN         3,0
      TRANSFER       ,ARGHT
CRGHT SPLIT          1,HLEFT
      TRANSFER       ,ARGHT
HLEFT ASSIGN         1,0
      ASSIGN         2,0
      ASSIGN         3,0
      TRANSFER       ,ALEFT
 HOOK SPLIT          1,ALEFT
      TRANSFER       ,ARGHT
    1 VARIABLE       236*1000/X3
ALEFT ADVANCE        V1
      TRANSFER       ,MODULE TO LEFT
    2 VARIABLE       60*1000/X3
ARGHT ADVANCE        V2
      TRANSFER       ,MODULE TO RIGHT
```

Figure 13. Source Listing of SPLIT Module

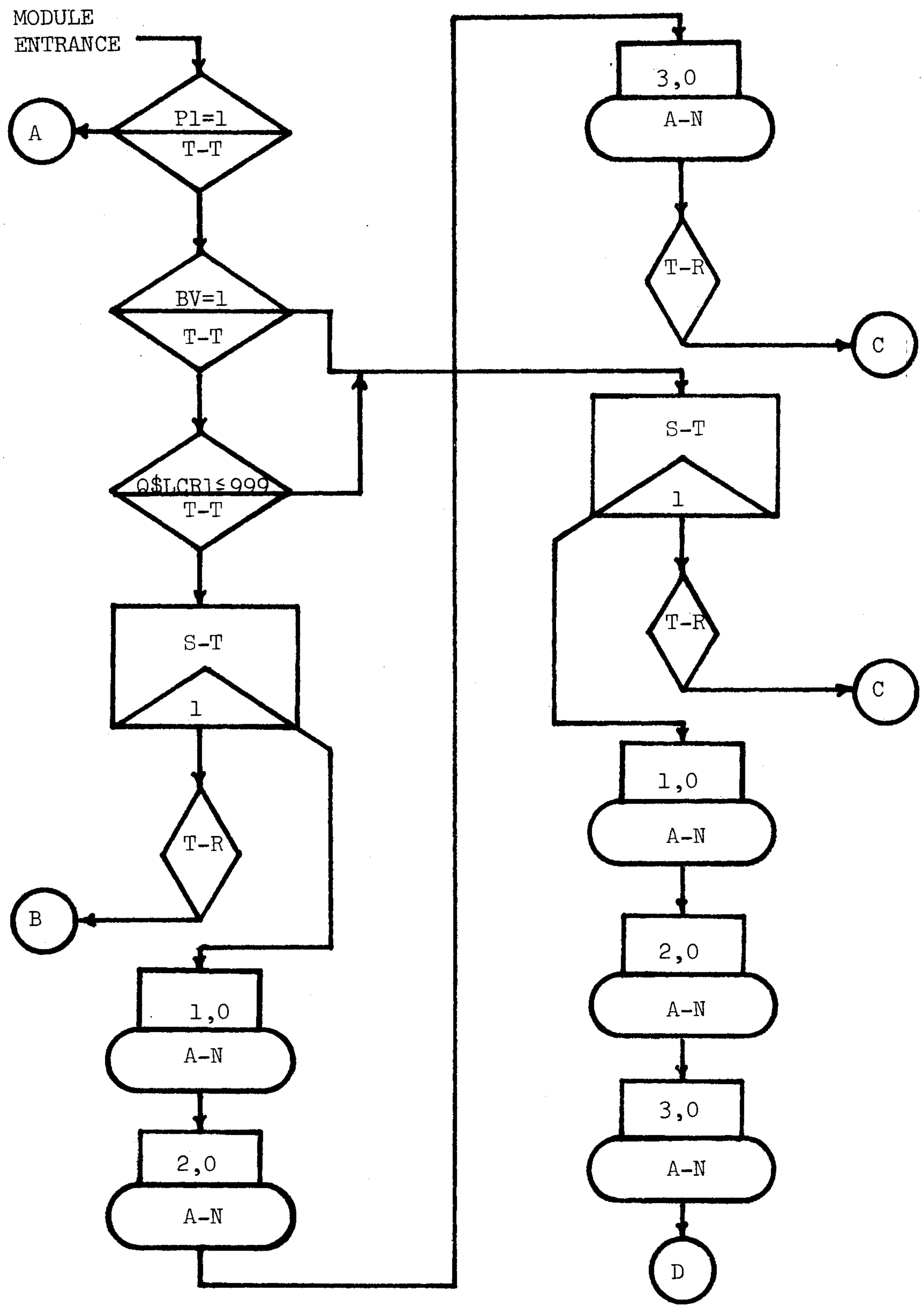

Figure 14. Flow Chart of SPLIT Module

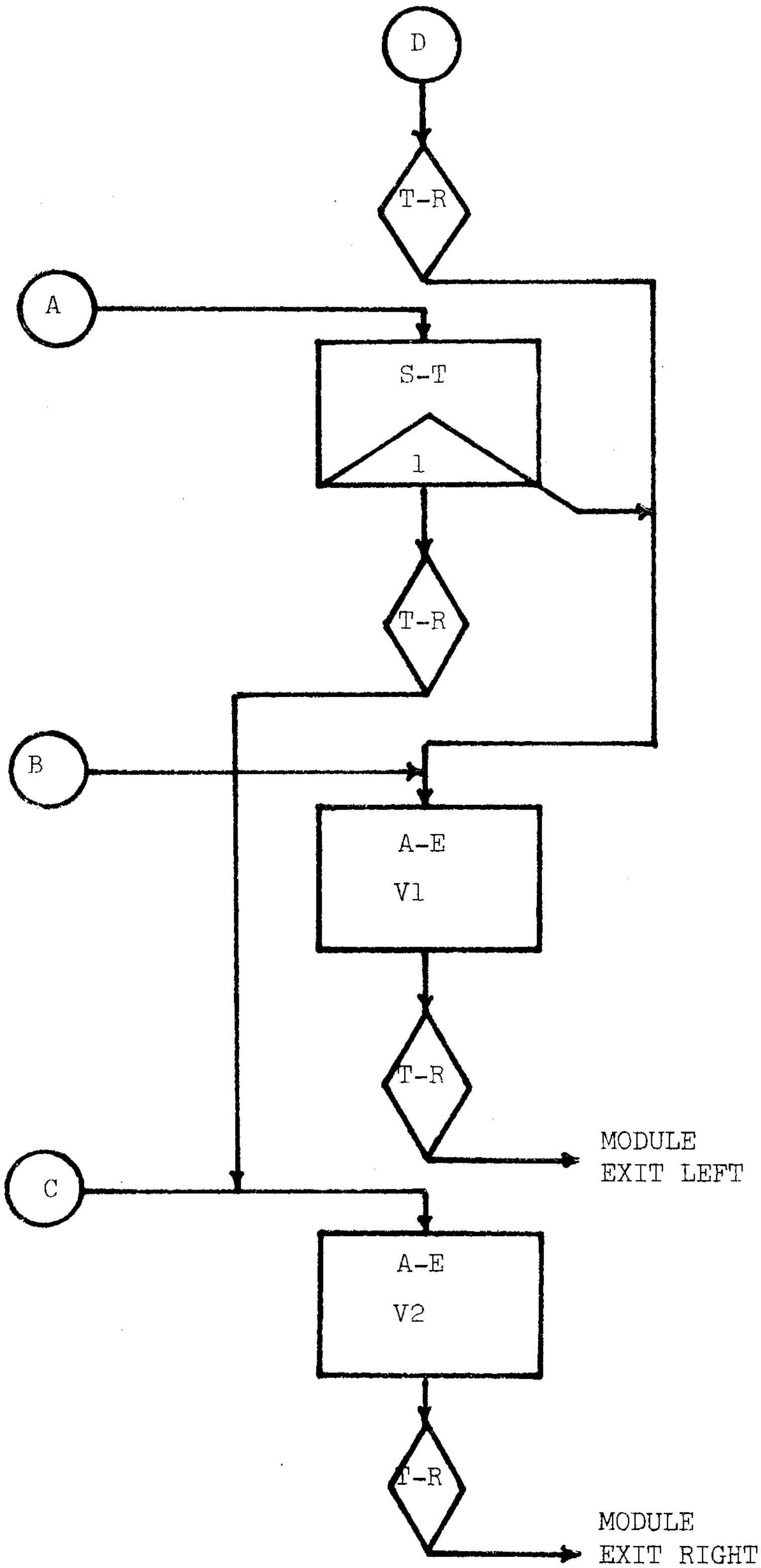

Figure 14. (Continued)

General Description

The UALS module may be represented as a box shown in Figure 15. Any transaction may enter this module; however, only those carts with the proper destination are allowed to be unloaded and or loaded. The module has only one entrance and one exit.

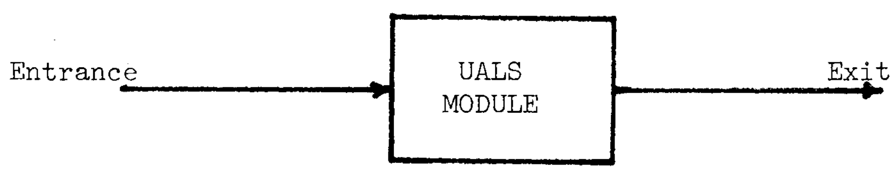

Figure 15. UALS Module

The user defines the load and unload times and the maximum station queue. The user also defines the maximum number of empty carts if any to keep at the station at all times. Destination functions and the distance to the next module entrance must be supplied by the user. The module logic maintains the timing of the towline as it passes through it.

Detailed Description

The first block that an entering transaction encounters in the UALS module determines if it is a cart or a hook.

```
ENTR TEST  E             P1,1,HOKE
```

A hook is sent to location HOKE.

A cart proceeds and is tested to determine if this module is its destination or not.

```
     TEST  E             P3,8,EXIT
```

If this module is not the proper destination, the cart is sent to the exit.

A cart whose destination is this module is tested again to determine if the station queue is full or not.

```
     TEST  L             Q$STA,15,EXIT
```

If the station queue is greater than or equal to some user specified number, the cart is sent to the exit to recirculate in the system.

If the station queue is smaller than the user specified number, the cart joins the station queue.

```
     QUEUE               STA
```

A transaction is then created and sent to location HOKE to be transformed into a hook to preserve the timing and integrety of the towline.

```
     SPLIT               1,HOKE
```

The cart is tested to determine if it is loaded or empty.

```
     TEST  E             P2,1,ECAR
```

An empty car is sent to location ECAR.

A loaded car proceeds and attempts to seize the unloading facility.

```
     SEIZE          UNLDR
```

The unload time is specified by the user and in this case it is a normally distributed random variable with a mean of four minutes and a standard deviation of .8 minutes.

```
UAV  VARIABLE       FN$NORM*800
     ADVANCE        4000,V$UAV
```

The cart is now unloaded and must leave the in process storage.

```
     LEAVE          IPS
```

The unloaded cart's parameter two is changed to zero to indicate that it is now empty and the unload facility is released.

```
     ASSIGN         2,0
     RELEASE        UNLDR
```

A policy that may or may not be adopted at the load and unload station modules is to keep a number of empty carts at the station to be loaded later on. The user specifies the maximum number empty carts to be retained at the station. After the empty cart releases the unload facility, it determines if the maximum number of empty carts is present at the station or not. If maximum number is not present, the empty cart is transferred to the queue of empty carts waiting at the station.

```
     TEST  GE       CH$UCH,1,ECAR
```

If the empty cart queue is at its maximum number, the empty cart continues to the next sequential block. The cart is given a destination by a user defined function and is transfered to a location in the module, FGOL, where it can capture a hook and go on line.

```
     ASSIGN         3,FN$DEC1
     TRANSFER       ,FGOL
```

Empty carts waiting to be loaded enter the empty car queue and then are linked onto user chain UCH.

```
ECAR QUEUE          ECAR
     LINK           UCH,FIFO,UCHO
```

One empty cart determines if the chain has reached its maximum number or not.

```
UCHO TEST  G        CH$UCH,1
```

When the number of empty carts becomes greater than the user specified maximum, the empty cart can seize the loading facility and depart the empty car queue.

```
     SEIZE          LDR
     DEPART         ECAR
```

The loading time is specified by the user and in this case it is a normally distributed random variable with a mean of two minutes and a standard deviation of .4 minutes.

```
UVL  VARIABLE       FN$NORM*400
     ADVANCE        2000,V$UVL
```

Since the cart has been loaded, it can now enter the in process storage and be designated as a loaded cart by changing parameter two to a one.

```
     ENTER          IPS
     ASSIGN         2,1
```

The loaded cart then releases the loading facility, unlinks the next empty cart from the user chain, and is assigned a destination by a user defined function.

```
     RELEASE        LDR
     UNLINK         UCH,UCH0,1
     ASSIGN         3,FN$DLC1
```

The logic necessary for a cart to capture a hook and proceed on the towline is contained in facility FGOL. The cart seizes the facility, sets logic switch four, and waits at a logic gate for a hook to open it.

```
FGOL SEIZE          FGOL
     LOGIC S        4
     GATE  LR       4
```

Once a hook has reset logic switch four, the cart can proceed through the gate release the facility, depart the station queue, and be transferred to the module exit.

```
     RELEASE        FGOL
     DEPART         STA
     TRANSFER       ,EXIT
```

A hook which enters this module or is created in this module is transferred to location HOKE where it is transformed into a hook.

```
HOKE ASSIGN         1,0
     ASSIGN         2,0
     ASSIGN         3,0
```

The hook then determines if a cart is waiting to capture it by passing through a logic gate.

```
     GATE LR           4,THKE
```

If no cart is waiting, the hook is transferred to the exit.

```
     TRANSFER           ,EXIT
```

If a cart is waiting, the hook takes the logic gate alternate exit THKE, resets logic switch four which allows the cart to proceed by opening its gate, and then the hook is destroyed.

```
THKE LOGIC R           4
     TERMINATE
```

The module exit of course consists of an ADVANCE block which delays the transaction for the time it takes it to reach the next module.

```
 UVB VARIABLE          (120*1000)/X3
EXIT ADVANCE           V$UVB
```

The transaction continues to the next sequential module.

A source listing of the UALS module is given in Figure 16 and a flow chart of the module is shown in Figure 17.

Merge Module

The MERGE module which has been previously described is a decision point or interface in the system at which two different powered towlines come together to form one powered towline.

General Description

The MERGE module may be represented as a box shown in Figure 18. This module has two entrances. Carts at the ROW

```
ENTR TEST E        P1,1,HOKE
     TEST E        P3,8,EXIT
     TEST L        Q$STA,15,EXIT
     QUEUE         STA
     SPLIT         1,HOKE
     TEST E        P2,1,ECAR
     SEIZE         UNLDR
 UAV VARIABLE      FN$NORM*800
     ADVANCE       4000,V$UAV
     LEAVE         IPS
     ASSIGN        2,0
     RELEASE       UNLDR
     TEST GE       CH$UCH,1,ECAR
     ASSIGN        3,FN$DEC1
     TRANSFER      ,FGOL
ECAR QUEUE         ECAR
     LINK          UCH,FIFO,UCHO
UCHO TEST G        CH$UCH,1
     SEIZE         LDR
     DEPART        ECAR
 UVL VARIABLE      FN$NORM*400
     ADVANCE       2000,V$UVL
     ENTER         IPS
     ASSIGN        2,1
     RELEASE       LDR
     UNLINK        UCH,UCHO,1
     ASSIGN        3,FN$DLC1
FGOL SEIZE         FGOL
     LOGIC S       4
     GATE LR       4
     RELEASE       FGOL
     DEPART        STA
     TRANSFER      ,EXIT
HOKE ASSIGN        1,0
     ASSIGN        2,0
     ASSIGN        3,0
     GATE LR       4,THKE
     TRANSFER      ,EXIT
THKE LOGIC R       4
     TERMINATE
 UVB VARIABLE      (120*1000)/X3
EXIT ADVANCE       V$UVB
```

Figure 16. Source Listing of UALS Module

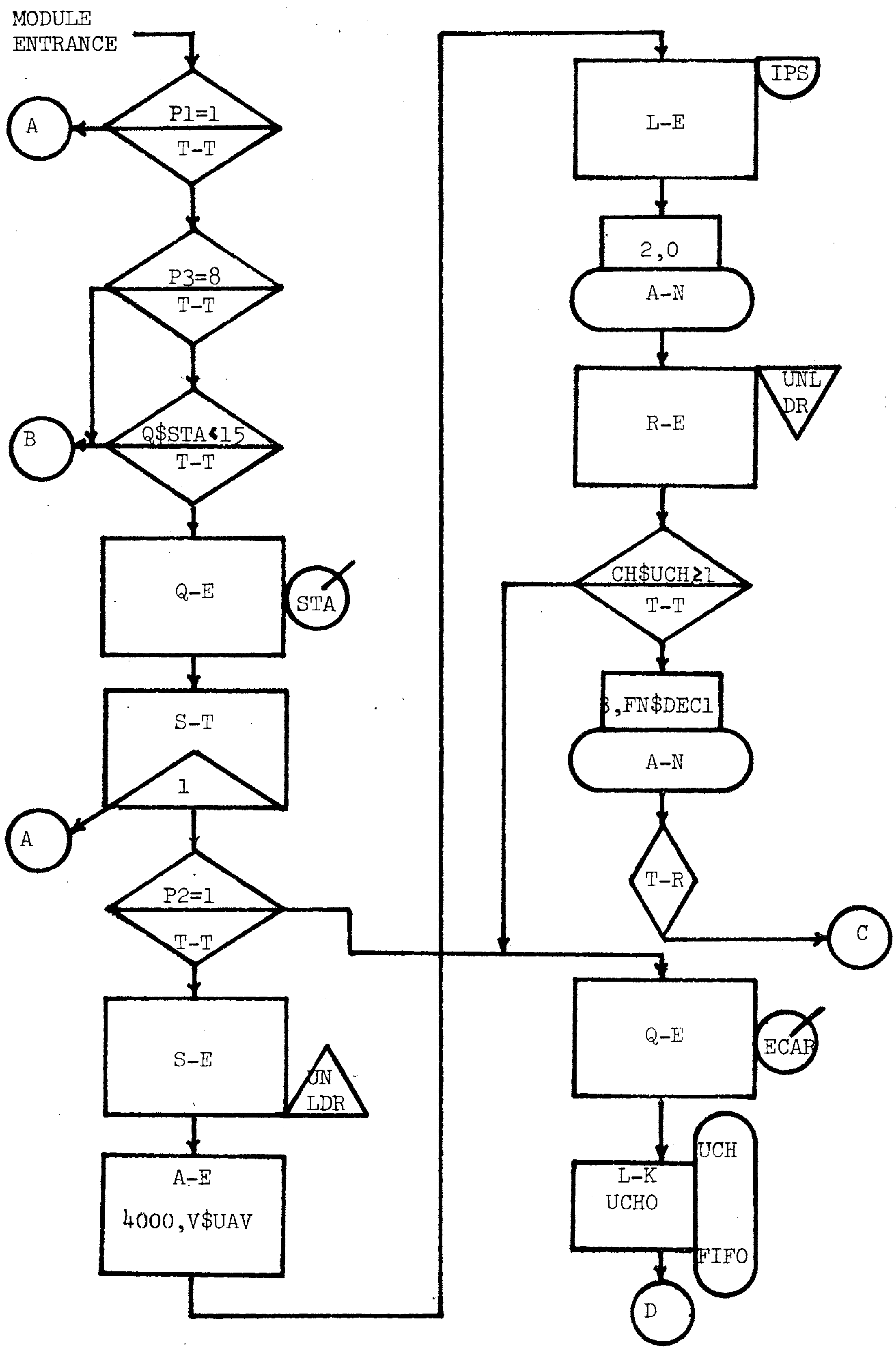

Figure 17. Flow Chart of UALS Module

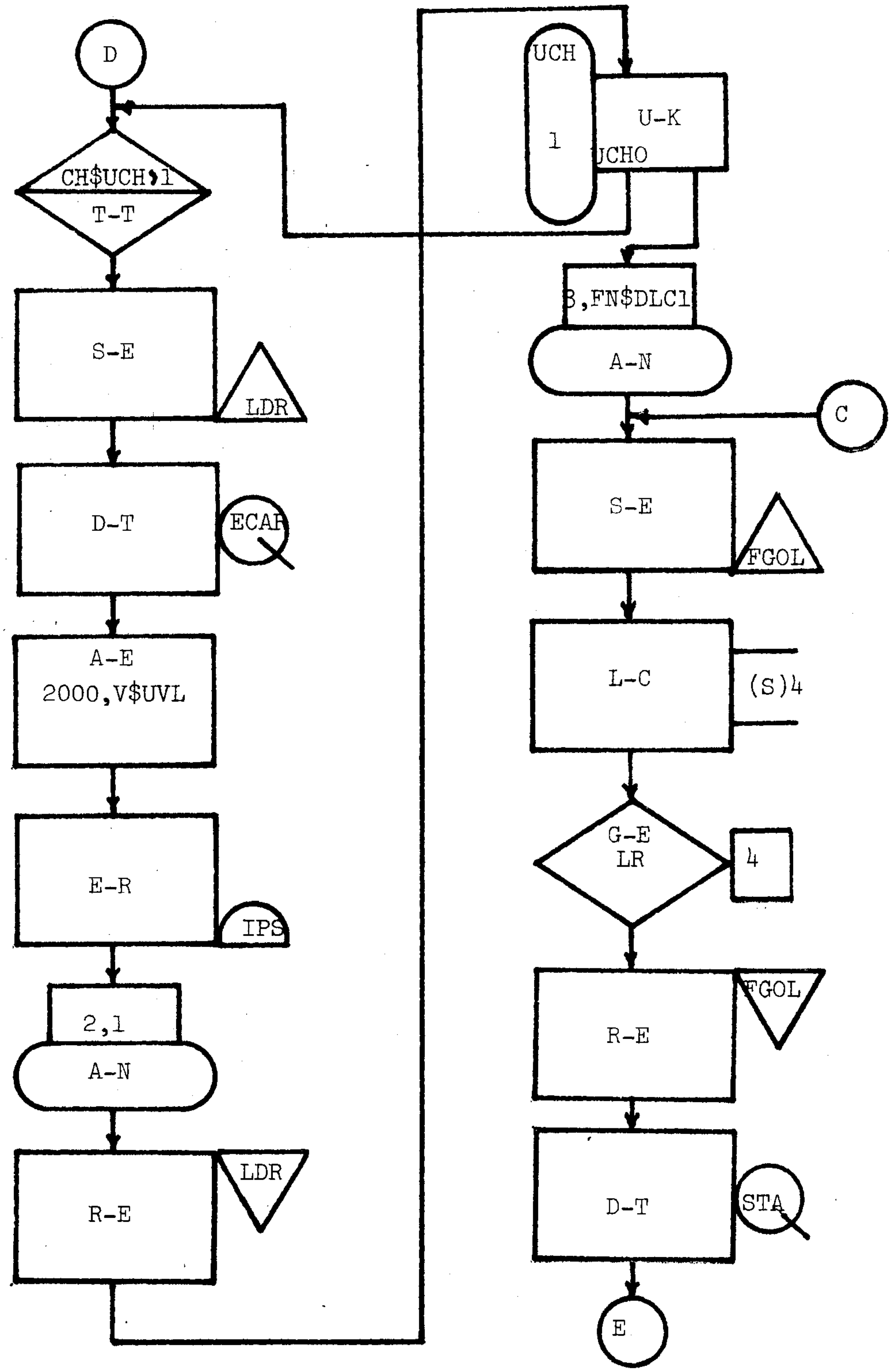

Figure 17. (Continued)

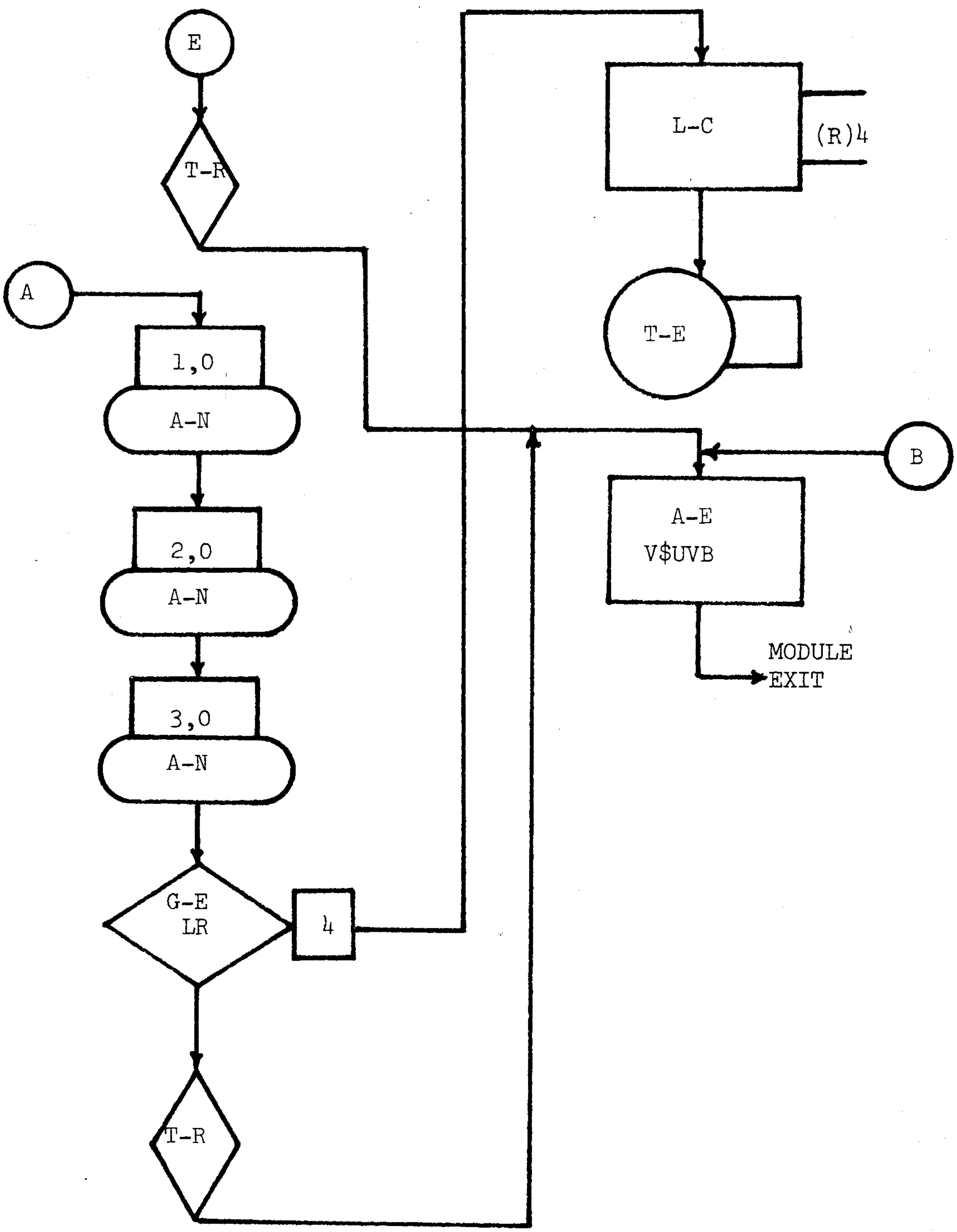

Figure 17. (Continued)

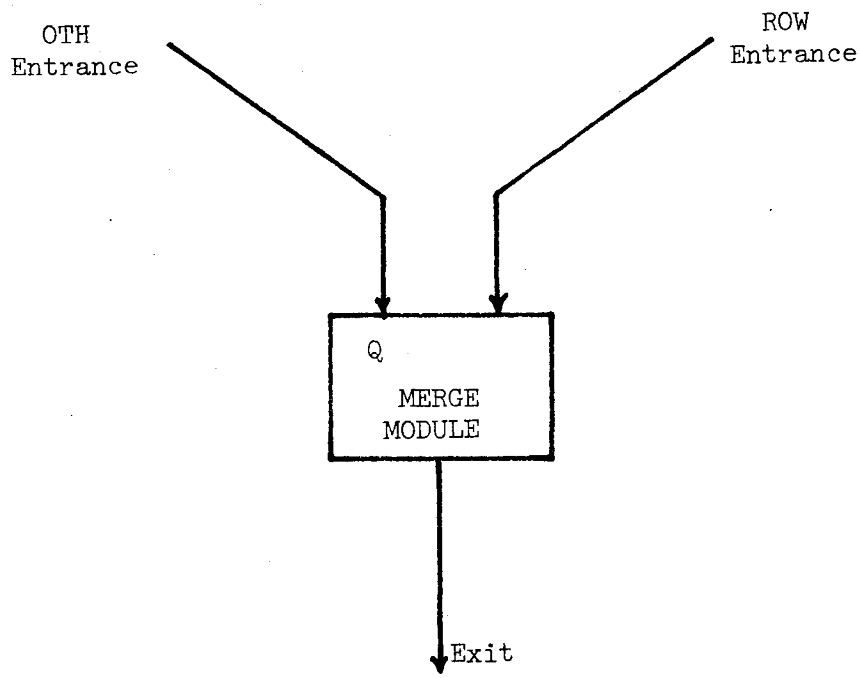

Figure 18. Merge Module

entrance have the right-of-way and can proceed to the exit without being delayed. Carts which enter the module at the OTH entrance may or may not be delayed. If delayed they join a queue shown symbolically as "Q" in Figure 18.

There are ten different logical situations which might occur at the MERGE module. The logic is designed to process each of these cases.

Case 1. (ROW = cart or hook and OTH = nothing) If a hook or a cart enters the module at ROW and nothing has entered the module at OTH, the hook or cart is transferred immediately to the module exit.

Case 2. (ROW = nothing and OTH = cart or hook) If a hook or a cart enters the module at OTH and nothing has entered the module at ROW, the hook or cart is transferred immediately to the module exit.

Case 3. (ROW = hook, OTH = hook, Q = 0) If a hook enters the module at ROW and at OTH, and there is nothing in the queue, then the OTH hook is destroyed and the ROW hook is transferred to the module exit.

Case 4. (ROW = hook, OTH = hook, Q = +) If a hook enters the module at ROW and at OTH, and there are carts in the queue, both hooks are destroyed and the first cart in the queue is transferred to the module exit.

Case 5. (ROW = hook, OTH = cart, Q = 0) If a hook enters the module at ROW and a cart enters at OTH, and there is nothing in the queue, the ROW hook is destroyed and the OTH cart is transferred to the module exit.

Case 6. (ROW = hook, OTH = cart, Q = +) If a hook enters the module at ROW and a cart enters at OTH, and there are carts waiting in the queue, the ROW hook is destroyed, the OTH cart joins the queue, and the first cart in the queue is transferred to the module exit.

Case 7. (ROW = cart, OTH = hook, Q = 0) If a cart enters the module at ROW, and a hook at OTH, and there is nothing in the queue, the OTH hook is destroyed and the ROW cart is transferred to the module exit.

Case 8. (ROW = cart, OTH = hook, Q = +) If a cart enters the module at ROW, and a hook at OTH, and there are carts waiting in the queue, the OTH hook is destroyed and the ROW cart is transferred to the module exit.

Case 9. (ROW = cart, OTH = cart, Q = 0) If a cart enters the module at ROW, and a cart enters at OTH, and there is nothing in the queue, the OTH cart joins the queue and the ROW cart is transferred to the module exit.

Case 10. (ROW = cart, OTH = cart, Q = +) If a cart enters the module at ROW, and a cart enters at OTH, and there are carts waiting in the queue, the OTH cart joins the queue, and the ROW cart is transferred to the module exit.

Detailed Description

This module has two entrances, and the program logic first deals with the entrance at which the carts have the right-of-way. Carts arriving at this entrance never have to wait or form a queue. This module contains several layers of logic to deal with any of the possibilities which might occur.

A cart which has been directed to the right-of-way entrance sets logic switch one and passes through a logic gate.

```
ROW  LOGIC S        1
     GATE  LS       2,EXIT
```

Before the conveyor system has been completely constructed, carts or hooks may arrive at only one entrance of the MERGE module (either the right-of-way entrance or the other entrance). The first entry at location ROW (the right-of-way entrance) sets logic switch one. This action indicates to the logic at the other entrance that there has been an entry at the ROW entrance. Similar logic appears at the other entrance (labelled OTH). The first entry at the other entrance sets logic switch two indicating to the logic at the ROW entrance that an entry has occurred at the OTH entrance. The entry at the ROW entrnace then passes through the logic gate. If there has been no entry at the OTH entrance, it takes the alternate exit of the gate block and proceeds to location EXIT at the end of this module.

If there has been an entry at the OTH entrance, the transaction proceeds to the next sequential block. The next layer of logic insures and maintains the timing and integrety of the towlines. First a transaction sets logic switch three and encounters a gate block operating in the conditional entry mode.

```
LOGIC S          3
GATE  LS         4
```

Logic similar to the above occurs at this point in the program at the OTH entrance. Transactions which encounter this logic must be timed with transactions encountering logic at the OTH entrance, but arrivals at both entrances may not occur at the same clock time. This logic causes the transaction which arrived at one of the entrances first to wait (at the gate block) for the transaction to arrive at the other entrance. Once both transactions have arrived, either one may begin to move first. First assume the transaction at the ROW entrance moves first. Later, the case in which the transaction at the OTH entrance moves first will be considered.

The next sequential block for the transaction at the ROW entrance determines if it is a cart or a hook.

```
TEST E          P1,1,HOOK
```

A hook takes the alternate exit and is transferred to location HOOK.

A cart proceeds and sets logic switch six.

```
LOGIC S         6
```

This indicates to the logic at the OTH entrance that a cart is present at the ROW entrance.

The cart then is stopped to allow the transaction at the OTH entrance to move if it has not already moved.

```
PRIORITY        0,BUFFER
```

The priority of the cart is changed back to one, and the cart is delayed again to allow the transaction at the OTH entrance to move first since it

```
PRIORITY        1
PRIORITY        0,BUFFER
```

must determine if it has to wait and join a queue or proceed.

Finally the cart's priority is changed back to one again and it proceeds on out the module exit.

```
PRIORITY        1
```

The transaction which leaves at the module exit resets the logic for the next pair of entries and is then transferred to the ADVANCE block at the end of the module.

```
EXIT LOGIC R    3
     LOGIC R    4
     LOGIC R    5
```

```
     LOGIC R          6
     TRANSFER         ,AOUT
```

The logic at the OTH entrance is somewhat parallel to the logic at the ROW entrance. The first transaction to arrive at the OTH entrance sets logic switch two indicating an arrival at this entrance, and then passes through a logic gate.

```
OTH  LOGIC S          2
     GATE  LS         1,EXIT
```

If a transaction has not arrived at the ROW entrance, the arrival at the OTH entrance takes the alternate exit through the GATE block and is transferred to location EXIT.

If there has been an arrival at the ROW entrance, the transaction at the OTH entrance continues to the next sequential block at which it sets logic switch four. It proceeds and encounters a gate block operating in the conditional entry mode.

```
     LOGIC S          4
     GATE  LS         3
```

The purpose of this layer of logic has been discussed previously. Now assume that the transaction at this entrance moves first since the case in which the transaction at the ROW entrance moves first has already been discussed.

The next block determines if the transaction is a hook or a cart.

```
     TEST  E          P1,1,TERM
```

If the transaction is a hook it is destroyed since the cart or hook at the ROW entrance will survive and continue out the module exit.

A cart continues and sets logic switch five which indicates a cart has arrived at the OTH entrance.

```
     LOGIC S            5
```

The cart is delayed to allow the transaction at the ROW entrance to move after which its priority is changed back to one.

```
     PRIORITY           0,BUFFER
     PRIORITY           1
```

The transaction at the ROW entrance moves until it encounters a sequence of blocks similar to those shown above. Now the cart at the OTH entrance continues to move.

The next sequential block determines if there is a queue of carts at the OTH entrance waiting for an empty hook to enter at the ROW entrance.

```
     GATE  NU           FAC,QUE
```

If the facility FAC is in use, a cart is waiting and the entering cart is transferred to the queue of carts at location QUE.

If <u>no</u> carts are waiting, the cart continues to the next block. The next block determines if there is a cart at both entrances or not. This is done by means of a boolean variable.

```
MBV  BVARIABLE          LS5*LS6
     TEST  E            BV$MBV,1,CRHK
```

If the value of the boolean variable is zero, there is a hook at the ROW entrance and the cart can continue out of the module by being transferred to location CRHK.

If the value of the boolean variable is equal to one, there is a cart at both entrances, and the cart at the OTH entrance must join the queue. It joins the queue and is linked onto a user chain to save CPU time.

```
QUE  QUEUE        MQU
     LINK         MCH,FIFO,MSZ
```

The first transaction in the waiting line can seize a facility which contains the logic necessary to capture a hook.

```
MSZ  SEIZE        FAC
```

It sets logic switch seven and then waits at a GATE block for a hook at the ROW entrance to reset logic switch seven to allow the cart to proceed.

```
     LOGIC S      7
     GATE  LR     7
```

After a hook at the ROW entrance opens the gate, the cart can depart the queue, release the facility, unlink the next cart from the user chain, and transfer to the module exit.

```
     DEPART       MQU
     RELEASE      FAC
     UNLINK       MCH,MSZ,1
     TRANSFER     ,EXIT
```

A cart at the OTH entrance captures a hook by setting logic switch seven before being transferred to the module exit.

```
CRHK LOGIC S      7
     TRANSFER     ,EXIT
```

A hook at the ROW entrance is transferred to location HOOK. Here it is first delayed twice for the same reason that a cart at the ROW entrance way delayed twice.

```
HOOK PRIORITY          0,BUFFER
     PRIORITY          1
     PRIORITY          0,BUFFER
     PRIORITY          1
```

Then the hook encounters a logic gate that determines if a cart is waiting at the OTH entrance or not.

```
     GATE LR           7,THOO
```

If a cart is not waiting the hook is transferred to the module exit.

```
     TRANSFER          ,EXIT
```

If a cart is waiting the hook opens the gate for the cart by resetting logic switch seven and is then destroyed.

```
THOO LOGIC R           7
     TERMINATE
```

At the end of the module is the ADVANCE block that delays the transaction for the time it takes it to reach the next module entrance.

```
AOUT ADVANCE           0
 MVB VARIABLE          (90*1000)/X3
     ADVANCE           V$MVB
```

The transaction then proceeds to the next sequential module.

A source listing of the MERGE module is given in Figure 19 and a flow chart of the module is shown in Figure 20.

Model Validation

Two concepts of ascertaining the model's representation of reality are used by this researcher. The first concept is

```
 ROW LOGIC S        1
     GATE LS        2,EXIT
     LOGIC S        3
     GATE LS        4
     TEST E         P1,1,HOOK
     LOGIC S        6
     PRIORITY       0,BUFFER
     PRIORITY       1
     PRIORITY       0,BUFFER
     PRIORITY       1
EXIT LOGIC R        3
     LOGIC R        4
     LOGIC R        5
     LOGIC R        6
     TRANSFER       ,AOUT
 OTH LOGIC S        2
     GATE LS        1,EXIT
     LOGIC S        4
     GATE LS        3
     TEST E         P1,1,TERM
     LOGIC S        5
     PRIORITY       0,BUFFER
     PRIORITY       1
     GATE NU        FAC,QUE
 MBV BVARIABLE      LS5*LS6
     TEST E         BV$MBV,1,CRHK
 QUE QUEUE          MQU
     LINK           MCH,FIFO,MSZ
 MSZ SEIZE          FAC
     LOGIC S        7
     GATE LR        7
     DEPART         MQU
     RELEASE        FAC
     UNLINK         MCH,MSZ,1
     TRANSFER       ,EXIT
CRHK LOGIC S        7
     TRANSFER       ,EXIT
HOOK PRIORITY       0,BUFFER
     PRIORITY       1
     PRIORITY       0,BUFFER
     PRIORITY       1
     GATE LR        7,THOO
     TRANSFER       ,EXIT
THOO LOGIC R        7
     TERMINATE
AOUT ADVANCE        0
 MVB VARIABLE       (90*1000)/X3
     ADVANCE        V$MVB
```

Figure 19. Source Listing of MERGE Module

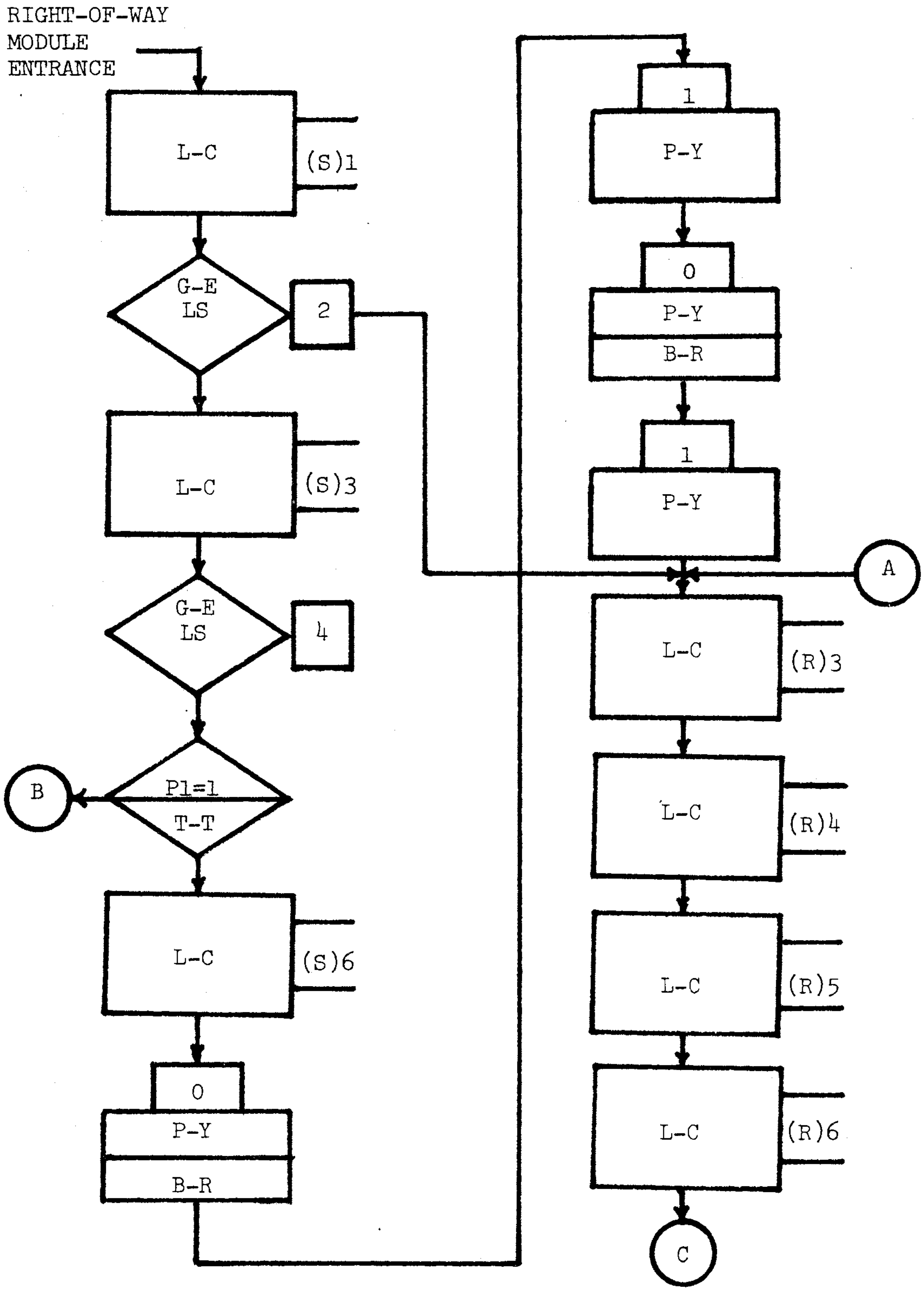

Figure 20. Flow Chart of MERGE Module

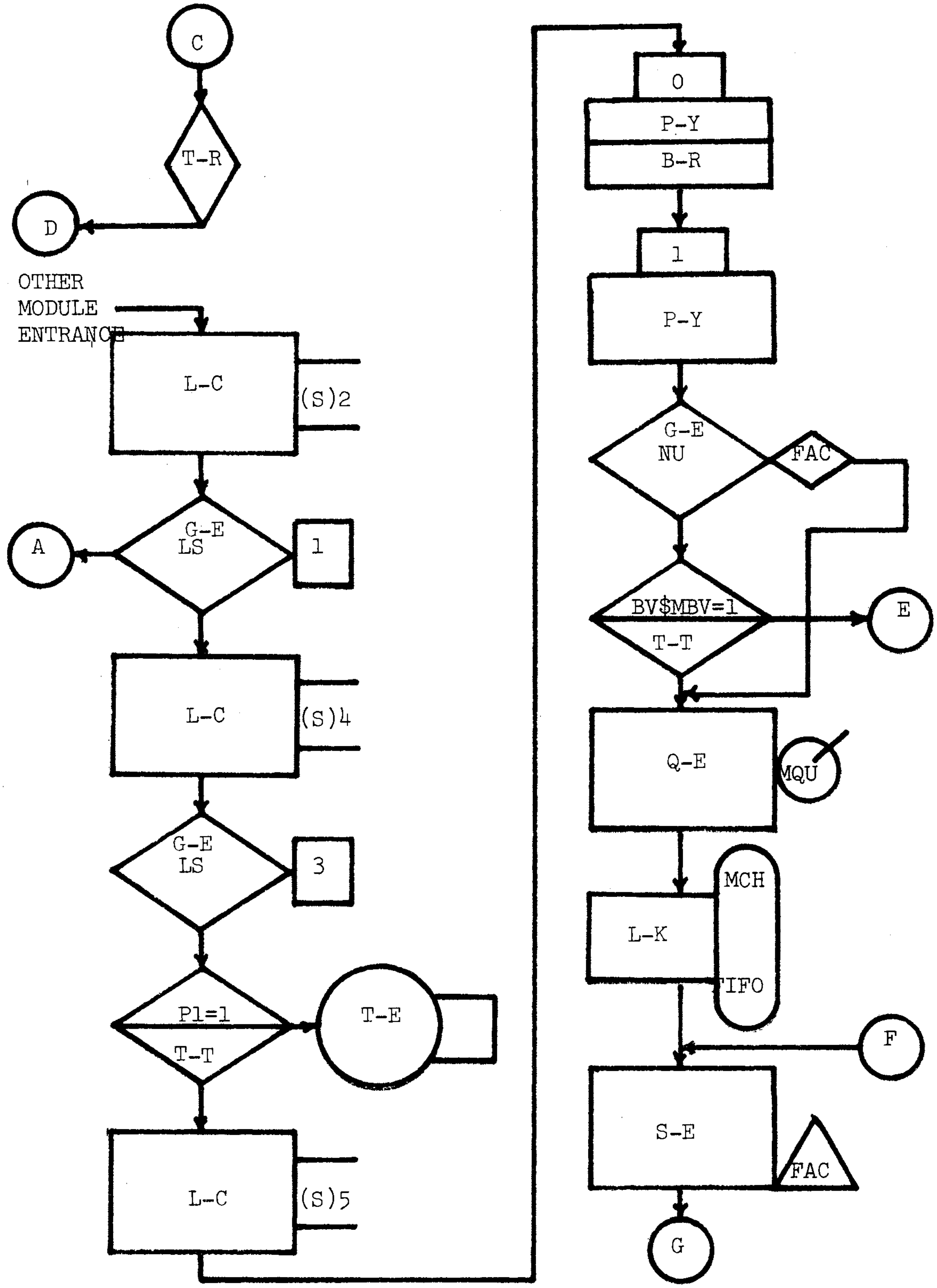

Figure 20. (Continued)

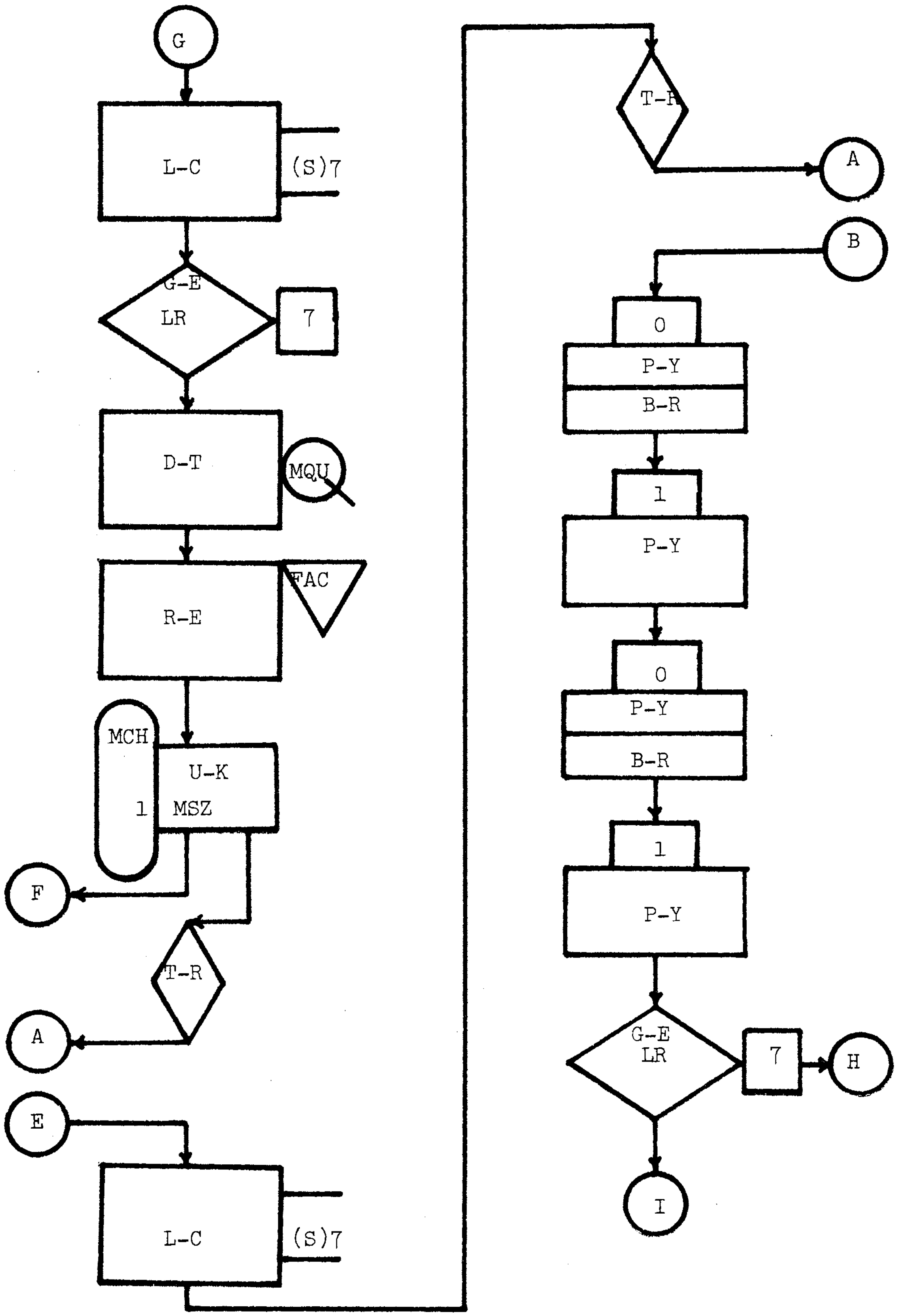

Figure 20. (Continued)

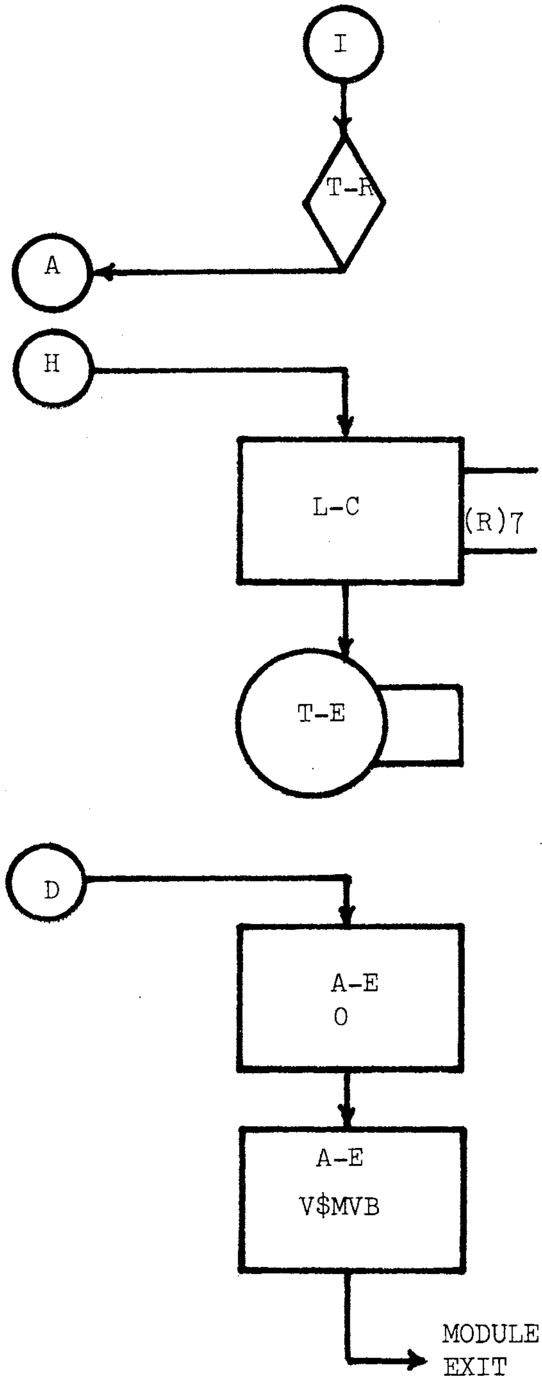

Figure 20. (Continued)

validation. The objective of validation is to establish that each module responds in a logical manner that is not unlike the actual system. This objective asks the question, "Is each module logically correct?" The second concept is verification. The objective of verification is to establish that the entire simulation model responds in a manner that does not misrepresent the response of the actual system under typical conditions.

The first phase of the model validation was accomplished during the model construction. In cases where logic was designed to deal with a number of different situations, the situations were exhaustively enumerated. This researcher then simulated each case of the module logic by hand to validate its construction.

The second phase of validation was accomplished by a series of trial computer simulations of each module to insure the correctness of the logic. All possible cases of module inputs were deterministically programmed and the output was analyzed to insure the module's correctness under all situations.

The third phase of validation consisted of building a small conveyor simulation model that consisted of one of each of the five modules. A series of trial computer simulations were performed with this model to test the modules. The future events chain, current events chain, users chains, and other GPSS output statistics were used to determine if each module's response was logically correct.

It was not the objective of this research to perform a model verification; however, further arguments for the model's validation are presented in Chapter VI and Chapter VII.

CHAPTER V

MODEL USER'S GUIDE

The model developed in the previous chapter is somewhat large and lengthy. For example, a conveyor system of average size and complexity may require more than 1000 GPSS/360 blocks, and on the IBM 360 system one hour of simulation time may require as much as one minute of CPU time. The purpose of this chapter is to assist the user in programming his conveyor system using the model developed through this research.

Primary Considerations

Conveyor systems of average complexity will probably require the 256 K version of GPSS/360 and the use of the REALLOCATE feature. Increasing the size of COMMON is the most important function of the REALLOCATE card in this model. The use of REALLOCATE is described in the GPSS/360 Operator's Manual (H20-0311 under OS/360 or H20-0327 under DOS/360).

If the normal distribution is used for load and unload times, then the standard normal distribution must be defined as a GPSS function. Other necessary functions include probability distributions of the possible destinations of empty carts from each UALS module, and probability distributions of the possible destinations of loaded carts from each UALS module. Many of these distributions may be the same and need not be duplicated. The functions should be labelled, not numbered.

Three savevalues used throughout the model must be specified. These may be specified by INITIAL cards. Savevalue number one (X1) must be initialized at the number of carts in the system. If the system does not use carts and the goods transferred on the conveyor are attached directly to the hooks, then X1 should be initialized at the number of hooks in the system. X2 must be initialized at the distance between hooks on the conveyor. X3 must be initialized at the speed of the conveyor. If X2 is defined in feet, then X3 must be defined in feet per minute.

One storage must be defined in the model. The storage label is IPS which stands for in process storage. It is defined by a STORAGE card as equal to the number of carts in the system. The purpose of this storage is to give the user an indication of the utilization of carts as an in process storage.

Any tables that the user wishes to use must also be defined. The user may want to tabulate the destinations of loaded carts that pass a particular point in the model. This may be a tabulation of carts that are recirculating in the system. The user must supply the TABLE card and insert TABULATE cards at proper places in the model.

The users considerations in the CAHG module and the PPLS module have been discussed in Chapter IV since these modules only occur once in the system. The other three modules occur from four to nineteen times throughout the model. To facilitate their programming and use, they have been encapsulated in GPSS/360 MACROS. The remainder of this chapter explains these MACROS.

Macro Modules

A source listing of the three modules programmed in macros is shown in Appendix A. A macro is a string of frequently used blocks defined by the user, which he may later call with only one card. The only advantage obtained by using macros is the elimination of the need to code and keypunch repetitive strings of blocks.

The definition of macros requires two control cards. A STARTMACRO card labelled with the name of the macro is placed in front of the actual macro blocks, and an ENDMACRO card is placed at the end of the macro. The actual macro definition cards are placed between these two control cards. These macro definition cards follow the normal GPSS block format except that some fields may be replaced by macro arguments. Macro arguments are represented by following a special character # with a letter (A-J) which represent arguments 1-10 respectively. A maximum of ten arguments per macro is allowed.

Macros are called by means of the MACRO card labelled with the name of the macro being called. The macro arguments to be substituted into the macro definition cards are listed in the MACRO card. As a simple example of a macro, the block sequence shown below defines a macro.

```
RONI STARTMACRO
  #C SEIZE             #A
     ADVANCE           #B
     RELEASE           #A
```

```
     ENDMACRO
```

This macro labelled RONI can be called with the MACRO card shown below.

```
RONI MACRO              1,400,FAC
```

The above card would produce the following block sequence in the compiled program.

```
FAC SEIZE               1
    ADVANCE             400
    RELEASE             1
```

Merge Module

The MERGE module is constructed of three GPSS/360 MACROS labelled MERG1, MERG2, and MERG3. These MACRO cards when used in order with the arguments defined will be compiled as a complete MERGE module. The remainder of this section is an explanation of the MACRO arguments.

```
MERG1 MACRO             #A,#B,#C,#D,#E,#F,#G,#H,#I,#J
```

#A - any unique three letter label

#B - any unique three letter label

#C - any unique three letter label

#D - any unique three letter label

#E - any unique three letter label

#F - any unique three letter label

#G - any unique three letter label

#H - any unique three letter label

#I - any unique three letter label

#J - any unique three letter label

MERG2 MACRO #A,#B,#C,#D,#E,#F,#G,#H,#I,#J

#A - same as #A of MERG1

#B - same as #B of MERG1

#C - any unique three letter label

#D - any unique three letter label

#E - BV$ (same as #D of MERG2)

#F - LS$ (same as #C of MERG1)*LS$

(same as #F of MERG1)

#G - any unique three letter label

#H - any unique three letter label

#I - any unique three letter label

#J - same as #I of MERG1

MERG3 MACRO #A,#B,#C

#A - any unique three letter label

#B - V$ (same as #A of MERG3)

#C - delay time in milliminutes to the next module entrance, i.e. (090*1000)/X3 or (Distance in feet * 1000)/X3

Split Module

The SPLIT module is also constructed of three GPSS/360 macros. They are labelled SPLT1, SPLT2, and SPLT3. The remainder of this section is an explanation of their MACRO arguments.

SPLT1 MACRO #A,#B,#C,#D,#E,#F,#G,#H,#I,#J

#A - any unique three letter label

#B - any unique three letter label

#C - any unique three letter label

#D - any unique three letter label

#E - any unique three letter label

#F - any unique three letter label

#G - any unique three letter label

#H - logical condition regarding P3 which is the argument of a boolean variable that equals one for a cart to proceed out the left exit, i.e.

P3'GE'9*P3'L'17 or P3'GE'17+P3'L'9

#I - BV$ (same as #G of SPLT1)

#J - the size that Q$LCR1 must reach for a cart with a destination to the left be diverted to the right, i.e. 999 or 36

SPLT2 MACRO #A,#B,#C,#D,#E

#A - any unique three letter label

#B - location label of the entrance to the next sequential module to the left

#C - same as #A of SPLT1

#D - V$ (same as #A of SPLT2)

#E - delay time to the entrance to the next sequential module to the left in milliminutes, i.e. (236*1000)/X3

SPLT3 MACRO #A,#B,#C,#D,#E

#A - any unique three letter label

#B - location label of the entrance to the next sequential module to the right

#C - same as #B of SPLT1

#D - V$ (same as #A of SPLT3)

#E - delay time to the entrance to the next sequential module to the left in milliminutes, i.e. (060*1000)/X3

Unload and Load Station Module

The UALS module is again constructed of three GPSS/360 macros. They are labelled ULST1, ULST2, and ULST3. The remainder of this section is an explanation of these MACRO arguments.

ULST1 MACRO #A,#B,#C,#D,#E,#F,#G,#H,#I,#J

#A - any unique three letter label

#B - any unique three letter label

#C - any unique three letter label

#D - any unique three letter label

#E - Q$ (same as #D of ULST1)

#F - V$ (same as #D of ULST1)

#G - destination number of this module, i.e. 1,2,3,etc.

#H - mean unload time in milliminutes, i.e. 4 minutes = 4000 milliminutes

#I - the maximum number of carts that can be in the station queue, i.e. 15 or 35

#J - variable argument which is the spread modifier of the mean unload time in milliminutes, i.e. FN$NORM*800

ULST2 MACRO #A,#B,#C,#D,#E,#F,#G,#H,#I

#A - same as #C of ULST1

#B - any unique three letter label

#C - CH$ (same as #A of ULST2)

#D - V$ (same as #B of ULST2)

#E - FN$ (the label of the function which defines the probability distribution of the possible destinations of empty carts which leave this module), i.e. FN$DEC1

#F - any unique three letter label

#G - mean load time in milliminutes, i.e. 2 minutes = 2000 milliminutes

#H - the maximum number of empty carts to be retained at the module minus one, i.e. 1,2,etc.

#I - variable argument which is the spread modifier of the mean load time in milliminutes, i.e. FN$NORM*400

ULST3 MACRO #A,#B,#C,#D,#E,#F,#G,#H,#I

#A - same as #B of ULST2

#B - any unique three letter label

#C - same as #B of ULST1

#D - same as #A of ULST1

#E - any unique three letter label

#F - V$ (same as #E of ULST3)

#G - same as #D of ULST1

#H - FN$ (the label of the function which defines the probability distribution of the possible destinations of loaded carts which leave this module), i.e. FN$DLC1

#I - delay time to the entrance to the next sequential module in milliminutes, i.e. (601*1000)/X3

Model Order

The general structure of the model should be similar to that of the conveyor system. Before the actual system modules, the deck should include:

1. REALLOCATE cards
2. SIMULATE card
3. Three general purpose MACRO modules
4. FUNCTION definition cards including the standard normal distribution if it is used.
5. TABLE definition cards if they are used.
6. Three INITIAL cards for X1,X2, and X3
7. STORAGE definition card labelled IPS

Since the model forms a closed loop, any point in the model may be used as a starting point. If a transaction which leaves a module should not enter the next sequential module, an unconditional transfer should be inserted into the deck for proper routing. The CAHG module and the PPLS module must be constructed by the user, but the three general purpose modules do not need to be constructed. To use these three modules, the user need only insert the three MACRO definition cards and supply their arguments.

The last part of the model deck should be a run timer to stop the simulation. The user can define his own run timer. The following run timer lets the model run for two hours to reach steady state. A RESET card is used, and the model is simulated for twenty hours.

```
GENERATE     120000
TERMINATE    1
START        1
RESET
START        10
```

CHAPTER VI

FIRST MODEL SIMULATION

After the conveyor system modules had been developed and validated, they were combined into a model of the first large manufacturing company's conveyor system which was described in Chapter III. This chapter includes a discussion of the simulation of that model and its output statistics.

Simulation Model

Figure 1 shown in Chapter III is a graphical representation of the manufacturing company's warehouse distribution conveyor system. This was a useful starting point in building the simulation model by visualizing the overall system. A blueprint of the floor plan of the towline was obtained. Measurements of distances along the towline were taken from the blueprint and transcribed on the towline floor plan shown in Figure 21. The blueprint floor plan was also used to aid in the identification of the position of the modules which were used to construct the simulation model of the system. To aid in building the model correctly, Figure 21 was transformed into Figure 22 which is a modular representation of the conveyor system. Figure 22 shows the type of module that was used at each interface, and the destination identification number is given for each of the UALS

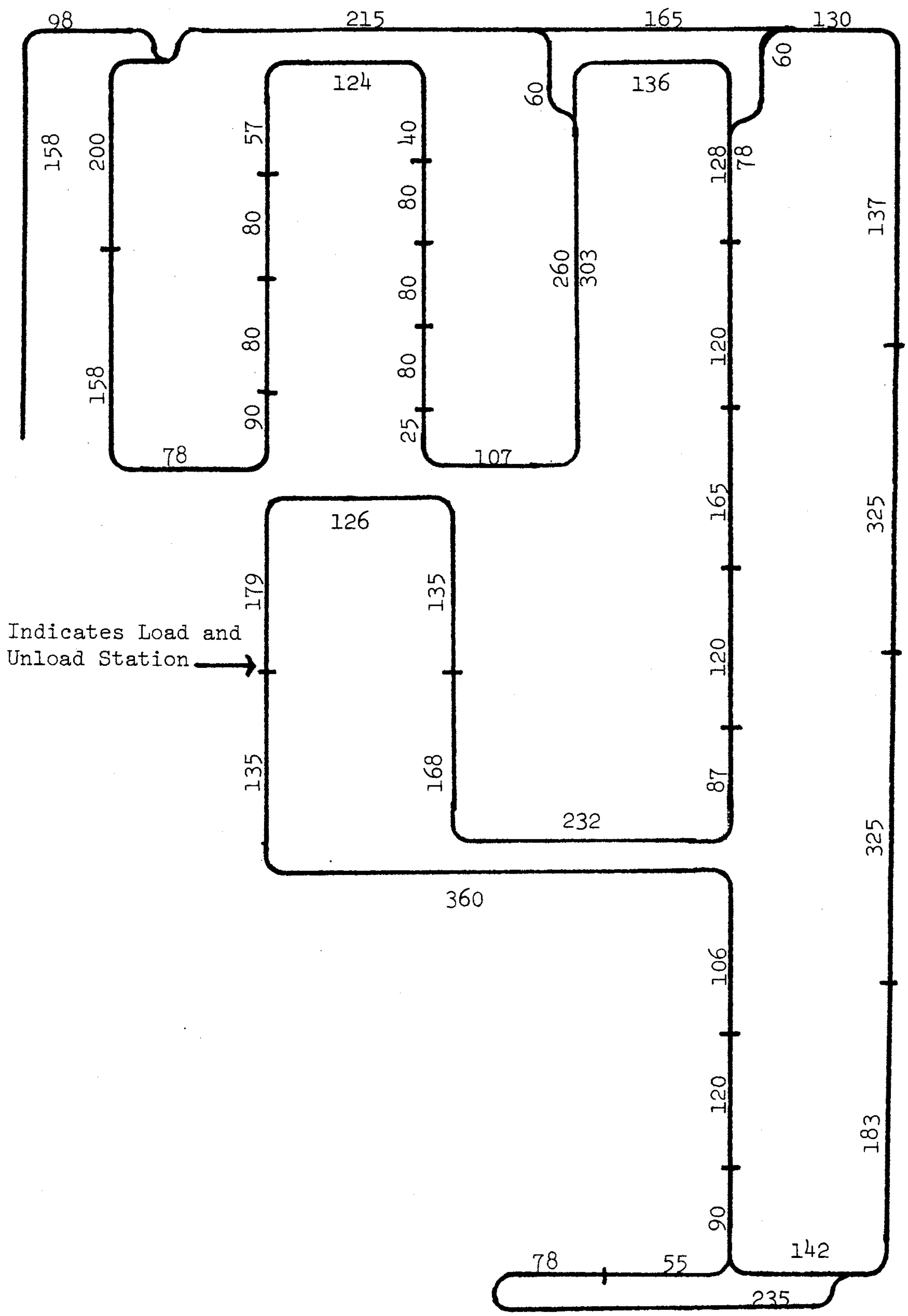

Figure 21. Conveyor System Floor Plan

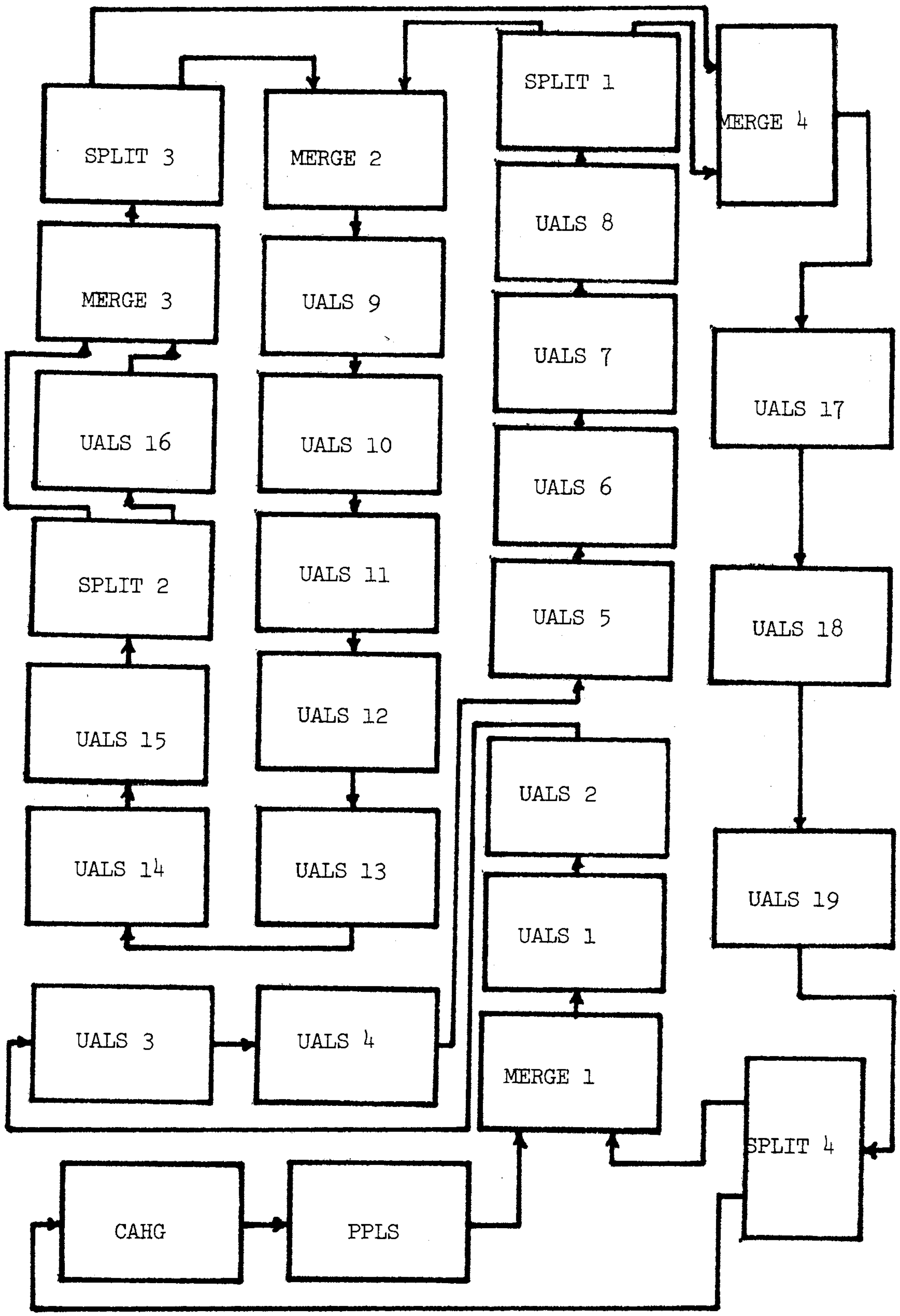

Figure 22. Modular Floor Plan of Conveyor

modules and the PPLS module. A complete source listing of this conveyor system is given in Appendix A.

The functions used for possible destinations of empty and loaded carts were estimated with the aid of the manufacturing company's Industrial Engineering Department. These functions are difficult to validate with hard data and often must be approximated. Two TABLE definition cards were used to tabulate the number of loaded carts that pass two points in the model. X1, the number of carts in the system, was initialized at 380, X2, the hook spacing, was initialized at 21 feet, and X3, the conveyor speed, was initialized at 70 feet per minute.

The module parameters or arguments such as maximum station queue etc. were obtained from the conveyor specifications on the blueprint. Other parameters such as the mean and standard deviation of the load and unload times etc. were estimated with the aid of the company's Industrial Engineering Department. Unconditional TRANSFER cards were added to the model where it was necessary to direct the transactions to their proper destinations. The series of blocks shown below was added to the model between the right exit of the third SPLIT module and the non right-of-way entrance to the second MERGE module and between the right exit of the fourth SPLIT module and the right-of-way entrance to the first MERGE module.

```
TAA  TEST  E           P2,1,TRA
     TABULATE          REC1
TRA  TRANSFER          ,MBO
```

The purpose of these blocks was to tabulate the number of loaded carts by destination which passed that point in the module. The table labelled REC1 tabulated the carts at the first location described above, and table labelled REC2 tabulated the carts at the second location described above.

Finally the conveyor system was simulated for twenty hours after having reached steady state. A snap interval of four hours was used to give output statistics after each four hours of simulation.

Output Statistics

The standard GPSS/360 output statistics produced at the end of the simulation is given in Appendix A. The user chain statistics are of little value to the analysis of the simulation because the user chains were added only to save CPU time. The data from them can be more easily and completely obtained from the queue statistics. Many of the facilities in the model were used for logical purposes only (allowing a cart to capture a hook). The statistics from these facilities is of little value. Each UALS module consists of a loading facility and an unloading facility. The percent utilization of these facilities and the PPLS module is summarized in Table I.

The Table I statistics directly reflect the user defined functions of possible destinations of loaded and empty carts. If these functions were changed, the changes would become apparent in the load and unload facility utilization statistics. The facility statistics also contain the average time per transaction. This time corresponds directly to the mean loading or unloading time and is of no value except for comparing it to the user defined mean. The total number of entries gives the user an idea of how many carts were processed by each facility. This statistic can be obtained from the queue or facility statistics. It will be discussed later in this chapter.

TABLE I

FACILITY UTILIZATION STATISTICS I

UALS Module (Destination)	Unload Facility Utilization (%)	Load Facility Utilization (%)
1	35.9	4.4
2	38.2	6.1
3	34.6	5.4
4	28.8	8.8
5	41.5	6.1
6	33.9	7.1
7	39.1	8.6
8	34.5	10.2
9	17.1	4.3
10	16.7	4.6
11	14.3	4.0
12	19.7	5.0
13	19.5	5.9
14	18.8	5.4
15	21.3	5.0
16	31.4	63.5
17	6.4	7.1
18	7.6	7.2
19	4.5	9.8
PPLS	NA	100.0

The value of recirculating conveyors as an in-process storage may be either under estimated or over estimated. Table II summarizes the storage statistics for this simulation.

TABLE II

IN-PROCESS STORAGE STATISTICS I

Total Capacity (no.)	Average Contents (no.)	Average Utilization (%)	Total Entries (no.)	Average Time/ Transaction (min.)	Maximum Contents (no.)
380	64	16.8	1722	44.6	131

The capacity of the storage was set by the user at the total number of carts in the system. In this simulation for this system, the utilization of this storage was low (16.8%). The average time/ transaction tells the user that it took an average of 44.6 minutes for a loaded cart to reach its destination and be unloaded. This time might be useful for planning purposes such as planning delays for customers in placing and receiving orders. The average time a cart is delayed at a UALS module might also be used in this estimate. This statistic and other queue statistics are summarized in Table III.

TABLE III

QUEUE STATISTICS

UALS Module (Destination)	Average Contents (no.)	Total Entries (no.)	Average Time/ Transaction (min.)
1	5.8	139	50.5
2	5.5	155	42.2
3	5.2	143	43.6
4	6.4	143	53.5
5	6.4	165	46.3
6	5.2	149	41.7
7	6.1	174	42.2
8	5.0	169	35.8
9	2.3	64	42.2
10	2.3	66	41.3
11	2.2	56	47.4
12	2.3	74	37.3
13	2.3	78	35.3
14	2.3	74	37.0
15	2.3	77	36.2
16	8.1	761	12.7
17	4.9	74	78.9
18	4.9	84	69.9
19	3.9	77	61.5
PPLS	40.4	635	76.4

The average station queue contents gives the user an indication of the average number of carts present at the module at any time. The total entries tells how many carts passed through each UALS module. The average time per transaction gives the average total time a cart was delayed at a UALS module for unloading and or loading plus waiting time. Queue statistics are also given for the waiting lines that can build up at the MERGE modules. These statistics indicate that the two most critical bottlenecks in the simulation model occur at the point where carts from the PPLS module attempt to capture a hook on the main loop and where the two loops merge just prior to the rail docks. The sizes of these queues may be influenced by the accuracy of the user defined functions which are probability distributions of possible destinations of empty and loaded carts. The sizes of these queues may also be influenced by the total number of carts that are loaded and unloaded at the UALS modules. The actual observed sizes of these queues and the simulated sizes of these queues can be used to test the system sensitivity to external or internal changes such as increasing the number of carts or decreasing the cart delay time at the UALS modules.

Finally the two user defined tables REC1 and REC2 are given in Table IV. These tables were used to count the number of carts that pass a point in the model. Table REC1 counts the number of loaded carts from UALS modules 8-15 which are recirculating around the loop or have a load to be unloaded at the truck docks. Table REC2 counts the loaded carts which pass another point in the model. The user may put these types of tables any place in the model where he desires to obtain statistics. The table may be configured to count empty carts, loaded carts or both. They may also be used for model verification purposes.

TABLE IV

TABLE STATISTICS I

UALS Module (Destination)	Observed Frequency	
	Table REC1 (no.)	Table REC2 (no.)
0	0	0
1	0	39
2	0	45
3	0	38
4	0	40
5	0	39
6	0	40
7	0	41
8	0	40
9	15	5
10	16	7
11	16	4
12	24	3
13	28	2
14	28	5
15	31	6
16	0	0
17	0	0
18	0	0
19	0	0

CHAPTER VII

SECOND MODEL SIMULATION

The second manufacturer's recirculating conveyor system was chosen for study because it is a different type of recirculating conveyor than the one modeled previously. This chapter includes a brief system description, a discussion of the simulation model, and the simulation output statistics.

System Description

This conveyor system is an overhead type conveyor which transports components from a subassembly load station to two final assembly unload stations. The products are placed directly onto discretely spaced hooks which are an integral part of the overhead conveyor. The conveyor system is somewhat less complex than the one previously studied; however, it is different in that carts are not used. The products are placed directly on the hooks.

A floor plan diagram of the conveyor system is shown in Figure 23. Components which are placed on the conveyor at the load station first pass through an inspection area. Here the components are given a 100% inspection as they move on the conveyor. This portion of the system does not affect the operational aspects of the conveyor itself and is represented in the model as a delay. Approximately 70% of the components are the type which are removed from the conveyor at the first unload station encountered and the remainder are destined for the second unload station.

There are 1200 hooks on the 600 foot conveyor which is operated at a speed of 10 feet per minute. The distance between hooks is 6 inches and it takes a hook one hour to complete the circuit. There are 360 feet of conveyor between the load station and the first unload station, 120 feet between the first and second unload stations, and 120 feet between the second unload station and the load station.

Simulation Model

The conveyor system may be completely constructed using four simulation modules developed earlier in this research. The CAHG module is necessary without modification to build the conveyor. The PPLS module without modification was used to represent the load station. Two UALS modules with one minor modification was used to represent the two unload stations. Since the two UALS modules were being used for unloading purposes only an unconditional TRANSFER block was added to the module to branch the transactions around the load portion of the module.

The function used for the possible destination of the loaded hooks was estimated by the company's Industrial Engineering Department. One table was defined in this simulation model to tabulate the number of components which recirculated on the conveyor. X1, the number of carts in the system, was initialized at 1200 which is the number of hooks in the system. To the model, this means there is a cart on every available hook. X3, the

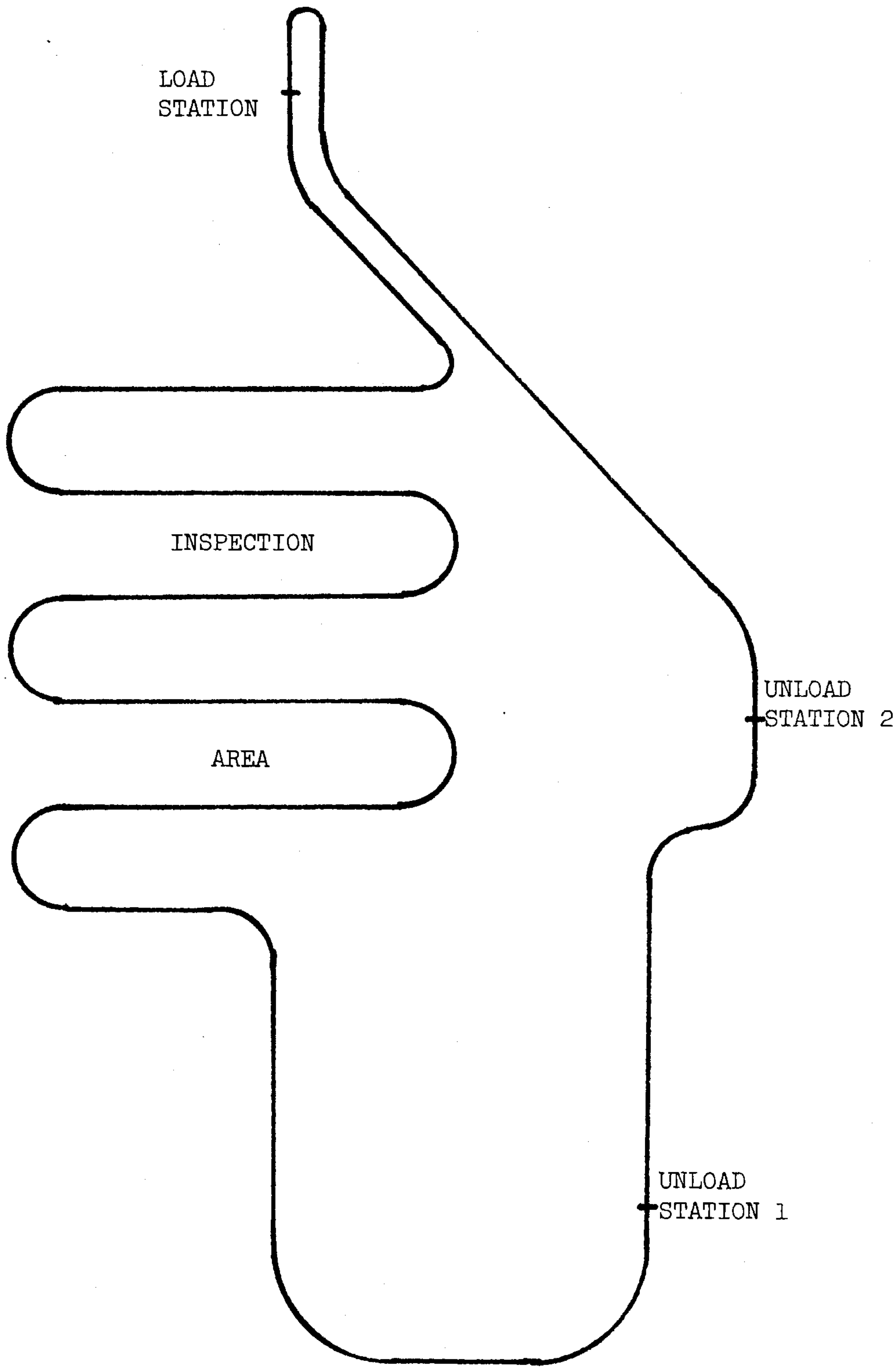

Figure 23. Conveyor Floor Plan

conveyor speed, was initialized at 10 feet per minute. The distance between hooks could not be directly incorporated into a savevalue since it was a fractional value. This distance is used only in variable number one and was placed in that variable directly.

The module parameters and the arguments of the two UALS modules were obtained from observation of the system in operation and from the company's supervisory personnel. The data for the load and unload times was estimated with the aid of the company's Industrial Engineering Department. Following the last UALS module, the sequence of blocks shown below was added to the model to tabulate the number of components that recirculated on the conveyor and then transfer the hooks to the entrance to the CAHG module.

```
    TEST E          P2,1,TRA
    TABULATE        REC1
TRA TRANSFER        ,NTR
```

Finally the model was simulated for eight hours of operation after having reached steady state. Appendix B shows a source listing of the conveyor system model and lists the standard GPSS/360 output statistics produced at the end of the simulation.

Output Statistics

Since the conveyor system is a simple one, only three different statistics are of any value. The facility statistics give the average utilization of the load and unload stations, the storage statistics give the utilization of the conveyor as an in process storage, and the table statistics can be used to calculate the percentage of the components that recirculate. The queue statistics and user chain statistics are of no value since no queues can form in this one loop conveyor system.

Table V gives the average utilization of the load station and two unload station modules. This statistic can be influenced by the maximum station queue policy that is used in the UALS modules. After observing this system in operation, it was determined that the person unloading components from the conveyor had enough time to select and unload only two items from the conveyor at once. The maximum station queue was therefore set at two.

TABLE V

FACILITY UTILIZATION STATISTICS II

Module	Average Utilization (%)
Load Station	73.3
First Unload	77.8
Second Unload	75.0

The capacity of the conveyor as an in-process storage was set by the user at the total number of hooks in the system. In this simulation the average utilization was somewhat higher (68.5%) than in the previous model (16.8%). This is probably due to the fact that the overhead conveyor is a different type of conveyor. It is also being used for a different purpose and it is loaded and unloaded in a different manner. Table VI summarizes the storage statistics for this simulation.

TABLE VI

IN-PROCESS STORAGE STATISTICS II

Total Capacity (no.)	Average Contents (no.)	Average Utilization (%)	Total Entries (no.)	Average Time/ Transaction (min.)	Maximum Contents (no.)
1200	822	68.5	9629	41.0	846

Table VII gives the results of the recirculation statistics tabulated in the model. These results were tabulated in table REC1. More of the items destined for unload station number two recirculated than those destined for unload station number one. Although less components are assigned to be unloaded at UALS module number two (30%), the mean unload time is significantly larger (.140 minutes compared to .060 minutes for UALS number one). The simulation time of eight hours means that 9600 (8 X 1200) hooks passed a given point in the system after the conveyor is constructed. There were 744 entries into table REC1. This means that 7.75% of the components recirculated on the conveyor or that the probability of recirculation of any one component is .0775.

TABLE VII

TABLE STATISTICS II

UALS Module (destination)	Observed Frequency (no.)
1	193
2	551

CHAPTER VIII

CONCLUSIONS AND RECOMMENDATIONS

This chapter includes a summary of how the research objectives set forth in Chapter I were accomplished and suggests areas for future research.

Conclusions

The first research objective was to examine the functional components of a particular complex integrated conveyor system, with the objective of identifying the functional components and parameters of the system. After confining the research to constant speed discretely spaced recirculating complex conveyor systems, a survey of the literature and an on site observation assisted this researcher in identifying the functional components and parameters of this particular type of conveyor system. These components and parameters were later incorporated into the basic structure of the simulation model. Examples of these components and parameters include: (1) conveyor speed, (2) hook spacing, (3) number of carts, (4) finite distance between decision points, etc.

The second research objective was to identify and describe the components and parameters of the types of interfaces that do occur between the functional components of the complex recirculating conveyor system. Chapter III of this dissertation described four major interfaces or decision points that occur in the particular system selected for study. A fifth interface was later identified by this researcher to complete the analytical description of the conveyor system.

The third objective was to develop and encode a computer simulation model using a modular format to represent the functioning of the components identified in the first two research objectives. The development and encoding of the five simulation modules of the second research objective is described in Chapter IV. The first section of Chapter V describes to the user how the components and parameters of the first research objective were incorporated into the simulation model.

The fourth research objective was to demonstrate that the "plug-in" simulation modules provide a feasible approach for building a general purpose simulation model. The manner in which the modules were developed in Chapter IV was centered around a general purpose technique. The validation of the modules in Chapter IV required the construction and simulation of a small conveyor system that consisted of one of each of the five modules. Without changes in the modules, they were in Chapter VI put together to form a large conveyor system. This flexibility of the modular approach demonstrates the feasibility of a general purpose simulation model for constant speed discretely spaced recirculating conveyor system. The general purpose approach is further demonstrated in Chapter V by providing the user with a general user guide in programming a simulation model using these five modules. Chapter VII also demonstrated the feasibility of the approach by using the general purpose modules to simulate another unrelated conveyor system.

Finally the fifth research objective was to use the "plug-in" simulation components to simulate the recirculating conveyor system to validate the model construction and to further validate the simulation modules and demonstrate the feasibility of the approach by using the modules to simulate another unrelated recirculating conveyor system. Chapter VI and Chapter VII of this dissertation describe the simulation models and their results.

Recommendations

There are three major areas for future research in the area of constant speed discretely spaced recirculating conveyor systems.

Since this dissertation proved its feasibility, the all-encompassing general purpose simulation model should be developed. This may require the development of additional modules to provide for all the cases that might be encountered. It also might require modification of one or more of the five modules that have been developed in this dissertation to provide compatibility with future modules or to provide flexibility in simulating a variety of conveyor systems.

A second area of research should be a rigid mathematical verification of a particular conveyor system simulation model. This may require the researcher to find a conveyor system about which a great deal of hard performance data already exists. If this is not possible, the researcher should be required to obtain a significant amount of hard performance data concerning a particular conveyor system. This verification should serve as a further test of the general purpose approach.

The third area of research should be to use the general purpose model, once developed, to devise a set of mathematical "prediction equations" for the general purpose model. The equations could be used to predict the outcome of simulation models of conveyor systems without having to run the simulation on the computer. The equations would emperically describe the functional components and complex interactions of the simulation model.

Just as Terrell and Bussey's work provided a spring board for this dissertation, this researcher hopes that this thesis provides a catalyst for yet further work in this field.

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APPENDIX A

SOURCE LISTING AND COMPUTER OUTPUT FOR FIRST MODEL SIMULATION

```
                              ***    G P S S / 3 6 0 / O S  V E R S I O N   1   * * *
                                   *** IBM PROGRAM NUMBER 360A-CS-17X (V1M4) ***
REALLOCATE XAC,1200,BLO,1200,FAC,100,STO,1,QUE,100,LOG,100                                    1
REALLOCATE TAB,5,FUN,12,VAR,75,FSV,5,HSV,5,CHA,30,GRP,1,BVR,10                                2
REALLOCATE FMS,1,HMS,1,COM,75000                                                              3
```

```
BLOCK                                                                    CARD
NUMBER  *LOC   OPERATION  A,B,C,D,E,F,G          COMMENTS              NUMBER
               SIMULATE                                                     4
        MERG1  STARTMACRO                                                   5
        #J     LOGIC S    #J                                                6
               GATE  LS   #G,#A                                             7
               LOGIC S    #D                                                8
               GATE  LS   #E                                                9
               TEST  E    P1,1,#B                                          10
               LOGIC S    #C                                               11
               PRIORITY   0,BUFFER                                         12
               PRIORITY   1                                                13
               PRIORITY   0,BUFFER                                         14
               PRIORITY   1                                                15
        #A     LOGIC R    #F                                               16
               LOGIC R    #C                                               17
               LOGIC R    #D                                               18
               LOGIC R    #E                                               19
               TRANSFER   ,#I                                              20
        #H     LOGIC S    #G                                               21
               GATE  LS   #J,#A                                            22
               LOGIC S    #E                                               23
               GATE  LS   #D                                               24
               TEST  E    P1,1,TERM                                        25
               LOGIC S    #F                                               26
               PRIORITY   0,BUFFER                                         27
               PRIORITY   1                                                28
               ENDMACRO                                                    29
        MERG2  STARTMACRO                                                  30
               GATE  NU   #G,#G                                            31
        #D     BVARIABLE  #F                                               32
               TEST  E    #E,1,#H                                          33
        #G     QUEUE      #G                                               34
               LINK       #C,FIFO,#C                                       35
        #C     SEIZE      #G                                               36
               LOGIC S    #C                                               37
               GATE  LR   #C                                               38
               DEPART     #G                                               39
               RELEASE    #G                                               40
               UNLINK     #C,#C,1                                          41
               TRANSFER   ,#A                                              42
        #H     LOGIC S    #C                                               43
               TRANSFER   ,#A                                              44
        #B     PRIORITY   0,BUFFER                                         45
               PRIORITY   1                                                46
               PRIORITY   0,BUFFER                                         47
               PRIORITY   1                                                48
               GATE  LR   #C,#I                                            49
               TRANSFER   ,#A                                              50
        #I     LOGIC R    #C                                               51
               TERMINATE                                                   52
        #J     ADVANCE    0                                                53
               ENDMACRO                                                    54
        MERG3  STARTMACRO                                                  55
        #A     VARIABLE   #C                                               56
               ADVANCE    #B                                               57
               ENDMACRO                                                    58
```

```
SPLT1 STARTMACRO
      TEST   E     P1,1,#C
#G    BVARIABLE    #H
      TEST   E     #I,1,#E
      TEST   LE    Q$LCR1,#J,#E
      SPLIT        1,#D
      TRANSFER     ,#A
#D    ASSIGN       1,0
      ASSIGN       2,0
      ASSIGN       3,0
      TRANSFER     ,#B
#E    SPLIT        1,#F
      TRANSFER     ,#B
#F    ASSIGN       1,0
      ASSIGN       2,0
      ASSIGN       3,0
      TRANSFER     ,#A
#C    SPLIT        1,#A
      TRANSFER     ,#B
      ENDMACRO
SPLT2 STARTMACRO
#A    VARIABLE     #E
#C    ADVANCE      #D
      TRANSFER     ,#B
      ENDMACRO
SPLT3 STARTMACRO
#A    VARIABLE     #E
#C    ADVANCE      #D
      TRANSFER     ,#B
      ENDMACRO
ULST1 STARTMACRO
#D    TEST   E     P1,1,#A
      TEST   E     P3,#G,#B
      TEST   L     #E,#I,#B
      QUEUE        #D
      SPLIT        1,#A
      TEST   E     P2,1,#C
      SEIZE        #A
#D    VARIABLE     #J
      ADVANCE      #H,#F
      LEAVE        IPS
      ASSIGN       2,0
      RELEASE      #A
      ENDMACRO
ULST2 STARTMACRO
      TEST   GE    #C,#H,#A
      ASSIGN       3,#E
      TRANSFER     ,#B
#A    QUEUE        #A
      LINK         #A,FIFO,#F
#F    TEST   G     #C,#H
      SEIZE        #B
      DEPART       #A
#B    VARIABLE     #I
      ADVANCE      #G,#D
      ENTER        IPS
      ASSIGN       2,1
```

```
        RELEASE     #B
        UNLINK      #A,#F,1
        ENDMACRO
ULST3   STARTMACRO
        ASSIGN      3,#H
#A      SEIZE       #C
        LOGIC S     #B
        GATE  LR    #B
        RELEASE     #C
        DEPART      #G
        TRANSFER    ,#C
#D      ASSIGN      1,0
        ASSIGN      2,0
        ASSIGN      3,0
        GATE  LR    #B,#E
        TRANSFER    ,#C
#E      LOGIC R     #B
        TERMINATE
#E      VARIABLE    #I
#C      ADVANCE     #F
        ENDMACRO
NORM    FUNCTION    RN1,C31
0,-5.00/.00023,-3.50/.00058,-3.25/.00135,-3.00/.00300,-2.75/
.00620,-2.50/.01220,-2.25/.02280,-2.00/.04010,-1.75/.06680,-1.50/
.10570,-1.25/.15870,-1.00/.22660,-0.75/.30850,-0.50/.40130,-0.25/
.50000,0.00/.59870,0.25/.69150,0.50/.77340,0.75/.84130,1.00/
.89440,1.25/.93320,1.50/.95990,1.75/.97730,2.00/.98780,2.25/
.99380,2.50/.99700,2.75/.99865,3.00/.99942,3.25/.99977,3.50/1.0,5.00
DLCP    FUNCTION    RN1,D15
.11,1/.22,2/.33,3/.44,4/.55,5/.66,6/.77,7/.88,8/.90,9/.92,10/.94,11/
.96,12/.98,13/.99,14/1.0,15
DECP    FUNCTION    RN1,D19
.04,1/.08,2/.13,3/.17,4/.22,5/.26,6/.3,7/.35,8/.38,9/.42,10/.45,11/
.49,12/.52,13/.56,14/.60,15/.75,16/.83,17/.91,18/1.0,19
DLC1    FUNCTION    RN1,D11
.01,9/.02,10/.03,11/.04,12/.06,13/.08,14/.1,15/.8,16/.87,17/.94,18/
1.0,19
DEC1    FUNCTION    RN1,D10
.40,0/.43,1/.47,2/.50,3/.54,4/.57,5/.61,6/.65,7/.70,8/1.0,16
DLC9    FUNCTION    RN1,D4
.7,16/.8,17/.9,18/1.0,19
DEC9    FUNCTION    RN1,D12
.25,0/.3,9/.35,10/.4,11/.45,12/.5,13/.55,14/.6,15/.85,16/.9,17/
.95,18/1.0,19
DLCT    FUNCTION    RN1,D15
.07,1/.14,2/.22,3/.29,4/.37,5/.44,6/.53,7/.60,8/.65,9/.70,10/.75,11/
.80,12/.86,13/.93,14/1.0,15
DECT    FUNCTION    RN1,D19
.7,0/.71,1/.72,2/.74,3/.75,4/.76,5/.77,6/.78,7/.8,8/.81,9/.82,10/
.84,11/.85,12/.87,13/.88,14/.9,15/.93,17/.96,18/1.0,19
DLCR    FUNCTION    RN1,D15
.09,1/.18,2/.27,3/.36,4/.44,5/.53,6/.61,7/.70,8/.75,9/.79,10/.83,11/
.87,12/.91,13/.96,14/1.0,15
DECR    FUNCTION    RN1,D2
.80,0/1.0,16
REC1    TABLE       P3,0,1,20
REC2    TABLE       P3,0,1,20
```

```
                 INITIAL     X1,380
                 INITIAL     X2,21
                 INITIAL     X3,70
        IPS      STORAGE     380
               1 VARIABLE    (X2*1000)/X3
 1               GENERATE    V1,,,X1,,3
 2               QUEUE       CARS
 3               SEIZE       CAR
 4               GATE LS     20
 5               LOGIC R     20
 6               DEPART      CARS
 7               RELEASE     CAR
 8      TERM     TERMINATE
 9               GENERATE    V1,,,,1,3
10               GATE LR     19,TERM
11               TRANSFER    ,BEGN
12      NTR      LOGIC S     19
13      BEGN     TEST  E     P1,0,SKIP
14               TEST G      Q$CARS,0,SKIP
15               TEST LE     Q$LCR1,35,BYPS
16               LOGIC S     20
17               ASSIGN      1,1
18      SKIP     TRANSFER    ,LST1
19      BYPS     LOGIC S     20
20               SPLIT       1,LHO1
21               ASSIGN      1,1
22               ASSIGN      3,FN$DECP
23               TRANSFER    ,LSZ1
24      LST1     TEST  E     P1,1,LHK1
25               SPLIT       1,LEC1
26      LHO1     ASSIGN      1,0
27               ASSIGN      2,0
28               ASSIGN      3,0
29      LHK1     GATE  LR    3,LTH1
30               TRANSFER    ,LSO1
31      LEC1     QUEUE       LCR1
32               LINK        LCH,FIFO,LFA1
33      LFA1     SEIZE       LCR1
34               DEPART      LCR1
35               TEST E      P2,0,LDC1
36               ENTER       IPS
        LVB1     VARIABLE    FN$NORM*400
37               ADVANCE     2000,V$LVB1
38               ASSIGN      2,1
39               ASSIGN      3,FN$DLCP
40      LDC1     RELEASE     LCR1
41               UNLINK      LCH,LFA1,1
42      LSZ1     SEIZE       LCH1
43               LOGIC S     3
44               GATE LR     3
45               RELEASE     LCH1
46               TRANSFER    ,LSO1
47      LTH1     LOGIC R     3
48               TERMINATE
        LAV1     FVARIABLE   (55/X3)(1000)
49      LSC1     ADVANCE     V$LAV1
50               TRANSFER    ,MAO
```

```
      MERG1 MACRO      MAX,MAH,MAA,MAB,MAC,MAD,MAE,MAO,MAG,MAR                              230
 51   MAR   LOGIC S    MAR                                                                  230
 52         GATE  LS   MAE,MAX                                                              230
 53         LOGIC S    MAB                                                                  230
 54         GATE  LS   MAC                                                                  230
 55         TEST  E    P1,1,MAH                                                             230
 56         LOGIC S    MAA                                                                  230
 57         PRIORITY   0,BUFFER                                                             230
 58         PRIORITY   1                                                                    230
 59         PRIORITY   0,BUFFER                                                             230
 60         PRIORITY   1                                                                    230
 61   MAX   LOGIC R    MAD                                                                  230
 62         LOGIC R    MAA                                                                  230
 63         LOGIC R    MAB                                                                  230
 64         LOGIC R    MAC                                                                  230
 65         TRANSFER   ,MAG                                                                 230
 66   MAO   LOGIC S    MAE                                                                  230
 67         GATE  LS   MAR,MAX                                                              230
 68         LOGIC S    MAC                                                                  230
 69         GATE  LS   MAB                                                                  230
 70         TEST  E    P1,1,TERM                                                            230
 71         LOGIC S    MAD                                                                  230
 72         PRIORITY   0,BUFFER                                                             230
 73         PRIORITY   1                                                                    230
      MERG2 MACRO      MAX,MAH,MAF,MAV,BV$MAV,LS$MAA*LS$MAD,MAQ,MAP,MAT,MAG                 231
 74         GATE  NU   MAQ,MAQ                                                              231
      MAV   BVARIABLE  LS$MAA*LS$MAD                                                        231
 75         TEST  E    BV$MAV,1,MAP                                                         231
 76   MAQ   QUEUE      MAQ                                                                  231
 77         LINK       MAF,FIFO,MAF                                                         231
 78   MAF   SEIZE      MAQ                                                                  231
 79         LOGIC S    MAF                                                                  231
 80         GATE  LR   MAF                                                                  231
 81         DEPART     MAQ                                                                  231
 82         RELEASE    MAQ                                                                  231
 83         UNLINK     MAF,MAF,1                                                            231
 84         TRANSFER   ,MAX                                                                 231
 85   MAP   LOGIC S    MAF                                                                  231
 86         TRANSFER   ,MAX                                                                 231
 87   MAH   PRIORITY   0,BUFFER                                                             231
 88         PRIORITY   1                                                                    231
 89         PRIORITY   0,BUFFER                                                             231
 90         PRIORITY   1                                                                    231
 91         GATE  LR   MAF,MAT                                                              231
 92         TRANSFER   ,MAX                                                                 231
 93   MAT   LOGIC R    MAF                                                                  231
 94         TERMINATE                                                                       231
 95   MAG   ADVANCE    0                                                                    231
      MERG3 MACRO      MAS,V$MAS,(090*1000)/X3                                              232
      MAS   VARIABLE   (090*1000)/X3                                                        232
 96         ADVANCE    V$MAS                                                                232
      ULST1 MACRO      UAH,UAO,UAB,UAQ,Q$UAQ,V$UAQ,1,4000,15,FN$NORM*300                    233
 97   UAQ   TEST  E    P1,1,UAH                                                             233
 98         TEST  E    P3,1,UAO                                                             233
 99         TEST  L    Q$UAQ,15,UAO                                                         233
100         QUEUE      UAQ                                                                  233
101         SPLIT      1,UAH                                                                233
```

```
102             TEST   E      P2,1,UAB                                                 233
103             SEIZE         UAH                                                      233
        UAQ     VARIABLE      FN$NORM*800                                              233
104             ADVANCE       4000,V$UAQ                                               233
105             LEAVE         IPS                                                      233
106             ASSIGN        2,0                                                      233
107             RELEASE       UAH                                                      233
        ULST2   MACRO         UAB,UAL,CH$UAB,V$UAL,FN$DEC1,UAS,2000,1,FN$NORM*400      234
108             TEST   GE     CH$UAB,1,UAB                                             234
109             ASSIGN        3,FN$DEC1                                                234
110             TRANSFER      ,UAL                                                     234
111     UAB     QUEUE         UAB                                                      234
112             LINK          UAB,FIFO,UAS                                             234
113     UAS     TEST   G      CH$UAB,1                                                 234
114             SEIZE         UAL                                                      234
115             DEPART        UAB                                                      234
        UAL     VARIABLE      FN$NORM*400                                              234
116             ADVANCE       2000,V$UAL                                               234
117             ENTER         IPS                                                      234
118             ASSIGN        2,1                                                      234
119             RELEASE       UAL                                                      234
120             UNLINK        UAB,UAS,1                                                234
        ULST3   MACRO         UAL,UAI,UAO,UAH,UAT,V$LAT,UAQ,FN$DLC1,(120*1000)/X3      235
121             ASSIGN        3,FN$DLC1                                                235
122     LAL     SEIZE         UAO                                                      235
123             LOGIC S       UAI                                                      235
124             GATE   LR     UAI                                                      235
125             RELEASE       UAO                                                      235
126             DEPART        UAQ                                                      235
127             TRANSFER      ,UAO                                                     235
128     UAH     ASSIGN        1,0                                                      235
129             ASSIGN        2,0                                                      235
130             ASSIGN        3,0                                                      235
131             GATE   LR     UAI,UAT                                                  235
132             TRANSFER      ,UAO                                                     235
133     LAT     LOGIC R       UAI                                                      235
134             TERMINATE                                                              235
        UAT     VARIABLE      (120*1000)/X3                                            235
135     UAO     ADVANCE       V$UAT                                                    235
        ULST1   MACRO         UBH,UBO,UBB,UBQ,Q$UBQ,V$UBQ,2,4000,15,FN$NORM*800        236
136     UBQ     TEST   E      P1,1,UBH                                                 236
137             TEST   E      P3,2,UBC                                                 236
138             TEST   L      Q$UBQ,15,UBO                                             236
139             QUEUE         UBQ                                                      236
140             SPLIT         1,UBH                                                    236
141             TEST   E      P2,1,UBB                                                 236
142             SEIZE         UBH                                                      236
        UBQ     VARIABLE      FN$NORM*800                                              236
143             ADVANCE       4000,V$UBQ                                               236
144             LEAVE         IPS                                                      236
145             ASSIGN        2,0                                                      236
146             RELEASE       UBH                                                      236
        ULST2   MACRO         UBB,UBL,CH$UBB,V$UBL,FN$DEC1,UBS,2000,1,FN$NORM*400      237
147             TEST   GE     CH$UBB,1,UBB                                             237
148             ASSIGN        3,FN$DEC1                                                237
149             TRANSFER      ,UBL                                                     237
150     UBB     QUEUE         UBB                                                      237
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151              LINK        UBB,FIFO,UBS                                              237
152     UBS      TEST   G    CH$UBB,1                                                  237
153              SEIZE       UBL                                                       237
154              DEPART      UBB                                                       237
        UBL      VARIABLE    FN$NORM*400                                               237
155              ADVANCE     2000,V$UBL                                                237
156              ENTER       IPS                                                       237
157              ASSIGN      2,1                                                       237
158              RELEASE     UBL                                                       237
159              UNLINK      UBB,UBS,1                                                 237
        ULST3    MACRO       UBL,UBI,UBO,UBH,UBT,V$UBT,UBQ,FN$DLC1,(601*1000)/X3       238
160              ASSIGN      3,FN$DLC1                                                 238
161     UBL      SEIZE       UBO                                                       238
162              LOGIC  S    UBI                                                       238
163              GATE   LR   UBI                                                       238
164              RELEASE     UBO                                                       238
165              DEPART      UBQ                                                       238
166              TRANSFER    ,UBO                                                      238
167     UBH      ASSIGN      1,0                                                       238
168              ASSIGN      2,0                                                       238
169              ASSIGN      3,0                                                       238
170              GATE   LR   UBI,UBT                                                   238
171              TRANSFER    ,UBO                                                      238
172     UBT      LOGIC  R    UBI                                                       238
173              TERMINATE                                                             238
        UBT      VARIABLE    (601*1000)/X3                                             238
174     UBO      ADVANCE     V$UBT                                                     238
        ULST1    MACRO       UCH,UCO,UCB,UCQ,Q$UCQ,V$UCQ,3,4000,15,FN$NORM*800         239
175     UCQ      TEST   E    P1,1,UCH                                                  239
176              TEST   E    P3,3,UCO                                                  239
177              TEST   L    Q$UCQ,15,UCO                                              239
178              QUEUE       UCQ                                                       239
179              SPLIT       1,UCH                                                     239
180              TEST   E    P2,1,UCB                                                  239
181              SEIZE       UCH                                                       239
        UCQ      VARIABLE    FN$NORM*800                                               239
182              ADVANCE     4000,V$UCQ                                                239
183              LEAVE       IPS                                                       239
184              ASSIGN      2,0                                                       239
185              RELEASE     UCH                                                       239
        ULST2    MACRO       UCB,UCL,CH$UCB,V$UCL,FN$DEC1,UCS,2000,1,FN$NORM*400       240
186              TEST   GE   CH$UCB,1,UCB                                              240
187              ASSIGN      3,FN$DEC1                                                 240
188              TRANSFER    ,UCL                                                      240
189     UCB      QUEUE       UCB                                                       240
190              LINK        UCB,FIFO,UCS                                              240
191     UCS      TEST   G    CH$UCB,1                                                  240
192              SEIZE       UCL                                                       240
193              DEPART      UCB                                                       240
        UCL      VARIABLE    FN$NORM*400                                               240
194              ADVANCE     2000,V$UCL                                                240
195              ENTER       IPS                                                       240
196              ASSIGN      2,1                                                       240
197              RELEASE     UCL                                                       240
198              UNLINK      UCB,UCS,1                                                 240
        ULST3    MACRO       UCL,UCI,UCO,UCH,UCT,V$UCT,UCQ,FN$DLC1,(430*1000)/X3       241
199              ASSIGN      3,FN$DLC1                                                 241
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200      UCL    SEIZE      UCO                                                          241
201             LOGIC S    UCI                                                          241
202             GATE  LR   UCI                                                          241
203             RELEASE    UCO                                                          241
204             DEPART     UCQ                                                          241
205             TRANSFER   ,UCO                                                         241
206      UCH    ASSIGN     1,0                                                          241
207             ASSIGN     2,0                                                          241
208             ASSIGN     3,0                                                          241
209             GATE  LR   UCI,UCT                                                      241
210             TRANSFER   ,UCO                                                         241
211      UCT    LOGIC R    UCI                                                          241
212             TERMINATE                                                               241
         UCT    VARIABLE   (430*1000)/X3                                                241
213      UCO    ADVANCE    V$UCT                                                        241
         ULST1  MACRO      UDH,UDO,UDB,UDQ,Q$UDQ,V$UDQ,4,4000,15,FN$NORM*800            242
214      UDQ    TEST  E    P1,1,UDH                                                     242
215             TEST  E    P3,4,UDO                                                     242
216             TEST  L    Q$UDQ,15,UDO                                                 242
217             QUEUE      UDQ                                                          242
218             SPLIT      1,UDH                                                        242
219             TEST  E    P2,1,UDB                                                     242
220             SEIZE      UDH                                                          242
         UDQ    VARIABLE   FN$NORM*800                                                  242
221             ADVANCE    4000,V$UDQ                                                   242
222             LEAVE      IPS                                                          242
223             ASSIGN     2,0                                                          242
224             RELEASE    UDH                                                          242
         ULST2  MACRO      UDB,UDL,CH$UDB,V$UDL,FN$DEC1,UDS,2000,1,FN$NORM*400          243
225             TEST  GE   CH$UDB,1,UDB                                                 243
226             ASSIGN     3,FN$DEC1                                                    243
227             TRANSFER   ,UDL                                                         243
228      UDB    QUEUE      UDB                                                          243
229             LINK       UDB,FIFO,UDS                                                 243
230      UDS    TEST  G    CH$UDB,1                                                     243
231             SEIZE      UDL                                                          243
232             DEPART     UDB                                                          243
         UDL    VARIABLE   FN$NORM*400                                                  243
233             ADVANCE    2000,V$UDL                                                   243
234             ENTER      IPS                                                          243
235             ASSIGN     2,1                                                          243
236             RELEASE    UDL                                                          243
237             UNLINK     UDB,UDS,1                                                    243
         ULST3  MACRO      UDL,UDI,UDO,UDH,UDT,V$UDT,UDQ,FN$DLC1,(487*1000)/X3          244
238             ASSIGN     3,FN$DLC1                                                    244
239      UDL    SEIZE      UDO                                                          244
240             LOGIC S    UDI                                                          244
241             GATE  LR   UDI                                                          244
242             RELEASE    UDO                                                          244
243             DEPART     UDQ                                                          244
244             TRANSFER   ,UDO                                                         244
245      UDH    ASSIGN     1,0                                                          244
246             ASSIGN     2,0                                                          244
247             ASSIGN     3,0                                                          244
248             GATE  LR   UDI,UDT                                                      244
249             TRANSFER   ,UDO                                                         244
250      UDT    LOGIC R    UDI                                                          244
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251              TERMINATE                                                                 244
          UCT    VARIABLE     (487*1000)/X3                                                244
252       UDC    ADVANCE      V$UCT                                                        244
          ULST1  MACRO        UEH,UEO,UEB,UEQ,Q$UEQ,V$UEQ,5,4000,15,FN$NORM*800            245
253       UEQ    TEST   E     P1,1,UEH                                                     245
254              TEST   E     P3,5,UEC                                                     245
255              TEST   L     Q$UEQ,15,UEO                                                 245
256              QUEUE        UEQ                                                          245
257              SPLIT        1,UEH                                                        245
258              TEST   E     P2,1,UEB                                                     245
259              SEIZE        UEH                                                          245
          LEQ    VARIABLE     FN$NORM*800                                                  245
260              ADVANCE      4000,V$UEQ                                                   245
261              LEAVE        IPS                                                          245
262              ASSIGN       2,0                                                          245
263              RELEASE      UEH                                                          245
          ULST2  MACRO        UEB,UEL,CH$UEB,V$UEL,FN$DEC1,UES,2000,1,FN$NORM*400          246
264              TEST   GE    CH$UEB,1,UEB                                                 246
265              ASSIGN       3,FN$DEC1                                                    246
266              TRANSFER     ,UEL                                                         246
267       UEB    QUEUE        UEB                                                          246
268              LINK         UEB,FIFO,UES                                                 246
269       LES    TEST   G     CH$UEB,1                                                     246
270              SEIZE        UEL                                                          246
271              DEPART       UEB                                                          246
          LEL    VARIABLE     FN$NORM*400                                                  246
272              ADVANCE      2000,V$UEL                                                   246
273              ENTER        IPS                                                          246
274              ASSIGN       2,1                                                          246
275              RELEASE      UEL                                                          246
276              UNLINK       UEB,UES,1                                                    246
          ULST3  MACRO        UEL,UEI,UEO,UEH,UET,V$UET,JEQ,FN$DLC1,(120*1000)/X3          247
277              ASSIGN       3,FN$DLC1                                                    247
278       LEL    SEIZE        UEO                                                          247
279              LOGIC  S     UEI                                                          247
280              GATE   LR    UEI                                                          247
281              RELEASE      UEO                                                          247
282              DEPART       UEQ                                                          247
283              TRANSFER     ,UEO                                                         247
284       LEH    ASSIGN       1,0                                                          247
285              ASSIGN       2,0                                                          247
286              ASSIGN       3,0                                                          247
287              GATE   LR    UEI,UET                                                      247
288              TRANSFER     ,UEO                                                         247
289       LET    LOGIC  R     UEI                                                          247
290              TERMINATE                                                                 247
          UET    VARIABLE     (120*1000)/X3                                                247
291       UEC    ADVANCE      V$UET                                                        247
          ULST1  MACRO        UFH,UFO,UFB,UFQ,Q$UFQ,V$UFQ,6,4000,15,FN$NORM*800            248
292       UFQ    TEST   E     P1,1,UFH                                                     248
293              TEST   E     P3,6,UFC                                                     248
294              TEST   L     Q$UFQ,15,UFO                                                 248
295              QUEUE        UFQ                                                          248
296              SPLIT        1,UFH                                                        248
297              TEST   E     P2,1,UFB                                                     248
298              SEIZE        UFH                                                          248
          LFQ    VARIABLE     FN$NORM*800                                                  248
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299              ADVANCE    4000,V$UFQ                                                    248
300              LEAVE      IPS                                                           248
301              ASSIGN     2,0                                                           248
302              RELEASE    UFH                                                           248
         ULST2   MACRO      UFB,UFL,CH$UFB,V$UFL,FN$DEC1,UFS,2000,1,FN$NORM*400           249
303              TEST   GE  CH$UFB,1,UFB                                                  249
304              ASSIGN     3,FN$DEC1                                                     249
305              TRANSFER   ,UFL                                                          249
306      UFB     QUEUE      UFB                                                           249
307              LINK       UFB,FIFO,UFS                                                  249
308      UFS     TEST   G   CH$UFB,1                                                      249
309              SEIZE      UFL                                                           249
310              DEPART     UFB                                                           249
         UFL     VARIABLE   FN$NORM*400                                                   249
311              ADVANCE    2000,V$UFL                                                    249
312              ENTER      IPS                                                           249
313              ASSIGN     2,1                                                           249
314              RELEASE    UFL                                                           249
315              UNLINK     UFB,UFS,1                                                     249
         ULST3   MACRO      UFL,UFI,UFO,UFH,UFT,V$UFT,UFQ,FN$DLC1,(165*1000)/X3           250
316              ASSIGN     3,FN$DLC1                                                     250
317      UFL     SEIZE      UFO                                                           250
318              LOGIC S    UFI                                                           250
319              GATE   LR  UFI                                                           250
320              RELEASE    UFO                                                           250
321              DEPART     UFQ                                                           250
322              TRANSFER   ,UFO                                                          250
323      UFH     ASSIGN     1,0                                                           250
324              ASSIGN     2,0                                                           250
325              ASSIGN     3,0                                                           250
326              GATE   LR  UFI,UFT                                                       250
327              TRANSFER   ,UFO                                                          250
328      UFT     LOGIC R    UFI                                                           250
329              TERMINATE                                                                250
         UFT     VARIABLE   (165*1000)/X3                                                 250
330      UFO     ADVANCE    V$UFT                                                         250
         ULST1   MACRO      UGH,UGO,UGB,UGQ,Q$UGQ,V$UGQ,7,4000,15,FN$NORM*800             251
331      UGQ     TEST   E   P1,1,UGH                                                      251
332              TEST   E   P3,7,UGO                                                      251
333              TEST   L   Q$UGQ,15,UGO                                                  251
334              QUEUE      UGQ                                                           251
335              SPLIT      1,UGH                                                         251
336              TEST   E   P2,1,UGB                                                      251
337              SEIZE      UGH                                                           251
         UGQ     VARIABLE   FN$NORM*800                                                   251
338              ADVANCE    4000,V$UGQ                                                    251
339              LEAVE      IPS                                                           251
340              ASSIGN     2,0                                                           251
341              RELEASE    UGH                                                           251
         ULST2   MACRO      UGB,UGL,CH$UGB,V$UGL,FN$DEC1,UGS,2000,1,FN$NORM*400           252
342              TEST   GE  CH$UGB,1,UGB                                                  252
343              ASSIGN     3,FN$DEC1                                                     252
344              TRANSFER   ,UGL                                                          252
345      UGB     QUEUE      UGB                                                           252
346              LINK       UGB,FIFO,UGS                                                  252
347      UGS     TEST   G   CH$UGB,1                                                      252
348              SEIZE      UGL                                                           252
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349          DEPART     UGB                                                     252
      UGL    VARIABLE   FN$NORM*400                                             252
350          ADVANCE    2000,V$UGL                                              252
351          ENTER      IPS                                                     252
352          ASSIGN     2,1                                                     252
353          RELEASE    UGL                                                     252
354          UNLINK     UGB,UGS,1                                               252
      ULST3  MACRO      UGL,UGI,UGO,UGH,UGT,V$UGT,UGQ,FN$DLC1,(120*1000)/X3     253
355          ASSIGN     3,FN$DLC1                                               253
356   UGL    SEIZE      UGO                                                     253
357          LOGIC S    UGI                                                     253
358          GATE  LR   UGI                                                     253
359          RELEASE    UGO                                                     253
360          DEPART     UGQ                                                     253
361          TRANSFER   ,UGO                                                    253
362   UGH    ASSIGN     1,0                                                     253
363          ASSIGN     2,0                                                     253
364          ASSIGN     3,0                                                     253
365          GATE  LR   UGI,UGT                                                 253
366          TRANSFER   ,UGO                                                    253
367   UGT    LOGIC R    UGI                                                     253
368          TERMINATE                                                          253
      UGT    VARIABLE   (120*1000)/X3                                           253
369   UGO    ADVANCE    V$UGT                                                   253
      ULST1  MACRO      UHH,UHO,UHB,UHQ,Q$UHQ,V$UHQ,8,4000,15,FN$NORM*800       254
370   UHQ    TEST  E    P1,1,UHH                                                254
371          TEST  E    P3,8,UHO                                                254
372          TEST  L    Q$UHQ,15,UHO                                            254
373          QUEUE      UHQ                                                     254
374          SPLIT      1,UHH                                                   254
375          TEST  E    P2,1,UHB                                                254
376          SEIZE      UHH                                                     254
      UHQ    VARIABLE   FN$NORM*800                                             254
377          ADVANCE    4000,V$UHQ                                              254
378          LEAVE      IPS                                                     254
379          ASSIGN     2,0                                                     254
380          RELEASE    UHH                                                     254
      ULST2  MACRO      UHB,UHL,CH$UHB,V$UHL,FN$DEC1,UHS,2000,1,FN$NORM*400     255
381          TEST  GE   CH$UHB,1,UHB                                            255
382          ASSIGN     3,FN$DEC1                                               255
383          TRANSFER   ,UHL                                                    255
384   UHB    QUEUE      UHB                                                     255
385          LINK       UHB,FIFO,UHS                                            255
386   UHS    TEST  G    CH$UHB,1                                                255
387          SEIZE      UHL                                                     255
388          DEPART     UHB                                                     255
      UHL    VARIABLE   FN$NORM*400                                             255
389          ADVANCE    2000,V$UHL                                              255
390          ENTER      IPS                                                     255
391          ASSIGN     2,1                                                     255
392          RELEASE    UHL                                                     255
393          UNLINK     UHB,UHS,1                                               255
      ULST3  MACRO      UHL,UHI,UHO,UHH,UHT,V$UHT,UHQ,FN$DLC1,(078*1000)/X3     256
394          ASSIGN     3,FN$DLC1                                               256
395   UHL    SEIZE      UHO                                                     256
396          LOGIC S    UHI                                                     256
397          GATE  LR   UHI                                                     256
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398             RELEASE     UHO                                                              256
399             DEPART      UHQ                                                              256
400             TRANSFER    ,UHO                                                             256
401      UHH    ASSIGN      1,0                                                              256
402             ASSIGN      2,0                                                              256
403             ASSIGN      3,0                                                              256
404             GATE  LR    UHI,UHT                                                          256
405             TRANSFER    ,UHO                                                             256
406      UHT    LOGIC R     UHI                                                              256
407             TERMINATE                                                                    256
         UHT    VARIABLE    (078*1000)/X3                                                    256
408      LHO    ADVANCE     V$UHT                                                            256
         SPLT1  MACRO       SAL,SAR,SAH,SAA,SAC,SAB,SAV,P3'GE'9*P3'L'17,BV$SAV,999           257
409             TEST  E     P1,1,SAH                                                         257
         SAV    BVARIABLE   P3'GE'9*P3'L'17                                                  257
410             TEST  E     BV$SAV,1,SAC                                                     257
411             TEST  LE    Q$LCR1,999,SAC                                                   257
412             SPLIT       1,SAA                                                            257
413             TRANSFER    ,SAL                                                             257
414      SAA    ASSIGN      1,0                                                              257
415             ASSIGN      2,0                                                              257
416             ASSIGN      3,0                                                              257
417             TRANSFER    ,SAR                                                             257
418      SAC    SPLIT       1,SAB                                                            257
419             TRANSFER    ,SAR                                                             257
420      SAB    ASSIGN      1,0                                                              257
421             ASSIGN      2,0                                                              257
422             ASSIGN      3,0                                                              257
423             TRANSFER    ,SAL                                                             257
424      SAH    SPLIT       1,SAL                                                            257
425             TRANSFER    ,SAR                                                             257
         SPLT2  MACRO       SAX,MBR,SAL,V$SAX,(236*1000)/X3                                  258
         SAX    VARIABLE    (236*1000)/X3                                                    258
426      SAL    ADVANCE     V$SAX                                                            258
427             TRANSFER    ,MBR                                                             258
         SPLT3  MACRO       SAY,MDO,SAR,V$SAY,(060*1000)/X3                                  259
         SAY    VARIABLE    (060*1000)/X3                                                    259
428      SAR    ADVANCE     V$SAY                                                            259
429             TRANSFER    ,MDO                                                             259
         MERG1  MACRO       MBX,MBH,MBA,MBB,MBC,MBD,MBE,MBO,MBG,MBR                          260
430      MBR    LOGIC S     MBR                                                              260
431             GATE  LS    MBE,MBX                                                          260
432             LOGIC S     MBB                                                              260
433             GATE  LS    MBC                                                              260
434             TEST  E     P1,1,MBH                                                         260
435             LOGIC S     MBA                                                              260
436             PRIORITY    0,BUFFER                                                         260
437             PRIORITY    1                                                                260
438             PRIORITY    0,BUFFER                                                         260
439             PRIORITY    1                                                                260
440      MBX    LOGIC R     MBD                                                              260
441             LOGIC R     MBA                                                              260
442             LOGIC R     MBB                                                              260
443             LOGIC R     MBC                                                              260
444             TRANSFER    ,MBG                                                             260
445      MBO    LOGIC S     MBE                                                              260
446             GATE  LS    MBR,MBX                                                          260
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447          LOGIC S     MBC                                                        260
448          GATE  LS    MBB                                                        260
449          TEST  E     P1,1,TERM                                                  260
450          LOGIC S     MBD                                                        260
451          PRIORITY    0,BUFFER                                                   260
452          PRIORITY    1                                                          260
      MERG2  MACRO       MBX,MBH,MBF,MBV,BV$MBV,LS$MBA*LS$MBD,MBQ,MBP,MBT,MBG       261
453          GATE  NU    MBQ,MBQ                                                    261
      MBV    BVARIABLE   LS$MBA*LS$MBD                                              261
454          TEST  E     BV$MBV,1,MBP                                               261
455   MBQ    QUEUE       MBQ                                                        261
456          LINK        MBF,FIFO,MBF                                               261
457   MBF    SEIZE       MBQ                                                        261
458          LOGIC S     MBF                                                        261
459          GATE  LR    MBF                                                        261
460          DEPART      MBQ                                                        261
461          RELEASE     MBQ                                                        261
462          UNLINK      MBF,MBF,1                                                  261
463          TRANSFER    ,MBX                                                       261
464   MBP    LOGIC S     MBF                                                        261
465          TRANSFER    ,MBX                                                       261
466   MBH    PRIORITY    0,BUFFER                                                   261
467          PRIORITY    1                                                          261
468          PRIORITY    0,BUFFER                                                   261
469          PRIORITY    1                                                          261
470          GATE  LR    MBF,MBT                                                    261
471          TRANSFER    ,MBX                                                       261
472   MBT    LOGIC R     MBF                                                        261
473          TERMINATE                                                              261
474   MBG    ADVANCE     0                                                          261
      MERG3  MACRO       MBS,V$MBS,(392*1000)/X3                                    262
      MBS    VARIABLE    (392*1000)/X3                                              262
475          ADVANCE     V$MBS                                                      262
      ULST1  MACRO       UIH,UIO,UIB,UIQ,Q$UIQ,V$UIQ,9,5000,5,FN$NORM*1000          263
476   UIQ    TEST  E     P1,1,UIH                                                   263
477          TEST  E     P3,9,UIO                                                   263
478          TEST  L     Q$UIQ,5,UIO                                                263
479          QUEUE       UIQ                                                        263
480          SPLIT       1,UIH                                                      263
481          TEST  E     P2,1,UIB                                                   263
482          SEIZE       UIH                                                        263
      UIQ    VARIABLE    FN$NORM*1000                                               263
483          ADVANCE     5000,V$UIQ                                                 263
484          LEAVE       IPS                                                        263
485          ASSIGN      2,0                                                        263
486          RELEASE     UIH                                                        263
      ULST2  MACRO       UIB,UIL,CH$UIB,V$UIL,FN$DEC9,UIS,2500,1,FN$NORM*500        264
487          TEST  GE    CH$UIB,1,UIB                                               264
488          ASSIGN      3,FN$DEC9                                                  264
489          TRANSFER    ,UIL                                                       264
490   UIB    QUEUE       UIB                                                        264
491          LINK        UIB,FIFO,UIS                                               264
492   UIS    TEST  G     CH$UIB,1                                                   264
493          SEIZE       UIL                                                        264
494          DEPART      UIB                                                        264
      UIL    VARIABLE    FN$NORM*500                                                264
495          ADVANCE     2500,V$UIL                                                 264
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496            ENTER      IPS                                                        264
497            ASSIGN     2,1                                                        264
498            RELEASE    UIL                                                        264
499            UNLINK     UIB,UIS,1                                                  264
      ULST3    MACRO      UIL,UII,UIO,UIH,UIT,V$UIT,JIQ,FN$DLC9,(080*1000)/X3        265
500            ASSIGN     3,FN$DLC9                                                  265
501   UIL      SEIZE      UIO                                                        265
502            LOGIC S    UII                                                        265
503            GATE  LR   UII                                                        265
504            RELEASE    UIO                                                        265
505            DEPART     UIQ                                                        265
506            TRANSFER   ,UIO                                                       265
507   UIH      ASSIGN     1,0                                                        265
508            ASSIGN     2,0                                                        265
509            ASSIGN     3,0                                                        265
510            GATE  LR   UII,UIT                                                    265
511            TRANSFER   ,UIO                                                       265
512   UIT      LOGIC R    UII                                                        265
513            TERMINATE                                                             265
      UIT      VARIABLE   (080*1000)/X3                                              265
514   UIO      ADVANCE    V$UIT                                                      265
      ULST1    MACRO      UJH,UJO,UJB,UJQ,Q$UJQ,V$UJQ,10,5000,5,FN$NORM*1000         266
515   UJQ      TEST  E    P1,1,UJH                                                   266
516            TEST  E    P3,10,UJO                                                  266
517            TEST  L    Q$UJQ,5,UJO                                                266
518            QUEUE      UJQ                                                        266
519            SPLIT      1,UJH                                                      266
520            TEST  E    P2,1,UJB                                                   266
521            SEIZE      UJH                                                        266
      UJQ      VARIABLE   FN$NORM*1000                                               266
522            ADVANCE    5000,V$UJQ                                                 266
523            LEAVE      IPS                                                        266
524            ASSIGN     2,0                                                        266
525            RELEASE    UJH                                                        266
      ULST2    MACRO      UJB,UJL,CH$UJB,V$UJL,FN$DEC9,UJS,2500,1,FN$NORM*500        267
526            TEST  GE   CH$UJB,1,UJB                                               267
527            ASSIGN     3,FN$DEC9                                                  267
528            TRANSFER   ,UJL                                                       267
529   UJB      QUEUE      UJB                                                        267
530            LINK       UJB,FIFO,UJS                                               267
531   UJS      TEST  G    CH$UJB,1                                                   267
532            SEIZE      UJL                                                        267
533            DEPART     UJB                                                        267
      UJL      VARIABLE   FN$NORM*500                                                267
534            ADVANCE    2500,V$UJL                                                 267
535            ENTER      IPS                                                        267
536            ASSIGN     2,1                                                        267
537            RELEASE    UJL                                                        267
538            UNLINK     UJB,UJS,1                                                  267
      ULST3    MACRO      UJL,UJI,UJO,UJH,UJT,V$UJT,UJQ,FN$DLC9,(080*1000)/X3        268
539            ASSIGN     3,FN$DLC9                                                  268
540   UJL      SEIZE      UJO                                                        268
541            LOGIC S    UJI                                                        268
542            GATE  LR   UJI                                                        268
543            RELEASE    UJO                                                        268
544            DEPART     UJQ                                                        268
545            TRANSFER   ,UJO                                                       268
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546      UJH    ASSIGN       1,0                                                                  268
547             ASSIGN       2,0                                                                  268
548             ASSIGN       3,0                                                                  268
549             GATE   LR    UJI,UJT                                                              268
550             TRANSFER     ,UJO                                                                 268
551      UJT    LOGIC R      UJI                                                                  268
552             TERMINATE                                                                         268
         UJT    VARIABLE     (080*1000)/X3                                                        268
553      UJO    ADVANCE      V$UJT                                                                268
         ULST1  MACRO        UKH,UKO,UKB,UKQ,Q$UKQ,V$UKQ,11,5000,5,FN$NORM*1000                  269
554      UKQ    TEST   E     P1,1,UKH                                                             269
555             TEST   E     P3,11,UKO                                                            269
556             TEST   L     Q$UKQ,5,UKO                                                          269
557             QUEUE        UKQ                                                                  269
558             SPLIT        1,UKH                                                                269
559             TEST   E     P2,1,UKB                                                             269
560             SEIZE        UKH                                                                  269
         UKQ    VARIABLE     FN$NORM*1000                                                         269
561             ADVANCE      5000,V$UKQ                                                           269
562             LEAVE        IPS                                                                  269
563             ASSIGN       2,0                                                                  269
564             RELEASE      UKH                                                                  269
         ULST2  MACRO        UKB,UKL,CH$UKB,V$UKL,FN$DEC9,UKS,2500,1,FN$NORM*500                 270
565             TEST   GE    CH$UKB,1,UKB                                                         270
566             ASSIGN       3,FN$DEC9                                                            270
567             TRANSFER     ,UKL                                                                 270
568      UKB    QUEUE        UKB                                                                  270
569             LINK         UKB,FIFO,UKS                                                         270
570      UKS    TEST   G     CH$UKB,1                                                             270
571             SEIZE        UKL                                                                  270
572             DEPART       UKB                                                                  270
         UKL    VARIABLE     FN$NORM*500                                                          270
573             ADVANCE      2500,V$UKL                                                           270
574             ENTER        IPS                                                                  270
575             ASSIGN       2,1                                                                  270
576             RELEASE      UKL                                                                  270
577             UNLINK       UKB,UKS,1                                                            270
         ULST3  MACRO        UKL,UKI,UKO,UKH,UKT,V$UKT,JKQ,FN$DLC9,(080*1000)/X3                 271
578             ASSIGN       3,FN$DLC9                                                            271
579      UKL    SEIZE        UKO                                                                  271
580             LOGIC  S     UKI                                                                  271
581             GATE   LR    UKI                                                                  271
582             RELEASE      UKO                                                                  271
583             DEPART       UKQ                                                                  271
584             TRANSFER     ,UKO                                                                 271
585      UKH    ASSIGN       1,0                                                                  271
586             ASSIGN       2,0                                                                  271
587             ASSIGN       3,0                                                                  271
588             GATE   LR    UKI,UKT                                                              271
589             TRANSFER     ,UKO                                                                 271
590      UKT    LOGIC R      UKI                                                                  271
591             TERMINATE                                                                         271
         UKT    VARIABLE     (080*1000)/X3                                                        271
592      UKO    ADVANCE      V$UKT                                                                271
         ULST1  MACRO        ULH,ULO,ULB,ULQ,Q$ULQ,V$ULQ,12,5000,5,FN$NORM*1000                  272
593      ULQ    TEST   E     P1,1,ULH                                                             272
594             TEST   E     P3,12,ULO                                                            272
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595             TEST   L     Q$ULQ,5,ULO                                                      272
596             QUEUE        ULQ                                                              272
597             SPLIT        1,ULH                                                            272
598             TEST   E     P2,1,ULB                                                         272
599             SEIZE        ULH                                                              272
        ULQ     VARIABLE     FN$NORM*1000                                                     272
600             ADVANCE      5000,V$ULQ                                                       272
601             LEAVE        IPS                                                              272
602             ASSIGN       2,0                                                              272
603             RELEASE      ULH                                                              272
        ULST2   MACRO        ULB,ULL,CH$ULB,V$ULL,FN$DEC9,ULS,2500,1,FN$NORM*500              273
604             TEST   GE    CH$ULB,1,ULB                                                     273
605             ASSIGN       3,FN$DEC9                                                        273
606             TRANSFER     ,ULL                                                             273
607     ULB     QUEUE        ULB                                                              273
608             LINK         ULB,FIFO,ULS                                                     273
609     ULS     TEST   G     CH$ULB,1                                                         273
610             SEIZE        ULL                                                              273
611             DEPART       ULB                                                              273
        ULL     VARIABLE     FN$NORM*500                                                      273
612             ADVANCE      2500,V$ULL                                                       273
613             ENTER        IPS                                                              273
614             ASSIGN       2,1                                                              273
615             RELEASE      ULL                                                              273
616             UNLINK       ULB,ULS,1                                                        273
        ULST3   MACRO        ULL,ULI,ULO,ULH,ULT,V$LLT,ULQ,FN$DLC9,(221*1000)/X3              274
617             ASSIGN       3,FN$DLC9                                                        274
618     ULL     SEIZE        ULO                                                              274
619             LOGIC  S     ULI                                                              274
620             GATE   LR    ULI                                                              274
621             RELEASE      ULO                                                              274
622             DEPART       ULQ                                                              274
623             TRANSFER     ,ULO                                                             274
624     ULH     ASSIGN       1,0                                                              274
625             ASSIGN       2,0                                                              274
626             ASSIGN       3,0                                                              274
627             GATE   LR    ULI,ULT                                                          274
628             TRANSFER     ,ULO                                                             274
629     LLT     LOGIC  R     ULI                                                              274
630             TERMINATE                                                                     274
        ULT     VARIABLE     (221*1000)/X3                                                    274
631     ULO     ADVANCE      V$ULT                                                            274
        ULST1   MACRO        UMH,UMO,UMB,UMQ,Q$UMQ,V$UMQ,13,5000,5,FN$NORM*1000               275
632     UMQ     TEST   E     P1,1,UMH                                                         275
633             TEST   F     P3,13,UMO                                                        275
634             TEST   L     Q$UMQ,5,UMO                                                      275
635             QUEUE        UMQ                                                              275
636             SPLIT        1,UMH                                                            275
637             TEST   E     P2,1,UMB                                                         275
638             SEIZE        UMH                                                              275
        UMQ     VARIABLE     FN$NORM*1000                                                     275
639             ADVANCE      5000,V$UMQ                                                       275
640             LEAVE        IPS                                                              275
641             ASSIGN       2,0                                                              275
642             RELEASE      UMH                                                              275
        ULST2   MACRO        UMB,UML,CH$UMB,V$UML,FN$DEC9,UMS,2500,1,FN$NORM*500              276
643             TEST   GE    CH$UMB,1,UMB                                                     276
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 644            ASSIGN      3,FN$DEC9                                               276
 645            TRANSFER    ,UML                                                    276
 646      UMB   QUEUE       UMB                                                     276
 647            LINK        UMB,FIFO,UMS                                            276
 648      UMS   TEST   G    CH$UMB,1                                                276
 649            SEIZE       UML                                                     276
 650            DEPART      UMB                                                     276
          UML   VARIABLE    FN$NORM*500                                             276
 651            ADVANCE     2500,V$UML                                              276
 652            ENTER       IPS                                                     276
 653            ASSIGN      2,1                                                     276
 654            RELEASE     UML                                                     276
 655            UNLINK      UMB,UMS,1                                               276
          ULST3 MACRO       UML,UMI,UMO,UMH,UMT,V$UMT,UMQ,FN$DLC9,(080*1000)/X3     277
 656            ASSIGN      3,FN$DLC9                                               277
 657      UML   SEIZE       UMO                                                     277
 658            LOGIC S     UMI                                                     277
 659            GATE   LR   UMI                                                     277
 660            RELEASE     UMO                                                     277
 661            DEPART      UMQ                                                     277
 662            TRANSFER    ,UMO                                                    277
 663      UMH   ASSIGN      1,0                                                     277
 664            ASSIGN      2,0                                                     277
 665            ASSIGN      3,0                                                     277
 666            GATE   LR   UMI,UMT                                                 277
 667            TRANSFER    ,UMO                                                    277
 668      UMT   LOGIC R     UMI                                                     277
 669            TERMINATE                                                           277
          UMT   VARIABLE    (080*1000)/X3                                           277
 670      UMO   ADVANCE     V$UMT                                                   277
          ULST1 MACRO       UNH,UNO,UNB,UNQ,Q$UNQ,V$UNQ,14,5000,5,FN$NORM*1000      278
 671      UNQ   TEST   E    P1,1,UNH                                                278
 672            TEST   E    P3,14,UNO                                               278
 673            TEST   L    Q$UNQ,5,UNO                                             278
 674            QUEUE       UNQ                                                     278
 675            SPLIT       1,UNH                                                   278
 676            TEST   E    P2,1,UNB                                                278
 677            SEIZE       UNH                                                     278
          UNQ   VARIABLE    FN$NORM*1000                                            278
 678            ADVANCE     5000,V$UNQ                                              278
 679            LEAVE       IPS                                                     278
 680            ASSIGN      2,0                                                     278
 681            RELEASE     UNH                                                     278
          ULST2 MACRO       UNB,UNL,CH$UNB,V$UNL,FN$DEC9,UNS,2500,1,FN$NORM*500     279
 682            TEST   GE   CH$UNB,1,UNB                                            279
 683            ASSIGN      3,FN$DEC9                                               279
 684            TRANSFER    ,UNL                                                    279
 685      UNB   QUEUE       UNB                                                     279
 686            LINK        UNB,FIFO,UNS                                            279
 687      UNS   TEST   G    CH$UNB,1                                                279
 688            SEIZE       UNL                                                     279
 689            DEPART      UNB                                                     279
          UNL   VARIABLE    FN$NORM*500                                             279
 690            ADVANCE     2500,V$UNL                                              279
 691            ENTER       IPS                                                     279
 692            ASSIGN      2,1                                                     279
 693            RELEASE     UNL                                                     279
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694              UNLINK     UNB,UNS,1                                                     279
         ULST3   MACRO      UNL,UNI,UNO,UNH,UNT,V$UNT,UNQ,FN$DLC9,(080*1000)/X3           280
695              ASSIGN     3,FN$DLC9                                                     280
696      UNL     SEIZE      UNO                                                           280
697              LOGIC S    UNI                                                           280
698              GATE  LR   UNI                                                           280
699              RELEASE    UNO                                                           280
700              DEPART     UNQ                                                           280
701              TRANSFER   ,UNO                                                          280
702      UNH     ASSIGN     1,0                                                           280
703              ASSIGN     2,0                                                           280
704              ASSIGN     3,0                                                           280
705              GATE  LR   UNI,UNT                                                       280
706              TRANSFER   ,UNO                                                          280
707      UNT     LOGIC R    UNI                                                           280
708              TERMINATE                                                                280
         UNT     VARIABLE   (080*1000)/X3                                                 280
709      UNO     ADVANCE    V$UNT                                                         280
         ULST1   MACRO      UOH,UOO,UOB,UOQ,Q$UOQ,V$UOQ,15,5000,5,FN$NORM*1000            281
710      UOQ     TEST  E    P1,1,UOH                                                      281
711              TEST  E    P3,15,UOO                                                     281
712              TEST  L    Q$UOQ,5,UOO                                                   281
713              QUEUE      UOQ                                                           281
714              SPLIT      1,UOH                                                         281
715              TEST  E    P2,1,UOB                                                      281
716              SEIZE      UOH                                                           281
         UOQ     VARIABLE   FN$NORM*1000                                                  281
717              ADVANCE    5000,V$UOQ                                                    281
718              LEAVE      IPS                                                           281
719              ASSIGN     2,0                                                           281
720              RELEASE    UOH                                                           281
         ULST2   MACRO      UOB,UOL,CH$UOB,V$UOL,FN$DEC9,UOS,2500,1,FN$NORM*500           282
721              TEST  GE   CH$UOB,1,UOB                                                  282
722              ASSIGN     3,FN$DEC9                                                     282
723              TRANSFER   ,UOL                                                          282
724      UOB     QUEUE      UOB                                                           282
725              LINK       UOB,FIFO,UOS                                                  282
726      UOS     TEST  G    CH$UOB,1                                                      282
727              SEIZE      UOL                                                           282
728              DEPART     UOB                                                           282
         UOL     VARIABLE   FN$NORM*500                                                   282
729              ADVANCE    2500,V$UOL                                                    282
730              ENTER      IPS                                                           282
731              ASSIGN     2,1                                                           282
732              RELEASE    UOL                                                           282
733              UNLINK     UOB,UOS,1                                                     282
         ULST3   MACRO      UOL,UOI,UOO,UOH,UOT,V$UOT,UOQ,FN$DLC9,(226*1000)/X3           283
734              ASSIGN     3,FN$DLC9                                                     283
735      UOL     SEIZE      UOO                                                           283
736              LOGIC S    UOI                                                           283
737              GATE  LR   UOI                                                           283
738              RELEASE    UOO                                                           283
739              DEPART     UOQ                                                           283
740              TRANSFER   ,UOO                                                          283
741      UOH     ASSIGN     1,0                                                           283
742              ASSIGN     2,0                                                           283
743              ASSIGN     3,0                                                           283
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744              GATE  LR     UOI,UOT                                                          283
745              TRANSFER     ,UOO                                                             283
746        UOT   LOGIC R      UOI                                                              283
747              TERMINATE                                                                     283
           LCT   VARIABLE     (326*1000)/X3                                                    283
748        UOO   ADVANCE      V$UOT                                                            283
           SPLT1 MACRO        SBL,SBR,SBH,SBA,SBC,SBB,SBV,P3'E'16,BV$SBV,999                   284
749              TEST  E      P1,1,SBH                                                         284
           SBV   BVARIABLE    P3'E'16                                                          284
750              TEST  E      BV$SBV,1,SBC                                                     284
751              TEST  LE     Q$LCR1,999,SBC                                                   284
752              SPLIT        1,SBA                                                            284
753              TRANSFER     ,SBL                                                             284
754        SBA   ASSIGN       1,0                                                              284
755              ASSIGN       2,0                                                              284
756              ASSIGN       3,0                                                              284
757              TRANSFER     ,SBR                                                             284
758        SBC   SPLIT        1,SBB                                                            284
759              TRANSFER     ,SBR                                                             284
760        SBB   ASSIGN       1,0                                                              284
761              ASSIGN       2,0                                                              284
762              ASSIGN       3,0                                                              284
763              TRANSFER     ,SBL                                                             284
764        SBH   SPLIT        1,SBL                                                            284
765              TRANSFER     ,SBR                                                             284
           SPLT2 MACRO        SBX,UPQ,SBL,V$SBX,(098*1000)/X3                                  285
           SBX   VARIABLE     (098*1000)/X3                                                    285
766        SBL   ADVANCE      V$SBX                                                            285
767              TRANSFER     ,UPQ                                                             285
           SPLT3 MACRO        SBY,MCR,SBR,V$SBY,(150*1000)/X3                                  286
           SBY   VARIABLE     (150*1000)/X3                                                    286
768        SBR   ADVANCE      V$SBY                                                            286
769              TRANSFER     ,MCR                                                             286
           ULST1 MACRO        UPH,UPO,UPB,UPQ,Q$UPQ,V$UPQ,16,1000,70,FN$NORM*200               287
770        UPQ   TEST  E      P1,1,UPH                                                         287
771              TEST  E      P3,16,UPO                                                        287
772              TEST  L      Q$UPQ,70,UPO                                                     287
773              QUEUE        UPQ                                                              287
774              SPLIT        1,UPH                                                            287
775              TEST  E      P2,1,UPB                                                         287
776              SEIZE        UPH                                                              287
           UPQ   VARIABLE     FN$NORM*200                                                      287
777              ADVANCE      1000,V$UPQ                                                       287
778              LEAVE        IPS                                                              287
779              ASSIGN       2,0                                                              287
780              RELEASE      UPH                                                              287
           ULST2 MACRO        UPB,UPL,CH$UPB,V$UPL,FN$DECT,UPS,2000,1,FN$NORM*400              288
781              TEST  GE     CH$UPB,1,UPB                                                     288
782              ASSIGN       3,FN$DECT                                                        288
783              TRANSFER     ,UPL                                                             288
784        UPB   QUEUE        UPB                                                              288
785              LINK         UPB,FIFO,UPS                                                     288
786        UPS   TEST  G      CH$UPB,1                                                         288
787              SEIZE        UPL                                                              288
788              DEPART       UPB                                                              288
           UPL   VARIABLE     FN$NORM*400                                                      288
789              ADVANCE      2000,V$UPL                                                       288
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790                ENTER      IPS                                                                  288
791                ASSIGN     2,1                                                                  288
792                RELEASE    UPL                                                                  288
793                UNLINK     UPB,UPS,1                                                            288
         ULST3     MACRO      UPL,UPI,UPO,UPH,UPT,V$LPT,UPQ,FN$DLCT,(256*1000)/X3                  289
794                ASSIGN     3,FN$DLCT                                                            289
795      LPL       SEIZE      UPO                                                                  289
796                LOGIC S    UPI                                                                  289
797                GATE  LR   UPI                                                                  289
798                RELEASE    UPO                                                                  289
799                DEPART     UPQ                                                                  289
800                TRANSFER   ,UPO                                                                 289
801      UPH       ASSIGN     1,0                                                                  289
802                ASSIGN     2,0                                                                  289
803                ASSIGN     3,0                                                                  289
804                GATE  LR   UPI,UPT                                                              289
805                TRANSFER   ,UPO                                                                 289
806      LPT       LOGIC R    UPI                                                                  289
807                TERMINATE                                                                       289
         UPT       VARIABLE   (256*1000)/X3                                                        289
808      LPO       ADVANCE    V$UPT                                                                289
809                TRANSFER   ,MCO                                                                 290
         MERG1     MACRO      MCX,MCH,MCA,MCB,MCC,MCD,MCE,MCO,MCG,MCR                              291
810      MCR       LOGIC S    MCR                                                                  291
811                GATE  LS   MCE,MCX                                                              291
812                LOGIC S    MCB                                                                  291
813                GATE  LS   MCC                                                                  291
814                TEST  E    P1,1,MCH                                                             291
815                LOGIC S    MCA                                                                  291
816                PRIORITY   0,BUFFER                                                             291
817                PRIORITY   1                                                                    291
818                PRIORITY   0,BUFFER                                                             291
819                PRIORITY   1                                                                    291
820      MCX       LOGIC R    MCD                                                                  291
821                LOGIC R    MCA                                                                  291
822                LOGIC R    MCB                                                                  291
823                LOGIC R    MCC                                                                  291
824                TRANSFER   ,MCG                                                                 291
825      MCO       LOGIC S    MCE                                                                  291
826                GATE  LS   MCR,MCX                                                              291
827                LOGIC S    MCC                                                                  291
828                GATE  LS   MCB                                                                  291
829                TEST  E    P1,1,TERM                                                            291
830                LOGIC S    MCD                                                                  291
831                PRIORITY   0,BUFFER                                                             291
832                PRIORITY   1                                                                    291
         MERG2     MACRO      MCX,MCH,MCF,MCV,BV$MCV,LS$MCA*LS$MCD,MCQ,MCP,MCT,MCG                 292
833                GATE  NU   MCQ,MCQ                                                              292
         MCV       BVARIABLE  LS$MCA*LS$MCD                                                        292
834                TEST  E    BV$MCV,1,MCP                                                         292
835      MCQ       QUEUE      MCQ                                                                  292
836                LINK       MCF,FIFO,MCF                                                         292
837      MCF       SEIZE      MCQ                                                                  292
838                LOGIC S    MCF                                                                  292
839                GATE  LR   MCF                                                                  292
840                DEPART     MCQ                                                                  292
841                RELEASE    MCQ                                                                  292
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843           TRANSFER    ,MCX                                                             292
844   MCP     LOGIC S     MCF                                                              292
845           TRANSFER    ,MCX                                                             292
846   MCH     PRIORITY    0,BUFFER                                                         292
847           PRIORITY    1                                                                292
848           PRIORITY    0,BUFFER                                                         292
849           PRIORITY    1                                                                292
850           GATE  LR    MCF,MCT                                                          292
851           TRANSFER    ,MCX                                                             292
852   MCT     LOGIC R     MCF                                                              292
853           TERMINATE                                                                    292
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855           ADVANCE     V$MCS                                                            293
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856           TEST  E     P1,1,SCH                                                         294
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857           TEST  E     BV$SCV,1,SCC                                                     294
858           TEST  LE    Q$LCR1,999,SCC                                                   294
859           SPLIT       1,SCA                                                            294
860           TRANSFER    ,SCL                                                             294
861   SCA     ASSIGN      1,0                                                              294
862           ASSIGN      2,0                                                              294
863           ASSIGN      3,0                                                              294
864           TRANSFER    ,SCR                                                             294
865   SCC     SPLIT       1,SCB                                                            294
866           TRANSFER    ,SCR                                                             294
867   SCB     ASSIGN      1,0                                                              294
868           ASSIGN      2,0                                                              294
869           ASSIGN      3,0                                                              294
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871   SCH     SPLIT       1,SCL                                                            294
872           TRANSFER    ,SCR                                                             294
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873   SCL     ADVANCE     V$SCX                                                            295
874           TRANSFER    ,MDR                                                             295
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      SCY     VARIABLE    (060*1000)/X3                                                    296
875   SCR     ADVANCE     V$SCY                                                            296
876           TRANSFER    ,TAA                                                             296
877   TAA     TEST  E     P2,1,TRA                                                         297
878           TABULATE    REC1                                                             298
879   TRA     TRANSFER    ,MBO                                                             299
      MERG1   MACRO       MCX,MCH,MDA,MDB,MDC,MDD,MDE,MDD,MDG,MDR                          300
880   MDR     LOGIC S     MDR                                                              300
881           GATE  LS    MDE,MDX                                                          300
882           LOGIC S     MDB                                                              300
883           GATE  LS    MDC                                                              300
884           TEST  E     P1,1,MDH                                                         300
885           LOGIC S     MDA                                                              300
886           PRIORITY    0,BUFFER                                                         300
887           PRIORITY    1                                                                300
888           PRIORITY    0,BUFFER                                                         300
889           PRIORITY    1                                                                300
```

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890        MDX    LOGIC R      MDD                                                        300
891               LOGIC R      MDA                                                        300
892               LOGIC R      MCB                                                        300
893               LOGIC R      MDC                                                        300
894               TRANSFER     ,MDG                                                       300
895        MDD    LOGIC S      MCE                                                        300
896               GATE  LS     MDR,MDX                                                    300
897               LOGIC S      MDC                                                        300
898               GATE  LS     MDB                                                        300
899               TEST  E      P1,1,TERM                                                  300
900               LOGIC S      MDD                                                        300
901               PRIORITY     0,BUFFER                                                   300
902               PRIORITY     1                                                          300
           MERG2  MACRO        MCX,MDH,MDF,MDV,BV$MDV,LS$MDA*LS$MDD,MDQ,MDP,MDT,MDG       301
903               GATE  NU     MDQ,MDQ                                                    301
           MDV    BVARIABLE    LS$MDA*LS$MDD                                              301
904               TEST  E      BV$MDV,1,MDP                                               301
905        MDQ    QUEUE        MDQ                                                        301
906               LINK         MDF,FIFO,MDF                                               301
907        MDF    SEIZE        MDQ                                                        301
908               LOGIC S      MDF                                                        301
909               GATE  LR     MDF                                                        301
910               DEPART       MDQ                                                        301
911               RELEASE      MDQ                                                        301
912               UNLINK       MDF,MDF,1                                                  301
913               TRANSFER     ,MDX                                                       301
914        MDP    LOGIC S      MDF                                                        301
915               TRANSFER     ,MDX                                                       301
916        MDH    PRIORITY     0,BUFFER                                                   301
917               PRIORITY     1                                                          301
918               PRIORITY     0,BUFFER                                                   301
919               PRIORITY     1                                                          301
920               GATE  LR     MDF,MDT                                                    301
921               TRANSFER     ,MDX                                                       301
922        MDT    LOGIC R      MDF                                                        301
923               TERMINATE                                                               301
924        MDG    ADVANCE      0                                                          301
           MERG3  MACRO        MDS,V$MDS,(267*1000)/X3                                    302
           MDS    VARIABLE     (267*1000)/X3                                              302
925               ADVANCE      V$MDS                                                      302
           ULST1  MACRO        UQH,UQQ,UQB,UQQ,Q$UQQ,V$UQQ,17,2000,35,FN$NORM*400         303
926        UQQ    TEST  E      P1,1,UQH                                                   303
927               TEST  E      P3,17,UQC                                                  303
928               TEST  L      Q$UQQ,35,UQO                                               303
929               QUEUE        UQQ                                                        303
930               SPLIT        1,UQH                                                      303
931               TEST  E      P2,1,UQB                                                   303
932               SEIZE        UQH                                                        303
           LQQ    VARIABLE     FN$NORM*400                                                303
933               ADVANCE      2000,V$UQQ                                                 303
934               LEAVE        IPS                                                        303
935               ASSIGN       2,0                                                        303
936               RELEASE      UQH                                                        303
           ULST2  MACRO        UQB,UQL,CH$UQB,V$UQL,FN$DECR,UQS,2500,1,FN$NORM*500        304
937               TEST  GE     CH$UQB,1,UQB                                               304
938               ASSIGN       3,FN$DECR                                                  304
939               TRANSFER     ,UQL                                                       304
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940      UQB    QUEUE       UQB                                                         304
941             LINK        UQB,FIFO,UQS                                                304
942      UQS    TEST   G    CH$UQB,1                                                    304
943             SEIZE       UQL                                                         304
944             DEPART      UQB                                                         304
         UQL    VARIABLE    FN$NORM*500                                                 304
945             ADVANCE     2500,V$UQL                                                  304
946             ENTER       IPS                                                         304
947             ASSIGN      2,1                                                         304
948             RELEASE     UQL                                                         304
949             UNLINK      UQB,UQS,1                                                   304
         ULST3  MACRO       UQL,UQI,UQO,UQH,UQT,V$UQT,UQQ,FN$DLCR,(325*1000)/X3         305
950             ASSIGN      3,FN$DLCR                                                   305
951      UQL    SEIZE       UQO                                                         305
952             LOGIC  S    UQI                                                         305
953             GATE   LR   UQI                                                         305
954             RELEASE     UQO                                                         305
955             DEPART      UQQ                                                         305
956             TRANSFER    ,UQO                                                        305
957      UQH    ASSIGN      1,0                                                         305
958             ASSIGN      2,0                                                         305
959             ASSIGN      3,0                                                         305
960             GATE   LR   UQI,UQT                                                     305
961             TRANSFER    ,UQO                                                        305
962      LQT    LOGIC  R    UQI                                                         305
963             TERMINATE                                                               305
         UQT    VARIABLE    (325*1000)/X3                                               305
964      UQO    ADVANCE     V$UQT                                                       305
         ULST1  MACRO       URH,URO,URB,URQ,Q$URQ,V$URQ,18,2000,35,FN$NORM*400          306
965      URQ    TEST   E    P1,1,URH                                                    306
966             TEST   E    P3,18,URO                                                   306
967             TEST   L    Q$URQ,35,URO                                                306
968             QUEUE       URQ                                                         306
969             SPLIT       1,URH                                                       306
970             TEST   E    P2,1,URB                                                    306
971             SEIZE       URH                                                         306
         URQ    VARIABLE    FN$NORM*400                                                 306
972             ADVANCE     2000,V$URQ                                                  306
973             LEAVE       IPS                                                         306
974             ASSIGN      2,0                                                         306
975             RELEASE     URH                                                         306
         ULST2  MACRO       URB,URL,CH$URB,V$URL,FN$DECR,URS,2500,1,FN$NORM*500         307
976             TEST   GE   CH$URB,1,URB                                                307
977             ASSIGN      3,FN$DECR                                                   307
978             TRANSFER    ,URL                                                        307
979      URB    QUEUE       URB                                                         307
980             LINK        URB,FIFO,URS                                                307
981      URS    TEST   G    CH$URB,1                                                    307
982             SEIZE       URL                                                         307
983             DEPART      URB                                                         307
         URL    VARIABLE    FN$NORM*500                                                 307
984             ADVANCE     2500,V$URL                                                  307
985             ENTER       IPS                                                         307
986             ASSIGN      2,1                                                         307
987             RELEASE     URL                                                         307
988             UNLINK      URB,URS,1                                                   307
         ULST3  MACRO       URL,URI,URO,URH,URT,V$URT,URQ,FN$DLCR,(325*1000)/X3         308
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989             ASSIGN     3,FN$DLCR                                                    308
990      URL    SEIZE      URO                                                          308
991             LOGIC S    URI                                                          308
992             GATE  LR   URI                                                          308
993             RELEASE    URO                                                          308
994             DEPART     URQ                                                          308
995             TRANSFER   ,URO                                                         308
996      URH    ASSIGN     1,0                                                          308
997             ASSIGN     2,0                                                          308
998             ASSIGN     3,0                                                          308
999             GATE  LR   URI,URT                                                      308
1000            TRANSFER   ,URO                                                         308
1001     URT    LOGIC R    URI                                                          308
1002            TERMINATE                                                               308
         URT    VARIABLE   (325*1000)/X3                                                308
1003     URO    ADVANCE    V$URT                                                        308
         ULST1  MACRO      USH,USO,USB,USQ,Q$USQ,V$USQ,19,2000,35,FN$NORM*400           309
1004     USQ    TEST  E    P1,1,USH                                                     309
1005            TEST  E    P3,19,USO                                                    309
1006            TEST  L    Q$USQ,35,USO                                                 309
1007            QUEUE      USQ                                                          309
1008            SPLIT      1,USH                                                        309
1009            TEST  E    P2,1,USB                                                     309
1010            SEIZE      USH                                                          309
         USQ    VARIABLE   FN$NORM*400                                                  309
1011            ADVANCE    2000,V$USQ                                                   309
1012            LEAVE      IPS                                                          309
1013            ASSIGN     2,0                                                          309
1014            RELEASE    USH                                                          309
         ULST2  MACRO      USB,USL,CH$USB,V$USL,FN$DECR,USS,2500,1,FN$NORM*500          310
1015            TEST  GE   CH$USB,1,USB                                                 310
1016            ASSIGN     3,FN$DECR                                                    310
1017            TRANSFER   ,USL                                                         310
1018     USB    QUEUE      USB                                                          310
1019            LINK       USB,FIFO,USS                                                 310
1020     USS    TEST  G    CH$USB,1                                                     310
1021            SEIZE      USL                                                          310
1022            DEPART     USB                                                          310
         USL    VARIABLE   FN$NORM*500                                                  310
1023            ADVANCE    2500,V$USL                                                   310
1024            ENTER      IPS                                                          310
1025            ASSIGN     2,1                                                          310
1026            RELEASE    USL                                                          310
1027            UNLINK     USB,USS,1                                                    310
         ULST3  MACRO      USL,USI,USO,USH,UST,V$UST,USQ,FN$DLCR,(193*1000)/X3          311
1028            ASSIGN     3,FN$DLCR                                                    311
1029     USL    SEIZE      USO                                                          311
1030            LOGIC S    USI                                                          311
1031            GATE  LR   USI                                                          311
1032            RELEASE    USO                                                          311
1033            DEPART     USQ                                                          311
1034            TRANSFER   ,USO                                                         311
1035     USH    ASSIGN     1,0                                                          311
1036            ASSIGN     2,0                                                          311
1037            ASSIGN     3,0                                                          311
1038            GATE  LR   USI,UST                                                      311
1039            TRANSFER   ,USO                                                         311
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1040      UST    LOGIC R     USI                                           311
1041             TERMINATE                                                 311
          UST    VARIABLE    (193*1000)/X3                                 311
1042      USC    ADVANCE     V$UST                                         311
          SPLT1  MACRO       SDL,SDR,SDH,SDA,SDC,SDB,SDV,P3'E'0,BV$SDV,36  312
1043             TEST  E     P1,1,SDH                                      312
          SDV    BVARIABLE   P3'E'0                                        312
1044             TEST  E     BV$SDV,1,SDC                                  312
1045             TEST  LE    Q$LCR1,36,SDC                                 312
1046             SPLIT       1,SDA                                         312
1047             TRANSFER    ,SDL                                          312
1048      SDA    ASSIGN      1,0                                           312
1049             ASSIGN      2,0                                           312
1050             ASSIGN      3,0                                           312
1051             TRANSFER    ,SDR                                          312
1052      SDC    SPLIT       1,SDB                                         312
1053             TRANSFER    ,SDR                                          312
1054      SDB    ASSIGN      1,0                                           312
1055             ASSIGN      2,0                                           312
1056             ASSIGN      3,0                                           312
1057             TRANSFER    ,SDL                                          312
1058      SDH    SPLIT       1,SDL                                         312
1059             TRANSFER    ,SDR                                          312
          SPLT2  MACRO       SDX,NTR,SDL,V$SDX,(313*1000)/X3               313
          SDX    VARIABLE    (313*1000)/X3                                 313
1060      SDL    ADVANCE     V$SDX                                         313
1061             TRANSFER    ,NTR                                          313
          SPLT3  MACRO       SDY,TAB,SDR,V$SDY,(142*1000)/X3               314
          SDY    VARIABLE    (142*1000)/X3                                 314
1062      SDR    ADVANCE     V$SDY                                         314
1063             TRANSFER    ,TAB                                          314
1064      TAB    TEST  E     P2,1,TRB                                      315
1065             TABULATE    REC2                                          316
1066      TRB    TRANSFER    ,MAR                                          317
1067             GENERATE    120000                                        318
1068             TERMINATE   1                                             319
                 START       1                                             320
                 RESET                                                     321
                 START       10,,2                                         322
                 END                                                       323
```

THIS IS SNAP 5 OF 5

RELATIVE CLOCK 1200000 ABSOLUTE CLOCK 1320000

BLOCK COUNTS

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
1	0	0	11	0	0	21	0	0	31	0	597	41	0	598
2	0	0	12	0	4007	22	0	0	32	0	597	42	0	598
3	0	0	13	0	4007	23	0	0	33	0	598	43	0	598
4	0	0	14	0	3410	24	0	4007	34	0	598	44	0	599
5	0	0	15	0	0	25	0	1194	35	0	598	45	0	599
6	0	0	16	0	0	26	0	597	36	0	598	46	0	599
7	0	0	17	0	0	27	0	597	37	1	598	47	0	599
8	0	15125	18	0	4007	28	0	597	38	0	598	48	0	599
9	0	4000	19	0	0	29	0	4007	39	0	598	49	3	4007
10	0	4000	20	0	0	30	0	3408	40	0	598	50	0	4006

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
51	0	4007	61	0	4007	71	0	598	81	0	636	91	0	647
52	0	4007	62	0	4007	72	0	598	82	0	636	92	0	9
53	0	4007	63	0	4007	73	0	598	83	0	636	93	0	638
54	0	4007	64	0	4007	74	0	598	84	0	636	94	0	638
55	0	4007	65	0	4007	75	0	13	85	0	2	95	0	4007
56	0	3360	66	0	4006	76	0	596	86	0	2	96	5	4007
57	0	3360	67	0	4006	77	0	596	87	0	647	97	0	4006
58	0	3360	68	0	4006	78	0	636	88	0	647	98	0	3997
59	0	3360	69	0	4007	79	1	636	89	0	647	99	0	134
60	0	3360	70	0	4007	80	0	636	90	0	647	100	0	134

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
101	0	268	111	0	26	121	1	26	131	0	143	141	0	151
102	0	134	112	0	26	122	0	132	132	0	11	142	0	114
103	0	108	113	0	26	123	1	132	133	0	132	143	0	114
104	0	108	114	0	26	124	0	132	134	0	132	144	0	115
105	0	108	115	0	26	125	0	132	135	5	4006	145	0	115
106	0	108	116	0	26	126	0	132	136	0	4007	146	0	115
107	0	108	117	0	26	127	0	132	137	0	3996	147	0	115
108	0	108	118	0	26	128	0	143	138	0	151	148	0	115
109	0	108	119	0	26	129	0	143	139	0	151	149	2	115
110	3	108	120	1	26	130	0	143	140	0	302	150	0	37

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
151	0	37	161	0	150	171	0	12	181	0	104	191	0	32
152	0	37	162	1	150	172	0	150	182	0	104	192	0	32
153	0	37	163	0	150	173	0	150	183	0	105	193	0	32
154	0	37	164	0	150	174	29	4007	184	0	105	194	1	32
155	0	37	165	0	150	175	0	4006	185	0	105	195	0	32
156	0	37	166	0	150	176	0	3994	186	0	105	196	0	32
157	0	37	167	0	162	177	0	137	187	0	105	197	0	32
158	0	37	168	0	162	178	0	137	188	0	105	198	0	32
159	1	37	169	0	162	179	0	274	189	0	33	199	2	32
160	0	37	170	0	162	180	0	137	190	0	33	200	0	136

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
201	1	136	211	0	136	221	0	87	231	0	53	241	0	138
202	0	136	212	0	136	222	0	87	232	0	53	242	0	138
203	0	136	213	21	4006	223	0	87	233	0	53	243	0	138
204	0	136	214	0	4006	224	0	87	234	0	53	244	0	138
205	0	136	215	0	3993	225	0	87	235	0	53	245	0	153
206	0	149	216	0	140	226	0	87	236	0	53	246	0	153
207	0	149	217	0	140	227	1	87	237	1	53	247	0	153
208	0	149	218	0	280	228	0	53	238	1	53	248	0	153
209	0	149	219	0	140	229	0	53	239	0	138	249	0	15
210	0	13	220	0	87	230	0	53	240	1	138	250	0	138

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
251	0	138	261	0	124	271	0	37	281	0	157	291	6	4006
252	23	4006	262	0	124	272	0	37	282	0	157	292	0	4006
253	0	4006	263	0	124	273	0	37	283	0	157	293	0	3985
254	0	3990	264	0	124	274	0	37	284	0	178	294	0	145
255	0	162	265	0	124	275	0	37	285	0	178	295	0	145
256	0	162	266	3	124	276	1	37	286	0	178	296	0	290
257	0	324	267	0	37	277	1	37	287	0	178	297	0	145
258	0	162	268	0	37	278	0	157	288	0	21	298	0	102
259	0	125	269	0	37	279	1	157	289	0	157	299	0	102
260	1	125	270	0	37	280	0	157	290	0	157	300	0	102

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
301	0	102	311	0	43	321	0	143	331	0	4007	341	0	118
302	0	102	312	0	43	322	0	143	332	0	3984	342	0	118
303	0	102	313	0	43	323	0	166	333	0	169	343	0	118
304	0	102	314	0	43	324	0	166	334	0	169	344	2	118
305	2	102	315	1	43	325	0	166	335	0	338	345	0	51
306	0	43	316	1	43	326	0	166	336	0	169	346	0	51
307	0	43	317	0	143	327	0	23	337	0	118	347	0	51
308	0	43	318	1	143	328	0	143	338	0	118	348	0	51
309	0	43	319	0	143	329	0	143	339	0	118	349	0	51
310	0	43	320	0	143	330	7	4006	340	0	118	350	0	51

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
351	0	51	361	0	168	371	0	3982	381	0	103	391	0	63
352	0	51	362	0	192	372	0	165	382	0	103	392	0	63
353	0	51	363	0	192	373	0	165	383	1	103	393	1	53
354	1	51	364	0	192	374	0	330	384	0	62	394	3	63
355	1	51	365	0	192	375	0	165	385	0	62	395	0	162
356	0	168	366	0	24	376	0	103	386	0	62	396	1	162
357	1	168	367	0	168	377	0	103	387	0	62	397	0	162
358	0	168	368	0	168	378	0	103	388	0	62	398	0	162
359	0	168	369	6	4007	379	0	103	389	0	62	399	0	162
360	0	168	370	0	4006	380	0	103	390	0	63	400	0	162

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
401	0	189	411	0	692	421	0	3287	431	0	4006	441	0	4006
402	0	189	412	0	1384	422	0	3287	432	0	4006	442	0	4006
403	0	189	413	0	692	423	0	3287	433	0	4006	443	0	4006
404	0	189	414	0	692	424	0	54	434	0	4006	444	0	4006
405	0	27	415	0	692	425	0	27	435	0	694	445	0	4006
406	0	162	416	0	692	426	11	4006	436	0	694	446	0	4006
407	0	162	417	0	692	427	0	4006	437	0	694	447	0	4006
408	4	4006	418	0	6574	428	3	4006	438	0	694	448	0	4006
409	0	4006	419	0	3287	429	0	4006	439	0	694	449	0	4006
410	0	3979	420	0	3287	430	0	4006	440	0	4006	450	0	255

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
451	0	255	461	0	66	471	0	3057	481	0	62	491	0	21
452	0	255	462	0	66	472	0	255	482	0	41	492	0	21
453	0	255	463	0	66	473	0	255	483	0	41	493	0	21
454	0	247	464	0	189	474	0	4006	484	0	41	494	0	21
455	0	66	465	0	189	475	19	4006	485	0	41	495	0	21
456	0	66	466	0	3312	476	0	4006	486	0	41	496	0	21
457	0	66	467	0	3312	477	0	961	487	0	41	497	0	21
458	0	66	468	0	3312	478	0	62	488	0	41	498	0	21
459	0	66	469	0	3312	479	0	62	489	0	41	499	1	21
460	0	66	470	0	3312	480	0	124	490	0	21	500	0	21

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
501	0	62	511	0	3045	521	0	40	531	0	23	541	0	53
502	0	62	512	0	62	522	0	40	532	0	23	542	0	64
503	0	62	513	0	62	523	0	40	533	0	23	543	0	64
504	0	62	514	4	4006	524	0	40	534	0	23	544	0	64

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
505	0	62	515	0	4006	525	0	40	535	0	23	545	0	64
506	0	62	516	0	963	526	0	40	536	0	23	546	0	3106
507	0	3107	517	0	64	527	0	40	537	0	23	547	0	3106
508	0	3107	518	0	63	528	0	40	538	1	23	548	0	3106
509	0	3107	519	0	126	529	0	23	539	0	23	549	0	3106
510	0	3107	520	0	63	530	0	23	540	0	63	550	0	3042
BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
551	0	54	561	0	35	571	0	19	581	0	54	591	0	54
552	0	64	562	0	35	572	0	19	582	0	54	592	3	4006
553	4	4006	563	0	35	573	0	19	583	0	54	593	0	4007
554	0	4006	564	0	35	574	0	19	584	0	54	594	0	970
555	0	967	565	0	35	575	0	19	585	0	3093	595	0	72
556	0	54	566	0	35	576	0	19	586	0	3093	596	0	71
557	0	54	567	0	35	577	1	19	587	0	3093	597	0	142
558	0	108	568	0	19	578	0	19	588	0	3093	598	0	71
559	0	54	569	0	19	579	0	54	589	0	3039	599	0	47
560	0	35	570	0	19	580	0	54	590	0	54	600	0	47
BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
601	0	48	611	0	24	621	0	72	631	11	4007	641	0	47
602	0	48	612	0	24	622	0	72	632	0	4006	642	0	47
603	0	48	613	0	24	623	0	72	633	0	975	643	0	47
604	0	48	614	0	24	624	0	3108	634	0	77	644	0	47
605	0	48	615	0	24	625	0	3108	635	0	76	645	0	47
606	0	48	616	1	24	626	0	3108	636	0	152	646	0	29
607	0	24	617	0	24	627	0	3108	637	0	76	647	0	29
608	0	24	618	0	72	628	0	3036	638	0	47	648	0	29
609	0	24	619	0	72	629	0	72	639	0	47	649	0	29
610	0	24	620	0	72	630	0	72	640	0	47	650	0	29
BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
651	0	29	661	0	76	671	0	4006	681	0	45	691	0	27
652	0	29	662	0	76	672	0	977	682	0	45	692	0	27
653	0	29	663	0	3107	673	0	72	683	0	45	693	0	27
654	0	29	664	0	3107	674	0	70	684	0	45	694	1	27
655	1	29	665	0	3107	675	0	140	685	0	25	695	0	27
656	0	29	666	0	3107	676	0	70	686	0	25	696	0	72
657	0	76	667	0	3031	677	0	45	687	0	26	697	0	72
658	0	76	668	0	76	678	0	45	688	0	26	698	0	72
659	0	76	669	0	76	679	0	45	689	0	26	699	0	72
660	0	76	670	4	4006	680	0	45	690	0	26	700	0	72
BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
701	0	72	711	0	982	721	0	52	731	0	23	741	0	3100
702	0	3099	712	0	77	722	0	52	732	0	23	742	0	3100
703	0	3099	713	0	75	723	0	52	733	1	23	743	0	3100
704	0	3099	714	0	150	724	0	23	734	0	23	744	0	3100
705	0	3099	715	0	75	725	0	23	735	0	75	745	0	3025
706	0	3027	716	0	52	726	0	23	736	0	75	746	0	75
707	0	72	717	0	52	727	0	23	737	0	75	747	0	75
708	0	72	718	0	52	728	0	23	738	0	75	748	16	4007
709	3	4006	719	0	52	729	0	23	739	0	75	749	0	4006
710	0	4007	720	0	52	730	0	23	740	0	75	750	0	981
BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
751	0	749	761	0	232	771	0	752	781	0	378	791	0	380
752	0	1498	762	0	232	772	0	752	782	0	378	792	0	380
753	0	749	763	0	232	773	0	752	783	0	378	793	1	380
754	0	749	764	0	6050	774	0	1504	784	0	377	794	0	380
755	0	749	765	0	3025	775	0	752	785	0	377	795	0	758
756	0	749	766	5	4006	776	0	377	786	0	379	796	0	758
757	0	749	767	0	4006	777	0	377	787	0	379	797	0	759
758	0	464	768	7	4006	778	0	378	788	0	379	798	0	759
759	0	232	769	0	4005	779	0	378	789	0	379	799	0	759
760	0	232	770	0	4006	780	0	378	790	0	380	800	0	759

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
801	0	4006	811	0	4006	821	0	4006	831	0	762	841	0	85
802	0	4006	812	0	4006	822	0	4006	832	0	762	842	0	85
803	0	4006	813	0	4005	823	0	4006	833	0	762	843	0	85
804	0	4006	814	0	4005	824	0	4006	834	0	739	844	0	679
805	0	3247	815	0	232	825	0	4006	835	0	83	845	0	679
806	0	759	816	0	232	826	0	4006	836	0	83	846	0	3774
807	0	759	817	0	232	827	0	4006	837	0	84	847	0	3774
808	12	4006	818	0	232	828	0	4006	838	0	84	848	0	3774
809	0	4006	819	0	232	829	0	4006	839	0	85	849	0	3774
810	0	4006	820	0	4006	830	0	762	840	0	85	850	0	3774

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
851	0	3010	861	0	748	871	0	6006	881	0	4006	891	0	4006
852	0	764	862	0	748	872	0	3003	882	1	4006	892	0	4006
853	0	764	863	0	748	873	8	4006	883	0	4006	893	0	4006
854	0	4006	864	0	748	874	0	4006	884	0	4006	894	0	4006
855	13	4006	865	0	510	875	3	4006	885	0	750	895	0	4006
856	0	4006	866	0	255	876	0	4006	886	0	750	896	0	4006
857	0	1003	867	0	255	877	0	4006	887	0	750	897	0	4006
858	0	748	868	0	255	878	0	158	888	0	750	898	0	4006
859	0	1496	869	0	255	879	0	4006	889	0	750	899	0	4006
860	0	748	870	0	255	880	0	4006	890	0	4006	900	0	3285

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
901	0	3285	911	0	3211	921	0	28	931	0	72	941	0	34
902	0	3285	912	0	3211	922	0	3228	932	0	38	942	0	34
903	0	3285	913	0	3211	923	0	3228	933	0	38	943	0	34
904	0	34	914	0	17	924	0	4006	934	0	38	944	0	34
905	0	3268	915	0	17	925	12	4006	935	0	38	945	0	34
906	0	3268	916	0	3256	926	0	4007	936	0	38	946	0	34
907	0	3211	917	0	3256	927	0	3977	937	0	38	947	0	34
908	1	3211	918	0	3256	928	0	72	938	0	38	948	0	34
909	0	3211	919	0	3256	929	0	72	939	0	38	949	1	34
910	0	3211	920	0	3256	930	0	144	940	0	34	950	2	34

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
951	0	70	961	0	33	971	0	46	981	0	35	991	1	80
952	1	70	962	0	69	972	0	46	982	0	35	992	0	79
953	0	69	963	0	69	973	0	46	983	0	35	993	0	79
954	0	69	964	16	4007	974	0	46	984	0	35	994	0	79
955	0	69	965	0	4006	975	0	46	985	0	36	995	0	79
956	0	69	966	0	3967	976	0	46	986	0	36	996	0	120
957	0	102	967	0	81	977	0	46	987	0	36	997	0	120
958	0	102	968	0	81	978	2	46	988	1	36	998	0	120
959	0	102	969	0	162	979	0	35	989	0	36	999	0	120
960	0	102	970	0	81	980	0	35	990	0	80	1000	0	41

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
1001	0	79	1011	0	27	1021	0	47	1031	0	73	1041	0	73
1002	0	79	1012	0	27	1022	0	47	1032	0	73	1042	10	4007
1003	15	4006	1013	0	27	1023	0	47	1033	0	73	1043	0	4006
1004	0	4007	1014	0	27	1024	0	48	1034	0	73	1044	0	3959
1005	0	3954	1015	0	27	1025	0	48	1035	0	116	1045	0	3401
1006	0	73	1016	0	27	1026	0	48	1036	0	116	1046	0	1194
1007	0	73	1017	1	27	1027	1	48	1037	0	116	1047	0	597
1008	0	146	1018	0	46	1028	0	48	1038	0	115	1048	0	597
1009	0	73	1019	0	45	1029	0	74	1039	0	43	1049	0	597
1010	0	27	1020	0	47	1030	1	74	1040	0	73	1050	0	597

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
1051	0	597	1061	0	4007									
1052	0	6724	1062	6	4006									
1053	0	3362	1063	0	4007									
1054	0	3362	1064	0	4007									

1055	0	3362	1065	0	354
1056	0	3362	1066	0	4007
1057	0	3362	1067	0	10
1058	0	94	1068	0	10
1059	0	47			
1060	14	4006			

USER CHAIN	TOTAL ENTRIES	AVERAGE TIME/TRANS	CURRENT CONTENTS	AVERAGE CONTENTS	MAXIMUM CONTENTS
LCH	635	76435.312	37	40.447	49
MAF	637	14715.570	12	7.811	52
UAB	27	46452.109	1	1.045	3
UBB	38	33656.050	1	1.065	3
UCB	35	36299.199	3	1.058	3
UDB	54	24330.218	1	1.094	3
UEB	38	33540.234	1	1.062	3
UFB	44	29287.203	1	1.073	3
UGB	52	25216.613	1	1.092	4
UHB	64	20988.765	1	1.119	4
MBF	8	150.000		.000	1
UIB	22	57106.589	1	1.046	3
UJB	24	52664.707	1	1.053	4
UKB	20	62443.097	1	1.040	2
ULB	25	50614.878	1	1.054	3
UMB	30	42445.632	1	1.061	3
UNB	28	45602.890	1	1.064	4
UOB	24	52507.582	1	1.050	3
UPB	381	19270.898	1	6.118	32
MCF	24	60.625		.001	1
MDF	3252	18859.996	58	51.110	71
UQB	35	36844.054	1	1.074	3
URB	37	34907.726	1	1.076	3
USB	49	27100.753	1	1.106	3

FACILITY	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN	SEIZING TRANS. NO.	PREEMPTING TRANS. NO.
LCR1	1.000	599	2003.338	431	
LCH1	.076	599	153.505		
MAQ	.986	637	1857.466	116	
UAH	.359	108	3990.925		
UAL	.044	26	2042.269		
UAC	.967	133	8725.304	91	
UBH	.382	115	3995.773		
UBL	.061	37	1998.053		
UBC	.970	151	7711.085	31	
UCH	.346	105	3959.856		
UCL	.054	33	1971.272	226	
UCO	.952	137	8346.195	444	
UDH	.288	87	3984.287		
UDL	.088	53	1996.811		
UDO	.971	139	8389.558	381	
UEH	.415	125	3985.575	237	
UEL	.061	37	2008.540		
UEO	.963	158	7318.472	179	
UFH	.339	102	3998.813		
UFL	.071	43	1983.906		
UFO	.937	144	7810.539	136	
UGH	.391	118	3982.872		
UGL	.086	51	2034.293		
UGO	.948	169	6734.558	297	
UHH	.345	103	4023.630		
UHL	.102	63	1956.000		
UHO	.921	163	6787.605	145	
MBQ	.026	66	485.621		
UIH	.171	41	5023.386		
UIL	.043	21	2499.666		
UIO	.019	62	368.838		
UJH	.167	40	5014.324		
UJL	.046	23	2412.912		
UJO	.027	64	508.187		
UKH	.143	35	4931.425		
UKL	.040	19	2558.578		
UKO	.013	54	309.277		
ULH	.197	48	4944.250		
ULL	.050	24	2548.416		
ULO	.018	72	307.694		
UMH	.195	47	4988.273		
UML	.059	29	2474.275		
UMO	.019	76	300.355		
UNH	.188	45	5038.843		
UNL	.054	27	2413.444		
UNO	.019	72	331.930		
UOH	.213	52	4916.730		
UOL	.050	23	2609.695		
UOO	.020	75	328.773		
UPH	.314	378	997.751		
UPL	.635	380	2006.581		
UPO	.102	759	162.379		
MCQ	.023	85	334.529		
MDQ	.977	3212	365.308	459	
UQH	.064	38	2025.447		
UQL	.071	34	2529.029		
UQO	.958	70	16437.511	514	
URH	.076	46	1986.021		
URL	.072	36	2414.222		
URO	.964	80	14467.074	466	
USH	.045	27	2044.407		

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      USL           .098               48        2463.916
    . USO           .952               74       15449.023          457

LOGIC SWITCH - SET (ON) STATUS
SWITCH     NR     NR     NR     NR     NR     NR     NR     NR     NR     NR     NR     NR     NR     NR     NR
          MAR    MAE    MAF    UAI    UBI    UCI    UDI    UEI    UFI    UGI    UHI    MBR    MBE    19     MCR    MCE
          MDR    MDE    MDB    MDF    UQI    URI    USI
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STORAGE	CAPACITY	AVERAGE CONTENTS	AVERAGE UTILIZATION	ENTRIES	AVERAGE TIME/TRAN	CURRENT CONTENTS	MAXIMUM CONTENTS
IPS	380	63.957	.168	1722	44569.457	63	131

QUEUE	MAXIMUM CONTENTS	AVERAGE CONTENTS	TOTAL ENTRIES	ZERO ENTRIES	PERCENT ZEROS	AVERAGE TIME/TRANS	$AVERAGE TIME/TRANS	TABLE NUMBER	CURRENT CONTENTS
LCR1	49	40.447	635		.0	76435.312	76435.312		37
MAQ	53	8.797	649		.0	16266.601	16266.601		13
UAQ	9	5.849	139		.0	50496.644	50496.644		7
UAB	3	2.000	28		.0	85753.812	85753.812		2
UBQ	8	5.454	155		.0	42227.972	42227.972		5
UBB	3	2.004	39		.0	61666.714	61666.714		2
UCQ	8	5.195	143		.0	43598.031	43598.031		7
UCB	3	2.004	35		.0	68726.250	68726.250		3
UDQ	10	6.370	143		.0	53460.320	53460.320		5
UDB	3	2.006	55		.0	43781.835	43781.835		2
UEQ	9	6.367	165		.0	46312.277	46312.277		8
UEB	3	2.000	39		.0	61543.921	61543.921		2
UFQ	7	5.180	149		.0	41724.132	41724.132		6
UFB	3	2.002	45		.0	53407.308	53407.308		2
UGQ	10	6.123	174		.0	42228.992	42228.992		6
UGB	4	2.006	53		.0	45424.808	45424.808		2
UHQ	8	5.045	169		.0	35829.000	35829.000		7
UHB	4	2.016	64		.0	37813.328	37813.328		2
MBQ	2	.027	66		.0	503.802	503.802		
UIQ	5	2.251	64		.0	42219.218	42219.218		2
UIB	3	2.003	23		.0	104515.250	104515.250		2
UJQ	5	2.269	66		.0	41261.589	41261.589		2
UJB	4	2.007	25		.0	96338.187	96338.187		2
UKQ	5	2.211	56		.0	47394.945	47394.945		2
UKB	3	2.000	21		.0	114297.562	114297.562		2
ULQ	5	2.300	74		.0	37302.160	37302.160		2
ULB	3	2.003	26		.0	92469.562	92469.562		2
UMQ	5	2.296	78		.0	35325.035	35325.035		2
UMB	3	2.001	31		.0	77471.437	77471.437		2
UNQ	5	2.283	74		.0	37033.984	37033.984		2
UNB	4	2.009	28		.0	86132.750	86132.750		2
UOQ	5	2.320	77		.0	36170.347	36170.347		2
UOB	3	2.000	25		.0	96006.312	96006.312		2
UPQ	37	8.063	761		.0	12715.593	12715.593		2
UPB	32	6.483	381		.0	20419.191	20419.191		2
MCQ	2	.024	85		.0	351.646	351.646		
MDQ	72	52.088	3270		.0	19115.007	19115.007		59
UQQ	6	4.866	74		.0	78917.812	78917.812		5
UQB	3	2.002	36		.0	66765.375	66765.375		2
URQ	6	4.890	84		.0	69868.750	69868.750		5
URB	3	2.003	37		.0	64991.187	64991.187		2
USQ	6	3.948	77		.0	61528.441	61528.441		4
USB	3	2.008	49		.0	49176.917	49176.917		2

$AVERAGE TIME/TRANS = AVERAGE TIME/TRANS EXCLUDING ZERO ENTRIES

TABLE REC1

ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS	
158	12.531	1.933	1980.000	NON-WEIGHTED

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	.00	.0	100.0	-.000	-6.481
1	0	.00	.0	100.0	.079	-5.963
2	0	.00	.0	100.0	.159	-5.446
3	0	.00	.0	100.0	.239	-4.929
4	0	.00	.0	100.0	.319	-4.412
5	0	.00	.0	100.0	.398	-3.895
6	0	.00	.0	100.0	.478	-3.377
7	0	.00	.0	100.0	.558	-2.860
8	0	.00	.0	100.0	.638	-2.343
9	15	9.49	9.4	90.5	.718	-1.826
10	16	10.12	19.6	80.3	.797	-1.309
11	16	10.12	29.7	70.2	.877	-.792
12	24	15.18	44.9	55.0	.957	-.274
13	28	17.72	62.6	37.3	1.037	.242
14	28	17.72	80.3	19.6	1.117	.759
15	31	19.62	100.0	.0	1.196	1.276

REMAINING FREQUENCIES ARE ALL ZERO

TABLE REC2

ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS	
354	5.158	3.125	1826.000	NON-WEIGHTED

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	.00	.0	100.0	-.000	-1.650
1	39	11.01	11.0	88.9	.193	-1.330
2	45	12.71	23.7	76.2	.387	-1.010
3	38	10.73	34.4	65.5	.581	-.690
4	40	11.29	45.7	54.2	.775	-.370
5	39	11.01	56.7	43.2	.969	-.050
6	40	11.29	68.0	31.9	1.163	.269
7	41	11.58	79.6	20.3	1.357	.589
8	40	11.29	90.9	9.0	1.550	.909
9	5	1.41	92.3	7.6	1.744	1.229
10	7	1.97	94.3	5.6	1.938	1.549
11	4	1.12	95.4	4.5	2.132	1.869
12	3	.84	96.3	3.6	2.326	2.189
13	2	.56	96.8	3.1	2.520	2.509
14	5	1.41	98.3	1.6	2.714	2.829
15	6	1.69	100.0	.0	2.907	3.149

REMAINING FREQUENCIES ARE ALL ZERO

APPENDIX B

SOURCE LISTING AND COMPUTER OUTPUT FOR SECOND MODEL SIMULATION

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                    ***     G P S S / 3 6 0 / O S   V E R S I O N   1   * * *
                          *** IBM PROGRAM NUMBER 360A-CS-17X (V1M4) ***
REALLOCATE XAC,1300,BLO,1200,FAC,100,STO,1,QUE,100,LOG,100                                    1
REALLOCATE TAB,5,FUN,12,VAR,75,FSV,5,HSV,5,CHA,30,GRP,1,BVR,10                                2
REALLOCATE FMS,1,HMS,1,COM,75000                                                              3
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BLOCK                                                                            CARD
NUMBER  *LOC    OPERATION   A,B,C,D,E,F,G            COMMENTS                    NUMBER
                SIMULATE                                                              4
        ULST1   STARTMACRO                                                            5
        #D      TEST   E    P1,1,#A                                                   6
                TEST   E    P3,#G,#B                                                  7
                TEST   L    #E,#I,#B                                                  8
                QUEUE       #D                                                        9
                SPLIT       1,#A                                                     10
                TEST   E    P2,1,#C                                                  11
                SEIZE       #A                                                       12
        #D      VARIABLE    #J                                                       13
                ADVANCE     #H,#F                                                    14
                LEAVE       IPS                                                      15
                ASSIGN      2,0                                                      16
                DEPART      #D                                                       17
                RELEASE     #A                                                       18
                ENDMACRO                                                             19
        ULST2   STARTMACRO                                                           20
                TRANSFER    ,#B                                                      21
                TEST   GE   #C,#H,#A                                                 22
                ASSIGN      3,#E                                                     23
                TRANSFER    ,#B                                                      24
        #A      QUEUE       #A                                                       25
                DEPART      #A                                                       26
                TRANSFER    ,#B                                                      27
                LINK        #A,FIFO,#F                                               28
        #F      TEST   G    #C,#H                                                    29
                SEIZE       #B                                                       30
        #B      VARIABLE    #I                                                       31
                ADVANCE     #G,#D                                                    32
                ENTER       IPS                                                      33
                ASSIGN      2,1                                                      34
                RELEASE     #B                                                       35
                UNLINK      #A,#F,1                                                  36
                ENDMACRO                                                             37
        ULST3   STARTMACRO                                                           38
                ASSIGN      3,#H                                                     39
        #A      SEIZE       #C                                                       40
                LOGIC  S    #B                                                       41
                GATE   LR   #B                                                       42
                RELEASE     #C                                                       43
                TRANSFER    ,#C                                                      44
        #D      ASSIGN      1,0                                                      45
                ASSIGN      2,0                                                      46
                ASSIGN      3,0                                                      47
                GATE   LR   #B,#E                                                    48
                TRANSFER    ,#C                                                      49
        #E      LOGIC  R    #B                                                       50
                TERMINATE                                                            51
        #F      VARIABLE    #I                                                       52
        #C      ADVANCE     #F                                                       53
                ENDMACRO                                                             54
        NORM    FUNCTION    RN1,C31                                                  55
       0,-5.00/.00023,-3.50/.00058,-3.25/.00135,-3.00/.00300,-2.75/                  56
       .00620,-2.50/.01220,-2.25/.02280,-2.00/.04010,-1.75/.06680,-1.50/             57
```

```
      .10570,-1.25/.15870,-1.00/.22660,-0.75/.30850,-0.50/.40130,-0.25/
      .50000,0.00/.59870,0.25/.69150,0.50/.77340,0.75/.84130,1.00/
      .89440,1.25/.93320,1.50/.95990,1.75/.97730,2.00/.98780,2.25/
      .99380,2.50/.99700,2.75/.99865,3.00/.99942,3.25/.99977,3.50/1.0,5.00
       DLCP  FUNCTION   RN1,D2
      .70,1/1.0,2
       REC1  TABLE      P3,0,1,5
             INITIAL    X1,1200
             INITIAL    X3,10
       IPS   STORAGE    1200
           1 VARIABLE   500/X3
1            GENERATE   V1,,,X1,,3
2            QUEUE      CARS
3            SEIZE      CAR
4            GATE LS    20
5            LOGIC R    20
6            DEPART     CARS
7            RELEASE    CAR
8      TERM  TERMINATE
9            GENERATE   V1,,,,1,3
10           GATE LR    19,TERM
11           TRANSFER   ,BEGN
12     NTR   LOGIC S    19
13     BEGN  TEST E     P1,0,SKIP
14           TEST G     Q$CARS,0,SKIP
15           TEST LE    Q$LCR1,35,BYPS
16           LOGIC S    20
17           ASSIGN     1,1
18     SKIP  TRANSFER   ,LST1
19     BYPS  LOGIC S    20
20           SPLIT      1,LHO1
21           ASSIGN     1,1
22           ASSIGN     3,0
23           TRANSFER   ,LSZ1
24     LST1  TEST E     P1,1,LHK1
25           SPLIT      1,LEC1
26     LHO1  ASSIGN     1,0
27           ASSIGN     2,0
28           ASSIGN     3,0
29     LHK1  GATE LR    3,LTH1
30           TRANSFER   ,LSO1
31     LEC1  QUEUE      LCR1
32           LINK       LCH,FIFO,LFA1
33     LFA1  SEIZE      LCR1
34           DEPART     LCR1
35           TEST E     P2,0,LDC1
36           ENTER      IPS
       LVB1  VARIABLE   FN$NORM*10
37           ADVANCE    40,V$LVB1
38           ASSIGN     2,1
39           ASSIGN     3,FN$DLCP
40     LDC1  RELEASE    LCR1
41           UNLINK     LCH,LFA1,1
42     LSZ1  SEIZE      LCH1
43           LOGIC S    3
44           GATE LR    3
45           RELEASE    LCH1
```

```
46                TRANSFER    ,LS01                                                        115
47       LTHI     LOGIC R     3                                                            116
48                TERMINATE                                                                117
         LAV1     VARIABLE    (360*1000)/X3                                                118
49       LS01     ADVANCE     V$LAV1                                                       119
         ULST1    MACRO       UAA,UAB,UAC,UAD,Q$UAD,V$UAD,1,60,2,FN$NORM*10                120
50       UAD      TEST   E    P1,1,UAA                                                     120
51                TEST   E    P3,1,UAB                                                     120
52                TEST   L    Q$UAD,2,UAB                                                  120
53                QUEUE       UAD                                                          120
54                SPLIT       1,UAA                                                        120
55                TEST   E    P2,1,UAC                                                     120
56                SEIZE       UAA                                                          120
         UAD      VARIABLE    FN$NORM*10                                                   120
57                ADVANCE     60,V$UAD                                                     120
58                LEAVE       IPS                                                          120
59                ASSIGN      2,0                                                          120
60                DEPART      UAD                                                          120
61                RELEASE     UAA                                                          120
         ULST2    MACRO       UAC,UAE,CH$UAC,V$UAE,0,UAF,0,0,0                             121
62                TRANSFER    ,UAE                                                         121
63                TEST   GE   CH$UAC,0,UAC                                                 121
64                ASSIGN      3,0                                                          121
65                TRANSFER    ,UAE                                                         121
66       UAC      QUEUE       UAC                                                          121
67                DEPART      UAC                                                          121
68                TRANSFER    ,UAE                                                         121
69                LINK        UAC,FIFO,UAF                                                 121
70       UAF      TEST   G    CH$UAC,0                                                     121
71                SEIZE       UAE                                                          121
         UAE      VARIABLE    0                                                            121
72                ADVANCE     0,V$UAE                                                      121
73                ENTER       IPS                                                          121
74                ASSIGN      2,1                                                          121
75                RELEASE     UAE                                                          121
76                UNLINK      UAC,UAF,1                                                    121
         ULST3    MACRO       UAE,UAG,UAB,UAA,UAH,V$UAH,JAD,0,(120*1000)/X3                122
77                ASSIGN      3,0                                                          122
78       UAE      SEIZE       UAB                                                          122
79                LOGIC S     UAG                                                          122
80                GATE   LR   UAG                                                          122
81                RELEASE     UAB                                                          122
82                TRANSFER    ,UAB                                                         122
83       UAA      ASSIGN      1,0                                                          122
84                ASSIGN      2,0                                                          122
85                ASSIGN      3,0                                                          122
86                GATE   LR   UAG,UAH                                                      122
87                TRANSFER    ,UAB                                                         122
88       UAH      LOGIC R     UAG                                                          122
89                TERMINATE                                                                122
         UAH      VARIABLE    (120*1000)/X3                                                122
90       UAB      ADVANCE     V$UAH                                                        122
         ULST1    MACRO       UBA,UBB,UBC,UBD,Q$UBD,V$UBD,2,140,2,FN$NORM*20               123
91       UBD      TEST   E    P1,1,UBA                                                     123
92                TEST   E    P3,2,UBB                                                     123
93                TEST   L    Q$UBD,2,UBB                                                  123
94                QUEUE       UBD                                                          123
```

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95              SPLIT       1,UBA                                            123
96              TEST  E     P2,1,UBC                                         123
97              SEIZE       UBA                                              123
         UBD    VARIABLE    FN$NORM*20                                       123
98              ADVANCE     140,V$UBD                                        123
99              LEAVE       IPS                                              123
100             ASSIGN      2,0                                              123
101             DEPART      UBD                                              123
102             RELEASE     UBA                                              123
         ULST2  MACRO       UBC,UBE,CH$UBC,V$UBE,0,UBF,0,0,0                 124
103             TRANSFER    ,UBE                                             124
104             TEST  GE    CH$UBC,0,UBC                                     124
105             ASSIGN      3,0                                              124
106             TRANSFER    ,UBE                                             124
107      UBC    QUEUE       UBC                                              124
108             DEPART      UBC                                              124
109             TRANSFER    ,UBE                                             124
110             LINK        UBC,FIFO,UBF                                     124
111      UBF    TEST  G     CH$UBC,0                                         124
112             SEIZE       UBE                                              124
         UBE    VARIABLE    0                                                124
113             ADVANCE     0,V$UBE                                          124
114             ENTER       IPS                                              124
115             ASSIGN      2,1                                              124
116             RELEASE     UBE                                              124
117             UNLINK      UBC,UBF,1                                        124
         ULST3  MACRO       UBE,UBG,UBB,UBA,UBH,V$UBH,UBD,0,(120*1000)/X3    125
118             ASSIGN      3,0                                              125
119      UBE    SEIZE       UBB                                              125
120             LOGIC S     UBG                                              125
121             GATE  LR    UBG                                              125
122             RELEASE     UBB                                              125
123             TRANSFER    ,UBB                                             125
124      UBA    ASSIGN      1,0                                              125
125             ASSIGN      2,0                                              125
126             ASSIGN      3,0                                              125
127             GATE  LR    UBG,UBH                                          125
128             TRANSFER    ,UBB                                             125
129      UBH    LOGIC R     UBG                                              125
130             TERMINATE                                                    125
         UBH    VARIABLE    (120*1000)/X3                                    125
131      UBB    ADVANCE     V$UBH                                            125
132             TEST  E     P2,1,TRA                                         126
133             TABULATE    REC1                                             127
134      TRA    TRANSFER    ,NTR                                             128
135             GENERATE    60000                                            129
136             TERMINATE   1                                                130
                START       1                                                131
                RESET                                                        132
                START       8,,2                                             133
                END                                                          134
```

THIS IS SNAP 4 OF 4

RELATIVE CLOCK 480000 ABSOLUTE CLOCK 540000

BLOCK COUNTS

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
1	0	1	11	0	0	21	0	0	31	0	9552	41	0	9552
2	0	1	12	0	9600	22	0	0	32	0	9552	42	0	9552
3	0	1	13	0	9600	23	0	0	33	0	9552	43	1	9552
4	0	1	14	0	49	24	0	9600	34	0	9552	44	0	9552
5	0	1	15	0	1	25	0	19104	35	0	9552	45	0	9552
6	0	1	16	0	1	26	0	9552	36	0	8808	46	0	9552
7	0	1	17	0	1	27	0	9552	37	1	8808	47	0	9552
8	0	9601	18	0	9600	28	0	9552	38	0	8808	48	0	9552
9	0	9600	19	0	0	29	0	9600	39	0	8808	49	720	9600
10	0	9600	20	0	0	30	0	48	40	0	9552	50	0	9600

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
51	0	9554	61	0	6238	71	0	0	81	0	6238	91	0	9600
52	0	6431	62	0	6238	72	0	0	82	0	6238	92	0	9555
53	0	6238	63	0	0	73	0	0	83	0	6284	93	0	3134
54	0	12476	64	0	0	74	0	0	84	0	6284	94	0	2573
55	0	6238	65	0	0	75	0	0	85	0	6284	95	0	5146
56	0	6238	66	0	0	76	0	0	86	0	6284	96	0	2573
57	1	6238	67	0	0	77	0	0	87	0	46	97	0	2573
58	0	6238	68	0	0	78	0	6238	88	0	6238	98	1	2573
59	0	6238	69	0	0	79	1	6238	89	0	6238	99	0	2573
60	0	6238	70	0	0	80	0	6238	90	240	9600	100	0	2573

BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL	BLOCK	CURRENT	TOTAL
101	0	2573	111	0	0	121	0	2573	131	240	9600			
102	0	2573	112	0	0	122	0	2573	132	0	9600			
103	0	2573	113	0	0	123	0	2573	133	0	744			
104	0	0	114	0	0	124	0	2618	134	0	9600			
105	0	0	115	0	0	125	0	2618	135	0	8			
106	0	0	116	0	0	126	0	2618	136	0	8			
107	0	0	117	0	0	127	0	2618						
108	0	0	118	0	0	128	0	45						
109	0	0	119	0	2573	129	0	2573						
110	0	0	120	1	2573	130	0	2573						

FACILITY	AVERAGE UTILIZATION	NUMBER ENTRIES	AVERAGE TIME/TRAN	SEIZING TRANS. NO.	PREEMPTING TRANS. NO.
CAR	.000	1	50.000		
LCR1	.733	9553	36.860	1138	
LCH1	.862	9553	43.315	1132	
UAA	.778	6239	59.907	393	
UAB	.781	6239	60.146	415	
UBA	.750	2574	139.898	1131	
UBB	.714	2574	133.166	158	

STCRAGE	CAPACITY	AVERAGE CONTENTS	AVERAGE UTILIZATION	ENTRIES	AVERAGE TIME/TRAN	CURRENT CONTENTS	MAXIMUM CONTENTS
IPS	1200	822.048	.685	9629	40978.644	818	846

TABLE REC1

ENTRIES IN TABLE	MEAN ARGUMENT	STANDARD DEVIATION	SUM OF ARGUMENTS	
744	1.740	.438	1295.000	NON-WEIGHTED

UPPER LIMIT	OBSERVED FREQUENCY	PER CENT OF TOTAL	CUMULATIVE PERCENTAGE	CUMULATIVE REMAINDER	MULTIPLE OF MEAN	DEVIATION FROM MEAN
0	0	.00	.0	100.0	-.000	-3.969
1	193	25.94	25.9	74.0	.574	-1.689
2	551	74.05	100.0	.0	1.149	.591

REMAINING FREQUENCIES ARE ALL ZERO

VITA

Robert Lee Gourley

Candidate for the Degree of

Doctor of Philosophy

Thesis: A MODULAR GENERAL PURPOSE APPROACH TO THE SIMULATION OF CONSTANT SPEED DISCRETELY SPACED RECIRCULATING CONVEYOR SYSTEMS

Major Field: Industrial Engineering

Biographical:

Personal Data: Born in Jonesboro, Arkansas, October 17, 1946, the son of MSG (Ret.) and Mrs. Robert L. Gourley.

Education: Graduated from Lawton Senior High School, Lawton, Oklahoma, in May, 1964; received Bachelor of Science degree in Electrical Engineering from Oklahoma State University in 1969; received Master of Science degree in Industrial Engineering and Management from Oklahoma State University in 1972; completed requirements for the Doctor of Philosophy degree at Oklahoma State University in December, 1973.

Professional Experience: Project Engineer, United States Army Security Agency, 1969-1970; graduate teaching assistant, Oklahoma State University, School of Industrial Engineering and Management, 1970-1973.