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Analysis of Local Anti-Islanding Detection Methods for Photovoltaic Generators in Distribution Systems

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ANALYSIS OF LOCAL ANTI-ISLANDING DETECTION METHODS FOR PHOTOVOLTAIC GENERATORS IN DISTRIBUTION SYSTEMS

by

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In the current decade, technology innovations and cost reduction of inverter-based Distributed Energy Resources (DERs) have led to higher integration of distributed energy storage and photovoltaic (PV) solar power systems. Increasing growth in PV penetration to the distribution system can raise operational and safety concerns especially in case of an unintended islanding.

In general, standards require distributed generators (DGs) to detect islanding from the main grid and cease to energize the local system. Multiple methods have been introduced in the literature to detect these islands reliably and quickly. In order to connect an inverter to distribution system, inverter should pass certain certification tests such as UL 1741 certification test. The anti-islanding test in UL 1741 standard tests only one type of load over a limited range of loading conditions with a single inverter and lumped load and no impedances in between them. The overall goal of this thesis is to determine those parameters to which run-on times (ROTs) are relatively insensitive and thus do not need to be emphasized in certification testing or risk of islanding studies. This thesis presents a generic MATLAB Simulink inverter model and studies sensitivity of anti-islanding tests to parameters such as inverter location, inverter operating point, load location, load type and circuit impedance. Inverters in these studies are equipped with Group 2A and Group

2B anti-islanding methods. The key contributions in this thesis can be summarized as follows:

- A comprehensive review of anti-islanding techniques in the literature.
- An anti-islanding detection model was developed in MATLAB software with at least one method from different groups of anti-islanding methods; the model can be used further for industrial applications and research purposes.
- The result of analyses indicated that the level of phase-phase imbalance, constant-power load, harmonic-current load and irradiance level have a low or negligible impact on anti-islanding and can be omitted from these studies. These findings are expected to lower the cost and improve the speed of these studies, in large distribution systems.

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LIST OF ABBREVIATION

AFD	Active Frequency Drift Anti-islanding method
AI	Anti-Islanding
Hz	Hertz (Cycles per second)
IDM	Islanding Detection Method
IEEE	Institute for Electrical and Electronics Engineers
Islanding:	Islanding is a condition in which a portion of the utility system, which contains both load and generation, is isolated from the remainder of the utility system and continues to operate via a photovoltaic power source.
MPPT	Maximum Power Point Tracking
NDZ	Non-detection zone. None detection zone is the range of loads inside a potential island that an AI detection method can fail to identify islanding.
OFP	Over Frequency Protection Device or Method
OVP	Over Voltage Protection Device or Method
POI	Point of interconnection
PCC	Point of Common Coupling

PJD	Phase Jump Detection Anti-islanding method
PLCC	Power-line Carrier Communications
PLL	Phase Lock Loop
QF	Quality Factor of a Resistor, Inductor, Capacitor in a parallel (RLC) Circuit is defined as: $Q = R\sqrt{\frac{C}{L}}$ It describes relative amounts of energy storage and energy dissipation in RLC load.
RPS	Renewable Portfolio standard is a regulation that requires the increased production of energy from renewable energy sources, such as wind, solar, biomass, and geothermal.
ROT	Run-on Time, time between the moment of creation of an island and inverter's shut down.
ROCOF	Rate of Change of Frequency
SCADA	Supervisory Control and Data Acquisition
SFS	Sandia Frequency Shift Anti-islanding method
SMS	Slip Mode Phase Shift Anti-islanding method
SVS	Sandia Voltage Shift Anti-islanding method
THD	Total Harmonic Distortion

UFP	Under Frequency Protection Device or Method
UL 1741 SA	Underwriters Laboratories 1741, is an inverter certification standard. [1]
UVP	Under Voltage Protection Device or Method
VCO	Voltage Controlled Oscillator

CHAPTER 1 INTRODUCTION

The traditional architecture of power grid was based on the large power plants operating at a remote location from customer loads. In a hierarchical structure, the power transfers from conventional generation units through transmission lines and distribution system to the electricity consumers. Historically, the main reason for this hierarchical structure was lower costs of producing power with few large plants as appose to numerous smaller plants. Smart technologies, however, have altered the electric grid in both supply and demand sectors. On the supply side, with advancements in technologies such as gas turbines, fuel cells, renewable power generations and power electronics, there is a shift from large power plants to smaller generators and intermittent generation resources (e.g. wind and PV) [2]. Additionally, customers' demand for higher power quality and public demand for more environmental friendly power production are shifting the power industry towards integration of more distributed energy resources (DERs) [3].

Each year, a large capacity of renewable generation is being installed at the distribution level in the United States and throughout the world [4]. Solar PV generation capacity in the United States has drastically increased in the last decade, and is expected to grow, in line with the renewable portfolio standards. A renewable portfolio standard (RPS) requires electric utilities and other retail electricity providers to supply a certain minimum percentage of customer demand with eligible sources of renewable electricity

[5]. Following this trend, twenty five of the states in the U.S. are expected to have higher than 1 gigawatt capacity of operating solar PV, by 2020 [6].

There are numerous benefits of distributed generation discussed in the literature [7]. The potential benefits include: improving electric system reliability; reduction of peak power requirement; provision of ancillary services, including reactive power; power quality improvements; investment deferral on distribution system infrastructure; reduction in grid vulnerability and resiliency improvement [8]. As an example, distributed solar photovoltaic (PV) systems have the potential to supply electricity during grid outages due to extreme weather condition or other emergencies, and therefore, may significantly increase the resiliency of the electricity system. In order to enable this capability, however, PV systems must often be combined with other technologies, such as energy storage systems to form a microgrid [9].

On the other hand, high penetration of the PV system poses a number of major concerns on distribution feeders. In the United States, more than 1.5 million PV systems were interconnected to the electric grid by September 2017 and thousands of PV installation applications are submitted each year in line with many States' aggressive renewable portfolio standards that encourage these installations [10]. A study looking at 21 utilities reported a high number of concerns about the impacts of integrating distributed generation PVs. These issues are not common among all utilities as each utility is different and has its own perspective, but the goal should be to prevent issues from becoming problematic [11]. Integration of PV generation sources raises the voltage locally which may potentially go beyond an acceptable range, while regulating the

voltage could create additional wear on the existing utility equipment. Widespread deployment of PV systems may also lead to a reverse power flow in power distribution lines. This reverse power flow can create system operation and protection problems. Another challenge is variability of the PV production due to weather changes and movement of clouds which as a result can cause more voltage fluctuations. Lastly, distributed generation including PV systems may falsely contribute to an unintentional islanding condition of the system [12].

At a high-level, grid islanding can be divided into two modes: the intentional (planned) and the unintentional (unplanned) islanding [13]. The purpose of intentional islanding is to divide the grid into one or multiple grid islands due to an occurrence of a disturbance. A common scenario of intentional islanding could be for maintenance purposes. The intentional island is in fact a microgrid that can supply its local load constantly by means of distributed generation through an energy management system until the utility is ready to be synchronized back with the grid. Since intentional islanding is planned, it is not expected to create unexpected issues and any problem can typically be managed during or after the grid disconnection. However, there are multiple reasons why distributed generators must cease to energize the system in case of an unintentional islanding condition. First, there is a risk of equipment damage due to operation outside the utility-allowable condition (e.g., voltage limits, nominal frequency, etc.). Second, there is a potential safety risk to utility crews who may be working on the islanded circuit and are expecting the circuit to be de-energized. In addition, operation of circuit reclosers could result in an out of phase reclosing with large transients and voltage peaks that

damage the utility and customer equipment [3]. In order to prevent significant influence on system instability during a disturbance, smart distributed generation technologies are needed to establish new operational requirements and functionality [2].

Standards and regulations have been prepared and mandated to ensure safe and reliable integration of distributed generation into the power system. Every state has its own interconnection process, and the implementation practices at the utility level may be different. At the highest level, the Federal Energy Regulatory Commission (FERC) is a federal entity that regulates electricity system of the United States. Distributed generation integration has been studied by several research organization and standard institutions such as Electric Power Research Institute (EPRI), National Renewable Energy Laboratory (NREL), North American Electric Reliability Council (NERC), Institute of Electrical and Electronics Engineers (IEEE) [14]. For example, Current interconnection standards require that distributed generators detect if they become separated from the main grid, and cease to energize the local islanded electric power system, accordingly [15].

It is essential that interconnection application procedures be streamlined, when possible, in order to avoid unnecessary interconnection studies, and at the same time, ensure reliable and safe operation of the grid. In California, for example, the California Public Utilities Commission (CPUC) issued an order to address interconnection standards for devices to the electric grid [16]. Rule 21 has identified screening process that allows low-impact generators to be interconnected relatively quickly and makes the review process more efficient for smaller generation integration into the distribution system. As

part of the fast-track process, a 15% threshold was established to identify situations where the amount of DG capacity on a distribution line section may not yet be considerable [17]. The 15% threshold refers to the distributed generation capacity penetrations. Capacity penetration is defined as the nameplate capacity of the combined distributed generation on a circuit divided by the peak annual load on that circuit [18]. This threshold is defined based on a discussion that adverse integration impacts such as unintentional islanding, voltage variations, and protection coordination effects are insignificant if the combined distributed generation on a line section is always less than the minimum load. However, it is important to note that PV and inverter systems have unique technical characteristics, and the 15%-based screening may not always be applicable for safe operation under unintentional islanding [15].

Grid-connected PV inverters are equipped with anti-islanding features, and they are required to be certified before they can be interconnected to the system. However, even with certification, due to multiple configurations and complexities of distribution systems, the ability of PV systems to detect islanded conditions may not always be efficient [12]. UL 1741 and IEEE 1547 provide certification and grid integration requirements. There are concerns raised by utilities regarding the unintentional islanding test in UL 1741 as the test addresses only a single inverter at a time; therefore, multiple inverters could interfere with each other in such a way that an unintentional island may not be detected [19]. IEEE 1547-2018 standard requires all the DERs to cease energizing the unintentionally islanded distribution system with a run-on time (ROT) of less than 2 seconds. The run-on time (ROT) is defined as the time between the moment at which a

switch opens to form the unintentional island, and the moment when the DERs detect the existence of the unintentional island and de-energize it [13]. The anti-islanding techniques implemented within PV inverters may differ among solar PV inverter manufacturers and models. Manufacturers are not usually willing to publish their inverter algorithms publicly. These methods can sometimes be disclosed via non-disclosure agreements (NDA) between manufacturers and the utility or a consultant that is performing grid islanding analysis. As a common characteristic, all inverters contain a window of ineffectiveness known as the non-detection zone (NDZ) [20]. The NDZ is the range of loads located inside the potential island for which the intended anti-islanding method can fail to detect islanding properly [21]. A potential condition contributing to the failure of islanding detection is when many inverter types exist in the islanded grid; in this case, an individual inverter's anti-islanding detection method may be interfered with by the other inverters in the grid [22].

During recent years, many algorithms have been developed for PV inverter islanding detection. At a high-level, these techniques can be divided into active, passive, hybrid, and communication-based methods [23] [24] [25]. Today, inverters mostly use active anti-islanding measures due to their smaller non-detection zone (NDZ) and better performance compared with the passive anti-islanding algorithms [23]. This research proposes a modeling and comparison of multiple local anti-islanding detection methods for photovoltaic generators in a distribution system. In addition, sensitivity analyses provide additional insight into the effect of various system loading types, power factors and imbalance as well as inverter location on the distribution system islanding detection.

Chapter 2 presents a detailed review of the existing islanding detection methods and their potential advantages and disadvantages. Chapter 3 discusses the methodology and modeling developed based on the modified IEEE 13 bus testbed, in detail. Chapter 4 contains the results obtained under six different cases, each containing nine different scenarios, and conclusions are provided in the last Chapter.

CHAPTER 2 REVIEW OF ISLANDING DETECTION METHODS

This section encompasses a literature survey on islanding detection methods in power systems. Islanding detection methods consist of monitoring DER parameters and/or system parameters, deciding the islanding occurrence based on the parameter values and sending the tripping signals. Various islanding detection methods have been presented in the literature since the introduction of concepts of DERs. Some technical papers have summarized and categorized the different methods throughout these years [3] [26] [21] [27] [24].

These methods can be grouped into two major categories: Remote methods and Local methods. Local methods can be split into active, passive and hybrid. Figure 1, shows the top-level categories of the islanding detection schemes. Remote technique is associated with the utility side and are commonly controlled by the utility or have communication between inverter and utility to shut down inverter. The local techniques are associated with the DG side [3] [26]. Passive methods simply monitor certain parameters such as voltage and frequency and their characteristic. Active methods generate deliberate changes to the connected circuit and monitor the response of the connected circuit to the changes [21].

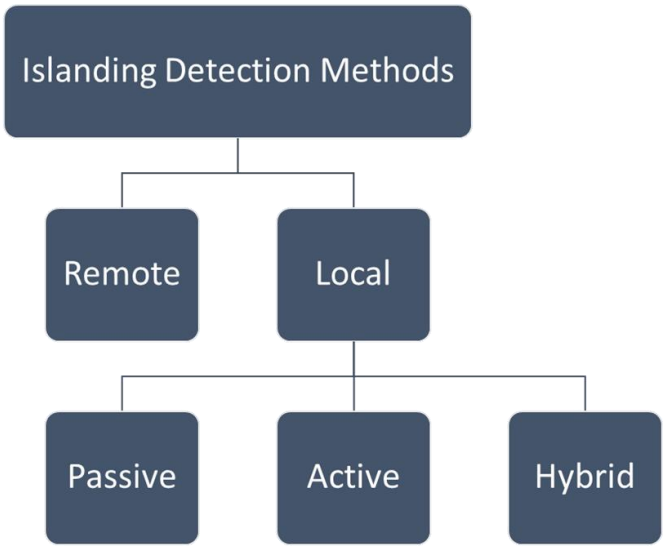

Figure 1. Power System Islanding Detection Schemes.

2.1 Remote Islanding Detection Techniques

Remote islanding detection methods are based on the communication between a utility and DGs. These methods have better reliability comparing to the local methods.

Figure 2 shows different remote islanding detection methods. Each one of the sections are explained below.

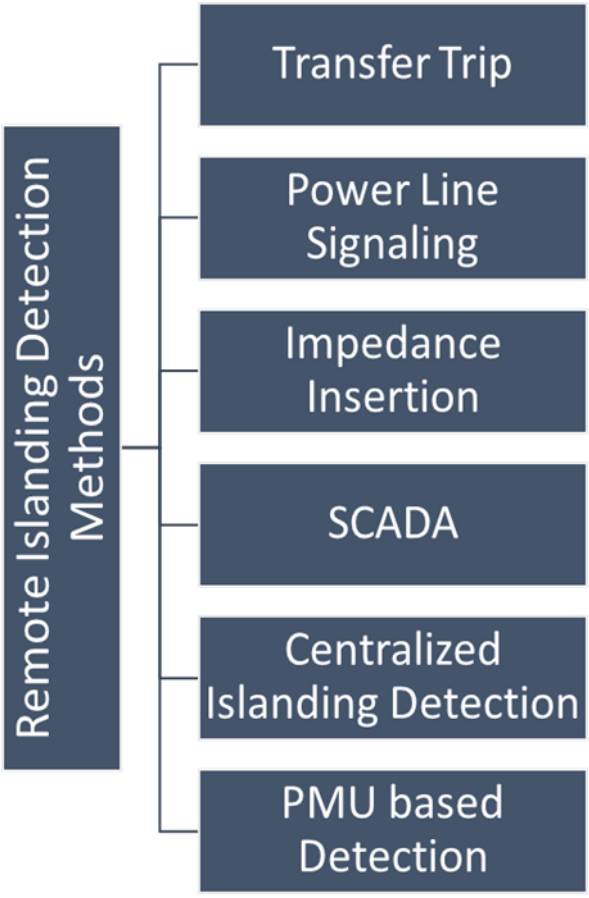

Figure 2. Remote Islanding Detection Schemes.

2.1.1 Transfer Trip Method

In this method, the status of all the circuit breakers and reclosers that can create an island containing DERs are communicated and monitored by a central control unit. Traditionally, telephone lines and radio communication have been the most common media. But nowadays, internet broadband, optic fibers, wireless communication and satellite communication have been suggested [27]. This method significantly increases the costs for both utility and DG owners [3].

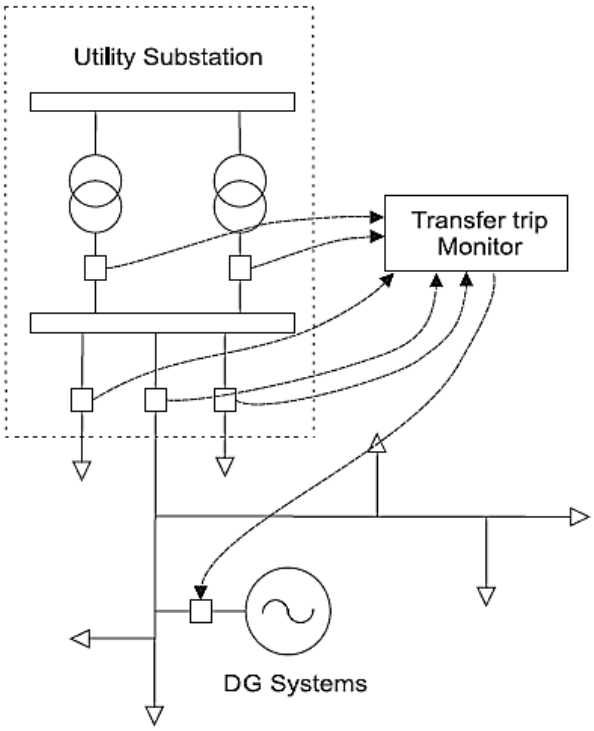

Figure 3. Transfer Trip method scheme [26].

2.1.2 Power Line Signaling Method

This method is also known as power line carrier communications (PLCC) method and technically it is a form of Transfer Trip method. In this method a signal transmitter which is located at the utility circuit sends a signal along the power lines to the receiver in the inverter side of the PCC. If the receiver does not collect the transmitted signal, a breaker has been opened and therefor an island exists [3], [21]. In this case receiver will send a trip signal to the inverter. PLCC signal should have three characteristics to be effective [21]. First, it must be sent from the utility end to the customer end. Second, signal should be continuous. Third, signal should have a low frequency so that it is not blocked by series inductance of the feeder. This method does not need circuit topology or breaker state information [28].

The main drawback of this method is its high cost of transmitter at the utility. Also, if the distance between the utility and DGs exceed 15 km signal boosters might be needed to compensate for signal attenuation [27]. Figure 4 shows a sample configuration scheme of this method.

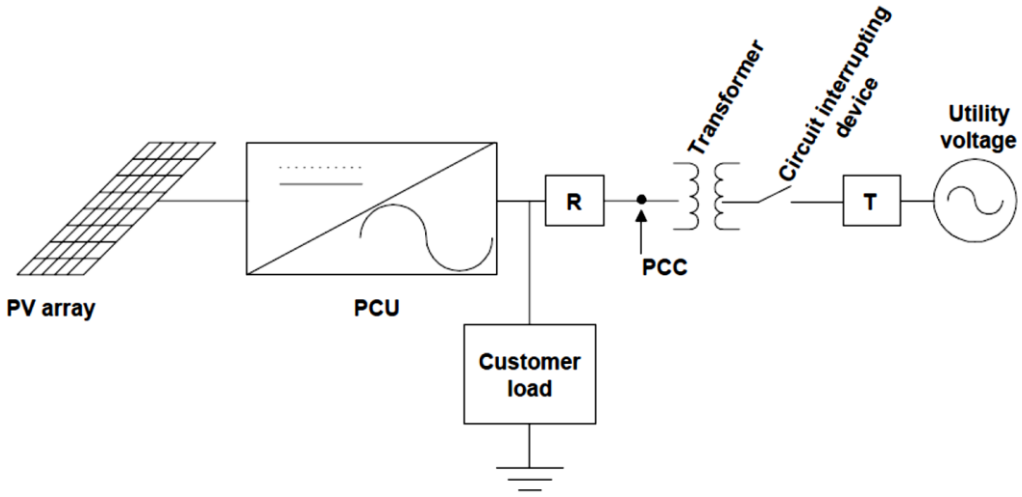

Figure 4. System configuration for power line carrier communication method [21].

2.1.3 Impedance Insertion

In this method, an impedance is installed at the location of grid breaker and inside the potential island through a normally open switch. When the grid breaker is opened, impedance switch is commanded to close with a short delay. If the generation and the load in the island are balanced, the addition of the impedance will disturb the power balance and cause the frequency to change and be detected by frequency relay. Generally capacitors are used in this method for voltage support [21].

This method can be highly effective however has some drawbacks. First, the cost of the capacitor can be high especially when there are multiple breakers that can create an

island. Another problem is that the delay in switching the capacitor can create noncompliance with the standards. This delay is necessary because addition of large capacitor might compensate an inductive load which would cause a islanding detection failure [21] [16]. Another disadvantage can of this method is that if the voltage in the island is already high then the addition of capacitor will add to the overvoltage. Figure 5 shows the impedance insertion method operating principle.

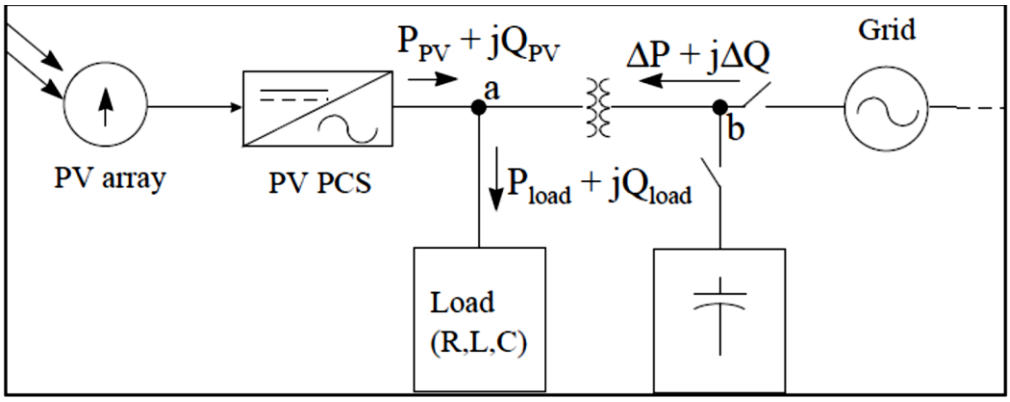

Figure 5. Scheme of impedance insertion method [21].

2.1.4 Supervisory Control and Data Acquisition

To implement this method, voltage sensors are installed on the local circuit. If the sensors measure an unexpected voltage when the utility breaker is open, further necessary action can be taken [21]. This method has the potential to eliminate islanding. Also, utility can have more control over DG. However, this involvement of utility in DG installation and permitting process can be a hassle. Another drawback of this method is that SCADA systems generally exist above substation level but most of DGs exist below substation level. So additional cost will be required to extend the SCADA system to below the substation system. Another disadvantage of this method is their slow speed.

2.1.5 Centralized Islanding Detection

Centralized islanding detection (CID) is a relatively new inter-tripping scheme introduced in [29]. This method is not sensitive to changes in network topology and the number of the DERs since it does not have a predetermined logic. In this method protection agent is installed in a central controller which is connected to other breakers. Controller constantly monitors the status of the breakers. If there is any generators connected to an islanded bus and generators are not connected to the main bus, controller sends tripping signals to generator breakers. Figure 6 shows the scheme of the CID method in a test circuit.

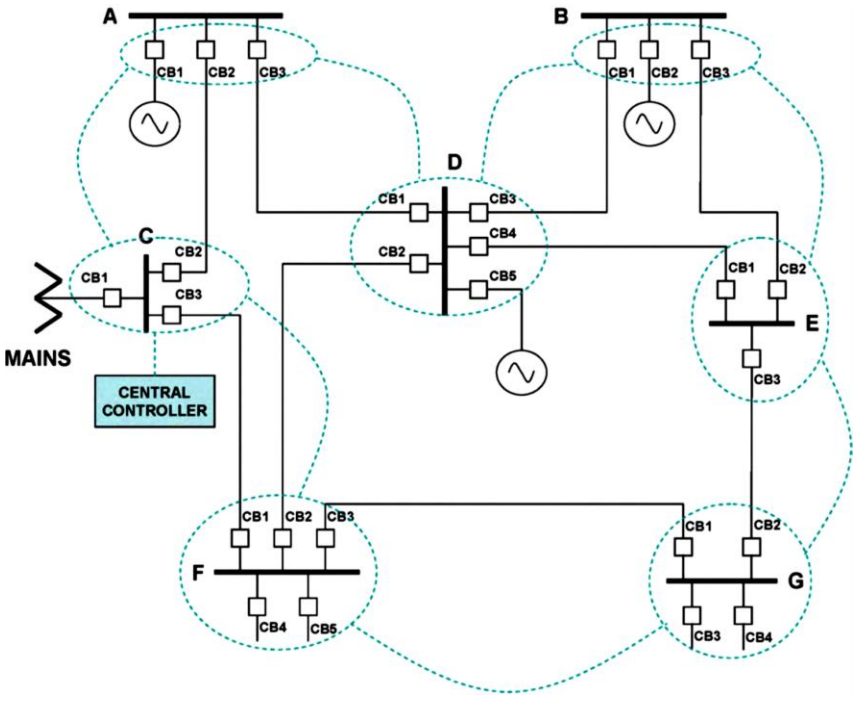

Figure 6. CID scheme example [29].

2.1.6 PMU based Islanding Detection [27], [28], [30]

In this method two relays one in the grid side and another in the DER side provide synchrophasor data for a central synchrophasor vector processor. The synchrophasor processor can detect the island either by angle difference method or slip acceleration method or correlation coefficient-based method (CCB). In the angle difference method processor compares the synchrophasor angle measured with two relays. If the difference of angles crosses a certain threshold, a tripping signal will be sent to the breaker. The slip-acceleration method, defines three operating zones: Normal operating zone, zone A and zone B, as shown in Figure 7. Zone A and B are islanding zones. Slip is defined as rate of change of phase and acceleration is defined as rate of change of slip. If slip and the acceleration of the operating point is either in zone A or B a tripping signal will be sent. CCB method relies on a statistical relationship between frequencies measured by the DER side PMU and grid side PMU. In grid connected DER, the two frequencies are strongly correlated, but when DER is separated from the grid, two frequencies are independently controlled and thus become uncorrelated and their correlation coefficient will drop. These three methods can be implemented at the same time which can eliminate any practical risk of anti-islanding of DERs.

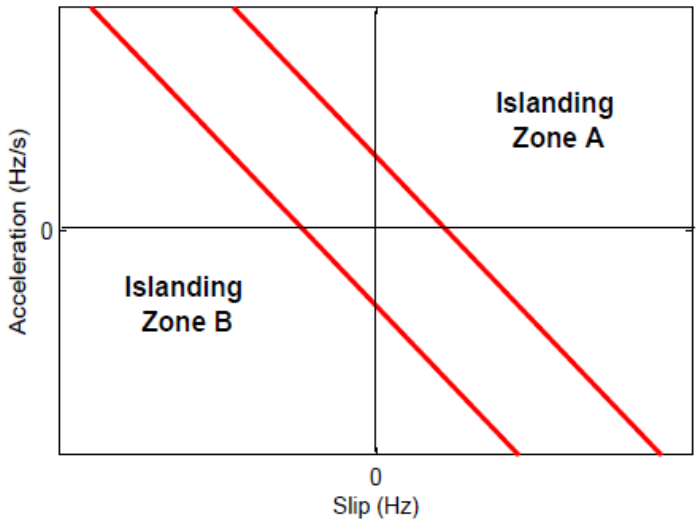

Figure 7. Slip-Acceleration method's characteristic [28].

2.2 Local Detection Methods

Local detection methods are resident in inverter and not at utility. Most of these methods are less expensive but they have larger NDZs comparing to the remote detection methods.

2.2.1 Passive Detection Methods

Passive methods monitor the system parameters such as voltage, frequency, harmonics etc. If a monitored parameter is changed more than a specified threshold, an island is detected. Passive methods operate fast and do not inject additional signals to the grid. However, they have a rather large non detection zone (NDZ) where they fail to detect the islanding. Setting the threshold values too aggressive may cause erroneous faults [3]. Figure 8 shows the passive anti-islanding detection methods. Table 1 compares the strength and weaknesses of discussed passive IDMs.

Passive methods are described below:

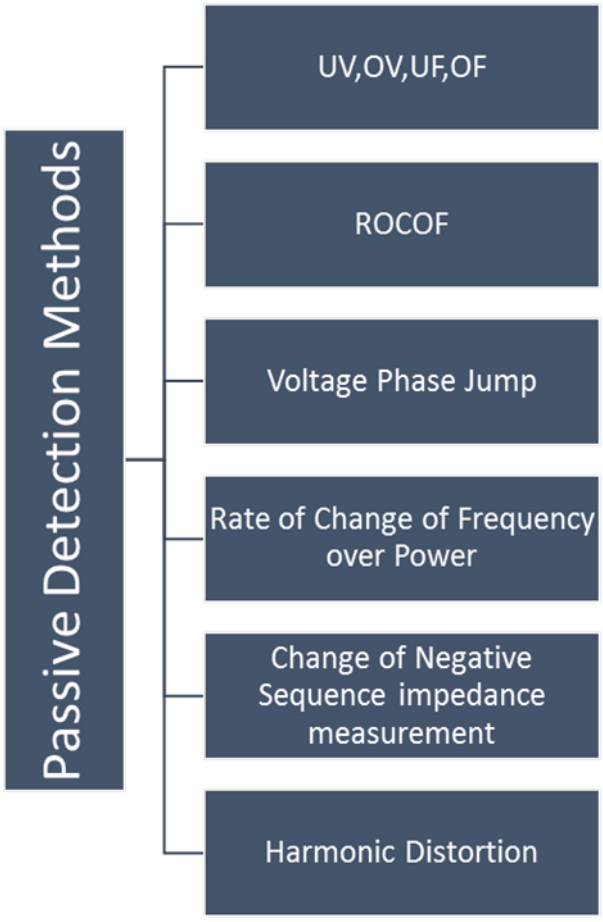

Figure 8. Passive Anti-Islanding Methods.

Table 1. Passive islanding detection methods [31]

No	IDM	Strength	Weakness
1	Over/Under voltage & Under/Over frequency	Low implementation cost since utilities use the same method to protect loads and equipment from damage	1. Large NDZ 2. Reaction time of protection equipment varies, leading to a difficult detection time prediction
2	Rate of change of frequency (ROCOF)	1. Higher sensitivity and faster detection speed than UOV/UOF 2. High detection effectiveness and fast speed even when power between DG generation and loads is closely matched	1. Difficult threshold selection 2. Susceptible to mal-operation, since it cannot distinguish the causes of frequency variation (e.g. islanding or load changes)
3	Rate of change of frequency over power (ROCOFOP)	1. High reliability 2. Smaller NDZ than ROCOF. Higher detection effectiveness for small power mismatch applications	
4	Negative Sequence change	1. High immunity to load fluctuation 2. Not sensitive to system disturbances	1. Extraction accuracy of negative sequence voltage may be affected by distortion 2. Difficult threshold selection
5	Phase jump detection	1. Easy implementation 2. Fast detection speed 3. Effectiveness does not degrade for multiple DGs	1. Difficult threshold selection since phase jump could also be caused by load switching, especially motor load 2. Large NDZ. Prone to fail if local loads, e.g. resistive load, cannot produce sufficient phase error
6	Harmonic distortion	1. Easy implementation 2. Fast detection speed for a wide range of applications	1. Difficult threshold selection 2. Large NDZ when load has a high quality factor 3. Detection effectiveness may degrade for system with multiple DGs 4. Prone to fail when island system does not have transformer(s) and/or output of inverters has low distortion

2.2.1.1 Under/over Voltage and under/over Frequency

All grid connected PV inverters are required to shut down if the frequency or voltage drift to higher or lower than a certain limit. From the anti-islanding perspective, if there is a mismatch between the power consumption and power generation when the islanding occurs, voltage or frequency will shift toward the limits and inverter trips [32]. Figure 9 shows a sample PV/grid configuration. Active power mismatch (ΔP) and reactive power mismatch (ΔQ) at the instance before islanding determine the system behavior after it. If $\Delta P \neq 0$ then the voltage amplitude at PCC will change and if $\Delta Q \neq 0$, load voltage will have a sudden change in phase thus the control system will change the frequency of inverter output current to get $\Delta Q = 0$ [33]. However, if the power mismatch is small, this method may fail to detect the island. Many active anti-islanding methods attempt to quicken this process and push the voltage and frequency to reach the limits faster [32]. Figure 10 shows the NDZ for changes of voltage and frequency. If the active power mismatch ΔP and ΔQ are located in the greyed area, the islanding is not detected.

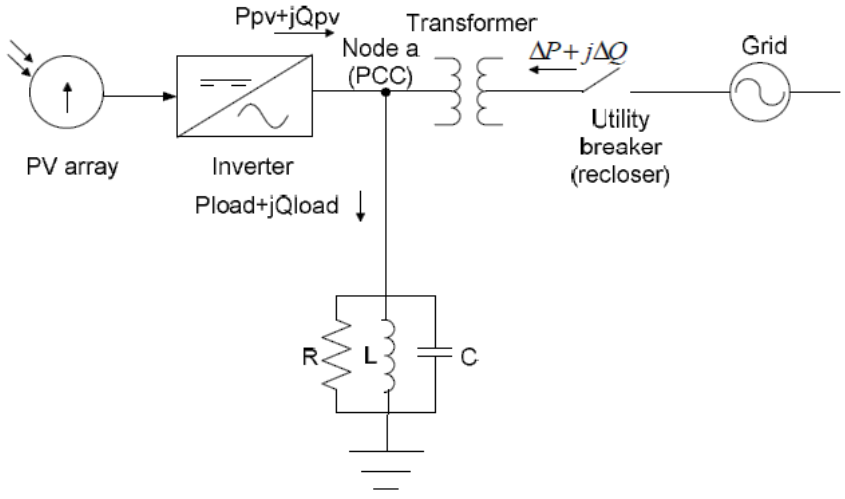

Figure 9. PV plant/grid configuration [33].

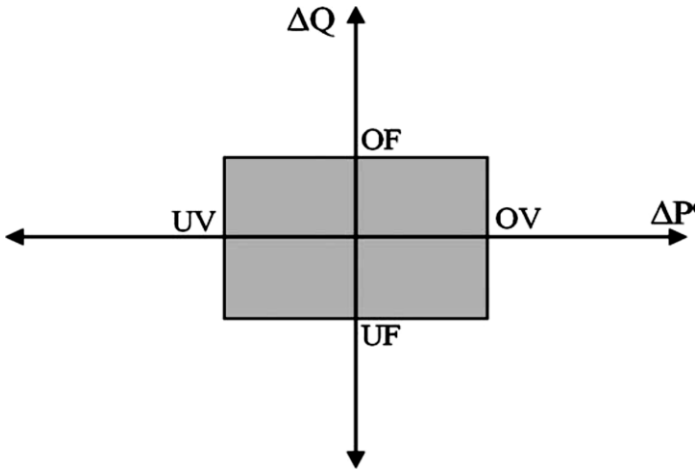

Figure 10. None-detection zone of OUV and OUF [34].

2.2.1.2 Rate of Change of Frequency (ROCOF)

In this method, rate of change of frequency is calculated by capturing voltage waveform over a window of a few cycles. Frequency variation will be very high after islanding. ROCOF relay will monitor the phase voltage and will send the trip signal if the rate of frequency change crosses a certain threshold. This threshold should be selected high enough so that the frequency change due to load switching is not mistaken for a islanding. If the DERs in the island match the load at the time of islanding ROCOF might be zero. Therefore ROCOF relay would fail to detect the island [32].

2.2.1.3 Rate of change of frequency over power

This method utilizes the fact the df/dP in smaller generation system is larger. The results have shown that this method is more sensitive than the ROCOF method for the small power mismatches between load and DERs of an island [3].

2.2.1.4 Change of negative sequence impedance

Authors in [35] employ the assumption that the negative sequence impedance of the islanded network is greater than the grid connected network as shown in (1). The negative sequence impedance is calculated with (2). If Z_2 is above a predefined threshold, inverters will trip. The method has been tested on a 600 V bus and the islanding is detected under a few cycles.

$$Z_{2\,Island} \gg Z_{2\,Utility\ Connected} \tag{1}$$

$$Z_{2\,Thevenin} \approx -\frac{V_2}{I_2} \tag{2}$$

Where:

Z_2 is the negative sequence impedance.

V_2 is the negative sequence voltage at the measurement point.

I_2 is negative sequence current at the measurement point.

2.2.1.5 Voltage Phase Jump

If the islanding causes a large change in the loading, then monitoring parameters such as voltage magnitude, phase displacement and frequency change can be used to detect the islanding [3]. The threshold of phase jump detection should be set high enough to avoid nuisance tripping of inverter. For this reason, the NDZ for this method is rather large in practice [32].

2.2.1.6 Harmonic Distortion

Change in the amount and configuration of load might result in different harmonic currents in the network, especially with presence of inverter based DERs. DERs with monitoring the voltage harmonics can detect the change and shut down the island. Total harmonic distortion (THD) and third harmonics are named for monitoring in [3]. THD is defined as below:

$$THD = \frac{\sqrt{\sum_{h=2}^{H} I_h^2}}{I_1} \times 100 \quad (3)$$

Where:

I_h is rms value of hth harmonic component

I_1 is the rms value of fundamental component

This method can detect the island (with monitoring sudden reduction in THD) if the grid has some harmonic pollution and the inverter is generating only fundamental frequency. Otherwise the THD does not change and AI detection method fails [24].

2.2.2 Active Detection Methods

Passive islanding detection methods do not interact with the connected grid. However, active detection methods generate a small perturbation in the grid. This small perturbation will cause a negligible disturbance if the DER is connected to the grid, and a considerable disturbance if they are not connected [3]. Comparing to the passive methods, they have the advantage of having smaller NDZs and disadvantage of creating instability in the grid especially if the number of connected inverters is high [24]. Figure

11 shows the active anti-islanding detection methods. Table 2 compares the strength and weaknesses of discussed active IDMs.

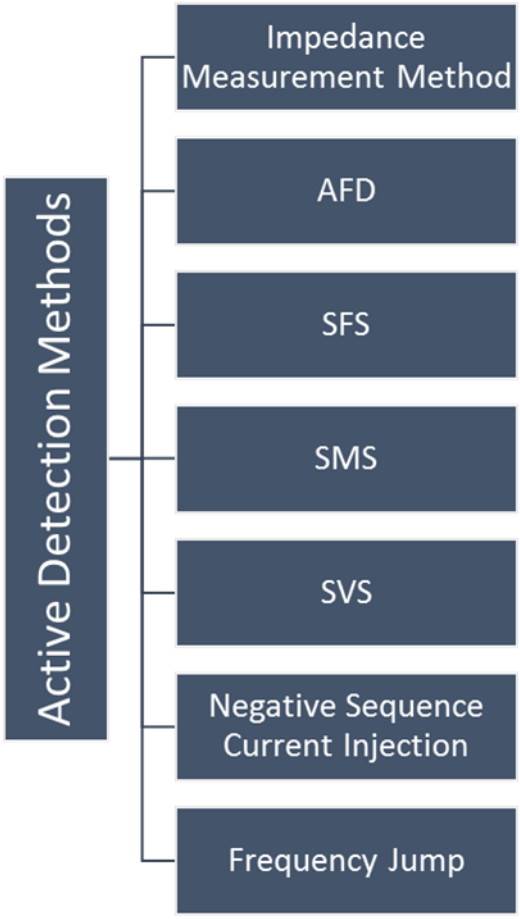

Figure 11. Active Anti-Islanding Detection Methods.

Table 2. Active islanding detection methods [31]

No	IDM	Strength	Weakness
1	Impedance measurement (IM)	Small NDZ for any given single inverter	1. Ineffective for multiple DGs, unless they operate synchronously 2. Difficult threshold selection since accurate value of grid impedance is required
2	Active frequency drift (AFD)	1. Easy implementation for a microprocessor – based DG 2. Small NDZ, and no NDZ for resistance load	1. Power quality degradation 2. NDZ is closely related to chopping factor 3. Effectiveness reduces for multiple DGs if their deviations on frequency bias are different 4. Effectiveness is highly affected by load parameters. For non-resistance loads, the detection time and NDZ increases with higher quality factor
3	Slip-mode frequency shift (SMS)	1. Small NDZ 2. Easy implementation 3. Highly effective for multiple DGs 4. A good compromise between detecting effectiveness, power quality and system transient stability	1. May degrade system power quality and transient stability 2. Relatively low stability with high penetration levels and high feedback loop gain
4	Sandia frequency shift (SFS)	1. One of the schemes enabling smallest NDZ 2. High effectiveness when coupled with Sandia Voltage Shift 3. A good compromise between detecting effectiveness, power quality and system transient stability	1. Slight degradation on system power quality and transient stability 2. Susceptible to noises and harmonics
5	Sandia voltage shift (SVS)	1. Easy implementation 2. High detection effectiveness when coupled with SFS	1. Slight degradation on system power quality and transient response 2. Needs to change inverter's output active power, hence affects the maximum power point tracking (MPPT) algorithm of PV inverter and reduces the energy efficiency
6	Frequency jump (FJ)	1. Effective if sophisticated frequency deviation scheme is used 2. For single inverter, NDZ is almost zero	Ineffective for multiple DGs if frequency dithering function is not synchronized
7	Negative Sequence current injection	1. Fast detection speed 2. Not sensitive to load change 3. Higher accuracy than detecting positive-sequence voltage variation	Degradation on system power quality

2.2.2.1 Impedance Measurement Method

This method is looking at change of voltage in response to change in current, or in other words it is looking at change in the impedance. If the inverter is connected to the grid, change in output current of inverter will cause a change in voltage by following equation:

$$\Delta V = \frac{\Delta P_{DG}}{2}\sqrt{\frac{R}{P_{DG}}} \quad (4)$$

Where:

P_{DG} is the active power output of the DG

V is the voltage at PCC

R is the load resistance

Voltage variation is directly proportional to active power variation since R and P_{DG} are constant [23]. The main advantage of this method is its small NDZ for single inverter case. If the load and PV inverter output are balanced at the time of islanding, inverter output variation will disturb the balance and cause a trip. The disadvantage of this method is that it becomes less effective in presence of multiple inverters. Multiple inverter can also cause flicker grid instability and false tripping [21].

2.2.2.2 Active Frequency Drift (AFD)

This is also known as frequency bias method and frequency shift up/down [21]. In this method, output current of inverter is altered to drift the frequency of voltage at PCC

up or down from normal value [36]. If the inverter is connected to the grid it would be impossible to change the frequency. In Figure 12, T_z is the dead or zero time which is the time between current zero crossing and voltage zero crossing. T_v is the period of the utility voltage and T_I is the period of the sinusoidal portion of the PV output current. Chopping fraction is defined as below:

$$cf = \frac{Tz}{Tv} \tag{5}$$

Please note that the zero time in the second half cycle does not need to be equal to the T_z. As shown in Figure 12 in the first half cycle, PV output current has a higher frequency than the voltage. If inverter is in an island with resistive load, the voltage will follow the current in the second half part of the waveform and go to zero at the same time as current. Thus the new voltage frequency is higher than the original voltage frequency. Inverter will generate the current in the next cycle with slightly higher frequency compared to the new voltage frequency. This means that the newly generated current will have $2*T_z$ zero time compared to the original T_v. This cycle continues until frequency passes the under/over frequency relay limits. Major advantage of this method is its relatively easy implementation. A major disadvantage of this method is that for capacitive loads it is not effective. Another disadvantage is that if multiple inverters are present in a potential island it should be confirmed that all the inverters are biased upwards or downwards so that the impact of AI in some inverters do not cancel the other inverters' AI effects [32] [21].

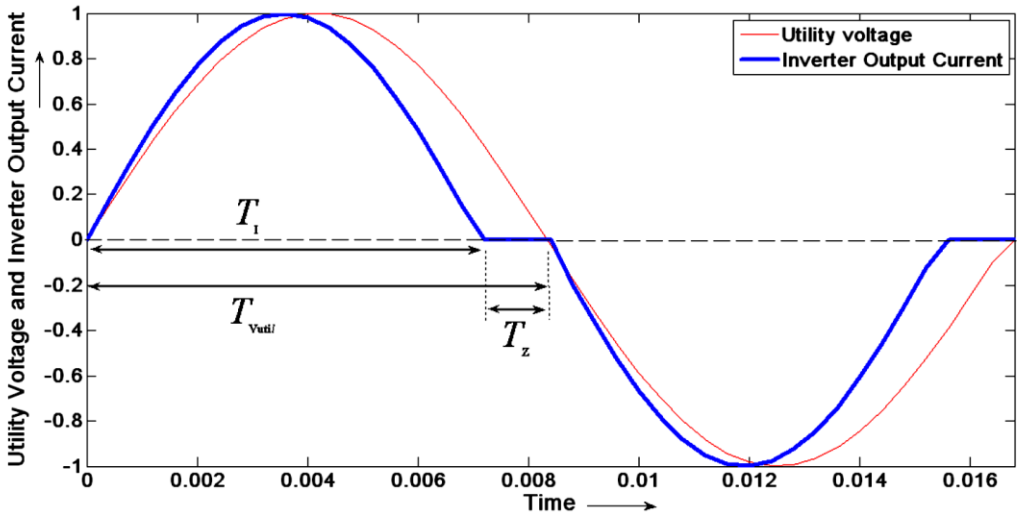

Figure 12. PV inverter output current implementing an upward AFD [33].

2.2.2.3 Sandia Frequency Shift (SFS)

This method is an extension of active frequency drift [21]. In this method the positive feedback perturbation is applied to the frequency of the voltage waveform. Meaning that the dead time of the inverter output current increases with increase in deviation of frequency from its nominal value [3].

$$cf = cf_0 + K(f_{PCC} - f_{line}) \quad (6)$$

Where:

cf is the chopping fraction

cf_0 is the chopping fraction when there is no frequency error,

K is an accelerating gain that does not change direction

f_{PCC} is the measured frequency of voltage waveform at the PCC.

f_{line} is the nominal line frequency.

When the utility is disconnected if f_{PCC} increases, then the frequency error increases which causes the increase in the chopping fraction. Same as AFD case, inverter tries to Main advantage of this method is that it has one of the smallest NDZs of all the active islanding methods. Disadvantages of this method are reduction of power quality (which is due to action of positive feedback to changes in the inverter) and that this method can create stability issues when it is connected to a weak grid [21]. Also islands may not get detected since the phase angle of a parallel RLC load depends on the operating frequency [3].

2.2.2.4 Slip Mode Frequency Shift (SMS):

This method used positive feedback to perturb the inverter. There are three parameters of a voltage that a positive feedback can be applied: amplitude, frequency and phase. SMS applies the positive feedback to the phase hence the short term frequency [21]. A SMS curve can be achieved by the following equation [37]:

$$\theta = \theta_m \sin \frac{\pi(f^{k-1} - f_n)}{2(f_m - f_n)} \quad (7)$$

Where:

θ_m is the maximum phase shift that occurs at frequency f_m.

f_n is the nominal frequency.

f^{k-1} is the frequency at previous cycle.

Phase angle between Current and Voltage as a function of frequency of an inverter with SMS AI is shown in Figure 13. After island formation, operating point of the frequency is at the crossing point of load frequency line and PV inverter response curve. When the grid is connected, inverter operates in the point labeled B. In an islanded grid slight change in frequency of voltage will increase the phase error. In this case, operation of AI will move towards the other stable operating points labeled with A and C. SMS is applied through design of an input filter of the phase lock loop [21]. This method can be used in a system with more than one inverter. The main drawback of this method is that if the slope of the phase of the load is higher than the slope of SMS line between its two peaks, the islanding can go undetected [3].

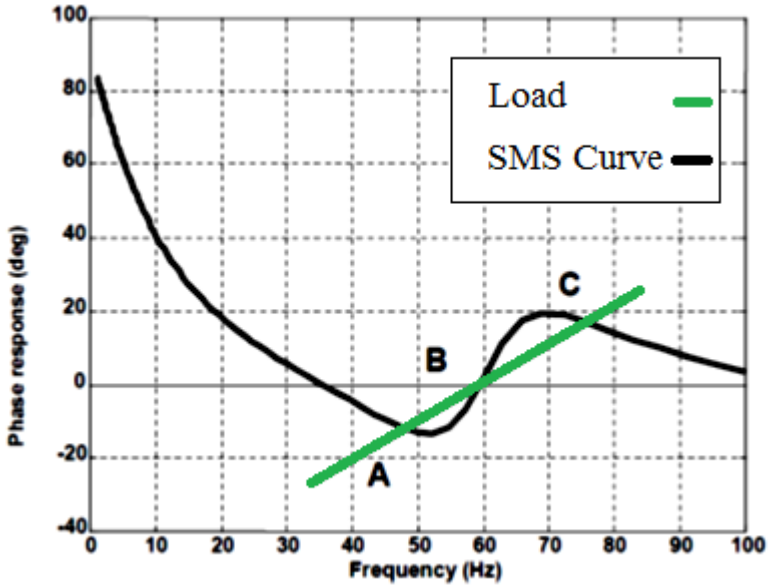

Figure 13. Phase difference of current and voltage (load) vs frequency of an inverter using SMS AI method [21].

2.2.2.5 Sandia Voltage Shift (SVS)

Another method that uses positive feedback is the Sandia Voltage Shift (SVS). This method applies positive feedback to the amplitude of the voltage waveform. If there is a decrease in the amplitude of voltage waveform, inverter will decrease its power output. If the utility is disconnected, a reduction in voltage will cause current reduction in the islanded constant impedance load. SVS is generally implemented simultaneously with the SFS, creating an extremely small NDZ [21]. The current reference to the inverter controller can be calculated from [23]:

$$I_{ref} = \frac{k_v \, \Delta V + P_{DG}}{V} \tag{8}$$

Where:

I_{ref} is reference current of inverter

k_v is the gain for voltage adjustments

ΔV is the measured voltage at PCC (V) amplitude of nominal voltage

This method has two minor disadvantages. First, because of having a positive feedback it will create a small power quality reduction. Second, small variations in amplitude of voltage waveform will cause PV inverter to work off of maximum power point for a period of time, hence lower inverter power efficiency [21].

2.2.2.6 Frequency Jump [21]

In this method similar to the active frequency drift method, dead times are inserted in the inverter's output current waveform. However, instead of dead times in every cycle, frequency is dithered according a pre-assigned pattern. This method can be effective when used with single inverter and if the pattern is sophisticated enough. Disadvantage of this method is similar to the active frequency drift. That is in multiple inverter case, AI of each inverter can cancel each other's effects unless they are synchronized.

2.2.2.7 Negative Sequence Current Injection

In this method, a negative sequence current is injected from a three phase voltage converter. Then, the corresponding negative sequence voltage at point of common coupling is measured. This method shows no NDZ in UL 1741 testbed and acts much faster in comparison to some other active methods. Drawback of this method is that it is sensitive to unbalance transients due to load change or rotating machine inrush currents which may cause a false islanding detection. Equipping this method with additional logics can possibly prevent the false tripping [38].

2.2.3 Hybrid Detection Methods

Hybrid methods contain both active and passive methods. The active technique is utilized only when islanding is suspected by passive technique. Ideally multiple passive techniques can be used simultaneously with one active detection method. Some of the techniques introduced in [3] are positive feedback and voltage imbalance and voltage and reactive power shift.

CHAPTER 3 MODELING OF THE DISTRIBUTION SYSTEM COMPONENTS:

This chapter describes the developed anti-islanding block and other test feeder's components in MATLAB 2016b. MATLAB software was chosen since it is widely used in both industry and academia. Also, MATLAB models can easily be translated to a different software.

3.1 PV Plant Model

The model developed here is a generic three-phase inverter model. This model generates commanded active and reactive power based on the available irradiance. The under-mask view of each inverter model is presented in Figure 14. The green block contains an I-V curve based generic PV array model as shown in Figure 15. The values of I-V curve are scaled based on the Irradiance inputted to the block which is in per-unit. The electric output of this block is connected to the blue block. This block encloses the electrical hardware (as oppose to controls) of the inverter. Figure 16 shows the under-mask view of this block which contains the DC and AC filters and the bridge. The orange block in Figure 14 is the "PV Inv Ctrls" block which contains the measurement, dq0-frame controls, relaying, and the actual anti-islanding (AI) blocks as shown in Figure 17. Figure 18 shows the closed loop controls of the inverter model which are located in "DQ Controller" block in Figure 17. In the top part of the figure, measured active power is subtracted from commanded active power. The resultant difference is sent to a PI

controller which outputs the reference current. The same as above, measured reactive power is then subtracted from commanded reactive power. The resulted error is inputted to a PI controller which outputs the reference current. If an additional phase shift is required by selected anti-islanding method, phase shift is added to the current here. In the bottom of the figure, current errors are sent to PI blocks which output the reference voltage in dq0-frame. Since the main focus of this thesis is the AI block, details of the other blocks are disregarded. Models of this type do not represent any specific inverter, but rather they model the basic functional mechanisms behind each block (PV array, inverter HW, inverter controls, relaying, and AI). As a result, the model should provide behaviorally reasonable results for each AI family that is included, but it will not, and should not be expected to, provide an exact representation of any specific make and model of inverter.

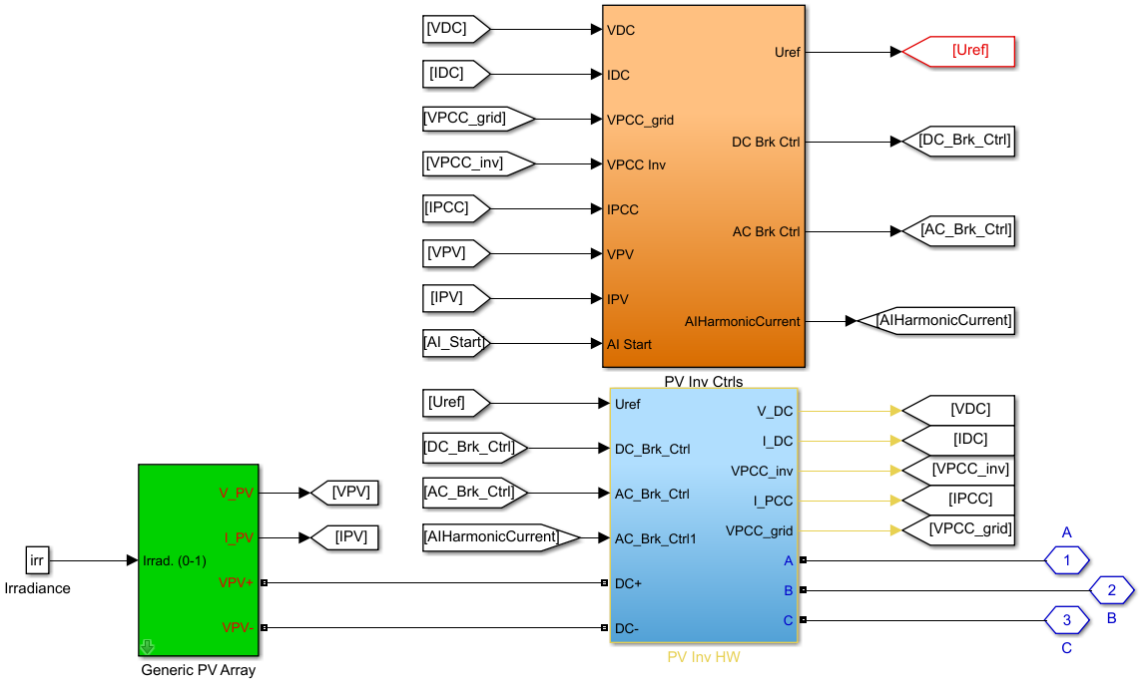

Figure 14. Under mask view of the inverter model.

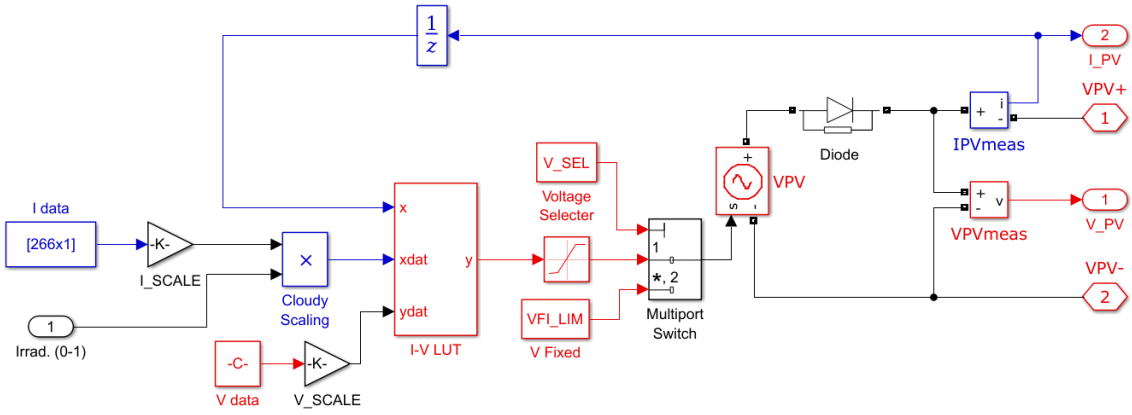

Figure 15. Under mask view of "Generic PV Array Block" in Figure 14.

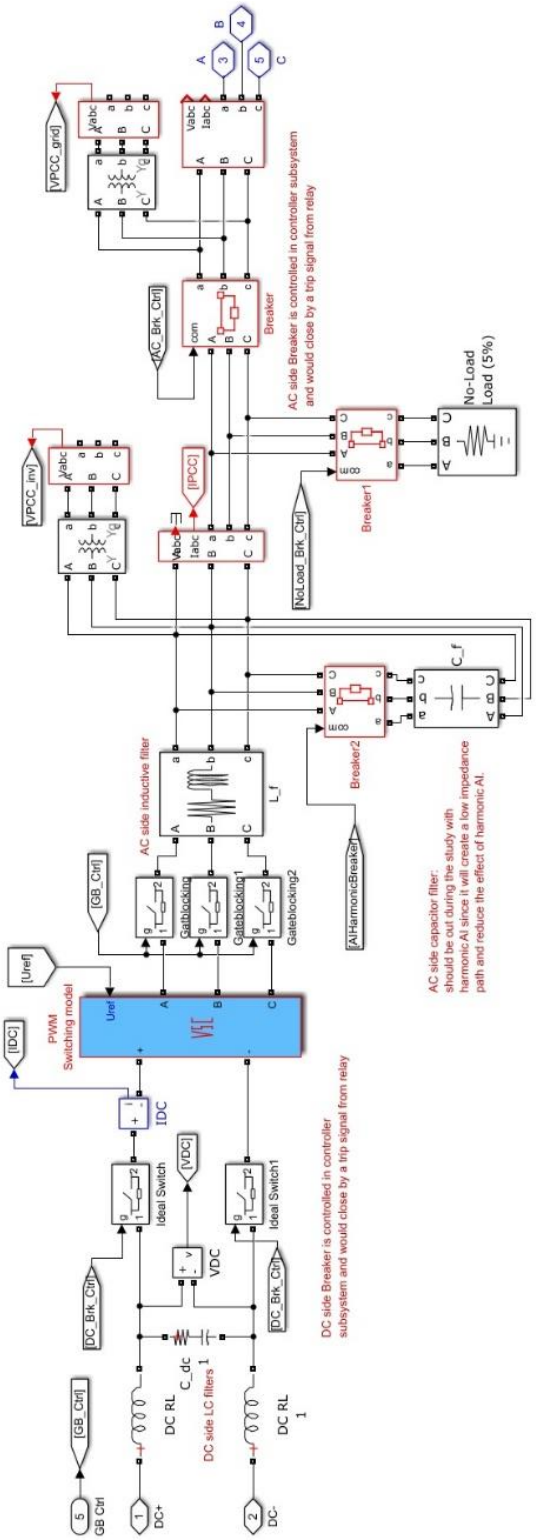

Figure 16. Under mask view of "PV Inv HW" Block (blue block) in Figure 14.

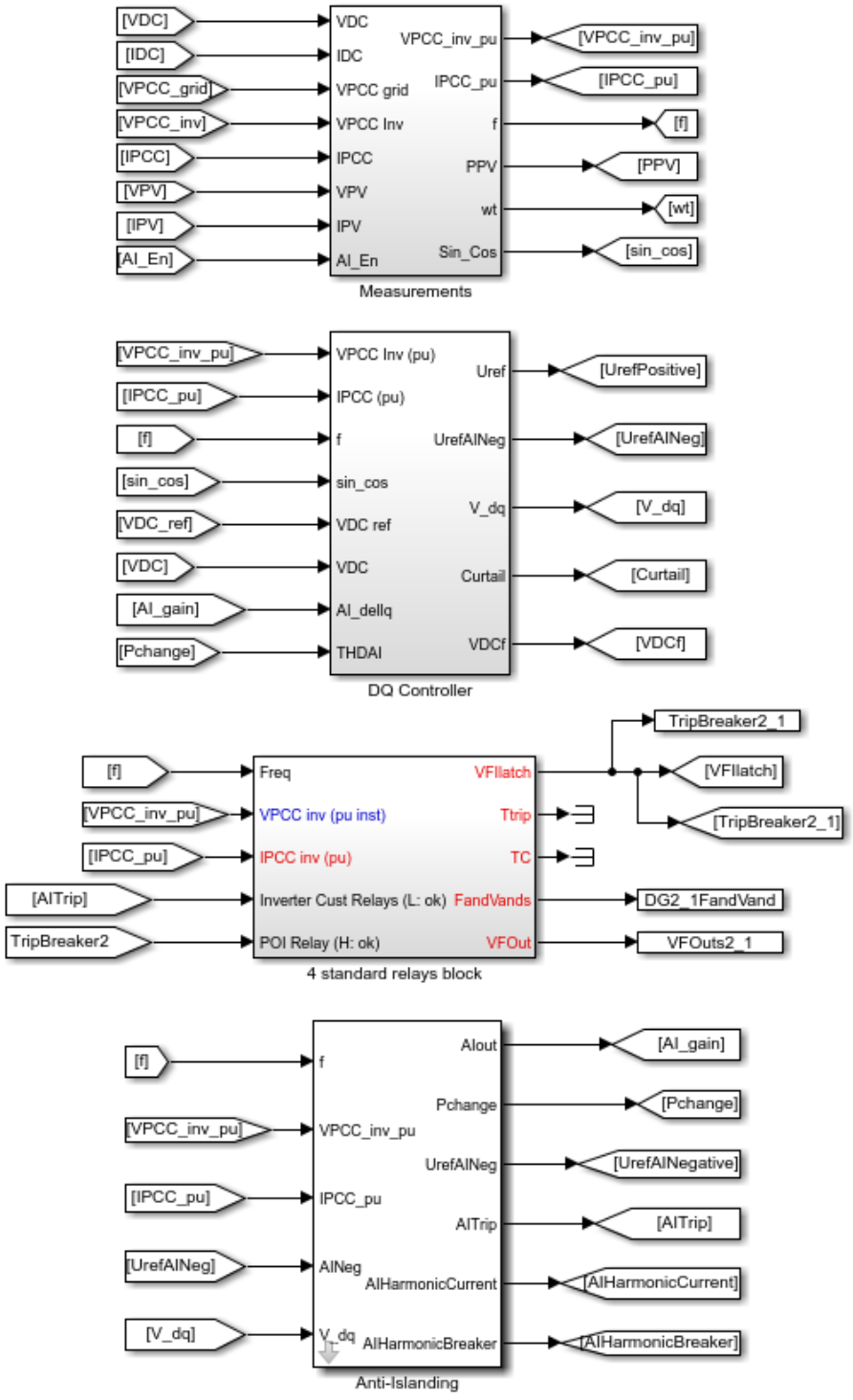

Figure 17. Under mask view of "PV Inv HW" Block (orange block) in Figure 14.

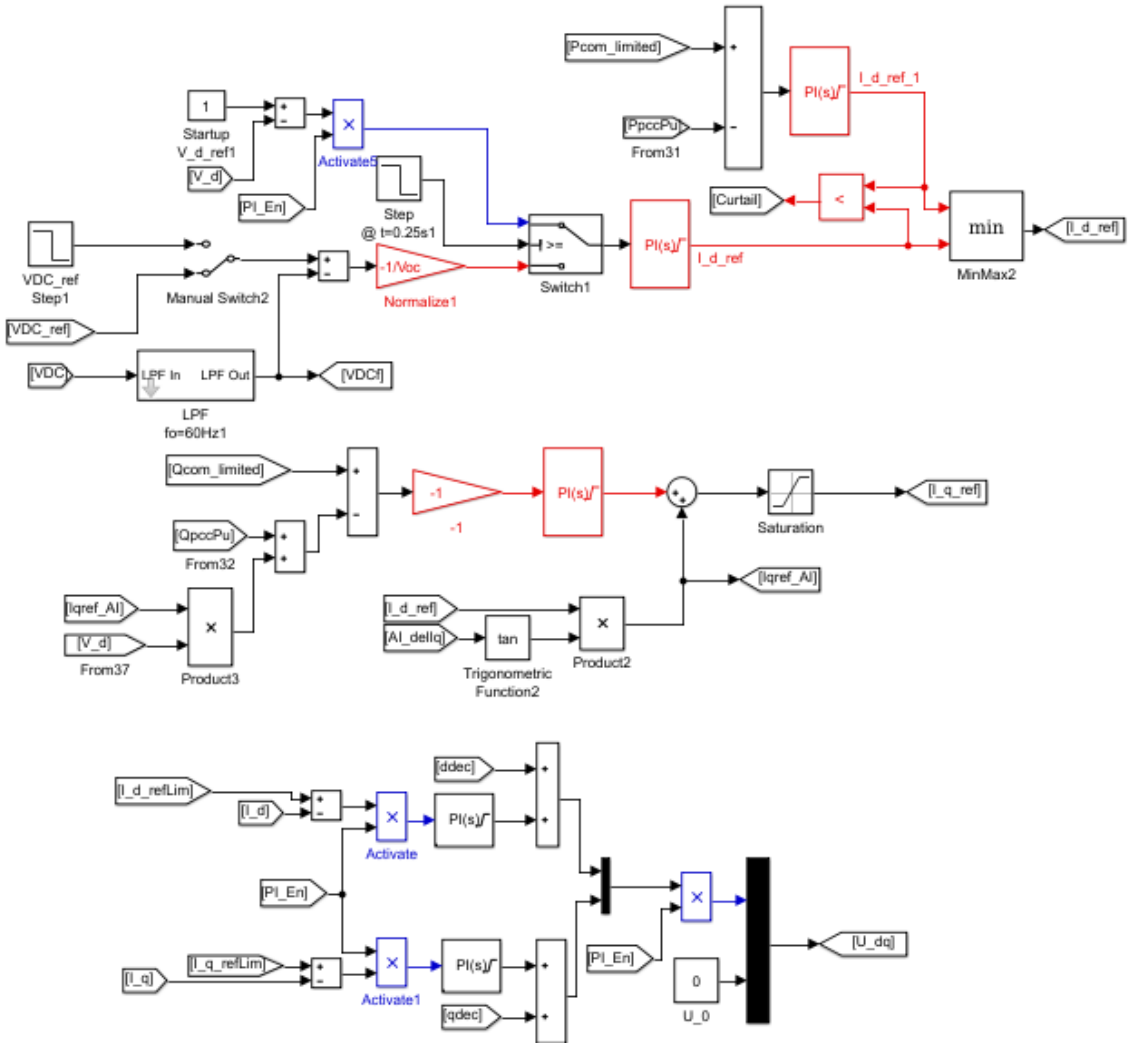

Figure 18. Closed loop controls existing under mask of "DQ Controller" Block in Figure 17.

3.2 Generic anti-islanding (AI) block

Figure 19 shows the AI block, along with its inputs and outputs. Table 3 lists and describes the inputs and outputs. This block contains a model for different anti-islanding methods. The generic anti islanding block can represent anti-islanding methods from any of eight groups introduced in [19]. Table 4 shows the different groups of AI detection method. The details of this plot are described below:

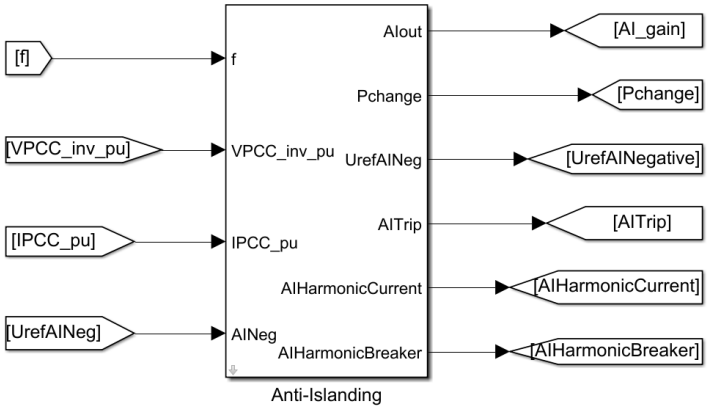

Figure 19. AI block inputs and outputs

Table 3. Inputs and outputs of AI block

INPUTS	
f	Measured frequency by the inverter PLL (Hz)
VPCC_inv_pu	Measured phase to ground voltage at the point of common coupling (pu)
IPCC_pu	Measured phase to ground current at the point of common coupling (pu)
UrefAINeg	Negative sequence reference voltage waveform generated by the controllers that will be edited in the AI block. (pu)

OUTPUTS	
AI_gain	Summation of the SFS and QuasiSFS AI gains. This parameter is added to the reactive power reference of the inverter.
Pchange	Change in active power which is triggered by THD AI (pu)
UrefAINegative	Negative reference voltage waveform to be send to the inverter bridge (pu)
AITrip	Trip signal due to either ROCOF, phase jump, Negative Sequence impedance or harmonic injection
AIHarmonicBreaker	Switches off the shunt ac filter of the hardware
AIHarmonicCurrent	Harmonic Current to be injected at the PCC (pu)

Table 4. Different groups of AI detection methods [39]

Group	Impact on transient stability	Impact on power quality	Magnitude of perturbation	Shape of perturbation	Dead band	Perturbation (Output)	Monitored variable	One example of the AI scheme*	Active or Passive?
1	Degrades at high penetration	Slightly degrade	Frequency or phase error dependent	Continuous or pulsed	None	Reactive power or phase shift	Frequency or phase angle of voltage	Classic Sandia Frequency Shift (SFS)	**Active**
2A	Degrades at high penetration	Slightly degrade	Frequency or phase error dependent up to a limit within thresholds	Continuous or stepped	None	Reactive power or phase shift	Frequency or phase angle of voltage	Group 1, Classic SFS with saturation limits	**Active**
2B	Degrade at high penetration	Slightly degrade	Does not change within dead band, otherwise same as group 2A	Pulsed or non-pulsed	Yes	Reactive power or phase shift	Frequency or phase angle of voltage	Impedance detection with positive feedback, and includes a small dead zone	**Active**
2C	Degrade at high penetration	Slightly degrade	depends on whether limits are applied / Same as group 1 or group 2A,	Continuous or pulsed	None	Reactive power or phase shift	Frequency or phase angle of voltage	Group 1 or 2A unidirectional positive feedback	**Active**
3	Minimal	Degrade	Does not grow with increasing frequency error	Pulsed	Either	Reactive power or phase shift	Magnitude, frequency or phase angle of voltage	Fixed pulse of reactive power	**Active**
4	Minimal	Degrade	May or may not increase with harmonic voltage at POI	AC current at harmonic frequency	Either	Reactive power or phase shift	Harmonic voltage	Injection of specific harmonic	**Active**
5	Can impact transient stability if false trips	Minimal	NA	NA	Yes	Harmonic current	Frequency change rate	ROCOF (Rate of Change of Frequency)	**Passive**
6	Minimal	Degrade	May or may not increase with negative sequence voltage at POI	AC current at negative sequence	Either	NA	Negative sequence voltage	Negative sequence disturbance (3-phase only)	**Active**

The eight groups of AI detection methods are defined and modeled as follows[19]:

AI Group 1: Inverters in this Group utilize an output perturbation in positive-sequence fundamental frequency or phase that is specifically intended for the purpose of island detection, and that grows continuously in magnitude as frequency error increases in a direction that increases the frequency error (i.e., positive feedback on frequency error), up to the frequency trip limits, and includes no dead zone. In other words, Group 1 inverters use positive feedback on frequency or phase to create instability when the island forms. The output perturbation may be pulsed or continuous, but the key is the positive feedback; the magnitude of the perturbation must continuously increase with increasing frequency error as long as the inverter is within the frequency trip bands.

AI Group 2A: These inverters are similar to Group 1 in that the inverter produces a pulsed or non-pulsed output perturbation in positive-sequence fundamental frequency or phase that is specifically intended for island detection and grows with frequency in a direction that increases the frequency error (i.e., positive feedback on frequency error), but not continuously to the trip bands. Inverters in this Group may have a stepped or otherwise discontinuous function of frequency, or a saturation limit that is reached prior to the frequency trip thresholds. However, because the impact of a dead zone (hysteresis about 60 Hz in which the anti-islanding perturbation is not produced) is a special case, inverters with a dead zone about 60 Hz are specifically excluded from Group 2A.

Figure 20 shows a block diagram of the SFS implementation in MATLAB. Two variants of SFS are implemented: a continuous variant in which the frequency error signal is multiplied by a certain gain entered by the user; and a discretized, "stair step" varaint in which the user enters a Q-F function in the AI dialog box similar to that depicted in Figure 21. The continuous mode of SFS with no saturation limit and no dead-zone (as shown in Figure 22) falls into Group 1 AI category. However, by selecting the discontinuous mode of SFS AI or intoducing a saturation limit, the SFS technique will be part of the Group 2A category as shown in Figure 23. The Q-F function is implemented by the threshold-triggered switches in the lower left quarter of Figure 20. The switch thresholds are equal to the values defined by the user in the "Frequency error limits" section of the dialog box. The measured frequency error is compared to each limit, and if it is larger than a certain limit then the corresponding reactive power value is selected. If higher than nominal frequency is observed, reactive power will be consumed to further destablize the grid.

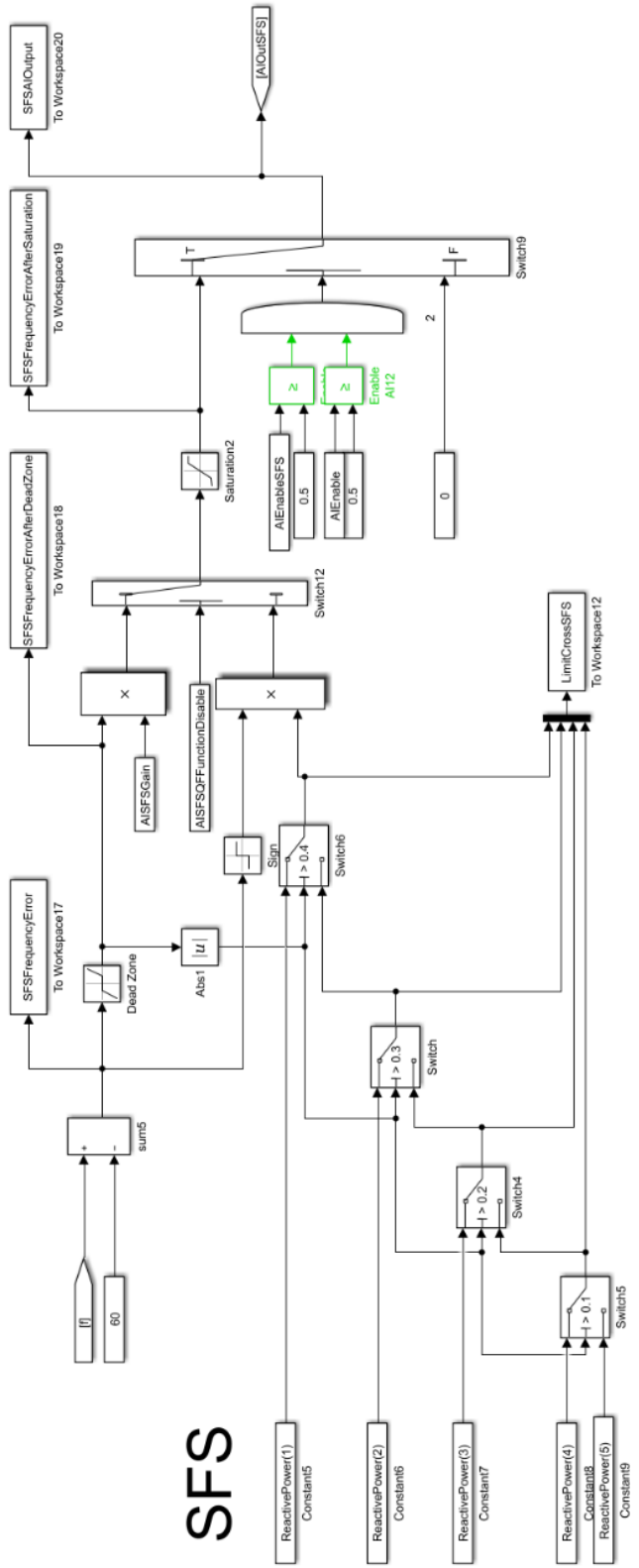

Figure 20. Implemented Sandia Frequency Shift anti-islanding scheme in the AI block.

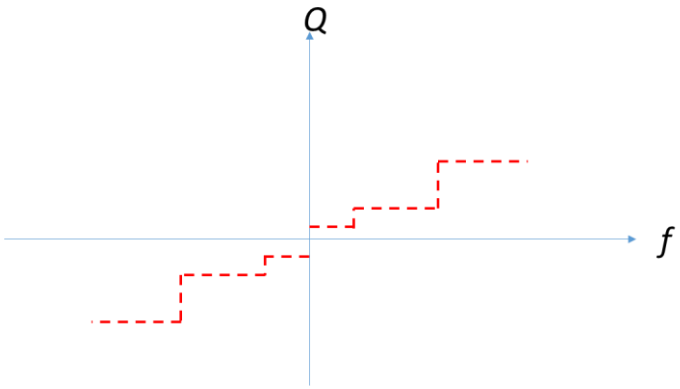

Figure 21. Sample Q-F function

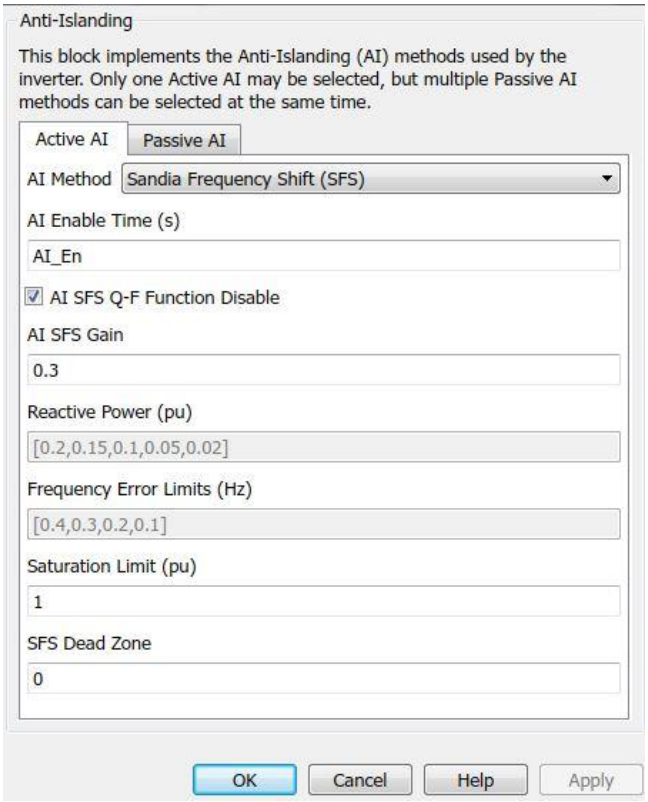

Figure 22. Dialog box of the implemented AI block showing sample parameter values for group 1.

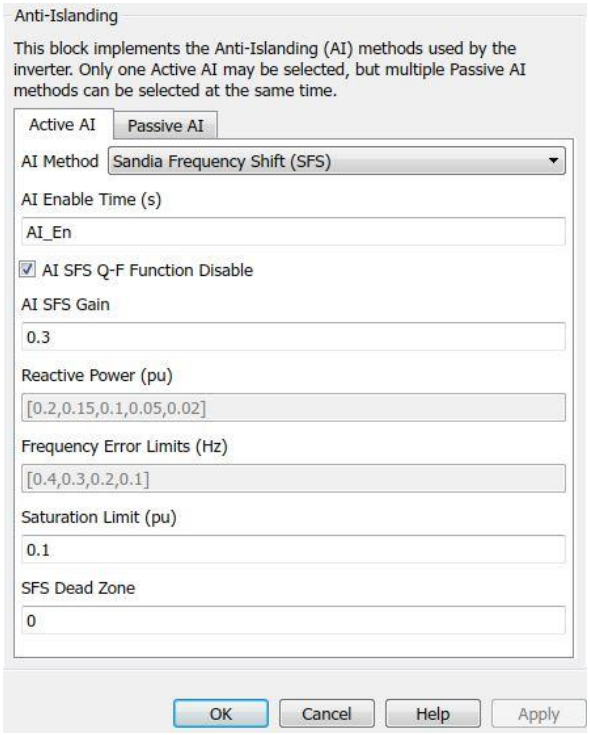

Figure 23. Dialog box of the implemented AI block showing sample parameter values for group 2A.

AI Group 2B: This Group has all of the properties of Group 2A, but with a dead zone about 60 Hz in which the active anti-islanding does not act.

"Quasi-SFS" refers to a combination of the SFS method described above, and the impedance detection method in which the inverter output is pulsed and a parameter change resulting from the pulse is monitored to determine whether an island exists. In this implementation, the frequency error is multiplied by a user-defined gain, and the resulting value is used to set the magnitude of the periodic impedance detection pulses, which in this case are pulses of reactive power. The block diagram of the quasi-SFS implementation is shown in Figure 24, and the GUI for setting its parameters is shown in Figure 25.

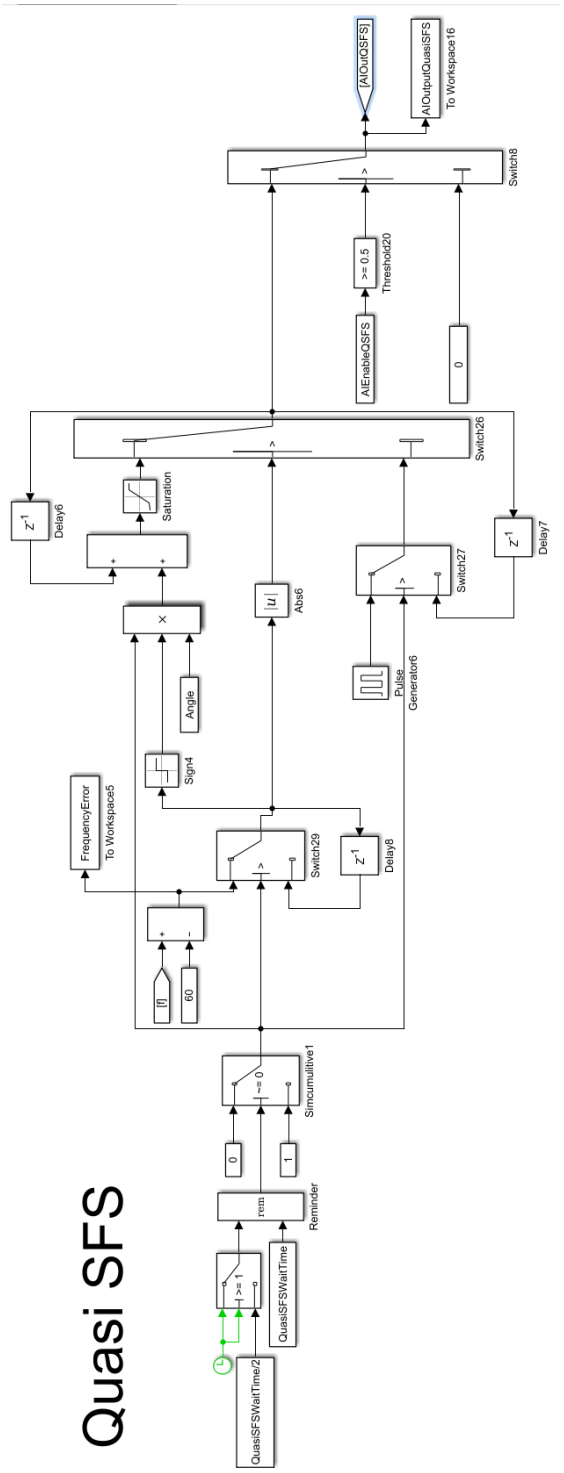

Figure 24. Implemented Quasi SFS anti-islanding scheme in AI block

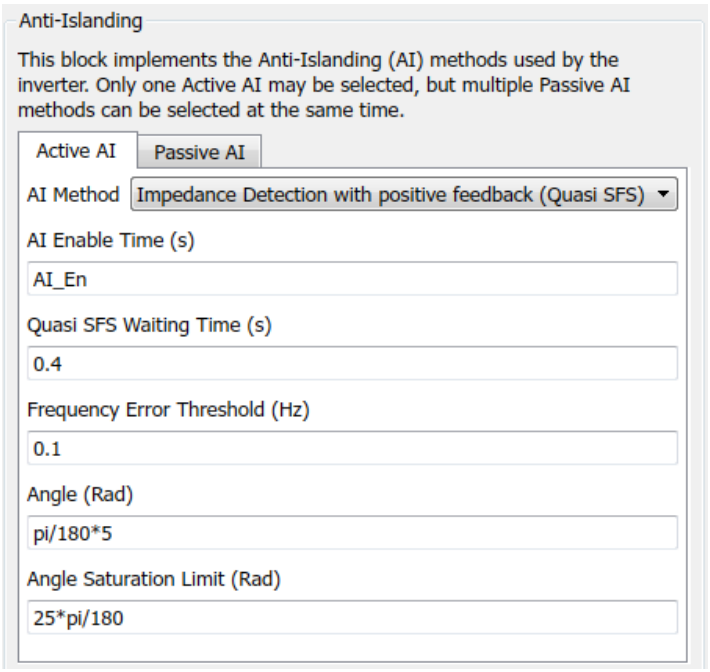

Figure 25. Dialog box of the implemented AI block showing the sample parameter values

AI Group 2C: This Group has all of the properties of either Group 1 or Group 2A, except that the positive feedback on frequency error is unidirectional; that is, the positive feedback is in the same direction regardless of the algebraic sign of the frequency error.

AI Group 3: This Group produces an output perturbation in positive-sequence fundamental frequency or phase, the magnitude of which does NOT grow with increasing frequency error or is NOT specifically designed for island detection.

AI Group 4: Inverters in this Group produce an output perturbation at a harmonic (not fundamental) frequency that is specifically for the purpose of detecting an island. Typically, these are independent of frequency error. MATLAB model for this method, a constant nth harmonic current signal is generated in the inverter. The magnitude and frequency of this current are adjustable by the user. When an island is formed, the impedance path of the harmonic will change, resulting in a change in the n^{th} harmonic voltage. That harmonic voltage is continuously monitored, and if it exceeds a certain threshold the inverter will shut down. Figure 26 shows the associated GUI with sample parameters and Figure 27 shows the method as implemented in the AI block.

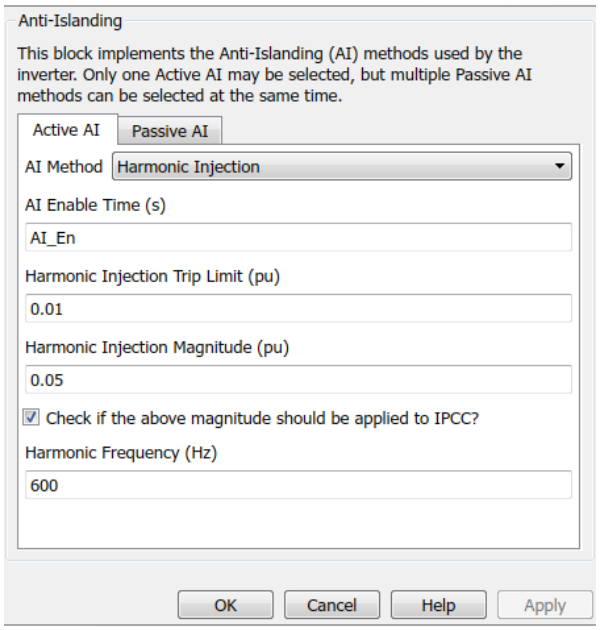

Figure 26. Anti-Islanding sample parameters.

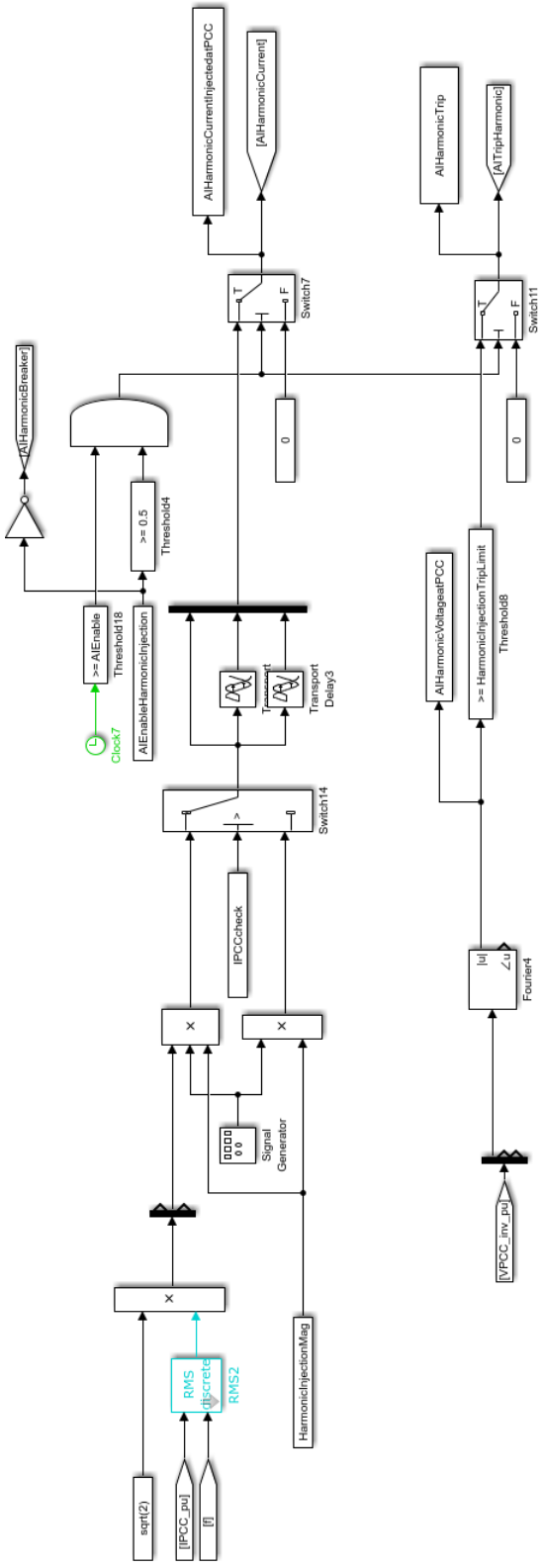

Figure 27. Implemented Harmonic Injection scheme in the AI block.

AI Group 5: Inverters in this Group rely on passive methods only (such as ROCOF or vector shift) or advanced signal processing of voltage or current measurements to detect island formation. A method that drives the frequency of an island to the frequency trip limits and then relies on the passive frequency trip, does NOT fall into Group 5.

ROCOF, or "Rate of Change of Frequency", compares the frequency at time step *k* with the frequency measured at time step *k*-1, and calculates the rate of change of frequency $\Delta f/\Delta t$. If the rate of change of the frequency is higher than a certain threshold, the inverter will trip. To improve false trip immunity, many inverters require that the ROCOF threshold be breached for a number of samples in a row before a trip will be signaled. Figure 28 shows the ROCOF implementation and Figure 29 shows the associated GUI.

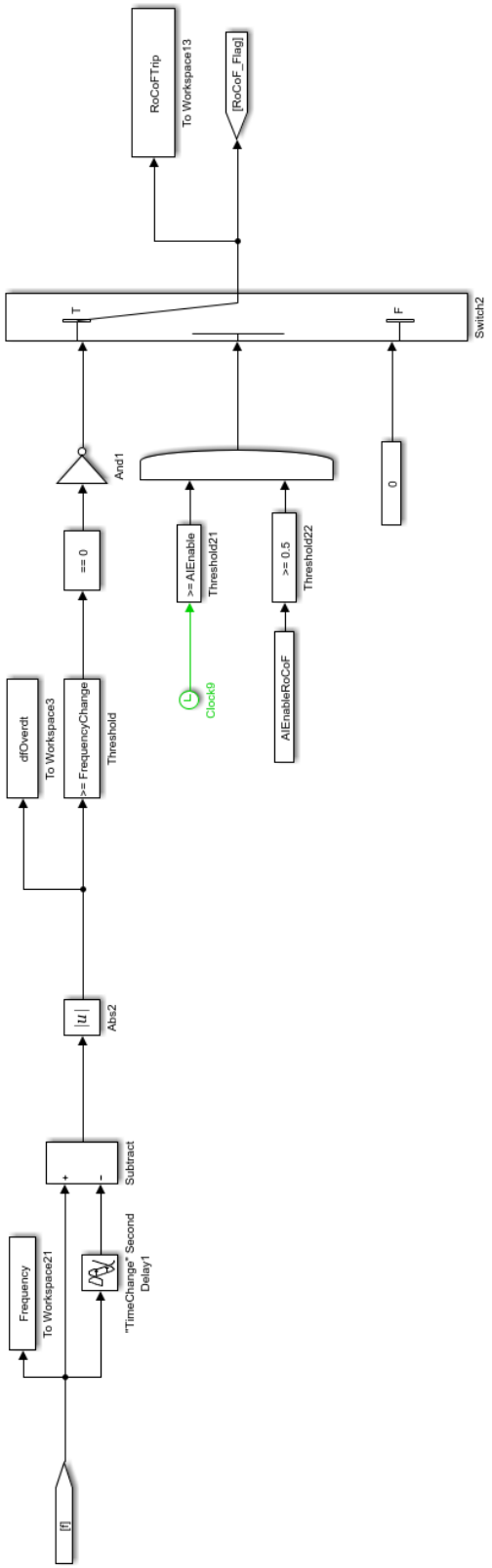

Figure 28. Implemented Rate of Change of Frequency (ROCOF) scheme in the AI block.

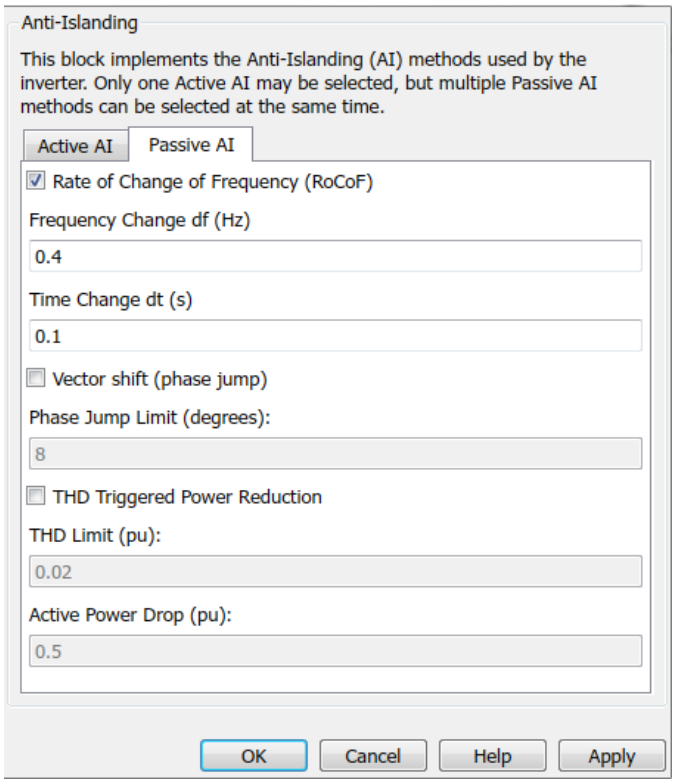

Figure 29. Anti-Islanding dialog box in the showing the parameters

Phase jump, also called vector shift, involves monitoring the voltage at a measurement point for a sudden change in the phase angle of the voltage. If this phase jump exceeds a selected threshold over a selected window, the AI block will send a trip signal to the relay block. The implementation of this method is shown in Figure 30, and the associated GUI is shown in Figure 31.

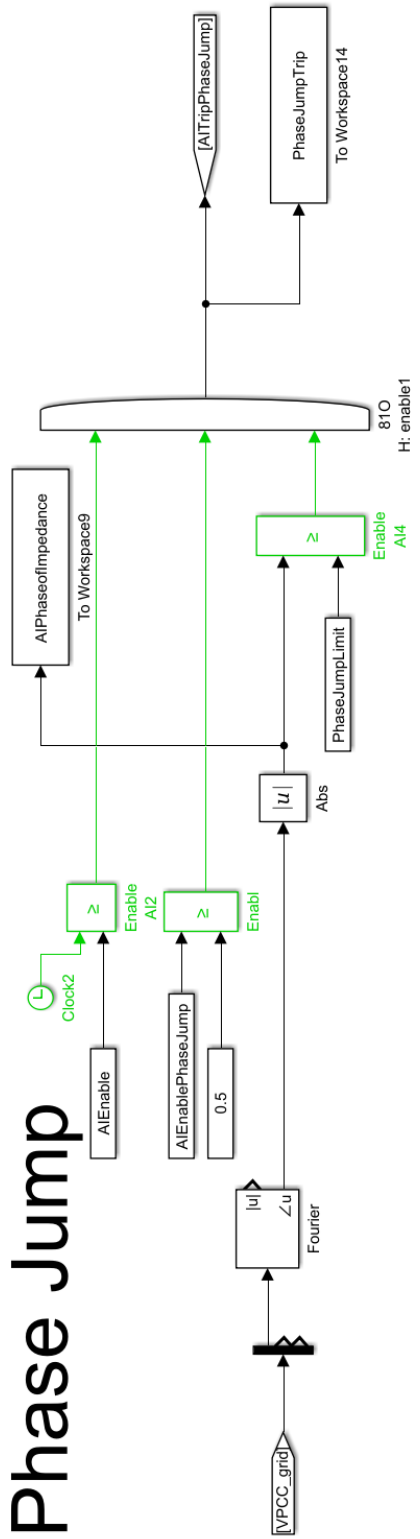

Figure 30. Implemented phase jump scheme in the AI.

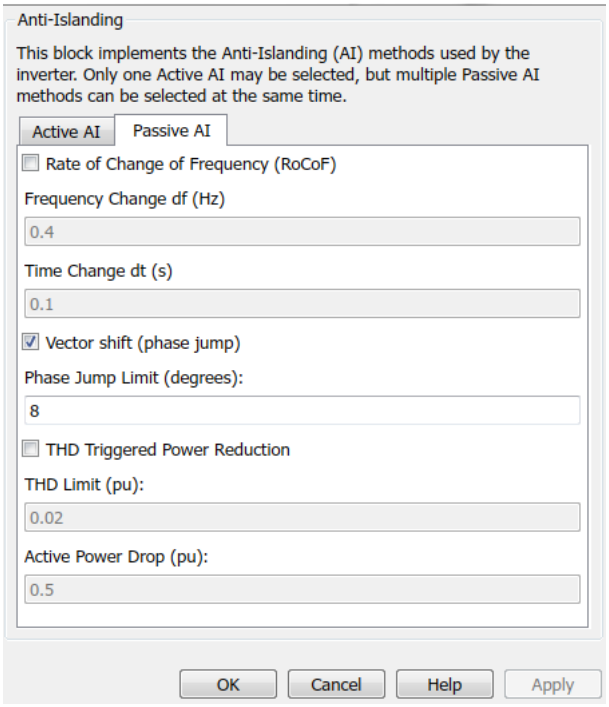

Figure 31. GUI associated with the phase jump scheme.

In the Total Harmonic Distortion method, the total harmonic distortion (THD) of the grid voltage at the point of common coupling is monitored. However, THD is not typically used as a trip signal by itself; more commonly, a jump in THD is used to trigger a reduction in real power, or a change in some other parameter. Thus, this method could be considered a passive-active hybrid. In the implementation used here, when the THD rises above a selected threshold, the AI block sends a signal to the controller to decrease the output power to a level selected by the parameter "ActivePowerDrop". If the inverter is islanded, the reduction in real power will lead to a voltage drop that can be detected and used to signal island formation. When this method is used, the low-voltage ride-throughs are overridden. The implementation of this scheme is shown in Figure 32, and the associated GUI is shown in Figure 33.

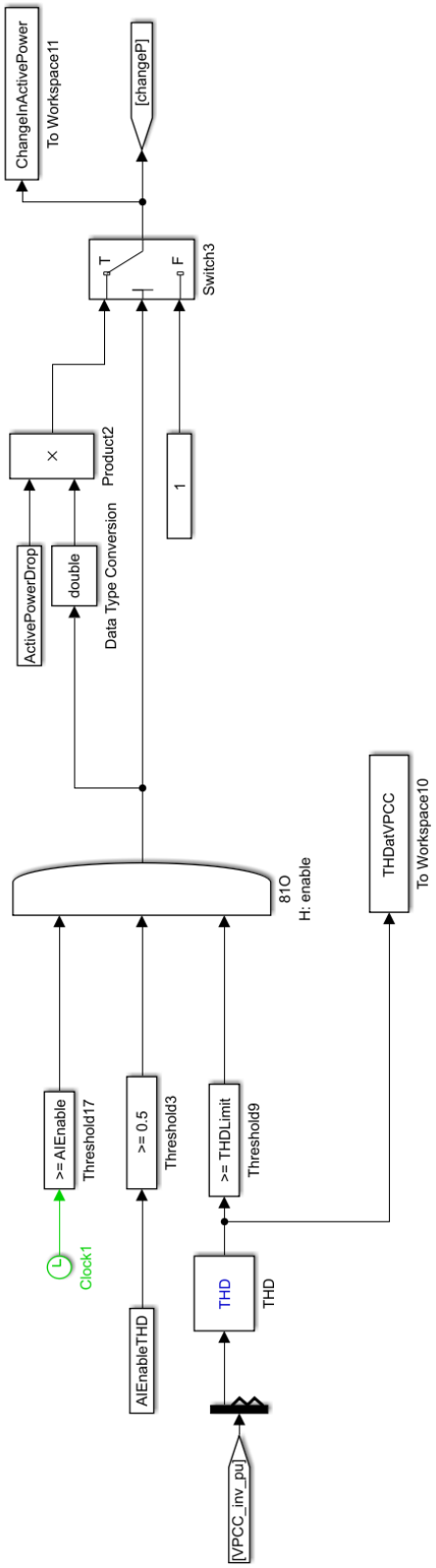

Figure 32. Implemented Total Harmonic Distortion (THD) scheme in the AI block.

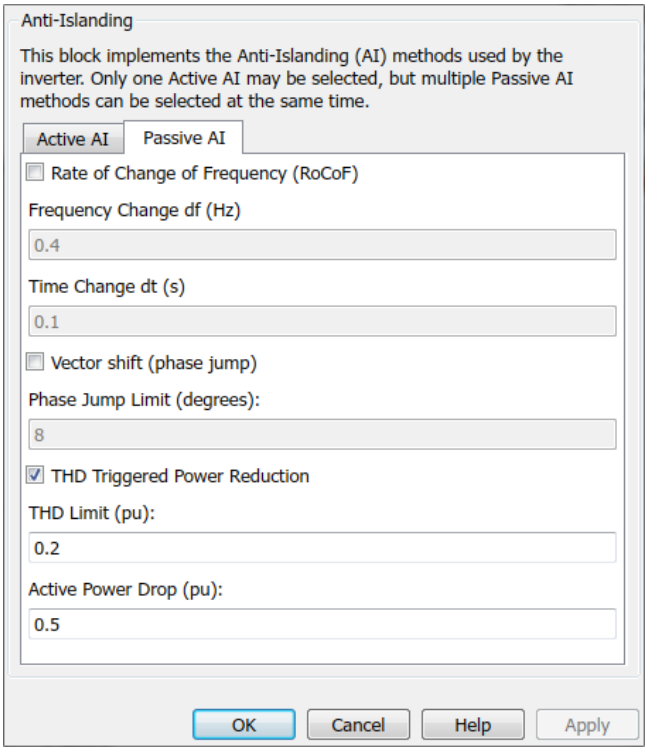

Figure 33. Anti-Islanding dialog box in the showing the parameters.

AI Group 6: Inverters in this Group manipulate the negative sequence current for the purpose of island detection, and apply positive feedback to that negative-sequence perturbation. This may be achieved by several means, including altering individual phase current magnitudes or dithering the phase angle separation between the three output current phases.

In this method, a negative sequence current is injected from the inverter into the grid. While grid-tied, this negative sequence current flows primarily back to the source, but during islanding it must flow into local loads, leading to a jump in negative sequence voltage. Monitoring the changes in the magnitude of the negative sequence voltage in the

grid can indicate island formation. Figure 20 shows the implementation of the negative sequence AI method, and Figure 21 shows the associated GUI. A Double second order generalized integrator (DSOGI) PLL [40] block is used to provide a better representation of the positive and negative-sequence components of the grid voltage. For more information about the PLL please refer to the Appendix A. This implementation does include positive feedback: if the negative-sequence voltage rises, that voltage is multiplied by a gain and used to further increase the negative sequence current. A trip occurs when the negative sequence voltage exceeds a threshold. No time delay is applied.

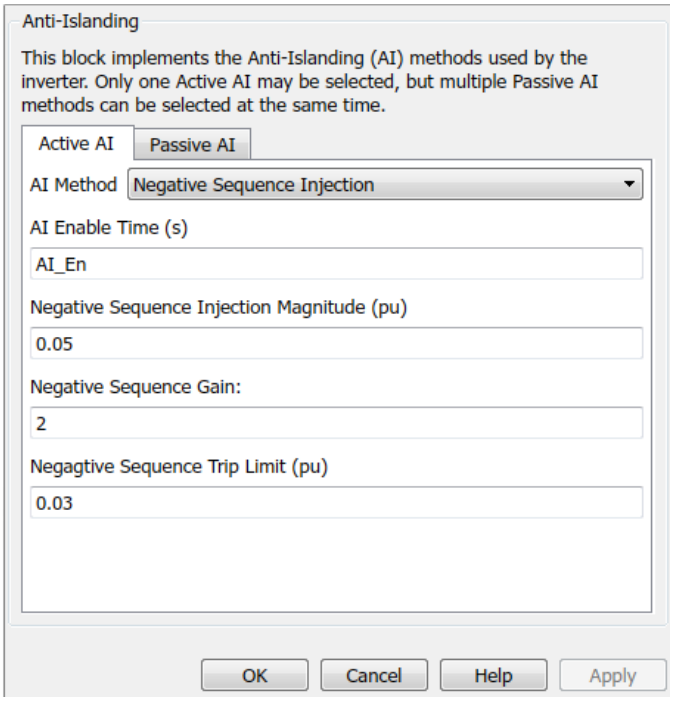

Figure 34. Anti-islanding dialog box showing negative sequence method

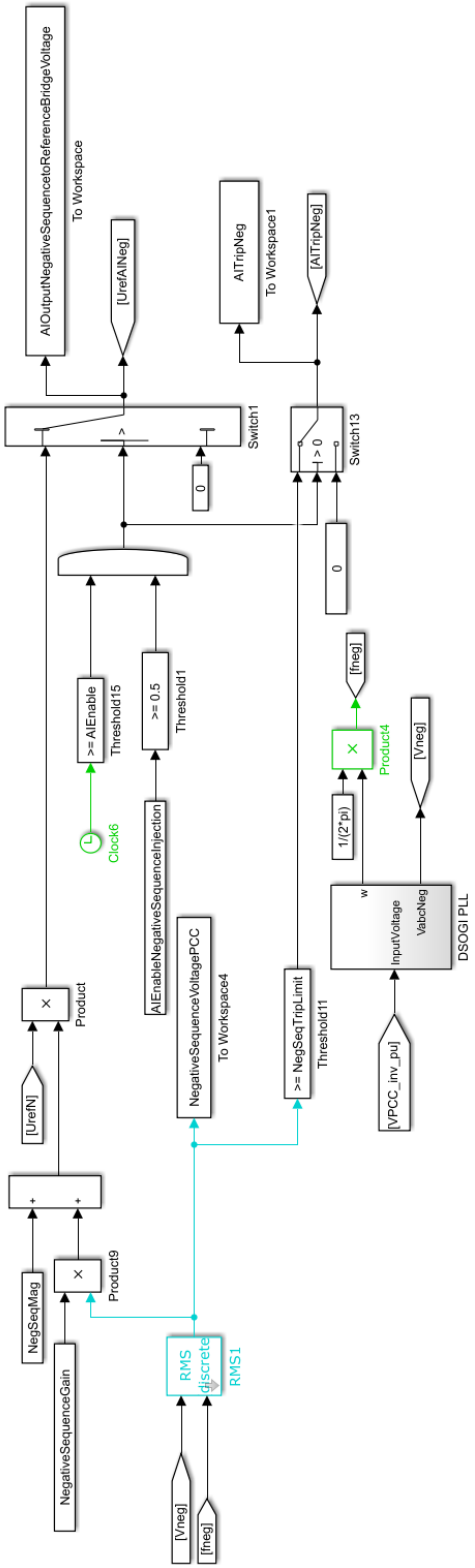

Figure 35. Implemented Negative Sequence Impedance scheme in the AI block.

3.3 Overhead Lines and Underground Cables

Three-phase overhead circuit segments are represented by sequence impedances, and single-phase overhead lines are represented by L-R parameters in which the mutual coupling between the phase conductor and neutral is represented. Underground three-phase segments are represented by a 6×6 matrix representation including each individual phase conductor's cable and concentric neutral, and the cable capacitance is also represented. Underground single-phase segments are represented by π sections because this was a convenient way to include the cable capacitance. All the impedance values are based on values in [41].

3.4 Transformers

Testbed contains 4 transformers in total. Three of them are generator start-up (GSU) transformers and one is a load transformer. GSU transformers all have the same settings. Figure 36 shows the GSU and load transformer used in the test feeder. GSU transformers are rated at 1 MVA connected in Yg: yg and with high voltage side of 4161 V and low voltage side of 385 V. Their impedance is set to 5.75% with X/R ratio of 5 which are typical for distribution systems. The load transformer is also connected in Yg:yg. This transformer is rated at 0.5 MVA with high voltage side of 4160 V and low voltage side of 480 V. The transformer has also 1.1% resistance and 2% inductance which are based on the values in [41].

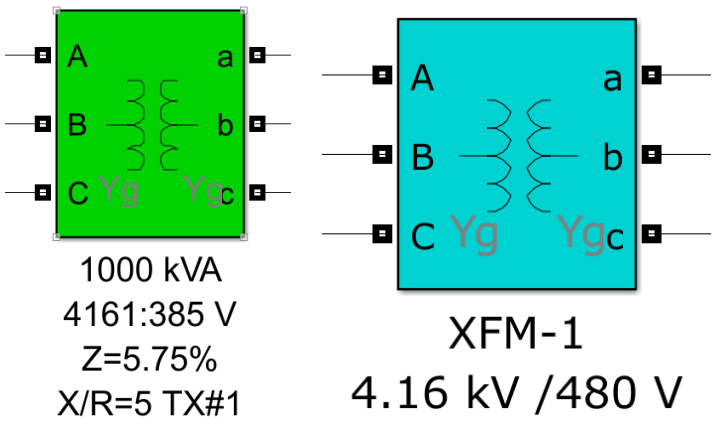

Figure 36. GSU (green) and load transformer in blue.

3.5 PQ Load Model

One of the factors examined in this work is the sensitivity of ROTs to the presence of constant-power loads, referred to as "PQ loads". The PQ load model used in this work is the built-in "Dynamic load" model in MATLAB/Simulink 2016b. This model regulates its P and Q to commanded values via very fast control of a controlled current source. Each single-phase dynamic load block was set to draw a certain amount of watts or vars which varied by voltage based on the equations:

$$P = P_O * (\frac{V}{V_O})^{np} \quad (9)$$

$$Q = Q_O * (\frac{V}{V_O})^{nq} \quad (10)$$

Where, P_O and Q_O are the load real and reactive power consumption and V_O is the nominal voltage. The parameters np and nq define the nature of the load. For example, for constant current load, np and nq should be set to 1 and for constant impedance load

they should be set to 2. Most constant-power loads are designed to operate at or near unity power factor, but for risk-of-islanding testing it is desirable to maintain a specific circuit quality factor. The parameters of these loads are in section 4.1.

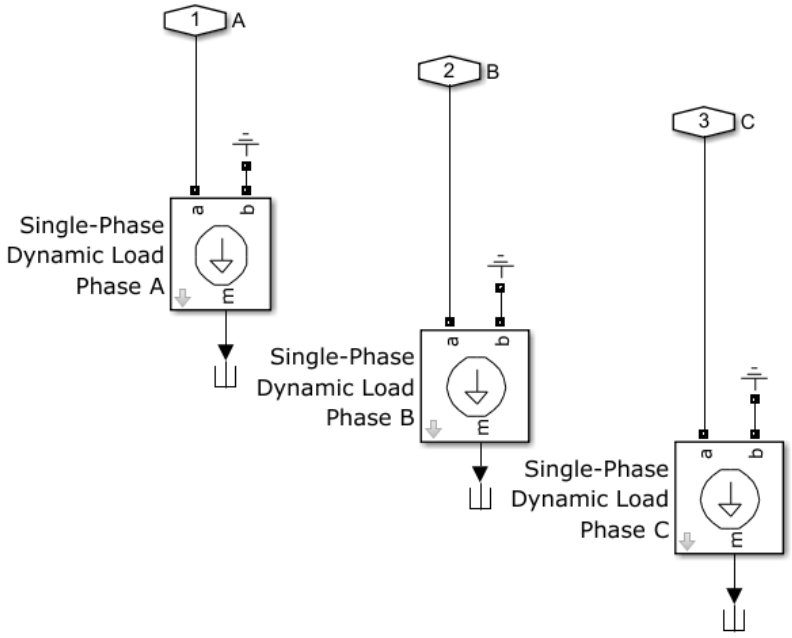

Figure 37. 3 single phase dynamic loads.

3.6 Motor Load Model

The induction motor load in the model was represented using MATLAB/Simulink's built-in single-phase motor model. Figure 38 shows the motor load model used in this thesis.

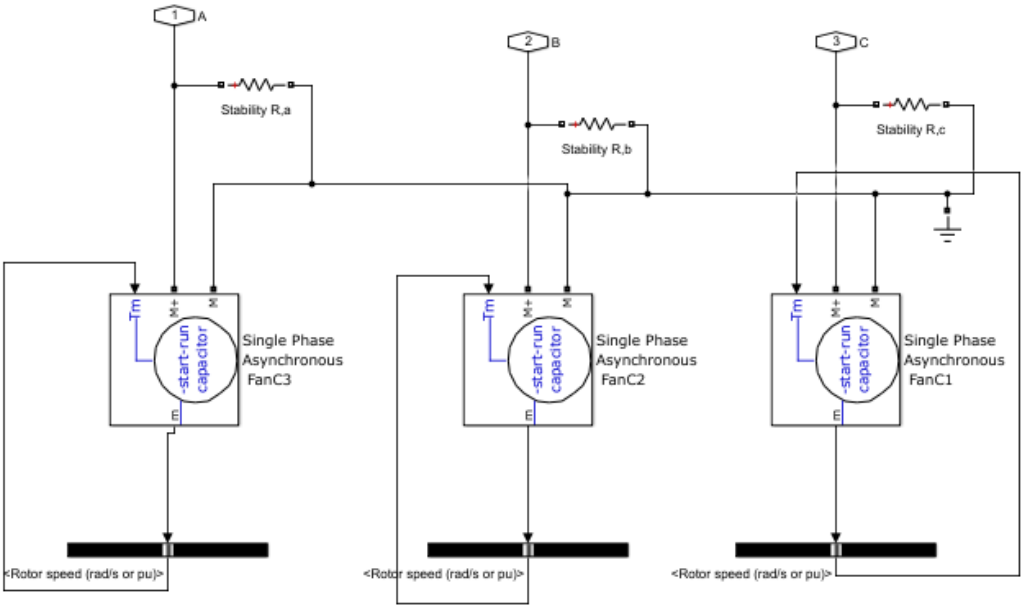

Figure 38. 3 single phase asynchronous machines.

3.7 Nonlinear Load Model

Single phase nonlinear loads such as personal computers generate odd harmonics. Three-phase nonlinear loads such as 3-phase DC drives, rectifiers etc., generate primarily 5^{th} and 7^{th} harmonics and lesser amount of 11^{th} and 13^{th} [42].

CHAPTER 4 SYSTEM STUDIES

This chapter starts with a detailed description of the employed testbed and selected parameters. Then, the simulation procedure as well as various scenarios and case studies are presented. The results of sensitivity analysis using these scenarios are provided and discussed.

4.1 Testbed Details

The feeder model used here is shown in Figure 39. It is based on the IEEE 13-bus Test Feeder [41]. The model was built in MATLAB Simulink version 2016b. The feeder operates at 4.16 kV with two capacitor banks, a 3-phase 600 kvar bank and a 100 kvar single-phase bank on phase C. Three PV locations exist which are labeled PV1, PV2, and PV3. The orange blocks are configurable loads. The total connected load (TCL) for the model is 12.173 MVA with 3.980 MVA, 3.701 MVA, and 4.492 MVA connected to phases A, B, and C respectively. Transformers are shown as green color with configurations and ratings shown and discussed in Chapter 3. The blue color blocks are for V-I measurements. Three PV plants were used in the modeling scenarios. Each PV plant was rated at 1000 kW and was configured as shown in Figure 39 unless otherwise noted.

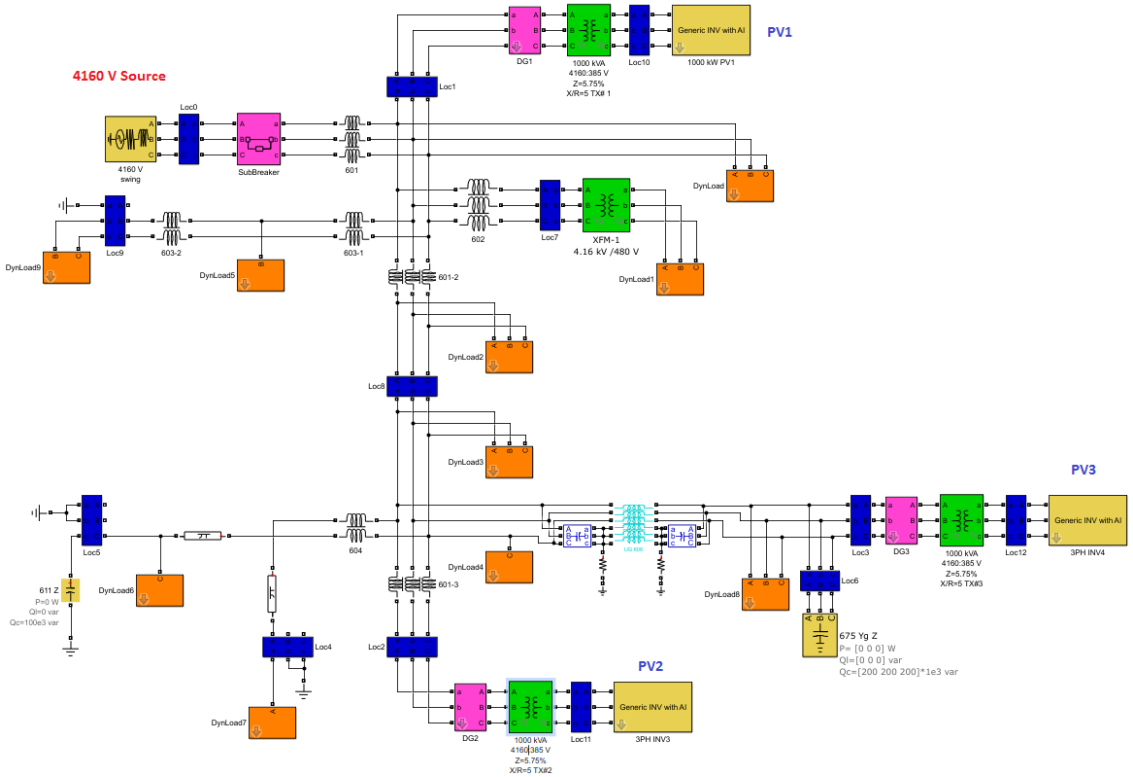

Figure 39. IEEE 13 bus test system feeder model used in this thesis [41].

The relay settings used in these plants are provided in

Table 5 through Table 8. IEEE 1547-2018 standard categorizes the required response of a DER to the abnormal conditions of its connected grid [13]:

- Category I is based on essential bulk power system (BPS) stability/reliability needs and is reasonably attainable by all DER technology that are in common usage today.

- Category II covers all BPS stability/reliability needs and is coordinated with existing reliability standards to avoid tripping for a wider range of disturbances of concern to BPS stability.

- Category III is based on both BPS stability/reliability and distribution system reliability/power quality needs and is coordinated with existing interconnection requirements for very high DER penetration.

These categories specify the range of allowable settings of control or trip parameter values. Categories with higher numbers are capable of meeting voltage and frequency ride-through requirements. The relay settings used in this thesis are compliant with either IEEE 1547-2018 Category III ride-through recommendations or Category II recommendations [13]. In any given simulation case, all PV plants had the same relay settings. In addition to the relays set by the user, inverters have internal self-protection overvoltage (SPOV) and self-protection overcurrent (SPOC) mechanisms that protect the inverters against damaging transients.

Table 7 shows the settings for the SPOV mechanism. Because SPOC mechanisms vary quite widely among manufacturers and these mechanisms are difficult to witness-test, SPOC is disabled in the models used in this work. The generic inverter also includes a rate-of-change-of-frequency (ROCOF) relay that complies with the IEEE 1547-2018 Category II requirement [13], which states that the ROCOF relay trips on a frequency rate of change that averages 2 Hz/sec or more over a minimum window time of 0.1 s—in other words, a trip is issued if abs (avg (df/dt)) ≥ 0.2 Hz runs over the 0.1 s window. The sampling rate of the ROCOF relay is 1 kHz, and the source of the frequency measurement is the inverter's PLL.

Table 5. Relay settings for PV plants in Cat III.

Element	Pickup Range	Time Delay
UNDERVOLTAGE (27)	0.5 pu	1 sec
UNDERVOLTAGE (27)	0.7 pu	10 sec
UNDERVOLTAGE (27)	0.88 pu	20 sec
OVERVOLTAGE (59)	1.1 pu	12 sec
OVERVOLTAGE (59)	1.2 pu	0.16 sec
UNDERFREQUENCY (81U)	56.5 Hz	0.16 sec
UNDERFREQUENCY (81U)	58.8 Hz	299 sec
OVERFREQUENCY (81O)	61.2 Hz	299 sec
OVERFREQUENCY (81O)	62.5 Hz	0.16 sec

Table 6.Relay settings for PV plants in Cat II.

Element	Pickup Range	Time Delay
UNDERVOLTAGE (27)	0.3 pu	Inst
UNDERVOLTAGE (27)	0.45 pu	0.16 sec
UNDERVOLTAGE (27)	0.65 pu	0.32 sec
UNDERVOLTAGE (27)	0.765 pu	4 sec
UNDERVOLTAGE (27)	0.88 pu	5 sec
OVERVOLTAGE (59)	1.1 pu	1 sec
OVERVOLTAGE (59)	1.15 pu	0.5 sec
OVERVOLTAGE (59)	1.175 pu	0.2 sec
OVERVOLTAGE (59)	1.2 pu	0.16 sec
UNDERFREQUENCY (81U)	57.0 Hz	0.16 sec

UNDERFREQUENCY (81U)	58.8 Hz	299 sec
OVERFREQUENCY (81O)	61.2 Hz	299 sec
OVERFREQUENCY (81O)	62 Hz	0.16 sec

Table 7. SPOV settings for PV plants in Cat II and Cat III

Element	Pickup Range	Time Delay
SPOV	1.4 pu	1 ms

Table 8. ROCOF Relay settings in Cat II cases

Element	Pickup Range	Time Delay
Rate-of-change-of-frequency	2 Hz/sec	0.1 sec

In this thesis, two AI Groups were studied: Group 2A and Group 2B. These two Groups were selected because of the active anti-islanding methods available in the developed block in MATLAB, these two are among the most commonly-used groups in industry [31]. The parameters used for the Group 2A inverters are shown in Figure 40, and those for the Group 2B implementation are given in Figure 41. The volt-var and frequency-watt functions were "off" in all cases. In all of the tests for each Case described below, all PV plants used the same AI method. This work did not consider mixtures of AI methods as that factor has been studied and described elsewhere [19].

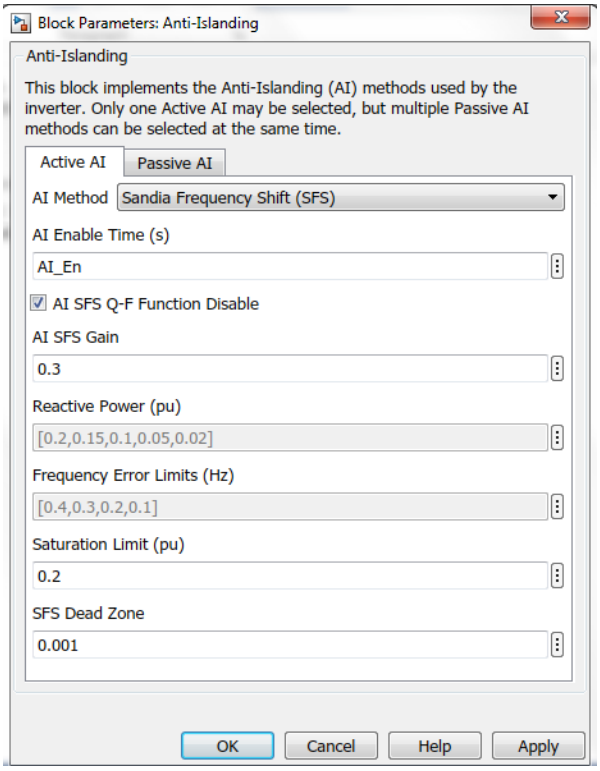

Figure 40. Parameters used for Group 2A AI implementation.

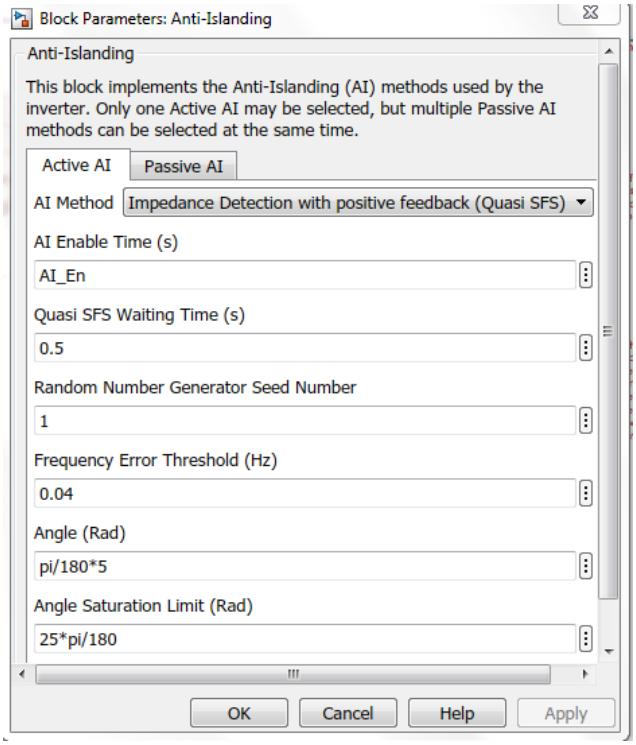

Figure 41. Parameters used for Group 2B parameter implementation.

The mechanical load (torque) on the motor is proportional to the motor rotational speed, such that 1 per unit speed results in 1 per unit (rated) torque. The parameters of this motor model are given in Figure 42.

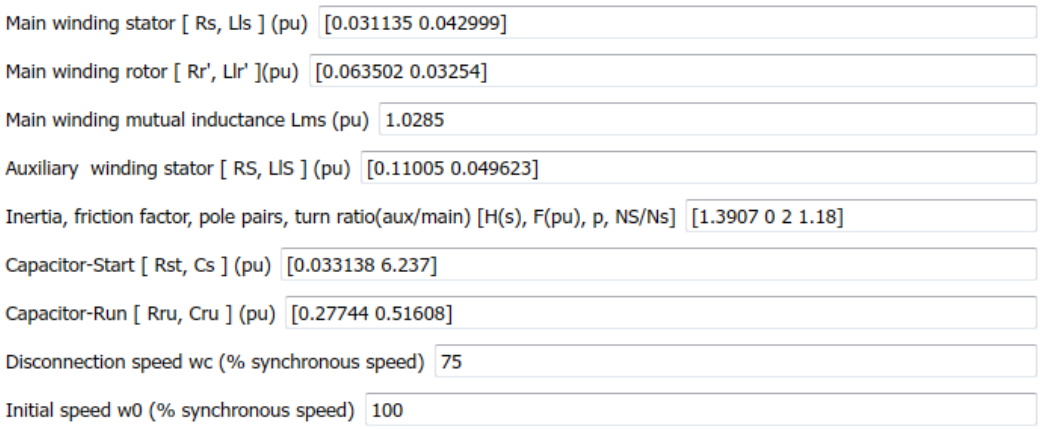

Figure 42. Parameters for single-phase motor load model.

One factor examined in this work was the sensitivity of ROTs to PQ loads. Because the PQ load blocks are offsetting standard constant-impedance blocks, it was decided to maintain the reactive portion of the load, hence the nq equals to 2. The np value of 1.3 sets off the real power demand of the PQ block to represent a combination of ~1/3 constant-power load and 2/3 constant-impedance load over a voltage range between 0.9 and 1.05 pu.

Another factor examined in this work was the sensitivity of ROTs to the presence of nonlinear loads, or more specifically harmonic current injections. To represent these, sensitivities current sources were used to add 3rd, 5th, and 7th harmonic injections. The phase angles of the harmonic loads were set according to the harmonic's sequence order, with the A-phase harmonic current in phase with the A-phase harmonic voltage at the

injection point. Two levels of harmonic injection were studied: one in which the peak amplitudes of each of the harmonics sums to 4% of the load peak current, and one in which that value was 8% of the load peak current. The 4% is the maximum current distortion limit introduced in IEEE 519-2014 [43] and 8% was selected to test the sensitivity of the results to the harmonic increase. Each of the three harmonics were given an equal share of the peak current value, either 1.333% or 2.666% in the two cases.

For this work, the values used for the constant power load exponents np and nq were np = 1.3 and nq = 2. The nq = 2 value causes the reactive power to behave as a constant reactance (i.e., not constant Q; the Q will vary with the square of voltage).

4.2 Simulation Procedure

The standard procedure for a risk-of-islanding study is to first select a breaker, switch or other device that can form an island that includes the DG under study, loads, and a var source. Then, the balance point is found at which the output of all real and reactive power sources in the island matches the total real and reactive demand of the loads in the island. Once the balance point is located, a batch-mode coarse-resolution sweep is run over a small range of loading fractions (LFs) and power factors (PFs). LF is given as a percentage of the total connected load (TCL), which for the test feeder used here is 12.173 MVA. The PF values given are the uncompensated PF values which are the values of the R-L loads, but without the utility capacitors included. Thus, the PF that is being varied in these simulations is that of the load and feeder only, excluding the capacitors. The commanded PF of the load becomes less reflective of the true power

factor of the system when the load is comprised of a portion of either motor or harmonic loading, because: a) the motor power factor is determined by its operating state and is not directly controlled by the "PF" variable; and b) the "PF" variable adjusts the displacement power factor, but the harmonic load contributes to the distortion power factor, which is independent of the "PF" variable. In these cases, sample points were investigated to determine more accurately the true power factor of the system load. The load is distributed throughout the circuit as described in the original IEEE 13-node test circuit [41]. The loading data given in the original model is assumed to be peak loading of the circuit. These peak values were multiplied by three to increase the peak rating of each load for a total connected load of 12.173 MVA. Batching of a model works best when referencing the total connected load of the system. For reference then, the peak loading of the system would be at a LF of 40%. For all LF and PF pairs in the batch, a simulation is run in which an island is formed without a fault by opening the breaker shown in Figure 39, and the resulting ROT[1] of the DG plant, defined as the time from switch opening to plant shutdown, is recorded. PF and LF values are increased with 0.01 steps. The coarse resolution allows the batch to be run in a reasonable length of time, and facilitates the location of the edges of any none-detection zone (NDZ) that may exist. A flowchart shown in Figure 43 illustrates the simulation process.

[1] ROT = run-on time. The run-on time is sometimes called the "clearing time" of the inverters. "Run-on time" or ROT is used here because it is more physically descriptive.

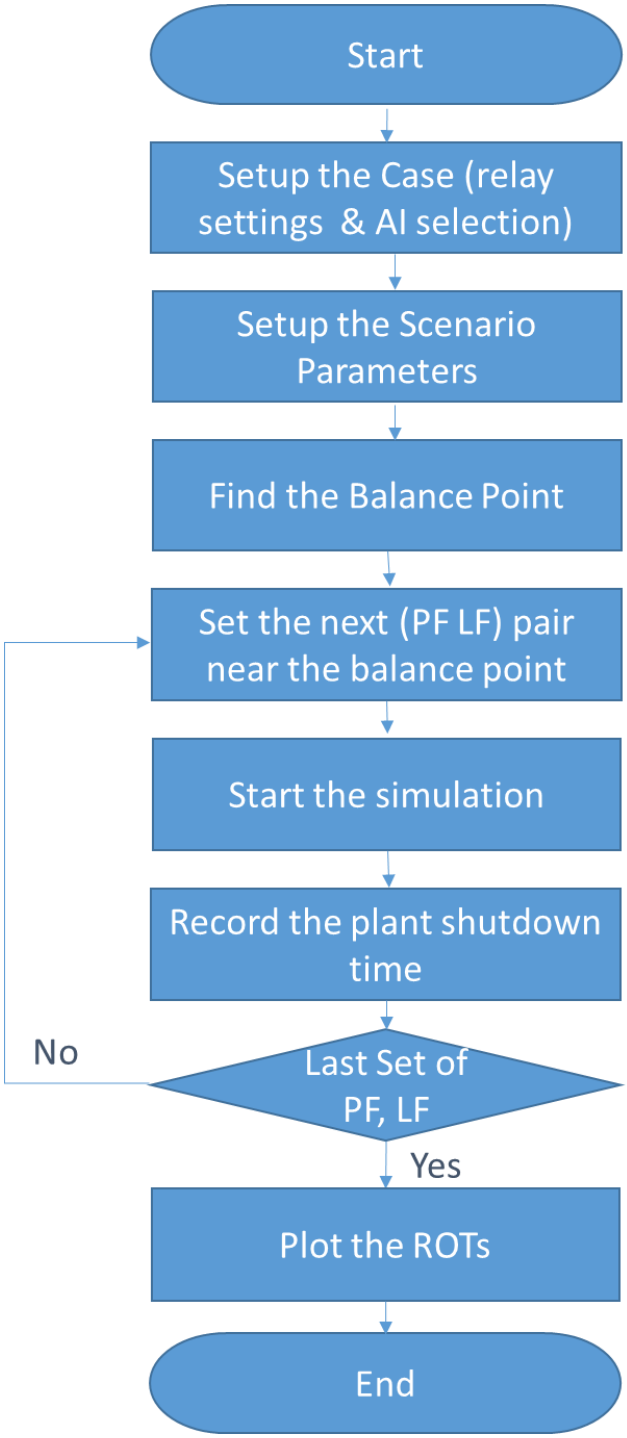

Figure 43. Flowchart of simulation process.

Sensitivity of the risk of islanding to certain key parameters was systematically investigated in the simulation. The ultimate goal was to determine to which of these parameters the inverter run-on times (ROTs) are relatively insensitive.

Initially four cases were designated to study. The four cases were considering Group 2A AI and Group 2B AI as well as Cat II and Cat III relay settings with ROCOF relay enabled. Results of the studies with Category II relay settings and with ROCOF enabled, showed that the tripping of inverters were mainly caused by ROCOF relay. In order to focus the study on the impact of relay settings and AI methods, ROCOF was disabled and Category II studies were repeated. Therefore six cases were studied in total which are summarized in Table 9. For case, nine scenarios were studied. These scenarios considered the impact of inverter location, inverter operating point, load location, load type and circuit impedance. The sensitivity of these parameters on ROTs had not been studied thoroughly in previous research. Table 10 summarizes these scenarios. The orange cells in the table highlight the difference of the corresponding scenario and the base scenario.

- Case 1. Group 2A AI with ROCOF Cat II

In this case, all PVs are using Group 2A AI and ROCOF relay is enabled.

Relay settings are set to comply with IEEE 1547-2018 Category II requirements.

- Case 2. Group 2A AI without ROCOF Cat II

In this case all PVs are using Group 2A AI and ROCOF relay is disabled.

Relay settings are set to comply with IEEE 1547-2018 Category II requirements.

- Case 3. Group 2B with ROCOF Cat II

In this case all PVs are using Group 2B AI and ROCOF relay is.

Relay settings are set to comply with IEEE 1547-2018 Category II requirements.

- Case 4. Group 2B without ROCOF Cat II

In this case all PVs are using Group 2B AI and ROCOF relay is.

Relay settings are set to comply with IEEE 1547-2018 Category II requirements.

- Case 5. Group 2A AI without ROCOF Cat III

In this case all PVs are using Group 2A AI and ROCOF relay is disabled.

Relay settings are set to comply with IEEE 1547-2018 Category III requirements.

- Case 6. Group 2B without ROCOF Cat III

In this case all PVs are using Group 2B AI and ROCOF relay is enabled.

Relay settings are set to comply with IEEE 1547-2018 Category III requirements.

Table 9. Summary of Studied Cases

Case Number	Anti-Islanding Method	Relay Standard	ROCOF
1	Group 2A	Category II	Enabled
2	Group 2A	Category II	Disabled
3	Group 2B	Category II	Enabled
4	Group 2B	Category II	Disabled
5	Group 2A	Category III	Disabled
6	Group 2B	Category III	Disabled

Table 10. Summary of Studied Scenarios in Each Case

Scenario	Inverter Locations	Each GSU and Inverter rating	Inverter Operating Point	Load Locations	Load Type	Circuit impedance
Base	PV1,PV2, PV3 POIs	1MW	100%	IEEE testbed	Constant Z (parallel R-L)	100%
1	PV1,PV2, PV3 POIs	a. 1.5 MW b. 3 MW	a. 67% b. 33%	IEEE testbed	Constant Z (parallel R-L)	100%
2	PV1,PV2, PV3 POIs	1MW	100%	PV 1&2 POIs	Constant Z (parallel R-L)	100%
3	PV1,PV2, PV3 POIs	1MW	100%	IEEE testbed	Constant Z (parallel R-L) a. Double imbalance b. no imbalance	100%
4	a. All on PV1 POI b. All in PV3 POI	1MW	100%	IEEE testbed	Constant Z (parallel R-L)	100%
5	PV1,PV2, PV3 POIs	1MW	100%	IEEE testbed	Constant Z (parallel R-L)	a. 50% b. 10%
6	PV1,PV2, PV3 POIs	1MW	100%	IEEE testbed	Of constant Z a. 33% Constant P b. 67% Constant P	100%

					c. 99% Constant P	
7	PV1,PV2, PV3 POIs	1MW	100%	IEEE testbed	Of constant Z a. 33% induction motor load b. 67% induction motor load c. 90% induction motor load	100%
8	PV1,PV2, PV3 POIs	1MW	100%	IEEE testbed	Constant Z plus 3^{rd}, 5^{th}, 7^{th} harmonics a. 4% load peak current b. 8% load peak current	100%

The nine scenarios are described further in the following:

- Scenario 0: Baseline

This is the baseline case which will be used as the basis for comparison against all other test cases. The three PV plants are each rated at 1 MW and operating a full, rated power. The loading is distributed throughout the circuit and by phase as it is in the IEEE test circuit, without modification. The circuit impedance is at 100% and a constant-Z (parallel R-L) load model is used.

- Scenario 1: Rated power output vs actual power output

The difference between scenario 1 and the baseline case is that in scenario 1 the ratings of the PV plants (inverters and GSU transformers) are increased to 1.5 MW and then 3 MW while the power output is reduced to 67% and 33% of rated capacity respectively. This way, the total output power of the PV plants is constant for all cases, but the PV plants are operating in a different part of their capacity range. This scenario

tests the impact of the PV plants operating in a lower part of their operational range on ROTs.

- Scenario 2: Distribution of the load along the circuit

The difference between scenario 2 and the baseline scenario is that the five loads at the top of Figure 39 are moved to the location of the PoI of PV1 and the rest of the loads are moved to the PoI of PV2. In this configuration, the total loading on the circuit is (approximately) the same, but the distribution of the loading is different. Thus, this case is designed to investigate the impact of the level of distribution of the load on ROTs along the circuit.

- Scenario 3: Phase-phase imbalance

The baseline scenario is not completely balanced phase-phase; the IEEE 13 bus circuit as provided contains a small level of imbalance. Thus, in scenario 3, two conditions were investigated: one in which the imbalance was removed, resulting in a nearly balanced (phase-phase) load; and one in which the level of imbalance was doubled. This case is designed to investigate the impact of phase-phase imbalance on ROTs.

- Scenario 4: Distribution of PV along a circuit

The difference between Scenario 4 and the baseline case is that all three PV plants are moved so that they all connect to the PoI of PV1, thereby investigating the impact of the distribution of PV on ROTs along the circuit. This was then repeated with all three plants moved to the PoI of PV3, so that there are test cases with the PV lumped near the

grid breaker and near furthest distance of grid breaker of the distribution feeder. Throughout Scenario 4, the three PV plant GSUs and all inverter ratings remain the same as those of the baseline scenario.

- Scenario 5: Circuit impedance

This scenario probes the impact of the impedance between inverters (or between loads) on ROTs. The difference between scenario 5 and the baseline scenario is that the impedances of the circuit conductors are all reduced to 50% of their given values, and then this scenario was repeated with all circuit impedances reduced to 10% of their original values.

- Scenario 6: Addition of constant-power loading

The difference between Scenario 6 and the baseline Scenario is that part of the constant-impedance load is replaced with constant-P load. Three percentages of PQ-block load were simulated: 33%, 67%, and 99%. This test probes the impact of the presence of constant-power load on ROTs. The reader is reminded that with the values chosen for np and nq in the PQ-load block, the reactive portion of the load remains constant-impedance, and the actual fraction of constant-power load is one-third of the fraction of PQ-block load. Based on prior results [44], it is expected that constant-power load should cause ROTs to decrease.

- Scenario 7: Addition of motor load

This test investigates the impact of induction motor load on ROTs. The difference between Scenario 7 and the baseline case is that part of the constant-

impedance load is replaced by three-phase induction motor load. Three motor-load fractions were used: 33%, 67%, and 90%. Note that in this case, the motor load is not included as part of the PF variation—that is, the power factor of the motor is determined by the motor's terminal voltage, mechanical loading, and internal parameters, and is not affected by the change in PF. Based on prior results [45] [44], it is expected that the presence of motor load will cause ROTs to increase, and the effect may be significant.

- Scenario 8: Nonlinear loading

This test probes the impact of nonlinear, current-harmonic-producing load on ROTs. The difference between Scenario 8 and the baseline case is that, in addition to the baseline scenario's impedance load, current sources are used to add 3^{rd}, 5^{th}, and 7^{th} harmonic injections to the load. Two levels of harmonic injection were studied: one in which the peak amplitudes of each of the harmonics is 4% of the load peak, and one in which that value was 8% of the load peak current. The constant-impedance load was not reduced when harmonic load was added. Prior work [44] suggests that harmonic-current-producing load will have only a minor impact on ROTs.

4.3 Results for Case 1, Group 2A AI with ROCOF Cat II

This section contains the results obtained with all PVs using Group 2A AI, for all nine scenarios (scenario 0 through 8), with ROCOF relays enabled. Figure 44 shows a summary of the longest ROTs found for each scenario. The ROTs vary slightly over the entire set of simulations; the shortest ROTs are 100 ms, and the longest 150 ms. From Figure 44, the following conclusions can be drawn:

- The addition of motor load did increase the ROTs. The trend was monotonic with increasing motor load fraction.
- Variations in the distribution of load along the circuit and in the PV output power level did not impact ROTs.
- For the phase-to-phase imbalance, DG location, conductor impedance, constant-P load fraction, and nonlinear loading, the differences between the baseline scenario and the experimental scenarios are statistically insignificant and show no clear trend.

The key reason for the tight clustering of the ROTs is the ROCOF relay. For nearly all of the data points tested with Group 2A AI, the ROCOF relay was the reason for tripping of the PV plants. This is a significant finding which indicates that a Category II IEEE 1547-2018-compliant ROCOF relay can still be a powerful tool in ensuring adequate anti-islanding protection, when used in conjunction with Group 2A AI. However, the ROCOF relay's effectiveness masks the impact on ROTs of varying the study parameters.

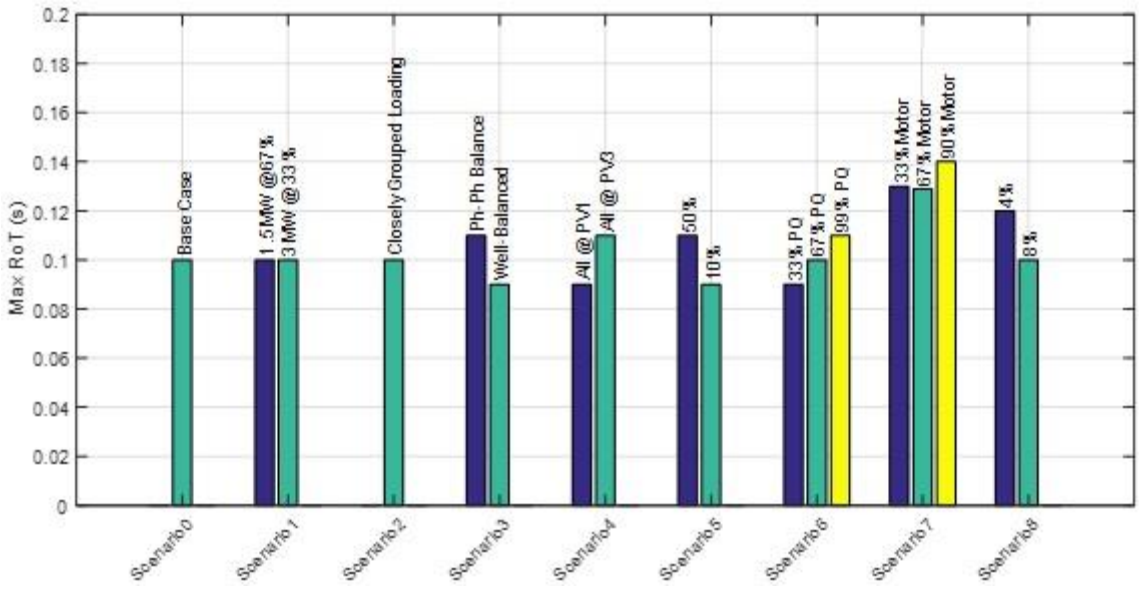

Figure 44. Summary of results using Group 2A anti-islanding.

Figure 45 and Figure 46 show the surface plot of ROTs for PV1 for base and seventh scenario as defined in Table 10 from a top-down angle, and with symbols superimposed to indicate the reason for trip at each value of load fraction and power factor: a dot "." indicates an over/underfrequency trip, a vee "v" indicates an under/overvoltage trip, a tilde "~" indicates a SPOV activation, and a hash "#" indicates a ROCOF trip.

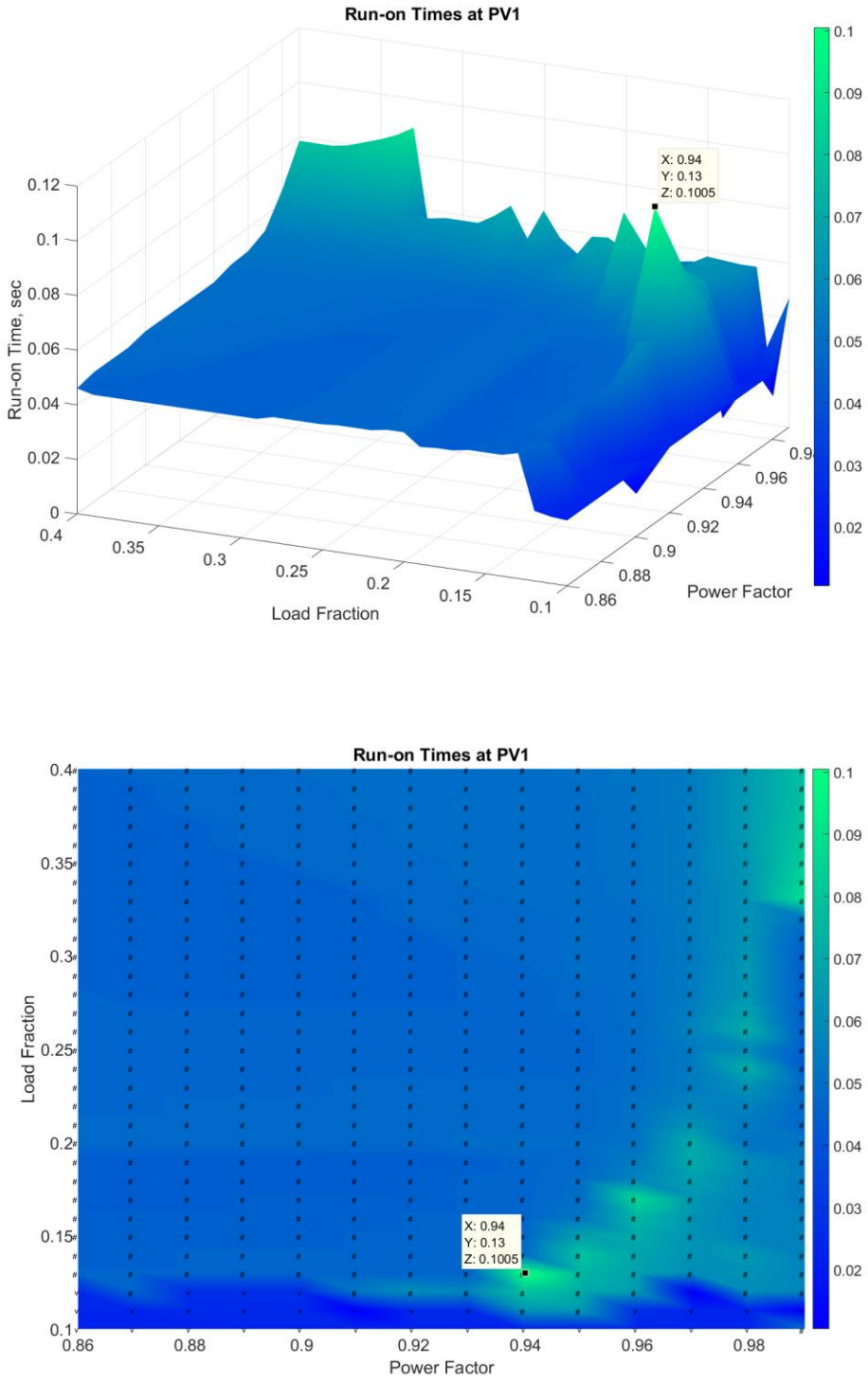

Figure 45. Surface plots of ROT of PV1 vs. LF and PF for Base Scenario: Group 2A.

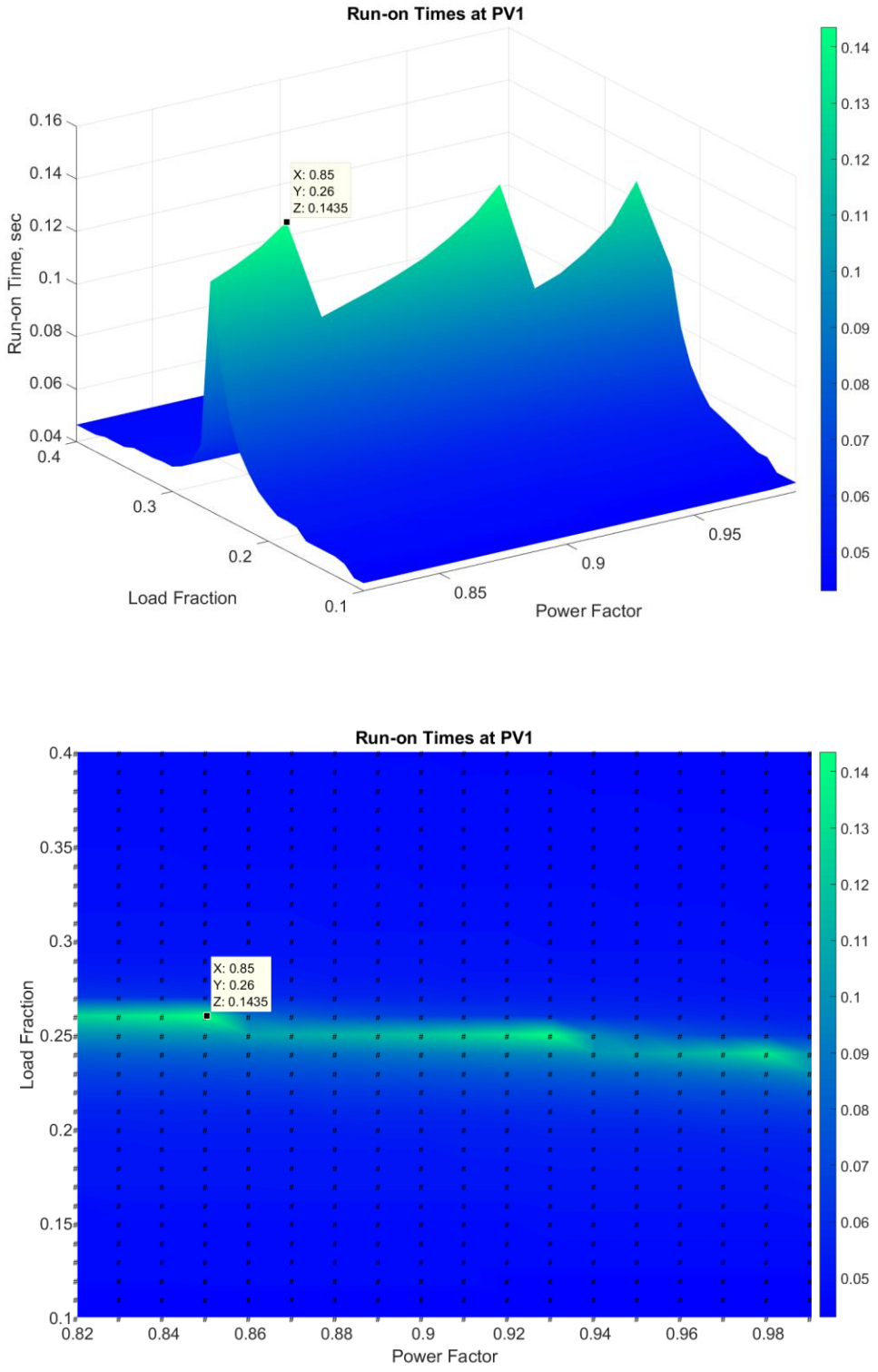

Figure 46. Surface plot of ROT of PV1 vs. LF and PF for Scenario 7: 90% motor load.

The longest ROT in the baseline scenario (scenario 0) was 0.10 s which is observed at a LF of 13% and a PF of 0.94 as shown in Figure 45. The additional figures for the rest of the scenarios show the familiar crescent-shaped "ridge" of slightly elevated ROTs that is typical for Group 2A AI. Nearly all of the points show that the reason for trip was the ROCOF relay, except along the bottom edge where at very low loading fractions there are some overvoltage trips and SPOV activations.

Figure 47 shows the voltage and frequency measured at PV1 for the longest-ROT in the base scenario. It shows that the voltage initially jumped upward, which "fooled" the PLL into seeing an initial upward jump in frequency, but eventually the fact that this island was slightly net-capacitive caused the frequency to decline. The Group 2A AI accelerated the frequency trend, triggering a ROCOF trip. Figure 48 shows the voltage and frequency for the longest overall ROT in this case, with a 0.143 s of ROT found during the Scenario 7 with 90% motor load. ROCOF was also the cause of trip in this scenario.

The crescent-shaped "ridge" of slightly elevated ROTs is present in all of the impedance load scenarios and changes minimally in the PQ load scenario, but it changes considerably in the motor load scenario (scenario 7), where the "ridge" starts to form almost a straight line. This is due to the aforementioned fact that the motor's PF is not controlled by the "PF" parameter in the simulation; the motor power factors are determined by their operating conditions, which vary only a little (probably due to slight changes in motor terminal voltage) as the constant-Z load power factor varies.

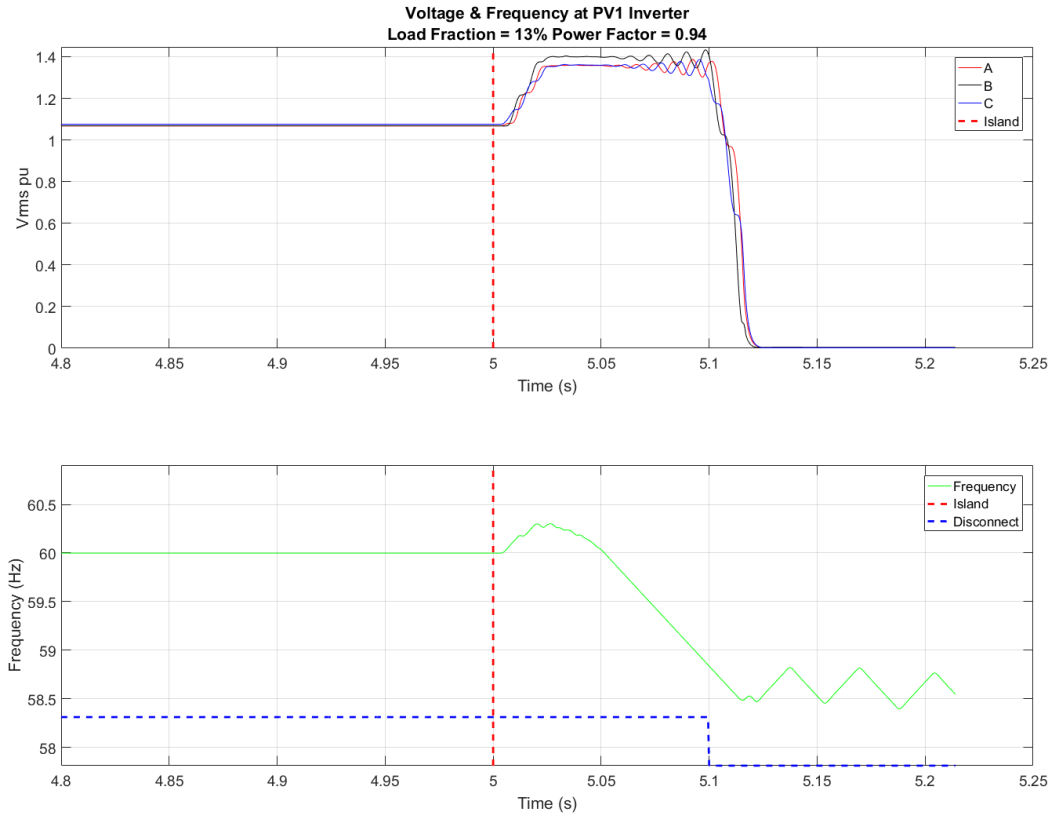

Figure 47. Voltage and frequency measured at inverters of PV1 for longest ROT of Scenario 0.

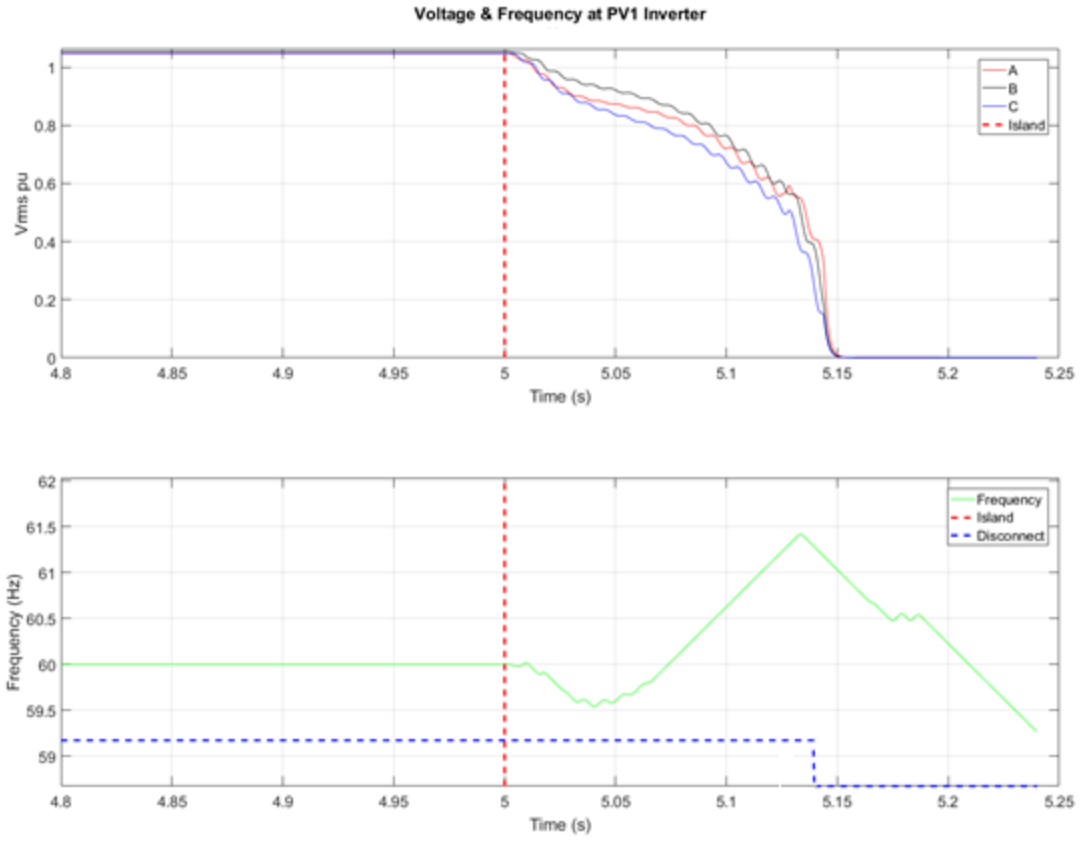

Figure 48. Voltage and frequency measured at inverters of PV1 for longest ROT of Scenario 7: 90%.

4.4 Results for Case 2, Group 2A without ROCOF Cat II

This section contains the results obtained with all PV using Group 2A AI for all nine scenarios, but with all ROCOF relays disabled. This way, any masking of results caused by the dominance of the ROCOF relay will be removed. Figure 49 shows a summary of the longest ROTs found for each scenario. The ROTs range from 140 ms up to 1.43 s with the baseline being 320 ms. This is a significant increase in ROTs from the

results in Figure 44 with ROCOF enabled. From Figure 49, the following conclusions can be drawn:

- ROTs were generally longer without the ROCOF relays.
- The factor that made the largest difference was the addition of motor load, which significantly increased the ROTs.
- The addition of constant-P loading decreased ROTs.
- The sensitivity of the ROTs to all other factors tested (irradiance level, phase-phase imbalance, DG location, interconnecting impedance, and addition of harmonic-producing load) was insignificant.

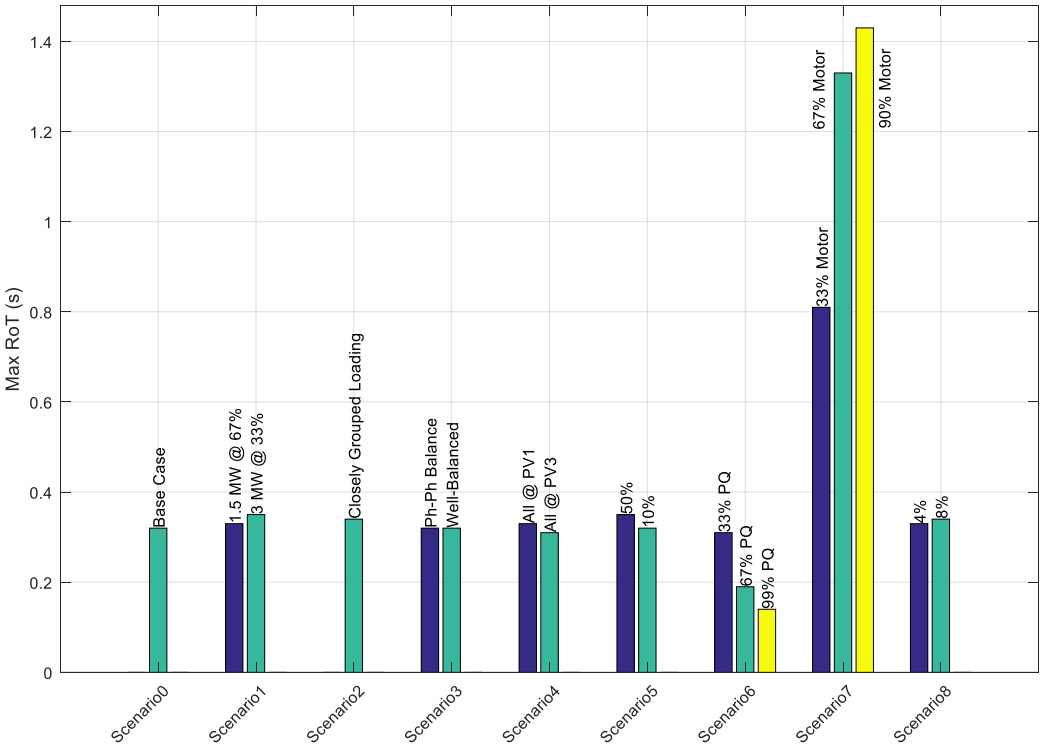

Figure 49. Summary of results using Group 2A anti-islanding without ROCOF.

Figure 50 and Figure 51 show the surface plots of ROTs for PV1 for base and max ROT scenarios shown in Figure 49. For each scenario, two figures are given. The first figure shows a perspective view of the data, with the longest ROT marked with a cursor. The second figure shows the same data from a top view, and with symbols superimposed to indicate the reason for the trip at each value of load fraction and power factor: a "." indicates an over/underfrequency trip, a "v" indicates an under/overvoltage trip, a "~" indicates a SPOV activation, and a "#" indicates a ROCOF trip.

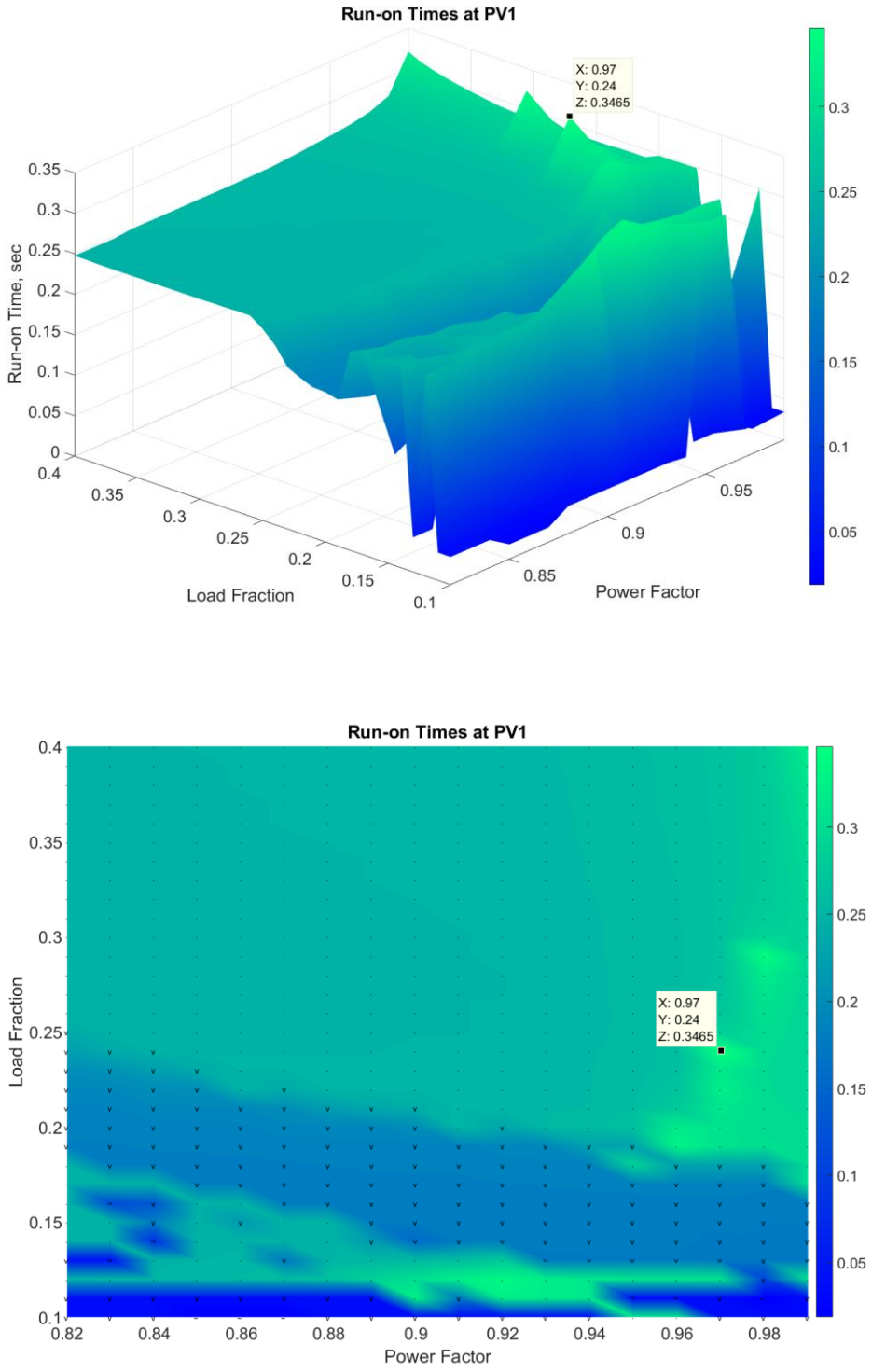

Figure 50. Surface plot of ROT of PV1 vs. LF and PF for scenario 0.

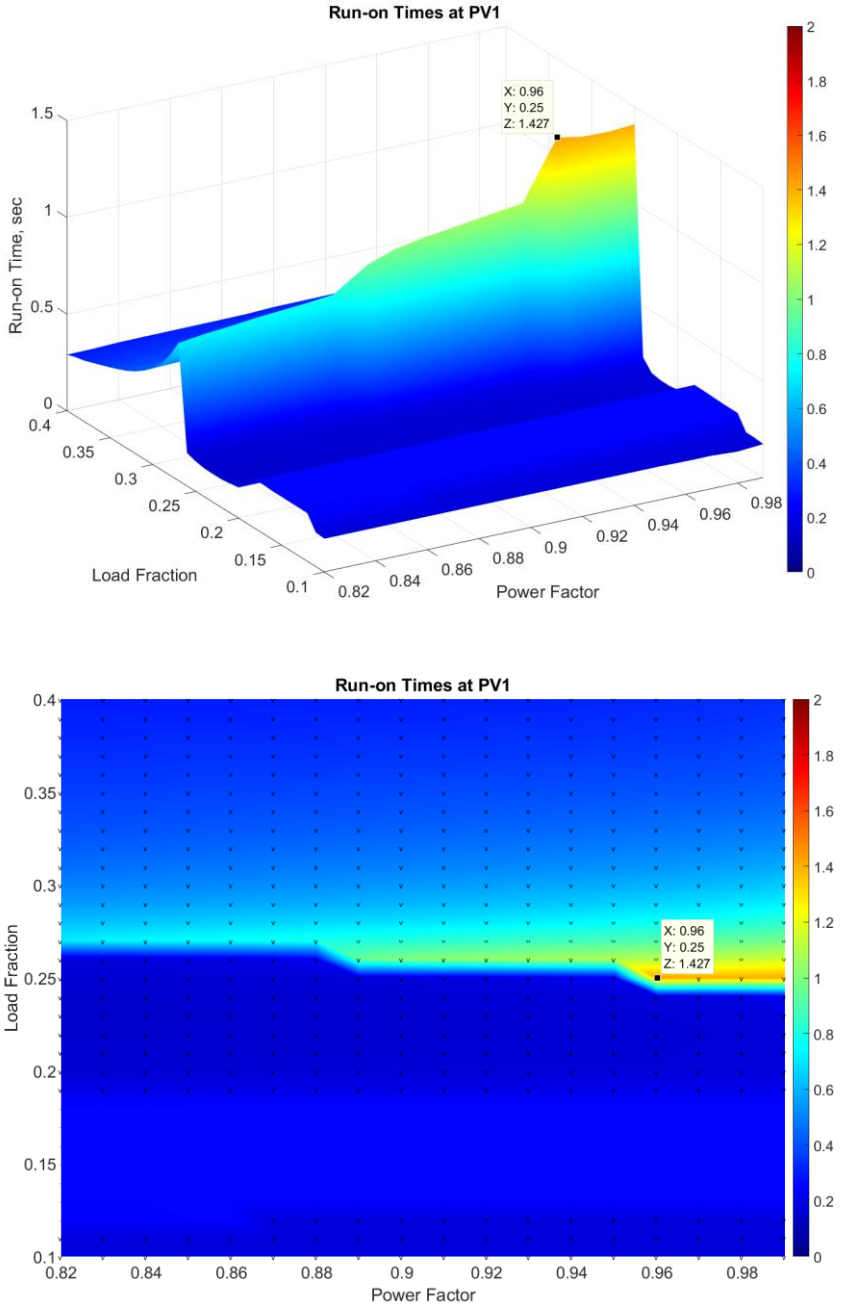

Figure 51. Surface plot of ROT of PV1 vs. LF and PF for scenario 7: 90% motor load.

4.5 Results for Case 3, Group 2B with ROCOF Cat II

This section contains results for all nine scenarios using Group 2B AI in the inverters, and with the ROCOF relays enabled in all DERs. Figure 52 shows a summary of the longest ROT observed in each scenario. The ROTs are generally higher for the Group 2B AI tests than they were for the Group 2A AI tests, which is consistent with the previous findings [19]. The ROCOF relay remains by far the dominant reason for tripping, although the fraction is not quite as high as was the case with Group 2A. The ROTs are slightly longer, and the ROCOF relay is not quite as dominant, because the Group 2B AI does not provide the same level of frequency "push" as the Group 2A AI.

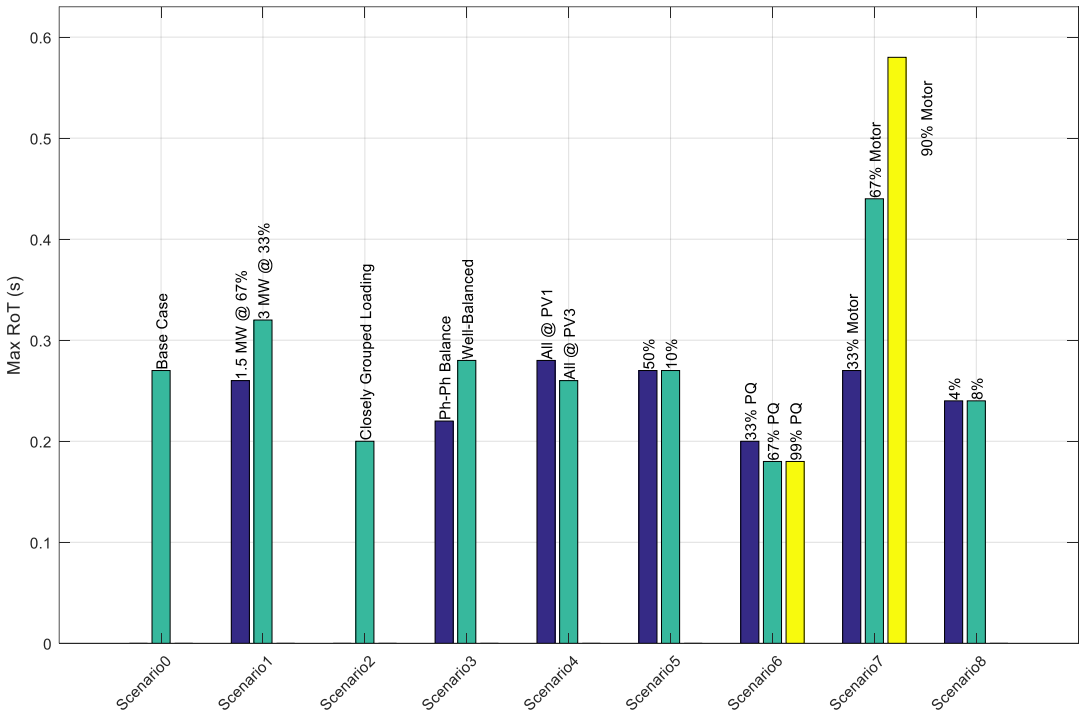

Figure 52. Summary of results using group 2B anti-islanding with ROCOF.

The maximum ROT in the baseline scenario was 270 ms. In general, the following conclusions can be drawn:

- The largest impact was seen when motor load was included, in which ROTs rose significantly and did increase continuously as the fraction of motor load was increased.
- Constant-power loading also had a significant impact, with the inclusion of constant-power load significantly reducing ROTs.
- Adding nonlinear load (harmonic current) caused ROTs to drop, although the effect was small.
- The results are inconclusive relative to phase-phase imbalance and DG location.
- Closely grouping the loading caused the ROT to decline. Past experience had led investigators to expect the opposite result [45], and this difference has not yet been fully explained.
- An initial examination suggests that ROTs also increased as the PV plant output was moved into a lower portion of the PV output range. However, closer examination of the longest ROT in this case revealed that this extended ROT is probably an outlier. It is well-known that for nearly any inverter-resident islanding detection method, if the real and reactive power in the island are balanced sufficiently close, a lengthy or even indefinite

ROT can be found. In this longest-ROT case, by the luck of the draw the conditions of LF = 34% and PF = 0.98 happened to catch a very precise balance point in which the overall system initially swings back and forth between net-capacitive and net-inductive, creating a longer ROT before the frequency ultimately rises and the island is detected. Figure 55 shows the voltage and frequency during this event. The likely reason for the increased ROT while the PV operated at a lower portion of its rated range was that the resolution of LF and PF during the batching happened to catch the absolute peak of the ridge shown in the surface plot. Thus, this increase in ROT as a function of lower PV operation range is taken to be an outlier.

Figure 53 and Figure 54 show the surface plots of ROTs for PV1 for base scenario and the seventh scenario shown in Figure 52. In the figures, the point with the longest ROT is identified by a cursor. Superimposed on these plots are symbols indicating which relay tripped at each value of load fraction and power factor: a "." indicates an over/underfrequency trip, a "v" indicates an under/overvoltage trip, a "~" indicates a SPOV activation, and a "#" indicates a ROCOF trip. Notice that because of the dynamic range seen in these results, the z-axis color scale is not the same in every surface plot.

The longest ROT in base scenario was 270 ms at an LF of 28% and a PF of 0.98. As shown in Figure 53, the longest ROT for any scenario with Group 2B AI was 580 ms, observed in Scenario 7 with a 90% motor load. The crescent-shaped "ridge" is visible

here as it was with Group 2A. As before, the vast majority of the scenarios tested tripped on ROCOF, although at lower LF values other reasons for trip also appear.

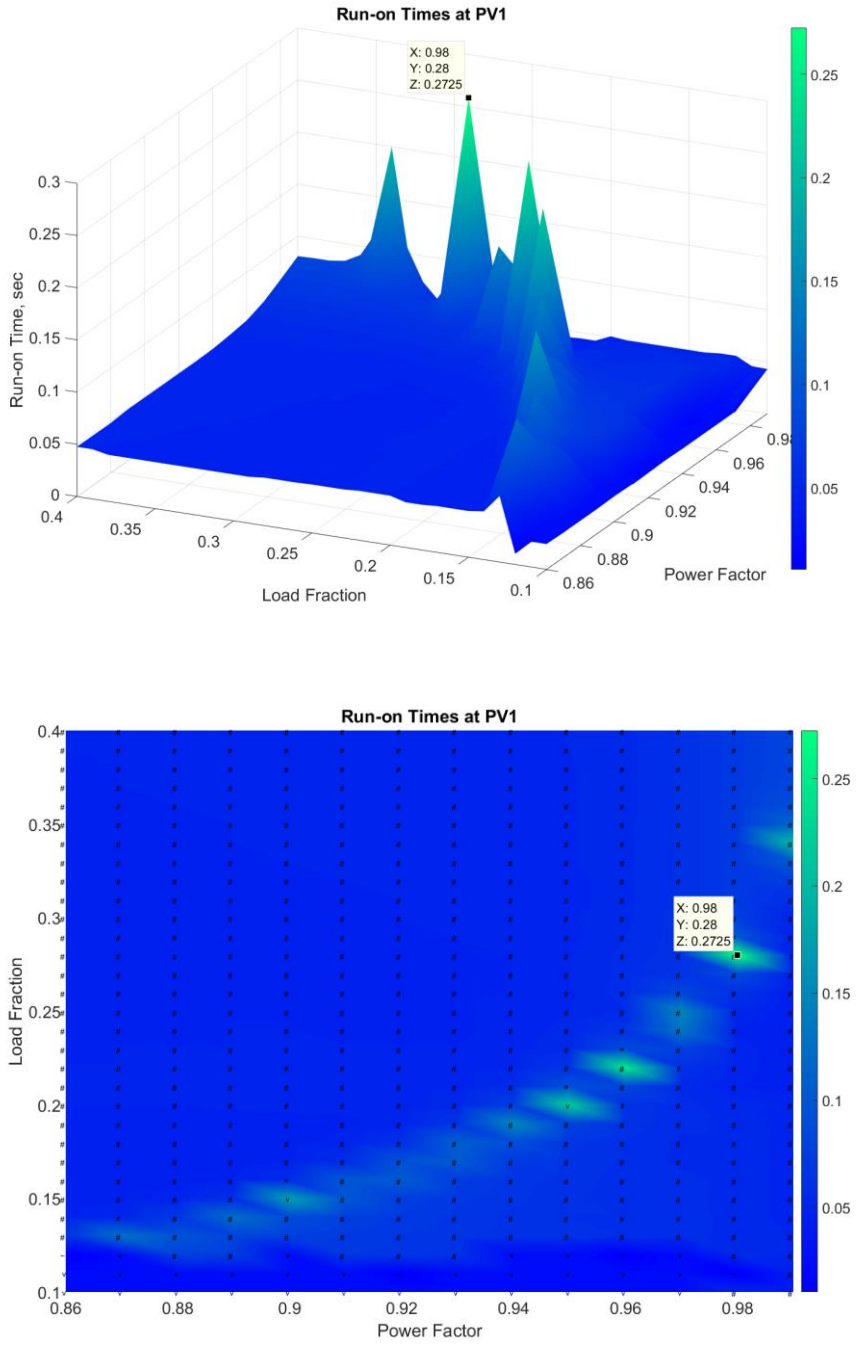

Figure 53. Surface plot of ROT of PV1 vs. LF and PF for base scenario.

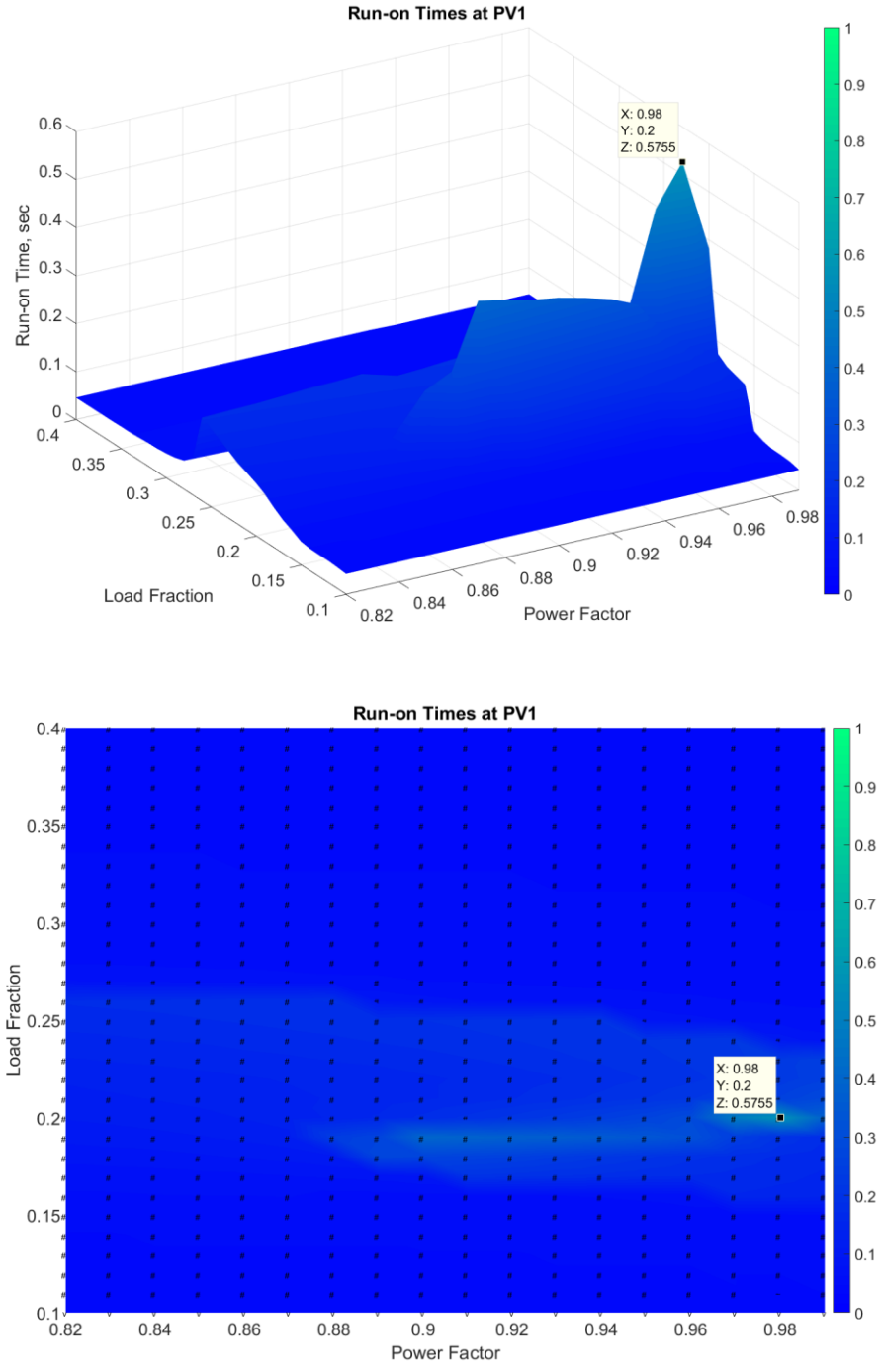

Figure 54. Surface Plot of ROT of PV1 Vs. Lf And PF for Scenario 7: 90% Motor Load.

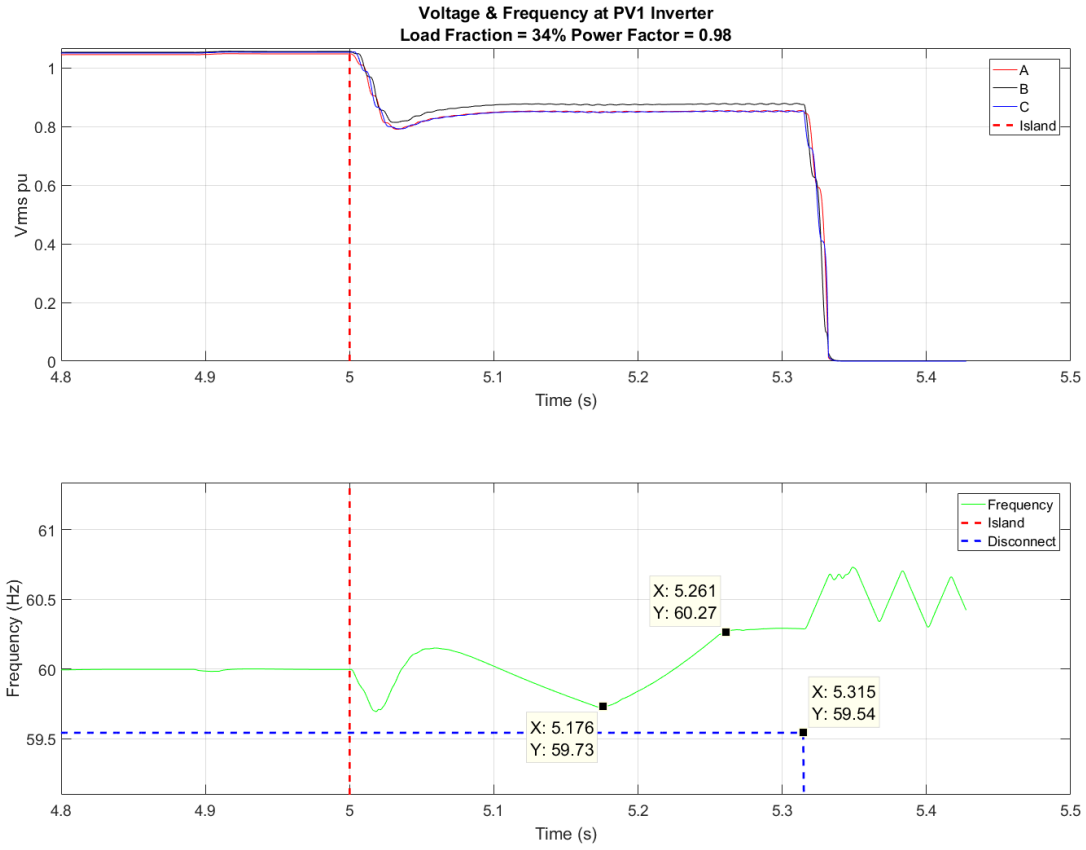

Figure 55. Voltage and frequency measured at inverters of PV1 for longest ROT of scenario 1: 33%.

4.6 Results for Case 4, Group 2B without ROCOF Cat II

This section contains the results obtained with all PV using Group 2B AI for all nine scenarios, but with the ROCOF relays disabled. Figure 56 shows a summary of the longest ROTs found for each scenario. The baseline ROT was 1.32 s, and test ROTs ranged from 250 ms up to 10 s. From Figure 56, the following conclusions can be drawn:

- ROTs were generally longer without the ROCOF relays.

- Scenario 1: As the percentage of rated power decreased, the longest ROT increased. The reader may recall that the sensitivity to this parameter was low with Group 2A AI, but Group 2B appears to be more sensitive to this factor.
- Scenario 2: Grouping the loading did cause the longest ROT to increase.
- Scenario 3: The ROT trend with phase-phase loading imbalance was inconclusive. The well-balanced load led to a considerably longer ROT than the baseline, but the load that was more unbalanced than the baseline also resulted in longer ROTs than the baseline tests.
- Scenario 4: Grouping all of the PV together at the location of PV1 (closest to substation) led to an ROT that was less than the baseline scenario, although the difference was small. However, grouping all PV at the location of PV3 (furthest location from substation) significantly increased the ROT to 3.77 s.
- Scenario 5: Both 50% and 10% conductor impedance tests resulted in longer ROTs. The 50% scenario resulted in an ROT over 4 s, the longest ROT for any scenario without a motor.
- Scenario 6: The addition of constant-P loading decreased ROTs.
- Scenario 7: The presence and amount of three-phase induction motor load can increase ROTs. The combination of Group 2B and motor loading on

the feeder in all three motor load amounts resulted in a ROT exceeding the IEEE 2013 recommended maximum of 2 s. In the 33% motor load test, the ROT reached 10 s, but based on an examination of the surface plots this is likely an outlier due to one of the simulation grid points falling onto an extremely closely-matched condition and is not indicative of an overall trend.

- Scenario 8: The harmonic injections of 4% and 8% appeared to have little effect on ROT.

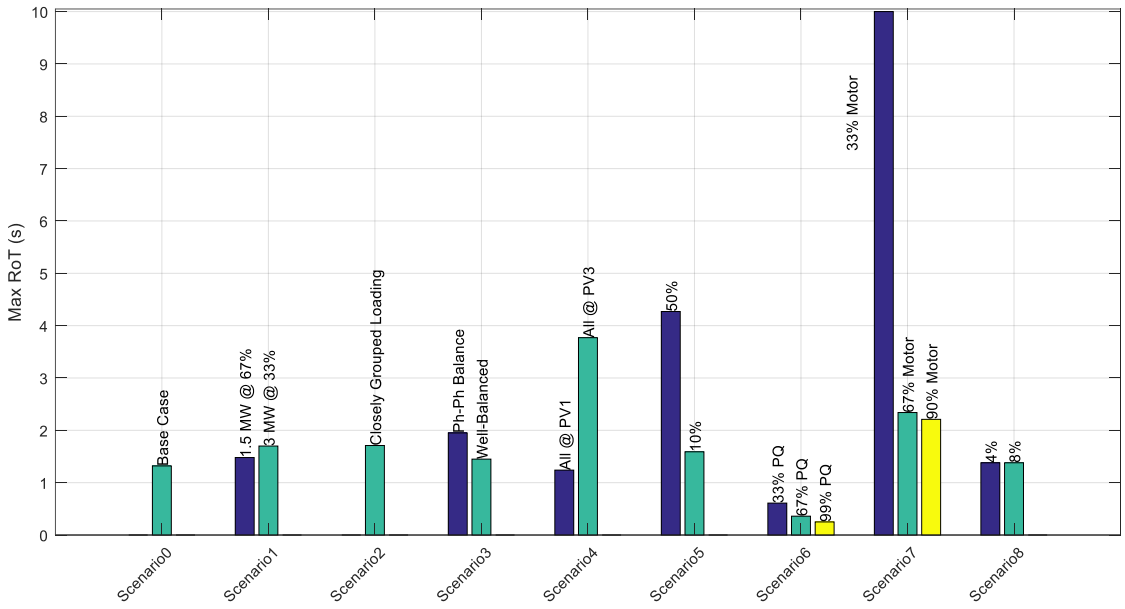

Figure 56. Summary of results using group 2B anti-islanding without ROCOF.

Figure 57 and Figure 58 show the surface plots of ROTs for PV1 for base scenario and longest instance in the seventh scenario shown in Figure 56. The longest

ROT in each figure is marked with a cursor. The figures also show a set of superimposed symbols to indicate the reason for trip at each value of load fraction and power factor: a "."indicates an over/under-frequency trip, a "v" indicates an under/overvoltage trip, a "~" indicates a SPOV activation, and a "#" indicates a ROCOF trip.

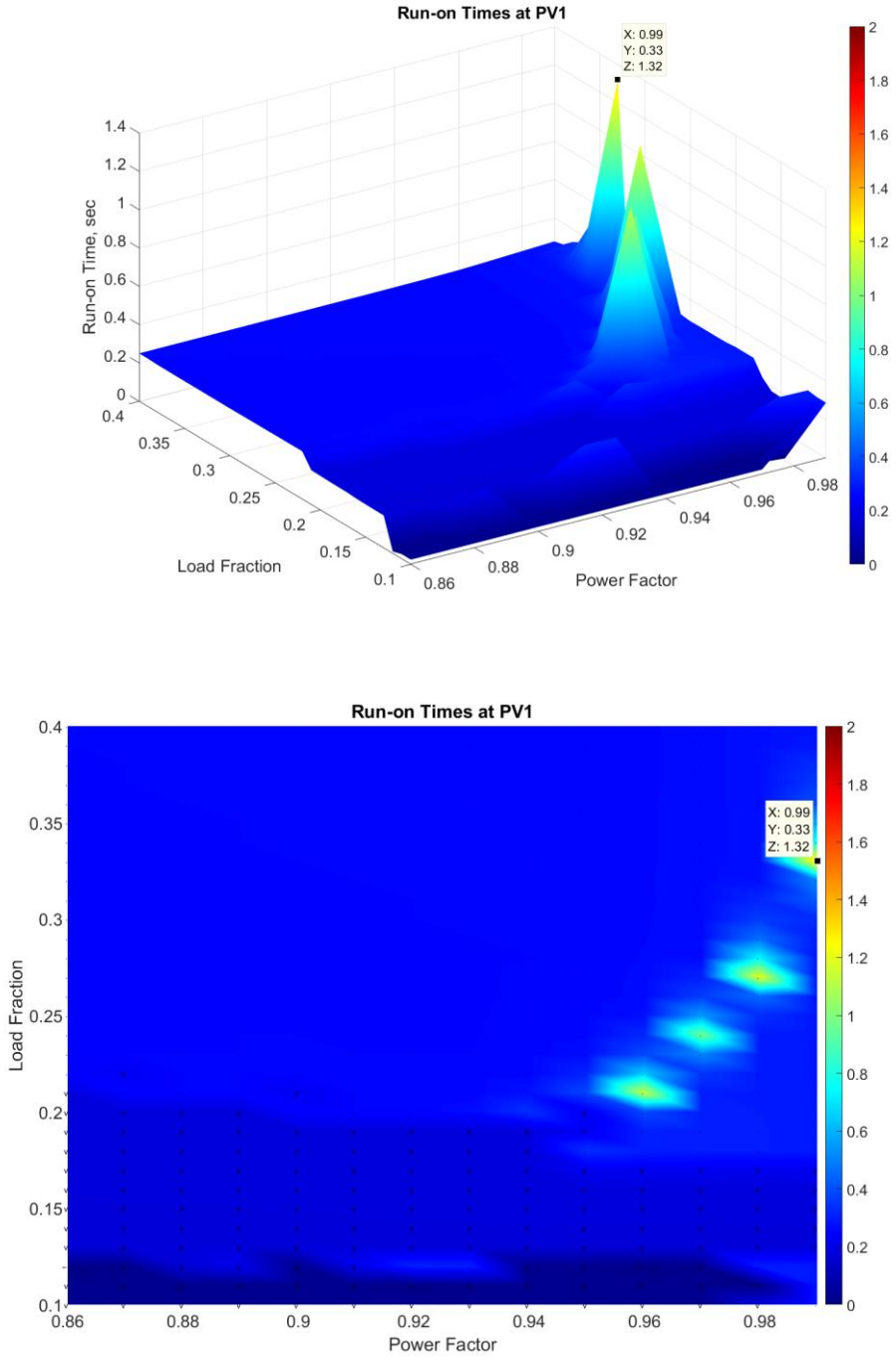

Figure 57. Surface plot of ROT of PV1 vs. LF and PF for Scenario 0: Group 2B.

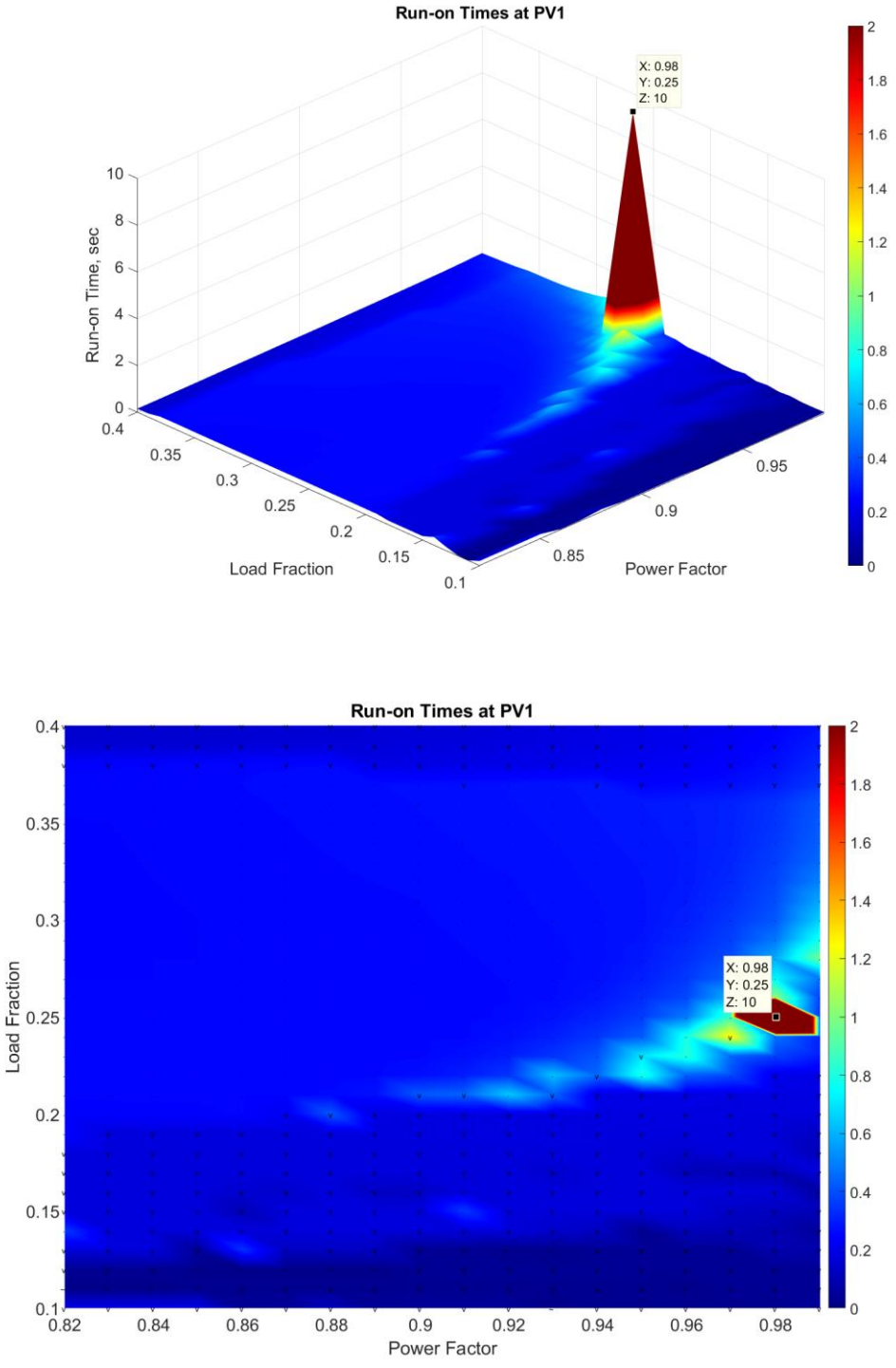

Figure 58. ROT of Group 2B PV1 vs. LF and PF for Scenario 7: 33% motor load.

4.7 Results for Case 5, Group 2A without ROCOF Cat III

This section contains the results obtained with all PV using Group 2A AI for all nine scenarios, with all ROCOF relays disabled. In this way, any masking of results caused by the dominance of the ROCOF relay will be removed. Figure 59 shows a summary of the longest ROTs found for each scenario. The ROTs range from 141 ms up to 1.676 s with the baseline being 352 ms. From Figure 59, the following conclusions can be drawn:

- The factor that made the largest difference was the addition of motor load, which significantly increased the ROTs.
- The addition of constant-P loading decreased ROTs.
- The sensitivity of the ROTs to all other factors tested (irradiance level, phase-phase imbalance, DG location, interconnecting impedance, and addition of harmonic-producing load) was insignificant.

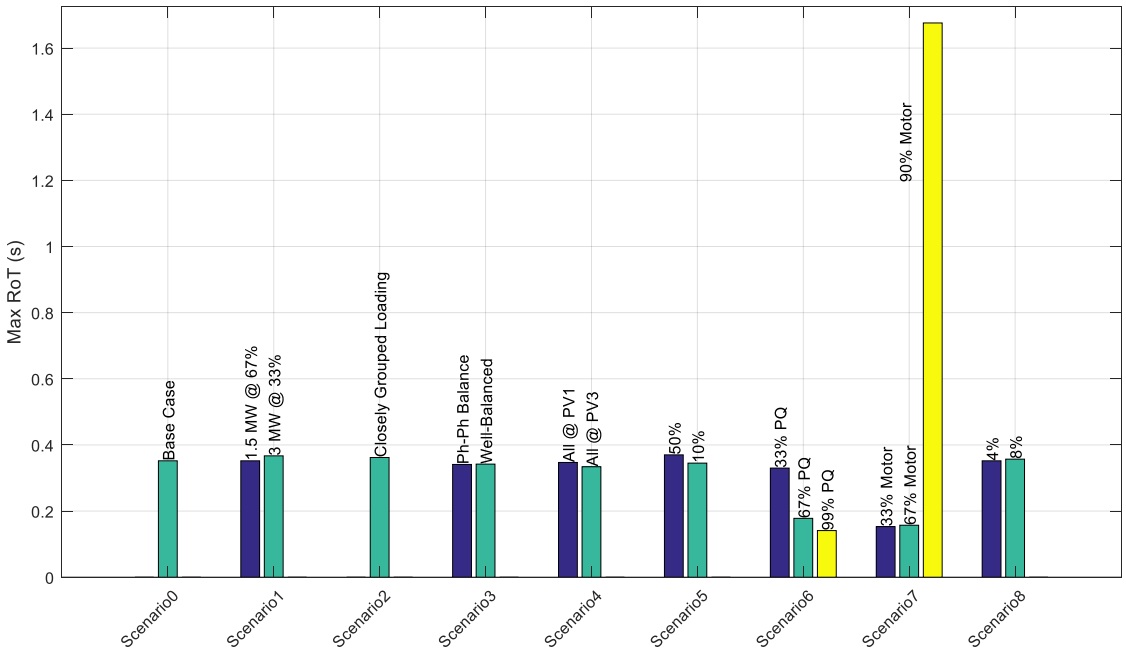

Figure 59. Summary of results using Group 2A anti-islanding without ROCOF (Cat III).

Figure 60 and Figure 62 show the surface plots of ROTs for PV1 for the base and the seventh scenario shown in Figure 59. The longest ROT in each figure is marked with a cursor. The figures also show a set of superimposed symbols to indicate the reason for trip at each value of load fraction and power factor: a "." indicates an over/underfrequency trip, a "v" indicates an under/overvoltage trip, a "~" indicates a SPOV activation, and a "#" indicates a ROCOF trip.

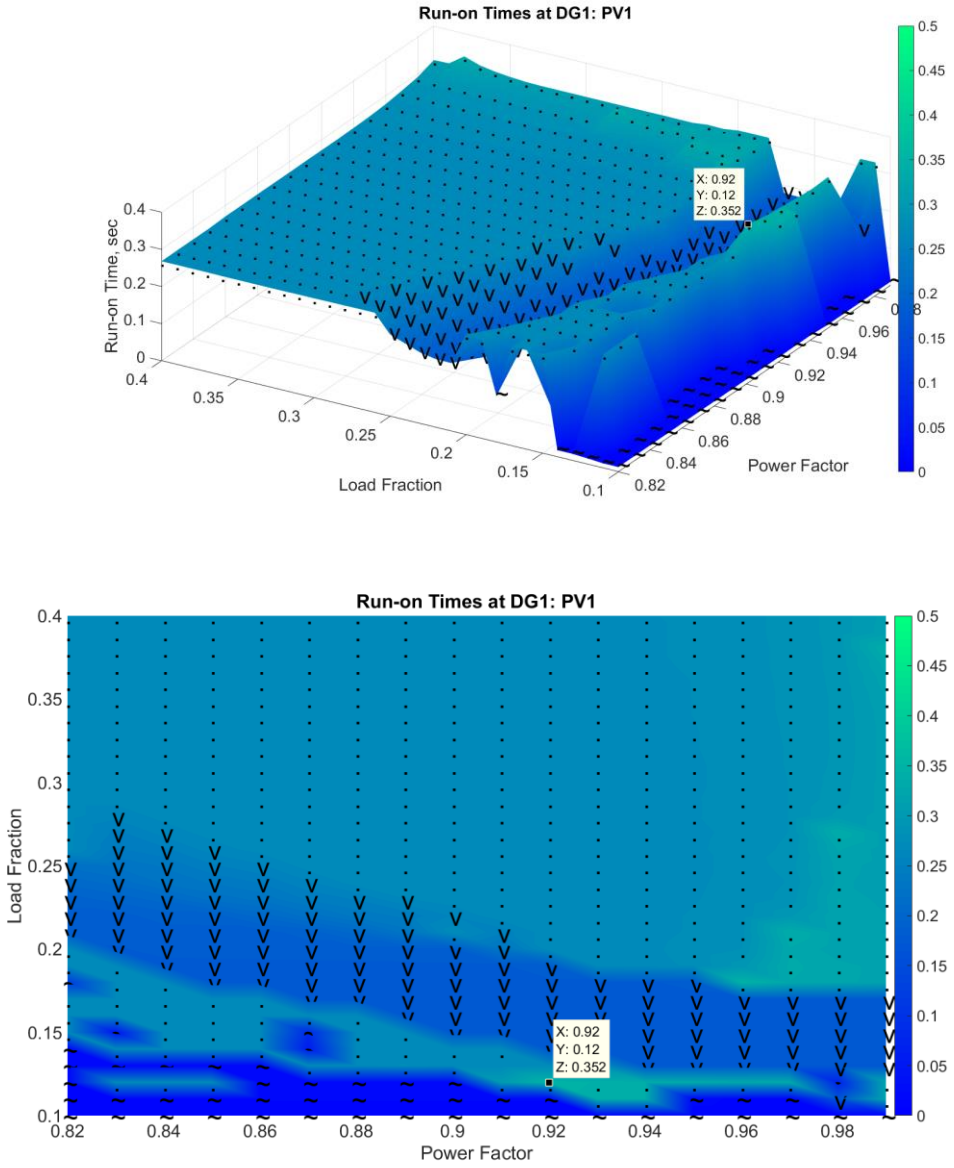

Figure 60. Surface plot of ROT of PV1 vs. LF and PF for Scenario 0: Group 2A.

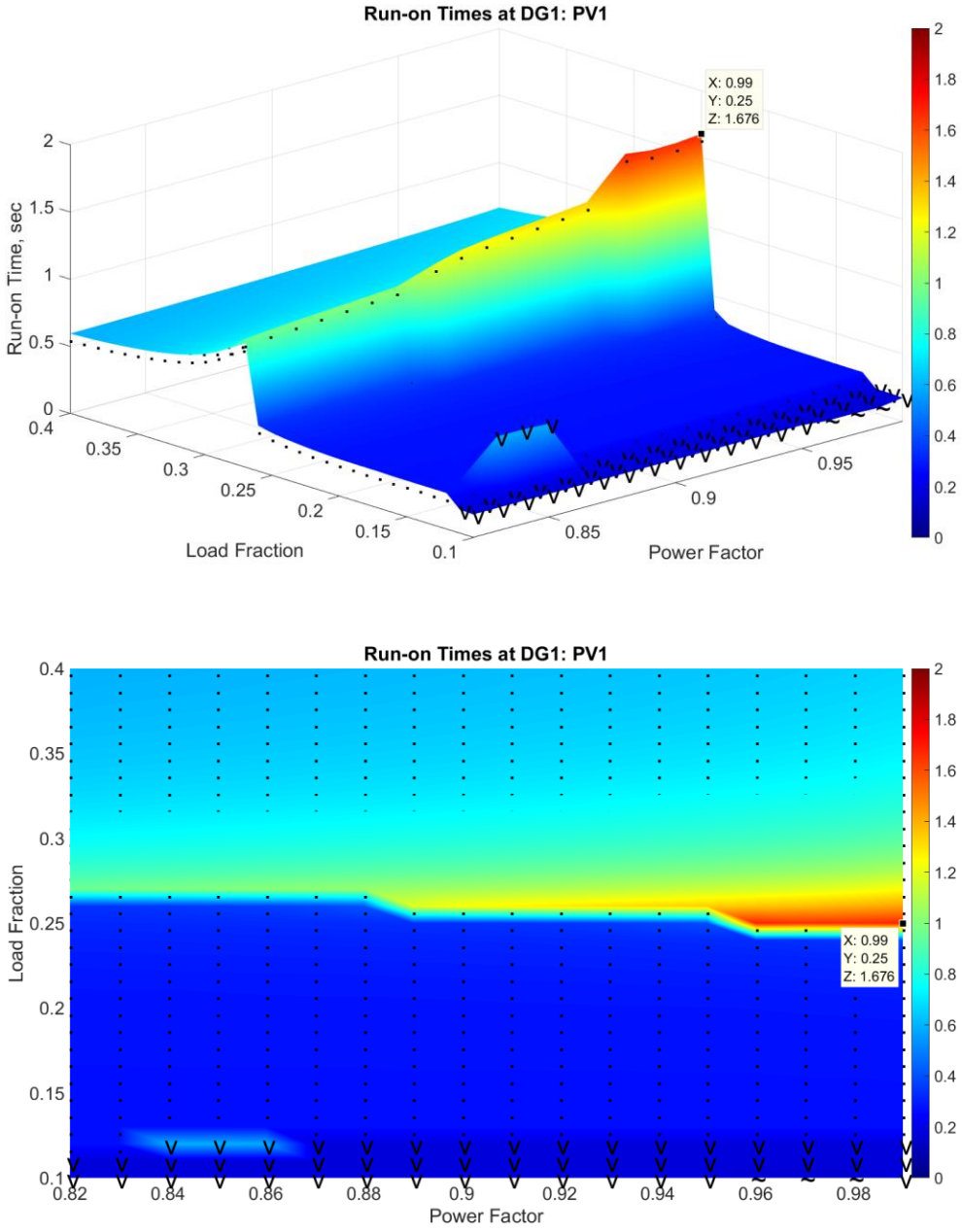

Figure 61. Surface plot of ROT of PV1 vs. LF and PF for Scenario 7: 90% Group 2A.

4.8 Results for Case 6, Group 2B without ROCOF Cat III

This section contains the results obtained with all PV using Group 2B AI for all nine Scenarios with the ROCOF relays disabled. Figure 62 contains a summary of the longest ROTs found for each scenario. The baseline ROT was 1.748 s, and resulted ROTs ranged from 233 ms up to 10 s. From Figure 62, the following conclusions can be drawn:

- Scenario 1: As the percentage of rated power increased, the longest ROT increased. The reader may recall that the sensitivity to this parameter was low with Group 2A AI, but Group 2B appears to be more sensitive to this factor. During previously tested case utilizing Category II relay settings the trend was reversed, with ROT decreasing as rated power was increased. This trend flip is due to the wider frequency ride-through settings when transitioning to Category III.
- Scenario 2: Grouping the loading did cause the longest ROT to increase.
- Scenario 3: The well-balanced load led to a longer ROT than the baseline, while the load that was more unbalanced than the baseline resulted in shorter ROTs than the baseline tests.
- Scenario 4: Grouping all of the PV together at the location of PV1 (closest to substation) led to an ROT that was less than the baseline scenario. However, grouping all PV at the location of PV3 (furthest location from substation) significantly increased the ROT to 3.944 s.

- Scenario 5: Both 50% and 10% conductor impedance tests resulted in longer ROTs. The 50% scenario resulted in an ROT over 4 s, the longest ROT for any scenario without a motor.
- Scenario 6: The addition of constant-P loading decreased ROTs.
- Scenario 7: The presence and amount of three-phase induction motor load can increase ROTs. The combination of Group 2B and motor loading on the feeder in all three amounts resulted in a ROT exceeding the IEEE 2013 recommended maximum of 2 s. In all three scenarios the ROT reached 10 s. Transitioning from Category II to Category III relay settings caused this to occur due to the much wider voltage trip settings.
- Scenario 8: The harmonic injections of 4% and 8% appeared to have little effect on ROT.

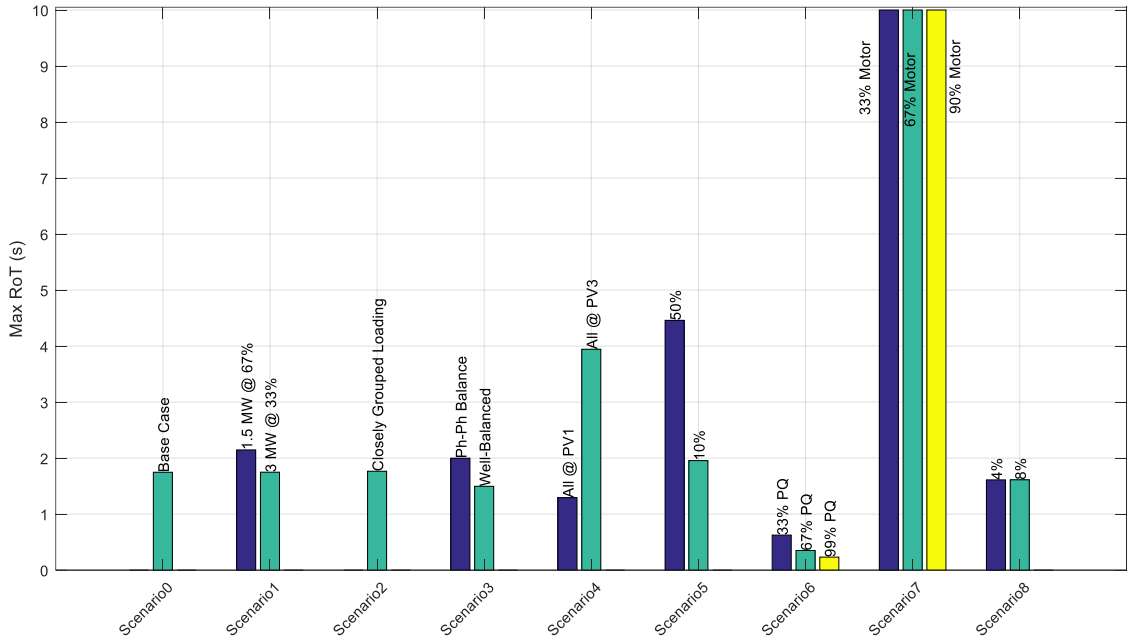

Figure 62. Summary of results using group 2B anti-islanding without ROCOF (Cat III).

Figure 63 through Figure 66 show the surface plots of ROTs for PV1 for the base and seventh scenario shown in Figure 62. The longest ROT in each figure is marked with a cursor. The figures also show a set of superimposed symbols to indicate the reason for trip at each value of load fraction and power factor.

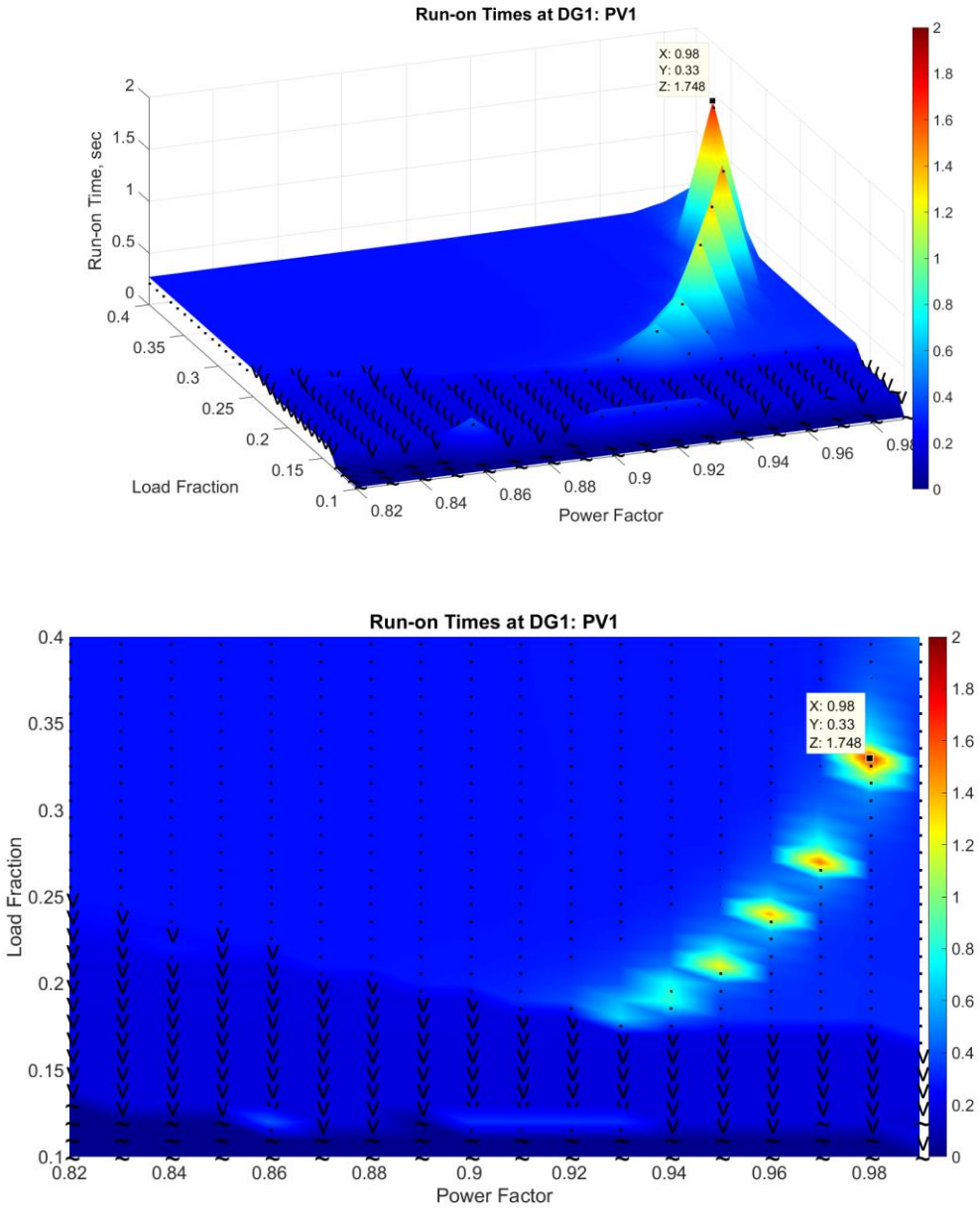

Figure 63. Surface plot of ROT of PV1 vs. LF and PF for Scenario 0: Group 2B.

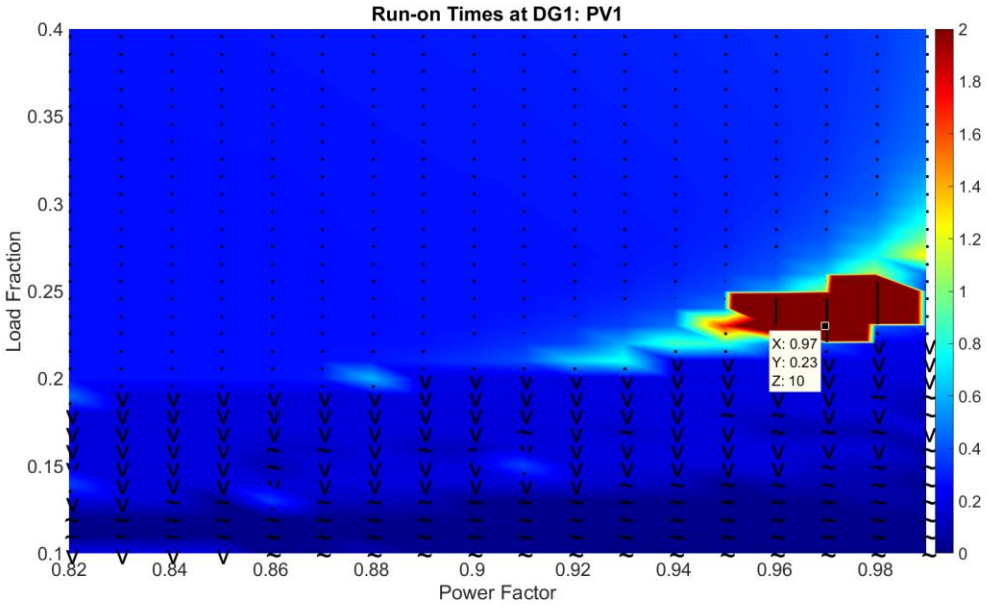

Figure 64. ROT of Group 2B PV1 vs. LF and PF for Scenario 7: 33% motor load.

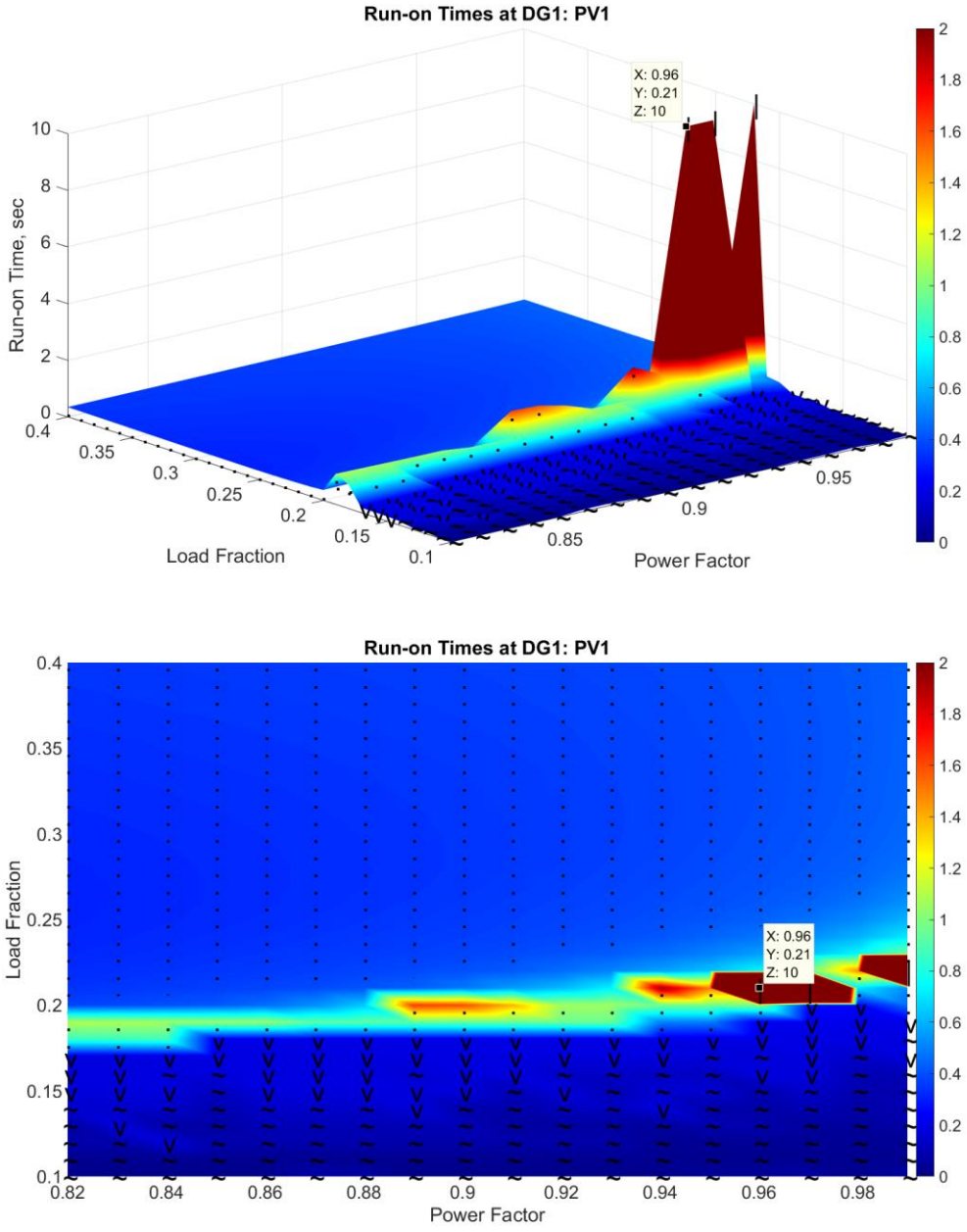

Figure 65. ROT of Group 2B PV1 vs. LF and PF for Scenario 7: 67% motor load.

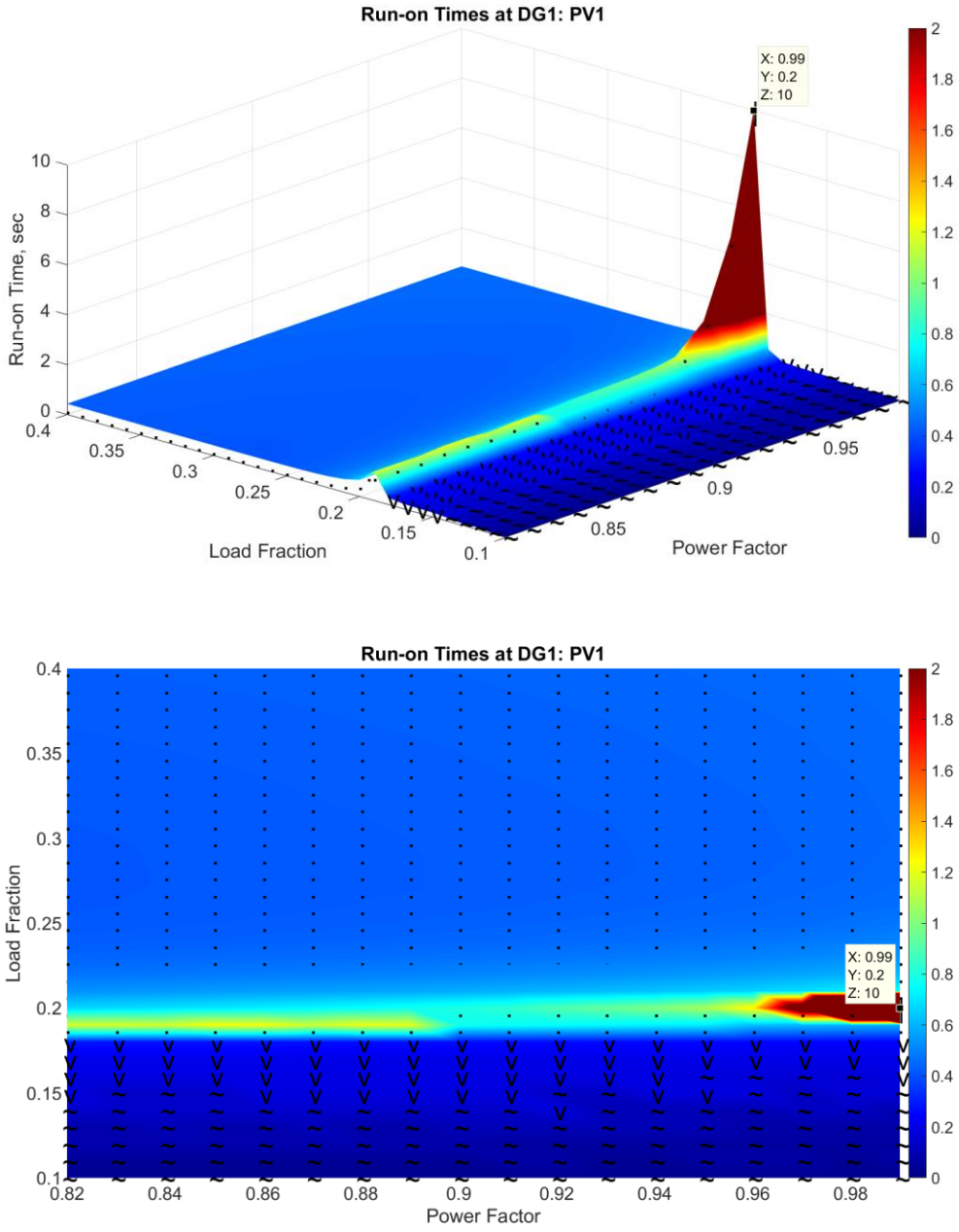

Figure 66. Surface plot of ROT of PV1 vs. LF and PF for Scenario 7: 90% Group 2B.

CHAPTER 5 CONCLUSIONS AND FUTURE RECOMMENDATIONS

Increasing trend in installation of distributed energy resources, despite of having tremendous positive effects, has created new risks in the distribution systems such as unintentional islanding. Multiple detection methods have been introduced in literature to mitigate such risks.

This chapter contains a summary of the main achievements of this work and also suggestions for future investigations. This thesis has presented a MATLAB Simulink model which contains at least one method, for each group of anti-islanding groups introduced in [19]. In addition, this thesis has thoroughly investigated the sensitivity of two anti-islanding methods to various conditions. More than 50 batches of simulations were conducted to develop the results. The results of this work lead to the following conclusions on the methods investigated.

5.1 Conclusions

In general, the transition from Category II to Category III ride-through settings led to longer maximum ROTs. The worst-case maximum run-ons were noted during motor load testing, with wider indefinite run-ons utilizing Category III compared to Category II.

Sensitivity analysis indicated that, sensitivity to irradiance level is mostly low and it depends on anti-islanding implementation.

In general, a lumped load appears to be the worst-case scenario relative to a distributed load. Thus, in anti-islanding testing and studies, a lumped load can be used as a surrogate for a more complex circuit, and should yield a conservative, worst-case result.

The level of phase-phase imbalance had little to no impact on ROTs. The impact of distribution of the PV along the circuit appears to depend on the islanding detection Group(s) represented.

It appears that the importance of circuit impedance may depend on the specific anti-islanding method used. Thus, the results are inconclusive at this time, and further investigation of this parameter, potentially combining circuit impedance with load and PV distribution variations, would be of value.

ROTs were slightly sensitive to the presence of constant-P load, with Group 2B without ROCOF showing the highest sensitivity. The addition of constant-power load to the island consistently led to a reduction in ROTs, which is consistent with prior work [44]. Thus, it can be concluded that it is acceptable to exclude constant-power load from risk-of-islanding testing or simulations.

ROTs consistently increased when motor load was present, and in general the ROTs increased with higher load fraction. These results are generally consistent with prior work on this subject [45].

The harmonic-current load in general had a negligible impact on ROTs, so the analysis suggest that ROTs are not sensitive to this parameter. This result is consistent

with prior findings [44] and suggests that it is acceptable to omit nonlinear loads from risk-of-islanding testing or simulations.

5.2 Recommendation for the Future Work

In the case of Group 2B AI without ROCOF using Category III settings, the case with well-balanced loads between phases did exhibit somewhat longer ROTs than the base scenario, which one might intuitively expect, and the case with increased imbalance between the phase loadings exhibited shorter ROTs than the base scenario. However, this trend was reversed for Category II settings. These results therefore are inconclusive at this time, and further investigation would be of value.

For Group 2A AI, circuit impedance made a slight difference in ROTs. For Group 2B, ROTs showed significant sensitivity to circuit impedance—in fact, the 50% impedance scenario for Group 2B showed an ROT of 4.27 s, which was the longest ROT of any scenario that did not have a motor in it. Thus, the results are inconclusive at this time, and further investigation of this parameter, potentially combining circuit impedance with load and PV distribution variations, would be of value.

Maximum ROTs were compared in different cases and scenarios in this thesis. Additional statistical parameters can be compared to obtain more insight.

This thesis investigated just two groups of AI methods. Additional groups can be investigated as part of future work as well.

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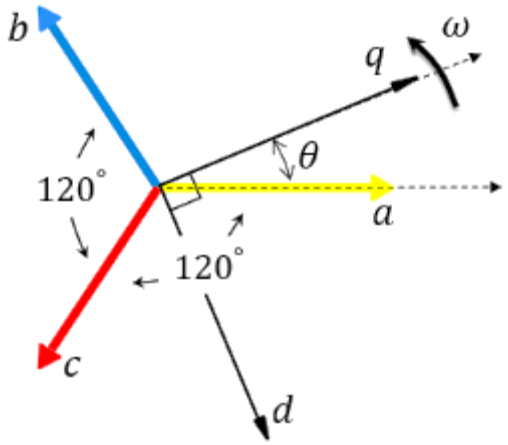
APPENDIX A. DEFENITIONS

Park Transformation

Park transform converts the time-domain components of a three–phase system in abc reference to direct quadrature and zero components in a rotating reference frame. For a balanced system the zero component is always zero. The a-axis and the q-axis are initially aligned.



In both cases, the angle $\theta = \omega t$, where:

- θ is the angle between the a and q axes for the q-axis alignment or the angle between the a and d axes for the d-axis alignment.
- ω is the rotational speed of the d-q reference frame.
- t is the time, in s, from the initial alignment.

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

Where:

- *a*, *b*, and *c* are the components of the three-phase system in the *abc* reference frame.
- *d* and *q* are the components of the two-axis system in the rotating reference frame.
- *0* is the zero component of the two-axis system in the stationary reference frame.

Phase Lock Loop (PLL)

The role of PLL in three phase context is to accurately estimate the angle of the grid voltage by measuring instantaneous voltage waveforms [46]. The Phase locked loop PLL concept was mainly used for synchronous reception of radio signals. Recently PLL techniques have been used for synchronization between grid- interfaced converters and utility grid [40] . The first synchronization schemes were zero-crossing detectors but these schemes were faulty specially in weak grids [47]. An ideal PLL is fast, accurate and invulnerable to disturbances, harmonics, unbalances, and other types or distortions [40].

Figure 67 shows the basic structure of a PLL. Phase detector measures the difference between phase angle of input and output signal. The result is passed through a loop filter and then it is sent to the voltage- control oscillator to generate output signal.

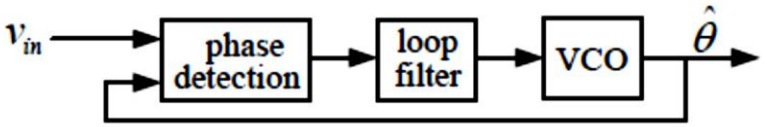


Figure 67. Basic PLL structure [40].

PLLs work in natural abc coordinates, αβ stationary reference frames or in dq rotating reference frames. In PLL algorithms operating in dq rotating frames, voltage signals are transformed to synchronous rotation frame using Park Transformation. The loop filter used in this method is usually a simple Proportional Integral (PI) controller. By representing the three-phase voltage in αβ form, phase of the voltage signal can be extracted by a simple arctan function. This method can work without filters and respond

to any disturbance in the grid voltage instantly [48]. A notable PLL method in αβ reference frame is Dual Second Order Generalized Integrator (DSOGI) which has been utilized in this thesis.

DSOGI Phase Lock Loop

Double second order generalized integrator PLL (DSOGI PLL) tracks the utility voltage by extracting the fundamental positive sequence. Therefore, it operates well under voltage distortions and imbalances. DSOGI uses Second Order Generalized Integrator (SOGI) based filters. Figure 68 shows the block diagram of the DSOGI PLL.

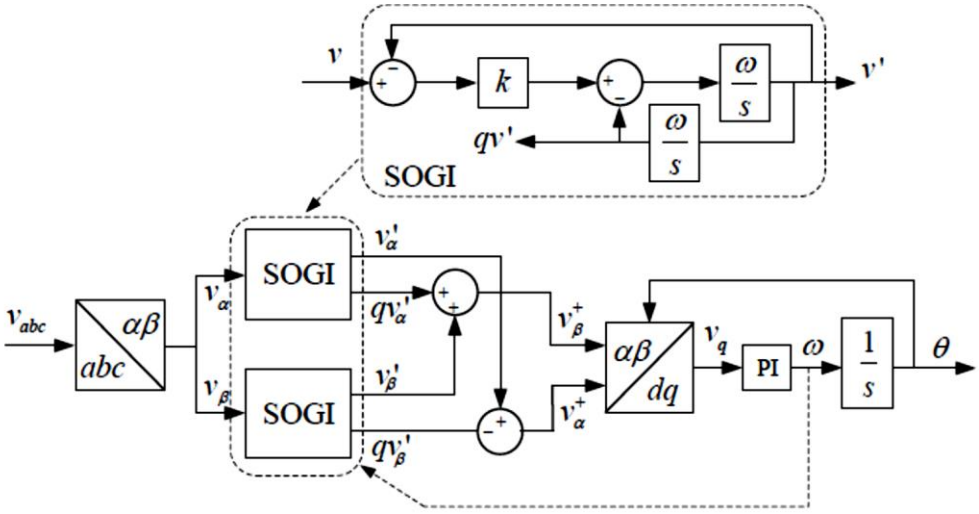


Figure 68. Block diagram of DSOGI-PLL [40].