SYNTHESIS OF OPTIMUM COMPLEX FLUID LOGIC SEQUENTIAL CIRCUITS

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CHAPTER I

INTRODUCTION

Spurred on by the invention and development of fluidic devices, fluid logic is rapidly gaining acceptance and respect as a means of controlling automatic operations. References (1) through (6) report on a wide variety of applications.[1] Two major automotive companies are replacing electrical controls on assembly line machines with recently developed pneumatic systems. Other uses include scrap baling machines, numerous machine tools, high speed packaging machines, automatic assembly machines, material handling systems, process controls, jet engine control and missile guidance.

There is a growing realization that fluid systems are capable of performing all the logic functions that electrical systems can and often at less cost and with greater reliability. Other important advantages include freedom from fire and electrical shock hazards, immunity to nuclear radiation, resistance to vibration and ability to operate in high temperature environments (7).

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[1]Numbers in parentheses refer to references in the Selected Bibliography.

Although pure fluid amplifiers are most frequently mentioned in articles concerning fluid control, moving-parts devices are also undergoing rapid development and are finding broad application in logic circuits. Some of the subminiature valve-type elements have such low-mass moving parts that their response times approach those of the pure fluid devices.

The terminology task group of the National Fluid Power Association committee working on standards have decided upon the term "fluidics" to include both the pure fluid and miniature conventional valves. The term is a contraction of the words "fluid" and "logic" and implies that the devices so classified are primarily logic control devices as opposed to the hardware in the "power" portion of a fluid system (8).

A large number of U.S. industries, as well as government agencies and several leading universities, are conducting research and development programs involving fluid control devices and applications. The result is that a broad selection of excellent hardware is available which can be used in the design of fluid logic systems.

In spite of the rapid evolution of logic devices, there has not been enough progress in the ability to systematically assemble the devices into efficient circuits. This lack of synthesis capability prevents the full exploitation of fluid logic in systems of large complexity.

A brief survey of the field of logic design is presented below.

Intuitive Circuit Design

Most of the circuits in use today have been designed by cut and try methods wherein the designer sketches schematic diagrams of various configurations until he arrives at one that will work. Intuitive circuit synthesis is extremely time consuming, even for skillful and experienced designers. As the complexity of the required sequence increases, the possible number of circuit configurations that will "work" grows until it is highly improbable that any two designers would develop the same circuits or that either circuit would be near optimum. (Criteria for optimum circuits are described in the next chapter.) In efforts to add some semblance of orderliness to intuitive synthesis, some of the more experienced designers have developed several practical aids and procedures.

E. L. Holbrook (9, 10), who has been active in pneumatics since 1929, has written a series of articles describing a number of applications using pneumatic logic functions. He has also suggested ways to improve the schematic representation of circuits. His technique is to separate a logic control system into isolated functions, control them individually and then tie them together. He

has designed some fairly large systems using these methods.

Salek (11) recommends using a cascaded or stacked memory valve system wherein air pressure is "distributed" to limit valves which are activated at the ends of the piston rod travel. Morgan (12) also recommends this method because it helps reduce the number of logic valves in the control system. The approach starts to get into difficulty, however, when a signal from one of the limit valves is required to go to different places at different times during the cycle. There is also the problem of properly switching the memory valves in the distribution circuit.

Hall (13) points out the advantage of using the "ladder" diagram in designing logic circuits. This is a device borrowed from electrical circuit designers with abstract fluid logic symbols substituted for the analogous electrical symbols. The chief feature of the ladder diagram is that it enhances visualization of circuit operation. It has limited utility for synthesizing circuits.

Application of Logic

One of the major steps toward development of non-intuitive circuit design procedures has been the application of Boolean algebra to describe the functions of fluid logic devices and combinations of these devices (14, 15). Once a circuit has been expressed as a function in this

mathematical system, a diagram of the circuit is not required in order to simplify the circuit. If a simpler circuit exists, it can be found by certain Boolean algebraic manipulations. Henke (16) and Ledgerwood (17) are strongly urging control circuit designers to learn the techniques of Boolean algebra and to depend less on the cut and try methods of the past.

The Timing Chart Method

The timing chart (also called sequence diagram or cycle chart) is a device widely employed in designing sequential circuits. Ronan (18) and Henke (19) recommend its use. The chart consists of vertical divisions with each division representing a certain time interval. The outputs and inputs are listed down the left-hand side of the chart. If a particular input or output is supposed to be "on" during a certain time interval, a solid bar is drawn horizontally through the interval. If the input or output is to be "off" in some interval, the space is left blank. Now, each interval is compared with the other intervals. Wherever the situation exists with different outputs occurring for the same combination of inputs, secondaries must be added. When the proper number of secondaries have been added and the intervals established during which each secondary must be "on" or "off", the chart is complete. A circuit is next designed which will satisfy the chart. Many variations will work and the

designer must be skillful in order to produce an optimum circuit.

Yuditskly (20) and Zenchenko (21) code each of the inputs with a weighted number and list this number beside the input at the left side of the chart. By going down each interval and summing weighted values where the bars cross the interval, a total for the column interval is reached. Secondaries are added when columns have the same total. Each secondary is also coded with a weighted value and where its bar crosses an interval, that value is added to the total. A unique situation exists when each column has a total of weighted values different from all the others. As before, a circuit is then assembled which will satisfy the chart.

The timing chart can be considered as one of the better aids in intuitive design. It displays the sequential specification in a graphical manner and provides for assigning secondaries or memory elements to cover appropriate intervals of the chart. The quality of the circuit resulting from the chart depends greatly on the skill of the designer. Ronan states that it is a good policy to investigate several arrangements so that a desirable circuit is not overlooked.

Application of Switching Circuit Theory

Professor E. C. Fitch (22, 23, and 24), of Oklahoma State University, was one of the first to recognize the

limitations of intuitive circuit design and has been instrumental in introducing formal logic synthesis techniques. By successfully adapting the procedures developed for electrical switching circuits to the synthesis of fluid logic systems, he has contributed considerably to extending the complexity to which circuits can be systematically designed.

With this method, the sequence specification is carefully represented in the Huffman flow table model. The flow table is then reduced and merged to assure a minimum number of secondaries or memory valves. Next, the table is rearranged into a required order and becomes the operational flow table. Information is taken from the operational flow table and entered into Karnaugh maps from which equations for the output circuit and memory circuit are obtained. Circuit diagrams can be drawn by simply implementing the equations with fluid logic symbols representing physical hardware.

The procedure or method is non-intuitive and greatly reduces the time required to synthesize a sequential circuit. Its advantages are being recognized by industry and at least one large company uses the method in designing hydraulic logic circuits. They also conduct an in-plant course which is similar to Oklahoma State University's "Fluid Logic" course.

In spite of its significant contribution to the problem of fluid logic synthesis, the method becomes extremely

unwieldly as the number of variables increases. Each additional input or secondary doubles the size of the maps involved. Even large digital computers soon become incapable of handling the mushrooming problem.

Synthesis Procedures Research

The development of digital computers and complex communications systems depends heavily on sequential synthesis procedures. Consequently, considerable effort is being made to improve existing methods and to develop new ones.

Marcus (25) shows how to use the Huffman flow table and Karnaugh maps to synthesize sequential circuits. His text is used for teaching a graduate course in switching circuits at Oklahoma State University and other universities.

Moore (26), one of the pioneers in developing sequential synthesis procedures, has published a collection of the more important papers on sequential machines and includes one by D. A. Huffman. An extensive bibliography of related work is included. This collection is primarily intended to supplement formal texts such as the one by Marcus.

Haring (27) outlines the recent work at M.I.T. which primarily involves investigating mathematical properties of sequential machines based on the Huffman model. As

yet, no major progress has been made in developing improved synthesis procedures.

McKellar (28) has investigated what he terms as a practical synthesis procedure. His method involves artificially opening the feedback loops in a sequential machine. Each time a loop is "opened", a secondary is replaced by an input and an output. The rows of the flow table are, thus, reduced while the number of columns increases. After a sufficient number of interactions, the flow table is reduced to one row which can be expressed as combinational circuits. The chief claim for this method is that it is iterative and can be programmed for a computer. Its disadvantage is that there is no assurance of an optimum or near optimum resulting circuit because the result depends on the order in which the loops are opened.

Tripp (29) employs a matrix system of function representation. His method again becomes unwieldly as the complexity increases. Halsey (30) attempted to apply linear programming techniques to the state assignment problem but reported negative results.

In summary, although a considerable effort is being made to develop better synthesis procedures, the progress is slow. It should be noted that almost all of the approaches are fairly abstract and general in nature.

The models (such as the Huffman flow table) succeed in expressing the sequence specifications in a rigorous

non-ambiguous manner. However, a model of this type inherently contains all of the solutions which can satisfy the specification. The problem becomes one of arriving at the right solution from all the possibilities and it is impractical or even impossible to develop all of the solutions.

CHAPTER II

OBJECTIVE AND SCOPE OF STUDY

The objective of this study has been to investigate and develop a new procedure for the systematic synthesis of fluid logic sequential circuits. Although greatly simplified in comparison to present techniques, the procedure is rigorous and powerful, permitting the straightforward synthesis of problems which are too complex for ready solution by existing methods.

The circuits synthesized by the new procedure have a structure or form based on carefully designed ideal simple or basic circuits. These circuits are considered optimum based upon the following important criteria:

1. They have the fastest possible response. That is, the minimum time elapses between the completion of one event and the beginning of the next event in the sequence. (The time required for the event to occur is outside the control of the logic circuit.)
2. The circuits contain a minimum assortment of logic elements.
3. None of the distribution valves are

switched with fluid flowing through the valves. This has the advantages of using lower switching signals, providing faster switching response and allowing possible valve simplication.

4. A minimum or near minimum of total system hardware. This feature is important from the standpoints of economy, over-all size, and system reliability.

The scope of the study was limited to closed systems having only feedback inputs. However, this is an important class of fluid logic systems, representing a very broad application in industry. A schematic representation of this type of circuitry is shown in Figure 1. The power system is made up of actuators and their power control valves. The actuators may be linear or rotary devices. Each actuator is controlled by its respective output signal from the fluid logic control circuit. At the completion of an actuation (called an event) a signal is emitted from the power system and is fed into the control circuit where it is directed through the circuitry to initiate the next event. At the same time the signal modifies the control circuit, preparing it for the next input signal. This process is repeated until a specified sequence of events has been completed, at which time the power system shuts down or repeats the sequence as many times as desired.

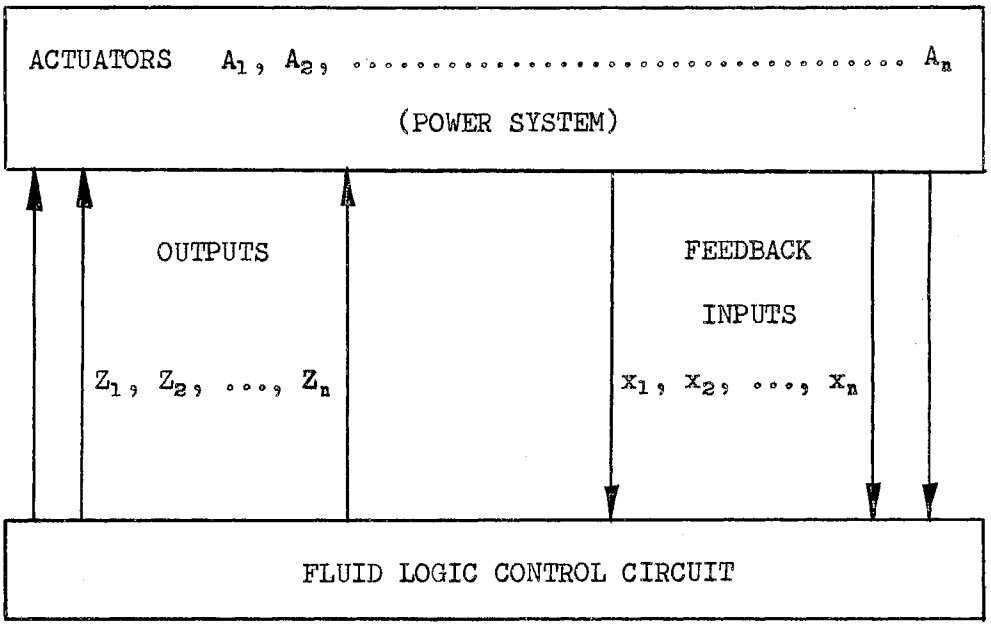


Figure 1. Sequential Control System Schematic

Both input and output signals are of the level type. That is, a signal is either off (at vent or tank pressure) or on (maximum pressure). A signal changing from off to on is considered a step input, going from a steady state vent pressure to a steady state maximum pressure. The only time an input signal changes is when an event (in the case of a cylinder, a complete extension or retraction) is completed. Thus, the circuits are asynchronous as opposed to synchronous circuits where all of the changes occur at clocked intervals.

This study also assumes that an operational event of finite time follows each output from the fluid logic control circuit. The actuation of devices in the power circuit serve as effective delays, assuring that the control circuit modification has stabilized before the subsequent event completion signal is fed back into the control circuit. With this concept, the problem of timing does not have to be considered as it would in the case where the output is fed directly back into the control circuit without first causing some event to occur in the power circuit. Such a situation could occur in computational circuits which are not considered in this study.

Critical races are avoided by making the usual restriction that inputs change only one at a time. One exception to this restriction is permissible and will be discussed later.

Input changes result from position sensing which

takes place at the limits of the actuator travel. This precludes the system from getting out of sequence or confused as a result of false signals which could inadvertently occur in pressure sensing or preset program systems. The development of accurate and reliable position detection devices has made position sensing the dominant method of actuating input signals in the feedback type systems.

There are three main types of fluid logic circuits commonly encountered in the above classification. These different types will each be investigated so that a general procedure will result, capable of handling all three types. These three types are:

1. Ordinary sequential circuits. If there are two or more actuators in the power circuit, then if some actuator A_i extends or retracts or cycles once, then some other actuator, say A_j, must extend or retract or cycle before actuator A_i can act again.
2. Counter circuits. The first actuator in the power circuit will cycle some specified number of times, then the next actuator will cycle its specified number of times and so on until the sequence is complete and stops or starts over.
3. Complex circuits. This circuit results

from mixing a counter circuit into an ordinary circuit. As the name implies, this type of circuit is the most complicated and is the most difficult to handle.

CHAPTER III

OPERATIONS TABLE SYNTHESIS APPROACH

Assume for the moment that a circuit has been synthesized by any of the existing methods and it is desirable to check its operation. If the circuit is simple, one can go through a schematic diagram and carefully check for proper operation. This requires mentally keeping track of the positions of the different valves in the circuit at the various stages of the sequence. Alternatively, the circuit may be breadboarded and checked for operation using actual hardware. In either case, if the circuit is very complicated, correcting errors becomes a very tedious and time consuming task.

In order to enhance the verification of a circuit's proper performance, the operations table or composite chart has been recently developed (23). A fluid logic sequential circuit is digital with changes taking place at discrete intervals. The operations table depicts the complete status of the circuit at each of these intervals. Each row of the operations table represents a stabilized state of the input variables and the corresponding stable states of the affected output and secondary variables. In comparing two rows of the table, it is apparent which

variables were in transition during the change of circuit state. The completed table includes the entire spectrum of the various circuit states or conditions during one cycle of the sequence. Checking the rows one at a time is somewhat analogous to examining a film strip frame-by-frame. If an error is contained in the circuit as synthesized, it will show up as a contradiction in the logic portrayed in the rows of the operations table. Not only does the contradiction appear, but the variables involved are directly identified.

Regardless of the procedure used to develop the sequential circuit, its operational logic structure can be fully displayed in the operations table. It was in checking out and examining the logic structure of various synthesized circuits in the operations table that led the writer to conclude that such a table could possibly be used for synthesizing a sequential circuit directly. The table contains the concise operational specification of the circuit in addition to the logic structure of the complete circuit for all stages of the sequence.

At the start of a synthesis procedure, all that is known to the designer is the sequence of events that the system is required to perform and the input signals associated with these events. Normally, this specification is expressed in a primitive flow table and from there the involved procedure of developing a solution is carried out.

If the operations table is used for direct synthesis, the problem is to start with the bare specification in the table and then proceed to develop the logic structure that completes the table and defines the circuit. As previously mentioned, there are always several distinct circuits that can satisfy even a simple sequential system or machine. As the complexity increases, the number of possible solutions rapidly becomes very large. Each distinct circuit realization for some specified sequence will appear differently in the operations table. Thus, it is immediately obvious that there are as many ways to construct a table as there are possible circuit realizations. Yet, it is this very feature which makes the synthesis approach attractive. For if it is possible to construct the logic in the table and derive workable circuits, then it might also be possible to construct a circuit having some desired form, since the manner in which the table is built up is at the discretion of the designer.

This construction of sequential fluid logic circuits having certain characteristics or form is precisely the object of this study.

To illustrate the approach to be taken, the beginning of an operations table is shown in Figure 2. There are two cylinders, A and B. The sequence of operations to be performed is specified as follows:

1. A extends	Shorthand notation:
2. B extends	A, B, $\underline{B}$, $\underline{A}$, A, B, $\underline{A}$, $\underline{B}$

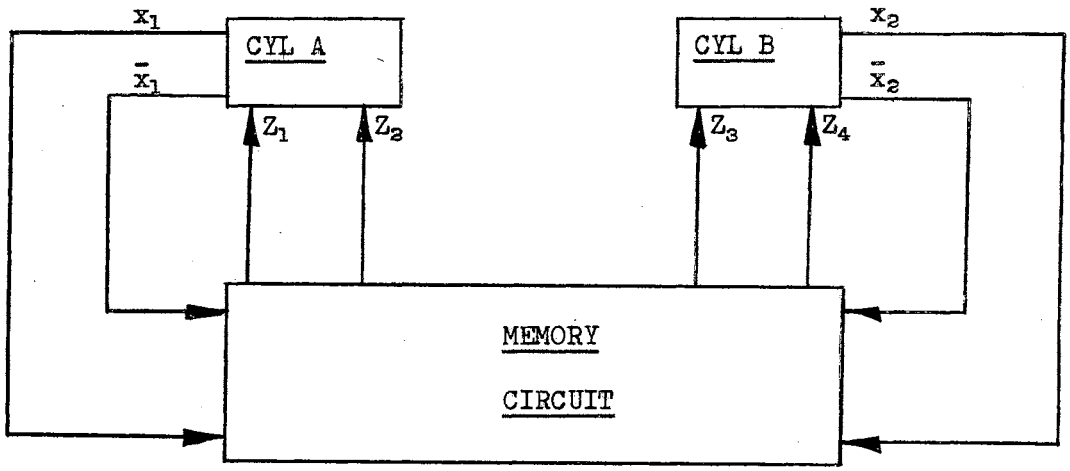
3. B retracts
4. A retracts
5. A extends
6. B extends
7. A retracts
8. B retracts
9. Sequence repeats

A basic schematic of the cylinder operation is also shown in Figure 2.

Z_1 and Z_2 are the output signals which cause cylinder A to extend and retract, respectively, while Z_3 and Z_4 are the respective extend and retract signals for cylinder B. Input signal x_1 denotes that cylinder A has extended, while signal $\bar{x}_1$ indicates that A has retracted. The corresponding input signals for cylinder B are x_2 and $\bar{x}_2$. The input signals affect the memory circuit so that the proper output signal occurs.

The preliminary operations table reveals that certain entries have been made. Starting at the left-hand side of the table, the event numbers are listed in the first column. The next column names the event that is associated with the number. The third column lists the stable condition of the inputs x_1 and x_2 just after completion of the previous event. For example, with the completion of event number 8, the final retraction of cylinder B in the sequence, the inputs x_1 and x_2 both stabilize at 0.

The next six columns are reserved for secondary



TWO CYLINDER SEQUENTIAL SCHEMATIC

			Secondaries						Outputs			
No.	Event	$x_1 x_2$	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Z_1	Z_2	Z_3	Z_4
1	A	00							$\bar{x}_2$	0	0	-
2	B	10							-	0	x_1	0
3	B	11							-	0	0	x_2
4	A	10							0	$\bar{x}_2$	0	—
5	A	00							$\bar{x}_1$	0	0	—
6	B	10							-	0	x_1	0
7	A	11							0	x_2	-	0
8	B	01							0	-	0	$\bar{x}_1$

PRELIMINARY OPERATIONS TABLE

Figure 2. Two Cylinder Schematic and Operations Table

variables which make up the memory circuit. Although space has been provided for six, a lesser number may be needed. The last four columns are for the Z_1, Z_2, Z_3, and Z_4 outputs. Zeros are entered where these signals must be off, as dictated by the sequential specifications. Dashes are entered where "don't care" conditions exist. This leaves blank spaces only for the conditions where the appropriate outputs must be on.

Now shifting back to the $x_1 x_2$ column, it is determined which variable changed as a result of the completion of the previous event. For example, upon completion of event number 8, x_1 remained at 0 while x_2 changed from one to zero. Thus, $\bar{x}_2$ is entered into the Z_1 output column in the first row. Subsequent variable changes are entered in the corresponding columns and rows. A systematic designation is, thus, derived for establishing the input that associates with the desired output. The task that remains is to assign secondaries appropriately so that they can be "anded" with the inputs in the Z columns. The proper secondary or combination of secondaries must be shifted to the appropriate memory positions prior to the time that the associated input signal appears. For example, when $\bar{x}_2$ is turned on in the first event, it goes directly through the stable memory valves to activate the Z_1 output.

One of the fundamental differences in this approach as compared to existing methods is to work with the input signal (or signals) that changes at the completion of an

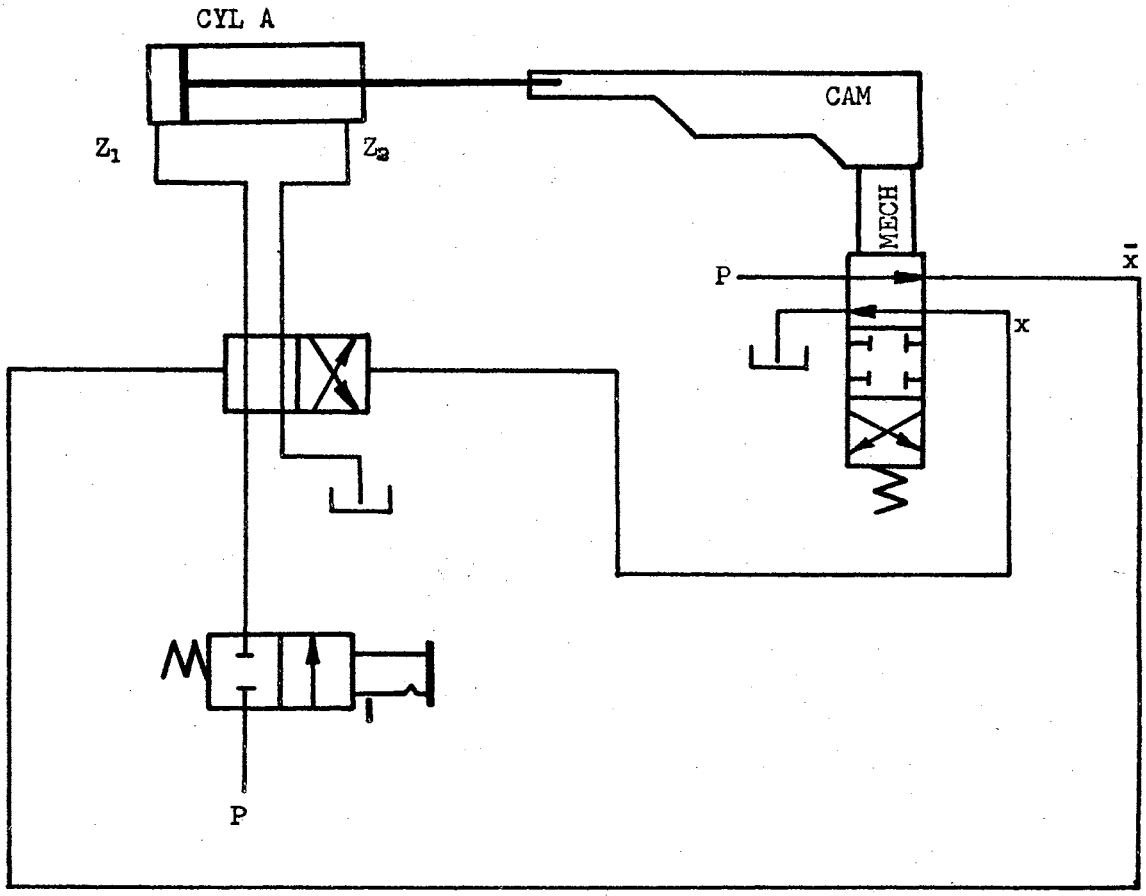
event rather than with the stabilized combination of input signals which exist at the completion of an event. The second aspect of the approach involves recognition of patterns in the operations tables for highly developed circuits. If these patterns can be identified and the basis for their occurrence established, the information can then be used to develop rules for the systematic assigning of secondaries. Circuits thus synthesized should be of the same basic type as the "ideal" circuits which were used to establish patterns in the operations table.

CHAPTER IV

OPERATIONAL PATTERNS OF BASIC CIRCUITS

As previously stated, the objective of this study is to develop a synthesis procedure which will yield complex fluid logic circuits exhibiting the same type of structure as well developed simple or basic circuits. Some of these simple circuits will now be examined.

Figure 3 shows the simplest possible automatic fluid circuit using feedback inputs. Fluid power symbols are used to represent the valves in the circuit schematic. As in all the circuits which will be considered, position sensing is employed to turn the extend and retract signals off and on. In this case, a cam attached to the rod of cylinder A activates the input signal valve. With the cylinder retracted as shown, signal line $\bar{x}$ is at maximum pressure while signal line x is vented to tank. During extension of the cylinder, the signal valve is in the center positions with lines x and $\bar{x}$ both blocked. Thus, the $\bar{x}$ line remains pressurized until the cylinder reaches the end of its extension, at which time line x is pressurized and line $\bar{x}$ is vented to tank. During cylinder retraction, the signal valve is again in the center position, blocking off both ports so that pressure is



NO	EVENT	x	Z_1	Z_2
1	A	0	$\bar{x}$	$0=\bar{x}$
2	$\underline{A}$	1	$0=x$	x

OPERATIONS TABLE

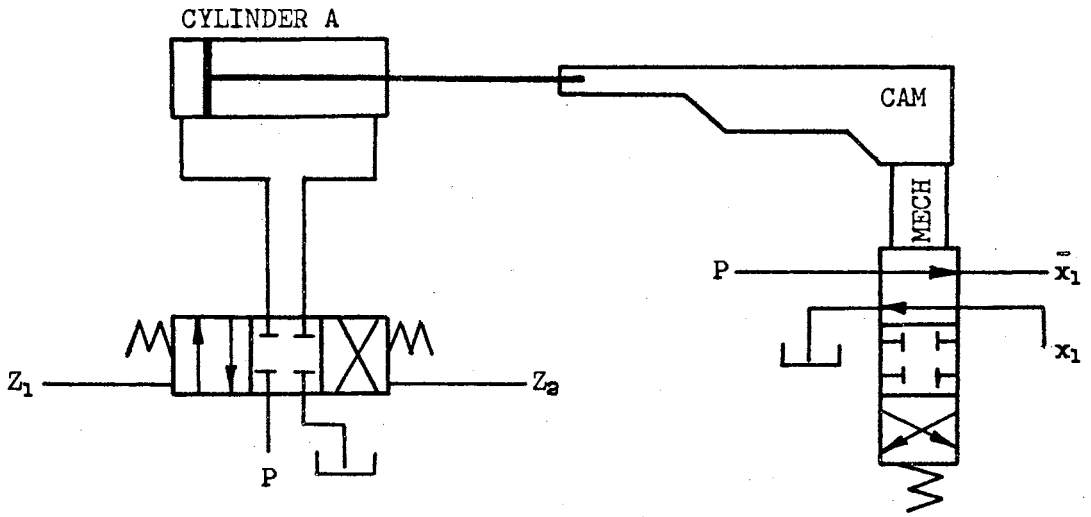
Figure 3. Schematic for Single Cylinder Which Automatically Extends and Retracts

maintained in line x until the end of the retraction stroke is reached. The input signals x and $\bar{x}$ directly switch the cylinder control valve, commanding the cylinder to reverse operation at the ends of the strokes. The manually operated valve beneath the cylinder control valve is for starting and stopping the automatic operation.

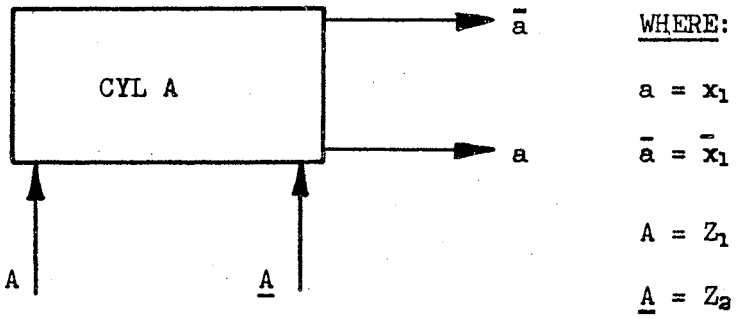
The operations table is shown at the bottom of the figure. Note that the signal which comes on at the completion of an event (extension or retraction) goes directly to change the states of the output signals Z_1 and Z_2.

In this first example, the cylinder control valve also acts as the logic valve. However, in subsequent circuits, the power control valve and the logic valve delivering the output signals Z_1 and Z_2 will be separate elements. This will permit separation of the logic circuitry from the power system. Such an arrangement is shown at the top of Figure 4.

Here, the power valve has three positions and is spring centered. With both output signals Z_1 and Z_2 off, the valve will be centered, locking the cylinder in the position it had at the time the output signal went off. Thus, an optional feature is added to the system. For example, if cylinder A is fully extended and is to remain extended while some other event occurs, it is optional whether or not signal Z_1 remains on during that time. Optional or "don't care" states of a system make a circuit



TYPICAL POWER CIRCUIT SCHEMATIC



SIMPLIFIED EQUIVALENT SCHEMATIC

Figure 4. Simplification of Power Circuit Schematic

easier to synthesize.

A simplified equivalent schematic of the power circuit is shown at the bottom of Figure 4. Although it is customary to use subscripted Z's to represent the output signals and subscripted x's to represent the input signals, a simpler and more meaningful notation is desirable for complex circuitry. Therefore, the output signal Z, commanding cylinder A to extend, becomes signal A, while $\underline{A}$ replaces the cylinder A retract signal Z_2. The input signals x, and $\bar{x}$, are replaced by a and $\bar{a}$, respectively. Thus, in a multicylinder circuit, it becomes easier to associate signals with cylinders.

In the previous examples, position sensing has been shown by the action of a cam and valve combination. A more recent and in some cases a more reliable and accurate method is to interrupt a jet of air. This sensing technique is especially useful when using fluidic devices without moving parts. A schematic representation of this type of sensing is shown in Figure 5. When the cylinder reaches the end of its travel, an interrupter attached to the cylinder rod or some part of the object being moved causes a back pressure to build up in the air tube. This back pressure switches a bistable amplifier causing a change in the output signals. Various other schemes of using the interrupted jet for position sensing are possible.

After the input signal is produced by the position

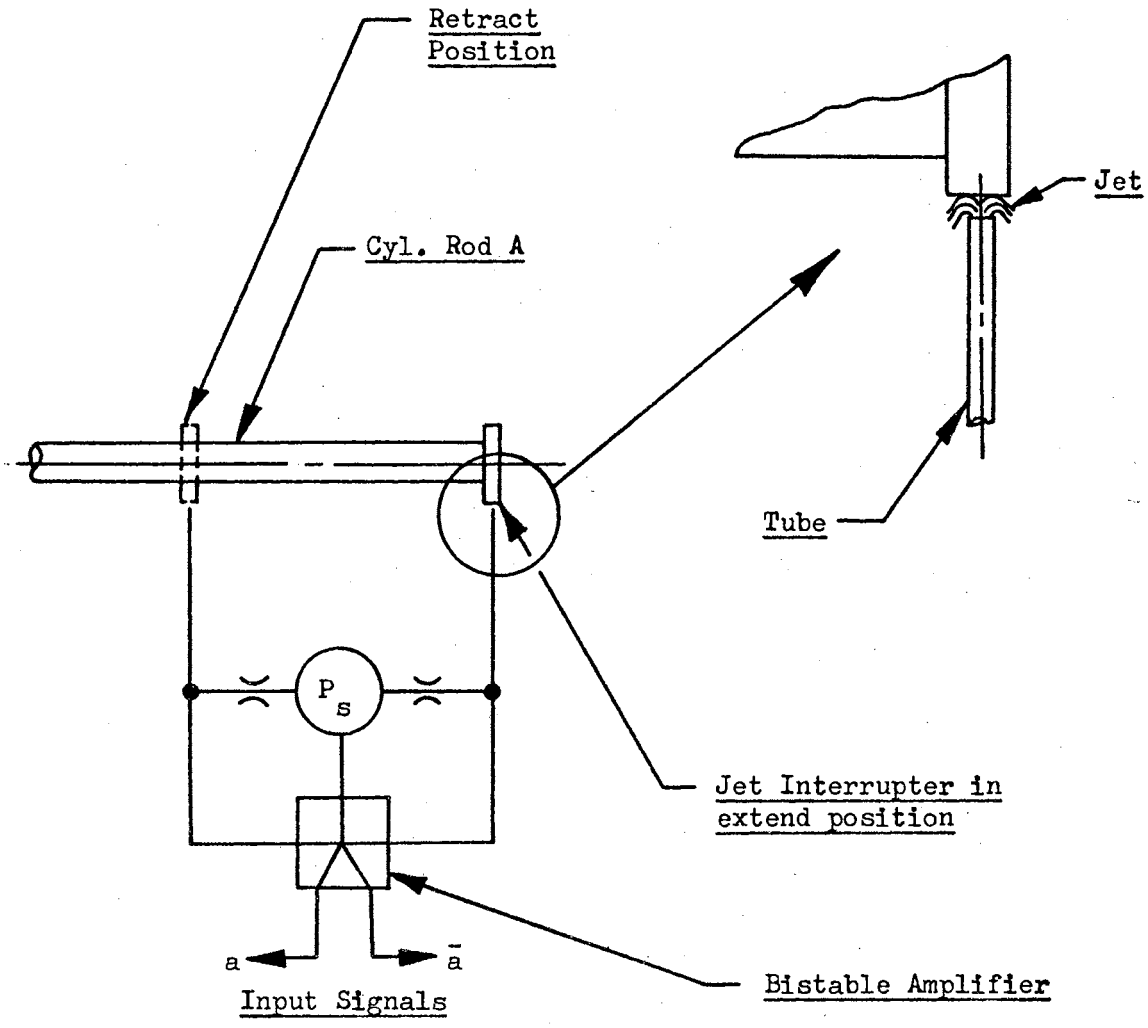
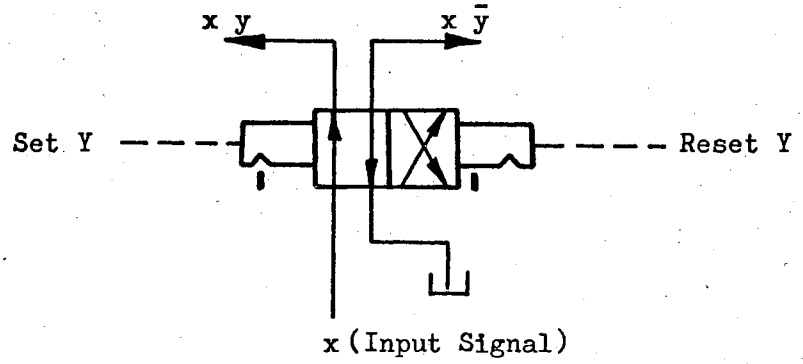


Figure 5. Interrupted Jet Position Sensing

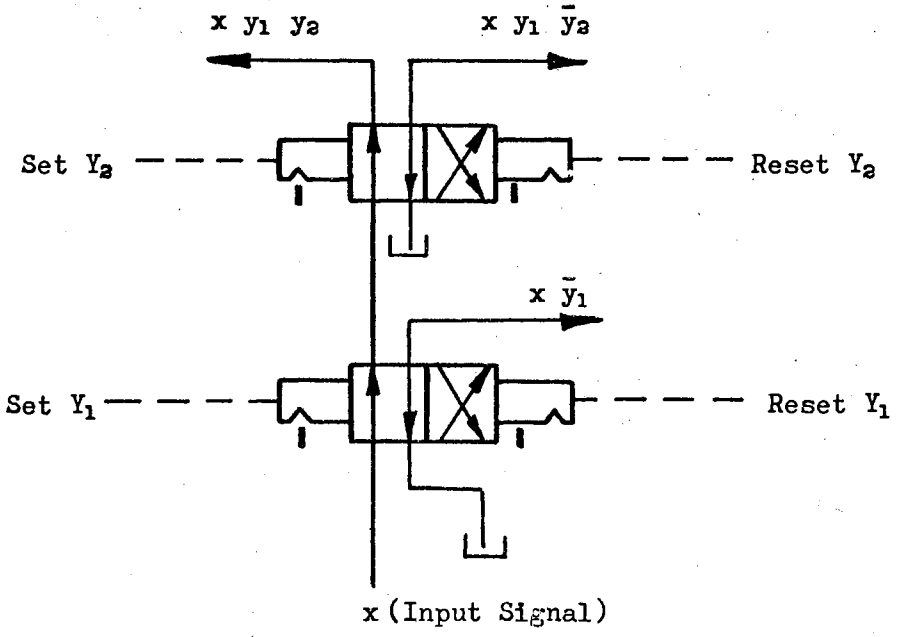
sensor, it is necessary to direct the signal to the desired part of the logic circuit. If the signal always goes to the same place, there is no problem. However, when a particular signal goes to different places at different intervals of the sequence, it is necessary to provide gating. The implementation of this gating using fluid power symbols is shown in Figure 6. Single gating for sending signal x to two different locations is shown at the top. The valve combination for sending signal x to three locations is shown at the bottom. The valves are detent held in their most recently activated position (set or reset) and will shift only when the opposite signal is applied. Both the set and reset signals will not be simultaneously applied. The notched portions on the sides of the symbols represent the detents. These will be eliminated on most of the subsequent symbols for simplicity. However, it is to be understood that whenever a pilot-operated logic valve is shown, it is a detent valve. The detent provides the "memory" function of the logic circuitry.

A memory valve combination for sending an input signal to four different locations is shown in Figure 7. This is referred to as "third order" memory since three separate activating signals are required to gate the input signal. The two-valve combination in Figure 6 represents second order memory and the one valve, first order memory. In general, if an input signal goes to n different places,



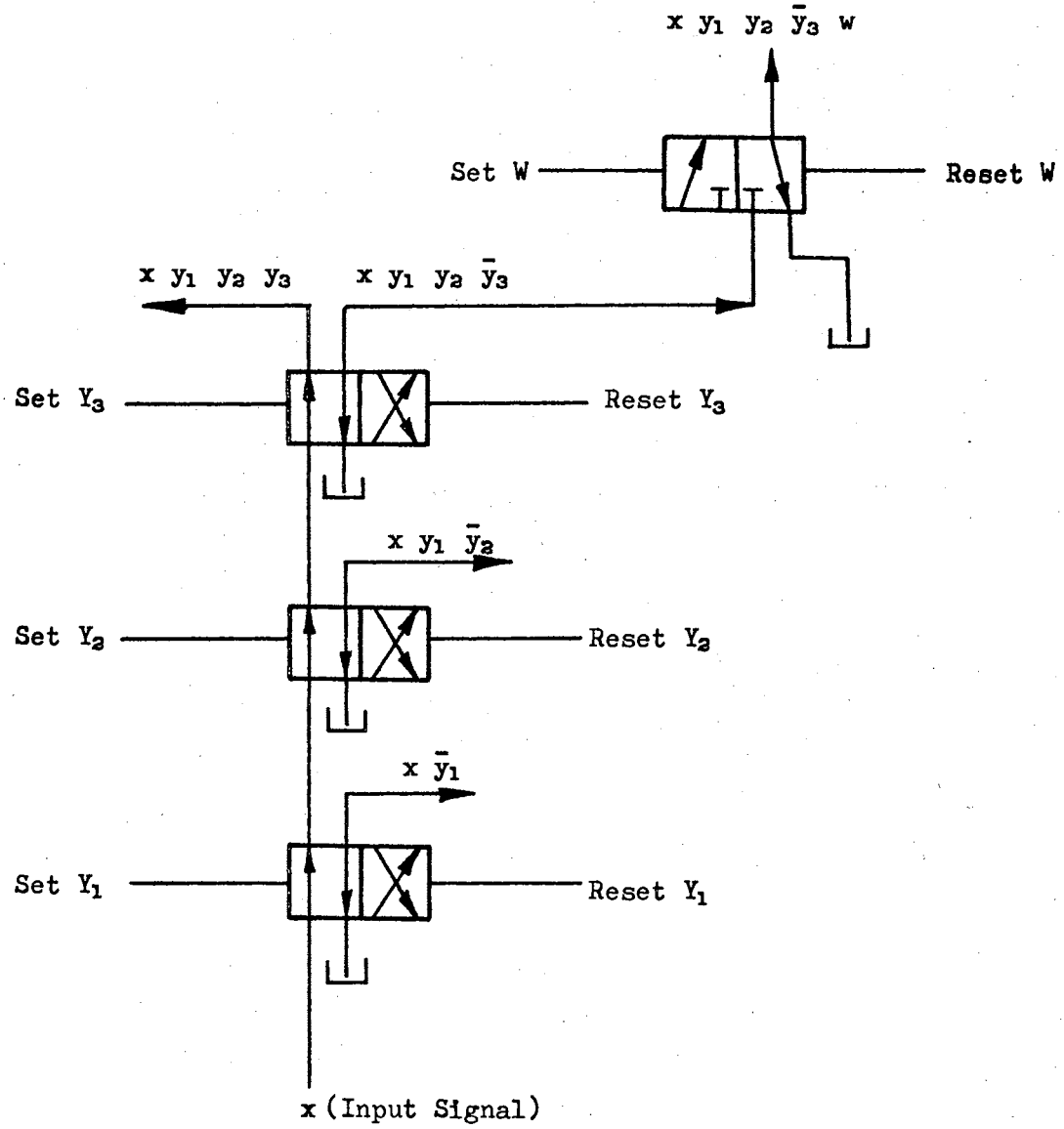
Memory Valve for Sending Input Signal x to Two Different Locations.

Note: Capital Y refers to the memory valve.
Lower case y refers to the state of the valve.



Memory Valve Combination for Sending Input Signal x to Three Different Locations

Figure 6. Memory Valve Combinations



Memory Valve Combination for Sending Input Signal x to Four Different Locations With Shut Off Provision for Signal $x\ y_1\ y_2\ \bar{y}_3$

Figure 7. Memory Valve Combination With Shut Off Provision

n-1 memory valves will be required to distribute the signal. The memory gating valves just discussed are referred to as "Y" valves. This nomenclature is appropriate because the valve does act as a "Y" or branch point in the logic circuit. Figure 7 also contains another type of memory or detent valve. This valve serves to shut off an input signal and vent the output port to tank when the valve is in the "reset" position shown. This valve will be referred to as a "shut-off" valve or a "W" valve. When the shut-off valve is in the "set" position, the input signal passes through. The purpose of the W valve is to prevent signals from opposing each other in the logic circuitry. The W valve function will be seen as more circuits are examined.

The gating functions just discussed can be implemented equally well with pure fluid components. A memory circuit for sending an input signal to two different locations is shown in Figure 8. The pair of bistable amplifiers enclosed by the dashed line is considered as a single element and can be made so physically. The reason for staging the amplifiers is to enable the element to remember its last setting even if the set or reset signal has been removed. The top amplifier is connected to supply pressure and is controlled by the set and reset signals. Once the amplifier is set or reset, it will remain in that state until the opposite signal comes on. Its output is a low level signal which biases the second amplifier. Thus,

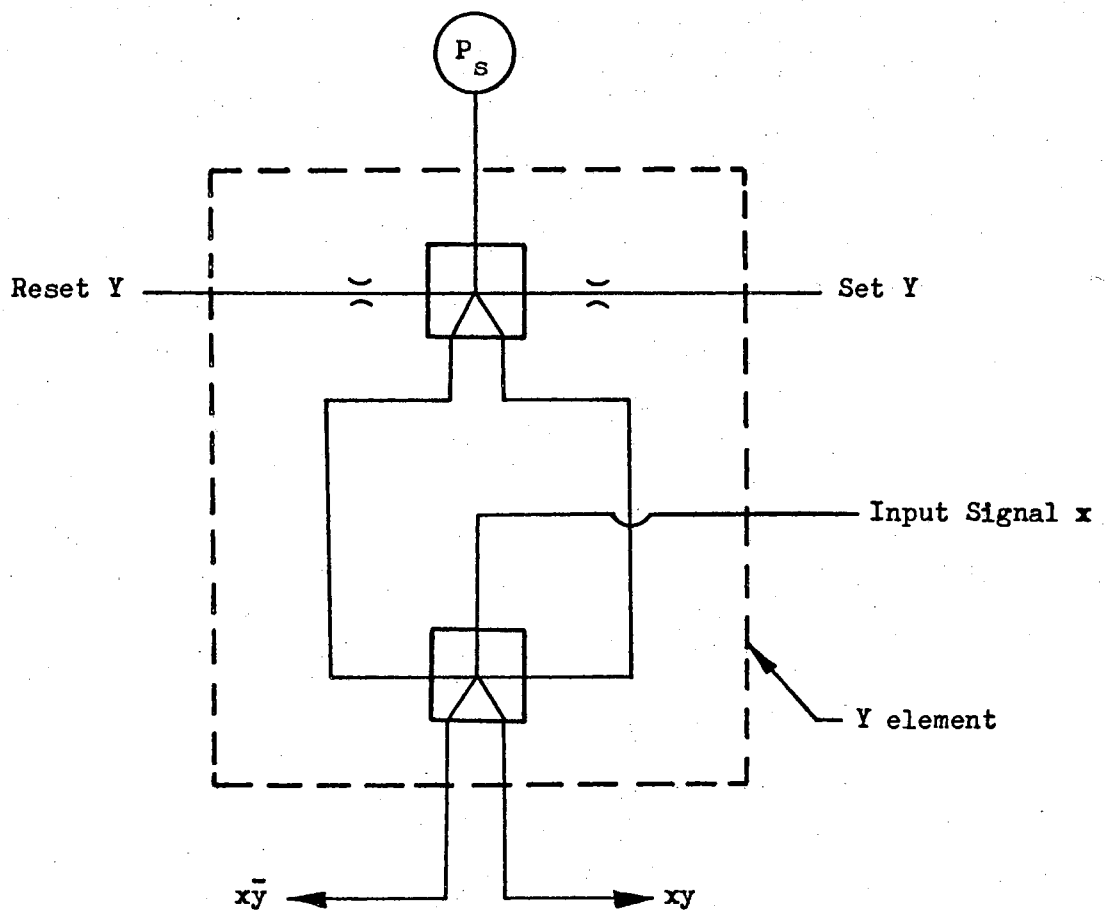


Figure 8. Memory Circuit for Sending Input Signal x to Two Different Locations

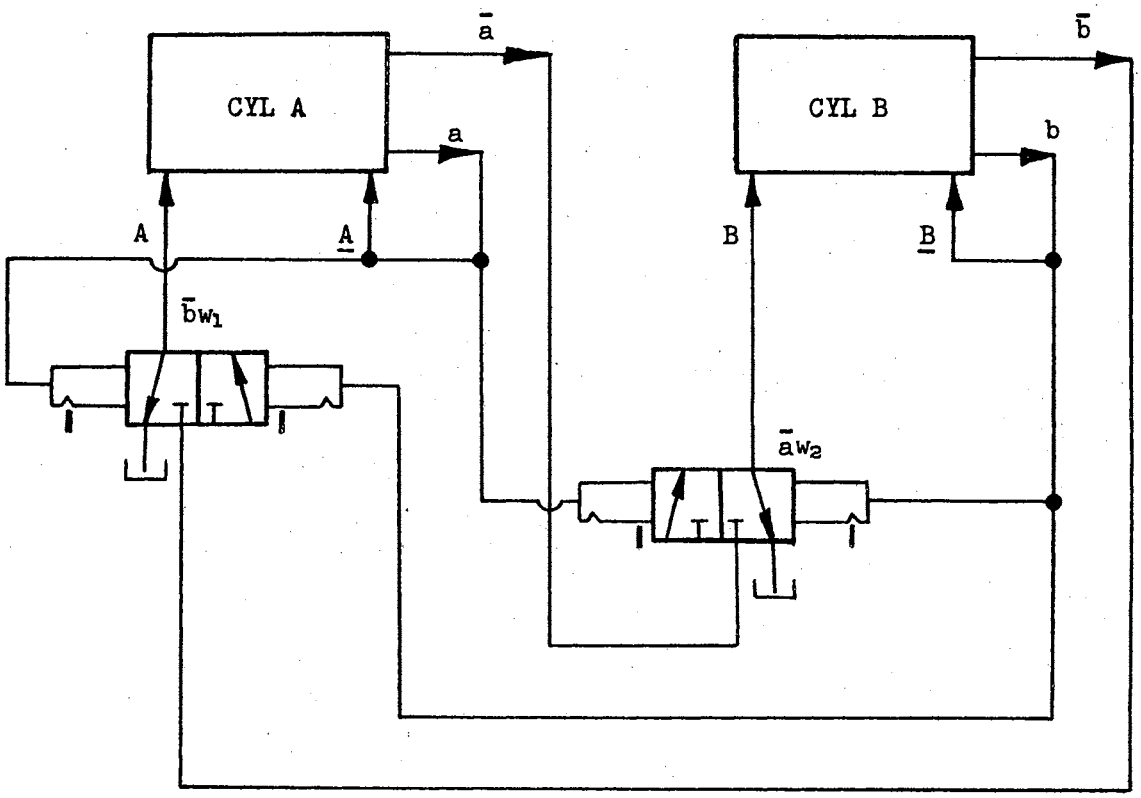
when the input signal x appears at the bottom amplifier, it is steered by the bias signal that happens to be controlling.

When there is no input signal x, there is no output xy or $x\bar{y}$ because the bias signal is strong enough to steer x through the second amplifier, but is not strong enough to cause an output without x. Wilson (31) has shown that a much weaker signal is needed at the control port to divert an incoming signal than is required to **switch** an established flow.

The shut-off function can be accomplished in an almost identical manner. In this case, however, one of the outputs is vented and the shut-off bias signal must be strong enough to switch an established flow.

The preceding discussion has shown that sensing and memory functions can be implemented with either pure-fluid or moving-parts fluidic elements. For the sake of brevity and consistency, only moving parts symbols will be used in the circuits involved in the remainder of this study. It is important to realize that the logic developed could also be implemented with pure fluid devices. The major purpose in discussing fluidic elements has been to provide an understanding of the key circuit functions involved in developing the synthesis procedure.

A very simple two-cylinder automatic circuit with feedback inputs is shown in Figure 9. Note that only shut-off valves are required in the control circuit. The



$A = \bar{b}\ w_1$ $\quad W_1$ set = b $\quad W_2$ set = a

$\underline{A} = a$ $\quad W_1$ reset = a $\quad W_2$ reset = b

$B = \bar{a}\ w_2$

$\underline{B} = b$

SCHEMATIC FOR AUTOMATIC CIRCUIT A, $\underline{A}$, B, $\underline{B}$

NO	EVENT	ab	A	$\underline{A}$	B	$\underline{B}$	W_1	W_2
1	A	00	$\bar{b}w_1$	$0 = \bar{a}$	$0 = \bar{w}_2$	$0 = \bar{b}$	DET	0 = DET
2	$\underline{A}$	10	$0 = \bar{w}_1$	a	0 = a	$0 = \bar{b}$	0 = a	a
3	B	00	$0 = \bar{w}_1$	$0 = \bar{a}$	$\bar{a}w_2$	$0 = \bar{b}$	0 = DET	DET
4	$\underline{B}$	01	0 = b	$0 = \bar{a}$	$0 = w_2$	b	b	0 = b

OPERATIONS TABLE

Figure 9. Schematic for Automatic Circuit A, $\underline{A}$, B, $\underline{B}$

circuit equations are written immediately below the schematic. These equations are obtained directly from the schematic simply by labeling the lines and valves with logic notation and then determining the combinations that result in actuation signals. After the equations are obtained, the circuit operation can be verified by filling out the operations table as shown at the bottom of the figure.

A distinguishing feature of this circuit is that the signal which switches on at the completion of an event goes directly through a prepared path to activate the next event in the sequence. For example, at the completion of event number 2, the retraction of cylinder A, signal $\bar{a}$ is turned on. Signal $\bar{a}$ passes through the open valve W_2 which was opened at the beginning of event number 2. Thus, the start of event number 3 is triggered in the minimum possible time. Had signal $\bar{a}$ been required to combine with another signal, there would have been a delay while this combination took place. In addition to its fast action, this circuit contains only two control valves and is the simplest circuit that could be used to perform the control function.

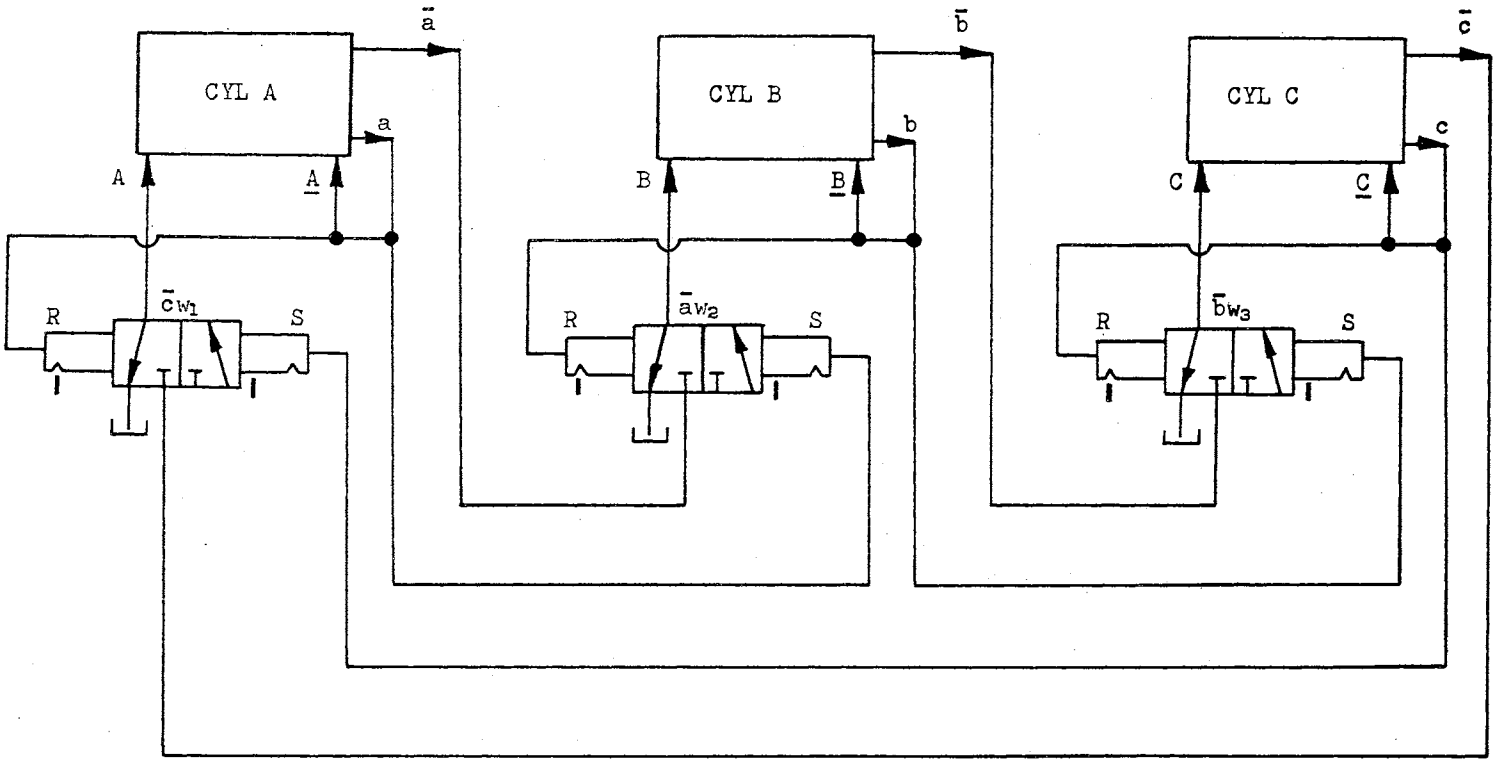
One more interesting observation should be made about this circuit. The shut-off valve is not normally considered to be a logic element in that it does not perform in the classical sense. Circuits synthesized by the classical methods would not contain such an element. Yet it is

not possible to design a circuit with classical logic devices which is faster acting or has less valves. The conclusion is that the memory shut-off function is a desirable feature, at least in the circuit just discussed, and could possibly be used effectively in more complicated circuits.

A slightly more complex automatic circuit is shown in Figure 10. Here, three cylinders are involved and an additional control valve is used. Again, the circuit equations are obtained and the operation verified in Table I. The comments made about Figure 9 also apply to this circuit.

Although the entire spectrum of circuit behavior is contained in the operations table, a clearer insight about what is taking place can be obtained by omitting some of the information and building up a table that is logically equivalent to the actual circuit diagram. Such a table for the circuit of Figure 9 is shown in Table II. The first three columns of this table are identical to those of the corresponding operations table. The fourth column labeled CS contains the signal which switches on at the completion of the previous event. For example, at the completion of event number 1, signal a appears and is entered in column 4 in row 2.

Now, in every case, the changed signal is the command signal for the event that is to occur. In the second row, signal a is commanding cylinder A to retract. However, as shown by the states in the input column, signal $\bar{b}$ is



A = $\bar{c}w_1$

$\underline{A}$ = a

B = $\bar{a}w_2$

$\underline{B}$ = b

C = $\bar{b}w_3$

$\underline{C}$ = c

S = SET

R = RESET

	SET	RESET
W_1	c	a
W_2	a	b
W_3	b	c

Figure 10. Schematic for Automatic Circuit A, $\underline{A}$, B, $\underline{B}$, C, $\underline{C}$

TABLE I

OPERATIONS TABLE FOR AUTOMATIC CIRCUIT A, $\underline{A}$, B, $\underline{B}$, C, $\underline{C}$

No.	EVENT	abc	A	$\underline{A}$	B	$\underline{B}$	C	$\underline{C}$	W_1	W_2	W_3
1	A	000	$\bar{c}w_1$	$0 = \bar{a}$	$0 = \bar{w}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	DET	$0 = DET$	$0 = DET$
2	$\underline{A}$	100	$0 = \bar{w}_1$	a	$0 = a$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	$0 = a$	a	$0 = DET$
3	B	000	$0 = \bar{w}_1$	$0 = \bar{a}$	$\bar{a}\ w_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	$0 = DET$	DET	$0 = DET$
4	$\underline{B}$	010	$0 = \bar{w}_1$	$0 = \bar{a}$	$0 = \bar{w}_2$	b	$0 = b$	$0 = \bar{c}$	$0 = DET$	$0 = b$	b
5	C	000	$0 = \bar{w}_1$	$0 = \bar{a}$	$0 = \bar{w}_2$	$0 = \bar{b}$	$\bar{b}\ w_3$	$0 = \bar{c}$	$0 = DET$	$0 = DET$	DET
6	$\underline{C}$	001	$0 = c$	$0 = \bar{a}$	$0 = \bar{w}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	c	c	$0 = DET$	$0 = c$

TABLE II

TABULAR DISPLAY OF STRUCTURE OF AUTOMATIC CIRCUIT
$A, \underline{A}, B, \underline{B}$

Event No.	Event	Inputs a b	CS	Shut Off	Shut Off Set	Shut Off Reset
1	A	0 0	$\bar{b}$	W_1	b	a
2	$\underline{A}$	1 0	a	R S		
3	B	0 0	$\bar{a}$	W_2	a	b
4	$\underline{B}$	0 1	b	R S		

simultaneously commanding cylinder A to continue to extend and, thus, a contradiction exists. To eliminate this undesirable situation, a shut-off valve, W_1, is placed in the $\bar{b}$ signal line. Now signal a directs cylinder A to retract and at the same time cuts off the opposing signal $\bar{b}$, venting the A extend side of the power control valve to tank. When the next signal $\bar{a}$ comes on, it will have to pass through valve W_2 before it can reach the power control valve for cylinder B. Therefore, signal a sets or opens W_2 at the same time it shuts off W_1. Likewise, signal b turns off or resets W_2 while opening W_1. The arrows indicate the action on the W valves. An arrow pointing down sets the valve while an arrow pointing up indicates a reset command.

The last two columns are a tabular equivalency of the arrows. In row 1, b is entered in the sixth column to indicate that signal b opens valve W_1, while in the last column and row 1, the lower case a indicates the shut-off or reset signal for W_1.

It must be noted that a delay in switching the power control valve can occur while the actuating signal cuts off the opposing signal. However, this delay is less than that which results from combining input signals. This is because the new actuating signal is already acting on the power control valve as it switches the shut-off valve. In the combined signal situation, the new signal must actuate a combination element before a resulting signal can act on

the power control valve.

Table III is a tabular display of the logic structure of the circuit of Figure 10. Again, this model clearly shows where the shut-off valves are needed to eliminate signal opposition and indicates the signals which are used to set and reset the shut-off valves.

The two tabular displays were constructed using information from existing automatic sequencing circuits and reveal in logic notation the circuit structure. However, the real significance is that these tables could have been used to synthesize the circuits if only the sequential specifications were known. For example, the first four columns can be completed with information implicitly contained in the specification. Now, assuming that the CS column signals are all that are required to activate events in the same rows, signal contradictions become revealed. When a contradiction occurs, a W valve is required to shut off the opposing signal. After the number of W valves are established, the problem is to select signals which will appropriately set and reset these valves.

Thus, recognition of the role which shut-off valves play in an automatic fluid logic circuit and establishment of a criterion for systematically selecting these valves are considered important steps in the development of a synthesis procedure. Next, a more complicated sequential circuit will be investigated to establish further

TABLE III

TABULAR DISPLAY OF STRUCTURE OF AUTOMATIC CIRCUIT
$A, \underline{A}, B, \underline{B}, C, \underline{C}$

Event No.	Event	Inputs a b c	CS	Shut Off	Shut Off Set	Shut Off Reset
1	A	0 0 0	$\bar{c}$	W_1	c	a
2	$\underline{A}$	1 0 0	a	R S		
3	B	0 0 0	$\bar{a}$	W_2	a	b
4	$\underline{B}$	0 1 0	b	R S		
5	C	0 0 0	$\bar{b}$	W_3	b	c
6	$\underline{C}$	0 0 1	c	R S		

desirable features.

An intuitively designed automatic circuit with the sequence A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$ is shown in Figure 11. The circuit is labeled so that the equations can be written in Boolean Algebra notation. The output equations are as follow:

$$A = \bar{a}(b\bar{y}_4\ \bar{a}y_1 + \bar{b}\ \bar{y}_3\ \bar{a}\ \bar{y}_1) = \bar{a}by_1\ \bar{y}_4 + \bar{a}\ \bar{b}\ \bar{y}_1\bar{y}_3$$

$$A = a\ \bar{y}_2$$

$$B = \bar{b}(\bar{a}\ y_1\ \bar{b}\ y_3 + a\ y_2\ \bar{b}\ \bar{y}_3) = \bar{a}\ \bar{b}\ y_1\ y_3 + a\ \bar{b}\ y_2\bar{y}_3$$

$$\underline{B} = b\ y_4$$

The equations for memory valve operation are tabulated below:

SECONDARY	SET	RESET
Y_1	$\bar{b}\ y_3$	$b\ a\ \bar{y}_2$
Y_2	$\bar{b}\ \bar{y}_3$	$\bar{b}\ y_3$
Y_3	$a\ b\ y_4$	$\bar{a}\ \bar{y}_1$
Y_4	$\bar{a}\ \bar{y}_1$	$\bar{a}\ y_1$

An operations table can now be prepared to verify the proper sequential operation of the circuit. This table is shown in Table IV. The table is started by listing the number and associated event in the first two columns. The states of the inputs are listed in the third column. The state of the input in each row represents the stabilized condition of the inputs at the completion of the previous

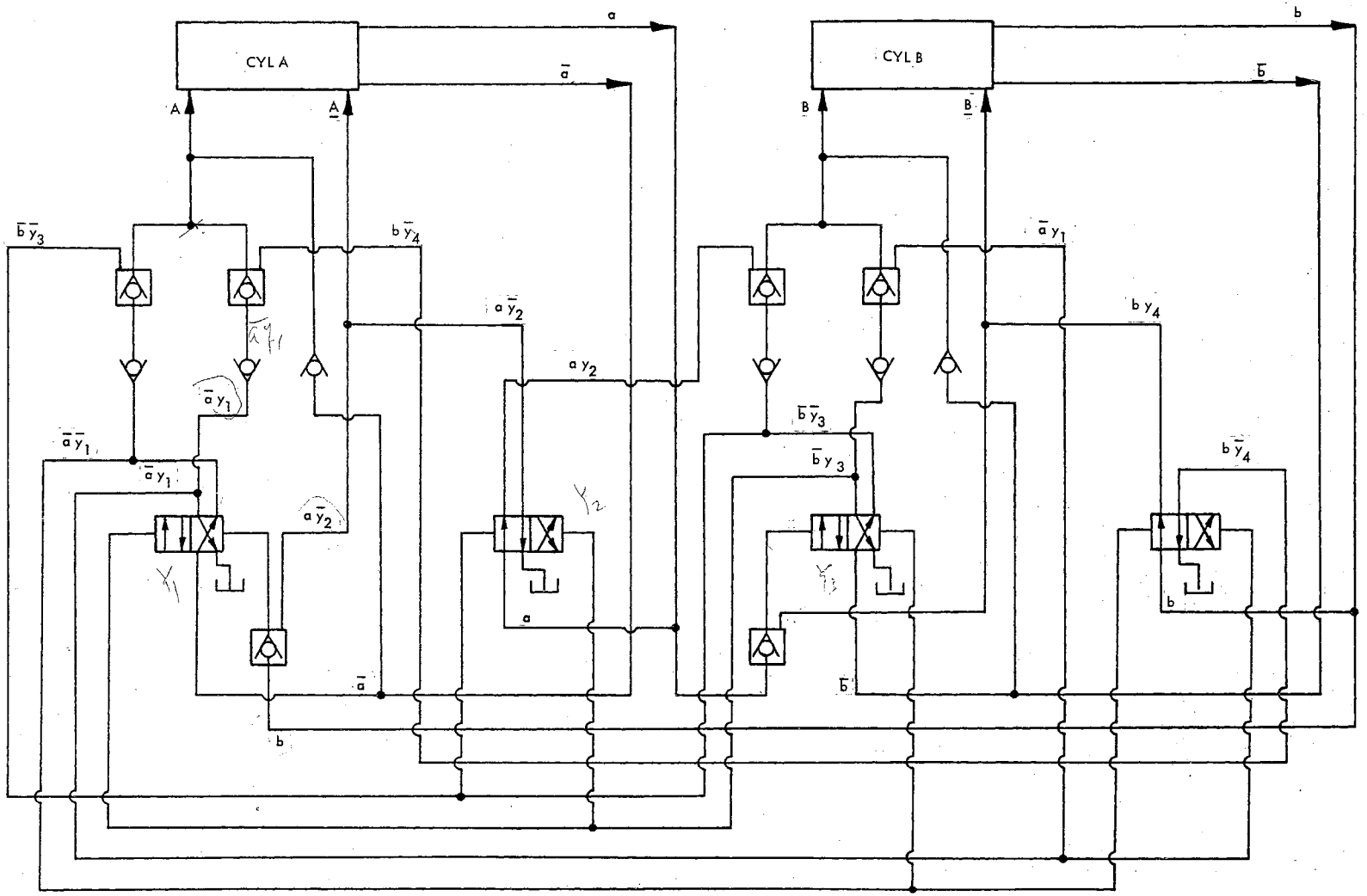


Figure 11. Intuitively Designed Automatic Circuit A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$

TABLE IV

OPERATIONS TABLE FOR INTUITIVELY DESIGNED AUTOMATIC CIRCUIT
$A, B, \underline{B}, \underline{A}, B, A, \underline{A}, \underline{B}$

No.	EVENT	ab	A	$\underline{A}$	B	$\underline{B}$	Y_1	Y_2	Y_3	Y_4
1	A	00	$\bar{a}\bar{b}y_1\bar{y}_3$	$0 = y_2$	$0 = \bar{a}\bar{y}_1$	$0 = \bar{b}$	$0 = DET$	$\bar{b}\ \bar{y}_3$	$0 = \bar{a}\bar{y}_1$	$\bar{a}\ \bar{y}_1$
2	B	10	$0 = a$	$0 = y_2$	$a\bar{b}y_2\bar{y}_3$	$0 = \bar{b}$	$0 = DET$	$\bar{b}\ \bar{y}_3$	$0 = DET$	DET
3	$\underline{B}$	11	$0 = a$	$0 = y_2$	$0 = b$	$b\ y_4$	$0 = DET$	DET	$a\ b\ y_4$	DET
4	$\underline{A}$	10	$0 = a$	$a\ \bar{y}_2$	$0 = ay_3$	$0 = \bar{b}$	$\bar{b}\ y_3$	$0 = \bar{b}\ y_3$	DET	DET
5	B	00	$0 = \bar{b}y_3$	$0 = \bar{a}$	$\bar{a}\bar{b}y_1y_3$	$0 = \bar{y}_4$	$\bar{b}\ y_3$	$0 = \bar{b}y_3$	DET	$0 = \bar{a}y_1$
6	A	01	$\bar{a}by_1y_4$	$0 = \bar{a}$	$0 = b$	$0 = \bar{y}_4$	DET	$0 = DET$	DET	$0 = \bar{a}\ y_1$
7	$\underline{A}$	11	$0 = a$	$a\ \bar{y}_2$	$0 = b$	$0 = \bar{y}_4$	$0 = ab\bar{y}_3$	$0 = DET$	DET	$0 = DET$
8	$\underline{B}$	01	$0 = by_4$	$0 = y_2$	$0 = b$	$b\ y_4$	$0 = DET$	$0 = DET$	$0 = \bar{a}\ \bar{y}_1$	$\bar{a}\ \bar{y}_1$

event. For example, in row 3, the desired event is for Cylinder B to retract. The input signals which are available to help accomplish the desired event are a = 1 and b = 1.

The next four columns of the table provide space for the equations which produce the desired outputs of the circuit. The last four columns are allocated to the equations associated with the secondaries or memory valves. Now, the table is ready to receive the circuit operation equations.

An explanation of how this table is filled out is in order since the circuit is considerably more complicated than the previously discussed circuits. In this case, it is necessary to work with the circuit schematic as well as with the algebraic equations, particularly in establishing which elements provide the tanking functions for the outputs which must be off.

Looking at row 1, it is apparent that the first desired event is for Cylinder A to extend. It is assumed at this point that a = 0 and b = 0 and that the memory valves are in their required positions. (These assumptions will be verified as the table is filled out, providing the circuit is actually designed to perform the desired sequence. Otherwise, the table will contain contradictions which show that the circuit will not work.) Now referring to the output equations, it is obvious that the only possible combination of signals and memory valve

positions which will permit Cylinder A to extend is $\bar{a}\ \bar{b}\ \bar{y}_1\bar{y}_3$. Therefore, this combination is entered in row 1 in the column A. Secondaries Y_1 and Y_3 must both be zero or in the "reset" position. From the tabulated memory valve operation equations, it can be seen that no set or reset signal is acting on Y_1. Thus, the detent must be holding Y_1 in the reset position and "0 = DET" is accordingly entered in row 1 and column Y_1. Looking at Y_3 and the tabulated equations, one can see that the signal $\bar{a}\ \bar{y}_1$ is acting to reset Y_3. Accordingly $0 = \bar{a}\ \bar{y}_1$ is entered in row 1 and column Y_3. Similarly, the combination $\bar{b}\ \bar{y}_3$ indicates that memory valve Y_2 is in the "set" or "on" position and $\bar{a}\ \bar{y}_1$ indicates that Y_4 is also set.

Since the desired output is A, the output $\underline{A}$ must be off and vented to tank. By looking at the equation $\underline{A} = a\ \bar{y}_2$ and the circuit, it is seen that this condition is satisfied by Y_2 being in the set position. Thus, $0 = y_2$ is entered in row 1 and column $\underline{A}$. Output B must also be off because Cylinder B is to remain retracted until A has completely extended. Both parts of the right side of the equation $B = \bar{a}\ \bar{b}\ y_1y_3 + a\ \bar{b}\ y_2\bar{y}_3$ must be zero to satisfy this condition. Since a = 0 and b = 0, y_1 or y_3 must be zero to make the first part zero. From row 1 of the table, y_1 and y_3 are both found to be zero, which takes care of the first part of the equation. The second part is also zero because a = 0. Therefore, the variables $\bar{a}$ and $\bar{y}_1$ are sufficient to prevent an output B. The

equation $O = \bar{a}\,\bar{y}_1$ is entered in the first row and column B. It does not matter whether the output signal $\underline{B}$ is on or not during the extension of cylinder A. However, $\underline{B} = O$ because $b = O$ and "$O = \bar{b}$" is entered under $\underline{B}$ in row 1.

The first row of the table is now complete. The next step is to establish the states of the memory valves in the second row. First, it is established that Y_4 could not have switched at the completion of the extension of Cylinder A and Y_4 remains in the "set" position because of the detent. "DET" is entered under Y_4 in row 2. This information is then used with the stabilized states of the inputs to show that Y_3 is being held in the "reset" position by the detent. In turn, the conditions of Y_1 and Y_2 are likewise established and the entries are accordingly made in the table.

After the states of the secondaries are determined for row 2, the output conditions can be found, completing the second row of the table. The third and subsequent rows are filled out by a similar procedure until the table is complete. The last row is checked to verify that it is compatible with the first row where the assumptions were made concerning the initial states of the memory valves.

As can be seen from Table IV, all of the output and memory valve operation conditions are satisfied. This confirms that the circuit will automatically operate in the specified sequential manner. It should be obvious from the preceding that the operations table is a very

powerful tool for analyzing and checking out an existing circuit. To have checked this circuit any other way would have been extremely difficult, especially if there had been something wrong with the circuit.

There are some interesting features of the circuit just analyzed which can best be shown in a tabular display similar to those made for the previous circuits. The first three columns of Table V are the same as the first three columns of the operations table (Table IV). The fourth column shows the signal which changed at the completion of the previous event. The last column contains the signal which was actually used to initiate the event in the same row.

In the first row, the new signal is $\bar{b}$ and the signal used to command cylinder A to extend is $\bar{a}\ \bar{y}_1 \cdot \bar{b}\ \bar{y}_3$. From the operations table it is apparent that the $\bar{a}\ \bar{y}_1$ signal is already on and the Y_3 valve is in the reset position. The circuit diagram shows that when $\bar{b}$ comes on, it is gated through Y_3 and opens a check valve "and" gate to let the $\bar{a}\ \bar{y}_1$ signal pass and act on the power control valve. Note that there is a delay which occurs when the $\bar{b}\ \bar{y}_3$ signal opens the "and" gate. Had the $\bar{b}\ \bar{y}_3$ signal gone directly to act on the power control valve, there would be no delay. A similar situation occurs in rows 2, 5, and 6.

In row 4, the new signal is $\bar{b}$ while the output signal is a $\bar{y}_2$. The operations table shows that signal $\bar{b}$ is gated through Y_3 and resets Y_2. Again, a delay results

TABLE V

TABULAR DISPLAY OF PARTIAL STRUCTURE OF INTUITIVELY DESIGNED SEQUENTIAL CIRCUIT
A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$

No.	Event	Inputs a b	CS	Signal Used
1	A	0 0	$\bar{b}$	$\bar{a}\bar{y}_1 \cdot \bar{b}\bar{y}_3$
2	B	1 0	a	$ay_2 \cdot \bar{b}\bar{y}_3$
3	$\underline{B}$	1 1	b	(by_4)
4	$\underline{A}$	1 0	$\bar{b}$	$a\bar{y}_2$
5	B	0 0	$\bar{a}$	$\bar{a}\bar{y}_1 \cdot \bar{b}y_3$
6	A	0 1	b	$\bar{a}y_1 \cdot by_4$
7	$\underline{A}$	1 1	a	$(a\bar{y}_2)$
8	$\underline{B}$	0 1	$\bar{a}$	by_4

while valve Y_2 is reset. This condition is repeated in row 8.

In rows 3 and 7 the output signals are circled. Note that the changed signal b in row 3 is directly involved in generating the output signal. The operations table shows that valve Y_4 was in the "set" state before b came on. Thus, signal b is gated through Y_4 and goes immediately to shift the power control valve. Likewise, in row 7, signal a goes directly through a prepared path to act on the power valve.

Summarizing, there are six delays built into the logic circuit. These occur when one signal has to combine with another to produce an output. In two instances, (rows 4 and 8) the memory valves are shifted while the input ports are pressurized. The most desirable output signals are circled in rows 3 and 7. In each case here, there is no delay because the event completion signal is guided through a pre-set memory valve directly to activate the next event.

Two desirable features of well-designed circuits were brought out in this chapter. These are the use of the shut-off valves to eliminate signal oppositions and the presetting of Y valves to avoid signal transmission delays. The next chapter will show how these features can be incorporated into circuits during synthesis.

CHAPTER V

DEVELOPMENT OF SYNTHESIS PROCEDURE

Initial Development

The objective of the following synthesis efforts will be to force the circuits to contain the same desirable features as the example circuits of Chapter IV.

The last example will be used as a starting point. A preliminary synthesis table is shown in Table VI. The first four columns contain the same information as the tabular display in Table V. This time, however, an attempt will be made to always use the changed input signal to start the next event. Looking at the fourth column from the left, one can see that signal $\bar{b}$ associates with event A in row 1 and with $\underline{A}$ in row 4. That is, $\bar{b}$ is the signal which commands these events to occur. Therefore, in the next column (Associated Events) A,$\underline{A}$ is entered. An arrow is drawn from $\bar{b}$ to A,$\underline{A}$ to show the relationship. Since signal $\bar{b}$ is asked to go to two different places at different intervals of the sequence, a memory gating valve is needed. The last column contains the signal and memory valve combination. In row 1, the combination is $\bar{b}\ y_1$, and in row 4 the combination becomes $\bar{b}\ \bar{y}_1$. Between events 1

TABLE VI

PRELIMINARY SYNTHESIS TABLE I FOR AUTOMATIC CIRCUIT
$A, B, \underline{B}, \underline{A}, B, A, \underline{A}, \underline{B}$

No.	Event	Inputs	I (Changed Input)	II (Assoc. Events)	*III
1	A	$\bar{a}\ \bar{b}$	$\bar{b}$	$A, \underline{A}$	$\bar{b}\ y_1$
2	B	$a\ \bar{b}$	a	$B, \underline{A}$	$a\ y_2$
3	$\underline{B}$	$a\ b$	b	$\underline{B}, A$	$b\ y_3$
4	$\underline{A}$	$a\ \bar{b}$	$\bar{b}$		$\bar{b}\ \bar{y}_1$
5	B	$\bar{a}\ \bar{b}$	$\bar{a}$	$B, \underline{B}$	$\bar{a}\ y_4$
6	A	$\bar{a}\ b$	b		$b\ \bar{y}_3$
7	$\underline{A}$	$a\ b$	a		$a\ \bar{y}_2$
8	$\underline{B}$	$\bar{a}\ b$	$\bar{a}$		$\bar{a}\ \bar{y}_4$

*III Changed input signal and memory valve combination.

and 4, the memory valve Y_1 will have to shift from "set" to "reset".

Similarly, events are associated with the remaining input signals and memory gating valves assigned to properly distribute the signals. The last column shows that four memory valves or Y valves are required. Note that at least two events occur before a particular Y valve changes from its previous state to a new state. For example, in row 3, Y_3 is in the set state and in row 6, Y_3 is required to be in the reset state. Thus, there are two opportunities to change the state of Y_3 between events 3 and 6. More will be said about this later.

It is now necessary to check the output signal combinations in the last column for contradictions. This is done by examining each event in the sequence and checking to see if an output signal which would cause the negation of the event is still on. This amounts to checking the output signal associated with the most recent negation of the event. For example, in row 1, the output combination is $\bar{b}\ y_1$, commanding event A to occur. The most recent negation was row 7 where the signal was a $\bar{y}_2$. It can be seen from the input combination in row 1, that signal a is off and signal a $\bar{y}_2$ must consequently be off. Thus, there is no conflict. Likewise, row 2 shows no conflict with row 8. However, rows 2 and 3 are found to represent a contradiction, with signal a y_2 still commanding cylinder B to extend while signal b y_3 orders cylinder B to retract.

Therefore, signal a y_2 must be cut off before cylinder B can retract. Accordingly, a shut off valve is added.

Table VII shows the table compressed somewhat with an additional column labeled "Shut-off Valves". Otherwise, the table is the same as Table VI. Two shut-off or W valves are required as indicated in the last column. It is also apparent when these valves must be on or off. Now, if appropriate signals can be selected for setting and resetting the Y and W valves, a workable circuit should result. The manner in which this is done is shown in Table VIII.

The first seven columns are the same as Table VII. The next four columns are for the Y valves and the last two for the two W valves. In row 1, the output signal that causes cylinder A to extend is $\bar{b}\ y_1$. This same signal is used to set valves Y_2 and W_1. After the first event is completed, signal a comes on and passes through Y_2 and W_1 so that the output signal for the second event is a $y_2\ w_1$, which also sets Y_3. The output signal for event number 3 is $b\ y_3$ which shuts off the opposing signal a y_2 and simultaneously resets Y_1. In a similar fashion, the set and reset signals are chosen for the remaining memory valves.

With the table complete, the circuit equations are read directly. The output equations for each event are read from columns III and IV and are written at the left below the table. For example, event A will occur as the

TABLE VII

PRELIMINARY SYNTHESIS TABLE II FOR AUTOMATIC CIRCUIT
$A, B, \underline{B}, \underline{A}, B, A, \underline{A}, \underline{B}$

No.	Event	a b	I	II	III	IV (Shut Off Valves)
1	A	$\bar{a}\,\bar{b}$	$\bar{b}$	$A, \underline{A}$	$\bar{b}\ y_1$	
2	B	$a\,\bar{b}$	a	$B, \underline{A}$	$a\ y_2$	w_1
3	$\underline{B}$	a b	b	$\underline{B}, A$	$b\ y_3$	$\bar{w}_1$ (w_1 must be off)
4	$\underline{A}$	$a\,\bar{b}$	$\bar{b}$		$\bar{b}\ \bar{y}_1$	
5	B	$\bar{a}\,\bar{b}$	$\bar{a}$	$B, \underline{B}$	$\bar{a}\ y_4$	
6	A	$\bar{a}$ b	b		$b\ \bar{y}_3$	w_2
7	$\underline{A}$	a b	a		$a\ \bar{y}_2$	$\bar{w}_2$ (w_2 must be off)
8	$\underline{B}$	$\bar{a}$ b	$\bar{a}$		$\bar{a}\ \bar{y}_4$	

TABLE VIII

SYNTHESIS OF EIGHT-EVENT SEQUENCE

No.	Event	ab	I	II	III	IV	Y_1	Y_2	Y_3	Y_4	W_1	W_2
1	A	$\bar{a}\,\bar{b}$	$\bar{b}$	A, $\underline{A}$	$\bar{b}\,y_1$			S			S	
2	B	$a\,\bar{b}$	a	B, $\underline{A}$	$a\,y_2$	w_1			S			
3	$\underline{B}$	a b	b	$\underline{B}$, A	$b\,y_3$	$\bar{w}_1$	R				R	
4	$\underline{A}$	$a\,\bar{b}$	$\bar{b}$		$\bar{b}\,\bar{y}_1$					S		
5	B	$\bar{a}\,\bar{b}$	$\bar{a}$	B, $\underline{B}$	$\bar{a}\,y_4$				R			S
6	A	$\bar{a}$ b	b		$b\,\bar{y}_3$	w_2		R				
7	$\underline{A}$	a b	a		$a\,\bar{y}_2$	$\bar{w}_2$				R		R
8	$\underline{B}$	$\bar{a}$ b	$\bar{a}$		$\bar{a}\,\bar{y}_4$		S					

SYNTHESIS TABLE

I. CHANGED INPUT SIGNAL

II. EVENTS ASSOCIATED WITH CHANGED INPUT SIGNAL

III. SIGNAL AND MEMORY VALVE COMBINATION

IV. SHUT-OFF VALVES

OUTPUT EQUATIONS

$A = \bar{b}\,y_1 + b\,\bar{y}_3 w_2$

$\underline{A} = \bar{b}\,\bar{y}_1 + a\,\bar{y}_2(\bar{w}_2)$

$B = a\,y_2 w_1 + \bar{a}\,y_4$

$\underline{B} = b\,y_3\,(\bar{w}_1) + \bar{a}\,\bar{y}_4$

MEMORY VALVE EQUATIONS

	SET	RESET
Y_1	$\bar{a}\,\bar{y}_4$	$b\,y_3$
Y_2	$\bar{b}\,y_1$	$b\,\bar{y}_3$
Y_3	$a\,y_2 w_1$	$\bar{a}\,y_4$
Y_4	$\bar{b}\,\bar{y}_1$	$a\,\bar{y}_2$
W_1	$\bar{b}\,y_1$	$b\,y_3$
W_2	$\bar{a}\,y_4$	$a\,\bar{y}_2$

result of output $\bar{b}\ y_1$ or $b\ \bar{y}_3 w_2$. Event A will occur as the result of output $b\bar{y}_1$, or a $\bar{y}_2$ ($\bar{w}_2$). The $\bar{w}_2$ in parentheses indicates cut off of the signal opposing signal a $\bar{y}_2$. The memory valve equations are read from the same columns and are tabulated below the table at the right.

Table VIII is called a "Synthesis Table" since it is used to synthesize the equations of a circuit which will satisfy the sequence specification. In completed form, the table is logically equivalent to the circuit which results from implementing the equations with fluid logic hardware.

To assure that the newly synthesized circuit will function properly, it is checked in the operations table (Table IX). The dashed lines indicate optional or "don't care" conditions for the outputs. The table is built up one row at a time in the same manner as described for the intuitively designed circuit of the previous chapter. Except for optional conditions, the stable states of all the output signals and memory valves are shown at every interval of the sequence as well as the conditions which produce or maintain these states.

Once the circuit equations have been determined from the synthesis table, a physical circuit can readily be implemented with fluid logic hardware or elements. A circuit schematic is shown in Figure 12. To avoid cluttering the diagram, the set and reset signal lines and segments of the input signal lines are omitted. However,

TABLE IX

OPERATIONS TABLE FOR AUTOMATIC CIRCUIT A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$

No.	Event	ab	A	$\underline{A}$	B	$\underline{B}$	Y_1	Y_2	Y_3	Y_4	W_1	W_2
1	A	00	$\bar{b}\ y_1$	$0 = y_1 y_2$	$0 = \bar{a}\ \bar{y}_4$	—	$\bar{a}\ \bar{y}_4$	$\bar{b}\ y_1$	$0 =$ DET	$0 =$ DET	$\bar{b}\ y_1$	$0 =$ DET
2	B	10	—	$0 = y_1 y_2$	$a\ y_2\ w_1$	$0 = \bar{b}\ a$	DET	$\bar{b}\ y_1$	$a\ y_2 w_1$	$0 =$ DET	$\bar{b}\ y_1$	$0 =$ DET
3	$\underline{B}$	11	—	$0 = b\ y_2$	$0 = \bar{w}_1 \bar{y}_4$	$b\ y_3$	$0 = b\ y_3$	DET	DET	$0 =$ DET	$0 = b\ y_3$	$0 =$ DET
4	$\underline{A}$	10	$0 = \bar{y}_1 \bar{w}_2$	$\bar{b}\ \bar{y}_1$	$0 = \bar{w}_1 a$	—	$0 =$ DET	DET	DET	$\bar{b}\ \bar{y}_1$	$0 =$ DET	$0 =$ DET
5	B	00	$0 = \bar{y}_1 \bar{b}$	—	$\bar{a}\ y_4$	$0 = \bar{y}_3 y_4$	$0 =$ DET	DET	$0 = \bar{a}\ y_4$	$\bar{b}\ \bar{y}_1$	$0 =$ DET	$\bar{a}\ y_4$
6	A	01	$b\ \bar{y}_3 w_2$	$0 = b\ \bar{a}$	—	$0 = \bar{y}_3 y_4$	$0 =$ DET	$0 = b \bar{y}_3 w_2$	$0 = a\ \bar{y}_4$	DET	$0 =$ DET	$\bar{a}\ y_4$
7	$\underline{A}$	11	$0 = \bar{y}_1 \bar{w}_2$	$a\ \bar{y}_2$	—	$0 = \bar{y}_3 a$	$0 =$ DET	$0 =$ DET	$0 =$ DET	$0 = a\ \bar{y}_2$	$0 =$ DET	$0 = a\ \bar{y}_2$
8	$\underline{B}$	01	$0 = b\ \bar{w}_2$	—	$0 = \bar{w}_1 \bar{y}_4$	$\bar{a}\ \bar{y}_4$	$\bar{a}\ \bar{y}_4$	$0 =$ DET	$0 =$ DET	$0 =$ DET	$0 =$ DET	$0 =$ DET

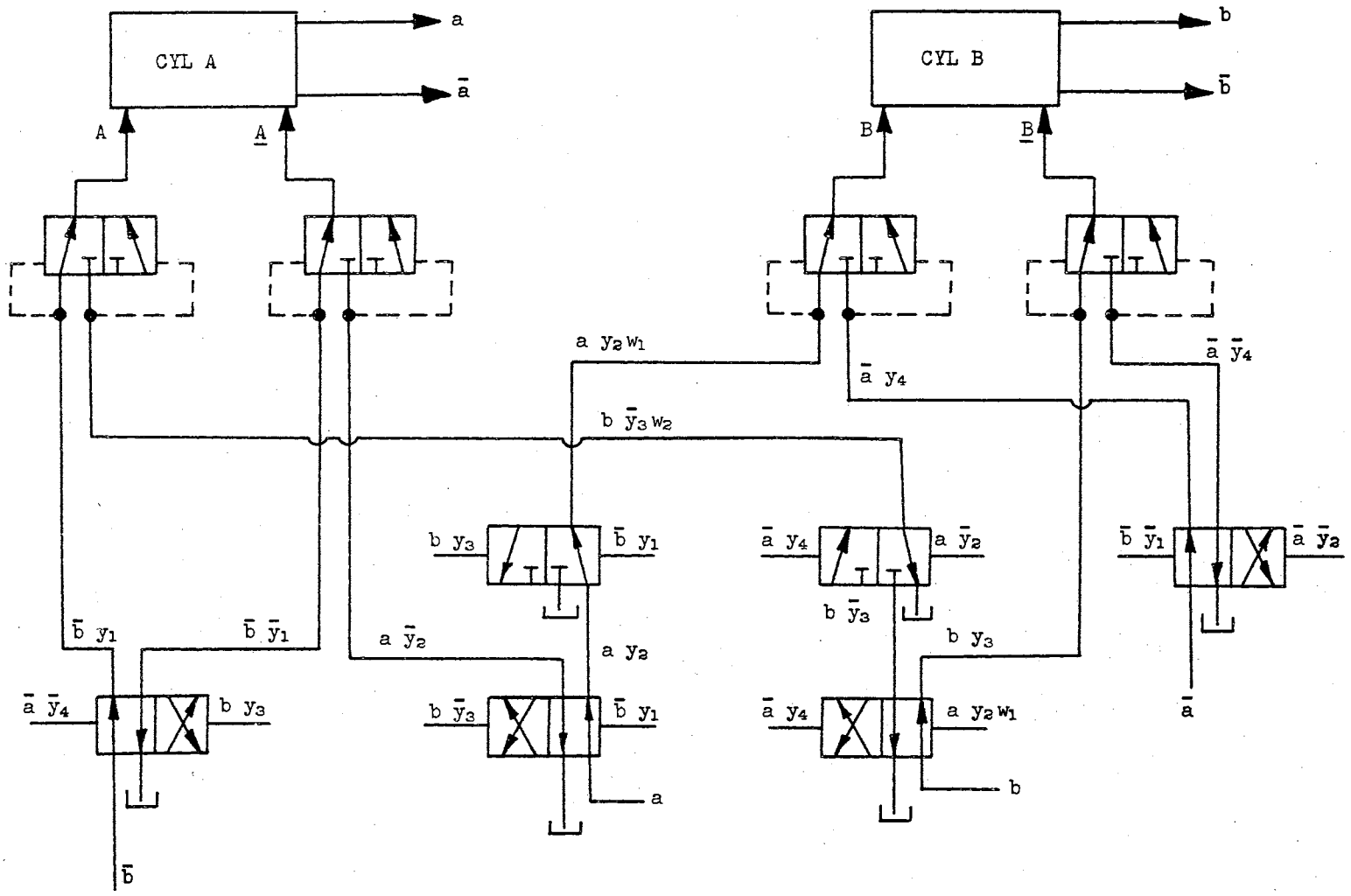


Figure 12. Schematic for Automatic Circuit A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$

it is easy to see where each of these lines would connect and the circuit could be implemented with actual hardware using the schematic as a guide.

The valves immediately beneath cylinders A and B are "or" valves so that output A, for example, is obtained from signal $\bar{b}\ y_1$ or $b\ \bar{\bar{y}}_3\ w_2$. This means that if the valve is in the position shown, and signal $b\ \bar{\bar{y}}_3\ w_2$ comes on, the valve will shift to the left, allowing the signal to pass through. A slight delay occurs while the "or" valve is shifting. Now, if the or valve could be shifted prior to the output signal's arrival and held by a detent, there would be no delay and a faster circuit would result.

It so happens that this pre-shifting of the "or" valve can be accomplished and the result is shown in Figure 13. Note that the circuit is the same except that the "or" valves are now pilot-operated detent valves and are the same type as the shut-off valves. The signal used to shift the "or" valve is the same signal used to set or reset the Y valve which directs the signal to the "or" valve. Inspection of the schematic shows that there is no conflict of signals by using this method.

A total of ten separate pilot-operated detent valves are required to implement this circuit. Four are gating valves and six are 3-way valves. Two signal transmission delays occur during a cycle of the sequence; one at the end of event 2 and the other at the end of event number 6.

Referring back to Figure 11, it is seen that the

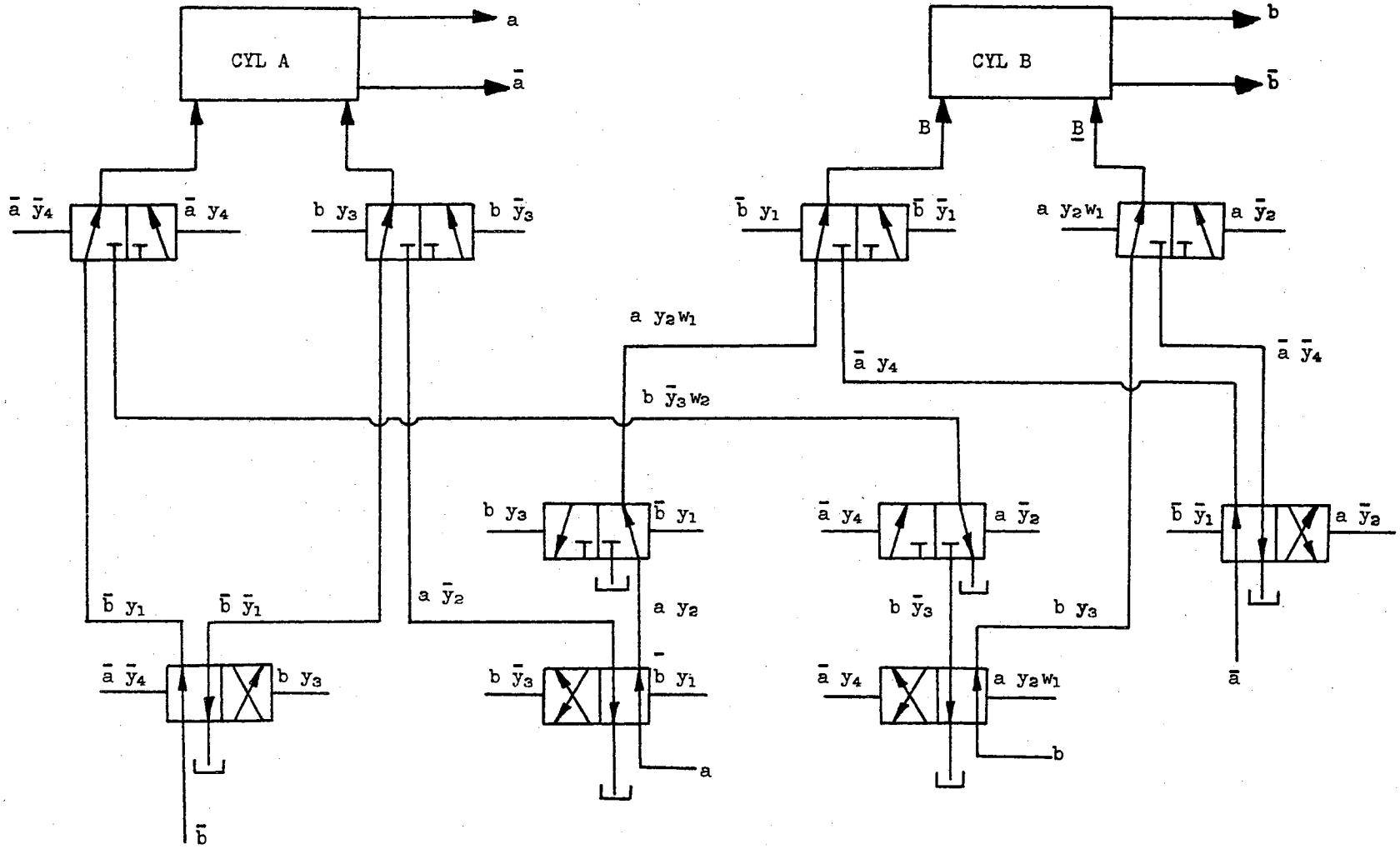


Figure 13. Schematic for Automatic Circuit A, B, B̲, A̲, B, A, A̲, B̲ (Modified)

intuitively designed circuit also contains a total of ten valves (counting a pilot check valve and a plain check valve combination as one element). Here too, four gating valves are used.

From a standpoint of complexity, the two circuits are identical. However, if speed of operation is to be counted as an important factor, the circuit synthesized by the table must be judged superior because it has only two delays while the other has six. The intuitively designed circuit provides a good basis for comparison. It was synthesized by an experienced designer and has been very carefully checked for possible simplification. Then too, other formal synthesis procedures have failed to yield an improved circuit (22).

The results obtained so far are encouraging. However, the procedure must be general if it is to be capable of handling the various types of sequences that may be encountered. The remainder of this chapter will be devoted to investigating a representative cross section of sequential problems and to developing the procedure as required to handle these problems.

The first step is represented by a modification of the sequential problem just completed, with the results contained in Table X. Note that only three Y valves are required this time because signal a always associates with event B. Also, shut-off valve W_1 must be open at two intervals (2 and 6) and closed during interval 3. In the

TABLE X

SYNTHESIS OF MODIFIED SEQUENCE

No.	Event	ab	I	II	III	IV	Y_1	Y_2	Y_3	W_1	W_2
1	A	$\bar{a}\,\bar{b}$	$\bar{b}$	A, $\underline{A}$	$\bar{b}\ y_1$			S			
2	B	$a\,\bar{b}$	a	B, B	a	w_1					
3	$\underline{B}$	a b	b	$\underline{B}$, $\underline{A}$	b y_2	$\bar{w}_1$	R			R	S
4	$\underline{A}$	$a\,\bar{b}$	$\bar{b}$		$\bar{b}\ \bar{y}_1$	w_2			S		
5	A	$\bar{a}\,\bar{b}$	$\bar{a}$	A, $\underline{B}$	$\bar{a}\ y_3$	$\bar{w}_2$		R		S	R
6	B	$a\,\bar{b}$	a		a	w_1					
7	$\underline{A}$	a b	b		b $\bar{y}_2$				R		
8	$\underline{B}$	$\bar{a}$ b	$\bar{a}$		$\bar{a}\ \bar{y}_3$		S				

SYNTHESIS TABLE

Output Equations:

$A = \bar{b}\ y_1 + \bar{a}\ y_3(\bar{w}_2)$

$\underline{A} = \bar{b}\ \bar{y}_1\ w_2 + b\bar{y}_2$

$B = a\ w_1$

$\underline{B} = b\ y_2(\bar{w}_1) + \bar{a}\ \bar{y}_3$

Memory Valve Equations

	Set	Reset
Y_1	$\bar{a}\ \bar{y}_3$	b y_2
Y_2	$\bar{b}\ y_1$	$\bar{a}\ y_3$
Y_3	$\bar{b}\ \bar{y}_1\ w_2$	b $\bar{y}_2$
W_1	$\bar{a}\ y_3$	b y_2
W_2	b y_2	$\bar{a}\ y_3$

output equations below the table, event B does not involve an "or" in its output equation. The $\bar{w}_1$ and $\bar{w}_2$ variables in parentheses indicate that the corresponding W valves must be off. However, the states of the W valves are accounted for in the memory valve equations so that it will not be necessary to include the variable in parentheses to correctly represent the circuit. After one more example, this notation will be dropped to allow more compact equations.

Proper operation of the circuit is verified in Table XI, while the circuit schematic is shown in Figure 14. Again, several of the interconnecting lines are omitted for clarity. The schematic indicates "or" valves for gating the output signals. However, these could be of the same preset type as shown in Figure 13. The same rules for selecting the preset signals would also apply.

A more complicated sequence will now be examined. Two cylinders are still involved, but the number of events is extended to ten. The synthesis is carried out in Table XII. Two new features are brought out in this example.

First of all, note that signal $\bar{a}$ associates with three separate events, requiring two Y valves to distribute the signal. This means that second order memory is involved. Secondly, signal a associates with two events, B and $\underline{A}$. However, it causes event $\underline{A}$ to occur twice during one cycle of the sequence. The consequences of this second feature will be brought out in the discussion

TABLE XI

OPERATIONS TABLE FOR AUTOMATIC CIRCUIT A, B, $\underline{B}$, $\underline{A}$, A, B, $\underline{A}$, $\underline{B}$

No.	Event	ab	A	$\underline{A}$	B	$\underline{B}$	Y_1	Y_2	Y_3	W_1	W_2
1	A	00	$\bar{b}\ y_1$	$0 = \bar{w}_2 y_2$	$0 = \bar{a}$	—	$\bar{a}\ \bar{y}_3$	$\bar{b}\ y_1$	$0 =$ DET	DET	$0 =$ DET
2	B	10	—	$0 = \bar{w}_2 y_2$	$a\ w_1$	$0 = \bar{b}a$	DET	$\bar{b}\ y_1$	$0 =$ DET	DET	$0 =$ DET
3	$\underline{B}$	11	—	$0 = b\ y_2$	$0 = \bar{w}_1$	$b\ y_2$	$0 = b\ y_2$	DET	$0 =$ DET	$0 = b\ y_2$	$b\ y_2$
4	$\underline{A}$	10	$0 = \bar{y}_1\ a$	$\bar{b}\bar{y}_1\ w_2$	$0 = \bar{w}_1$	—	$0 =$ DET	DET	$\bar{b}\ \bar{y}_1 w_2$	$0 =$ DET	DET
5	A	00	$\bar{a}\ y_3$	$0 = \bar{w}_2 \bar{b}$	$0 = \bar{a}$	—	$0 =$ DET	$0 = \bar{a}\ y_3$	DET	$\bar{a}\ y_3$	$0 = \bar{a}\ y_3$
6	B	10	—	$0 = \bar{w}_2 \bar{b}$	$a\ w_1$	$0 = \bar{y}_2 y_3$	$0 =$ DET	$0 =$ DET	DET	DET	$0 =$ DET
7	$\underline{A}$	11	$0 = \bar{y}_1\ \bar{y}_3$	$b\ \bar{y}_2$	—	$0 = \bar{y}_2 a$	$0 =$ DET	$0 =$ DET	$0 = b\ \bar{y}_2$	DET	$0 =$ DET
8	$\underline{B}$	01	$0 = b\ \bar{y}_3$	—	$0 = \bar{a}$	$\bar{a}\ y_3$	$\bar{a}\ \bar{y}_3$	$0 =$ DET	$0 = b\ \bar{y}_2$	DET	$0 =$ DET

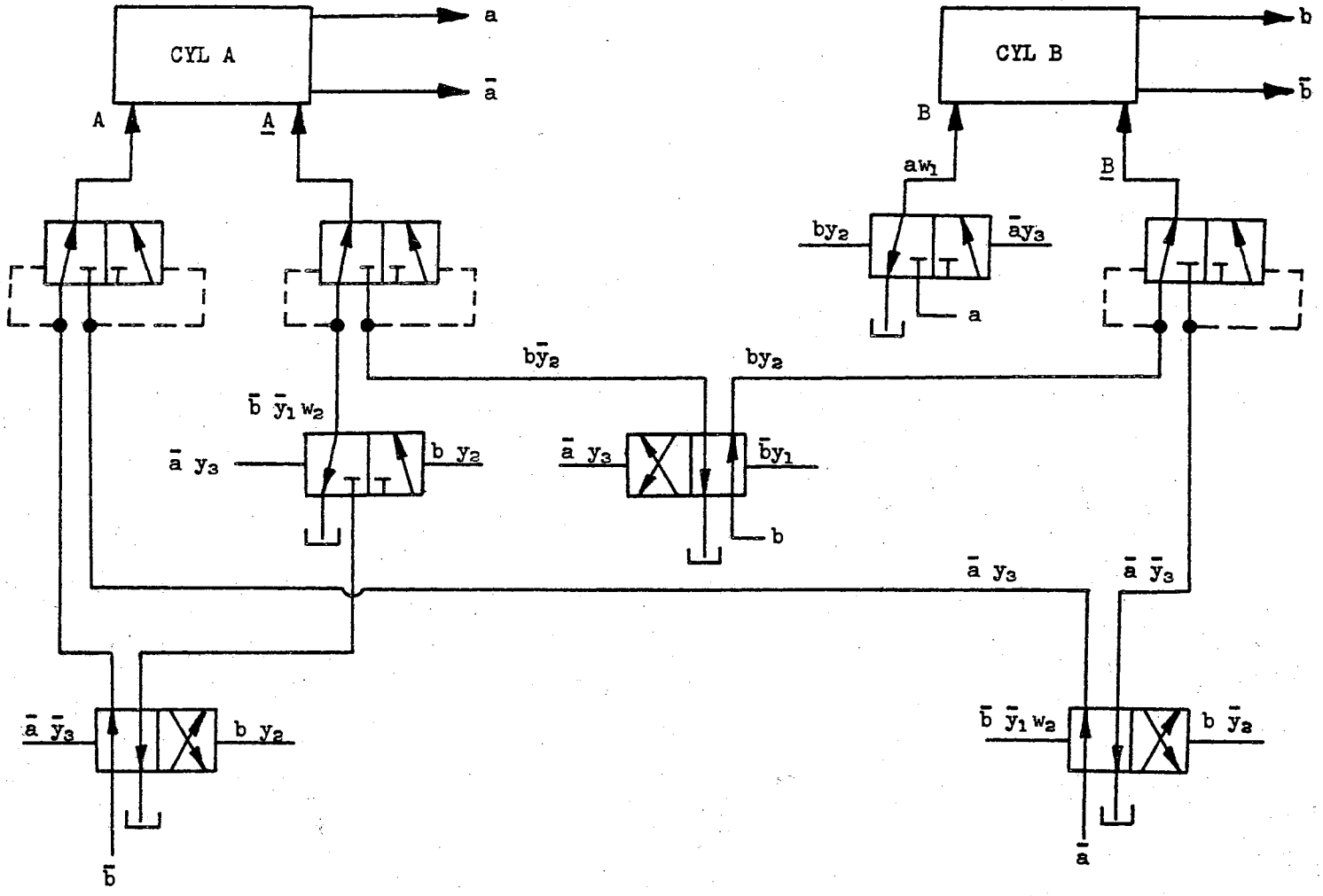


Figure 14. Schematic for Automatic Circuit A, B, $\underline{B}$, $\underline{A}$, A, B, $\underline{A}$, $\underline{B}$

TABLE XII

SYNTHESIS OF TEN-EVENT SEQUENCE

No.	E	ab	1	II	III	IV	Y_1	Y_2	Y_3	Y_4	Y_5	W_1	W_2	W_3	Y_6
1	A	$\bar{a}\bar{b}$	$\bar{a}$	A, B, $\underline{B}$	$\bar{a}\ y_1\ y_2$				S			S			
2	B	$a\bar{b}$	a	B, $\underline{A}$, $\underline{A}$	$a\ y_3$	w_1				S					
3	$\underline{B}$	ab	b	$\underline{B}$, A	$b\ y_4$	$\bar{w}_1$					S	R			
4	$\underline{A}$	$a\bar{b}$	$\bar{b}$	$\underline{A}$, A	$\bar{b}\ y_5$			R							
5	B	$\bar{a}\bar{b}$	$\bar{a}$		$\bar{a}\ y_1\ \bar{y}_2$					R			S		
6	A	$\bar{a}b$	b		$b\ \bar{y}_4$	w_2			R						S
7	$\underline{A}$	ab	a		$a\ \bar{y}_3\ \bar{y}_6$	$\bar{w}_2$	Ry_6						Ry_6		
8	$\underline{B}$	$\bar{a}b$	$\bar{a}$		$\bar{a}\ \bar{y}_1$						R			S	
9	A	$\bar{a}\bar{b}$	$\bar{b}$		$\bar{b}\ \bar{y}_5$	w_3									R
10	$\underline{A}$	$a\bar{b}$	a		$a\ \bar{y}_3\ \bar{y}_6$	$\bar{w}_3$	$S\bar{y}_6$	$S\bar{y}_6$						$R\bar{y}_6$	

SYNTHESIS TABLE

Output Equations

$A = \bar{a}\ y_1\ y_2 + b\ \bar{y}_4\ w_2 + \bar{b}\ \bar{y}_5\ w_3$

$\underline{A} = \bar{b}\ y_5 + a\ y_3(\bar{w}_2 + \bar{w}_3)$

$B = a\ y_3\ w_1 + \bar{a}\ y_1\ \bar{y}_2$

$\underline{B} = b\ y_4(\bar{w}_1) + \bar{a}\ \bar{y}_1$

Memory Valve Equations

	Set	Reset
Y_1	$a\ \bar{y}_3\ \bar{y}_6$	$a\ \bar{y}_3\ y_6$
Y_2	$a\ y_3\ y_6$	$b\ y_5$
Y_3	$\bar{a}\ y_1\ y_2$	$b\ y_4\ w_2$
Y_4	$a\ y_3\ w_1$	$\bar{a}\ y_1\ \bar{y}_2$
Y_5	$b\ y_4$	$\bar{a}\ y_1$
Y_6	$b\ y_4\ w_2$	$b\ y_5\ w_3$
W_1	$\bar{a}\ y_1\ y_2$	$b\ y_4$
W_2	$\bar{a}\ y_1\ y_2$	$a\ y_3\ y_6$
W_3	$a\ y_1$	$a\ y_3\ \bar{y}_6$

that follows.

The column labeled III contains the input signal and memory valve combinations which are needed to cause the associated events to occur. The next column, labeled IV, indicates which outputs are contradictory and require shut-off valves. At this point of the synthesis, five Y valves and three W valves are required. The next step is to select set and reset signals for the eight memory valves.

As in the previous synthesis table, a column is allocated to each of the memory valves. The last column is labeled Y_6 and the need for this sixth Y valve will now be discussed. Note that Y_1 must be in the reset state at the beginning of event number 8. Now, the resetting is not allowed during the interval of event number 6 because input signal $\bar{a}$ is still on and switching the Y_1 valve with $\bar{a}$ on would cause a premature extension of cylinder B. Therefore, Y_1 must be reset during the interval of event number 7 and the only signal that can be used is a $\bar{y}_3$. In row 1, it is clear that Y_1 must be set before the start of event number 1. It is not permissible to shift Y_1 in row 9 because signal $\bar{a}$ is on and an unwanted output would result. For proper sequencing, Y_1 must be set in row 10 and the only signal that is available is a $\bar{y}_3$. Thus, a contradiction is evident because signal a $\bar{y}_3$ must both set and reset memory valve Y_1. This problem is overcome by providing an additional Y valve to gate the a $\bar{y}_3$ signal

appropriately for setting and resetting Y_1. The new valve, called an auxiliary valve, is labeled Y_6 and a column is provided in the table to permit selection of the associated set and reset signals. In row 7 the notation Ry_6 means that output signal a $\bar{y}_3$ is gated through Y_6 to reset Y_1. This resulting combination a $\bar{y}_3 y_6$ is also used to reset shut-off valve W_2.

The remaining set and reset signals are appropriately selected and shown in the table. The circuit equations are obtained by inspection directly from the table and written below. Note that the variable y_6 and its complement do not appear in the output equations, but are contained in the memory equations.

Proper circuit operation is verified in Table XIII. A more compact notation is used in the memory portion of the table. The capital letter D means that the valve heading that column is held in the set state by the detent during the row interval. The combination "D/S" means that the valve is being held in the reset position by the detent. "S" means that the memory valve is set by the active output signal in that row. Similarly, "R" means that the active output signal is resetting the memory valve. The y_6 or $\bar{y}_6$ in parentheses means that the active output signal is gated through Y_6 for the set or reset action.

The circuit schematic is shown in Figure 15. The second order memory combination mentioned in Chapter IV is

TABLE XIII

OPERATIONS TABLE FOR AUTOMATIC CIRCUIT A, B, $\underline{B}$, $\underline{A}$, B, A, $\underline{A}$, $\underline{B}$, A, $\underline{A}$

No.	E	ab	A	$\underline{A}$	B	$\underline{B}$	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	W_1	W_2	W_3
1	A	00	$\bar{a}\ y_1\ y_2$	$0 = \bar{y}_5 y_3$	$0 = \bar{a}\ y_2$	—	D	D	S	O/D	O/D	O/D	S	O/D	O/D
2	B	10	—	$0 = \bar{y}_5 y_3$	$a\ y_3\ w_1$	$0 = \bar{b}\ y_1$	D	D	D	S	O/D	O/D	D	O/D	O/D
3	$\underline{B}$	11	—	$0 = b\ y_3$	$0 = \bar{w}_1 y_2$	by_4	D	D	D	D	S	O/D	R	O/D	O/D
4	$\underline{A}$	10	$0 = \bar{y}_2 \bar{w}_2 \bar{w}_3$	$\bar{b}\ y_5$	$0 = \bar{w}_1\ a$	—	D	R	D	D	D	O/D	O/D	O/D	O/D
5	B	00	$0 = \bar{y}_2 \bar{b} \bar{w}_3$	—	$\bar{a}\ y_1\ \bar{y}_2$	$0 = \bar{y}_4 \bar{y}_1$	D	R	D	R	D	O/D	O/D	S	O/D
6	A	01	$b\ \bar{y}_4\ w_2$	$0 = b\ \bar{a}$	—	$0 = \bar{y}_4 y_1$	D	O/D	R	R	D	S	O/D	S	O/D
7	$\underline{A}$	11	$0 = \bar{y}_2 \bar{w}_2 \bar{w}_3$	$a\ \bar{y}_3$	—	$0 = \bar{y}_4 a$	R(y_6)	O/D	O/D	O/D	D	D	O/D	R(y_6)	O/D
8	$\underline{B}$	01	$0 = \bar{y}_2 \bar{w}_2 b$	—	$0 = \bar{w}_1 \bar{y}_1$	$\bar{a}\ \bar{y}_1$	O/D	O/D	O/D	O/D	R	D	O/D	O/D	S
9	A	00	$\bar{b}\ \bar{y}_5 w_3$	$0 = \bar{y}_5 \bar{a}$	$0 = \bar{w}_1 \bar{y}_1$	—	O/D	O/D	O/D	O/D	R	R	O/D	O/D	S
10	$\underline{A}$	10	$0 = a \bar{w}_2 \bar{w}_3$	$a\ \bar{y}_3$	$0 = \bar{w}_1 y_2$	—	S($\bar{y}_6$)	S($\bar{y}_6$)	O/D	O/D	O/D	O/D	O/D	O/D	R($\bar{y}_6$)

S = Set R = Reset
D = Detent Set O/D = Detent Reset

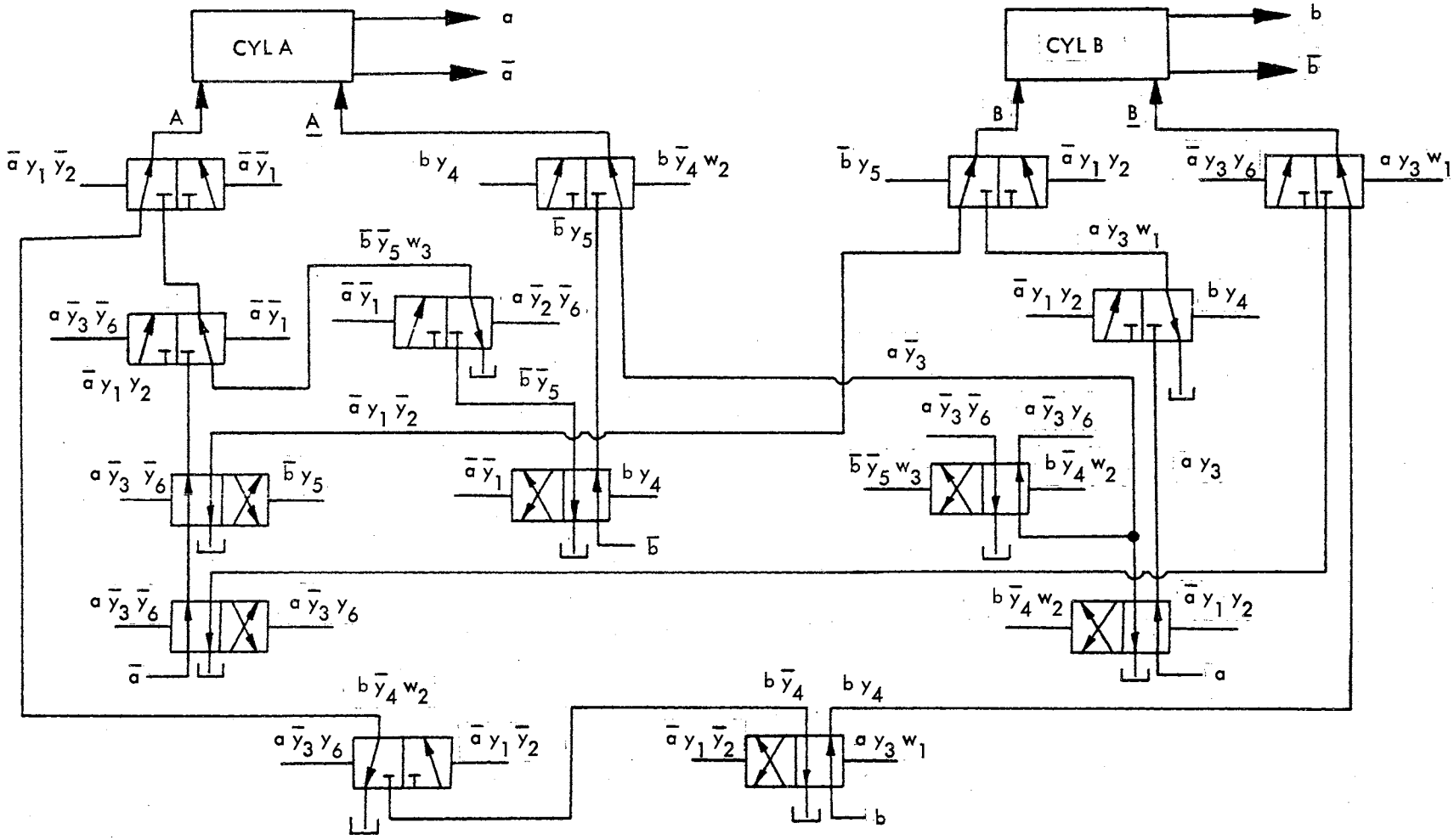


Figure 15. Schematic for Automatic Circuit A, B, B, A, B, A, A, B, A, A

at the lower left. The schematic also indicates how the a $\bar{y}_3$ signal combination line is tapped and gated through Y_6 to provide the set and reset signals for Y_1. Again, the interconnecting lines are omitted.

An evaluation of this circuit can be made by comparing it with the first circuit in this chapter. Figure 15 shows a total of fourteen valves whereas ten were required for the eight-event sequence. Two additional Y valves were required to distribute the input signals and one more W valve was needed. The third Y valve was necessary in order to overcome the contradiction in setting and resetting Y_1. Thus, it may be concluded that the circuit increased in complexity in direct relation to the increased complexity of the sequence specification. One more delay was added as a result of the extra W valve.

Counter Circuits

The three circuits discussed so far have been of the ordinary sequential type described in Chapter II. Now, counting sequences will be considered. The synthesis of a 2:2:1 counter is shown in Table XIV. Three cylinders, A, B, and C are involved. The specification requires cylinder A to cycle twice, then B to cycle twice and C to cycle once.

An additional use is made of column II in this problem. As usual, the events associated with each input signal are entered in the row in which that signal first

TABLE XIV

SYNTHESIS TABLE 2:2:1 COUNTER

No.	E	abc	I	II	III	IV	Y_1	Y_2	W_1	W_2	W_3	Y_3	Y_4
1	A	$\bar{a}\bar{b}\bar{c}$	$\bar{c}$	A		w_1						S	
2	$\underline{A}$	$a\bar{b}\bar{c}$	a	$\underline{A},\underline{A}$			Sy_3		Ry_3				
3	A	$\bar{a}\bar{b}\bar{c}$	$\bar{a}$	A,B	y_1							R	
4	$\underline{A}$	$a\bar{b}\bar{c}$	a	Y_3			$R\bar{y}_3$			$S\bar{y}_3$			
5	B	$\bar{a}\bar{b}\bar{c}$	$\bar{a}$		$\bar{y}_1$	w_2							S
6	$\underline{B}$	$\bar{a}b\bar{c}$	b	$\underline{B},\underline{B}$				Sy_4		Ry_4			
7	B	$\bar{a}\bar{b}\bar{c}$	$\bar{b}$	B,C	y_2								R
8	$\underline{B}$	$\bar{a}b\bar{c}$	b	Y_4				$R\bar{y}_4$			$S\bar{y}_4$		
9	C	$\bar{a}\bar{b}\bar{c}$	$\bar{b}$		$\bar{y}_2$	w_3							
10	$\underline{C}$	$\bar{a}\bar{b}c$	c	$\underline{C}$					S		R		

Output Equations

$A = \bar{c}\ w_1 + \bar{a}\ y_1$

$\underline{A} = a$

$B = \bar{a}\ \bar{y}_1 w_2 + \bar{b}\ y_2$

$\underline{B} = b$

$C = \bar{b}\ \bar{y}_2 w_3$

$\underline{C} = c$

Memory Valve Equations

	Set	Reset
Y_1	$a\ y_3$	$a\ \bar{y}_3$
Y_2	$b\ y_4$	$b\ \bar{y}_4$
Y_3	$\bar{c}\ w_1$	$\bar{a}\ y_1$
Y_4	$\bar{a}\ \bar{y}_1 w_2$	$\bar{b}\ y_2$
W_1	c	$a\ y_3$
W_2	$a\ \bar{y}_3$	$b\ y_4$
W_3	$b\ \bar{y}_4$	c

appears. Next, the signal distribution valves are selected and located in column III. Then the W valve requirements are determined and appropriate entries made in column IV. A column is allocated for each of these memory valves at the right of the table. Now, going back to column II, it can be seen that repeated events are entered in rows 2 and 6. This means that the input signal in each of these rows will appear twice in the sequence and cause the same event to occur each time. As far as output signal requirements are concerned, this situation is satisfactory. However, the signals appearing in column 1 must also change the states of the memory elements in the circuit. Therefore, when a repeated signal initiates the same event, the signal must be augmented by gating valves to properly switch the memory valves.

In row 2, signal a is seen to associate with event A twice; once in row 2 and the second time in row 4. Dropping down to row 4, Y_3 is entered in column II. Y_3 will also associate with the a signal in row 2. Similarly, Y_4 is entered in row 8 with the understanding that Y_4 is also associated with the b signal in row 6. The significance of these entries will become clear as the set and reset signals for the Y and W valves are selected. Finally, columns are provided for Y_3 and Y_4 at the right of the table.

The combination Sy_3 is entered in row 2 and column

Y_1, meaning that signal and valve combination ay_3 is used to set valve Y_1. Similarly, the combination $a\bar{y}_3$ is used to reset valve Y_1 in row 4. Now valve Y_3 must be reset during the interval of row 3. Therefore, the signal and valve combination $\bar{a}\ y_1$ is used to reset Y_3, and is indicated by the "R" in column Y_3. Likewise, signal b is used with valve Y_4 to set and reset Y_2. As in the previous example, valves Y_3 and Y_4 are termed "auxiliary" valves.

So far, not much has been said about the selection of signals for switching the memory valves. In some cases there is no choice in the selection while in others the selection is arbitrary. For example, it was just pointed out that Y_1 had to be reset by a $\bar{y}_3$ and Y_3 reset by $\bar{a}\ y_1$. Also, Y_1 must be reset by ay_3 because row 2 represents the only row after row 5 in which signal $\bar{a}$ is off. Now, valve Y_3 could have been set in any of the rows 5 through 10 without affecting circuit performance or the complexity of the system.

The procedure recommended by the writer is to first assign the mandatory set and reset signals and then select the remaining signals in an arbitrary, but systematic, manner. For example, Y_3 had to be reset in row 3. Row 1 was selected for setting Y_3 because it is the latest row in which Y_3 could be set. The only condition placed on the arbitrary selection is that the set and reset signals are not both on at the same time, resulting in an indeterminate state of the valve. Had the signal in row 1 been

unsuitable, row 10 would have been next choice and so on until a compatible signal was reached. This provides a pattern of consistency and assures that two designers would develop identical circuits. Also, this method would facilitate writing a computer program for mechanizing the synthesis procedure.

If integrated fluidic circuits are to be used to implement the logic, perhaps physical conditions might cause a different choice of the signals to be preferrable. It is also conceivable that interconnection of pilot lines in a large system would be simplified by some optimum choice of signals. However, these are possibilities that can only be dealt with at the implementation stage of the design. It would be a simple matter to code the arbitrary selections and indicate which alternate signals could be used.

Table XV confirms that the circuit equations just developed will produce a properly functioning fluid logic circuit. Figure 16 is the corresponding circuit schematic. As in the other example circuits, only two types of valves are needed.

Until now, all of the example circuits have been synthesized using the single input signal that came on at the completion of one event to trigger the next event. Now, a different approach will be taken. Referring back to Table XIV, the input signal column shows that the combination $\bar{a}\ \bar{b}\ \bar{c}$ occurs every other row. This combination

TABLE XV

OPERATIONS TABLE 2:2:1 COUNTER

No.	E	abc	A	$\underline{A}$	B	$\underline{B}$	C	$\underline{C}$	Y_1	Y_2	Y_3	Y_4	W_1	W_2	W_3
1	A	000	$\bar{c}w_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	O/D	O/D	S	O/D	D	O/D	O/D
2	$\underline{A}$	100	$0 = \bar{w}_1 a$	a	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	S y_3	O/D	D	O/D	R y_3	O/D	O/D
3	A	000	$\bar{a}y_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	D	O/D	R	O/D	O/D	O/D	O/D
4	$\underline{A}$	100	$0 = \bar{w}_1$	a	$0 = a\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	R $\bar{y}_3$	O/D	O/D	O/D	O/D	S $\bar{y}_3$	O/D
5	B	000	$0 = \bar{w}_1\bar{y}_1$	$0 = \bar{a}$	$\bar{a}y_1 w_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	O/D	O/D	O/D	S	O/D	D	O/D
6	$\underline{B}$	010	$0 = \bar{w}_1\bar{y}_1$	$0 = \bar{a}$	$0 = \bar{w}_2 b$	b	$0 = \bar{w}_3$	$0 = \bar{c}$	O/D	Sy_4	O/D	D	O/D	Ry_4	O/D
7	B	000	$0 = \bar{w}_1\bar{y}_1$	$0 = \bar{a}$	$\bar{b}y_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	O/D	D	O/D	R	O/D	O/D	O/D
8	$\underline{B}$	010	$0 = \bar{w}_1\bar{y}_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	b	$0 = b$	$0 = \bar{c}$	O/D	Ry_4	O/D	O/D	O/D	O/D	$S\bar{y}_4$
9	C	000	$0 = \bar{w}_1\bar{y}_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$\bar{b}\,\bar{y}_2 w_3$	$0 = \bar{c}$	O/D	O/D	O/D	O/D	O/D	O/D	D
10	$\underline{C}$	001	$0 = c\,\bar{y}_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	c	O/D	O/D	O/D	O/D	S	O/D	R

S = Set R = Reset
D = Detent Set O/D = Detent Reset

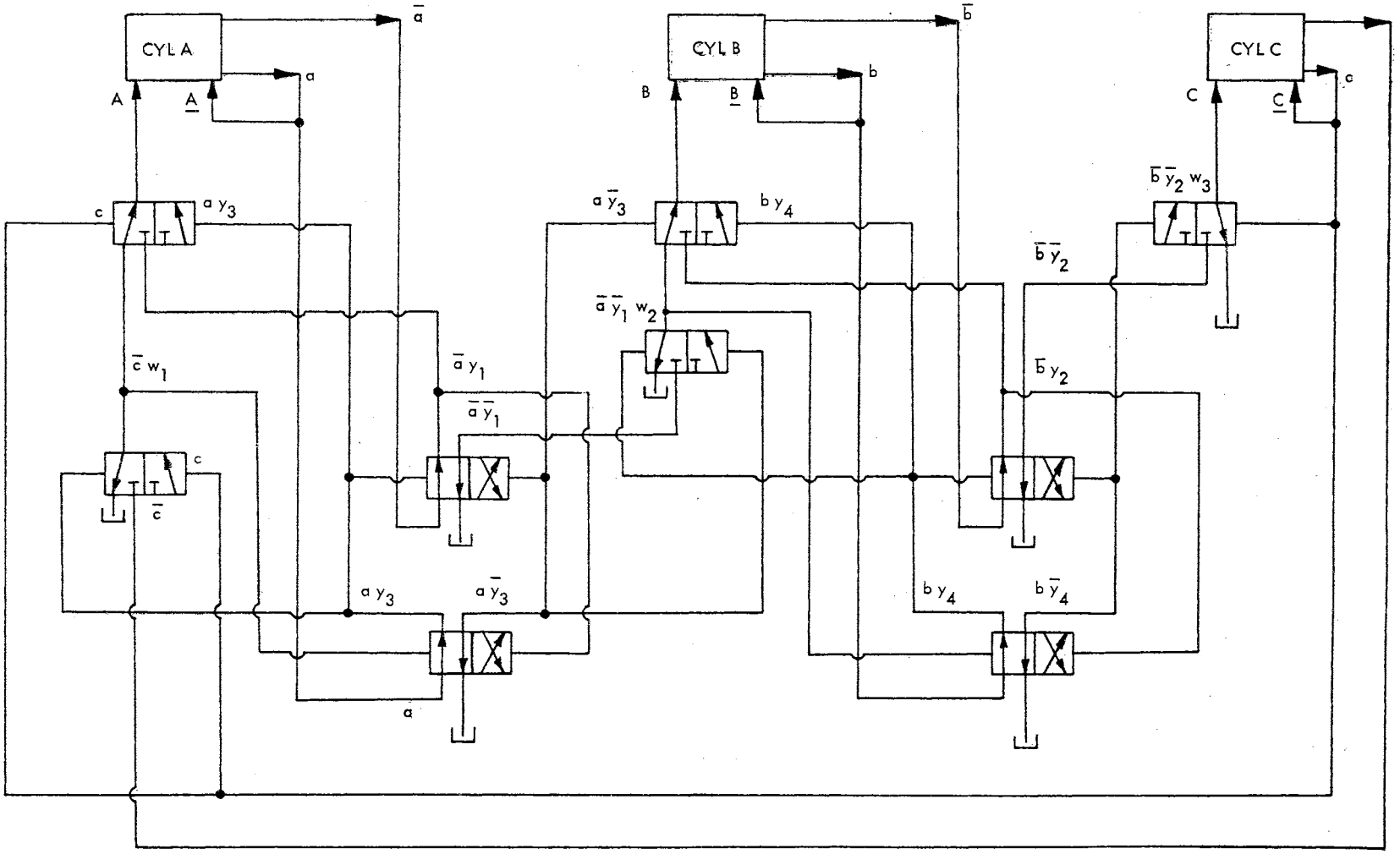


Figure 16. Circuit Schematic for 2:2:1 Counter

of signals is used to synthesize an alternate circuit realization as shown in Table XVI.

In this table, the input variables are replaced by their equivalent binary values and the combination $\bar{a}\ \bar{b}\ \bar{c}$ is replaced by the single variable d. When the coded value of the combined input signals is not 000, the value of d is zero. A "d" is placed in column I in every row in which the coded value 000 appears. In the remaining rows of column I, the variable is entered which makes the coded combination different from 000. Column II shows the association of the variables in column I with the events in column E. Variable d associates with A twice, then with B twice and with C once. Variable a associates with A twice and variable b associates with B twice while variable c associates with C only once. The Y valves required to distribute the signals are entered in column 3. This time, d is the only signal which must be distributed.

A check for contradictions indicates that no shut-off or W valves are required. Signal b activates the same event twice in the sequence, so Y_3 is entered in row 8 with the implication that Y_3 is also associated with row 6. Similarly, Y_4 is assigned to signal a in rows 4 and 2. Now, the signal and memory valve combination $dy_1\bar{y}_2$ appears twice, resulting in the assignment of Y_5 to rows 5 and 7. Rows 1 and 3 receive Y_6 because dy_1y_2 occurs in both of these rows.

TABLE XVI

SYNTHESIS TABLE 2:2:1 COUNTER (ALTERNATE)

No.	E	abc	I	II	III	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
1	A	000	d	A,A,B,B,C	$y_1 y_2$				$R\bar{y}_6$		
2	$\underline{A}$	100	a	$\underline{A},\underline{A}$							$S\bar{y}_4$
3	A	000	d	Y_6	$y_1 y_2$				Sy_6		
4	$\underline{A}$	100	a	Y_4			Ry_4			Ry_4	
5	B	000	d	Y_5	$y_1 \bar{y}_2$			$R\bar{y}_5$			
6	$\underline{B}$	010	b	$\underline{B}$, $\underline{B}$						$S\bar{y}_3$	
7	B	000	d		$y_1 \bar{y}_2$			Sy_5			
8	$\underline{B}$	010	b	Y_3		Ry_3					
9	C	000	d		$\bar{y}_1$						
10	$\underline{C}$	001	c	$\underline{C}$		S	S				R

Output Equations

Let $d = \bar{a}\bar{b}\bar{c}$

$A = d\ y_1 y_2$

$\underline{A} = a$

$B = d\ y_1 \bar{y}_2$

$\underline{B} = b$

$C = d\ \bar{y}_1$

$\underline{C} = c$

Secondaries

	Set	Reset
Y_1	c	by_3
Y_2	c	ay_4
Y_3	$dy_1\ \bar{y}_2\ y_5$	$dy_1\ \bar{y}_2\ \bar{y}_5$
Y_4	$dy_1\ y_2\ y_6$	$dy_1\ y_2\ \bar{y}_6$
Y_5	$b\ \bar{y}_3$	$a\ y_4$
Y_6	$a\ \bar{y}_4$	c

Six columns are provided at the right of the table - one for each Y valve. Selection of set and reset signals completes the table. Circuit equations are obtained directly from the table and written below. Table XVII verifies that the circuit will function properly.

Figure 17 is the schematic of the fluid logic circuit obtained from the equations of Table XVI. There are no shut-off valves in this circuit. However, two "and" valves are shown at the lower left. Their function is to provide the combination $d = \bar{a}\,\bar{b}\,\bar{c}$. This circuit contains a total of eight valves whereas the circuit in Figure 16 requires nine. Thus, a savings of one valve resulted from the alternate synthesis method. However, Figure 17 contains five delays while Figure 16 contains three. The question as to which of these circuit realizations is better would be the subject of a trade-off study. The significance here is that two circuits with somewhat different features have been synthesized by systematic methods. This means that the synthesis procedure is more versatile in that the designer is provided with options which may be used to best satisfy some set of conditions.

A 3:2:1 counter circuit is synthesized in Table XVIII and verified in Table XIX. The same procedure was used as in the first 2:2:1 counter. Note that second order memory is involved in the auxiliary part of the circuit as indicated in row 4 and column II. A schematic is not shown because it is only a matter of implementing the equations

TABLE XVII

OPERATIONS TABLE 2:2:1 COUNTER (ALTERNATE)

No.	E	abc	A	$\underline{A}$	B	$\underline{B}$	C	$\underline{C}$	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
1	A	000	$dy_1 y_2$	$0 = \bar{a}$	$0 = y_2$	$0 = \bar{b}$	$0 = y_1$	$0 = \bar{c}$	D	D	D	$R\bar{y}_6$	D	O/D
2	$\underline{A}$	100	$0 = \bar{d}$	a	$0 = y_2$	↑	↑	↑	D	D	D	O/D	D	$S\bar{y}_4$
3	A	000	$dy_1 y_2$	$0 = \bar{a}$	$0 = y_2$	↕	↕	↕	D	D	D	Sy_6	D	D
4	$\underline{A}$	100	$0 = \bar{y}_2$	a	$0 = \bar{d}$	↓	↕	↕	D	Ry_4	D	D	Ry_4	D
5	B	000	↑	$0 = \bar{a}$	$dy_1 \bar{y}_2$	$0 = \bar{b}$	↕	↕	D	O/D	$R\bar{y}_5$	D	O/D	D
6	$\underline{B}$	010	↕	↑	$0 = \bar{d}$	b	↓	↕	D	O/D	O/D	D	$S\bar{y}_3$	D
7	B	000	↕	↕	$dy_1 \bar{y}_2$	$0 = \bar{b}$	$0 = y_1$	↕	D	O/D	Sy_5	D	D	D
8	$\underline{B}$	010	↓	↕	$0 = \bar{y}_1$	b	$0 = \bar{d}$	↓	Ry_3	O/D	D	D	D	D
9	C	000	$0 = \bar{y}_2$	↓	$0 = \bar{y}_1$	$0 = \bar{b}$	$d\bar{y}_1$	$0 = \bar{c}$	O/D	O/D	D	D	D	D
10	$\underline{C}$	001	$0 = \bar{d}$	$0 = \bar{a}$	$0 = y_2$	$0 = \bar{b}$	$0 = y_1$	c	S	S	D	D	D	R

S = Set R = Reset
D = Detent Set O/D = Detent Reset

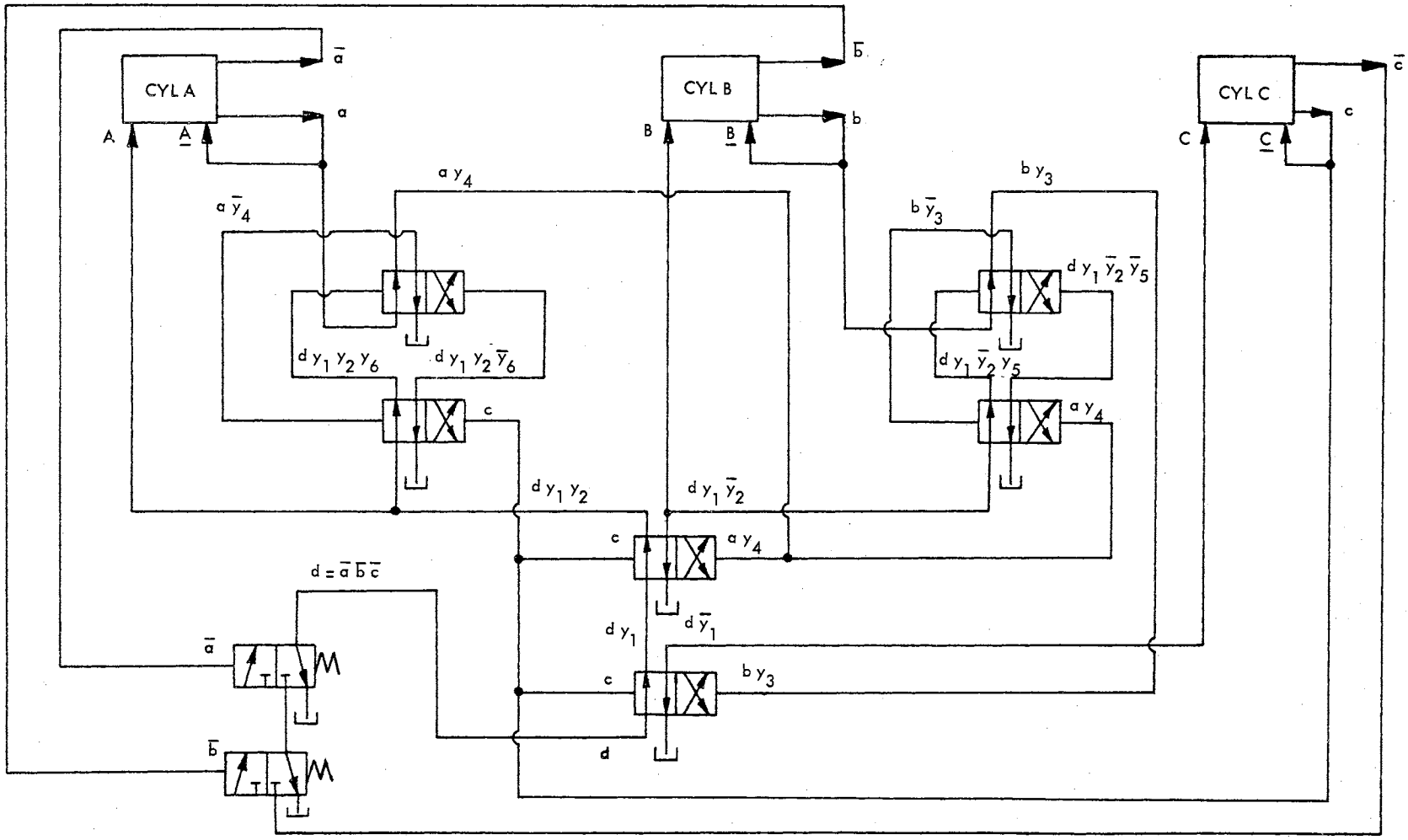


Figure 17. Circuit Schematic 2:2:1 Counter (Alternate)

TABLE XVIII

SYNTHESIS TABLE FOR 3:2:1 COUNTER

N	E	abc	I	II	III	IV	Y_1	Y_2	W_1	W_2	W_3	Y_3	Y_4	Y_5	Y_6
1	A	$\bar{a}\bar{b}\bar{c}$	$\bar{c}$	A		w_1						S	S		
2	$\underline{A}$	$a\bar{b}\bar{c}$	a	$\underline{A},\underline{A},\underline{A}$			Sy_3y_4		Ry_3y_4					Sy_3y_4	
3	A	$\bar{a}\bar{b}\bar{c}$	$\bar{a}$	A,A,B	y_1								Ry_5		
4	$\underline{A}$	$a\bar{b}\bar{c}$	a	Y_3Y_4										$Ry_3\bar{y}_4$	
5	A	$\bar{a}\bar{b}\bar{c}$	$\bar{a}$	Y_5	y_1							$R\bar{y}_5$			
6	$\underline{A}$	$a\bar{b}\bar{c}$	a				$R\bar{y}_3$			$S\bar{y}_3$					
7	B	$\bar{a}\bar{b}\bar{c}$	$\bar{a}$		$\bar{y}_1$	w_2									S
8	$\underline{B}$	$\bar{a}b\bar{c}$	b	$\underline{B},\underline{B}$				Sy_6		Ry_6					
9	B	$\bar{a}\bar{b}\bar{c}$	$\bar{b}$	B,C	y_2										R
10	$\underline{B}$	$\bar{a}b\bar{c}$	b	Y_6				$R\bar{y}_6$			$S\bar{y}_6$				
11	C	$\bar{a}\bar{b}\bar{c}$	$\bar{b}$		$\bar{y}_2$	w_3									
12	$\underline{C}$	$\bar{a}\bar{b}c$	c	$\underline{C}$					S		R				

Output EQ's

$A = \bar{c}w_1 + \bar{a}y_1$

$\underline{A} = a$

$B = \bar{a}\bar{y}_1 w_2 + \bar{b}y_2$

$\underline{B} = b$

$C = \bar{b}\bar{y}_2 w_3$

$\underline{C} = c$

Secondaries

	Set	Reset
Y_1	ay_3y_4	$a\bar{y}_3$
Y_2	by_6	$b\bar{y}_6$
Y_3	$\bar{c}w_1$	$\bar{a}y_1\bar{y}_5$
Y_4	$\bar{c}w_1$	$\bar{a}y_1y_5$
Y_5	ay_3y_4	$ay_3\bar{y}_4$
Y_6	$\bar{a}\bar{y}_1w_2$	$\bar{b}y_2$

	Set	Reset
W_1	c	ay_3y_4
W_2	$a\bar{y}_3$	by_6
W_3	$b\bar{y}_6$	c

TABLE XIX

OPERATIONS TABLE 3:2:1 COUNTER

No.	E	abc	A	$\underline{A}$	B	$\underline{B}$	C	$\underline{C}$	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	W_1	W_2	W_3
1	A	000	$\bar{c}\ w_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	$0 = \bar{c}$	O/D	O/D	S	S	O/D	O/D	D	O/D	O/D
2	$\underline{A}$	100	$0 = \bar{w}_1 a$	a	↑	↑	↑	↑	Sy_3y_4	O/D	D	D	Sy_3y_4	O/D	Ry_3y_4	O/D	O/D
3	A	000	$\bar{a}y_1$	$0 = \bar{a}$	↕	↕	↕	↕	D	O/D	D	Ry_5	D	O/D	O/D	O/D	O/D
4	$\underline{A}$	100	$0 = \bar{w}_1 a$	a	↓	↕	↕	↕	D	O/D	D	O/D	$Ry_3\bar{y}_4$	O/D	O/D	O/D	O/D
5	A	000	$\bar{a}y_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	↕	↕	↕	D	O/D	$R\bar{y}_5$	O/D	O/D	O/D	O/D	O/D	O/D
6	$\underline{A}$	100	$0 = \bar{w}_1\bar{y}_1$	a	$0 = a\bar{y}_2$	↓	↕	↕	$R\bar{y}_3$	O/D	O/D	O/D	O/D	O/D	O/D	$S\bar{y}_3$	O/D
7	B	000	↑	$0 = \bar{a}$	$\bar{a}\bar{y}_1 w_2$	$0 = \bar{b}$	↕	↕	O/D	O/D	O/D	O/D	O/D	S	O/D	D	O/D
8	$\underline{B}$	010	↕	↑	$0 = \bar{w}_2 b$	b	↓	↕	O/D	Sy_6	O/D	O/D	O/D	D	O/D	Ry_6	O/D
9	B	000	↕	↕	$b\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	↕	O/D	D	O/D	O/D	O/D	R	O/D	O/D	O/D
10	$\underline{B}$	010	↓	↕	$0 = \bar{w}_2\bar{y}_2$	b	$0 = b$	↓	O/D	$R\bar{y}_6$	O/D	O/D	O/D	O/D	O/D	O/D	$S\bar{y}_6$
11	C	000	$0 = \bar{w}_1\bar{y}_1$	↓	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$\bar{b}\bar{y}_2 w_3$	$0 = \bar{c}$	O/D	O/D	O/D	O/D	O/D	O/D	O/D	O/D	D
12	$\underline{C}$	001	$0 = c\bar{y}_1$	$0 = \bar{a}$	$0 = \bar{w}_2\bar{y}_2$	$0 = \bar{b}$	$0 = \bar{w}_3$	c	O/D	O/D	O/D	O/D	O/D	O/D	S	O/D	R

S = Set R = Reset
D = Detent set O/D = detent reset

at the bottom of Table XVII and the method for doing this has been adequately demonstrated by previous examples.

An alternate 3:2:1 counter circuit is synthesized in Table XX in the same manner as the alternate 2:2:1 counter. Table XXI confirms proper operation. Again, one less valve is required to implement the alternate circuit and no shut-off valves are called for. Second order memory is used two places in the auxiliary portion of the circuit.

Large Ordinary Sequences

Two more ordinary sequential circuits will be investigated now to permit further development of the synthesis procedure. The first is a fourteen-event sequence shown in Table XXII. The synthesis is carried out the same as in earlier examples. Because of the large number of memory valves involved in this problem, the synthesis table nearly fills the page. A more compact form appears as Table XXIII.

The first five columns of the two tables are the same except that the inputs are given binary values in Table XXIII. The sixth column from the left is labeled Y and the seventh is labeled W. Now, only the subscripted numbers appear in these columns. For example, 5 in the Y column means y_5 and $\bar{3}$ means $\bar{y}_3$. In the W column, the "w-not" variables are omitted. The 7, for example, in this column means w_7. Two double columns are placed at the right of the table. One pair for the W valves and the

TABLE XX

SYNTHESIS TABLE 3:2:1 COUNTER (ALTERNATE)

No.	E	abc	I	II	III	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8
1	A	000	d	A, A, A, B, B, C	$y_1 y_2$							$Sy_4 y_5$	$Sy_4 y_5$
2	$\underline{A}$	100	a	$\underline{A}$, $\underline{A}$, $\underline{A}$						$Ry_7 y_8$			
3	A	000	d	Y_4 Y_5	$y_1 y_2$								$Ry_4 \bar{y}_5$
4	$\underline{A}$	100	a	Y_7 Y_8					$Ry_7 \bar{y}_8$				
5	A	000	d		$y_1 y_2$							R $\bar{y}_4$	
6	$\underline{A}$	100	a				$R\bar{y}_7$				$S\bar{y}_7$		
7	B	000	d	Y_6	$y_1 \bar{y}_2$			Sy_6					
8	$\underline{B}$	010	b	$\underline{B}$, $\underline{B}$							Ry_3		
9	B	000	d		$y_1 \bar{y}_2$			$R\bar{y}_6$					
10	$\underline{B}$	010	b	Y_3		$R\bar{y}_3$							
11	C	000	d		$\bar{y}_1$								
12	$\underline{C}$	001	c	$\underline{C}$		S	S		S	S			

Output Equations

Let $d = \bar{a}\,\bar{b}\,\bar{c}$

$A = d\,y_1\,y_2$

$\underline{A} = a$

$B = d\,y_1\,\bar{y}_2$

$\underline{B} = b$

$C = d\,\bar{y}_1$

$\underline{C} = c$

Secondaries

	Set	Reset
Y_1	c	$b\bar{y}_3$
Y_2	c	$a\bar{y}_7$
Y_3	$dy_1\bar{y}_2y_6$	$dy_1\bar{y}_2\bar{y}_6$
Y_4	c	$ay_7\bar{y}_8$
Y_5	c	ay_7y_8
Y_6	$a\bar{y}_7$	by_3
Y_7	$dy_1y_2y_4y_5$	$dy_1y_2\bar{y}_4$
Y_8	$dy_1y_2y_4y_5$	$dy_1y_2y_4\bar{y}_5$

TABLE XXI

OPERATIONS TABLE 3:2:1 COUNTER (ALTERNATE)

No.	E	abc	A	$\underline{A}$	B	$\underline{B}$	C	$\underline{C}$	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8
1	A	000	dy_1y_2	$0 = \bar{a}$	$0 = y_2$	$0 = \bar{b}$	$0 = y_1$	$0 = \bar{c}$	D	D	O/D	D	D	O/D	Sy_4y_5	Sy_4y_5
2	$\underline{A}$	100	$0 = \bar{d}$	a	↑	↑	↑	↑	D	D	O/D	D	Ry_7y_8	O/D	D	D
3	A	000	dy_1y_2	$0 = \bar{a}$	↕	↕	↕	↕	D	D	O/D	D	O/D	O/D	D	$Ry_4\bar{y}_5$
4	$\underline{A}$	100	$0 = \bar{d}$	a	↓	↕	↕	↕	D	D	O/D	$Ry_7\bar{y}_8$	O/D	O/D	D	O/D
5	A	000	dy_1y_2	$0 = \bar{a}$	$0 = y_2$	↕	↕	↕	D	D	O/D	O/D	O/D	O/D	$R\bar{y}_4$	O/D
6	$\underline{A}$	100	$0 = \bar{y}_2$	a	$0 = \bar{d}$	↓	↕	↕	D	$R\bar{y}_7$	O/D	O/D	O/D	$S\bar{y}_7$	O/D	O/D
7	B	000	↑	$0 = \bar{a}$	$dy_1\bar{y}_2$	$0 = \bar{b}$	↕	↕	D	O/D	Sy_6	O/D	O/D	D	O/D	O/D
8	$\underline{B}$	010	↕	↑	$0 = \bar{d}$	b	↓	↕	D	O/D	D	O/D	O/D	Ry_3	O/D	O/D
9	B	000	↕	↕	$dy_1\bar{y}_2$	$0 = \bar{b}$	$0 = y_1$	↕	D	O/D	$R\bar{y}_6$	O/D	O/D	O/D	O/D	O/D
10	$\underline{B}$	010	↓	↕	$0 = \bar{y}_1$	b	$0 = \bar{d}$	↓	$R\bar{y}_3$	O/D	O/D	O/D	O/D	O/D	O/D	O/D
11	C	000	$0 = \bar{y}_2$	↓	$0 = \bar{y}_1$	$0 = \bar{b}$	$d\bar{y}_1$	$0 = \bar{c}$	O/D	O/D	O/D	O/D	O/D	O/D	O/D	O/D
12	$\underline{C}$	001	$0 = \bar{d}$	$0 = \bar{a}$	$0 = y_2$	$0 = \bar{b}$	$0 = \bar{d}$	c	S	S	O/D	S	S	O/D	O/D	O/D

S = Set R = Reset
D = Detent set O/D = Detent reset

other for the Y valves. The 6 in the "Set" column under "W-Valves" means that W_6 is set by signal b $\bar{y}_3 w_7$. Each expression can be checked against Table XXII, which contains identical information in a different form.

Circuit equations obtained from Table XXIII are listed in Table XXIV. Here another step is made toward more compact notation. The output equations in their complete form are listed at the top left with the equivalent expressions for these equations at the right. Output signal A is equal to $\bar{a}\ y_1$ in row 1 and is equal to $\bar{c}\ \bar{y}_6 w_8$ in row 12. Thus, the expression A = A(1) + A(12) means the same thing. The advantage of this notation is that it simplifies writing the secondary equations as shown at the bottom of the table. This also emphasizes that the secondaries are all set and reset by the output signals.

All of the previous examples have used the operations table to check the developed circuits for proper operations. However, after one has become experienced in using the synthesis table, this additional check is unnecessary because the synthesis table can be checked directly for contradictions. Therefore, the operations table will not be used in the remainder of this chapter. In actual practice, it would be advisable to verify all circuits in the operations table because it does provide an independent check and presents all of the information in a form that is possibly more convenient for row-by-row checking.

Table XXV contains an alternate synthesis of the

TABLE XXII

SYNTHESIS TABLE FOR FOURTEEN-EVENT AUTOMATIC CIRCUIT

No.	E	abcd	I	II	III	IV	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	W_1	W_2	W_3	W_4	W_5	W_6	W_7	W_8
1	A	$\bar{a}\bar{b}\bar{c}\bar{d}$	$\bar{a}$	A, C	$\bar{y}_1$			S					R	S						
2	B	$a\bar{b}\bar{c}\bar{d}$	a	B, $\underline{B}$	y_2	w_2			S											
3	$\underline{B}$	$ab\bar{c}\bar{d}$	b	$\underline{B}$, $\underline{A}$	y_3					S				R		S				
4	C	$a\bar{b}c\bar{d}$	$\bar{b}$	C, $\underline{A}$	y_4	w_4					S									
5	D	$a\bar{b}\bar{c}d$	c	D, $\underline{D}$	y_5											R	S			
6	$\underline{C}$	$a\bar{b}cd$	d			w_5						S							S	
7	B	$a\bar{b}\bar{c}d$	$\bar{c}$	B, A	y_6				R								R			
8	$\underline{A}$	$ab\bar{c}d$	b		$\bar{y}_3$	w_7	R											S		
9	C	$\bar{a}b\bar{c}d$	$\bar{a}$		$\bar{y}_1$	w_6					R								R	
10	$\underline{D}$	$\bar{a}bcd$	c		$\bar{y}_5$										S			R		
11	$\underline{C}$	$\bar{a}bc\bar{d}$	$\bar{d}$			w_3						R								S
12	A	$\bar{a}\bar{b}\bar{c}\bar{d}$	$\bar{c}$		$\bar{y}_6$	w_8		R							R					
13	$\underline{B}$	$ab\bar{c}\bar{d}$	a		$\bar{y}_2$					R			S							R
14	$\underline{A}$	$a\bar{b}\bar{c}\bar{d}$	$\bar{b}$		$\bar{y}_4$	w_1	S													

TABLE XXIII

MODIFIED SYNTHESIS TABLE FOR FOURTEEN-EVENT AUTOMATIC CIRCUIT

							W-Valves		Y-Valves	
No.	E	abcd	I	II	Y	W	Set	Reset	Set	Reset
1	A	0000	$\bar{a}$	A,C	1		2	1	2	
2	B	1000	a	B,$\underline{B}$	2	2			3	
3	$\underline{B}$	1100	b	$\underline{B}$,$\underline{A}$	3		4	2	4	
4	C	1000	$\bar{b}$	C,$\underline{A}$	4	4			5	
5	D	1010	c	D,$\underline{D}$	5		5	4		
6	$\underline{C}$	1011	d			5	7		6	
7	B	1001	$\bar{c}$	B,A	6			5		3
8	$\underline{A}$	1101	b		$\bar{3}$	7	6			1
9	C	0101	$\bar{a}$		$\bar{1}$	6		7		5
10	$\underline{D}$	0111	c		$\bar{5}$		3	6		
11	$\underline{C}$	0110	$\bar{d}$			3	8			6
12	A	0100	$\bar{c}$		$\bar{6}$	8		3		2
13	$\underline{B}$	1100	a		$\bar{2}$		1	8		4
14	$\underline{A}$	1000	$\bar{b}$		$\bar{4}$	1			1	

TABLE XXIV

EQUATIONS FOR FOURTEEN-EVENT AUTOMATIC CIRCUIT

Output Equations

$A = \bar{a}\ y_1 + \bar{c}\ \bar{y}_6 w_8$	$= A(1) + A(12)$
$\underline{A} = b\ \bar{y}_3\ w_7 + \bar{b}\ \bar{y}_4\ w_1$	$= \underline{A}(8) + \underline{A}(14)$
$B = a\ y_2\ w_2 + \bar{c}\ y_6$	$= B(2) + B(7)$
$\underline{B} = b\ y_3 + a\ \bar{y}_2$	$= \underline{B}(3) + \underline{B}(13)$
$C = \bar{b}\ y_4\ w_4 + \bar{a}\ \bar{y}_1\ w_6$	$= C(4) + C(9)$
$\underline{C} = d\ w_5 + \bar{d}\ w_3$	$= \underline{C}(6) + \underline{C}(11)$
$D = c\ y_5$	$= D(5)$
$\underline{D} = c\ \bar{y}_5$	$= \underline{D}(10)$

Secondary Equations

	Set	Reset
Y_1	$A(14)$	$\underline{A}(8)$
Y_2	$A(1)$	$A(12)$
Y_3	$B(2)$	$B(7)$
Y_4	$\underline{B}(3)$	$\underline{B}(13)$
Y_5	$C(4)$	$C(9)$
Y_6	$\underline{C}(6)$	$\underline{C}(11)$

	Set	Reset
W_1	$\underline{B}(13)$	$A(1)$
W_2	$A(1)$	$\underline{B}(3)$
W_3	$\underline{D}(10)$	$A(12)$
W_4	$\underline{B}(3)$	$D(5)$
W_5	$D(5)$	$B(7)$
W_6	$\underline{A}(8)$	$\underline{D}(10)$
W_7	$\underline{C}(6)$	$C(9)$
W_8	$\underline{C}(11)$	$\underline{B}(13)$

TABLE XXV

SYNTHESIS TABLE FOR FOURTEEN EVENT SEQUENCE (ALTERNATE)

No.	E	abcd	I	II	y_1	y_2
1	A	0000	1		S	S
2	B	1000	B,C,$\underline{A}$	$y_1 y_2$		
3	$\underline{B}$	1100	$\underline{B}$,$\underline{B}$			R
4	C	1000	1	$y_1 \bar{y}_2$		
5	D	1010	1			
6	$\underline{C}$	1011	1			
7	B	1001	1			
8	$\underline{A}$	1101	1			
9	C	0101	1			
10	$\underline{D}$	0111	1			
11	$\underline{C}$	0110	1			
12	A	0100	1		R	
13	$\underline{B}$	1100	2			R
14	$\underline{A}$	1000	1	$\bar{y}_1$		

OUTPUT EQUATIONS

$A = \bar{a}\bar{c}\bar{d}$

$\underline{A} = abd + \bar{a}\bar{b}\bar{c}\bar{d}\ \bar{y}_1$

$B = a\bar{b}\bar{c}\bar{d}\ y_1\ y_2 + \bar{b}\bar{c}d$

$\underline{B} = ab\bar{d}$

$C = \bar{a}\bar{b}\bar{c}\bar{d}\ y_1\ \bar{y}_2 + \bar{a}\bar{c}d$

$\underline{C} = \bar{a}c\bar{d} + \bar{b}cd$

$D = ac\bar{d}$

$\underline{D} = \bar{a}cd$

SECONDARY EQUATIONS

	Set	Reset
Y_1	$\bar{a}\bar{b}$	$\bar{a}bc\bar{d}$
Y_2	$\bar{a}\bar{b}$	$ab\bar{d}$

fourteen-event sequence which results in a different circuit realization. This time, the entire combination of input signals is considered. Column I contains information about the input signal combinations and the associated events. In row 1, the number 1 indicates that the coded combination 0000 occurs only once in the sequence. In row 2, the combination 1000 associates with three different events, B, C, and A. Row 3 shows that the combination 1100 associates only with B and occurs twice. A 2 is entered in row 13 to indicate that combination 1100 is used elsewhere. The remaining combinations are unique, associating only with the event in the same row. Thus, 1's are entered in these rows.

Since the combination 1000 represents a signal which goes to three places, two Y valves are required for distribution. These two valves are shown in column II. A check for output signal contradictions shows that W valves are not required. Set and reset signals are selected for the memory valves and are indicated in the two right-hand columns. The circuit equations are read from the table and after simplification, are shown at the right. Simplification is accomplished by eliminating redundant terms from the signal combinations. Only the variables required to maintain the uniqueness of the output signals are retained. For example, the first equation was reduced from $A = \bar{a}\,\bar{b}\,\bar{c}\,\bar{d} + \bar{a}\,b\,\bar{c}\,\bar{d}$ to $A = \bar{a}\,\bar{c}\,\bar{d}$.

By comparison of the circuit equations in Table XXV

with those of Table XXIV, it would appear that a simpler circuit has been provided by the alternate synthesis. However, twenty-four valves are required to implement the alternate circuit while only twenty are needed for the circuit represented by Table XXIV. (The numbers of valves required are obtained by counting the number of logic "ands" and "ors" represented by the equations and adding to these the number of W and Y valves listed under "secondaries".) Also, several more delays are present in the combined-signal circuit. In an actual system, the available hardware could possibly cause one of these circuits to be preferred.

Tables XXVI and XXVII represent the development of an eighteen-event ordinary sequence. Second order memory is required four times to distribute the signal as can be seen in the Y column. Commas are inserted between the numbers in the Y column to prevent misreading. In row 10, the input-signal and Y-valve combination that causes an output $\underline{B}$ is c $y_7\bar{y}_8$. Commas are also used to separate numbers in the Set and Reset columns, but a slightly different meaning is given. For example, in the Reset column of row 11, the expression "4,6" means that Y_4 and Y_6 are both reset in that row. Modified notation is used again to simplify writing the secondary equations.

A different circuit realization is obtained for the eighteen-event sequence by the synthesis method used in Table XXVIII. The same procedure was used as in the

TABLE XXVI

SYNTHESIS TABLE FOR EIGHTEEN-EVENT AUTOMATIC CIRCUIT

							W-Valves		Y-Valves	
No.	E	abc	I	II	Y	W	Reset	Set	Set	Reset
1	A	000	$\bar{c}$	A,B,B	1	$\bar{1}$			2,3	
2	B	100	a	B,$\underline{B}$,C	2,3		1	2	4,5	
3	$\underline{A}$	110	b	$\underline{A}$,C,$\underline{B}$	4,5	2			6	
4	C	010	$\bar{a}$	C,$\underline{C}$,$\underline{C}$	6		2	3	7,8	
5	A	011	c	A,$\underline{B}$,$\underline{A}$	7,8					3
6	$\underline{B}$	111	a		2,$\bar{3}$	3			9,10	
7	$\underline{C}$	101	$\bar{b}$	$\underline{C}$,$\underline{A}$,A	9,10		3	4		1,5
8	B	100	$\bar{c}$		$\bar{1}$	4				
9	C	110	b		4,$\bar{5}$					8
10	$\underline{B}$	111	c		7,$\bar{8}$					10
11	$\underline{A}$	101	$\bar{b}$		9,$\bar{10}$					4,6
12	$\underline{C}$	001	$\bar{a}$		$\bar{6}$					
13	B	000	$\bar{c}$		$\bar{1}$	4				
14	$\underline{B}$	010	b		$\bar{4}$		4	5		9
15	A	000	$\bar{b}$		$\bar{9}$	5				2
16	C	100	a		$\bar{2}$		5			7
17	$\underline{A}$	101	c		$\bar{7}$			1	1	
18	$\underline{\bar{C}}$	001	$\bar{a}$		$\bar{6}$					

TABLE XXVII

EQUATIONS FOR EIGHTEEN-EVENT AUTOMATIC CIRCUIT

Output Equations

$A = \bar{c}\ y_1\ w_1 + c\ y_7 y_8 + \bar{b}\ \bar{y}_9\ w_5 = A(1) + A(5) + A(15)$

$\underline{A} = b\ y_4\ y_5\ w_2 + \bar{b}\ y_9\ \bar{y}_{10} + c\ \bar{y}_7 = \underline{A}(3) + \underline{A}(11) + \underline{A}(17)$

$B = a\ y_2\ y_3 + \bar{c}\ \bar{y}_1\ w_4 = B(2) + B(8,13)$

$\underline{B} = a\ y_2\ \bar{y}_3\ w_3 + c\ y_7\ \bar{y}_8 + b\ \bar{y}_4 = \underline{B}(6) + \underline{B}(10) + \underline{B}(14)$

$C = \bar{a}\ y_6 + b\ y_4\ \bar{y}_5 + a\ \bar{y}_2 = C(4) + C(9) + C(16)$

$\underline{C} = b\ y_9\ y_{10} + \bar{a}\ \bar{y}_6 = \underline{C}(7) + \underline{C}(12, 18)$

Secondary Equations

	Set	Reset
Y_1	$\underline{A}(17)$	$\underline{C}(7)$
Y_2	A(1)	A(15)
Y_3	A(1)	A(5)
Y_4	B(2)	$\underline{A}(11)$
Y_5	B(2)	$\underline{C}(7)$
Y_6	$\underline{A}(3)$	$\underline{A}(11)$
Y_7	C(4)	C(16)
Y_8	C(4)	C(9)
Y_9	$\underline{B}(6)$	$\underline{B}(14)$
Y_{10}	$\underline{B}(6)$	$\underline{B}(10)$

	Set	Reset
W_1	$\underline{A}(17)$	B(2)
W_2	B(2)	C(4)
W_3	C(4)	$\underline{C}(7)$
W_4	$\underline{C}(7)$	$\underline{B}(14)$
W_5	$\underline{B}(14)$	C(16)

TABLE XXVIII

SYNTHESIS TABLE AND CIRCUIT EQUATIONS FOR EIGHTEEN-EVENT AUTOMATIC SEQUENCE (ALTERNATE CIRCUIT)

No.	E	abc	I	Y	S	R
1	A	000	A,B,A	1		
2	B	100	B,B,C	2		
3	$\underline{A}$	110	$\underline{A}$,C	3	4	
4	C	010	C,$\underline{B}$	4		
5	A	011	A		5	
6	$\underline{B}$	111	$\underline{B}$,$\underline{B}$			
7	$\underline{C}$	101	$\underline{C}$,$\underline{A}$,$\underline{A}$	5		3
8	B	100		2		
9	C	110		$\bar{3}$		1,5
10	$\underline{B}$	111				
11	$\underline{A}$	101		$\bar{5}$	2	
12	$\underline{C}$	001	$\underline{C}$,$\underline{C}$			
13	B	000		$\bar{1}$		4
14	$\underline{B}$	010		$\bar{4}$	1	2
15	A	000		1		
16	C	100		$\bar{2}$	3	
17	$\underline{A}$	101		$\bar{5}$	2	
18	$\underline{C}$	001				

Output Equations

$A = \bar{a}\,\bar{b}\,\bar{c}\,y_1 + \bar{a}\,b\,c$

$\underline{A} = a\,b\,\bar{c}\,y_3 + a\,\bar{b}\,c\,\bar{y}_5$

$B = a\,\bar{b}\,\bar{c}\,y_2 + \bar{a}\,\bar{b}\,\bar{c}\,\bar{y}_1$

$\underline{B} = a\,b\,c + \bar{a}\,b\,\bar{c}\,\bar{y}_4$

$C = \bar{a}\,b\,\bar{c}\,y_4 + a\,b\,\bar{c}\,\bar{y}_3 + a\,\bar{b}\,\bar{c}\,\bar{y}_2$

$\underline{C} = a\,\bar{b}\,c\,y_5 + \bar{a}\,\bar{b}\,c$

Secondary Equations

	Set	Reset
Y_1	$\underline{B}$(14)	C(9)
Y_2	$\underline{A}$(11,17)	$\underline{B}$(14)
Y_3	C(16)	$\underline{C}$(7)
Y_4	$\underline{A}$(3)	B(13)
Y_5	A(5)	C(9)

alternate fourteen-event sequence in Table XXV. This time, the output equations contained no redundant terms and could not be simplified. It is interesting to note that the alternate circuit can be implemented with twenty-four valves, whereas twenty-five valves are needed to implement the equations of Table XXVII. However, the alternate circuit contains eighteen delays while the other circuit has only five.

In the four example sequences which have been synthesized two ways, there has been little difference in the total amount of circuit components needed. The two counter circuits and the eighteen-event sequence each required one less component when synthesized by the alternate method. The fourteen-event sequence used four more in the alternate configuration. This variation is probably due to the fourteen-event sequence having more cylinders and fewer repetitions in comparison to the other sequences. In every case, the faster circuit operation was provided by the procedure which used only one input signal rather than input signal combinations for initiating the events.

Complex Sequences

Two types of sequential circuits have been synthesized. These are the ordinary sequential and counter circuits. Combinations of these two are called complex sequential circuits. It will now be shown that complex sequences can also be treated by the procedures which have

been developed.

A twenty-four-event sequence which includes a 3:2:1 counter dispersed in the sequence is synthesized in Table XXIX. The table has been modified slightly and additional notation included. A new column has been added between the Y and W columns. This is a check column. Whenever an input signal and Y valve combination occurs only once, an "X" is entered in that row in the check column and that row need not be considered for auxiliary memory valves. For example, the combination $\bar{a}\ y_1 \bar{y}_2$ appears only in row 4. Therefore, an "X" is placed in the check column. The combination $b\ y_5 \bar{y}_6$ appears in rows 8, 10, and 12 and, consequently, the check column is left blank. Note that all of the unchecked rows, with the exceptions of 13 and 22, contain auxiliary Y valves as shown in column II. The signal combination appearing in rows 13 and 22 is not used for switching any memory valves and does not need an auxiliary valve.

The new notation is contained in the S and R columns at the right of the table. For example, "4,5($\overline{13}$)" is entered in row 12 and the S column under "W-Valves". This means that W_4 and W_5 are set by the combination $b\ y_5 \bar{y}_6 \bar{y}_{13}$. The first three variables, $b\ y_5 \bar{y}_6$, represent the $\underline{B}$ signal in row 12. The numbers in parentheses refer to the auxiliary Y valves required to direct the output signals to their desired switching locations.

The circuit equations are obtained directly from the

TABLE XXIX

SYNTHESIS TABLE FOR TWENTY-FOUR-EVENT SEQUENCE
INCLUDING 3:2:1 COUNTER

								W-Valves		Y-Valves	
No.	E	abc	1	II	Y		W	R	S	S	R
1	A	000	$\bar{a}$	A,C,A,B 17	1,2			1(17)		3,4(17)	
2	B	100	a	B,A,A,B	3,4	X			2	5,6	
3	A	110	b	A,B,B,B,C	5,6	X					2
4	C	010	$\bar{a}$		1,$\bar{2}$	X	2			7,8	
5	B	011	c	B,A,C	7,8	X		2		9,10	
6	C	001	$\bar{b}$	C,B,B,C,C	9,10	X			3	11,12	
7	B	000	$\bar{c}$	B,A,A	11,12	X	3			13,14	6
8	B	010	b	13,14	5,$\bar{6}$			3(13,14)		16(13,14)	10(13,14)
9	B	000	$\bar{b}$	16	9,$\overline{10}$						14(16)
10	B	010	b	13,$\overline{14}$	5,$\bar{6}$						16(13,$\overline{14}$)
11	B	000	$\bar{b}$	16	9,$\overline{10}$						13($\overline{16}$)
12	B	010	b	$\overline{13}$	5,$\bar{6}$				4,5($\overline{13}$)		8,9($\overline{13}$)
13	C	000	$\bar{b}$		$\bar{9}$		5				
14	A	001	c		7,$\bar{8}$	X	4			15	4
15	A	101	a	15	3,$\bar{4}$			4(15)		2(15	17(15)
16	A	001	$\bar{a}$	$\overline{17}$	1,2						15($\overline{17}$)
17	A	101	a	$\overline{15}$	3,$\bar{4}$						1($\overline{15}$)
18	B	001	$\bar{a}$		$\bar{1}$	X					5
19	C	011	b		$\bar{5}$	X					12
20	A	010	$\bar{c}$		11,$\overline{12}$	X					3
21	B	110	a		$\bar{3}$	X					7
22	C	110	$\bar{b}$		$\bar{9}$		5				
23	C	101	c		$\bar{7}$	X		5	1		11
24	A	100	$\bar{c}$		$\overline{11}$	X	1			1,17	

synthesis table and are listed in Table XXX. Note in the secondary equations W_4 and W_5 are set by $\underline{B}(12)\bar{y}_{13}$. This is the combination discussed in the preceding paragraph.

An attempt will now be made to indicate the effort that would be involved in synthesizing a circuit for the preceding problem using the flow table approach. Table XXXI is a primitive flow table containing the twenty-four-event sequence specification. Table XXXI is also the reduced flow table because there are no redundant rows. Table XXXII shows the flow table merged. This merger is not necessarily optimum but is merely meant to show the number of rows that remain after merging. In this case there are twelve. As indicated at the left, four active secondary valves are required to provide unique coded values for each row.

The four secondaries plus the three input signals make this a seven-variable problem. This means that seven-variable Karnaugh maps would be required for obtaining the circuit equations. Ten of these maps would have to be filled out and read to provide the four "set" equations for the secondaries and the six output equations. Each map would contain spaces for 2^7 or 128 possible entries. The "reset" equations for the secondaries would then be developed by solving the "set" equations for their complements. An operations table verification of the circuit would be mandatory because of the high probability of making mistakes during the procedure. By comparison,

TABLE XXX

CIRCUIT EQUATIONS FOR TWENTY-FOUR-EVENT SEQUENCE

Output Equations

A	A(1,16) + A(14) + A(20)	$= \bar{a}y_1\ y_2 + cy_7\ \bar{y}_8\ w_4 + \bar{c}\ y_{11}\ \bar{y}_{12}$
$\underline{A}$	A(3) + $\underline{A}$(15,17) + $\underline{A}$(24)	$= by_5\ y_6 + a\ y_3\ \bar{y}_4 + \bar{c}\ \bar{y}_{11}\ w_1$
B	B(2) + B(7) + B(9,11) + B(18)	$= ay_3\ y_4 + \bar{c}y_{11}\ y_{12}\ w_3 + \bar{b}y_9\ \bar{y}_{10} + \bar{a}\bar{y}_1$
$\underline{B}$	$\underline{B}$(5) + $\underline{B}$(8,10,12) + $\underline{B}$(21)	$= cy_7\ y_8 + by_6\ \bar{y}_6 + a\bar{y}_3$
C	C(4) + C(13,22)	$= \bar{a}y_1\ \bar{y}_2\ w_2 + \bar{b}\bar{y}_9\ w_5$
$\underline{C}$	$\underline{C}$(6) + $\underline{C}$(19) + $\underline{C}$(23)	$= \bar{b}y_9\ y_{10} + b\bar{y}_6 + c\bar{y}_7$

Secondary Equations

	Set	Reset
Y_1	$\underline{A}$(24)	$\underline{A}(17)\bar{y}_{15}$
Y_2	$\underline{A}(15)y_{15}$	$\underline{A}$(13)
Y_3	$A(1)y_{17}$	A(20)
Y_4	$A(1)y_{17}$	A(14)
Y_5	B(2)	B(18)
Y_6	B(2)	B(7)
Y_7	C(4)	$\underline{B}$(21)
Y_8	C(4)	$\underline{B}(12)\bar{y}_{13}$
Y_9	$\underline{B}$(5)	$\underline{B}(12)\bar{y}_{13}$
Y_{10}	$\underline{B}$(5)	$\underline{B}(8)y_{13}\ y_{14}$
Y_{11}	$\underline{C}$(6)	$\underline{C}$(23)
Y_{12}	$\underline{C}$(6)	$\underline{C}$(19)
Y_{13}	B(7)	$B(11)\bar{y}_{16}$
Y_{14}	B(7)	$B(9)y_{16}$
Y_{15}	A(14)	$A(16)\bar{y}_{17}$
Y_{16}	$\underline{B}(8)y_{13}\ y_{14}$	$\underline{B}(10)y_{13}\ \bar{y}_{14}$
Y_{17}	$\underline{A}$(24)	$\underline{A}(15)y_{15}$
W_1	$\underline{C}$(23)	$A(1)y_{17}$
W_2	B(2)	$\underline{B}$(5)
W_3	$\underline{C}$(6)	$\underline{B}(8)y_{13}\ y_{14}$
W_4	$\underline{B}(12)\bar{y}_{13}$	$\underline{A}(15)y_{15}$
W_5	$\underline{B}(12)\bar{y}_{13}$	$\underline{C}$(23)

TABLE XXXI

PRIMITIVE FLOW TABLE FOR TWENTY-FOUR-EVENT SEQUENCE

No.	E	abc 000	001	011	010	110	111	101	100	Outputs AABBCC
1	A	(1)							2	100-0-
2	B					3			(2)	-0100-
3	A				4	(3)				01-00-
4	C			5	(4)					0--010
5	B		6	(5)						0-01-0
6	C	7	(6)							0-0-01
7	B	(7)			8					0-100-
8	B	9			(8)					0-010-
9	B	(9)			10					0-100-
10	B	11			(10)					0-010-
11	B	(11)			12					0-100-
12	B	13			(12)					0-010-
13	C	(13)	14							0-0-10
14	A		(14)					15		100--0
15	A		16					(15)		010--0
16	A		(16)					17		100--0
17	A		18					(17)		010--0
18	B		(18)	19						0-10-0
19	C			(19)	20					0--001
20	A				(20)	21				10-00-
21	B					(21)			22	-0010-
22	C							23	(22)	-00-10
23	C							(23)	24	-00-01
24	A	1							(24)	010-01

TABLE XXXII

MERGED FLOW TABLE FOR TWENTY-FOUR-EVENT SEQUENCE

$Y_1 Y_2 Y_3 Y_4$	abc 000	001	011	010	110	111	101	100
0 0 0 0	(1)	6	(5)	(4)	(3)			(2)
0 0 0 1	7	(6)		8				
0 0 1 1	9			(8)				
0 0 1 0	(9)			10				
0 1 1 0	11			(10)				
0 1 1 1	(11)			12				
0 1 0 1	(13)	(14)		(12)			15	
0 1 0 0		16					(15)	
1 1 0 0		(16)					17	
1 1 0 1		(18)	(19)	(20)	(21)		(17)	22
1 1 1 1							23	(22)
1 1 1 0	1						(23)	(24)
1 0 1 0								
1 0 1 1								
1 0 0 1								
1 0 0 0								

the synthesis table approach required only one sheet of paper for developing a circuit. Thus, the effort is many times less.

To truly emphasize the power of this new method, a larger complex sequence will now be discussed. The synthesis of a forty-two-event sequence including a counter circuit is contained in Table XXXIII. Eight cylinders are involved. The Y column indicates third order memory. Otherwise, the discussion of the previous problem applies here. Table XXXIV lists the circuit equations.

It can be shown that this problem would involve thirteen variables if a synthesis attempt were made using the flow table method. A total of twenty-one 13-variable maps would be required to obtain the circuit equations. The writer is unaware of anyone who can interpret such large maps without the aid of a computer. It is also doubtful that many designers have the skill and experience to design such a complex circuit by intuitive methods.

The forty-two-event sequence was synthesized on two 8½ x 11 sheets using the synthesis table procedure. It should be obvious that much larger problems can be readily solved by this approach.

Procedure Outline

In order to provide a check list or guide for synthesizing circuits, the basic procedure which has been developed in this chapter is summarized in a step-by-step

TABLE XXXIII

SYNTHESIS TABLE FOR 42 EVENT SEQUENCE
(INCLUDES 3:2:2:1:1 COUNTER)

								W-Valves		Y-Valves	
N	E	abcdeghk	l	ll	Y		W	R	S	S	R
1	A	00000000	$\bar{k}$	A,H	1	X	2			2	
2	B	10000000	a	B,A,A,A	2	X	1			3,4	
3	C	11000000	b	C,K,B,B	3,4	X		1		5	
4	B	11100000	c	B,D	5	X			4	6,7,8	
5	D	10100000	$\bar{b}$	D,H,B,C	6,7,8	X		2	6	9	
6	A	10110000	d	A,D	9	X	6			10,11	
7	E	00110000	$\bar{a}$	E,A,A,G	10,11	X	4			12	
8	C	00111000	e	C,B	12	X			5	13	
9	B	00011000	$\bar{c}$	B,H	13	X	5	3			4
10	K	01011000	b		$3,\overline{4}$	X		4	8,9	14	
11	E	01011001	k	E,C	14	X	9			15	
12	G	01010001	$\bar{e}$	G,K	15	X	8	5	7	16	
13	B	01010101	g	B,G,G	16	X					8
14	H	00010101	$\bar{b}$		$6,7,\overline{8}$	X		6		17	
15	A	00010111	h	A,H	17	X	7		11	22,23	2
16	A	10010111	a	22,23	$\overline{2}$			7(22,23)		24(22,23)	11(22,23)
17	A	00010111	$\bar{a}$	24	$10,\overline{11}$						23(24)
18	A	10010111	a	$22,\overline{23}$	$\overline{2}$						$24(22,\overline{23})$
19	A	00010111	$\bar{a}$	$\overline{24}$	$10,\overline{11}$				$11(\overline{24})$		$22(\overline{24})$
20	A	10010111	a	$\overline{22}$	$\overline{2}$			$8(\overline{22})$	$10(\overline{22})$		$10(\overline{22})$
21	G	00010111	$\bar{a}$		$\overline{10}$	X	11	9		18,19	

TABLE XXXIII (Continued)

								W-Valves		Y-Valves	
N	E	abcdeghk	l	ll	Y		W	R	S	S	R
22	E	00010011	$\bar{g}$	E,G,D	18,19	X					12
23	B	00011011	e		$\overline{12}$	X	10			25	3
24	B	01011011	b	25	$\bar{3}$			10(25)			7(25)
25	B	00011011	$\bar{b}$		6,$\bar{7}$	X			13,16		25
26	B	01011011	b	$\overline{25}$	$\bar{3}$				12($\overline{25}$)		6($\overline{25}$)
27	C	00011011	$\bar{b}$		$\bar{6}$	X	16				5
28	D	00111011	c		$\bar{5}$	X	13	11		20	
29	G	00101011	$\bar{d}$	G,E	20	X	12			26	16
30	G	00101111	g	26	$\overline{16}$			12(26)			19(26)
31	G	00101011	$\bar{g}$		18,$\overline{19}$	X			14		26
32	G	00101111	g	$\overline{26}$	$\overline{16}$			13($\overline{26}$)			18($\overline{26}$)
33	D	00101011	$\bar{g}$		$\overline{18}$	X	14				9
34	D	00111011	d		$\bar{9}$	X		14	15		20
35	E	00101011	$\bar{d}$		$\overline{20}$	X					15
36	K	00100011	$\bar{e}$		$\overline{15}$	X	15				1
37	H	00100010	$\bar{k}$		$\bar{1}$	X		15		21	
38	K	00100000	$\bar{h}$	K,K	21	X		16	17		14
39	C	00100001	k		$\overline{14}$	X					13
40	H	00000001	$\bar{c}$		$\overline{13}$	X	17				17
41	H	00000011	h		$\overline{17}$	X		17	1,2,3		21
42	K	00000001	$\bar{h}$		$\overline{21}$	X	3			1	

TABLE XXXIV

CIRCUIT EQUATIONS FOR FORTY-TWO EVENT SEQUENCE

Output Equations

$A = A(1) + A(15) + A(17,19) = \bar{k}\, y_1\, w_2 + h\, y_{17}\, w_7 + \bar{a}\, y_{10}\, \bar{y}_{11}$

$\underline{A} = \underline{A}(6) + \underline{A}(16,18,20) = d\, y_9\, w_6 + a\, \bar{y}_2$

$B = B(2) + B(9) + B(23) + B(25) = a\, y_2\, w_1 + \bar{c}\, y_{13}\, w_5 + e\bar{y}_{12}\, w_{10} + \bar{b}y_6\bar{y}_7$

$\underline{B} = \underline{B}(4) + \underline{B}(13) + \underline{B}(24,26) = c\, y_5 + g\, y_{16} + b\, \bar{y}_3$

$C = C(3) + C(27) = b\, y_3\, y_4 + \bar{b}\, \bar{y}_6\, w_{16}$

$\underline{C} = \underline{C}(8) + \underline{C}(39) = e\, y_{12} + k\, \bar{y}_{14}$

$D = D(5) + D(33) = \bar{b}\, y_6\, y_7\, y_8 + \bar{g}\, \bar{y}_{18}\, w_{14}$

$\underline{D} = \underline{D}(28) + \underline{D}(34) = c\, \bar{y}_5\, w_{13} + d\, \bar{y}_9$

$E = E(7) + E(22) = \bar{a}\, y_{10}\, y_{11}\, w_4 + \bar{g}\, y_{18}\, y_{19}$

$\underline{E} = \underline{E}(11) + \underline{E}(35) = k\, y_{14}\, w_9 + \bar{d}\, \bar{y}_{20}$

$G = G(12) + G(29) + G(31) = \bar{e}\, y_{15}\, w_8 + \bar{d}\, y_{20}\, w_{12} + \bar{g}\, y_{18}\, \bar{y}_{19}$

$\underline{G} = \underline{G}(21) + \underline{G}(30,32) = \bar{a}\, \bar{y}_{10}\, w_{11} + g\, \bar{y}_{16}$

$H = H(14) + H(40) = \bar{b}\, y_6\, y_7\, \bar{y}_8 + \bar{c}\, \bar{y}_{13}\, w_{17}$

$\underline{H} = \underline{H}(37) + \underline{H}(41) = \bar{k}\, \bar{y}_1 + h\, \bar{y}_{17}$

$K = K(10) + K(38) = b\, y_3\, \bar{y}_4 + \bar{h}\, y_{21}$

$\underline{K} = \underline{K}(36) + \underline{K}(42) = \bar{e}\, \bar{y}_{15}\, w_{15} + \bar{h}\, \bar{y}_{21}\, w_3$

TABLE XXXIV (Continued)

Y	Set	Reset
1	K(42)	K(36)
2	A(1)	A(15)
3	B(2)	B(23)
4	B(2)	B(9)
5	C(3)	C(27)
6	B(4)	B(26)$\overline{25}$
7	B(4)	B(24)25
8	B(4)	B(13)
9	D(5)	D(33)
10	A(6)	A(20)$\overline{22}$
11	A(6)	A(16)22,23
12	E(7)	E(22)
13	C(8)	C(39)
14	K(10)	K(38)
15	E(11)	E(35)
16	G(12)	G(29)
17	H(14)	H(40)
18	G(21)	G(32)$\overline{26}$
19	G(21)	G(30)26
20	D(28)	D(34)
21	H(37)	H(41)
22	A(15)	A(19)$\overline{24}$
23	A(15)	A(17)24
24	A(16) 22,23	A(18)22,$\overline{23}$
25	B(23)	B(25)
26	G(29)	G(31)

W	Set	Reset
1	H(41)	C(3)
2	H(41)	D(5)
3	H(41)	B(9)
4	B(4)	K(10)
5	C(8)	G(12)
6	D(5)	H(14)
7	G(12)	A(16)22,23
8	K(10)	A(20)$\overline{22}$
9	K(10)	G(21)
10	A(20)$\overline{22}$	B(24)25
11	A(19)$\overline{24}$	D(28)

TABLE XXXIV (Continued)

W	Set	Reset
12	B(26)$\overline{25}$	G(30)26
13	B(25)	G(32)$\overline{26}$
14	G(31)	D(34)
15	D(34)	H(37)
16	B(25)	K(38)
17	K(38)	H(41)

outline as follows:

1. Write out the sequence specification in shorthand notation.
2. Place the event numbers and operational symbols in the two left columns of a synthesis table such as Table XXIX.
3. Examine the specification to determine the initial conditions of all the actuators in the system. It is assumed here that each actuator will be in one of its extreme positions at the beginning of the sequence. This will establish the states of the input signals before the first event starts to occur.
4. Using logic notation, enter the initial condition input signal combination in row 1 in the column next to the symbol representing event number 1.
5. After event number 1 is complete, a new stabilized combination of input signals will result.
6. Enter this new combination in row 2 in the column beside event number 2.
7. In a like manner, list the appropriate signal combinations successively in the remaining rows.
8. Compare the signal combination in row 2

with the combination in row 1. One of the signals will have changed. Enter this signal in row 2 in the fourth column of the table.

9. Now, compare the combination in row 3 with that in row 2 to get the changed signal for row 3.
10. Similarly, obtain the changed signal for each succeeding row through the last row. Now, compare the last row with the first row and place the changed signal in row 1.
11. Column 5 is for showing the events associated with each signal. Starting with the changed signal in row 1, list the event that occurs in row 1. Check each of the remaining rows for a repetition of that signal. Each time the signal appears, list the event of that row back in row 1.
12. After all of the rows have been checked for the first signal, move down to row 2 and repeat the process for the second signal, placing all the events associated with the second signal in row 2.
13. Likewise, check each of the remaining signals and list the associated events in column 5 in the row in which the signal first appears.

14. The number of distinct events in a row of column 5 determines how many places the signal in that row must go. If a signal goes n places, it will take n - 1 Y memory valves to distribute the signal. If a particular signal appears only in one row or repeatedly associates with only one event, no Y valve is required.
15. Y valves are assigned in the Y column or column 6 in accordance with the techniques shown in Figures 6 and 7 of Chapter IV. The first event calls for all the Y valves to be set. The next different event calls for the highest numbered Y valve in the combination to be reset, and so on. Finally, the last distinct event associated with the signal requires the lowest numbered Y valve to be reset.
16. After the Y valve assignment is complete, check the signal and valve combination in each row for uniqueness. If the changed input signal and Y valve combination appears only once in the entire sequence, place an "X" in the row containing the combination.
17. Determine the W-valve requirements by checking each event output signal (changed input signal and Y valve combination) against the

most recent negation of that event. If the output signals for the event and its negation are both on, a shut-off or W valve must be assigned to the negation event output signal. This is done by placing a subscripted w in the row of the negation event. The first assignment is w_1, the second w_2, and so forth, until all contradictions have been accounted for. Note that if a W valve, say w_1, is assigned to a specific signal and Y valve combination, w_1 must be entered in every row in which the combination appears.

18. Assign auxiliary Y valves to the fourth column. If a changed input signal and Y valve combination associates with the same event k times, k - 1 auxiliary valves are assigned to the combination. If it later develops that a valve is not needed when the set and reset assignments are made, it will be eliminated.

19. Select mandatory W reset signals. If the output signals in adjacent rows are contradictory, the reset must occur in the latter of these rows. For example, see rows 7 and 8 of Table XXIX. Should the adjacency involve the last and first rows, the reset

must occur in row 1. Again see Table XXIX.

If there is an intervening row between the contradictory signals, the W reset must occur in that row. See rows 4, 5, and 6. (The reset is in row 5.) Otherwise, an unnecessary delay will occur.

20. Select remaining W reset signals. If more than one row intervenes between contradictory signals, reset the W valve in the row immediately preceding the row in which the W valve must be off.

21. Select W set signals. If possible, choose the set signal in the row immediately preceding the row in which the W valve must be on. If this causes a contradiction with the reset signal, try the signal in the next earlier row and so on until a satisfactory set signal is reached.

22. Select mandatory set and reset signals for the Y valves. Referring to Table XXIX, it is obvious that Y_1 must be reset in row 17, Y_{11} reset in row 23, Y_9 reset in row 12, and Y_{10} reset in row 8.

23. Select remaining Y reset signals. Reset each valve in the row immediately preceding the row in which the valve must be off. However, if the immediately preceding row

contains a repeated input signal and Y valve combination, try the next earlier row to see if the use of auxiliary Y valves can be avoided. In most instances, auxiliary valves are necessary where repeated combinations occur. Do not reset a Y value if its associated input signal is on.

24. Select remaining Y set signals. Again choose the set signal in the row immediately preceding the row in which the Y valve must be set and check for conflict with the corresponding reset signal. If necessary, move up to the next row until a suitable set signal is found.

25. Obtain the circuit equations. Each output consists of the changed input signal and the Y and W valves in columns 6 and 8. The set and reset signals consist of the output signals and auxiliary Y valves in column 5.

The alternate procedure is very similar to the one just outlined. In this case, however, the input signal combination is used instead of the single signal, with the result that W valves are not required. The same procedures apply in selecting distribution Y valves, auxiliary Y valves and set and reset signals.

CHAPTER VI

TREATMENT OF SPECIAL SITUATIONS

Hazards

In the normal design of sequential circuits, one must be alert to the problem of hazards which can appear as the result of imperfect switching of physical elements. However, hazards are automatically excluded in circuits synthesized by the procedure developed in the last chapter. The reasons are as follow:

1. The Y valves are passive steering gates, having no output of their own. When a Y valve is switched, nothing happens until the changed signal later comes through the valve.
2. The Y valves (and W valves) are all set and reset by signals having only one conjunctive term. No false signals can be generated during input transitions to inadvertently switch a memory valve.
3. The 3-position, spring centered power valve locks the actuator when the output signal goes off. Before the actuator can reverse,

an opposing output signal must be generated. False output signals cannot occur because a new output signal comes on only at the completion of an event.

The example in the last chapter assumed that the output signal had to be on only during the time that an event was occurring and could go off or stay on when the event was complete providing, of course, that the negation of the completed event was not the next required event. However, it is feasible that some systems would require maximum pressure to remain available to the actuator while one or more subsequent events take place. In this case, two or more different output signals might be required to maintain the power valve in the shifted position during table row transitions. As one signal went off and the next one came on, the output could temporarily go off, letting the power valve momentarily return to the center position.

There is some question that the condition cited above would constitute a hazard. However, if the temporary re-centering of the power valve were objectional, a two-position detent valve could replace the

power valve. Thus, the detent would keep the valve shifted during a momentary loss of output.

Hazards could result if a two-position, spring-return pilot operated valve were used for the power valve. In this case, momentary loss of the output signal could result in the actuator reversing directions, especially in a very fast system. If it is absolutely necessary to use such a power valve and the valve has to remain shifted during a transition of output signals, redundant logic hardware must be used to assure a continuous signal.

If a particular event occurs more than once during a sequence and as the result of different output signals, each of the individual output signals involved will become a disjunctive term of the combined output equation. Each of the terms will be separated by a logic "or" which is symbolically written as "+". For example, a typical output expression might appear as $B = a\ y_1 + \bar{a}\ y_3$.

This equation by itself has the appearance of a hazard because of the variable a and its complement. In reality, a hazard would be involved only if the output signal B had to remain on during the transition from one term to the other in the equation. As previously mentioned, this situation does not exist when either the spring centered power valve or the detent power valve is used. Only in the case of the two-way, spring returned power valve would this happen.

Since the designer is aware of the type of valve being used, he knows when he is writing the output equations from the table if a hazard is involved. If a hazard does exist, he can make an identifying note beside the equation. If there is no note, the equation will be understood to be hazard free.

Simultaneous Events

In the examples used in the synthesis procedure development, only one event was allowed to occur at a time. Generally, this is a necessary restriction. However, several events may be allowed to occur simultaneously, providing it is unimportant in what order the events are completed. In this case, the input signals from the simultaneous events can be combined to produce the signal for initiating the next required event. Other exceptions may be possible, but would have to be considered in light of the specific situation involved.

Sequence as Sub-Function of Larger Sequence

A particular sequence as synthesized by the procedure developed in Chapter V could become a sub-function of a larger program. For example, a sequence could cycle a specified number of times and then another specified sequence would cycle some number of times and so on. If desired, the first sequence or any of the others could be called upon to recycle a different number of times until

the over-all program was complete. In brief, each sequence of a large program could be treated as an event with the over-all program appearing as a sequence.

Emergency Procedures

Emergency handling techniques can be designed into the system after the logic circuitry has been synthesized. Such provisions could allow manual shutdown or automatic shutdown in the event of trouble. The automatic action could be provided by actuator overload signals, over-travel signals, temperature signals, etc. Provisions can also be made to return the system to the starting position or to set it at some intermediate stage of the sequence should an interruption take place.

CHAPTER VII

SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

Summary

A procedure has been developed which permits complex fluid logic sequential circuits to be synthesized directly in a logic table. The development was carried out using a comprehensive cross section of feedback sequences to assure generality of the approach.

The method calls for listing the circuit sequence specification in a tabular form using compact logic notation. Next, a step-by-step procedure is employed for assigning logic elements in the table. When all of the steps have been completed, the table contains the entire logic structure of the desired circuit. The status of all the elements in the circuit at each interval of the sequential operation is easily determined. The circuits are obtained directly from the table by inspection. This new table is called the synthesis table.

The procedure was demonstrated to be capable of yielding two types of circuits. One type results from working with the single input signal that changes state at the completion of an event, while the other results from

working with the stabilized combination of input signals which exists at the completion of an event.

Conclusions

A fundamentally different philosophy of circuit synthesis is represented by this study. The usual approach is to transform the sequential problem into a combinational or static problem, where the time-independent methods of logic algebra can be applied. This treatment considers the sequential circuit as a dynamic system involving time. Several important conclusions, which can be drawn as a result of this approach, are as follows:

1. A new procedure has been developed which permits a fluid logic designer to systematically and rapidly synthesize circuits of large complexity.
2. Circuits synthesized by this procedure are considered to be optimum. They have the fastest possible response time because the input signal that is produced at the completion of one event is routed directly through a prepared path to start the next event. Delays occur only when a previous input signal must be shut off by the new input signal before the next event can begin. Only two types of logic functional elements are required to implement the equations for

large sequential problems. This is the minimum number that can be used in large sequences. The circuits contain a minimum or near minimum of total logic elements. This claim is based on the fact that large circuits synthesized by the new procedure exhibit the same desirable logic structure as that of carefully designed ideal simple circuits. Then, too, the procedure builds up workable circuits by adding only the logic elements which are required. With the exception of some of the shut-off valves, all of the memory valves are switched with no flow through the valves. This feature permits the use of lower level switching signals and provides faster response.

Efforts to produce large circuits of the above type by other synthesis methods have not been successful.

3. The procedure is more versatile than was initially believed. It can work with combined inputs or single inputs to yield different types of circuit realizations. The fastest acting circuits result when the single input signal is used. The use of combined signals sometimes results in a

slight reduction in total logic elements and does not require shut-off valves.

4. Circuits can be synthesized much faster by the new synthesis table method than by any of the existing techniques, whether formal or intuitive. For example, it would require about fifteen separate tables and maps to synthesize the 24-event sequence of Chapter V by the flow table method, whereas the new method required only one table. The amount of effort saved increases rapidly as the sequences become larger.
5. Hazards are automatically excluded provided the synthesis is carried out in accordance with the recommended procedures. Other logical complications such as critical races, oscillations, lockups, and cycles are also avoided.
6. The last example in Chapter V demonstrates the procedure's ability to handle a large problem without resorting to a computer as would have been required by other methods. However, by programming the procedure for computer operation, extremely large problems could be solved. (A flow chart description of such a program is contained in the Appendix.)

In the flow table method, each additional variable, whether an input or a secondary, doubles the size of the problem to be solved. Even large computers soon reach a limit in their ability to handle the situation. This condition does not hold for the synthesis table method because it is not necessary to provide space for all the solution possibilities. This procedure starts with the bare specification and adds only what is necessary to realize a specific type of circuit. Thus, the number of variables does not quickly become a limiting factor and the opportunity is provided for the development of very complicated sequential circuits.

7. Combinational circuits are those which can be realized without memory elements because each event can be produced by some unique combination of input signals. However, such circuits may also be synthesized using the new procedure which works only with the single input signal rather than combinations. The advantages are faster response and possible circuit simplification.
8. This procedure helps to change fluid logic design from an art, which it has largely

been, into a rational synthesis technique. Thus, an engineer with basic knowledge can quickly learn to derive circuits systematically, whereas in the past, he would have had to develop considerable skill and experience to become an efficient circuit designer.

9. Although the synthesis method has been developed specifically to meet the needs of fluidic circuits, the logic is fundamental and can be adapted to electrical circuits just as the flow table method is used in both disciplines.

Recommendations for Further Study

This study has demonstrated that the synthesis table method is effective in developing two types of circuits which satisfy sequential specifications involving feedback inputs. Modifications or extensions of this method are expected to result in more general procedures which can handle a broader range of sequential problems. Areas recommended for further investigation are as follow:

1. Modification of the procedure to yield circuits containing active secondaries or memory valves. The flow table method now produces circuits of this type. However, the synthesis table approach should

offer the following advantages:

a. Larger sequences could be handled.

b. Hazards could be easily detected and eliminated.

c. Continuous insight would be maintained throughout the process.

d. Minimum hardware circuits of this type should result.

2. Extension of the procedure for synthesizing circuits with non-feedback inputs. A first step would be to control the inputs with logic circuitry to **preclude** the inputs from getting out of a desired sequence. The second step would be to develop a procedure which can handle the problem when alternate input sequences are allowed. It is possible that this problem can best be treated using active secondaries.

3. Non-feedback input sequential problems in which the outputs are signals and do not involve physical events such as the extension or retraction of cylinders. Computational circuits would be of this type. Signal delays would have to be considered.

4. Circuits which use pulse signals rather than the level type. Such circuits could use more types of hardware including

triggerable flip flops, binary counters and pulse shaping devices.

5. Development of programs to permit computer solutions using the procedures resulting from the above efforts.

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APPENDIX

This study has concentrated upon developing the mechanics of a new procedure for the systematic synthesis of fluid logic sequential circuits. As demonstrated, the circuit equations for large complex sequences can now be developed directly in a synthesis table in a routine manner.

Although the synthesis table is an effective format for mechanizing the synthesis process, the procedure which the table contains is also well suited for adaptation to computer operation. Each step of the procedure involves a logical decision and does not depend on intuition. A block diagram or flow chart corresponding to the procedure outlined in Chapter V is shown in Figure 18. The operation which a computer would perform at each step of the process is indicated. A program realization of this chart would cause the computer to write out the circuit equations as a result of feeding in the sequence specification.

As further exploitation of automation requires large numbers of events to be scheduled, a computerized procedure will become not only desirable, but necessary. A computer method would be faster than the tabular method and would permit the synthesis of practically any size sequence.

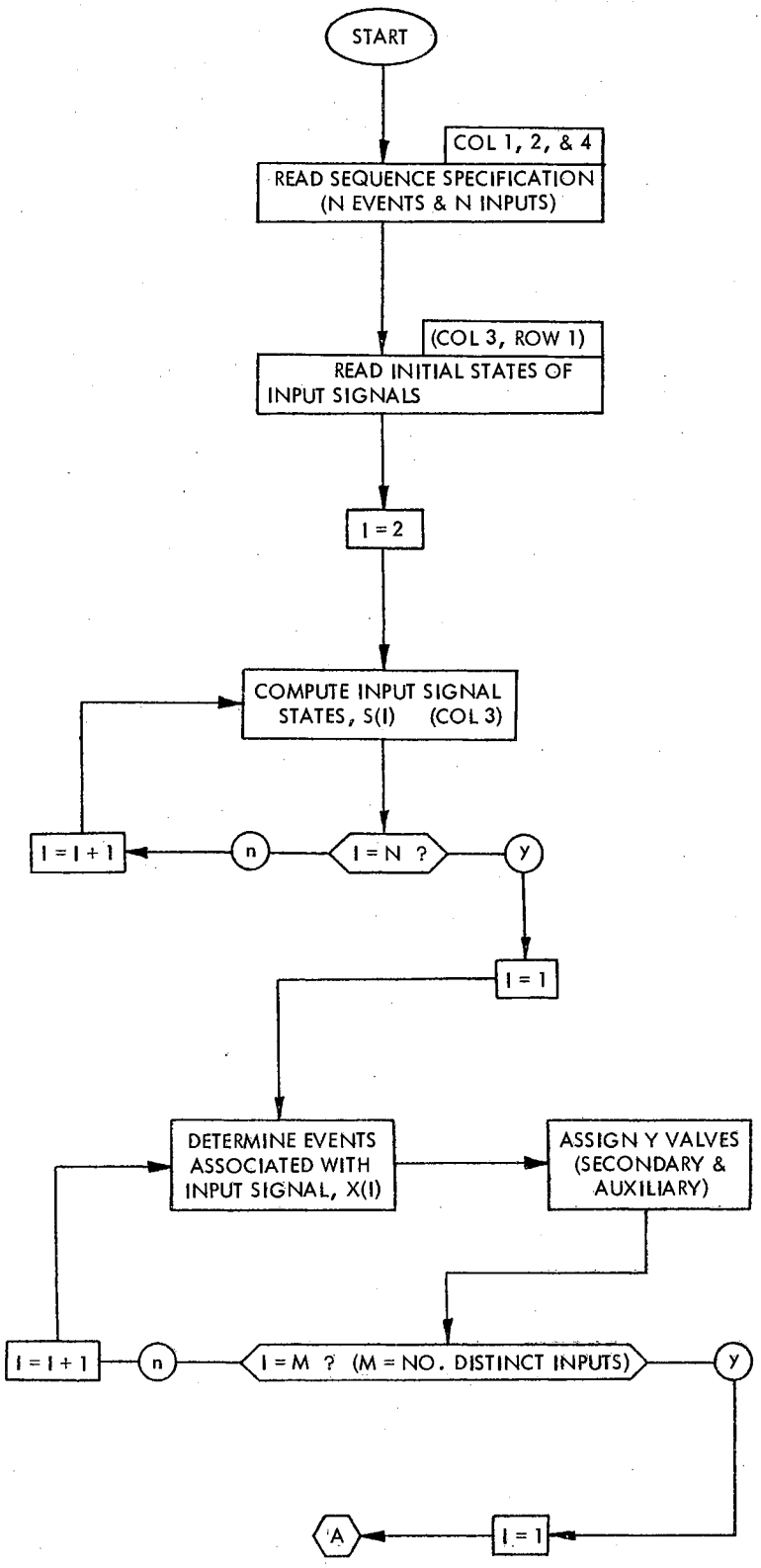

Figure 18. Logic Flow Chart of Synthesis Procedure

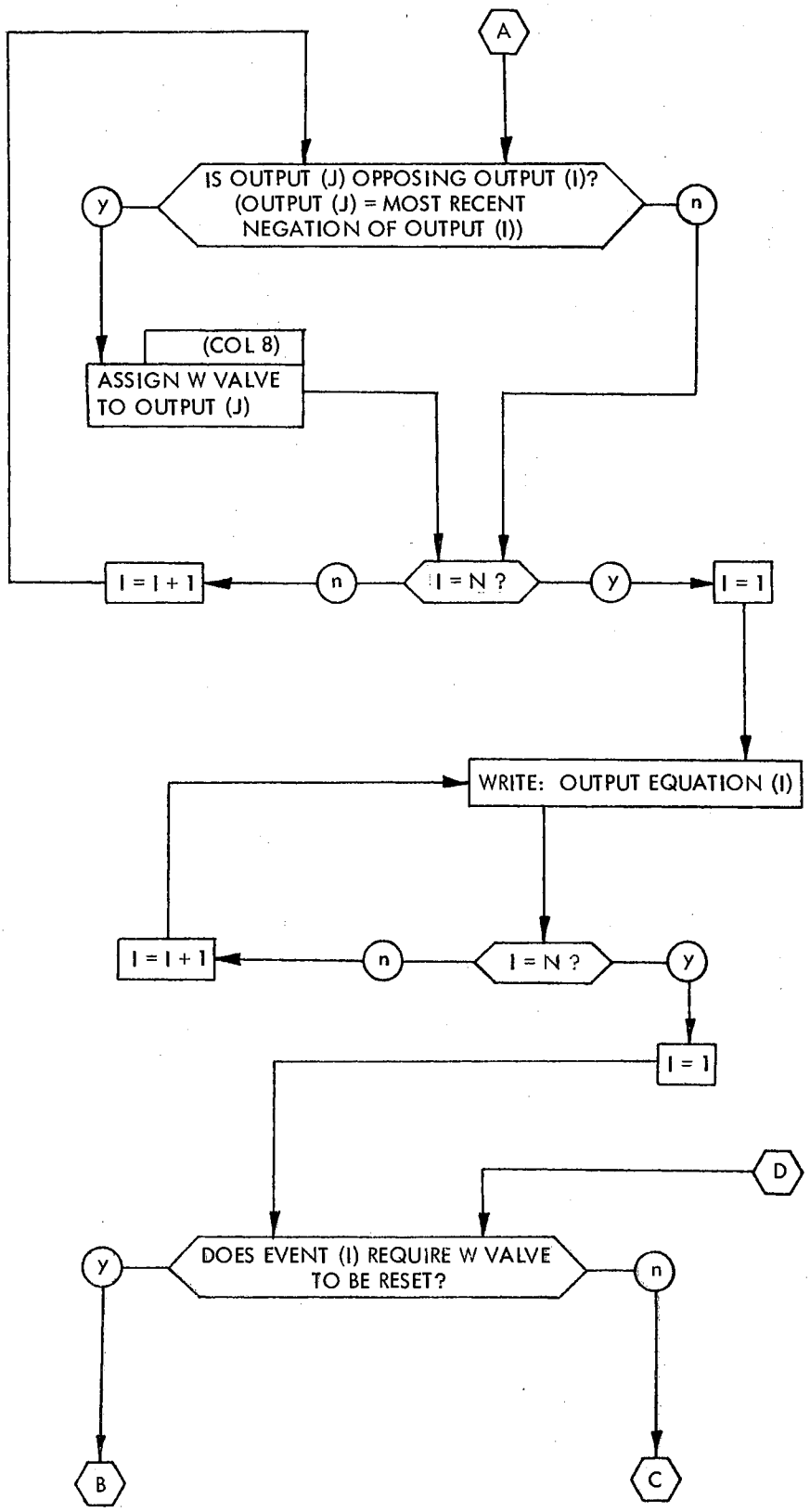

Figure 18. (Continued)

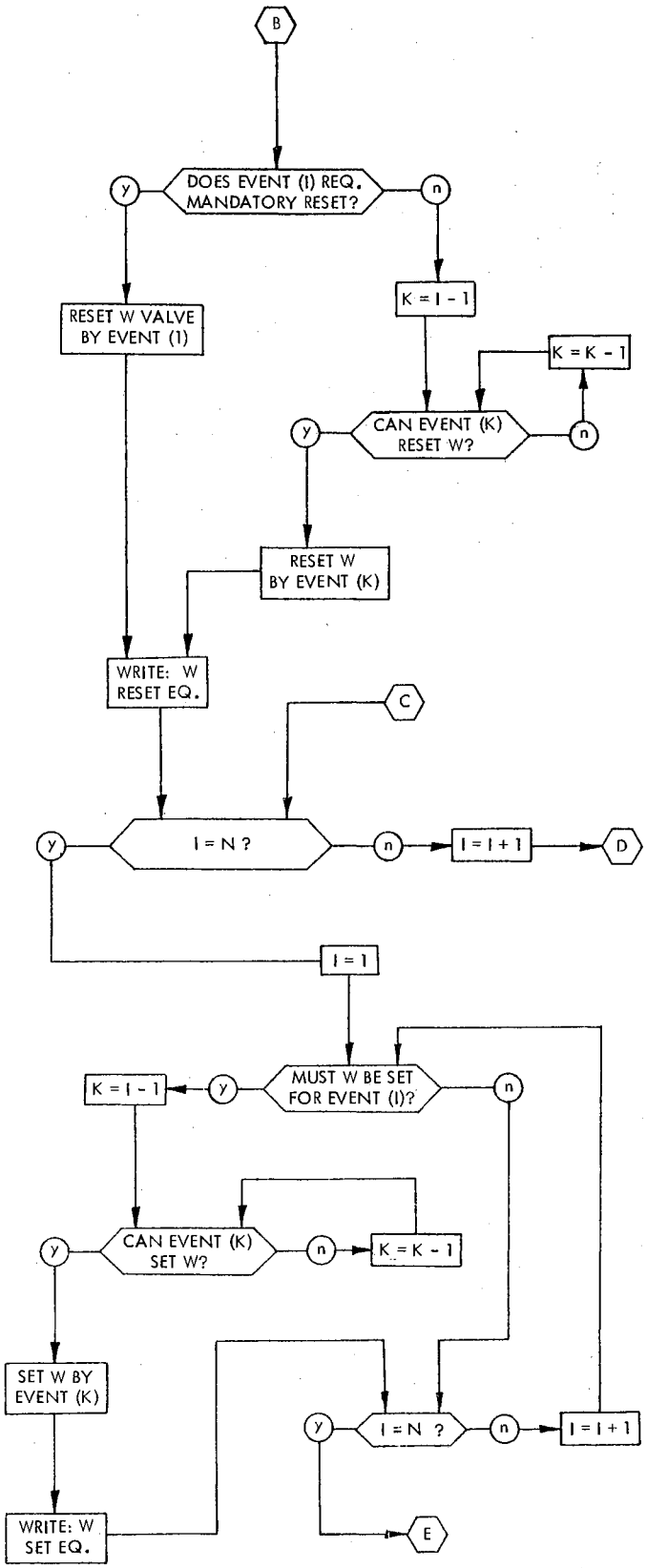

Figure 18. (Continued)

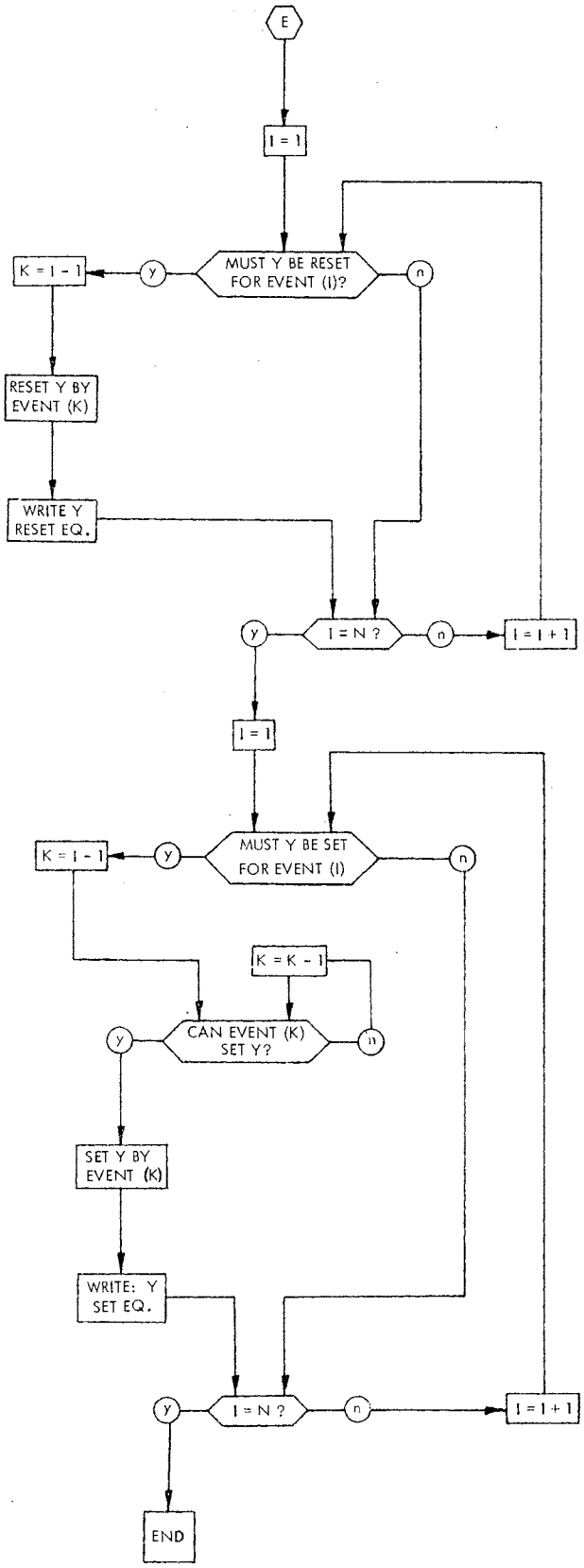

Figure 18. (Continued)

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