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AN INVESTIGATION OF SILICON TRANSISTOR STORAGE TIMES AT LOW TEMPERATURES

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AN INVESTIGATION OF SILICON TRANSISTOR STORAGE TIMES

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CHAPTER I

INTRODUCTION

The field of low temperature solid state research has been characterized by two divergent approaches. The physicist has long used decreased temperatures in his studies of the properties of solid state and semiconductor materials in order to adequately separate intrinsic and extrinsic effects. The bulk of such research has been concerned with the resistivity and Hall coefficient for single crystals or aggregate crystal ingots under various impurity conditions. The engineer is more interested in the possible optimization of devices as related to their operating characteristics at low temperatures. In most cases the engineer has tended to make the assumption that the operating temperature band for solid state devices such as transistors and diodes is limited to a small region as compared to the wide range of ambient temperatures to which many present systems are being subjected. In particular the advent of cryogenic techniques into the computer field, as well as the emergence of space flight computers has given rise to the requirement that electronic subsystems be designed to operate at reduced temperatures. An example of this is a

recent requirement set forth by the National Aeronautics and Space Administration (9) which states that electronic subsystems used in lunar landing vehicles be able to operate over the ambient temperature experienced at the lunar surface.

The particular area of interest developed in this dissertation is concerned with the storage time of silicon transistors subjected to low ambient temperatures. Storage time as used here is defined as the time necessary for a transistor driven into a saturated state of operation to return to a normally biased active region of operation after removal of the driving current. From this definition it is apparent that this work is of immediate interest to engineers concerned with the design of circuits and systems which utilize binary or pulse coding techniques as well as those engineers and scientists responsible for the design and fabrication of transistors to be utilized for such circuits. In particular those scientists and engineers responsible for the design of space flight systems and components must consider the effects of low ambient temperatures on storage time since environmental conditions dictate this mode of operation.

Active researchers working in this general area may be broken down into three general classifications. There are those investigating the properties of semiconductors at low temperatures, those concerned with the development of switching models for transistors, and a smaller group interested in the cryogenic applications of solid state devices. Typical of these groups is the work of the low temperature physics group at Purdue which has done extensive work in the process

of investigating the properties of silicon and other materials under cryogenic conditions, the work of Ebers and Moll (5) in developing a classical theory of large signal behavior of junction transistors, and the recent work reported by Credle (2) in measuring the active state parameters of alloy transistors at reduced temperatures. The Purdue group has been primarily concerned with the development of fundamental theories concerning the properties of semiconductor materials, and have not considered active devices as an entity. Groups working on the development of circuit models for transistors have generally assumed operation at fixed temperatures and thus avoid the problems arising from wide temperature variations. Credle has neglected the problems arising from saturation effects by limiting his experiments to the active or non-saturated state.

None of the groups working in this area have attempted to operate at low temperatures with saturated conditions on the transistor. It is not possible to use models or theories developed by the previous work to explain some effects noted under these conditions. The investigations performed in this experimental program show a definite trend away from results as predicted from classical theory. It has not been possible to explain the deviation of observed phenomena on the basis of known perturbations such as surface recombination, or crystalline dislocations. It was decided that the deviations from trends predicted by classical theory required detailed investigation to determine and define the processes and factors giving rise to such departures from expected variations.

The present program of research was undertaken in order to develop a thorough understanding of silicon transistors in the saturated state with particular emphasis on the response of the storage time at low temperatures. Through development of the physical significance of the factors giving rise to an observed anomalous behavior at low temperatures, it is hoped that some measure of knowledge will be contributed to the understanding of low temperature solid state device operation. There should be great value in this type of information in order that special devices may be fabricated to obviate the difficulties outlined.

CHAPTER II

STATEMENT OF THE PROBLEM AND REVIEW OF PREVIOUS WORK

Objectives of the Study

The increasing complexity of electronic circuits used for information processing and storage, as well as the increased speed necessary for handling large amounts of information has led to serious consideration of thin film crossed field cryotron memory systems. While such systems are still in the research phase, their promising characteristics of high packing density and fast switching speed make them extremely attractive for future computer applications. There is in addition an increased usage of micro-electronic circuits for high packaging density systems for use in space flight applications. These systems and their associated pulse drive and telemetry circuits will be subjected to ambient temperatures not presently experienced by standard solid state systems.

A large number of the systems to be used for space flight and cryotronic memory systems will involve transistors in the switching mode of operation. Cryotronic memory systems and the associated solid state circuitry must be designed to operate at the optimum condition in regard to switching times.

Calculations based on classical theory tend to indicate that

the rise time, fall time, and storage time of a transistor used in the switching mode should decrease with temperature decrease. Based on such considerations it is reasonable to use the cryogenic plant to cool some of the drive circuits associated with the memory banks. In addition it would appear that best performance might be obtained by operating the telemetry and pulse drive circuitry in space flight electronic systems at the low ambient temperatures on the dark side of the spacecraft.

Due to these considerations it has become necessary to take a serious and critical look at the behaviour of active semiconductor devices at cryogenic temperatures. In particular, the variation of switching time must be determined as a function of the device ambient temperature.

Previous Work

Previous work on switching characteristics stems from a classic paper by Ebers and Moll in the December 1954 issue of the Proceedings of the Institute of Radio Engineers. In this article definitions of the various parameters and an analysis of the coefficients in the current equations for a transistor in the three operating regions of cutoff, active state, and saturation were defined. An equivalent circuit valid in each region was determined. No attempt has been made by the authors to determine the efficacy of these circuits for large temperature changes. In all cases reported the temperature was assumed to be 300°Kelvin.

The relations developed by Ebers and Moll seem to hold for the

rise and fall time in a temperature band from about $200^{o}K$ to $400^{o}K$. This band is further limited by the doping characteristics and geometrical construction of the transistor.

It is generally conceded that the analysis of Ebers and Moll is adequate for the cutoff and active state regions of operation at normal temperatures. Much additional work has been devoted to a better analysis of the processes involved in the saturated or region three state. Notable among contributors in this field are Gariano (7), Lin and Jordan (12), Wiencek (16), and Nanavati (13).

Nanavati has concentrated his efforts upon the establishment of a method for predicting the storage time of a transistor from a knowledge of the small signal parameters. This method of storage time determination has some merit since an indication of switching performance may be determined from available manufacturers data. No attempt has been made to consider the variation of the small signal parameters due to variables inherent in the switching process such as instantaneous emitter current change, collector to emitter voltage deviation, potential gradient, and large signal modulation. No analysis has been attempted for the case of large temperature deviation.

Wiencek has applied three diffusion process equations for the analysis of the three current regions, onset, storage, decrease, which occur in the saturated state. The model derived by this technique is superimposed on the active state model of Ebers and Moll to determine a model which is stated to hold in all regions of operation. It should

be noted that no real advantage is gained over that of the Ebers and Moll model, since each current source included in the Wiencek model is active only in a certain region of operation. While this model is indicative of the actual diffusion processes which occur in the saturated state, in reality it sets up two distinct models. The models degenerate into the models as determined by Ebers and Moll. No attempt has been made to specify the parameters of the circuit as functions of the ambient temperature.

Lin and Jordan have derived a series of expressions which show that the maximum energy transferred to the transistor base during transient or switch conditions is determined by the sustain voltage and the external load. The energy transferred will cause excessive dissipation due to the current amplification occurring in the collector region. It has also been noted that the junction temperature rise during switching is directly proportional to the transient energy delivered to the transistor. From the results obtained it is possible to state that cooling or maintaining the junction temperature at a constant value will render the device less susceptible to injury from transient surges, and obviate the necessity of extensive protective devices.

Gariano has carried out an interesting analysis of the diffused junction and surface barrier transistor regarding transient switching effects. His analysis is based upon a first order solution of the diffusion equation and is quite extensive. The results obtained from

this analysis agree well with the results obtained from the model of Ebers and Moll, and in addition have the geometric and electronic characteristics predominant, which allows further insight into possible device improvement. The analysis falls somewhat short of the desired results inasmuch as the variation with temperature is neglected.

Credle has reported results of a series of tests run on a group of similar pnp alloy junction transistors where the ambient temperature was varied from $76^{o}K$ to $300^{o}K$. The major part of this report is concerned with the high frequency small signal "y" parameters. It is reported that grounded emitter pulse tests were conducted where the transistor was driven to the edge of saturation, and the results showed a decrease in rise time for a given output pulse. In addition it was noted that since rise time decreases with increased output pulse, it is possible to deliver large output current pulses from small signal transistors when they are immersed in liquid nitrogen. No attempt was made by Credle to analyze either the rise or decay time in an attempt to discover the causes of this decrease. In addition to these pulse measurements, Credle has measured the high frequency "y" parameters and concludes from the results that the expressions developed by Shockley (15) for the pnp germanium alloy transistor are valid and may be extended over this temperature range. From the results as measured by Credle it is possible to state that the bandwidth, current carrying capability, and frequency cutoff may be increased by lowering the ambient temperature.

Hickmott (8) has developed an amplifier which will operate at liquid nitrogen temperatures. In the course of this development Hickmott measured the effect of lowered temperatures on batteries, paper capacitors, electrolytic capacitors, ceramic capacitors and resistors. The amplifier finally developed was not capable of being totally immersed in liquid nitrogen. This was not due to the transistor, but to the large value of capacitance required for emitter bypass. Hickmott has found that electrolytic capacitors are not usable below about zero degrees centigrade. It should be noted that this should not be such a great problem if sintered anode tantalum capacitors are used, since they are rated usable to minus fifty degrees centigrade. In the report by Hickmott no data on pulsing or switching effects is included.

A large number of papers have been published in the past twenty years concerning the properties of semi-conductors. Notable among groups working in this field have been the scientists at Bell Telephone Laboratory, the physics department at Purdue, and more recently the scientists at the Watson Laboratory at Columbia.

For work done prior to 1950 concerning the behavior of both silicon and germanium at low temperatures, and for information on basic transistor phenomena, an excellent source of material is Shockley's book (15). In Chapter 11 of this reference, the works of Pearson and Bardeen, Horovitz, and many other investigators are presented in some detail. Of major interest in this connection, the resistivity of silicon (lightly doped) alloys are seen to decrease

from room temperature (25°C) to slightly below 0°C, and then to increase with further temperature reduction. In addition, highly doped materials are shown to be either independent of temperature, or of slightly higher conductivity as the temperature decreases.

Most of the work on the low temperature behavior of semiconductors since 1950 has centered around an attempt to explain an anomalous behavior exhibited by resistivity versus temperature plots for germanium. In addition many measurements on the Hall coefficient have been published. The steep maximum in the log R versus 1/T curves for germanium crystals at liquid helium and liquid hydrogen temperatures has received particular attention. Fritzsche (6) and Hung (10) have reported extensive investigations into the properties of single crystal germanium. In addition, Fritzsche has reported the effect of compensator additions which tend to change the resistivity slope and the required ionization energy. Using this technique Fritzsche has developed an empirical relation for the conductivity which takes the form:

$$\sigma = C_1 \exp(-E_1/kT) + C_2 \exp(-E_2/kT) + C_3 \exp(-E_3/kT)$$

where E_1 is the donor ionization energy and the first term represents the conduction band conductivity.

E_2 is determined from the slope of the conductivity curves at low temperatures.

E_3 is determined by subtraction of the other two terms from the value of conductivity in the 3°K to 10°K temperature range for samples of moderate impurity concentration.

It should be noted that this expression does little to explain the process of conduction, or to resolve the question of the anomaly, it does however give a basis for stating that evidently three conduction processes are involved. Since E_3 and E_2 are highly dependent upon impurity concentration Fritzsche and others have concluded that the conduction between impurity centers as proposed by Hung is a highly probable process.

Debye and Conwell (3) as well as Kohane (4) have made further measurements on the electrical properties of germanium for n type doping. They have measured the conductivity and Hall coefficient for samples in a temperature range from 11°K to 300°K. Great care was used in the preparation of the samples used in these experiments, and results which are predictable using classical theory are reported. In some aspects the agreement is questionable, since only 10 percent agreement was used as a basis for their conclusions. Two principal conclusions concerning n type germanium lattice mobilities are obtained. The mobility varies as $T^{-1.64}$, not $T^{-1.5}$ for the temperature range of 20.4°K to 300°K, and at temperatures below the inversion or intrinsic bound, the impurity mobility varies less rapidly than predicted by theory. The exponent on T for impurity mobility varies between 1.0 and 1.5 depending upon concentration. It has also been noted that an effective carrier mass of about one fourth the free electron mass gives a best fit relation. Deviations from the -1.5 and +1.5 exponents on T are easily explained by pointing out that these exponents are based on the assumption that the band edge is

located at the center of the Brillouin zone, and that the assumption of spherical constant energy surfaces is not true for either silicon or germanium based on the magnetoresistance measurements of Johnson and Horovitz (11).

Scalar and others (13) have reported a low temperature breakdown effect in germanium. By using both d.c. step functions and microsecond pulses on germanium at liquid helium temperatures the existence of a reversible, non-destructive breakdown effect at low voltages has been observed. The breakdown occurs in both n and p type germanium and is manifested as a sharp increase of current for a small voltage change. The charge carrier multiplication due to impact ionization of impurity neutral particles is suggested as a possible source of carriers necessary for the breakdown effect. The high mobility of charge carriers at these temperatures seems to indicate the probability of such a process.

Measurements made by Johnson and Horovitz on semiconductors in the liquid hydrogen, liquid helium range have provided much of the information about the behavior of semiconductors at low temperatures. These scientists have reported on resonance phenomena, energy band structure, Hall coefficient, conductivity, impurity band phenomena, microwave absorption, and thermo-electric power measurements. Of particular interest are values determined for silicon, both n and p types. Cyclotron resonance experiments on n type silicon suggest that constant energy surfaces for the conduction band in silicon are not spherical, but rather are ellipsoids of revolution about the cubic axis in the

Brillouin zones. The cyclotron effective mass is made up of both a transverse and a longitudinal component and the orientation of the magnetic intensity relative to the major axis of the ellipsoid. Measured values are respectively:

$$m_l = 0.98\ m_o \text{ , and } m_t = 0.19\ m_o$$

For p type silicon two resonance peaks have been observed, which indicates the presence of two mass components, one "heavy" and one "light" hole with masses $m_1 = 0.16\ m_o$, $m_2 = 0.5\ m_o$.

Energy band structures based on these measurements reveals a conduction band edge which does not lie at the k=0,0,0 point, but slightly off this point, while the valence band edge does lie at the 0,0,0 point. The significance of this picture lies in its ability to help clarify deviations from theoretical considerations concerning the mobility, and thus electron and hole relaxation times.

Due to the low temperatures used for the work done by this group and others at Purdue, all impurity conduction was predominatly caused by either positive (p-type), or negative (n-type) carriers. If this is allowed as a basic assumption, then the conductivity mobility may be expressed as:

$$\mu = q\tau/m_\sigma$$

where τ = relaxation time

m_σ = "conductivity" mass, $0.26\ m_o$ for n type silicon,

$0.38\ m_o$ for p type silicon.

Since τ depends upon the scattering process, its temperature dependence and therefore the temperature dependence of the conductivity

mobility depends upon the type of scattering dominant in a particular temperature band. The experimental results show that an additional source of scattering is present at low temperatures, which is thought to be due to the scattering of conduction electrons by impurity ions.

Past efforts by workers in the field of transistor switching circuit theory have yielded satisfactory results of both a theoretical and experimental nature regarding device behaviour at normal ambient temperatures. No previous work has been reported on switching characteristics at low temperatures except for measurements of fall and rise time on a non-saturating alloy junction germanium transistor. Much of the basic numerical data on conductivity processes in semiconductors at low temperatures has been reported by various groups. The fundamental properties and their deviations from classical predictions have been determined and evaluated by several low temperature physics groups, but this information has not led to a clear cut definition of the physical process which gives rise to such deviations. The theory of impurity center conduction as proposed by Hung has not been generally accepted, although many other proposed theories degenerate into a different statement of Hung's theory. The impurity center conduction picture will explain empirical results based on measured conductivities at low temperatures.

Many of the early textbooks written on transistor device behaviour, and some of their more recent competitors make a flat statement that "transistors and other solid state devices will not work at low temperatures in the liquid hydrogen or helium range." This

statement is never accompanied by any reference to published works, and is in general attributable to hasty conclusions drawn from approximate equations describing device operation which are not meant to be extrapolated over such a wide range. It is a matter of some concern that such statements are allowed in view of the published results of many tests on tunnel diode oscillators which operate from liquid helium temperatures into the ambient region of normal rooms.

Specific Objectives of the Present Investigation

The successful implementation of switching circuits for high speed computer applications demands optimum device operation. In conjunction with proposed cryogenic memory elements it has been suggested that an optimum temperature situation may be achieved for excitation circuits which would give fast rise and decay times for control purposes. While it is true that lowering the temperature will in general speed up the rise time of transistors, no consideration seems to have been given to saturated state operation.

The largest group of transistor digital control circuits in use at present are of the saturated state type. Since any major deviation from this principle would entail laborious and time consuming individual circuit designs, no major changes are to be expected.

Taking such matters into consideration, it was decided that an investigation into the behaviour of silicon transistors at low temperatures with particular emphasis on the storage properties and storage times should be carried out. The storage time parameter represents the worst case condition, and was chosen for intensive study

since equipment was available to make precise measurements on this effect.

An anomaly in the storage time at low temperatures was observed and it became necessary to measure various other parameters of the transistor at lowered temperatures in an attempt to determine the basis for the storage time deviation from classical predictions.

CHAPTER III

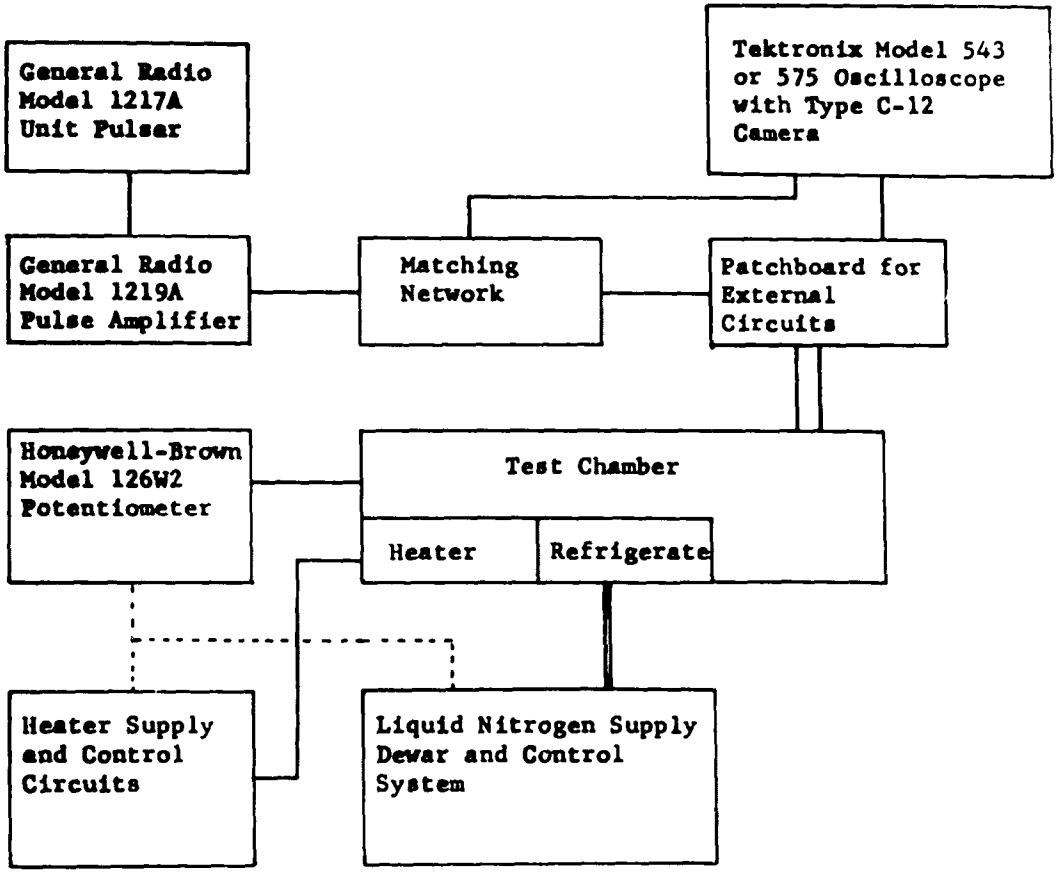
DESCRIPTION OF EXPERIMENTAL APPARATUS

Experimental apparatus used in this program consisted of two major groups: (a) low temperature test chamber and heater with temperature monitoring and control equipment, (b) various signal generating, measuring and recording equipment. A block diagram of the experimental apparatus in a typical configuration is shown in figure 1.

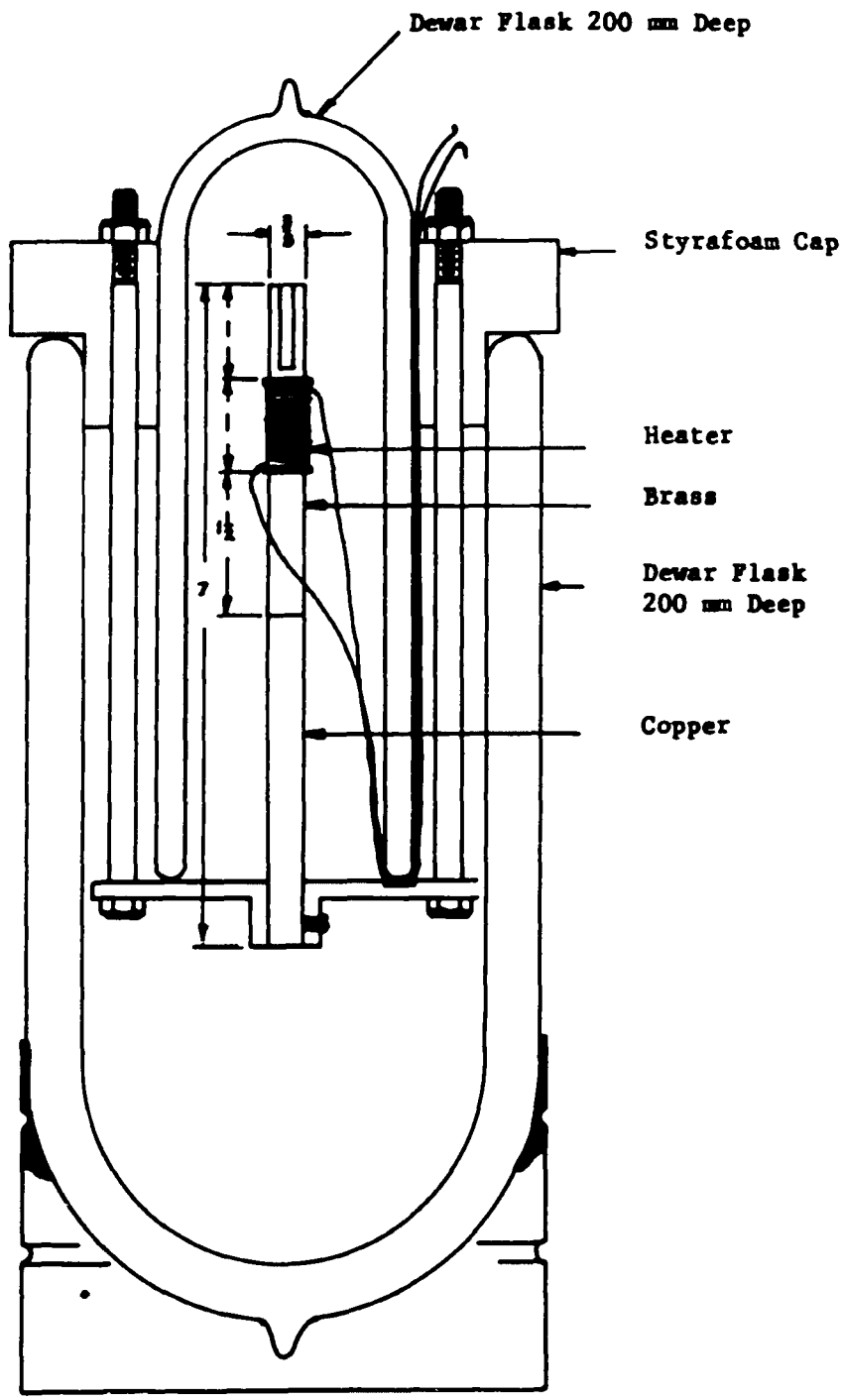
Test Chamber

The low temperature test chamber consisted of a standard liquid nitrogen large mouth dewar filled with liquid nitrogen, and an inverted dewar chamber with a brass and copper rod axially situated so that an electrical resistance heater of 105 ohms resistance could expel heat radially and maintain a uniform temperature. The inverted dewar was used as the sample chamber. A drawing of the test chamber is shown in figure 2.

The control system for the heater consists of a power supply utilizing a full wave bridge rectifier and a slide wire rheostat for current control. A temperature monitoring potentiometer was used for visual checks on the temperature stability of the chamber. By varying the pulse duration of the heat input it is possible to maintain the specimen at any desired temperature from $77^{o}K$ to $300^{o}K$ with a stability of $0.1^{o}K$.



Block Diagram of Typical Measurement System
Figure 1



Low Temperature Test Chamber

Figure 2

Pulse Generation System

Generation. Pulses used for testing the transistors were generated by a General Radio model 1217A unit pulse generator. The pulses used varied from 2 to 10 microseconds duration and were used at repetition rates of 1 and 2 thousand per second.

Amplification. The output pulses from the model 1217A were amplified by a General Radio type 1219A pulse amplifier matched to a 50 ohm external load.

Measuring Instruments and Recording Devices

Small Signal Parameters. The measuring instruments used for determination of the small signal "y" parameters consisted of a General Radio model 1210C sinusoidal oscillator, 561D vacuum tube bridge, and a type 1232A null detector. Current and voltage measurements made in conjunction with these tests were made with a Measurements Corporation model 62 vacuum tube voltmeter, a Triplett model 626 microammeter, and a Beede Electric Instrument Company model 157 milliammeter.

Temperature Measurement. The temperature of the test specimen was measured by means of a copper-constantan thermocouple attached to the specimen with silicone rubber tape. This thermocouple tape assembly had a 2.6 millisecond thermal time lag, and was monitored by a Honeywell-Brown Instrument company model 126W2 potentiometer. This potentiometer has a scale and reference scale calibrated for the 1937 calibration data on copper-constantan. The assembly and potentiometer dial were checked at 25°C against a mercury thermometer, at 0°C in an ice

bath, and at 76°K against liquid nitrogen.

Recording Instruments. The output response of the test section was monitored and recorded using a Tektronix model C-12 oscilloscope camera used with a Tektronix model 543 oscilloscope with a type CA dual trace plug in for the pulse measurements. The same camera was used with a Tektronix type 575 transistor curve tracer for recording the static input and output volt-ampere characteristics of the transistor under test.

Other Measurement Devices. Additional equipment used consisted of General Radio type 722N and 222F precision variable capacitors, a Simpson model 270 multimeter, and a General Electric d.c. ammeter.

CHAPTER IV

PROCEDURE

The initial phases of the experimental work were concerned with the variation of storage time for various silicon and germanium transistors as the ambient temperature was varied from $77^{o}K$ to $300^{o}K$. These measurements resulted in the selection of a particular silicon npn transistor for intensive investigation. Further investigations concerned the determination of various transistor parameters in an attempt to ascertain factors relating to an anomaly observed in the initial measurements.

Storage Time Measurements

Common Base

Storage time measurements for the common base configuration were made with the transistor mounted in a pre-calibrated socket at the termination of a shielded 50 ohm cabling system. A type "T" Leeds and Northrup copper constantan thermocouple was firmly attached to the transistor and the entire assembly was sealed with silicone rubber tape. The transistor was placed in the test chamber and allowed to cool to $77.2^{o}K$. The cabling system was connected to a patch panel where the base lead was connected to the common shield. A variable resistance was placed in series with the emitter in order to maintain

a fixed voltage for one series of tests, and a fixed current for a second series. The emitter to base junction was connected to the "B" input of the dual trace preamplifier for the fixed voltage tests, and a clip on milliammeter (type 456A Hewlett Packard) was connected to the "B" input for the fixed current tests. The collector of the transistor was connected to a six and a twelve volt lead acid storage battery through 1000 ohms, and to the input of the "A" section of the preamplifier. The type 1219A General Radio pulse amplifier was connected to the series resistor in the emitter circuit to provide the driving pulse. This amplifier received driving pulses from the type 1217A General Radio unit pulser. The unit pulser was connected to drive the pulse amplifier with negative pulses and to provide synchronization trigger pulses to the type 543 Tektronix oscilloscope.

The transistor received a fixed voltage or fixed current pulse of 2 microseconds duration at a repetition rate of 1000 pulses per second. The output pulse was displayed on the oscilloscope and was photographed using the C-12 Tektronix camera set at f2.8;1/18. As the test chamber was heated, convenient temperature points were stabilized so that the specimen temperature remained constant for one minute, and the input pulse was monitored and reset when required. The output pulse was then photographed and temperature and approximate value recorded. This was necessary in order to later identify the proper trace for each temperature. During this phase of measurements it was found that changing the external circuit resulted in a change in the storage duration, but not in its variation with temp-

erature. All succeeding tests were carried out with a 1000 ohm load, and a six volt source.

Common Emitter

With the transistor inserted in the test socket and connected through cabling to the patch panel as previously described, the emitter was connected to the common shield. The input from the 1217A pulser was shifted to give a positive pulse to the base, and the series resistor was adjusted for a typical level of input current and voltage which would drive the collector to emitter voltage to approximately zero volts and give a sharp rise to the onset of the pulse measured at the collector. The input pulse system was shifted from emitter to base at the patch panel in order to accomplish the proper drive situation. A photograph of the test equipment as set up for the pulse tests is shown in figure 3.

Base Charge Storage

In order to determine correlation between observed storage time at the collector and the charge storage at the base emitter junction, a measurement of the saturation base charge has been carried out.

The transistor was connected into a circuit as shown in figure 4. A photograph of the test equipment set up for this measurement is shown in figure 5. The pulse input to the base was observed on the oscilloscope, and at each temperature of interest the capacitor was adjusted to give a saturation peak. Capacitors used were the General Radio types 722N and 222F precision variable air capacitors. By pre-loading the

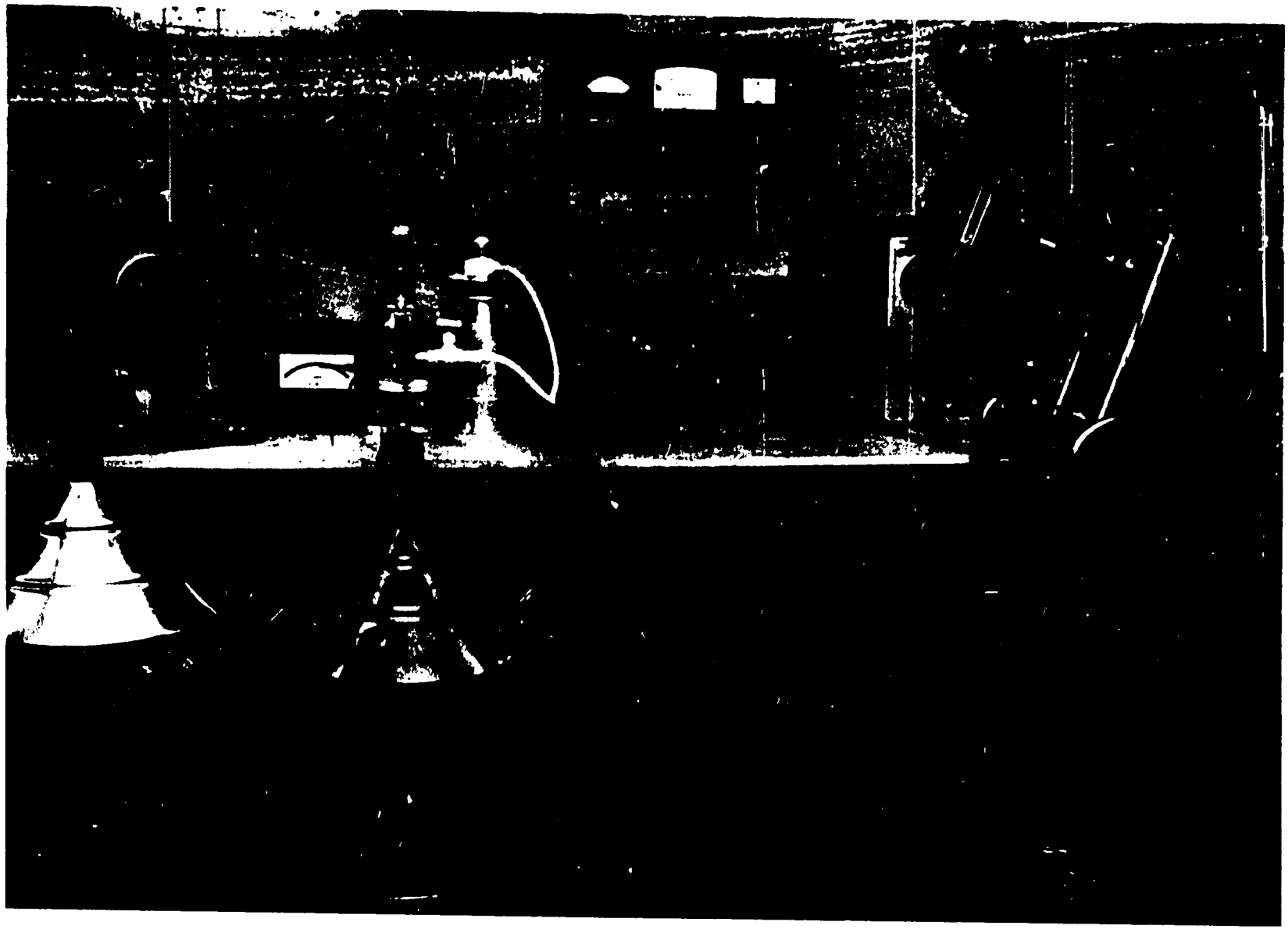
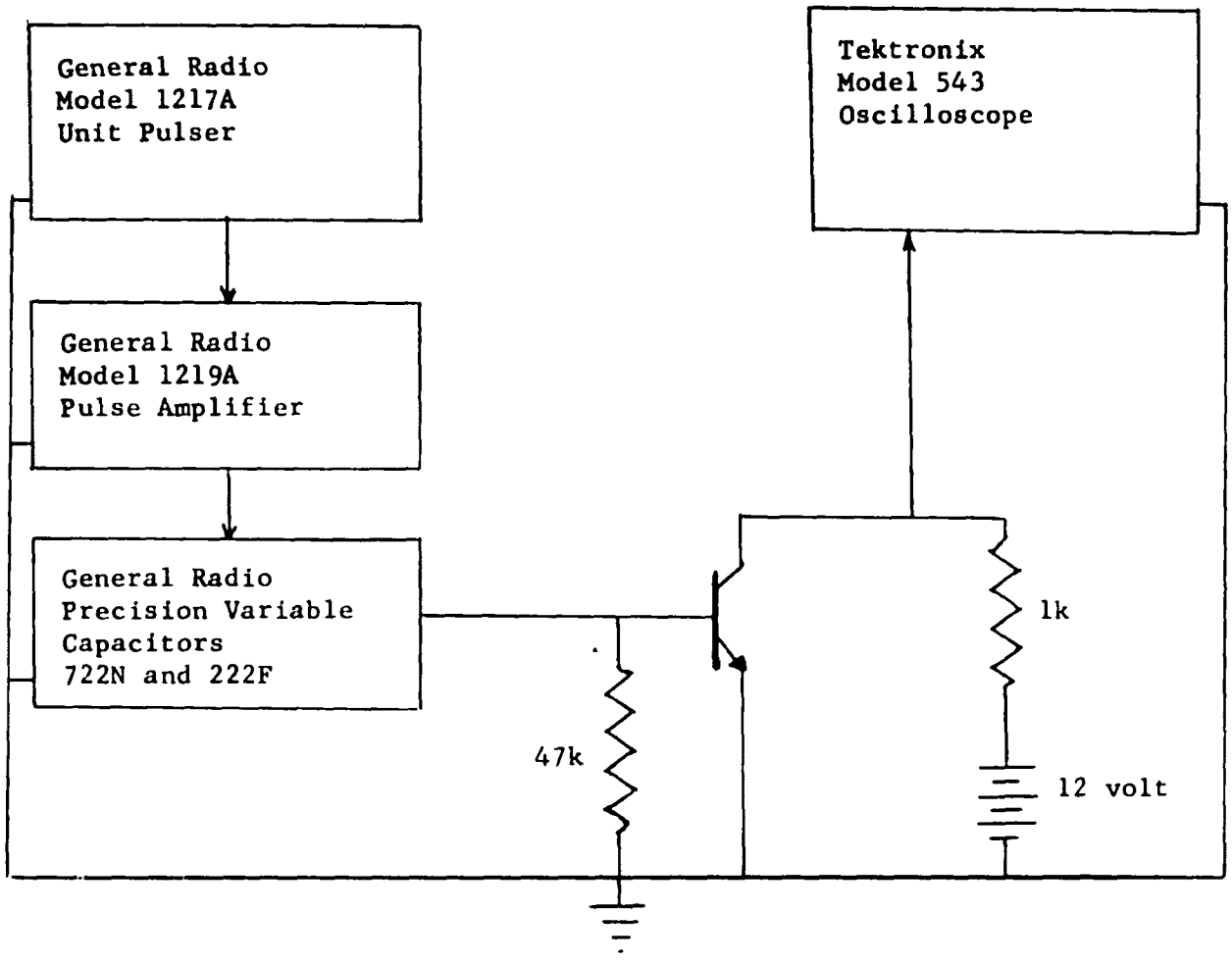


Figure 3 - Test Equipment for Pulse Tests



Base Charge Test Circuit

Figure 4

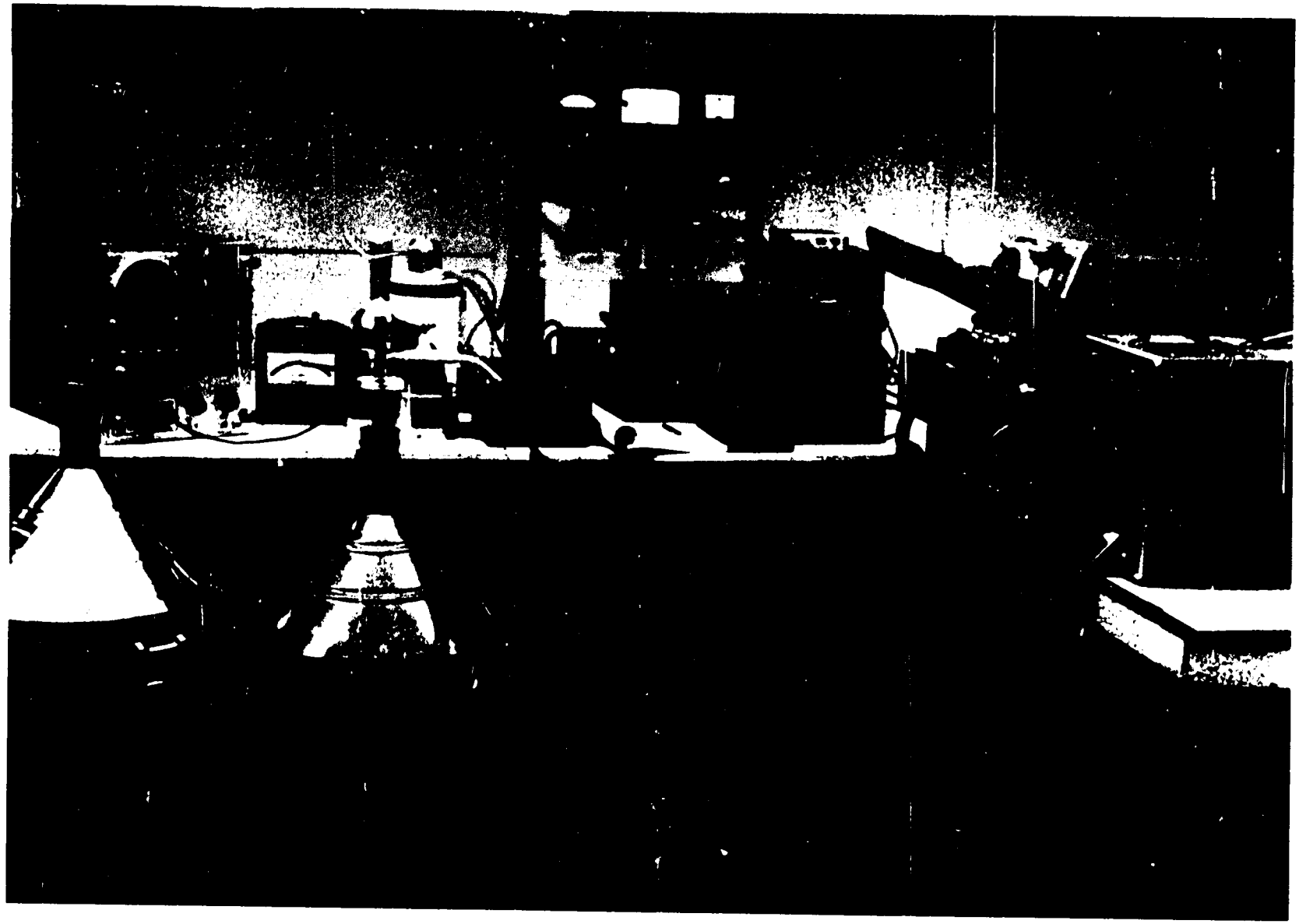


Figure 5 - Equipment for Base Charge Tests

pulse amplifier with a 50 ohm resistor a stable pulse height of 15 volts is applied to the capacitor transistor combination. The static volt-ampere characteristics of the transistor can be measured for both the input and output at the same time as the saturation level is measured, and the base to emitter saturation capacitance is then calculated.

Static Volt-Ampere Characteristics

In order to calculate the value of base to emitter saturation resistance it is necessary to determine the voltage from base to emitter at saturation. A measurement of both the input volt-ampere characteristics and the output volt-ampere characteristics for the transistor was carried out at the same temperature points as the ones chosen for base charge measurements. The type 575 Tektronix transistor curve tracer has two input sections which may be selected for display by means of a front panel switch. A set of input leads was therefore connected so as to measure the base to emitter volt ampere curve at input number one, while another set of leads was connected to measure the output characteristics at input number two. The curve tracer was set up so that the output curves were measured with the simulated six volt source and 1000 ohm load. These curves were alternately displayed and photographed by the C-12 camera. This measurement circuit is shown in the photograph on page 28.

Measurement of Ico

Since the minority current carriers are generally considered as a major cause of difficulty in storage time response it was

considered necessary to measure the value of Ico to determine whether it could be considered as a negligible quantity. A Lambda model 71 power supply was connected in series with a 10 megohm resistor and the collector terminal. The base terminal was grounded and the emitter left open. The power supply was set at 50 volts, and as the temperature was varied the voltage across the collector base junction was measured with a model 62 vacuum tube voltmeter. This voltmeter is reported by the manufacturer to have an input impedance in excess of 10^9 ohms, so negligible loading was assumed. The current was found to be less than 10^{-7} amperes at the highest temperature and decreased as expected, and therefore was neglected as insignificant in the remainder of the tests.

Small Signal Parameters

The small signal "y" parameters were measured in an attempt to check the results of Credle, and to determine the behaviour of the transistor in the active region as the temperature was varied. A special transistor mount was utilized in connection with the type 561D vacuum tube bridge. This bridge will measure the y parameters of any three terminal device at a frequency of 1000 cycles per second. The transistor mount was inserted into the bridge with connections made to the transistor in the test chamber by means of teflon insulated strip line.

Bias for the transistor was effected from a fully charged 6 volt storage cell. The collector to emitter voltage was maintained at a constant level and monitored with the model 62 vacuum tube voltmeter. The bias current at the base was kept constant by means of

a small rheostat and monitored with the Triplett microammeter. The input bias terminals were shunted with a 2000 microfarad electrolytic capacitor to simulate the required short circuit for the bridge measurements. This capacitor effectively isolated the bridge from the microammeter and rheostat loading.

The signal source for the bridge was the 1210C oscillator set to 1000 cycles per second. The detector used was the model 1232A null detector set for logarithmic voltage reading at a tuned frequency of 1000 cycles per second. The source, bridge, detector combination was peaked for maximum sensitivity with the bridge in an unbalance condition before each measurement.

A photograph of the overall instrumentation involved in these tests is shown in figure 6. It should be noted that some measurements on this transistor were attempted using the liquid helium transport dewar shown as the test chamber. These measurements were abortive, although other devices tested in this chamber gave reasonable results during their cooling phase. Tunnel diodes were also tested in this chamber using a constructed curve tracer and showed definite useable characteristics.

Figure 6 - Complete Instrumentation

CHAPTER V

THEORY

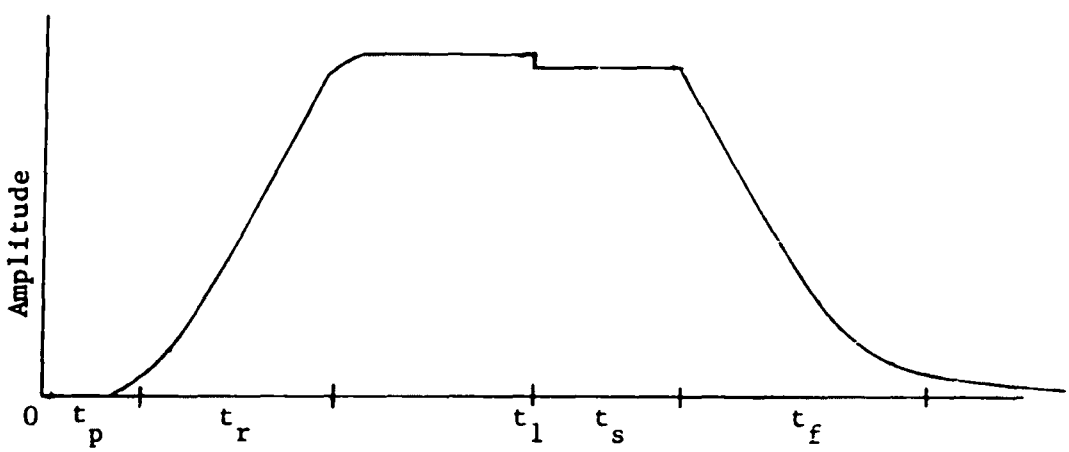
To consider the case of a transistor in the switching mode, three distinct states are covered. The first state of operation is termed the cut-off or region I state. The second state is termed the active or region II state. The third state is termed the saturated or region III state, and is characterized by forward bias at both junctions.

During a normal saturation switching cycle the sequence of events may be characterized by the time necessary for each change of region to occur as related to the driving or saturating pulse. These characteristic times are outlined for the case of a rectangular input pulse as follows:

1. Time necessary to bring the collector into the active region of operation. This is the time required for the pulse front to propagate through the base or emitter region and be felt at the collector. This time is usually symbolized as t_p .
2. Time required for the collector to reach saturation. This time is symbolized by t_r and is called the rise time. By definition it is measured as the time necessary to go from 10 percent to 90 percent of the final value.

3. Time held in saturation, this is determined by the duration of the input pulse and is not considered as a characteristic trait of the transistor.
4. Time required to switch from saturation to active operation after removal of the driving pulse. This is known as the collector storage time and is symbolized as t_s.
5. Time required for the transistor to switch from the end of the storage period to the cut-off region. The time is called fall time and is symbolized as t_f. By definition this time is measured as the time necessary to go from 90 percent to 10 percent of the initial value.

A sketch of a typical output or collector current pulse is shown below with the appropriate times indicated. This sketch is for an input pulse of rectangular form with duration t_1.



In formulating a model to adequately cover the effects at low temperatures two approaches may be used. The first approach would be to attempt an interpretation of effects from a physical model of the transistor. The alternate approach would entail calculations from an equiv-

alent circuit model whose parameters are temperature responsive, and the dependence is known. The circuit model approach is appealing, but too many variables other than temperature will upset the model parameters. The first approach is used with model parameters being used where their dependence is known and will aid in the determination of terms arising in the developed equations.

For the grown junction transistor at room temperature it is assumed that a condition of uniform carrier density, resistivity, and lifetime exists on each side of the emitter base junction. The total current through the junction can be calculated from Shockley's equation:

$$j = q (\mu_n n + \mu_p p) \xi + q (D_n \nabla n - D_p \nabla p)$$

For the grown junction npn transistor with axial symmetry it is suffecient to take the current density in the longitudinal direction times the cross sectional area to determine the total current. This direct method gives an expression of the form:

$$I_x = 2\pi r j_x$$

where j_x is the current density as determined by the one dimensional form of Shockley's equation.

In order to study the effect of temperature on storage time, it is necessary to consider the effect of carrier injection into the base region upon the various parameters and portions of the transistor.

Consider the case of an npn grown junction transistor with the collector to base region reverse biased, and where the emitter to

base junction is either forward biased or zero biased. If a large carrier injection for a time t_1 is effected at the base, then the base and emitter resistances will be modulated by the carriers.

The current density in the semi-conducting region subjected to an electric field ξ , where axial symmetry of the semiconductor is assumed has been proposed as that given by the one dimensional case of Shockley's equation:

$$j_x = q (\mu_n n + \mu_p p) \xi_x + q (D_n \nabla n - D_p \nabla p)$$

where j_x = current density in the longitudinal direction

μ_n = electron mobility

μ_p = hole mobility

p = hole density

n = electron density

ξ_x = electric field intensity = V_{DC} / L_B

V_{DC} = average value of base voltage

L_B = effective base width

D_n = electron diffusion constant

D_p = hole diffusion constant

q = charge of a free carrier = $1.602\ (10)^{-19}$

If an initial equilibrium condition is assumed to exist across the base region, the diffusion terms may be neglected and the current density equation rewritten as;

$$j_x = q (\mu_n n + \mu_p p) \frac{V_{DC}}{L_B}$$

For an npn type transistor, the base conductivity can be expressed as a function of the equilibrium density since before in-

jection only one type of carrier is considered to be present in the conduction sense. The conductivity in the equilibrium state is expressed as:

$$\sigma_o = q\mu_p p_o$$

where σ_o = equilibrium conductivity of the base material

p_o = equilibrium hole density of the base material = $N_a - N_d$

N_a = density of acceptors in the base

N_d = density of donors in the base.

If a block of material with this conductivity has electrons injected from an external generator, then the electron and hole densities are changed so that the following relations are set up:

$$n(xyz) = n_o + \Delta n$$

$$p(xyz) = p_o + \Delta p$$

$$\xi(xyz) = \xi_o + \Delta\xi = \frac{V_{DC}}{L_B} + \Delta\xi$$

where Δn = excess electron density

Δp = excess hole density

$\Delta\xi$ = change in electric intensity due to external field.

Substitution of these terms into the current density relation sets up a modified relation such as follows:

$$j_x = q \quad \mu_n (n_o + \Delta n) + \mu_p (p_o + \Delta p) \quad \xi_o + \Delta\xi$$

For an npn transistor biased class B, subjected to an applied positive rectangular voltage pulse at the base, the following conditions prevail at the base:

$$\Delta\xi_x \gg \xi_{xo} \; ; \; \Delta n = \Delta p \ll p_o \; ; \; n_o \ll p_o$$

Using these relations, the base current may be determined by integrating over the volume of the base:

$$I_x L_B = q \int_S \left[\mu_n (n_o + \Delta n) + \mu_p (p_o + \Delta p) \right] \left[\Delta \xi_x \right] dS$$

It is also possible to state that $\Delta \xi_x$ will not be a function of the geometry if diffusion terms are neglected, this amounts to making the applied pulse duration long compared to the propagation time. Under this condition the current - base width product may be written as:

$$I_x L_B = G_o \Delta \xi_x L_B^2 + q \Delta \xi_x (\mu_n + \mu_p) \int \Delta p \, dS$$

or:
$$I_x L_B = G_o \Delta V L_B + q \frac{\Delta V}{L_B} (\mu_n + \mu_p) \Delta N$$

where ΔN = excess number of carriers in the base (holes or electrons)

ΔV = height in volts of the pulse applied from base to emitter.

This equation may be rewritten in terms of a conductance term and a conductance modulation term as follows:

$$I_x = G_o \Delta V + q (\mu_n + \mu_p) \frac{\Delta N}{L_B^2} \Delta V$$

let
$$\Delta G = q (\mu_n + \mu_p) \frac{\Delta N}{L_B^2}$$

then
$$I_x = \Delta V (G_o + \Delta G)$$

The continuity equation for carriers in a system such as this may be written as:

$$\frac{\partial (p - p_o)}{\partial t} = - \frac{(p - p_o)}{\tau_s} - \frac{1}{q} \nabla \cdot I_p + g_p$$

or
$$\frac{\partial (n - n_o)}{\partial t} = - \frac{(n - n_o)}{\tau_s} - \frac{1}{q} \nabla \cdot I_n + g_n$$

where the signs are appropriate to the charges and currents and

where $p - p_o = \Delta p$

$n - n_o = \Delta n$

g_p = external hole generation rate

g_n = external electron generation rate

I_p = hole current

I_n = electron current

If diffusion effects are neglected then the continuity equation for holes may be rewritten as:

$$\frac{d\Delta p}{dt} + \frac{\Delta p}{\tau_s} = g_p$$

the excess hole density Δp can be expressed as Q/Ω where Ω = volume of the base. The rate of external hole generation can be expressed as:

$$g_p = {}^{I_B}/_{\Omega}$$

and the Laplace transform of Q(t) can be expressed as:

$$Q(s) = \frac{I_B}{s}\left[\frac{1}{s + 1/\tau_s}\right] \qquad \text{for } Q(0) = 0$$

and $$Q(t) = I_B\tau_s\left[1 - \exp\left(-t/\tau_s\right)\right]$$

therefore:

$$\Delta p(t) = \frac{Q(t)}{\Omega} = \overline{\Delta p}\left[1 - \exp\left(-t/\tau_s\right)\right]$$

where $$\overline{\Delta p} = \frac{I_B\tau_s}{\Omega}$$

At some time less than the pulse width, the density of holes at a distance x from the emitter-base junction may be determined. At time t this density is given by an expression of the following type:

$$\Delta p(x) = \overline{\Delta p}\left\{1 - \exp\left(\frac{-\left(t - x/\mu_n\Delta\xi_x\right)}{\tau_s}\right)\right\}$$

integration of this expression from 0 to x_1 will yield the expression for the change in the number of carriers:

$$\Delta N = \int_0^{x_1} \frac{A\Delta p}{q} \left(1 - \left[\exp\ (-t/\tau_s) \right] \left[\exp\ \frac{x}{\mu_p \Delta\xi_x \tau_s} \right] \right) dx$$

where A = cross-sectional area of the active base region.

$$\Delta N = \frac{A\overline{\Delta p}}{q} \left(x_1 + \left[\mu_p \Delta\xi_x \tau_s \right] \left[1 - \exp \frac{x_1}{\mu_p \Delta\xi_x \tau_s} \right] \right)$$

If the first order term in the series expansion is assumed to be sufficient for an expression of the exponential term in x, then;

$$\exp \frac{x_1}{\mu_p \Delta\xi_x \tau_s} = 1 + \frac{x_1}{\mu_p \Delta\xi_x \tau_s}$$

and $$\Delta N = \frac{Ax_1}{q} \overline{\Delta p}\ (1 - \exp\ -t/\tau_s)$$

since $$\overline{\Delta p} = \frac{I_B \tau_s}{\Omega}$$

and $$\Omega = Ax_1 \quad \text{for } x_1 = L_B$$

then $$\Delta N = \frac{I_B \tau_s}{q}\ (1 - \exp\ -t/\tau_s)$$

The change in conductance due to the application of a drive current I_B is given by the expression:

$$\Delta G(t) = \frac{\mu_n + \mu_p}{L_B^2}\ \tau_s I_B\ (1 - \exp\ -t/\tau_s)$$

Defining $(\mu_p + \mu_n)\tau_s/L_B^2$ as M, the conductance of the base may be written as:

$$G(t) = G_o + MI_B\ (1 - \exp\ -t/\tau_s)$$

and the base resistance may be written as:

$$r_{bb} = \frac{1}{G(t)} = \frac{r_{bb_o}}{1 + r_{bb_o} MI_B \left(1 - \exp -t/\tau_s \right)}$$

where $r_{bb_o} = 1/G_o = {}^{L_B}/_{q\mu_p p_o A}$

If the total charge in the base during the application of the base drive current I_B is expressed as:

$$Q = I_B \tau_s$$

then the electron density in the base during carrier injection is given by the relationship:

$$n = n_o + Q/\Omega$$

Due to recombination processes, the excess electron density will decrease in an exponential manner with time, and the excess term may be expressed as:

$$\Delta n = \frac{I_B \tau_s}{\Omega} \exp -t/\tau_s \ .$$

From the continuity equation the following relationships may be set up:

$$\frac{\Delta n}{n_o} = \frac{\Delta p}{p_o} = \exp qV/kT$$

If this equation is solved for V, the potential across the base to emitter junction may be determined:

$$V = \frac{kT}{q} \ln \frac{\Delta p}{p_o} = \frac{kT}{q} \ln \frac{\Delta n}{n_o}$$

substituting the expression previously obtained for Δp into the above

equation gives the following result for V:

$$V = \frac{kT}{q}\left(\ln \frac{I_B \tau_s}{\Omega} - \ln p_o - \frac{t}{\tau_s}\right)$$

The first two terms in this expression may be defined as $V_{BE(Sat.)}$ which equals the potential across the base at the moment the pulse is removed, and the total potential across the base may then be written as:

$$V = V_{BE(Sat.)} - \frac{kT}{q} \cdot \frac{t}{\tau_s}$$

To determine the collector current it is necessary to evaluate each term of the continuity equation under the conditions previously defined. The continuity equation for the one dimensional case is expressed as:

$$\frac{dn}{dt} = \frac{-\Delta n}{\tau_s} - \frac{1}{q} \nabla I_n + g_n$$

where Δn has been previously determined as Q/Ω . The rate of density change is proportional to the net rate of change in charge, and may be expressed by:

$$\frac{d\Delta n}{dt} = \frac{1}{\Omega} \frac{dQ}{dt}$$

for the one dimensional case under consideration the diffusion equation for electrons may be written as:

$$I_n = qD_n \frac{dn}{dx}$$

therefore:

$$\frac{dI_n}{dx} = qD_n \frac{d^2 n}{dx^2}$$

If a linear electron density is assumed, then the second derivative term will be zero and the diffusion portion of the continuity equation will indeed vanish. For the case of a grown junction axially symmetric transistor with a large base the assumption of linear electron density is reasonable. Since the net rate of electron or hole generation in the base region has previously been defined as:

$$g_n = \frac{I_B}{\Omega}$$

then the continuity equation may be rewritten as:

$$\frac{1}{\Omega}\frac{dQ}{dt} = \frac{-Q(t)}{\Omega\tau_s} + \frac{I_B}{\Omega}$$

Taking the Laplace transform of this expression for the condition that Q (t=0) = 0 yields the following equation:

$$sQ(s) = -\frac{Q(s)}{\tau_s} + \frac{I_B}{s}$$

or $$Q(s) = \frac{I_B}{s}\left[\frac{\tau_s}{1 + s\tau_s}\right]$$

Taking the inverse Laplace transform for this expression yields the expression for Q(t) as follows:

$$Q(t) = I_B\tau_s\ (\ 1 - \exp -t/\tau_s\ )$$

For the npn transistor being considered it is possible to assume that the electron current in the base is primarily due to collector current under saturated conditions, therefore the equation for the base electron charge may be written as:

$$Q(t) = \frac{I_C\tau_s}{\beta} = I_B\tau_s\ (\ 1 - \exp -t/\tau_s\ )$$

solving this equation for I_C gives:

$$I_C = \beta I_B \ (1 - \exp - t/\tau_s)$$

where β = common emitter current transfer ratio $\Delta I_c/\Delta I_B$

During storage time the continuity equation for charge processes may be written as:

$$\frac{dQ}{dt} = \frac{Q}{\tau_s} - I_R$$

where a linear charge gradient has been assumed. I_R is the reverse current during the storage time which occurs in the base. The Laplace transform for the time variation of charge in this case is:

$$sQ(s) = I_B\tau_s + \frac{Q(s)}{\tau_s} - \frac{I_R}{s}$$

or $$Q(s) = \frac{I_B}{s + 1/\tau_s} \cdot \frac{I_R}{s(s + 1/\tau_s)}$$

Taking the inverse Laplace the equation for time variation of charge is determined as:

$$Q(t) = I_B\tau_s \exp - t/\tau_s - I_R\tau_s (1 - \exp - t/\tau_s)$$

If the current through the base is primarily due to collector current, then the time variation of charge may be written in terms of the collector current and expressed as:

$$Q(t) = \frac{I_C\tau_s}{\beta}$$

If this expression is joined with the previous expression then an expression is determined for I_C as a function of the base current and the reverse current. This equation is given on the following page as:

$$I_C = \beta \left[I_B \exp -t/\tau_s - I_R (1 - \exp -t/\tau_s) \right]$$

During saturation and storage time the external circuit constants and the saturation voltage of the transistor determine a simultaneous value for I_C such that :

$$I_C = (V_{CC} - V_{CE(Sat.)}) / R_L$$

where $V_{CE(Sat.)} = I_C R_{CS}$

R_{CS} = collector saturation resistance.

therefore:

$$I_C = \frac{V_{CC}}{R_L} - \frac{I_C R_{CS}}{R_L}$$

since $R_L >> R_{CS}$ we may assume that $I_C = V_{CC} / R_L$.

Combining the two equations for I_C under saturated and storage conditions it is possible to write the following relationship:

$$\exp \frac{-t_s}{\tau_s} = \frac{V_{CC} / R_L + \beta I_R}{\beta (I_B - I_R)}$$

This equation may now be solved to determine the storage time equation:

$$t_s = \tau_s \ln \frac{\beta (I_B - I_R)}{\beta I_R + V_{CC} / R_L}$$

The reverse base current I_R may be determined from the following relation:

$$I_R = \frac{Q}{\tau_s}$$

where Q represents the charge stored in the base to emitter capacitance.

The capacitance at the base and the charge may be related by the expression; $Q = C_{BE}V_{BE}$, where the value of V_{BE} has previously been determined as a function of both temperature and time as:

$$V_{BE} = V_{BE(Sat.)} - \frac{kT}{q} \cdot \frac{t}{\tau_s}$$

The value of $V_{BE(Sat.)}$ has been observed in the course of the experimental program, and an empirical relation of the form:

$$V_{BE(Sat.)} = mT + B$$

has been determined. In the case of the silicon transistor studied, the slope was found to be equal to -1.36 millivolts per degree Kelvin, while the interpolated intercept was approximately 1.3 volts. The actual limit on $V_{BE(Sat.)}$ as T approaches zero is more likely the gap potential of 1.1 to 1.14 volts as reported by various investigators. The potential difference measured for silicon diodes having junctions of essentially plane construction was 0.989 volts at a temperature of $4.2^{o}K$.

The capacitance at the base should be approximately determined by the following expression:

$$C_{BE} = \left[\frac{q}{kT}\right]^2 \frac{I_E L_B^2}{2\mu_n \tau_s}$$

where $I_E = (I_B - I_R) \cdot (1 + \beta)$

and μ_n is known to be proportional to $T^{-1.5}$ from statistical theory. If we choose the average value of I_E for use in this equation then it is possible to effect a simple solution. If the time dependence of I_E and

V_{BE} are used, then a circular mathematical path for solution of the storage time equation is involved. It was decided that for purposes of determining temperature dependence the average level could be used for I_E and the base to emitter voltage could be used as a linear function of temperature based on the empirical relation. If these assumptions are used then the value of I_R may be determined as:

$$I_R = \left[\frac{q}{kT}\right]^2 \left(\frac{(1+\beta) I_B L_B^2 \ (mT+B)}{4\mu_n \tau_s} \right)$$

Substitution of the above relation into the previously determined equation for the storage time was effected in order to determine the temperature dependence of this parameter. This step gave rise to the following equation:

$$t_s = \tau_s \ln \left[\frac{I_B - \left\{ \left(\frac{q}{kT}\right)^2 \left[\frac{(1+\beta) \ I_B L_B^2 \ (mT+B)}{4\mu_n \tau_s} \right] \right\}}{\left(\frac{q}{kT}\right)^2 \left[\frac{(1+\beta) I_B L_B^2 \ (mT+B)}{4\mu_n \tau_s} \right] + \frac{V_{CC}}{\beta R_L}} \right]$$

This equation will reduce to the relation found by Gariano for the pnp alloy germanium transistor, and also to the equation determined by Ebers and Moll for the alloy transistor, if proper conditions are placed on the signs and allowances make for the defined values of C_{BE} , I_R , and I_E used to determine the above. It has the further advantage of indicating what factors are important in designing a transistor for minimal storage times. One of the most important factors to consider is the relaxation time or recombination time, as symbolized by τ_s.

Since the lifetime τ_s is one of the most important factors in the storage time equation, it is necessary to consider probable recombination processes which determine the value of τ_s .

For a general treatment of the factors governing carrier transition rate probabilities, it should first be noted that the energy form for carrier activation is most probably that of impact ionization. For every excitation or ionization process there must be a converse recombination process whereby the excited carriers undergo transitions to lower energy states. If the idea of impact ionization from externally generated carriers is accepted, then this means that collision processes are highly probable for the recombination.

A correlation should exist between the rate of a process and its converse. The connection between these two rates is provided by the principle of detailed balance. The statistical concept of this principle may be stated as follows:

"For a system in thermal equilibrium the rates of a process and its inverse are equal and balance in detail."

When a semiconductor departs from thermal equilibrium due to any external stimulus, then the principle of detailed balance will no longer hold, but the principle of microscopic reversibility is still maintained. This principle states that the transition probabilities for an event and for its converse are equal. Due to the application of these two principles on probabilities under conditions of steady state excitation it is generally possible to apply the

ideas of detailed balance to a semiconductor.

It is the tendency of a non-equilibrium electron density n to restore itself to an equilibrium density n_o. This tendency may or may not be proportional to the excess density Δn. It is in general possible to state that the deviation in linearity of the restoration tendency from Δn is small, and under this assumption the continuity equation may be written as:

$$\frac{\partial \Delta n}{\partial t} = g_n + \frac{1}{q} \nabla I_n - \frac{\Delta n}{\tau_n}$$

where g_n = electron generation rate

τ_n = electron bulk lifetime

The simplest model for semiconductors makes the assumption that τ_n is completely independent of Δn. If this model is assumed, it is possible to solve the continuity equation regardless of the positional dependence of g_n and I_n . Where τ_n does depend upon the excess electron density , the equation becomes difficult to solve since the positional dependence of g_n and I_n must be known either functionally or in terms of a statistical matrix. Since the usual case for τ_n is one of virtual independence of Δn for small samples and external generation processes, it is possible to state that ∇I_n does vanish, and that g_n is independent of positional terms. The continuity equation becomes a simple first order equation in this case and may be written as;

$$\frac{d\Delta n}{dt} = g_n - \frac{\Delta n}{\tau_n} = g_n - \Delta n \upsilon_n$$

where $\upsilon_n = 1/\tau_n$ = bulk recombination rate.

For long term generation, where the rate of generation is large compared to the bulk lifetime, the bulk lifetime will be the ratio of the excess electron density to the external generation rate. When excess generation stops, then the recombination rate υ_n is the logarithmic decrement of Δn, and sets the rate at which conditions tend towards equilibrium:

$$\upsilon_n = \frac{-1}{\Delta n} \frac{d\Delta n}{dt}$$

When the recombination processes are restricted to band to band transitions, then the recombination rates for electrons and for holes are identical. Under these conditions the lifetime may be symbolized as: $\tau_s = \tau_n = \tau_p$.

When an electron in the conduction band undergoes a transition and falls to the valence band, its potential energy difference must be given up as some other form of energy. The principle of detailed balance and microscopic reversibility leads to a statement of general balance which might be applicable to this case, whereby the energy form for the recombination transistion is of the same type as the generative form. It should be noted that this statement comes as a result of a combination of the principle of detailed balance and microscopic reversibility and refers to the form of the recombination energy and not to the transition probability. In order to develop a physical theory for the dynamics of the transition process, a generative process must be defined.

For the transistor junction at thermal equilibrium in a shielded

radiationless environment the most probable generation process would be impact ionization from an external source. The injected carriers will accelerate the carriers present and raise them to higher conduction states. The inverse process for this generative cause is known as Auger recombination.

The Auger recombination process involves two parallel phenomenon. One of these consists of electron-electron collisions while the other involves hole-hole collisions. In the case of electron-electron collision, a finite probability exists that an electron pair may collide in such a manner that one drops to the valence band, while the other rises to an empty state high in the conduction band. The static electron-electron recombination rate may be designated as R_{ee}, while the dynamic value is designated as r_{ee}. The inverse of this process consists of electron pair creation by impact ionization. The generation rate for this type of process has a static value represented as G_{ee}, and a dynamic value which is symbolized as g_{ee}. From the principle of detailed balance it is possible to state:

$$R_{ee} = G_{ee}$$

Hole-hole collisions may result in excitation to a low valence state and recombination with an electron from the conduction band. In this case the recombination and generation rates are symbolized as:

$$R_{hh} = G_{hh}$$

In a semiconductor with heavy holes such that:

$$\zeta = (m_e / m_h) \ll 1 ,$$

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In a semiconductor with heavy holes such that:

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then the difference in the electron-electron recombination rate and the electron-electron generation rate will dominate the recombination for n-type, p-type, or intrinsic material. In heavily doped p-type material hole-hole processes will become dominant.

Blakemore (1) has pointed out that calculations based on a model of Beattie and Landsberg yield the following expressions for the two thermal equilibrium rates:

$$G_{ee} = A\, n_i^2\, T^{-1.5} \exp\left[-\zeta E_i \,/\, (1+\zeta)kT\right]$$

$$R_{ee} = B\, n_i^2\, T^{-1.5} \exp\left[-\, E_i \,/\, (1+\zeta)kT\right]$$

where A and B are proportionality constants, and E_i is the intrinsic energy gap.

The generation and recombination rates as expressed represent equal upwards and downward rates. When the semiconductor block receives injected excess carriers such that $\Delta n = (n - n_o) = (p - p_o)$, then the recombination rate exceeds the generation rate. This condition sets up a dynamic recombination rate given by the expression:

$$r_{ee} = G_{ee}\left(\frac{n^2 p}{n_o^2 p_o}\right)$$

since the electron-electron recombination involves two electrons and one hole. The generation rate for the dynamic condition is given by:

$$g_{ee} = G_{ee}\left[\frac{n}{n_o}\right]$$

The net rate of recombination is given by the difference of these two dynamic rates. The recombination rate (net) is therefore given as:

$$(r_{ee} - g_{ee}) = G_{ee} \left\{ \frac{np - n_i^2}{n_i^2} \right\} \frac{n}{n_o} .$$

The continuity equation may now be written in terms of the transition rates as:

$$g_n - \frac{dn}{dt} = (r_{ee} + r_{hh}) - (g_{ee} + g_{hh}) = \frac{np - n_i^2}{n_i^4} (G_{ee} np_o + G_{hh} pn_o).$$

Since the regular continuity equation has already given the value of $1/\tau_s$ as;

$$\frac{1}{\tau_s} = \frac{g_n}{\Delta n} \frac{dn}{dt}$$

then the lifetime due to Auger recombinations may be written as equal to τ_A , where $\tau_A = \tau_s$ and is given by the following expression:

$$\tau_A = \frac{n_i^4}{(n_o + p_o + \Delta n) (G_{ee} np_o + G_{hh} pn_o)}$$

The Auger lifetime equation may be rearranged in terms of the intrinsic lifetime and a constant of proportionality which turns out as a function of temperature in the following manner:

$$\tau_A = \frac{2n_i^2 \tau_i}{(n_o + p_o + \Delta n) [(n_o + \Delta n) + \gamma(p_o + \Delta n)]}$$

where $$\tau_i = C_1 (kT)^{-1.5} \exp\left\{ \left(\frac{1+2\zeta}{1+\zeta} \right) \frac{E_i}{kT} \right\}$$

and $$\gamma = \left(\frac{\zeta^{0.5} (1 + 2\zeta)}{2 + \zeta} \right) \exp\left(\frac{1 - \zeta}{1 + \zeta} \left[\frac{E_i}{kT} \right] \right)$$

The intrinsic carrier density n_i varies in accordance with an expression of the form:

$$n_i = C_a T^{1.5} \exp(-E_i/kT)$$

and the terms $n_i^2 \tau_i$ in the Auger lifetime vary with temperature according to the expression:

$$\tau_A = C_b T^{1.5} \exp\left[\left(\frac{\zeta}{1+\zeta}\right) \frac{E_i}{kT}\right]$$

All processes in a semiconductor vary with doping level, and the density of hole - electron pairs. The small modulation lifetime is given by the expression:

$$\tau_o = \frac{2n_i^2 \tau_i}{(n_o + p_o)(n_o + \gamma p_o)}$$

for $\Delta n \ll n_o , p_o$

Rearrangement results in the expression:

$$\tau_o = \frac{2\tau_i}{(1 + n_o / p_o)(1 + \gamma p_o / n_o)}$$

It should be noted that in the intrinsic region where $\gamma << 1$, the expression for τ_o reduces to τ_i. For a p type semiconductor the ratio of n_o/p_o moves rapidly to a value which is much less than one upon cooling due to the reduction in thermal electrons in the conduction band. The first effect noted would be an increase in the denominator to the value one, and the lifetime would approach $2\tau_i$. On further cooling, the lifetime rises less rapidly. The transition would occur when the electron supply becomes extremely limited in

comparison with that of free holes, and the hole-hole processes dominate. When the second term in the denominator ($1 + \gamma p_o / n_o$) reaches a value of 2, the transition temperature will be reached. At temperatures rather lower than this transition, the hole-hole processes take over completely and the lifetime is given by the term $n_i^2 \tau_i$.

When donor atoms are more numerous than acceptors, the semiconductor goes to an extrinsic n type upon cooling. Where the majority carriers consist of electrons, it is probable that a large recombination rate will be maintained over a wide temperature range. Letting the symbol $\Delta n_o = n_o - p_o$ be used to denote the excess density of ionized donors over ionized acceptors, then:

$$n_o = \frac{1}{2} \Delta n_o + \sqrt{\frac{1}{4} \Delta n_o^2 + 4 n_i^2}$$

If it is assumed that $(n_o + \Delta n) >> \gamma (p_o + \Delta n)$, then the Auger lifetime may be written as:

$$\tau_A = \frac{4 n_i^2 \tau_i}{(\Delta n + \Delta n_o^2 + 4 n_i^2) (2\Delta n + \Delta n_o + \Delta n_o^2 + 4 n_i^2)}$$

If we take the equality case where $n_o = p_o = n_i$, then this expression reduces to the following:

$$\tau_A = \frac{2 n_i^2 \tau_i}{(2 n_i + \Delta n) (n_i + \Delta n)}$$

As the semiconductor cools, the lifetime diverges since the value of n_i decreases due to the reduction of conduction electrons, and the

lifetime for an n type material approaches a limiting value given by the expression:

$$\tau_A = \frac{2n_i^2\tau_i}{(\Delta n_o + \Delta n)^2} \qquad \text{for } n_o \approx \Delta n_o \gg n_i$$

It has previously been shown that the storage time for a transistor may be expressed as:

$$t_s = \tau_s \ln \frac{\beta (I_B - I_R)}{\beta I_R + V_{CC}/R_L}$$

where the predominant term was shown to be that due to τ_s . It has further been shown that τ_s is a lifetime due to Auger recombination processes, and that the Auger process is proportional to the product of the carrier density squared and the intrinsic lifetime for n type materials. The Auger lifetime is proportional to the intrinsic lifetime for p type materials at low temperatures where hole-hole processes dominate.

If the logarithmic terms could be neglected in the equation for t_s as being independent of the temperature, then the lifetime would be the only variable term, and the storage time could be written as:

$$t_s = AT^{1.5} \exp(-E_i / kT)$$

If the logarithmic terms are not neglected, but all terms which are not temperature dependent are called constants, then the storage time may be written as:

$$t_s = C_1 T^{1.5} \left[\exp (-E_i/kT)\right] \left\{\ln \left(C_2 T^{-1.5} \left[\frac{aT-b}{cT+d}\right]\right)\right\}$$

CHAPTER VI

RESULTS

General Comments

In the initial investigations attempted, the pulse response test of Ebers and Moll was set up with a transistor mounted in a shielded socket inside the variable temperature dewar. It was expected from the theoretical considerations that the storage time should vary as $T^{1.5}$, and that an optimum temperature point could be determined for best switching condition in terms of lowered storage time and fair values of β. The tests were also run on the supposition that the exponent on T would not be exactly 1.5, but that it could be determined and should lie somewhere between 1.0 and 2.0. Upon the initial cooling to liquid nitrogen temperatures using a 2N118 grown junction transistor, the decrease in storage time was observed on a Tektronix oscilloscope. During this initial observation the storage time was seen to decrease as cooling was effected. At the point of thermal stability the storage time suddenly increased to a value of approximately 2.5 times the room temperature value. This unexpected phenomenon led to a careful check of the test circuit, including parameter changes on the input and output circuit. No external causes could be ascertained for the unusual result, so a different transistor was inserted. Using an alloy junction

transistor the phenomenon disappeared. Subsequent cooling of the alloy transistor by insertion into a liquid helium bath showed an increase in the storage time at some temperature less than $76^{o}K$. Successive tests of some ten mixed types (diffused mesa, micro-alloy, grown-rate, planar mesa, epitaxial, and planar epitaxial) showed the same results at different temperatures. As a general rule it can be stated that the lower the value of storage time at room temperature the lower the transition temperature. This gave credence to the view that some different type of recombination might be taking place at lowered temperatures since the only variable in the storage time equation which might be a definite function of temperature for different geometries was the value of τ_s.

Due to the difficulty of controlling the temperature in the region from $76^{o}K$ to $10^{o}K$, which seems to encompass most of the transition temperatures, it was decided that more intensive investigation would be carried out on the grown junction transistor. Two factors dictated the choice of this transistor. The geometry is relatively simple, fitting the axial symmetry conditions, and the anomaly occurs within the temperature range of the variable dewar.

Storage Time Results

Measurements were carried out on several grown junction silicon transistors using the grounded emitter test circuit of Ebers and Moll. The pulse input was kept constant first in voltage and then in current for this set of measurements. No essential difference in the variation was detected for either of the particular pulses used as long as the saturated condition was achieved. In order to take as accurate a

measurement as possible, a copper constantan thermocouple was fixed to the transistor case and calibrated at room temperature ($72^{o}F$ on a mercury thermometer), ice point ($32^{o}F$ on a mercury thermometer) and at liquid nitrogen temperature (assumed as - $320.4^{o}F$). The output pulse as measured by the Tektronix scope was then photographed as the temperature was increased from the liquid nitrogen point. Plate 1 of figure 7 shows the output pulse for several temperatures from liquid nitrogen temperature to $130^{o}K$ with delays at increasing temperatures moving to the left from the maximum value of 5.98 microseconds at liquid nitrogen temperature to a minimum value of 1.8 microseconds at the highest temperature. Plate 2 of figure 7 shows the delay from left to right as the temperature was increased from $150^{o}K$ to room temperature, with the value of approximately two microseconds storage at $150^{o}K$ to about 6 microseconds at the room temperature. The lower pulse in each plate is a photograph of the input pulse at the base. Table I on page 62 shows the values taken from a photographic set of this type for a typical transistor. Note that the delay on storage time from liquid nitrogen temperature to 135^{o}Kelvin is decreasing, while further increase to room temperature sets up an increasing storage time. These two plates are presented as typical of the many photographs taken from which the data has been abstracted.

The storage time plotted as a function of the temperature for the common emitter configuration is presented in figure 8. Figure 9 is a presentation of the storage time as a function of temperature

for the common base configuration. These curves represent the results for a typical grown junction silicon transistor. Table II is a presentation of the data as abstracted from photographic plates for the common base circuit.

The minimum storage time in both configurations occurs at a temperature of $132^{O}K$. Below this temperature the storage time varies as some function of the form:

$$t_s = CT^{-m} \exp(-E_g / kT) \ .$$

If a value of $m = 1.64$ is chosen for the exponent, the gap energy term E_g may be determined from the curve. A close fit to both the common base and common emitter curves may be obtained for a value of $E_g = 0.05$ electron volts. This corresponds to the activation energy and exponent reported by Johnson and Horovitz for n type silicon under impurity center conduction conditions. If Hung's theory of impurity conduction is correct then it is reasonable to suppose that at low temperatures an impurity scattering will take place giving rise to a different form or value for the relaxation time. Attempts made to fit the experimental data with reasonable functions over the entire range have not been successful. This gives further credence to the belief that an essentially different type of process is occurring.

It is possible to fit this curve with a polynomial expression in T, but such a fit yields no information on processes giving rise to the variation in storage time. Since the storage time has been determined for a typical transistor as a function of temperature having the form:

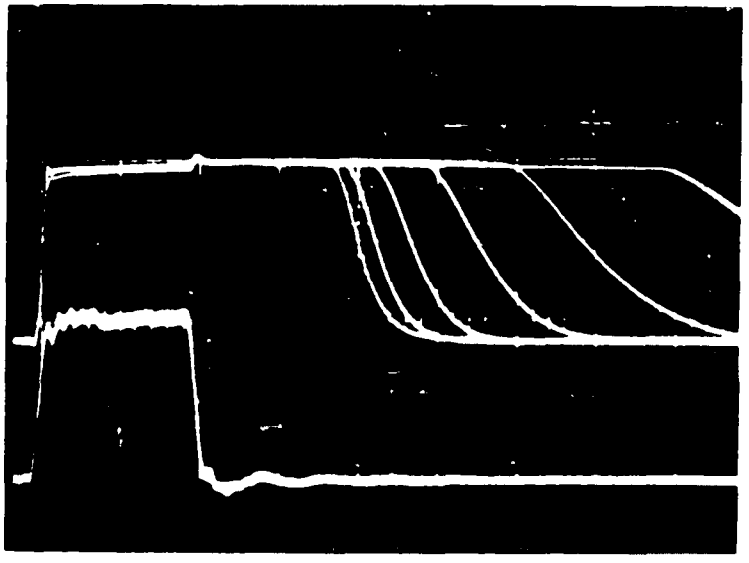

Plate 1 - Output pulse in the temperature range from 76°K to 130°K. Pulses move left with increasing temperature.

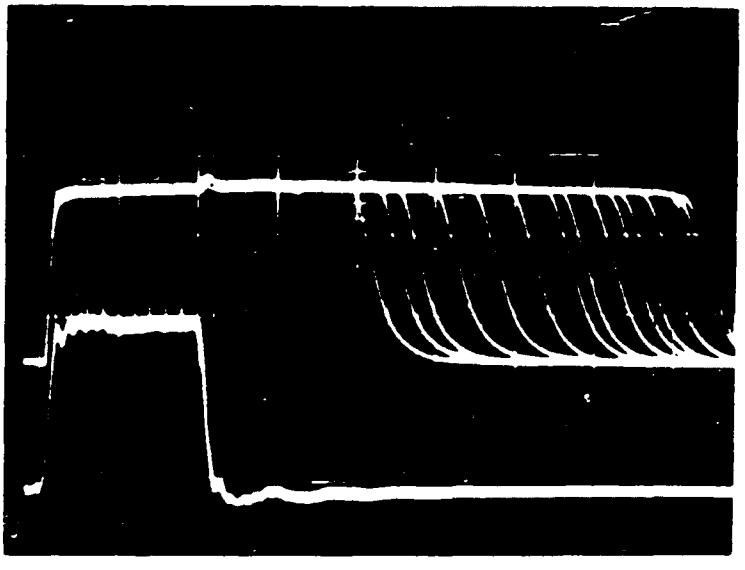

Plate 2 - Output pulse in the temperature range from 150°K to 300°K. Pulses move right with increasing temperatures.

Figure 7 - Photographs of Common Emitter Output Pulses

TABLE I

EXPERIMENTAL RESULTS COMMON EMITTER STORAGE TIME

Temperature - Degrees Kelvin	Storage Time - Microseconds
77.35	5.98
83.15	4.0
88.7	2.95
94.25	2.23
99.8	1.9
105.35	1.7
108.15	1.6
122.05	1.425
141.5	1.4
150.95	1.45
164.25	1.525
169.8	1.555
182.05	1.725
185.95	1.8
208.15	2.16
222.03	2.4
237.5	2.9
248.15	3.36
252.6	3.82
257.6	4.28
260.95	4.45
269.0	4.80
270.4	5.09
275.4	5.22
283.15	5.5
294.25	5.86
299.8	5.9
304.25	6.0

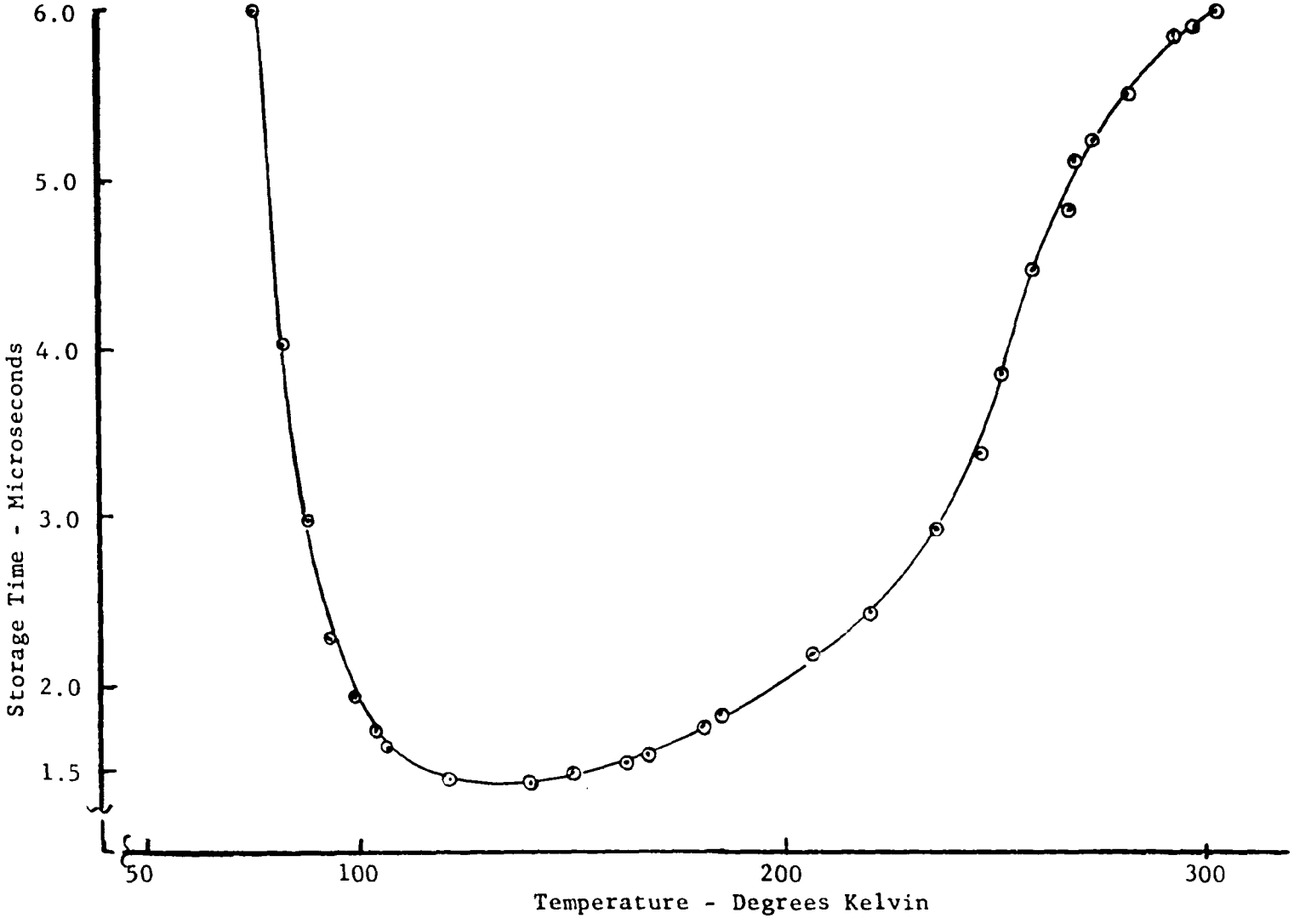

Figure 8 - Storage Time vs Temperature - Common Emitter

TABLE II

EXPERIMENTAL RESULTS COMMON BASE STORAGE TIME

Temperature - Degrees Kelvin	Storage Time - Microseconds
77.35	14.10
77.6	12.4
78.7	9.4
79.8	8.45
80.95	7.15
83.15	6.20
84.25	5.80
88.7	5.25
89.8	4.60
94.25	3.8
98.7	3.56
99.8	3.45
119.25	2.80
136.5	2.62
147.05	2.58
166.5	2.70
177.6	2.90
199.8	3.0
227.6	3.3
244.3	3.8
255.4	4.75
269.25	5.2
283.3	5.6
294.25	5.9

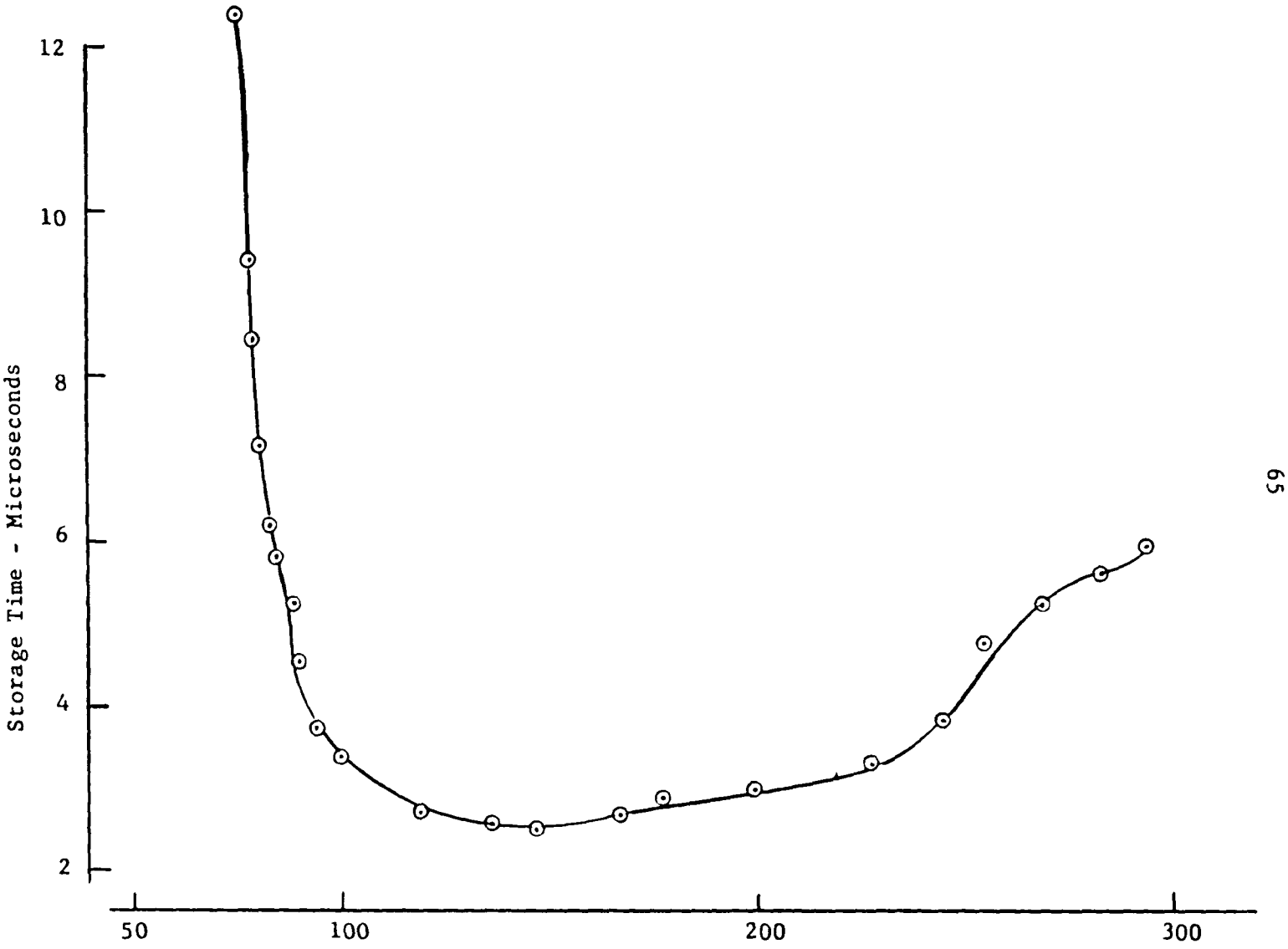

Figure 9 - Storage Time vs Temperature Common Base

$$t_s = C_1 T^{1.5} \exp\left(-E_i / kT\right) \left\{ \ln\left(C_2 T^{-1.5} \left[\frac{aT-b}{cT+d} \right] \right) \right\}$$

it would be possible to fit this function to the data quite well. There are six constants to be determined. An iterative least squares fit could be determined using a computer of the 7090 class, with a set of data points presented in successive array with respect to temperature. This expression would of course not necessarily fit if the constants were arbitrarily pre-determined. This is the case for the actual transistor since the six constants are functions of the device, doping, modulation carrier density, and geometry.

It is possible to fit the data with an expression of the form :

$$t_s = C_1 T^m \exp\left(-E_i/kT\right) + C_2 T^n \exp\left(-E_g/kT\right) + f\,(T-T_o)^2,$$

where $m = 1.8$ for $E_i = 0.5$ electron volts

$n = -1.64$ for $E_g = 0.05$ electron volts

or $m = -2.2$ for $E_i = 1.14$ electron volts

$n = -1.64$ for $E_g = 0.05$ electron volts,

with $f(T-T_o)^2$ being determined such that a fit is obtained at $T = 132^{\circ}K$, where the tangents must be matched to the other sections at $185^{\circ}K$ and $99.8^{\circ}K$. The two values of m for the high temperature end for different values of E_i are proposed as each being a possible mechanism. The value of -2.2 at 1.14 electron volts was determined using the premise that the storage time would be proportional to the Auger lifetime. This does not seem to be likely since the Auger lifetime is in essence proportional

$$t_s = C_1 T^{1.5} \exp\left(-E_i / kT\right) \left\{ \ln\left(C_2 T^{-1.5} \left[\frac{aT-b}{cT+d} \right] \right) \right\}$$

it would be possible to fit this function to the data quite well. There are six constants to be determined. An iterative least squares fit could be determined using a computer of the 7090 class, with a set of data points presented in successive array with respect to temperature. This expression would of course not necessarily fit if the constants were arbitrarily pre-determined. This is the case for the actual transistor since the six constants are functions of the device, doping, modulation carrier density, and geometry.

It is possible to fit the data with an expression of the form :

$$t_s = C_1 T^m \exp\left(-E_i/kT\right) + C_2 T^n \exp\left(-E_g/kT\right) + f\left(T-T_o\right)^2,$$

where $m = 1.8$ for $E_i = 0.5$ electron volts

$n = -1.64$ for $E_g = 0.05$ electron volts

or $m = -2.2$ for $E_i = 1.14$ electron volts

$n = -1.64$ for $E_g = 0.05$ electron volts,

with $f(T-T_o)^2$ being determined such that a fit is obtained at $T = 132^{\circ}K$, where the tangents must be matched to the other sections at $185^{\circ}K$ and $99.8^{\circ}K$. The two values of m for the high temperature end for different values of E_i are proposed as each being a possible mechanism. The value of -2.2 at 1.14 electron volts was determined using the premise that the storage time would be proportional to the Auger lifetime. This does not seem to be likely since the Auger lifetime is in essence proportional

to the square of the intrinsic carrier density multiplied by the intrinsic relaxation time. The intrinsic relaxation time is proportional to the mobility. This should give a positive exponent on T of value 1.0 to 2.0. The 1.8 exponent at an activation energy of 0.5 electron volts would tend to support a scattering caused by a sea of ionized carriers in which the relaxation time would be proportional to the electron density.

Other Parameters

After determining that an anomaly did exist in the value of storage time at lowered temperatures, and after consideration of the possible scattering processes was not revealing in determination of the transition temperature, it was decided that other parameters might yield information concerning the transition point.

From the model and technique determined by Nanavati, it was apparent that any deviation in the small signal parameters would show up as a deviation of the storage time. Credle has measured the small signal parameters for micro-alloy germanium transistors as a function of temperature down to 76^{o}K, but it has been determined by previous measurements that the micro-alloy transition temperature is in the liquid hydrogen range.

The small signal "y" parameters for the transistor were measured as the temperature was varied from 76^{o}K to 300^{o}K. The frequency used for these measurements was 1000 cycles per second which was determined by the bridge used. The results are plotted in figures 10 through 13.

Figure 10 is a plot of the variation in the small signal input conductance parameter "y_{11}" as a function of temperature over the temperature interval from 76°K to 300°K. Table III presents this data in tabular form. This curve shows good agreement with theoretical predictions. Modification of the input spreading conductance equation as derived in chapter IV to include the variation of the unmodulated carrier density with temperature gives an expression of the form:

$$G(t) = G_o + M(T)\ I_B\ (1-\exp -t/\tau_s)$$

where $M(T) = M_o T^{-1.5} \exp(-E_i/kT)$

and $\tau_s = \tau_o T^{-1.5}$

Since y_{11} is proportional to the conductance term it is normal to expect a continual decrease in the value as T increases. No deviation which would account for the dramatic and abrupt change in the value of storage time is noted for this parameter.

The short circuit small signal reverse transfer ratio "y_{12}" is plotted as a temperature function in figure 11. Tabulated values for this measurement are presented in table IV. This parameter attains a maximum and relatively constant value in the 160 to 220 degree range, with smaller values on either side of this range. This is the same type of measurement reported by Credle for the case of three different assumed lifetimes. This parameter is rather difficult of calculation, since it is proportional to the base to collector transfer efficiency, to the bulk resistivity of the base and emitter blocks, and to the relative gap potentials at the junctions. No abrupt change which might account for the variation in storage time is noted.

TABLE III

EXPERIMENTAL RESULTS SMALL SIGNAL INPUT CONDUCTANCE

Temperature - Degrees Kelvin	Conductance "y_{11}" - Millimhos
77.45	8.547
83.15	8.264
88.15	8.130
95.9	7.407
99.8	7.143
105.35	6.944
114.25	5.917
117.03	5.618
121.5	5.155
127.6	4.717
133.15	4.219
138.7	3.597
144.25	3.344
149.8	2.849
155.4	2.646
160.92	2.410
165.4	2.193
172.05	2.004
177.6	1.905
182.6	1.748
184.8	1.626
185.95	1.600
188.7	1.538
199.8	1.272
210.9	1.093
222.1	0.870
233.15	0.725
244.25	0.606
255.35	0.538
265.9	0.476
279.8	0.418
288.7	0.388
299.8	0.357
294.8	0.372

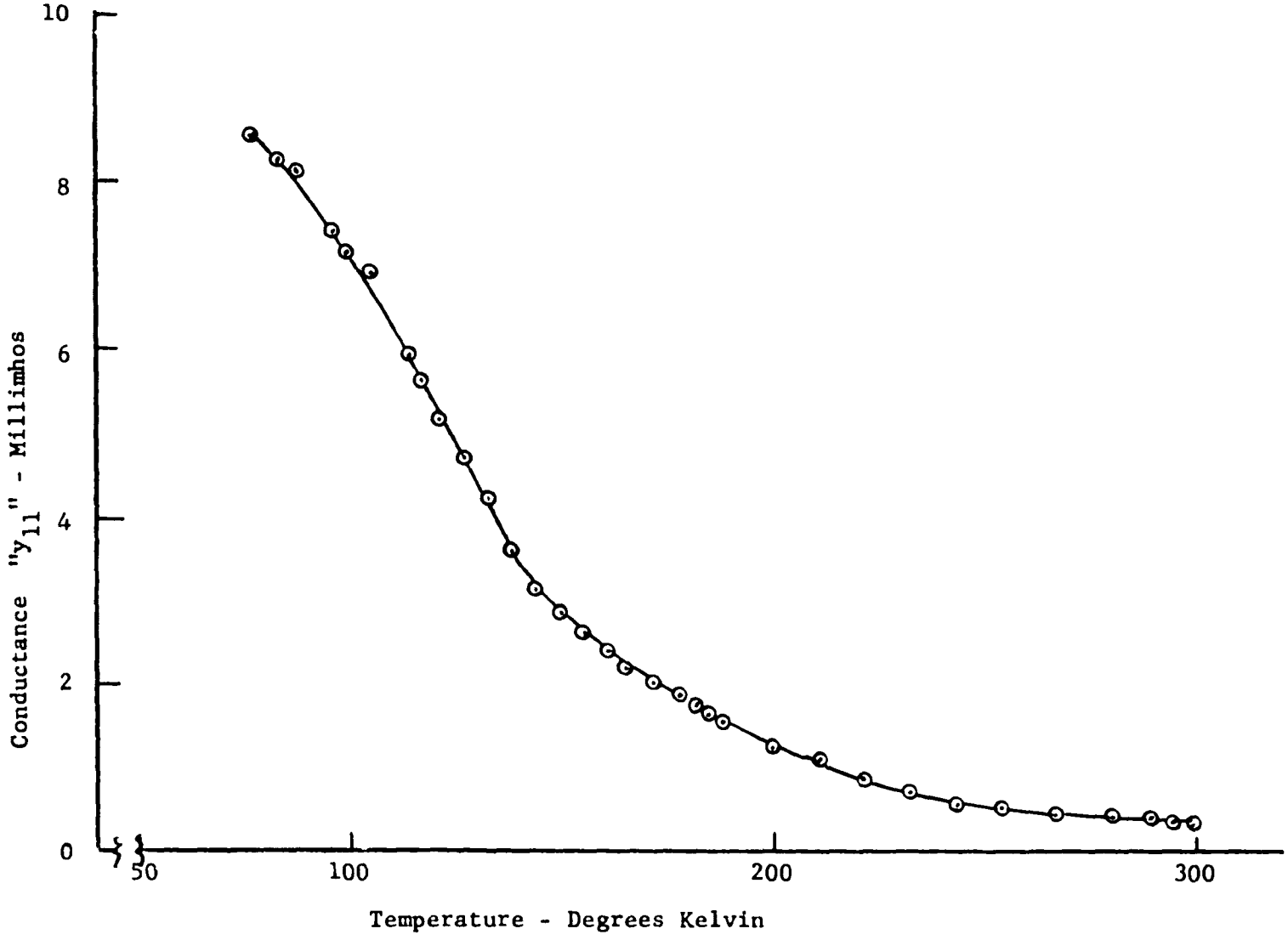

Figure 10 Small Signal Input Conductance "y_{11}" vs Temperature

TABLE IV

EXPERIMENTAL RESULTS SMALL SIGNAL REVERSE CONDUCTANCE

Temperature - Degrees Kelvin	Reverse Conductance "y_{12}" Micromhos
77.6	0.262
88.7	0.251
117.6	0.280
129.25	0.300
145.95	0.341
158.7	0.360
176.5	0.365
184.8	0.361
200.95	0.366
215.4	0.357
225.95	0.352
247.6	0.320
255.95	0.310
266.5	0.290
281.5	0.270
293.7	0.250
295.4	0.250

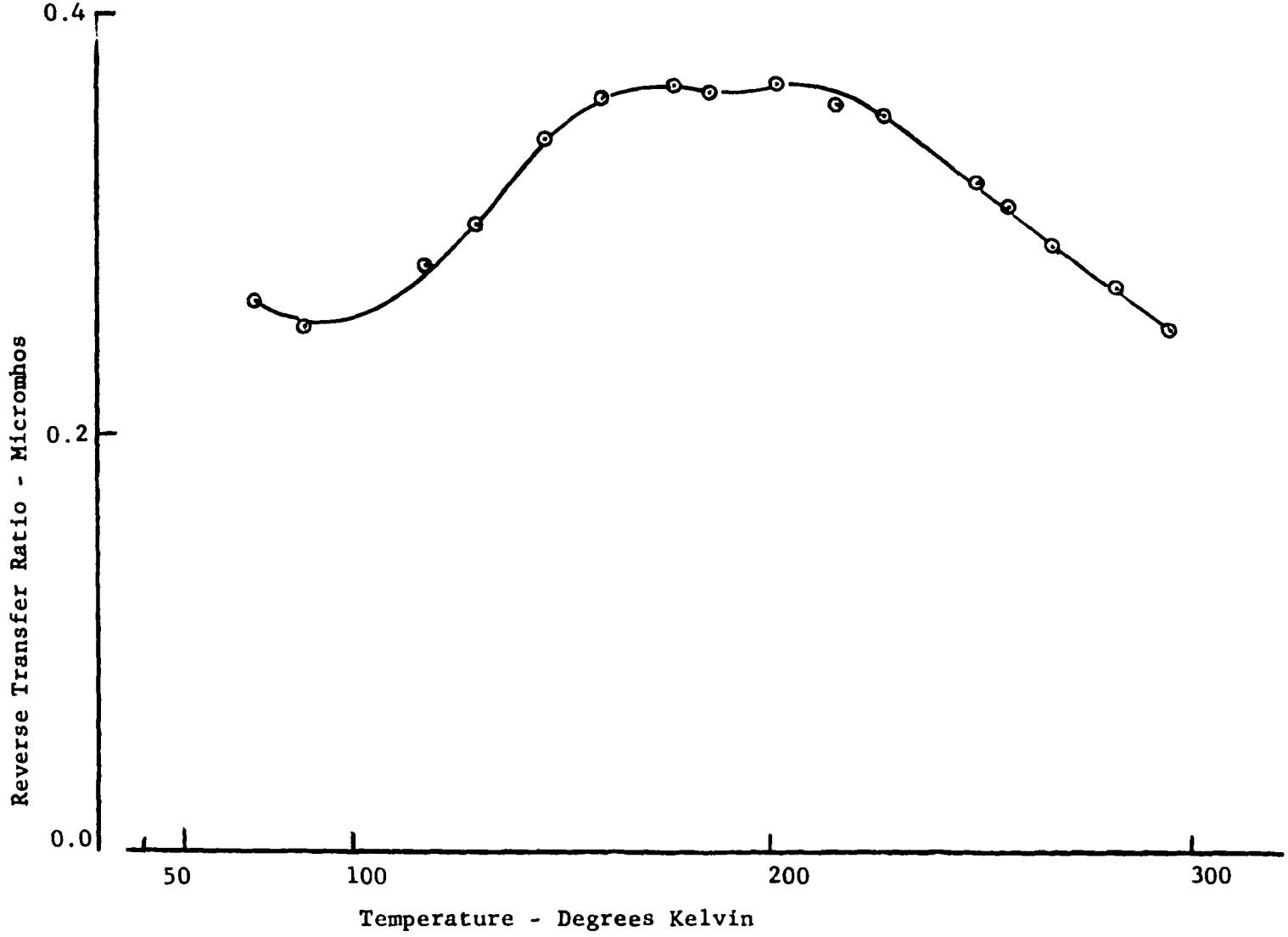

Figure 11 Short Circuit Reverse Transfer Ratio "y_{12}" vs Temperature

The short circuit forward conductance "y_{21}" is presented as a plotted function of temperature in figure 12. Data for this plot is tabulated in table V. The parameter is generally considered as a function of the emitter current, being equal to some KI_E term. Since the measurements conducted in these tests were carried out at a constant value of collector current because of the bridge arrangement, this value was expected to decrease as the required emitter current increased. The emitter current required to maintain the collector at a constant value is proportional to the emitter to collector efficiency in the following manner:

$$I_E = \frac{I_C}{\alpha}$$

where α = the product of the emitter to base efficiency, the base transport ratio, and the collector to base efficiency by far the largest temperature variable term is the emitter base efficiency. This factor is proportional to the lattice mobility, and causes α to change as the negative three-halves power of the temperature. The collector efficiency is inversely proportional to the breakdown voltage and therefore increases slightly due to the reduction of thermal electrons in the conduction band. No major deviations which might account for the transition temperature are noted in this parameter.

Figure 13 is a representation of the short circuit output conductance as the temperature varies. This parameter varies in much the same manner as the real part of the output conductance as measured

TABLE V

EXPERIMENTAL RESULTS SMALL SIGNAL FORWARD CONDUCTANCE

Temperature - Degrees Kelvin	Conductance "y_{21}" Millimhos
77.35	34.3
81.5	34.9
86.5	34.9
86.5	34.7
88.7	34.6
90.4	34.4
94.8	33.2
105.9	31.0
112.6	27.5
119.25	25.4
138.15	20.6
144.8	19.0
160.95	16.1
167.6	14.6
174.8	14.4
181.5	13.9
192.05	12.4
208.7	12.2
213.7	11.9
226.5	11.4
235.9	10.9
255.35	10.4
261.5	10.3
273.0	9.83
284.8	9.49
294.8	8.95

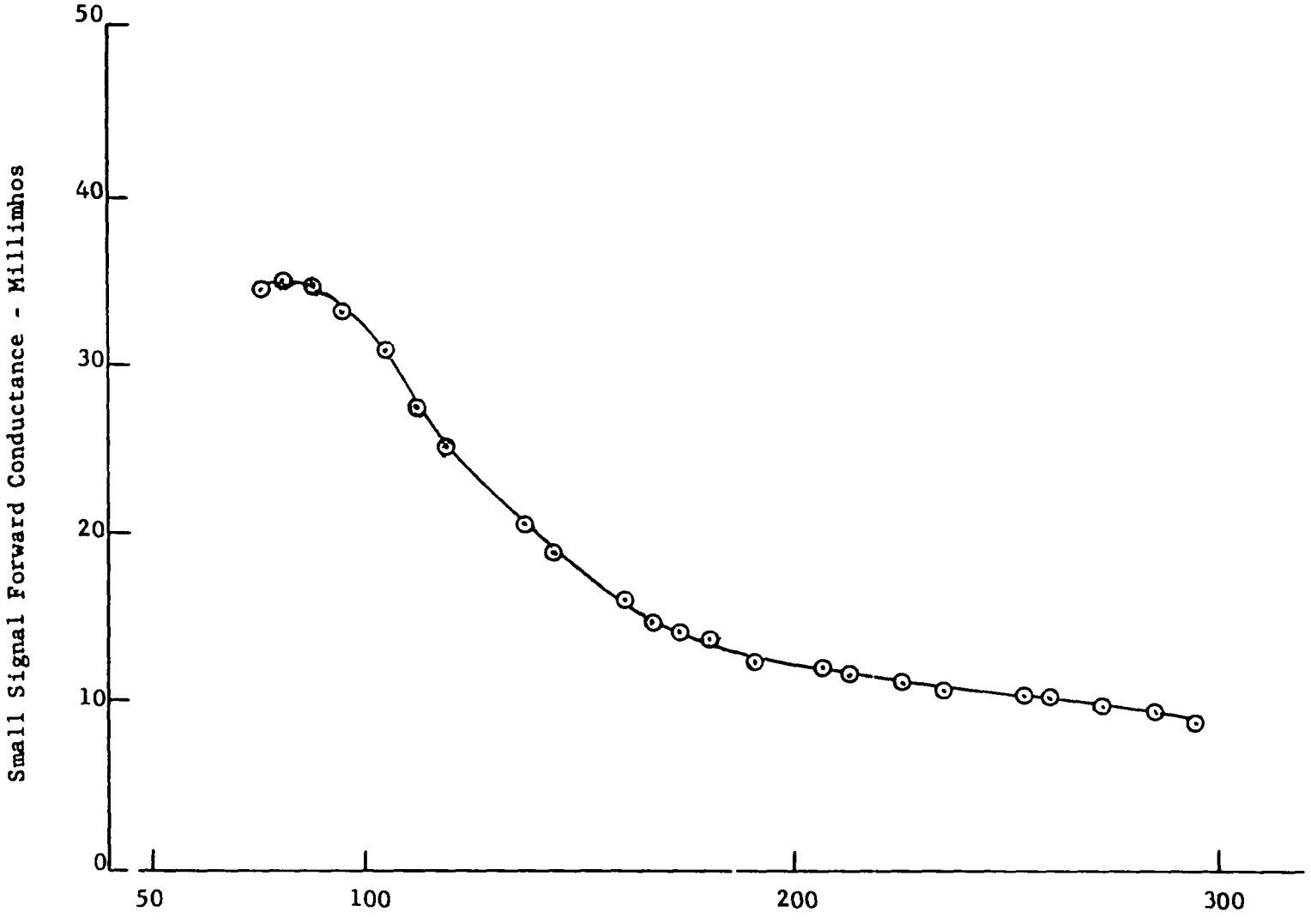

Figure 12 - Small Signal Forward Conductance vs Temperature

TABLE VI

EXPERIMENTAL RESULTS SMALL SIGNAL OUTPUT CONDUCTANCE

Temperature - Degrees Kelvin	Conductance "y_{22}" Mhos
77.35	1.515
77.6	1.613
80.95	1.761
85.4	1.887
85.95	1.953
102.05	2.326
108.7	2.439
116.5	2.632
127.6	2.703
144.25	2.857
154.25	2.941
167.05	2.857
175.35	2.778
187.6	2.857
205.14	2.703
219.8	2.778
233.15	2.778
252.04	2.941
268.15	3.030
275.35	3.096
282.6	3.125
293.15	3.226

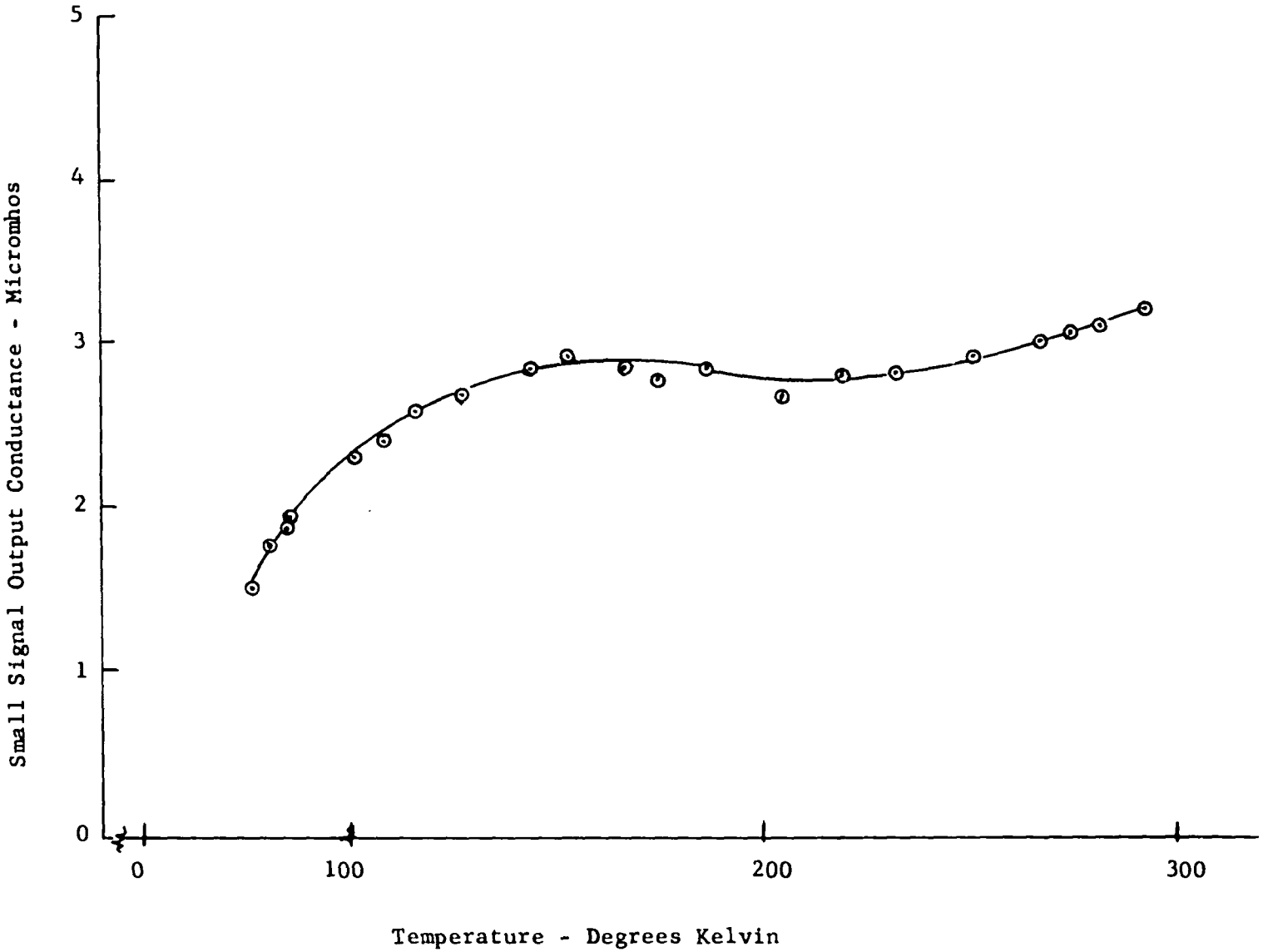

Figure 13 - Small Signal Output Conductance vs Temperature

by Credle. The greater slope at lowered temperatures is a function of the larger bulk resistivity due to the reduction in conduction electrons in the n type collector.

The y parameters for this transistor vary in accordance with predictions based on simple classical theory. Normal operation is experienced throughout the temperature band. From these measurements it is possible to state that the transistor could be used as a standard small signal amplifying element at liquid nitrogen temperatures. Difficulties are expected in attempts to stabilize the operating point and the current gain for wide ranges of temperature in this region, but from measurements on h_{fe} it is noted that an operating region from about $77^{o}K$ to $180^{o}K$ could be used with good results on stability if a suitable resistance is used in the feedback path from collector to base. The measurements on h_{fe} are presented in tabular form in table VII, and plotted as a function of temperature in figure 14. The current transfer ration h_{fe} is essentially a function of majority carriers in the emitter and collector regions, and the decreased value as the temperature is decreased is therefore as expected. The decrease in current transfer will yield a considerable decrease in the current gain as the temperature decreases. This will be partially offset by the decrease in the input impedance and in the output conductance terms.

It should also be noted that if the emitter current could be kept at a relatively constant value then a constant voltage amplifier could be designed to operate over the temperature range of interest. This can be accomplished by proper thermistor feedback elements.

TABLE VII

EXPERIMENTAL RESULTS SMALL SIGNAL CURRENT TRANSFER

Temperature - Degrees Kelvin	Current Transfer Ratio "h_{fe}"
77.45	3.4
83.15	3.52
88.15	3.55
95.9	3.68
99.8	3.79
105.35	3.73
114.25	3.97
117.03	4.00
121.5	4.17
127.6	4.24
133.15	4.34
138.7	4.59
144.25	4.72
149.8	5.00
155.4	5.05
160.92	5.26
165.4	5.52
172.05	5.74
177.6	5.88
182.6	6.10
184.8	6.25
185.95	6.41
188.7	6.58
199.8	7.14
210.9	8.06
222.1	9.09
233.15	11.11
244.25	12.20
255.35	12.82
265.9	14.29
279.8	14.71
288.7	15.63
299.8	16.67

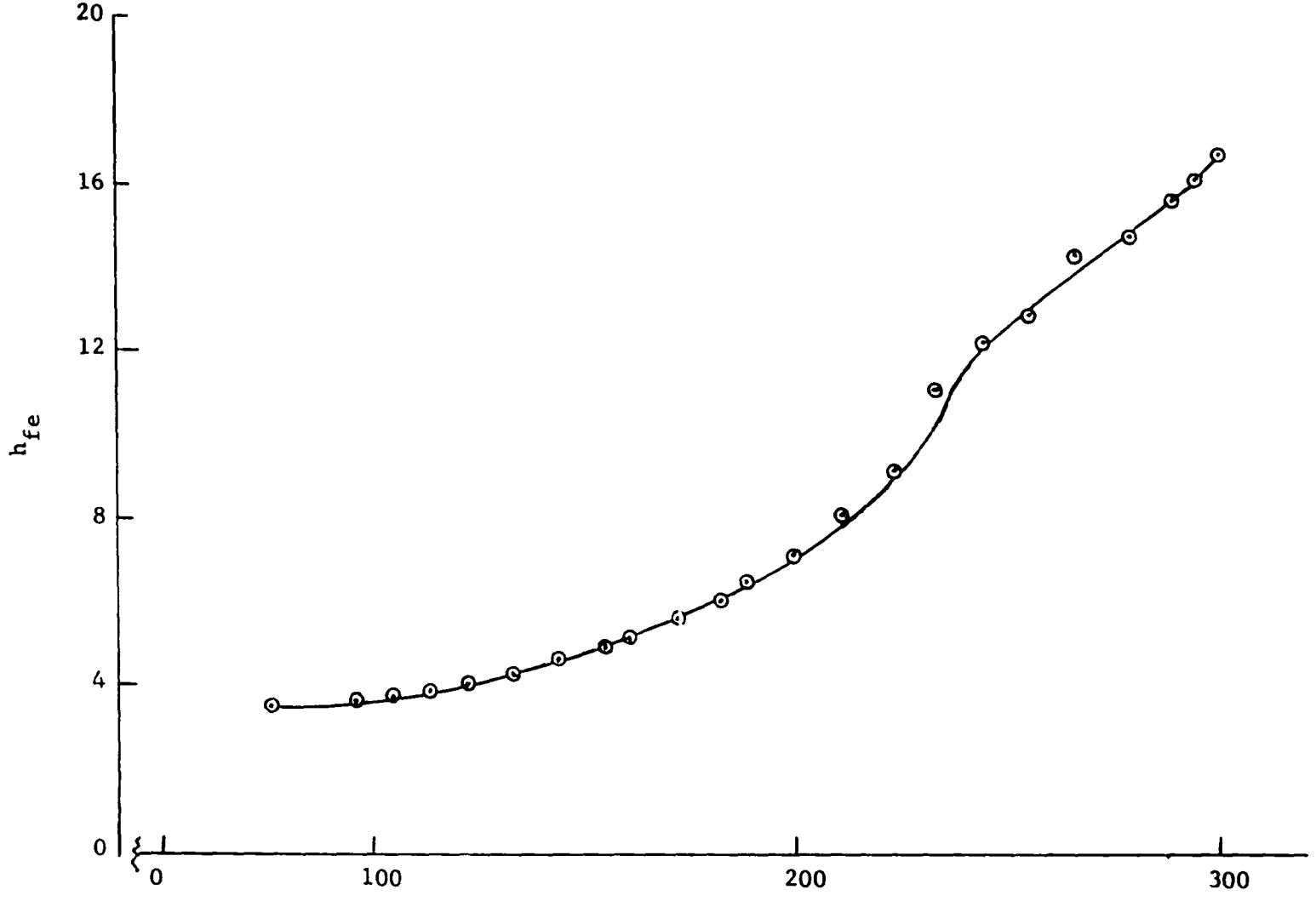

Figure 14 - Small Signal Current Transfer vs Temperature

Base Charge Measurement

The small signal measurements have revealed no sudden or abrupt change in the normal transistor operation in the active region. Since the storage time is the amount of time required for the charge stored in the base to emitter junction region to become depleted through the external circuit so that the base becomes a non-conducting system, a measurement of the amount of charge required for the transistor to become saturated was carried through. Base saturation charge is plotted as a function of temperature in figure 15. The data on the capacitance in series and the calculated value of charge is tabulated in table VIII. The amount of charge required for saturation at low temperatures shows a marked correspondence to the storage time. This is as expected, but a careful consideration of the expected value of charge does not support this result any more than the expected variation in storage time was met by classical considerations. If the charge is assumed as a non time variant quantity at saturation, then the charge will be proportional to the product of the voltage at saturation and the base to emitter capacitance.

The capacitance of a semiconducting junction is a function of the voltage applied, so the charge becomes a function of the saturated voltage. This function is generally expressed as:

$$C_{BE} = K \left(V_{BE(Sat.)} \right)^{1.5}$$

In order to check this expression it was necessary to determine the variation of $V_{BE(Sat.)}$ as the temperature was changed. This value

TABLE VIII

EXPERIMENTAL AND CALCULATED VALUES FOR BASE CHARGE DATA

Temperature ^{o}K	Series Capacitance $\mu\mu f$	Charge μ-coulombs
77.35	371.7	5110
83.15	301.8	4140
88.7	230.6	3160
94.25	206.0	2830
99.8	179.5	2460
105.35	164.3	2250
116.5	136.6	1870
130.4	112.9	1540
139.25	90.2	1230
162.05	77.5	1050
182.05	76.5	1040
199.8	73.0	988
216.5	61.0	824
230.4	79.0	1070
237.6	90.0	1210
244.25	96.8	1300
255.4	113.8	1530
266.5	136.4	1830
290.4	167.5	2240
296.5	174.1	2330

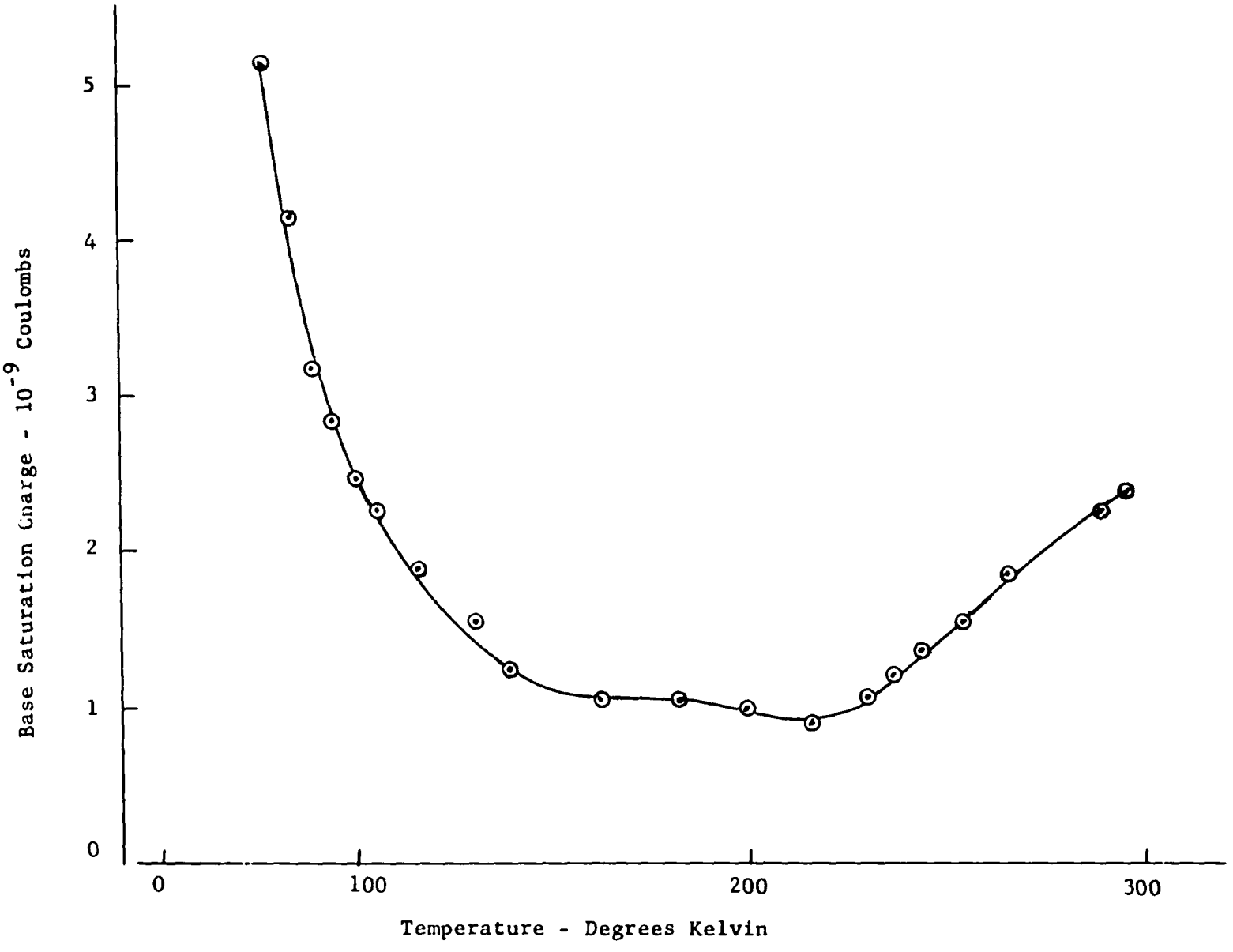

Figure 15 - Saturation Base Charge vs Temperature

was checked by measurement of the input and output volt-ampere characteristics of the transistor with a type 575 curve tracer as the temperature was changed. Photographic records were taken of these curves, and the data as abstracted is tabulated in table IX. This data is plotted as a function of temperature in figures 16,17,18.

The saturated value of base to emitter voltage was found to vary as follows:

$$V_{BE(Sat.)} = mT + B$$

where

$$B = 1.13 \text{ volts}$$

$$m = -1.36\ (10)^{-3} \text{ volt} - {}^{o}K^{-1}$$

If this expression is inserted into the equation previously stated for Q_s, and the derivative is taken and set equal to zero, a slope equal to zero will be found which should occur at $T = 837^{o}K$. This temperature is found to correspond to a relative maximum for the equation and is obviously meaningless.

In light of this data, it has been concluded that some other process has occurred which changes C_{BE} as a function of temperature independent of the applied voltage. Such processes can also be accounted for as an impurity scattering change on the relaxation time, which is not inconsistent with the storage time results.

From the static characteristic curves used to obtain the saturated value of base to emitter voltage, the curves of saturation base current and saturation beta (current transfer ratio at saturation) were also plotted. The results as plotted are expected and are predictable from classic equations shown by Shockley.

TABLE IX

SATURATION DATA FROM STATIC CHARACTERISTICS

Temperature ^{o}K	Base Current Milliamperes	Base Voltage Volts	Beta -
77.35	2.4	1.036	3
88.7	2.0	1.0	4
116.5	1.6	0.95	5
144.5	1.3	0.92	6
172.05	1.04	0.87	8
199.8	0.82	0.83	9.5
233.1	0.475	0.77	20
255.4	0.338	0.72	35
293.7	0.25	0.67	44

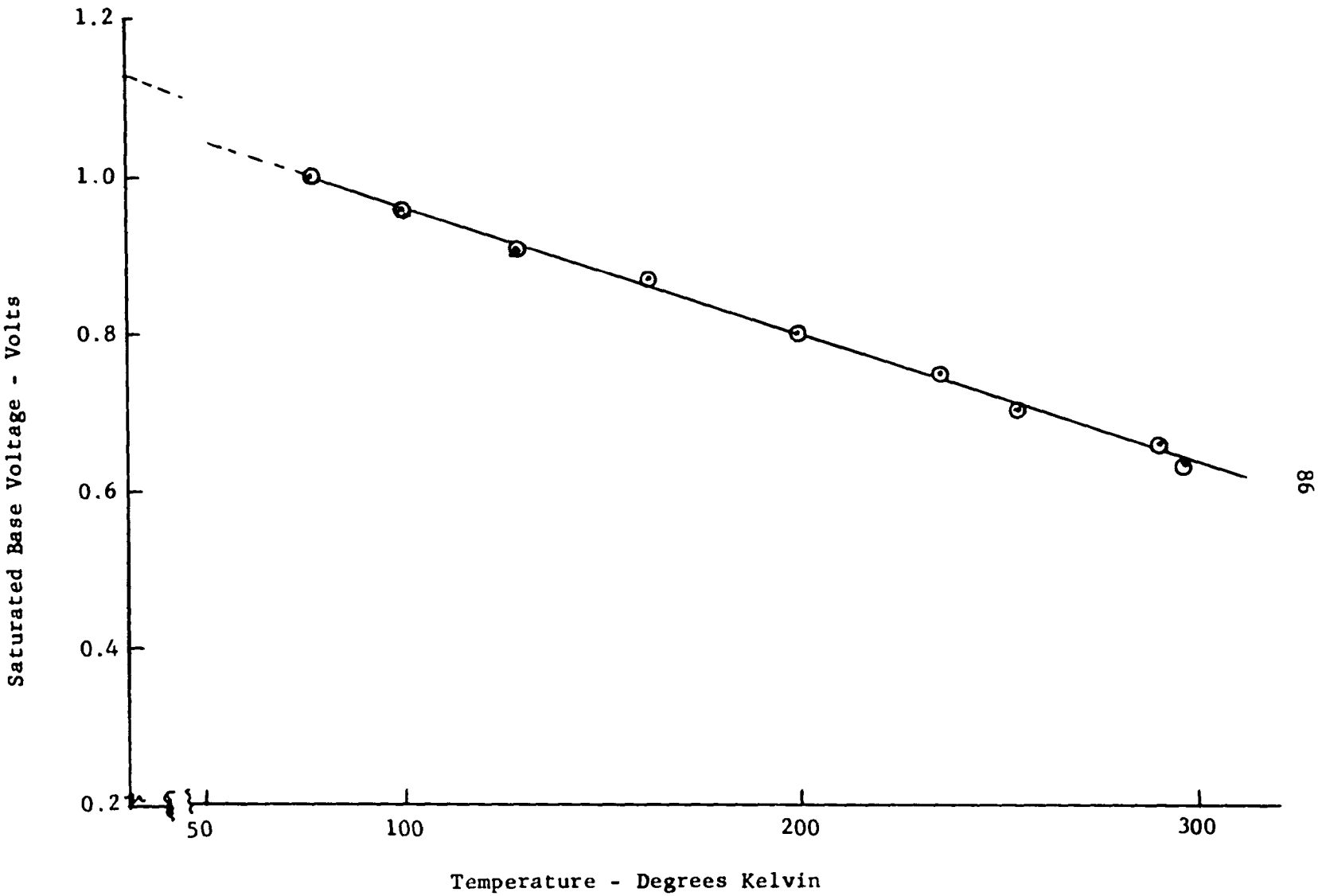

Figure 16 - Saturation Base Voltage vs Temperature

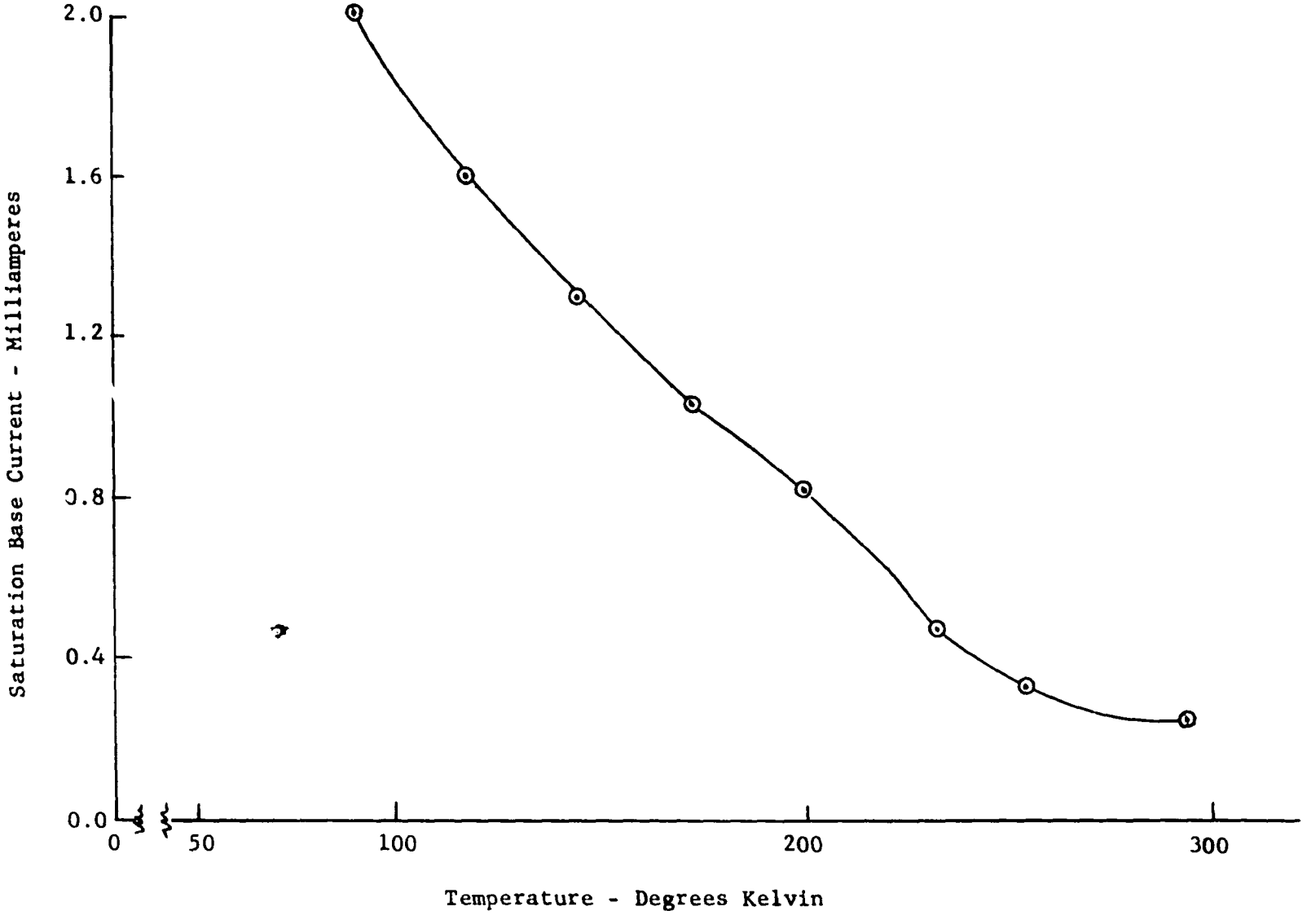

Figure 17 - Saturation Base Current vs Temperature

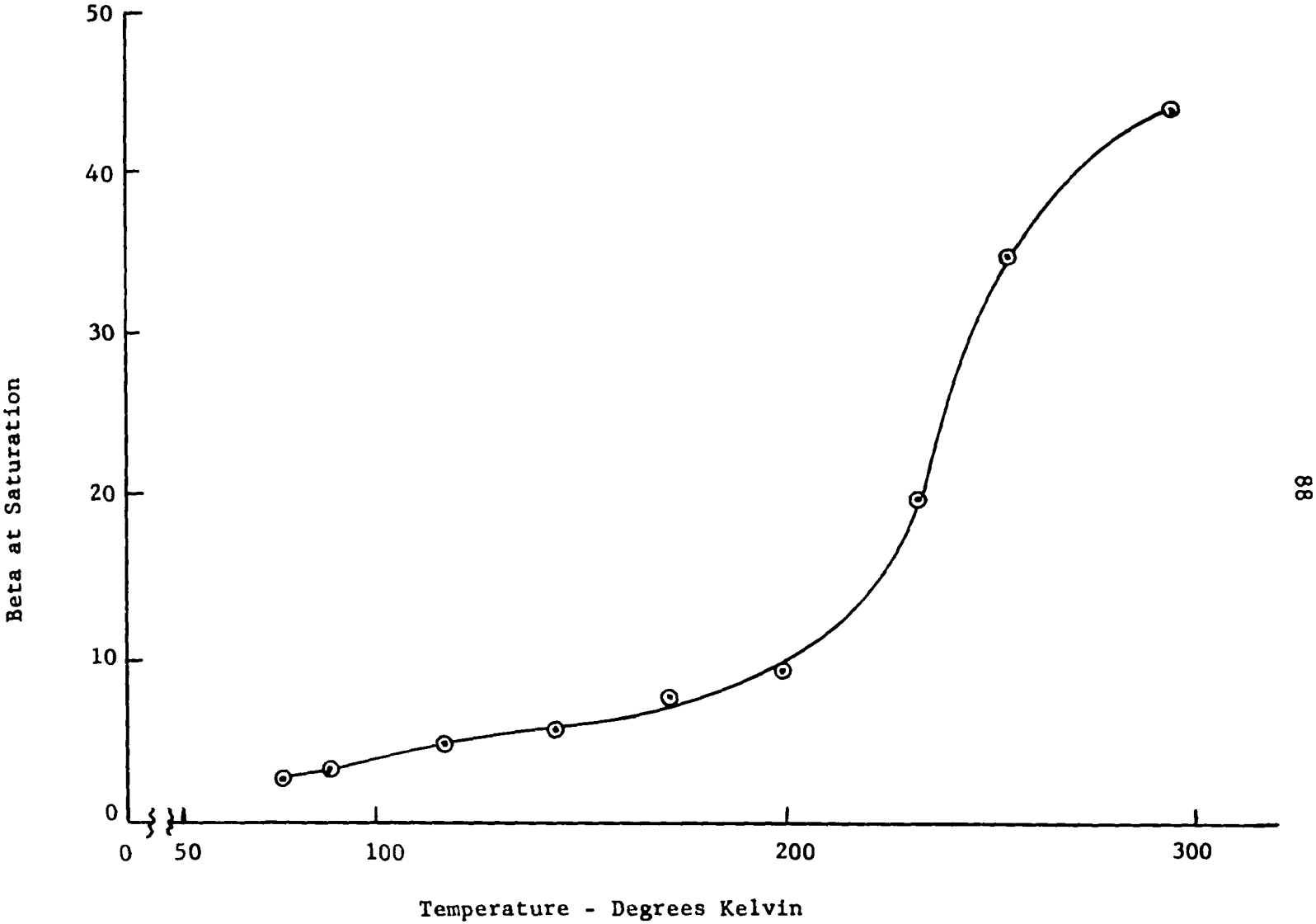

Figure 18 - Saturation Charge Transfer vs Temperature

CHAPTER VII

CONCLUSIONS AND RECOMMENDATIONS

The storage time for silicon transistors has been measured as a function of temperature. Several transistor types have been observed, and detailed measurements carried out on one particular type. The one chosen was a grown junction transistor of relatively low current gain, large physical size and with a high value of storage time at ambient room temperatures. Classical theory, as developed for switching states, would seem to indicate that over the operating range of the device the storage time should decrease with temperature decrease. An anomalous behavior has been noted in all transistor types tested. At some value of lowered temperature the storage time suddenly increases at a high rate with temperature decrease.

A theoretical approach has been carried out to indicate that if all terms are included with their proper temperature dependence, the storage time should correspond to a function of the form:

$$t_s = C_1 T^{1.5} \exp\left(-E_i/kT\right) \left(\ln C_2 T^{-1.5} \left[\frac{aT-b}{cT+d}\right] \right).$$

While this function is capable of being fitted to measured data, it does not adequately account for the sudden increase if the six constants are functions of the transistor dimensions and currents applied.

Other parameters of the transistor have been investigated, and only one parameter, the saturated base charge, has been found to vary in a manner which might give rise to this phenomenon. The variation of this charge with temperature as determined by classical theory, is also seriously violated by the measured results.

One existing theory which has previously been applied to germanium single crystal conductivity measurements shows promise as a possible explanation of the effect measured. Hung has postulated a theory of impurity center conduction at low temperatures to account for the sharp rise in conductivity at extremely low temperatures. This theory has encountered some opposition, and has been explained as more probably due to tunnelling, Rutherford scattering, or breakdown phenomena by various other experimenters. It must be stated that the theory of Hung is based on strictly empirical considerations, and does seem to correlate the data obtained for various measurements. One drawback to the application of this theory for the present case, is the conventional conductivity change measured for the transistor.

It is concluded that an impurity center recombination process is set up at low temperatures. This conclusion is based solely upon an empirical fit to the curve of storage time as a function of temperature in the anomalous region. For the transistors tested a fit to the curve was obtained using the exponent on T as 1.64 at an activation energy of 0.05 electron volts. This corresponds to the case of an n type semiconductor with a k center or band edge located off the 000 point, and an impurity gap energy of 0.05 electron volts as

reported by Johnson and Horovitz.

It has not been possible at this time to determine specific causes for the value of the transition temperatures. Quantitative measurements on different transistors seem to indicate that the relative cross-sectional area of the base-emitter junction, and the doping level of the emitter region are contributing factors to the transition temperature value. This is consistent with the impurity conduction theory, since for lightly doped emitters with large areas compared to the base effective area, the transition temperature is decreased. For these conditions the density of impurity centers is decreased and lower temperatures would be required before impurity center scattering commences to dominate.

The small signal parameter measurements carried out in the course of this research verify the contention that no good reason should exist for the avoidance of cryogenic cooling of transistor circuitry in order to increase the power handling capability per unit volume. Since extremely low ambient temperatures are experienced on the dark side of space probes, and are expected on the dark and in the twilight regions of immediately forseeable planetary stations, it would seem that advantage should be taken of this natural cooling region to package higher power systems in smaller volumes. Some degradation of current gain is inevitable, but for many sensing and transmitting applications a stable voltage gain and proper matching circuitry is adequate. In addition the use of dimensionally smaller transistors will yield an increase in the upper frequency limit.

It is recommended that a program of study should be instituted to determine if Hung's theory of impurity center conduction is applicable to scattering processes. On the basis of data measured during this program such a possibility is highly probable. In addition a major program of both experimental research and numerical analysis could be undertaken to determine the factors in transistor construction which would give optimum design for low temperature transistors. On the basis of the work done this would seem to be some function of both transistor geometry and relative doping level. While such a program is beyond the capability of equipment available to the author at the present time, it is probable that such a program will be initiated. The basis for this statement is evident when one considers the growing number of research laboratories working on micro-electronic systems.

ANOTATED BIBLIOGRAPHY

1. Blakemore, J. S. "Semiconductor Statistics", Pergamon Press, N Y., 1962.

2. Credle, A. B., "Effects of Low Temperatures on Transistor Characteristics", IBM Journal, January 1958.

3. Debye, P. P., E. M. Conwell, "Electrical Properties of N-Type Germanium", Physical Review, Vol. 93, February 1954.

4. Debye, P. P., T. Kohane, "Hall Mobility of Electrons and Holes in Silicon", Physical Review, Vol. 94, May 1954.

5. Ebers, J. J., J. L. Moll, "Large-Signal Behavior of Junction Transistors", Proceedings of the I.R.E., Vol. 42, December 1954.

6. Fritzsche, H., "Electrical Properties of Germanium Semiconductors at Low Temperatures", Physical Review, Vol. 99, July 1955.

7. Gariano, W. F., "Transient Analysis of Junction Transistors", I.R.E. Transactions on Electron Devices, Vol. ED-6, January 1959.

8. Hickmott, J. T., "Notes on Transistor Circuits for Lowered Temperatures", Project Michigan Report No. 2144-360-T, ASTIA AD 211818.

9. Hoffmann, John, (Personal Communication), Electronics and Telemetry Division, Gemini Project, NASA Manned Space Center, Houston, Texas.

10. Hung, C. S., J. R. Gliessmann, "Resistivity and Hall Effect of Germanium at Low Temperatures", Physical Review, Vol. 96, December 1954.

11. Johnson, V. A., K. Lark-Horovitz, "Semiconductors at Low Temperatures", Progress in Low Temperature Physics, Vol. II, North-Holland Publishing Company, Amsterdam, Holland.

12. Lin, H. C., W. F. Jordan, "Effect of Transient Voltages on Transistors", I.R.E. Transactions on Electron Devices, Vol. ED-6, January 1959.

13. Nanavati, R. P., "Prediction of Storage Time in Junction Transistors", I.R.E. Transactions on Electron Devices, Vol.ED-7, January 1960.

14. Scalar, N. E. Burstein, W. J. Turner, and J. W. Davisson, "Low Temperature "Breakdown" Effect in Germanium," Physical Review, Vol. 91, p. 215, 1953.

15. Shockley, W., "Electrons and Holes and Semiconductors", D. Van Nostrand Company, Inc., Princeton, New Jersey. 1950.

16. Wiencek, Z., "An Analysis and Representation of Junction Transistors in the Saturation State", I.R.E. Transactions on Electron Devices, Vol. ED-8, January 1961.

References Not Specifically Noted in the Text

Books

Bremer, J. W., "Superconductive Devices," McGraw Hill Book Company, New York, 1962.

Brillouin, L., "Wave Propagation in Periodic Structures," Dover Publications, Inc., 1953.

Dekker, A. J., "Solid State Physics," Prentice Hall, Inc., Englewood, Cliffs, New Jersey, 1957.

Gartner, W. W., "Transistors: Principles, Design and Application," D. Van Nostrand Company, Inc., Princeton, New Jersey, 1960.

Hannay, N. B., "Semiconductors," Reinhold Publishing Corporation, New York, 1959.

Kittel, C., "Introduction to Solid State Physics - Second Edition," John Wiley and Sons, Inc., New York, 1956.

Mariot, L., "Group Theory and Solid State Physics," Prentice-Hall, Englewood Cliffs, New Jersey, 1962.

Middlebrook, R. D., "An Introduction to Junction Transistor Theory," John Wiley and Sons, Inc., New York, 1958.

Mott, N. F. and H. Jones, "The Theory of the Properties of Metals and Alloys," Oxford University Press, New York, 1936.

Mott, N. F., "Elements of Wave Mechanics," Cambridge University Press, 1958.

Nussbaum, A., "Semiconductor Device Physics," Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1962.

Seitz, F., "The Modern Theory of Solids," McGraw Hill Book Company, New York, 1940.

Spenke, E., "Electronic Semiconductors," McGraw Hill Book Company, New York, 1958.

Van Der Ziel, A., "Solid State Physical Electronics," Prentice-Hall, Inc. Englewood Cliffs, New Jersey, 1957.

White, G. K., "Experimental Techniques in Low Temperature Physics," Oxford at the Clarendon Press, 1959.

Articles

Aigrain, P., "Mesures de durée de vie des porteurs minoritaires dans les semiconducteurs," Ann. Radioelectrique 9, 291-226, July, 1954.

Bemski, G., "Lifetime of Electrons in p type Silicon," Physical Review 100, 523-524, October, 1955.

Bemski, G., "Recombination in Semiconductors," Proceedings of the I.R.E. Vol. 46, June, 1958.

Brooks, H., "Scattering by Ionized Impurities in Semiconductors," Physical Review 83, 879(A), 15 August, 1951.

Chih-Tang Sah, "Effect of Surface Recombination and Channel on P-N Junction and Transistor Characteristics," I.R.E. Transactions on Electron Devices, Vol. ED-9, January, 1962.

Chynoweth, A. G., and K. G. McKay, "Threshold Energy for Electron-Hole Pair Production by Electrons in Silicon," Physical Review 106, 418, 1957.

Chynoweth, A. G., "Internal Field Emission," Progress in Semiconductors Vol. 4, John Wiley and Sons, New York, 1960.

Conwell, E. M. and V. F. Weisskopf, "Theory of Impurity Scattering in Semiconductors," Physical Review 77, 388, - 1 February, 1950.

Conwell, E. M., "Properties of Silicon and Germanium," Proceedings of the I. R. E., Vol. 46, June, 1958.

Early, J. M., "Effect of Space Charge Layer Widening in Junction Transistors," Proceedings of the I.R.E., Vol. 40, November, 1952.

Early, J. M., "Design Theory of Junction Transistors," Bell System Technical Journal, Vol. 32, November, 1953.

Fan, H. Y., "Effect of Traps on Carrier Injection in Semiconductors," Physical Review, Vol. 92, December, 1953.

Fritzsche, H., "Resistivity and Hall Coefficient of Antimony Doped Germanium at Low Temperatures," Journal Physical Chemistry Solids, Vol. 6, 1958.

Goldstein, S, Mette H. and W. W. Gartner, "Carrier Recombination in Germanium as a Function of Temperature Between 100°K and 550°K," Journal Physical Chemistry Solids 8, 78 - 1959.

Hall, R. N., "Electron-Hole Recombination in Germanium," Physical Review 87, 387 - 15 July, 1952.

Hall, R. N., "Tunnel Diodes," I.R.E. Transactions on Electron Devices, Vol. ED-7, January, 1960.

Herring, C., "Theory of Transient Phenomena in the Transport of Holes in an Excess Semiconductor," Bell System Technical Journal 28, 401 1949.

Huaang, C., "A Physical Theory of Junction Transistors in the Collector-Voltage-Saturation Region," I.R.E. Transactions on Electron Devices, Vol. ED-6, April, 1959.

Lin, H. C., W. F. Jordan, "Effect of Transient Voltages on Transistors," I.R.E. Transactions on Electron Devices, Vol. ED-6, January, 1959.

Longini, R. L., "The Tunneling P-N Junction," I.R.E. Transactions on Electron Devices, Vol. ED-9, January, 1962.

Moll, J. L., "Large Signal Transient Response of Junction Transistors," Proceedings of the I.R.E., Vol. 42, December, 1954.

Parkinson, D. H., "Infrared Spectroscoping and Low Temperatures," Cryogenics, Vol. 3, No. 1, March, 1963.

Shockley, W., "Electrons and Holes and Semiconductors," D. Van Nostrand Company, Inc., Princeton, New Jersey, 1950.

Shockley, W., and W. T. Read, Jr., "Statistics of the Recombination of Holes and Electrons," Physical Review 87, 835 - 1 September, 1952.

Wolff, P. A., "Electron Multiplication in Silicon and Germanium," Physical Review 95, 1415 - 15 September, 1954.