DESIGN AND IMPLEMENTATION OF A LOW POWER T-GATE CELL LIBRARY AND COMPARISON WITH ITS CMOS EQUIVALENT

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2010

Submitted to the Faculty of the
Graduate College of the
Oklahoma State University
in partial fulfillment of
the requirements for
the Degree of
MASTER OF SCIENCE
December, 2014

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ACKNOWLEDGEMENTS

I would like to take this opportunity to thank my committee chair and advisor Dr. Chris Hutchens and express my sincere gratitude for his valuable advice, cooperation, patience and understanding. I wish to express my sincere thanks to Dr. L. Johnson and Dr. C. Latino for serving on my graduate committee. I feel proud to have served as a research assistant in the Mixed Signal VLSI Design Lab at Oklahoma State University. It had been a wonderful and exciting journey and learning experience to work at MSVLSI Design Lab. History of electronic design had shown ups and downs following its nature. The advent of new technology heralds the obsoletion of the old one. Down the road in future in another 25-30 years we might see a dramatic change in technology node with CMOS design being no longer into great practice but the knowledge that I received at MSVLSI Lab will always be extendable to new technologies.

I appreciate MSVLSI Lab team members Mr. Rehan Ahmed, Dr. Ran Liao, Dr. An Guanglei, Mr. Cheng Hao and Mr. Aniket Kulkarni for all their cooperation, valuable suggestions and comments along the course of working at MSVLSI Lab. Above all, I am grateful to my parents for their constant moral and financial support that inspired me to carry on my research ignoring all obstacles in my way.

Acknowledgements reflect the views of the author and are not endorsed by committee members or Oklahoma State University.

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Date of Degree: DECEMBER, 2014

Title of Study: DESIGN AND IMPLEMENTATION OF A LOW POWER T-GATE CELL LIBRARY AND COMPARISON WITH ITS CMOS EQUIVALENT

Major Field: ELECTRICAL ENGINEERING

Abstract:

This work presents the design methodologies, considerations and practical implementation techniques of a sub-threshold/ moderate inversion variability aware Transmission Gate based digital cell library. The implementation method of a reduced ASIC cell library containing minimum number of logic gates sufficient for further front end and back end processing is described. The proposed library targets a reduced implementation time and effort suitable for academic and industrial environment aiming minimum power consumption in battery less devices, portable electronic gadgets or wireless micro sensor networks where computation speed is not of prime concern. To the authors best knowledge, none of the literature till date demonstrates clearly and in a consolidated manner the applicability of T-Gate logic topology as a candidate for ultra-low power applications. Hence, a comparison is presented with equivalent low power CMOS logic gates. Circuit behavior can be significantly impacted due to MOSFET parameter variation. Clear simulation based measurement techniques are presented for measuring concerned parameters like input capacitance, Static Noise Margin(SNM) and I_{OFF} of the T-Gate logic cells and compared with its CMOS equivalent at the same PVT corners. It is observed that the T-Gate shows lower normalized input capacitance than CMOS logic gates. A statistical analysis of logic failure is also presented along with its potential solutions for improvement. As compared to the CMOS gates, the T-Gate logic gates are found to demonstrate slightly narrower distribution of the switching threshold point(V_{Trip}) when performed 200 point Monte Carlo simulation taking process variation and mismatch into account. The CMOS gates demonstrate better static noise margin and hence more robust than T-Gate logic cell and suitable for lower supply voltage operation. A comparison of I_{OFF} is presented to compare the static behavior of the two topologies. The details of device and gate sizing methodology are described along with necessary references. The library is characterized and abstracted to generate necessary files for further processing. A target system is synthesized and a seven stage ring oscillator is simulated in both topologies and is compared to make conclusion based on the observations. T-Gate logic cells demonstrate better static behavior but outperformed by its CMOS logic equivalent in terms of energy consumed per cycle within the range of VDDD from 400mV to 600mV. T-Gate logic gates are slower than its CMOS counterpart at any VDDD of operation and insignificant improvement is achieved with increasing power supply.

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CHAPTER I

INTRODUCTION TO SUBTHRESHOLD OPERATION AND APPLICATIONS

1.1 INTRODUCTION

Sub-threshold operation is popular where circuit applications have a tight power budget and computational speed is of lesser interest. The supply voltage is scaled down near or below threshold voltage resulting in reduced energy consumption for both active operations and static or leakage power dominated circuits [26]. Energy constrained applications having lower activity rate and a lower speed requirement [26] often demands longer battery life and can account on wireless power harvesting as a potential alternative. Micro-sensor networks and RFIDs are examples of such applications used for habitat or interment monitoring, i,e, health and structural monitoring and automotive sensing[26]. The extremely low rate of change of information in environment and health monitoring applications accounts for the reduced performance requirements of the circuit as a result reduction in power consumption becomes a key factor. The radio frequency identification (RFID) tags and application specific digital signal processor and micro-controlling units for portable devices are other examples of such kind of energy constrained operations. The TI C5xx family of DSPs or the TI MSP430 family of MCUs has been used for portable measurements successfully.

1.2 GOVERNING EQUATIONS AND REGION OF OPERATIONS

The sub-threshold equation[1] of current irrespective of region of operation (saturation or linear) can be expressed as

$$Id = I0.\exp\frac{(VGS - VT)}{nUT}(1 - \exp(\frac{-VDS}{UT}))$$

Where,

$$I0 = \mu0.Cox\,\frac{W}{L}(n-1).UT^2$$

n is the sub-threshold slope and given by the equation below $n = (1 + \frac{Cd}{Cox})$ where, Cd is depletion capacitance and Cox is the oxide capacitance

W and L are channel width and length respectively, VGS and VDS are gate to source and drain to source voltage respectively, UT is the thermal voltage and is approximately 26mV at room temperature. Sub-threshold region of operation could be defined as VGS being less than VT(threshold voltage of the MOSFETs) while VDS(drain to source voltage of the MOSFET) could vary depending on whether the device is operating in linear or saturation region. Theoretically at VDS=(3-5)UT and above, the term $(1 - \exp(\frac{-VDS}{UT}))$ becomes approximately equal to one and the device is called to operate in sub-threshold saturation(sub-threshold linear otherwise).The threshold voltage of a minimum geometry NMOS(W=220nm,L=180nm, NOF=1) in this process is measured to be approximately 430mV (neglecting the effect of DIBL at lower supply voltages. See Figure 1.9).Similar I_D vs VDS curves can be observed for both for Sub-threshold and super threshold region of operation with the exception that in sub-threshold the current is orders of magnitude less and follows a log-linear behavior with VGS. The I_D vs VDS curve for sub-threshold and above threshold VGSs are shown in Figure 1.1.

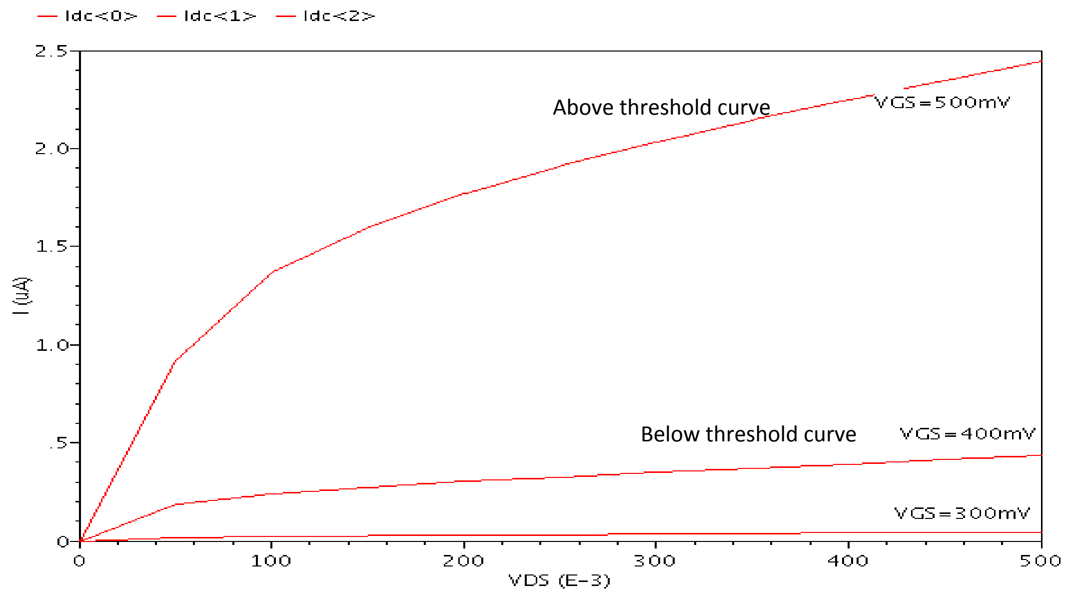

Figure 1.1 Id vs VDS for sub-threshold and above VGSs for NMOS

Typical log-linear behavior in sub-threshold may be obtained by tying the gate to drain of the NMOS(minimum geometry) and varying the VGS from 200mV(device being in sub-threshold saturation) to 800mV(device being in velocity saturation).See Figure 1.2.

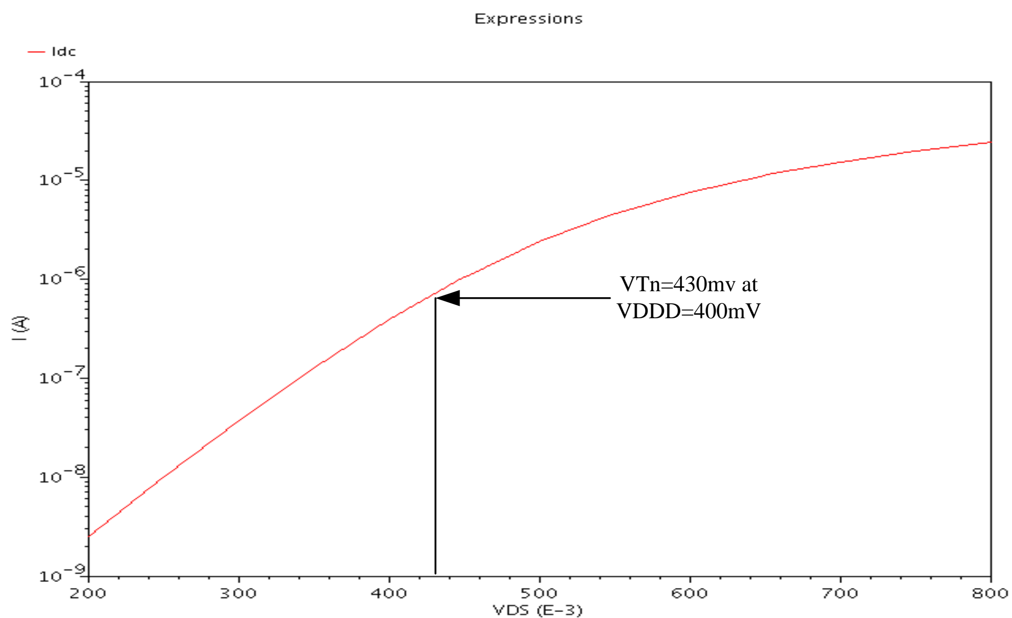

Figure 1.2 Log-Linear behavior of Id vs VDS, VTn=430mV at VDDD=400mV

Table 1.1 Transistor parameters comparison, VTn =430mV at VDDD=400mV

Parameters of Interest	*Sub-Threshold*	*Moderate Inversion*	*Strong Inversion*
gm Efficiency	High	Moderate	Low
VDS(Sat)	5xUT	130-250mV	250mV and Above
Band Width($g_{m/Cgg}$)	Low	Moderate	High
Noise	Low	Moderate	High
Self-Gain(($g_{m/gds}$)	VA/nUT	2VA/(VGS-VT)	VA/(VGS-VT)
Area(WL)	High	Moderate	Low

A comparison of the more significant transistor parameters are given in Table 1.1[27]. The change in Cgg, gm and Log(gm) as we move from sub-threshold saturation to velocity saturation is shown in Figure 1.3, Figure 1.4.a, Figure 1.4.b respectively. Both of

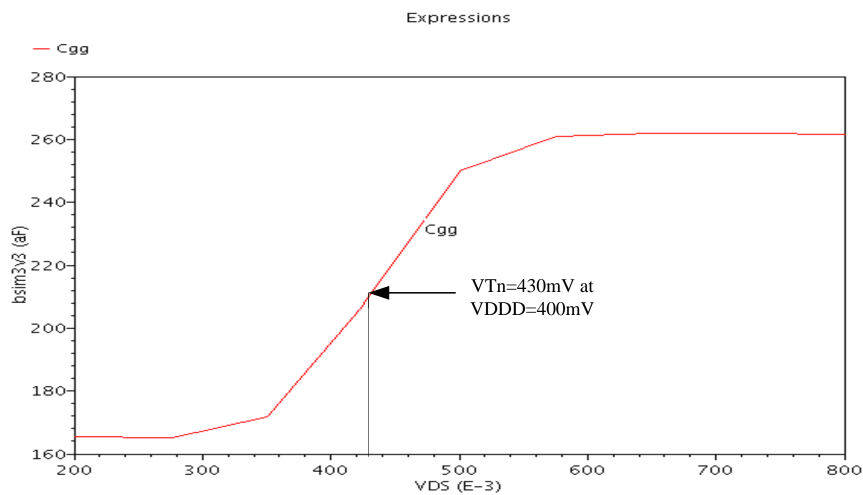

Figure 1.3 Change in Cgg w.r.t. varying VDS, VTn=430mV at VDDD=400mV

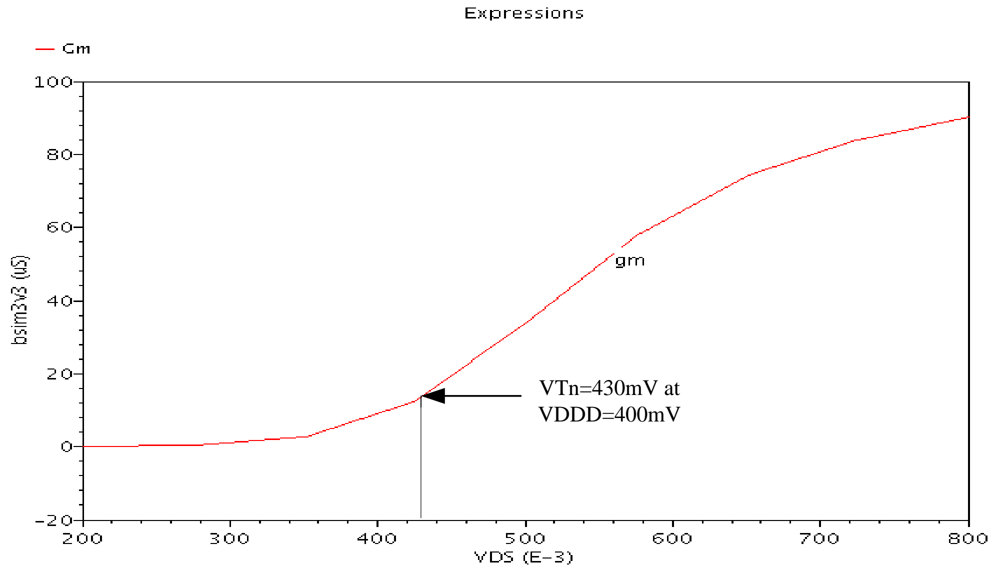

Figure 1.4.a Change in gm w.r.t. varying VDS, VTn=430mV at VDDD=400mV

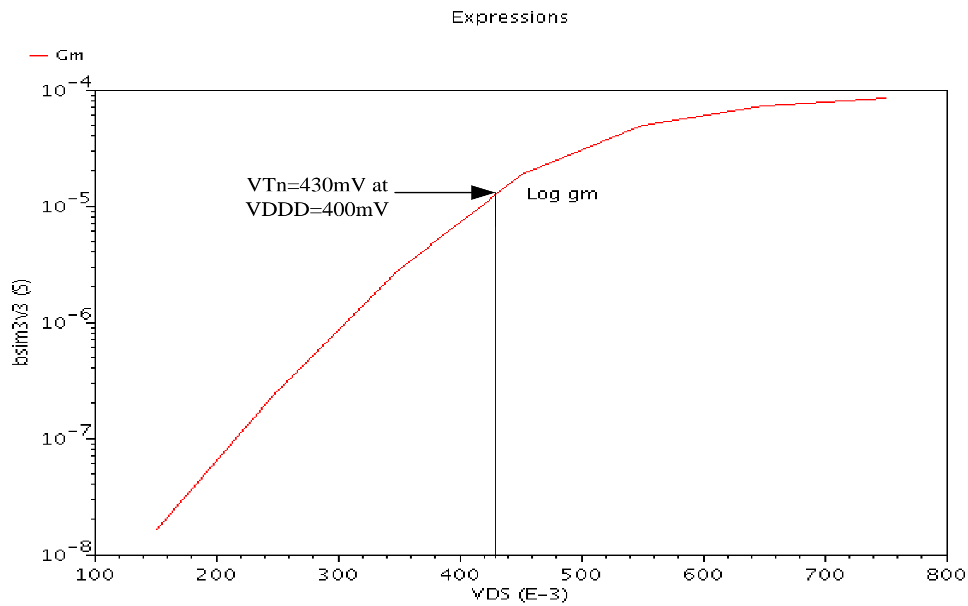

Figure 1.4.b Change in Log(gm) w.r.t. varying VDS, VTn=430mV at VDDD=400mV

these parameters increases as we move towards velocity saturation resulting in a net change in band-width i.e. gm/Cgg as shown in Figure 1.5. The change in gds and self-gain i.e. gm/gds has been shown in Figure 1.6 and 1.7 respectively. It is observed that the self-gain first increases but

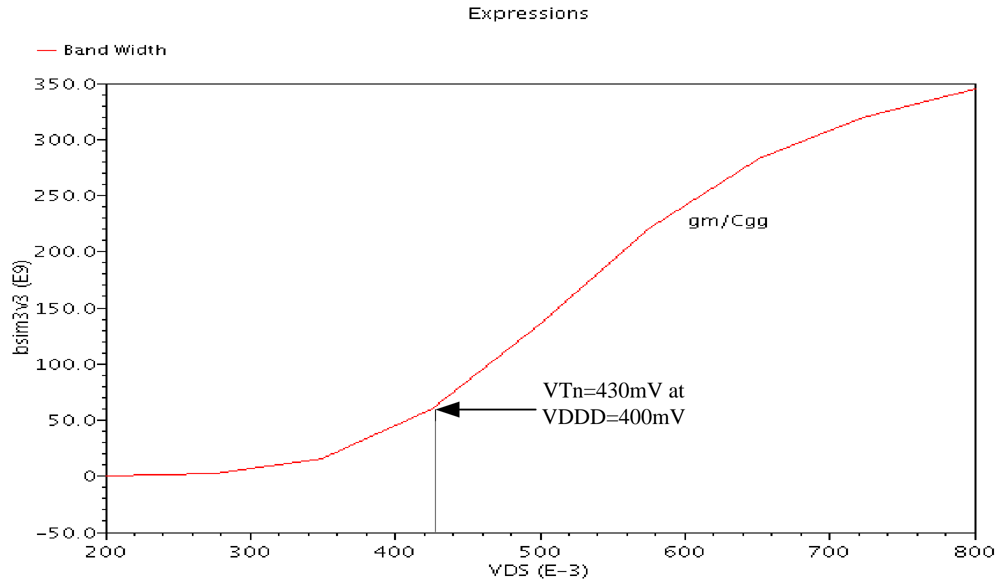

Figure 1.5 Change in gm/Cgg with increasing VDS, VTn=430mV at VDDD=400mV

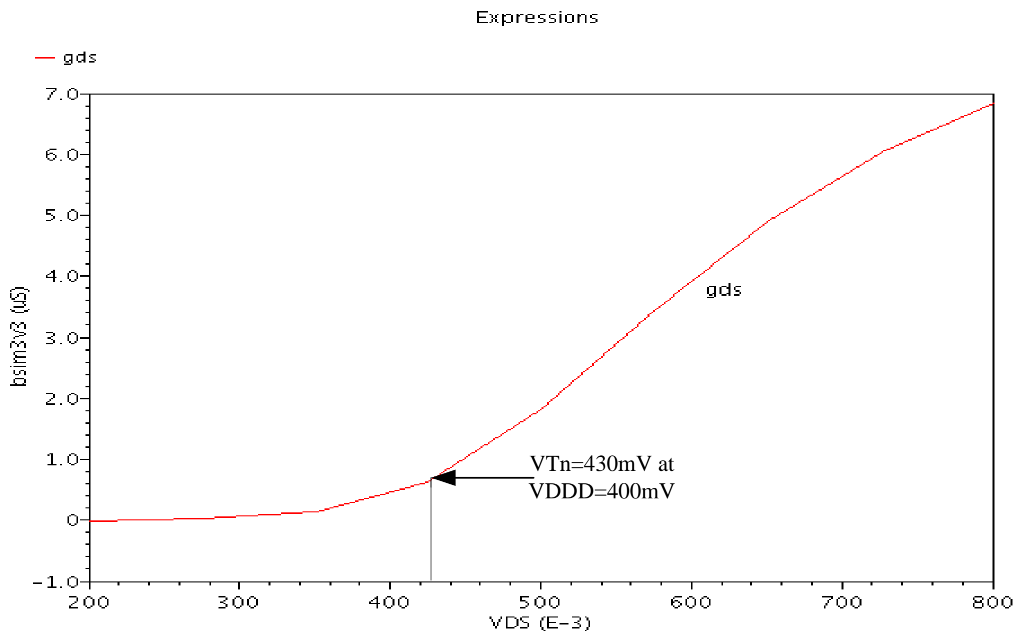

Figure 1.6 Change in gds w.r.t. varying VDS, VTn=430mV at VDDD=400mV

near threshold voltage it reaches its maxima and there after starts falling whereas gds monotonically increases with increasing VDS. The gm efficiency(gm/Id) is shown in Figure 1.8 which is highest in sub-threshold and then falls as VDS increases.

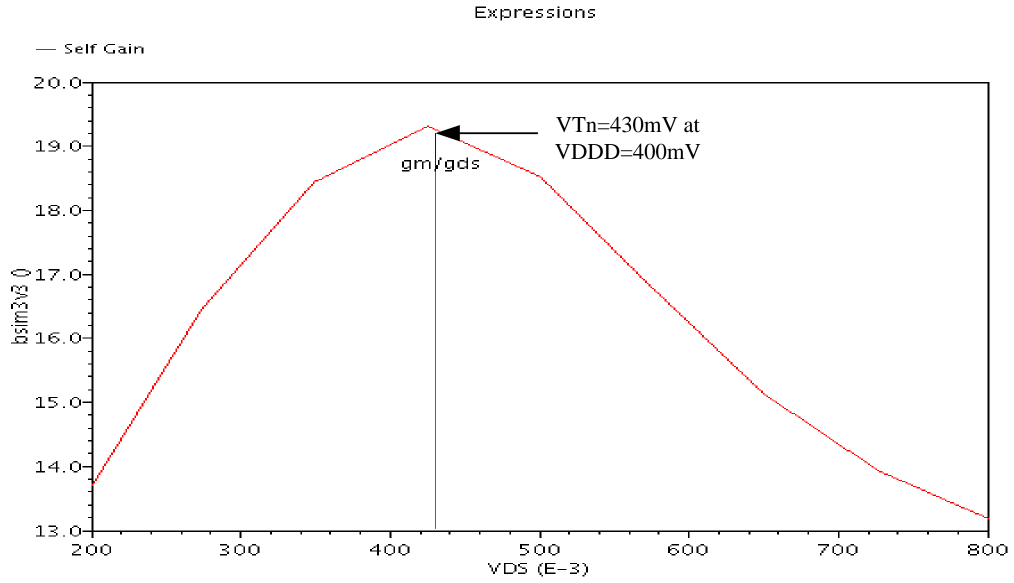

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Figure 1.7 gm/gds w.r.t. varying VDS, VTn=430mV at VDDD=400mV

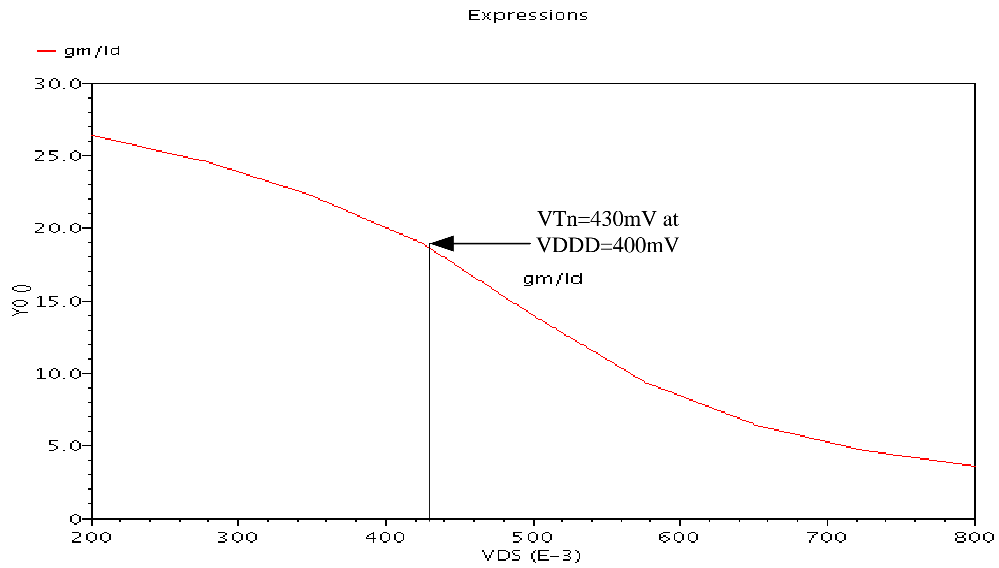

Figure 1.8 gm efficiency (gm/Id) w.r.t. changing VDS, VTn=430mV at VDDD=400mV

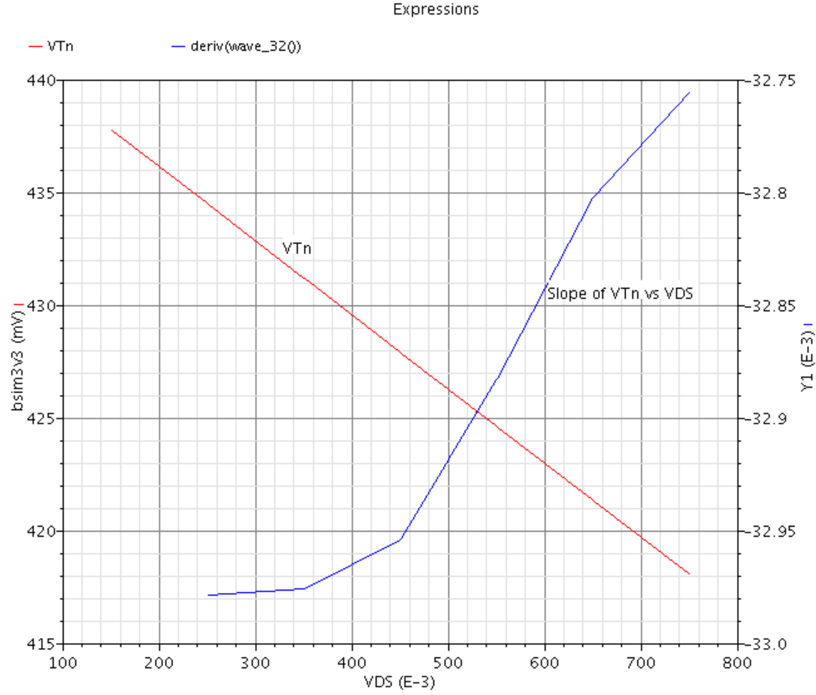

Figure 1.9 VTn variation due to DIBL with increasing VDS.

1.3 VTrip OR SWITCHING THRESHOLD POINT OF AN INVERTER

The VTrip point or the switching threshold point of an inverter in velocity saturation can be expressed by the following equation [32]:

$$VTrip = \frac{Gn.VTn + Gp(VDDD - |VTp|)}{Gn + Gp}$$

where VTn and VTp are PMOS and NMOS threshold voltages respectively. Gn and Gp are the NMOS and PMOS conductance respectively. MOSFET VT varies due to process variation and mismatch i.e. VTn and VTp are two independent statistical parameters having their own sets of statistical distribution. Consequently VTrip has a statistical distribution associated with it which is dependent on VTp and VTn. Impact of this variation is severe in sub-threshold (i.e. VDDD is scaled down below threshold). For a beta matched inverter (i.e. both NMOS and PMOS carrying same ON current) VTrip equals to VDDD/2. The Voltage Transfer Curve (VTC) of a beta batched inverter is marked in blue in Figure 1.10 with its VTrip distribution. The distribution is considered as a normal distribution i.e. drains current will have a corresponding log normal distribution [1] in sub-threshold. The Sigma(σ) of the distribution is also highlighted in the figure. It can be noticed that if the VTC is shifted to the furthest left corner (See Figure 1.10) due to variability the inverter can result in logic failure due to degraded output high(OH) logic level. If the OH of any gate is lower than the input high (IL) logic level requirement of the succeeding gate, it causes logic failure. Similarly on the other side failure may occur because of poor output low (OL) logic level. This failure is a static failure. Even in an ideal and completely noiseless

system this failure may occur as a result of variability. There are two solutions to this particular problem. Either we can increase VDDD to increase margin i.e. shift these entire set of VTC curves along the ‘Vin’ axis to higher values (i.e. higher Mean(μ)) or we can increase the device area to narrow down the VTrip distribution (i.e. reduce Sigma(σ)). Probability of failure can be reduced with both of these above mentioned techniques. A detailed discussion on which one is a better option to reduce failure is presented in Chapter III.

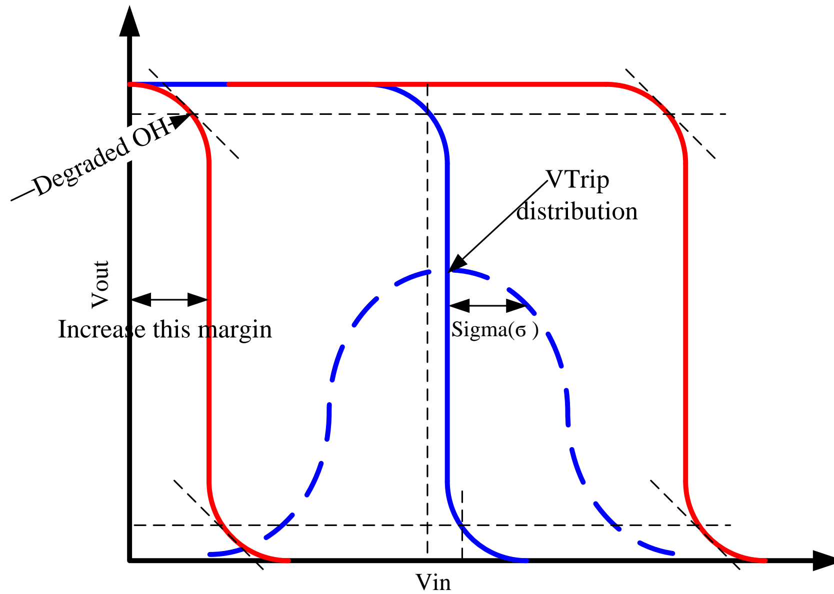

Figure 1.10 VTC of a beta matched inverter and the impact of variability.

1.4 PREVIOUS WORK AND MOTIVATION

A detailed discussion on sub-threshold design methodologies could be found in [1] which describes the impact of supply voltage scaling down aiming minimum energy operation. Even though it mentions T-Gate topology as low power architecture the implementation is primarily focused on CMOS logic gates and device sizing for sub-threshold. Tae-Hyoung Kim et al[28] takes into account the impact of reverse short channel effect on device sizing for sub-threshold operation while[29] considers Inverse Narrow Width Effect on sub-threshold device sizing. Ran et al[18] combines this two impacts in moderate inversion device sizing in achieving a robust digital cell library designing for ultra-low power applications. It also explores the impact of varying device sizing on MOSFET threshold voltage and comes up with a method of finger based device sizing in order to manage threshold voltage variation keeping it independent of device geometry to a first order. All of the above work focused on CMOS topology while targeting reduced power consumption. Hence we focus on T-Gate topology to evaluate its merits and demerits as a candidate for low-power architectures and compare with its near VT CMOS logic equivalent to establish its usefulness in sub-threshold.

1.5 THESIS ORGANIZATION

An introduction to sub-threshold region of operation is presented in Chapter I along with the changes in different concerned MOSFET parameters as we move from sub-threshold to moderate inversion to finally velocity saturation. The capacitance at the input of a logic gate is a factor of concern as higher the input capacitance, the greater is the drive strength requirement to drive that gate. Hence a comparison of normalized input capacitance of T-Gate and CMOS logic gate is summarized in chapter II that shows that T-Gates are having lower normalized total input capacitance. Chapter III deals with prime factor in sub-threshold operation i.e. robustness. The static noise margin is compared between two logic gate topologies under consideration to verify their robustness. The experiments uncover the fact that the CMOS gates are more robust in Sub-threshold due to having better noise margin but T-Gate shows better rate of decrease of logic failure with increasing VDDD due to having narrower distribution of switching threshold point(V_{Trip}) w.r.t. process variation and mismatch. A comparison of I_{oFF} is presented in Chapter IV between CMOS and T-Gate logic equivalent showing that CMOS should show better I_{OFF} performance which is a prime factor for static operation. The device sizing methods to achieve an optimum Power Delay product(PDP) and optimum loading are discussed in Chapter V and Chapter VI which leads to the choice of device finger geometry at specified PVT corner and given specific target system requirement. Target system architecture has been described in Chapter VII to exercise the libraries in this study and a reduced ASIC cell library implementation method has been described in Chapter VIII aiming reduced implementation time and effort. T-Gate based logic gate sizing is described in Chapter IX in details for all concerned gates for the target library whereas the T-Gate library design, implementation, characterization and abstraction flow is described in Chapter X. Finally, the target system is synthesized with the implemented T-Gate library as well as with an existing low power CMOS cell library and the results are compared with each other in Chapter XI. The comparison shows performances at static and dynamic that helps to choose one library over the other one based on requirements and region of operation. Supporting files are provided in appendix A and appendix B.

CHAPTER II

NORMALIZED INPUT CAPACITANCE COMPARISON

2.1 INTRODUCTION

The normalized input capacitance or Logical effort of any digital logic gate has been designated as the ratio of the total input capacitance to the input capacitance of an inverter that can deliver the same output current [20]. The prerequisites to be eligible for logical effort analysis impose certain restrictions on the designated logic gates as described in [20]. The input of the logic gates has to be connected to the gate of a MOSFET and not to the drain or the source terminal. This makes logical effort analysis more valid for CMOS logic gates. Hence, for T-Gate the more fundamental term will be normalized input capacitance (w.r.t.INVX1) as we are not exactly sure of the drive strength of a T-Gate. Keane et al [21] shows a sub-threshold standard CMOS gate device sizing method that takes into account the DIBL effect and compares the new logical effort with the traditional standard CMOS gate logical effort and reports improvement in performance. Chang et al [22] describes the impact of voltage and temperature variation on delay and proposes a new logical effort formulation that takes into account the above two variation mentioned. Wang et al [23] demonstrates the error incorporated in logical effort calculation due to unequal slope of input and output transition of a gate when a multistage log is tapered to reduce the internal energy and introduces a slope correction model. Morgenshtein et al [24] shows that the delay and effort is dependent on the input combinations of the gate switching due to presence of parasitic intermodal capacitance and varies. A delay analysis using modified logical effort is presented in [25]. However none of the above literature proposes any effective way to calculate the logical effort of a T-gate based logic gate design or compares the logical effort of a T-gate based logic design and a standard cell based logic gate design in order to make firm argument on their performance in terms of delay. The effective computation of logical effort of a T-gate based design can be cumbersome as we deal mostly with the inter nodal parasitic capacitance in a T-Gate for effective input capacitance calculation. Here we propose an simulation based method to calculate the normalized input capacitance of T-Gate based logic gate by simulation and compare the worst case computed effort with the traditional standard CMOS based cell's logical effort(Note Normalized Input capacitance is the logical effort itself in case of CMOS logic). For simplicity we limit our analysis to two input gates.

2.2 EXPERIMENT SETUP

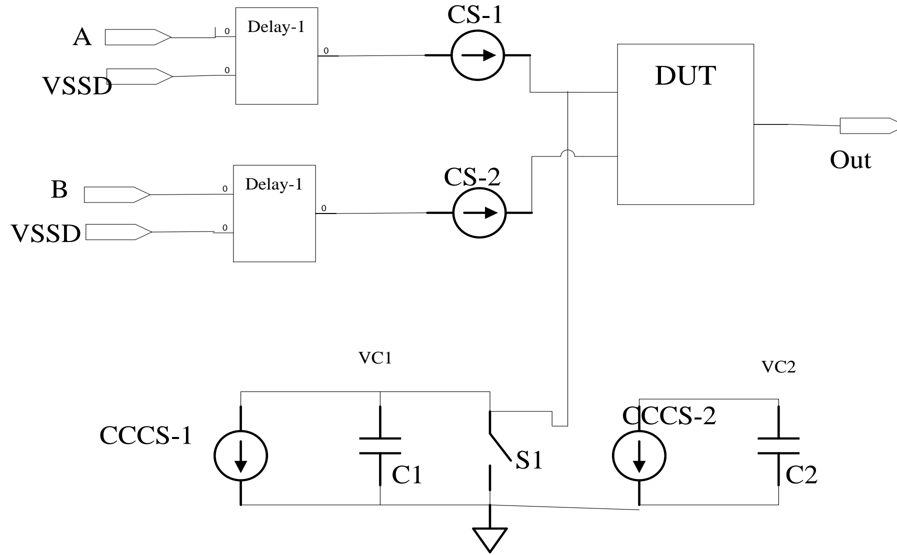

Figure 2.1: Experiment setup for normalized input capacitance calculation

Figure.2.1 shows the experiment setup used for this purpose. DUT represents the Design under test i.e. the two input T-gate logic gates for which we want to calculate the effort. Inclusion of Delay-1 and Delay-2 is optional and does not impact the experiment results. [Cs-1, CCCS-1] and [CS-2,CCCS2] are two current controlled current sources with current gain(k) = -1, used for this setup.C1 and C2 are the capacitors to calculate the input capacitance of port A and B. C1=C2=10fF in this case.
Now, the change in voltage (assuming VC1) across C1 is measured while switching the inputs to cover all possible input combinations and the charge accumulated on C1 is calculated as Q=C1*(VC1 -0); The input capacitance at port A for any particular combination could be calculated as Cinput-A ,=Q/(VDDD-0) where VDDD is the power supply voltage and 400mv in this case. The input capacitance at port B(i.e. Cinput-B)could be found following a similar methodology. After calculating the worst case capacitance seen looking into both of the input ports it could be normalized w.r.t. the input capacitance of INVX1 to get the normalized input capacitance.

Table 2.1 shows a comparison of normalized input capacitance of T-Gate and CMOS logic gates. Note that the logical effort for the standard CMOS based design [20] does not include the inter nodal parasitic capacitances which will increase the effective Logical Effort.

Table 2.1 Normalized Input capacitance comparison between T-Gate and CMOS

Gate Type	Normalized Input capacitance- T-gate Logic		Normalized Input Capacitance- CMOS Logic	
	Port A	Port B	Port A	Port B
NAND	143.3m	1.69	1.3	1.3
NOR	134.5m	2	1.6	1.6
XOR	322.1m	2.8	4	4
XNOR	231.4m	2.3	4	4
MUX	993.3m	254.3m	2	2

It's notable that the total normalized input capacitance in case of T-gate logic is actually less than that of equivalent CMOS design.

2.3 SIMULATION RESULTS AND DETAILED ANALYSIS

A Transmission gate based NAND2X1 gate is shown in Figure 2.2

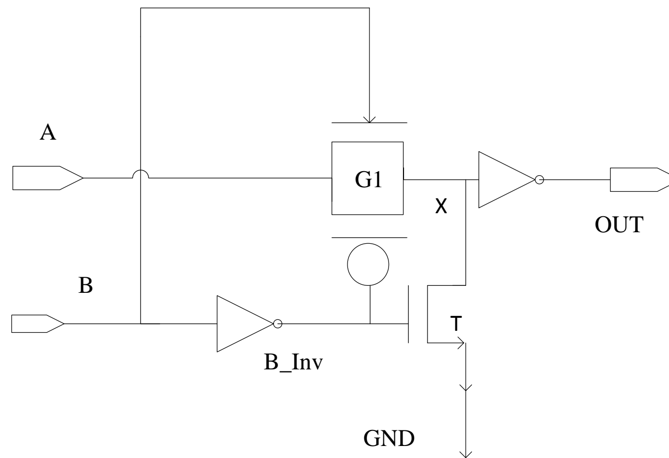

Figure 2.2 T-Gate NAND2X1

Operation observation and calculation:

when A=0 and B=1: T-Gate G1 will be selected; B_Inv=0; Port B drives an 1X inverter and parasitic capacitance as Port A is at 0; Any charge that is stored at node x can flow forward or reverse way.

When A=1,B=0: T-Gate G1 is deselected i.e. off. Port A will drive the parasitic capacitance(as B=0) and will supply the leakage current through G1.B=0 i.e. B_inv=1 and the NMOS T will be on and pull node x down. The leakage through G1 will find a path to ground through T. From the

simulation, it's verified that at this input combination a lot of leakage current flows through A(waveform IA at A=1,B=0)

When A=1, B=1: T-GateG1 is On. Since A is 1 it will drive the output inverter through G1 and the parasitic cap as B_Inv=0; Both the NMOS T and the Cgs of output inverter will provide leakage path and Port A will supply all these current

Worst case normalized input capacitance at port A: At A=0, B=1; port A drives the maximum capacitance. Capacitance at the input of A= (Peak voltage(IA)x 10Pf/ (VDD))= 3.39mv x 10Pf/.4 = 87.81a . From the simulation Input capacitance of an INVX1 is Cin_1X= 612.8a. So normalized input capacitance at port A= 87.81a/612.8a= 0.143

Worst case normalized input capacitance at Port B:When B=1, A=0, Port B drives the maximum capacitance , (One 1X inverter + two parasitic capacitances as A=0 + One NMOS (from G1)).From the simulation, Capacitance at the input of B == (Peak voltage(IB)x 10Pf/ (VDD))=41.45mvx10pf/0.4 =1.036f. Normalized input capacitance at the input of Port B= 1.036f/612.8a=1.69. See Figure 2.3.

	Name/Signal/Expr	Value
1	CiA	87.81a
2	CiB	1.036f
3	Cin_1X	612.8a
4	Logical_effort_Port_A	143.3m
5	Logical_effort_Port_B	1.691

Figure 2.3 Simulation data for T-Gate NAND2X1

The simulation setup for input capacitance calculation for NAND2X1 is shown in Figure 2.4. Figure 2.5 shows the simulated waveforms for the same. The propagation delay is shown in Figure 2.6 and measured to be 43ns. The input capacitance for the additional logic gates are calculated similarly and are given in Table 2.1. The propagation delays for VDDD equal 400mV(tt corner and room temperature) as measured for the concerned logic gates are summarized in Table 2.2 below.

Table 2.2 Propagation Delay for different T-Gate logic gates

T-Gate Type	Propagation Delay (ns)
NAND2X1	43
NOR2X1	39
XOR2X1	35
XNOR2X1	32
MUX2X1	32

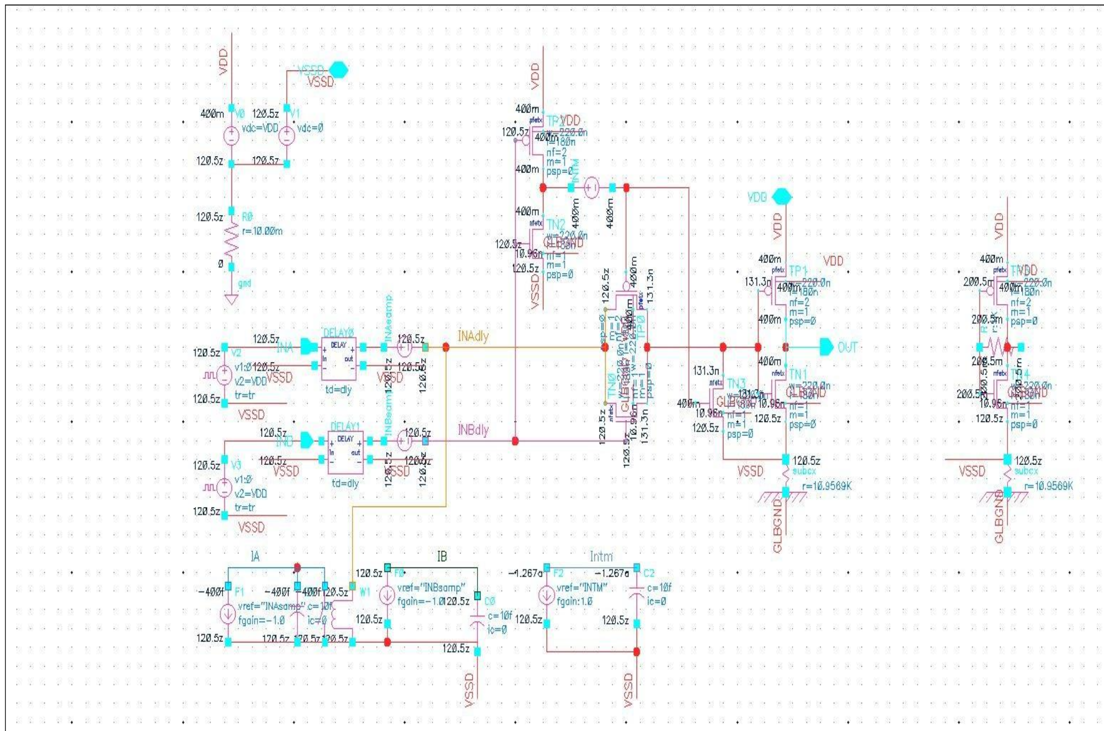

Figure 2.4 Experiment setup for input capacitance calculation of NAND2X1

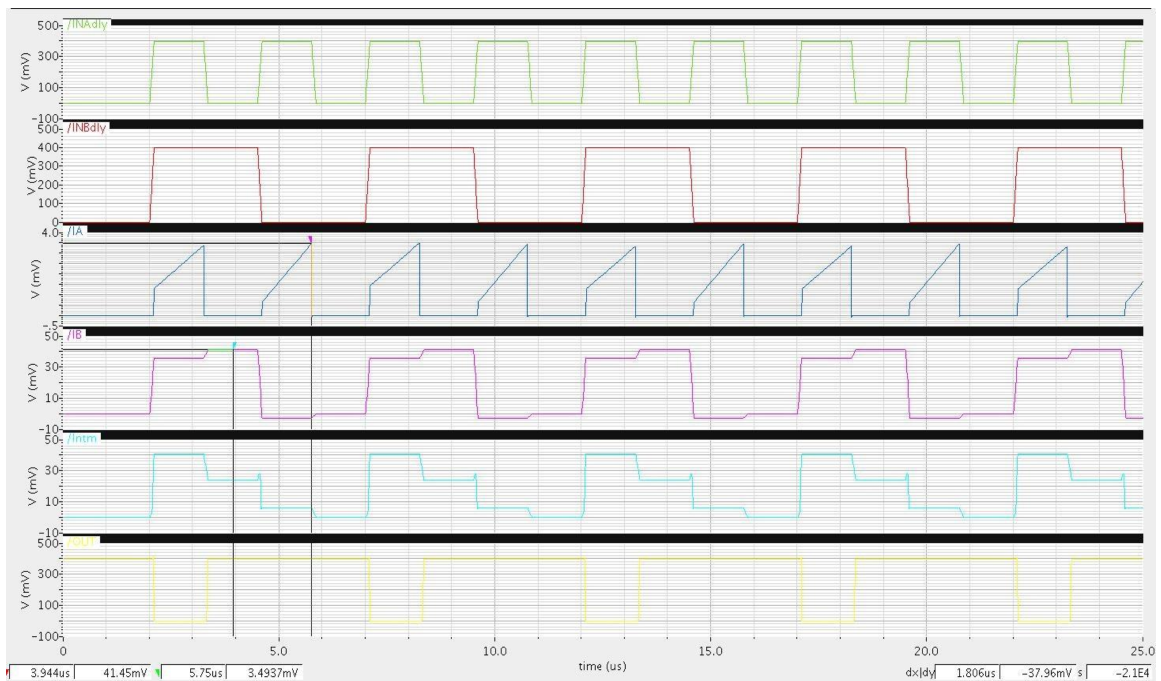

Figure 2.5 Simulation waveform for NAND2X1

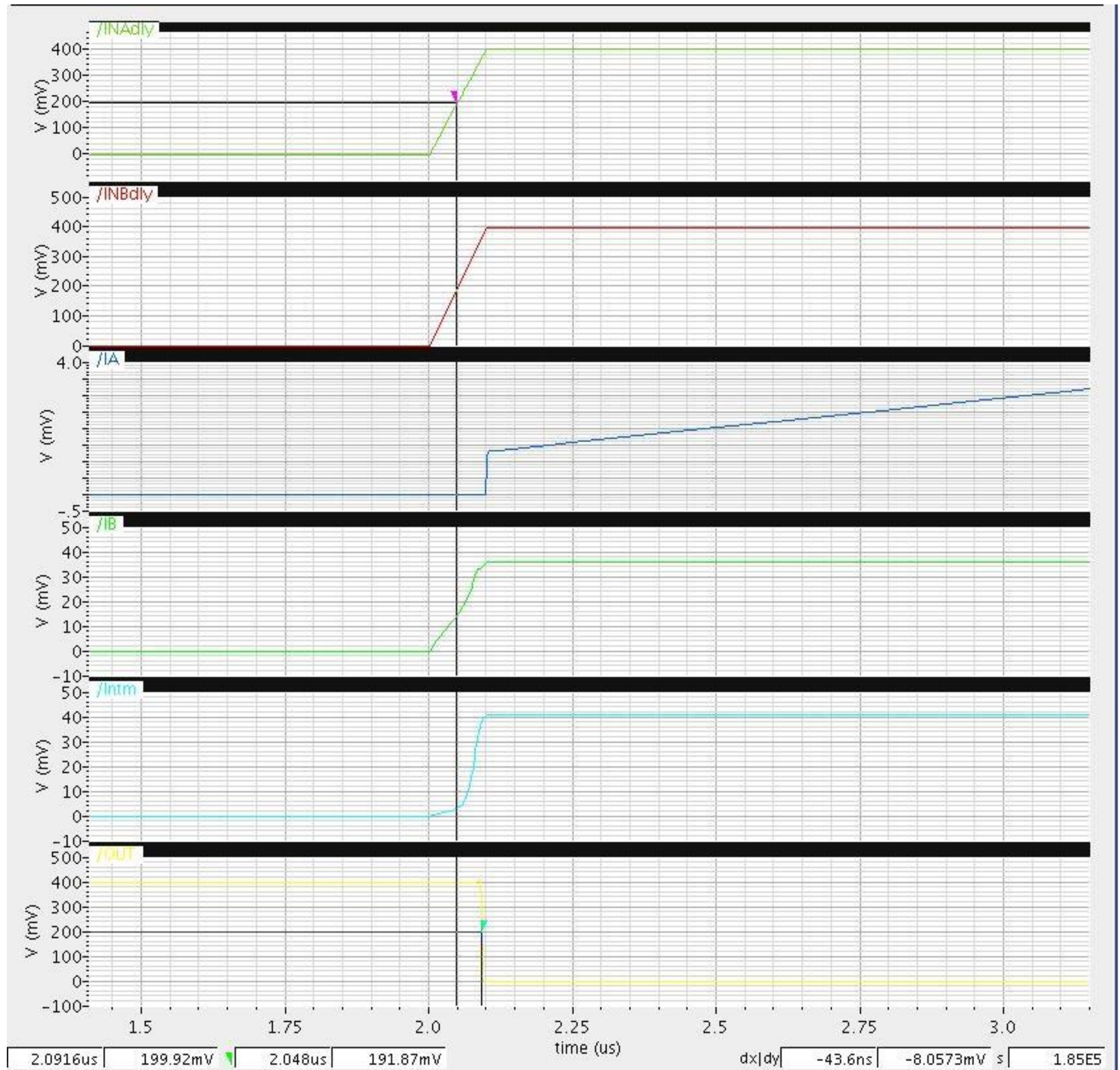

Figure 2.6 Propagation delay measurement for NAND2X1

2.4 CHAPTER SUMMERY

It is notable from Table 2.1 that the total normalized input capacitance for the T-Gates are less than their corresponding CMOS counterpart. But it does not conclude that the T-Gate cells are having lower logical effort and faster. The CMOS gates, in this case are CONVENTIONALLY sized to produce 1X output drive. That is why, when their input capacitance is normalized w.r.t. to the input capacitance of a INVX1 it shows us the corresponding logical effort in case of CMOS cells. On the contrary, the T-Gates contains two stages with an INVX1 as their output stage and T-Gate network as first stage. Dividing the input capacitance of the T-Gate w.r.t. the total input capacitance of an INVX1 does not produce the logical effort as the output drive strength of the T-Gate here depends on the driving gate along with the T-Gate sizing. The logical effort of a T-Gate can be derived in a different manner and discussed in details in Chapter IX.

CHAPTER III

COMPARISON OF SNM AND FAILURE RATE

3.1 INTRODUCTION

Variability is one of the prime concerns as supply voltage scales below 1V and to a much greater extent as VDDD scales near the MOSFET threshold voltage (VT) Circuits operating in moderate inversion or sub-threshold aim to achieve the lower power consumption. Variability in transistor parameters e.g. Threshold voltage (VT) exist irrespective of region of operation but the impact is more severe in sub-threshold as I_{ON} is comparable to $I_{OFF.}$ Due to exponential dependency of current on threshold voltage, minor change in threshold voltage can cause major change in I_{ON}. The current in sub-threshold is given by the following equation below

$$Id = I0.\exp\frac{(VGS - VT)}{nUT}(1 - \exp(\frac{-VDS}{UT}))$$

Where,

$$I0 = \mu0.Cox\,\frac{W}{L}(n-1).UT^2$$

n is the sub-threshold slope and given by the equation below $n = (1 + \frac{Cd}{Cox})$ where, Cd is depletion capacitance and Cox is the oxide capacitance.

Threshold Voltage(VT) distribution of minimum geometry transistor for the CMOS 180nm process under investigation has been shown in Figure 3.1 as obtained by 200 point Monte Carlo simulation taking both process variation and mismatch into account. The matching properties of MOS transistors and threshold voltage model for MOSFETs are demonstrated in [10] and [11] respectively. This initiates the need for further investigation of digital logic gates and their topologies to fit ultra-low power applications. Static Noise Margin is one of the standard methodologies followed in order to quantify and measure rate of failure in standard cell design[1]. Several authors proposed variability aware device sizing and cell library design techniques for sub-threshold operation. Kwong et al [1], [2] considers the skewed P/N process corners (i.e. strong NMOS and week PMOS or the vice versa) as in both case either the circuit

can't drive the output to logic high or logic low to full output swing properly given a clock rate and if the output high (OH) or output low (OL) of one stage is below the trip point (V_{Trip}) of the successive gate, logic failure may occur. *The above stated impact is most prominent when an NAND is driving a NOR or vice versa*. The NAND is having degraded output low (OL) as a result of the stronger pull up network (parallel PMOS) and consequently the worst case input high (IH) requirement. Whereas the NOR shows poor output high(OH) as a result of the stronger pull down network (parallel NMOS) and hereby the worst case input low (IL) requirement. The failure rate of INVX1, NAND2X1 and NOR2X1 w.r.t. upsized device width and VDDD is evaluated in [1] and [2] , defining failure as closing of either of the lobes of the butterfly. The failure is measured by the help of 5k point Monte Carlo simulation. Increasing device geometry reduces the Standard Deviation (SD) of the distribution of threshold voltage variation via a large gate area sampling. A narrower distribution indicates reduced variability but not necessarily an improved SNM. An asymmetrical butterfly results in a higher failure as the smaller lobe indicates a higher probability of closing under worst PVT consideration [8]. Formulation for measuring the SNM for above threshold SRAM cells are provided by [3]. A clearer way of analytical measurement of the SNM and butterfly plot is demonstrated in [12]. Dasdan et al [4] focuses on variability aware cell library design on the basis of Statistical Timing Analysis (SSTA) requirements. Liu et al[5] discuss the implementation of fuzzy logic controller for controlling body bias of the transistors while operating in sub-threshold and hereby achieve better energy savings and performance optimization. Gemmeke et al [6] considers INWE and RSCE into account while sizing the devices. Lohstroh et al [7] shows the flip flop approach of measuring the worst case SNM– is equivalent to an infinitely long chain w.r.t. worst case SNM and gives a mathematical equivalence of four different ways of calculation of SNM. Calhoun et al [9] analyzes SNM of SRAM dependencies on sizing, VDDD, temperature and local and global threshold variation and also gives a mathematical model for sub-threshold SNM.

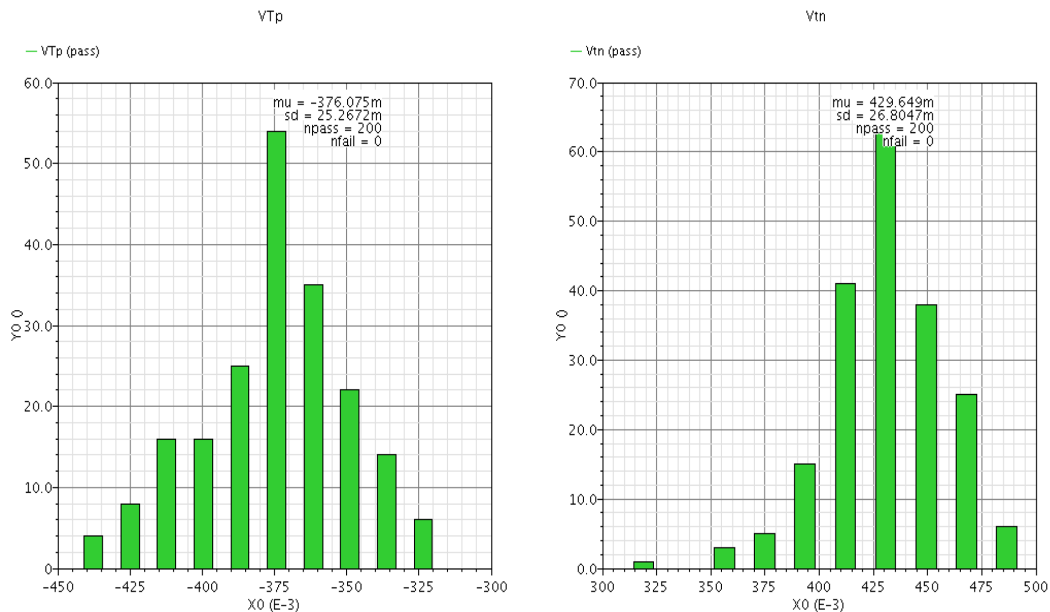

Figure 3.1: Threshold Voltage(VT) distribution for NMOS(right) and PMOS(left)

3.2 OBJECTIVE

The focus of the following experiment and analysis is to derive an optimum SNM given a particular VDDD where we define optimum SNM to be the gate, having equal noise margins on both lobes of the butterfly plot in order to avoid a higher probability of failure for either of the output logic state under worse case PVT considerations [8]. A NAND2X1 driving a NOR2X1 and vice versa is considered as the worst case circuit under test [1] and 3 input NAND/NOR are disallowed. Different device sizing methodology for the test circuit is explored to obtain the best case SNM and the impact of increasing VDDD and device geometry is analyzed aiming reduction in logic failure rate. Considering the fact that increasing VDDD essentially shifts the V_{Trip} Mean (μ) of V_{Trip} distribution of the logic gates to higher values with minimal or insignificant change in Sigma(σ) of the trip point distribution. Analysis has been done for both CMOS topology and T-Gate based design and their SNM is compared as a measure of robustness. Finally the optimum operating frequency for each of the topologies has been derived by simulating a seven-stage NAND-NOR ring oscillator as VDDD is varied from 300mV to 400mV with a step of 20mV.

3.3 EXPERIMENT SETUP AND PROCEDURE

The trip point (V_{Trip}) of a beta matched inverter at VDDD=300mV is measured. This is as expected to be set at or near VDDD/2. In a skewed P/N process corner the NMOS is typically going to be stronger w.r.t. the PMOS or vice versa. As a result, the trip point is going to move up or down from its ideal balanced state (VDDD/2) resulting in an asymmetric butterfly. Considering process variation and mismatch, the VTn may vary by 1,2 or 3 Sigma(σ) etc. where sigma is shown in Figure 3.1. This is modeled as shown by the arrangement in Figure 3.2. The DC sources are set to 0,1,2,3 Sigma voltage values to represent variation of NMOS threshold voltage, where the sigma is obtained by a 200 point Monte Carlo simulation taking process variation and mismatch into account. The VTC curves for each as these cases is obtained by an input dc sweep and are shown in Figure 3.3. It is observed that as the threshold voltage reduces, the inverter is no longer beta matched and the VTC curve shifts towards left which impacts the butterfly causing an asymmetric SNM . The butterfly plots for each of these cases are shown in Figure 3.4.

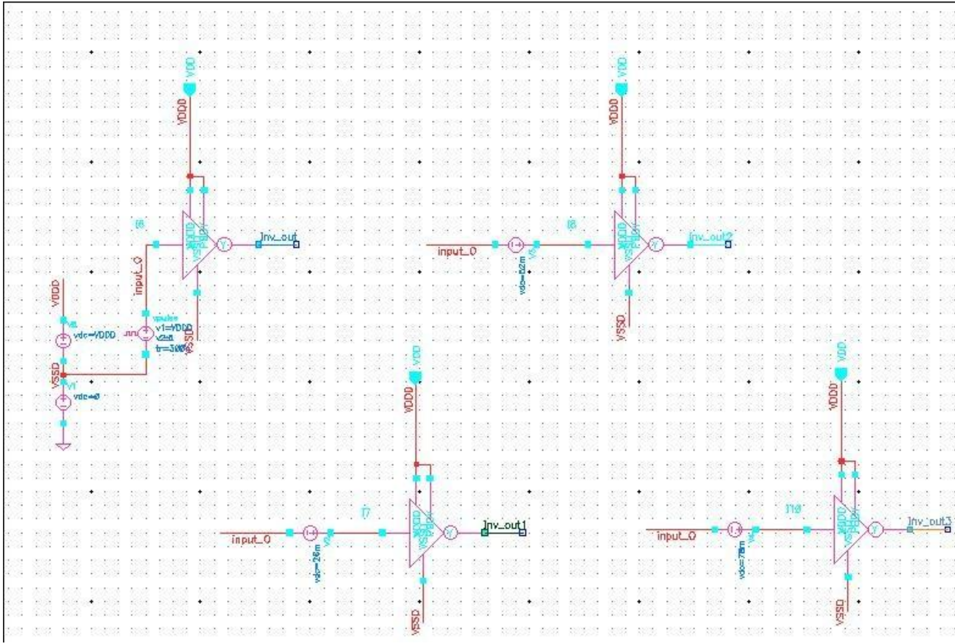

Figure 3.2 Experiment setup for butterfly plot with varying Sigma VTn

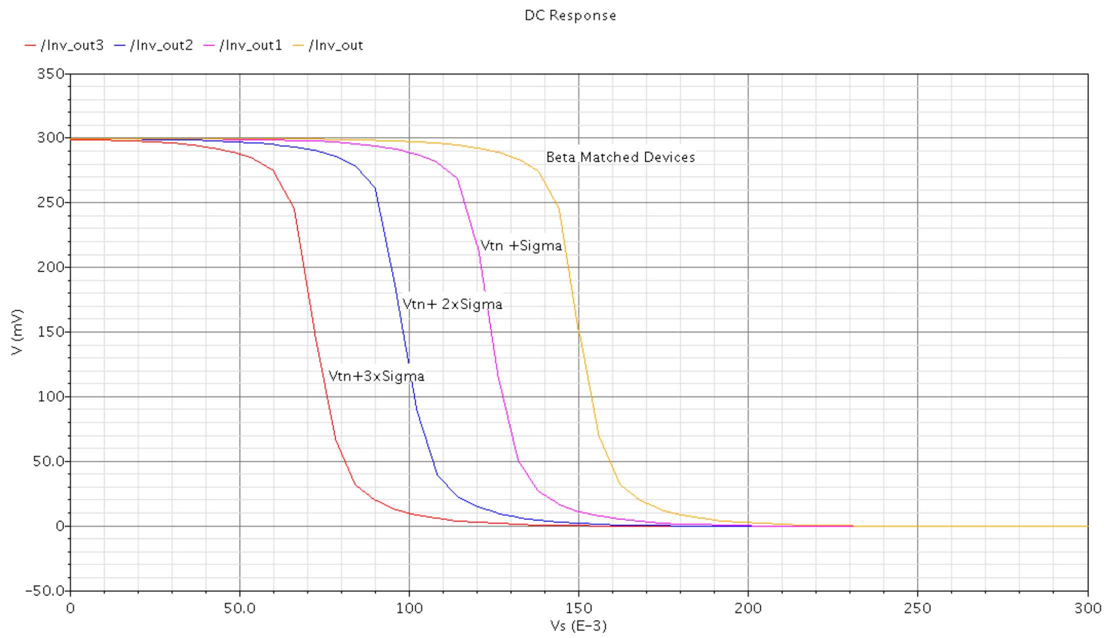

Figure 3.3 VTC curves with changing Sigma VTn

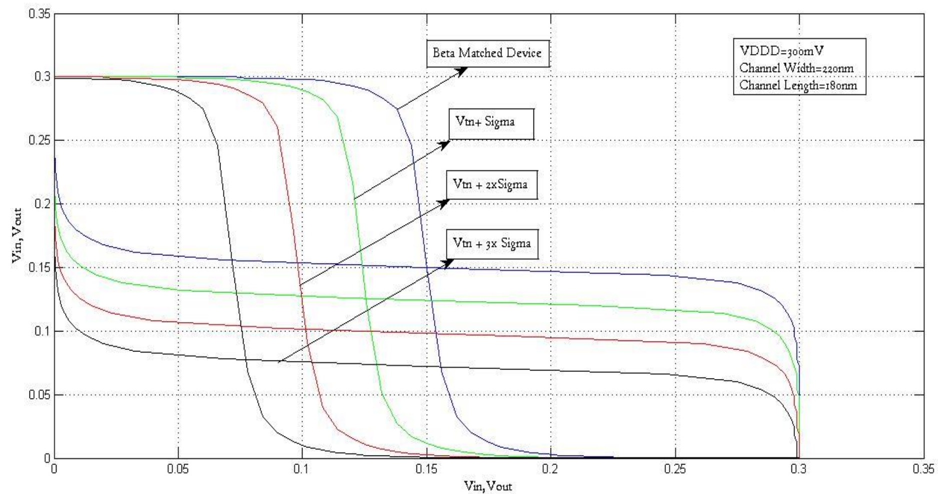

Figure 3.4 Butterfly plot and SNM change with varying VTn

From Figure 3.4 we see that beta matched gates result in an optimum SNM as shown by the symmetric butterfly plots as per our definition and with increasing Sigma(σ) VTn, the bottom lobe in the butterfly is becoming smaller resulting in lower SNM for output logic low. The opposite effect is observed as VTp of the PMOS is varied. Beta matched logic results in a symmetric butterfly plot and an optimum SNM for both out logic states with an equal probability of failure of both SNM.

As stated in [1], a chain of NAND and NOR driving each other is consider to be the worst case in terms of SNM. We now seek to optimize noise margins following our definition by focusing on device sizing for the NAND2X1 and NOR2X1 gates. The two parallel NMOSs (T1, T2, Figure 3.5) in NOR2X1 and the two parallel PMOSs (T3,T4, Figure 3.5) degrades the output logic high OH) and low(OL) respectively. This is the main cause of degraded SNM in case of NAND2X1 and NOR2X1 and them driving each other.

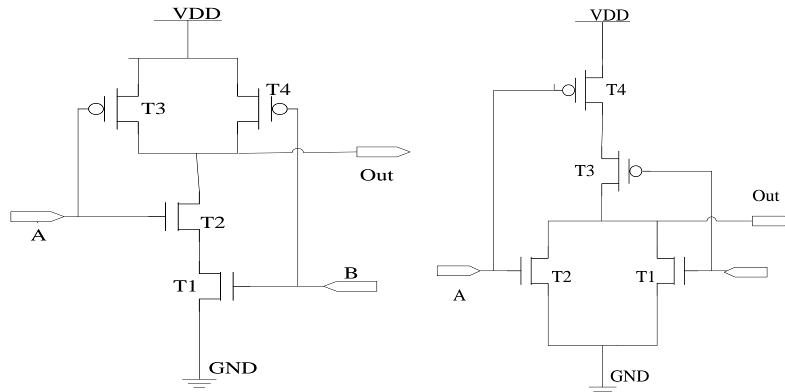

Figure 3.5 CMOS NAND2X1 (left) and NOR2X1 (right)

Threshold voltage (VTn and VTp) variation with device geometry in the process under consideration is shown in Figure 3.6.

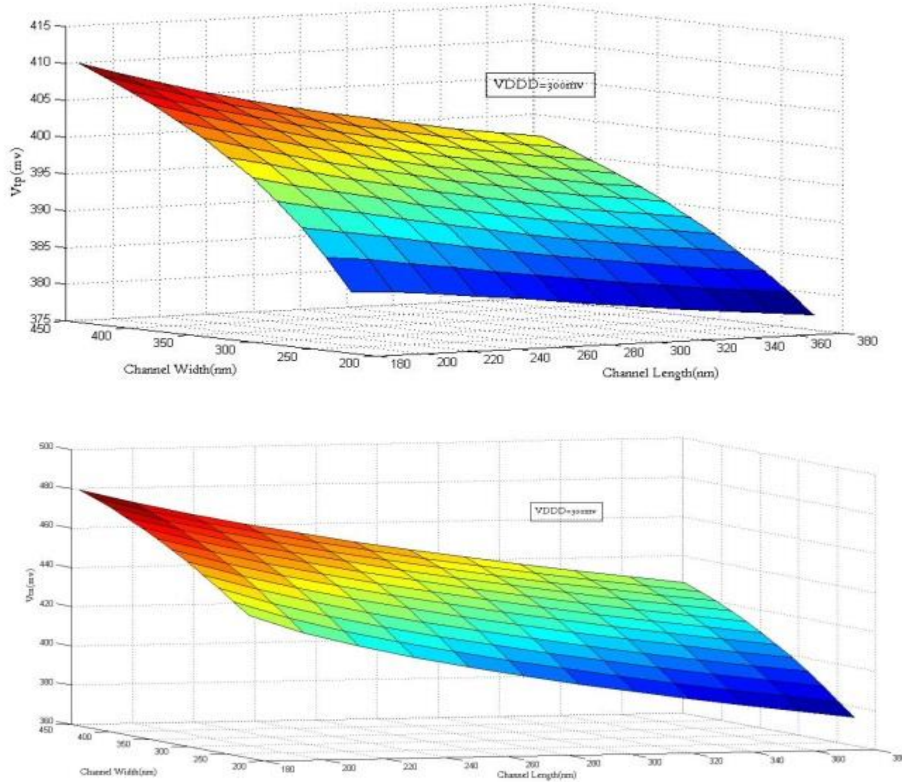

Figure 3.6 VTn (top) and VTp(bottom) variation w.r.t. device geometry

Figure 3.6 shows that both the threshold voltages (VTn and VTp) increases with increasing device width for any given channel length. On the contrary, both VTn and VTp decreases with increasing channel length for any given device width of choice. This property is exploited in order to derive a symmetric SNM for the logic circuit under test. The following two possibilities are considered.

a) If we increase PMOS finger width in NAND2X1 and NMOS finger width in NOR2X1, the I_{OFF} will reduce due to increase in threshold voltage which might improve SNM and hence balance the trip point at VDDD/2 resulting in symmetric butterfly.
b) If we increase channel length of NMOS of NAND and PMOS of NOR, Ion will increase due to the resulting reduction in threshold voltage and will improve SNM by more closely balancing the V_{Trip} at mid-rail resulting in more symmetric butterfly.

We employ the above methodology to verify improvement in SNM. The results are shown in Table 3.1.The 1st 5 data correspond to method (a) stated above and the last 5 data correspond to method (b). In both cases the trip point(V_{Trip}) distribution of NAND2X1 and NOR2X1 connected as inverter has been measured with their input and output sorted together , along with mean and Sigma of distribution by 200point Monte Carlo simulation(with process variation and mismatch

into account). It is observable that we don't get any significant improvement in trip point in NAND2X1 with increasing device width but the NOR2X1 shows improvement in trip point(V_{Trip}) which is close to VDDD/2 at a NMOS finger width=440nm at VDDD=300mV.

Table 3.1 V_{Trip} of NAND2x and NOR2X1 vs Increasing Width(top 5) and Length(bottom 5)

Width (nm)	Length (nm)	Vtrip_NAND (mV)	Mean_Vtrip_NAND (mV)	Sigma_Vtrip_NAND (mV)	Vtrip_NOR (mV)	Mean_Vtrip_NOR (mV)	Sigma_Vtrip_NOR (mV)
220	180	161.7	162.2	14.66	138.9	137.8	14.06
280	180	161.7	161.9	14.29	142.8	142.1	13.56
340	180	162	162.2	14.09	145.9	145.4	13.3
400	180	162.5	162.6	13.95	148.1	147.7	13.16
440	180	162.9	163	13.87	149.1	148.8	13.09
220	216	156.8	156.6	15.48	136.4	135.4	13.78
220	252	154.3	153.9	15.81	134.6	133.6	13.65
220	288	152.6	152	15.94	133.2	132.2	13.57
220	324	151.1	150.5	15.98	131.9	131	13.51
220	360	149.8	149.1	15.99	130.8	129.8	13.48

On the other hand increasing channel length shows improvement in NAND trip point at L=360nm but degradation in NOR trip point with increasing channel length. However none of this shows a drastic improvement in Sigma(σ) of trip point(V_{Trip}) distribution as sigma varies proportional to 1/SQRT(WL). The butterfly plots against both (a) and (b) has been shown in Figure 3.7 and Figure 3.8 respectively.

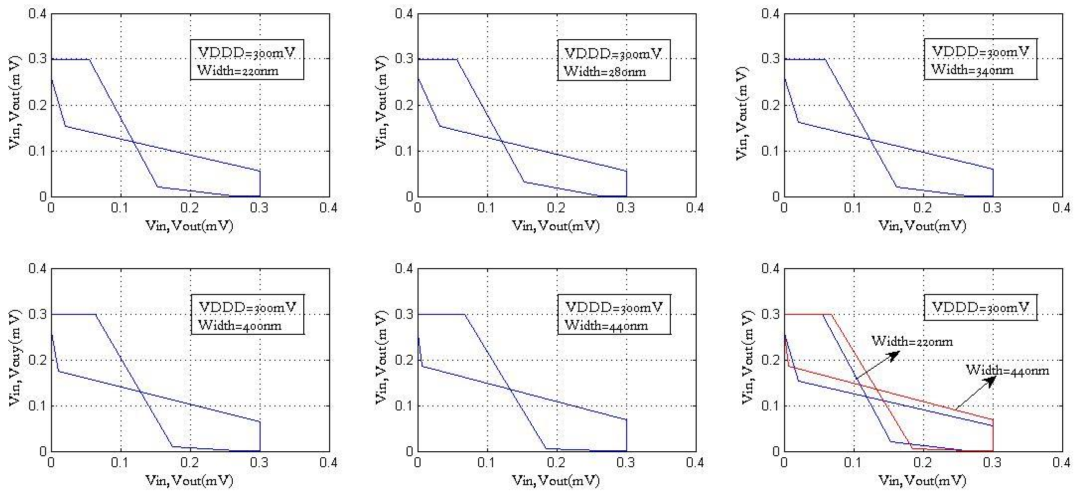

Figure 3.7 Butterfly plots w.r.t. increasing Width (method a, top 5 data in Table 3.1)

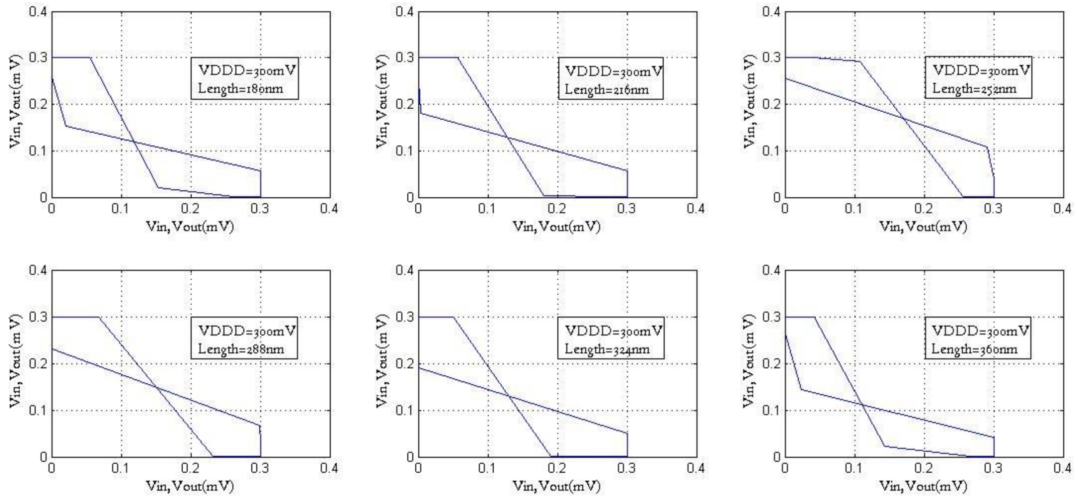

Figure 3.8: Butterfly plot w.r.t. increasing Channel length (method b, Bottom 5 data in Table 3.1)

The change in trip point (V_{Trip}) of NAND2X1 and NOR2X1 w.r.t. changing Channel Length are shown in Figure 3.9 and change in trip point (V_{Trip}) of NOR2X1 w.r.t. channel width is shown in Figure 3.10 respectively.

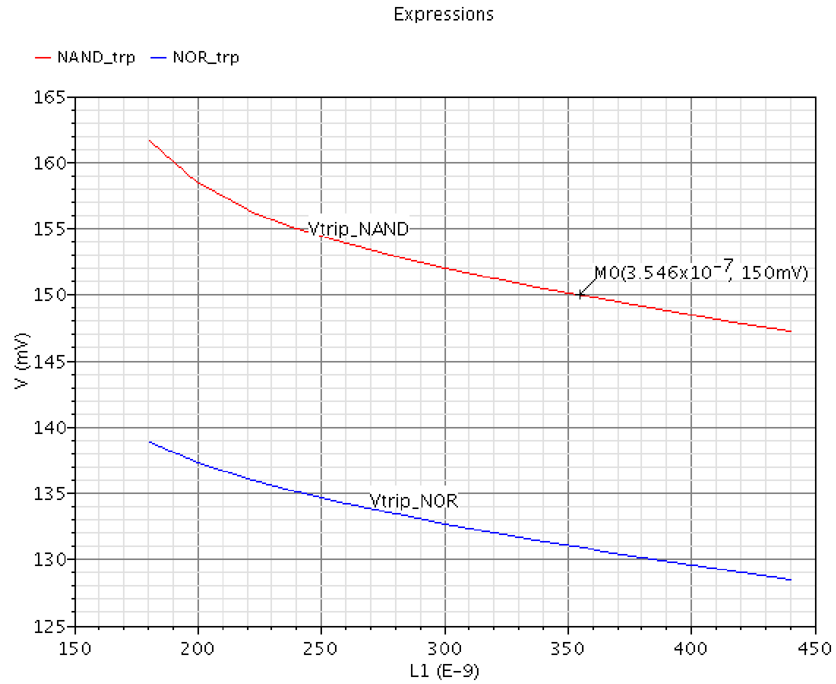

Figure 3.9: Change in V_{Trip} with increasing Channel Length (nm) for NAND2X1-NMOS, NOR2X1-PMOS(VDDD=300mV)

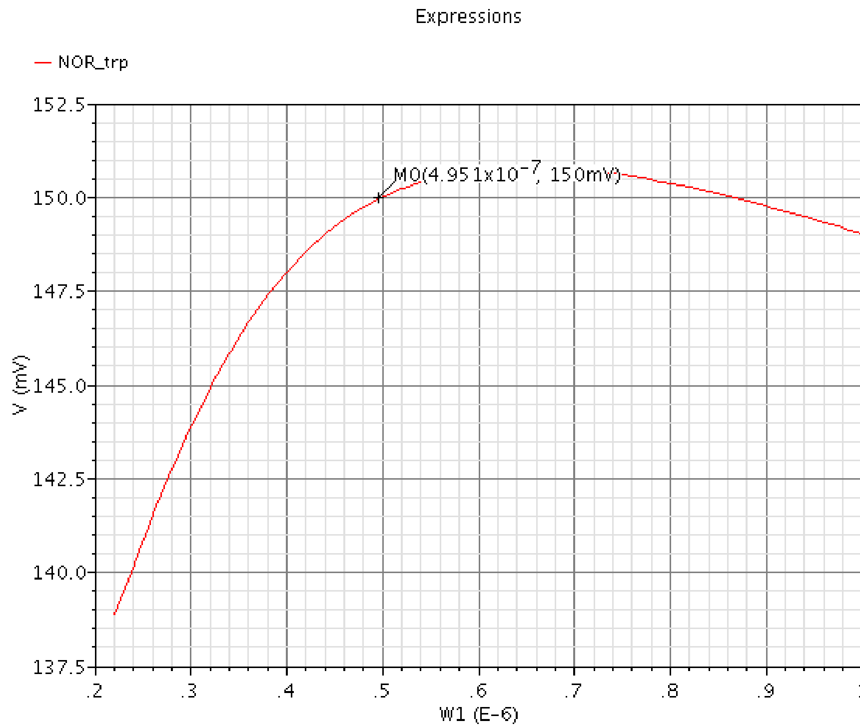

Figure 3.10: Change in NOR2X1 V_{Trip} w.r.t. increasing NMOS device width(nm)

Based on Table 3.1, Figure 3.9 and Figure 3.10, I propose an optimum device (finger) sizing for CMOS NAND2X1 and NOR2X1 for best case SNM and symmetric butterfly shown in Table 3.2 and Table 3.3 respectively.

Table 3.2 Proposed Device sizing for CMOS NAND2X1

NAND_NMOS_ Width	NAND_NMOS_ Length	NAND_NMOS_ NOF	NAND_PMOS_ Width	NAND_PMOS_ Width	NAND_PMOS_ NOF
220	355	2	220	180	2

Table 3.3 Proposed Device sizing for CMOS NOR2X1

NOR_NMOS_ Width	NOR_NMOS_ Length	NOR_NMOS_ NOF	NOR_PMOS_ Width	NOR_PMOS_ Length	NOR_PMOS_ NOF
495	180	1	220	180	4

However there are two more possibilities of optimization of SNM. We can add a few extra fingers to the NMOS of NAND2X1 and PMOS of NOR2X1 and that will attempt to balance the trip point at the mid-rail and consequently result in symmetric butterfly and equal SNMs-. The change in trip point of NAND2X1 and NOR2X1 along with the Sigma (σ) and Mean (μ) of trip point (V_{Trip}) distribution has been shown in Table 3.4 and table 3.5 respectively.

Table 3.4 Change in V_{Trip} of NAND2X1 with increasing NMOS no of fingers

NAND_NMOS_ Width(nm)	NAND_NMOS_ Length(nm)	NOF_NMOS	Vtrip_NAND (nm)	Mean_Vtrip (mV)	Sigma_Vtrip (mV)
220	180	2	161.7	162.2	14.66
220	180	3	154.4	154.7	14.55
220	180	4	149.3	149.6	14.49
220	180	5	145.4	145.6	14.45

It can be seen from Table 3.4 and Table 3.5 that the trip point (V_{Trip}) of NAND2X1 is closed to VDDD/2 when NOF_NMOS is 4. The trip point (V_{Trip}) of NOR2X1 shows similar behavior at PMOS NOF=7. Also reducing the PMOS NOF in NAND to NOF=1(instead of NOF=2) will balance the trip point to VDDD/2 as shown in Table 3.6.

Table 3.5 Change is V_{Trip} of NOR2X1 with increasing no of PMOS fingers.

NOR_PMOS_ Width(nm)	NOR_PMOS_ Length(nm)	NOF_PMOS	Vtrip_NOR (nm)	Mean_Vtrip (mV)	Sigma_Vtrip (mV)
220	180	4	138.9	137.8	14.06
220	180	5	142.6	141.6	13.88
220	180	6	145.7	144.7	13.75
220	180	7	148.2	147.3	13.66

Table 3.6 NAND2X1 V_{Trip} with NOF PMOS=1

NAND_NMOS_Width	NAND_NMOS_Length	NAND_NMOS_NOF	NAND_PMOS_Width	NAND_PMOS_Length	NAND_PMOS_NOF	Vtrip_NAND (mV)
220	180	2	220	180	1	150

Based on this analysis we have four overall different combinations of device and figure sizing for NAND2X1 and NOR2X1 that gives close to VDDD/2 Vtrip. This is shown in Table 3.7. We need to choose the best case combination out of this. To do so, we plot the butterfly for each of this combination considering a NAND2X1 is driving a NOR2X1 and vice versa. The butterfly plots are shown in Figure 3.11, 3.12.a, 3.12.b, 3.13 respectively corresponding to each combination of NAND2X1 and NOR2X1 in Table 3.8.

Table 3.8 Device sizing for NAND2X1 and NOR2X1 resulting close to mid-rail V_{Trip}

NAND_NMOS_Width	NAND_NMOS_Length	NAND_NMOS_NOF	NAND_PMOS_Width	NAND_PMOS_Length	NAND_PMOS_NOF	NOR_NMOS_Width	NOR_NMOS_Length	NOR_NMOS_NOF	NOR_PMOS_Width	NOR_PMOS_Length	NOR_PMOS_NOF	Vtrip_NAND (mV)	Vtrip_NOR (mV)
220	355	2	220	180	2	495	180	1	220	180	4	149.8	150
220	180	4	220	180	2	220	180	1	220	180	7	149.3	148.2
220	180	2	220	180	1	495	180	1	220	180	4	150	150
220	180	2	220	180	1	220	180	1	220	180	7	150	148.2

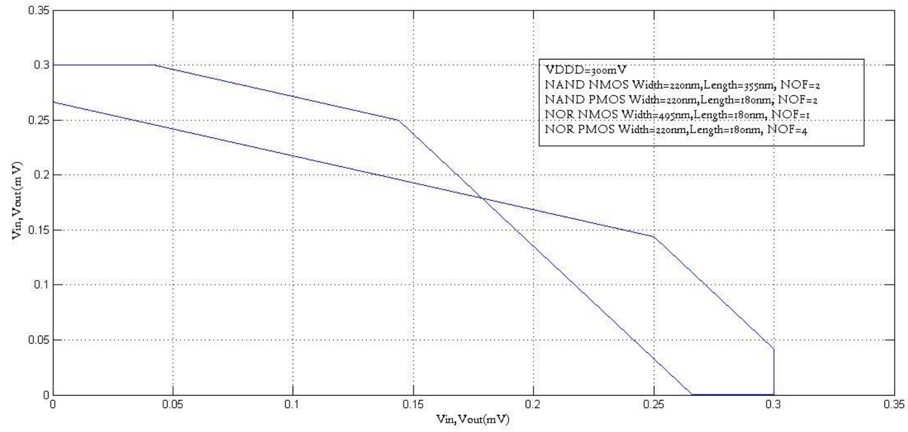

Figure 3.11: Butterfly for 1st combination in Table3.8

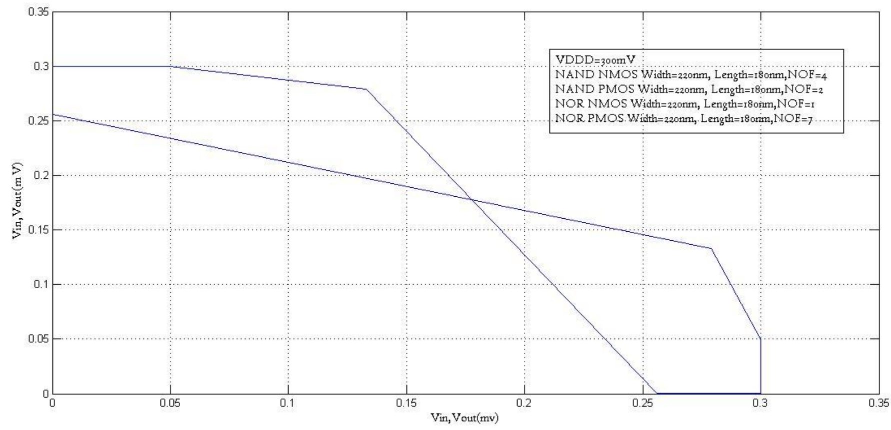

Figure 3.12.a: Butterfly for 2nd combination in Table 3.8

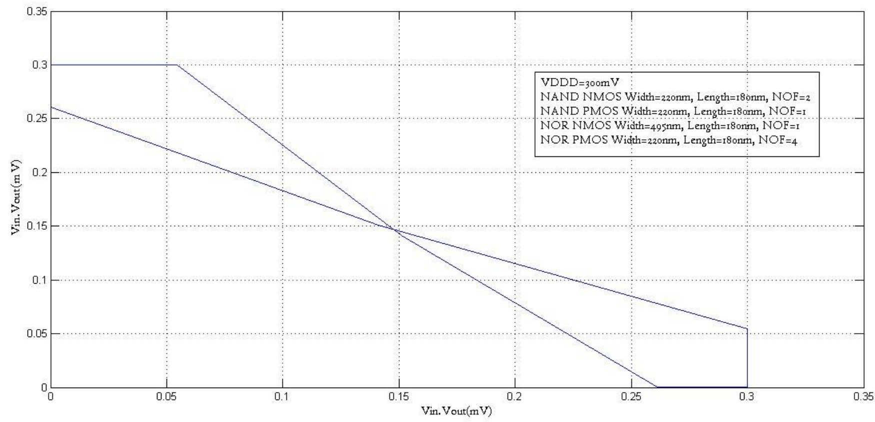

Figure 3.12.b: Butterfly for 3rd combination in Table 3.8

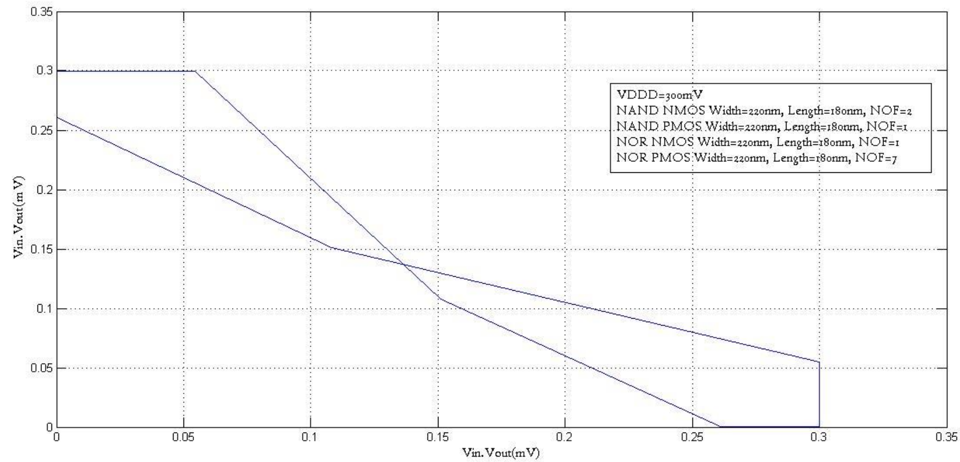

Figure 3.13: Butterfly for 4th combination in Table 3.8

From Figure 3.11, 3.12, 3.13, 3.14 it is clear that the 3rd and 4th combination does not produce enough SNM even though all of them have close to mid-rail V_{Trip}. So we discard them. Whereas, the 1st two combinations in Table 3.8 produces almost comparable SNM. Now we make a best case choice between 1st and 2nd combinations of Table 3.8. In addition we consider the power delay product(PDP) as the determining or most significant factor. To achieve this we measure the delay, Integrated Current and average current over a cycle[1], Pavg and PDP all at VDDD=300mv using a 7 stage NAND-NOR(configured as an inverter) chain. The results are displayed in Table 3.9 in sequential order for combination 1 and 2 of Table 3.8. This show that the best case NAND2X1 and NOR2X1 will be given by 1st device sizing method of Table 3.8. This is the optimum SNM we achieve by device resizing at a particular VDDD. Beyond this, in order to reduce logic failure or to increase frequency of operation, we must increase VDDD. Increasing VDDD shifts the distribution and the Mean of Vtrip to a higher value. From Table 3.9 the 1st combination geometry combination of Table 3.8 turns out to be the best solution at the VDDD under consideration.

Table 3.9 PDP measurements corresponding to 1st and 2nd combinations in Table 3.8

Delay(ns)	Integrated current(fA)	Avg_current(A)	VDD(mV)	Pavg(watt)	PDP(J)
223	5.555	2.49103E-08	300	7.47309E-09	1.6665E-15
196	6.879	3.50969E-08	300	1.05291E-08	2.0637E-15

3.4 FAILURE AND REDUCTION IN FAILURE BY INCREASING VDDD

In digital logic, devices should operate in saturation when in the act of switching in order to retain maximum current and limited gain and band width. In sub-threshold (and weak inversion), when VDS is equal to 3-5 UT i.e. 75-125 mV, the device is considered to be in saturation. To be a little conservative we consider that the devices should at least maintain 125mV(5.UT) of VDS across

them. Hence for an INVX1, we define failure as downward shift of the trip point (V_{Trip}) below 125mV and upwards shift beyond (VDDD-125)mV= 175 mV for VDDD=300mV. When considering the trip points for the NAND2X1 and NOR2X1, they are essentially connected as inverters if the inputs are shorted together. Hence, the same analogy could be extended for NAND2X1 and NOR2X1 gates. The failure has been measured by a 200 point Monte Carlo simulation (with process variation and mismatch) for increasing VDDD while measuring the samples falling outside the acceptable lower limit (125mV) and upper limit (VDDD-125mV). The results are displayed in Table 3.10, 3.11, 3.12 respectively for INVX1, NAND2X1 and NOR2X1.

Table 3.10 Failure Rate for INVX1 vs increasing VDDD(200pt MC simulation)

VDDD (mV)	Vtrip_Lower Bound (mV)	Vtrip_Upper Bound (mV)	Vtrip_Inverter (mV)	Vtrip_Inverter_ Mean (mV)	Vtrip_Inverter_ Sigma (mV)	No of inverter out of range	Inverter_ Faliure Rate%
300	125	175	150	150.1	15.674	33	16.5
320	125	195	160.1	160.224	15.7047	11	5.5
340	125	215	170.2	170.367	15.7314	6	3
360	125	235	180.3	180.465	15.755	0	0

Table 3.11 Failure Rate for NAND2X1 vs increasing VDDD(200pt MC simulation)

VDDD(mV)	Vtrip_Lower Bound (mV)	Vtrip_Upper Bound (mV)	Vtrip_NAND (mV)	Vtrip_ NAND_ Mean(mV)	Vtrip_NAND_ Sigma (mV)	No of NAND out of range	NAND_Faliure Rate%
300	125	175	149.8	149.364	15.1059	44	22
320	125	195	160.2	159.746	15.1339	11	5.5
340	125	215	170.6	170.112	15.158	6	3
360	125	235	181	180.463	15.1797	1	0.5

Table 3.12 Failure rate of NOR2X1 vs increasing VDDD(200pt MC simulation)

VDDD(mV)	Vtrip_Lower Bound(mV)	Vtrip_Upper Bound (mV)	Vtrip_NOR (mV)	Vtrip_NOR_ Mean(mV)	Vtrip_NOR_ Sigma(mV)	No of NOR out of range	NOR_Faliure Rate%
300	125	175	150	148.989	11.1461	8	4
320	125	195	160.1	159.041	11.1591	7	3.5

340	125	215	170.2	169.068	11.1681	2	1
360	125	235	180.2	179.006	11.1738	0	0

It is clearly observable that the failure rate for INVX1, NAND2X1 and NOR2X1 is zero at VDDD=360mV for CMOS logic. The reason is, the trip point(V_{Trip}) distribution Mean(μ) shifts to a higher value while the Sigma(σ) changes insignificantly. However, we can also decrease the failure rate by increasing NOF(area) of both NMOS and PMOS. This is shown in Table 3.13 where we measure the Vtrip variation of an Inverter with increasing NOF for both NMOS and PMOS. It shows that sigma_Vtrip actually decreasing w.r.t. increasing NOF proportional to 1/SQRT(WL) as expected.

Table 3.13 Change in INVX1 Failure Rate with increasing device fingers at VDDD=300mV

Inverter NMOS Width	Inverter NMOS Length	Inverter NMOS NOF	Inverter PMOS Width	Inverter PMOS Length	Inverter PMOS NOF	Vtrip_Inverter	Sigma_Vtrip_Inverter	Mean_Vtrip_Inveter	Failure Rate %
220	180	1	220	180	2	150	15.674	150.1	16.5
220	180	2	220	180	4	148.3	13.42	148.53	6.5
220	180	3	220	180	6	147.8	12.6632	147.789	2.5
220	180	4	220	180	8	147.5	12.2665	147.399	2.5

Now we verify as to which of the following is a better approach to reducing failure rate.

1. Increase VDDD to shift the distribution and Vtrip_Mean to a higher value so that more samples fall within acceptable range. This produces an insignificant change in Sigma_Vtrip.
2. Increase NOF or area of both PMOS and NMOS to reduce Sigma(σ) of Vtrip distribution.

To make the choice, we take the best cases from Table 3.10 and Table 3.13 for an inverter where they have lower failure rates. We take the beta matched INVX1 (1st device sizing in Table 3.13) and make an 11 stage FO4 inverter stage[1] to measure Delay, Pavg, PDP at 360 mV (we obtained a failure rate of zero at VDDD=360mV). We then run the same experiment taking 4th the device sizing for INVX1 from Table 3.13) and measure the same parameter at VDDD=300mV and compare these two cases. The results are displayed in Table 3.14. *Table 3.14 reveals the fact that reducing the failure rate by increasing VDDD is preferred in terms of PDP.*

Table 3.14 PDP measurement for INVX1 from Table 3.10 and Table 3.13

NMOS Width (nm)	NMOS Length (nm)	NMOS NOF	PMOS Width (nm)	PMOS Length	PMOS NOF	Halfpt_diff(ns)	Integrated current(fA)	avg_current (A)	VDD(mV)	Pavg(watt)	PDP (J)
220	180	4	220	180	8	376	27.5	7.31383E-08	300	2.19415E-08	8.25E-15

220	180	1	220	180	2	124.3	8.103	6.51891 E-08	360	2.34681 E-08	2.917 08E-15

3.5 EXTENSION TO T-GATE LOGIC GATES

We next extend our analysis to T-Gate designs and then compare the proposed T-Gate designs with classical CMOS logic. The trip point of T-Gate based NAND2X1 and NOR2X1 is acceptably close to VDDD/2 due to having beta matched inverters as the output stage. In this case varying the device size has no useful effect. The butterfly plot at VDDD=300mV for T-gate NAND2X1 driving T-Gate NOR2X1 and vice versa, is used to obtain the worst case scenario of SNM and plotted (Figure 3.14) side by side with the best case of CMOS topology for comparison. Figure 3.14 clearly shows that standard CMOS logic having better noise margin compared to the T-gate design. Thus verifying that standard CMOS design topology is more robust compared to T-Gate logic designs.

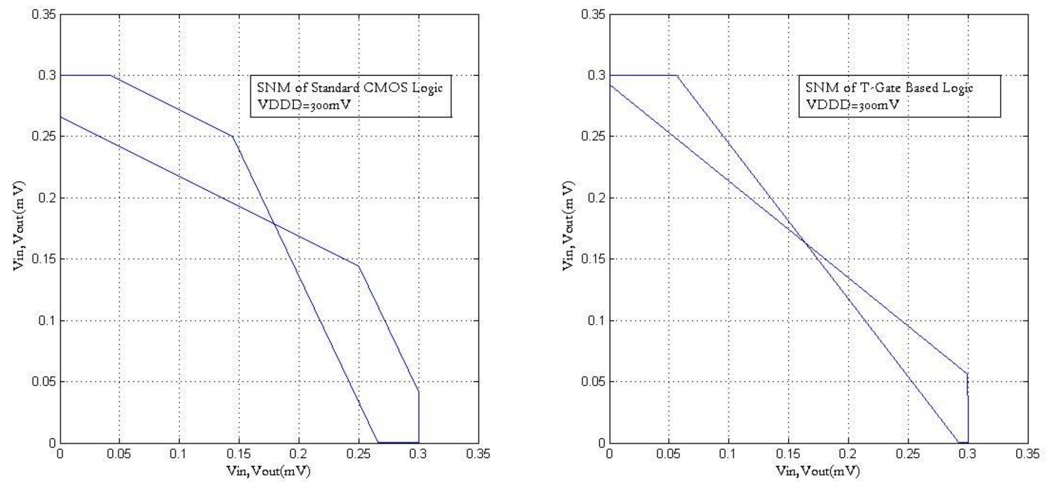

Figure 3.14: Butterflies: best case of CMOS Logic and best case of T-gate Logic

We measure the failure (as defined earlier) rate as described earlier and then attempt to reduce it by increasing VDDD. The results are shown for INVX1, NAND2X1 and NOR2X1 as before, in Table 3.15, 3.16, 3.17 respectively.

Table 3.15 Failure Rate of INVX1 vs Increasing VDDD

VDDD(mV)	Vtrip_Lower Bound(mV)	Vtrip_Upper Bound(mV)	Vtrip_Inverter(mV)	Vtrip_Inverter_Mean(mV)	Vtrip_Inverter_Sigma(mV)	No of inverter out of range	Inverter_Faliure Rate%
300	125	175	150	150.1	15.674	33	16.5
320	125	195	160.1	160.224	15.7047	11	5.5

340	125	215	170.2	170.367	15.7314	6	3

Table 3.16 Failure Rate of T-Gate NAND2X1 vs increasing VDDD

VDDD(mV)	Vtrip_Lower Bound(mV)	Vtrip_Upper Bound(mV)	Vtrip_NAND (mV)	Vtrip_NAND _Mean(mV)	Vtrip_NAND _Sigma(mV)	No of NAND out of range	NAND_Faliure Rate%
300	125	175	147.1	148.564	11.69	18	9
320	125	195	157	158.394	11.878	5	2.5
340	125	215	166.9	168.21	12.0715	0	0

Table 3.17 Failure Rate of T-Gate NOR2X1 vs increasing VDDD

VDDD(mV)	Vtrip_Lower Bound(mV)	Vtrip_Upper Bound(mV)	Vtrip_NOR(mV)	Vtrip_NOR_Mean(mV)	Vtrip_NOR_Sigma(mV)	No of NOR out of range	NOR_Failure Rate%
300	125	175	149	145.242	11.3954	28	14
320	125	195	159.4	155.608	11.5774	2	1
340	125	215	169.8	165.925	11.7501	1	0.5

It is clear that the failure rate for T-gate NAND2X1 and NOR2X1 goes to zero at a lower voltage (340mV) than its standard CMOS equivalent. However, INVX1 does not produce a zero failure rate at VDDD=340mv (From Table 3.15).

Finally we find the optimum operating frequency given a particular VDDD of interest. To do so, we simulate a 7 stage NAND-NOR ring oscillator representing a hypothetical critical path. We find out the optimum clock frequency that can propagate through this loop. Also the drift in frequency is noted as we move from tt process corner to ss process corners. The results are summarized in Table 3.18.

Table 3.18 Ring Oscillator frequency vs increasing VDDD

Design Topology	VDDD(mV)	Ring Oscillator Output Freq_TT Corner(MHz)	Ring Oscillator Output Freq_SS Corner(MHz)	% Frequency Degradation
T-Gate Design	300	1.05	0.4816	54.13333333
T-Gate Design	320	1.573	0.7344	53.3121424
T-Gate Design	340	2.325	1.105	52.47311828
T-Gate Design	360	3.382	1.638	51.56712005

T-Gate Design	380	4.838	2.392	50.55808185
T-Gate Design	400	6.789	3.434	49.41817646
CMOS Standard Logic	300	2.27	1.006	55.68281938
CMOS Standard Logic	320	3.403	1.543	54.65765501
CMOS Standard Logic	340	5.012	2.331	53.49162011
CMOS Standard Logic	360	7.243	3.495	51.74651388
CMOS Standard Logic	380	10.25	5.039	50.83902439
CMOS Standard Logic	400	14.18	7.19	49.29478138

It is clear from Table 3.18 that for a particular VDDD standard CMOS Logic gate design topologies operate at higher frequency and have better computational speed i.e. reduced delay than their equivalent T-Gate Logic designs. The T-Gate logic cells seems to have somewhat narrower distribution of V_{Trip} w.r.t. Process variation and mismatch which causes the failure rate of the gate to reduce with a faster rate than that of its equivalent CMOS counterpart. But the CMOS logic gates show better SNM at any VDDD of operation i.e. more robust and suitable for low power operation.

3.6 CHAPTER SUMMERY

The T-Gate cells have narrower VTrip distribution than its equivalent CMOS logic i.e. with increasing VDDD, T-Gate logic gates show better rate of reduction of failure. However, CMOS logic shows better static noise margin (SNM) at any VDDD of operation and hence more suitable for low power operations. Failure can be reduced by either increasing VDDD or by increasing device area. Increasing VDDD shifts Mean of VTrip distribution to a higher value with insignificant change in Sigma of the distribution. Increasing area causes reduction in Sigma of VTrip distribution and narrows down the VTrip distribution while results in insignificant change in Mean of the distribution. Increasing VDDD is a better choice than increasing area in order to reduce failure as it causes improved power delay product (PDP).

CHAPTER IV

I_{Off} COMPARISON BETWEEN T-GATE AND CMOS LOGIC

4.1 INTRODUCTION

In a standard CMOS logic gate Ion is supplied by the pull up network and Ioff is supplied by the pull down network or vice versa. The effective load current (Ion-Ioff) drives the output load to change or discharge. In super-threshold design (circuit is operating in velocity saturation) Ion/Ioff ratio is large enough due to much higher Ion w.r.t. Ioff and more over the impact of process variation on Ion/Ioff is less significant. However, in sub-threshold the degradation of Ion/Ioff created by the process variation at the worst VT corner may cause logic failure at given frequency.

A Comparison of T-Gate based logic gates with its standard CMOS logic equivalent in terms of OFF current(Ioff) has been provided later in this chapter. The current-equation for sub-threshold is given as

$$Id = I_0 . \exp\frac{(VGS-VT)}{nUT}(1-\exp(\frac{-VDS}{UT}))$$

Ioff is the current(Id) at VGS=0V.

A methodology of measuring the active current variability with increasing width has been presented in [1, 2]. However, it shows active current variability for individual and stacked transistors but does not show the variation of Ion/Ioff which is of greater importance. Furthermore, it does not consider any impact of device length. Hereby we investigate the Ion/Ioff change with increasing device geometry and try to find out an optimum VDDD depending on our variability tolerance. We consider Ion being supplied by pull up network and Ioff being supplied by pull down network or the other way because that is a more de facto parameter.

4.2 EXPERIMENT SETUP

The experiment setup has been shown in Figure 4.1. The gate of the NMOS and PMOS both are connected to VDDD=300mv to supply Ion and Ioff respectively. We calculate Ion/Ioff by calculating the dc current of the transistors. Then run 200 point Monte-carlo simulation to verify Mean and Sigma(SD) of distribution of Ion/Ioff consideration process variation. Sigma (SD) of distribution is expected to reduce as proportional to inverse of square root of device area. After this, we run the same experiment by altering the gate connection and run the same steps while

increase channel width from 220nm to 460nm with step size of 40nm and increase channel length for each width from 180nm to 360nm with step size of 30nm.

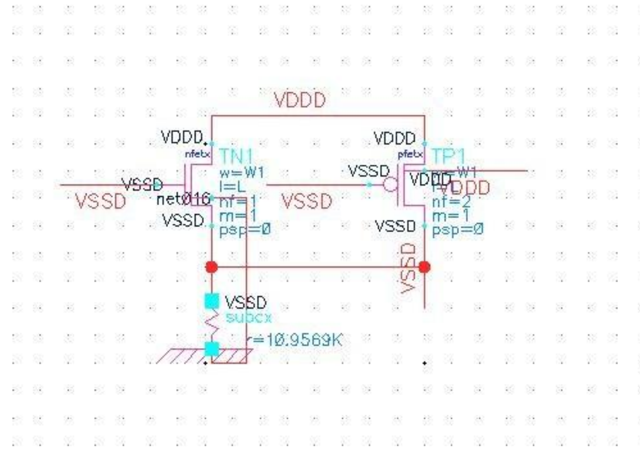

Figure 4.1 Experiment Setup

4.3 OBSERVATIONS

The Ion/Ioff vs device geometry obtained from the experiment has been plotted in Figure 4.2(PMOS->Ion, NMOS-> Ioff) and Figure 4.3(NMOS->Ion, PMOS-> Ioff). Figure 4.2 shows that Ion/Ioff decreases with increasing Channel Length but increases with increasing Channel width. Figure 4.3 shows completely different pattern with Ion/Ioff increasing with increasing channel length. This leads to the investigation of a common line of solution where both these Ion/Ioff are the same. Beyond that line of solution we sacrifice either of these two Ion/Ioff as we go for geometry change. If we maximize Ion/Ioff for output rise, we sacrifice in terms of fall time which might cause operating frequency limitation and failure. However, to do this we subtract the two matrix, plot the surface and the contour and find the points where the results are close to zero because that is the point where both this Ion/Ioff are same(line of solution).

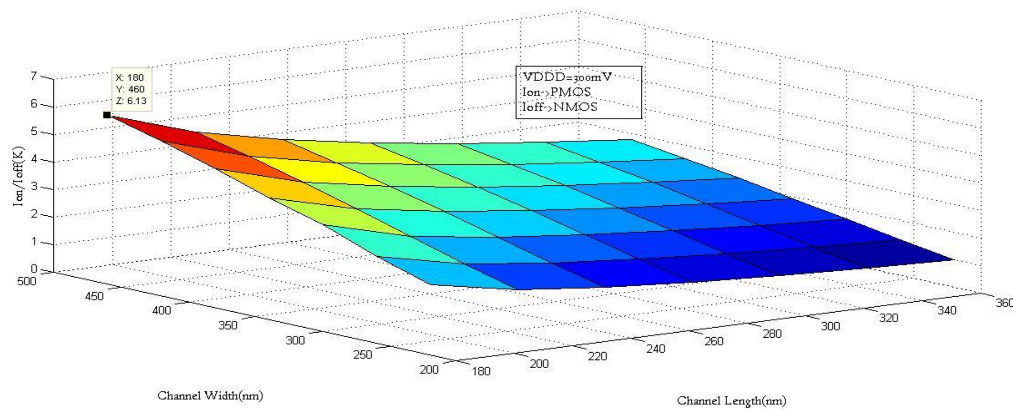

Figure 4.2 Ion/Ioff , PMOS supplying Ion and NMOS supplying Ioff

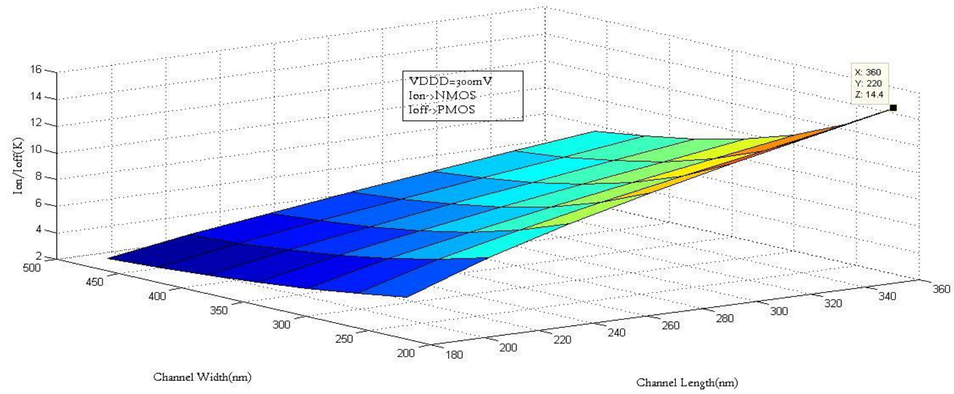

Figure 4.3: Ion/Ioff, NMOS supplying Ion and PMOS supplying Ioff

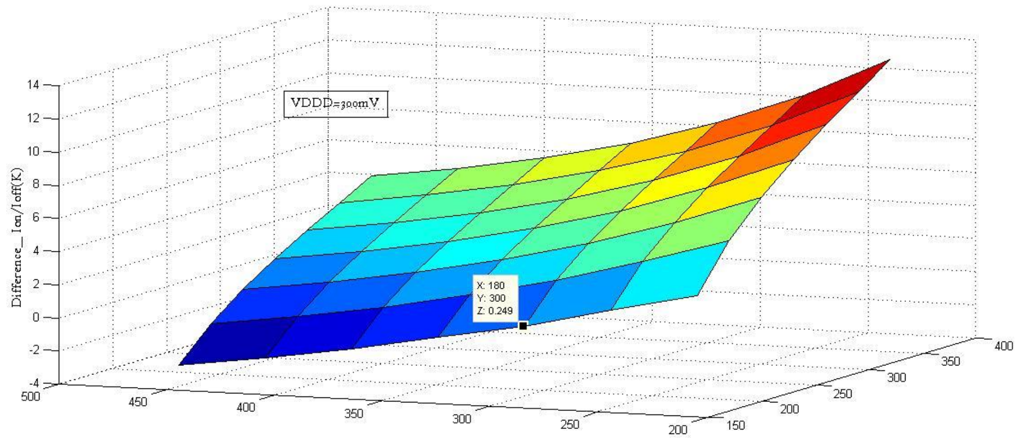

Figure 4.4: Surface plot for Difference_(Ion/Ioff)

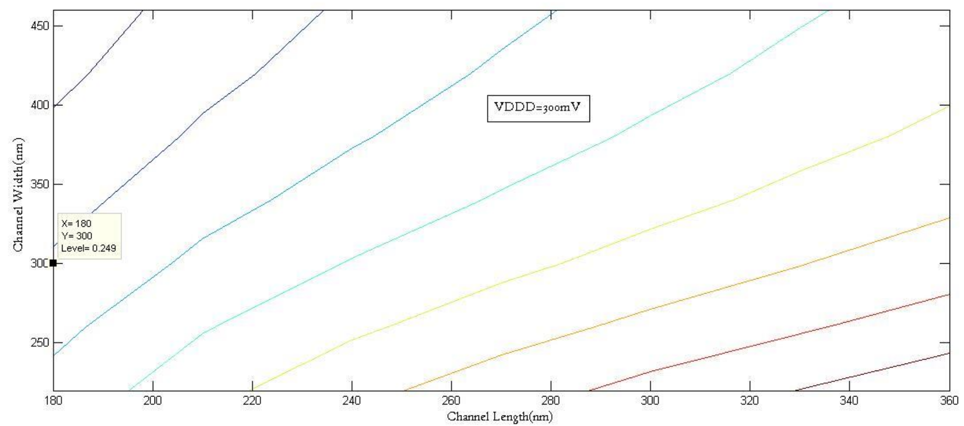

Figure 4.5: contour plot for Difference_(Ion/Ioff)

From Figure 4.4 and Figure 4.5, we find that at Width=300nm and length=180nm this two Ion/Ioff are closest to equal. However, so far we haven't addressed the issue of variability and have be taken into account to determine acceptable Sigma(SD) for Ion/Ioff variation due to process. Figure 4.6 and Figure 4.7 shows Sigma_(Ion/Ioff) for both of the above mentioned cases.

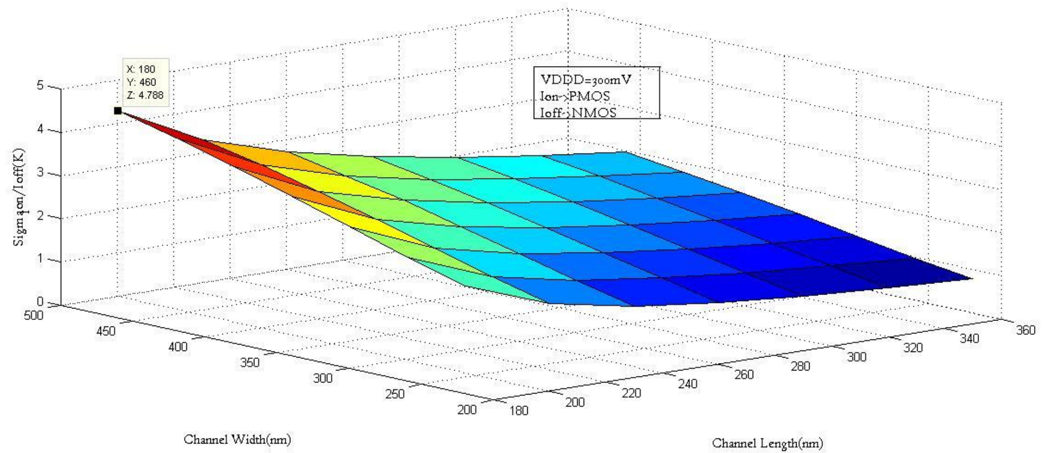

Figure 4.6 Sigma(Ion/Ioff), Ion->PMOS, Ioff-> NMOS

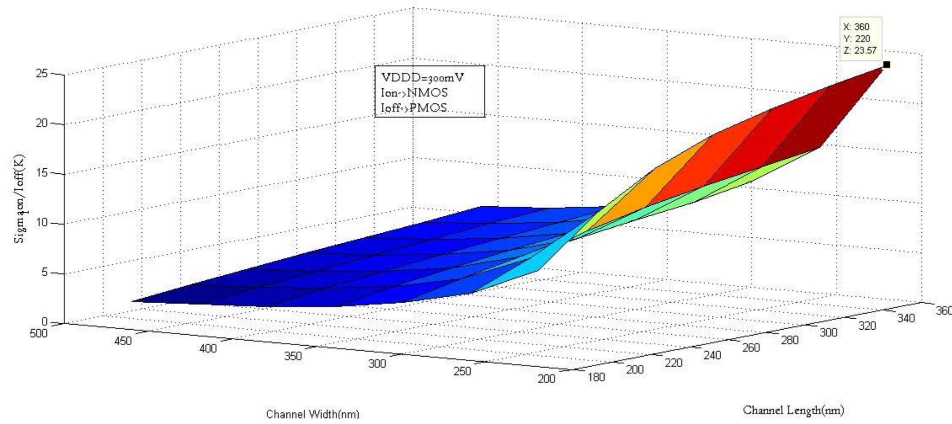

Figure 4.7: Sigma(Ion/Ioff), Ion->NMOS, Ioff-> PMOS

Figure 4.6 and Figure 4.7 shows complete different trend of sigma variation. We also investigate the Mean of Ion/Ioff and Sigma at width=300nm and Length =180nm for both of the cases which is shown in Table 4.1 below.

Table 4.1 Ion/Ioff at width=300nm and Length=180nm

Ion supplier	Width(nm)	Length(nm)	Mean_Ion/Ioff (K)	Sigma(Ion/Ioff) (K)
PMOS	300	180	4.467	3.281
NMOS	300	180	5.73	5.154

The above table shows that the Sigma (Ion/Ioff) is almost comparable to the Mean(Ion/Ioff) of distribution. By considering 3 Sigma variations it needs to be determined whether the degraded Ion/Ioff is acceptable for a particular operating frequency or not. If not, the impact of variability has to be suppressed by increasing VDDD. The change in device geometry impact the magnitude of Sigma of a distribution whereas increasing supply voltage shifts the distribution along with its Mean to a higher value such that the magnitude of the variability is acceptable despite of insignificant change in Sigma(σ). Hereby Sigma/Mean is our statistical parameter of greater concern when we scale up power supply. Figure 4.8 shows the change of Mean and Sigma with increasing VDDD at width=300nm and Length=180nm.

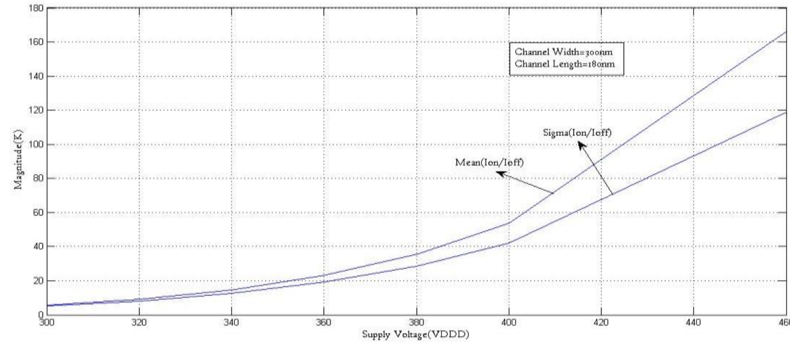

Figure 4.8: Mean and Sigma of Ion/Ioff, Ion->NMOS, Ioff-> PMOS vs VDDD

From the Figure 4.8, it is clear that Mean of the distribution shifts to a higher value with a greater slope than that of Sigma and eventually Sigma starts to separate. So if we take Sigma/Mean as our concerned parameter, it is expected to decrease with increasing VDDD and this is shown in Figure 4.9 and Figure 4.10. Ion/Ioff is a critical parameter as it determines the active drive current and consequently the output rise time of a logic gate. The relative value of Sigma(Ion/Ioff) w.r.t. Mean(Ion/Ioff) is more important because with an higher Mean we are more tolerant to variation.

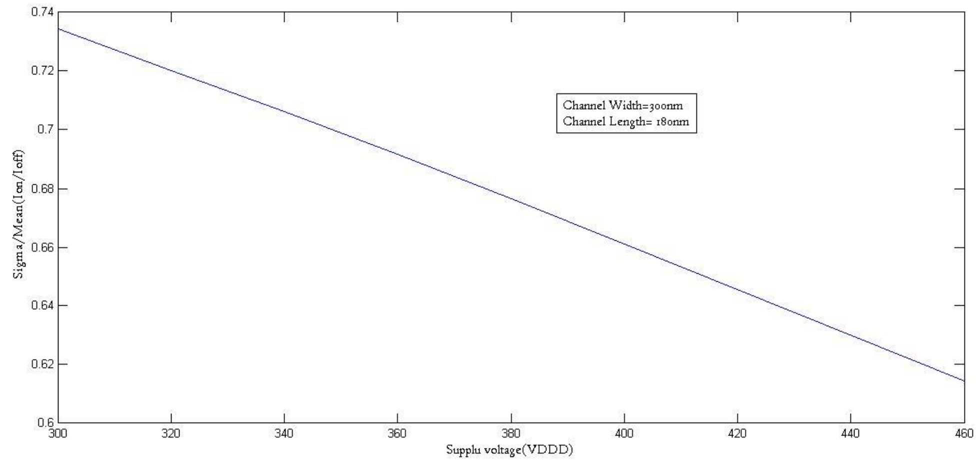

Figure 4.9: Sigma (Ion/Ioff) vs VDDD, Ion-> PMOS, Ioff->NMOS

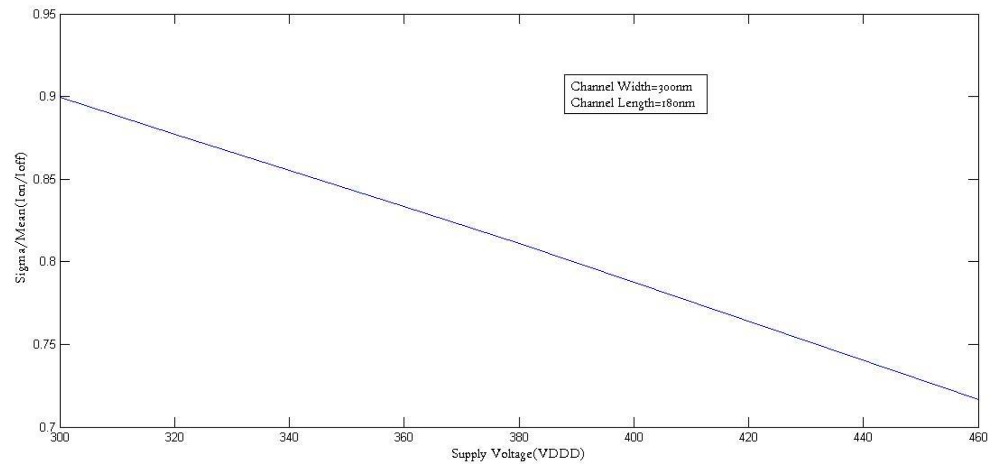

Figure 4.10: Sigma (Ion/Ioff) vs VDDD, Ion-> NMOS, Ioff->PMOS

The simulation result plotted in Figure 4.9 and Figure 10 comes into agreement to our expectation mentioned earlier. A comparison of Ioff between standard CMOS based logic and T-Gate based logic is provided next in this chapter.

4.4 I_{OFF} COMPARISON BETWEEN CMOS AND T-GATE LOGIC

Comparison of IOFF two input T-gate and CMOS NAND:

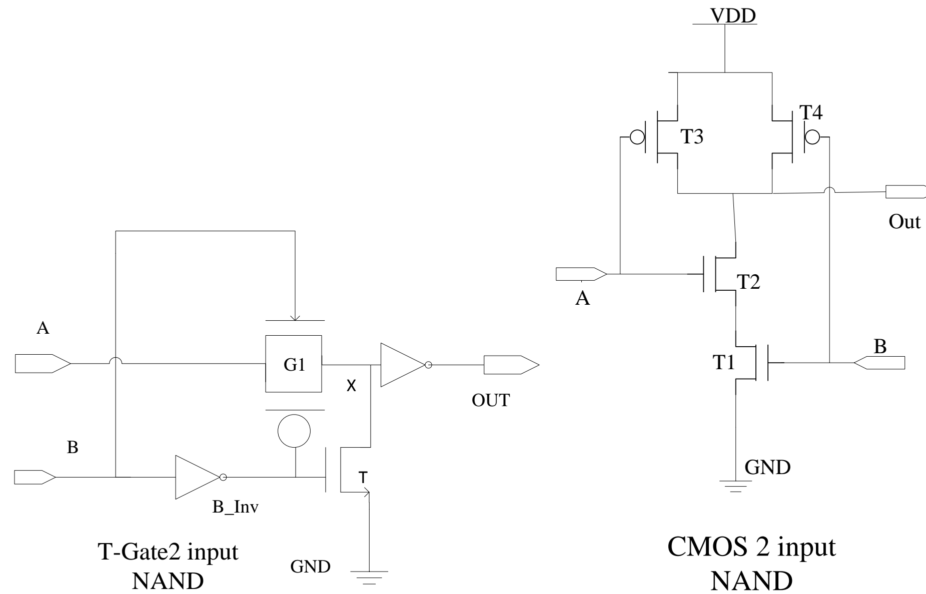

Figure 4.11 T-gate(left) and CMOS(right) two input NAND

Analysis: from Figure 4.11

When A=0,B=0: For the T-gate based design there are two IOFF path for this particular input combination, The NMOS of the input inverter and the output inverter will provide sub threshold current path to the ground. PMOS of the output inverter will charge up the output load with ION. In contrary for the CMOS equivalent design there will be only oneIOFF path through NMOS T1 and T2 to ground. Both the PMOS in the pull up network in CMOS design will be turned ON and ILoad=(2xION-IOFF) will charge up the output load.

When A=0,B=1: In this case the NMOS 'T' of the T-gate based design will causeIOFF to ground along with the NMOS of the output transistor.PMOS of the output inverter will charge up the output load.However inverter at the input B will cause another IOFF to ground. So there will be three contributors to the IOFF to ground for T-gate based design for this particular combination. For the CMOS based design, at this input combination T2 will cause IOFF current which will flow through T1 to ground. In the pull up network T4 will provide a path for IOFF which will compensate for the current through T2 and T1. T3 will be turned ON and charge up the output load with ION.

When A=1,B=0:In caseof T-gate design T-gate G1 will provide path for IOFF that will flow through NMOS -T . NMOS of output inverter will also cause aIOFF to ground. Inverter generating B_Inv is another source of IOFF.So there are three contributors. For the CMOS design T1 will cause IOFF to ground but this will be compensated by current through T4. T3 will charge up the output load.

When A=1,B=1: In the T-gate design NMOS -T will be responsible for IOFF to ground and the inverter generating B_Inv will also cause IOFF.PMOS of the output inverter will provide another path for IOFF. So in this case (ION-IOFF) at output will discharge the output load to logic 0.Whereas, in the CMOS design T1 and T2 will be turned ON and T3 and T4 will cause IOFF. So (ION-2xIOFF) will discharge the output load to logic zero

Comparison of IOFF between CMOS 2 input NOR and T_Gate2 input NOR

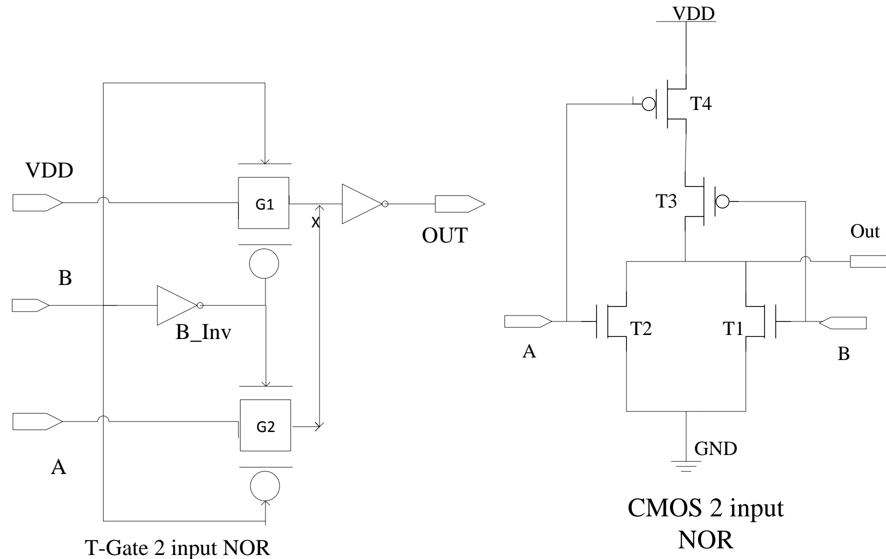

Figure 4.12 T-gate(left) and CMOS(right) two input NOR

Analysis: From Figure 4.12

When A=0,B=0: For the T-gate Based design, T-gate G1 will be off and G2 will be ON, however G1 will provide path for IOFF as input of G1 tied to VDD. There will be another current path through G1 via node X to G2 . But Input inverter at input B will provide another path to IOFF. The NMOS of the output inverter will provide IOFF to ground. So overall it will be three IOFFpath to ground. In contrary, In the CMOS based design both T1 and T2 will provide separate IOFF path to ground. The PMOS in the pull up network will be turned ON and (ION-2xIOFF) will charge up the output load.

When A=0,B=1:For T-Gate Based design G1 is turned ON and G2 is turned OFF. So there will be one IOFF path through G2 as input A is connected to logic zero. Inverter at output is another source for IOFF . For the CMOS based design T2 is providing path for IOFFpath to ground but this will be compensated by the IOFF through T4 and T3. T1 will discharge the output load to logic zero.

When A=1,B=0: G1 is OFF and G2 is ON. The twoIOFFpath for this particular input combination would be through the NMOS of the inverter at the input terminal B and through the PMOS at the output inverter. Whereas in the CMOS based design T1 is providing path for IOFF

to ground but this will be compensated by the IOFF through T4 and T3. T2 will discharge the output load to logic zero.

When A=1,B=1:Here IOFF will be caused by the inverter at the output and at the input terminal B,in case of T-Gate based design. In the CMOS design T1 and T2 will be ON and T3 and T4 will account for IOFF. In this case (2xION- IOFF) will discharge the output load to logic zero.

Comparison of IOFF between CMOS 2 input XOR and T_Gate 2 input

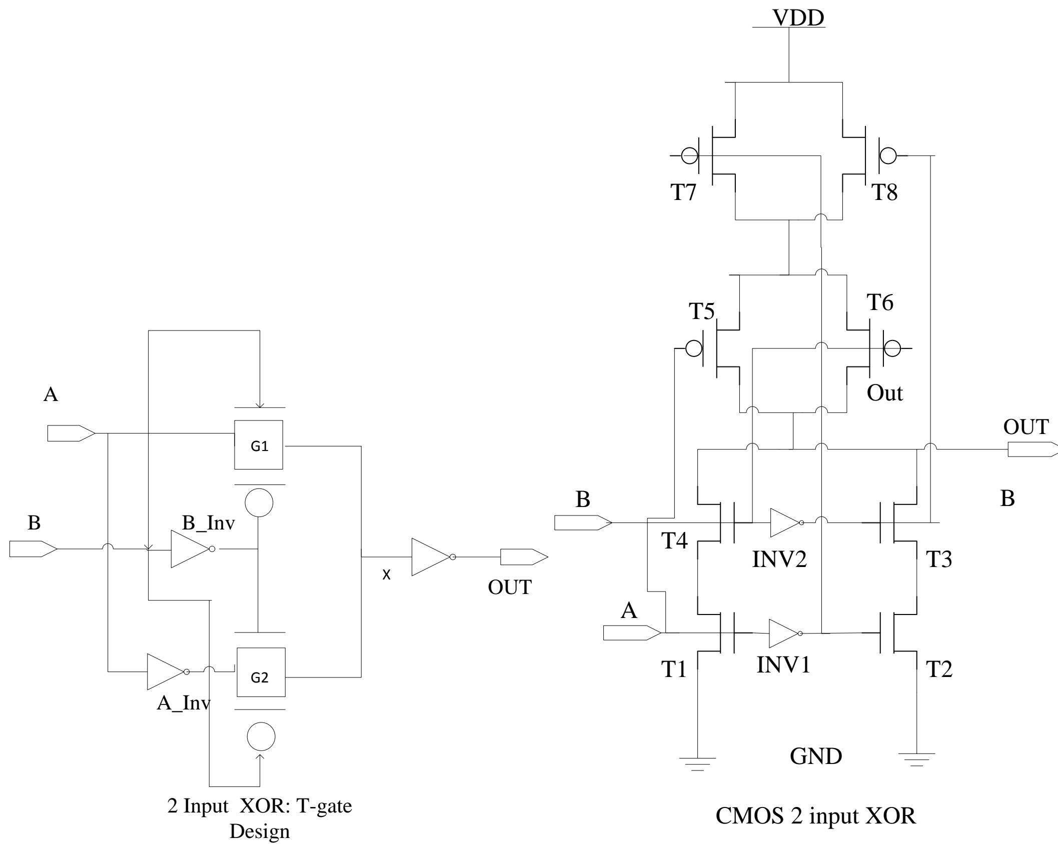

Figure 4.13 T-gate(left) and CMOS(right) two input XOR

Analysis: From Figure 4.13

When A=0,B=0: For the T-gate based design G1 is OFF and G2 will be ON. The two NMOS of the inverter generating B_Invand A_Invwill provide paths for IOFF to ground. Inverter at the output will also cause an IOFF. G1 will provide another path for IOFF as A is at logic zero and node x is at logic 1. So overall there are four IOFFpaths to ground. This might pull down node x a bit. For the CMOS equivalent design T1 and T4 will construct a path for IOFF to ground. T5 and T6 will be ON and IOFF will flow through T7 and T8 in the pull up network. This IOFF in the pull up network will counterbalance the IOFF in pull down network through T4 and T1. T3 and T2 will pull the output load down to logic zero. However INV1 and INV2 both will cause IOFF.So there will be overall threeIOFFflowing to ground.

When A=0,B=1: In case of T-gate based design, G1 will be turned ON and G2 will be turned OFF.NMOS of Inverter generating A_Inv(NMOS)and B_Inv(PMOS) will causeIOFFflow.G2 will be another path for IOFF as A_Inv is at logic 1 node x at logic 0. Also the NMOS of the output inverter will also be a path for IOFF to ground. So for this particular combination again we see four IOFF paths to ground. For the CMOS design T1 and T3 will be OFF and T2 and T4 areON. However both these tails now provide IOFFpaths to ground through T1 and T3 respectively. The output load will be charged up to logic 1 through T5 and T8 in the pull up network as they are ON. However the IOFFthrough T7 and T6 will compensate for one of the two IOFF in the pull down network. Also INV1 and INV2 will cause two IOFFs to ground. So overall there will be four IOFFpath to ground.

When A=1,B=0: G1 will be OFF and G2 will be ON for this particular input combination in T-Gate design. NMOS of inverter generating B_inv will cause IOFF to ground.G2 will also provide a path for IOFF. G1 is ON and A is at logic 1. So there will be another IOFF from A to ground via G1, G2, NMOS of the inverter generating A_Inv. This will try to pull node x low.In addition we have to consider the IOFFof the output inverter. So overall there are fourIOFF paths to ground in case of T-gate design. For the CMOS design T1 and T3 will be ON and T2 and T4 will be OFF. However there will be two IOFF paths through T4 and T2. T6 and T7 in the pull up network will be ON and will charge up the output load to logic 1. IOFF through T5 and T8 will compensate for one of the IOFF paths in the pull down network. So overall there is one IOFFpath to ground.INV2 and INV1 both will cause IOFFflow.So we find fourIOFF path to ground.

When A=1,B=1:G1 will be ON and G2 will be OFF in this case in the T-gate design. However, G2 will cause an IOFF flow through the NMOS of the inverter generating A_Inv pulling node x down. Also we need to consider the IOFF of the output inverter. So we have twoIOFF paths to ground in this case. For the CMOS design T1 and T4 both will be ON and T2 and T3 will be OFF and will cause one IOFF current path to ground. T5 and T6 will be OFF but the IOFF flowing through then will compensate for the IOFF through T2 and T3. T1 and T4 will discharge the output load to logic 0.INV2 and INV1 both will cause IOFF flow. So it will be threeIOFF path to ground.

Comparison of IOFF between CMOS 2 input XNOR and T-Gate 2 input XNOR

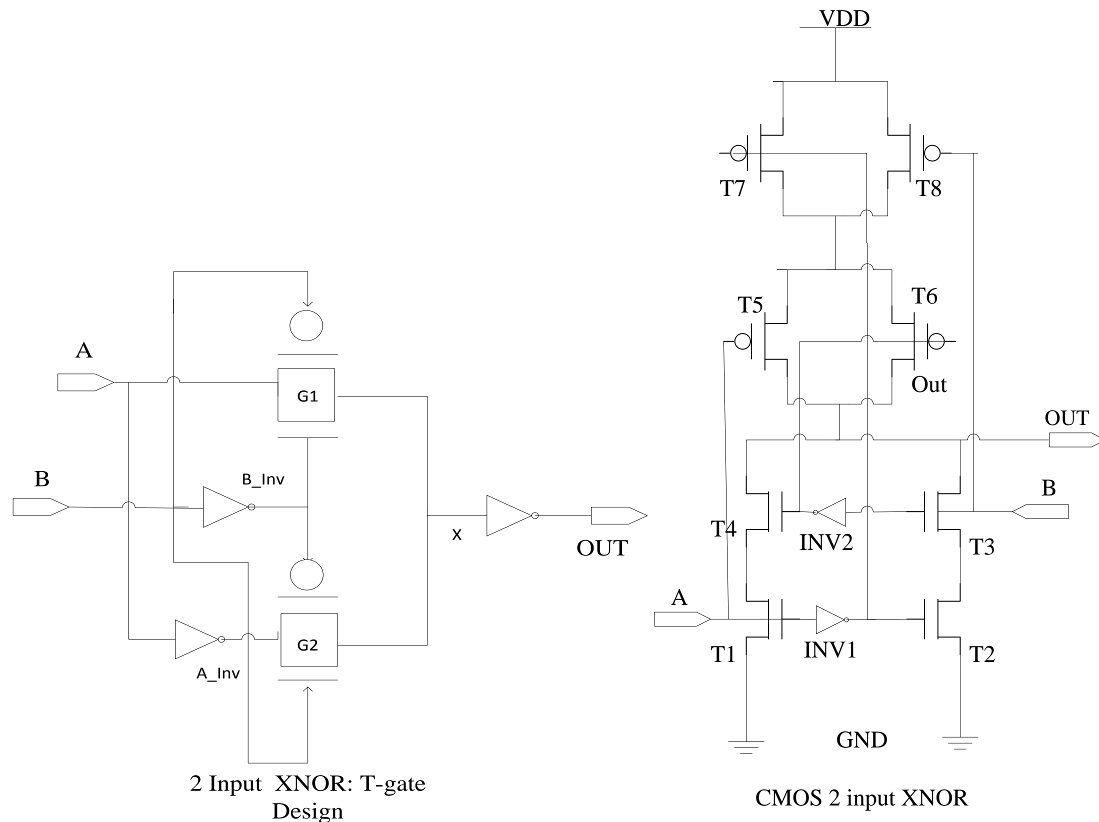

Figure 4.14 T-gate(left) and CMOS(right) two input XNOR

Analysis: From Figure 4.14

When A=0,B=0:For the T-gate design G1 will be ON and G2 will be OFF. NMOS of inverters generating A_Inv and B_Inv both will cause one IOFF to ground. Also the output inverter will cause one IOFFto ground through NMOS. Another IOFFpath will be from Inverter(generating A_Inv)to A via G2 and G1.So overall four IOFF would be flowing in this case. For the CMOS design, T1 and T3 will be OFF and T2 and T4 will be ON. However these two tail will cause IOFF to ground. INV1 and INV2 will cause another 2 IOFF currents to ground. In the pull up network T5 and T8 will be ON and will charge up the load to logic 1. T6 and T7 will be OFF and will cause IOFF. So overall in this case there will be four IOFFflow.

When A=0,B=1: In case of T-gate design, G2 will be ON and G1 will be OFF. NMOS of inverter generating A_Invand PMOS of Inverter generating B_Inv will cause two flow. However G1 will cause one IOFF as node x would be at logic 1 and A is at zero. Output inverter also causes another IOFF flow. So there are fourIOFF to ground. For the CMOS design T1 and T4 will be OFF will cause one IOFF to ground .INV1 and INV2 will cause twoIOFFto ground. T3 and T2

will pull the output load down to logic 0. T5 and T6 will cause IOFF . So there are threeIOFF to ground for this particular combination.

When A=1,B=0: G1 is selected and G2 is deselected. Inverters generating B_Invand A_Inv and at the output will each causeone IOFFto ground. G2 will cause another IOFF to flow through the NMOS of the inverter generating A_Inv and will pull down node x a bit. So there are fourIOFFpaths to ground. For the CMOS design T1 and T4 will be ON and T2 and T3 will be OFF and will cause IOFF to ground. INV2 and INV1 each will cause one IOFFto ground. T5 and T6 will be OFF and will cause IOFF. So overall we get three IOFFflowing to ground.

When A=1,B=1: G2 will be selected and G1 is deselected. There is one IOFF flow from A to ground via G1, G2 and NMOS of the Inverter generating A_Inv. NMOS of the output inverter will cause another IOFF flow to ground. Both of the input inverters will cause one IOFF each. So we get fourIOFF path to ground. For the CMOS design T1 and T3 will be ON and T2 and T4 will be OFF. Both of these tails in the pull down network will cause IOFF to flow to ground. T6 and T7 in the pull up network will be ON and will pull the output load to logic high. However T5 and T8 will cause IOFF to flow. IOFFdue to INV1 and INV2 also need to be considered. So we get overall four IOFFflowing to ground.

A comparison is given considering all the input combinations are equally probable and having probability of occurrence 25%. See Table 4.2

Table 4.2 Comparison of IOFFs between T-Gate and CMOS logic Gates

Gate Type	No of Inputs	Input Combination	No of IOFF for T-Gate Design	No of IOFF for CMOS Design	Comparison
NAND	2	00	2	1	CMOS design is better
		01	3	1	
		10	3	1	
		11	3	2	
NOR	2	00	3	2	CMOS design is better
		01	3	1	
		10	2	1	
		11	2	1	
XOR	2	00	4	3	CMOS design is better
		01	4	4	
		10	4	4	
		11	4	3	
XNOR	2	00	4	4	CMOS design is better
		01	4	3	
		10	4	3	
		11	4	4	

Comparison of IOFF between 2:1 CMOS and T_Gate MUX.

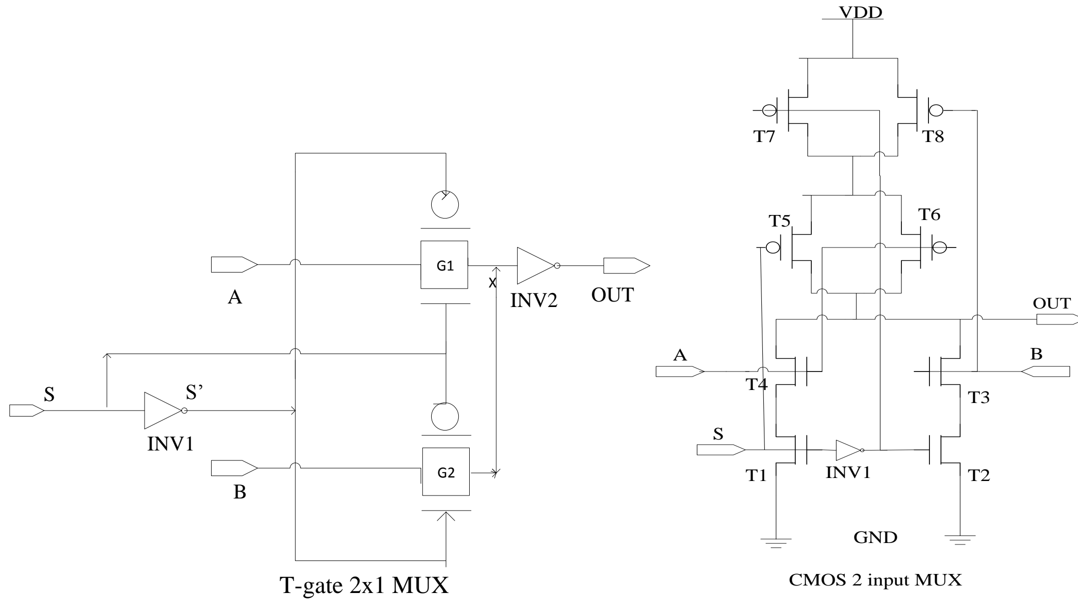

Figure 4.15 T-gate(left) and CMOS(right) 2:1 MUX

Analysis: From Figure 4.15

The OFF current comparison has been shown below in Table 4.3

Table 4.3 IOFF Comparison for T-gate and CMOS 2:1 MUX

Gate Type	No of Inputs	S/Select	Input Combination(A,B)	IOFF contributors in CMOS design	Total of IOFF-CMOS	IOFF contributors in T-Gate design	Total No o	Conclusion
MUX	2	0	00	INV1 Through T1 and T4 Through T2 and T3 Through T7	4	INV1 INV2	2	T-gate design is better
			01	INV1 Through T1 and T4 Through T7 Through T8	4	INV1 INV2 From B to A via G2 and G1	3	
			10	INV1 Through T1 and T4 Through T2 and T3 Through T8 and T6	4	INV1 INV2 From A to B via G1 and G2	3	
			11	INV1 Through T4 and T1 Through T7 and T6 Through T8 and T6	5	INV1 INV2	2	
		1	00	INV1 Through T1 and T4 Through T2 and T3 Through T5	4	INV1 INV2	2	
			01	INV1 Through T1 and T4 Through T2 and T3 Through T8 and T5	4	INV1 INV2 From B to A via G2 and G1	3	
			10	INV1 Through T3 and T2 Through T5 Through T6	4	INV1 INV2 From A to B via G1 and G2	3	
			11	INV1 Through T3 and T2 Through T8 and T6 Through T8 and T5	7	INV1 INV2	2	

4.5 CHAPTER SUMMERY

Ion/Ioff is a dynamic issue as it determines the active load current and hence rise time for a given load whereas Ioff is a static issue as it determines the static power dissipation and degradation in output logic level. Ion/Ioffi is poor in sub-threshold and variability makes situation worse. The relative ratio of Sigma(σ)/Mean(μ) for Ion/Ioff (for either rise or fall or both) can be reduced by increasing VDDD to an operating value of users choice. Except for the MUX2X1, the other CMOS logic gates under consideration should perform better in terms of Ioff than its equivalent T-Gate logic.

CHAPTER V

DEVICE SIZING FOR MINIMUM POWER DELAY PRODUCT

5.1 INTRODUCTION

Sub-threshold operation is popular for applications with a tight power budget and computational speed is a lesser concern. Minimum power consumption would be a desired state to achieve if delay was not an important factor of consideration [13]. The goal is to minimize energy while maintain adequate delay performance is. *Ideally the design has the leverage to take the desired energy delay tradeoffs at design.* Hence power delay product(PDP) i.e. energy is a more fundamental factor to be investigated as the supply voltage is scaled down to near threshold or below threshold voltage of MOSFET. Tertz et al [14] presents an analytical solution for above threshold minimum EDP- device sizing. A numerical solution and model has been provided in [16] that deals with sub-threshold minimum energy operation whereas [15] gives an analytical solution for the same and introduces minimum energy operation. Schrom et al [19] shows that minimum VDDD operation is possible for a logic gate when both PMOS and NMOS are sized to carry equal current i.e. they are β matched. However [1] explains that minimum VDDD operation does not necessarily ensure minimum energy operation. The total energy consumed by a logic gate could be summarized by the formula [1], Section 1.3.2]

ET = EDYN+ ELEAK = $(Ceff.VDDD^2) + (Weff.I_{leak}.VDDD.td.L_{DP})$

Where, Ceff if the effective capacitance, f being the operating frequency, I_{leak} and td are the leakage current and delay respectively of a characteristic inverter, L_{DP} is the logic path depth

With decreasing VDDD dynamic energy(EDYN) consumption goes down quadratically whereas leakage current (I_{leak}) is proportional to DIBL. On the contrary, delay (td) increases exponentially, resulting an increment in total energy consumption. This moves the optimum operating VDDD (where we get minimum energy operation) to a higher voltage rather than minimum VDDD[1]. Kwong et al [1] has investigated the impact of varying β ratio against energy consumption and delay performance in sub-threshold. It has been shown in [1] that β ratio=1 i.e. Wp=Wn is the optimum solution for energy consumption and delay for any VDDDs of choice in sub-threshold. However keeping β ratio=1, upsizing both PMOS and NMOS simultaneously only causes more energy consumption and increased delay as shown in [1] and β ratio=1(See Figure 5.4) with minimum device width is the optimum solution for energy consumption and delay (and hence PDP) at any VDDD (both for optimum VDDD and not optimum VDD of operation) of choice in

sub-threshold. However, no effect of Channel length has been considered to date to the best of author's knowledge till Jindan et al[17] introduces the concept of Gate Length Biasing(GLB) in order to reduce leakage current. It's been stated in [17] that increasing channel length increases the threshold voltage and hereby reduces leakage with small performance impact which is an direct contradiction to our findings as discussed later in this chapter. Ran et al [18] shows that threshold voltage is a function of device geometry. The combined impact of device finger Width and Length variation aiming to achieve an optimum PDP is yet to be investigated.

5.2 EXPERIMENT SETUP

As explained in [1] a 11 stage FO4 inverter chain has been selected as the design under test(DUT) as shown in Figure: 5.1. Delay has been defined as the time taken as the edge to edge propagate through the stages and reach output[1]. The current drawn by the power supply has been measured by integrating the current over the delay period (designated as Iintegrated) and Iavg has been measured (Iavg=Iintegrated/delay period) to calculate Pavg (Pavg=Iavg*VDDD). PDP can now be measured as a product of Pavg and delay. VDDD has been taken as 300 mv which is well below the threshold voltage for a minimum sized device and β ratio=1 has been considered [1].

5.3 ALGORITHM FOR PDP VS DEVICE GEOMETRY MEASUREMENT

Start Loop: Increase both Wn(NOF=1) and Wp(NOF=1) starting from 220nm to 440nm with step size of 20nm and β ratio=1.

Start Loop: Increase L from 180nm to 378nm with step size of 18nm.

Measure VTn, VTp, Delay , Iintegrated, Iavg, Pavg, PDP

End Loop

End Loop

We obtain 144 data points out of this experiment and plot them with the help of MATLAB script (given in Appendix A).

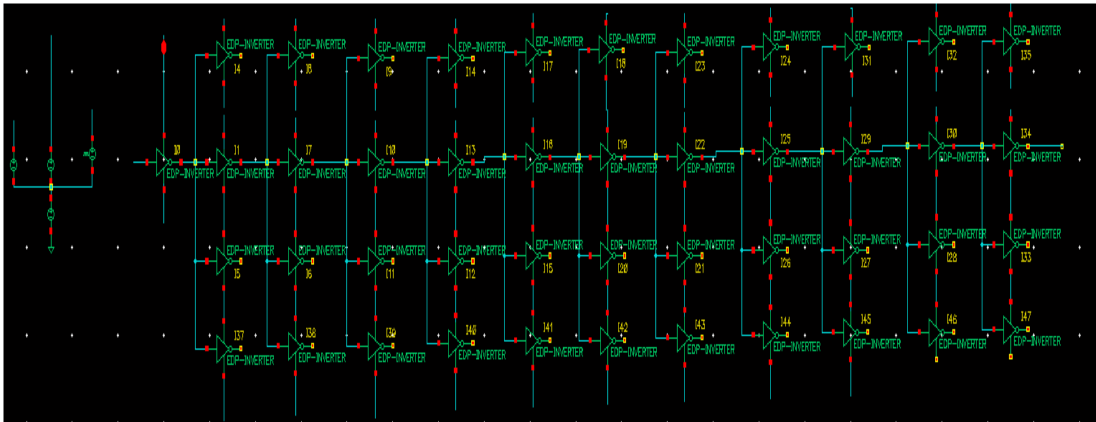

Figure 5.1: FO4 inverter chain as circuit under test

5.4 EXPERIMENT RESULTS AND OBSERVATION

The threshold voltage variation with increasing device finger Width and Length has been shown in Figure 4.2.

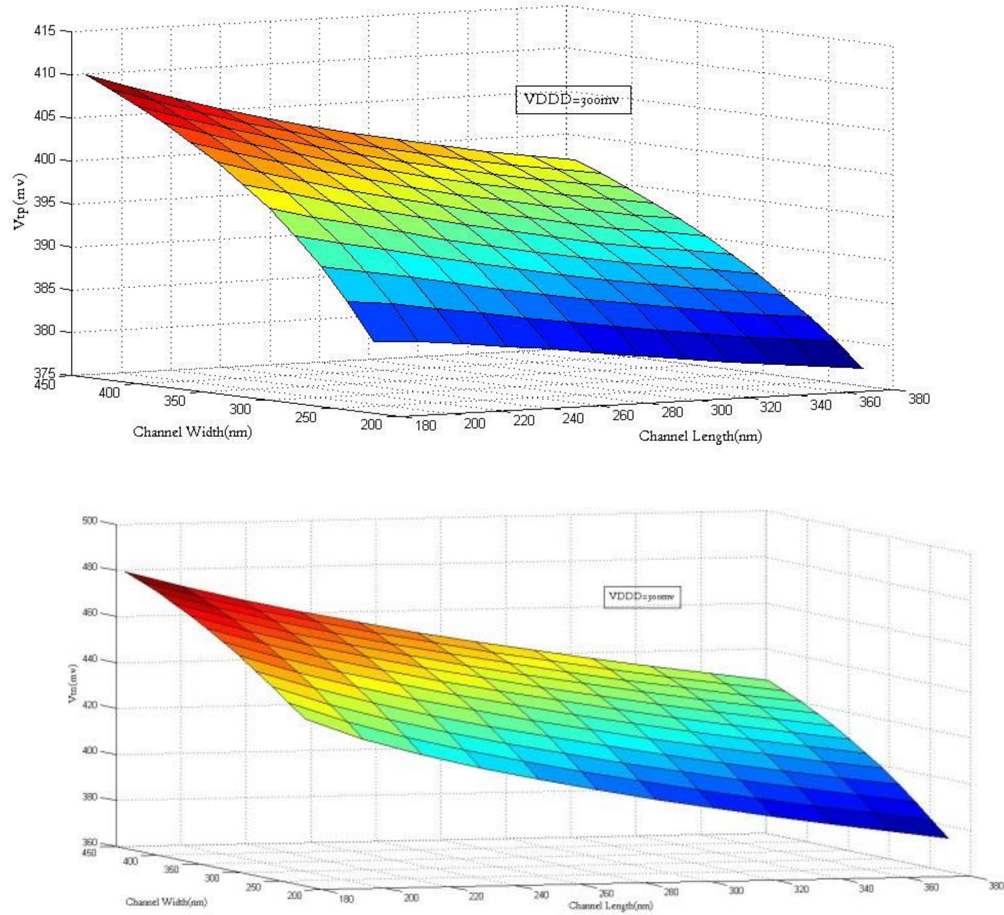

Figure 5.2: VTp(top) and VTn(bottom) variation with changing finger Width and Length.

From figure 4.2, at any particular finger Width, the threshold voltage falls monotonically with increasing channel length which is a direct contradiction to[17].Whereas the threshold voltages (VTn and VTp)increases with increasing finger width given a particular channel Length. This change in threshold voltage along with the changing device geometry is going to impact the current consumption i.e. Iintegrated. See Figure 5.3.

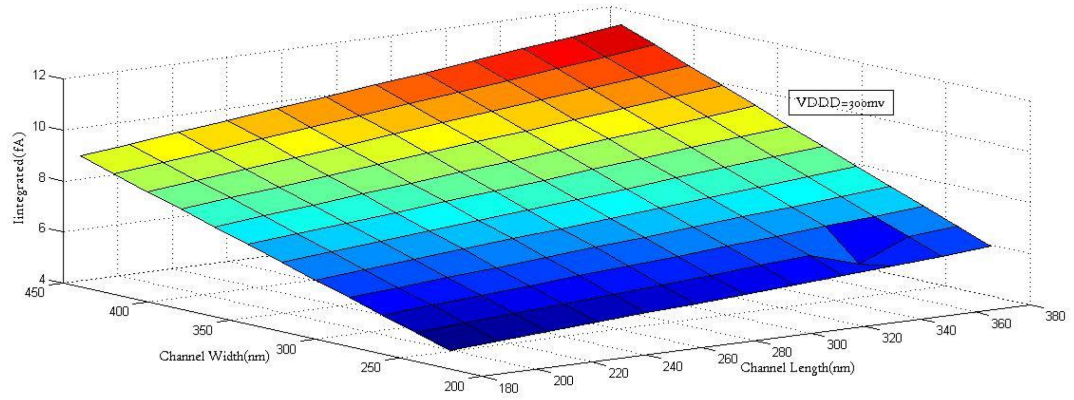

Figure 5.3: change in Integrated Current with changing device geometry.

As expected, the integrated current (Iintegrated) increases in magnitude when length is increased (given a fixed Width) as threshold voltage falls. The change in width has a higher impact as noticed from Figure 5.3. When we increase L, it lowers VT by ΔV_T. Figure 5.2 shows that the relationship is approximately linear with different slops for NMOS and PMOS respectively i.e.
$\frac{\partial VT}{\partial L} = -K_{n,p}$ where Kn,p is the slope

.Because of the fact that exp(ΔVT) have faster slope of rising than L^2 (See equation 5.3)the delay does not deteriorate to a great extent. But increasing L decreases variability by narrowing down the distribution of threshold voltage. If L changes to 2L, Sigma(σ) of VT distribution reduces by 1/SQRT(2) which also allows us to reduce out power supply down to $VDDD/\sqrt{2}$ which can compensate against the increased ELEAK due to increased delay and I_{leak} (I_{leak} increases if VT falls). If we are at the same power supply, with increased L (i.e. with reduced VT) we have higher B.W and drive strength as current is proportional to $\exp(\Delta V_T)$. However, static power dissipation is increased in this case due to threshold voltage reduction and dynamic power increases proportional to L(as Cgg =CoxWL).

Delay in sub-threshold could be expressed by the formula given in [4]

$$td = \frac{K.Cgg.VDDD}{I0.\frac{\exp(Vgs - VT)}{n.UT}}. \quad (5.1)$$

$$td = \frac{K.(Cox.W.L).VDDD}{\left(Cox.\left(\frac{W}{L}\right).(n-1).UT^2\right).\frac{\exp(Vgs-(VT-\Delta VT)}{n.UT}}. \quad (5.2)$$

$$td = \frac{K.(L^2).VDDD}{\left((n-1).UT^2\right).\frac{\exp(Vgs-VT)}{n.UT}.\exp\left(\frac{\Delta VT}{n.UT}\right)}. \quad (5.3)$$

Where I0 is given as below, Cox is the oxide capacitance, n is the sub-threshold slope, UT is volt equivalent temperature and approximately 25mV at 27^0C[2].

$$I0 = Cox.\left(\frac{W}{L}\right).(n-1).UT^2$$

The impact on delay for change in width(for any fixed Length) is in agreement with the experiment result demonstrated in [1] as it increases with increasing device width which causes VT to increase. From the delay equation Cg is proportional to Channel length and I_0 is inversely proportional to channel length, which makes delay proportional to the square of channel length. An increase in delay has been observed with increasing channel length for any fixed width as expected. This is shown in Figure 5.4 and Figure 5.5.

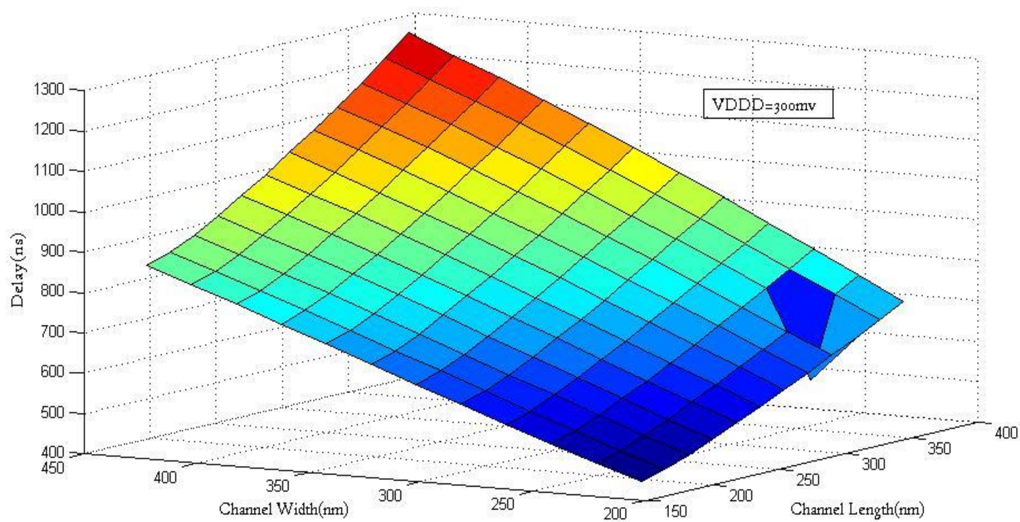

Figure 5.4: Surface Plot: Impact of device geometry change on delay

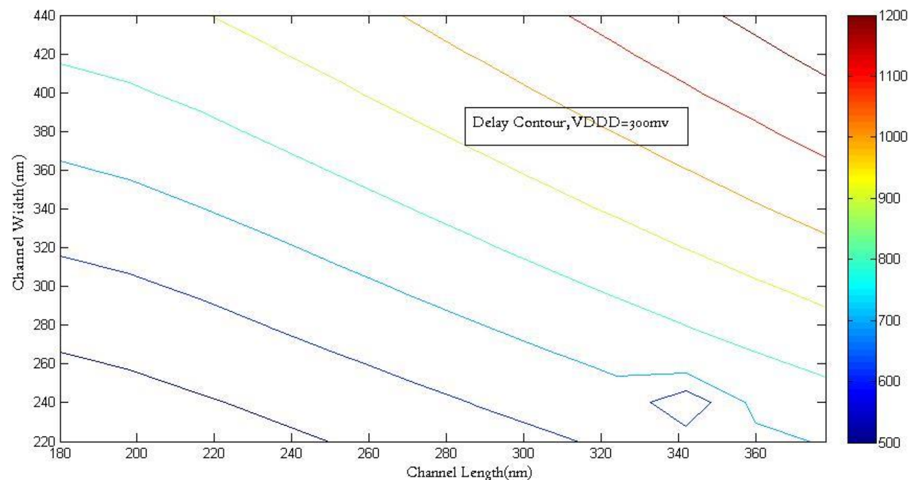

Figure 5.5: Contour Plot: Impact of device geometry change on delay

The delay has a greater derivative with increasing length than that of the current. As an expected result, we show a negative slope for the Iavg and Pavg with increasing length. This(Pavg plot) is presented in Figure 5.6 and Figure 5.7. If delay is of no concern, increasing channel length is a good option in order to reduce average power consumption as minimum Pavg point is achieved at higher channel length.

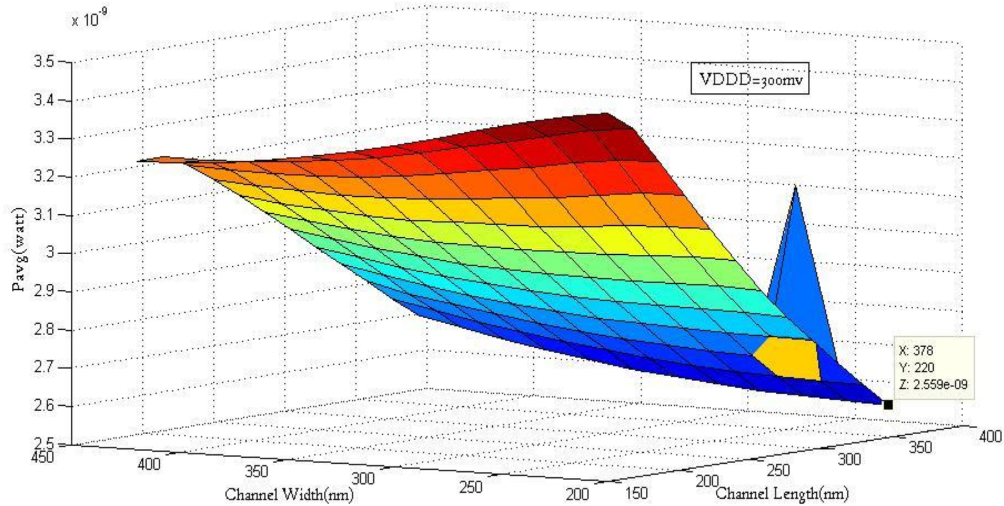

Figure 5.6: Surface plot: Pavg variation with changing device geometry

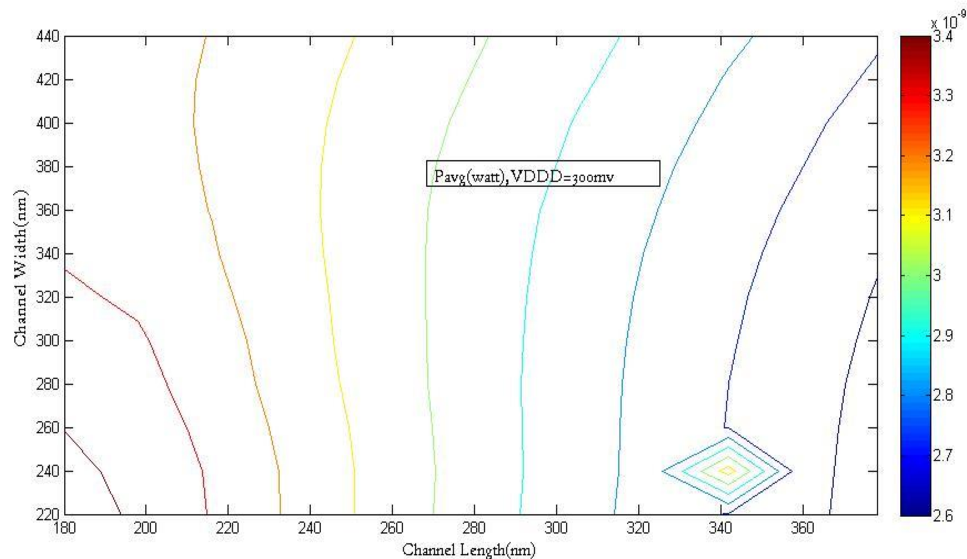

Figure 5.7: Contour plot: Pavg variation with changing device geometry

Finally we plot the PDP w.r.t. variable device sizes in order to find optimum point of solution. See Figure 5.8 and Figure 5.9. It shows that optimum point is achieved at minimum device finger width and minimum length. However, there is a small penalty for device length increase. *It*

should be noted that given an acceptable trip point variability as designed that VDD can now be dropped to VDD/√2 allowing a power savings approaching 2X.

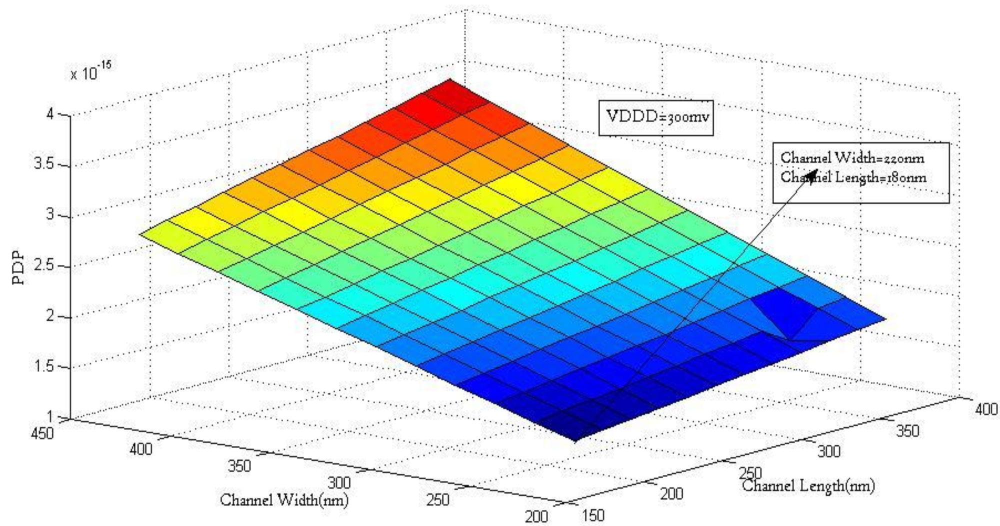

Figure 5.8: Surface plot: PDP variation with changing geometry.

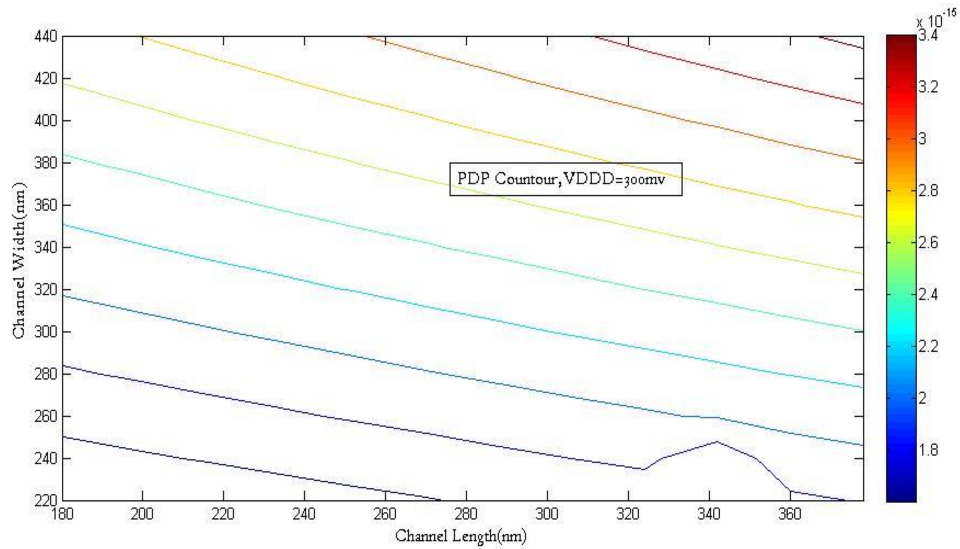

Figure 5.9: Surface plot: PDP variation with changing geometry

Hereby it can be concluded that minimum device finger width and Length with β ratio=1 gives the optimum PDP solution for all VDDD of choice in sub-threshold.

5.5 CHAPTER SUMMERY

Minimum finger size is the best choice is order to achieve minimum power delay product(PDP). Delay increases with increasing finger width and length. Average power (PAvg) reduces with increasing channel length. If delay is of no concern then increased channel length can be used to reduce average power consumption. Increased channel length reduces VT due to RSCE resulting in higher over drive and more drive current but load also increases proportionally causing in no net improvement in rise time in the particular process under consideration. However increased device length reduces variability. If device length is increases to twice of minimum length then threshold variability is reduced by 1/SQRT(2). Now VDDD can also be reduced by 1/SQRT(2) having an acceptable failure rate. Considering PDP as an important factor we use minimum geometry finger size for implementing the logic gates.

CHAPTER VI

LOAD BASED DEVICE SIZING

6.1 INTRODUCTION

Irrespective of the region of operation logic gates should be sized to drive specific load given a clock rate and operating VDDD. We define our INVX1 should be able to drive an FO4 Load as FO4 is technology independent. However, the wire parasitic plays an important role as it adds to the active load that any logic gate drives. So we define that a 1X load should typically drive a 5 to 6X active load at maximum including parasitic wire capacitance. A 2um long M3 metal wire is considered as our average routing distance (without buffering). Its parasitic capacitance is found to be 0.19fF by extraction in the process under consideration. Assuming that a 0.5-0.7fF approximates a 1X load (4 to 5 active loads plus the wire loads represents a 5 to 6X load). For a Beta matched inverter the total input capacitance becomes (2Cggp+Cggn) where Wn equals Cggn/LCox.

6.2 EXPERIMENT SETUP

The experiment setup is shown in Figure 6.1. The INVX1 is driving 4 INVX1 to imitate FO4 load and parasitic capacitance of 0.19fF representing the wire capacitance. The clock frequency is chosen as 200KHz as our frequency of operation and VDDD=300mV to start with, i.e. circuit is in sub-threshold.

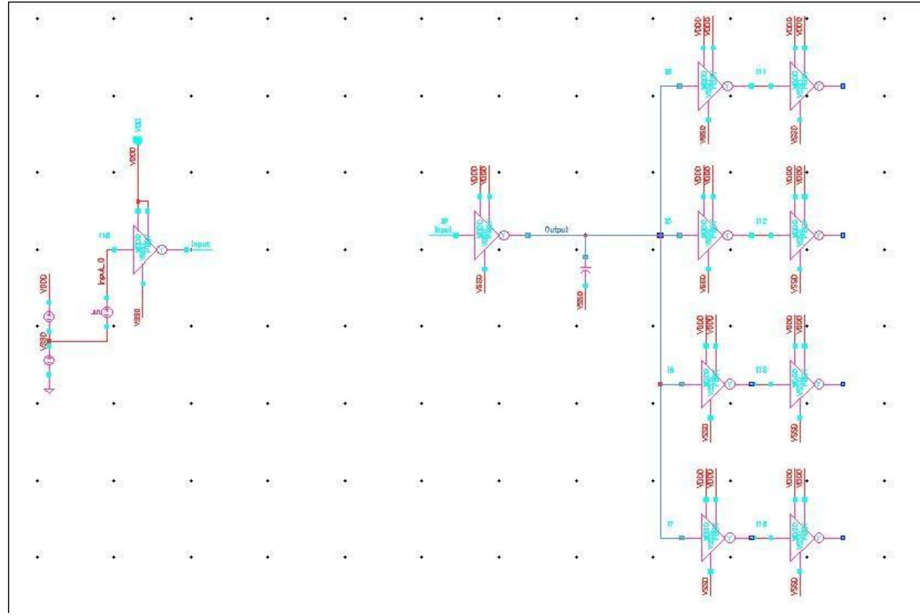

Figure 6.1: Experiment Setup for calculation of load based device sizing

6.3 SIMULATION RESULTS AND OBSERVATION

We start with the minimum geometry i.e. L=180nm and W=220n for figure size of each device and we measure the Electrical Effort (i.e. Load/input-capacitance) for the INVX1, which ideally we want to be close to 4. The Electrical Effort has been plotted against increasing channel width and has been shown in Figure 6.2. The Electrical Effort at minimum geometry has been captured to be 7.035 and the rise time at VDDD=300mv, minimum geometry, tt corner and Room temperature is captured as 31.92ns as shown in Table 6.1. Figure 6.2 also reveals the fact that to maintain a FO4 loading (i.e. electrical effort=4)the width of the transistor has to be increased beyond 1um, which is unrealistic in terms of average power consumption, area, slew rate and propagation delay. Detailed explanation is given in previous chapter. Figure 6.3 shows Temperature vs Rise time plot and Figure 6.4 shows Temperature vs Propagation delay plot at VDDD=300mv and at minimum geometry. It reveals the fact that in sub-threshold low temperature is a worse case corner. We hereby investigate the applicability of minimum sized beta matched inverter at the worst case PVT corner i.e. 10% reduced power supply voltage(VDDD) and at -55^{0}C. If we constrain out rise time to be maximum 10% of pulse width, then by the following equation we find,

Tmin/2 x 10% =31.92ns

Or, Tmin= 638.4 ns or Fmax= 1.6MHz for minimum sized devices, in optimum PVT corner with VDDD=300mV. Since our frequency of operation is 200KHz we can tolerate up to 250ns of rise time for efficient operation with the current size. However, in this analysis the worse PVT corner as defined earlier is considered for successful operation under worse case.

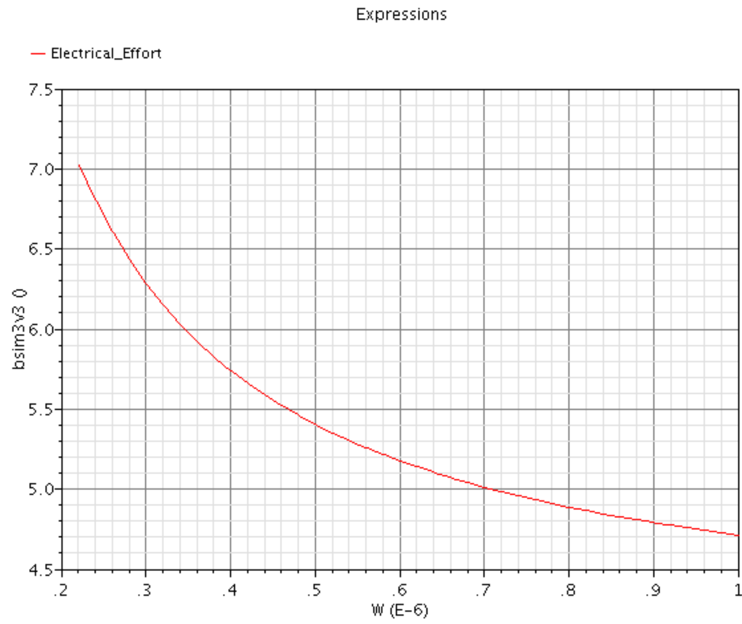

Figure 6.2: Electrical Effort of INVX1 vs Channel Width

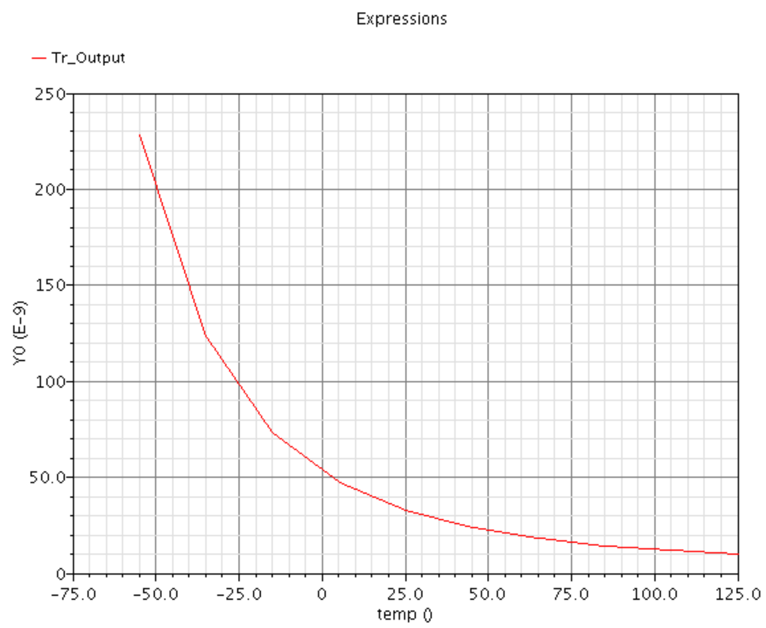

Figure 6.3: Rise Time vs Temperature (in degree centigrade)

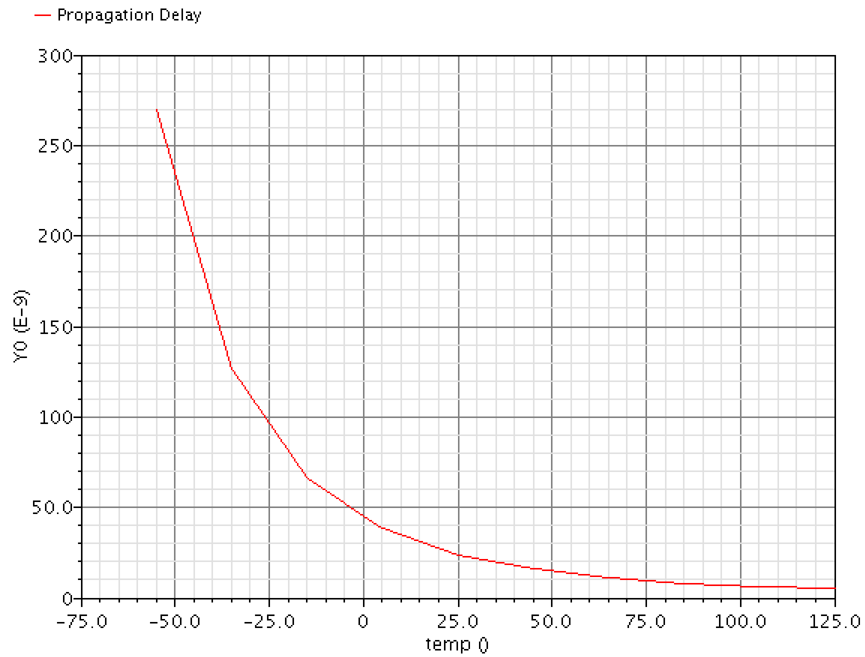

Figure 6.4: Propagation delay vs Temperature(in degree centigrade)

Table 6.1 Rise time and Electrical effort

Rise Time	31.92ns
Electrical Effort	7.035

However, we verify the rise time under T=-55°C, VDDD=270mv, and ss process corner. Figure 6.5 shows Rise time vs Width plot under worse case situation i.e. VDDD=270mv and ss process corner and T=-55^{0}C. The plot clearly shows the circuit fails to operate at 200 KHz frequency with a rise time of 2.07us rise time under worse case situation and increasing width does not help at all, rather worsen the situation even though it reduces the Electrical Effort to some extent. So our conclusion is VDDD=300mV is not at all suitable for reliable operation to operate in 200KHZ. We also verify the rise time vs width for different VDDDs(300mV and 330mV) at the defined worse case corner. The simulation result for VDDD=330mV is shown in Figure 6.6.. The simulation result shows that at degraded VDDDof at least 330mV($VDDD_{Actual}$ x 90%=330mV) is required i.e the actual minimum VDDD will be 366mV for reliable operation under worse PVT corner(considering 10% degradation in supply voltage). The simulation also explores the fact that optimum rise time is obtained at minimum width i.e. 220nm for this process at any VDDD of operation as it neither improves rise time neither improves propagation Delay {Figure 6.7}.

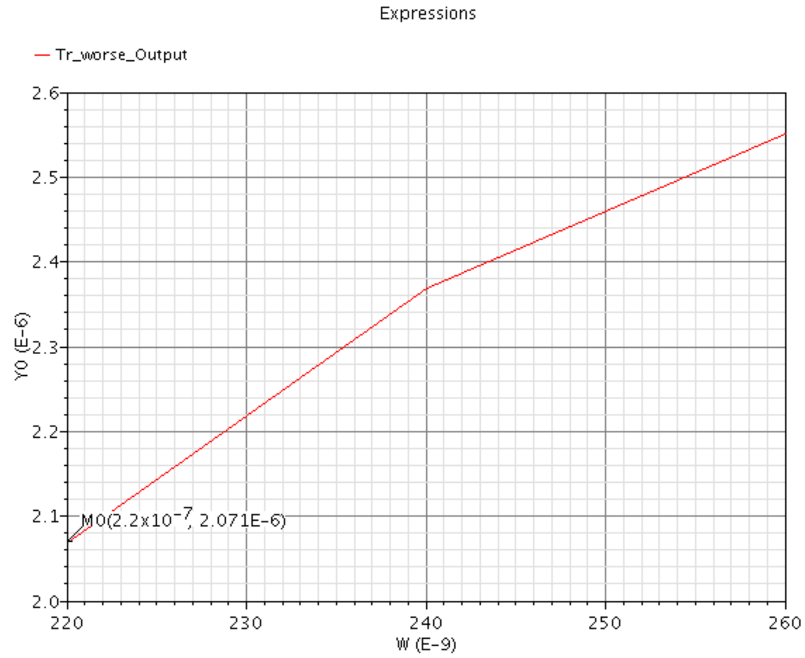

Figure 6.5: Rise Time vs Channel width, VDDD=270mv, ss corner, T=-55^{0}C

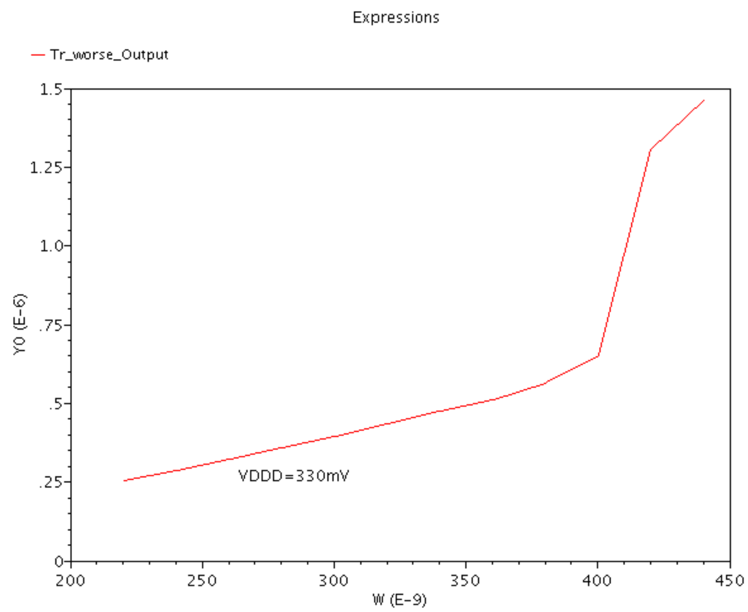

Figure 6.6 Rise Time vs Channel width for different VDDD=330mV, ss corner, T=-55^{0}C

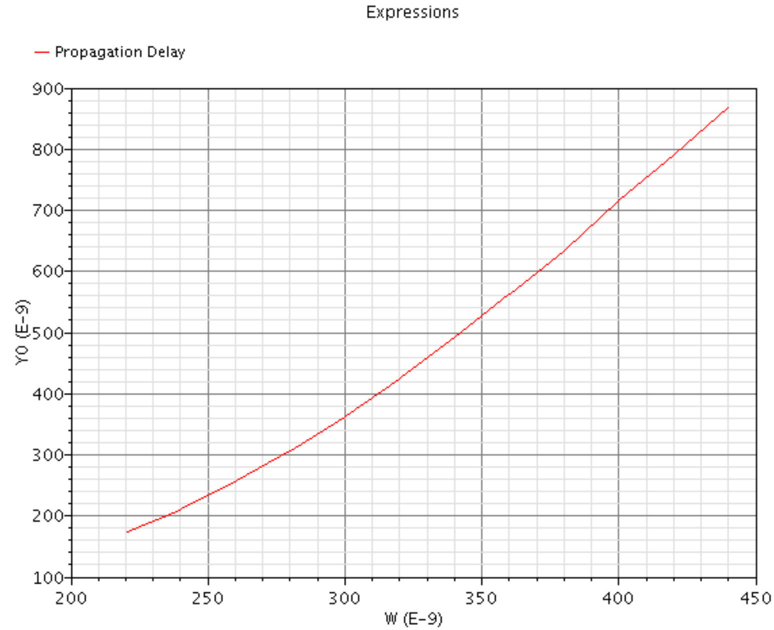

Figure 6.7: Propagation delay vs Channel width at VDDD=330mv.worst case PVT corner.

Minimum geometry fingers are the optimum solution for sub-threshold in terms of load based device sizing. Increasing finger Width to compensate the current is not suggested because load increases proportionally to width. Previously in Chapter III we have seen that increasing number of device fingers causes higher PDP. So, VDDD is to be increased till we find minimum power supply sufficient for reliable operation under worst case PVT corner given a particular frequency of operation. In this particular case device finger size of Wn=Wp=220nm and Ln=Lp=180nm will be chosen for further operation considering VDDD of 400mV and operating frequency of 200KHz.

6.4 CHAPTER SUMMERY

Given a particular clock rate a 1X logic gate should be able to drive FO4 load along with some nominal wire parasitic even under worst case PVT corner consideration. Drain current in sub-threshold has an exponential dependency on over drive and linear dependency on carrier mobility. With reduction in temperature threshold increases and mobility also increases but threshold being the dominant factor in sub-threshold causes higher output rise time for the logic gates. Hence low temperature, reduced VDDD and SS process corner is the worst case PVT corner for sub-threshold operation. The nominal wire parasitic is considered to be 0.19ff in this case. It is observed that a minimum VDDD of approximately 370mv is required in order to sustain the required clock rate (200kHz in this case) ensuring sufficient drive current to drive FO4 load with nominal wire parasitic under worst PVT corner consideration. Presence of stack device logic gate in the library would require higher VDDD for reliable operation.

CHAPTER VII

CONTROLLER FOR MICRO NEURAL INTERFACE

7.1 ARCHITECTURE DESCRIPTION

The architecture of the MNI controller can be subdivided into two major modules as shown in Figure 7.1. The central controller has the responsibility to serially transmit data (neural spikes detected by an amplifier-thresholder combination) every 1ms interval at a data rate of 200kbps and the thresholder controller is responsible for controlling the dynamic behavior of the thresholder based on number of neural spikes detected per unit time interval and set an appropriate voltage reference level to maximize the possibility of capturing actual neural data.

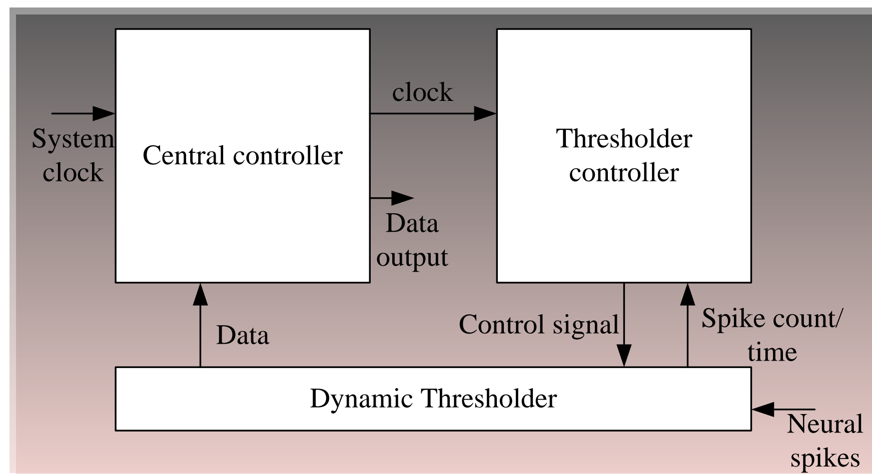

Figure 7.1: Block diagram of MNI Controller

Central controller: The central controller has been shown in Figure 8.2 in form of block diagram and is a designed for 8 channel MNI interface. The operating frequency for the system is 200 KHz. The controlled clock pulse generator generates 10 clock pulses every 1ms interval time as well as generates a “Registerfile_control” signal every 1ms interval time. A 8 bit parallel input and serial out register file has been utilized to capture 8 bit data from the thresholder and then serially transmit 10 bit data packet with one parity bit and start-bit (always set to logic one) padded in the front. The “Registerfile_control” signal makes the necessary selection between data

loading and serial transmission mode every 1ms interval as shown in the state diagram in Figure 7.3.

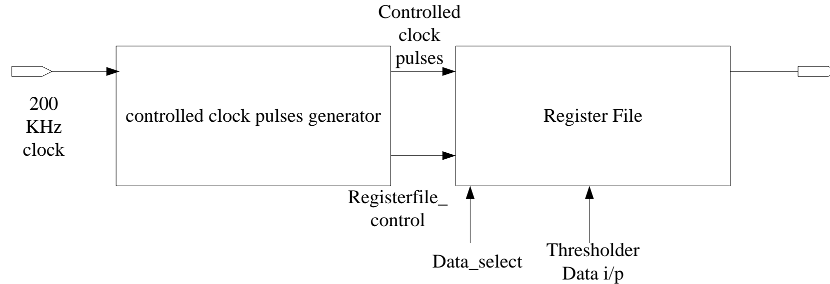

Figure 7.2 Central controller block diagram

The controlled clock pulse generator circuit is shown in Figure 8.4. An additional “Data_select” signal is provided in order to make selection between thresholder data and any hard coded specific test pattern with fixed parity bit.

Thresholder controller: The architecture diagram of the thresholder controller has been shown in Figure 7.5. The thresholder controller has the following responsibilities:

1. Given a set, select voltage reference such that no two spike occurs within 1ms time interval.
2. If more than two spikes occurs within 1ms time interval, increment the thresholder voltage reference level by one.
3. If no spike occurs within 20ms time interval, decrement the thresholder voltage reference by one.
4. If counter has been incremented or decremented once, wait for another time interval of 20ms before any further change in the voltage reference level.

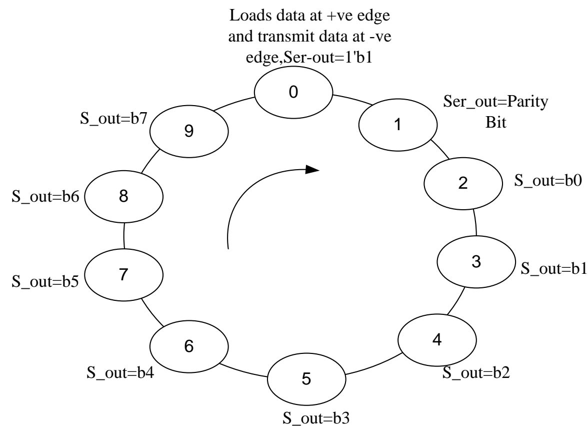

Figure 7.3: State diagram for central controller

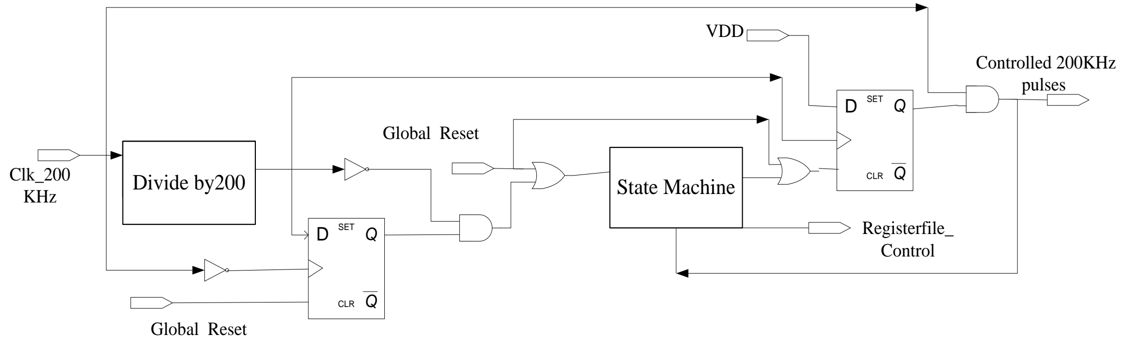

Figure 7.4: Controlled pulse generator circuit

The thresholder controller block diagram describes the overall operation of the circuit. The "Fast spike count" circuit counts number of spikes detected every one millisecond interval. The detailed circuit and its state diagram are shown in Figure 7.6 and Figure 7.7 respectively.

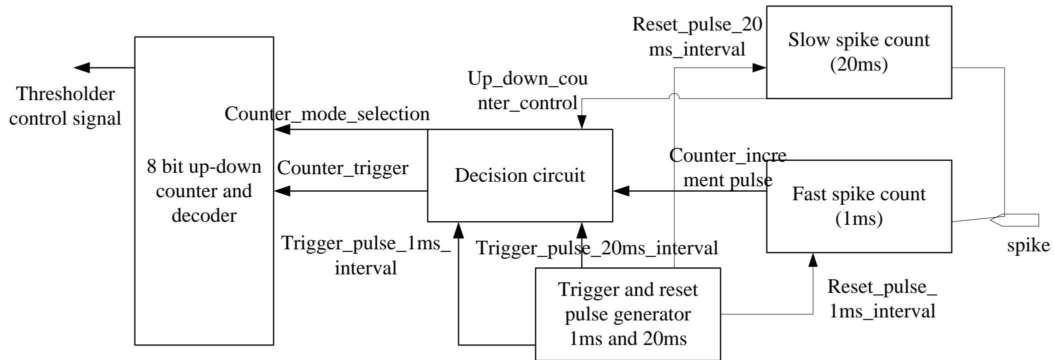

Figure 7.5: Thresholder controller block diagram

The fast spike detection circuit has four states as shown in the state diagram. Initially all the sequential elements are reset. Hence the circuit starts from "00" state. Whenever it detects s pike, the counter is incremented to its next state. After reaching state "11" the state machine remains in that state until "Reset_pulse_1ms_interval" reinitializes to state "00". The "Reset_pulse_1ms_interval" generator circuit is shown in Figure 7.8

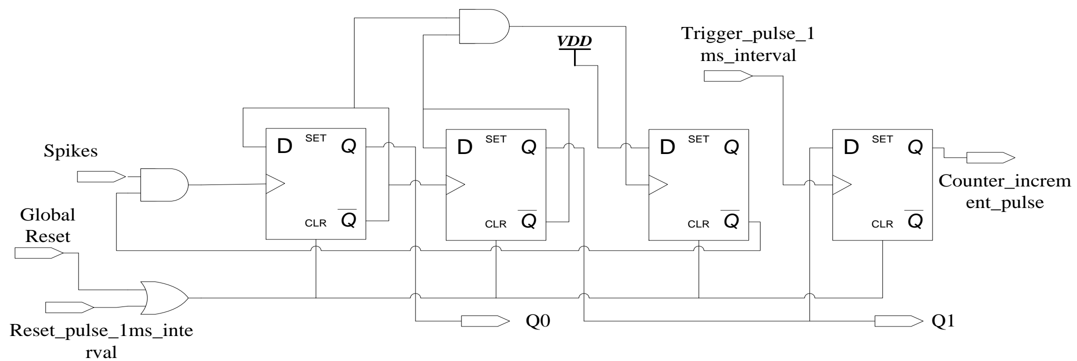

Figure 7.6: Fast spike detection module

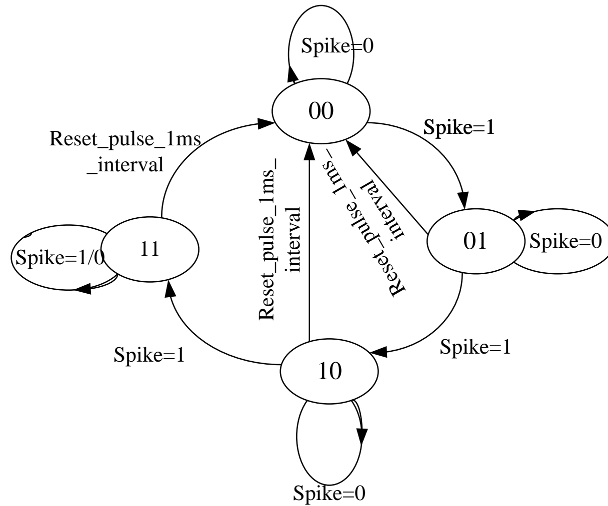

Figure 7.7: State diagram for fast spike detection module

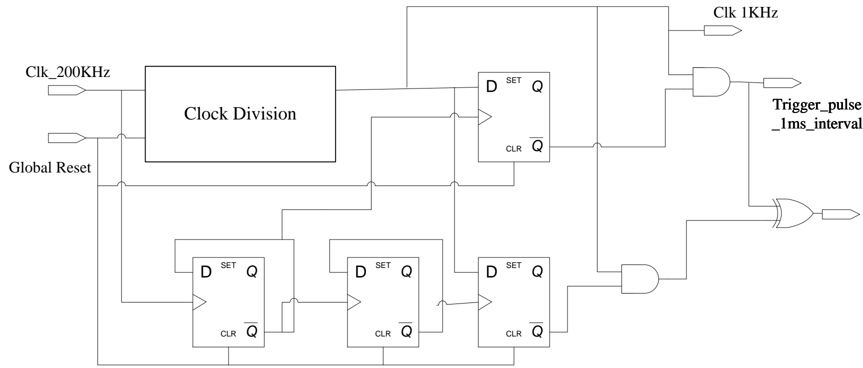

Figure 7.8: 1ms interval Reset and Trigger pulse generator.

. If the state is above “01”, “Counter_increment_pulse” is generated every 1ms interval. In the similar fashion “Trigger_pulse_20ms_interval” and “Reset_pulse_1ms_interval” is generated. The inputs and outputs of the “Decision circuit” are shown in Figure 5.The “Decision circuit” takes the decision whether to increment or decrement or make no change to the output up-down counter-decoder stage. The outputs of this block are the “Counter_Trigger” and “Counter_mode_selection” which is applied to counter-decoder stage. Since there are 8 numbers of thresholder, 8 separate sets of “Fast_spike_count”, “slow_spike_count” and “up-down counter-decoder” stages are implemented. An RTL code simulation for the above described system is shown in Figure 7.9. From Figure 7.9 we can verify that the signal “Cntl” is going high every 1ms time interval controlling the register file to load and start neural data transmission. “THdata” represents the input neural data(provided by the test bench) and “Ser_Out” is the serial data transmission by the controller which is “THdata” captured at the time instance when “Cntl” goes high.

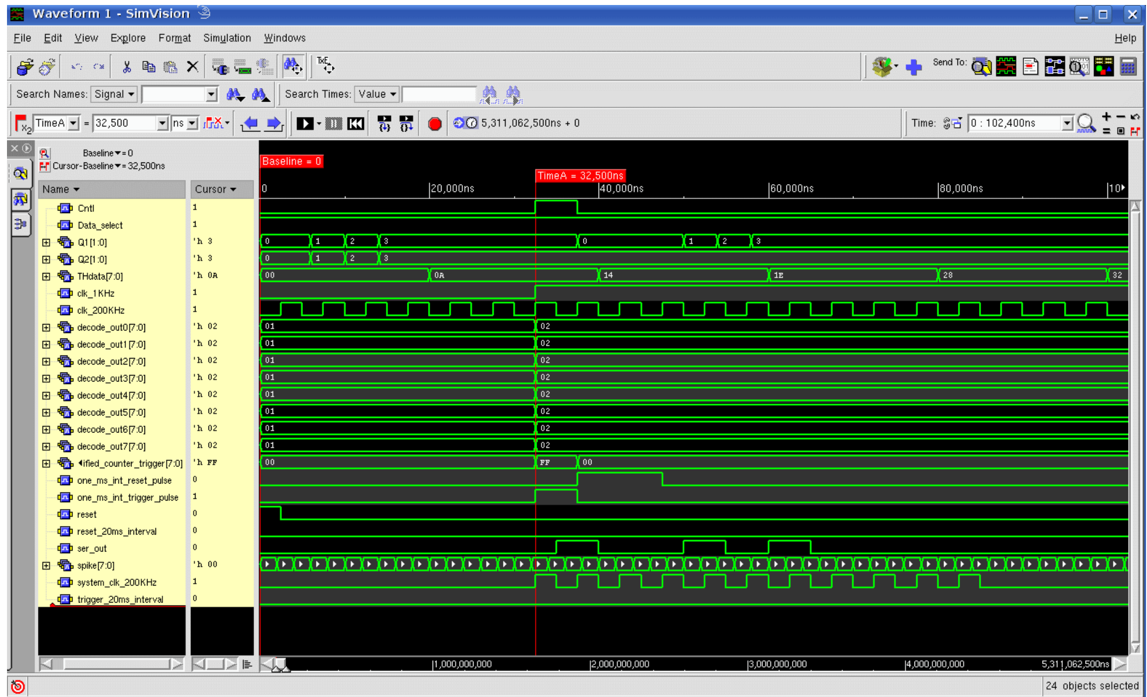

Figure 7.9: RTL simulation for MNI controller.

CHAPTER VIII

REDUCED ASIC CELL LIBRARY DESIGN

8.1 INTRODUCTION

The target architecture having been described in the last chapter and we focus on deriving an appropriate digital cell library for front end and back end processing. Noullet et al [30] shows the process of deriving a reduced ASIC cell library starting from a parent cell library containing 216 cells. The implementation stated above involves a series of optimization phases resulting in reduced implementation time, effort and manpower. The optimization is based on standard cell count reduction from the parent library based on valid assumptions and logical reasons. It has been shown that a cell library containing 18 cells is sufficient to give an equivalent performance in the process of synthesis in terms of slack time and area[30] relative to large or full libraries. Following the same methodology we derive our reduced ASIC cell library for our target system with an extension to sub-threshold/moderate inversion. Moreover, we verify our observations by using two additional standard designs to generalize our final reduced ASIC cell library.

8.2 LIBRARY IMPLEMENTATION METHOD

Starting with a parent digital cell library (referred to Golbal_Library) we apply techniques of cell reduction as shown in Figure 8.1. The parent 180nm CMOS low power cell library contains 58 cells. The cell list is the libraries are shown in Table 8.1. The reduction steps are mentioned below.

Designs Under Test (DUT): MNI controller (Target design), 8 bit Carry save array multiplier, 28 bit Carry look ahead adder.

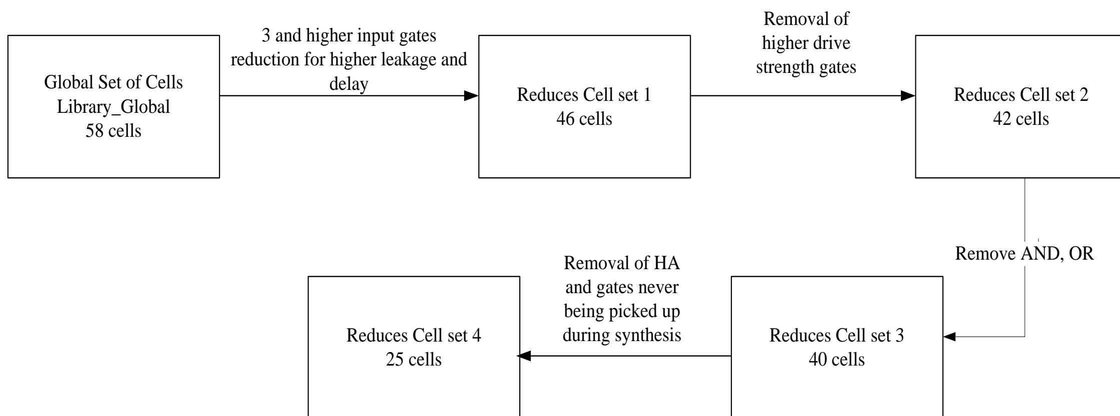

Figure 8.1: Library reduction flow

Step 1: Three and higher input gates are removed from the library to avoid high leakage (poor I_{ON}/I_{OFF} ratios) and delay. The Designs under test are synthesized with Reduced cell set 1. The slack time and area have been recorded for comparison.

Step 2: As we have diverse range of inverters and buffers to provide different drive strength and we anticipate a low area design, we remove all gates having X2 and X3 drive strength from the library to derive reduced cell set 2. The DUTs are synthesized and timing and area recorded for comparison with previous results.

Step3. Further the AND, OR are removed as it could easily be synthesized by using NAND and NOR with a range of buffers. We leave it on synthesize and reduced cell set 3 is derived.

Step 4: Finally the gates which have never been selected during synthesis are removed from the cell library and reduced cell set 4 emerges as our target library.

Table 8.1: Library cell lists

Global_Library	Reduced Set 1	Reduced set 2	Reduced Set 3	Reduced Set 4
AND2X1	AND2X1	AND2X1	BUFX1	BUFX1
AND2X2	AND2X2	BUFX1	BUFX2	BUFX2
AND2X3	AND2X3	BUFX2	BUFX3	BUFX3
AND3X1	BUFX1	BUFX3	BUFX4	BUFX4
AND3X2	BUFX2	BUFX4	BUFX5	BUFX5
AND3X3	BUFX3	BUFX5	BUFX6	BUFX6
AOI21X1	BUFX4	BUFX6	BUFX7	BUFX7
AOI22X1	BUFX5	BUFX7	BUFX8	BUFX8
BUFX1	BUFX6	BUFX8	BUFX9	BUFX9
BUFX2	BUFX7	BUFX9	DFFNEGNRX1	DFFNEGNRX1
BUFX3	BUFX8	DFFNEGNRX1	DFFPOSNRX1	DFFPOSNRX1
BUFX4	BUFX9	DFFPOSNRX1	INVX1	INVX1

BUFX5	DFFNEGNRX1	INVX1	INVX1_5	INVX1_5
BUFX6	DFFPOSNRX1	INVX1_5	INVX2	INVX2
BUFX7	INVX1	INVX2	INVX2_5	INVX2_5
BUFX8	INVX1_5	INVX2_5	INVX3	INVX3
BUFX9	INVX2	INVX3	INVX3_5	INVX3_5
DFFNEGNRX1	INVX2_5	INVX3_5	INVX4	INVX4
DFFPOSNRX1	INVX3	INVX4	INVX4_5	INVX4_5
INVX1	INVX3_5	INVX4_5	INVX5	INVX5
INVX1_5	INVX4	INVX5	INVX5_5	MUX21X1
INVX2	INVX4_5	INVX5_5	INVX6	NAND2X1
INVX2_5	INVX5	INVX6	INVX6_5	NOR2X1
INVX3	INVX5_5	INVX6_5	INVX7	XNOR2X1
INVX3_5	INVX6	INVX7	INVX7_5	XOR2X1
INVX4	INVX6_5	INVX7_5	INVX8	XOR2X1
INVX4_5	INVX7	INVX8	INVX8_5	
INVX5	INVX7_5	INVX8_5	INVX9	
INVX5_5	INVX8	INVX9	INVX9_5	
INVX6	INVX8_5	INVX9_5	INVX10	
INVX6_5	INVX9	INVX10	INVX18	
INVX7	INVX9_5	INVX18	INVX27	
INVX7_5	INVX10	INVX27	MUX21X1	
INVX8	INVX18	MUX21X1	NAND2X1	
INVX8_5	INVX27	NAND2X1	NOR2X1	
INVX9	MUX21X1	NOR2X1	XNOR2X1	
INVX9_5	NAND2X1	OR2X1	XOR2X1	
INVX10	NOR2X1	XNOR2X1	LATCHNEGX1	
INVX18	OR2X1	XOR2X1	LATCHPOSX1	
INVX27	OR2X2	HAX1	HAX1	
LATCHNEGX1	OR2X3	LATCHNEGX1		
LATCHPOSX1	XNOR2X1	LATCHPOSX1		
MUX21X1	XOR2X1			
NAND2X1	HAX1			
NAND3X1	LATCHNEGX1			
NOR2X1	LATCHPOSX1			
NOR3X1				
OAI21X1				
OAI22X1				
OR2X1				
OR2X2				
OR2X3				
OR3X1				

OR3X2
OR3X3
XNOR2X1
XOR2X1
HAX1

All the designs are synthesized at VDDD=400mV at a target frequency of 200 KHz. The slack time and area estimation obtained by synthesis for different cell library sets are shown in Table 8.2 (In absence of HA in reduced Set 3) and Table 8.3 (in presence of HA in Reduced set 3).

In absence of HA				
System under synthesis	Cell Library	No of gates in the Library	Time Slack from Synthesis(ps)	Area Estimation from Synthesis(sq um)
Controller for MNI interface with thesholder control	Global	58	2293367	84845
	Reduced Set 1	46	2287927	86148
	Reduced Set 2	42	2293367	86227
	Reduced Set 3	39	2292546	90508
8 bit Carry Save array Multiplier	Global	58	3776531	35510
	Reduced Set 1	46	3776531	35510
	Reduced Set 2	42	3766808	38700
	Reduced Set 3	39	3875569	55940
28 bit CLA	Global	58	4434279	38599
	Reduced Set 1	46	4408969	38599
	Reduced Set 2	42	4371576	40378
	Reduced Set 3	39	4437016	38974

Table 8.2: Synthesis result for different cell libraries (without HA in reduced set 3)

In presence of HA				
System under synthesis	Cell Library	No of gates in the Library	Time Slack from Synthesis(ps)	Area Estimation from Synthesis(sq um)
Controller for MNI interface with thesholder control	Global	58	2293367	84845
	Reduced Set 1	46	2287927	86148
	Reduced Set 2	42	2293367	86227
	Reduced Set 3	40	2290888	89910
8 bit Carry Save array Multiplier	Global	58	3776531	35510
	Reduced Set 1	46	3776531	35510
	Reduced Set 2	42	3766808	38700
	Reduced Set 3	40	3945738	68587
28 bit CLA	Global	58	4434279	38599
	Reduced Set 1	46	4408969	38599
	Reduced Set 2	42	4371576	40378
	Reduced Set 3	40	4418862	42649

Table 8.3: Synthesis result for different cell libraries (without HA in reduced set 3)

It can be noticed that there are insignificant changes in timing slack for different libraries for a particular design. In case of 8 bit CSAM and 28 bit CLA the reduced set 3 results in better slack time. The penalty in some cases is little more area. As area not a great concern, we select reduced cell set 3 for our target design. Also, INVX5 and the higher order inverters and the latches are never selected during synthesis. By comparing Table 8.2 and Table 8.3 we see that in case of

MNI and CLA we get slightly degraded performance in slack time in presence of Half Adder (HAX1). So we discard the inverters not being selected and HAX1 to derive our reduced cell Set 4, 25 cells as shown in Table 8.1. Hence forward we proceed with the cell Set 4library for all further experiments.

8.3 CHAPTER SUMMERY

A reduced ASIC cell library with minimum cell count is implemented with extension to sub-threshold with reduced implementation time and effort. It is observed that as minimum as 25 cells in the library are sufficient to mitigate the synthesis requirements under consideration. Negligible change in slack time is observed when reduction techniques are applied on an existing low power, CMOS parent library. However, insignificant area penalty is noticed in synthesis when synthesized the same design with different sub sets of the library.

CHAPTER IX

T-GATE SIZING METHODOLOGY

9.1 INTRODUCTION

It has already been shown in previous chapter that minimum geometry device finger is beneficial in terms of achieving minimum power delay product. *In this section we focus on T-gate sizing for designing T-Gate based reduced cell set 4(See Chapter VIII) by using Logical Effort Analysis(LEA), a powerful tool for log gate sizing*. A detailed discussion on logical effort alone with device sizing for T-gate, skewed gate and standard CMOS gate can be found in [20]. The analysis below is based on this reference.

9.2 GATE SIZING METHODOLOGY

Harris et al [20] show that the method of logical effort does not apply to arbitrary Transistor network but only to logic gates and the logic gates under analysis are subjected to the following restrictions:

1. “The gate of each transistor is connected to an input, a power supply or the output.
2. Inputs are connected only to transistor gates.”

Satisfying restriction 2, it is important to consider the driving gate while analyzing T-gate device sizing. Chapter 4 of [20] also introduces 3 different ways of representing efforts, useful for Logical effort analysis. Below is the description for these efforts.

i. Logical effort per input: Logical effort of individual signal input.
ii. Logical Effort of a bundle: Logical Effort of bundle of complementary pairs of signals e.g. the true and complementary select signals in multiplexer.
iii. Total Logical Effort: Logical Effort of all the inputs taken together.

Here it is considered that the input of the transmission gate driven by an INV1X resulting in a worst case logical effort and all the gates (excluding the higher drive strength inverters and buffers) in the discussed library are having an INVX1 at the output stage.

9.3 DEVICE SIZING

NAND2X1

The T-gate NAND2X1 circuit is shown in Figure 9.1. We consider that

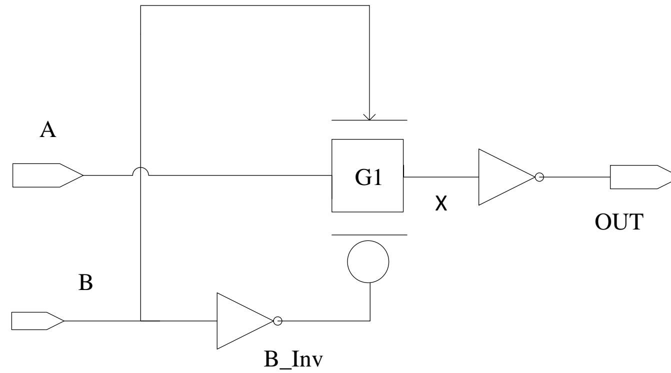

Figure 9.1 T-Gate NAND2X1

Port A is being driven by an INVX1 with β = (PMOS width)/(NMOS width) equal 2 (beta matched in the process under investigation) The circuit is shown in Figure 9.2. The T-Gate is made of β matched devices as well to equalize rise and fall times. S and Sb are the true and complementary selections of the T-Gate.

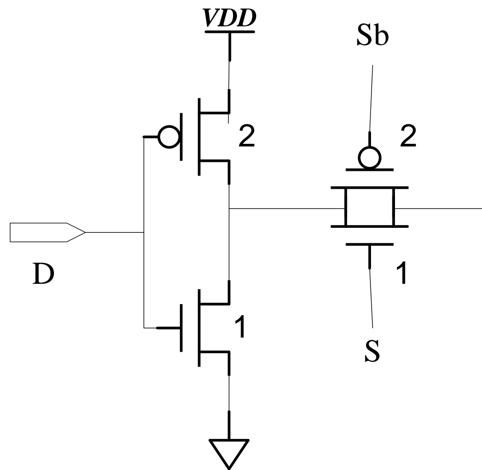

Figure 9.2: INVX1 driving T-Gate

The circuits in Figure 9.1 and Figure 9.2 are combined and redrawn in Figure 9.3. Following the

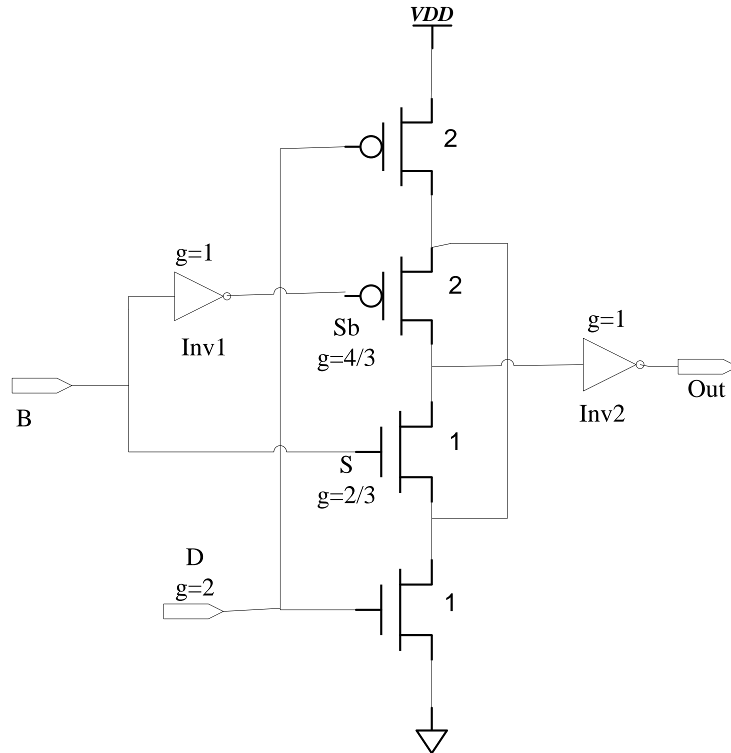

Figure 9.3: NAND2 driven by INVX1

methods for Logical Effort Calculation from [20], the Logical effort of input D turns out to be g=2, of the inverters g=1 and the Logical Effort of the bundle s*= (Logical Effort of S and Logical Effort of Sb)= (4/3 + 2/3)= 2. If we scale up our INVX1 as well as the T-Gate as shown in Figure 9.4, the logical Effort still remains independent of geometry (i.e. propagation delay does not change) but consumes proportionally more power for increased device fingers.

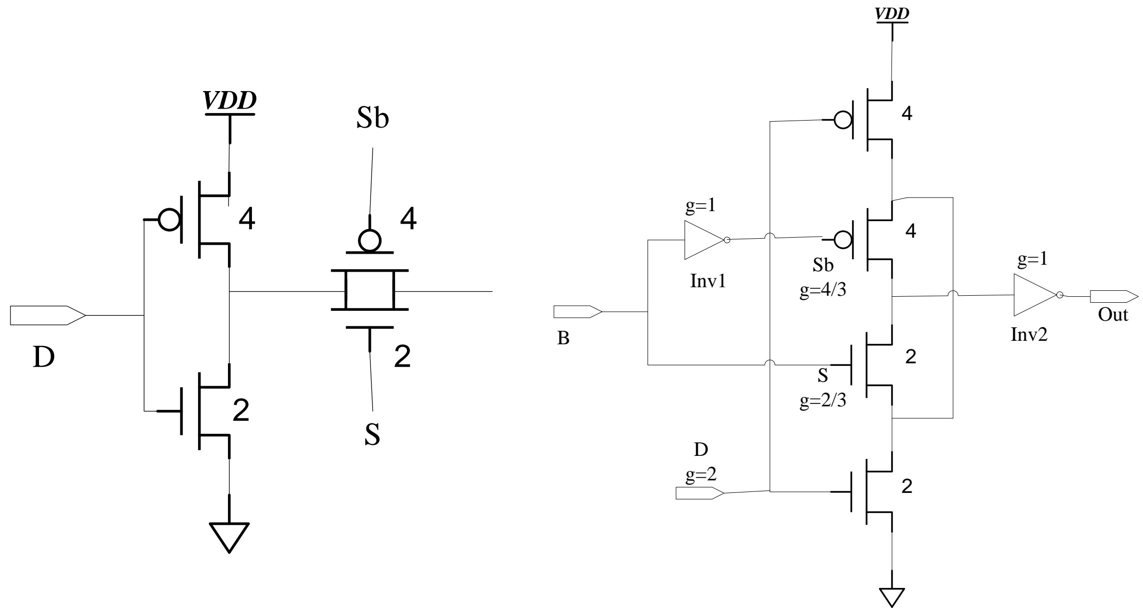

Figure 9.4 upsized devices and Corresponding Logical Effort

As the 1X device geometry is scaled up the Electrical Effort i.e. Cout/Cin remains nearly constant) from input "B" to "Out" is unchanged as does the propagation delay. Other possible combinations where the driving inverter is as shown in Figure 9.4 and the T-Gate is sized as shown in Figure 9.2, would cause asymmetric rise and fall transition time at the output of the transmission gate as discussed in Chapter 9 of [20] and hereby, excluded from consideration. Hence we choose the T-Gate sizing topology shown in Figure 9.3. The balance of the gates in the library will be sized with identical T-Gate sizing. Sizing of the T-gate based logic gates and their Standard CMOS equivalent is shown below. Port A of these gates always presents a logical effort of 2 when driven by INVX1 as shown above.

NAND2X1:

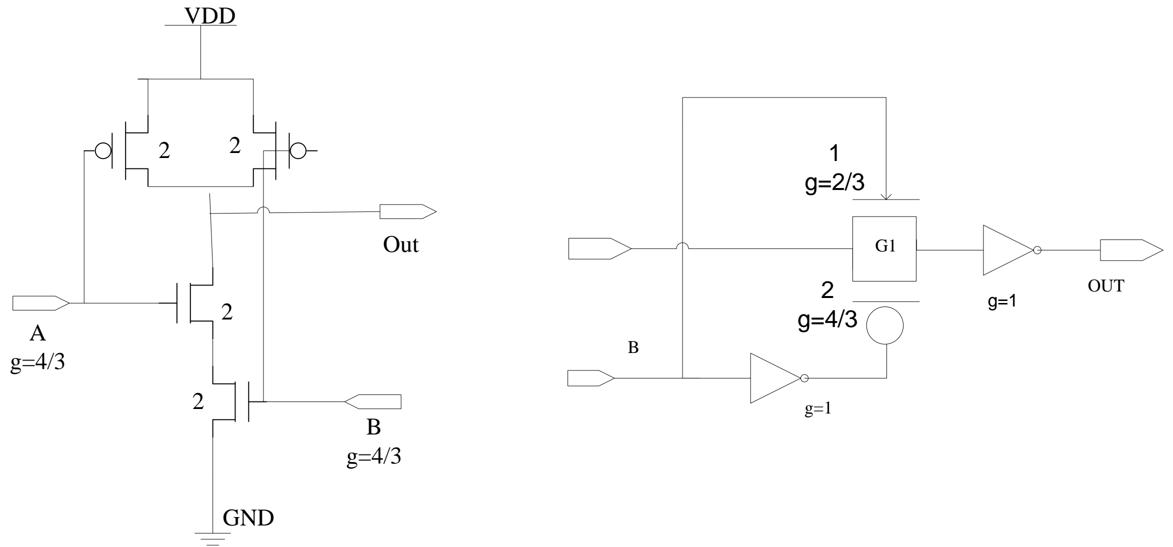

Figure 9.5 Gate sizing for standard CMOS NAND2X1 (left) and T-Gate NAND2X1 (right)

NOR2X1:

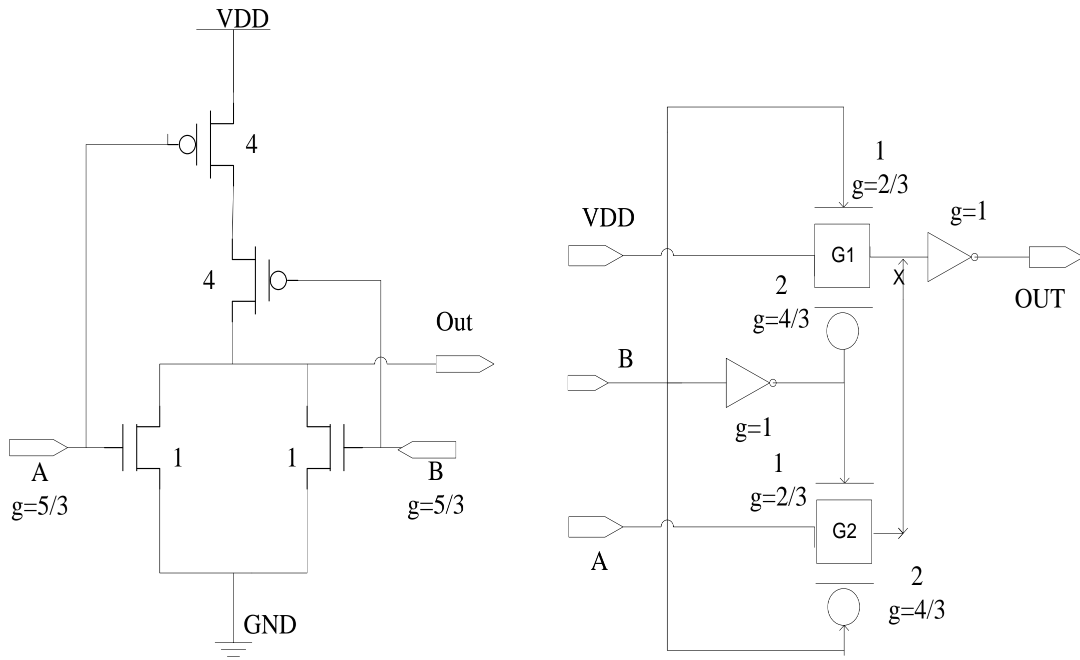

Figure 9.6: Gate sizing for standard CMOS NOR2X1 (left) and T-Gate NOR2X1 (right)

XOR2X1:

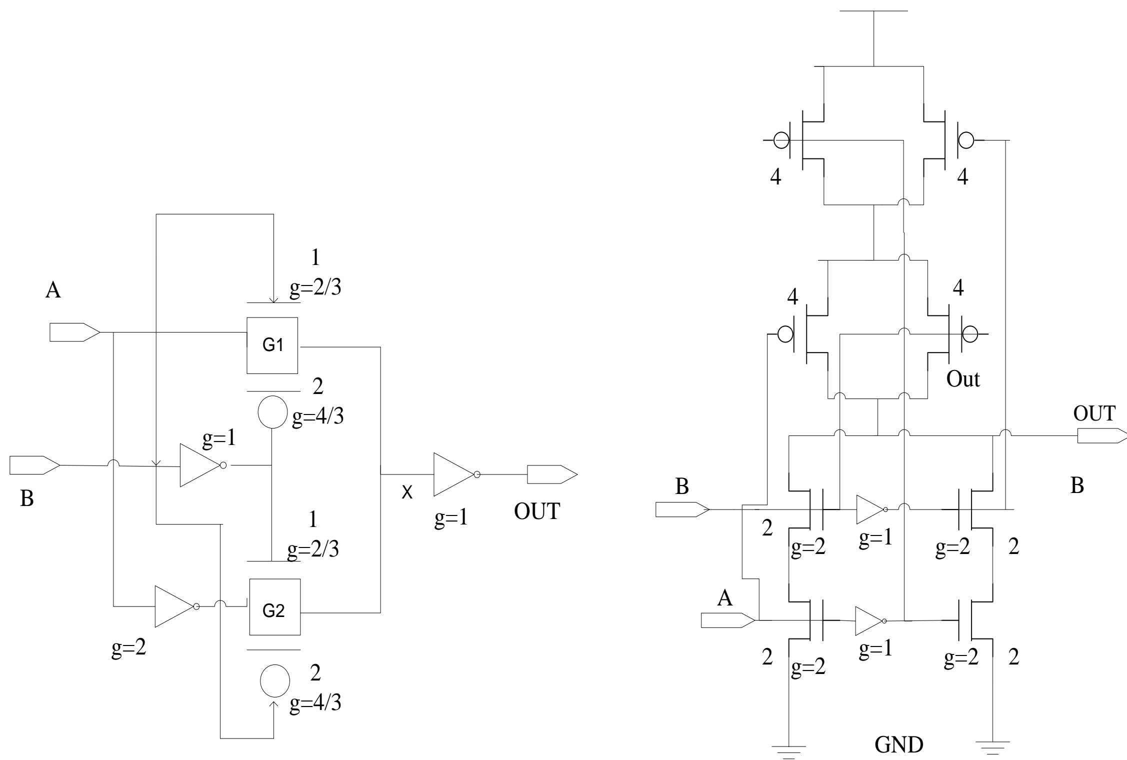

Figure 9.7: Device sizing for T-Gate XOR2X1 (left) and standard CMOS XOR2X1 (right)

XNOR2X1

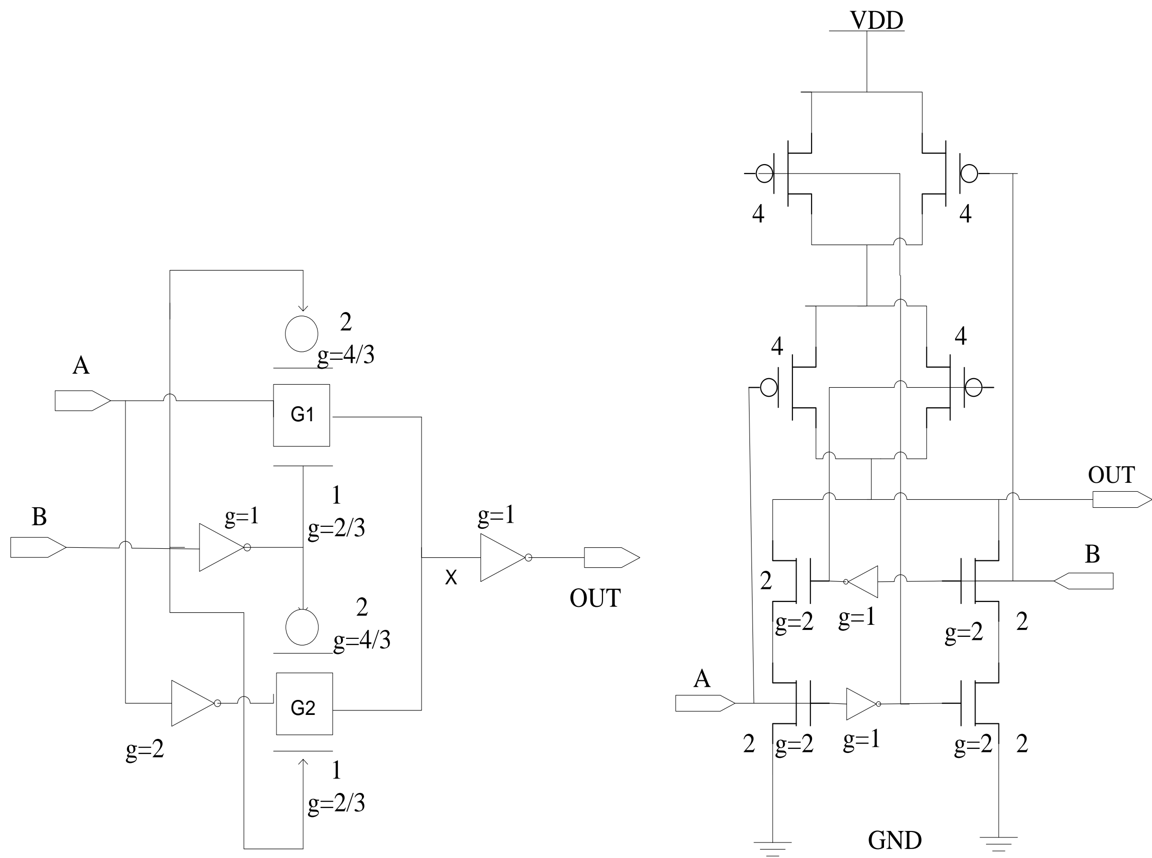

Figure 9.8: Device sizing for T-Gate XNOR2X1 (left) and standard CMOS XNOR2X1 (right)

MUX2X1:

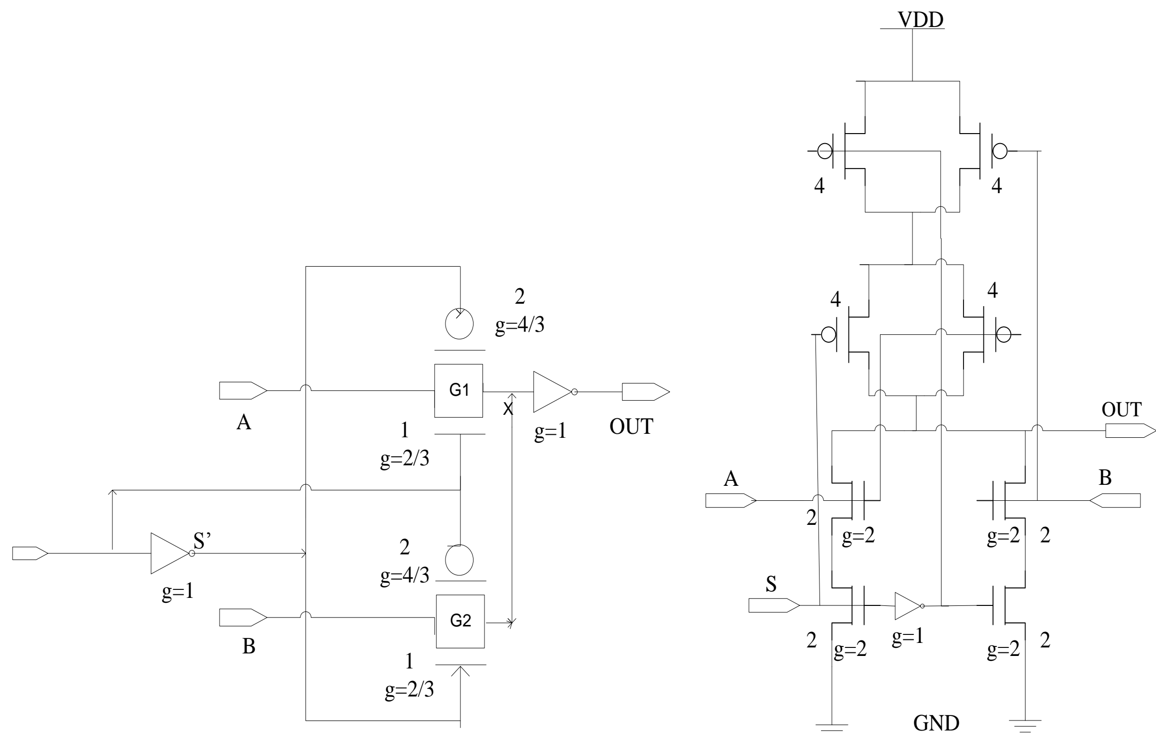

Figure 9.9: Device sizing for T-Gate MUX2X1 (left) and Standard CMOS MUX2X1 (right)

Flip-Flop: It has been shown in [1] that the dynamic registers are not at all appropriate for sub-threshold application due to leakage throughout comparatively longer clock period and more prone to lose its state due to poor noise margin. Hence [1] compares two static register architectures: Multiplexer based T-gate Flip-Flop and PowerPC 603. The experiment results in [1] clearly demonstrate that T-Gate design is better in terms of SNM, setup and hold time, total energy and clock to Q propagation delay. So we use a T-Gate based Flip Flop Architecture in our design.

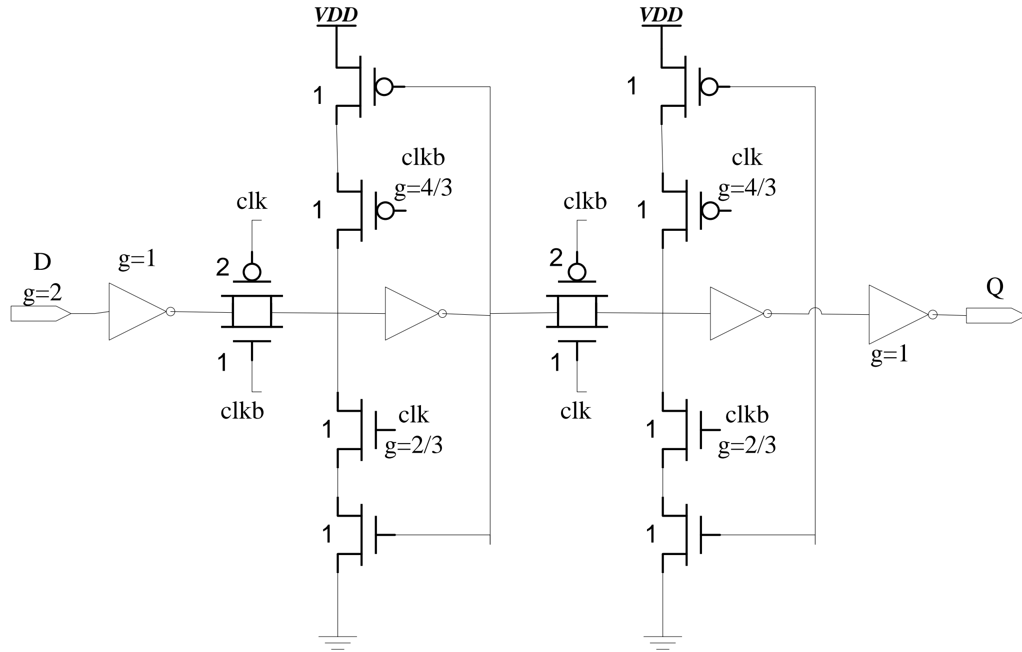

Figure 9.10: Power PC 603 static register

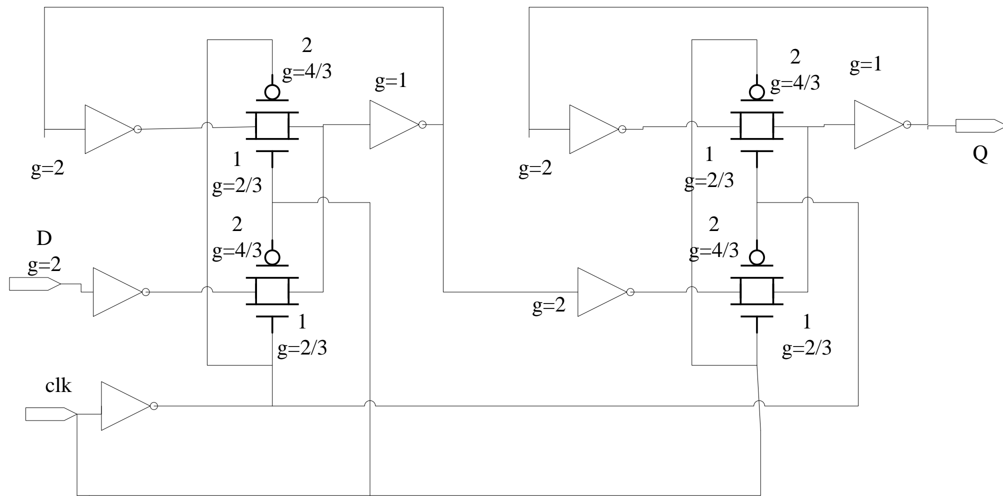

Figure 9.11: Multiplexer based T-Gate Register

CHAPTER X

T-GATE CELL LIBRARY IMPLAMENTATION

10.1 IMPLEMENTATION FLOW REVIEW

The T-Gate cell library implementation flow[20] is shown in Figure 10.1. Physical implementation starts with transistor level schematic entry in cadence schematic editor. The schematic of a T-Gate NAND2X1 gate is shown in Figure 10.2. After the schematic is entered the implemented logic functionality is verified with a test bench in cadence analog design environment

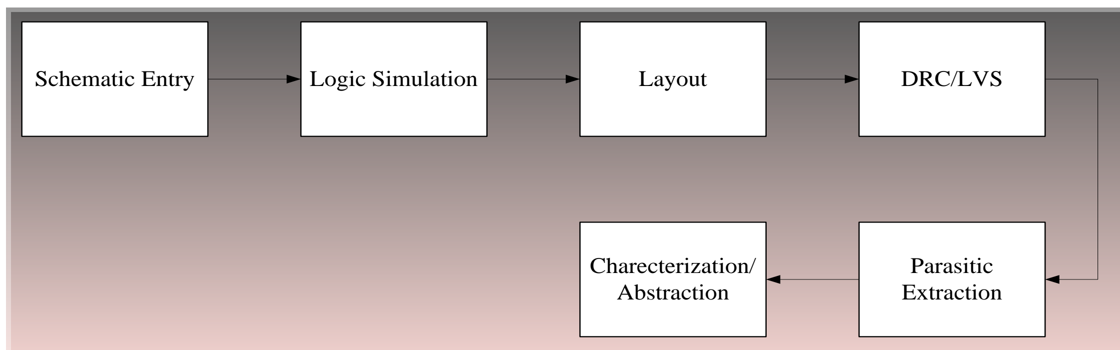

Figure 10.1 Digital cell library implementation flows

If the functionality passes the test, the next step is to implement the physical layout. The layout is made as per the process specification in order to remove any design rule violation(DRC). The grids are calculated for the layout following the method described in [31] and 0.6um in case of this particular implementation The layout view of a 2 input T-gate NAND is shown in Figure 10.3.

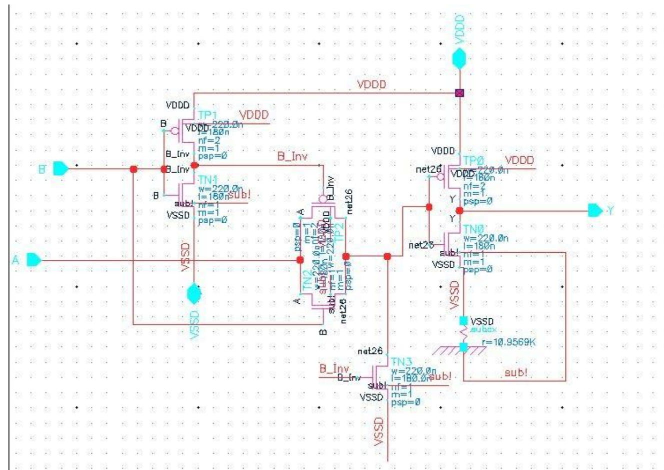

Figure 10.2 T-Gate NAND2X1 schematic

The next step is to do a DRC and LVS check on the layout. In order to run LVS, the layout has to be DRC error free. After clearing the DRCs, a LVS(Layout vs Schematic check) is done to confirm that the layout matches the corresponding schematic. LVS will pass when the transistor network and pins in the layout match with that of the respective schematic. This step should be followed by a parasitic extraction in cadence. Figure 10.3 shows an extracted view of the same layout shown in Figure 10.3. The next stage is library characterization and abstraction. Defined boundaries are ensuring DRC abutment, boundary box and girding for pin placement.

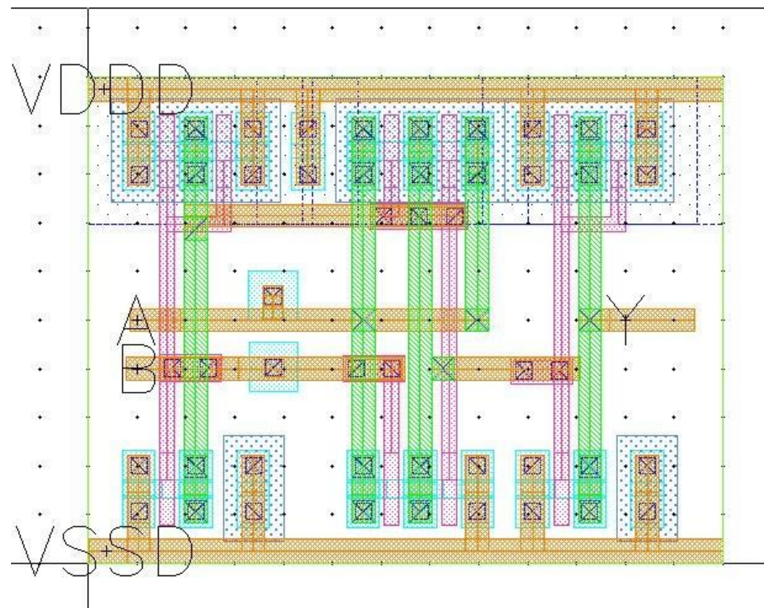

Figure 10.3: T-Gate NAND2X1 gate layout

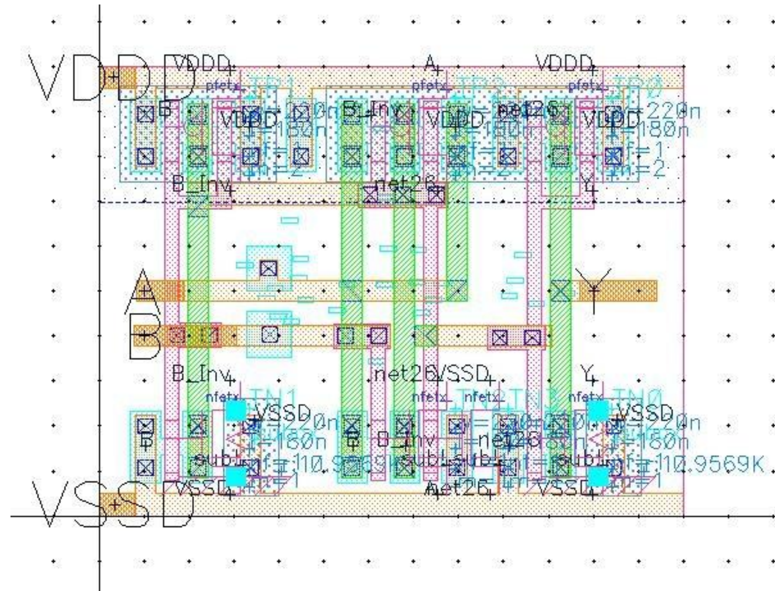

Figure 10.4 T-Gate NAND2X1 extracted view

The next step is the characterization of the digital cell library. A detailed description of the characterization process is given in [31]. In this case the library is characterized at a VDDD of 400mv and room temperature (for typical PVT consideration) and the setup file modified accordingly. Encounter library characterizer is used for library characterization. The input and output files for this process has been shown in Figure 10.5. The output files produced by ELC are <filename.>.lib(timing file), <filename>.v (Verilog description of logic gates) e.t.c. a sample .lib, .htm and .v file is shown in Appendix A, showing timing description(.lib file) for a few T-Gates logic cells, along with a sample setup file specific for the T-Gate cell library under development.

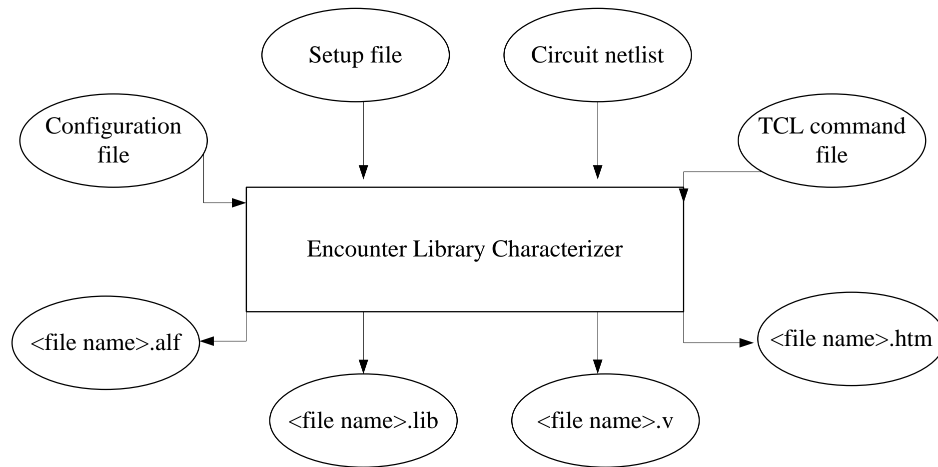

Figure 10.5: input and output files of ELC

After the characterization, an abstract view can be generated for the T-gate cell library using cadence abstract generator for back end processing. The abstract view only contains information

about the bounding box, signal connections and wiring blockage of the cells. Figure 10.6 shows the abstract view of T-Gate NAND2X1 gate. The abstract generator outputs library exchange format file (<filename>.lef) containing the abstract information of the cells and is shown in Appendix B.

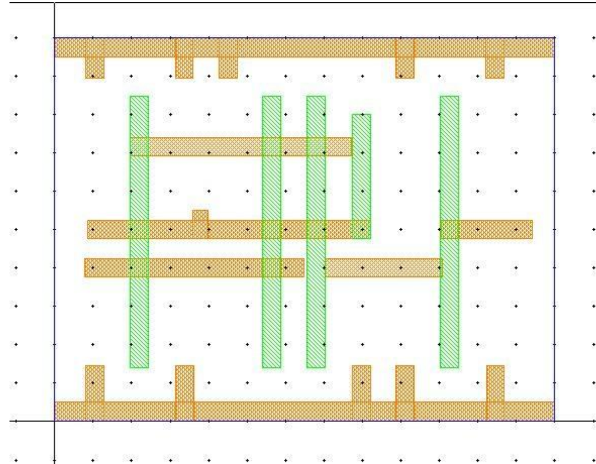

Figure 10.6: Abstract view for T-Gate 2 input NAND gate

CHAPTER XI

SYNTHESIS RESULTS COMPARISON

11.1 RESULTS COMPARISON

The T-Gate cell library has been characterized at VDDD equals 400mV, typical process corner and 27o Centigrade temperature as was the standard CMOS cell library under comparison. A seven stage NAND-NOR ring oscillator(RO) is simulated both in standard CMOS and with a T-Gate topology at the typical process corner, room temperature while varying VDDD to measure the energy consumed per cycle (EPC). The results are shown in Table 11.1. The T-Gate ring oscillator demonstrates higher energy per cycle (EPC) within the range of VDDDs from 400mV to 600mV but outperforms CMOS at VDDD=800mV. The T-Gate ring oscillator output frequency is lower than its CMOS equivalent at any VDDDs under consideration while showing a better static performance in the range of 400mV to 800mV and better dynamic behavior at 800mV however with a penalty in clock rate. The MNI controller is synthesized at a target frequency of 200 KHz with both of these libraries and their results are compared. A comparison of time slack, Area and power estimations at VDDD=400mV are presented in Table 11.2. The CMOS library performs better in terms of area and total power while the T-Gate exhibits better slack times. Table 11.2 also presents synthesis results for MNI controller with the T-Gate library at different operating VDDDs and it can be noticed that the change in VDDD does not produce a significant improvement in slack time. From the results in Table 11.1 it is noticed the T-gate ring oscillator is much slower than its CMOS logic counterpart at all VDDDs of operation.

Table 11.1 static power, dynamic power and energy per cycle comparison between T-Gate and CMOS RO

VDDD (mV)	Design	Freq (MHz)	Power Dynamic (nW)	Power static (nW)	EPC (f J)
400	T-Gate	6.8	81.5	0.13	1.19
500	T-Gate	25.8	459.5	0.18	1.77
600	T-Gate	64.5	2057.45	0.25	3.18
800	T-Gate	170.9	14305.4	0.44	8.36
400	CMOS	30.65	248.69	0.47	0.81
500	CMOS	103.41	1409.09	1.22	1.36
600	CMOS	215.51	3848.18	280.6	1.78
800	CMOS	486.38	61520.0	51184	12.64

Table 11.2 Synthesis results for MNI controller

Library Type	VDDD (mv)	Area (sq um)	Time Slack (us)	Total Power (uW)
CMOS	400	90853.0	2.29	15.39
T-Gate	400	99590.0	2.35	16.96
T-Gate	500	78218.8	2.46	19.42
T-Gate	600	64715.2	2.48	28.07

A parametric-frequency sweep is performed on a chain of 7 stage alternate NAND-NOR both in CMOS and in T-Gate to plot and measure the static and dynamic behavior of the logic cells observed. The static behavior is verified by sweeping the frequency of the input clock from dc to 60 KHz in 1 KHz steps while keeping VDDD at 400mv. See Figure 11.1. The parametric-frequency sweep reveals that the T-Gate shows a better static performance in the range of 1 to 60KHz. At certain frequency beyond 60 kHz, dynamic power starts dominating and T-Gates are outperformed by CMOS. This is in agreement to the results of Table 11.1.

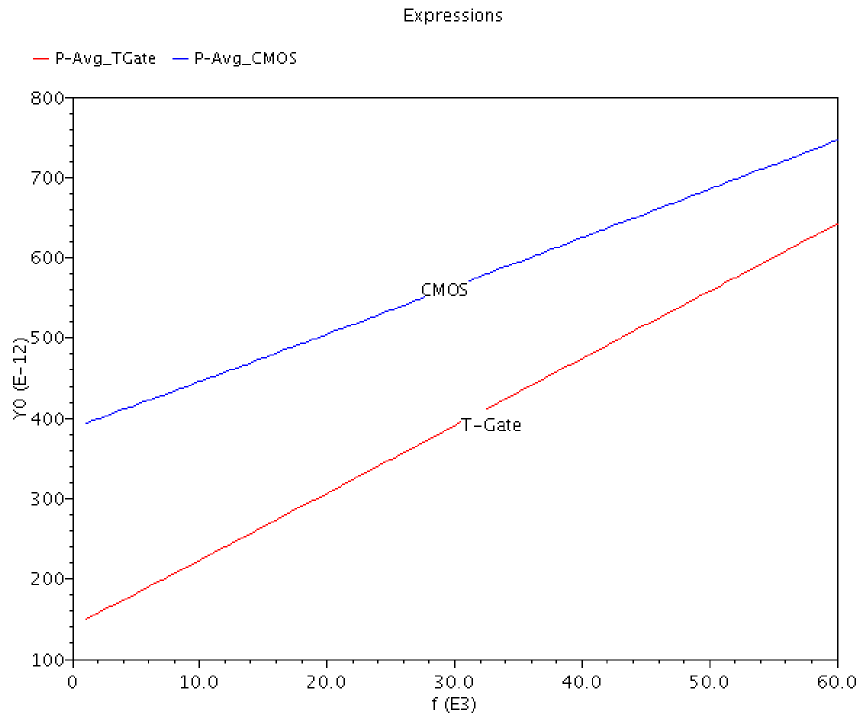

Figure 11.1 Static behavior of T-Gate vs CMOS

The dynamic behavior can be verified by performing a frequency sweep on the same circuit but with a greater range of frequency. A parametric frequency sweep is performed on the input clock of the NAND-NOR chain as before over the range of 50Hz to 7MHz with a step size of 75 KHz. The results for different VDDDs are plotted in Figure 11.2 and Figure 11.3 for T-Gate and CMOS respectively. These two figures reveal the fact that T-Gate is having a higher slope of average power dissipation. In the region where dynamic power is dominant $P_{Avg} \sim C_L \times VDDD^2 \times freq$ and $P_{Avg}/freq$ determines the slope of the power carve if VDDD is fixed. This is termed as Energy per Cycle(EPC) previously and the plot comes in agreement with Table 11.1 demonstrating higher energy per cycle (EPC).

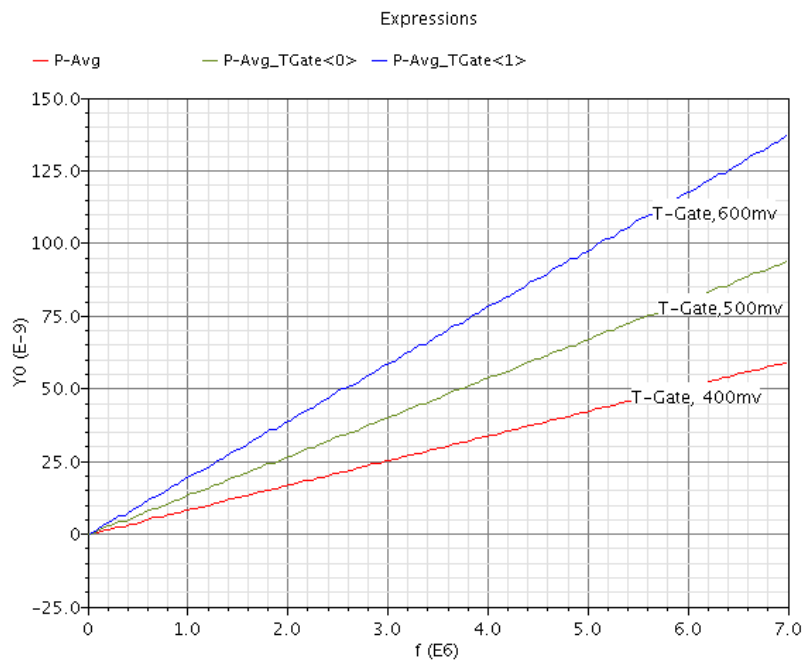

Figure 11.2 Dynamic power behaviors of T-Gate NAND-NOR chain vs VDDD

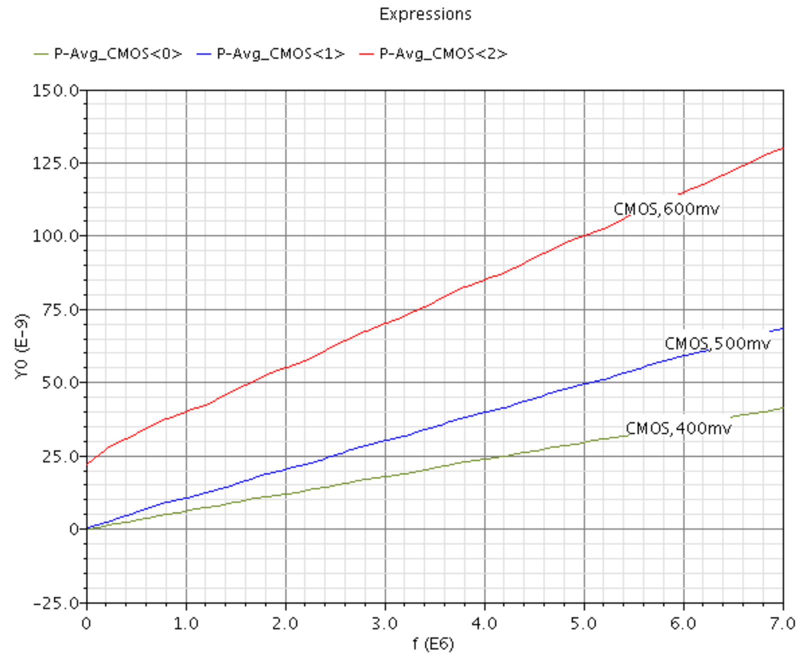

Figure 11.3 Dynamic power behaviors of CMOS NAND-NOR chain vs VDDD

The V_{Trip} distribution obtained by 200 point MC simulation taking process variation and mismatch into account along with the VTC for a T-gate based NAND2X1 is shown in Figure 11.4. The failure rate is zero as measured in Chapter III as the number no sample falls beyond our acceptable range at VDDD=400mV. Sigma(σ) for the distribution is 13.058mV as displayed in Figure 11.4. We also perform a 5k point MC simulation on VTrip of T-Gate based NAND2X1 with process variation and mismatch into account

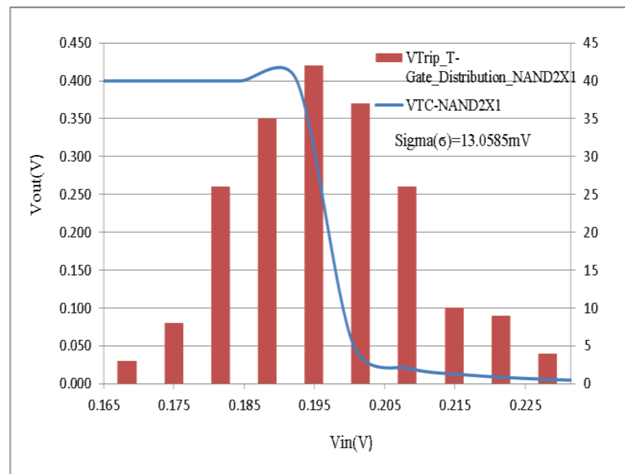

Figure 11.4 VTC and VTrip distribution(200 Point MC) of T-Gate NAND2X1

and record the Mean and Sigma of the VTrip distribution as presented in Table 11.3 along with the 200 point MC simulation data. We notice insignificant change in Mean and Sigma Values as we move from 200 point to 5k point MC simulation.

Table 11.3 MC simulation for VTrip of T-Gate NAND2X1 at VDDD=400mV

Gate Type	Type	Number of Samples	Mean of VTrip (mV)	Sigma of VTrip (mV)
T-Gate NAND2X1	Process variation and mismatch	200	198..92	13.05
T-Gate NAND2X1	Process variation and mismatch	5000	198.55	12.77

11.2 CONCLUSION

The T-Gate cells are observed to have lower input capacitance than its CMOS logic gate equivalent. The T-Gate cells have narrower VTrip distribution(hence better rate of reduction of failure with increasing VDDD) than CMOS logic gates but CMOS gate shows better SNM at any VDDD of operation and hence more suitable for low power operation. Except for MUX2X1 the CMOS logic gates under consideration should be a better performer than T-Gate logic gates in terms of the off current. Minimum PDP is achieved at minimum device finger size which is also verified to be sufficient to mitigate rise time requirement to maintain FO4 loading along with some nominal wire capacitance under worst case PVT consideration. While compared with the existing low power CMOS logic equivalent, the T-Gates shows better static behavior but slower in clock rate at any VDDD of operation. The energy per cycle(EPC) is higher in case of T-Gate within the range of VDDD from 400mv to 600mv while at 800mv the T-Gate logic gates perform better in terms of EPC than the existing low power CMOS logic gates. Comparable slack time is noticed when the target design is synthesized at typical PVT corner with both the libraries under test with penalty in power in case of T-Gate logic.

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APPENDICES

Appendix A

Sample timing file<.lib> for T-Gate NAND2X1 and NOR2X1, at VDDD=400mV, 27^0 C and tt corner.

```
/* ---------------- *
 * Design : NAND2X1 *
 * ---------------- */
cell (NAND2X1) {
  area : 0.0;
  cell_leakage_power : 0.266194;
  pin(A)  {
    direction : input;
    capacitance : 0.00190482;
    rise_capacitance : 0.00190482;
    fall_capacitance : 0.00185689;
    rise_capacitance_range ( 0.000827756, 0.00298188) ;
    fall_capacitance_range ( 0.000773478, 0.00294029) ;
    internal_power() {
      rise_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.000073, 0.000073, 0.000073, 0.000073, 0.000073,
0.000073");
      }
      fall_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.000073, 0.000073, 0.000073, 0.000073, 0.000073,
0.000073");
      }
    }
  }
  pin(B)  {
    direction : input;
    capacitance : 0.00100275;
    rise_capacitance : 0.00100231;
    fall_capacitance : 0.00100275;
    rise_capacitance_range ( 0.00096594, 0.00103869) ;
    fall_capacitance_range ( 0.000966702, 0.0010388) ;
    internal_power() {
      rise_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.00001, 0.000007, 0.000005, 0.000004, 0.000005,
0.000013");
```

```
      }
      fall_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.000236, 0.000234, 0.000231, 0.000231, 0.000231,
0.000236");
      }
    }
  }
  pin(Y)  {
    direction : output;
    capacitance : 0;
    rise_capacitance : 0;
    fall_capacitance : 0;
    rise_capacitance_range ( 0, 0) ;
    fall_capacitance_range ( 0, 0) ;
    max_capacitance : 0.000114858;
    function : "(!(A B))";
    timing() {
      related_pin : "A";
      timing_sense : negative_unate;
      cell_rise(delay_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "3.99739, 4.39519, 4.84576, 5.72013, 6.58355, 7.01323", \
          "5.08883, 5.48414, 5.93423, 6.8093, 7.67312, 8.10342", \
          "7.4132, 7.80379, 8.25212, 9.1263, 9.98999, 10.4199", \
          "12.0251, 12.4438, 12.8875, 13.76, 14.6201, 15.0486", \
          "19.8101, 20.6521, 21.4144, 22.668, 23.6794, 24.1554", \
          "31.3916, 33.1034, 34.6795, 37.2323, 39.218, 40.0915");
      }
      rise_transition(delay_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "1.45527, 2.04878, 2.76428, 4.23805, 5.71305, 6.45418", \
          "1.466, 2.0564, 2.78235, 4.23816, 5.71554, 6.45624", \
          "1.48453, 2.07212, 2.77902, 4.23558, 5.71052, 6.45995", \
          "1.92834, 2.39386, 3.02638, 4.35804, 5.80539, 6.52244", \
          "4.57263, 4.92868, 5.40152, 6.38102, 7.48317, 8.05238", \
          "11.7441, 12.1873, 12.4472, 13.5329, 14.8067, 15.2464");
      }
      cell_fall(delay_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "4.20118, 4.5378, 4.91305, 5.63078, 6.33398, 6.6767", \
          "5.20855, 5.54412, 5.91808, 6.63271, 7.3332, 7.68305", \
          "7.39251, 7.72673, 8.09929, 8.81223, 9.51236, 9.86081", \
          "11.78, 12.1665, 12.5526, 13.2684, 13.9667, 14.3139", \
          "19.0566, 19.9329, 20.6935, 21.9289, 22.8666, 23.3084", \
          "29.8883, 31.5122, 33.1156, 35.6812, 37.6417, 38.5699");
      }
      fall_transition(delay_template_6x6) {
```

```
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "1.40991, 1.93544, 2.57732, 3.88261, 5.20231, 5.85545", \
        "1.41368, 1.94076, 2.58137, 3.88008, 5.20505, 5.8641", \
        "1.43966, 1.95815, 2.59196, 3.89084, 5.20832, 5.87052", \
        "1.93313, 2.34172, 2.88885, 4.07492, 5.32568, 5.9631", \
        "4.6614, 4.92904, 5.52916, 6.46889, 7.47143, 7.9808", \
        "10.8593, 11.8696, 12.6107, 14.1491, 15.4901, 15.9531");
    }
  }
  timing() {
    related_pin : "B";
    timing_sense : negative_unate;
    cell_rise(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "7.1504, 7.55316, 8.00623, 8.88214, 9.74545, 10.175", \
        "8.24288, 8.64503, 9.09816, 9.97522, 10.8387, 11.2677", \
        "10.4614, 10.8633, 11.3156, 12.1921, 13.0552, 13.4841", \
        "14.8369, 15.2397, 15.6923, 16.5662, 17.4288, 17.8576", \
        "22.152, 22.5565, 23.0088, 23.882, 24.746, 25.175", \
        "33.6124, 34.0274, 34.4792, 35.3546, 36.2147, 36.6431");
    }
    rise_transition(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "1.46456, 2.06277, 2.76404, 4.24366, 5.71534, 6.45726", \
        "1.4674, 2.05482, 2.78353, 4.24008, 5.72324, 6.4575", \
        "1.46487, 2.05524, 2.78405, 4.23499, 5.7226, 6.45757", \
        "1.46768, 2.05913, 2.7888, 4.23472, 5.71489, 6.4581", \
        "1.49307, 2.08464, 2.77942, 4.22356, 5.70909, 6.44293", \
        "1.58552, 2.14841, 2.86491, 4.28151, 5.69638, 6.46846");
    }
    cell_fall(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "6.28286, 6.62211, 6.99679, 7.71449, 8.41576, 8.7641", \
        "7.42243, 7.76267, 8.1383, 8.85578, 9.55874, 9.90231", \
        "9.74477, 10.077, 10.4503, 11.1669, 11.8687, 12.2131", \
        "14.247, 14.5839, 14.9571, 15.6699, 16.37, 16.7178", \
        "21.8276, 22.1683, 22.5418, 23.2604, 23.9576, 24.3047", \
        "33.6479, 34.0026, 34.3831, 35.1048, 35.8115, 36.1559");
    }
    fall_transition(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "1.40402, 1.93623, 2.57421, 3.87874, 5.20105, 5.86393", \
        "1.40205, 1.9309, 2.572, 3.87566, 5.2034, 5.85911", \
        "1.40261, 1.93383, 2.57527, 3.88051, 5.20148, 5.86386", \
```

```
          "1.40515, 1.93476, 2.57908, 3.8767, 5.19876, 5.85614", \
          "1.44738, 1.96749, 2.59766, 3.88917, 5.21042, 5.8727", \
          "1.62335, 2.112, 2.71685, 3.97189, 5.26481, 5.91697");
      }
    }
    internal_power() {
      related_pin : "A";
      rise_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000274, 0.000275, 0.000276, 0.000278, 0.000279,
0.000279", \
          "0.000273, 0.000274, 0.000275, 0.000276, 0.000277,
0.000278", \
          "0.000271, 0.000272, 0.000273, 0.000274, 0.000276,
0.000276", \
          "0.00027, 0.000271, 0.000272, 0.000273, 0.000274,
0.000274", \
          "0.000273, 0.000273, 0.000272, 0.000273, 0.000273,
0.000273", \
          "0.000279, 0.000278, 0.000277, 0.000276, 0.000276,
0.000276");
      }
      fall_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000131, 0.00013, 0.000129, 0.000127, 0.000126,
0.000125", \
          "0.000133, 0.000132, 0.000131, 0.000129, 0.000128,
0.000127", \
          "0.000134, 0.000133, 0.000132, 0.000131, 0.00013,
0.00013", \
          "0.000134, 0.000134, 0.000133, 0.000133, 0.000132,
0.000132", \
          "0.000132, 0.000131, 0.000132, 0.000132, 0.000132,
0.000132", \
          "0.000124, 0.000124, 0.000126, 0.000127, 0.000128,
0.000128");
      }
    }
    internal_power() {
      related_pin : "B";
      rise_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000508, 0.00051, 0.000512, 0.000513, 0.000514,
0.000514", \
          "0.000506, 0.000508, 0.00051, 0.000511, 0.000512,
0.000512", \
          "0.000504, 0.000506, 0.000507, 0.000509, 0.00051,
0.00051", \
```

```
          "0.000503, 0.000504, 0.000506, 0.000507, 0.000508,
0.000508", \
          "0.000501, 0.000503, 0.000504, 0.000505, 0.000506,
0.000507", \
          "0.000504, 0.000506, 0.000507, 0.000508, 0.000509,
0.000509");
      }
      fall_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000073, 0.000072, 0.00007, 0.000069, 0.000067,
0.000067", \
          "0.000076, 0.000075, 0.000073, 0.000072, 0.000071,
0.00007", \
          "0.000078, 0.000077, 0.000076, 0.000074, 0.000073,
0.000073", \
          "0.00008, 0.000078, 0.000077, 0.000076, 0.000075,
0.000075", \
          "0.000079, 0.000078, 0.000077, 0.000075, 0.000075,
0.000074", \
          "0.000073, 0.000072, 0.000071, 0.000069, 0.000068,
0.000068");
      }
    }
  }
}

/* --------------- *
 * Design : NOR2X1 *
 * --------------- */
cell (NOR2X1) {
  area : 0.0;
  cell_leakage_power : 0.265889;
  pin(A)  {
    direction : input;
    capacitance : 0.0022224;
    rise_capacitance : 0.0021694;
    fall_capacitance : 0.0022224;
    rise_capacitance_range ( 0.000937433, 0.00340137) ;
    fall_capacitance_range ( 0.000990908, 0.0034539) ;
    internal_power() {
      rise_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.000073, 0.000074, 0.000074, 0.000074, 0.000074,
0.000073");
      }
      fall_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.000073, 0.000074, 0.000074, 0.000073, 0.000073,
0.000073");
      }
    }
  }
```

```
  pin(B)  {
    direction : input;
    capacitance : 0.00136646;
    rise_capacitance : 0.00136631;
    fall_capacitance : 0.00136646;
    rise_capacitance_range ( 0.00123347, 0.00149914) ;
    fall_capacitance_range ( 0.00123404, 0.00149887) ;
    internal_power() {
      rise_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.000019, 0.000019, 0.00002, 0.000022, 0.000025, 
0.000033");
      }
      fall_power(passive_energy_template_6x1) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        values ("0.00027, 0.000266, 0.00026, 0.000255, 0.000251, 
0.000252");
      }
    }
  }
  pin(Y)  {
    direction : output;
    capacitance : 0;
    rise_capacitance : 0;
    fall_capacitance : 0;
    rise_capacitance_range ( 0, 0) ;
    fall_capacitance_range ( 0, 0) ;
    max_capacitance : 0.00000274907;
    function : "(!(A+B))";
    timing() {
      related_pin : "A";
      timing_sense : negative_unate;
      cell_rise(delay_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "4.5052, 4.9166, 5.37193, 6.24803, 7.11022, 7.53954", \
          "5.53479, 5.94291, 6.39812, 7.27577, 8.13946, 8.56972", \
          "7.80114, 8.20608, 8.66183, 9.54001, 10.4042, 10.8345", \
          "12.3702, 12.7723, 13.2326, 14.0815, 14.9691, 15.3979", \
          "20.4257, 21.2141, 21.9447, 23.0959, 24.083, 24.539", \
          "32.4806, 34.124, 35.6469, 37.971, 39.8845, 40.7303");
      }
      rise_transition(delay_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "1.52657, 2.10597, 2.81292, 4.27403, 5.73748, 6.45386", \
          "1.53521, 2.11572, 2.82297, 4.27438, 5.72658, 6.45718", \
          "1.56098, 2.12724, 2.83036, 4.28152, 5.74065, 6.47667", \
          "1.89077, 2.40517, 3.01648, 4.36993, 5.81596, 6.54014", \
          "4.35886, 4.62766, 5.09534, 6.07829, 7.13822, 7.73516", \
          "11.2319, 11.2555, 11.6575, 12.9154, 13.9139, 14.4409");
      }
```

```
    cell_fall(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "4.29647, 4.64048, 5.02083, 5.73836, 6.44221, 6.79178", \
        "5.31452, 5.65652, 6.03422, 6.7526, 7.45597, 7.8055", \
        "7.53665, 7.88422, 8.25568, 8.97278, 9.67981, 10.0286", \
        "12.0275, 12.3901, 12.7614, 13.4815, 14.1709, 14.5062", \
        "19.6154, 20.3815, 21.0966, 22.2646, 23.2084, 23.6223", \
        "30.8468, 32.4635, 33.9829, 36.2817, 38.2526, 39.1052");
    }
    fall_transition(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "1.43542, 1.96632, 2.60344, 3.90459, 5.21662, 5.87115", \
        "1.44269, 1.97035, 2.60884, 3.90609, 5.21925, 5.87672", \
        "1.46327, 1.98686, 2.61785, 3.9079, 5.22396, 5.88452", \
        "1.84723, 2.2821, 2.87447, 4.06132, 5.32279, 5.9749", \
        "4.38917, 4.75692, 5.27761, 6.18008, 7.19273, 7.70641", \
        "10.5454, 11.1199, 11.8822, 13.503, 14.7337, 15.2003");
    }
  }
  timing() {
    related_pin : "B";
    timing_sense : negative_unate;
    cell_rise(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "6.91186, 7.32035, 7.77582, 8.65283, 9.5163, 9.94584", \
        "8.03068, 8.43823, 8.89291, 9.7679, 10.6294, 11.0587", \
        "10.263, 10.6708, 11.1289, 12.0037, 12.8668, 13.2963", \
        "14.697, 15.104, 15.5584, 16.433, 17.2946, 17.7242", \
        "22.1078, 22.5186, 22.9733, 23.8423, 24.7014, 25.1325", \
        "33.6928, 34.1154, 34.5747, 35.4488, 36.3072, 36.735");
    }
    rise_transition(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "1.52342, 2.10063, 2.81704, 4.27123, 5.73596, 6.47656", \
        "1.5209, 2.10129, 2.81046, 4.27253, 5.73562, 6.45905", \
        "1.52068, 2.10222, 2.80852, 4.27153, 5.73452, 6.474", \
        "1.52273, 2.10229, 2.81185, 4.27465, 5.73775, 6.45616", \
        "1.54907, 2.11643, 2.81234, 4.24034, 5.7159, 6.45119", \
        "1.6507, 2.20132, 2.88843, 4.29762, 5.70927, 6.44322");
    }
    cell_fall(delay_template_6x6) {
      index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
      index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
      values ( \
        "6.61316, 6.96142, 7.33343, 8.05567, 8.75952, 9.10847", \
        "7.75149, 8.10012, 8.48059, 9.20172, 9.90499, 10.2539", \
```

```
          "10.0599, 10.4101, 10.7918, 11.5131, 12.2172, 12.5667", \
          "14.5545, 14.9033, 15.2835, 16.0041, 16.707, 17.0555", \
          "22.1348, 22.488, 22.8636, 23.5802, 24.2767, 24.6239", \
          "34.0155, 34.3729, 34.765, 35.4862, 36.1951, 36.5436");
      }
      fall_transition(delay_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "1.46094, 1.984, 2.61785, 3.91192, 5.21963, 5.87861", \
          "1.46223, 1.98418, 2.6221, 3.91273, 5.22393, 5.88865", \
          "1.45884, 1.98277, 2.61811, 3.91459, 5.22707, 5.88826", \
          "1.46012, 1.98514, 2.62023, 3.91106, 5.22731, 5.88873", \
          "1.49491, 2.01306, 2.65334, 3.92628, 5.22024, 5.87969", \
          "1.65293, 2.15945, 2.75821, 3.9973, 5.27856, 5.92669");
      }
    }
    internal_power() {
      related_pin : "A";
      rise_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000369, 0.00037, 0.000371, 0.000373, 0.000374,
0.000374", \
          "0.000368, 0.000369, 0.00037, 0.000371, 0.000372,
0.000373", \
          "0.000366, 0.000367, 0.000368, 0.000369, 0.00037,
0.000371", \
          "0.000366, 0.000367, 0.000367, 0.000367, 0.000368,
0.00037", \
          "0.000368, 0.000368, 0.000367, 0.000368, 0.000367,
0.000369", \
          "0.000374, 0.000373, 0.000371, 0.000371, 0.00037,
0.00037");
      }
      fall_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000226, 0.000225, 0.000224, 0.000222, 0.000221,
0.00022", \
          "0.000228, 0.000226, 0.000225, 0.000224, 0.000223,
0.000222", \
          "0.000229, 0.000228, 0.000227, 0.000226, 0.000225,
0.000225", \
          "0.000229, 0.000229, 0.000228, 0.000228, 0.000228,
0.000228", \
          "0.000227, 0.000227, 0.000226, 0.000227, 0.000227,
0.000227", \
          "0.000219, 0.00022, 0.000221, 0.000222, 0.000223,
0.000223");
      }
    }
```

```
    internal_power() {
      related_pin : "B";
      rise_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000587, 0.000589, 0.00059, 0.000591, 0.000592,
0.000592", \
          "0.000588, 0.000589, 0.00059, 0.000592, 0.000592,
0.000593", \
          "0.00059, 0.000591, 0.000592, 0.000594, 0.000594,
0.000595", \
          "0.000595, 0.000596, 0.000597, 0.000598, 0.000599,
0.000599", \
          "0.000602, 0.000603, 0.000604, 0.000605, 0.000606,
0.000606", \
          "0.000615, 0.000617, 0.000617, 0.000619, 0.000619,
0.00062");
      }
      fall_power(energy_template_6x6) {
        index_1 ("2.4, 4.8, 9.6, 19.2, 38.4, 76.8");
        index_2 ("0.0001, 0.0006, 0.0012, 0.0024, 0.0036, 0.0042");
        values ( \
          "0.000352, 0.000354, 0.000355, 0.000357, 0.000358,
0.000358", \
          "0.000352, 0.000354, 0.000355, 0.000357, 0.000358,
0.000358", \
          "0.000355, 0.000356, 0.000357, 0.000359, 0.00036,
0.00036", \
          "0.000359, 0.000361, 0.000362, 0.000363, 0.000364,
0.000365", \
          "0.000368, 0.000369, 0.000371, 0.000372, 0.000373,
0.000373", \
          "0.000388, 0.000389, 0.00039, 0.000392, 0.000392,
0.000393");
      }
    }
  }
}
```

Sample Verilog description file<.v> for T-Gate NAND2X1 and NOR2X1, at VDDD=400mV, 27^0 C and tt corner.

```
`timescale 1ns/10ps
`celldefine
module NAND2X1 (A, B, Y);
input  A ;
input  B ;
output Y ;
```

```
   and (I0_out, A, B);
   not (Y, I0_out);

   specify
     // delay parameters
     specparam
       tplhl$A$Y = 4.2:4.2:4.2,
       tphlh$A$Y = 4:4:4,
       tplhl$B$Y = 6.3:6.3:6.3,
       tphlh$B$Y = 7.2:7.2:7.2;

     // path delays
     (B *> Y) = (tphlh$B$Y, tplhl$B$Y);
     (A *> Y) = (tphlh$A$Y, tplhl$A$Y);

   endspecify

endmodule
`endcelldefine

`timescale 1ns/10ps
`celldefine
module NOR2X1 (A, B, Y);
input  A ;
input  B ;
output Y ;

   or  (I0_out, A, B);
   not (Y, I0_out);

   specify
     // delay parameters
     specparam
       tplhl$A$Y = 4.3:4.3:4.3,
       tphlh$A$Y = 4.5:4.5:4.5,
       tplhl$B$Y = 6.6:6.6:6.6,
       tphlh$B$Y = 6.9:6.9:6.9;

     // path delays
     (B *> Y) = (tphlh$B$Y, tplhl$B$Y);
     (A *> Y) = (tphlh$A$Y, tplhl$A$Y);

   endspecify

endmodule
`endcelldefine
```

Appendix B

Sample Library exchange format file<.lef> for T-Gate NAND2X1 and NOR2X1

```
MACRO NAND2X1
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN NAND2X1 0 0 ;
  SIZE 7.8 BY 6 ;
  SYMMETRY X Y ;
  SITE CORE ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 2.15 2.86 2.39 3.3 ;
        RECT 0.51 2.86 4.92 3.14 ;
    END
  END A
  PIN B
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 0.47 2.26 3.89 2.54 ;
    END
  END B
  PIN VDDD
    DIRECTION INOUT ;
    USE POWER ;
    SHAPE ABUTMENT ;
    PORT
      LAYER M1 ;
        RECT 0.48 5.36 0.76 6 ;
        RECT 1.88 5.36 2.16 6 ;
        RECT 2.56 5.36 2.84 6 ;
        RECT 5.32 5.36 5.6 6 ;
        RECT 6.72 5.36 7 6 ;
        RECT 0 5.7 7.8 6 ;
    END
  END VDDD
```

```
  PIN VSSD
    DIRECTION INOUT ;
    USE GROUND ;
    SHAPE ABUTMENT ;
    PORT
      LAYER M1 ;
        RECT 0.48 0 0.76 0.88 ;
        RECT 1.89 0 2.17 0.88 ;
        RECT 4.64 0 4.92 0.88 ;
        RECT 5.32 0 5.6 0.88 ;
        RECT 6.73 0 7.01 0.88 ;
        RECT 0 0 7.8 0.3 ;
    END
  END VSSD
  PIN Y
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 6.03 2.86 7.45 3.14 ;
    END
  END Y
  OBS
    LAYER M1 ;
      RECT 0.47 2.26 3.89 2.54 ;
      RECT 1.18 4.15 4.62 4.43 ;
      RECT 0.51 2.86 4.92 3.14 ;
      RECT 2.15 2.86 2.39 3.3 ;
      RECT 4.22 2.26 6.04 2.54 ;
      RECT 6.03 2.86 7.45 3.14 ;
      RECT 0.48 5.36 0.76 6 ;
      RECT 1.88 5.36 2.16 6 ;
      RECT 2.56 5.36 2.84 6 ;
      RECT 5.32 5.36 5.6 6 ;
      RECT 6.72 5.36 7 6 ;
      RECT 0 5.7 7.8 6 ;
      RECT 0 0 7.8 0.3 ;
      RECT 0.48 0 0.76 0.88 ;
      RECT 1.89 0 2.17 0.88 ;
      RECT 4.64 0 4.92 0.88 ;
      RECT 5.32 0 5.6 0.88 ;
      RECT 6.73 0 7.01 0.88 ;
    LAYER M2 ;
      RECT 1.18 0.85 1.46 5.08 ;
      RECT 3.24 0.85 3.52 5.08 ;
      RECT 3.94 0.85 4.22 5.08 ;
      RECT 4.64 2.86 4.92 4.8 ;
      RECT 6.02 0.85 6.3 5.08 ;
  END
END NAND2X1
```

```
MACRO NOR2X1
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN NOR2X1 0 0 ;
  SIZE 9.6 BY 6 ;
  SYMMETRY X Y ;
  SITE CORE ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 0.41 3.46 7.02 3.74 ;
    END
  END A
  PIN B
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER M1 ;
        RECT 0.49 2.26 6.83 2.54 ;
    END
  END B
  PIN VDDD
    DIRECTION INOUT ;
    USE POWER ;
    SHAPE ABUTMENT ;
    PORT
      LAYER M1 ;
        RECT 0.48 4.97 0.76 6 ;
        RECT 1.88 4.97 2.16 6 ;
        RECT 2.58 4.97 2.86 6 ;
        RECT 3.26 4.97 3.54 6 ;
        RECT 4.66 4.97 4.94 6 ;
        RECT 7.42 4.97 7.7 6 ;
        RECT 8.82 4.97 9.1 6 ;
        RECT 0 5.7 9.6 6 ;
    END
  END VDDD
  PIN VSSD
    DIRECTION INOUT ;
    USE GROUND ;
    SHAPE ABUTMENT ;
    PORT
      LAYER M1 ;
        RECT 0.48 0 0.76 1.03 ;
        RECT 1.89 0 2.17 1.03 ;
        RECT 7.42 0 7.7 1.03 ;
        RECT 8.83 0 9.11 1.03 ;
        RECT 0 0 9.6 0.3 ;
    END
  END VSSD
```

```
    PIN Y
      DIRECTION OUTPUT ;
      USE SIGNAL ;
      PORT
        LAYER M1 ;
          RECT 8.26 2.86 9.03 3.14 ;
      END
    END Y
    OBS
      LAYER M1 ;
        RECT 1.3 4.05 4.58 4.33 ;
        RECT 0.49 2.26 6.83 2.54 ;
        RECT 0.41 3.46 7.02 3.74 ;
        RECT 4.1 2.86 7.91 3.14 ;
        RECT 8.26 2.86 9.03 3.14 ;
        RECT 0.48 4.97 0.76 6 ;
        RECT 1.88 4.97 2.16 6 ;
        RECT 2.58 4.97 2.86 6 ;
        RECT 3.26 4.97 3.54 6 ;
        RECT 4.66 4.97 4.94 6 ;
        RECT 7.42 4.97 7.7 6 ;
        RECT 8.82 4.97 9.1 6 ;
        RECT 0 5.7 9.6 6 ;
        RECT 0 0 9.6 0.3 ;
        RECT 0.48 0 0.76 1.03 ;
        RECT 1.89 0 2.17 1.03 ;
        RECT 7.42 0 7.7 1.03 ;
        RECT 8.83 0 9.11 1.03 ;
      LAYER M2 ;
        RECT 1.18 0.73 1.46 5.16 ;
        RECT 3.26 0.73 3.54 5.16 ;
        RECT 3.96 0.73 4.24 5.16 ;
        RECT 5.34 0.73 5.62 5.16 ;
        RECT 6.04 0.73 6.32 5.16 ;
        RECT 6.74 3.45 7.02 5.36 ;
        RECT 8.12 0.73 8.4 5.16 ;
    END
  END NOR2X1
```

VITA

Kanishka De

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