

AN ALGORITHM FOR TANT SYNTHESIS AND
ITS SEQUENTIAL APPLICATION

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ITS SEQUENTIAL APPLICATION

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CHAPTER I

INTRODUCTION

Digital logic circuit designers have many computer-aided design (CAD) packages at their disposal. That most current computers were designed by computers proves the practicality of such CAD programs. On a smaller scale, many algorithms and associated software packages solve the gate minimization problem for combinational logic design or select the optimum memory device from among given candidates to yield gate minimization for sequential problems. Digital logic designers choose a memory device, find the resulting logic equations, and minimize the combinational portion of the sequential feedback circuit. Another memory device is utilized only after dissatisfaction with the first has resulted. However, a CAD program can test all types of memory devices and yield a minimum combinational circuit for each device. Thus, the designer can be assured of finding the optimal design for given constraints. The problem investigated in this thesis is the design of optimal sequential circuits using NAND gates for the combinational portion. A list of several familiar memory devices is specified for the sequential portion of the problem. The number of gates and, secondarily, the number of inputs to those gates are minimized for each type of device.

Background

Historically, the problem of finding a minimum logic circuit has been divided into two parts: the combinational logic design problem and the memory selection problem. The usual criteria for minimization are propagation time and package count. In this thesis, the combinational problem under consideration is the design of optimal TANT networks, i.e., three-level NAND-gate circuits with true inputs only (1). Used in the examples as a convenient tool for visualization in combinational problems with few inputs is the circuit-action Karnaugh map. In the sequential problem, some of the memories to choose from are the D flip-flop, RS flip-flop, JK flip-flop, T (or toggle) flip-flop, and, of course, any clocked version of any of these.

The TANT restriction of three levels or less is used to minimize propagation time since any logic function can be realized in three levels, and propagation time is a function of the number of levels through which the signal must pass. Solving the minimum package count is not as straightforward and, in fact, is not the consideration when logic component (chip) design is considered. Therefore, for ease in the first case and correctness in the second, rather than minimum package count, minimum-gate and minimum-input realizations will be the goal. The solution of NAND circuits is easily used in an analogous manner to solve for NOR circuits (1-3). The uncomplemented requirement is typical for inputs to a logic circuit. However, since complemented inputs will be available as outputs from memory devices, this thesis actually deals with a modified TANT problem.

The majority of previous work on the NAND/NOR synthesis problem has been four categories: the double-complement technique (4-6),

decomposition (7-9), the head-tail approach (10-12), the map factoring approach (13-15). Although there has been some work in using integer programming (16-19), it has been of a much more general nature and not explicitly advantageous in the solution of the TANT problem. There also has been work done using exhaustive search (20, 21), but this method was used to generate a table of solutions for all possible small number of input problems and is not very practical for situations involving many input variables.

The double-complement technique, which is solving the two-level AND/OR problem by essentially a Quine-McCluskey approach and then inverting inputs to achieve the necessary negated inputs, is the most straightforward technique because of the equivalence of any two-level NAND structure and its corresponding AND/OR circuit (22). Although straightforward, this procedure usually does not yield an optimal (i.e., minimum-gate, minimum-input) realization for a given problem. A double-complement method was developed early by Gimpel (4) which involved certain extensions involving a prime implicant cover and closure (CC) table. Hohulin and Muroga (5) reported several alternative methods for solving the CC-table in Gimpel's algorithm suitable for computer processing, and these methods are implemented as computer programs. Ellis (6) extended the double-complement technique to NOR gates as well as NAND. Davidson (7) used decomposition, in which a first cut of the double-complement method is made, followed by backtracking for improvements while considering fan-in, fan-out, and level constraints. Dietmeyer and Su (8) used decomposition with factoring, assuming complemented inputs available and no level constraint. Schneider and Dietmeyer (9) extended decomposition solutions for multiple

outputs. Koh's (10) head-tail approach is based on first obtaining the essential prime implicants and then generating useful prime implicants. By various methods groupings are made to reduce the NAND circuit. Then a table analogous to the CC table is solved. Chakrabarti, Choudhury, and Basu (11) proposed an early head-tail investigation based upon analysis of production at the second-level gate outputs of the complement of the function as well as the desired minterms. Frackowiak (12) presented two approaches, one yielding a quasi-minimal hazardless solution and the other yielding a strictly minimal solution. Maley and Earle (13) initiated map factoring for finding gates from prime implicants by a method analogous to circling n-cubes on a Karnaugh map; hence, the name map factoring is appropriate. Eisenberg's (14) work was extended by Torng (15) to yield a systematic realization procedure for NAND networks by alternately inhibiting 0 and 1 entires in the Karnaugh map as the number of switching levels increases. After this primitive realization is obtained, a level reduction procedure is applied to reduce the number of levels to at most three. A transform technique is used to complete the design procedure. These various procedures provide a wide range of solutions to the TANT problem, with most of them having been implemented on digital computers. None of these procedures attacks the problem of associated sequential problems. Also, none of the publications give very extensive analysis of memory or CPU time requirements for computer implementations.

An Example

To demonstrate the TANT solution of a particular problem using the double-complement technique and subsequent improvements until an optimum

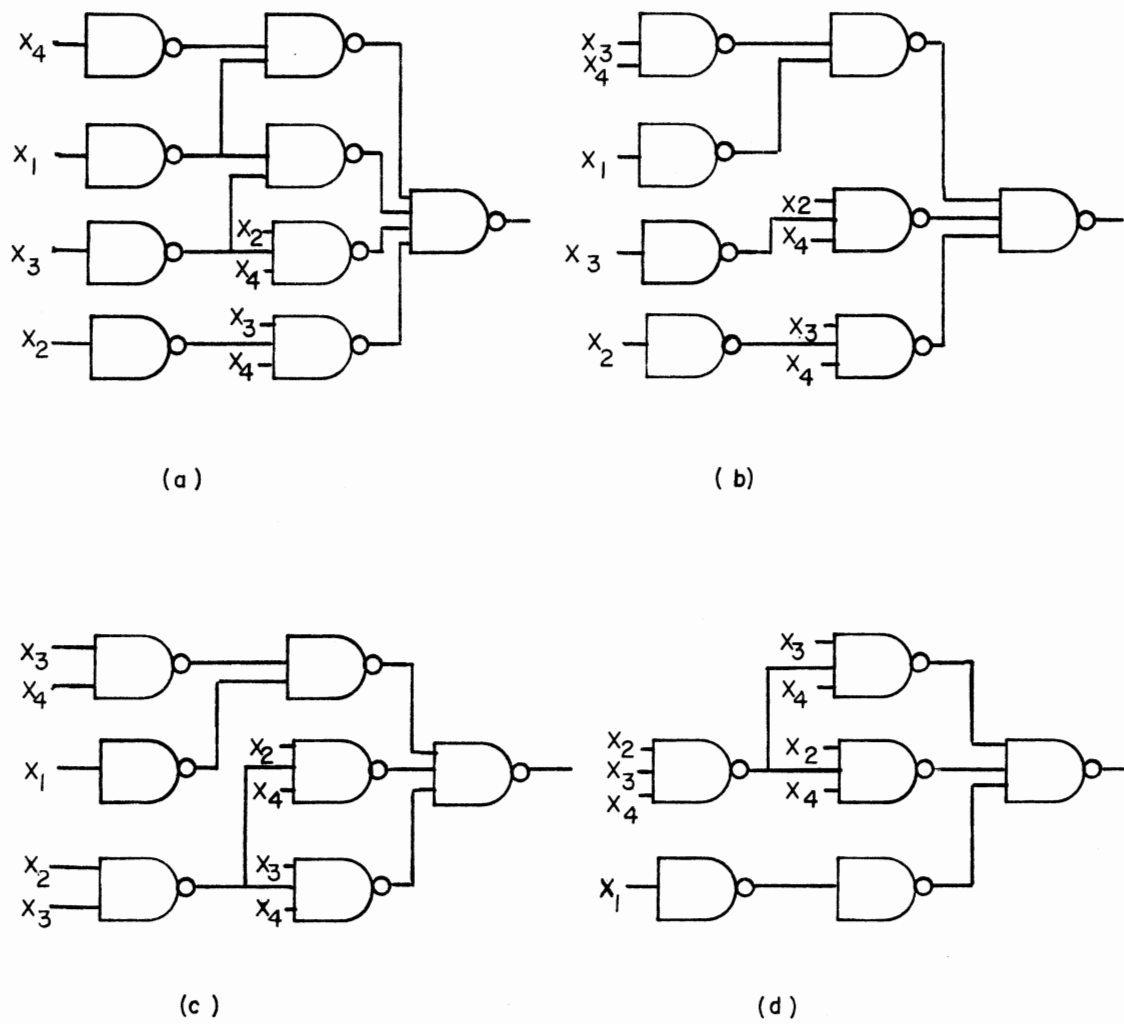


Figure 1. Example NAND Gate Circuit Improvements

solution is found, consider the function

$$F(x_1, x_2, x_3, x_4) = \sum m(0, 2, 3, 4, 5, 6, 11, 13). \quad (1)$$

The solution corresponding to the optimal AND/OR network is

$$F(x_1, x_2, x_3, x_4) = \bar{x}_1\bar{x}_3 + \bar{x}_2x_3x_4 + x_2\bar{x}_3x_4 + \bar{x}_1\bar{x}_4 \quad (2)$$

which is shown as a circuit using NAND gates in Figure 1(a). Note that single input NAND gates are used as inverters to get the complemented inputs. This realization has 9 gates and 18 inputs to those gates.

Now using the first and fourth terms of the right-hand side of (2) we see that

$$\bar{x}_1\bar{x}_3 + \bar{x}_1\bar{x}_4 = \bar{x}_1(\bar{x}_3 + \bar{x}_4), \quad (3)$$

and substituting (3) into (2) the result is

$$F(x_1, x_2, x_3, x_4) = \bar{x}_1(\bar{x}_3 + \bar{x}_4) + \bar{x}_2x_3x_4 + x_2\bar{x}_3x_4. \quad (4)$$

This realization is shown in Figure 1 (b). It has only 8 gates and 16 inputs. Further reduction is seen by ORing zero to the second and third terms of (4), i.e.,

$$\begin{aligned} \bar{x}_2x_3x_4 + x_2\bar{x}_3x_4 &= \bar{x}_2x_3x_4 + \bar{x}_2x_2x_4 + x_2\bar{x}_3x_4 + x_3\bar{x}_3x_4 \\ &= (\bar{x}_2 + \bar{x}_3)(x_2x_4 + x_3x_4) \\ &= (\overline{x_2x_3})(x_2x_4 + x_3x_4). \end{aligned} \quad (5)$$

Now substituting (5) into (4) yields

$$F(x_1, x_2, x_3, x_4) = \bar{x}_1(\bar{x}_3 + \bar{x}_4) + (\overline{x_2x_3})(x_2x_4 + x_3x_4) \quad (6)$$

which is shown as a NAND circuit in Figure 1(c). This circuit has only 7

gates but still 16 inputs. With some more manipulations, the result is

$$F(x_1, x_2, x_3, x_4) = (\overline{x_2 x_3 x_4})(x_3 x_4 + x_2 x_4 + \overline{x_1}) \quad (7)$$

and this result is shown in Figure 1 (d). This is the optimal TANT network for this problem with only 6 gates and 15 inputs. This is the same solution as found by Torng (15) on page 125 by using his level-reduction and gate-reduction technique. Also, this is the solution found using the algorithm developed later in this thesis. This example demonstrates the straightforward initial solution using double-complement method and that the result was not the optimal TANT circuit. With some algebraic manipulations, the optimal solution was found and matched the result using level-reduction gate-reduction technique's solution. This same example will be treated in detail using this thesis' algorithm in the next chapter.

Problem Formulation and Approach

The problem to be investigated in this thesis is the TANT problem in conjunction with memory. The combinational portion of the problem uses three-level NAND-gate circuits with only true externally supplied inputs and both true and complemented inputs available from the memory devices. Also, the combinational portion must cover multiple output cases. The memory, or sequential, portion simply tries different flip-flops and solves the related combinational problem. This combined effort of both the combinational and sequential problem does not appear in the literature.

The algorithm was initially programmed to simply solve the TANT problem with true inputs only. The program was then exercised with many

large examples with a spinoff effort to decide whether minimum gate was a prerequisite for a circuit to have minimum inputs. The program was then exercised with different implementations of arbitrary steps to determine the best on the basis of computer time, core storage requirements, and ease to user. Finally, the TANT synthesis algorithm was matched with the flip-flop selection and implemented as a computer-aided design package.

Thesis Outline

Following this introductory chapter, the TANT synthesis algorithm is rigorously developed and described in detail in Chapter II. The CAD package for the TANT problem, along with several large examples, is presented in Chapter III. Chapter IV describes the sequential problem, along with presenting a key example. Discussion of extensions, improvements, and conclusions are presented in Chapter V.

CHAPTER II

SYNTHESIS OF OPTIMAL TANT NETWORKS

This chapter presents and proves the optimality of an algorithm to solve the TANT problem. A firm theoretical basis is presented in the form of theorems and rigorous proofs, followed by a detailed discussion of the synthesis algorithm. The underlying concept was first worked on by Layton (23) beginning in 1973. The early concepts have been formalized in the form of theorems and some of his third-level gate selections have been modified to allow a form of backtracking. Also, a very extensive gate and input reduction scheme has been added onto the end of the algorithm. One of his examples is used, while two new examples have been added to demonstrate the improvements.

Basic Theorems

This section presents fundamental theorems to be used as a basis for the TANT network synthesis procedure. Notationally, the first-level gate is defined as the gate from which the output is obtained. Second-level gates feed first-level gates and third-level gates feed second-level gates. Additionally, no feedback is allowed whereby lower-level gates feed higher-level gates. Theorems 1 through 4 provide for second-level and third-level gate candidate generation. The completeness of an iterative procedure based on these first four theorems is guaranteed by Theorem 5. Theorems 6 and 7 describe a necessary selection of certain

second-level gate candidates for the optimal network. A key network reduction is indicated by Theorem 8, and Theorems 9 and 10 minimize gate inputs. Finally, Theorem 11 shows that an optimal TANT network is obtained.

Theorem 1

Each 1-set containing the primary cube is a candidate for a second-level gate in a three-level NAND network having only true inputs.

Proof:

Let $F(x_1, x_2, \dots, x_n)$ be some Boolean switching function with n inputs defined as

$$F(x_1, x_2, \dots, x_n) = Q + \sum_{j=1}^m S_j \quad (8)$$

where m is the number of 1-set terms containing only true inputs, S_j is the product of true inputs for the j^{th} 1-set, and Q is some function covering the remaining 1-sets. Using the standard involution theorem (2) gives

$$F(x_1, x_2, \dots, x_n) = \overline{\overline{Q + \sum_{j=1}^m S_j}} \quad (9)$$

Applying De Morgan's Theorem (2) yields

$$F(x_1, x_2, \dots, x_n) = \overline{Q} \cdot \prod_{j=1}^m \overline{S_j} \quad (10)$$

which can be recognized as a two-level NAND network with S_j as inputs to the j^{th} gate at the second level. Moreover, the m outputs from these second-level gates and \overline{Q} are inputs to the first level.

The primary cube (22) is the 0-cube having the set of coordinates (111...1), i.e., all of the true inputs. Thus, any N-cube with only true inputs must contain the primary cube.

Theorem 2

Each 0-set containing the primary cube is a candidate for a third-level gate in a TANT network.

Proof:

Let $F(x_1, x_2, \dots, x_n)$ be defined as

$$F(x_1, x_2, \dots, x_n) = R \cdot \prod_{i=1}^{\ell} \left[\sum_{k=1}^{p_i} \bar{x}_{\xi_k} \right] \quad (11)$$

where there are ℓ 0-sets composed of the sums of p_i complemented inputs, \bar{x}_{ξ_k} denotes the k^{th} complemented input in the i^{th} sum, and R is some function covering the remaining 0-sets. For example, one such function might be $(\bar{x}_1 + x_2) (\bar{x}_1 + \bar{x}_3) (\bar{x}_2 + \bar{x}_3 + \bar{x}_4) \bar{x}_5$, where $R = \bar{x}_1 + x_2$.

Invoking involution and De Morgan's theorems gives

$$F(x_1, x_2, \dots, x_n) = R \cdot \prod_{i=1}^{\ell} \left[\sum_{k=1}^{p_i} \bar{x}_{\xi_k} \right] \quad (12)$$

$$F(x_1, x_2, \dots, x_n) = R \cdot \prod_{i=1}^{\ell} \left[\prod_{k=1}^{p_i} x_{\xi_k} \right] \quad (13)$$

Therefore, the inputs to the third-level gates are the p_i true inputs.

Theorem 3

For a three-level NAND network, the input combinations to a third-level gate place "don't cares" in the 1-sets being considered as

candidates for second-level gates.

Proof:

Let the input set to the combinational network be represented by*

$$T_{3rd} = \sum_{i=1}^{2^n} t_i \quad (14)$$

where n is the number of input variables, t_i is the i^{th} combination of the input variables, and Σ denotes the logical sum of the t_i . The k applied input combinations which yield a "1" and $2^n - k$ which yield a "0" at the output of the third-level gate may be expressed as

$$T_{3rd} = \sum_{i=1}^k t_i + \sum_{i=k+1}^{2^n} t_i \quad (15)$$

Since the output of this third-level gate can be an input to the second level, the total number of inputs to the second level is $n+1$. The resulting 2^{n+1} combinations of inputs to the second level may be expressed as

$$T_{2nd} = \sum_{i=1}^{2^{n+1}} t_i \quad (16)$$

With Z_{3rd} as the output of the third-level gate,

$$T_{2nd} = \bar{Z}_{3rd} \cdot T_{3rd} + Z_{3rd} \cdot T_{3rd} \quad (17)$$

*The summation upper limit 2^n indicates only that there are 2^n distinct values which i can assume over the entire summation. No relation between the binary value of the particular input t_i and i is implied.

Substituting (8) into (10) and simplifying yields

$$T_{2nd} = \bar{Z}_{3rd} \sum_{i=1}^k t_i + \bar{Z}_{3rd} \sum_{i=k+1}^{2^n} t_i$$

$$+ Z_{3rd} \sum_{i=1}^k t_i + Z_{3rd} \sum_{i=k+1}^{2^n} t_i$$
(18)

Observe that \bar{Z}_{3rd} is zero for the $\sum_{i=1}^k t_i$ input combinations and Z_{3rd} is zero for the $\sum_{i=k+1}^{2^n} t_i$ input combinations. Therefore, the inputs corresponding to the first and fourth terms in (18) are never applied and may be considered as "don't cares" for any second-level gate into which Z_{3rd} feeds.

Theorem 4

If some second-level gate candidates in a three-level NAND network have been determined, then the corresponding 1-set input combinations may be treated as "don't cares" in the 0-sets being considered as candidates for third-level gates.

Proof:

If q members of the 1-set are covered by the second-level gate candidates already determined, then the output of the network will be "1" regardless of whether the remaining switching would result in an output of "1" or "0" for the q members of the 1-set previously covered.

Theorem 5

If a necessary third-level gate candidate is determined but discarded in favor of another candidate (or candidates), then it will be

regenerated subsequently for 0-set coverage at the third level.

Proof:

Suppose a third-level gate candidate is generated but not needed as a "don't care" (Theorem 3) for particular 1-set input combinations being considered for second-level gate candidates. Even though discarded at this stage of generation, the third-level gate candidate may be required subsequently as a "don't care" to feed a second-level gate candidate covering yet another 1-set. Therefore, to cover this other 1-set with a second-level gate, it will be necessary to regenerate the given third-level gate candidate. Furthermore, it is entirely possible that an improved third-level gate candidate having fewer inputs (and containing as a subset the previously discarded gate candidate) will be generated. In the worst case, the discarded gate candidate itself will be regenerated.

Theorem 6

The last second-level gate candidate generated must be selected for the TANT network.

Proof:

Since second-level gate candidates are generated to cover members of the 1-set (Theorem 1), each new candidate generated must cover at least one member of the 1-set not covered by candidates generated previously. The generation of these second-level gate candidates ceases when all members of the 1-set have been covered. Therefore, the last candidate generated must be selected because it covers at least one member of the 1-set not covered by any other candidate.

Theorem 7

If the first stage of generation of second-level gate candidates yields only one candidate, then that candidate must be selected for the TANT network.

Proof:

At least one member of the 1-set covered by the sole second-level gate candidate must be used as a "don't care" (Theorem 4) for the subsequent generation of one or more third-level gate candidates. By Theorem 2, the resulting third-level gate candidate(s) prevent any subsequent second-level gate candidates from covering the particular member(s) of the 1-set being used in Theorem 4.

Theorem 8

If a third-level gate candidate feeds only one second-level gate candidate as the sole input to that gate candidate, then both of these gate candidates may be discarded and the inputs to the original third-level gate candidate fed directly into the first-level gate.

Proof:

Let $F(x_1, x_2, \dots, x_n)$ be defined as

$$F(x_1, x_2, \dots, x_n) = \overline{\overline{t_{3rd}}^P} \quad (19)$$

where t_{3rd} is the input combination to the third-level gate under consideration and P is some function that covers the remainder of the members of the 1-set. Using the involution theorem yields

$$F(x_1, x_2, \dots, x_n) = \overline{t_{3rd}^P} \quad (20)$$

which corresponds to t_{3rd} being fed directly into the first-level gate.

Theorem 9

If any input x_ζ is fed to a particular third-level gate and to each of the second-level gates which that gate feeds, then x_ζ may be removed, as an unnecessary input, from the third-level gate.

Proof:

Let the switching function $F(x_1, x_2, \dots, x_n)$ be represented by

$$F(x_1, x_2, \dots, x_n) = \overline{(R_1 x_\zeta (\overline{x_\zeta x_\eta}))} \overline{(R_2 x_\zeta (\overline{x_\zeta x_\eta}))} \quad (21)$$

where x_ζ and x_η are inputs to a third-level gate which feeds two second-level gates. In addition to this input, R_1 feeds one of the second-level gates, R_2 feeds the other, and x_ζ feeds them both directly, where R_1 and R_2 are arbitrary. Using De Morgan's theorem gives

$$F(x_1, x_2, \dots, x_n) = R_1 x_\zeta (\bar{x}_\zeta + \bar{x}_\eta) + R_2 x_\zeta (\bar{x}_\zeta + \bar{x}_\eta) \quad (22)$$

which may further be expressed as

$$F(x_1, x_2, \dots, x_n) = R_1 x_\zeta \bar{x}_\zeta + R_1 x_\zeta \bar{x}_\eta + R_2 x_\zeta \bar{x}_\zeta + R_2 x_\zeta \bar{x}_\eta \quad (23)$$

Observe that the first and third terms in (23) are zero and that the remaining terms are due to the appearance of x_ζ as a direct input to the second-level gates. Therefore, the x_ζ input may be omitted from the third-level gate.

Theorem 10

To obtain an optimal network, any inputs which do not affect the output must be removed.

Proof:

If an input is present in Network A and not in Network B with all gates and other inputs being the same, then Network B obviously has fewer inputs. Provided that the two networks have identical outputs under all input conditions, Network A cannot be the optimal network.

Theorem 11

Among the networks generated by using Theorems 1 through 10, there exists an optimal network.

Proof:

Theorems 5 and 6 guarantee that all of the necessary gate candidates have been generated. Using these candidates to cover the 1-set of the desired switching function and applying Theorem 8 yields a minimum number of gates. The fewest number of inputs to these gates are determined by Theorems 9 and 10. Therefore, these exhaustive searches on covering and input reduction yield an optimal network.

The Network Synthesis Procedure

A detailed description of the TANT network synthesis procedure based upon the theorems of the previous section is presented here. A flow chart is given in Figure 2, and a detailed explanation of each step is given below.

Step 1

Determine whether the primary cube contains a "1" or a "0". If the primary cube contains a "1", then go to Step 2. If the primary cube contains a "0", go to Step 4.

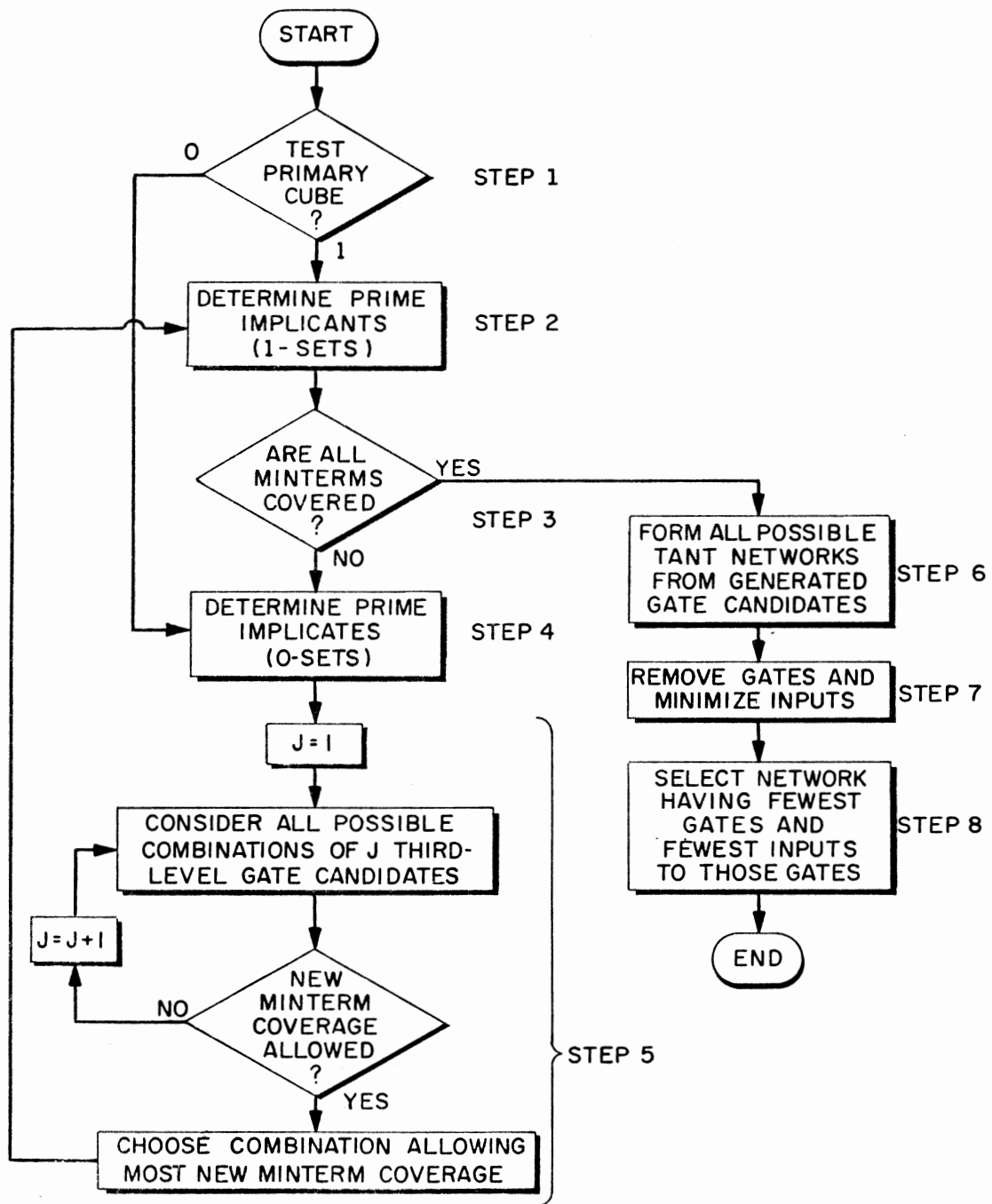


Figure 2. Flow Chart of the TANT Network Synthesis Procedure

Step 2

Determine the prime implicants (largest 1-sets) not requiring complemented inputs. This step uses Theorem 1 to generate second-level gate candidates by forming, with true inputs only, the largest groups of minterms (1-set members).*

Step 3

Test for coverage of the minterms for the desired switching function. If all of the minterms are covered, then go to Step 6; otherwise, more gate candidates must be generated, and, therefore, go to Step 4.

Step 4

Using all minterms that have been covered previously as "don't cares" by Theorem 4, determine the prime implicates (largest 0-sets) not requiring complemented inputs. Thus, by Theorem 2, third-level gate candidates are generated from the largest groups of maxterms (0-set members).

Step 5

This step determines which third-level gate candidates to retain. Test whether each gate candidate, considered singly, creates suitably placed "don't cares" (by Theorem 3) to allow additional second-level gate candidates to be generated that cover at least one minterm not

*Particularly for TANT networks having relatively few input variables, the Karnaugh map is a convenient tool for forming these largest groups by circling on the minterms in Step 2 and maxterms in Step 4. A computer program should be considered for handling networks with large numbers of input variables.

already covered. If none allow another second-level gate candidate to be generated, try all possible combinations of two, then all combinations of three, etc., until at least one new second-level gate candidate can be generated. When at least one new minterm can be covered by this procedure, select the combination of third-level gate candidates that allows the most new minterms to be covered. For example, let third-level gate candidates considered singly or in combinations of two permit no new second-level gate generation. Furthermore, suppose two groups of these third-level gate candidates considered in combinations of three do allow new second-level gate generations. Therefore, the group consisting of a combination of three third-level gate candidates which yields the second level gate candidate(s) covering the most new minterms retained. By Theorem 5, the discarded combination, if needed for the optimal network, will be generated subsequently. Consider all the implicants covered by these third-level gate candidates to be "don't cares" for subsequent gate candidate generation. Return to Step 2.

Step 6

Create all possible networks that cover the desired switching function by using the second-level and third-level gate candidates generated. Use Theorems 6 and 7, and then form a covering and closure table.

Step 7

Use Theorem 8 to eliminate third-level gates which solely feed second-level gates by feeding the third-level gate inputs directly to the first-level gate. Use Theorems 9 and 10 to eliminate the unnecessary inputs for the remaining second-level and third-level gates.

Step 8

Determine from among the several resulting networks the one(s) having a minimum number of gates and a minimum number of inputs to those gates. By Theorem 11, an optimal network is guaranteed.

The optimality of the resulting TANT network is based upon the procedure's adherence to the theorems of the previous section. Although more efficient steps might possibly be appropriate in selected cases, the synthesis procedure presented here does yield an optimal TANT network. Specifically, the discarding of third-level gate candidates in Step 5 may be avoided by a parallel storage and the subsequent consideration of all possible candidates. The particular selections in this step of the procedure yield an effective solution without unduly large amounts of storage. The directness of this procedure is demonstrated in the following examples.

Examples

Three examples are presented in this section to illustrate the developed network synthesis procedure. The first example appeared in the introduction and is included here for comparison as well as a detailed explanation of the steps of the present algorithm. Example 2 demonstrates the regeneration principle of Step 5 (Theorem 5) and gate selection procedures of Step 6, and Example 3 shows the details of input reduction in Step 7 (Theorems 9 and 10).

Example 1

It is required that an optimal TANT network be designed to realize the combinational switching function given by

$$F(x_1, x_2, x_3, x_4) = \sum m(0, 1, 2, 3, 4, 5, 6, 11, 13) \quad (24)$$

The minterms in (24) are indicated by 1's in the Karnaugh map of Figure 3(a), and 0's are shown in all other map locations. In Step 1 of the synthesis procedure, the primary cube contains a 0, which directs the algorithm to Step 4. Two prime implicants are identified and labeled as T_1 and T_2 in Step 4. In Step 5, results are shown in Figures 3(b) and 3(c) for T_1 and T_2 , respectively, by replacing the appropriate 0's by d's, allowing the tentative formation of prime implicants. Since the new 1-set coverage for the prime implicants obtained by using T_1 is greater than T_2 , only T_1 is retained. Proceeding to Step 2, the two prime implicants of Figure 3(b) become second-level gate candidates and are labeled S_1 and S_2 . In Step 3, Minterms 0, 1, 2, 4, and 6 are not yet covered, and the procedure returns to Step 4. Additional "don't cares" (d's) due to S_1 and S_2 are shown in Figure 3(d), along with the d's due to T_1 determined earlier. The prime implicate labeled T_3 covers the remaining five 0's (Step 4). Since only one prime implicate is generated, proceed past Step 5 directly to Step 2. Replacing the entries in T_3 by d's in Figure 3(e) yields the second-level gate candidate labeled S_3 , which is composed of the entire map. Since all minterms are covered (Step 3), proceed to Step 6 to form possible TANT networks. In the second-level, S_3 must be selected, since it was the last second-level gate candidate. Minterms 0 through 6 are covered by S_3 , as indicated by checks (✓) in Figure 3(a). Third-level gates whose outputs feed into the NAND-gate with output S_3 have outputs T_1 and T_3 . T_3 covers Maxterms 8, 9, 10, 12, 14, and 15. Maxterms 7 and 15 are covered by T_1 . Additional second-level gates are needed to cover Minterms 11 and 13. The gate candidate with output S_1 covers Minterms 3 and 11, and

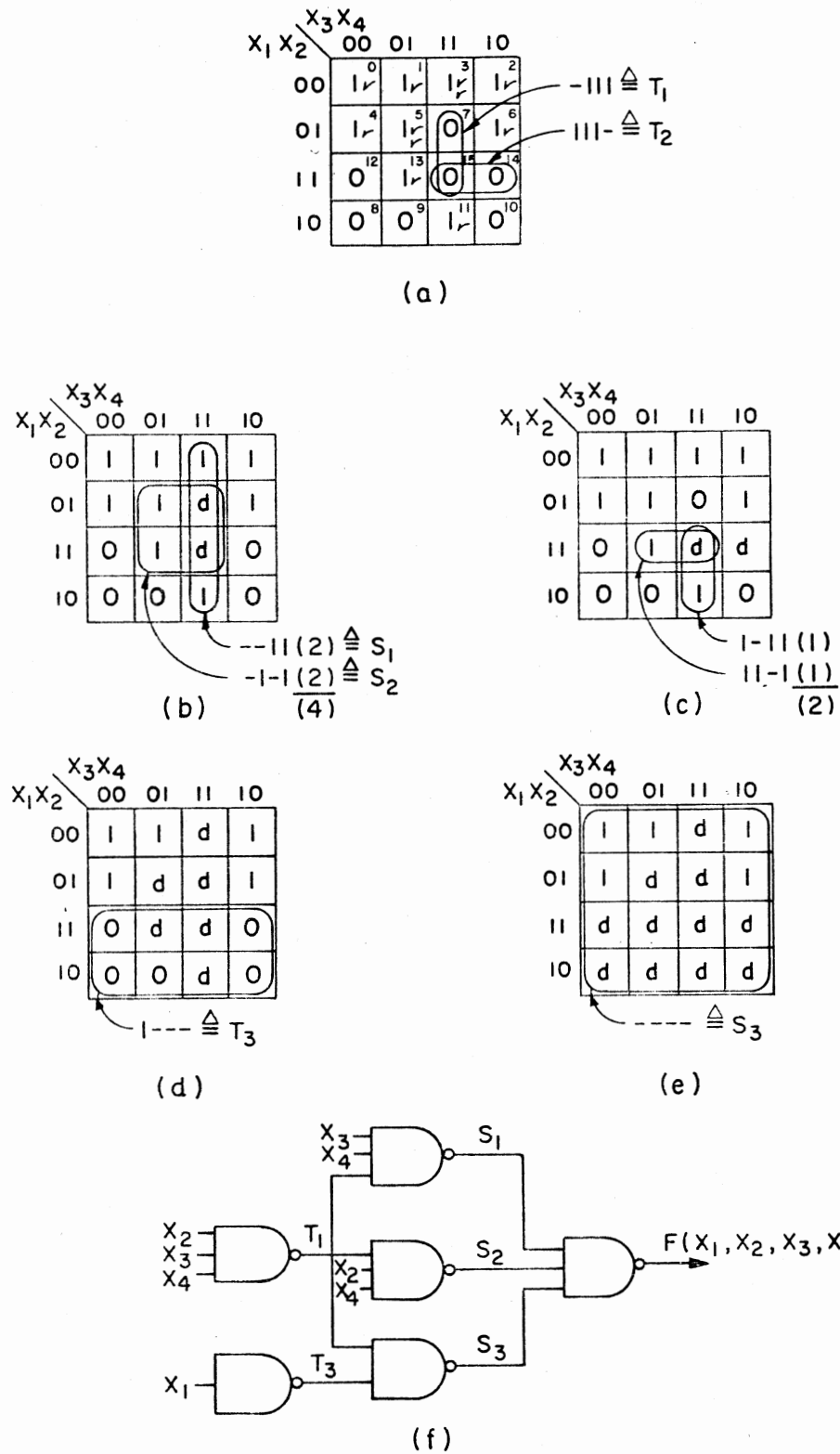


Figure 3. Design Steps and Optimal TANT Network for Example 1

the gate candidate with output S_2 covers Minterms 5 and 13. Both of these gate candidates require T_1 as an input to cover Maxterms 7 and 15. Input variables needed for these second-level and third-level gate candidates are identified in the expressions for S_1 , S_2 , S_3 , T_1 , and T_3 in Figures 3(a), 3(b), 3(d), and 3(e). No other possible TANT networks covering the desired minterms can be formed from these gate candidates. Furthermore, no gate or input reduction (Step 7) is possible. Therefore, the combinational switching circuit shown in Figure 3(f) is the optimal TANT network (Step 8).

This example was worked by Torng (15) using Eisenberg's method (14) as Example 8.5 on Pages 118 through 125. The result in Figure 3(f) is identical to Torng's switching circuit realization in Figure 8.20 on Page 125 of (15), which was obtained after applying a level-reduction technique to the primitive realization.

Example 2

As a second example, consider the switching function given by

$$F(x_1, x_2, x_3, x_4) = \sum m(0, 1, 2, 6, 7, 8, 11, 12, 14) \quad (25)$$

which is indicated on the Karnaugh map of Figure 4(a). Step 1 directs the algorithm to Step 4, where the single prime implicate T_1 is formed. Passing through Step 5 to Step 2 yields the three prime implicants S_1 , S_2 , and S_3 in Figure 4(b). Since not all minterms have been covered (Step 3), return to Step 4. The four prime implicants T_2 , T_3 , T_4 , and T_5 are formed in Figure 4(c). None of these prime implicants considered singly allows new minterm coverage in Step 5. Taken two at a time, T_3 with T_4 allows Minterm 8 to be covered and T_2 with T_3 allows Minterm 2

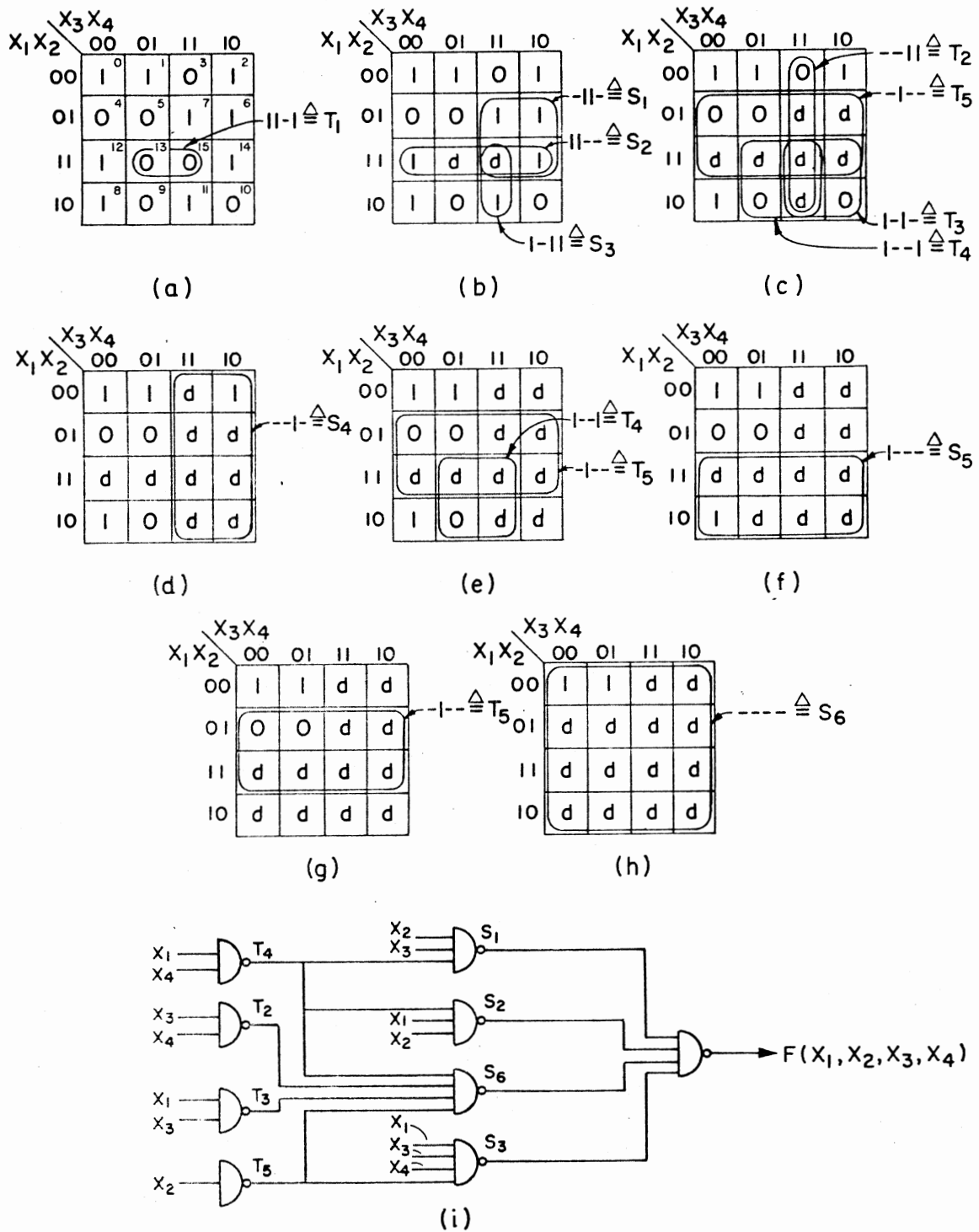


Figure 4. Design Steps and Optimal TANT Network for Example 2

to covered. Arbitrarily choosing the T_2 and T_3 combination yields S_4 in Step 2, as shown in Figure 4(d). Again, return to Step 4. T_4 and T_5 are regenerated (Figure 4(e)), but when considered singly, only T_4 allows new minterm coverage. Returning to Step 2 yields S_5 (Figure 4(f)), which covers Minterm 8. Once again, return to Step 4. T_5 is regenerated (Figure 4(g)), allowing in Step 2 the coverage of the entire map (S_6 in Figure 4(h)). Since all minterms have now been covered (Step 3), proceed to Step 6. Select S_6 , which covers Minterms 0, 1, 2, and 8, as the last gate candidate formed. Moreover, select S_1 to cover Minterms 6, 7, and 14, S_2 to cover Minterms 12 and 14, and S_3 to cover Minterm 11. Observe that T_2 , T_3 , T_4 , and T_5 must be used as inputs to S_6 to cover all maxterms. Rather than selecting T_1 to feed S_1 , S_2 , and/or S_3 , T_4 may be used to feed S_1 and S_2 , and T_5 to feed S_3 , as shown in Figure 4(i). Alternately, S_2 may be used to cover only Minterm 12, since Minterm 14 is already covered by S_1 . If both T_3 and T_4 are used to feed S_2 , then the x_2 input to S_2 can be removed, and S_2 covers Minterms 8 and 12. Therefore, this input change yields a second optimal TANT network, in addition to the one shown in Figure 4(i).

Example 3

The purpose of this final example is to illustrate input reductions for second-level and third-level gates. Let the switching function to be realized be given by

$$F(x_1, x_2, x_3, x_4) = \sum m(0, 2, 3, 4, 5, 6, 7, 8, 10, 12, 15) \quad (26)$$

Step 1 directs the algorithm to Step 2, where S_1 is formed in Figure 5(a). Passing through Step 3, Prime Implicates T_1 and T_2 are generated in

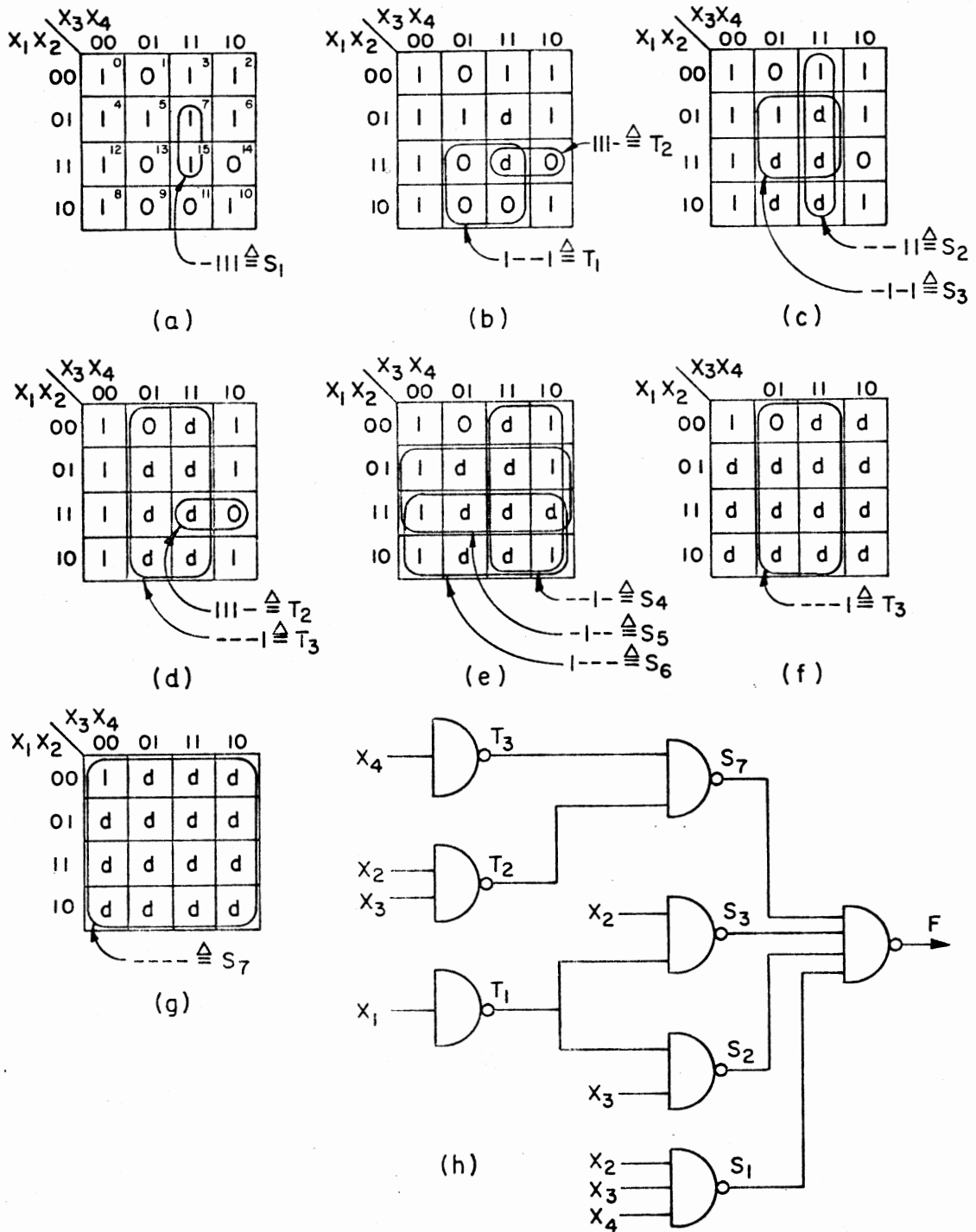


Figure 5. Design Steps and Optimal TANT Network for Example 3

Step 4 (Figure 5(b)). In Step 5, T_1 covers more new minterms, and T_2 is discarded. Returning to Step 2, S_2 and S_3 are generated (Figure 5(c)). In Step 4, T_2 and T_3 are generated, but only T_2 is retained in Step 5 (Figure 5(d)). Figure 5(e) shows the results of forming S_4 , S_5 , and S_6 in Step 2. Thereafter, T_3 is regenerated in Step 4, allowing S_7 to be formed in Step 2 (Figures 5(f) and 5(g)).

It is the application of Steps 6 and 7 in this example which requires special attention. S_7 is selected, as the last gate candidate generated, for a second-level gate to cover Minterms 0, 2, 4, 6, 8, 10, and 12. Both T_2 and T_3 are needed as inputs to this gate. In particular, T_2 covers Maxterm 14, and T_3 covers Maxterms 1, 9, 11, and 13. The sole first second-level gate candidate generated (S_1) covers Minterms 7 and 15, and no third-level gate outputs are required as added inputs to this gate. Only Minterms 3 and 5 remain to be covered at this point. Minterm 3 can be covered by using either S_2 with inputs x_3 , x_4 , and T_1 or S_4 with inputs x_3 , T_1 , and T_2 . Minterm 5 can be covered by using either S_3 with inputs x_2 , x_4 , and T_1 or S_5 with inputs x_2 , T_1 , and T_2 . Therefore, using either S_2 and S_3 or S_4 and S_5 should result in a TANT network covering all the minterms. However, if S_2 and S_3 are used, then the x_4 input to T_1 is redundant and can be removed by Theorem 9. Moreover, the x_4 input can be omitted from both the S_2 and S_3 second-level gates as shown in Figure 5(h), since Minterms 2 and 6 and Minterms 4 and 6 are included in the desired switching function (Theorem 10). Theorem 10 also allows x_1 to be removed as an input to T_2 , since Minterm 6 is now covered by both S_2 and S_3 . The resulting optimal TANT network is shown in Figure 5(h).

Summary

The theorems provided a firm groundwork for the steps in a network synthesis algorithm for the design of optimal three-level NAND-gate combinatorial switching networks having only uncomplemented inputs (TANT). A detailed description of the procedure has been provided and a flowchart included for easy reference. Three examples have been presented to demonstrate pertinent details of the algorithm. The network synthesis procedure utilizes cyclical gate candidate generation and exhaustive input optimization, which is very amenable to digital computers.

CHAPTER III

THE CAD SOFTWARE PACKAGE

This chapter discusses the computer implementation of the algorithm described in Chapter II. The first section gives a detailed description of the program and some major subroutines. The second section discusses evaluation of the CAD package. The third section of this chapter analyzes alternative methods for Step 5 of the algorithm, which is the choosing of third-level gate candidates. The fourth section describes the slight modification required for the NOR version, and the final section provides a summary.

Program Description

The program, like the algorithm, has two main parts: the part which finds the gate candidates and the part which finds and minimizes circuits using these candidates. Figure 2 (for the algorithm) and Figure 6 (for the program) differ primarily in the part on prime implicant generation. The difference allows more of the interdependence to be seen for Steps 1 through 5 in the program. This interdependence is dictated in part by the choice of a method for Step 5. This first part finds gate candidates by continuing to circle alternately on the 1-sets and 0-sets until all minterms are covered. The second part differs in that the algorithm does all of the work in parallel; whereas, the program enters a loop. In the loop of Part II, some circuit is formed from

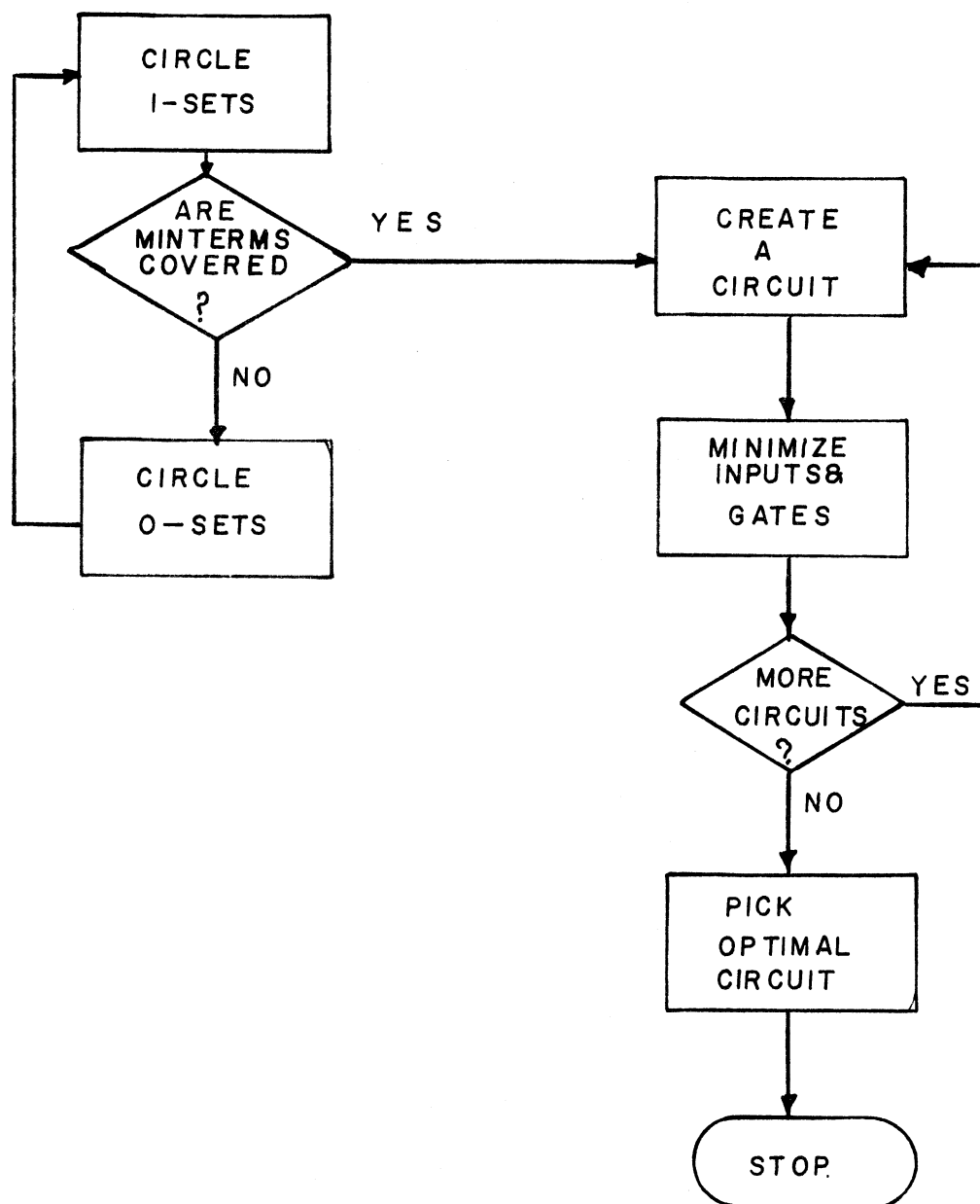


Figure 6. CAD Program Flow Chart

the candidates and then minimized, then another circuit is formed and minimized, and so forth until all possible circuits are formed and minimized. Finally, the best of these circuits is chosen as the solution.

Circling on the 1-sets (Step 2) and circling on the 0-sets (Step 4) are actually performed by the same subroutine with an input parameter indicating whether to circle on 1's or 0's. The subroutine SUBFN simply starts with the lowest minterm (maxterm), checks to determine whether it is a cell which includes the needed cube (the primary cube for TANT problems), then tests whether all members of that cell are minterms (maxterms) and, if so, that cell becomes a candidate. This subroutine is essentially finding implicants (implicates) as gate candidates. All entries within the cell are then reassigned values indicating "don't cares" for subsequent gate candidate generation. Steps 2 (circling the 1-sets), 4 (circling the 0-sets), and 5 (choosing which 0-set to discard) are all contained in a large loop, which uses minterm coverage (Step 3) to terminate the loop. Proof that these steps produce the necessary gates for an optimal network is contained in Theorems 1 through 5.

Subroutine CKFND is used to find circuits, i.e., generate different combinations of second-level gate candidates to cover the minterms. Theorem 6 states that the last candidate generated must be used. If the first second-level candidate were generated solely, it must also be used (Theorem 7). The other candidates are chosen for the circuit by a simple covering and closure table. This routine also eliminates those third-level gates solely feeding second-level gates by feeding their inputs directly into the first-level gate (Theorem 8). Subroutine CKFND corresponds to part of Steps 6 and 7.

Subroutine M3RDI eliminates from the third-level gates any inputs

that are also present in all second-level gates it feeds. This is part of Step 7 and is covered by Theorem 9. Subroutines EL2IN and EL3IN eliminate unnecessary inputs to the second- and third-level gates, respectively. This part of Step 7 uses exhaustive search. An input is removed and, if the resulting output function is unaltered, the change is made permanent; otherwise, the input is replaced. After input reduction, some gates may have identical inputs. Subroutine DUPGT finds these redundancies and eliminates them.

At the beginning of the circuit selection sequence, CKFND found a combination of second-level gates and generated a circuit. This circuit was then minimized. Now, Subroutine ALTCK modifies the feeding third-level gates in an effort to come up with an alternate circuit with the same prime implicants (second-level gate candidates), which is then minimized. ALTCK and CKFND are called until all possible circuits are found and minimized. Step 8, the choosing of the optimal circuit(s), is then executed. The Appendix contains a listing of the computer program.

CAD Evaluation

Three categories for evaluation of a CAD software package are execution time, core storage required, and user convenience. Algorithm correctness to yield an optimal network is necessary before any of these measures even has any significance. The first two categories lend themselves readily to numerical analysis, whereas the third is a rather subjective quality. This section uses tabular and graphical displays of the first two categories.

Table I shows the measurements on many problems (including several from the literature) allowing a very thorough evaluation of this

TABLE I
TIME REQUIREMENTS FOR SEVERAL TANT SOLUTIONS

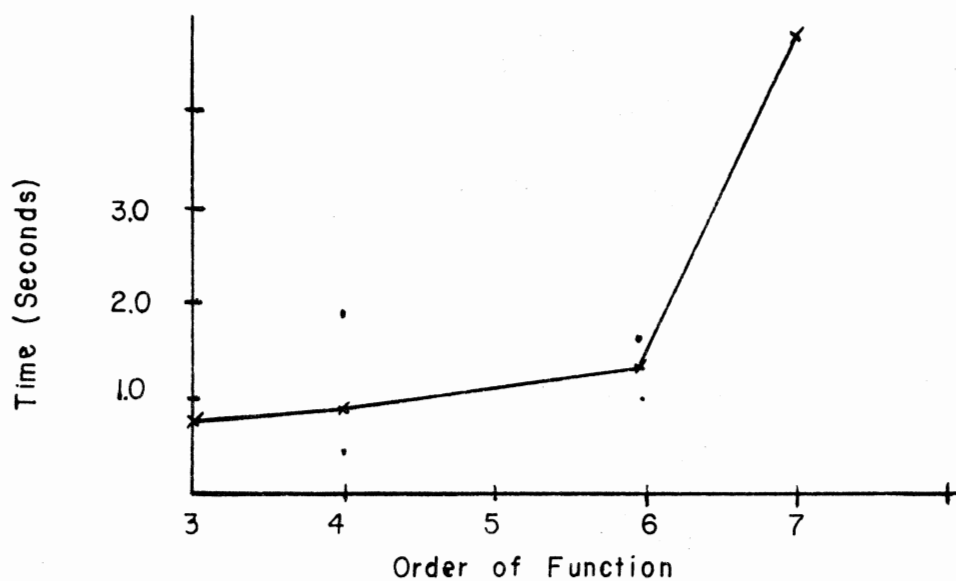
Case Number	Order	Number of Minterms	Number of Don't Cares	Execution Time (sec)	Number of Gates	Number of Inputs
1	4	11	0	1.23	8	17
2	4	9	0	0.56	6	15
3	4	9	0	1.18	9	25
4	4	11	0	0.68	6	17
5	4	1	0	0.56	6	9
6	4	8	0	1.78	8	19
7	4	1	1	0.58	6	9
8	4	3	3	0.51	5	8
9	4	3	0	0.61	7	13
10	4	7	0	0.89	6	15
11	3	5	0	0.49	3	5
12	4	7	0	0.50	5	11
13	6	20	0	1.54	9	23
14	4	7	0	0.61	7	19
15	4	6	0	0.74	6	15
16	4	7	0	0.59	6	16
17	4	7	0	0.92	7	15
18	6	10	0	1.11	8	18
19	7	15	0	3.21	8	18
20	4	6	0	0.60	7	21
21	4	9	0	1.00	8	20

package. The predominance of fourth-order problems is due both to the ease of hand analysis and to their presence in most of the literature. The timing analysis is, therefore, very accurate for the fourth-order problem, but not quite as complete for the higher-order problems. The times for the fourth-order problem range (from 0.50 seconds to 1.78 seconds. The time for the third-order problem was 0.49 seconds. The average for the fourth-order problems was 0.78 seconds. These are shown in Table I. Figure 7(a) shows a graph of the timing data. This data seems to point out a steep (perhaps exponential) rise of execution time with increased order.

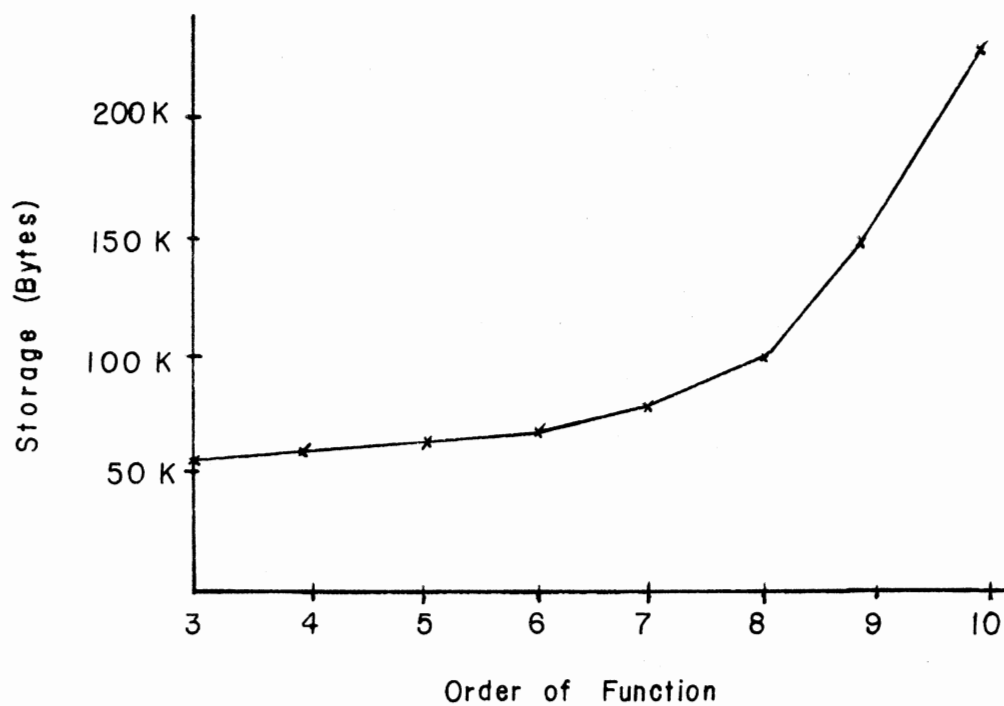
The storage analysis is shorter primarily because the number of runs to find out the required storage is one, that is one fourth-order problem will take as much storage as any other fourth-order problem. The graph in Figure 7(b) displays the storage requirements for various order problems. As one might expect, the storage requirement is relatively constant over the range of lower order problems because program statement storage predominates. As the order increases, the array storage begins to dominate and the storage requirement begins to soar. The information in this section is sufficient for a complete numerical evaluation of the CAD package.

Alternate Procedures for Choosing Prime Implicates as Third-Level Gate Candidates

The algorithm describes a Step 5 procedure which chooses an 0-set as a gate candidate based upon how many new minterms that particular 0-set allows new 1-sets to cover. This procedure is not intrinsic to the algorithm, and, consequently, other methods are possible. The



(a)



(b)

Figure 7. Timing and Storage Analysis of the CAD Program

choice could be based upon the number of 1-sets allowed to be generated, number of 0's covered, minterms in "hard" places, maxterms in "hard" places, or the first candidate which allows generation of a new 1-set.

Since the operation of circling on 0's is to allow second-level gate candidates to be generated, the method of choosing the 0-set which allows the most 1-sets has merit. The disadvantage of this method comes in the form of extra or unnecessary candidates being generated in some cases. The method of finding the most new 0's follows from the fact that 0's must be covered to allow second-level gate candidate generation. However, it is obviously not the purpose of this algorithm to cover all of the maxterms, or even as many as possible. A "hard" places criterion can be defined as those terms farthest from the primary cube. This would generate larger cells and fewer inputs to the candidates. The method chosen does not affect the optimality of the solution, as regeneration comes into play, but different methods result in faster or slower execution times. For example, the method of choosing the first 0-set allowing new minterm coverage is faster in the choosing stage but may be slower in the long run by taking more time to generate all of the second-level candidates. Saving all of the candidates and solving in parallel, thus avoiding any choices, would not only increase time requirements, because of having to solve for all possible candidates, but would increase storage space in memory.

Table II shows the execution time and storage requirements for some of the choices for Step 5. The execution times are for an ensemble of 20 problems of various orders. The storage requirement is for up to an eighth order problem. Almost immediately apparent is the very small difference in core storage requirements. This is due to the fact that

TABLE II
TIMING AND STORAGE COMPARISONS FOR METHODS
OF CHOOSING PRIME IMPLICATES

Method	Execution Time	Storage
Original Step 5	11.56	103k Bytes
Maximum 1-sets	11.60	103k Bytes
Maximum maxterms	11.85	103k Bytes
Minterms in "hard" places	10.90	104k Bytes
Maxterms in "hard" places	11.77	104k Bytes
Simplistic	8.79	100k Bytes

much of the storage requirement is due to the input and gate optimization portion of the program.

The original Step 5 chose third-level gate candidates based upon the number of new minterms allowed to be covered. The other methods are self-explanatory. All of the sophisticated methods, i.e., the original, the maximum 1-set, the maximum minterms, the maximum maxterms, minterms in hard places, and maxterms in hard places, seemed justifiable. Actually, these methods took more time and storage than the simplistic method of choosing the first 0-set or sets to allow minterm coverage to be chosen as third-level gate candidates. Regeneration of necessary gate candidates guaranteed the optimality of any of the methods. The difference of about 4K bytes between the sophisticated methods and the simplistic method was the subroutine to determine gate candidate choice. More significant, the simplistic method used only 8.79 seconds of CPU time to solve the examples, compared to 10.9 to 11.85 seconds for the sophisticated approaches.

NOR Example

This section describes how the NAND algorithm can be used to find a NOR circuit. In fact, Theorem 12 proves that any NAND circuit finding algorithm can be used to find a NOR circuit, or vice versa. The procedure is to complement the function, then complement the inputs, and solve as if solving for a NAND circuit. The resulting circuit is merely implemented using NOR gates to realize the original function. This procedure is based upon the complemented equivalency of NAND and NOR circuits as proven by Theorem 12.

Theorem 12

When every NAND gate in a circuit is replaced in that same circuit with NOR gates, the new circuit is the realization for the complement of the original switching function with complemented inputs.

Proof:

Given a switching function

$$F(x_1, x_2, x_3) = \overline{x_1 \cdot (x_2 \cdot \bar{x}_3)} \quad (27)$$

the NAND circuit can be readily recognized. Replacing the NAND gates with NOR gates yields

$$\begin{aligned} F'(x_1, x_2, x_3) &= \overline{x_1 + \overline{(x_2 + \bar{x}_3)}} \\ &= \overline{x_1 + (\bar{x}_2 \cdot x_3)} \\ &= \bar{x}_1 \cdot \overline{(\bar{x}_2 \cdot x_3)} \\ &= \bar{x}_1 \cdot (\bar{\bar{x}_2} \cdot \bar{x}_3) \end{aligned} \quad (28)$$

which is the complement of F with complemented inputs.

Example

Let the combinational function to be realized be given by

$$F(x_1, x_2, x_3, x_4) = \prod M(0, 3, 4, 7, 8, 11, 12, 13, 15). \quad (29)$$

Figure 8(a) shows the complement of this function, which is just replacing the maxterms with minterms, and vice versa. Complementing the inputs essentially moves the minterms around; e.g., 0 becomes 1 and 13 becomes 2, which is illustrated in Figure 8(b). Step 1 indicates that the

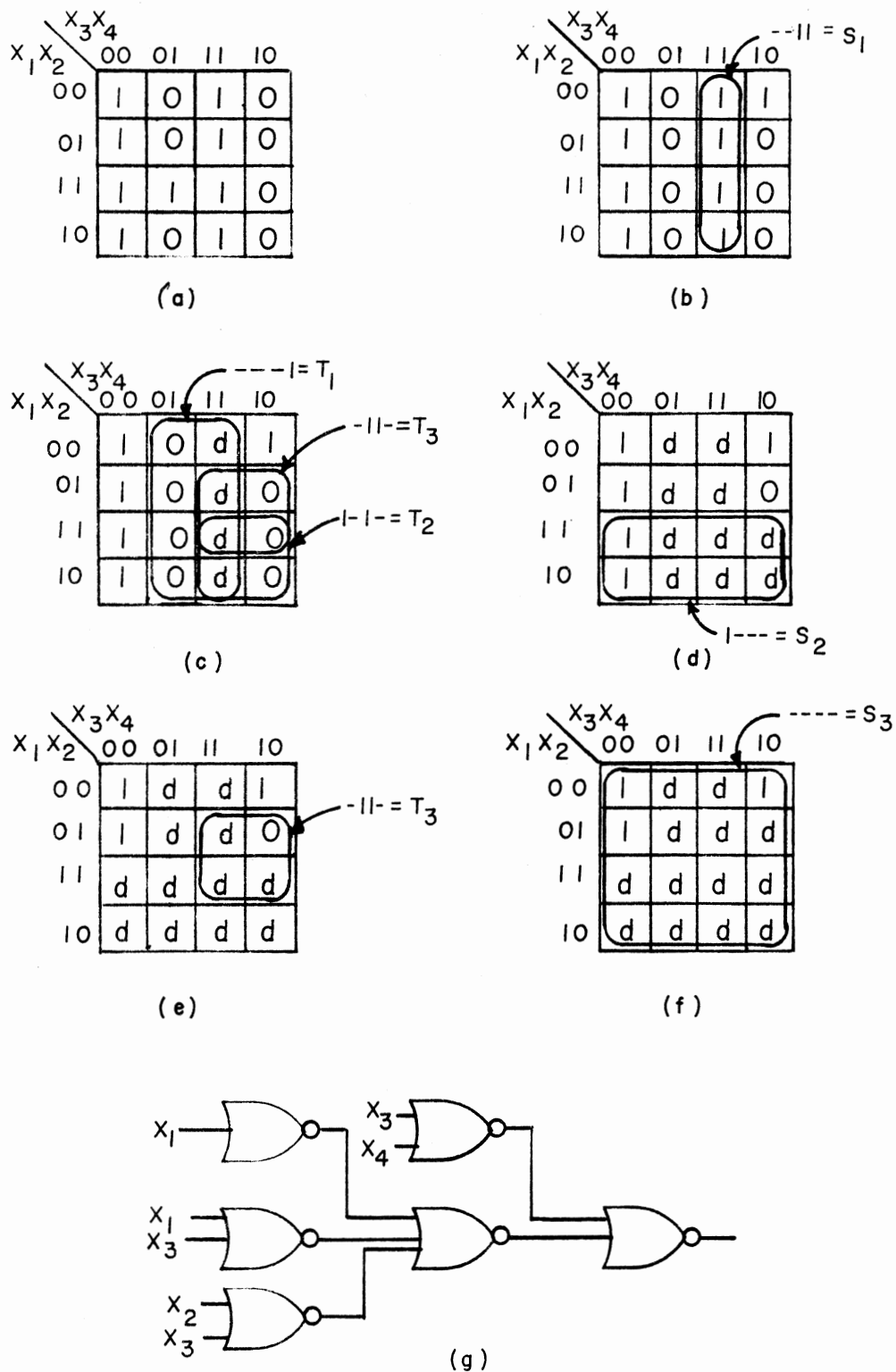


Figure 8. Design Steps and Optimal Network for NOR Example

primary cube is a 1; therefore, circling on the 1's yields S1 as shown also in Figure 8(b). Step 5 then circles on the 0's and T1 and T2 are chosen as candidates from the 0-sets generated, as shown in Figure 8(c). Returning to Step 2, S2 is generated as is shown in Figure 8(d). Figure 8(e) shows T3 which was actually regenerated by Step 5. Step 2 now generates S1 which covers the whole map and is shown in Figure 8(f). Step 3 exits the candidate-generation loop, as all of the minterms have been covered. Step 6 finds that only S1 and S3 are needed to cover all of the minterms, and that T1, T2, and T3 must feed S3. Steps 7 and 8 find no minimization or alternate circuits. The resulting NOR circuit is shown in Figure 8(g).

Summary

This chapter has described the computer implementation of the algorithm of Chapter II, and the slight differences required. A detailed description of the program and some major subroutines has been given. The CAD package has been evaluated based upon time and storage requirements. Alternative methods for choosing from among 0-sets for third-level gate candidates in Step 5 have been discussed. Finally, the adaptation to the NOR problem has been presented and proved.

CHAPTER IV

SEQUENTIAL DESIGN WITH TANT NETWORKS

This chapter describes the solution of sequential problems which use the TANT criteria for the combinational portion. The first section formulates the problem requiring sequential machines with TANT combinational logic. The second section describes the modifications required for the algorithm in Chapter II to solve the sequential problem. The third section describes the computer modifications for solving the generalized excitation table. A sequential example is given in the fourth section, and the final section provides a summary.

Problem Description

In general, a sequential problem is composed of two portions, a combinational logic circuit and some memory devices, as shown in Figure 9. The primary inputs are the $n x$'s, and the $m z$'s are the output. The j memory devices are fed by the excitation variables represented by E 's, and feedback y 's to the combinational portion. The sequential portion of the problem proceeds from the primitive flow table to the generalized excitation table. The generalized excitation table is used to start the TANT solution for the combinational portion of the problem. The sequential design portion is well documented, but the application of the TANT algorithm of Chapter II to the generalized excitation table is a new concept.

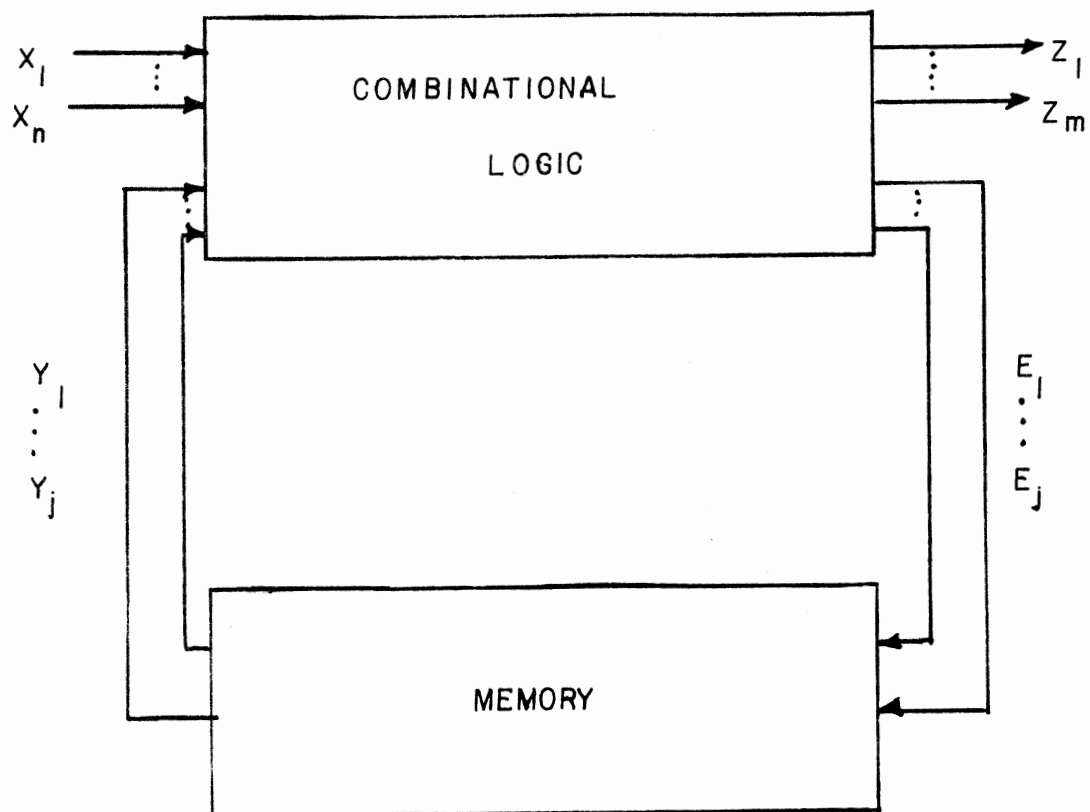


Figure 9. The General Sequential Circuit

The sequential problem begins by converting the word statement of the problem into a primitive flow table; i.e., a flow table with only one stable state per row. The next step is to use state reduction techniques to find a minimal row flow table. Next, state assignments are made and the transition table is generated. From the transition table a generalized excitation table is generated. This is a key step, in that one does not need to choose a particular type of flip-flop yet. In many design procedures the type of flip-flop is chosen at this point and excitation tables are used to produce the Boolean equations for the combinational portion of the problem. By using the generalized excitation tables, the choice of a particular flip-flop may be postponed until the optimal combinational circuit is found for each option and, thus, the overall optimal sequential machine is determined. The combinational portion of the problem proceeds as in the algorithm of Chapter II for the solving of a TANT problem.

Modifications for Sequential Applications

The basic TANT algorithm requires two modifications to be used effectively for sequential design problems. Since the state values from the memory are available in both complemented and uncomplemented form, the TANT restriction of true inputs only must be relaxed for the optimal combinational logic design problem. Secondly, the memory requires excitation values which must be supplied by the combinational portion of the circuit. These outputs, as well as the total network's output require that the TANT algorithm be capable of simultaneous optimization to provide multiple outputs. These modifications are useful as well for other applications. For example, many problems in combinational

logic require multiple outputs, and often some inputs will be available in uncomplemented form.

The presence of some uncomplemented inputs relaxes the restriction that the primary cube (111...1) be contained within every cell used as a gate input combination. The primary cube becomes a primary cell, with the requirement that every implicant or implicate used as a gate candidate must contain at least one member of the primary cell. The primary cell does contain the primary cube. The extended TANT algorithm will solve regular TANT problems, as they are a special case of the set of problems requiring a primary cell (i.e., TANT has a primary cell of dimension 1).

The multiple output case for TANT problems proceeds similar to multiple output AND/OR problems. The minterms are "tagged" to indicate for which function (outputs or excitations) the minterm is intended. As the prime implicants are generated the "tags" are carried along, and any implicant with all minterms having the same flag(s) becomes "tagged" for the same function(s) as the minterms. The final count can, thus, be minimized by using some of the same gates for two (or more) functions. The circling on the 0's need not be tagged, as any function can use any third-level gate it might need. The multiple output extension is merely a bookkeeping procedure, but does result in the overall optimal result.

The Generalized Excitation Table

An excitation table shows what the next state will be given the current state and the input, a generalized excitation table (25) shows what action will be taken when given the current state and the applied inputs. Each type of flip-flop has a unique excitation table for a

given problem. However, a generalized excitation is applicable to any flip-flop. The computer program uses the generalized excitation table to generate the excitation for each of the types of flip-flops within its library. The TANT algorithm will solve the combinational circuit for each excitation table and print the optimal result. The computer program merely uses the generalized excitation to postpone the selection of a particular flip-flop.

The entries in a generalized excitation table are: a 1, which indicates that the current state is 1 and the next state is 1; a 0, which indicates the current state is 0 and the next state is 0; a θ , which represents the transition from a current state of 1 to a next state of 0, and, finally, an I, which represents a current state of 0 and a next state of 1. Table III shows how each of these entries relates to some common flip-flop devices. Table III is essentially the library that the computer uses for converting the generalized excitation table into a list of minterms for input to the TANT algorithm.

Although there are many design steps leading to the formulation of the generalized excitation table, the table is merely the beginning point for the combinational circuit which will provide the excitation values and the outputs.

A Sequential Example

This example demonstrates the solution of a sequential problem with TANT circuitry for the combinational portion. The major emphasis will be the TANT solutions. A word statement is presented with its associated primitive flow table. The minimal row table is given without showing explicitly the row reduction. The state assignments are made and the

TABLE III
TRANSLATION OF GENERALIZED EXCITATION TABLE ENTRIES FOR
SOME COMMON TYPES OF FLIP-FLOPS

		R	S	J	K	T	D
I	$0 \rightarrow 1$	0	1	1	-	1	1
0	$1 \rightarrow 0$	1	0	-	1	1	0
1	$1 \rightarrow 1$	0	-	-	0	0	1
0	$0 \rightarrow 0$	-	0	0	-	0	-
-	-	-	-	-	-	-	-

transition table presented, which readily yields the generalized excitation table. The solution for T flip-flops is shown in detail, and some other flip-flop type solutions are presented. Finally, an optimal sequential circuit with TANT is shown in a diagram.

The desired sequential circuit is to respond to a series of input which will produce an output to trigger the release of a combination lock. The circuit is to operate in fundamental mode, have inputs of x_1 and x_2 , and produce outputs of z_1 and z_2 . To open the lock an output of $z_1 z_2 = 11$ is to occur after the $x_1 x_2$ input sequence of: 01, 00, 10, 11. The circuit is initialized to $y_1 y_2 x_1 x_2 = 0001$, and only single bit changes in the inputs will be allowed. While the correct combination is being entered the output $z_1 z_2$ shall be 10. Upon any deviation from the correct sequence the output will become 00, which will trigger external gates to bring the system back to the 0100 initial conditions.

The primitive flow table and reduced flow table are shown in Figure 10. Using the adjacency diagram of Figure 11(a) and the state assignment map of Figure 11(b), the state assignments of: $\alpha = 00$, $\beta = 01$, $\gamma = 11$, $\delta = 10$ are found. Figure 11(x) displays the transition table, and Figure 11(d) shows the generalized excitation table.

The generalized excitation table must be converted to an excitation table for a particular type of flip-flop to begin the modified TANT design. Figure 12(a) shows this conversion for T flip-flops. ET will represent the excitation inputs for T flip-flops. The tags are A for ET_1 , B for ET_2 , C for z_1 , and D for z_2 . The primary cell in this case is $y_1 y_2 x_1 x_2 = (--11)$. The "don't cares" in the output subtable are due to the unstable states. Step 1 of the algorithm from Chapter II shows 1's present in the primary cell, so proceeding to Step 2 (circling the 1-sets)

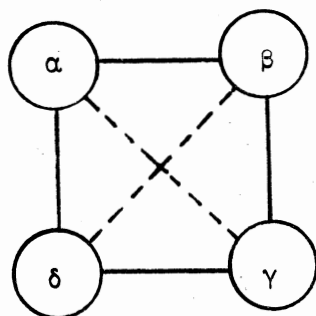
	NEXT STATE				OUTPUT $Z_1 Z_2$			
	INPUT $X_1 X_2$				INPUT $X_1 X_2$			
	00	01	11	10	00	01	11	10
A	B	(A)	G	—	10	10	-0	—
B	(B)	A	-	C	10	10	—	10
C	E	—	D	(C)	-0	—	1-	10
D	-	A	(D)	F	—	1-	11	—
E	(E)	A	—	F	00	-0	—	-0
F	E	—	G	(F)	00	—	00	00
G	—	A	(G)	F	—	-0	00	00

(a)

	NEXT STATE				OUTPUT $Z_1 Z_2$			
	INPUT $X_1 X_2$				INPUT $X_1 X_2$			
	00	01	11	10	00	01	11	10
AB α	(α)	α	δ	β	10	10	-0	10
C β	δ	—	γ	(β)	-0	—	1-	10
D γ	—	α	(γ)	δ	—	1-	11	—
EFG δ	(δ)	α	(δ)	(δ)	00	10	00	00

(b)

Figure 10. The Primitive and Reduced Flow Tables



(a)

		Y_2	
		0	1
Y_1	0	α	β
	1	δ	γ

(b)

		$X_1 X_2$			
		00	01	11	10
$Y_1 Y_2$	00	00	00	10	01
	01	11	—	11	01
	11	10	10	11	10
	10	10	00	10	10

(c)

		$X_1 X_2$			
		00	01	11	10
$Y_1 Y_2$	00	00	00	10	01
	01	11	—	11	01
	11	10	10	11	10
	10	10	00	10	10

(d)

Figure 11. Sequential Design Tables

generates $S_1 - S_4$ as shown in Figure 12(a). S_1 is tagged with D for z_2 , S_2 , and S_3 are tagged with a B, and S_4 is tagged with an A. The Step 3 test indicates that not all minterms are covered; therefore, proceed to Step 4. Figure 12(b) shows the cells generated by Step 4. T_1 allows the coverage of more new minterms; therefore, it is kept: Note that the T's need not be tagged as they are available to feed any second level gate. Step 3 indicates not all minterms are covered, and Step 4 regenerates T_2 . Step 5 passes this sole 0-set to Step 2 which generates S_9 , as in Figure 12(d). All minterms are now covered, so Step 6 is now executed. Only one possible circuit is found and no minimizations are possible. The resulting circuit with 13 gates and 33 inputs and/or interconnections is shown in Figure 13.

The input and gate counts for the combinations of flip-flops is shown in Table IV for both the TANT algorithm and the double-complement algorithm. Due to the state assignment, only 2 flip-flops are required in any of the circuits. The T,D flip-flop version (i.e., using a D flip-flop for memory device 1, and a T flip-flop for memory device 2) is shown in Figure 14. The circuit using only T's has the same number of gates as the D,T version, but more inputs. The D,T version has the interesting phenomena in that a third-level gate for one function directly feeds the first-level gate of another function. The result is that a particular gate is both a second- and a third-level gate at the same time.

This example shows (a) the TANT algorithm of Chapter II, when slightly modified, yields better (fewer gates and interconnections) sequential circuits than the double-complement method, and (b) allowing multiple types of flip-flops in the same circuit can at least result in

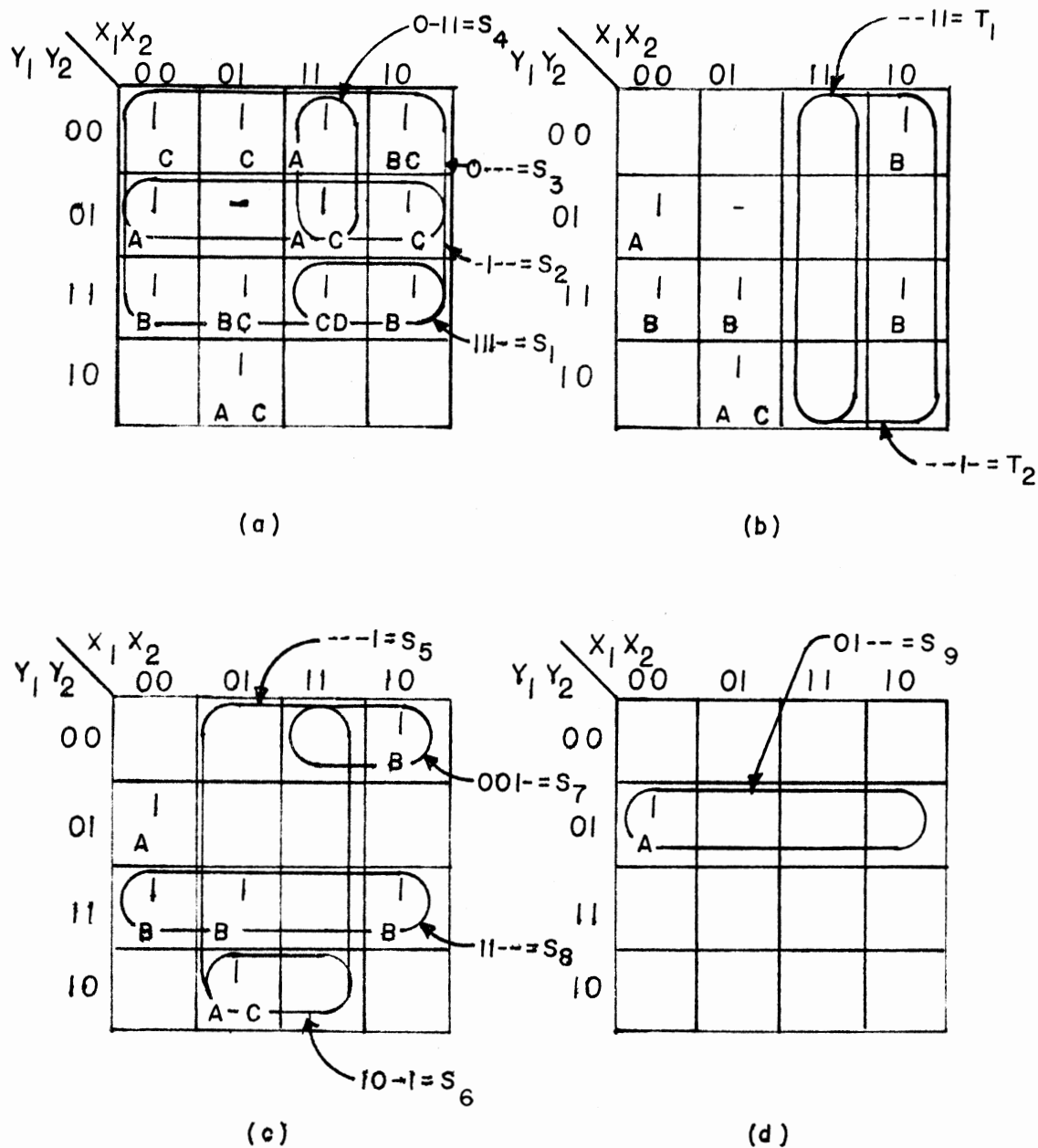


Figure 12. TANT Solution for Toggle Flip-Flops

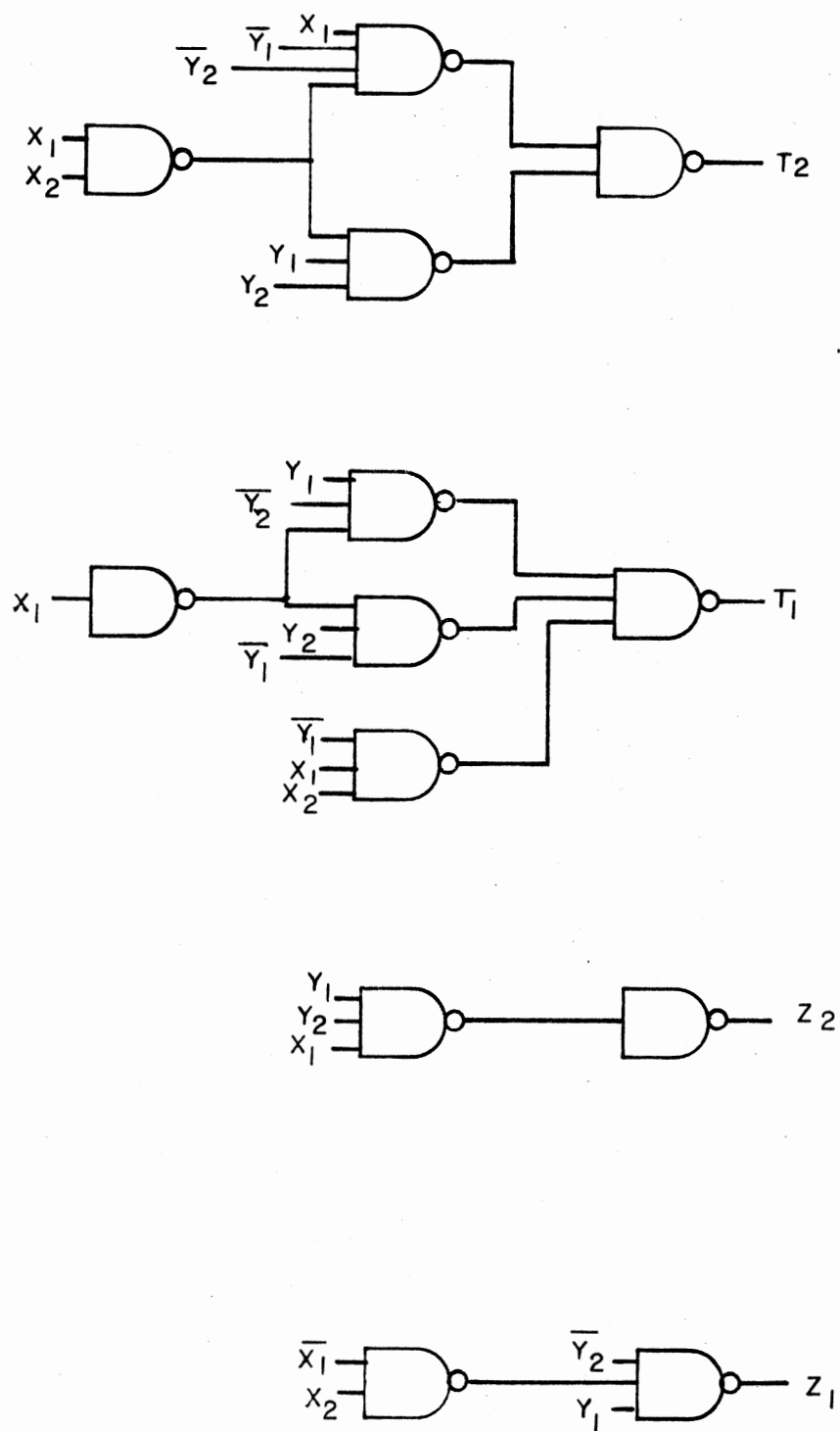


Figure 13. The Toggle-Toggle Flip-Flop Solution

TABLE IV
INPUT AND GATE COUNTS FOR SOLUTIONS TO THE
SEQUENTIAL EXAMPLE

Flip-Flop Types		Using Thesis Algorithm		Using Double-Complement	
FF1	FF2	Number of Gates	Number of Inputs	Number of Gates	Number of Inputs
T	T	13	33	14	37
D	D	14	31	14	31
RS	RS	14	28	16	31
JK	JK	14	28	16	31
T	D	14	35	14	35
T	RS	14	33	15	34
T	JK	14	33	15	34
D	T	13	29	14	32
D	RS	14	29	15	30
D	JK	14	29	15	30
RS	T	13	30	15	34
RS	D	14	31	15	32
RS	JK	14	28	16	31
JK	T	13	30	15	34
JK	D	14	31	15	32
JK	RS	14	28	16	31

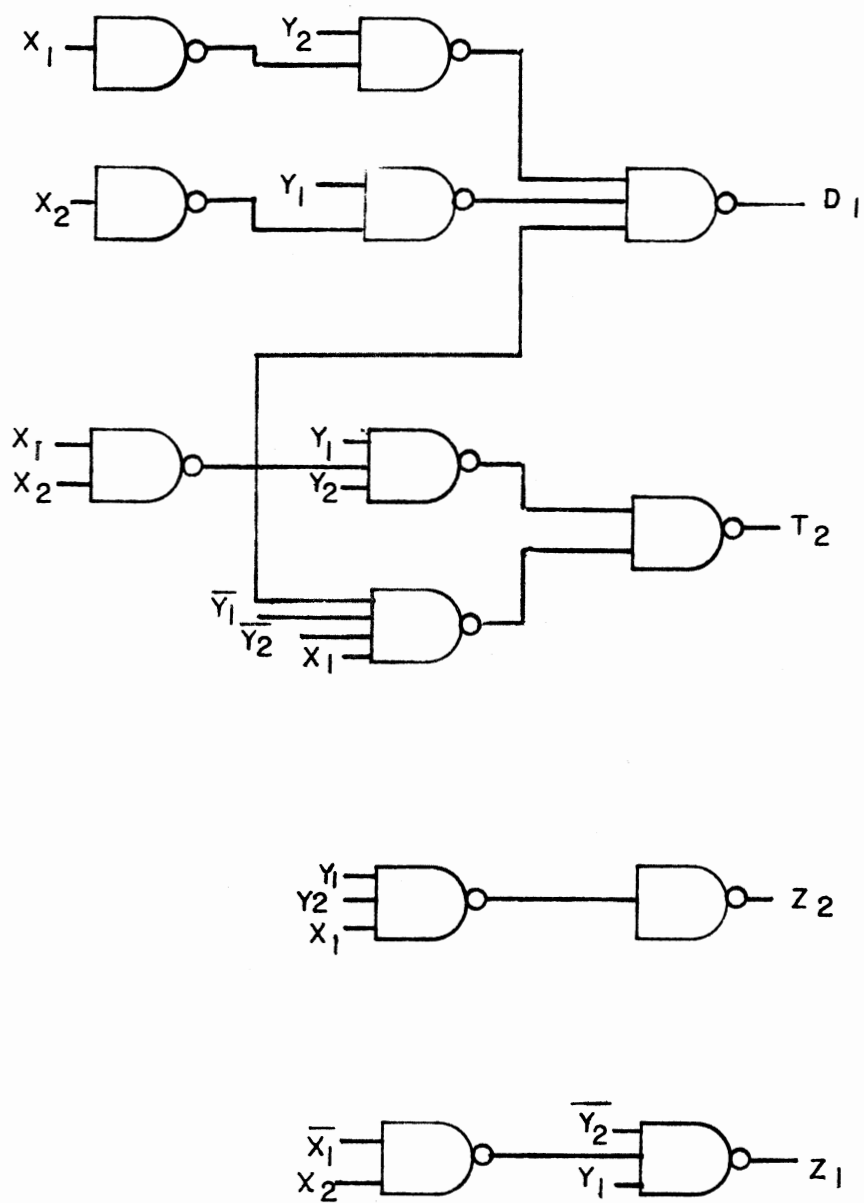


Figure 14. The Toggle-Delay Flip-Flop Solution

fewer interconnections.

Summary

This chapter described the general problem for sequential design with NAND gate combinational logic, and only true external inputs available. The modifications for the algorithm of Chapter II to handle the special requirements of primary cell and multiple output were described. The use of the generalized excitation table as the starting point for the computer program was presented. Finally, an example with detailed explanation for some cases was presented.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

This thesis applied a new map-factoring type of algorithm to the solution of three-level NAND-gate problems with only uncomplemented inputs allowed. A set of theorems proved the optimality of the solution found by the basic algorithm. The theorems formed a constructive proof, and the steps of the procedure for the algorithm followed the theorems closely. Expansion of the basic algorithm allowed solutions to problems with sequential applications.

Conclusions

Third-level and second-level gates correspond to prime implicants and prime implicants, respectively. Not all of the prime implicants for a given function are required for the minimum realization of that function. These points with some input reduction allow the generation of an optimal circuit realization without using an exhaustive search on all possible combinations of gates. The procedure is readily implemented on a computer. While the algorithm considered many situations in parallel, the computer, being essentially a sequential machine, required that many steps be converted to loops. The NOR problem is easily handled by the algorithm due to the complemented function with complemented inputs relationship between NAND and NOR gates. The overall procedure produces an optimal result independent of the particular method of implementation of

some of the steps, particularly the choice of prime implicants for third-level gate candidates.

The basic TANT problem is a subset of combinational problems which allow some complemented inputs. The extension of the basic algorithm to solve problems with some complemented inputs involved expanding the primary 1-cube concept to a primary r-cube. Multiple outputs are required in many combinational problems. The multiple output procedure entailed the tagging of minterms and generated prime implicants. The extensions of some uncomplemented inputs and multiple outputs allows sequential problems to be solved.

Recommendations

The creation of hazardless networks being a desirable goal, the investigation of covering minterms more than once by adding selected gates to the optimal circuit is suggested. Work on fault analysis is suggested to both determine a circuit's sensitivity to a particular fault as well as fault detection and correction. One possible approach to this problem is the generation of input test sequences, i.e., a series of inputs with known expected outputs which yields the most information with the least effort. Further investigation of fan-in and fan-out restrictions would increase the applicability of the algorithm to common design problems. A concentrated effort is needed to create a sequential CAD package to utilize fully the TANT algorithm in sequential applications.

The generality of the concept behind the algorithm could be investigated by considering more complex units than NAND gates as the basic building blocks. The basic objective is to search for an optimal circuit

without total exhaustive search upon the set of all possible circuits.

This concept could be used for NAND-trees, minimizing package counts in microprocessor circuits, of a general method of attack on logic circuits.

Since much of today's logic is implemented in software, the use of this algorithm to minimize programming steps in microprocessors should be investigated.

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APPENDIX

COMPUTER PROGRAM LISTING

M A I N .

VARIABLES:

IN-LOGICAL UNIT NUMBER FOR THE INPUT DEVICE.
 ICUT-LOGICAL UNIT NUMBER FOR OUTPUT DEVICE.
 LPI-LEVEL PLUS 1.
 LMI-LEVEL MINUS 1.
 NCTST- ARRAY OF VALUES FOR TESTING CRITERIA
 FOR STEP 5 CHOICES OF PRIME IMPLICATES.
 JCRT- INDEX FOR TYPE OF STEP 5 BEING USED:
 =1 MOST 1-SETS GENERATED.
 =2 MOST NEW MINTERMS COVERED.
 =3 MOST NEW MAXTERMS COVERED.
 =4 FIRST 0-SET GENERATED ALLOWING NEW MINTERM
 COVERAGE.
 =5 MAXTERMS IN HARD PLACES COVERED.
 =6 MINTERMS IN HARD PLACES COVERED.
 NITMP-NUMBER OF NEW SUBFUNCTIONS(TEMPORARY).
 ITTMP-NEW SUBFUNCTIONS(TEMPORARY).
 JPA,JMA2-LOOP INDEXING VARIABLES.

 IPRIM-THE PRIMARY CUBE.
 NCTRM-NUMBER OF MINTERMS INPUT.
 ICRDR-ORDER OF FUNCTION TO BE MINIMIZED.
 NDC -NUMBER OF DONT CARES READ IN.
 ISET-TYPE OF SET TO BE PROCESSED(1-SET OR 0-SET).
 MCELL-NUMBER OF MAXTERM CELLS FOUND.
 MCELL-LIST OF MAXTERM CELLS FOUND.
 MXTM-LIST OF MAXTERMS.
 MTRMS-LIST OF MINTERMS.
 ICUBE-0-SET CUBES NOW BEING CONSIDERED.
 NSTCF-NUMBER OF 0-SET CUBES NOW BEING CONSIDERED.
 NCMX-NUMBER OF MAXTERMS.
 NTMP-PARTICULAR 0-SET CUBE NOW BEING CONSIDERED.
 IS-LIST OF SUBFUNCTIONS.
 NCSF-NUMBER OF SUBFUNCTIONS.
 IT-LIST OF RESIDUAL FUNCTIONS.
 ACTF-NUMBER OF RESIDUAL FUNCTIONS.
 IFUNC-FUNCTION VALUE AT VARIOUS LEVELS OF SOLUTION.
 LEVEL-CURRENT LEVEL OF FUNCTION.
 ICCV-COVERING TABLE WHERE ROW IS SUBFUNCTION AND COLUMN IS MINTERM
 NEPI-S-NUMBER OF ESSENTIAL PI'S.
 IEPI-S-LIST OF ESSENTIAL PI'S.
 IFST-FIRST LEVEL DIRECT INPUT CUBE MINIMUM.
 NCKT-NUMBER OF CIRCUITS.
 NGATS-NUMBER OF GATES FOR A CIRCUIT.
 NINPT-NUMBER OF INPUTS FOR A CIRCUIT.
 ISWIC-SWITCH FOR DEBUG PRINT, IF ON(= TO IDBUG) THEN PRINT ALL
 DEBUG PRINTS.
 IPRT-LOGICAL UNIT NUMBER FOR LINE PRINTER.
 ICBG-TEST VALUE FOR DEBUG SWITCH.
 IDUM-LOGICAL UNIT NUMBER FOR NOWHERE.

VARIABLES INDEXING KEYS:

IT(JQ,1)=THE MINIMUM OF THE INPUT CELL FOR THE JQTH 0-SET.
 IS(JR,1)=THE MINIMUM OF THE INPUT CELL FOR THE JRTH 1-SET.
 IS(JR,2)=THE # OF IT'S BEFORE THE JRTH 1-SET.

00000010
 00000020
 00000030
 00000040
 00000050
 00000060
 00000070
 00000080
 00000090
 00000100
 00000101
 00000102
 00000103
 00000104
 00000105
 00000106
 00000107
 00000108
 00000109
 00000110
 00000120
 00000130
 00000140
 00000150
 00000160
 00000170
 00000180
 00000190
 00000200
 00000210
 00000220
 00000230
 00000240
 00000250
 00000260
 00000270
 00000280
 00000290
 00000300
 00000310
 00000320
 00000330
 00000340
 00000350
 00000360
 00000370
 00000380
 00000390
 00000400
 00000410
 00000420
 00000430
 00000440
 00000450
 00000460
 00000470
 00000480
 00000490
 00000500
 00000510
 00000520

```

IS(JR,3)=THE LEVEL OF IFUNC FOR THE FUNCTION VALUES FOR THE JRTH 100000530
I2NC(JS)=THE JRTH 1-SET FOR THE JSTH 2ND LEVEL GATE. 00000540
I3RC(JT)=THE JQTH 0-SET FOR THE JTTH 3RD LEVEL GATE. 00000550
IFEED(JU,1)=# OF FEEDING GATES FOR THE I2ND(JU)TH GATE. 00000560
IFEED(JU,JV)=THE JVTH FEEDING JQ FOR THE I2ND(JU)TH GATE. 00000570
MASK2(JW,JTERM)=VALUE OF THE SECOND LEVEL GATE AT JTERM FOR THE 00000580
I2ND(JW)TH GATE. 00000590
MASK3(JX,JTERM)=VALUE OF THE THIRD LEVEL GATE AT JTERM FOR THE 00000600
I3RD(JX)TH GATE. 00000610
ICCNV(JQ)=JX USED FOR INDEX CONVERSION. 00000620
00000630
00000640
00000650
00000660
00000670
00000680
00000690
00000700
00000710
00000720
00000730
00000740
00000750
00000760
00000770
00000780
00000790
00000800
00000810
00000820
00000830
00000840
00000850
00000860
00000870
00000880
00000890
00000900
00000910
00000920
00000921
00000930
00000940
00000950
00000960
00000970
00000980
00000990
0001000
0001010
0001020
0001030
0001040
0001050
0001060
0001070
0001080
0001090
0001100
0001110
0001120
0001130
0001140
0001150
0001160
0001170

<<<INPUT CARDS>>>

THERE IS A SET OF CARDS FOR EACH PROBLEM
TC BE SOLVED. A BLANK TRAILER CARD
FOLLOWS THE LAST SET AND TERMINATES
EXECUTION.

EACH SET CONTAINS THESE CARDS:
CARD 1- TITLE OR NOTE(MUST NOT BE BLANK).
CARD 2-IN 415 FORMAT
COLS 1-5 ORDER,I.E. NUMBER OF INPUTS
COLS 6-10 NUMBER OF MINTERMS TO BE READ
COLS 11-15 NUMBER OF DON'T CARES
COLS 16-20 EXTRA DEBUG OUTPUT DUMP SWITCH,
IF 1 IN COL 20 DUMP IS ON,
IF 0 OR BLANK IN COL 20 ONLY SOLUTION PRINT
COLS 21-25 NOR INDICATOR(IF BLANK SOLVE A NAND
CIRCUIT, BUT IF A POSITIVE VALUE THEN
SOLVE FOR A NOR CIRCUIT).

CARD 3(AND MORE IF NECESSARY)-CONTAINS THE MINTERMS
IN 1615 FORMAT,I.E. EACH MINTERM IS RIGHT
JUSTIFIED IN A FIELD OF 5 COLS.

DIMENSION NGATS(30),NINPT(30)
DIMENSION NCTST(10)
DIMENSION MCKTS(30)
DIMENSION IEPIS(30)
DIMENSION I3RD(30),IFEED(30,10)
DIMENSION MCELL(20)
DIMENSION MXTRM(256)
DIMENSION IFUNC(40,256)
DIMENSION MTRMS(256),IDC(256),ICELL(20)
DIMENSION ICUBE(20)
DIMENSION IS(30,3)
DIMENSION IT(30,2)
DIMENSION ISTMP(20),ITTMP(20)
DIMENSION ICOV(20,256)
DIMENSION LPTST(20)
DIMENSION LPINE(20),I2ND(20),ICOVT(20,256)
DIMENSION TITLE(20)
DIMENSION ITT(30)
DIMENSION MASK3(32,256),MASK2(32,256)
COMMON IN,IOUT,IPRIM,ISSET,IFUNC,LEVEL,
*ICCNV(30),MASK3,MASK2
DATA BLANK/' '/
DATA IBLNK/' '/
DATA IPLUS/'+' /
DATA MINUS/'-' /

IA=5

```

```

INITIALIZE IDBUG. IF IDBUG IS EQUAL
TO ISWTC(ON THE INPUT CARDS) THEN
THE SWITCH IS TURNED ON AND ALL
DEBUG OUTPUT WILL BE PRINTED.

IDBUG=1

IPRT12=12
IDUM=13
IPRT=6
ICUT=6
INRLN=4

INITIALIZE AND PRINT RUN COUNT.

READ(INRUN,20)JRUN,JCRIT,IDBUG,NCASES
20 FCRMAT(I10,I1,2I2)
JRUN=JRUN+1
REWIND INRUN
WRITE(INRUN,20)JRUN,JCRIT,IDBUG,NCASES
WRITE(IOUT,30)JRUN,JCRIT,IDBUG,NCASES
30 FCRMAT(' JRUN=',I10,10X,'JCRIT=',I2,10X,'IDBUG=',I3,10X,
* 'NCASES=',I3)

INITIALIZE CASE COUNT.

JCASES=0

I N P U T

FIRST CARD HAS TITLE.

90 ICUT=IPRT
READ(IN,91)TITLE
91 FCRMAT(20A4)

TEST FOR BLANK CARD(IF BLANK ALL DONE).
(FIRST 72 CCLS BLANK)

DC 52 JMA=1,18
IF(TITLE(JMA)-BLANK)93,92,93
92 CONTINUE

GC TC 9000
93 CONTINUE

STOP IF NCASES HAVE BEEN PROCESSED.

IF(JCASES-NCASES)54,8990,8990
94 CONTINUE
JCASES=JCASES+1

PRINT TITLE.

WRITE(IOUT,96)TITLE
96 FCRMAT('1',20A4)

SECOND CARD HAS FUNCTION PARAMETERS
ON I5 FORMAT.

READ(IN,100)ICRDR,NOTRM,NODC,ISWTC,NOR
100 FCRMAT(16I5)

```

```

000C1180
00001190
00001200
00001210
00001220
000C1230
000C1240
00001250
000C1260
000C1270
00001280
000C1290
00001291
00001292
000C1293
00001294
00001295
00001296
00001297
00001298
000C1299
00001300
00001301
000C1302
000C1303
00001310
00001320
000C1330
00001350
00001360
000C1370
00001380
000C1390
00001400
00001410
000C1420
00001430
00001440
000C1450
00001451
00001452
000C1460
000C1470
00001480
000C1490
00001500
00001510
00001520
000C1530
00001540
00001550
000C1560
00001570
000C1580
00001590
000C1600
000C1610
000C1620
00001630
000C1640
000C1650
000C1660
000C1670
000C1680
000C1690
000C1700

```



```

NCK1=0
LEVEL=1
NCTF=0
MCOV=0
NISF=0
NCSF=0
JSTCP=2**IORDR
IPRIM=JSTOP-1
JPI=JSTOP+1
DO 107 JMA=1,JPI
IFUNC(1,JMA)=0
DO 107 JMA2=1,10
ICOV(JMA2,JMA)=IBLNK
107 CCNTINUE

WRITE(IOUT,110)IORDR,NOTRM,NODC,ISWTC,IDBUG
110 FCRMAT('O FUNCTION OF ORDER:',I5/' WITH',I5,' MINTERMS AND ',I5,'
*DCN'T CARES'/' ISWTC=',I5,' IDBUG=',I5)

READ MINTERMS AND SET FUNCTION VALUE.

READ(IN,100)(MTRMS(JMA),JMA=1,NOTRM)
WRITE(IOUT,111)(MTRMS(JMA),JMA=1,NOTRM)
111 FCRMAT('O MINTERMS ARE:',50(/16I5))

DC 120 JMA=1,NOTRM
JTMP=MTRMS(JMA)+1
IF(JTMP-JSTOP)115,115,113
113 WRITE(IOUT,114)MTRMS(JMA),IORDR
114 FCRMAT('O*****GOOF***** YOU HAVE ENTERED',I10,
# ' WHICH IS TOO BIG AS A MINTERM IN A FUNCTION OF ORDER',
# I2,' *****')
115 CCNTINUE
IFUNC(1,JTMP)=1
120 CCNTINUE

READ DON'T CARES AND FILL FUNCTION VALUES

IF(NODC)141,141,130
130 READ(IN,100)(IDC(JMA),JMA=1,NODC)
WRITE(IOUT,131)(IDC(JMA),JMA=1,NODC)
131 FCRMAT('O DONT CARES ARE:',50(/16I5))
DO 140 JMA=1,NODC
JTMP=IDC(JMA)+1
IFUNC(1,JTMP)=2
140 CCNTINUE
141 CCNTINUE
IF(NOR)150,150,142
142 CCNTINUE

COMPLEMENT INPUTS USING IFUNC(2,J) AS
A SCRATCH PAD.

DC 143 JMA=1,JSTOP
JTMP=JSTOP-JMA+1
IFUNC(2,JTMP)=IFUNC(1,JMA)
143 CCNTINUE

COMPLEMENT FUNCTION AND FIND NEW
WORKING MINTERMS. RESET # OF WORKING
MINTERMS.

NCTRM=0
DO 146 JMA=1,JSTOP
JTMP=IFUNC(2,JMA)

```

IF(JTMP-1)144,146,147	00002340
144 NOTRM=NOTRM+1	00002350
MTRMS(NOTRM)=JMA	00002360
146 IFUNC(2,JMA)=1-JTMP	00002370
147 CCNTINUE	00002380
	00002390
150 CCNTINUE	00002400
	00002410
TEST FOR DEBUG AND SET SWITCH.	00002420
	00002430
IF(ISWTC-IDBUG)152,153,152	00002440
152 ISWTC=IDUM	00002450
GC TO 154	00002460
153 ISWTC=IPRT	00002470
154 ICU1=ISWTC	00002480
	00002490
	00002500
SET MAXTERMS.	00002510
	00002520
JMAII=1	00002530
NCMX=JSTOP-NODC-NCTRM	00002540
JTMP=NCMX	00002550
CC 160 JMA=1,JSTOP	00002560
IF(JTMP)161,161,155	00002570
155 IF(IFUNC(1,JMA))160,156,160	00002580
156 MXTM(JMAII)=JMA-1	00002590
JMAII=JMAII+1	00002600
JTMP=JTMP-1	00002610
160 CCNTINUE	00002620
161 CCNTINUE	00002630
	00002640
	00002650
TEST FOR 1 OR 0 SET.	00002660
	00002670
IF(IFUNC(1,JSTOP))170,180,170	00002680
	00002690
	00002700
F I N D 1 S E T .	00002710
	00002720
170 ISET=1	00002730
CALL SUBFN(NOTRM,MTRMS,NOCEL,ICELL,IS,NOSF)	00002740
	00002750
IF(ACCEL)300,300,171	00002760
	00002770
NOTE: AT THIS POINT NOCEL SHOULD NEVER BE	00002780
	00002790
171 CCNTINUE	00002800
IF(NISF)172,172,173	00002810
	00002820
NISF=NUMBER OF INITIAL SUBFUNCTIONS.	00002830
	00002840
172 CCNTINUE	00002850
NISF=NOCEL	00002860
173 CCNTINUE	00002870
CALL CLPRT(IORDR,NOCEL,ICELL)	00002880
*	00002890
*	00002900
DEBUG STATEMENT NUMBER PRINT.	00002910
*	00002920
ISTMT=173	00002930
WRITE(IOUT,700)ISTMT	00002940
*	00002950
*	00002960
INITIALIZE NEXT LEVEL OF IFUNC.	00002970
	00002980
LP1=LEVEL+1	00002990


```

NCTST(4)=0
NCTST(5)=0
NCTST(6)=0
NTMP=0
ICUBE(1)=1
NSTCP=1
182 NTMF=1
NEWMAX=0
MAXDST=0
183 LCW=MCELL(ICUBE(NTMP))

SUM UP DISTANCES FOR MAXTERMS AS
HARD PLACES CRITERIA.

MAXDST=MAXDST+IDIST(LCW,ICDR)

FILL IN D'S(HERE USE A 2).

JSTRT=LOW+1
DO 190 JMA=JSTRT,JSTOP
IF(IFUNC(LEVEL,JMA)-2)186,190,186
186 JTMP=JMA-1
ITEST=IAND(LCW,JTMP)
IF(ITEST-LCW)190,187,190
187 IFUNC(LEVEL,JMA)=2

INCREMENT NEW MAXTERM COVERED COUNT.

NEWMAX=NEWMAX+1
190 CCNTINUE

IF(NTMP-NSTOP)191,193,193
191 NTMP=NTMP+1
GO TO 183
193 CCNTINUE
WRITE(IOUT,7777)(IFUNC(LEVEL,JKK),JKK=1,JSTOP)
7777 FORMAT(1H ,40I3)
*
* DEBUG STATEMENT NUMBER PRINT.
*
ISTMT=193
WRITE(IOUT,700)ISTMT
*
ISET=1
CALL SUBFN(NOTRM,MTRMS,NOCEL,ICELL,IS,NOSF)

IF(NCCEL)195,195,194
194 CCNTINUE

COUNT NEW MINTERMS AND DISTANCES
TO MINTERMS IN HARD PLACES.

NEWMIN=0
MINDST=0
DO 192 JMA=1,NOCEL
LCW=ICELL(JMA)
MINDST=MINDST+IDIST(LCW,IORDR)
DO 192 JMA2=1,NOTRM
IF(MTRMS(JMA).LT.LCW) GO TO 192
JTMP=MTRMS(JMA)+1
IF(IFUNC(LEVEL,JTMP).NE.1) GO TO 192

```

```

      ITEST=IAND(LOW,MTRMS(JMA2))
      IF(ITEST.NE.LCW) GO TO 192
      IFUNC(LEVEL,JTMP)=3
      NEWMIN=NEWMIN+1
192 CCNTINUE

      CALL STEPS FOR TESTING FOR WHICH
      PRIME IMPLICATE TO KEEP AS A
      THIRD LEVEL GATE CANDIDATE

      CALL STEPS(JCRIT,NCTST,NOCEL,NITMP,NSTOP,ITTMP,MCELL,
      * ICUBE,ISTMP,ICELL,NEWMAX,NEWMIN,MAXDST,MINDST)

195 CCNTINUE

      RESET IFUNC.

      DC 196 JMA2=1,JSTCP
      IFUNC(LEVEL,JMA2)=IFUNC(LM1,JMA2)
196 CCNTINUE

      IF THE CRITERIA IS 4, USE THESE PRIME
      IMPLICATES AS GATE CANDIDATES.

      IF(JCRIT.EQ.4) GO TO 201

      TEST FOR END OF THIS SERIES OF 0 SETS.

      JMA=NSTOP
      NTEST=MOCEL
197 IF(ICUBE(JMA)-NTEST)198,199,199
198 ICUBE(JMA)=ICUBE(JMA)+1
      GC TO 182
199 IF(JMA-1)201,201,200
200 JMA=JMA-1
      NTEST=NTEST-1
      GC TO 197

      THAT NUMBER OF 0-SETS HAS BEEN COMPLETELY
201 CCNTINUE
      IF(NCTST(1))210,210,230

      THESE 0-SETS DID NOT INCREASE 1-SET COVERAGE
210 IF(NSTOP-MOCEL)220,9010,9010
220 NSTOP=NSTOP+1

      REINITIALIZE ICUBE.

      DC 225 JMA=1,NSTOP
      ICUBE(JMA)=JMA
225 CCNTINUE

      GC TO 182
230 CCNTINUE
      WRITE(IOUT,235)
235 FCRMAT('0 ENVELOPE PLEASE, THE CHOSEN 0-SET CELL IS:')
      MCELL=NITMP

      MORE MINTERMS WERE COVERED,MAKE FINDINGS
      DC 252 JMA=1,NITMP
      NOTF=NOTF+1
      LCW=ITTMP(JMA)
      MCELL(JMA)=LOW

```

```

IT(NTF,1)=LOW
JSTRT=LOW+1
                                00004610
                                00004620
                                00004630
                                00004640
                                00004650
                                00004660
                                00004670
                                00004680
                                00004690
                                00004700
                                00004710
                                00004720
                                00004730
                                00004740
                                00004750
                                00004760
                                00004770
                                00004780
                                00004790
                                00004800
                                00004810
                                00004820
                                00004830
                                00004840
                                00004850
                                00004860
                                00004870
                                00004880
                                00004890
                                00004900
                                00004901
                                00004910
                                00004920
                                00004930
                                00004940
                                00004950
                                00004960
                                00004970
                                00004980
                                00004990
                                00005000
                                00005010
                                00005020
                                00005030
                                00005040
                                00005050
                                00005060
                                00005070
                                00005080
                                00005090
                                00005100
                                00005110
                                00005120
                                00005130
                                00005140
                                00005150
                                00005160
                                00005170
                                00005180
                                00005190
                                00005200
                                00005210
                                00005220
                                00005230
                                00005240
                                00005250

                                FILL IN WITH D'S(HERE WITH -NTF AS D'S.

DC 250 JMA2=JSTRT,JSTOP
246      JTMP=JMA2-1
          ITEST=IAND(LOW,JTMP)
          IF(ITEST-LOW)250,248,250
248      IFUNC(LEVEL,JMA2)=-NTF

250 CONTINUE

252 CONTINUE

      ISET=0
      CALL CLPRT(IORDR,MOCEL,MCELL)
      WRITE(IOUT,7777)(IFUNC(LEVEL,JKK),JKK=1,JSTOP),LEVEL
*
*                                DEBUG STATEMENT NUMBER PRINT.
*
      ISTMT=252
      WRITE(IOUT,700)ISTMT
*
      ISET=1

                                GO TO 1-SET HANDLING OF R'S.

      NCCEL=NCTST(1)
      NCTEMP=NCTST(1)
      DC 280 JMA=1,NCTEMP
      ICELL(JMA)=ISTMP(JMA)
280 CONTINUE
      GC TC 171

      C U T P U T .

300 CONTINUE
      CALL CLPRT(IORDR,NOCEL,ICELL)
*
*                                DEBUG STATEMENT NUMBER PRINT.
*
      ISTMT=300
      WRITE(IOUT,700)ISTMT
*
      WRITE(IOUT,400)
400 FORMAT(1H0)
      GC TC 90

                                PRINT HEADINGS AND THEN S AND T FUNCTIONS.

500 CONTINUE
      WRITE(IOUT,505)
505 FORMAT('O LEVEL 3      LEVEL 2')
*
*                                DEBUG STATEMENT NUMBER PRINT.
*
      ISTMT=500
      WRITE(IOUT,700)ISTMT
*

VARIABLES.
ISNCW-THE 1-SET NCW BEING CONSIDERED.
ITFIN-THE 0-SET LAST FINISHED.

```

	ISNCW=1	000C5260
	ITFIN=0	000C5270
	IF(NOSF)550,550,510	00005280
510	CONTINUE	00005290
	IF(IS(ISNOW,2)-ITFIN)520,520,530	000C5300
520	ISET=1	00005310
	CALL CLPR2(IORDR,IS(ISNOW,1))	000C5320
	ISNCW=ISNOW+1	000C5330
	IF(ISNCW-NOSF)510,510,550	00005340
530	ISET=0	00005350
	ITFIN=ITFIN+1	000C5360
	CALL CLPR2(IORDR,IT(ITFIN,1))	000C5370
	GC TC 510	000C5380
		00005390
550	CONTINUE	000C5400
		000C5410
	PRINT INITIAL COVERING TABLE.	000C5420
		000C5430
	LAST=MTRMS(NOTRM)+2	000C5440
	MINI=MTRMS(1)+1	000C5450
	ICCV(NOSF, LAST)=MINUS	000C5460
	N=NOSF	00005470
	WRITE(IOUT,555)	000C5480
555	FORMAT('OINITIAL COVERING TABLE:')	000C5490
*		000C5500
*	DEBUG STATEMENT NUMBER PRINT.	00005510
*		00005520
	ISTMT=555	00005530
	WRITE(IOUT,700)ISTMT	00005540
		00005550
	WRITE(IOUT,560)(MTRMS(JMA),JMA=1,NOTRM)	00005560
560	FORMAT(1H0,4X,32I3)	000C5570
	DC 580 JP=1,N	000C5580
	WRITE(IOUT,570) JP,(ICCV(JP,MTRMS(JMA)+1),JMA=1,NOTRM)	00005590
570	FORMAT(16,32(1X,A1,1X))	000C5600
		000C5610
580	CONTINUE	00005620
	NP1=NOSF+1	000C5630
	NEPIS=1	000C5640
	IEPIS(1)=NOSF	000C5650
		000C5660
	PUT LAST SUBFUNCTION INTO IPI ROW OF ICCV.	000C5670
		00005680
	DC 590 JMA=1,NOTRM	000C5690
	JTMP=MTRMS(JMA)+1	00005700
	ICCV(NP1,JTMP)=ICCV(NOSF,JTMP)	000C5710
590	CONTINUE	00005720
		000C5730
		00005740
	TEST FOR ONLY ONE SUBFUNCTION FOUND DURING	000C5750
	FIRST 1-SET SEARCH.	00005760
		00005770
	JSTCR=0	000C5780
	IF(NISF-1)300,600,630	000C5790
600	CONTINUE	00005800
		000C5810
	CHECK FOR A CNE IN THE PRIMARY CUBE.	000C5820
		00005830
	IF(IPRIM-1)630,620,630	000C5840
620	CONTINUE	00005850
	JSTCR=1	000C5860
630	CONTINUE	00005870
	CALL REDPI(NEPIS,JSTOR,ICOV,NOTRM,MTRMS,MCOV,NOSF,IEPIS,NP1)	000C5880
*		00005890
*	DEBUG STATEMENT NUMBER PRINT.	000C5900
*		00005910

```

      ISTMT=630
      WRITE(IOUT,700)ISTMT
700  FORMAT(1H+,125X,15)
*
      IF(MCOV)2000,2000,1000
1000 CCNTINUE
      CALL      RESET(JSTOP,NEPIS,IEPIS,IS,IT,NOTRM,MTRMS)

      CALL CKFND(NEPIS,IEPIS,IS,IT,I3RD,ICRDR,IFEEC,N3RD,IFST)

1002 CCNTINUE

      CALL M3RDI(NEPIS,IEPIS,N3RD,I3RD,IS,IT,IFEED,ISWTC)

      CALL EL2IN(NEPIS,IEPIS,IS,IT,IFEED,JSTOP,IORDR)

      CALL EL3IN(N3RD,I3RD,IT,NEPIS,IEPIS,IS,IFEED,NGTRM,MTRMS,IORDR,
      $JSTOP,IFST)

      CALL DUPGT(N3RD,I3RD,NEPIS,IT,ISWTC,IFEED)

      ICUT=IPRT

      OUTPUT THIS CIRCUIT.

      JCKT=NCKT+1
      WRITE(IOUT,2205)JCKT

      CALL CKPRT(NEPIS,I3RD,N3RD,IEPIS,IFEED,IS,IT,IORDR,IFST,NCKT,NGATS
      $*,NINPT)

      ATTEMPT TO FIND ALTERNATE
      CIRCUIT.

      ICUT=ISWTC
      N2ND=NEPIS
      WRITE(IOUT,1010)(IEPIS(JMA),JMA=1,NEPIS)
1010 FORMAT(' THE ESSENTIAL PI'S ARE',2X,1015/
      $(25X,1015/))

      CALL ALTCKT(IEPIS,IS,IT,I3RD,IFEED,IFLAG,JSTOP,N3RD,
      $N2ND,NEPIS,IORDR)

      IF(IFLAG)2400,2400,1002

2000 CCNTINUE

      INITIALIZE I2ND'S FIRST PLACES TO ESSENTIAL
      PI'S.

      DO 2010 JMA=1,NEPIS
      I2ND(JMA)=IEPIS(JMA)
2010 CCNTINUE

      INITIALIZE LPINE=LIST OF PRIME IMPLICANTS,
      ESSENTIAL.

      NLPI=0
      DO 2030 JMA=1,NOSF
      IF(ICOV(JMA,LAST)-MINUS)2020,2030,2020
2020 CONTINUE
      NLPI=NLPI+1
      LPINE(NLPI)=JMA
2030 CCNTINUE

C

      INITIALIZE CONSTANTS.

```



```

NMBR=NUMBER OF PI'S CURRENTLY BEING CONSIDERED.
NSTOP=LAST NONESSENTIAL PI TO BE CONSIDERED.
LPTST=LIST OF NONESSENTIAL PI'S CURRENTLY BEING CONSIDERED.

NMBR=1
JNMBR=NLPI
LPTST(1)=1
ISTOP=NLPI

2040 DO 2050 JMA=1,NP1
      DC 2050 JMA2=1, LAST
      ICOVT(JMA,JMA2)=ICOV(JMA,JMA2)
2050 CONTINUE
      NTMP=1
2060 N2NDT=NEPIS+NTMP
2065 I2ND(N2NDT)=LPINE(LPTST(NTMP))
      JSTCR=LPINE(LPTST(NTMP))

      N2NDT REDUCED BECAUSE REDPI INCREMENTS IT.

      N2NDT=N2NDT-1
      CALL REDPI(N2NDT,JSTCR,ICOVT,NOTRM,MTRMS,MCOV,NOSF,I2ND,NP1)
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP)
      *,LPINE(LPTST(NTMP)),N2NDT
*
*          DEBUG STATEMENT NUMBER PRINT.
*
      ISTMT=2065
      WRITE(IOUT,700)ISTMT
*
      IF(NTMP-NMBR)2070,2080,2080
2070 NTMP=NTMP+1
2074 CCNTINUE
      IF(ICOVT(LPINE(LPTST(NTMP)),LAST)-MINUS)2060,2075,2060
2075 LPTST(NTMP)=LPTST(NTMP)+1
      IF(LPTST(NTMP)-ISTOP)2074,2060,2210
2080 WRITE(IOUT,2090)(I2ND(JMA),JMA=1,N2NDT)
2090 FORMAT('ONOW CONSIDERING',2015)
*
*          DEBUG STATEMENT NUMBER PRINT.
*
      ISTMT=2080
      WRITE(IOUT,700)ISTMT
*
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP)
      *,LPINE(LPTST(NTMP)),N2NDT
      IF(MCOV)2300,2300,2200
2200 CCNTINUE

      CALL RESET(JSTOP,N2NDT,I2ND,IS,IT,NCTRM,MTRMS)
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP)
      *,LPINE(LPTST(NTMP)),N2NDT
*
*          DEBUG STATEMENT NUMBER PRINT.
*
      ISTMT=2200
      WRITE(IOUT,700)ISTMT
*
      CALL CKFND(N2NDT,I2ND,IS,IT,I3RD,IORCR,IFEED,N3RD,IFST)

      FILL ITT, A TEMPORARY IT.

      DC 2203 JMA=1,NOTF
      ITT(JMA)=IT(JMA,1)
2203 CCNTINUE

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```

2204 CCNTINUE                                00007240
      JCKT=NCKT+1                            00007250
                                           00007260
      CALL M3RDI(N2NDT,I2ND,N3RD,I3RD,IS,ITT,IFEED,ISWTC) 00007270
                                           00007280
                                           00007290
      CALL EL2IN(N2NDT,I2ND,IS,ITT,IFEED,JSTOP,IORDR)      00007300
      CALL EL3IN(N3RD,I3RD,ITT,N2NDT,I2ND,IS,IFEED,NOTRM,MTRMS,IORDR, 00007310
*JSTCP,IFST)                                                00007320
      N3RCT=N3RD                                           00007330
      CALL DUPGT(N3RD,I3RD,N2NDT,ITT,ISWTC,IFEED)          00007340
      ICUT=IPRT                                           00007350
                                           00007360
      WRITE(IOUT,2205)JCKT                                00007370
2205 FCRMAT('THIS IS CKT #',I2)                          00007380
      CALL CKPRT(N2NDT,I3RD,N3RD,I2ND,IFEED,IS,ITT,IORDR,IFST,NCKT,NGATS 00007390
*,NINPT)                                                    00007400
                                           00007410
                                           00007420
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                                           00007490
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                                           00007870
                                           00007880
                                           00007890

      ATTEMPT TO FIND ALTERNATE
      CIRCUIT.

      ICUT=ISWTC
      CALL ALTCKT(I2ND,IS,ITT,I3RD,IFEED,IFLAG,JSTOP,N3RD,
*N2NCT,NEPIS,IORDR)

      IF(IFLAG)2207,2207,2204
2207 CCNTINUE
      N3RD=N3RDT
      IOUT=ISWTC
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP)
*,LPINE(LPTST(NTMP)),N2NDT
      MCCV=0
      IF(NMBR-JNMBR)2230,2230,2210
2210 CCNTINUE

      HAVING FOUND A COVERAGE, TRY NEW COMBINATIO
      IF(JNMBR-1)2400,2400,2220
2220 JNMBR=JNMBR-1
      NTMF=1
      NMBR=1
      LPTST(1)=LPTST(1)+1
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP)
*,LPINE(LPTST(NTMP)),N2NDT
2222 FCRMAT('JNMBR=',I3,' NMBR=',I3,' NTMP=',I3,' ISTOP=',I3,' LPTST=' 00007680
*,I3,' LPINE=',I3,' N2NDT=',I3) 00007690
* 00007700
* 00007710
* 00007720
* 00007730
* 00007740
* 00007750
* 00007760
* 00007770
* 00007780
* 00007790
* 00007800
* 00007810
* 00007820
* 00007830
* 00007840
* 00007850
* 00007860
* 00007870
* 00007880
* 00007890

      ISTMT=2220
      WRITE(IOUT,700)ISTMT

      IF(LPTST(1)-ISTOP)2040,2040,2400
2230 CCNTINUE
      LPTST(NTMP)=LPTST(NTMP)+1
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP)
*,LPINE(LPTST(NTMP)),N2NDT
* 00007810
* 00007820
* 00007830
* 00007840
* 00007850
* 00007860
* 00007870
* 00007880
* 00007890

      ISTMT=2230
      WRITE(IOUT,700)ISTMT

      IF(LPTST(NTMP)-ISTOP)2040,2040,2240
2240 NTMF=NTMF-1
      IF(NTMF)2400,2400,2245

```

```

2245 CCNTINUE                                00007900
      NMBR=NMBR-1                            00007910
      LPTST(NTMP)=LPTST(NTMP)+1              00007920
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP) 00007930
      *,LPINE(LPTST(NTMP)),N2NDT             00007940
*                                             00007950
*                                           DEBUG STATEMENT NUMBER PRINT. 00007960
*                                           00007970
      ISTMT=2240                             00007980
      WRITE(IOUT,700)ISTMT                   00007990
*                                           00008000
2250 IF(NMBR)2210,2210,2040                 00008010
                                           00008020
2300 CCNTINUE                                00008030
                                           00008040
                                           MINTERMS HAVE NOT BEEN COVERED, INCREASE 00008050
                                           NUMBER OF NONESSENTIAL PI'S TO TRY. 00008060
                                           00008070
      NMBR=NMBR+1                            00008080
      IF(NMBR-JNMBR)2310,2310,2210          00008090
2310 CCNTINUE                                00008100
      NMPF=NTMP+1                            00008110
      LPTST(NTMP)=LPTST(NTMP-1)+1           00008120
2320 CCNTINUE                                00008130
      IF(LPTST(NTMP)-ISTOP)2330,2330,2210   00008140
2330 CCNTINUE                                00008150
      WRITE(IOUT,2222)JNMBR,NMBR,NTMP,ISTOP,LPTST(NTMP) 00008160
      *,LPINE(LPTST(NTMP)),N2NDT             00008170
      IF(ICVLT(LPINE(LPTST(NTMP))),LAST)-MINUS)2060,2340,2060 00008180
2340 CCNTINUE                                00008190
      LPTST(NTMP)=LPTST(NTMP)+1             00008200
      GO TO 2320                             00008210
                                           00008220
                                           PRINT OUT CKT ANALYSIS. 00008230
                                           00008240
2400 ICUT=IPRT                              00008250
      WRITE(IOUT,2410)                       00008260
2410 FORMAT('OCT#   # OF GATES   # OF INPUTS') 00008270
      MING=2000                              00008280
      DO 2490 JMA=1,NCKT                     00008290
      WRITE(IOUT,2420)JMA,NGATS(JMA),NINPT(JMA) 00008300
2420 FORMAT(15,2I13)                        00008310
      IF(NGATS(JMA)-MING)2470,2430,2490      00008320
2430 IF(NINPT(JMA)-MININ)2480,2485,2490      00008330
2470 MING=NGATS(JMA)                         00008340
2480 MININ=NINPT(JMA)                       00008350
      MCKT=JMA                              00008360
      NMCKT=0                               00008370
2485 NMCKT=NMCKT+1                          00008380
      MCKTS(NMCKT)=JMA                     00008390
2490 CCNTINUE                                00008400
      IF(NMCKT-1)2495,2495,2510             00008410
2495 CCNTINUE                                00008420
      WRITE(IOUT,2500)MCKT,MING,MININ        00008430
2500 FORMAT('OBSVIOUSLY CKT#',15,' IS THE MINIMUM WITH ONLY',15,' GATES 00008440
      * AND ONLY',15,' INPUTS')              00008450
      GO TO 90                               00008460
2510 WRITE(IOUT,2520)MING,MININ,(MCKTS(JMA),JMA=1,NMCKT) 00008470
2520 FORMAT('OA TIE AMNG CIRCUITS WITH',13,' GATES AND', 00008480
      *13,' INPUTS/' THE WINNING CIRCUITS ARE:',10I5) 00008490
      GO TO 90                               00008500
                                           00008510
                                           PRINT NUMBER OF CASES PROCESSED. 00008520
                                           00008530
8990 WRITE(IOUT,8991)NCASES                 00008540
                                           00008550

```

[illegible]

```

END
00009210
00009220
00009230
00009240
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SUBROUTINE SUBFN(N,LIST,NCEL,ICELL,IP,NIP)
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THIS SUBROUTINE FINDS THE MEMBERS OF THE X-SET.
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N=NUMBER OF VALUES IN LIST.
LIST=ARRAY OF VALUES(MINTERMS OR MAXTERMS) TO BE CIRCLED ON.
VARIABLES:
IP=PREVIOUSLY CREATED CELLS.
IN=LOGICAL UNIT NUMBER FOR THE INPUT DEVICE.
IOUT=LOGICAL UNIT NUMBER FOR THE OUTPUT DEVICE.
NIP=NUMBER OF PREVIOUS CELLS.
IPRIM=THE PRIMARY CUBE.
ISET=TYPE OF SET TO BE PROCESSED(1-SET OR 0-SET).

JANUARY 16, 1977
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DIMENSION IP(30,2)
DIMENSION IFUNC(40,256)
DIMENSION LIST(1),ICELL(1)
COMMON IN,IOUT,IPRIM,ISET,IFUNC,LEVEL

NCT=1-ISET
NCEL=0

DO 1000 JMA=1,N
LCW=LIST(JMA)
LCW=IAND(LCW,IPRIM)

TEST IF ALL VERTICES ARE IN X-SET.

JTEMP=LOW
30 IF(JTEMP-IPRIM)40,40,100
40 ITEST=IAND(JTEMP,LOW)
IF(ITEST-LOW)60,50,60
50 IF(IFUNC(LEVEL,JTEMP+1)-NOT)60,1000,60
60 JTEMP=JTEMP+1
GO TO 30
100 CCNTINUE

TEST IF THIS CELL IS COVERED.

IF(NCEL)110,210,110
110 CCNTINUE
DO 200 JTEMP=1,NCEL
ITEST=IAND(ICELL(JTEMP),LOW)
IF(ITEST-ICELL(JTEMP))200,1000,200
200 CCNTINUE

TEST IF THIS CELL WAS PREVIOUSLY CREATED.

210 CCNTINUE
IF(NIP)250,250,220
220 DO 240 JTEMP=1,NIP
ITEST=IAND(LOW,IP(JTEMP,1))
IF(ITEST-IP(JTEMP,1))240,1000,240
240 CCNTINUE

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[illegible]

[illegible]

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IGATE=I2ND(JMA)                                00011190
MIN=IS(IGATE,1)                                00011200
JLEVL=IS(IGATE,3)                              00011210
                                                00011220
                                FIND FEEDING 3RD LEVEL GATES FOR THIS GATE. 00011230
                                                00011240
IBEGIN=MIN+1                                    00011250
ISTCP=IPRIM+1                                    00011260
DO 200 JMA2=IBEGIN,ISTOP                        00011270
JTMP=JMA2-1                                      00011280
ITEST=IAND(JTMP,MIN)                            00011290
IF(ITEST-MIN)200,10,200                         00011300
10 CCNTINUE                                     00011310
IF(IFUNC(1,JMA2))15,15,200                      00011320
15 CCNTINUE                                     00011330
IGAT3=IFUNC(JLEVL,JMA2)                        00011340
IF(IGAT3)20,200,200                            00011350
20 CCNTINUE                                     00011360
                                                00011370
                                TEST AND ADD THIS GATE TO 3RD LEVEL LIST. 00011380
                                                00011390
                                                00011400
                                CHECK IF THIS GATE HAS BEEN USED, AND ADD 100011410
                                TO IWUSE IF IT HASN'T BEEN USED.          00011420
                                                00011430
45 IF(NWUSE)70,70,50                           00011440
                                                00011450
50 DO 60 JMA3=1,NWUSE                           00011460
IF(IWUSE(JMA3)-IGAT3)60,200,60                 00011470
60 CCNTINUE                                     00011480
                                                00011490
70 NWUSE=NWUSE+1                                00011500
IWUSE(NWUSE)=IGAT3                             00011510
200 CCNTINUE                                    00011520
                                                00011530
                                IF MIN=0 AND NWUSE=1 THIS IS REDUCIBLE. 00011540
                                                00011550
IF(MIN)205,204,205                             00011560
204 IF(NWUSE-1)205,350,205                     00011570
205 CCNTINUE                                    00011580
                                                00011590
IF(NWUSE)500,500,210                           00011600
210 CCNTINUE                                    00011610
ITEMP=1                                          00011620
DO 300 JMA2=1,NWUSE                             00011630
IFFEED(JMA-IREF,1)=ITEMP                       00011640
ITEMP=ITEMP+1                                    00011650
IGAT3=-IWUSE(JMA2)                              00011660
IFFEED(JMA-IREF,ITEMP)=IGAT3                   00011670
IF(N3RD)290,290,240                             00011680
240 CCNTINUE                                    00011690
DO 280 JMA3=1,N3RD                             00011700
IF(IGAT3-I3RD(JMA3))280,300,280                00011710
280 CCNTINUE                                    00011720
290 CCNTINUE                                    00011730
N3RE=N3RD+1                                      00011740
I3RC(N3RD)=IGAT3                                00011750
300 CCNTINUE                                    00011760
GC TC 500                                        00011770
350 CCNTINUE                                    00011780
IFST=IT(-IWUSE(1),1)                           00011790
N2T=N2T-1                                        00011800
IREF=IREF+1                                      00011810
IF(JMA-N2T)360,360,380                         00011820
                                                00011830
                                MOVE 2ND LEVEL GATES UP TO COVER ELIMINATED 00011840

```


[illegible]

250	CONTINUE		00012510
			00012520
	PRINT 2ND LEVEL.		00012530
			00012540
	IF(NEPIS-JMA)300,260,260		00012550
260	CONTINUE		00012560
	CALL CELL(1S(12ND(JMA),1),IPRIM,IBIN2,NSIZE,IORDR)		00012570
	NTS=IFEED(JMA,1)		00012580
	NINPT(NCKT)=NINPT(NCKT)+NTS+(IORDR-NSIZE)		00012590
	WRITE(IOUT,270)(IBIN2(JMA2),JMA2=1,IORDR)		00012600
270	FORMAT(1H+,27X,10A1)		00012610
	IF(NTS)300,300,280		00012620
280	NTS=NTS+1		00012630
	WRITE(IOUT,290)(ICOMT,IFEED(JMA,JMA2),JMA2=2,NTS)		00012640
290	FORMAT(1H+,37X,9(A2,I2)/)		00012650
			00012660
	PRINT OUT FIRST LEVEL.		00012670
			00012680
300	CONTINUE		00012690
	IF(1-JMA)500,310,310		00012700
310	CONTINUE		00012710
	IF(1FST)500,320,320		00012720
320	CALL CELL(1FST,IPRIM,IBIN2,NSIZE,IORDR)		00012730
	NINPT(NCKT)=NINPT(NCKT)+(IORDR-NSIZE)		00012740
	WRITE(IOUT,330)(IBIN2(JMA2),JMA2=1,IORDR)		00012750
330	FORMAT(1H+,80X,10A1)		00012760
500	CONTINUE		00012770
			00012780
	RETURN		00012790
	END		00012800
			00012810
	////////////////////		00012820
			00012830
			00012840
			00012850
	SUBROUTINE RESET(JSTOP,NEPIS,IEPIS,IS,IT,NOTRM,MTRMS)		00012860
			00012870
	DIMENSION IS(30,1),IT(30,1)		00012880
	DIMENSION IFUNC(40,256)		00012890
	DIMENSION ICOV(20,256),IEPIS(1),MTRMS(1)		00012900
	COMMON IN,IOUT,IPRIM,ISET,IFUNC,LEVEL		00012910
			00012920
	ISTRM=1		00012930
			00012940
			00012950
	SET SUBFUNCTION LEVEL INDICES.		00012960
			00012970
	IF(1S(1,3)-2)1010,1010,1020		00012980
1010	LSTMP=2		00012990
	GO TO 1030		00013000
1020	LSTMP=3		00013010
1030	CONTINUE		00013020
			00013030
	REGENERATE IFUNC VALUES.		00013040
			00013050
C	DO 1300 JMA=2,LEVEL		00013060
	LM1=JMA-1		00013070
	IF(JMA-LSTMP)1040,1070,1040		00013080
			00013090
	RESER IFUNC VALUE FOR RESIDUALS.		00013100
			00013110
1040	DO 1060 JMA2=1,JSTOP		00013120
	IF(1FUNC(JMA,JMA2))1060,1050,1050		00013130
1050	1FUNC(JMA,JMA2)=1FUNC(LM1,JMA2)		00013140
1060	CONTINUE		00013150
	GO TO 1300		00013160

[illegible]

DC 625 JMA=1,NOTRM	00013830
IF(ICOV(NP1,MTRMS(JMA)+1)-IPLUS)630,625,630	00013840
625 CCNTINUE	00013850
MCCV=1	00013860
GC TC 700	00013870
630 CCNTINUE	00013880
	00013890
	00013900
FIND ESSENTIAL PI'S.	00013910
	00013920
DC 680 JMA=1,NOTRM	00013930
JTMP=MTRMS(JMA)+1	00013940
IF(ICOV(NP1,JTMP)-IPLUS)640,680,640	00013950
640 CCNTINUE	00013960
I=0	00013970
DC 660 JMA2=1,NOSF	00013980
IF(ICOV(JMA2,JTMP)-IPLUS)660,650,660	00013990
650 CCNTINUE	00014000
JSTCR=JMA2	00014010
I=I+1	00014020
660 CCNTINUE	00014030
IF(I-1)680,600,680	00014040
680 CCNTINUE	00014050
	00014060
	00014070
ELIMINATE COVERED SUBFUNCTIONS.	00014080
	00014090
700 CCNTINUE	00014100
DC 810 JMA=1,NOSF	00014110
IF(ICOV(JMA,LAST)-MINUS)780,810,780	00014120
780 CCNTINUE	00014130
DC 800 JMA2=1,NOTRM	00014140
JTMP=MTRMS(JMA2)+1	00014150
IF(ICOV(NP1,JTMP)-IPLUS)790,800,790	00014160
790 CCNTINUE	00014170
IF(ICOV(JMA,JTMP)-IPLUS)800,810,800	00014180
800 CCNTINUE	00014190
ICOV(JMA,LAST)=MINUS	00014200
810 CCNTINUE	00014210
	00014220
PRINT REDUCED PI TABLE.	00014230
	00014240
WRITE(IOUT,820)	00014250
820 FORMAT('REDUCED TABLE.')	00014260
	00014270
WRITE(IOUT,830)(MTRMS(JMA),JMA=1,NOTRM)	00014280
830 FORMAT(1H0,4X,32I3)	00014290
DC 900 JP=1,NP1	00014300
IF(ICOV(JP,LAST)-MINUS)850,900,850	00014310
850 CCNTINUE	00014320
WRITE(IOUT,860)JP,(ICOV(JP,MTRMS(JMA)+1),JMA=1,NOTRM)	00014330
860 FORMAT(16,32(1X,A1,1X))	00014340
900 CCNTINUE	00014350
IF(MCOV)905,905,1000	00014360
905 CCNTINUE	00014370
	00014380
CHECK FOR MINTERM COVERAGE.	00014390
	00014400
DC 910 JMA=1,NOTRM	00014410
IF(ICOV(NP1,MTRMS(JMA)+1)-IPLUS)2000,910,2000	00014420
910 CCNTINUE	00014430
MCOV=1	00014440
	00014450
1000 CCNTINUE	00014460
2000 CCNTINUE	00014470
RETRN	00014480

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END
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MINIMIZE 3RD LEVEL INPUTS.
SUBROUTINE M3RDI(N2ND,I2ND,N3RD,I3RD,IS,IT,IFEED,ICUT)

I2ND=LIST OF 2ND LEVEL GATES.
I3RD=LIST OF 3RD LEVEL GATES.
N2ND=NUMBER OF 2ND LEVEL GATES.
N3RD=NUMBER OF 3RD LEVEL GATES.
IFEED=FEEDING 3RD LEVEL GATES TO A PARTICULAR 2ND LEVEL GATE.
IS= CELL MINIMUMS FOR 2ND LEVEL INPUTS.
IT= CELL MINIMUMS FOR 3RD LEVEL INPUTS.
IELIM=LIST OF INPUTS TO BE ELIMINATED.
JMA= LOCP INDEX.
JMA2=INTERIOR LOOP INDEX.
ICUT=OUTPUT DEVICE LOGICAL UNIT NUMBER
DIMENSION IT(30,1),IS(30,1)
DIMENSION IFEED(30,1)
DIMENSION IELIM(30)
DIMENSION I2ND(1),I3RD(1)

IF(N3RD)1000,1000,10
10 IF(N2ND)1000,1000,20
20 CCNTINUE

INITIALIZE POTENTIAL INPUT ELIMINATIONS.

DC 40 JMA=1,N3RD
IG=I3RD(JMA)
IELIM(IG)=IT(IG,1)
WRITE(IOUT,30)JMA,IG,IELIM(IG)
30 FORMAT('0JMA=',I4,' IG=',I4,' IELIM(IG)=',I5)
40 CCNTINUE

AND EACH 3RD LEVEL POTENTIAL INPUT ELIMINATION
WITH THE 2ND LEVEL GATES IT FEEDS TO
FIND INPUTS TO BE ELIMINATED.

DC 80 JMA=1,N2ND
IF(IFEED(JMA,1))80,80,50
50 ITEMP=IFEED(JMA,1)+1
MIN=IS(I2ND(JMA),1)
DC 60 JMA2=2,ITEMP
IG=IFEED(JMA,JMA2)
IELIM(IG)=IAND(MIN,IELIM(IG))
WRITE(IOUT,55)JMA,JMA2,IG,IELIM(IG),MIN
55 FORMAT(' JMA=',I4,' JMA2=',I4,' IG=',I4,' IELIM=',I4,' MIN=',I4)
60 CCNTINUE
80 CCNTINUE

ELIMINATE THE INPUTS BY EXCLUSIVE ORING.

DC 100 JMA=1,N3RD
IG=I3RD(JMA)
IT(IG,1)=IXOR(IT(IG,1),IELIM(IG))
WRITE(IOUT,30)JMA,IG,IELIM(IG)
100 CCNTINUE
1000 CCNTINUE

RETURN
END

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[illegible]

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                                ATTEMPT TO REMOVE 2ND LEVEL INPUTS.

JENC=MAXC+1

DO 250 JMA2=1,IORDR
IF(1B(IN(JMA2)-JONE)250,150,250
150 CCNTINUE
    IRMCV=2**((IORDR-JMA2)
    MINT=MIN-IRMOV
    IF(MINT)250,155,155
155 CCNTINUE
    JBEG=MINT+1

                                TEST IF ALL THE ENTRIES IN THE NEW CELL
                                ARE MINTERMS OR DON'T CARES.

DO 200 JMA3=JBEG,JEND

                                TEST IF THIS TERMS VALUE IS A MINTERM OR
                                IF((IFUNC(1,JMA3))160,160,200
160 CCNTINUE

                                TEST IF THIS TERM IS THE NEW CELL.

JTERM=JMA3-1
JTEST=IAND(JTERM,MINT)
IF(JTEST-MINT)200,170,200
170 CCNTINUE
JTEST=IAND(JTERM,MAXC)
IF(JTEST-JTERM)200,180,200
180 CCNTINUE

                                THIS TERM IS IN THE CELL BUT IS NOT A VALUE
                                OF ONE OR A D.C. IN THE ORIGINAL FUNCTION.
                                DO NOT ELIMINATE IRMOV, JUMP TO NEXT TRY.

GC TO 250
200 CCNTINUE

                                HAVING CHECKED ALL VALUES IN THE NEW CELL
                                AND FOUND THAT THEY ARE 1'S OR DC'S, ELIMIN
                                INPUT IRMOV BY SETTING MIN TO MINT.

MIN=MINT
250 CCNTINUE

                                MAKE NEW CELL MIN PERMANENT.

IS(J2ND,1)=MIN
GC TC 1000

300 CCNTINUE

                                MORE THAN ONE FEEDING 3RD LEVEL GATE SPECIA
                                INITIALIZE INHIBITING 3RD LEVEL MASK.

                                SET ALL VALUES TO ONES.

CC 350 JMA2=1,JSTCP
MASK3(JMA2)=1
350 CCNTINUE

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PLACE ZEROES IN TERMS COVERED BY 3RD LEVEL
NFEED=NFEED+1
DC 400 JMA2=2,NFEED
MINF3=1T(IFEED(JMA,JMA2),1)
JBEG=MINF3+1
DO 380 JMA3=JBEG,JSTOP
JTEST=JMA3-1
JTEST=1AND(JTEST,MINF3)
IF(JTEST-MINF3)380,360,380
360 MASK3(JMA3)=0
380 CONTINUE

400 CONTINUE

FIND SECOND LEVEL CELL.

CALL CELL(MIN,MAX,IBIN,NSIZE,IORDR)

BEGIN REMOVING INPUTS.

DO 600 JMA2=1,IORDR
IF(IBIN(JMA2)-JONE)600,410,600
410 CONTINUE
IRMCV=2** (IORDR-JMA2)
MINT=MIN-IRMOV
JBEG=MINT+1

TEST IF ALL NEW ENTRIES ARE MINTERMS OR D.C.
DC 500 JMA3=JBEG,JSTOP
IF(IFUNC(1,JMA3))450,450,500

TEST IF THIRD LEVEL MASK INHIBITS THIS TERM
450 IF(MASK3(JMA3))500,500,460
460 CONTINUE

TEST IF THIS TERM IS IN THE CELL.

JTEST=JMA3-1
JTEST=1AND(JTEST,MINT)
IF(JTEST-MINT)500,600,500
500 CONTINUE

HAVING CHECKED ALL NEW TERMS AND FOUND THEM
MINTERMS OR DC'S, ELIMINATE THIS INPUT.

MIN=MINT
600 CONTINUE

MAKE ELIMINATIONS PERMANENT.

IS(J2ND,1)=MIN

1000 CONTINUE
RETURN
END

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SUBROUTINE EL3IN(N3RD,I3RD,IT,N2ND,I2ND,IS,IFEED,NOTRM,MTRMS,IORDRO J017130
$,JSTOP,IFST) 00017140
00017150
00017160
00017170
J3RC-THIRD LEVEL GATE TO BE PUT INTO MASK3. 00017180
J2ND-SECOND LEVEL GATE TO BE PUT ONTO MASK2. 00017190
N2NC-NUMBER OF SECCND LEVEL GATES. 00017200
I2NC-LIST OF SECOND LEVEL GATES. 00017210
IS-LIST OF SECOND LEVEL GATE CELL MINIMUMS. 00017220
N3RC-NUMBER OF 3RD LEVEL GATES. 00017230
I3RC-LIST OF THIRC LEVEL GATES. 00017240
IT-LIST OF THIRD LEVEL GATE INPUT CELL MINIMUMS. 00017250
IFEED-LIST OF FEEDING 3RD LEVELS TO 2ND LEVEL. 00017260
MASK2-MASK OF VALUES FOR SECOND LEVEL GATES. 00017270
MASK3-MASK OV VALUES FOR 3RD LEVEL GATES. 00017280
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DIMENSION IFUNC(40,256)
DIMENSION LFST(256)
DIMENSION MTRMS(1)
DIMENSION IT(30,1),IS(30,1),IFEED(30,1)
DIMENSION I3RD(1),I2ND(1)
DIMENSION IBIN(10)
DIMENSION MASK3(32,256)
DIMENSION MASK2(32,256)
DIMENSION ICONV(30)
COMMON IN,IOUT,MAX,JSET,IFUNC,LEVEL,ICONV,MASK3,MASK2
DATA JCNE/'1'/

INITIALIZE CONVERSION INDEX. THIS CONVERTS
THE VALUE OF IFEED,WHICH IS AN INDEX FOR ITO
TO AN INDEX FOR MASK3.

DC 20 JMA=1,N3RD
JTMP=I3RD(JMA)
ICONV(JTMP)=JMA
20 CONTINUE

JFILL=0
IF(IFST)50,40,40
40 JFILL=1
50 CONTINUE

CLEAR THE MASKS.

DC 100 JMA=1,JSTOP
DO 80 JMA2=1,N3RD
MASK3(JMA2,JMA)=1
80 CONTINUE

DC 90 JMA2=1,N2ND
MASK2(JMA2,JMA)=0
90 CONTINUE

INITIALIZE FIRST LEVEL VECTOR.

LFST(JMA)=JFILL
100 CONTINUE

WRITE(IOUT,110)
110 FORMAT('OMASK3',120X,'EL3IN')

FILL MASK3 WITH ACTUAL VALUES.

```

```

DO 250 JMA=1,N3RD
J3RD=I3RD(JMA)
MIN=IT(J3RD,1)
JBEG=MIN+1
DO 200 JMA2=JBEG,JSTOP
JTMP=JMA2-1
JTST=IAND(JTMP,MIN)
IF(JTST-MIN)200,190,200
190 CCNTINUE
MASK3(JMA,JMA2)=0
200 CCNTINUE

WRITE(IOUT,210)JMA,(MASK3(JMA,JMA2),JMA2=1,JSTCP)
210 FORMAT(1X,I5,',',',',16I6)
250 CCNTINUE

FILL FIRST LEVEL VECTOR IF INPUTS ARE
AT THE FIRST LEVEL GATE.

IF(IFST)280,260,260
260 MIN=IFST
JBEG=MIN+1
DC 270 JMA=JBEG,JSTOP
JTST=JMA-1
JTST=IAND(JTST,MIN)
IF(JTST-MIN)270,265,270
265 LFST(JMA)=0
270 CCNTINUE

280 CCNTINUE

WRITE(IOUT,285)(LFST(JMA),JMA=1,JSTOP)
285 FORMAT('0LFST ',16I6)

FILL MASK2.

DO 340 JMA=1,N2ND
J2ND=I2ND(JMA)
MIN=IS(J2ND,1)
JBEG=MIN+1
DC 300 JMA2=JBEG,JSTOP
JTMP=JMA2-1
JTST=IAND(JTMP,MIN)
IF(JTST-MIN)300,290,300
290 MASK2(JMA,JMA2)=1
300 CCNTINUE

WRITE(IOUT,210)JMA,(MASK2(JMA,JMA2),JMA2=1,JSTCP)
340 CCNTINUE

ELIMINATE INPUTS TO 3RD LEVEL GATE BY GATE.

DO 700 JMA=1,N3RD
J3RD=I3RD(JMA)
MIN=IT(J3RD,1)
CALL CELL(MIN,MAX,IBIN,NSIZE,IORDR)

WRITE(IOUT,345)(IBIN(JMA2),JMA2=1,IORDR)
345 FORMAT(1H0,10A1)

IF(IORDR-NSIZE-1)700,700,350
350 CCNTINUE

ELIMINATE INPUTS ONE AT A TIME.

DO 600 JMA2=1,IORDR

```

```

00017790
00017800
00017810
00017820
00017830
00017840
00017850
00017860
00017870
00017880
00017890
00017900
00017910
00017920
00017930
00017940
00017950
00017960
00017970
00017980
00017990
00018000
00018010
00018020
00018030
00018040
00018050
00018060
00018070
00018080
00018090
00018100
00018110
00018120
00018130
00018140
00018150
00018160
00018170
00018180
00018190
00018200
00018210
00018220
00018230
00018240
00018250
00018260
00018270
00018280
00018290
00018300
00018310
00018320
00018330
00018340
00018350
00018360
00018370
00018380
00018390
00018400
00018410
00018420
00018430
00018440

```

```

IF (IBIN(JMA2)-JONE)600,360,600
360 CCNTINUE
IRMCV=2** (IORDR-JMA2)
MINT=MIN-IRMOV
JBEG=MINT+1

REVALUE MASK3.

DO 380 JMA3=JBEG,JSTOP
JTST=JMA3-1
JTST=IAND(JTST,MINT)
IF (JTST-MINT) 380,370,380
370 CCNTINUE
MASK3(JMA,JMA3)=0
380 CONTINUE

WRITE(IOUT,381) (MASK3(JMA,JMA3),JMA3=1,JSTOP)
381 FORMAT('OMASK3 ',16I6)

TEST FOR MINTERM COVERAGE.

DO 500 JMA3=1,NOTRM
MTERM=MTRMS(JMA3)+1

IF (LFST(MTERM))390,390,500
390 CCNTINUE

TEST EACH SECOND LEVEL GATE FOR A MASK2
VALUE OF 1.

DO 480 JMA4=1,N2ND
IF (MASK2(JMA4,MTERM))480,480,400
400 CCNTINUE
NFEED=IFEED(JMA4,1)
IF (NFEED)500,500,410
410 NFEED=NFEED+1

TEST EACH THIRD LEVEL GATE MASK3 FOR A
VALUE OF 1.

DO 470 JMA5=2,NFEED
JTMP=MASK3(ICCNU(IFEED(JMA4,JMA5)),MTERM)
IF (JTMP)480,480,470
470 CONTINUE

THIS GATE COVERS A ONE, GO TO NEXT
MINTERM FOR TESTING.

GO TO 500
480 CCNTINUE

THIS MINTERM WAS NOT COVERED, DO NOT
ELIMINATE THIS INPUT. REINITIALIZE THE MASK3

GO TO 510

500 CCNTINUE

MINTERMS ARE COVERED MAKE THIS NEW MIN.

MIN=MINT
GO TO 600

SOME MINTERM NOT COVERED, REINITIALIZE MASK3

```

[illegible]

```

      DO 100 JMA3=JMA2,N3RD
      I3RD(JMA3)=I3RD(JMA3+1)
100  CCNTINUE
200  JMA2=JMA2+1
      GC TO 25
300  JMA=JMA+1
      GC TO 15
                                00019770
                                00019780
                                00019790
                                00019800
                                00019810
                                00019820
                                00019830
                                00019840
                                00019850
      FINISHED SEARCHING FOR DUPLICATES.
      TEST FLAG TO SEE IF ANY DUPLICATES WERE FOUND
                                00019860
                                00019870
                                00019880
                                00019890
                                00019900
                                00019910
                                00019920
                                00019930
                                00019940
                                00019950
                                00019960
                                00019970
                                00019980
                                00019990
                                00020000
                                00020010
                                00020020
                                00020030
                                00020040
                                00020050
                                00020060
                                00020070
                                00020080
                                00020090
                                00020100
                                00020110
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                                00020170
                                00020180
                                00020190
                                00020200
                                00020210
                                00020220
                                00020230
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

400  IF(IFLAG)500,700,500
                                00019870
                                00019880
                                00019890
                                00019900
                                00019910
                                00019920
                                00019930
                                00019940
                                00019950
                                00019960
                                00019970
                                00019980
                                00019990
                                00020000
                                00020010
                                00020020
                                00020030
                                00020040
                                00020050
                                00020060
                                00020070
                                00020080
                                00020090
                                00020100
                                00020110
                                00020120
                                00020130
                                00020140
                                00020150
                                00020160
                                00020170
                                00020180
                                00020190
                                00020200
                                00020210
                                00020220
                                00020230
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

      CORRECT IFEEED FOR REMOVED GATES.
                                00019910
                                00019920
                                00019930
                                00019940
                                00019950
                                00019960
                                00019970
                                00019980
                                00019990
                                00020000
                                00020010
                                00020020
                                00020030
                                00020040
                                00020050
                                00020060
                                00020070
                                00020080
                                00020090
                                00020100
                                00020110
                                00020120
                                00020130
                                00020140
                                00020150
                                00020160
                                00020170
                                00020180
                                00020190
                                00020200
                                00020210
                                00020220
                                00020230
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

500  CCNTINUE
      DO 600 JMA=1,N2ND
      NFEED=IFEEED(JMA,1)
      IF(NFEED)600,600,510
510  NFEED=NFEED+1
      WRITE(IOUT,520)JMA,(IFEEED(JMA,JMA2),JMA2=2,NFEED)
520  FORMAT('0JMA=',I5,' IFEEED=',I21,16I5/)
      DO 580 JMA2=2,NFEED
      IFEEED(JMA,JMA2)=IDUP(IFEEED(JMA,JMA2))
580  CCNTINUE
      WRITE(IOUT,520)JMA,(IFEEED(JMA,JMA2),JMA2=2,NFEED)
600  CCNTINUE
                                00020040
                                00020050
                                00020060
                                00020070
                                00020080
                                00020090
                                00020100
                                00020110
                                00020120
                                00020130
                                00020140
                                00020150
                                00020160
                                00020170
                                00020180
                                00020190
                                00020200
                                00020210
                                00020220
                                00020230
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

700  CCNTINUE
      RETRN
      END
                                00020100
                                00020110
                                00020120
                                00020130
                                00020140
                                00020150
                                00020160
                                00020170
                                00020180
                                00020190
                                00020200
                                00020210
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                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

SUBROUTINE ALTCKT(I2ND,IS,IT,I3RD,IFEEED,IFLAG,
1JSTCP,N3RD,N2ND,NEPIS,IORDR)
                                00020160
                                00020170
                                00020180
                                00020190
                                00020200
                                00020210
                                00020220
                                00020230
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

      THIS ROUTINE ATTEMPTS TO MODIFY A CIRCUIT
      BY REPLACING FEEDING THIRD LEVEL GATES.
                                00020200
                                00020210
                                00020220
                                00020230
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

NCV 24, 1977
VARIABLES:
      JMA,JMA2,JMA3,JMA4-LOOP INDICES.
      IFLAG-FLAG WHICH INDICATES ALTERED CIRCUIT.
      =0 MEANS NO ALTERATIONS.
      =+ MEANS SOME ALTERATIONS.
      NRMOV-NUMBER OF REMOVED 3RD LEVEL FEEDING GATES.
      MIN2 -MINIMUM OF CELL FOR SECOND LEVEL GATE.
      MFEED-MINIMUM FOR CELL OF 3RD LEVEL FEEDING GATE.
      IGATE-FEEDING 3RD LEVEL GATE.
      IGTMP-TEMP 3RD LEVEL GATE TO ALTER CIRCUIT.
                                00020240
                                00020250
                                00020260
                                00020270
                                00020280
                                00020290
                                00020300
                                00020310
                                00020320
                                00020330
                                00020340
                                00020350
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

      DIMENSION I2ND(1),I3RD(1),MASK2(32,256)
      DIMENSION MASK3(32,256),IS(30,1),IT(30,1)
      DIMENSION IFEEED(30,1),IFUNC(40,256)
                                00020360
                                00020370
                                00020380
                                00020390
                                00020400
                                00020410
                                00020420

      CCMCN IN,IOUT,IPRIM,ISSET,IFUNC,LEVEL,
1 ICCNV(30),MASK3,MASK2
                                00020400
                                00020410
                                00020420

```

```

IFLAG=0
NRMOV=0

INITIALIZE MASKS.

CLEAR MASKS.

DO 100 JMA=1,JSTOP
DC 80 JMA2=1,N3RD
MASK3(JMA2,JMA)=1
80 CCNTINUE

DC 90 JMA2=1,N2ND
MASK2(JMA2,JMA)=0
90 CCNTINUE

100 CCNTINUE

FILL MASK3 WITH ACTUAL VALUES.

DO 250 JMA=1,N3RD
J3RC=I3RD(JMA)
MIN=IT(J3RD,1)
JBEG=MIN+1

DO 200 JMA2=JBEG,JSTOP
JTMP=JMA2-1
JTST=IAND(JTMP,MIN)
IF(JTST-MIN)200,190,200
190 CCNTINUE

MASK3(JMA,JMA2)=0
200 CCNTINUE

WRITE(IOUT,210)JMA,(MASK3(JMA,JMA2),JMA2=1,JSTOP)
210 FORMAT(' ALTCKT ',I5/(I3X,16I6))
250 CCNTINUE

FILL MASK2 WITH ACTUAL VALUES.

DO 340 JMA=1,N2ND
J2ND=I2ND(JMA)
MIN=IS(J2ND,1)
JBEG=MIN+1
WRITE(IOUT,260)JMA,J2ND,MIN
260 FORMAT('O GATE=',I5,' CNE-SET=',I5,' CELLMIN=',
+I5)

DC 300 JMA2=JBEG,JSTOP
JTMP=JMA2-1
JTST=IAND(JTMP,MIN)
IF(JTST-MIN)300,290,300
290 MASK2(JMA,JMA2)=1
300 CCNTINUE

WRITE(IOUT,210)JMA,(MASK2(JMA,JMA2),JMA2=1,JSTOP)
340 CCNTINUE

CREATE ALTERNATE CIRCUITS.

LOOP THROUGH ALL SECOND LEVEL GATES(EXCEPT
LAST ONE GENERATED).

```

```

00020430
00020440
00020450
00020460
00020470
00020480
00020490
00020500
00020510
00020520
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00020790
00020800
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00020900
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00020970
00020980
00020990
00021000
00021010
00021020
00021030
00021040
00021050
00021060
00021070
00021080

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DC 500 JMA=2,N2ND	00021090
NFEED=IFEED(JMA,1)	00021100
	00021110
	00021120
LOOP THROUGH FEEDING THIRD LEVEL GATES TO	00021130
SEE IF ANY CAN BE REPLACED.	00021140
	00021150
IF(NFEED)500,500,350	00021160
350 CCNTINUE	00021170
NFEED=NFEED+1	00021180
J2ND=I2ND(JMA)	00021190
MIN2=IS(J2ND,1)	00021200
JBEG2=MIN2+1	00021210
	00021220
	00021230
DC 450 JMA2=2,NFEED	00021240
IGATE=IFEED(JMA,JMA2)	00021250
MFEED=IT(IGATE,1)	00021260
	00021270
	00021280
LOOP THROUGH POSSIBLE REPLACEMENTS.	00021290
	00021300
DO 400 JMA3=1,N3RD	00021310
IF(IGATE-I3RD(JMA3))360,400,400	00021320
360 IGTMP=I3RD(JMA3)	00021330
	00021340
LOOP THROUGH TERMS TO CHECK FOR MAXTERM	00021350
COVERAGE AND AVOID MINTERM INHIBITION.	00021360
	00021370
DO 380 JMA4=JBEG2,JSTOP	00021380
	00021390
TEST IF WE ARE IN THE CELL.	00021400
	00021410
JTEMP=JMA4-1	00021420
JTST=IAND(JTEMP,MIN2)	00021430
IF(JTST-MIN2)380,362,380	00021440
362 CCNTINUE	00021450
	00021460
TEST FOR EFFECT OF OTHER	00021470
FEEDING THIRD LEVEL GATES.	00021480
	00021490
IF(NFEED-2)366,366,363	00021500
363 CCNTINUE	00021510
	00021520
DC 365 JMA5=2,NFEED	00021530
IF(JMA5-JMA2)364,365,364	00021540
364 IF(MASK3(ICONV(IFEED(JMA,JMA5)),JMA4))365,380,365	00021550
365 CCNTINUE	00021560
	00021570
366 CCNTINUE	00021580
JTMP=MASK3(ICONV(IGTMP),JMA4)	00021590
	00021600
TEST FOR FUNCTIONAL EQUALITY.	00021610
	00021620
IF(JTMP*MASK2(JMA,JMA4)-IFUNC(1,JMA4))400,380,400	00021630
380 CCNTINUE	00021640
	00021650
IFLAG=IFLAG+1	00021660
IFEED(JMA,JMA2)=IGTMP	00021670
GO TO 450	00021680
400 CCNTINUE	00021690
	00021700
	00021710
450 CCNTINUE	00021720
	00021730
500 CCNTINUE	00021740

```

                                00021750
                                00021760
                                00021770
                                00021780
                                00021790
                                00021800
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                                00021920
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                                00021950
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                                00021980
                                00021990
                                00022000
                                00022010
                                00022020
                                00022030
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                                00022280
                                00022290
                                00022300
                                00022310
                                00022320
                                00022330
                                00022340
                                00022350
                                00022360
                                00022361
                                00022362
                                00022363
                                00022364

UPDATE I3RD IN THE EVENT OF A
    GATE HAVING BEEN REMOVED.

                                CHECK WHETHER ANY 3RD LEVEL GATE
                                HAS BEEN COMPLETELY REPLACED IN
                                ALL CASES.

                                FIRST TEST IF ANY CHANGES WERE MADE.

IF(IFLAG)510,510,550
510 WRITE(IGUT,520)
520 FORMAT(' ALTCKT FOUND NO CHANGES FOR FEEDING GATES')
    RETURN

                                LOOP THROUGH I3RD.

550 JMA=1
560 IF(JMA-N3RD)570,570,1010

570 WRITE(IGUT,580)JMA,I3RD(JMA)
580 FORMAT(' JMA=',I5,' NOW CONSIDERING REMOVING GATE',
    *I5)

                                LOOP THROUGH IFEEED.

DC 800 JMA2=1,N2ND
NFEED=IFEEED(JMA2,1)

                                TEST FOR ANY FEEDING 3RD LEVEL GATES.

IF(NFEED)800,800,600
600 NFEED=NFEED+1

DC 800 JMA3=2,NFEED
IF(IFEEED(JMA2,JMA3)-I3RD(JMA))800,1000,800
800 CONTINUE

WRITE(IGUT,810)NRMOV
810 FORMAT(1H+,40X,'THIS IS THE',I3,'TH GATE REMOVED.')

NRMOV=NRMOV+1
N3RC=N3RD-1
DC 850 JMA3=JMA,N3RD
I3RD(JMA3)=I3RD(JMA3+1)
850 CONTINUE

GC TC 560
1000 JMA=JMA+1
GC TC 560

1010 CONTINUE

WRITE(IGUT,1020)IFLAG,NRMOV
1020 FORMAT(' ALTCKT HAS MADE ',I5,' CHANGES AND ',I5,' 3RD LEVEL '
    *, 'GATE REMOVALS')
    RETURN
END
FUNCTION IDIST(MIN,IORDR)

    THIS FUNCTION FINDS THE DISTANCE FROM THE
    PRIMARY CUBE IN A SYSTEM OF ORDER IORDR AND

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```

SCME VALUE MIN.
J=C
DO 100 JMA=1, IORDR
  ITEST=2**{JMA-1}
  ITEST=IAND(MIN, ITEST)
  IF(ITEST)100, 50, 100
50 J=J+1
100 CONTINUE
  ICIST=J
  RETURN
END
SUBROUTINE STEP5(JCRIT, NCTST, NOCEL, NITMP, NSTOP, ITTMP, MCELL,
* ICUBE, ISTMP, ICELL, NEWMAX, NEWMIN, MAXDST, MINDST)

  THIS SUBROUTINE DOES THE STEP5 CHOOSING FOR SVAING
  PRIME IMPLICANTS AS GATE CANDIDATES.

  DIMENSION NCTST(1), ITTMP(1), MCELL(1), ICUBE(1), ISTMP(1)
  DIMENSION ICELL(1), IFUNC(40, 256)
  COMMON IN, IOUT, IPRIM, ISET, IFUNC, LEVEL

  GO TO THE CRITERIA FOR THIS METHOD.

  GC TC(50, 10, 20, 190, 30, 40), JCRIT

  TEST IF THIS COUNT OF NEW MINTERMS IS GREATER
  THAN PREVIOUSLY COVERED.

10 IF(NEWMIN.LE.NCTST(2)) RETURN
  NCTST(2)=NEWMIN
  GC TC 190

  TEST IF THIS COUNT OF NEW MAXTERMS IS
  GREATER THAN PREVIOUSLY COVERED.

20 IF(NEWMAX.LE.NCTST(3)) RETURN
  NCTST(3)=NEWMAX
  GO TO 190

  TEST FOR MAXTERMS IN HARD PLACES(TOTAL DISTANCE
  FORM PRIMARY CUBE.).

30 IF(MAXDST.LE.NCTST(5)) RETURN
  NCTST(5)=MAXDST
  GC TC 190

  TEST FOR MINTERMS IN HARD PLACES.

40 IF(MINDST.LE.NCTST(6)) RETURN
  NCTST(6)=MINDST
  GC TC 190

  TEST FOR MOST SUBFUNCTIONS(1-SETS) GENERATED.

50 IF(NOCEL.LE.NCTST(1)) RETURN
190 NCTST(1)=NOCEL
  NITMP=NSTOP

  DO 192 JMA=1, NSTOP
    ITTMP(JMA)=MCELL(ICUBE(JMA))
192 CONTINUE

  NCTEMP=NCTST(1)
  DO 202 JMA=1, NCTEMP
    ISTMP(JMA)=ICELL(JMA)
202 CONTINUE

```

EXAMPLE 2 FIGURE 3 PAGE 52 IN PAPER

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FUNCTION OF ORDER: 4
WITH 7 MINTERMS AND 0 DCN'T CARES
ISWTC= 1 IDBUG= 2

MINTERMS ARE:

3 8 10 11 12 13 15

THIS IS CKT # 1

3RD LEVEL GATES

T 2 ---1
T 1 -11-

2ND LEVEL GATES,AND INPUTS FROM 3RD LEVEL

1--- ,T 2,T 1
--11 ,T 1
1-11
11-1

DIRECT INPUTS TO FIRST LEVEL

THIS IS CKT # 2

3RD LEVEL GATES

T 2 ---1
T 1 -11-

2ND LEVEL GATES,AND INPUTS FROM 3RD LEVEL

1--- ,T 2,T 1
--11 ,T 1
1-11
11-- ,T 1

DIRECT INPUTS TO FIRST LEVEL

THIS IS CKT # 3

3RD LEVEL GATES

T 2 ---1
T 1 -11-

2ND LEVEL GATES,AND INPUTS FROM 3RD LEVEL

1--- ,T 2,T 1
--11 ,T 1
11-1

DIRECT INPUTS TO FIRST LEVEL

CKT#	# OF GATES	# OF INPUTS
1	7	19
2	7	19
3	6	15

OBVIOUSLY CKT# 3 IS THE MINIMUM WITH ONLY 6 GATES AND ONLY 15 INPUTS

H. P. LEE EG. 6 PG 22

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FUNCTION OF ORDER: 6
WITH 20 MINTERMS AND 0 DON'T CARES
ISWTC= 1 IDBUG= 2

MINTERMS ARE:

0 1 2 4 5 6 8 9 16 17 18 20 21 22 24 25
34 38 40 41

THIS IS CKT # 1

3RD LEVEL GATES

T 1 ----11

T 4 --1-1-

T 2 --11--

T 5 1-----

T 3 -1-----

2ND LEVEL GATES, AND INPUTS FROM 3RD LEVEL

-----, T 1, T 4, T 2, T 5

-----1-, T 1, T 4, T 3

--1----, T 4, T 2, T 3

DIRECT INPUTS TO FIRST LEVEL

CKT#	# OF GATES	# OF INPUTS
1	9	23

OBVIOUSLY CKT# 1 IS THE MINIMUM WITH ONLY 9 GATES AND ONLY 23 INPUTS

EXAMPLE 2 FIGURE 3 PAGE 16 IN PROPOSAL

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FUNCTION OF ORDER: 3
WITH 5 MINTERMS AND 0 DON'T CARES
ISWTC= 1 ICBUG= 2

MINTERMS ARE:
0 1 2 3 5

THIS IS CKT # 1

3RD LEVEL GATES
T 1 -1-

2ND LEVEL GATES, AND INPUTS FROM 3RD LEVEL
--1 ,T 1

DIRECT INPUTS TO FIRST LEVEL
1--

CKT#	# OF GATES	# OF INPUTS
1	3	5

OBVIOUSLY CKT# 1 IS THE MINIMUM WITH ONLY 3 GATES AND ONLY 5 INPUTS

VITA

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