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Reconocimiento de validez oficial de estudios de nivel superior según acuerdo secretarial 15018, publicado en el Diario Oficial de la Federación el 29 de noviembre de 1976.

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Departamento de Electrónica, Sistemas e Informática

**MAESTRÍA EN DISEÑO ELECTRÓNICO**



## **REPORTE DE FORMACIÓN COMPLEMENTARIA EN ÁREA DE CONCENTRACIÓN EN DISEÑO ELECTRÓNICO DE ALTA FRECUENCIA**

Trabajo recepcional que para obtener el grado de

**MAESTRO EN DISEÑO ELECTRÓNICO**

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# Introduction

Moderns life demands data transfers at all times, from personal computers, smart phones, cars, televisions and many other devices connected over the internet, generating roughly 2.5 quintillion bytes of data per day in 2017. To be able to attend such amount of information, the operation frequencies of many electronic devices are growing exponentially, considering that data should be delivered as fast as possible to meet the requirements of different applications such voice calls, video streaming, driving directions and so on. This enhances the need for specialized professionals to deal with the design of appliances that provide the required support to this demanding industry.

The present reception document includes the summaries of the projects carried out in the subjects of *High Frequency Electronics Design*, *Methods of Simulation of Electronic Circuits* and *Modeling and Design of Circuits Based on Optimization*, which make up the concentration area in high frequency electronic design. Those projects included the analysis of a parallel coupled band-pass filter for WLAN, the study of via stitching to improve signal integrity quality on high performance PCBs and the optimization of a single-stub shunt tuning network using space mapping techniques. The experience acquired when developing each of the practices has been directly applied to real work cases for the design of server boards in both aspects: electrically (schematics and components selection) and physically (PCB design).

In particular, this specialization path covers a design cycle considering that a high frequency design can be developed, properly simulated with appropriate software and even optimized to guarantee its operation under the given specifications. None the less, other classes of this program like PCB design, digital design and analog design with commercial devices strengthen the reached skills.



# 1. Analysis of a Parallel Coupled Band-Pass Filter for WLAN

## 1.1. Introduction

The microwave filter is a two port network which is used to control the frequency response, admitting frequencies within the pass band and rejecting or attenuating them in the stop band of the filter. This project consisted in designing and analyzing a parallel coupled band pass filter operating at 2.4 GHz with a 240 MHz bandwidth, common in the 802.11 standard for WLAN. Its objective is to become familiar with the design methods revised during classes and get certain level of expertise designing from the analytical perspective up to the simulation space.

## 1.2. Background

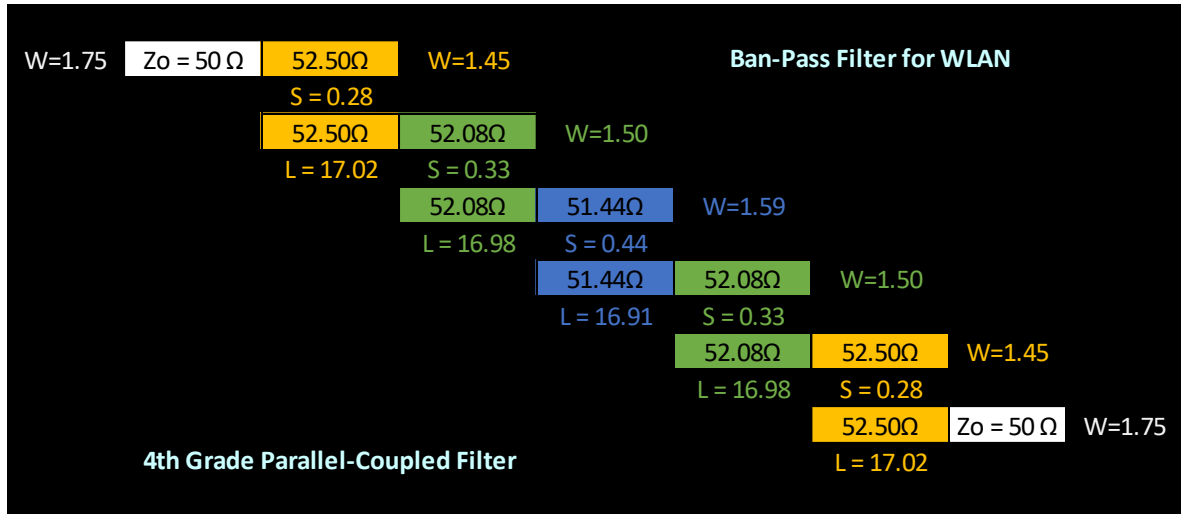
The filter structure consists of open circuited coupled microstrip lines that are quarter wavelength long ( $\lambda/4$ ) and are equivalent to a shunt resonant circuit. The coupling gaps correspond to the admittance inverters in the low-pass prototype circuit. Even-odd mode characteristic impedances of parallel coupled half wave resonators are computed using admittance inverters. These even-odd mode impedances were then used to compute physical dimensions of the filter. Specifications considered microstrip copper traces in a FR4 material and the parameters obtained are summarized in Table I.

**Table I**

$N$	$Z_{odd}$	$Z_{even}$	$Z_0$	$W$	$L$
1	39.36	70.03	52.5	1.45	17.02
2	39.9	67.98	52.08	1.5	16.98
3	40.98	64.58	51.44	1.59	16.91
4	39.9	67.98	52.08	1.5	16.98
5	39.36	70.03	52.5	1.45	17.02

# 1. ANALYSIS OF A PARALLEL COUPLED BAND-PASS FILTER FOR WLAN

The result constitutes a five coupled pairs that placed together form a 4th grade filter with a layout defined as in figure 1-1.



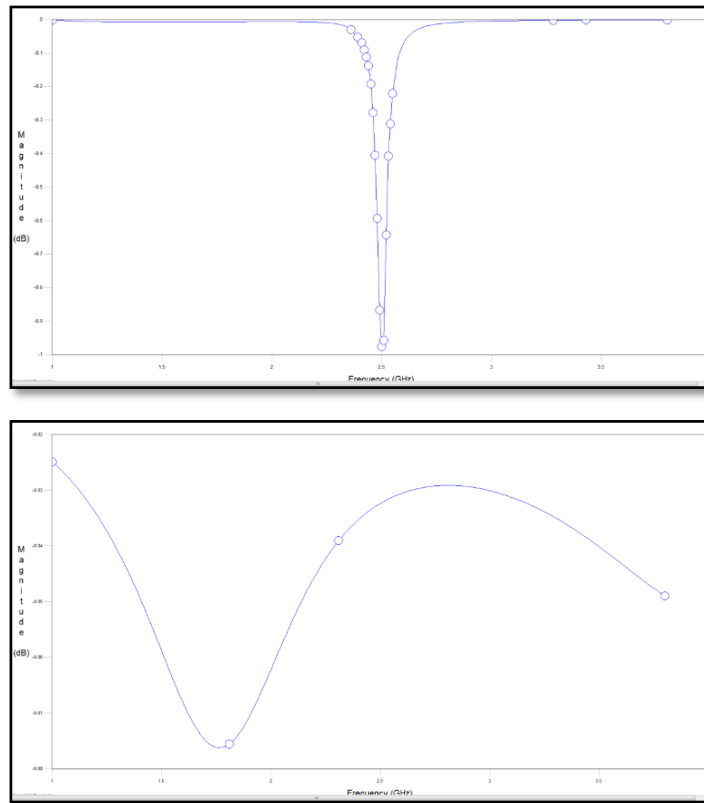
**Figure 1-1** Parallel coupled microstrip band filter for 2.4 GHz.

Since under the same specifications, the number of poles in Butterworth filters it is more elevated than Chebyshev filters, the second filter option was selected for practical implementation reasons, considering that the number of elements required to build it will be significantly lower.

## 1.3. Results

When setting up the simulation it is possible to ignore some effects as the losses of the material, in which case the results trend to be more precise but inexact when taken to real world or when a stricter set of parameters is considered. The simulation of the filter using a basic setup, matches the 2.4 GHz frequency as expected, but when adding losses and a more robust simulation set up the response moved drastically to the left to approximately 1.6 GHz as shown in the bottom of figure 1-2.

## 1. ANALYSIS OF A PARALLEL COUPLED BAND-PASS FILTER FOR WLAN



**Figure 1-2** Filter response with lossless material in top and lossy material in bottom.

### 1.4. Conclusions

Even when the initial design works under some parameters and considerations, the final result can be different if the initial assumptions and requirements are not well defined and/or considered in the design process. This highlights the importance of analyzing simulation results, verifying that the outcome responds as expected and that significant effects are adequately contemplated. Personally, the experience acquired during the course and particularly during the project developed, enhances the importance of understanding not only the design requirements and the tools used to create it but also the environment that it will be submitted to as part of a bigger system. This practice would highlight assumptions that must be consider in order to deliver better designs with less prototypes, which can be traduced in quicker developments and cost reductions.



## **2. Via Stitching to Improve Signal Integrity Quality on High Performance PCBs**

### **2.1. Introduction**

Via hole transitions are the major contributors to signal degradation in PCB interconnections, the higher the frequency of the signal the higher the signal deterioration. There are many considerations to mitigate such undesired effects, like selecting better materials which will add more cost to the systems or choosing wisely the layers of routing to minimize via stubs, but via stitching is one of the most common manner to alleviate the problem. However, in modern PCB designs the real state is highly demanded to accommodate all elements required to make the system work in form factors that are normally too tight. Then an optimal position on the stitching vias is crucial to avoid over designs or even worst under designs. The intention of this analysis is to better understand the stitching vias effects depending on the distance from the signal via.

### **2.2. Background**

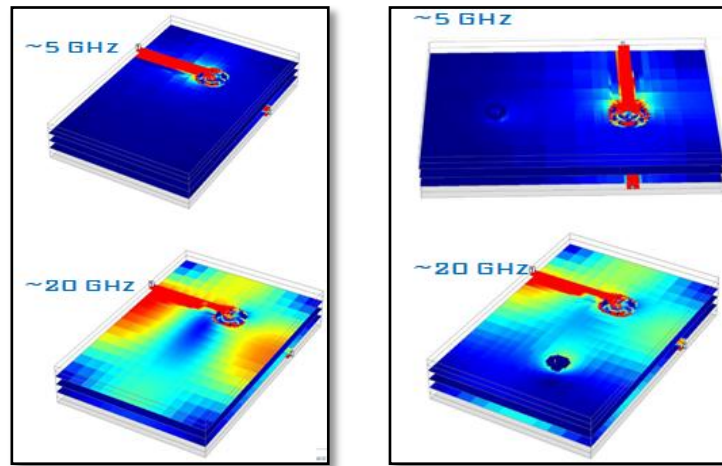
A stitching via is used to tie together larger copper areas on different layers, creating a strong vertical connection through the board structure, helping to maintain a low impedance and short return loops.

The study has considered a frequency swept from 5 to 20 GHz with a single stitching via initially located 400 mils away from the signal via. Then it will move closer to the signal via to up to 200, 100 and 50 mils. The effects on each case are mean to be analyzed to be able to conclude where those vias are worth in a design.

## 2. VIA STITCHING TO IMPROVE SIGNAL INTEGRITY QUALITY ON HIGH PERFORMANCE

### 2.3. Results

The graphs of the different tests evidently shows how the via provides a continuous return path, but their effect varies from distance to distance.



**Figure 2-1** Signal via with no stitching via is shown on the left and with a stitching via located 100 mils away is shown on the right.

Table II summarizes results of each of the cases, detailing the magnitude in dB for the different frequencies, considering 5, 10, 15 and 20 GHz. Numbers in different color indicate the closest case (signal via distance) that meets the  $\lambda/8$  rule for each frequency.

**Table II**

SV Distance (mils)	$S_{21}$ at 5 GHz (dB)	$S_{21}$ at 10 GHz (dB)	$S_{21}$ at 15 GHz (dB)	$S_{21}$ at 20 GHz (dB)
NA	-2.5	-3.1	-1	-10.5
400	-2.4	-3	-1	-8.2
200	-2.2	-2.8	-0.8	-15
100	-2.1	-2.6	-0.6	-9
50	-2	-2.5	-0.5	-8

## 2. VIA STITCHING TO IMPROVE SIGNAL INTEGRITY QUALITY ON HIGH PERFORMANCE

### 2.4. Conclusions

Stitching vias need to be placed close to signal vias, the closer the better, without exceeding  $c$ . This aligns with the practical and common approach that states that if the ground vias spaces from  $1/8$  or less of the wavelength of the signal of interest, the ground plane will look like a solid ground. When stitching vias are placed far away from the signal via, in this case over the  $\lambda/8$ , they may represent a miss usage of board real estate that do not help to improve signal quality since it will not provide a continuous return path.

The addition of grounding vias in very crowded designs with vague design guidelines like "as close as possible" becomes an issue if initially considerations are not made. Having a better approach of how this rule can be practically implemented helps to make the right decision for each case. Besides the described case, in the topic of *Methods of Simulation of Electronic Circuits*, the study of statistical analysis like Monte-Carlo and yield, are tools highly used in the industry that add value to the design process due to its data contributions that predicts the behavior of the system by considering tolerances, ensuring a robust customer ready design.

### 3. Optimization of a Single-Stub Shunt Tuning Network Through Space Mapping

#### 3.1. Introduction

This work shows the optimization of a single stub shunt tuning network on a transmission line using space mapping (Figure 3-1). This is a simple synthetic problem that has been used to illustrate the benefits of using a space-mapping approach over other techniques like direct optimization algorithms.

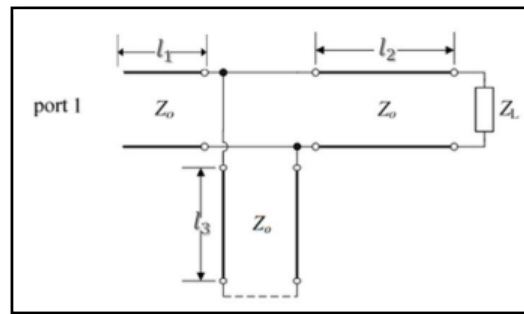


Figure 3-1 Single stub shunt tuning network layout.

#### 3.2. Background

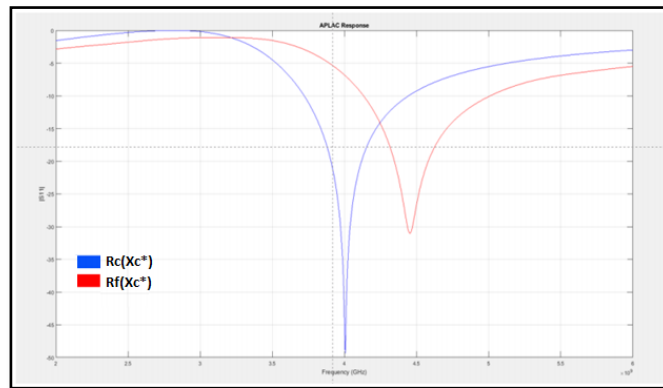
The transmission line described in figure 3-1, must match a load impedance ( $Z_L$ ) that consist of 0.8 pf in parallel with 73 ohms, considering a characteristic impedance of 50 ohms and a operation frequency of 4GHz. In one hand, the coarse model will use ideal and lossless transmission lines and will start from an optimized point that satisfies the requirements of the design (3-1). On the other hand, the fine model uses lossy microstrips equivalent circuits.

$$xc = [100 \text{ mm} \ 0.99 \text{ mm} \ 13.11 \text{ mm}] \quad (3-1)$$

For this case the Broyden-based input space-mapping algorithm will be used to find a suitable solution.

### 3. OPTIMIZATION OF A SINGLE-STUB SHUNT TUNING NETWORK THROUGH SPACE MAPPING

Initial response, obtained when using  $X_c^*$  at the coarse and the fine model is shown in figure 3-2. It is noted how the coarse model provides an exact response at 4GHz (blue line), while the fine model response deviates from the target (red line).

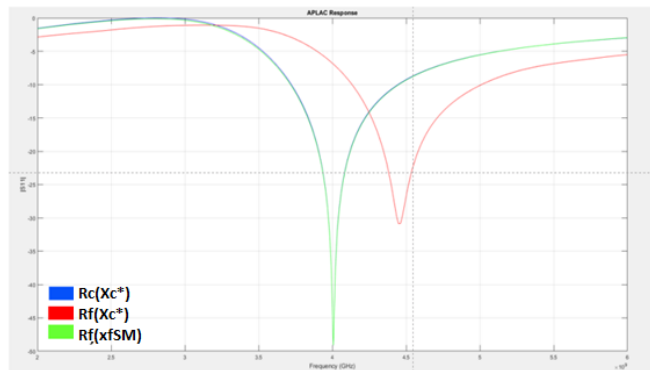


3-1 Coarse and fine models response on the initial design.

### 3.3. Results

After 22 iterations from the initial design the new variable values found a better response when using the fine model that follow closely the response of the coarse model (3-2) represented by the green line in figure 3-3.

$$\mathbf{R}_f(\mathbf{x}^{fSM}) = [1 \text{ mm } 1 \text{ mm } 15.0072 \text{ mm}] \quad (3-2)$$



3-3 Optimized response.

### 3. OPTIMIZATION OF A SINGLE-STUB SHUNT TUNING NETWORK THROUGH SPACE MAPPING

#### 3.4. Conclusions

Based on the responses obtained, it is clear that just few evaluations using the fine model are needed to achieve the desired response, reducing significantly the computing power required to run heavy simulations that may take days to get completed. For this specific case, the number of iterations may reduce if the feeding line is not included as one variable because it is not really a design variable and can be selected arbitrarily. However, since it got included, its value was modified on the final response compensating part of the losses.

For this case, Broyden algorithm contemplated three cases to stop: when a solution is found, when the relative change in the optimization variable is small enough and when the maximum number of iterations is reached:

$$\| f(x_{i+1}) \|_{\infty} < \varepsilon_f \quad \vee \quad \| x_{i+1} - x_i \|_2 < \varepsilon_x (\| x_i \|_2 + \varepsilon_x) \quad \vee \quad i > i_{max}$$

Although, the study case is focused on the space mapping technique, there are other topics that are being exploited in professional applications like parameter extraction, to obtain recipes of a driver in a particular channel (transmission lines with some specific characteristics) and neural networks that are getting used in the ascendant marked of the artificial intelligence, also known as AI. Those advanced topics complement the formation of resources that need to apply more advanced techniques to stay in sync and respond to the demands of the every time more accelerated electronics industry in any of its wide segments.

## 4. Conclusions

Summarize the learnings and describe the experiences of the last years in a single page, it is a challenging task. Five years back, I remember my interview to get accepted into the program, there was one question that I would like to retake now, it was: Why I was interested in the electronic design masters studies plan?. My reason was that I wanted to keep building a solid technical formation in electronic design, complement it with skills on the product development, technological entrepreneurship, businesses plans and a set of personal attributes need to succeed as professional and as person. Today, I can proudly say that the objective has been met. During this time, I have developed a stronger capacity for the design and development of innovating electronics systems with a business perspective, integration, experimentation and an integral view to address technological problems in multidisciplinary teams.

The three described projects in the present document are probe of the acquired knowledge on the concentration area in high frequency electronic design. The same and other principles on this field have been incorporated in my professional career developing server systems that not only represent a technical challenge but also a social compromise to rise up the design standards to take care and minimize the negative impact to the environment by efficiently using energy, and selecting and promoting the usage of more friendly materials but always keeping the percepts of global business like schedule, cost quality of products.

This has been a great endeavor that will constitute a strength pillar in my personal and professional life.

# Appendix





## **A. ANALYSIS OF A PARALLEL COUPLED BAND-PASS FILTER FOR WLAN**

### **Introduction**

Nowadays the operation frequency of modern systems is increasing exponentially. Therefore, the technologies used in the day to day require more complex systems which in turn challenging the design techniques to create in series manufacturable systems, balancing their performance and cost. One of the most exploited wireless technology is the WLAN (Wireless Local Area Network), connecting to internet, millions of people around the world every day. Computers, tablets, smart phones, televisions and even refrigerators are connected to the net providing a modern life style. Key parts on these complex systems are the filters designed to either transmit or receive data through the endpoints, particularly to the known operation frequency of 2.4 GHz that covers the popular standard 802.11.

This study presents a band-pass filter operating at a center frequency of 2.4 GHz with 240 MHz of bandwidth. It will be designed and simulated only. Since the micro-strip filters are considered as one of the important components for a Local Area Network, many different designs can be found in both academic studies and the industry, however our objective is to become familiar with the design methods presented in class, and get certain level of expertise designing from the analytical perspective to the simulation (unfortunately there is no chance to fabricate the design and correlate data). Optimization processes are out of the scope of the work.

### **Theoretical Analysis**

From the basic design parameters mentioned previously, we can list the following:

- Filter Type = Band-Pass
- $f_c = 2.4$  GHz
- BW = 240 MHz
- $f_1 = 2.28$  GHz
- $f_2 = 2.52$  GHz
- 0.5 dB Ripple
- FR4
- $\epsilon_r = 4.7$
- Loss Target=0.021
- H=1mm
- T=0.01m

It is known that under the same specifications, the number of poles in Butterworth filters is more elevated than Chebyshev filters, this means that the order of the filters is more elevated. This fact leads us to select the Chebyshev type for practical implementation reasons, since the number of components required to construct one or the other will be reduced significantly. Thus, we would start with the calculations by obtaining the frequency delta and based on the “g” parameters, which are obtained from the plotting of the normalized frequency versus attenuation, we can calculate the value of the concentrated parts. In order to do all calculations we will use the following scilab script that helps with all the processing. Note that the targeted outcome is a 4th grade filter.

```

// *****//
// Parallel Coupled Filter for WLAN - High Frequency Electronic Design //
// Edgar Abraham Rodriguez Jiménez //
// //
// // December, 2014 //
// *****//

// Defining Project Requirements:
fc =2.4e9; // Central Frequency
f1 =fc-120e6; // Low Frequency
f2 =fc+120e6; // High Frequency
Zo =50; // Characteristic Impedance
N = 4; // Filter Grade

// FR4 physical characteristics and PCB parameters definitions:
Er = 4.7; // Relative permittivity
lt = 0.021 // Loss Tangent
H = 0.001; // Dielectric thickness specified in meters
T = 0.00001; // Trace thickness specified in meters

// First Set of calculations:
D = (f2-f1)/fc;
iat = (f2/fc)-1;
Wo = sqrt((2*pi*f1)*(2*pi*f2));
Vp = 3e8/sqrt(Er);

// Defining column vectors to store values/results
J_N = zeros(5,1);
ZO_N = zeros(5,1);
ZE_N = zeros(5,1);

// For a 4th order Chebyshev Filter, the g parameters are:
g0 = 1;
g1 = 1.6703;
g2 = 1.1926;
g3 = 2.3661;
g4 = 0.8419;
g5 = 1.9841;

```

```
// Transforming the low pass filter to band pass filter //
```

```
// Parallel Components
```

```
L1=(Zo*D)/(Wo*g1);  
C1=g1/(Zo*Wo*D);
```

```
L3=(Zo*D)/(Wo*g3);  
C3=g3/(Zo*Wo*D);
```

```
L5=(Zo*D)/(Wo*g5);  
C5=g5/(Zo*Wo*D);
```

```
// Serial Components
```

```
L2=(Zo*g2)/(Wo*D);  
C2=D/(Zo*Wo*g2);
```

```
L4=(Zo*g4)/(Wo*D);  
C4=D/(Zo*Wo*g4);
```

```
// Odd and Even Z characteristics calculations:
```

```
J_N(1,:) = (1/Zo)*sqrt((%pi*D)/(2*g0*g1));  
J_N(2,:) = (1/Zo)*sqrt((%pi*D)/(2*g1*g2));  
J_N(3,:) = (1/Zo)*sqrt((%pi*D)/(2*g2*g3));  
J_N(4,:) = (1/Zo)*sqrt((%pi*D)/(2*g3*g4));  
J_N(5,:) = (1/Zo)*sqrt((%pi*D)/(2*g4*g5));
```

```
ZO_N(1,:) = Zo*(1-(Zo*J_N(1))+((Zo*J_N(1))^2));  
ZO_N(2,:) = Zo*(1-(Zo*J_N(2))+((Zo*J_N(2))^2));  
ZO_N(3,:) = Zo*(1-(Zo*J_N(3))+((Zo*J_N(3))^2));  
ZO_N(4,:) = Zo*(1-(Zo*J_N(4))+((Zo*J_N(4))^2));  
ZO_N(5,:) = Zo*(1-(Zo*J_N(5))+((Zo*J_N(5))^2));
```

```
ZE_N(1,:) = Zo*(1+(Zo*J_N(1))+((Zo*J_N(1))^2));  
ZE_N(2,:) = Zo*(1+(Zo*J_N(2))+((Zo*J_N(2))^2));  
ZE_N(3,:) = Zo*(1+(Zo*J_N(3))+((Zo*J_N(3))^2));  
ZE_N(4,:) = Zo*(1+(Zo*J_N(4))+((Zo*J_N(4))^2));  
ZE_N(5,:) = Zo*(1+(Zo*J_N(5))+((Zo*J_N(5))^2));
```

```
// Displaying Results
```

```
disp("WLAN BAND-PASS FILTER");  
disp("L1 = "+string(L1));  
disp("C1 = "+string(C1));  
disp("L2 = "+string(L2));  
disp("C2 = "+string(C2));  
disp("L3 = "+string(L3));  
disp("C3 = "+string(C3));  
disp("L4 = "+string(L4));  
disp("C4 = "+string(C4));  
disp("L5 = "+string(L5));  
disp("C5 = "+string(C5));  
disp("Zodd = "+string(ZO_N));  
disp("Zeven = "+string(ZE_N));
```

Found results are shown below:

```
Scilab 5.5.1 Console
-->exec('G:\Proyecto\WLAN_Filter.sce', -1)

WLAN BAND-PASS FILTER

Concentrate Components Topology:

-- Z0 -----L2--C2-----L4--C4-----

      |   |       |   |       |   |
      L1  C1      L3  C3      L5  C5
      |   |       |   |       |   |
-----

L1 = 1.988D-10
C1 = 2.218D-11
L2 = 3.959D-08
C2 = 1.113D-13
L3 = 1.403D-10
C3 = 3.142D-11
L4 = 2.795D-08
C4 = 1.577D-13
L5 = 1.673D-10
C5 = 2.635D-11

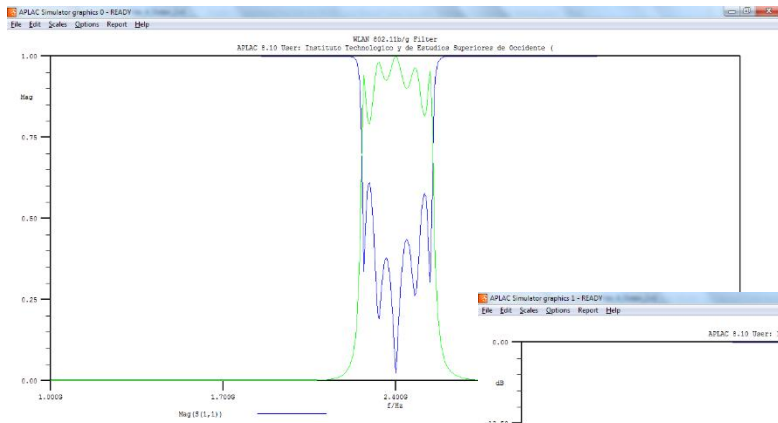
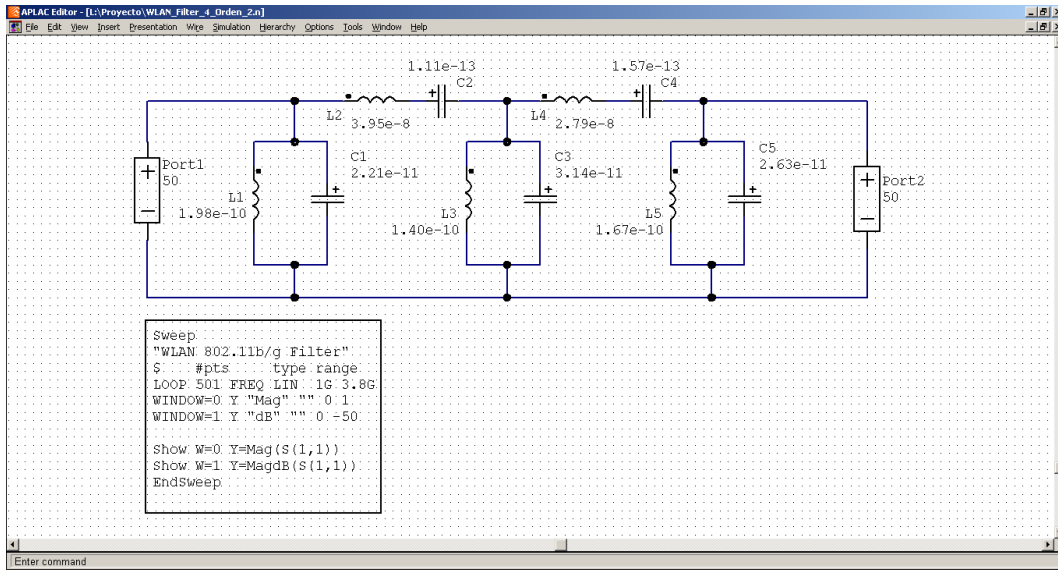
!Zodd = 39.368942 !
!
!Zodd = 39.902174 !
!
!Zodd = 40.986464 !
!
!Zodd = 39.902205 !
!
!Zodd = 39.369144 !

!Zeven = 70.035335 !
!
!Zeven = 67.98335 !
!
!Zeven = 64.580161 !
!
!Zeven = 67.983241 !
!
!Zeven = 70.034492 !

-->
```

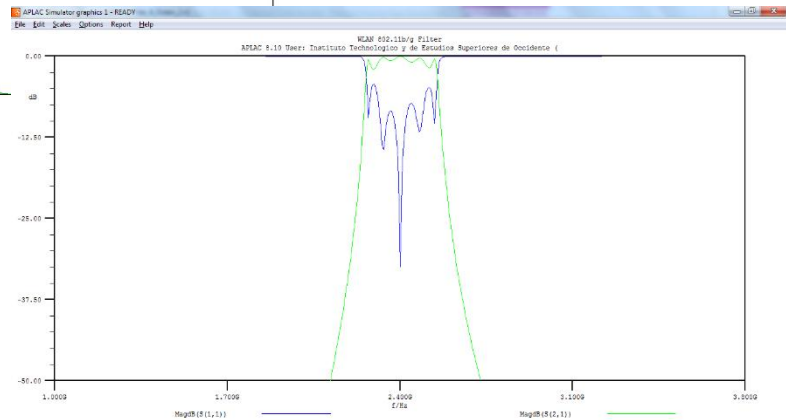
Up to this point we can start simulating the circuit made of concentrated devices only. This will demonstrate that the filter as it was specified is well calculated at this point. It will be simulated from 1GHz to 3.8GHz, plotting  $S_{11}$  in dB and magnitude.

APLAC simulations with concentrated components:



**Mag**

**dB**



Now it is time to define the geometry we will use for our filter. Since the Richardson's and Kouda's transformations do not work as desired due to the low impedance traces needed, we foresee another option: The Parallel-Coupled filter. To properly define the shapes, and spaces, it was necessary to calculate the  $Z_{odd}$  and  $Z_{even}$ , and then considering the results, the characteristic impedance of each coupled trace (Calculus found in the scrip shown before).

Once we reach this point, it is mandatory to think about what material will be used for the filter, depending on the material parameters itself or even on availability and price. For this study, we have decided to use the popular FR-4 with the following physical parameters:

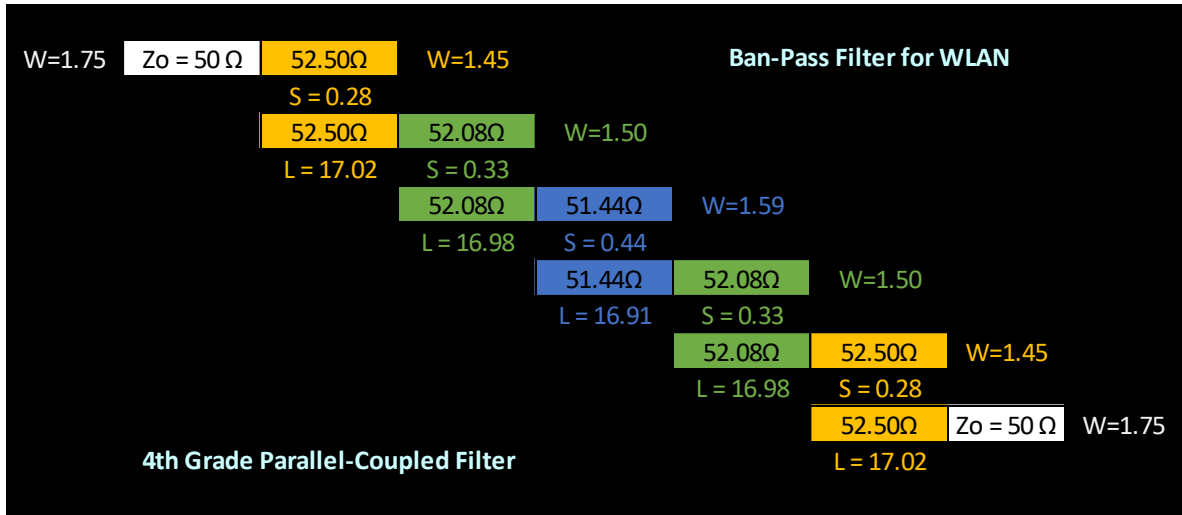
### Rigid FR4 standard PCBs – electrical characteristics

Characteristic	Unit	Value/property/content
Dielectric coefficient ( $\epsilon_r$ )	-	4,7
$\tan \delta$	-	0,021
Volume resistant	$\Omega\text{cm}$	$3,0 \times 10^{13}$
Electric strength	kV/mm	30
Surface resistant	$\Omega$	$2,0 \times 10^{13}$
CTI	V	>175

Whit all the data gotten up to this point, we used a synthesis calculator to define the  $W$  (Width),  $L$  (Length) and  $S$  (Spacing) that will provide the desired response. The table below summarizes the parameters:

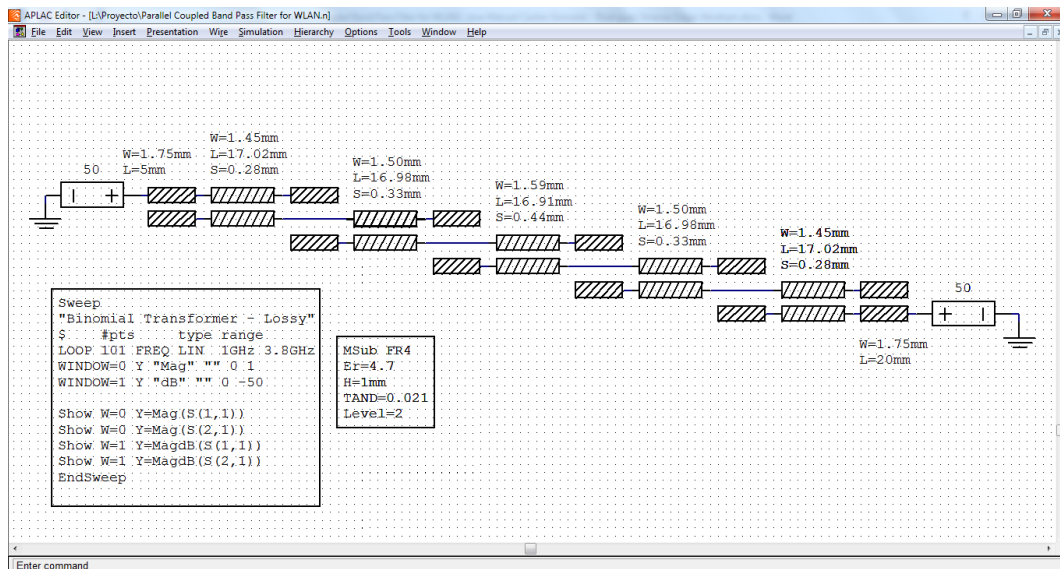
$N$	$Z_{odd}$	$Z_{even}$	$Z_0$	$W$	$L$
1	39.36	70.03	52.5	1.45	17.02
2	39.9	67.98	52.08	1.5	16.98
3	40.98	64.58	51.44	1.59	16.91
4	39.9	67.98	52.08	1.5	16.98
5	39.36	70.03	52.5	1.45	17.02

Finally, the final topology outcome consist of 5 coupled pairs that placed together form a 4th grade filter working at the central frequency of 2.4 GHz and a 240 MHz band-width:

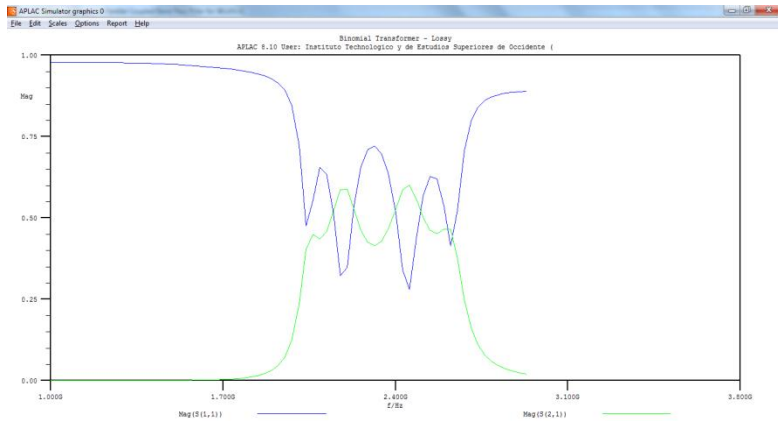


APLAC implementation is demonstrated below using lossy traces, which in reality has a depredated performance compared to the concentrated simulation.

APLAC simulations with concentrated components:

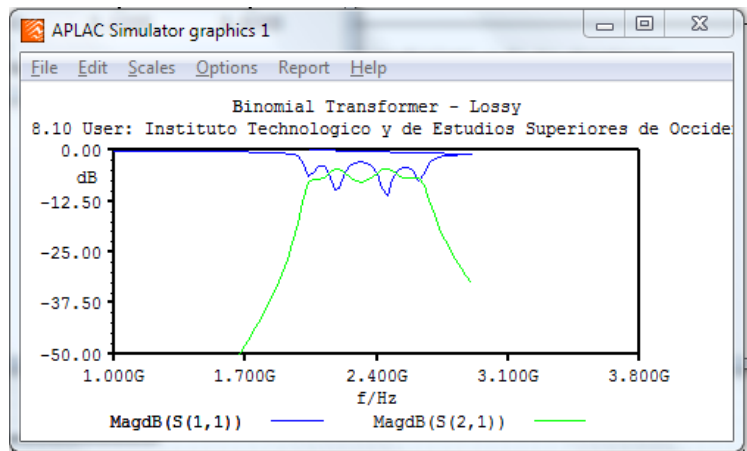




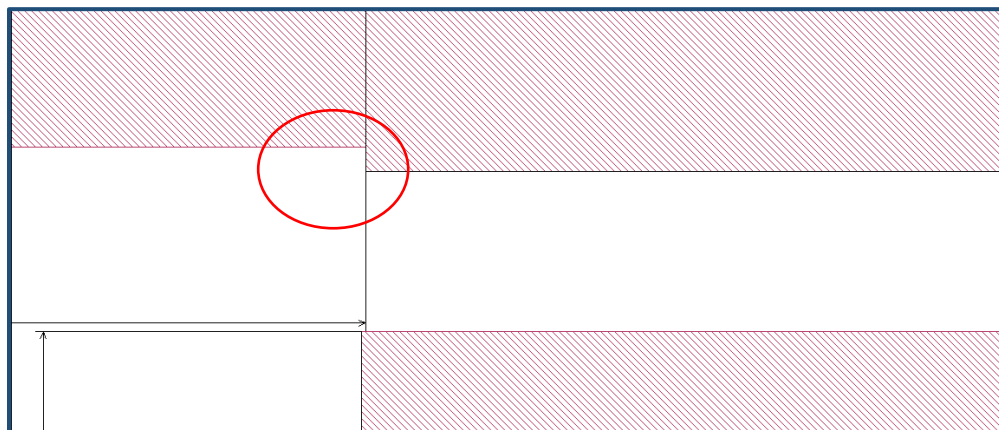


**Mag**

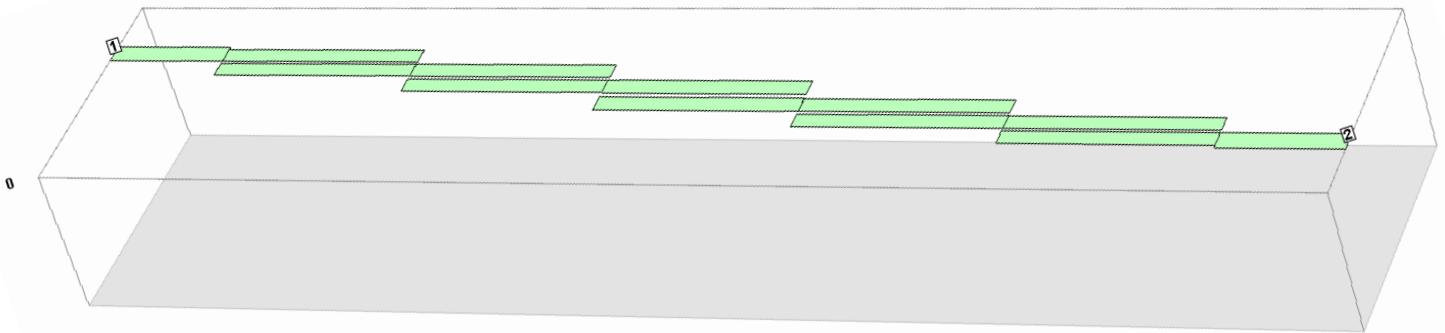
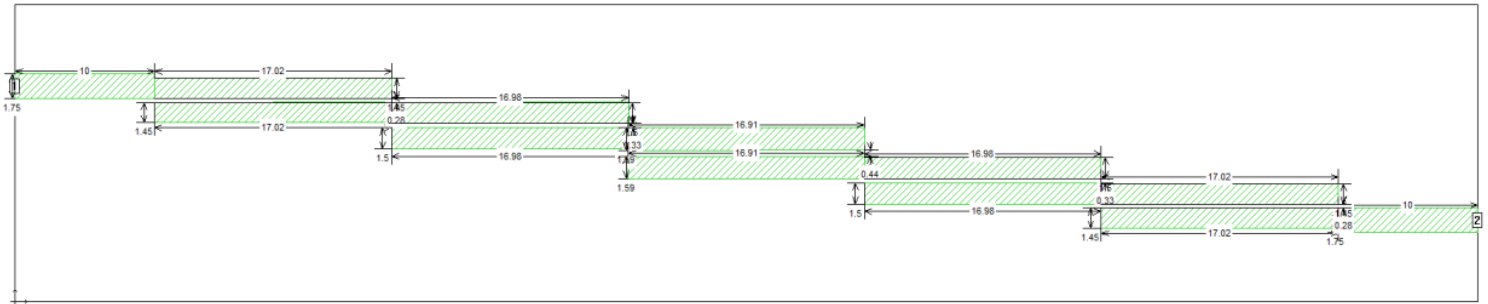
**dB**



Additionally Sonnet simulations were performed to compare against APLAC, to appreciate the effects of the details that APLAC cannot consider as the mismatch in the borders of the joins.



## Sonnet simulations with distributed components:



Box Settings-Parallel Coupled Band Pass Filter for WLAN.son

Sizes

	X	Y	
Cell Size	0.01	0.01	<input type="checkbox"/> Lock
Box Size	104.89	21.2	<input type="checkbox"/> Lock
Num. Cells	10489	2120	<input type="checkbox"/> Lock

Buttons: Set Box Size with Mouse, Cell Size Calculator

---

Dielectric Editor-Parallel Coupled Band Pass Filter for WLAN.son

Select dielectric from library...

Mat. Name: FR-4

Thickness: 1 mm

Specify Using: Conductivity

Anisotropic

Erel	Dielectric Loss Tan	Conductivity [S/m]	Mrel
4.7	0.021	0.0	1.0

Buttons: OK, Cancel, Help

Planar Metal Editor-Parallel Coupled Band Pass Filter for WLAN.son

Planar Metal

Name: Copper

Pattern:

Model: Normal

Usage: For relatively thin metal modeled as a 2D sheet

Specify Using: Conductivity

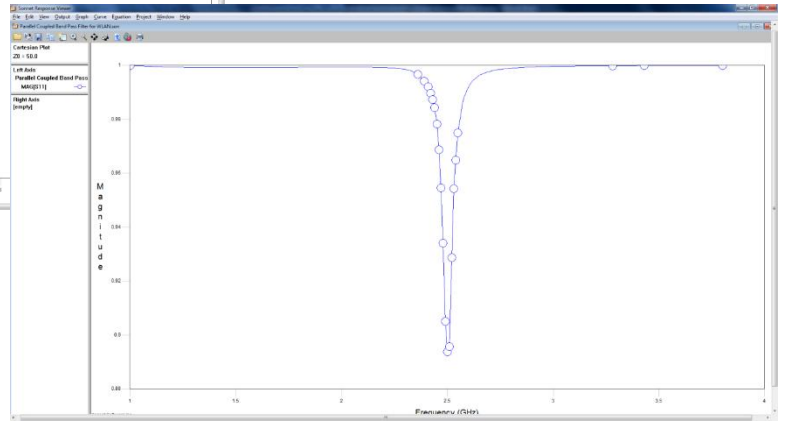
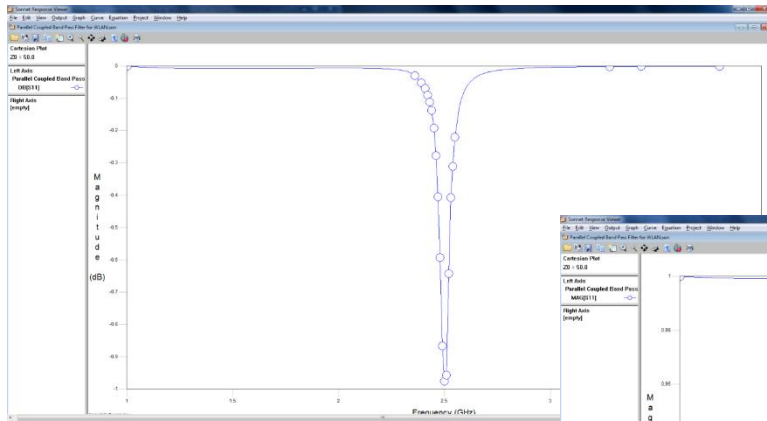
Conductivity: 5.8e7 S/m

Thickness: 0.01 mm

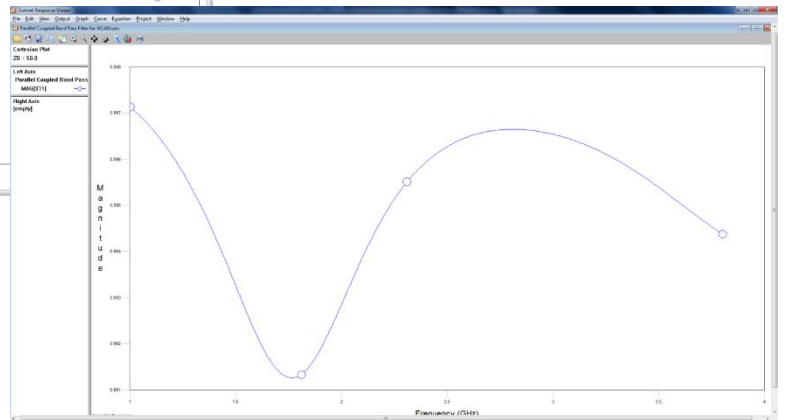
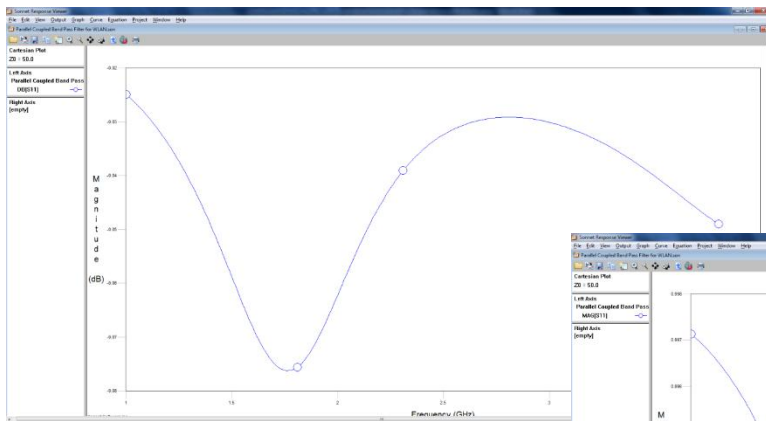
Current Ratio: 0.0

Buttons: OK, Cancel, Help

## Lossless:



## Lossy:



## Conclusions:

As conclusion of the experience we got during this work, we can summarize three main points that we consider as the “key” for a good design:

- Central frequency, band-width and the grade of the resulting filter are essential factor on the design. It may be kind of obvious but it is not when defining the geometry that better suits your design. Mathematically most of the times it is possible to find solutions but not always these solutions are practical. Depending on the application, and the frequencies defined the topology may be totally different, further more if variables as the material, space (real estate), and more are considered for practical and real applications.
- Simulation results and their interpretation. We must never forget that a simulation is just a tool that helps to create a workable design, but it is not a matter of “design and build”. You need to always question your simulation tools and methods and make sure you understand how they work to make accurate decisions not only on the design itself but on the tools and mythologies. Our belief is that time spent during simulations is the part that makes you design successful or unsuccessful.
- Choose wisely, not always the first approach it is the right way to go. Open your mind, eyes and as much books and papers as possible. They will make you learn and understand better. And of course share your own results!

Optimization process will improve filter performance. But for this course it is out of the scope and so for the analysis.

## References

- Sonnet Software, Inc. " APLAC RF Design Tool". Reference Vol. III. Passive RF Components. Version 8.10.
- APLAC Solutions Corporation. Class notes: "Simulation Methods for Electronic Circuits (graduate course)". High-frequency circuit simulation, Full-wave EM simulation.
- Synthesis calculator; [http://wcalc.sourceforge.net/cgi-bin/coupled\\_microstrip.cgi?wc\\_unit\\_menu\\_2\\_0=dB&wc\\_unit\\_menu\\_3\\_0=dB&wc\\_unit\\_menu\\_3\\_1=inch&wc\\_unit\\_menu\\_7\\_0=mil&wc\\_unit\\_menu\\_6\\_0=ns&wc\\_unit\\_menu\\_8\\_0=mil&w=&wc\\_unit\\_menu\\_0\\_0=mm&s=&l=&tmet=0.01&rho=3e-08&wc\\_unit\\_menu\\_4\\_0=Ohm&wc\\_unit\\_menu\\_4\\_1=m&rough=0.001&wc\\_unit\\_menu\\_5\\_0=mil&h=1&es=4.7&tand=0.021&freq=2.4&wc\\_unit\\_menu\\_1\\_0=GHz&analyze=Analyze&stype=evod&Ro=&k=&zeven=70.03&zodd=39.36&elen](http://wcalc.sourceforge.net/cgi-bin/coupled_microstrip.cgi?wc_unit_menu_2_0=dB&wc_unit_menu_3_0=dB&wc_unit_menu_3_1=inch&wc_unit_menu_7_0=mil&wc_unit_menu_6_0=ns&wc_unit_menu_8_0=mil&w=&wc_unit_menu_0_0=mm&s=&l=&tmet=0.01&rho=3e-08&wc_unit_menu_4_0=Ohm&wc_unit_menu_4_1=m&rough=0.001&wc_unit_menu_5_0=mil&h=1&es=4.7&tand=0.021&freq=2.4&wc_unit_menu_1_0=GHz&analyze=Analyze&stype=evod&Ro=&k=&zeven=70.03&zodd=39.36&elen)

## **B. VIA STITCHING TO IMPROVE SIGNAL INTEGRITY QUALITY ON HIGH PERFORMANCE PCBs**

### **Introduction**

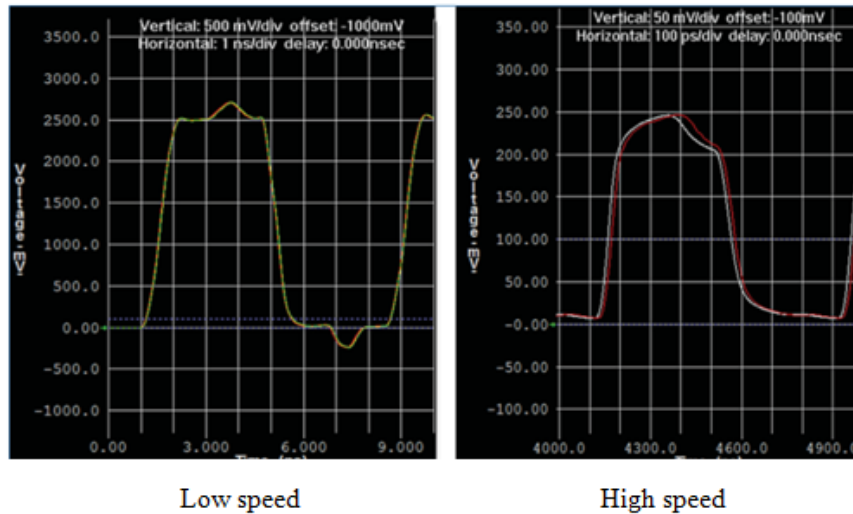
Nowadays the operation frequency of modern systems is increasing exponentially. Therefore, the need of techniques to improve performance, play a key role to reach desirable operational frequencies. For instance, via-hole transitions are the major contributors to signal degradation in PCB interconnections. Via Stitching is the most common manner to mitigate such effects. However, the placement of the vias in relation with the routing is not quite clearly defined. The objective of this work is to understand how the position (distance) and number of stitching vias improves signal integrity, allowing achieving an optimal performance.

Considering that these extra vias take up precious space on board, designers often need to know when stitching vias are absolutely necessary, and when a design still works without using stitching vias. Simulating and understanding the stitching via effect will help make such decisions.

### **Background**

A stitching via is used to tie together larger copper areas on different layers, creating a strong vertical connection through the board structure, helping maintain a low impedance and short return loops.

For low speed signals (more precisely, with longer rise/fall times), via effects are not significant at all, but with faster signal edge rate (rise-fall time is reduced to about 100ps), via causes noticeable delay and signal degradation.



Some designers decide to be on the conservative side and put at least 2 stitching vias around every differential signal via pair that carries signals with data rates over 1Gbps; some do not follow the guideline at all and include no stitching vias for any multi-Gbps signals. Regarding the locations of stitching vias, some designers leave stitching vias wherever there is room for them; while some pay attention to make sure stitching vias are placed in the vicinity of designated signal vias.

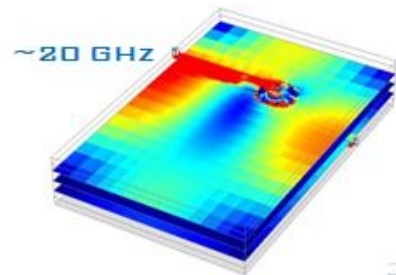
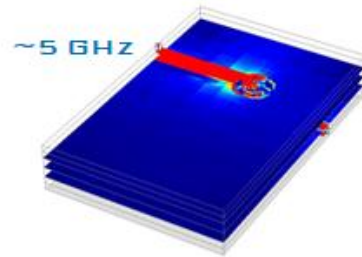
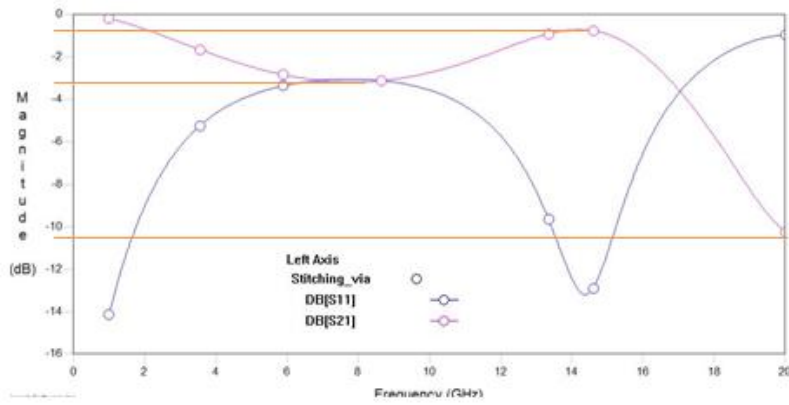
With all these different design practices, some boards are over designed which results in higher product costs, to mention one drawback. To avoid those design problems and maintain cost budget, designers need to understand the effects of stitching vias.

### **Analysis Description**

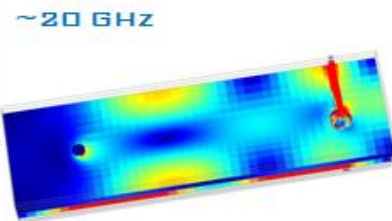
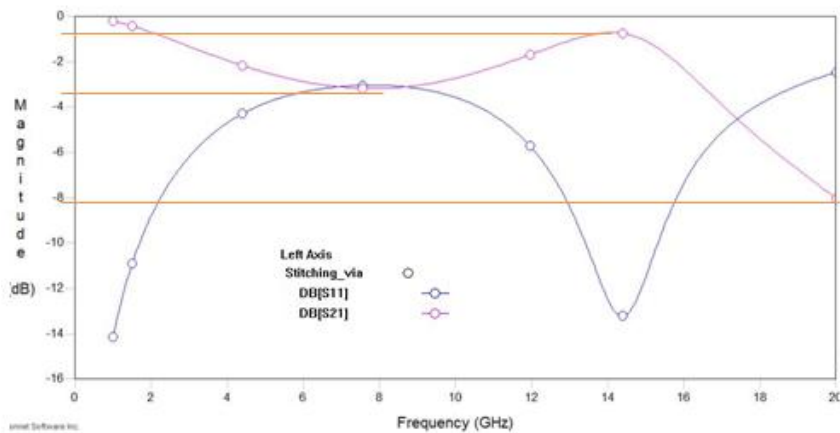
The intention of this project is to understand what are the trade offs when placing grounding vias depending on the signal of interest and the PCB material. The experiment will analyze the effect of a stitching via at different distances from signal vias of 5, 10, 15 and 20 GHz signals.

## Simulation Results

Generic Stack up with no stitching vias:

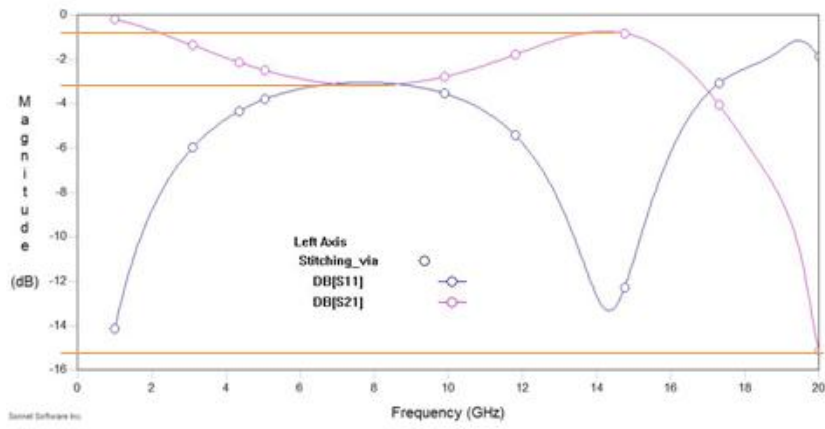


Generic Stack up with stitching vias at 400 mils from signal via:

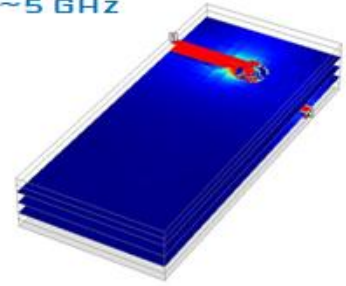




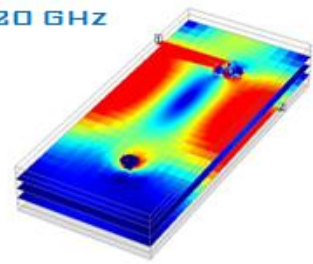
Generic Stack up with stitching vias at 200 mils from signal via:



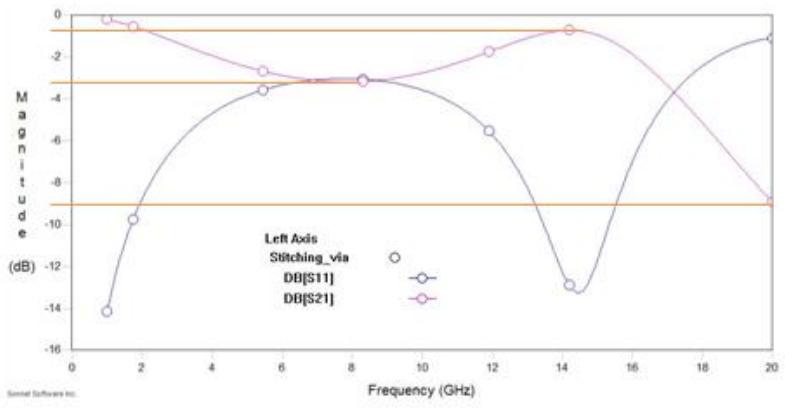
~5 GHz



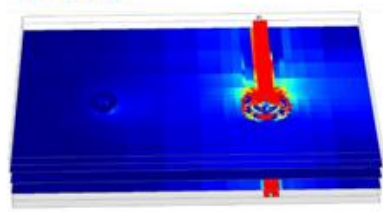
~20 GHz



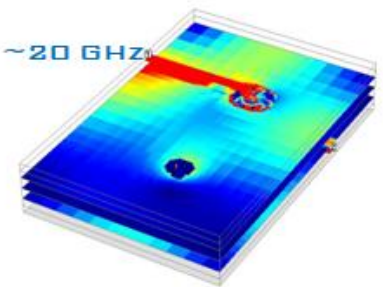
Generic Stack up with stitching vias at 100 mils from signal via:



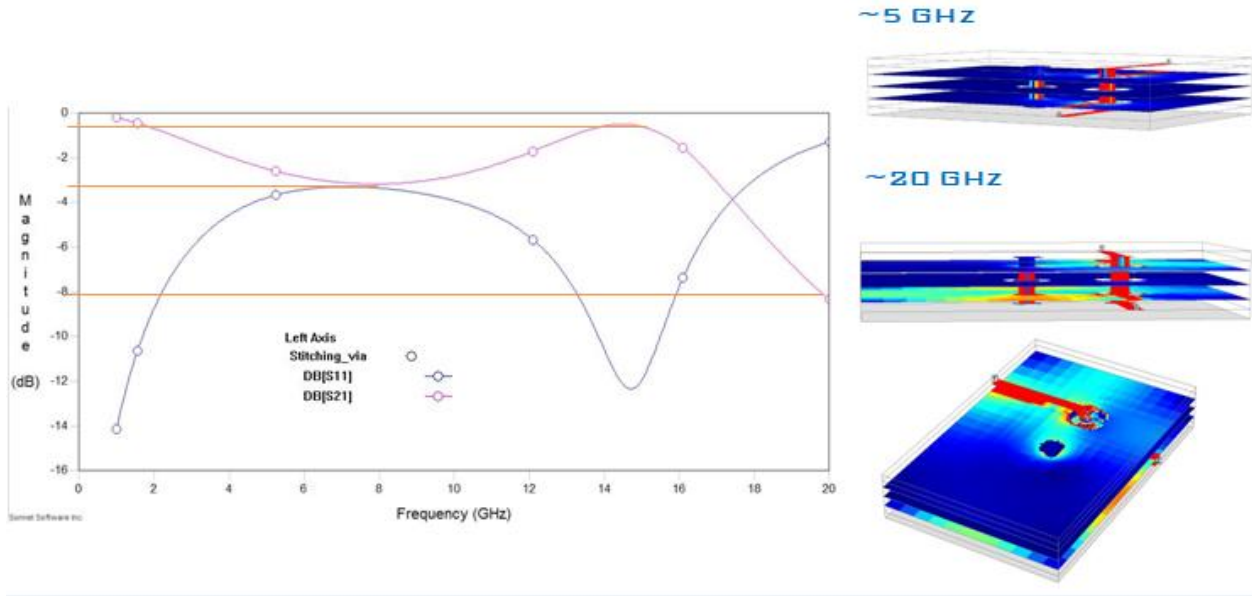
~5 GHz



~20 GHz



Generic Stack up with stitching vias at 50 mils from signal via:



In general, it is observed that stitching vias need to be placed close to the signal vias. Stitching vias far away from the signal vias waste board space and will not help provide a continuous return path. The table below summarizes the results of the simulations for each of the cases:

SV Distance (mils)	$S_{21}$ at 5 GHz (dB)	$S_{21}$ at 10 GHz (dB)	$S_{21}$ at 15 GHz (dB)	$S_{21}$ at 20 GHz (dB)
NA	-2.5	-3.1	-1	-10.5
400	-2.4	-3	-1	-8.2
200	-2.2	-2.8	-0.8	-15
100	-2.1	-2.6	-0.6	-9
50	-2	-2.5	-0.5	-8

## Conclusions

There is a practical and common approach to add grounding vias that says: "If you space your ground vias at  $1/8$  of a wavelength or less your ground plane will look like a solid ground". If this assumption is taken, then the following numbers would apply for each of the cases simulated on this project:

frequency (GHz)	$\lambda$ (m)	$\lambda$ (inches)	$\lambda/8$ (inches)
5	0.028612303	1.126466	0.140808
10	0.014306152	0.563233	0.070404
15	0.009537434	0.375489	0.046936
20	0.007153076	0.281617	0.035202

So, comparing those numbers with what it was obtained from simulations, it can be concluded that:

- Stitching vias need to be placed close to the signal vias, the closer the better without exceeding  $\lambda/8$ .
- Stitching vias far away from the signal vias waste board space and will not help provide continuous return path.

## References

- Understanding Via Effects, Mentor Graphics.  
DR. Zhen Mu.
- Sonnet Software, Inc. " APLAC RF Design Tool". Reference Vol. III. Passive RF Components. Version 8.10.
- APLAC Solutions Corporation. Class notes: "Simulation Methods for Electronic Circuits (graduate course)". High-frequency circuit simulation, Full-wave EM simulation

## C. OPTIMIZATION OF A SINGLE-STUB SHUNT TUNING NETWORK THROUGH SPACE MAPPING

### Introduction

During development of state of the art technologies, high speed signals require special treatment due to their speed increasing. Matching loads is one parameter to take care, using micro strip configurations is a good option to matching loads for high speed signal.

This work shows the optimization of a single stub shunt tuning network on a transmission line using space mapping (Figure 1). This is a simple synthetic problem that will be used to illustrate the benefits of using a space-mapping approach over other techniques like parameter extraction.

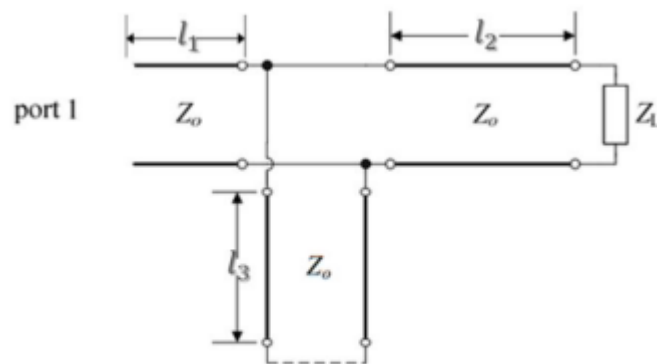


Figure 1

### Optimization Problem

The transmission line described in figure 1, must match a load impedance ( $Z_L$ ) that consist of 0.8 pf in parallel with 73 ohms, considering a characteristic impedance of 50 ohms and a operation frequency of 4GHz.

*Design parameters:*

- $H = 0.25$  mm,  $\epsilon_r = 4.12$  and  $\tan \delta d = 0.01$ .

Coarse model will not consider losses on the transmission line and will start from an optimized point, which satisfies the requirements of the design (figure 2).

$$xc = [100 \text{ mm} \ 0.99 \text{ mm} \ 13.11 \text{ mm}]$$

*Note: Optimized values extractions are explained on "Complementary Information".*

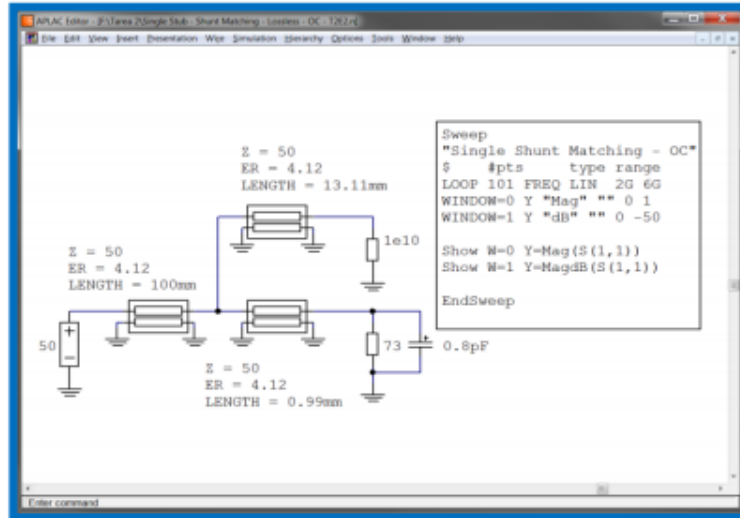


Figure 2

Whereas fine model will take into consideration the losses of the material (Figure 3)

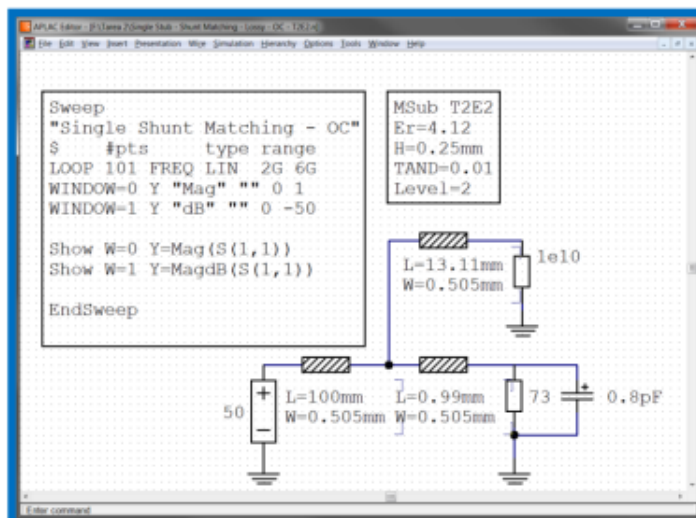
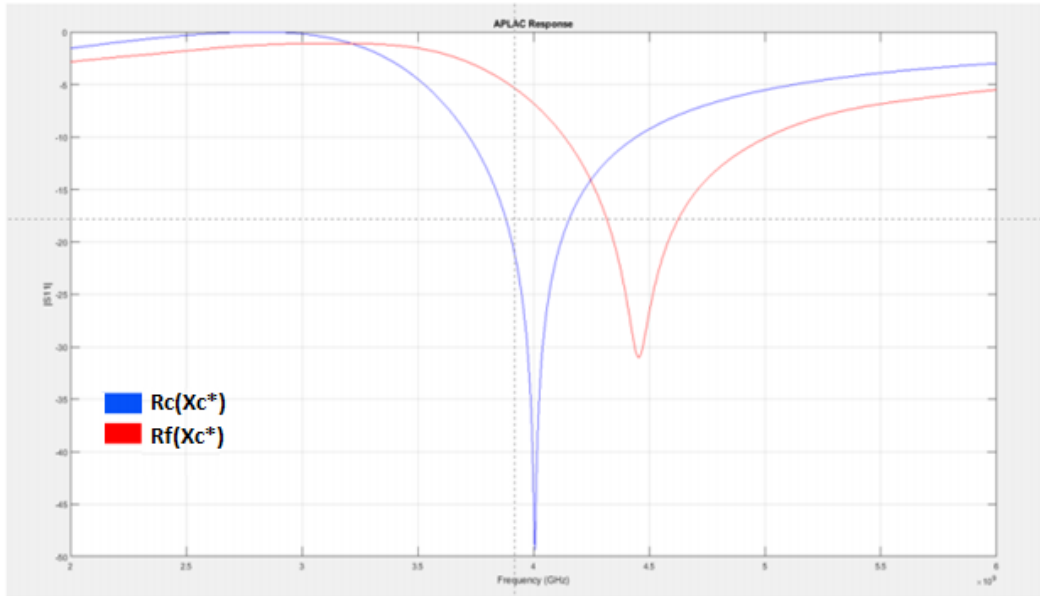


Figure 3

Initial Response using coarse model and fine model is shown in figure 4, in blue is the coarse model which provides the exact response required at 4GHz, whereas in red is the response of fine model is deviated from the expected response. The objective of optimize fine model with Space mapping is to get a  $xf^*$  which response complies the 4GHz on spec.



**Figure 4**

Basic requirements to use Space mapping optimization is having fine model and coarse model, once those models are available,  $xc$  optimized need to be gotten as first step to develop Space mapping.

Current work was optimized using the “Broyden based input space mapping algorithm”, which requires as input the  $xc$  optimized, and get the parameter extraction on coarse model in a cycling routing, once parameter extraction are gotten results of new  $xf$  is evaluated on fine model, to look for the parameters that Fine model needs to get a response of 4Ghz as the coarse model. Figure 5 depicts the flow diagram of the “Broyden based input space mapping algorithm”.

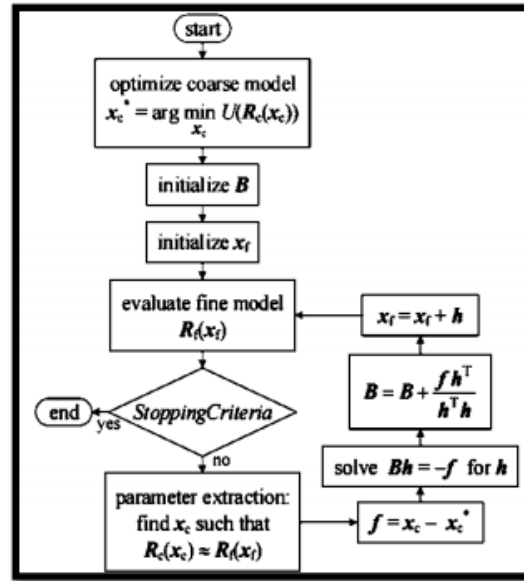


Figure 5

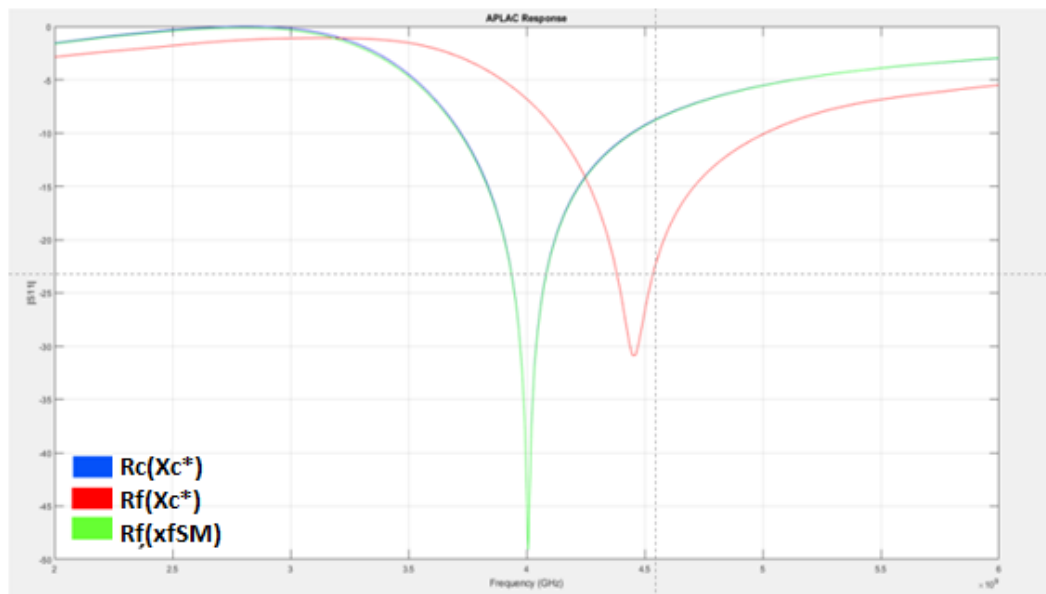
After running “Broyden based input space mapping algorithm”, the gotten results are:

- $x_f^*$  In green, behaves the same as  $x_c^*$  as expected.
- The lengths needed by fine model to comply the specs are:

$$\mathbf{R}_f(x_f^{SM}) = [1 \text{ mm } 1 \text{ mm } 15.0072 \text{ mm}]$$

Number of iterations to find out the  $x_f^*$  were 22.

Next figure shows the comparison among  $x_c^*$ ,  $x_f$  and  $x_f^*$ .



## Conclusions

- Just some evaluations of fine model are needed, this avoid the usage of computing power in excess. Almost all the simulations in APLAC are done with coarse model, which required less time and less computing power than using the fine model.
- During optimization, the response behavior oscillated and took a lot of iterations, this could be for 2 reasons:
  1. Length for input of the shunt tuning network was added as optimization variable, when it could be ignored.
  2. Because normally shunt networks has a 2 optimized solutions, but at the end the algorithm converged to 1 of them.
- Different response is expected if the model is simulated on electromagnetic simulator as Sonnet.

## References

- Space mapping techniques Notes. Dr. José Ernesto Rayas Sánchez
- D. M. Pozar, Microwave Engineering, Wile
- Matlab Help



## Complementary Information

The process to calculate  $x_{c^*}$  is as follows:

Calculating the inductive reactance for the capacitor on the load:

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi * 4x10^9 * 0.8x10^{-12}} \approx 49.735 \Omega$$

And calculate the parallel of the resistor and the capacitor:

$$Z_L = \frac{R_L * (-X_C)}{R_L + (-X_C)} = \frac{73 * (-49.735)}{73 + (-49.735)} \approx 23.143 - 33.968j$$

The Smith chart will be used to find a suitable solution.

Normalizing  $Z_L$ :

$$z_L = \frac{Z_L}{Z_o} = \frac{23.143 - 33.968j}{50} \approx 0.46 - 0.68j$$

From the chart (added at the end) it is observed that two points of the SWR circle intersects the  $1+jb$  perimeter:

$$y_1 = 1 + 1.25j$$

$$y_2 = 1 - 1.25j$$

Then we obtain the distance from the normalized load admittance to both points towards generator:

$$d_1(\text{to } y_1) = 0.170 - 0.143 = 0.027 \lambda \text{ (d}_{\min})$$

$$d_2(\text{to } y_2) = 0.330 - 0.143 = 0.187 \lambda$$

Thus, two solutions will be discovered for the minimum distance ( $d_1$ ), one for open and one for short circuit. For open we move from the left side of the smith chart to the point marked as L1, resulting:

$$l_{oc} = 0.358\lambda$$

To simulate in APLAC the results, it is necessary to transform to millimeters  $d_{min}$ ,  $\ell_{OC}$ :

$$v_p = \frac{c}{\sqrt{\epsilon_r}} = \frac{3 \times 10^8}{\sqrt{4.12}} \approx 147.8 \times 10^6$$

$$\lambda = \frac{v_p}{f} = \frac{147.8 \times 10^6}{4 \times 10^9} \approx 0.0369 \text{ m} \approx 36.9 \text{ mm}$$

$$d_{min} = 0.027 * \lambda \approx 0.99 \text{ mm}$$

$$\ell_{OC} = 0.358 * \lambda = 13.11 \text{ mm}$$

# Smith Chart

