UNIVERSITÉ DE MONTRÉAL

CHARACTERIZATION OF INTERCONNECTION DELAYS IN FPGAS DUE TO SINGLE EVENT UPSETS AND MITIGATION

MOSTAFA DARVISHI

DÉPARTEMENT DE GÉNIE ÉLECRIQUE

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

THÈSE PRÉSENTÉE EN VUE DE L'OBTENTION

DU DIPLÔME DE PHILOSOPHIAE DOCTOR

(GÉNIE ÉLECTRIQUE)

AVRIL 2018

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Cette thèse intitulée :

CHARACTERIZATION OF INTERCONNECTION DELAYS IN FPGAS DUE TO SINGLE EVENT UPSETS AND MITIGATION

présentée par : DARVISHI Mostafa

en vue de l'obtention du diplôme de : Philosophiae Doctor

a été dûment acceptée par le jury d'examen constitué de :

M. SAWAN Mohamad, Ph. D., président

M. AUDET Yves, Ph. D., membre et directeur de recherche

M. BLAQUIÈRE Yves, Ph. D., membre et codirecteur de recherche

M. SAVARIA Yvon, Ph. D., membre

M. AIT MOHAMED Otmane, Ph. D., membre externe

DEDICATION

To my love, Masoumeh

To the loving memory of my parents

To my siblings, Fatemeh & Mahdi

ACKNOWLEDGEMENTS

First and foremost, it is a genuine pleasure, indeed honor, to express my sincere gratitude to my advisors, Professor Yves Audet and Professor Yves Blaquière for their understanding, insightful comments, meticulous scrutiny, enthusiasm and dynamism added considerably to my research experience and made an important part of this dissertation. It has been an honour and pleasure to purse the Ph.D. studies with both of you. This Ph.D. project could not be accomplished without your continuous support and inspiring guidance. I owe you my eternal gratitude for all I have learned from both of you, Thank you!

My sincere thanks go to the members of the examination jury, Professor Mohamad Sawan, Professor Yvon Savaria, and Professor Otmane Ait Mohamed for reading my thesis and providing their invaluable comments. I also would like to express my gratitude to Professor Claude Thibeault at ÉTS for his insightful comments and providing the financial support.

I would like to thank the faculty and staff members of Electrical Engineering Department at Polytechnique Montréal, especially Réjean Lepage and also Jean Bouchard for their technical assistance. My special gratitude extends to Mrs. Nathalie Lévesque for her assistance with all the administrative works. As I always have mentioned : "*Nathalie, vous êtes vraiment comme une maman gentille pour les étudiants de notre département…! Merci à vous*"

At this point, I cannot forget the endless love and care of my late beloved parents who introduced me the joy of reading since the birth. You sacrificed your life to raise me with a true love to reach to this level with your compassion, kindness and unfailing support. Absolutely, you are always alive in my heart and I sense your presence whenever I feel loneliness. There is no day that I never remember you, talk to you and ask you to pray for me! May your gentle souls rest in peace my beloved Mom and Dad! Thank you! I also would like to express my deepest thanks to my beloved siblings, Fatemeh and Mahdi, for their endless love, encouragement, and prayers.

The last, but absolutely not the least, I would like to thank my love, Masoumeh for her extraordinary and unconditional love and kindness who has touched my heart with her lovely eyes! I am very much indebted to her for accompanying me faithfully. She also sacrificed a lot of time to help me transform my scribbling into a readable thesis. Thank you my dear!

RÉSUMÉ

L’utilisation incessante de composants électroniques à géométrie toujours plus faible a engendré de nouveaux défis au fil des ans. Par exemple, des semi-conducteurs à mémoire et à microprocesseur plus avancés sont utilisés dans les systèmes avioniques qui présentent une susceptibilité importante aux phénomènes de rayonnement cosmique. L'une des principales implications des rayons cosmiques, observée principalement dans les satellites en orbite, est l'effet d'événements singuliers (SEE). Le rayonnement atmosphérique suscite plusieurs préoccupations concernant la sécurité et la fiabilité de l'équipement avionique, en particulier pour les systèmes qui impliquent des réseaux de portes programmables (FPGA). Les FPGA à base de cellules de mémoire statique (SRAM) présentent une solution attrayante pour mettre en œuvre des systèmes complexes dans le domaine de l’avionique. Les expériences de rayonnement réalisées sur les FPGA ont dévoilé la vulnérabilité de ces dispositifs contre un type particulier de SEE, à savoir, les événements singuliers de changement d’état (SEU). Un SEU est considérée comme le changement de l'état d'un élément bistable (c'est-à-dire, un bit-flip) dû à l'effet d'un ion, d'un proton ou d’un neutron énergétique. Cet effet est non destructif et peut être corrigé en réécrivant la partie de la SRAM affectée.

Les changements de délai (DC) potentiels dus aux SEU affectant la mémoire de configuration de routage ont été récemment confirmés. Un des objectifs de cette thèse consiste à caractériser plus précisément les DC dans les FPGA causés par les SEU. Les DC observés expérimentalement sont présentés et la modélisation au niveau circuit de ces DC est proposée. Les circuits impliqués dans la propagation du délai sont validés en effectuant une modélisation précise des blocs internes à l'intérieur du FPGA et en exécutant des simulations. Les résultats montrent l’origine des DC qui sont en accord avec les mesures expérimentales de délais. Les modèles proposés au niveau circuit sont, aux meilleures de notre connaissance, le premier travail qui confirme et explique les délais combinatoires dans les FPGA.

La conception d'un circuit moniteur de délai pour la détection des DC a été faite dans la deuxième partie de cette thèse. Ce moniteur permet de détecter un changement de délai sur les sections critiques du circuit et de prévenir les pannes de synchronisation engendrées par les SEU sans utiliser la redondance modulaire triple (TMR). Cette méthode conserve la fonctionnalité du

système en abaissant temporairement la fréquence d'opération pour éviter une panne de délai jusqu'à ce que le bit défectueux responsable ait été corrigé.

La sensibilité aux SEU du réseau d'interconnexions programmable dans un FPGA de la famille Zynq-7000 est validée expérimentalement sous bombardement de neutrons. Une méthode pour configurer une architecture d'oscillateurs en anneau, principalement avec des ressources de routage et un minimum de ressource logique, est proposée. Un contrôle total des ressources de routage permet de cibler les différents types d'interconnexions disponibles dans le FPGA et de créer des oscillateurs dont la fréquence est fixée par la longueur du routage (RO). De plus, un algorithme de routage à travers des matrices de commutation est présenté pour identifier automatiquement les points d'interconnexion programmables associés à une paire d'interconnections. Une configuration expérimentale pour mesurer sans équipement externe les DC sur les différents types de routage dans le FPGA est proposée. Les résultats expérimentaux montrent que la configuration permet de mesurer des DC induits par SEU aussi faible que 8 psec. Il est également démontré que les différents types d'interconnexion présentent différentes durées moyennes avant l'apparition d'un DC.

ABSTRACT

The unrelenting demand for electronic components with ever diminishing feature size have emerged new challenges over the years. Among them, more advanced memory and microprocessor semiconductors are being used in avionic systems that exhibit a substantial susceptibility to cosmic radiation phenomena. One of the main implications of cosmic rays, which was primarily observed in orbiting satellites, is single-event effect (SEE). Atmospheric radiation causes several concerns regarding the safety and reliability of avionics equipment, particularly for systems that involve field programmable gate arrays (FPGA). SRAM-based FPGAs, as an attractive solution to implement systems in aeronautic sector, are very susceptible to SEEs in particular Single Event Upset (SEU). An SEU is considered as the change of the state of a bistable element (i.e., *bit-flip*) due to the effect of an energetic ion or proton. This effect is non-destructive and may be fixed by rewriting the affected part.

Sensitivity evaluation of SRAM-based FPGAs to a physical impact such as potential delay changes (DC) has not been addressed thus far in the literature. DCs induced by SEU can affect the functionality of the logic circuits by disturbing the race condition on critical paths. The objective of this thesis is toward the characterization of DCs in SRAM-based FPGAs due to transient ionizing radiation. The DCs observed experimentally are presented and the circuit-level modeling of those DCs is proposed. Circuits involved in delay propagation are reverse-engineered by performing precise modeling of internal blocks inside the FPGA and executing simulations. The results show the root cause of DCs that are in good agreement with experimental delay measurements. The proposed circuit level models are, to the best of our knowledge, the first work on modeling of combinational delays in FPGAs.

In addition, the design of a delay monitor circuit for DC detection is investigated in the second part of this thesis. This monitor allowed to show experimentally cumulative DCs on interconnects in FPGA. To this end, by avoiding the use of triple modular redundancy (TMR), a mitigation technique for DCs is proposed and the system downtime is minimized. A method is also proposed to decrease the clock frequency after DC detection without interrupting the process.

The susceptibility of the programmable interconnection network in a state-of-the-art Zynq-7000 FPGA family to SEU is experimentally validated. It is known that a bit-flip induced by an SEU in the routing network leads to an undesired bridge between an unrouted interconnect and a live

interconnect. A method to configure architectures mostly with routing resources and minimal logic resources is proposed. A full control over routing resources enables us to employ different interconnections available in the FPGA in order to create routing-based ring oscillators (RO). In addition, a novel algorithm enabling the configuration of routing paths through switch matrices, which automatically identify interconnection points between a pair of interconnections is presented. An experimental setup to measure DCs on the routing resources of an APSoC is proposed. The experimental results show that the proposed setup, requiring no external equipment for DC measurement, is able to measure induced DCs as low as 8 psec. It is also shown that different interconnection types presents different mean time before DC occurrence.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

ADL	Adjustable delay line
APSoC	All programmable system-on-chip
ATGP	Automatic test pattern generator
BIST	Built-in self test
BJT	Bipolar junction transistor
BRAM	Block RAM
CDC	Cumulative delay change
CDC	Cumulative delay change
CEA	Composite electric aircraft
CEU	Code emulating upset
CEU	code emulating upset
CLB	Configurable logic block
CLE	Configurable logic element
CMT	Clock management tile
CRC	Cyclic redundancy check
CSA	Canadian space agency
DC	Delay change
DCM	Digital clock manager
DFS	Depth-first search
DLL	Delay-locked loop
DMR	Dual modular redundancy
DOM	Detection only mode

DRAM	Dynamic random access memory
DSET	Digital SET
DSP	Digital signal processor
DUT	Device/Design under test
ECD	Extra combinational delay
ECD	Extra combinational delay
EDC	Error detection and correction
FPGA	Field programmable gate array
FSM	Finite state machine
GMM	Gaussian mixture model
HDL	Hardware description language
IBIS	Input/output buffer information specification
IC	Integrated circuit
ICAP	Internal configuration access port
IEC	International electrotechnical commission
ILA	Integrated logic analyzer
IMUX	Input multiplexer
IOB	Input/output block
IP	Intellectual property
ISS	Instruction set simulator
ISS	Instruction set simulator
LANSCE	Los Alamos neutron science center
LET	Linear energy transfer
LFSR	Linear feedback shift register

LPC	low-pin-count
LUT	Look-up-table
MBE	Multiple-bit error
MBU	Multiple bit upset
MTTDC	Mean time to delay change
MTTF	Mean time to failure
NoC	Network-on-chip
ODC	Observed delay change
PCORE	Processor core
PDF	Probability density function
PIP	Programmable Interconnection Point
PL	Programmable logic
PLL	Phase-locked loop
PS	Processor system
PUF	Physical unclonable function
PVT	process-voltage-temperature
RO	Ring oscillator
SB	Switch box
SBE	Single-bit error
SBU	Single-bit upset
SCR	Silicon-controlled rectifier
SDC	Single delay change
SEB	Single-event burnout
SED	Single-event disturb

SEDR	Single-event dielectric rupture
SEE	Single-event effect
SEFI	Single-event functional interrupt
SEGR	Single-event gate rupture
SEL	Single-event latchup
SEM	Single-event mitigation
SESB	Single-event snapback
SET	Single-event transient
SEU	Single-event upset
SEUC	SEU controller
SHE	Single hard error
SM	Switch matrix
SoC	System-on-chip
SOI	Silicon-on-insulator
SRAM	Static random access memory
STA	Static timing analyzer
STAR	Self-testing area
SUT	Signal under test
TDC	Time-to-digital converter
TDL	Tapped delay line
TMR	Triple modular redundancy
TPG	Test pattern generator
TRNG	True random number generator
TRNoC	Timing-error-resilient network-on-chip

TSMC	Taiwan semiconductor manufacturing company
VDL	Vernier delay line
WSM	Wilton switch matrix
XDL	Xilinx design language

LIST OF APPENDICES

CHAPTER 1 INTRODUCTION

1.1 Motivation

In the design of electronic systems, cosmic rays with high ionizing radiation levels are problematic challenges. A single charged particle can ionize thousands of electrons and create electronic noise and signal spikes [1]. In the case of digital circuits, this may cause failures or functional errors. CMOS electronic components are especially susceptible to ionizing radiations. This is a critical issue in the design of artificial satellites, airplanes, and mission aircrafts, since they contain a huge amount of electronic modules and components. In order to ensure the proper operation of such systems, integrated circuits (IC) manufacturers make efforts to design ICs and embedded systems which are more robust against cosmic rays.

Another limitation in today's manufacturing industry (especially the spacecraft and aircraft providers using FPGAs) that makes the electronic devices very susceptible to ionizing radiation is technology down scaling. More specifically, as the feature sizes of components reduce, their sensitivity to ionizing radiations increase.

In avionic applications, as the aircraft traffic increases, new flight corridors should be defined at higher altitude that exposes the aircraft to more radiation. At the earth level, most of this radiation is absorbed by the atmosphere. However, on- board control devices are more exposed to radiation and hence the risk of an electronic fault is higher which could be a threat for passengers' safety. The radiation usually generates single-event upset (SEU) by changing the state of a logical bit inside an integrated circuit and creating a soft error. Fortunately, SEUs are hardly destructive and may be fixed or avoided by proper circuit architectures or restoring algorithms.

In this thesis, SEUs occurring in SRAM-based FPGAs are studied due to their wide application range in aircraft electronic systems. The proper operation of an aircraft and its electronic components functionality must be guaranteed in high altitudes against cosmic rays. Therefore, it is of primary importance to develop mitigation techniques to ensure the robustness of FPGAs against ionizing radiations in order to reduce the on-board electronics downtime. In view of this, in collaboration with three industrial partners, i.e., Bombardier Aerospace, MDA Corporation, and Canadian Space Agency (CSA), the concerns on single-event effects (SEE) implications in FPGA-based applications intended for aircrafts travelling at high altitudes, are investigated.

1.2 Background on Radiation Effects

The presence of radiation is one of the effective elements to distinguish the space environment. The natural environment contains lots of electrons and protons that are trapped by planetary magnetic fields. Protons and a very small fraction of heavier nuclei are produced in energetic solar events and cosmic rays within and outside of our galaxy [2]. The cosmic rays consist of approximately 85% protons, 14% alpha particles, and 1% heavy ions, as well as x-ray and gamma-ray radiations. Although, most of these particles are filtered out by atmosphere, they still remain as a primarily concern for spacecrafts and the aircrafts travelling at high altitudes. This makes new challenges in avionic applications and space missions. When a particle beam interacts with materials, the secondary neutrons are created [3]. These neutrons can make a threat to SEEs in electronics. In addition, the protons are significant sources of creating SEEs especially in digital devices and embedded systems. For the charged particles, the amount of energy going into ionization is expressed by the stopping power or linear energy transfer (LET) function, commonly in units of $\mathrm{MeV.cm^2/g}$ or as energy per unit length $(\mathrm{dE/dx})$ in kiloelectronvolts per micrometer [2].

SEE phenomenon has primarily been observed only in orbiting satellites. However, since the beginning of 1980's, by considering new flight corridors at higher altitudes, the SEE was defined as the main radiation concern for the avionics. SEE causes major concerns regarding the reliability and safety of avionic equipments, particularly for those systems that employ SRAM-based FPGAs for control and processing purposes. One particular type of SEE, namely SEU as a soft-error threats the reliability of SRAM-based FPGAs in avionics. As it will be considered throughout this thesis, the static memory cell of the SRAM-based FPGA is very susceptible to SEU. One of the main implications of this susceptibility that is considered in this work is the delay fault that has been thus far neglected in the literature. Following this section, some backgrounds on radiation effects, SEE and SEU implications in digital systems, as well as other phenomena caused by radiation will be drawn.

1.2.1 Radiation Effects on Electronic Devices

Statistical analysis and precise experimental designs in manufacturing companies have shown that the radiation effects are often the main cause of erroneous behavior of electronic

components, i.e., faults. These faults could be ignored in some applications. Though, for high reliability applications, especially in digital designs, it is essential to assess the faults caused by radiation effects. Among the problems in electronic systems caused by SEEs, a type of soft errors, also called SEU, is considered as the main challenge in avionic systems [4].

Although the ICs utilized in avionic systems operate in irradiative environments, they are sensitive to transient faults caused by interaction of ionizing particles with the silicon substrate of electronic components. In general, if a particle has the capability to divide a quite atom into ions, it is considered as an ionizing particle [5].

1.2.2 Single-Event Effect (SEE)

When a high-energy particle passes through a semiconductor, it creates an ionized track behind. This ionization may create a glitch in the output of the circuit or device, a *bit-flip* in the memory or a register, and a destructive latch-up and burnout in high-power transistors [6]. A *bit-flip* is defined as the change of the state of a bistable element, (e.g., a flip-flop or other memory elements) due to the effect of an energetic ion or proton. In designs without latches, it is recommended to employ RC time constant circuits in order to slow down the circuit response time during an SEE occurrence.

An SEE can be destructive or non-destructive. Destructive effects result in catastrophic device failure, while non-destructive effects will cause loss of data and/or control. The main implication of SEE is in the silicon substrate of semiconductor devices. When an ionizing particle strikes the silicon substrate, a nuclear reaction occurs between them caused by charge generation. The charge generated by single non-destructive strikes is collected and will produce a spurious voltage on a sensitive node of the design [2]. The charge can be deposited *directly* or *indirectly* into the material. For example, the neutron strikes will generate the secondary particles such as protons and alpha particles which are charged and may perturb the functionality of a electronic component of the circuit [5].

A single charged particle passes through an electronic component in three main successive steps, namely, the charge deposition by the energetic particle striking the sensitive region, transporting the released charge into the device, and the charge collection in the sensitive region of the device [7]. Figure 1-1 shows the three steps in the case of an energetic charged particle passing through

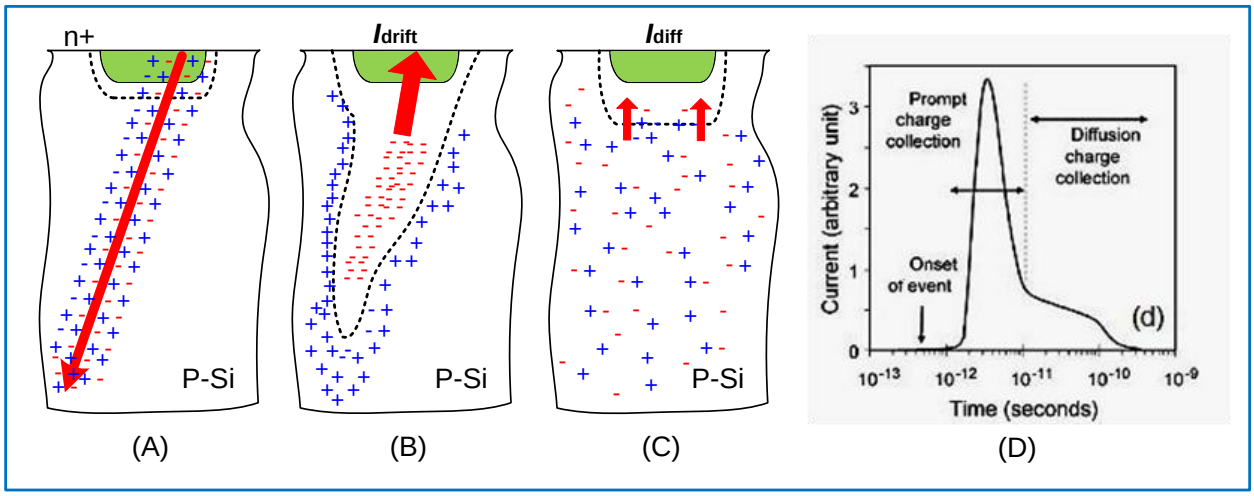


Figure 1-1 : Charge generation (A), collection and transport (B), (C) phases in a reverse-biased junction and the resultant current pulse caused by the passage of a particle (D) [7]

a reverse-biased n^+/p junction [8]. The steps of this mechanism are described in more details in the following.

Charge deposition/generation : When the particle strikes the sensitive region of the inverse biased *p-n* junction, it collides with the crystal lattice of the semiconductor and penetrates to the substrate. Consequently, the ions are generated that transfer a large amount of energy to the electrons of the struck atoms and a cylindrical track of electron-hole pairs with a submicron radius is generated along the particle path (Figure 1-1A).

Charge Collection and transport : When the track of electron-hole pairs is generated in the semiconductor substrate, the released carriers are quickly transported and then collected by elementary structures (e.g., p-n junctions). The charge transport is performed through two mechanisms : *charge drift* in regions with an electric field (Figure 1-1B) and *charge diffusion* in neutral zones (Figure 1-1C) [7]. The transported charges in the device induce a parasitic transient current (Figure 1-1D), which may induce disturbances in the device and associated circuits. If the parasitic current is large enough, it may also induce a permanent damage on gate insulators, such as single-event gate rupture (SEGR) or single-event latch-up (SEL). These phenomena are considered as permanent failures in electronic devices caused by cosmic rays. Depending on the amount of the charge transferred directly or indirectly and its location, the interaction of the

ionizing particles with the silicon substrate of electronic devices may provoke transient or permanent effects to the material as the consequence of particle collision [5].

As mentioned earlier, SEEs could be destructive (hard error, permanent effect) or non-destructive (soft error, transient effect). In the following section, the SEE classification and its related phenomena are briefly discussed.

1.2.3 SEE Classification

In recent years, the use of commercial and non-assessed electronic components with smaller feature sizes has been increased, especially in avionic industry. In view of this and in order to meet the standard requirements in aviation, design engineers have found that different approaches are required to ensure the integrity and reliability of the electronic components used in avionic applications [9]. The International Electrotechnical Commission (IEC) committee has forced the avionic industries to address the key points of reliability during the avionic systems assembly. This committee released the first report in IEC TS 62239 [10] providing a method for electronic components management and introducing the main atmospheric radiation effect on avionics. The SEE effects on avionic electronics was classified in three groups [9], as depicted in Figure 1-2 [11].

- ***Soft Error*** : is a non permanent type of damage, yet may be catastrophic by affecting the circuit functionality. A soft error may create an alteration in the status of a logic value stored in a memory cell, delay the signal transition, or modify the proper functionality of a module. The recovery of the affected part by soft error is possible through reinitializing the device. It is noted that single-event transient (SET) is a type of soft error leading to erroneous data at the output of the system affected by radiation, if not filtered properly. SET sometimes emerges as spikes that may propagate significantly through the circuit. Single-event functional interrupt (SEFI) phenomenon occurs when the radiation modifies a special register's value controlling the device functionality. The temporal loss of intended device functionality is the consequence of SEFI's effect in digital circuits. Single-event disturb (SED) affects the combinational logic and latches in a design that is referred to the momentary corruption of the stored data. SEU itself, defined as changing the state of a logical bit and creating a soft error in Section 1.1, is classified into two

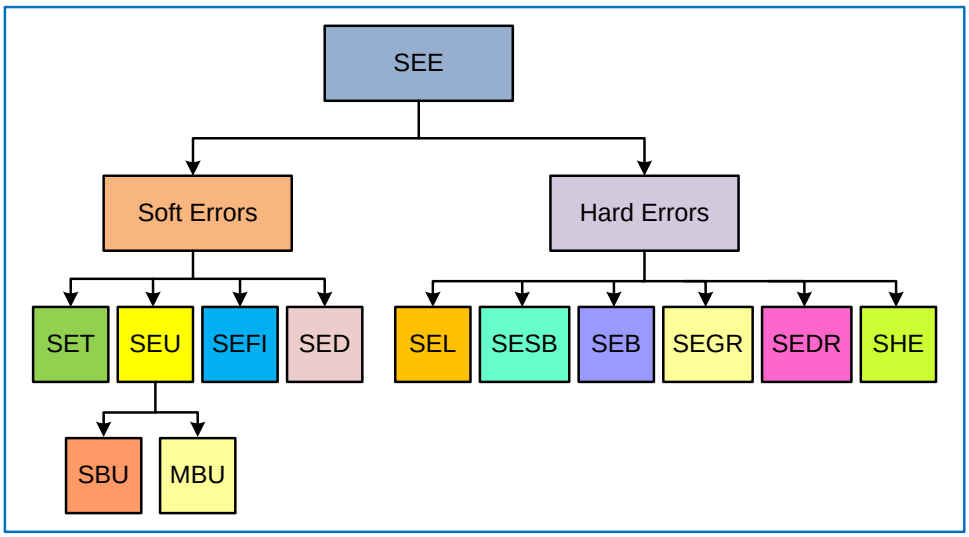


Figure 1-2 : SEE classification [11]

events; single-bit upset (SBU), where the SEU flips only one bit of the memory element; and multiple-bit upset (MBU), where more than one bits are flipped due to the particle striking a shallow angle almost parallel to the silicon surface of the device [11].

- ***Hard Error*** : Hard error occurs when the functionality of the device is permanently lost due to SEE. Stuck bit is an example of this phenomenon that may lead to stuck-at '0' or stuck-at '1'. Single-event latch-up (SEL) is another catastrophic situation that leads to high current flowing during the latch-up and therefore a hard error. Single-event snapback (SESB) leads to local heating of the device and is mostly observed in n-channel MOSFETs and silicon-on-insulator (SOI) transistors operating under high-current condition. Single-event burnout (SEB) is also another example of hard error that occurs in power MOSFETs and high voltage devices. Single-event gate rupture (SEGR) phenomenon occurs when a heavy ion strikes the gate region of the MOS transistor while the gate is biased with a high voltage. Local overheating and eventually destruction of the gate region may occur as a consequence of local breakdown caused by SEGR in MOS devices. Single-event dielectric rupture (SEDR) is similar to SEGR and lead to failure in memory and anti-fuse FPGAs.

Single hard error (SHE) occurs when an energetic heavy ion strikes the gate of the MOS device and permanently affects the electrical parameters of the device [11]. IEC has provided the following considerations for the avionic systems regarding the SEE issue :

- The radiation environment for avionic applications must be confirmed.
- Reliability level of system development must be identified.
- Design of the primarily electronic equipment for SEE must be assessed as :
  - ✓ Identify the sensitivity of electronic components to SEE,
  - ✓ SEE rates for sensitive parts must be quantified,
- Verify that the reliability level requirements for system development are met concerning SEE.
- Perform corrections when necessary.

This thesis focuses mostly on SEU effects, mainly the SBU, in SRAM-based FPGAs creating delay faults that may disturb the functionality of the implemented circuit. In the following section, a brief introduction regarding the SEU phenomenon is presented.

1.2.4 Single-Event Upset (SEU)

SEU is considered as the change of the state of a bistable element, (e.g., a flip-flop or other memory elements) due to the effect of an energetic ion or proton. This effect is non-destructive and may be fixed by rewriting the affected part. The change of the state in the element due to the upset is known as a *bit-flip* and may occur in many electronic devices [2].

Static random access memory (SRAM) and dynamic random access memory (DRAM) are two types of digital memories that are susceptible to SEU. SRAM structures require the continuous power supply in order to maintain the stored bit. An SEU in SRAM modules may easily change the state of the stored bit and generate erroneous data. Since the reshuffling of the SRAM memory modules leads to data loss, a mitigation technique is necessary to keep these memory modules unchanged against SEU. DRAM structure includes some cells that represent data via charge storage in a capacitor. The cells should regularly be refreshed in order to maintain the stored information. An ion strike readily upsets the DRAMs and causes the cell storage error or bit line error.

It is known that very small featured size memory circuits may have MBUs due to ion strikes. This usually occurs when the ion track is close to both bits or the angle of incidence is close to being parallel with the die. It is noted that MBUs are more probable when reducing the size of fabrication technology. In this case, the sensitive nodes of the circuit are closer to each other and also the amount of critical charge (Q_{Crit}) required for creating an upset is smaller. The critical charge is the minimum amount of charge collected by a circuit due to SEU in order to change the state of the circuit. Figure 1-3 depicts MBU, SET and SEU in the combinational and sequential logics associated with ICs [5]. The other types of destructive SEEs are presented in the following section.

1.2.5 Other Destructive Phenomena

SETs are transient voltages at a node in an IC caused by passing a charged particle through the device. Most SETs do not affect the device operation. However, there are several types of SET that can cause catastrophic situations or corrupt data in digital circuits [2]. The phenomenon called SEFI was introduced in 1996 for the first time in EIA/JEDEC standard [12], [13]. A SEFI is a type of SEE that leads to a temporary non- functionality or even an interruption in the normal operation of a circuit. SEFIs are most probably caused by a particle strike, and are not always harmful [2], yet may produce data, control, or functional-interrupt errors [14]. Thus, a complex recovery mechanism is necessary in order to maintain the circuit in its normal operating state.

Stuck bits are another type of permanent failure caused when a bistable element is stuck in one of its two possible states, i.e., stuck-at ‘0’ or stuck-at ‘1’ [15].

CMOS ICs inherently contain parasitic bipolar junction transistors (BJT) created by CMOS structures, which form the n-channel and p-channel transistors (Figure 1-4) [16], [17]. The collector of each parasitic bipolar transistor forms the base of another parasitic device connected in a positive feedback loop. This circuit is equivalent to a four-layer diode device known as a silicon-controlled rectifier (SCR) [17]. It is noted that under normal operation, no current flows through the parasitic base regions. Due to the charge collected from a single-particle energy deposition, if a small amount of current is injected into a base region, the positive feedback may increase the current quickly. It is noted that the current continues to flow within the IC’s power supply pins, i.e., SEL. In this case, a latched chip may permanently be damaged. It is known that SEB phenomenon [18] is similar to SEL. However, it is triggered by heavy ions travelling

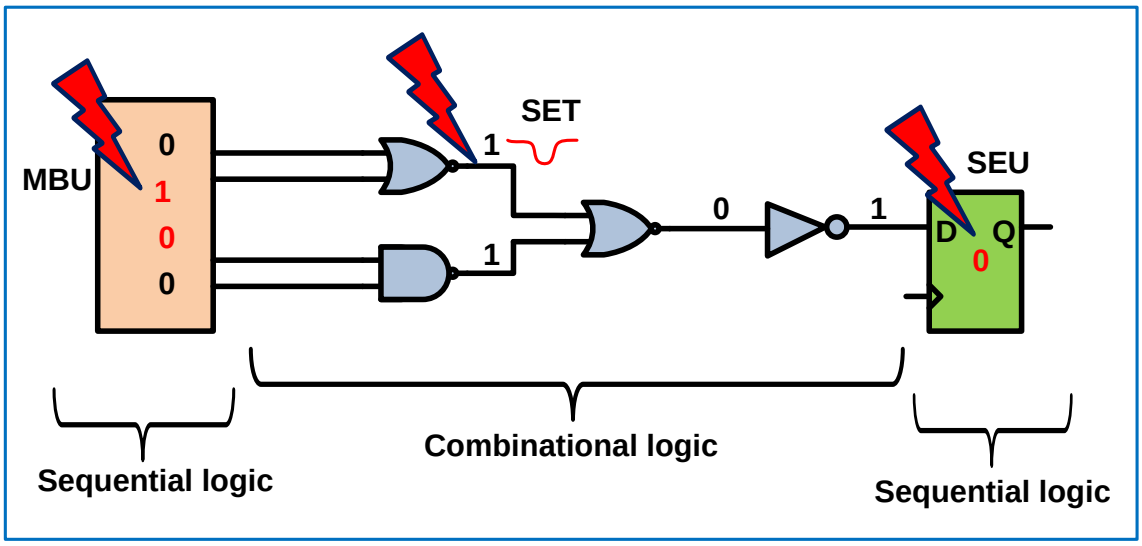


Figure 1-3 : SEU and MBU in the sequential logic and SET in the combinational logic [5]

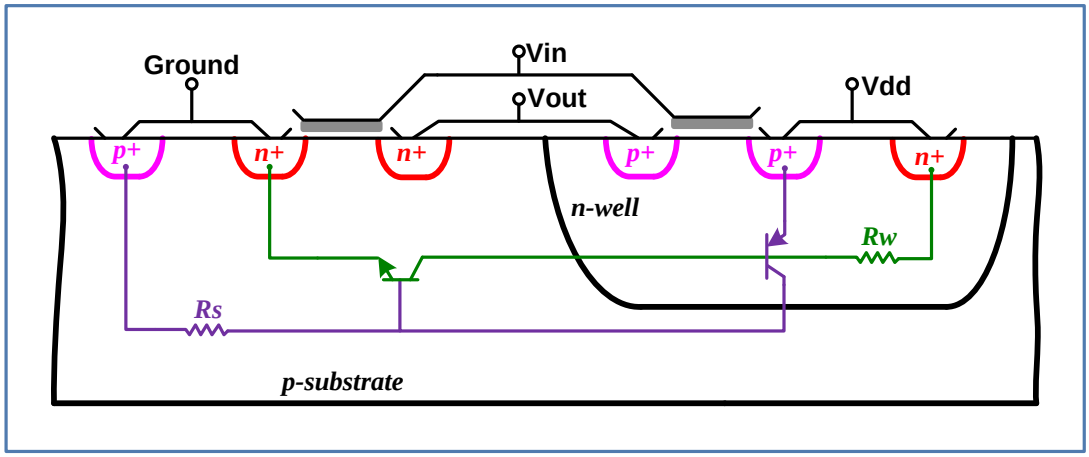


Figure 1-4 : Bulk CMOS inverter architecture cross-section showing the parasitic bipolar SCR structure susceptible to SEL [16], [17]

through the MOSFET [6], [19] and leads to a catastrophic device failure [2]. SEB is a high-current situation in a parasitic n-p-n bipolar structure similar to latch-up.

SEGR phenomenon [20] is generated when the incident particle forms a conduction path in the gate oxide of a MOS transistor resulting in device damages. SEDR may occur when a charge builds up in dielectric region around the gate of a power MOSFET.

In the following section, an introduction to the Xilinx Virtex-5 SRAM-based FPGA which is the core of the experiments and findings in this thesis mainly in CHAPTER 3 and CHAPTER 4 is presented.

1.3 Xilinx Virtex-5 SRAM-Based FPGA

FPGAs are semiconductor devices that are based around an array of configurable logic blocks (CLB) connected via a hierarchy of configurable interconnects [21]. FPGAs have become the preferred common solution to implement digital systems targeting different applications [17]. SRAM-based FPGA comprises some I/O blocks (IOB), memory modules, logic blocks and routing resources controlled by SRAM cells, called configuration bits [21]. It is noted that the main focus of CHAPTER 3 is on the Xilinx Virtex-5 FPGAs. In addition, these FPGAs have been employed by our industrial partners in avionic systems. In view of this, the structure of these devices is now presented.

Virtex-5 FPGA is fabricated based on the 65nm copper technology and contains an array of CLBs that are surrounded by IOBs located on the four sides of the FPGA die. CLBs are building blocks that contain logic elements for implementing gates, flip flops, etc. The communication between the implemented internal circuits with the external world is realized by IOBs. Also, the 36-Kbit BRAMs/FIFOs provide the facility of data storage in synchronous or asynchronous modes. Moreover, the digital signal processor (DSP), phase-locked-loop (PLL), and digital clock manager (DCM) are available user-accessible cores inside the FPGA [22]. Figure 1-5 shows the matrix architecture of Xilinx Virtex-5 FPGA. The XC5VLX50T package provided on the Genesys^{TM} Digilent board contains 28,800 slice registers and look-up tables (LUT), 480 IOBs, 32 buffers, and 6 PLLs/DCMs [23].

1.3.1 Virtex-5 CLB Overview

CLBs in Virtex-5 are some logic resources available in the FPGA fabric for implementing the sequential and combinational logic circuits. In order to access to general routing matrix, each CLB element is coupled with a switch matrix (SM), also called switch box (SB) [24]. The slice structure in Virtex-5 was organized differently as compared to the previous products, e.g., Virtex-4 and downward. In this fabric, each slice comprises of four LUTs and four flip-flops [23].

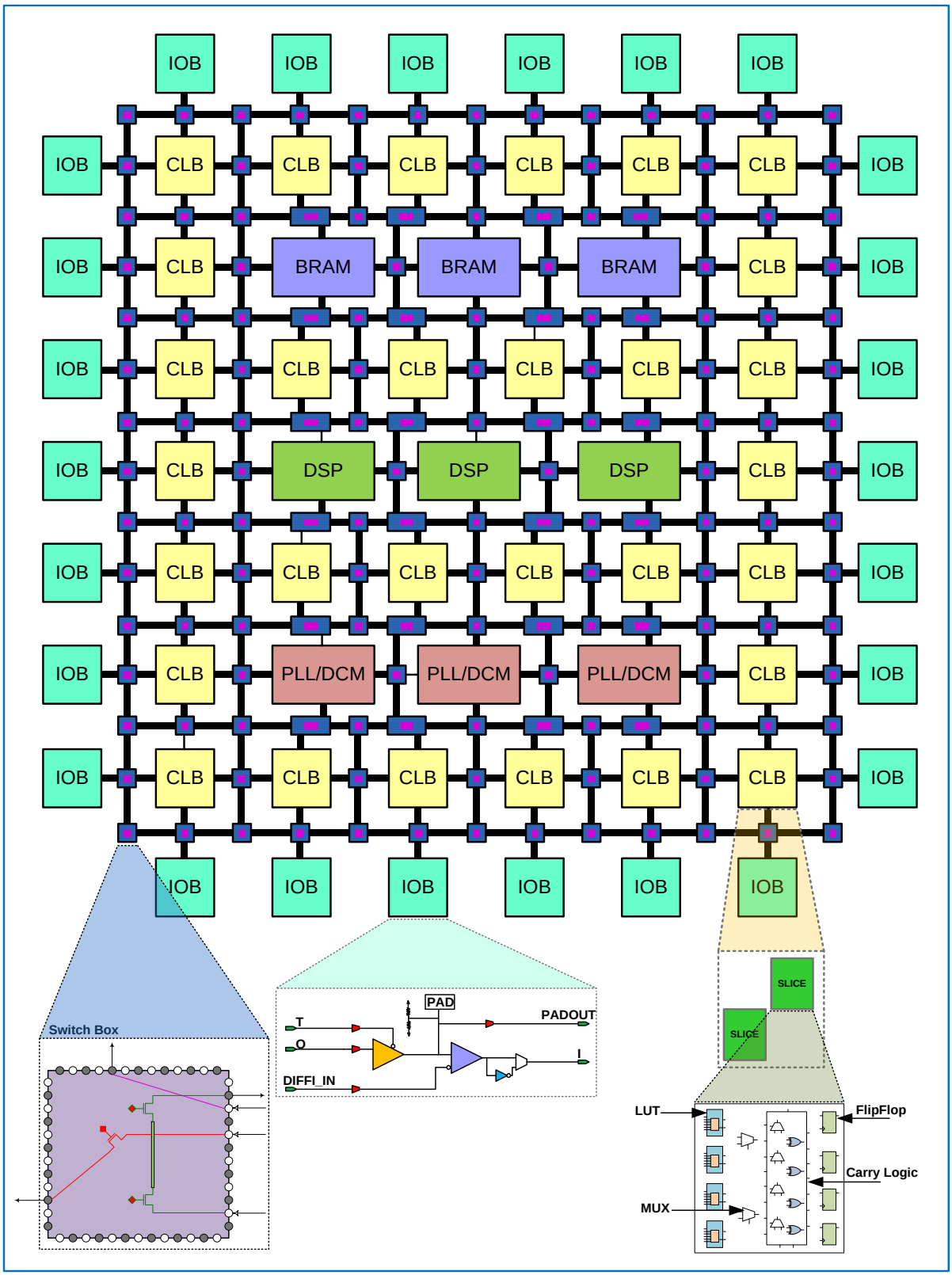


Figure 1-5 : Matrix architecture of Xilinx Virtex-5 FPGA [25], [26]

1.3.2 Virtex-5 Slice Configuration

Each slice in Virtex-5 FPGA contains four LUTs. There are some internal multiplexers intended in each slice to control the connectivity of internal resources. Some logic blocks are dedicated in each slice for implementing arithmetic logics. The detailed slice structure in Virtex-5 FPGA is depicted in Figure 1-6 [24].

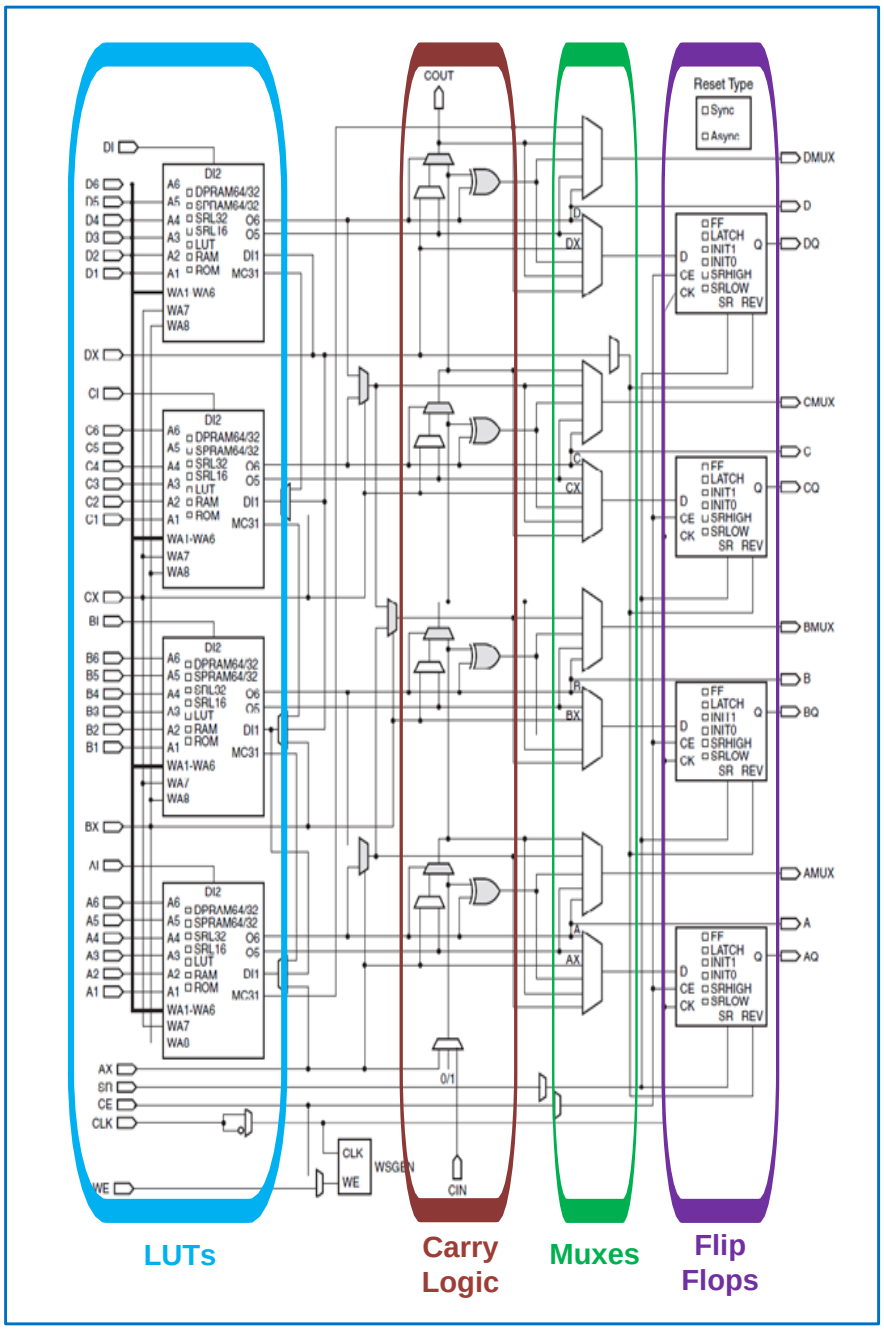


Figure 1-6 : Slice architecture in Xilinx Virtex-5 FPGA [24]

1.3.3 Virtex-5 Interconnection Network

Global routing interconnection network in Virtex-5 FPGA contains the following routing interconnects :

- ***Long interconnects*** : Routing of long interconnects have three connections : *beginning*, *middle*, and *end*. Between the beginning and end, there are five connections into a SM that can source all four directions. The long interconnections span within twenty four rows/columns of components with a SM connection for every six components.
- ***Double interconnects*** : These interconnections span within three rows/columns with a SM connection for each component.
- ***Hex interconnects*** : These interconnections have three connections into a SM and span within six rows/columns [27].

Figure 1-7 shows the interconnection network for a part of a design implemented into Virtex-5 FPGA extracted by Xilinx FPGA Editor Tool [28]. The SM structure is made of some programmable interconnection points (PIP) enabled by a configuration memory cell.

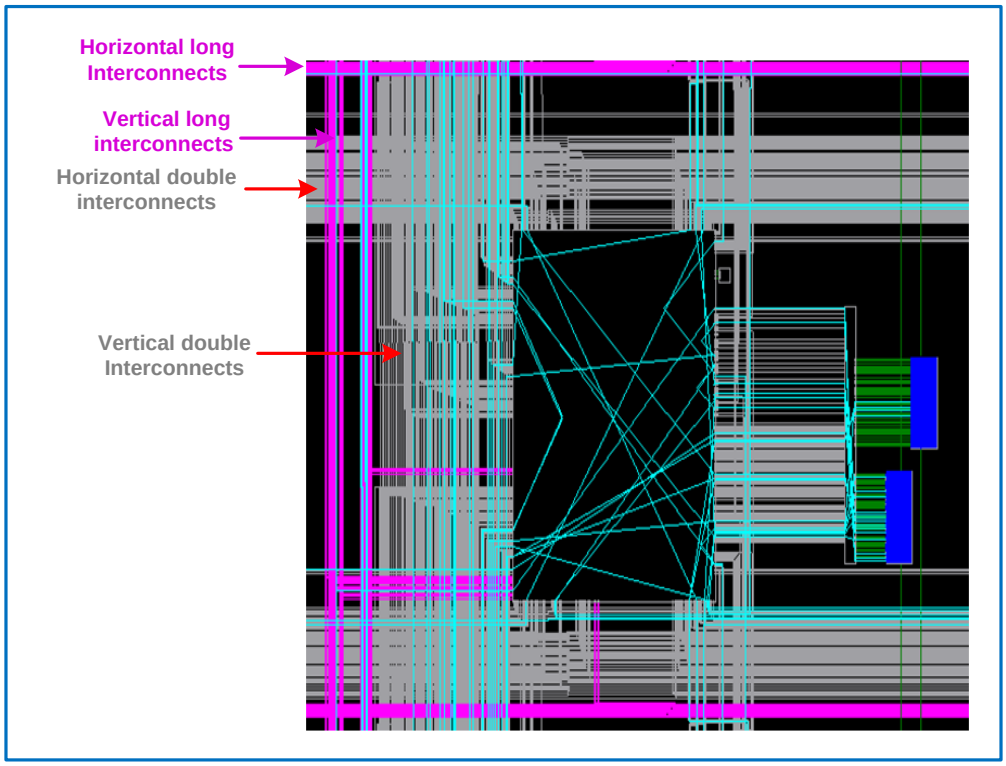


Figure 1-7 : Partial interconnection network in Xilinx Virtex-5 FPGA [28]

1.3.4 SEU Controller Macro

SEU controller macro (SEUC) provided by Xilinx Inc. is available in most Virtex FPGAs that performs two main actions. First, it corrects the configuration upsets caused by SEU once they are detected, i.e., *scrubber*. It then emulates SEUs via a controlled and predictable method by injecting errors into the configuration memory [29]. Thus, the upset evaluation in a design implemented into the FPGA is facilitated [30].

The SEUC occupies less than 4% in Virtex-5 device. Inside the macro, ICAP_Virtex5 and FRAME_ECC_VIRTEX5 primitives are employed in order to check the configuration status while the readback CRC scans (reads) the device. It is noted that the SEUC is susceptible to SEUs, yet may be fixed as the SEUC has the ability to scrub itself [31].

1.4 Fault Models in the SRAM-based FPGA Resources

SEU may lead to fault occurrence in the FPGA resources and malfunction of the circuit. In this section, the fault models for different resources available in SRAM-based FPGAs are discussed.

1.4.1 Fault Model in PIPs

PIPs are the main components in SRAM-based FPGAs that contribute to route a source component to a destination component. A PIP is a pass-transistor linking two interconnections that can either be ‘ON’ or ‘OFF’. PIP failures due to SEU effect are classified as PIP *short* failure, PIP *open* failure and, the most important one, the PIP *parasitic* failure, also called PIP *load* failure. The PIP short failure occurs when an SEU strikes the configuration bit of the PIP that is already ‘OFF’ and links two active interconnections together while they have different functions in the design. On the other hand, PIP open failure occurs when an SEU flips the configuration bit of a PIP that is already ‘ON’ and breaks an interconnection into two parts. This corrupts the data transmission between source and destination points. The PIP parasitic or load failure occurs when an SEU flips the configuration cell of a PIP connecting a live interconnect to an unrouted one. Consequently, a parasitic capacitance is induced to the active interconnect delaying data propagation in the affected routes [32]. Figure 1-8 shows the fault models for a PIP in different scenarios. In Figure 1-8A, the PIP is initially “OFF” and connected between two active interconnects with different functions. Once an SEU flips the configuration bit, PIP switches to “ON” and links two active interconnections together (Figure 1-8B). This

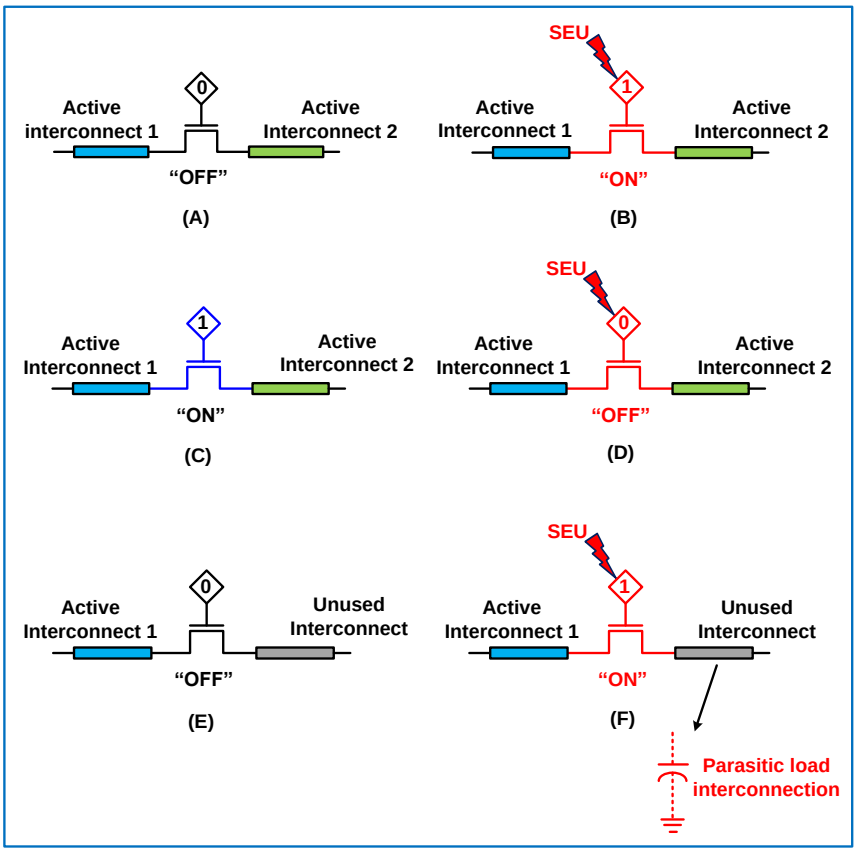


Figure 1-8 : PIP failure models due to an injected SEU [32]

phenomenon is called PIP short and its consequence is the transmission of wrong information due to this undesired connection. In Figure 1-8C, two active interconnections with the same function are connected through a PIP that is "ON". When an SEU flips the configuration bit, the PIP switches to "OFF" and disconnects the data transmission link between two interconnects that is called PIP open (Figure 1-8D). Interruption in the flow of data from *active interconnect* 1 to *active interconnect* 2 is the result of a PIP open failure. Figure 1-8E represents an active interconnect connected to one side of an "OFF" PIP that is linked to an unused interconnect at the other side. Due to SEU injection, the configuration bit is flipped and connects the unused interconnect to the active interconnect (Figure 1-8F). This phenomenon may result in a change of circuit timing due to an additional parasitic load on the active interconnect.

1.4.2 Fault Model in Buffers

Buffers are the components used in most of the FPGA families especially Xilinx Virtex devices. A buffer is a driver which can either be "ON" or "OFF". There are two types of buffers in Virtex

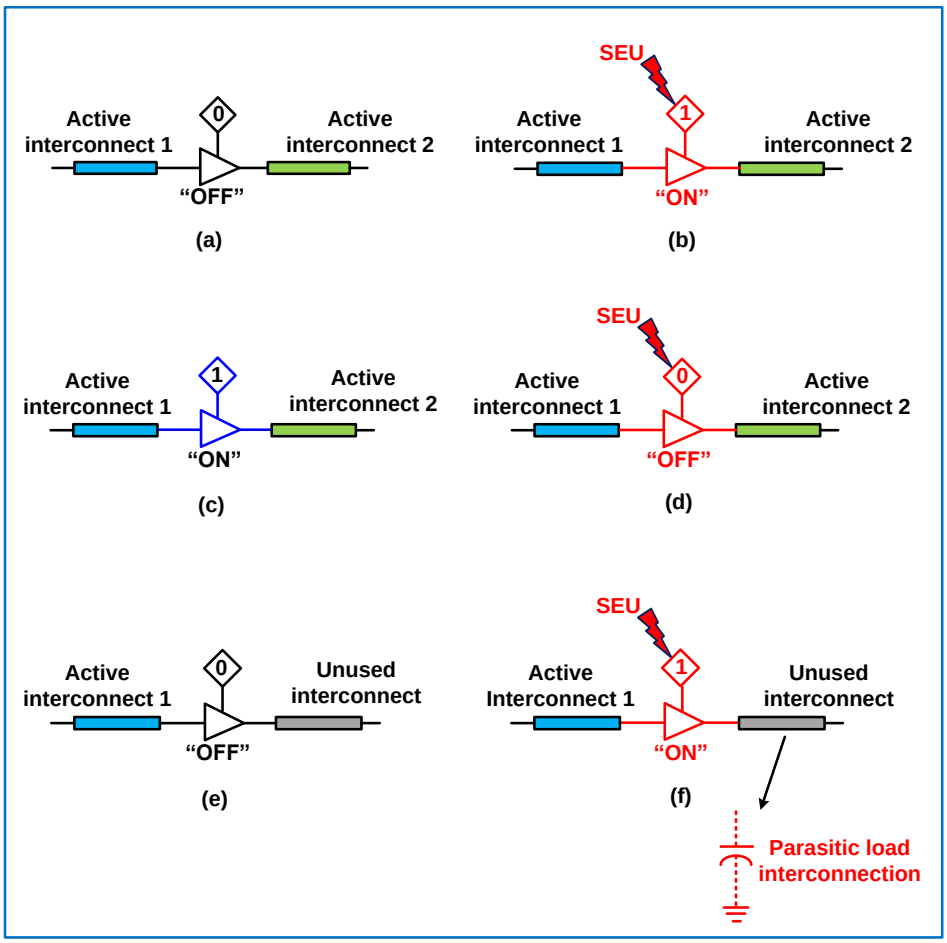


Figure 1-9 : Fault models for buffers due to an injected SEU [33]

FPGAs, namely, global buffers and clock buffers. Global buffers (BUFG) distribute high fanout signals throughout the device and are automatically inserted by Xilinx implementation tool for a targeted design. The other type of buffers, i.e., clock buffers, include clock enabled BUFG (BUFGCE), BUFGDLL, BUFGMUX, BUFGP, BUFCTRL, and BUFGMUX_CTRL. Regional and feature-specific clock buffers are BUFR, BUFIO, and BUFCF that are supported in most of Virtex devices [24]. Figure 1-9 shows the fault models for buffers due to SEU injection. The same models explained for PIP fault in Section 1.4.1 are also valid for fault model in buffers.

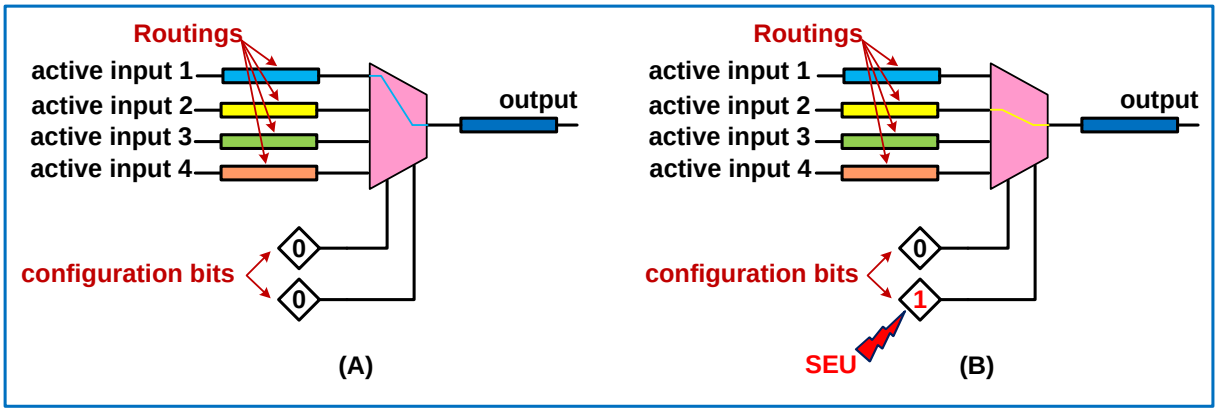


Figure 1-10 : Fault model for multiplexer due to an injected SEU [33]

1.4.3 Fault Model in Multiplexers

A Multiplexer is an *n*-by-1 selectable switch controlled by configuration bits. The single output of the multiplexer is enabled by one of its *n* inputs activated through the control bits. Multiplexers are available in each slice of the most Xilinx Virtex family devices. They contribute in the routing interconnection network. Figure 1-10 shows the existing fault model for a 4-by-1 multiplexer controlled by two configuration bits [33]. In the case of an SBU event, once an SEU flips one of the configuration bits, a different routing configuration is created and the logic behavior of the multiplexer changes. This is called a logic error. The consequence of SEU effect on the multiplexer is the transmission of wrong information through the multiplexer.

1.4.4 Fault Model in LUTs

LUTs are the useful logic resources available in each slice that are utilized as function generators in Virtex FPGAs. Virtex-5 contains four separate LUTs associated with each slice. Each LUT comprises of six independent inputs (A inputs – A1 to A6) and two independent outputs (O5 and O6). Any arbitrary defined six-input Boolean function can be implemented with LUTs. It is noted that, implementation of two arbitrary defined five-input Boolean functions are also possible. In addition, any combination of arithmetic operators (summation, multiplication, inversion) can be implemented through LUTs. Figure 1-11A shows the original LUT architecture extracted by Xilinx FPGA Editor Tool [28]. Figure 1-11B and C represent a 6-input AND gate implemented by LUT and its faulty model, respectively. It is seen from these figures that the faulty model shows a different logic behavior (constantly ‘0’) due to SEU effect in the LUT.

1.4.5 Fault Model in Switch Matrices

SMs comprise of very short interconnections along with some PIPs that are used to link routings between slices and CLBs or between CLBs throughout the fabric. Each slice-to-slice connection requires passing through SMs. The PIPs as the main components of an SM are sensitive to SEU. A bit-flip in their configuration cell may change the routing configuration [34]. The routing resources are classified into two groups; the *inter*-CLB, and the *intra*-CLB routings. The inter-CLB routings and used for CLB-to-CLB interconnection. These routing are longer and have to pass through SMs. The intra-CLB routings are shorter and located inside a CLB. The SMs are commonly used to route inter-CLB, while the buffers and MUXes are employed for intra-CLB routings. Figure 1-12 shows the SM model comprised of some PIPs and routes. Once an SEU flips the configuration bit of a PIP, the fault will occur and it might induce a delay due to the created parasitic path or it may change the routing configuration and cause malfunction in the design.

1.4.6 Fault Model in Slice Registers

The slice registers (latches or flip-flops) are the bit storage components available within the slice of Virtex FPGAs. Virtex-5 includes four flip-flops per slice. Available control signals for slice registers are set/reset (SR), clock enable (CE), and clock. The SR signal can be set as synchronous or asynchronous depending on the design criteria.

The available register primitives in most Virtex families are [35] :

- FDR : D flip-flop with synchronous reset,
- FDS : D flip-flop with synchronous set,
- FDRS : D flip-flop with synchronous set/reset,
- FDC : D flip-flop with asynchronous clear,
- FDE : D flip-flop with clock enable,
- FDP : D flip-flop with asynchronous preset.

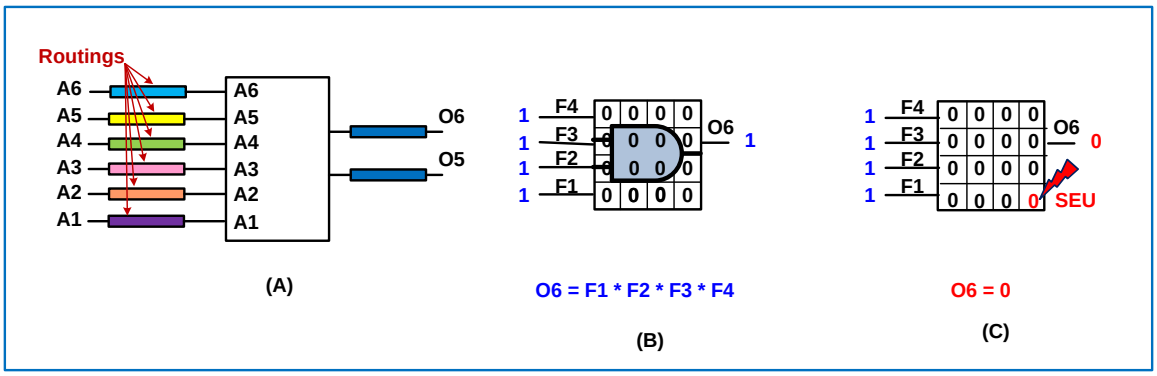


Figure 1-11 : Fault model for LUT [33]

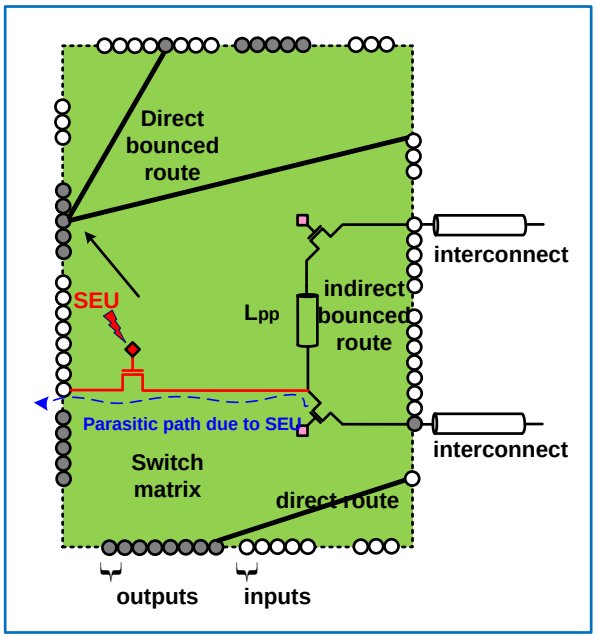


Figure 1-12 : SM model and SEU effect [28]

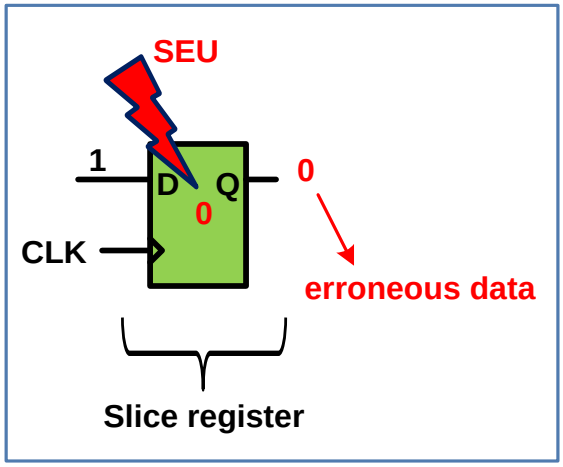


Figure 1-13 : Fault model in slice register due to SEU effect

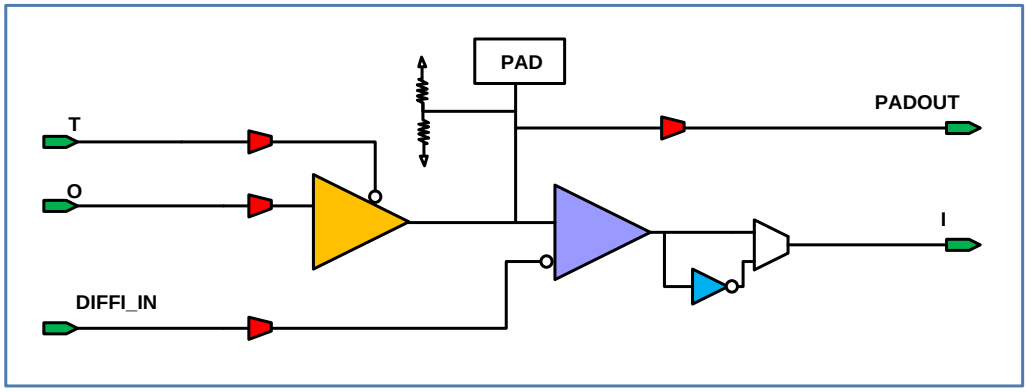


Figure 1-14 : IOB model for Xilinx Virtex FPGA [28]

Figure 1-13 shows the fault model for the slice register due to SEU effect. Once the SEU is injected, at the next rising edge of the clock signal, it provides erroneous data at the output *Q* which may cause malfunction in the circuit operation or wrong data transmission through the circuit.

1.4.7 Fault Model in IOBs

IOBs are group of basic elements that are used to implement the input and output functions of an FPGA device. The IOBs make the FPGA core accessible for the user for monitoring and measurement purposes. Figure 1-14 shows the IOB model for Xilinx Virtex FPGAs extracted by

Xilinx FPGA Editor tool [28]. It is noted that in most cases, an SEU breaks the IO circuitry and ceases the signal transmission to the output pads. As experimentally observed in [36] it may also generate DCs, while the top side of the FPGA is exposed to proton radiation. Toward the characterization of DCs in IOBs, it is conjectured that the SEU may alter the IO drive/standard of IOBs.

1.5 AVIO-403 Project

The AVIO-403 project was a team research work on the effect of cosmic rays on aircraft electronic devices and development of mitigation methods to reduce the on-board electronics' downtime. Researchers from four academic institutions namely, Polytechnique Montréal, École de Technologie Supérieure (ÉTS), Université du Québec à Montréal (UQAM) and Concordia University were part of the team. Also, three industrial partners, Bombardier Aerospace, Canadian Space Agency (CSA), and MDA Corporation, were participating and funding the project partially. Several students were involved in this project, including three master's and seven Ph.D. students as well as internship programs provided to undergraduate students.

The main objective of AVIO-403 project was to provide a better understanding of cosmic radiation effects on electronic systems with an emphasis on SRAM-based FPGAs. The objectives include the qualification and quantification of radiation effects along with means for prediction and mitigation of these effects. By adapting conventional design and integration techniques of embedded systems to consider the cosmic radiation effects on the functionality and reliability of electronic modules, the following key objectives were guided the research [37] :

a. The definition and implementation of an early assessment technique for high level digital design implemented into the FPGAs.
b. The definition and implementation of a verification technique for different levels of abstraction in order to simulate the faults induced by radiation.
c. The definition of a design approach in order to facilitate the pre-certification tests for radiation tolerance.
d. The investigation of fault-tolerant techniques employed in complex industrial systems.

1.6 EPICEA Project

The Electromagnetic Platform for lightweight Integration/Installation of electrical systems in

Composite Electrical Aircraft (EPICEA) project is a team research work that has a very wide scope including the study of electromagnetic waves' effect on aircraft, and cosmic rays effect on avionic systems that covers more objectives.

This three-year European-Canadian joint research project will address numerous avionic engineering design issues in the development of future aircrafts, aiming at a significant reduction of energy consumption through more electrical aircraft and systems integration. To be more specific, this research will release, validate and verify a unique computer-modeling platform assimilating a complete understanding of electromagnetic (EM) issues on composite electric aircraft (CEA). This includes the analysis and characterization of EM coupling, interconnections, and cosmic radiations on electrical systems together with new concepts of antennas designed to maintain performance in composite environment without modifying aircraft aerodynamics. The targeted computer platform will support a decision-making process for selection of the best strategy for the integration of electrical systems. This project will also create a more robust EM protection for electrical systems, i.e., lightweight and cost effective, a lighter and safer electrical system architecture for EM protected, less redundant, safety compliant, easy to maintain systems, a less drag on new systems of antenna while maintaining EM performance, and also will point to best possible health monitoring solutions. The research outcome will limit the recourse for over conservative protection and unnecessary redundancy in architecture design. This will overcome the weight penalty currently jeopardizing the development of energy-efficient CEAs and will strengthen the aircraft safety. The anticipated activities create a great example of Canadian international collaborative research. It attracts, involves and trains numerous highly qualified personnel for emerging CEA development. Research expertise and novel knowledge generated by this project not only enhance Canadian research profile and spur corporate growth, but have an impact on our daily life. The project focuses on emerging market needs, and timely addresses worldwide challenges. This promotes a sustainable development of Canadian society.

1.7 Problem Definition

Almost 98% of all memory elements in SRAM-based FPGAs are configuration bits, of which 90% and more control the routing resources. FPGAs are used in avionic industry and it is desired to come up with robust implemented designs against SEU. Once an SEU strikes the configuration bit of a routing interconnection, an extra delay may be induced by creating a short between a

routed path and an unused interconnection. Propagation of the induced delays in the consecutive logic modules implemented into FPGA may cause malfunctions in circuit behavior or cease the circuit operation. In order to characterize the effect of SEUs on SRAM-based FPGAs, two series of proton irradiation experiments have been performed at TRIUMF laboratory by our team in AVIO-403 project [32], [36]. The first report on extra combinational delays due to transient ionizing radiations has been presented in [32], where the existence of extra delays due to SEUs induced by proton irradiation has experimentally been observed and measured. The proposed setup in [32] has been shown to be able to detect extra combinatorial delays as small as 40 psec, and delays of more than 400 psec that may affect the targeted FPGA. Extra combinational delays have been observed when the board was bombarded by different protons energy levels. The experimental setup for the two series of experiments at TRIUMF is explained in details in CHAPTER 2.

Understanding the root cause of observed delay changes in the experiments performed in [32] and [36], as the first problem stated in this thesis, requires elaborating characterization techniques as well as accurate models for the observed delay changes.

High frequency designs implemented to the SRAM-based FPGAs are more susceptible to SEU-induced delay changes due to the shorter clock period and the slack time. The slack time in a synchronous design is defined as the minimum delay between the combinational logic data arrival time and the active edge of the clock, minus the flip-flop setup time. Creating measurement techniques for high frequency circuits for delay changes is considered as the second problem in this thesis.

Sensitivity evaluation of the routing resources to delay faults caused by radiations, has not been addressed thus far in the literature. The susceptibility of the routing interconnection network in a state-of-the-art APSoC device exposed to neutron irradiation is taken into consideration as the third problem. An APSoC device comprises different types of interconnection with different topologies for each, and thus it is necessary to evaluate the sensitivity of each interconnection type and topology to radiation. To this end, a method to configure ring oscillators mostly with routing resources is proposed where logic resources rarely contribute. An experimental setup is proposed in order to measure DCs induced to the routing resources of the APSoC device, when it is exposed to neutron radiation at TRIUMF laboratory.

To provide the justification for this research project in delay faults detection and correction, while performing experimental measurements at TRIUMF, it was observed that 68 ring oscillators had broken, i.e., logic faults, against 56 observed ODCs, i.e., delay faults, during the same time lapse. As a rule of thumb, for TRIUMF experiments, these values justify that the delay faults detection and correction mitigate about 50% of faults caused by SEU in digital circuits implemented into FPGA. In addition, almost 98% of all memory elements in SRAM-based FPGAs are configuration bits, of which more than 90% control the routing resources. Moreover, our recent in-beam neutron irradiation experiments on the APSoC devices involving SRAM-based FPGAs show the high vulnerability of routing interconnection network to SEUs inducing DCs. It is observed that as we get towards the higher levels of DC, the probability of receiving more DCs increases. This is mostly attributed to the growth of parasitic interconnection network caused by SEU. Hence, the use of delay monitor circuit on sensitive nodes of the design is necessary in order to capture the transitions that may lead to delay faults. Sensitive node is defined as the endpoint of critical paths with the worst (smallest) slack time.

1.8 Objectives

The objectives of this research project are as follows :

1. Explore characterization techniques to better understand propagation delays and delay changes (DC) induced by SEU in SRAM-based FPGAs of avionic systems in the aircrafts;

2. Elaborate accurate models of extra combinational delays (ECD) in SRAM-Based FPGAs due to transient ionizing radiations;

3. Create measurement techniques for high frequency circuits implemented into the SRAM-based FPGAs in order to detect and measure DCs caused by SEUs on sensitive nodes;

4. Elaborate mitigation techniques for DCs induced by SEUs toward a realistic and robust design of digital circuits implemented into the FPGAs while avoiding the TMR and minimizing the system downtime;

5. Investigate the likelihood and significance of DC occurrence in the routing interconnection network of state-of-the-art APSoC devices exposed to neutron irradiation;

1.9 Research Contributions

The contributions of this thesis achieved per each journal article are listed as follows.

Article 1 : M. Darvishi, *et. al.*, “Circuit Level Modeling of Extra Combinational Delays in SRAM-Based FPGAs Due to Transient Ionizing Radiation,” *IEEE Transactions on Nuclear Science,* vol. 61, pp. 3535-3542, 2014.

- ❖ Investigate the root cause of observed DCs in the Core and IOBs;
- ❖ Elaborate circuit level models and simulation of delay changes;
- ❖ Obtain good agreement with experiment results.

Article 2 : M. Darvishi, Y. Audet, and Y. Blaquière, "Delay Monitor Circuit and Delay Change Measurement due to SEU in SRAM-Based FPGA," *IEEE Transactions on Nuclear Science,* (Early Access), DOI : 10.1109/TNS.2018.2828785, 2018.

- ❖ Design and implementation of a delay monitor circuit for high frequency circuits
- ❖ Propose algorithms for SDC and CDC detection and measurement
- ❖ Incorporate the delay monitor as a part of mitigation technique
- ❖ Find the exact location (address) of PIP that contributes in DC generation in different levels

Article 3 : M. Darvishi, Y. Audet, Y. Blaquière, *et.al*., “On the Susceptibility of SRAM-Based FPGA Routing Network to Delay Changes Induced by Ionizing Radiation,” *IEEE Transactions on Nuclear Science,* Submitted.

- ❖ Evaluate the sensitivity of routing network to SEU in PL part of APSoC devices
- ❖ Propose a method to configure ring oscillators mostly with routing resources

- Propose an algorithm to identify extra parasitic interconnects in switch matrices automatically
- Define the MTTDC notion, proving the relation between the order of DC and probability of receiving a subsequent DC
- Prove the delay monitor efficiency for DC detection

1.10 Organization of the Thesis

The thesis is organized as follows. The literature review is presented in CHAPTER 2. This chapter provides a literature review on the existing works on characterization of delay faults in FPGAs and mitigation techniques mainly for ASICs and FPGAs, as well as their advantages and limitations. Process for the research project as a whole and general organization of the document indicating the coherence of the articles in relation to the research goals is presented at the end of Chapter 2. In CHAPTER 3, the proposed circuit-level models for extra combinational delays in SRAM-based FPGAs due to transient ionizing radiation are presented. This is the first work on modeling of combinational delays in FPGAs. In CHAPTER 4, a delay monitor circuit for delay change/fault detection and measurement is proposed which can be applied to high speed designs implemented into the SRAM-based FPGAs. The monitor's functional behavior and characterization are investigated and an experimental setup is introduced to verify its functionality in real implementation. CHAPTER 5 presents the in-beam experimental results for the likelihood and significance of delay fault occurrence in the routing resources of a Zynq-7000 APSoC device due to high-energy neutron irradiation. A method to configure ring oscillators mostly with routing resources is proposed, where logic resources rarely contribute. A full control over routing resources enables us to employ different interconnections available in this device to create routing-based ring oscillators. General discussion of the objectives and the achievements in this thesis is presented in CHAPTER 6. Finally, concluding remarks and scope for further research are presented in CHAPTER 7.

1.11 Summary

In this chapter, the fundamentals of the project along with the thesis objectives have been defined. A background of the cosmic ray effects in avionic electronics was presented and the destructive and non-destructive phenomena caused by SEUs on the electronic devices especially

those involved FPGAs have been introduced. Xilinx Virtex-5 FPGA, which is the device under test in part of this thesis, and its corresponding resources have been reviewed. Fault models in FPGA resources generated by SEU have been stated. Then, an introduction to AVIO-403 and EPICEA projects where this thesis was involved in them has been stated. The problem and the objectives of the research have been introduced along with the research contributions. Finally, the organization of the thesis has been stated. The literature review concerning the cosmic rays effects in avionic electronics especially the SEU effects on FPGAs will be addressed in CHAPTER 2.

CHAPTER 2 LITERATURE REVIEW

2.1 Introduction

In this chapter, the important aspects of the existing body of literature are presented. In particular, the related works on characterization of SEUs in CMOS SRAM memories and digital logic ICs are studied. The existing experiments for SEE and SEU characterization in SRAM-based FPGAs and mitigation strategies are then discussed. The concept of triple modular redundancy (TMR) and partial reconfiguration as the available and commonly-used mitigation techniques for design of fault-tolerant embedded systems are presented. Formal SEU detection and correction techniques in FPGAs are also discussed. Related works on design and implementation of time-to-digital converters (TDC) applied to FPGAs are presented. In addition, delay fault detection schemes, testing strategies and their application in ASICs and mainly FPGAs are discussed. The last part of this chapter presents a review on routing faults detection and correction schemes applied to the FPGAs.

2.2 SEU Effects in Digital ICs

It is known that if the MOSFET fabrication technology is scaled down, sensitivity of ICs to ionizing radiation emitted by sun and galactic events is increased [38], [39], [7]. The ultra-scaled memory ICs are very sensitive to SEU. In addition, digital devices are more prone to digital single-event transient (DSET). Charge collection measurements in devices or junctions are commonly used to provide an insight about SEU effects in complex circuits such as SRAM cells [40], [41].

In order to simulate the SEE effects at circuit level, the transient induced by single-event is modeled as a current source connected at the struck node of the circuit as shown in Figure 2-1 [38]. Although this approach might be efficient for many applications, there are some drawbacks and limitations. In particular, the accuracy of the transient current used as the input source may affect the accuracy of the circuit simulation. A memory cell has been simulated in [42], the presence of single-events with the SPICE tools, when a current pulse has been applied as the stimuli in the circuit to reproduce the ionizing particle effect.

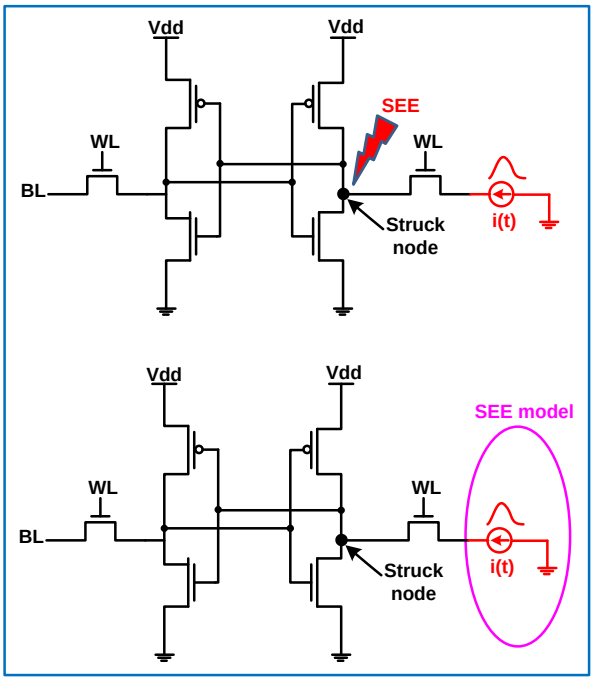


Figure 2-1 : Simulation of SRAM cell to investigate SEE [38]

To circumvent the drawbacks of the SPICE simulation to investigate SEE, the mixed-mode technique is utilized by employing device simulation to predict the response to ionizing radiation of the struck device. The affected device by single-event is studied by simulation of the device-level model while the other devices are presented by circuit-level model. This technique is called a mixed-mode technique and has been presented in [38], [43]. Mixed-mode analysis is useful in circuits including a few numbers of devices such as SRAM cells. Another advantage of mixed-mode technique is the ability of simulating ionizing radiation effect in new devices such as ultra-scaled multiple-gate devices. In this case, all transistors included in an SRAM cell can be simulated in 3-D device domain [44], [45]. On the other hand the main drawback of the mixed-mode simulation is an increase in simulation time especially for large circuits. In addition, 3-D mixed-level simulation has low accuracy in existence of coupling effects between devices [46]. More specifically, scaling-down the CMOS fabrication technology increases the integration level and results in substantial coupling effects [47-49]. In order to overcome the high time consumption drawback of the mixed-mode simulation, full numerical simulation is used as an alternative, which provides higher accuracy for SEU evaluation in SRAM cells. This technique

models all the devices entirely in 3-D mode. This technique has been employed to perform a fully numerical simulation of SRAM cell in 3-D mode [46], [47], [48].

2.3 Radiation Experiments on FPGAs

In this section, existing works on radiation experiments on the FPGAs is studied. In order to characterize SEEs on FPGAs, some experiments are conducted to emulate the cosmic environment in the laboratory. Laboratories with special equipments for SEE investigation are called particle accelerator labs. There are several particle accelerators around the world [50]. Two leading particle acceleration labs are located in North America, Canada; Canadian Light Source (University of Saskatchewan), and Canada's National Laboratory for Particle and Nuclear Physics (TRIUMF), Vancouver, British Colombia.

A cross comparison of SEU responses in more than thirty devices (SRAM microprocessors and FPGAs) using different neutron/proton beams has been studied in [51]. It has been shown that the proton and neutron beams can be used for SEU test. Thus, the proton and neutron beams have been used in order to measure the atmospheric neutron SEU cross section in SRAMs, FPGAs, microprocessors, and SDRAMs.

The "Rosetta experiment", the atmospheric soft error rate testing in different technology FPGAs has been reported in [52]. In real-time experiments by evaluating large FPGAs fabricated in different CMOS technologies (0.15 μm, 0.13 μm, and 90 nm), their sensitivity to radiation-induced SEUs has been investigated. The results have been comparable with those obtained by circuit simulations as well as with the Los Alamos Neutron Science Center[1] (LANSCE) neutron beam results and Crocker Nuclear Laboratory (University of California, Davis) [52]. It has been shown that the sensitivity to atmospheric upsets is at least eight times less than that predicted by the Boeing experiments for SRAM devices. Moreover, it has been shown that the actual upset rate experienced by users is less than that of the rate of configuration memory cell upsets.

SEU mitigation techniques for Virtex FPGAs exposed to proton radiation has been reported in [53]. In [53] the SEU characterization for both static and dynamic modes of operation with heavy ion and proton test has also been studied. Based on the results obtained, an SEU mitigation

---

1 . World's biggest and fully equipped radiation lab located in Los Alamos, New Mexico, US established in 1943.

technique has been developed by combining TMR and SEU correction through configuration scrubbing to preserve the functionality of the implemented design in the case of upsets occurrence.

A comprehensive framework of SEU-like fault injection has been presented in [54]. This framework has been considered as a method of reproducing radiation ground test results in order to investigate the vulnerability of microprocessors to SEUs. The fault injection strategies have been classified into two categories : hardware and software-based methods. In the software-based method, based on the DUT description level, some possibilities for fault injection have been shown to be summarized as follows :

- Fault injection via SPICE, where the netlist is available [55];
- Fault injection via VHDL/Verilog coding, where the RTL or behavioral description of the design is available [56];
- Fault injection via instruction set simulator (ISS) model that is a simulation model using high-level programming languages. ISS mimics the microprocessor's behavior [57];
- Fault injection with a laser beam [58];
- Fault injection via an FPGA where the RTL description of the design is available and is mapped to the FPGA [59];
- Fault injection via code emulating upset (CEU) technique [60]. This method applies a bit-flip to the struck memory cell randomly in time [61].

The first report on extra combinational delays in SRAM-based FPGAs due to transient ionizing radiations has been presented in [32]. A novel experimental setup has been presented in order to measure the extra combinational delays in a commercial FPGA-based test board (Digilent Genesys, including Virtex-5 XC5VLX50T). Employing this setup, enabled the detection of extra combinational delays between 40 psec and 400 psec. It is known that, there are five areas of the FPGA's CLB that are susceptible to SEU as illustrated in Figure 2-2 [62]. It can be seen from this figure, the configuration bit of each part that is responsible to control its functionality is susceptible to SEU.

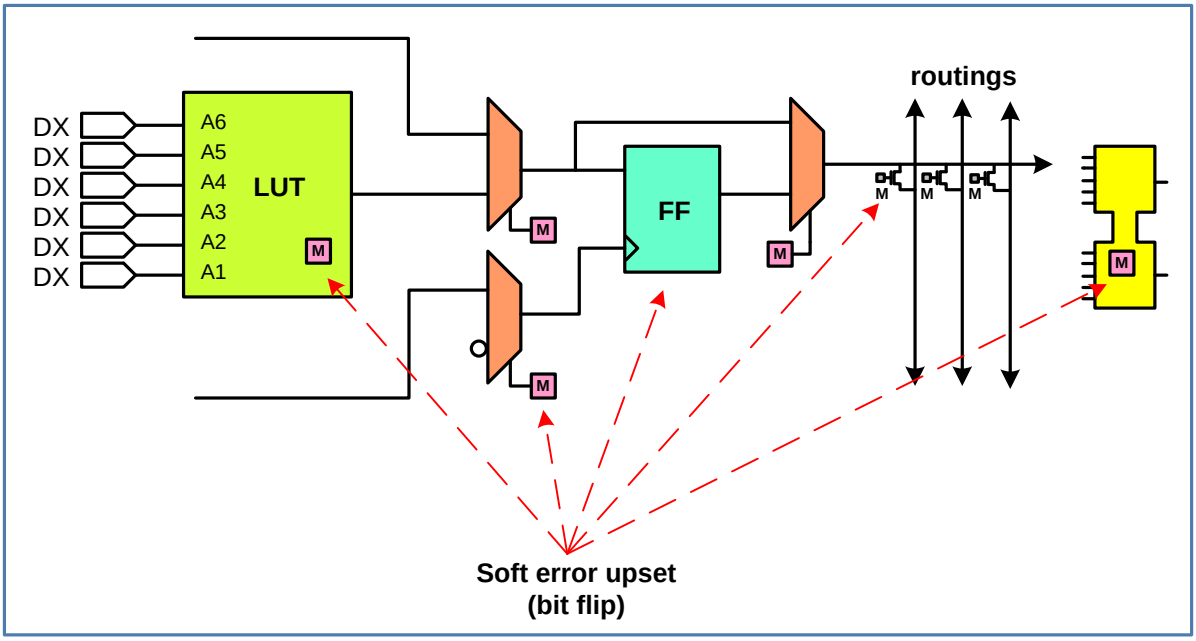


Figure 2-2 : SEU sensitive areas in a CLB in FPGA [62]

The main focus in [32] has been on the routing configuration bits of the SRAM-based FPGAs. These configuration bits are very sensitive to SEUs and the stored value could be inverted, i.e., bit-flip [63]. It should be noted that not all of the bit-flips induced by SEUs lead to an error, since some of them refer to the unused resources and do not affect the implemented design on the FPGA. However, those bit-flips that occur within the implemented design may give rise a design failure even in logic or timing. The common implications of bit-flip on the routing configuration bits are the creation of a *short* or an *open*. These two phenomena have been explained in [32] by using simplified implementation of a 2-input AND gate as shown in Figure 2-3. In this figure, the bold lines are the interconnections involved in the logic network and the pale lines are the unused interconnections. The unfilled squares represent the disabled PIPs and the filled squares refer to the activated PIPs. Figure 2-3A shows the implementation of an AND gate which is fault free, and Figure 2-3B shows an open state due to the bit-flip in a configuration bit (‘1’ to ‘0’) disabling the intended interconnect. Figure 2-3C illustrates a short state by flipping ‘0’ to ‘1’ in configuration cell enabling an unintended interconnection. Finally, Figure 2-3D represents a delay, in which a bit-flip (‘0’ to ‘1’) on a routing configuration enables its PIP and imposes an undesired connection between a live and an unrouted line. This results in creating an extra parasitic capacitance and hence an extra delay along the struck signal path.

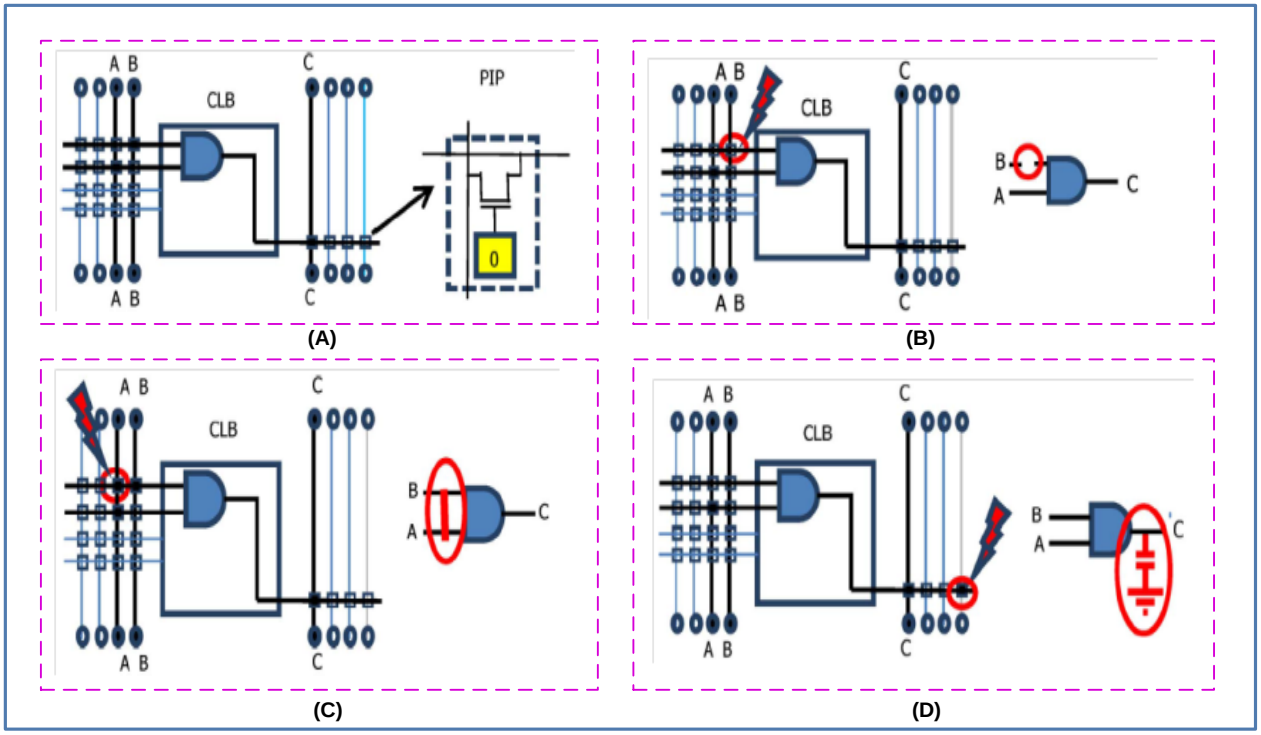


Figure 2-3 : Simplified view of the bit flip impact on an implemented 2-input AND gate : (A) Fault free implementation, (B) an open case, (C) a short case, and (D) a delay case [32]

Two identical ring oscillators (RO) functioning at almost the same frequency (F_1 and $F_2 = 1.25$ MHz) have been implemented at the core of FPGA in [32]. Instead of individual ROs frequency measurement, the intermodulation frequency $F_2 - F_1 \approx 12.4$ kHz of the ROs has been measured. Using the setup in [32], a resolution of 18 Hz has been obtained when measuring the frequency difference, and 12 psec on observed delay variations. A set of 48 experiments has been performed when the proton source bombarded the top side of the FPGA. Each delay measurement has been stopped when the oscillation of one RO ceased due to a functional failure triggered by an SEU or after a specified period of time (10 minutes). Twenty three of those experiments came with one or cumulative ODCs. The delay change could produce either a reduction or an increase of the measured frequency difference depending on which of the two ROs affected. Figure 2-4 shows two sets of experimental results indicating the observed delay changes in [32]. Considering the initial assumptions in [32], the extra combinational delays may be the result of an undesired connection of unrouted interconnects to the live interconnects.

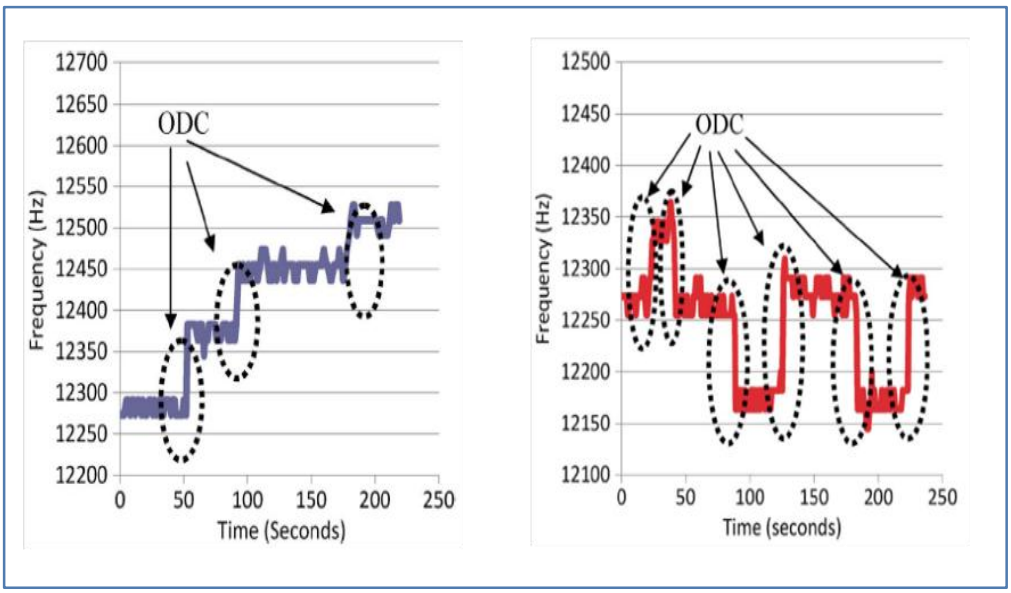


Figure 2-4 : Experimental results indicating ODCs observed in [32]

Following the experiments performed in [32], another set of experiments has been performed at TRIUMF laboratory on delay faults affecting the IOBs of an SRAM-based FPGAs as reported in [36]. The experimental setup consists of two ROs created directly in the IOBs using their IOBUF primitives and have been implemented into the Virtex-5 FPGA. The ROs oscillated at slightly different frequencies, $F_1 \approx 802$ kHz and $F_2 \approx 902$ kHz. The first RO occupied 179 IOBs configured as a long delay chain connected to one inverter, while the second one occupied 160 IOBs linked to one inverter. Three sets of experiments have been performed for delay measurement while each set comprised of ten experiments with different energy levels of 63 MeV, 50 MeV, and 35 MeV. Each experiment has been stopped when one RO ceased oscillation. A delay change produced a variation in the frequency difference of two ring oscillators. In the experiments of [36], larger ODCs than the ones obtained in [32] have been measured. A maximum magnitude of a single ODC observed was almost 6.2 nsec and in total four ODCs had a value larger than 1.5 nsec. It is shown that the large delay changes are due to accumulation of delays along the RO within a same IO bank.

2.4 SEU Mitigation Techniques in FPGAs

As discussed in Section 2.3, if an SEU occurs in a Virtex-5 FPGA device, it may affect the device configuration or alter the data flow in design [30].

In some circumstances, the alteration of a single bit within data can be ignored because of its limited effect. Since a bit-flip in a PIP can be recovered by data rewriting, the effect of SEU is short lived. In the cases where the data determines the operation of a system or forms the instructions, the error caused by bit-flip is significant and should be corrected. For instance, a bit-flip in a finite state machine (FSM) can result in entering into an illegal or undetermined state. In these cases, some design prerequisites and assessment strategies are required to ensure the proper operation of the system against SEUs [30]. It is noted that the technique used to remove the effect of SEU is called *mitigation* [62].

If an error occurs in an FPGA device, it may be fixed in the next reconfiguration time. However, an important question remains. What happens during the time period between the failure caused by SEU and the device next reconfiguration cycle? Depending on the reliability level of the device and condition of its operation, the device may continue its normal operation or it may fail as a result of the SEU effect. In the next two sections, the TMR and partial reconfiguration are described as two well-known available techniques for SEU mitigation in FPGAs.

2.4.1 Triple Modular Redundancy (TMR)

Some methods employ redundant logics and modules that are identical with the original ones in design. The final output of the redundant modules is generated through a voter circuit. The faulty module can be identified where the redundant modules provide disparate outputs. Two common redundant techniques are dual modular redundancy (DMR) [64-66] and TMR [67-69]. The DMR technique duplicates the modules of a design and the final output is generated through a 2-input voter. Although DMR has low cost and area overhead, it is not able to identify the affected module (original or redundant) when a fault happens [64].

TMR method is a well-known SEU mitigation technique which triplicates the design under test [70]. The final output is generated through a voter. The voter reports the detected fault when one of the redundant modules provides a disparate value to the voter that is different from the values provided by the other redundant modules. When one module is failed due to the SEU, a safe functionality of the logic is ensured since the two redundant modules continue to provide the correct output. However, the errors should be corrected and not accumulated [70]. When two modules fail at the same time or within a certain period of time (less than detection time), TMR technique is not able to handle the fault detection process. In addition, the large cost, area

overhead, and power inefficiency due to the triplication of all modules associated with the design are considered as the disadvantages of this method. These limitations make the TMR less popular to be used individually. Thus, it is usually combined with other mitigation techniques in order to provide a robust fault-tolerant mitigation scheme.

In [53] two mitigation techniques have been combined in order to achieve a robust design; TMR and static SEU correction through configuration scrubbing. The mitigation technique in [53] has shown to preserve the functionality of the device against SEUs. Moreover, in this technique, the soft errors do not create functional errors, the static errors do not create functional errors, and the self recovering feature of the TMR can automatically update the internal state data, when the configuration correctness is restored.

2.4.2 Partial Reconfiguration

Partial reconfiguration technique addresses the change of a small fraction of a reconfigurable hardware by loading a partial configuration file, usually a partial BIT file while the other parts are operating. After a full BIT file configures the FPGA, the partial BIT files can be downloaded into the FPGA to modify the reconfigurable regions while the integrity of the running application is preserved. It is noted that similar to the software, the hardware electronic systems can also be designed modularly by dividing the entire system to several sub-modules. It is desirable to alter one or several sub-modules in a system while the other sub-modules are operating. This is the main challenge in the current partial reconfiguration techniques.

However, partial reconfiguration technique is not supported by all FPGAs, and thus, it requires dedicated software for modular design to achieve a partially configured system. Based on the design functionality, the partial reconfiguration technique is categorized into two groups [71], [72] :

- *Dynamic partial reconfiguration*, also called active *partial reconfiguration* : allows to modify a part of the device while the other parts of the design mapped into the FPGA are still operating;
- *Static partial reconfiguration* : when the device is deactivated during the reconfiguration process. It is noted that when downloading the partial BIT file into the FPGA, the other parts of the device are in shutdown mode. After the completion of the reconfiguration process, the stopped modules will start operating [73].

Xilinx offers two types of partial reconfiguration for FPGA devices : *module-based* and *difference-based* [73]. Module-based partial reconfiguration allows reconfiguring separated modules of a whole design implemented into the FPGA. Successful communication between separate modules of a design is ensured through special bus macros. The bus macro acts as a bridge connecting the reconfigurable modules to the other parts of the design. Also, a separate bitstream should be generated for each reconfigurable module in a design that is used to perform partial reconfiguration in the FPGA.

Difference-based partial reconfiguration is used when a small change is applied to the design. For example, it can be used when LUT equations or contents of the memory blocks are changed. In this case, the generated bitstream contains the information of the difference between the structure of the current design and the new contents of an FPGA. There exist two types of difference-based partial reconfiguration, namely, the *front-end* and *back-end* methods. The front-end method is based on the design modification in hardware description language (HDL) and it requires the repetition of the synthesis and design implementation process. The back-end method allows applying the modifications during the implementation stage of the design and it does not require the design re-synthesis. Utilizing any of these methods leads to the generation of a partial bitstream which is used to perform partial reconfiguration in the FPGA [74].

Figure 2-5 shows the premise behind the partial reconfiguration technique. It is shown in this figure that the logic in FPGA design is divided into two regions : *Static* region and *Reconfigurable* region. The static region remains functional and is not affected while performing the partial reconfiguration [74]. It can be seen from Figure 2-5 that the logic implemented in *Block A* is modified by downloading one of the *A1.bit to A4.bit* partial BIT files.

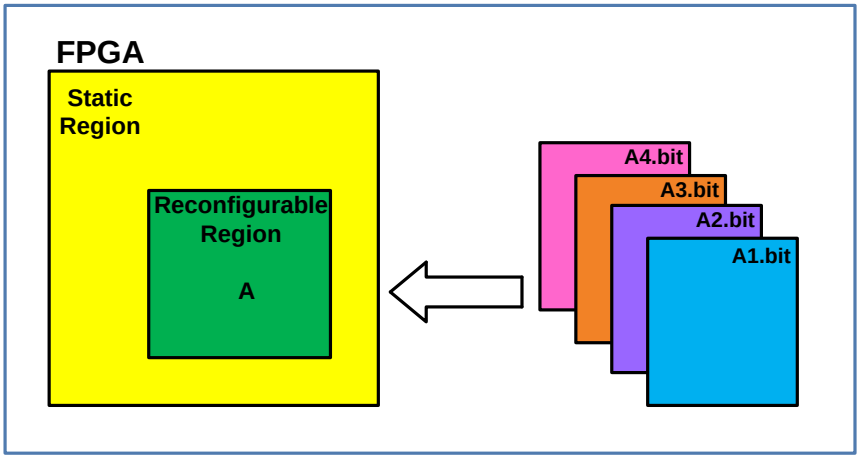


Figure 2-5 : Basic premise of partial reconfiguration [74]

Figure 2-6 represents a timeline with different time steps in order to clarify the functionality of the dynamic partial reconfiguration. For instance, at t_0 the reconfiguration hardware starts its operation while it contains no configuration information. After a time period reaching t_1, the configuration data is transferred to the device. After a successful data transfer, the FPGA continues processing within *Configuration A* and *Configuration B*. Each of these configurations can be considered as an FSM, an algorithm, or even the processing element. The target is to partially reconfigure the *Configuration B* with *Configuration C* while the *Configuration A* continues operating. At t_2, the functionality of *Configuration B* is stopped and is replaced with *Configuration C*. Once the configuration data corresponding to *Configuration C* is transferred successfully, the device continues processing with *Configuration A* and *Configuration C*. This shows the advantage of dynamic partial reconfiguration in adapting the system architecture to the application requirements when the system is running.

The advantages of partial reconfiguration technique are summarized as follows : area and power reduction [75], performance improvement [76], ability to change hardware [76], hardware sharing [76], shorter reconfiguration time [76], quick system start [75], and its wide application [75].

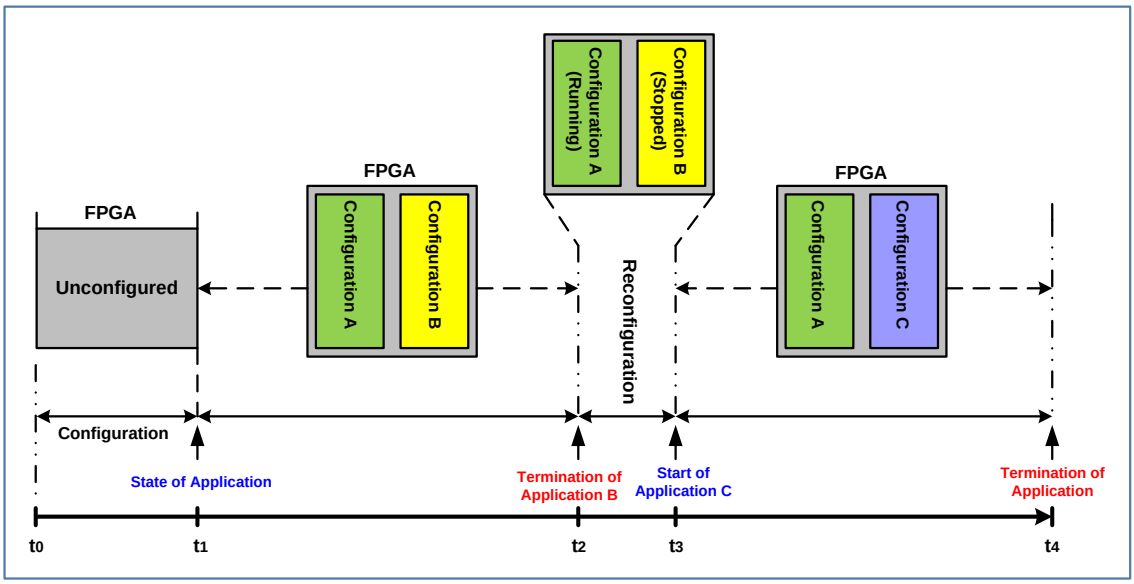


Figure 2-6 : Partial dynamic reconfiguration process [62]

2.5 SEU Detection Techniques in FPGAs

In general, SEU mitigation in FPGAs consists of two steps, *SEU detection*; and *SEU correction*. Therefore, a SEU-fault tolerant system consists of two sub-systems : *fault detection* and *fault correction* schemes. Most of the available techniques for SEU-induced fault detection applied to ASICs and FPGAs, stop the design for some cycles when the fault is detected. However, this is not a preferred solution in most of the applications especially in the avionic system of airplanes and spacecrafts travelling at very high altitudes. Generally, the SEU detection techniques are classified into readback and comparison, cyclic redundancy check (CRC), off-line test, and roving test [77], [78]. A brief discussion of these techniques is presented in the following.

2.5.1 Readback and Comparison

A traditional available technique to verify the stored data in the configuration memory is to read back the data and perform a bit-by-bit comparison [77]. The readback is performed through the mask (.msk) and readback (.rbb) files that are equal in size with the original bitstream used for configuring the FPGA. This method effectively triplicates the amount of the memory required for configuration and readback tasks. Therefore, this method is not considered as an efficient solution in avionic applications.

2.5.2 Cyclic Redundancy Check (CRC)

CRC frame check is another method for continuous readback of configuration data [79] and SEU detection developed by Los Alamos National Laboratories Space Data Systems Group [77]. This feature in Virtex-5 FPGA facilitates the SEU detection. Once the readback CRC is enabled, the configuration logic continuously reads back the content of the configuration memory and a 32-bit CRC value is generated. The first round of readback CRC value is considered as the golden value and the subsequent readback CRC values are compared with the golden one. When a mismatch is detected, the crc_error pin of the FRAME_ECC_VIRTEX5 primitive is asserted to high and the device is reconfigured [79].

2.5.3 Off-line test

This technique applies some test vectors to the design implemented into the FPGA in order to diagnose a fault occurrence [80-82]. The off-line test method is applied only when the FPGA is not performing its main operational task. This is considered as a drawback of this technique [83-86]. In addition, the limited number of test vectors and application dependency are the other limitation of the off-line test method [83], [87], [88].

2.5.4 Roving test

This technique relies on swapping blocks related to the implemented design and performs a progressive scan test in order to find a fault. Interrupting the entire system for one to three seconds and substantially reduced performance of the system are considered as the limitations of roving test. Another drawback of this technique is the increased latency for fault detection by increasing the design complexity [84], [89-91].

Readback and comparison, and the CRC are the SEU detection techniques embedded in some FPGAs. The latter four SEU detection techniques are compared in some comparable features as presented in Table 2-1 [78].

Table 2-1 : Comparison matrix of fault detection methods

Method	Speed of Detection	Resource overhead	Performance overhead	Granularity	Coverage
Modular Redundancy	**Fast** as soon as fault is manifested	**Very large** Triplication plus voting logic	**Very small** latency of voting logic	**Coarse** Limited to size of module	**Good** All manifested errors are detected
Concurrent Error Detection	**Fast** as soon as fault is manifested	**Medium** trade-off with coverage	**Small** additional latency of cyclic redundancy check (CRC) logic	**Medium** trade-off with resource	**Medium** Not practical for all types of functionality
Off-line BIST	**Slow** only in off-line mode	**Very small**	**Small** slight start-up delay	**Fine** possible to detect the exact error	**Very Good** All faults including dormant
Roving test	**Medium** order of 1 second	**Medium** Empty test block plus test controller	**Large** clock must be stopped to swap blocks. Critical paths may lengthen	**Fine** possible to detect the exact error	**Very Good** Multiple manifest and latent faults are detected

2.6 SEU Correction Techniques in FPGAs

Once the SEU is detected through one of the techniques described in Section 2.5, the SEU correction should be applied. In general, two important SEU correction techniques are single frame correction, and SEU scrubbing (also called active partial reconfiguration) [70], [77]. A brief discussion of these techniques is described in the following.

2.6.1 SEU Detection and Single Frame Correction

Once an upset in the configuration memory is detected through readback method, only the affected data frame needs to be corrected. This technique writes *only* a single data frame while

the configuration logic is put in “write state” for a short time. Therefore, most of the times, the configuration logic operates in the “read state” [77].

2.6.2 SEU Scrubbing (Active Partial Reconfiguration)

The readback technique for SEU detection requires hardware implementation of the algorithms for reading and evaluating each data frame. In addition, a large memory space is required in order to store the variables and constants. Therefore, a beneficial technique can be employed by removing the readback and SEU detection parts and reloading the configurable logic block (CLB) frame segment entirely at a chosen interval to be used for SEU correction. This technique is called scrubbing or active partial reconfiguration. Scrubbing requires less overhead in the system, however it puts the configuration logic in “write state” for a longer time which depends on the design complexity [77].

2.7 Review of TDCs Implemented in FPGAs

Events recognition and their time of occurrence representation in digital format is a key point in the most recent electronic instrumentation systems. The recognition and digital interpretation can be achieved by a TDC. For example, the arrival time of some incoming pulses or the time interval between two events can be measured by a TDC [92]. TDCs are also called *time digitizers* that measure a time interval between two pulses (start and stop) and convert it to a binary output.

Depending on the accuracy and the range of measurement, two types of time measurement are addressed in the concept of TDCs; *coarse* and *fine measurement*. In most of the applications, it is desired to measure a time interval between a start and stop events. One solution is to measure the time of the start and stop events and then applying a subtraction. A course counter is based on a reference clock signal. As shown in Figure 2-7, once the start signal is asserted, the counter starts counting and ends when the stop signal is detected [93]. In this case, the time interval between the start and stop signals is $T = n\,.T_0$ where T_0 is the period of the reference clock. As shown in Figure 2-7, in order to measure the time T, the main time intervals of T_s, T_a and T_b can be measured. The course counter measures the time interval of T_s by direct counting of full period of the reference clock signal [93]. A more accurate measurement technique with smaller measurement range is required for the small time intervals of T_a and T_b. Some analogue methods such as *time interval stretching* or *double conversion* and also some digital techniques such as

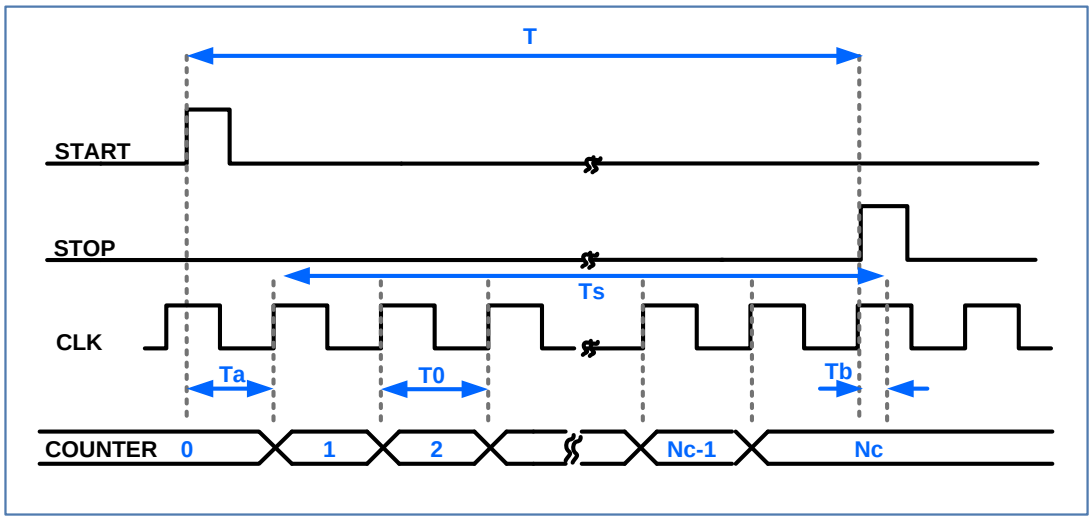


Figure 2-7 : Time interval measurement method [93]

Vernier method and *tapped delay lines* are available to measure the small time intervals of T_a and T_b. Although the analogue methods obtain better accuracies, they suffer from temperature variation which disturbs the measurement resolution. Therefore, the digital techniques for time interval measurement are preferred due to their flexibility and robustness against external environment variations such as the temperature [94], [95].

The clock frequency limits the accuracy of the implemented counter. For example, a 200 MHz clock frequency provides a resolution of 5 nsec. If a resolution better than the clock period is required, interpolation circuits need to be employed [94], in which a fraction of clock period is measured rather than the whole clock period. A significant amount of time is often required in interpolation circuits to perform their function.

Among the digital techniques, the Vernier interpolator that is based on Vernier technique is very popular [96]. It includes a triggerable oscillator along with a coincidence circuit. Vernier technique is the digital version of the time stretching technique. Two oscillators are tuned at f_1 and f_2 frequencies and start oscillation at the arrival time of START and STOP signals. Once the leading edges of the oscillators coincide, the measurement is terminated and the number of periods counted for oscillators (n_1 and n_2) leads to the time interval T extraction as [92] :

$$T = \frac{n_1 - 1}{f_1} - \frac{n_2 - 1}{f_2}$$

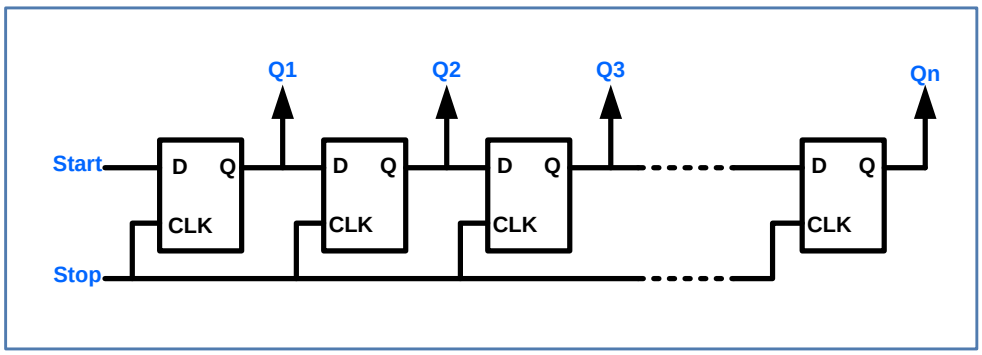


Figure 2-8 : Simplified circuit diagram of a tapped delay line [92]

Design of oscillators with accurate and stable frequency is a challenge in Vernier technique. This technique is realized by two tapped delay lines with slightly different delay times τ, also called *differential delay line* or *Vernier delay line*. Figure 2-8 shows a simplified circuit diagram of a tapped delay line. Propagating the signal through D flip-flops delays the START signal. The delayed versions of this signal are sampled at the arrival time of STOP signal. The STOP signal latches all the flip-flops. Therefore, the time interval between START and STOP signals is propagated through a certain number of flip-flops [97].

It is shown that the counters can be used to measure long time intervals but with a low resolution while the interpolation circuits can only measure small time intervals with high resolution. Therefore, a combination of these techniques, called the *Hybrid method*, may be employed for coarse and fine time measurement [94]. One of the most common techniques for hybrid measurement is the *Nutt method* [98]. As it is shown in Figure 2-7, the time interval of T_s is a factor of the clock period ($T_0 = 1/f_0$). Based on the Nutt method, the time interval of T is calculated as $T = T_s + T_a - T_b$.

A digital circuit can be considered as a network of transistors switching between low and high states along with some interconnection lines. In a digital circuit, propagation delay in signals is caused by transistors and interconnections that route a source point to a destination point. Therefore, some applications such as delay lines and asynchronous logic circuits require a precise delay control between two points in a circuit. Configuring the routing matrices enables the precise control of the delay in an FPGA [99], [100].

Several TDC architectures such as tapped delay lines (TDL) [101], delay locked loop (DLL) [102], Vernier delay line (VDL) [103], multi-level TDC [104] and the triggered RO [105] have

been so far presented by researchers. Most of the implementation tools used in existing architectures rely on full custom ASIC design or standard cell ASIC design. However, these implementations suffer from inflexibility, high cost, and long time to market. In addition, these design modules cannot be implemented into the FPGAs. In other words, not all of these designs can be converted directly into an HDL code for FPGA targets [106].

2.8 Delay Fault Detection and Test

An SEU may cause a bit-flip in configuration cell and induce DCs in the design implemented in SRAM-based FPGAs. In this section, some recent works on delay faults detection, correction and testing are discussed.

An approach for delay faults testing in Xilinx Spartan FPGAs applicable for on-line and off-line manufacturing test has been presented in [89]. This approach is based on built-in self test (BIST) method that requires no expensive external test equipment. Figure 2-9 shows the outline of the delay fault BIST architecture in [89]. Several paths under test have been configured where each path had the same sequence of programmable logic blocks wire segments. In this design, each PLB acts as a buffer for the signal traversing along the path. Also, the propagation delay associated with each programmable logic block is assumed to be identical in a fault-free design. The main idea of this technique is to compare the delays of paths under test. When a rising transition occurs at the input, the transition propagates through the paths under test and reaches at the input of the OR and NAND gates. Then, the signal *FIRST* and $\overline{LAST}$ respond to the fastest the slowest arriving transitions, respectively. The signal *FIRST* enables the local oscillator and the signal $\overline{LAST}$ will cease it. Therefore, the number of counted pulses for the oscillator can determine the delay *D* along the paths under test. In a fault-free circuit, the *D* value is smaller than a predetermined threshold delay value associated with the programmable logic blocks. Therefore, for the *D* values greater than the threshold, a delay fault is reported. This design has been utilized for delay fault testing in programmable logic blocks, LUTs and Adder configurations.

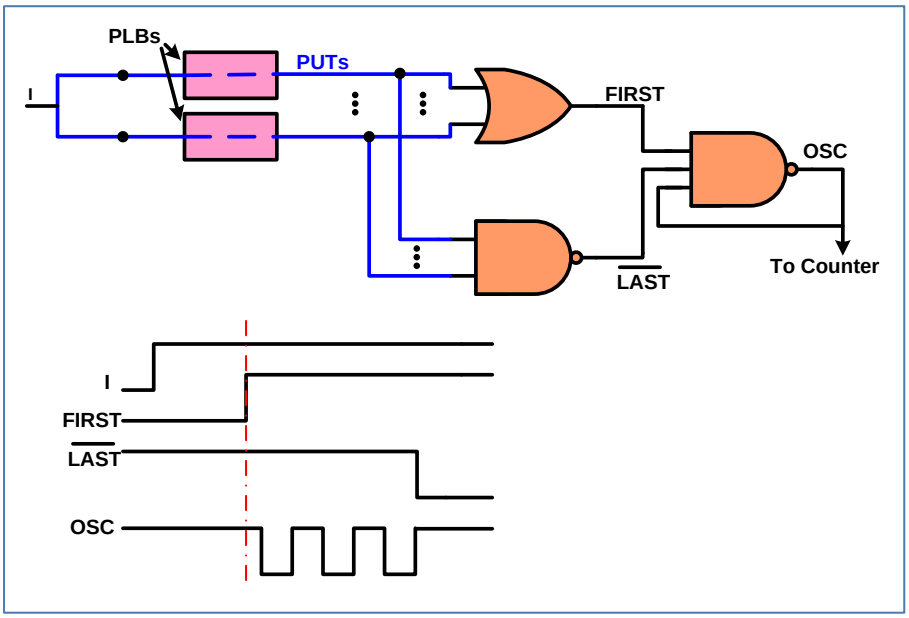


Figure 2-9 : Delay fault BIST architecture studied in [89]

An automatic test pattern generator (ATPG) for open, short and delay fault on 3-D FPGA interconnections have been studied in [107]. It has been shown that twelve test patterns were sufficient to achieve 100% open faults coverage while forty TPs were required to cover short faults. The fault models used in ATPG are shown in Figure 2-10. The open and short faults are defined as :

- An open fault is a line segment open when the switch controlling the line is stuck at ‘0’.
- A short fault occurs when the line’s control switch is stuck at ‘1’ and the line segment may tie to another line segment (L2LSF[1]), or the line’s switch control (L2SSF[2]), or a control line is tied to another control line (S2SSF[3]).

1 . Line-to-Line Short Fault

2 . Line-to-Switch Short Fault

3 . Switch-to Switch Short Fault

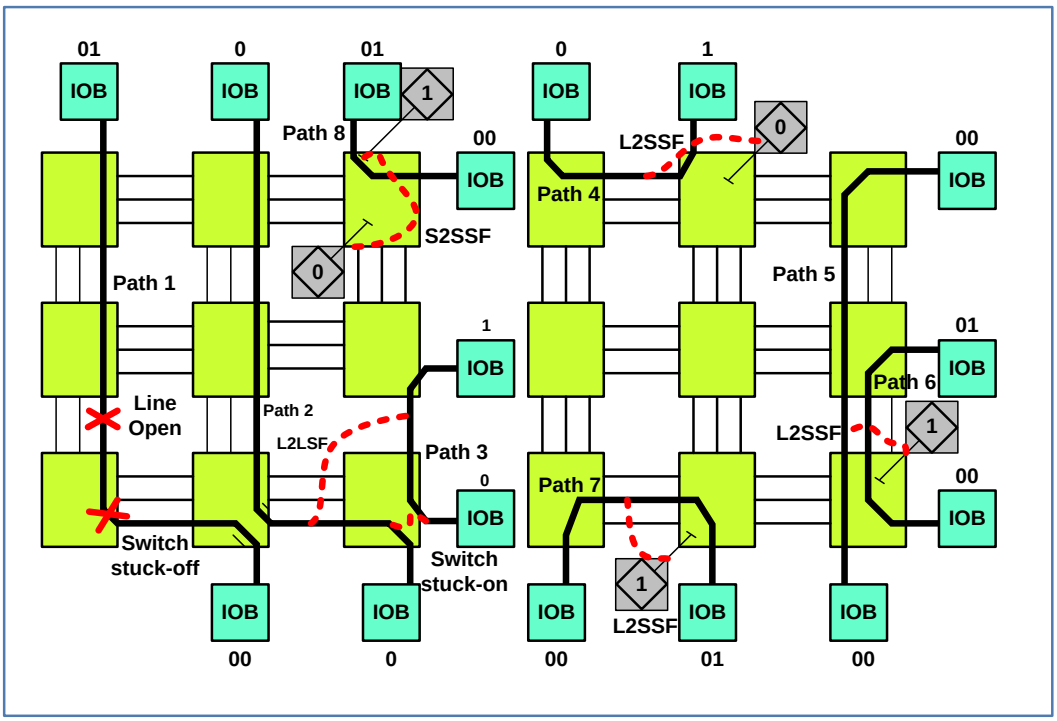


Figure 2-10 : Presented ATPG architecture for delay fault detection in [107]

Regarding the delay faults, since the shortest path in the design has the smallest variation in the slack time, it can determine the sensitivity of the delay fault detection. It should be mentioned that since the delay faults often occur at high frequency clock signals, the shortest path is a better choice than a long path. The shortest path for a target segment does not ensure that its wire length is also the shortest. For instance, a path including a double-length line can be longer than a path including two single-length lines. In the design shown in Figure 2-11, the shortest path comprises of three lines, two SMs linked to a flip-flop (FF) and a LUT. The extracted delay associated with the fault-free path was 2.45 nsec and the delay value after fault occurrence in the path was almost 2.85 nsec resulted in detection of 0.4 nsec delay fault [107]. Using the presented models and algorithms, an ATPG has been established to generate test patterns to detect all the opens, shorts and delay faults. In addition, the scalability of the model has been considered for different types of FPGAs.

A mechanism called timing-error-resilient network-on-chip (TRNoC) has been presented in [108]. It allows the network-on-chip (NoC) to operate at higher frequencies at the expense of some sporadically timing errors. The timing errors have been compensated by employing an error recovery strategy. In addition to the static variations, dynamic variations such as VDD drops,

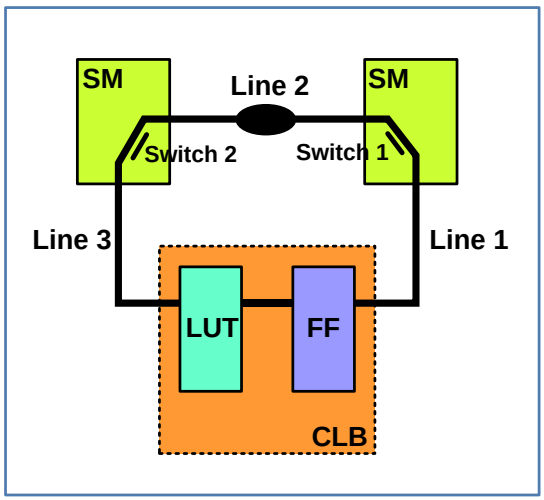


Figure 2-11 : Segment delay fault model presented in [107]

temperature and aging affect the NoC. These dynamic variations result in unpredictable behavior in the timing characteristics of the NoC. This may be a challenging issue in NoC design especially for the components that require significant timing margins. The TRNoC architecture comprises a lightweight timing-error detection mechanism along with a distributed error recovery mechanism. These mechanisms provide the lossless operation of the design, while leaving the fault-free paths of the network unaffected. The salient characteristics of the TRNoC architecture are summarized as :

- Independent per-input and per-output error handling confined only to the control paths of the design routes.
- Full protection against single and back-to-back timing errors and no package loss guarantee.
- Unaffected components by timing errors are kept isolated.

The technique in [108] is highly restricted to the available slack. The drawbacks of this architecture tailored to network-on-chip applications are summarized as :

- This technique is based on double sampling method that requires additional clock signal (CLK and CLK + Δ). Providing additional clock signals with fine timing margins is a costly and overwhelming challenge in ASIC design.
- In TRNoC architecture, once an error is detected, the requests from the affected input port should be stopped. During the next cycle (which is spent for error recovery), no request

should be sent to the output ports until the state of the affected input port returns to normal.

- In addition to the request-masking, at the time of error detection, all credit updates should also be stopped.
- The TRNoC architecture cannot handle receiving consecutive delayed dequeue signals at the input.

Time-borrowing circuit architecture along with hardware prototyping for timing error resilience has been studied in [109]. A technique called TIMBER has been employed for error resilience that masks the timing errors by borrowing time from successive pipeline stages in ASICs. The motivation behind TIMBER technique is the analysis of the distribution of critical paths in a processor, where only a small fraction of flip-flops serve as both start and end-points.

The time-borrowing technique is realized when the time borrowed from the next pipeline stage is absorbed by a noncritical path being sensitized in the next stage. This may lead to timing errors especially in high frequency applications. Therefore, the time-borrowing technique is not recommended for high frequency designs. As shown in Figure 2-12, the TIMBER-based error detection and masking mechanisms divide the checking period into three identical intervals; one interval for time borrowing (TB) and two intervals for error detection (ED). Thus, an increase in clock frequency is 30 /3 = 10% which delivers less benefit for high speed applications. A conventional master-slave TIMBER flip-flop comprised of two master latches and one slave latch. When the TIMBER flip-flop is configured in non time-borrowing mode, the slave latch serves to hold the previous data to drive the inputs to the subsequent pipeline stage. On the other hand, when the TIMBER flip-flop is configured in time-borrowing mode, two master flip-flops can switch between sampling data and driving the inputs to the subsequent pipeline stages. In view of this, the slave latch is not required in the circuit. The circuit design of the optimized TIMBER flip-flop is called *Dedicated TIMBER flip-flop*. Figure 2-13 shows the dedicated TIMBER flip-flop circuit along with the clock control design [109]. The key features of the dedicated TIMBER flip-flop architecture are summarized as :

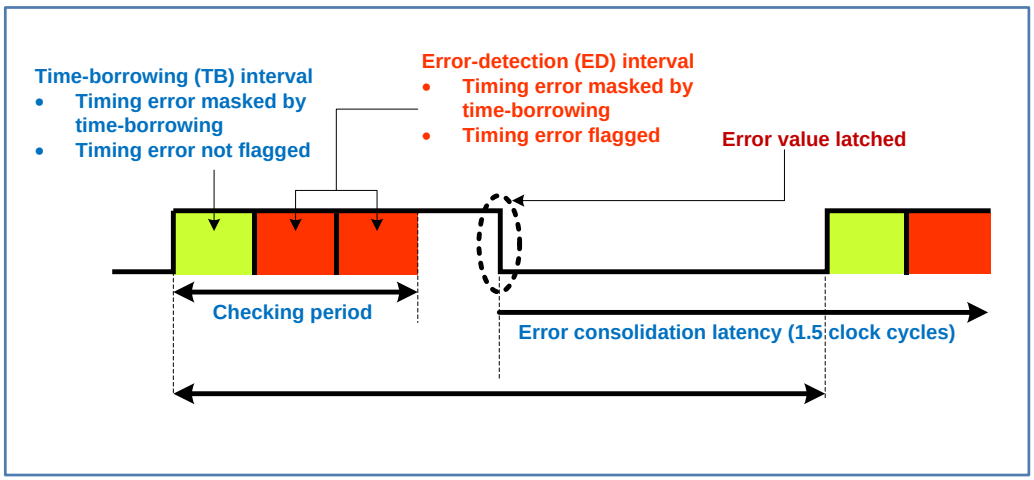


Figure 2-12 : TIMBER-based error detection and error masking technique [109]

- Replaying the faulty instruction or Roll-back the entire process,
- This technique is not effective for high speed applications since the time budget for time borrowing and error detection is limited.
- The timing error is propagated through at least three successive pipeline stages. Consequently, the performance improvement compared to traditional error detection schemes is not more than 10%.
- The main drawback of this technique is propagating glitches during the error detection process.
- Using inverter chains in control logic circuitry for delaying clock in TIMBER technique results in low resolution due to the large latency of the inverters.
- TIMBER technique decreases the slack time on critical paths which are linked since it adds a substantial delay on the critical path due to the large latency caused by delay inverters.
- This technique is only useful for low frequency applications and it cannot detect the timing error values of greater than 60 MHz.

A time redundancy technique to derive low-cost soft-error tolerant implementations for ASICs has been studied in [110], in which a perturbation tolerant circuit based on time redundancy has been designed. In a single-ended combinational circuit, hardware triplication is required in order to distinguish between correct and incorrect values. However, this is not the case for all the products because of the cost, area and power inefficiency. It is noted that it is possible to overcome this issue by exploiting the temporal nature of transient faults. Since the transient faults

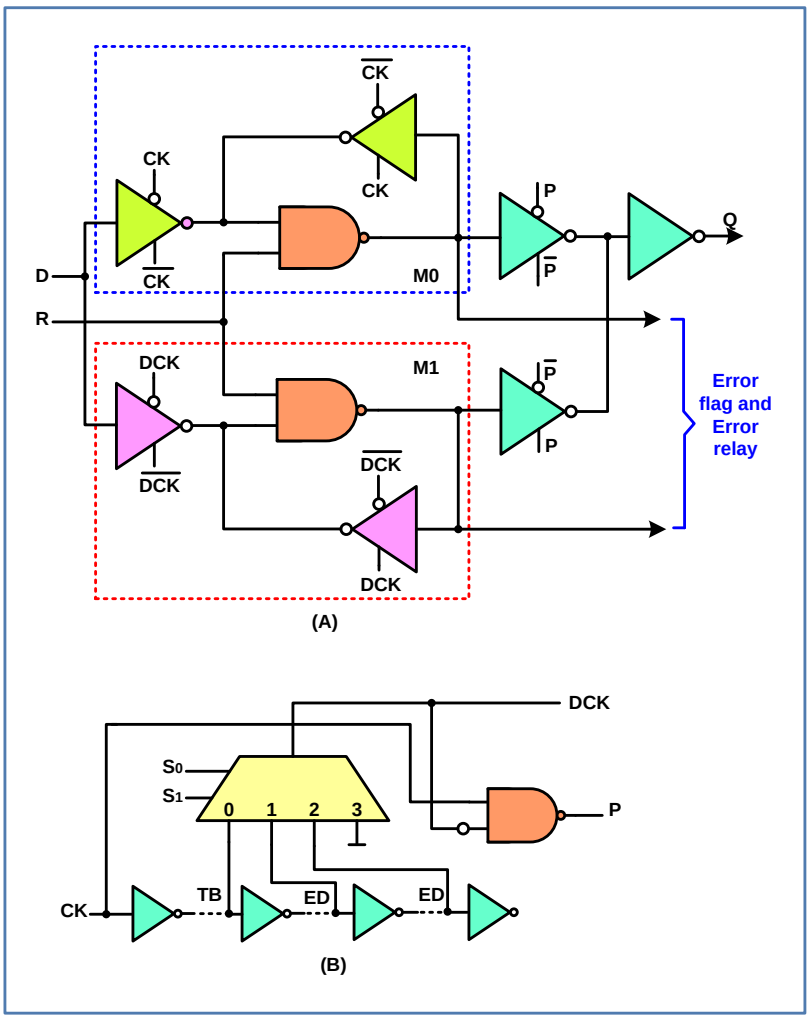


Figure 2-13 : Dedicated TIMBER flip-flop (A), and clock control design (B) [109]

manifest for a short period of time, only the majority voter circuit could be triplicated rather than the entire hardware.

Figure 2-14 shows the implementation of time-domain majority voter in [110]. The scheme is based on employing three latches with identical input (the single-ended output from combinational circuit) and delayed versions of the clock signal. As shown in Figure 2-14A, *Latch* 2 and *Latch* 3 are clocked with a certain delay of δ and 2δ compared to the clock of *latch* 1, respectively.

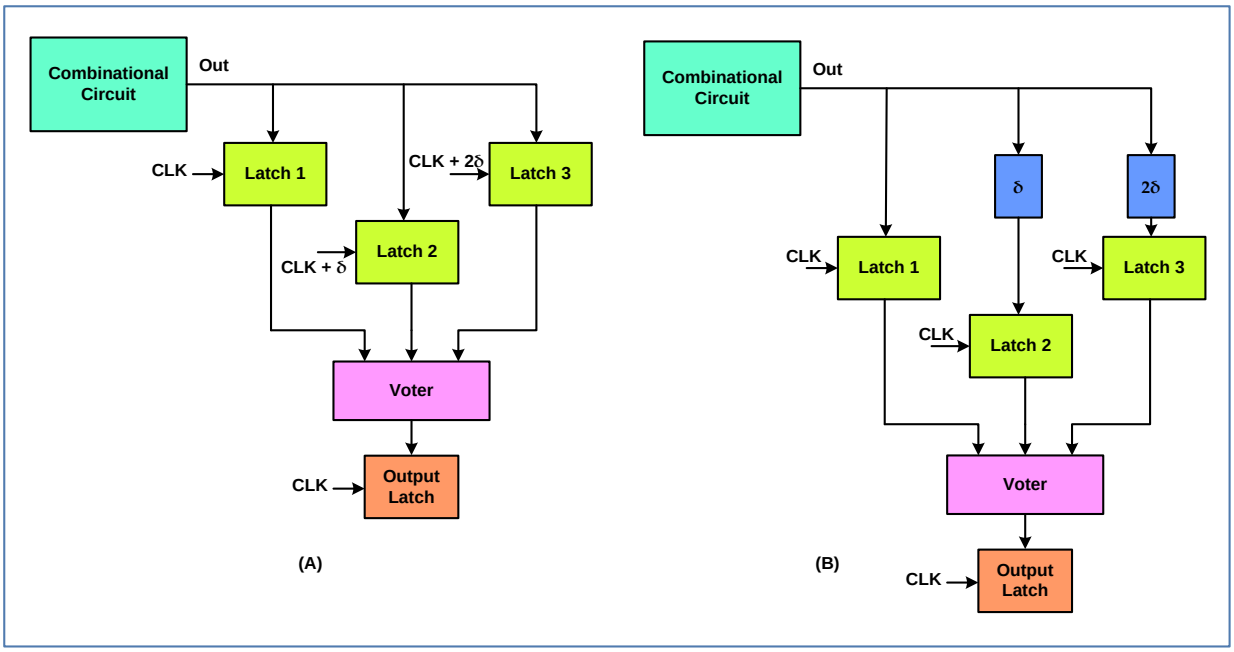


Figure 2-14 : Digital circuit implementation of time-domain majority voter; with delayed clock signals (A), and with delayed output signal (B) [110]

Employing the TMR architecture in time-domain majority voter along with redundant delayed clock signals (CLK + δ, and CLK + 2δ) is costly and also area and power inefficient. In addition, generating redundant clock signals with a certain delay value requires an accurate clock control circuit. Figure 2-14B shows an alternative design implementation where three latches share the same clock signal. The input of *Latch* 2 is delayed with a certain amount of δ and the input of *Latch* 3 is delayed by 2δ. The realization of this scheme is straightforward as compared to the one in Figure 2-14A. Error detection and correction (EDC) codes are the base functions of this technique that are suitable only for small designs. The time redundancy technique requires to repeat each circuit operation, the clock signal should be stopped and the faulty operation should be re-executed. The utilized TMR architecture induces substantially large amount of parasitic delays to the critical path of the DUT.

The Razor pipeline architecture has been presented in [111] and [112]. In Razor flip-flops' architecture, each Razor flip-flop comprises a main system flip-flop plus an assistant shadow latch linked to a multiplexer and an XOR gate. The main system flip-flop is clocked with system clock (CLK) while the shadow latch is clocked with a delayed version of the clock signal (CLK + δ). The delayed version of the output of combinational logic is presented at the latch output. The

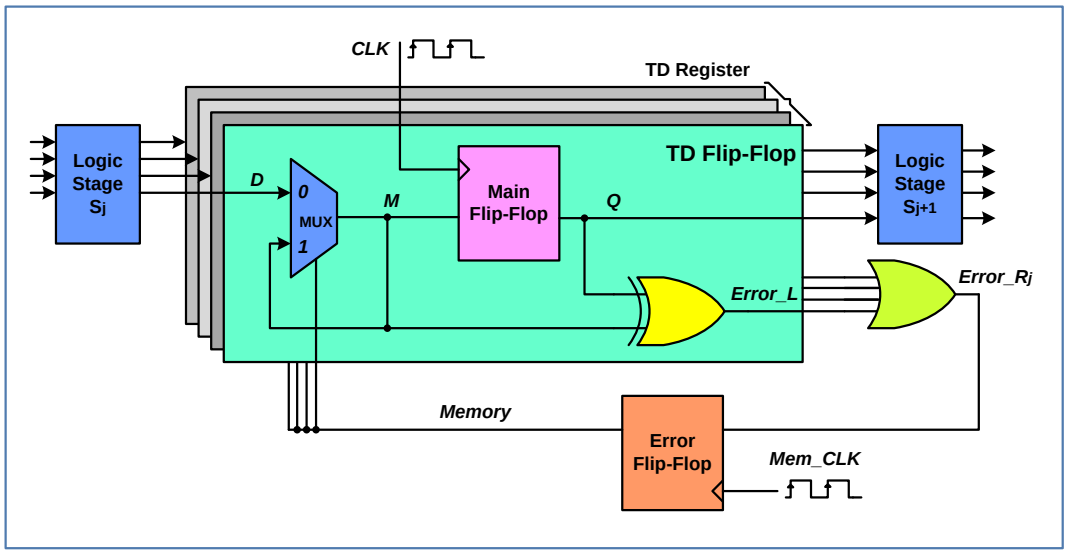


Figure 2-15 : Time dilation flip-flop for error detection and correction studied in [113]

XOR gate compares the outputs of the main system flip-flop and the shadow latch raising a flag once a difference is observed. The main drawback behind Razor flip-flop technique is high silicon area cost since a shadow latch, a multiplexer and an XOR gate are required for each main system flip-flop. In addition, the realization of the extra clock signal used in the architecture requires an accurate clock control circuit.

A time dilation technique that provides concurrent error detection and correction along with support of off-line manufacturing scan testing for ASICs has been studied in [113]. Employing new scan flip-flop architecture allowed detecting and correcting errors at the penalty of one clock cycle. The silicon area, cost and power consumption have been substantially reduced compared to the Razor design technique. Figure 2-15 shows the time dilation flip-flop architecture in [113]. The topology employs a multiplexer and an XOR gate linked to the main flip-flop in order to serve the timing error detection and correction. This topology is required for each main flip-flop in the system. In TD flip-flop topology shown in Figure 2-15, the error detection is performed by comparing the sampled input and output of the main flip-flop. The multiplexer with the feedback configuration forms a memory element, also called multiplexer-latch, which captures delayed data from the error flip-flop for error correction.

The error flip-flop is clocked with a delayed version of the main system clock. The features of the time dilation flip-flop architecture are summarized as follows :

- High silicon area cost due to the large extra logic gates insertion

- Performance degradation due to a complex circuit employed for error detection
- Required large number of control signals
- High penalty of latency in error detection due to the complex detection scheme
- TD flip-flop architecture is able to detect timing errors only in the range of nanoseconds and larger
- Generation of extra clock signal requires an accurate clock control circuit design

A robust digital sensor and sensor insertion flow for in-situ path timing slack monitoring in system-on-chips (SoC) has been presented in [114]. In this technique, the timing slack is converted to a digital format and stored in a scan register chain to be fetched at any time during test and operation modes. In addition, layout-aware and netlist-level sensor insertion flow have also been introduced. The sensor has been designed with 28 nm standard cell library. In the past few years, the CMOS technology is scaling down very quickly and paving the way for lots of core-processor and SoCs. However, the decreased transistor area per technology as well as the increased variability in MOS transistor parameters limits the technology scaling. The variations such as : static process variation due to manufacturing, dynamic variations such as power supply and temperature, and aging variations are increasingly emerged in the scaled down fabrication technologies. PVT variation and bias temperature instability have induced aging variations especially in smaller fabrication technologies of SoCs. The circuit diagram of the sensor architecture in [114] for the SoCs is shown in Figure 2-16. The capture flip-flop records the slack time of the circuit path at its D and Q ports. The D and Q ports are linked to the small size buffers in sensor block for the monitoring purpose. The small size of the buffers linked to the D and Q ports of the capture flip-flop ensures the low parasitic load added to the circuit path.

The data sampled by capture flip-flop is stored at the next rising edge of the clock inside the *rise transition detector* module. This value is compared with the data sampled by capture flip-flop at current rising edge of clock. The ACT flag is raised when the current data and the precedent data are mismatched. This flag is used to latch the states from *monitor unit* (MU) to the *capture and result storage unit* (CRSU). The delay line consists of a minimum size chain of buffers. The flip-flops attached to the end of the buffers capture the state of delay line at each rising edge of the clock signal. The delay line buffers and their associated flip-flops convert the timing slack into a corresponding digital data. The output data from MU is sampled by the flip-flops associated with the scan chain inside the CRSU module. In order to ensure the glitch immunity, the flip-flops in

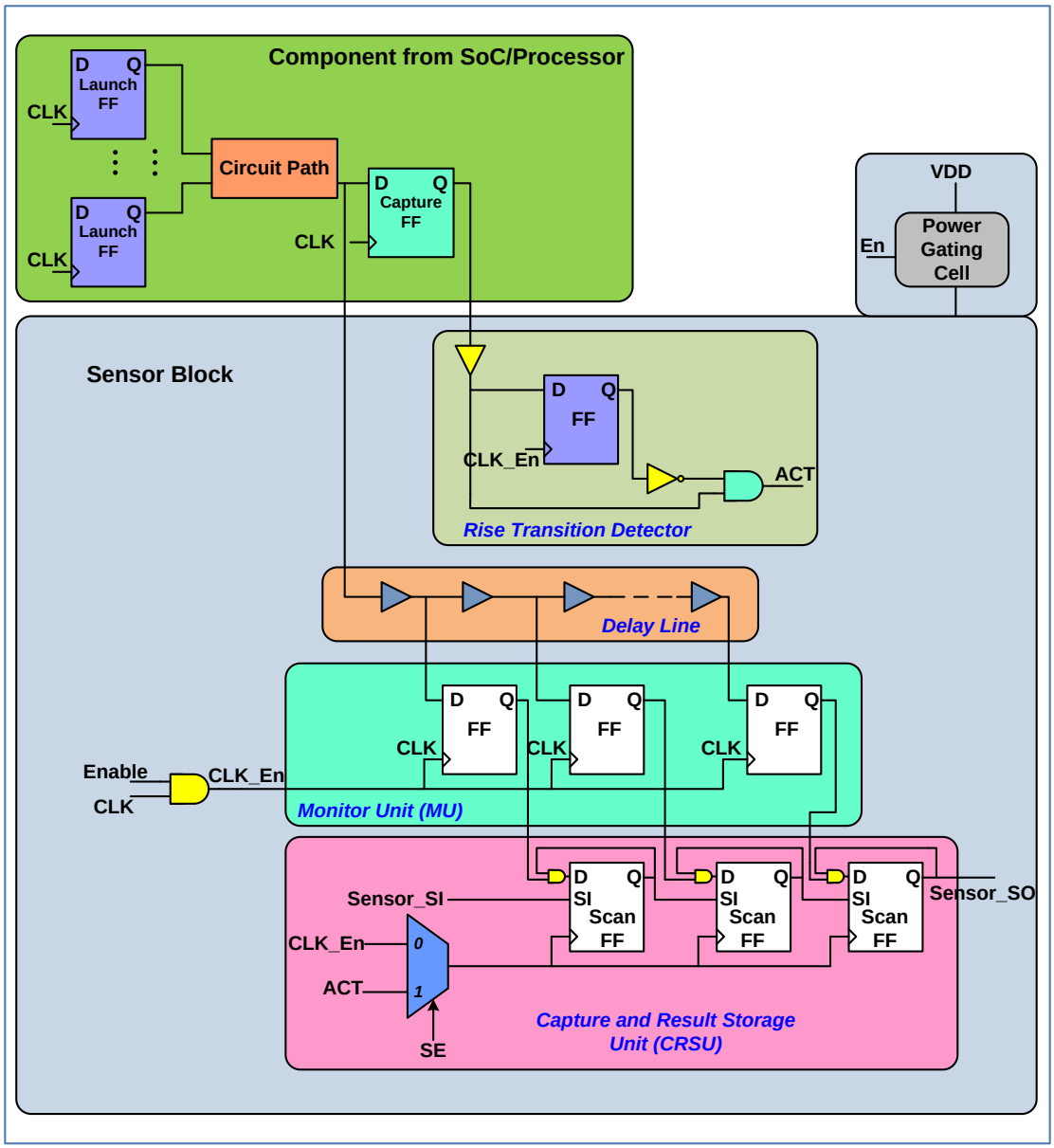


Figure 2-16 : Sensor architecture presented in [114]

this unit are clocked with the ACT signal rather than system CLK. The Sensor_SI signal is tied to a logic '1' that is considered as the scan input for the first flip-flop in CRSU module.

Employing minimum size buffers as delay line elements in the sensor architecture restricts its application to SoCs since the resolution of the delay intervals is limited to the net delay of each buffer. This sensor may not be a preferred solution for high speed application, where the slack time is narrower, especially for the designs relying on FPGAs.

2.9 Routing Fault Detection and Correction

In order to test and detect manufacturing defects in the interconnect structure of the FPGAs, several techniques have been presented. Most of these techniques rely on BIST that exhaustively tests all cross-points in the switch matrices in order to find the faulty point [115-119].

Test pattern generators (TPG) are another technique to detect the faults in interconnections [80], [81]. The algorithm in [120] relies on the technique used in [119], which employs linear feedback shift register (LFSR) in order to generate multiple test configurations from a single test configuration. Self-testing areas (STAR) technique in [82] is comprised of several disjoint tiles to scan the FPGA for fault detection. The tiles include a basic BIST architecture called BISTER and apply some test patterns to the blocks under test and the wires under test.

In order to detect the faulty cell, the STARs are roved across the FPGA based on the concept of partial reconfiguration. The drawback of the STAR technique is interrupting the entire system for one to three seconds, since the BISTER tiles have to be reconfigured in order to rove the STARs. Thus, the performance of the system employing the STAR technique is substantially degraded. Another disadvantage of this technique is the increased latency for fault detection by increasing the design complexity implemented to the FPGA. This is due to the fact that the roving time increases with the number of tiles that are used to implement the design.

A partitioning method for interconnect fault recovery has been studied in [121]. It partitions the physical design into a set of tiles where each tile comprises of some logic blocks and routing interconnects. In order to provide a reliable logic and local interconnection in the implemented design, multiple configurations have been considered. Correcting the configuration upsets in this method has been performed by swapping the configurations for each tile independently. However, this technique requires some spare logic resources for the case of logic faults in LUTs and also some global interconnects for the case of fault in the segmented interconnects. Once a routing error is detected, reconfiguration of the FPGA is sufficient to mitigate the fault. However, reconfiguration of the FPGA entirely takes more time, and thus the time required for fault detection should be significantly lower than the time taken for the FPGA reconfiguration.

In the technique presented in [122], the routing faults such as stuck-at faults and bridging faults in the SMs of the FPGA have been detected via a test configuration. This technique relies on sending different values across every two nets that are routed through a common SM. The bitwise parity value received by the inputs of a LUT is compared with the pre-computed parity value and

in the case of a distinct value, a routing error is reported. Taking advantage of the partial reconfiguration, the cost and time for an entire FPGA's reconfiguration is decreased. Therefore, the time required for fault detection in the routings is lower as compared to other existing works discussed in Section 2.9. However, large area overhead, power consumption increase, and significant delay added to the routings due to the excess number of logic gates are the main drawbacks of this technique. In view of this, this technique may not be generalized to high speed applications. In addition, reconfiguration of the entire design at the time of fault detection in routings is another issue that makes this technique inefficient.

2.10 Coherence of the Articles in Relation to the Research Goals

In the last two chapters up to now, we discussed the current challenges regarding the impact of cosmic rays on electronic components employed in the aircrafts that travel at very high altitudes. The SRAM-based FPGAs have attracted a great deal of interest in aerospace and aeronautic sector due to their system integration, high configurability, and flexibility. However, they are very susceptible to cosmic rays. The susceptibility of the SRAM-based FPGAs to SEEs particularly the SEU has been extensively studied in the literature. We reviewed the state-of-the-art of SEU effects in SRAM-based FPGAs as well as the existing mitigation techniques in CHAPTER 2. However, the vulnerability of the routing resources of the FPGAs to SEU, to the best of our knowledge, has been overlooked thus far. Since in modern FPGAs almost 90% of configuration bits control the routing resources, it is desired to investigate the sensitivity of the routing network to SEU.

This thesis is based on three journal articles. In the first article, the susceptibility of routing resources in an SRAM-based FPGA to SEU is presented while the device has been exposed to ionizing proton radiation to induce DCs. In the first report on the observation of DCs in the routing resources of the SRAM-based FPGAs by members of our research team, a hypothesis has been suggested for the root cause of the observed DCs. In this article, circuits involved in delay change generation and propagation are reverse-engineered with precise models using the Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm CMOS technology, similar to the 65 nm triple-oxide technology node used to build Xilinx Virtex-5 FPGA.

In the second article, a delay monitor circuit is proposed to detect and measure the DCs observed in the experiment performed on an SRAM-based FPGA. The observed DCs presented in the first

article can be detected with the proposed delay monitor and the results are compared to those obtained experimentally and by circuit level simulations. In this paper, based on the results obtained, we claim that as the level of DC detection increases, the probability of receiving more DCs in the routing resources of an SRAM-based FPGA will increase. In addition, it is shown that the proposed delay monitor circuit can be a part of mitigation technique for SEUs targeting routing interconnection network of the FPGA. A method to lower the clock frequency at the time of DC detection is proposed in order to tolerate further DCs on the critical path and avoiding system downtime.

In the third article, an investigation on the vulnerability of routing resources in APSoC devices including SRAM-based FPGA is presented. The in-beam neutron experiments are performed at TRIUMF laboratory. In this article, a method to configure ring oscillators mostly with routing resources and a few logic resources with full control over the routings is proposed. Also, an algorithm to automatically identify the extra parasitic interconnects linked to a logical net due to SEU is proposed. In this article, it is shown that there exists a relation between the order (level) of DCs and the probability of getting more DCs. Results obtained for each RO support the trend that as DCs occur, the probability of getting a subsequent DC increases as shown be the steady decrease of the mean time to delay change (MTTDC) as the order (level) of DC occurrence increases.

CHAPTER 3 presents the first article on the circuit level modeling of extra combinational delay in SRAM-based FPGAs due to transient ionizing radiation. CHAPTER 4 covers the second article with the emphasis on the design and implementation of a delay monitor circuit for the DCs induced by SEU in SRAM-based FPGAs. CHAPTER 5 presents the content of the third article in which the characterization of the susceptibility of routing resources in SRAM-based FPGAs to SEUs induced by ionizing radiation is investigated. A general discussion on the objectives of this thesis and the achievements obtained are presented in CHAPTER 6. Finally, some concluding remarks and scope for future research are outlined in CHAPTER 7.

2.11 Summary

In this chapter, a review of the state-of-the-art works regarding different topics related to this thesis has been presented. SEE effects in digital ICs and FPGA fabrics have been reviewed with an emphasis on the SEU. Related radiation experiments and SEE characterization methods on the

SRAM-based FPGAs have been reviewed. Available SEU mitigation techniques as well as the detection and correction schemes applied to the FPGAs have been presented. A review on TDCs implemented in FPGAs has been presented. Finally, the available fault detection and correction techniques applied to the routings of the FPGAs have been reviewed.

CHAPTER 3 ARTICLE 1 : CIRCUIT LEVEL MODELING OF EXTRA COMBINATIONAL DELAYS IN SRAM-BASED FPGAS DUE TO TRANSIENT IONIZING RADIATION

3.1 Overview

The SRAM-based FPGAs are sensitive to ionizing radiation inducing SEU. These semiconductor devices are structured in an array of Configurable Logic Blocks (CLB) connected via a programmable routing interconnection network. Routing interconnection network is controlled by SRAM cells that are called configuration bits which are susceptible to SEU. An SEU may change the configuration of a programmable interconnection point (PIP) controlled by an SRAM memory cell in SRAM-based FPGAs. PIPs are the main components that contribute to route a source to a destination component. This chapter is the reproduction of a published article in IEEE Transactions on Nuclear Science.

– M. Darvishi, Y. Audet, Y. Blaquière, C. Thibeault, S. Pichette, and F. Z. Tazi, "Circuit Level Modeling of Extra Combinational Delays in SRAM-Based FPGAs Due to Transient Ionizing Radiation," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 3535-3542, 2014.

3.2 Abstract

This paper presents circuit level models that explain the extra combinational delays in a SRAM-based FPGA (Virtex-5) due to Single Event Upsets (SEUs). Several scenarios of extra combinational delays are simulated based on the circuit architecture of the FPGA core, namely Configurable Logic Blocks (CLBs) and routing. It is found that the main delay contribution originates from extra interconnection lines that are unintentionally connected to the main circuit path via pass transistors activated by SEUs. Moreover, longer delay faults observed on Input/Ouput Blocks (IOBs) due to SEU were investigated through simulations. In all cases, results are in close agreement with the ones obtained experimentally while exposing the FPGA to proton irradiation.

3.3 Introduction

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around an array of Configurable Logic Blocks (CLBs) connected via a hierarchy of configurable interconnects [21]. FPGAs have become the preferred common solution to implement digital systems targeting different applications [17]. The SRAM-based FPGA comprises some I/O blocks (IOBs), memory modules, logic blocks and routing resources controlled by SRAM cells, called configuration bits [21]. The sensitivity to radiation of SRAM-based FPGAs has been studied over the years [52, 123-126]. The first report on extra combinational delays due to transient ionizing radiations has recently been presented in [32] where their existence due to Single-Event-Upsets (SEUs) induced by proton radiation has experimentally been observed.

The main contribution of this paper is the validation of the root causes of extra combinatorial delays, also called Observed Delay Changes (ODCs), on SRAM-based FPGA through circuit level simulations of the internal circuitry of Configurable Logic and I/O Blocks [127-129] and their interconnections.

This paper presents circuit models created to understand and simulate the source of extra combinational delays experimentally observed, which are ranging from 22 psec to as much as 422 psec in the core logic of FPGA [32]. To our knowledge, the proposed model and methodology represent the first work ever on the simulation of extra combinational delays due to SEU occurring in FPGAs. The models are accurate enough to obtain close correlation with the experimental results. The proposed methodology can also be used to predict the probable delay values due to radiation in any design implemented on FPGA.

The effects of SEUs on delay faults affecting the Virtex-5 IOBs were investigated and some substantially larger delay changes were observed while exposing the FPGA to irradiation [36]. The root cause of these large observed delay changes was verified in this paper with, circuit level simulations employing the Input/Output Buffer Information Specification model (IBIS) [130]. FPGA irradiation experiments were also performed at the TRIUMF laboratory using a variable energy and fluence proton beam [36].

This paper is structured as follows. Some background information regarding the previous work is presented in Section 3.4. Section 3.5 describes FPGA's circuit level models for observed delay change root cause validation. Typical circuit-level configurations that could induce ODCs in the core of SRAM-based FPGA are presented in Section 3.6. Simulations of SEU effect on delay

faults affecting the Virtex-5 IOBs are presented as well as the comparison between simulation results and experimental ones observed by proton irradiation for both core-based and IOB-based Ring Oscillator (RO) circuits are discussed in Section 3.7, and finally, conclusions are drawn in Section 3.8.

3.4 Background on Extra Combinational Delays in SRAM-Based FPGAs

Configuration memory cells in SRAM-based FPGA are sensitive to radiation that causes a bit-flip of the stored values [34, 131, 132]. These SRAMs are mainly used to configure interconnects, look-up tables and I/O blocks. The two impacts of a bit-flip on configuration bits related to interconnections are open, a disappearing link between two nodes; or short, usually defined as an undesired connection between two routed signals. While SEU can modify logic behavior in SRAM-based FPGA, it was conjectured in [32] that delays could be induced by a short between a routed path and an unused wire.

Figure 3-1 illustrates the experimental setup that was utilized at the TRIUMF laboratory to demonstrate the induced extra delays in SRAM-based FPGA. Extra combinational delays were observed while the board was bombarded by protons of energy ranging from 35.4 MeV to 105 MeV for several runs. The Xilinx Virtex-5 FPGA (XC5VLX50T) was used to implement two ring oscillators, RO1 and RO2, made of look-up tables (LUTs) configured as inverters in the core of Virtex-5 operating at similar frequencies. The output of each ring oscillator was connected to an external inverter (7404). The outputs of the two 7404 inverters were shorted by a 5.1 kΩ resistor while one inverter output is monitored by a spectrum analyzer. The resistive shorted outputs provide a signal with a frequency spectrum containing the frequency difference between the two RO frequencies (F_2 - F_1). This difference is mainly due to the parameter variation in fabrication process and slight difference in the oscillator's routing. The measurement of the frequency difference (F_2 - F_1) instead of the individual frequency F_1 or F_2, led to a better resolution. The ring oscillators were adjusted to the length of 1799 inverters giving $F_1 \approx F_2 \approx 1.25$ MHz and a frequency difference of about 12.4 kHz. The supply voltage (V_{CC}) for inverter chip (7404) was 1.2 V, while the supply voltage for the core and the inputs/outputs of the FPGA was 1.0 V and 3.3V respectively. Other experiments were performed with ring oscillators implemented in IOB and will be described in section 3.7.2.

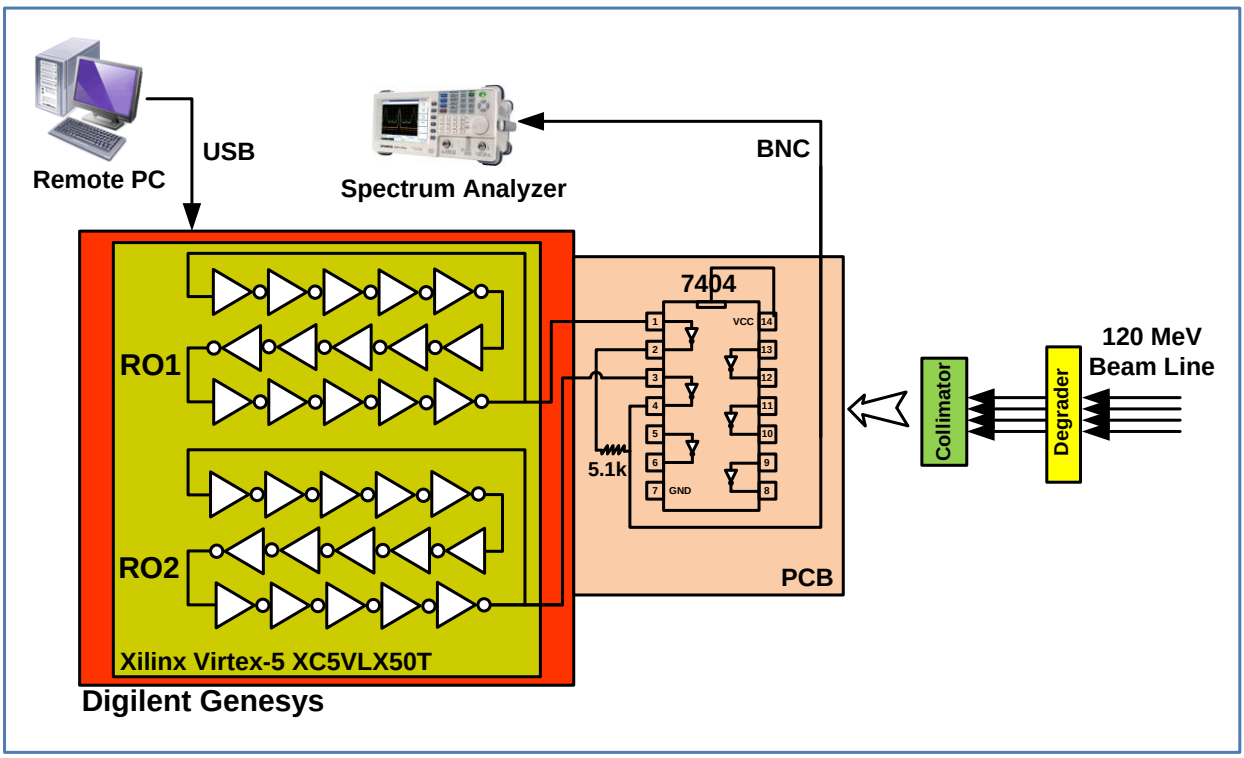


Figure 3-1 : Experimental setup used by AVIO403 team at TRIUMF to measure extra delays [32]

3.5 FPGA Circuit-Level Models for ODC Root Cause Validation

A set of 48 experiments were performed in which the proton source bombarding the top side of the FPGA. Each delay measurement was stopped when the oscillation of one RO ceased due to a functional failure triggered by an SEU. Twenty three of those experiments came with one or cumulative ODCs. The delay change could produce either a reduction or an increase of the measured frequency difference depending on which of the two ring oscillators was affected.

3.5.1 Circuit Level Models

One contribution of this paper is to present circuit level models of the FPGA that takes into account the CLB along with their interconnection modules in order to simulate SEU-induced delays. The Virtex-5 FPGA is based on an array of configurable logic blocks with two slices each [21]. The circuit is modeled as a two dimensional array comprising slices and switch boxes/switch matrices (SB) interconnected by a network of routing wires as shown in Figure 3-2. Xilinx does not formally provide any detail on internal Virtex-5 FPGA circuitries. However, according to [127, 128], SBs are made of an array of nMOS pass transistors with some vertical

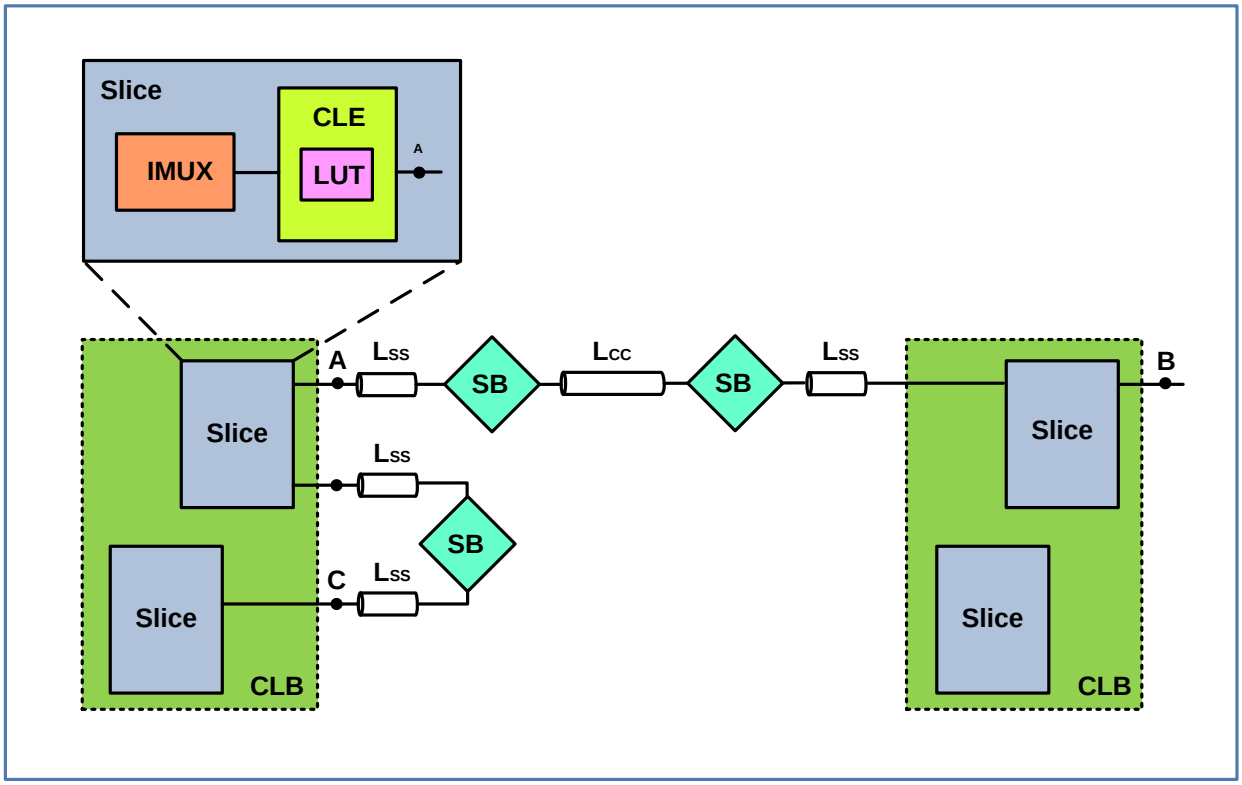


Figure 3-2 : Model of a two configurations of slice to slice interconnection in Virtex-5

and horizontal interconnects inside. A slice includes a Configurable Logic Element (CLE) and 8:1 input multiplexers (IMUX). Also, the CLE is comprised of a LUT [133].

Figure 3-2 presents the top level view of two adjacent CLBs, where two different configurations of slice-to-slice interconnection are shown as examples. The first configuration, path A-to-B, is introduced to simulate the behavior of direct slice-to-slice link of the RO between two adjacent CLBs. The second configuration, path C-to-A, represents the other possible interconnection between two slices in a same CLB. Both configurations are reported by the Xilinx FPGA Editor tool [28]. In the first configuration, the CLB-to-CLB interconnection length, L_{CC}, is longer than the Slice-to-SB interconnection length, L_{SS}, in the second configuration. These configurations are introduced as models for ROs implemented on FPGA enabling the prediction of the probable ODCs.

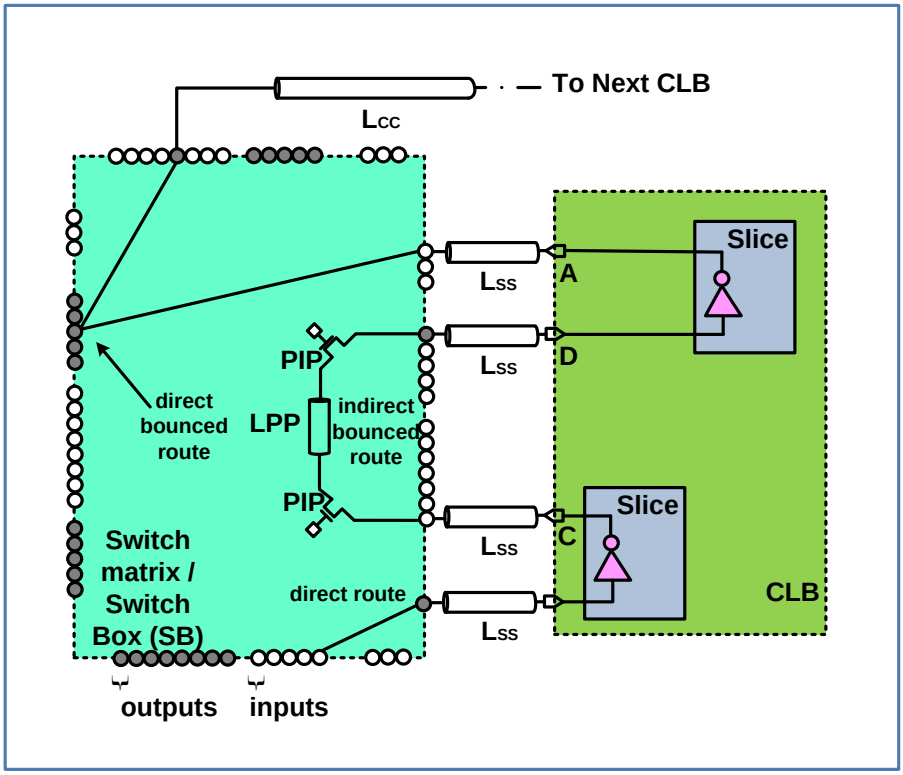


Figure 3-3 : Switch matrix structure reported by Xilinx FPGA Editor including our equivalent circuit for the second configuration

3.5.2 Model Configuration Tuning

Figure 3-3 represents our circuit model for the main switch matrix structure used by ROs, as reported by the Xilinx FPGA Editor tool. The model includes the location of pass transistors (PIP) and the Pass-transistor to Pass-transistor interconnection, L_{PP}, (bounce model) for nodes C-to-A configuration of Figure 3-2.

A signal crosses the switch box SB from their input to output pins (circles in Figure 3-3) via vertical and horizontal interconnects and through Programmable Interconnection Point (PIP) made of pass transistors. Indeed, based on the Xilinx FPGA Editor tool, an input signal can be routed directly to one or more output pins through a single PIP, named direct route. Also, it is possible to bounce the input signal indirectly through an intermediate interconnect and PIP and then fed to an output pin, named indirect bounced route. Two bounced routes are shown in Figure 3-3. An indirect bounced route would be typically used for a C-to-A route while a direct bounced route is used for A-to-B configuration shown in Figure 3-2.

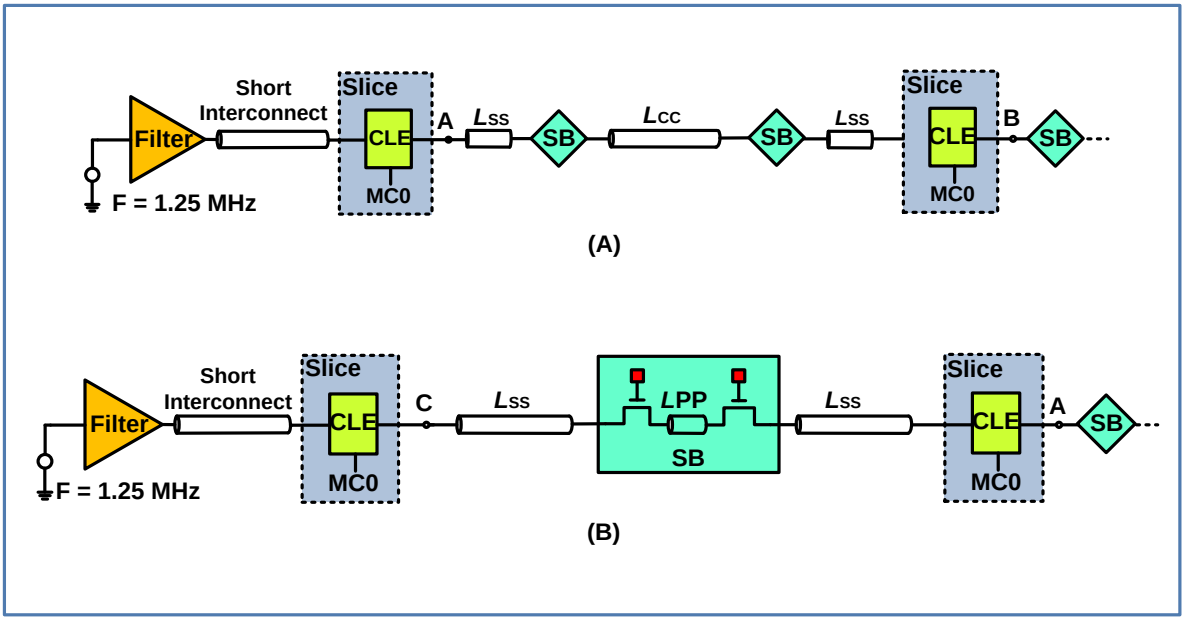


Figure 3-4 : Structure of slice-to-slice interconnection A) between two adjacent CLBs, B) in a single CLB

The circuit models employed to simulate both interconnect configurations of the RO implementation used in the experiments are detailed in Figure 3-4A (path A-to-B) and Figure 3-4B (path C-to-A), respectively. A signal shaping filter comprised of four inverters generates a realistic pulse signal waveform. According to Figure 3-4A, any interconnection between two slices located in two adjacent CLBs has to pass through two switch boxes with an interconnection length of L_{CC}. In Figure 3-4B, the interconnection between two slices located in a same CLB passes through a switch box with two interconnections of length L_{SS}. The switch box is comprised of an array of pass transistors and very short interconnections shown as L_{PP} in Figure 3-4B. Our simulations show that the effect of L_{PP} on propagation delays is negligible compared to the one of a pass transistor along the path.

The proposed models have been adjusted to match the delay extracted from the Xilinx ISE Static Timing Analysis (STA- TRACE) tool [134] run on the place and route netlist and used for the proton irradiation experiments. Simulations were performed with Cadence Spectre circuit simulator [135] having the interconnect lengths L_{SS} and L_{CC} configured as the sweeping variables for both configurations using the Taiwan Semiconductor Manufacturing Company (TSMC) 1.2 V 65 nm CMOS technology [136], similar to the 65 nm triple-oxide technology node used to build

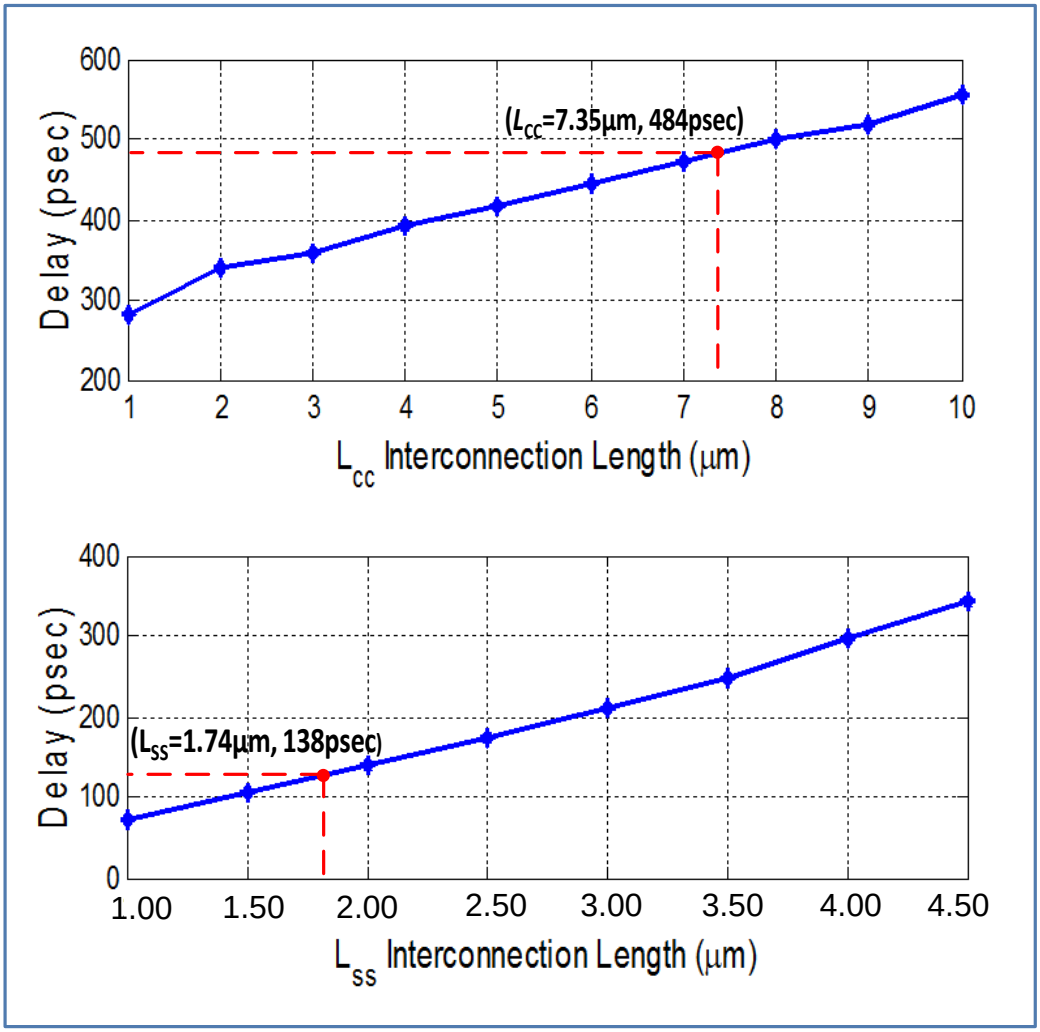


Figure 3-5 : Delay variation as a function of short interconnection length for the configurations used to define L_{CC} in Figure 3-4A and L_{SS} in Figure 3-4B

Xilinx Virtex-5 FPGA. Simulations were performed with minimum size transistors and the metal3 layer for interconnects.

Figure 3-5 presents the propagation delay results from Slice-to-SB (node C to node A) and Slice-to-Slice (node A to node B) as a function of the interconnection length to adjust L_{SS} and L_{CC} in the first and second configurations. We found that an interconnection length of L_{SS} = 1.74 µm in the second configuration (node C to node A) matches the inverter and net delay of 138 psec that was extracted by Xilinx STA-TRACE. The same procedure was performed to match the value of L_{CC} in the first configuration (node A to node B) and the corresponding value amounts to 7.35 µm, which matches the net delay of 484 psec. Our simulation results showed that the effect

of L_{PP} on the delay is negligible compared to PIP's effect, so its value was neglected. As shown in the following section, the adjusted lengths L_{CC} and L_{SS} and our circuit models provided sufficient accuracy to reproduce the ODCs observed experimentally.

3.6 Circuit Level Configurations Inducing ODCs in FPGA Core

An SEU in SRAM-based FPGA can affect a configured circuit by creating a short, an open or a modification in the propagation delay. Indeed, it is assumed in this paper as in [32] that the experimentally observed delay change is caused by an SEU that increases the interconnect load parasitic capacitance. Under these circumstances, three circuit scenarios of delay changes were investigated, as explained in the following subsections.

3.6.1 Models for Delay Change Due to Extra Parasitic Interconnects

An SEU affecting an SRAM-cell controlling a PIP could create a short, for example, between a vertical line and the main horizontal routing line, as shown in the simplified schematic view of Figure 3-6A. This model is valid for both inter-slice routing configurations presented in Figure 3-3. According to our simulation results, the main contributor to the delay is the PIP pass-transistor that is turned 'on' and increases the parasitic capacitance by connecting an undesired vertical unused interconnection to the main routing path. While Figure 3-6A is an example of a single interconnect parasitic (1-SEU case), Figure 3-6B shows that cumulative SEUs can create larger parasitic load than the 1-SEU case on the main routing path. In Figure 3-6B, it is assumed that a primary SEU affected the configuration bit of the SRAM-cell and turned on the corresponding PIP pass transistor and made a permanent connection between one horizontal and one vertical interconnect that are not yet connected to the main routing path. The extra capacitance is added on the main routing path when another SEU flips the configuration bit of the SRAM-cell that connects the two former parasitic lines to the main routing path and therefore creates an extra parasitic delay. Figure 3-7 illustrates a 3-SEU case where an even larger combinational delay is created by a sequence of three consecutive SEUs. The first two SEUs enabled PIP_B and PIP_C, and then another SEU activated PIP_A to create a combinational delay larger than the one observed in the 2-SEU case.

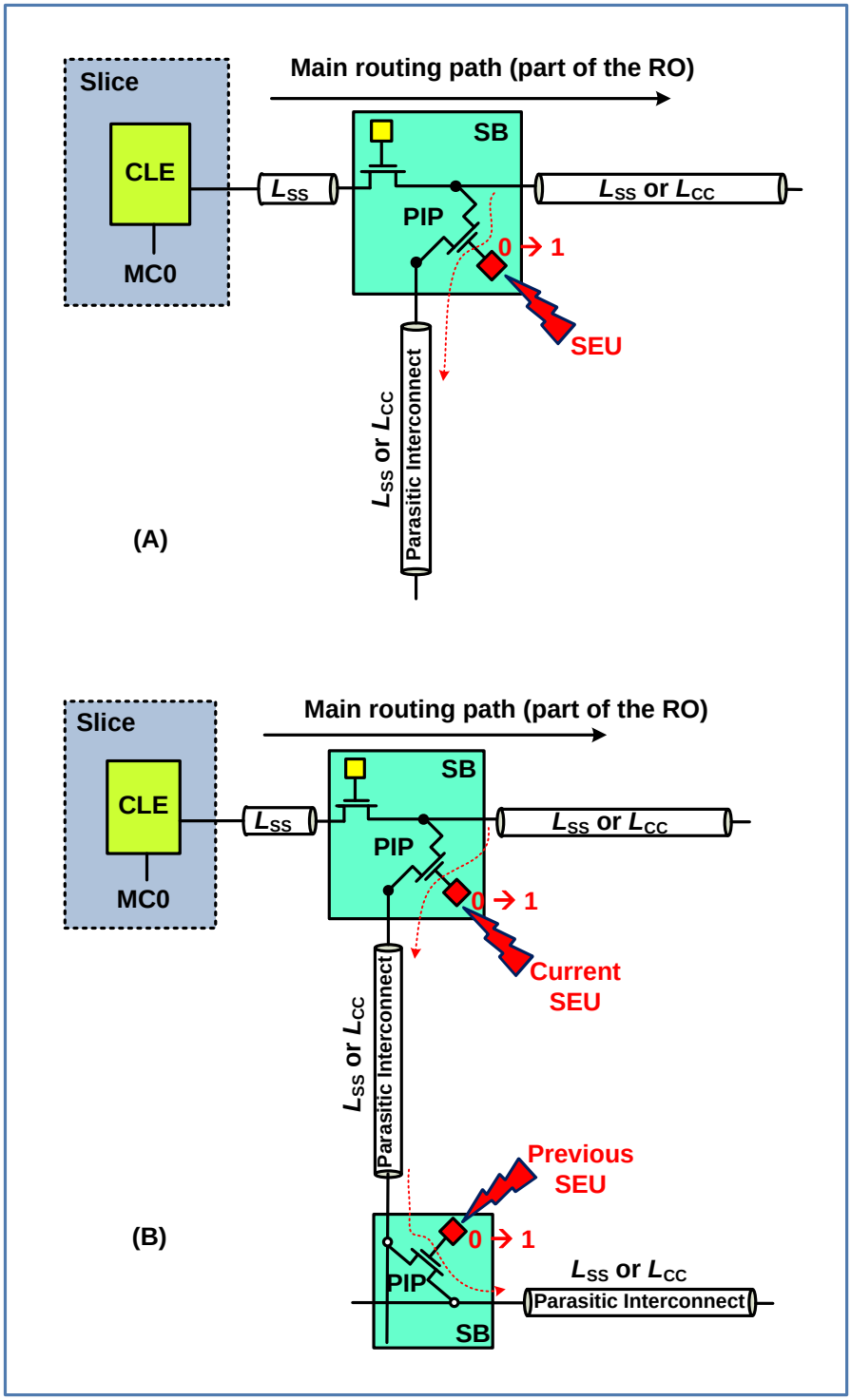


Figure 3-6 : Effect of an SEU on a Programmable Interconnection Point (PIP) in SB, adding a combinational delay : A) 1 ODC case (1 SEU), B) 2 ODC case (2 SEUs)

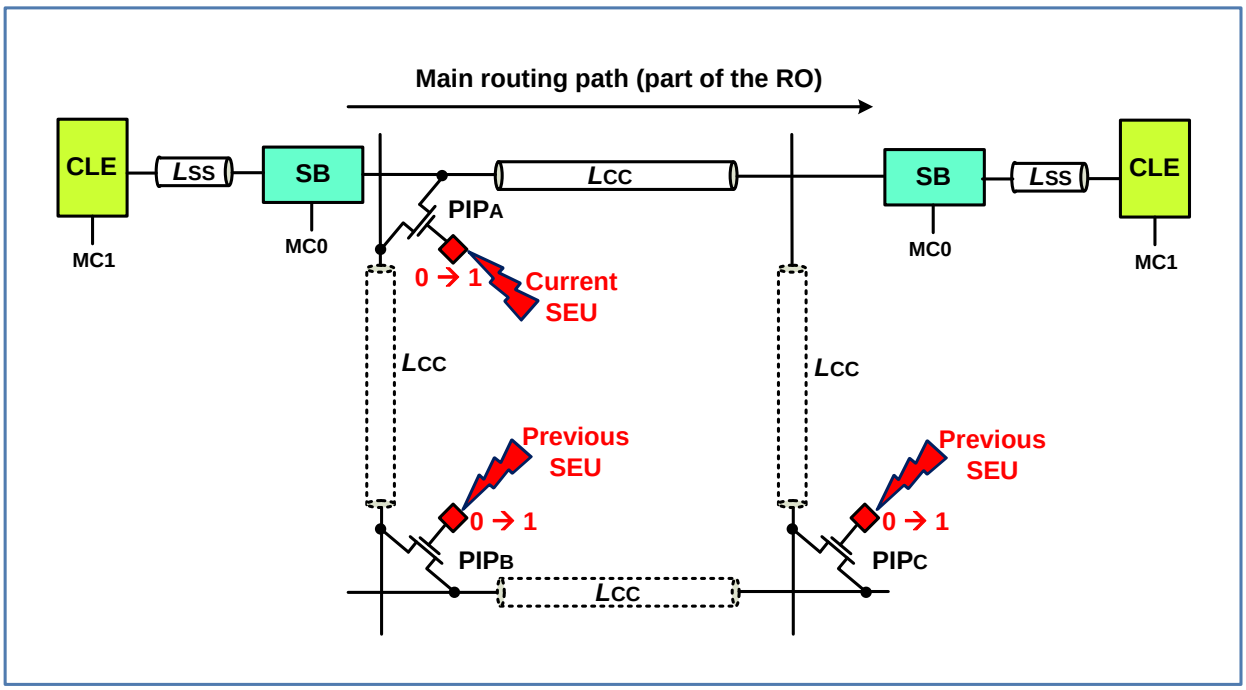


Figure 3-7 : A sequence of three SEUs connecting three interconnects of length $1L_{CC}$ to the main routing path

It is noticeable that the presented structures can be applied for both configurations introduced in Figure 3-3. In our convention, for the configuration presented in Figure 3-4B, the (1) case was simulated, which means 1 SEU has shorted a parasitic interconnect to the main routing path while its length is $1\ L_{SS}$. The (1), (2) and (4) cases were simulated for the configuration presented in Figure 3-4A, while an SEU has connected a parasitic interconnect to the main routing path with the lengths of $1\ L_{CC}$, $2\ L_{CC}$ or $4\ L_{CC}$, respectively.

Notice that regarding the probable interconnection lengths in Virtex-5, direct CLB-CLB connections in Virtex-5 FPGA can be $1\ L_{CC}$, $2\ L_{CC}$ or $4\ L_{CC}$ [129, 137], as shown in Figure 3-8. More scenarios have been simulated for the configuration of Figure 3-4A that includes 2-SEU and 3-SEU cases. The nomenclatures of (1,1), (1,2), (1,4), (2,1), (2,2), (2,4), (4,1), (4,2) and (4,4) are defined while the main routing path is affected by 2 SEUs. For instance, the case (1,1) identifies a cumulative case where two parasitic interconnects with the length of $1\ L_{CC}$ due to two consecutive SEUs are connected to the main routing path as shown in Figure 3-6B. Also, the case (1,2) implies two parasitic interconnects with the length of $1\ L_{CC}$ and $2\ L_{CC}$ respectively connected to the main routing path. The case (4,4) represents two parasitic interconnects both with the length of $4\ L_{CC}$ linked to the main routing path.

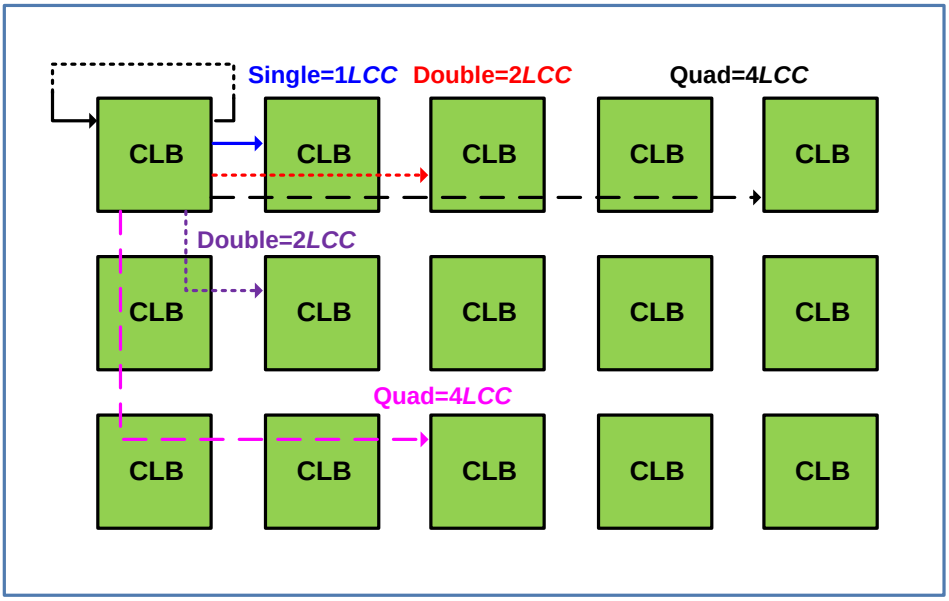


Figure 3-8 : Examples of various interconnection lengths in Virtex-5 FPGA [129, 137]

In addition, different scenarios were simulated for a sequence of three SEUs where the equivalent of three interconnects of lengths (*1*, *2* or *4*) L_{CC} become connected to the main routing path between two slices located in two adjacent CLBs. The proposed nomenclatures for the sequence of three SEUs are as the following : (1,1,1), (1,1,2), (1,1,4), (1,2,1),…, (4,4,4) for a total amount of 27 cases. For instance, the (1,1,1) case introduces the case where three parasitic interconnects due to three consecutive SEUs are connected to the main routing path, while their length equals to $1L_{CC}$, as illustrated in Figure 3-7. Notice that the delay change created by the (4,4,4) case is quite larger than the delay change due to (1,1,1) case. It is noticeable that the horizontal interconnect length for both configurations presented in Figure 3-4 is the unit length that is kept constant at L_{CC} = 7.35 µm or L_{SS} = 1.74 µm.

3.6.2 Models for Delay Change Due to SEU Effect on IMUX

As stated in Section 3.5, the IMUX circuit couples the input terminals of CLE to the general interconnect. The assumption for delay change due to pass transistors in IMUX is illustrated with the example in Figure 3-9. In this case, the main routing path passes through pass transistors M1 and M2 while M4 is off and its configuration bit is '0'.

Once an SEU affects the configuration bit of the SRAM-cell MC2 that controls the pass transistor M4, it creates a bit-flip that makes M4 ‘on’. Since M3 was previously driven by activated

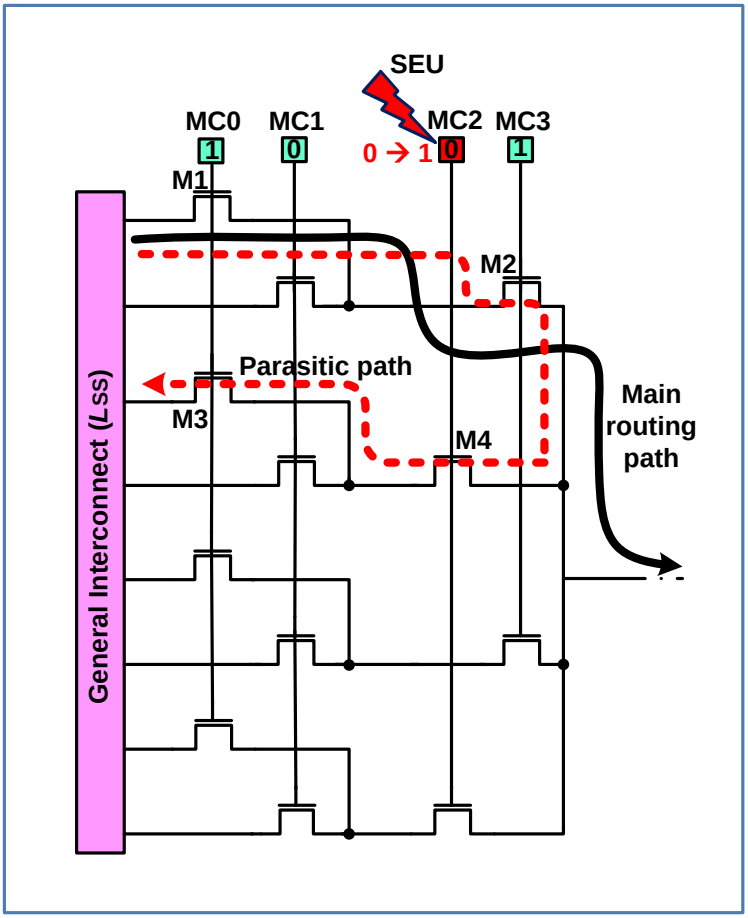


Figure 3-9 : Mechanism of delay change creation in IMUX circuit

configuration bit MC0, a parasitic path (dotted) is created via M1, M2, M4 and M3 back to the general interconnect that is assumed to be L_{SS}. This SEU on MC2 produced a noticeable delay change of 26 psec found by our circuit level simulation.

3.6.3 Models for Delay Change Due to Extra Stuck-at Parasitic Interconnect

Furthermore, another phenomenon observed in FPGA is caused by an extra parasitic interconnect that is stuck-at logic state '0' or '1' [138, 139]. This situation can occur when a logic node is tied to a specific logic value (by the synthesis tool or the designer). Indeed, examinations of some XDL files describing existing routed designs revealed that the tied specific logic value could pass through up to 5 PIPs before reaching its final destination. On a main routing path, this parasitic stuck-at interconnect can create a stuck-at fault or induce an extra combinational delay.

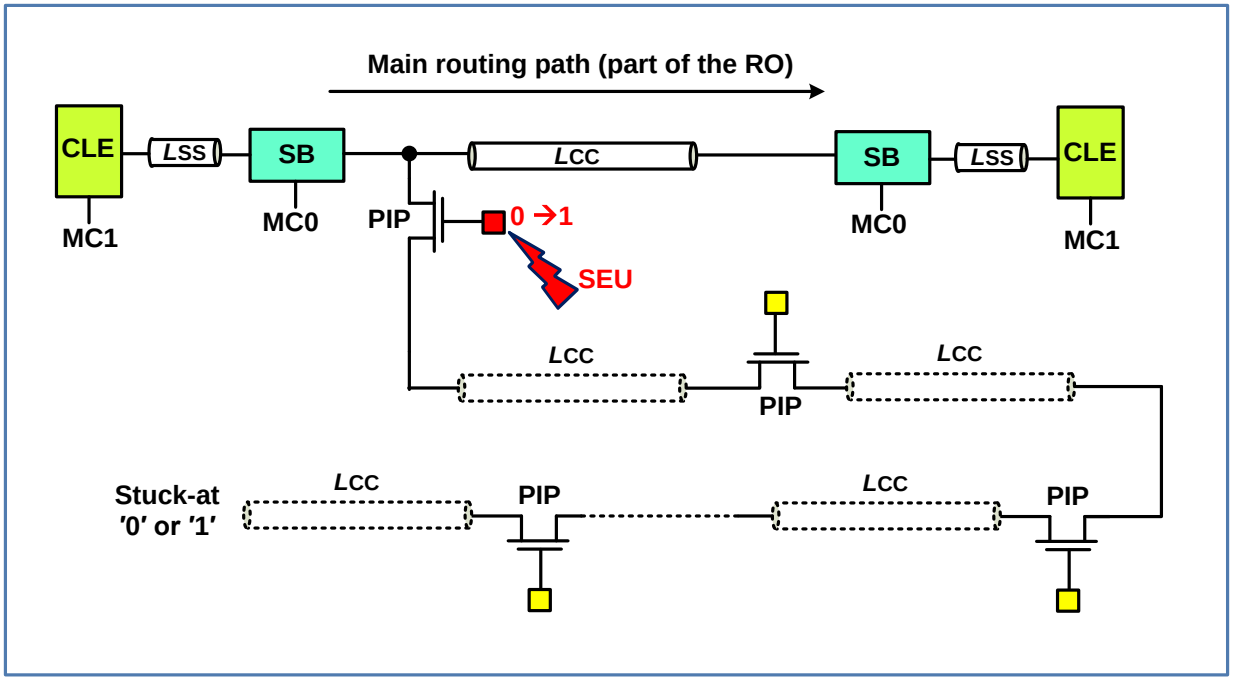


Figure 3-10 : Extra stuck-at parasitic interconnect

This phenomenon is shown in Figure 3-10. The stuck-at fault or extra combination delay effect mainly depends on the number of PIPs between the main routing path and the parasitic stuck-at interconnect. Section 3.7 presents the simulation results that demonstrate these two effects. It shows that there exists a threshold on the number of PIPs that generates a delay instead of a stuck-at fault.

Assume a ring oscillator implemented in an FPGA as shown in Figure 3-11. An SEU can affect the SRAM-cell that controls the pass transistor linking a parasitic interconnect to the main routing path between two consecutive inverters. Under some circumstances, the end of parasitic line could be stuck at '0' or '1'; and may produce a delay change in the main routing path that would change the frequency of the ring oscillator or would cease the oscillation. Our circuit model started with one cross line added into the main routing path via a pass transistor enabled by an SEU, while the end of the line was stuck at '0' or at '1'. This additional cross line broke the ring oscillator for both cases. Then for both cases, additional lines with pass transistors were added in series of the first one until the ring oscillator started ringing.

Simulation results obtained with these 3 models are compared to bombardment results in Section 3.7.

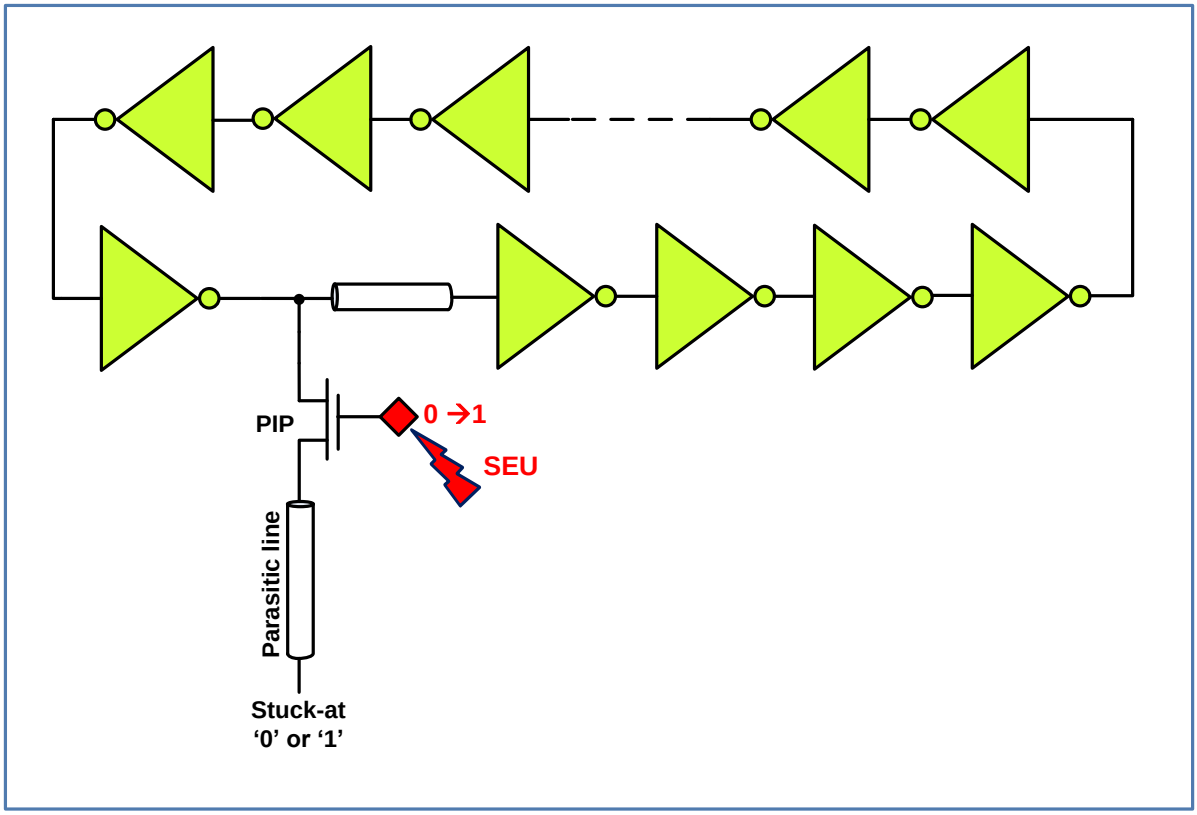


Figure 3-11 : Delay change mechanism in ring oscillator by additional cross lines stuck at '0' or '1' induced by SEU

3.7 Comparison of Simulated and Measured Delays

3.7.1 Delay Fault Results in Virtex-5 FPGA Core

Circuit-level simulations of ODCs were performed for the three proposed scenarios presented in Section 3.6 and illustrated in Figure 3-6, Figure 3-7, Figure 3-9 and Figure 3-10 for a total of three different scenarios. The simulated delays correlate fairly well with the ODCs measured at TRIUMF. The histogram of Figure 3-12 shows all the delay changes observed during all the experiments at TRIUMF. In the case where more than one ODC was observed during an experiment; each individual ODC was measured independently and included in the histogram. The number n_i on top of each bin in Figure 3-12 refers to number of configurations that provide a delay change within the delay span represented by bin n_i as listed in Table 3-1.

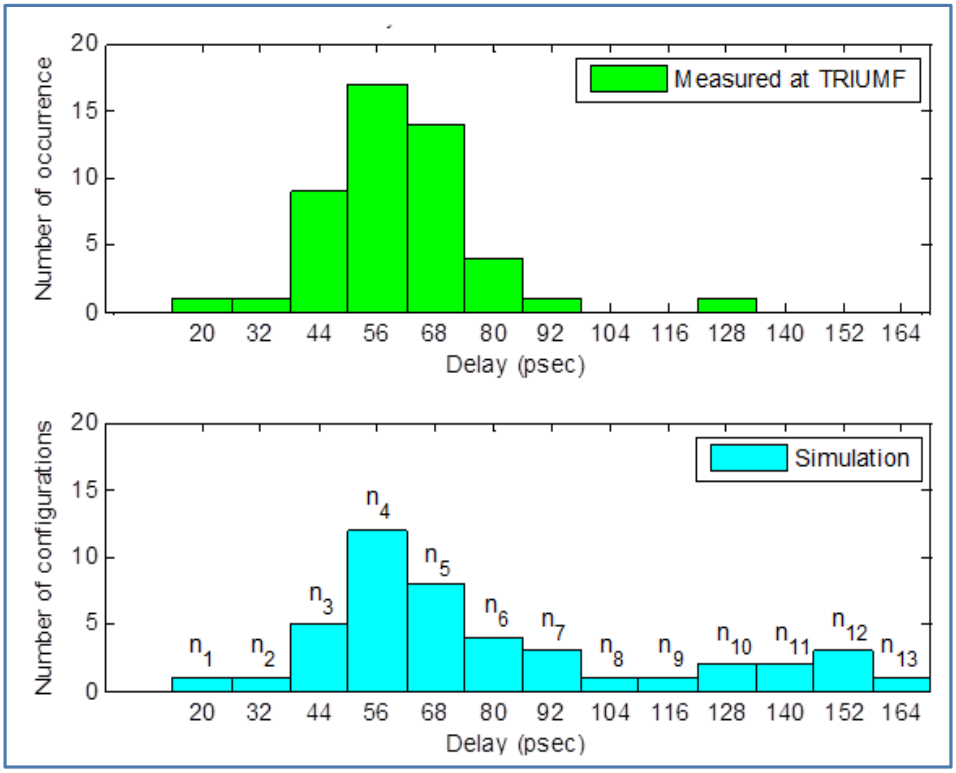


Figure 3-12 : Histogram of measured delays at TRIUMF [32] and simulated delays for the ring oscillators implemented in the core of FPGA

Notice also that the index '2nd' stated in Table 3-1 corresponds to the second configuration shown in Figure 3-4B that connects a parasitic interconnect to the main routing path while its length could be *1* L_{SS}. Recall that *1* L_{CC} represents the unit length extracted when tuning our model for the first configuration in Section 3.5.2, equal to 7.35 µm. The three introduced scenarios in Section 3.6 due to extra parasitic interconnects were simulated according to the possible interconnection lengths defined in Figure 3-8.

For example, a simulation delay of 39.2 psec was obtained with the 1 ODC case (1-SEU) shown in Figure 3-6A, which is stated in as the configuration (1) in bin number n_3 of Table 3-1. This value is a close match with the 38 psec measured value at TRIUMF.

Regarding the delay change due to SEU effect on IMUX circuit (defined in Section 3.6.2) in bin n_1, a small simulation delay change of 25.8 psec was observed.

Table 3-1 : Simulated configurations for ODC root cause validation reported in Figure 3-12

Number	Corresponded Configurations, as Defined in Sec. IV
n_1	IMUX Circuit
n_2	$(1)_{2nd}$
n_3	(1), (2), (1,1), (1,2)
n_4	(4), (1,4), (2,1), (2,2), (2,4), (4,1), (4,2), (4,4), (1,1,1), (1,1,2), (1,2,1), (1,2,2)
n_5	(1,1,4), (1,2,4), (1,4,1), (1,4,2), (1,4,4), (2,1,1), (2,1,2), (2,2,1)
n_6	(2,1,4), (2,2,2), (2,2,4), (2,4,1)
n_7	(2,4,2), (2,4,4), (4,1,1)
n_8	(4,1,2)
n_9	(4,1,4)
n_{10}	(4,2,1), (4,4,1)
n_{11}	(4,2,2), stuck-at ‘1’
n_{12}	(4,2,4), (4,4,2), stuck-at ‘0’
n_{13}	(4,4,4)

In the case of extra stuck-at parasitic interconnects (Section 3.6.3), our simulations for the stuck at '0' case showed that the first four cross lines break the ring oscillator while with a fifth line, the ring oscillator started ringing and produced a delay change of 148.9 psec, as reported in bin n_{12}. For the stuck at '1' case, the first eight cross lines stopped the oscillation of the ring oscillator

while with the ninth one, the ring oscillator was functional and produced a delay change of 135.2 psec as reported in bin n_{11}. These results are explained by the fact that an nMOS pass transistor is able to pass a '0' better that a '1' in its ‘on’ state.

The histogram of the simulated ODCs shows a trend indicating that the most probable delay changes are ranging from 40 psec to 100 psec, as observed also experimentally at TRIUMF. It confirms that the proposed scenarios and configurations for simulation were sufficient to detect those delay changes and consequently the histogram of simulated results is in good agreement with the experimental one.

3.7.2 Delay Fault Results in Virtex-5 FPGA IOB

This section investigates the delay faults affecting I/O blocks (IOBs) of Virtex-5 FPGA due to transient ionizing radiation [140]. The experimental setup is the same as shown in Figure 3-1 but the two ring oscillators are made of IOBs rather than LUT inverters in the FPGA core as shown in Figure 3-13. The two ROs oscillate at slightly different frequencies, $F_1 \approx 802$ kHz and $F_2 \approx 902$ kHz. The first ring oscillator occupies 179 IOBs configured as a long delay chain connected to one inverter, while the second one occupies 160 IOBs with one inverter. Overall, the two ring oscillators occupy 71% of the 480 available IOBs in Virtex-5 with FF1136 package [141].

The FPGA including the implemented design was bombarded with proton source irradiation under different energy levels (63, 50 and 35MeV). On some experiments, the one RO oscillation ceased before observing any delay change. The experimental results [36] clearly provided larger delay changes than those obtained with RO in the FPGA core (Section 3.4). Our hypothesis behind the origin of these large delay changes is that an SEU event modifies the drive and/or the buffer standard of IOBs. The bias voltage for FPGA IOBs was 3.3 V.

To validate this hypothesis, SPICE simulations were performed with the Input/Output Buffer Information Specification (IBIS) models [130] extracted from Xilinx ISE tool. IBIS models are generally used to perform various board level signal integrity simulations and timing analysis especially for high speed signals.

For each IBIS model simulation, the difference between two consecutive rise times/fall times of the output signal with the ones of the 12 mA LVCMOS25 I/O standard was measured while

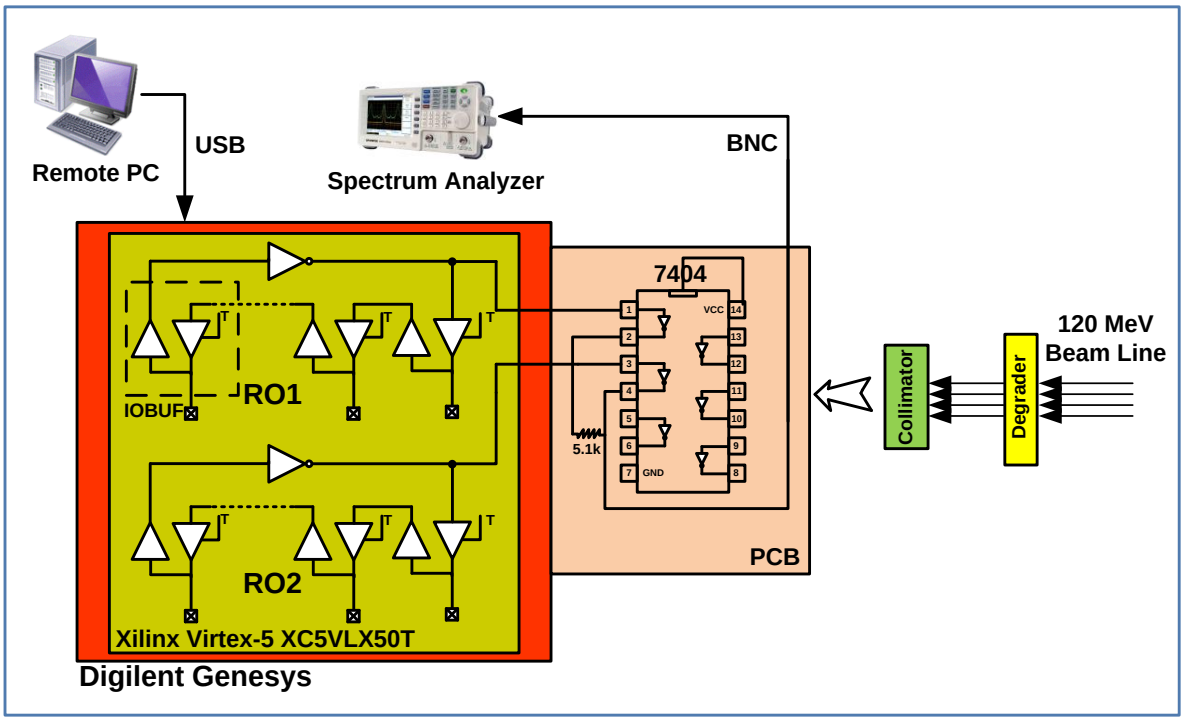


Figure 3-13 : Implementation of two ring oscillators created by Virtex-5 IOBs [140]

changing the I/O standard and/or drive strength of intended IOBs in the ROs. Each measurement was also performed for Maximum, Typical and Minimum cases of the intended output signal while the measurement threshold levels, called V_{inl} and V_{inh} in the IBIS model, were varied according to each I/O standard. These Max, Typ and Min output voltages take into account the worst cases and typical combinations of varying temperature, voltage and process population sample [130].

Alongside the IBIS model simulation, an emulation experiment was performed to support the hypothesis behind the origin of these large delay changes due to SEU that modifies the drive and/or the buffer standard of IOBs. In emulation, the buffer type and I/O standard for all IOBs was modified while the frequency of two ring oscillators (ROs) were measured instantly with oscilloscope. Recall that two ROs oscillate at slightly different frequencies, $F_1 \approx 802$ kHz and $F_2 \approx 902$ kHz with 12 mA LVCMOS25 I/O standard. While changing the I/O standard, if the oscillation frequency changes, it confirms that the buffer type and standard will change by SEU.

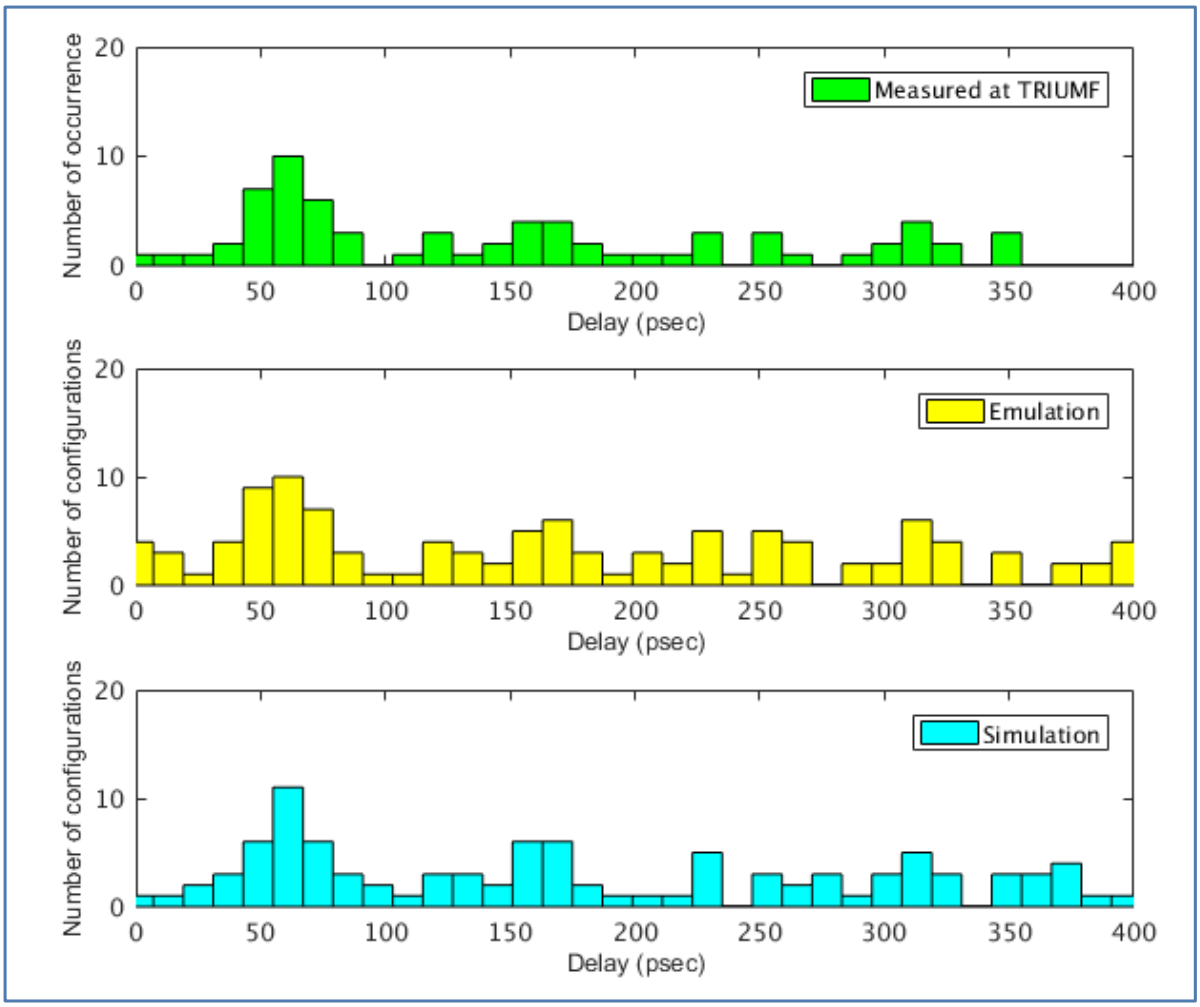


Figure 3-14 : Histogram of measured delays at TRIUMF [36], emulation and simulated delays for the ring oscillators implemented inside the FPGA utilizing the Virtex-5 IOBs

The histograms of experimental, emulation, and simulation results corresponding to delay faults affecting IOBs of the Virtex-5 FPGA are shown in Figure 3-14. Also, that some large delay values in the range of nano-seconds (2.3 nsec to 3.9 nsec) that would appear as outliers on the histogram were measured and also obtained by simulations. These longer delay values have been created by some I/O standards such as LVTTL, LVCMOS18, LVCMOS33 and PCI.

All the measured delays at TRIUMF were divided into single ODCs. It should be noted that there was also a 6.2 nsec observed at TRIUMF. This particular case is still under investigation in order to reproduce it through simulations.

The emulation and simulation results employing the SPICE IBIS model show a good agreement with experimental results, which indicates the usefulness of the IBIS model to evaluate delay

change due to irradiation affecting the IOBs. Indeed, the simulation results show a trend for the most probable delay changes while bombarding the board with proton source. This trend is similar to delay changes trend observed experimentally which supports the hypothesis of I/O standard change due to proton irradiation. This trend was also confirmed by emulation as presented in Figure 3-14.

Notice that the blank bins observed on the simulation histogram correspond to blank bins on the experimental histogram as well. Blank bins are most likely due to delay configurations having a low probability of occurrence and have not been observed since the limited amount of 97 measured ODCs.

3.8 Conclusion

This paper presented results supporting the assumption that extra combinational delays in SRAM FPGAs due to radiations are caused by bit-flip of SRAM-cells configuring FPGA interconnections and switch boxes. The simulation results are closely correlated to those observed during proton irradiation experiments. Several delay causing scenarios have been simulated.

Regarding delay changes affecting the I/O blocks of Virtex-5 FPGA, an experimental setup was also tested at TRIUMF including two ring oscillators inside the FPGA created directly in the IOBs. The hypothesis of I/O standard alteration while bombarding the FPGA board performed in [36] was verified through circuit level simulations and also emulation. IBIS models of I/O blocks were used to compare delays of the primarily implemented design to that of supported I/O standards and drive strengths in Xilinx Virtex-5 FPGA. Each measurement was performed for Maximum, Typical and Minimum levels of the intended output signal. The simulation results are in good agreement with the ones obtained at TRIUMF which supports the I/O standard alteration hypothesis. Emulations were also performed to validate the hypothesis behind the origin of large delay changes observed due to SEU event that modifies the drive and/or the buffer standard of IOBs. In emulation, the buffer type and I/O standard of all IOBs were changed while the oscillation frequency of two ROs was measured. In the case where the oscillation frequency changed, it confirms the alteration of I/O standard due to SEU effect.

CHAPTER 4 ARTICLE 2 : DELAY MONITOR CIRCUIT AND DELAY CHANGE MEASUREMENT DUE TO SEU IN SRAM-BASED FPGA

4.1 Overview

As stated in CHAPTER 3, extra combinational delay in SRAM-based FPGAs due to transient ionizing radiation have been modeled in circuit-level using Taiwan Semiconductor Manufacturing Company (TSMC) 1.2 V 65 nm CMOS technology, similar to the 65 nm triple-oxide technology node used to build Xilinx Virtex-5 FPGA. Simulation results for the design implemented at the core of FPGA and also with IOBs were in good agreement with those results obtained experimentally at TRIUMF laboratory. This chapter intends to discuss the design and implementation of a delay monitor circuit in an SRAM-based FPGA for real-time delay detection and measurement on a sensitive node of a design. This chapter is the reproduction of a published article in IEEE Transactions on Nuclear Science.

– M. Darvishi, Y. Audet, and Y. Blaquière, "Delay Monitor Circuit and Delay Change Measurement due to SEU in SRAM-Based FPGA," *IEEE Transactions on Nuclear Science*, vol. 65, pp. 1-8, (Early Access), DOI : 10.1109/TNS.2018.2828785, 2018.

4.2 Abstract

This paper presents a monitor circuit designed for the detection of extra combinational delays in a high frequency SRAM-Based FPGA. As in most of SRAM-based FPGAs more than 90% of the configuration bits control the routing resources, systems designed on FPGA are particularly vulnerable to interconnection delay changes caused by Single Event Upset (SEU) affecting the configuration memory. The proposed monitor is part of a mitigation technique dedicated to protect the circuit routing delay integrity while the system is being exposed to SEUs generated by radiation. Experimental results show that the probability of a delay change occurrence can increase as the number of delay changes affecting a node increases. Indeed, this increase depends on the configurable interconnection network and design placement in FPGA. Delay measurements using the proposed monitor revealed the existence of single delay changes ranging from 29 up to 151 psec. Also, cumulative delay changes in the range of 279 to 309 psec being the results of an extra interconnection network added by SEUs have been detected. Measured delay

values are in good agreement with those observed experimentally under proton radiation and also circuit-level simulations and emulations.

4.3 Introduction

Field Programmable Gate Arrays (FPGAs) are an attractive solution to implement systems for space and aeronautic applications. Configuration bits in SRAM-based FPGA are sensitive to radiation and have been studied over years [52, 66, 124, 142-146]. Almost 98% of all memory elements in SRAM-based FPGAs are configuration bits, of which 90% and more control the routing resources [147]. Recent studies reported observations of permanent extra combinational delays due to SEU induced by proton radiation in addition to short and open faults [32, 140]. Circuit-level models and simulations determined the most probable root cause of delay changes being bit-flips of SRAM-cells configuring interconnections and switch boxes, which create shorts between routed and unused wires, named parasitic interconnects [148-150]. The stuck-at faults can also induce a delay change to the path rather than just a logic fault [148, 151]. An SEU affecting a configuration bit of interconnections or switch boxes in SRAM-based FPGA can permanently delay the arrival of data signal. A delay observed on a node due a configuration bit flipped by an SEU is defined in this paper as a Single Delay Change (SDC). An SEU as a Single-Bit Error (SBE) affects one location in FPGA fabric at a time. In the case where a sequence of SEU injections creates delay change on a same node, the probability to observe larger delay changes can increase. The latter is named Cumulative Delay Change (CDC) in this paper. Experiments in [32] showed that the SDC due to the bombardment of the top side of the Virtex-5 FPGA with proton irradiation could be as large as 128 psec for the core circuit. A CDC up to 422 psec was also observed.

These permanent delay changes may lead to malfunction of circuits by generating delay faults. Increasing the timing margin or reducing the operating frequency is a trivial mitigation technique to reduce the likelihood of these delay faults and tolerating delay changes on combinational paths. For high frequency FPGA designs where timing closure is an issue, it might not be possible to use these additional timing margins. To reduce the timing cost, some mitigation techniques employ in-situ monitors on data path to sample signals before or after the clock edge in order to predict or to detect timing errors respectively [109, 110, 113, 152]. The TIMBER technique [109] detects a late arriving signal and correct the delay fault by borrowing time from

successive pipeline stages. This technique is not timing efficient for most SRAM-based FPGA applications due to the overhead imposed by its “TIMBER flip-flops” topology. Other timing error detection techniques allow high frequency operation at the expense of sporadically experiencing run-time timing errors on the affected path, such as the one proposed in [152] tailored to network-on-chip applications. However, the detection and recovery mechanisms of these techniques cannot be generalized to any applications. The scan flip-flop [113] allows concurrent error detection and correction by an extra single clock cycle for error correction while stopping the whole design on error detection and re-executing erroneous operations. The large extra logic gates occupy high silicon area and create performance degradation.

The main contribution of this paper is a circuit that performs real-time monitoring of delay changes. The monitor can be configured according to the timing budget (or available timing slack) of each selected node in the FPGA. An experimental setup confirmed the functionality of the monitor circuit in real implementation. This setup emulates SEU injection into the FPGA and allows locating the exact bit location and position that creates the delay change within the configuration memory frames. The observation of CDCs has been shown in the past by circuit-level modeling, simulation, and emulation [148]. This paper confirms experimentally that CDCs are directly linked to SRAM bits used to configure the interconnection network.

It is worth mentioning that some stuck-at faults may create delay change ([32, 148]) and they will be detected by the proposed delay monitor. However, other stuck-at faults (logic faults) are not detectable with the proposed monitor because only the transitions on the paths are taken into consideration in this application.

This paper is structured as follows. The motivation and design of the proposed real-time monitor architecture is discussed in Section 4.4. Detailed discussions on CDC detection and measurement and the proposed methodologies employing the delay monitor circuit are covered in Section 4.5. Validation of the proposed technique with an experimental setup on a Virtex-5 FPGA is presented in Section 4.6 along with results for experiments to detect CDCs and to locate upset configuration bit location. Finally, we conclude in Section 4.7.

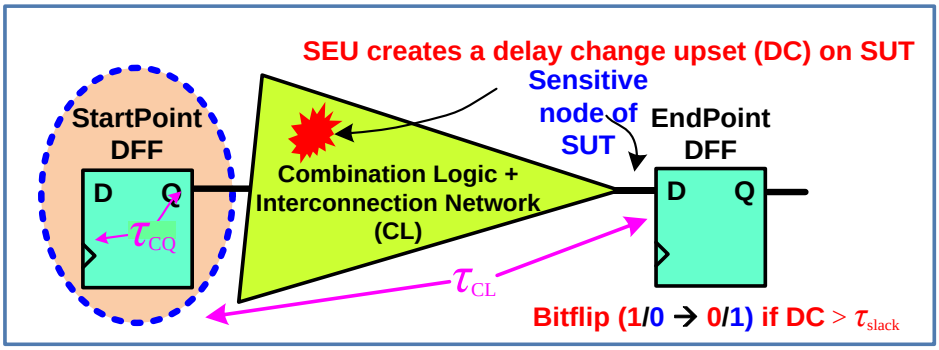


Figure 4-1 : Timing issues in synchronous circuits : SEU implication on a configuration bit of interconnections or switch boxes associated with logic cone of SUT

4.4 Real-Time Monitor for Delay Change Detection

An SEU affecting a configuration bit of interconnections or switch boxes in SRAM-based FPGA can permanently delay the arrival of data signal, labeled Signal Under Test (SUT), from a StartPoint flip-flop to any EndPoint flip-flop in a synchronous circuit as shown in Figure 4-1.

A Delay Change (DC) on an SUT induced by an SEU larger than its worst timing slack (τ_{slack}) may lead to circuit malfunction. τ_{slack} is defined as the minimum delay between the combinational logic data arrival time (τ_{CQ}+τ_{CL}) and the active edge of the clock (T_{clk}), minus the flip-flop setup time τ_{su} (Figure 4-2B). A data signal path with a slack smaller than a DC can potentially generate a delay fault. It is worth mentioning that there are two slacks for each logic path in the cone (i.e. rising and falling transitions), and the number of paths grows exponentially with the depth of the logic cone. A DC on a logic cone net will not necessarily be observed on the SUT. To be observed, this DC must be received on the critical path and a transition on this critical path must occur. The likelihood of delay faults is reduced if the clock frequency is such that τ_{slack} is larger than any DC for all circuit nodes. However, this timing overhead could be prohibitive for high speed circuits, especially if CDC must be mitigated. Proton irradiation experiments conducted on Virtex-5 FPGA showed that CDC on a signal path can be 3.3 times larger than SDC [32, 140], as will also be seen in Section 4.6.

The slack time of a path is relative to the operating clock period (T_{clk}) and the longest critical path (slowest) determined in the design. Critical paths with negligible slack times are more susceptible to timing failure due to a DC. In this paper, sensitive nodes are defined as the endpoint of these

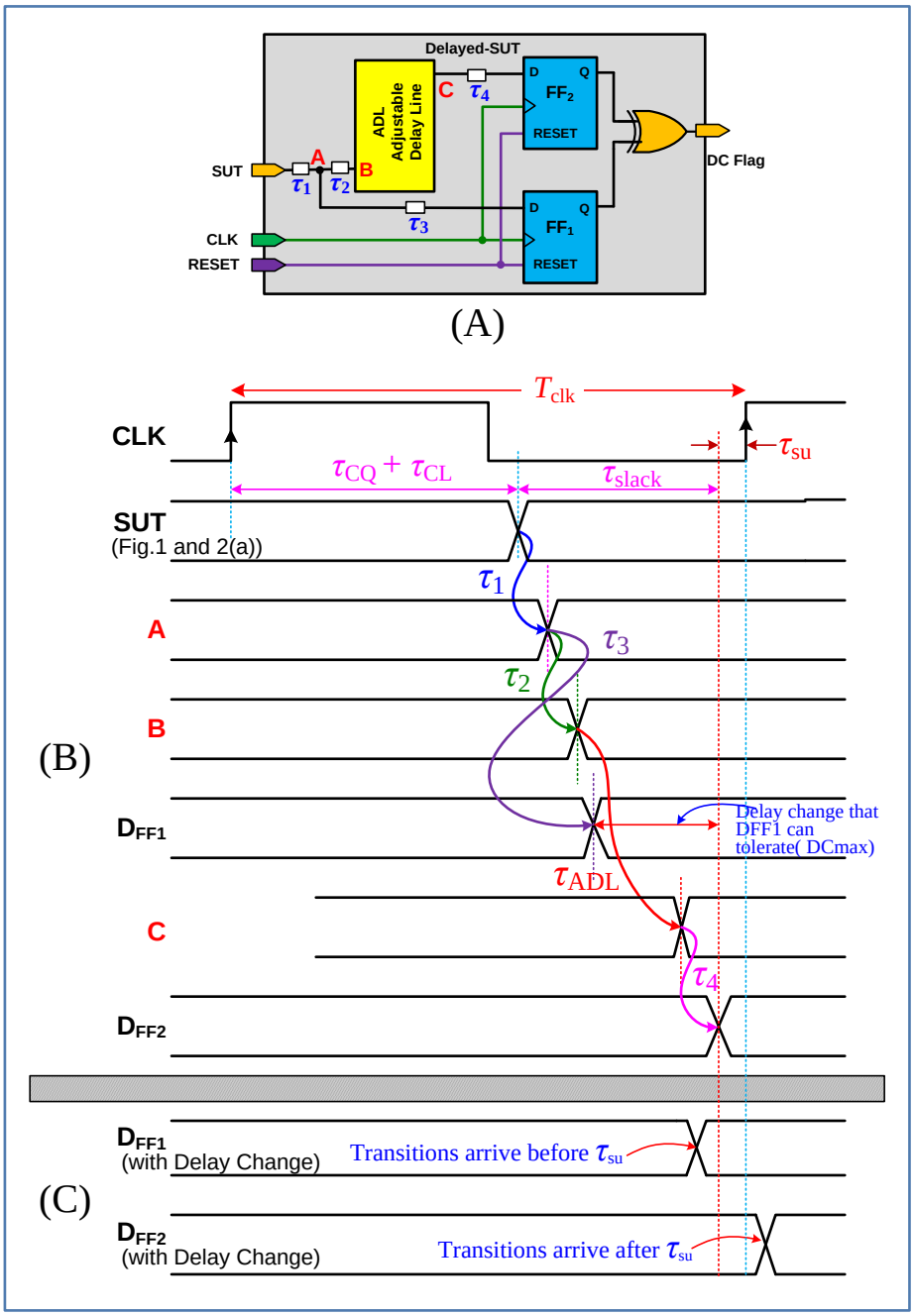


Figure 4-2 : DC Monitor architecture for delay change detection (A). Its timing diagram is shown without delay change (B), and with delay change (C)

critical paths with the worst (smallest) slack time. For some designs, latency optimization could limit the number of critical paths where monitors can be inserted to their corresponding sensitive nodes [153]. Since the monitor circuit must be physically placed and routed in the fabric, its overhead will significantly affect the time required for design's placement and routing. Hence,

reasonable effort has to be made at the design stage in order to limit the number of critical paths. However, the delay monitor is efficient when the design comprises few numbers of sensitive nodes.

A design implemented into the FPGA comprises sensitive nodes and non-sensitive nodes. It is worth mentioning that SDC on non-sensitive nodes can be mitigated with the feature available in SEU Controller (SEUC) IP core in the FPGA which can detect and correct an SBE occurred by an SEU. Without SEUC, the design could crash due to CDCs induced on the non-sensitive nodes where no monitor is linked. Scrubbing technique to correct the errors encompasses a wide range of techniques [154-156]. The scrubbing cycles for the intended Xilinx Virtex-5 FPGA (XC5VLX50T) in this paper is almost 7.10 msec. Notice that the SEUC is itself susceptible to SEUs. Some of SEUs that are less critical can be corrected as the SEUC has the ability to scrub itself [31].

In order to reduce the timing overhead of making a circuit tolerant to a DC, we propose : first, to make the circuit tolerant to any SDC with a clock frequency such that τ_{slack} is larger than $SDC_{\max}$ (maximum possible SDC) for all sensitive nodes and second, to add a DC monitor on nodes to allow the detection of SDCs. Actions can then be taken as soon as an SDC is detected on these sensitive nodes, such as scrubbing (localized bitwise partial reconfiguration), raise a system flag, reduce the clock frequency [24], or apply any other mitigation actions. Stopping the clock signal is not the preferred solution for designs implemented into FPGAs, especially for real-time control applications. Therefore, on DC detection, the system clock period could be temporarily increased to compensate for the maximum second DC occurrence on sensitive nodes, hence avoiding any system down time. This reduced frequency mode is applied until the circuit affected by an SEU is partially or entirely reconfigured. Lowering the operating frequency of the system at the time of DC detection is achieved by using the BUFGMUX_CTRL primitive provided by Xilinx which is available in Virtex-5 FPGAs and onwards. This logic primitive is a clock buffer with two clock inputs and one clock output. A select pin S can switch anytime between two clock inputs without causing any glitch. In our application, as soon as the DC Flag of Figure 4-2A is asserted, it is used to command the S pin of BUFGMUX_CTRL to switch to a lower frequency.

The proposed monitor raises a flag upon the occurrence of any DC induced by an SEU on an SUT in Figure 4-2. Its timing diagram emphasizes routing delays τ_1 to τ_4 that can be significant in

the monitor. An adjustable delay line (ADL) is configured with a threshold delay τ_{ADL} to satisfy both Equations (4-1) and (4-2) to make the circuit run. Equation ((4-1) gives the limitation of the routing delays for FF_2 in Figure 4-2 in order to detect a DC. τ_{ADL} can be adjusted in order to match a DC threshold (DC_{Th}) that needs to be detected as shown in the relationship of Equation ((4-2). This DC_{Th} takes into account the delay sensitivity to process, voltage and temperature (PVT) variations and also to the τ_{ADL} accuracy. In fact, in the ideal case where $\tau_1 = \tau_2 = \tau_4 = 0$, a precise τ_{ADL} adjustment will put its value equal to $\tau_{\mathrm{slack}} - DC_{\mathrm{Th}}$. Equation ((4-3) states the criteria for FF_1 where DC_{max} is defined as the maximum DC that will not assert the output of FF_1, hence will be detected by the monitor.

$$\tau_1 + \tau_2 + \tau_{\mathrm{ADL}} + \tau_4 \leq \tau_{\mathrm{slack}} \tag{4-1}$$

$$\tau_1 + \tau_2 + \tau_{\mathrm{ADL}} + \tau_4 = \tau_{\mathrm{slack}} - DC_{\mathrm{Th}} \tag{4-2}$$

$$\tau_1 + \tau_3 \leq \tau_{slack} - DC_{max} \tag{4-3}$$

In normal operation without DC (Figure 4-2B), the ADL can be configured such that the SUT transition propagates up to inputs D_{FF1} and D_{FF2} and both arrive before T_{CLK} - τ_{su} and sample the same data value and the circuit runs without any error. When a delay change such as SDC occurred, the transitions at D_{FF1} and D_{FF2} arrive before and after the clock transition respectively (Figure 4-2C), and the DC flag is asserted. To fulfill the monitor's functionality and detect SDC, τ_{ADL} must be tuned according to the unavoidable routing delays τ_1, τ_2, τ_3, and τ_4 and depends on monitor placement in the FPGA.

Fine Adjustable Delay Lines (ADL) can be made with carry logic blocks available in most FPGAs. ADL tuning can be done using the two types of outputs for each carry logic stage in Virtex-5 used in ADL configuration; MUXCY, and OR-gate outputs. Four carry logic stages form a CARRY4 primitive. Therefore, eight possible outputs can be properly chosen in order to satisfy Equation ((4-1). Notice that the accuracy/precision of the τ_{ADL} also depends on the delay line resources and how it is performed. Other structures might be used with better precision at the cost of logic or routing area. Details on ADL architectures are out of the scope of the paper. The sensitivity of SEUC to SEU can be counted as a drawback in the first glance; however, SEUC is able to scrub itself. The proposed monitor architecture is efficient when the design comprises few

numbers of sensitive nodes. The logic overhead of the monitor must be taken into consideration especially when the Design Under Test (DUT) occupies a large area in the FPGA fabric.

It is worth mentioning that it is possible for the transition on FF_2 to enter the metastability under a small DC. In the worst case, the monitor will not flag this small DC.

The main contribution and value of the proposed delay monitor circuit is to perform real-time DC detection while increasing temporarily the clock period by the order of the maximum delay change (DC_{max}) value in order to counter extra DCs received on the same SUT. Thus, the design is kept functional at high frequency while the SEUC will do a full scrubbing cycle of configuration bits.

The proposed monitoring scheme is employed in addition to the scrubbing cycle occurring every 7.1 msec approximately in the Virtex-5. According to our observation, SEU created DCs are the probable event. Therefore, our scheme aims at detecting in real time those DCs affecting the most sensitive nodes in order to avoid a failure caused by a second delay change that could happen before the next scrubbing cycle. Moreover, the latest generation of FPGAs show longer scrubbing times, consequent to the gate count increment.

4.5 Cumulative Delay Change Detection

The proposed delay monitor circuit is able to detect DC occurrence on an SUT. Two conditions must be met to detect a DC on a node : (a) only a DC larger than the worst slack on a sensitive node can be detected if the signal transition propagates on the path related to the worst slack (i.e. critical path), (b) the monitor must be configured to satisfy Equations ((4-1) to ((4-3) taking into account that the ADL resolution depends on which output (OR-gate or MUXCY) is selected.

4.5.1 Sensitivity to Cumulative Delay Changes

Any first DC occurs when an SEU flips a configuration bit of a Programmable Interconnection Point (PIP) in a switch box (such as SB1 in Figure 4-3) connected to a node in SUT's logic cone, which adds the capacitive load of a parasitic interconnect (A), named *Level* 1 DC. DC is accumulated on SUT if successive *Level* 1 SEUs hit any other PIP directly connected to a node in the SUT's logic cone.

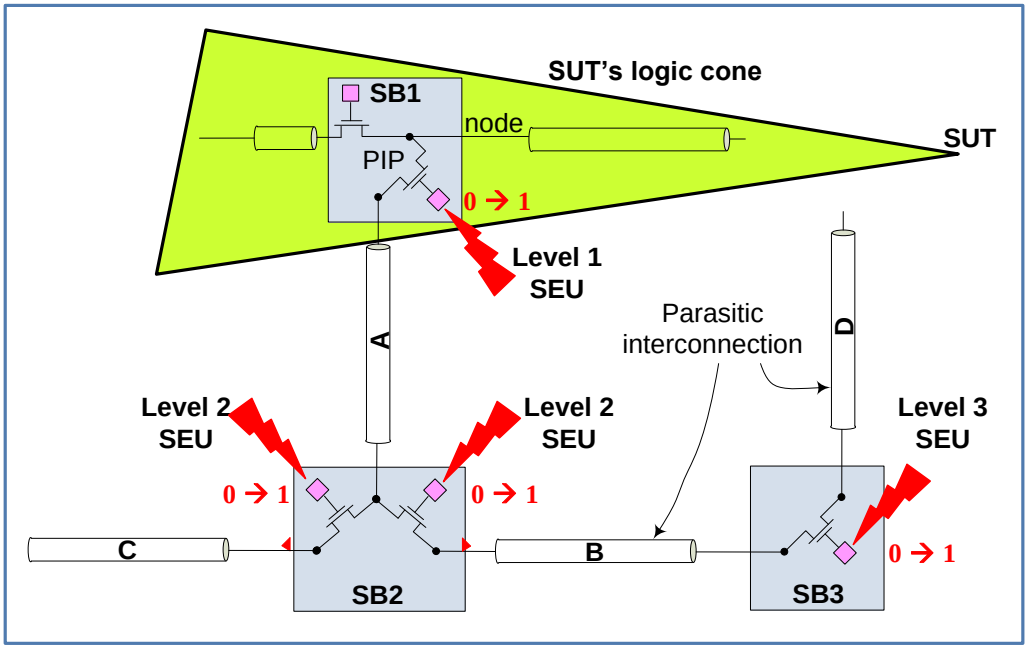


Figure 4-3 : Levels of SEU connecting parasitic interconnects to the SUT's logic cone resulting in CDC occurrence

Higher *Level* SEU can also create CDC, such as shown in Figure 4-3 where *Level* 2 SEU hits any PIP in SB2 connected to the parasitic interconnect A and then *Level* 3 SEU adds parasitic interconnect D to the parasitic network. Notice that any added parasitic interconnect makes SUT more susceptible to receive further DCs.

4.5.2 Proposed Algorithm for Detection of Cumulative Delay Changes

This section provides the algorithm proposed to detect CDCs on an SUT thanks to the delay monitor circuit. In reality, the average time between two DCs depends on many factors such as SEU injection speed, SUT's logic cone cross section, and it is not exactly predictable. In an emulation sequence, bit-flips are injected sequentially at the SRAM configuration addresses; however, two consecutive location addresses do not necessarily belong to the same SUT's logic cone. A new experimental setup is proposed to detect and measure CDCs with our proposed DC monitor. This setup performs sequential scan of configuration bits during multiple SEU injections and reports the configuration bit location that generates a DC on SUT.

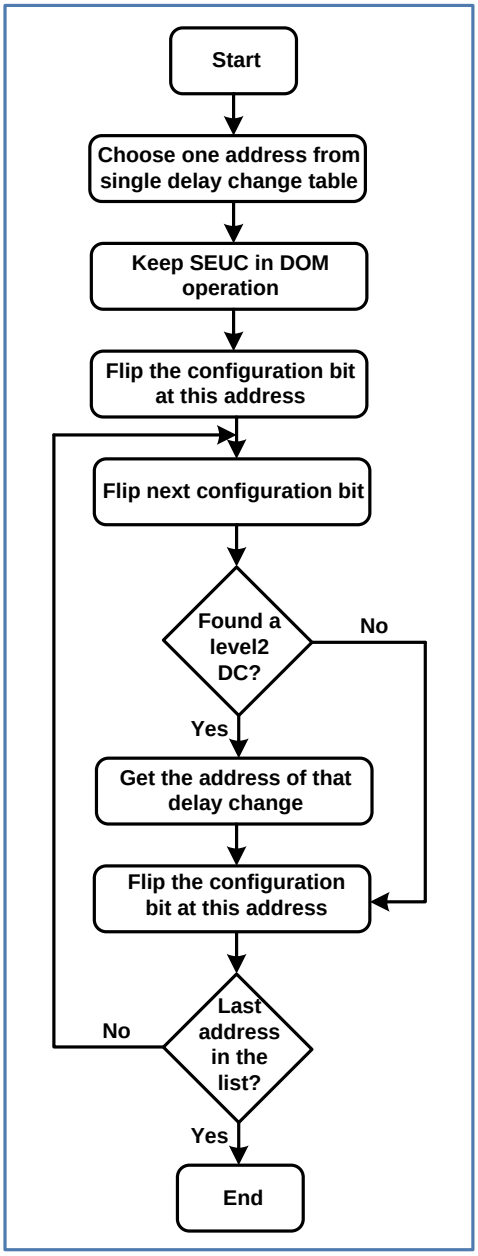


Figure 4-4 : Flow graph of level 2 DC detection

Our experimental bench injects cumulative SEUs into the FPGA using the SEU Controller macro (SEUC) in Xilinx Virtex-5. The SEUC is configured in Detection Only Mode (DOM), which allows sequential injection of SEUs into the FPGA without error correction and let the user control the time of injection.

In order to detect and measure these CDCs on an SUT, we proposed to instantiate multiple DC monitor circuits configured with different threshold delay values. In this case, a given monitor would detect a DC according to a defined DC_{Th}. In fact, this strategy can detect and measure CDCs with accuracy depending on the span of each bin (container), the number of bins and the bin accuracy, which is sensitive to process, voltage and temperature (PVT) variations. The span of a bin depends on the values of DC_{Th} of two consecutive monitors including the PVT variation. If the span of a bin is larger than the minimum DC value, multiple delay changes could then fall into the same bin. In fact, our proposed setup allows the detection of CDCs only when the added DC falls into different bin.

In this paper, in addition to the *level* 1 DCs, the *level* 2 and the *level* 3 DCs generated on an SUT node in Figure 4-2A due to an SEU injection have been detected and measured.

Figure 4-4 shows the flow graph of the proposed methodology in order to detect *level* 2 DCs induced on the SUT node. An address is chosen from a *level* 1 DC table, and is injected into the FPGA while the SEUC is configured in DOM. Then, all the configuration bit addresses are scanned by the SEUC, and in the case where a second DC is detected, its address is captured as well as its monitor's DC bin. If this address is not already in *level* 1 DC table, it is registered in the *level* 2 DC table.

The proposed recursive pseudo-code shown in Figure 4-5 generalizes the detection concept for any CDC, which discovers the parasitic interconnect network using a Depth-First Search (DFS) algorithm. In this algorithm, there is a table of location addresses for each DC levels. Two arguments are associated with the *DC_Detection* function : *level*, which means the rank of occurrence of DC, and *parent*, which refers to the address of the previous DC level belonging to the chain of DCs. Notice that for the *level* 1 DC, there is no address associated to the previous parent.

Detection of *level* 3 DCs due to SEU injection has a concept similar to the algorithm in Figure 4-4 with an additional step where for each of the *level* 1 DC addresses chosen, a *level* 2 child DC address will be selected and injected into the FPGA to induce an SEU.

```
DC_Detection (order,parent)
For each addr in the FPGA do
   If Addr is unexplored
        Flip Addr configuration bit in the FPGA;
       If DC is observed then
           Label Addr as explored;
           Push the pair (Addr, DC) in Table(order,parent);
           DC_Detection (order+1, Addr);
           Label Addr as unexplored;
    Flip Addr configuration bit in the FPGA;
End
```

Figure 4-5 : Proposed recursive pseudo-code (DFS) for DC detection

4.6 Experiments and Results

4.6.1 Test Bench

The DC monitoring functionality was validated by an implementation in a Xilinx Virtex-5 FPGA linked to an SUT sensitive node. The objective is to characterize the probability of occurrence and values of 2nd and 3rd DCs on a given node.

This has been done experimentally by flipping one by one all the routing bits allocated in the SRAM and reporting the ones which affected the particular node under test. A simple benchmark is sufficient for characterization. The SUT is a logic cone of only one node, from a 64-bit Linear Feedback Shift Register (LFSR) at the rate of system clock, 400 MHz in order to assess its susceptibility to SEU and measure cumulative delay changes affecting the node. The test bench is depicted in Figure 4-6. A PLLs_CLKMUX module generates the system clock. While no delay change is injected to the SUT, both FF_1 and FF_2 sample the same value at the rising edge of the clock signal. The value of τ_{ADL} (FF_2 only) must be tuned with respect to the unavoidable routing delays τ_1, τ_2 and τ_4 in order to fulfill the requirements for signal transition to both FF_1 and FF_2 according to Equations ((4-1) to ((4-3). However, other values of τ_{ADL} can be set in order to detect longer or shorter DCs. Notice that the timing slack varies with Process-Voltage-

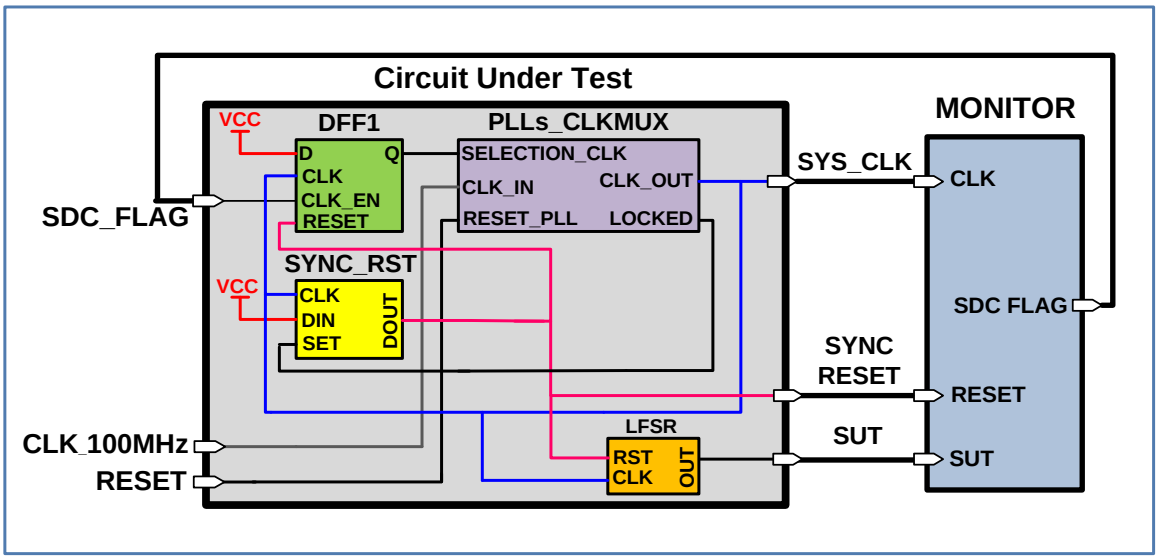


Figure 4-6 : The test bench configured to validate the delay monitor's functionality

Temperature (PVT), as will be described in Section 4.6.3. The ADL was implemented with carry chain blocks

and flip-flops available in FPGA slices. The ADL outputs can be provided by the outputs of CARRY4 primitive, which are two types : OR-gates output; and the carry multiplexers (MUXCYs) output. The ADL delay is adjusted from the selection of any of these outputs in the carry chain. The minimum extracted resolution for each carry logic output in Virtex-5 (65 nm technology) is around 20 psec.

4.6.2 Experimental Validation of the Proposed DC Monitor

An experimental setup was employed to confirm the functionality of the monitor circuit in real implementation. The experiment benefits from the SEU Controller macro (SEUC) IP core in Virtex-5 FPGA [29]. Bit-flips are injected through emulation using SEUC via an UART serial communication port. For each bit-flip injection, the status of the monitor circuit is captured by ILA. The SEUC is set on Detection Only Mode (DOM), which does not perform error correction. For each injected SEU, the SEUC sends back the exact location and position of the bit-flip (upset) within the configuration memory frames as well as the type of error (i.e., Single-Bit error (SBE) or Multiple-Bit error (MBE) [29]. When the DC flag is asserted, the configuration bit location is automatically sampled by Chipscope.

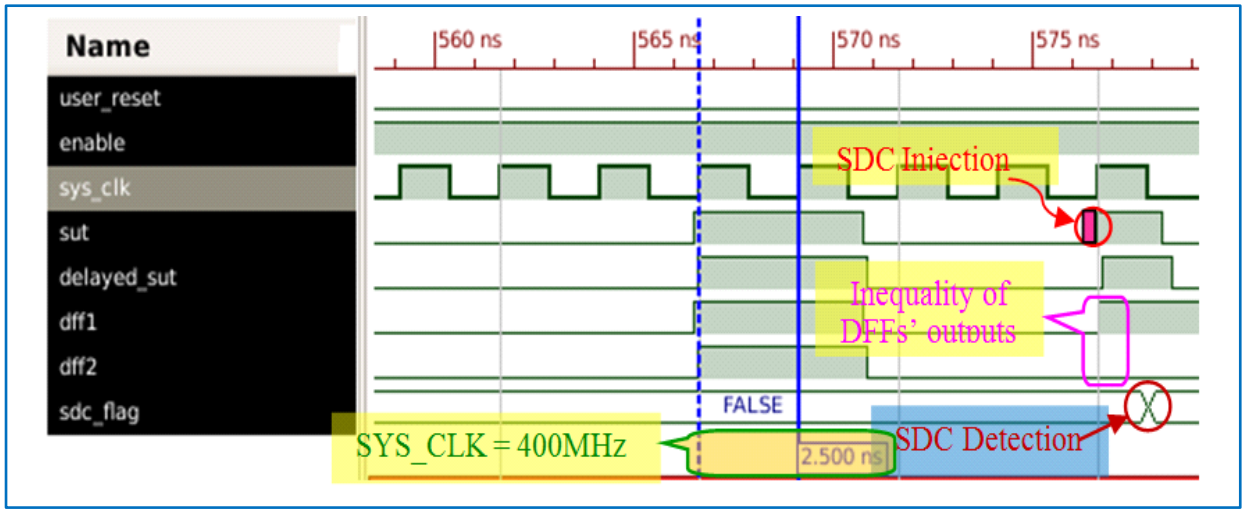


Figure 4-7 : Post place and route simulation results of SDC detection scheme using the DC monitor

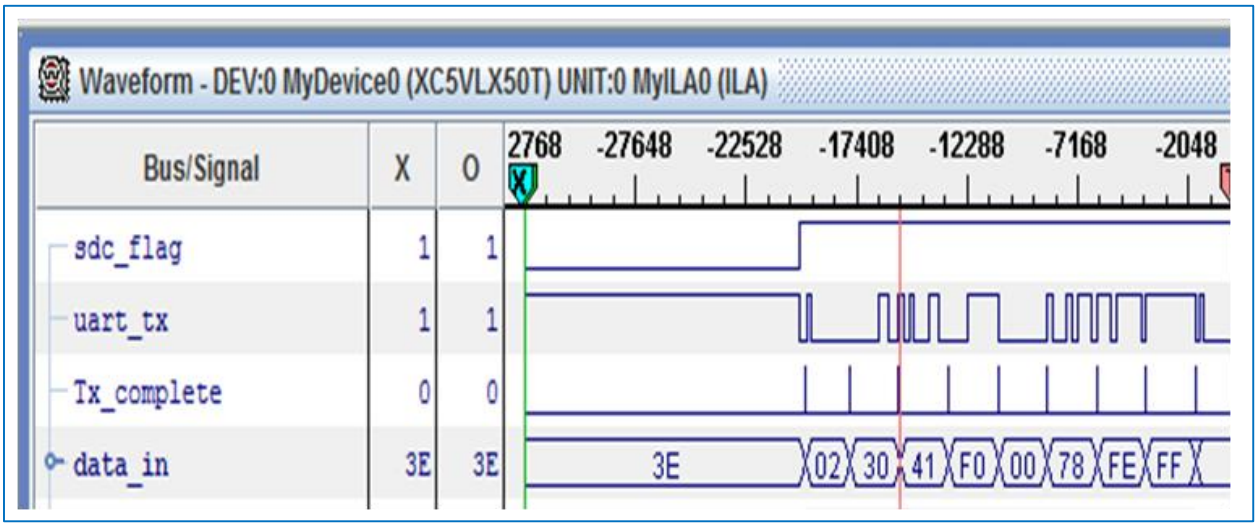


Figure 4-8 : Experimental result of SDC detection obtained by ChipScope Pro Analyzer (ILA)

Figure 4-7 shows the post place and route simulation results of the circuit in Figure 4-6. The `sut` signal is fed to FF_1 and its delayed version (`delayed_sut`) is fed to FF_2 (Figure 4-2). At the time of SDC injection on the SUT node (at 576 nsec), the signals `dff1` and `dff2` are shifted by the same delay change, hence, the two flip-flops sample different values and the `sdc_flag` is asserted.

Table 4-1 : Comparison of our proposed monitor with alternative methods

Feature	Timing Error Coverage	Delay Element Type	Operational Mode	Technology
TIMBER Flip-Flop [109]	Range of nsec	Inverter chains	Low frequency	90 nm
Scan Flip-Flop [113]	Range of nsec	OR tree	Mid frequency	90 nm
This Work	*n* times of ~20 psec	Carry chain	High frequency	Virtex-5 (65 nm)

Experimental waveforms extracted by the ILA tool are shown in Figure 4-8. The UART interface in SEUC makes a brief report that provides the opportunity to record the exact configuration bit location of any injected bit-flip.

When SEUC operates in DOM, the faulty location is reported by tracing `uart_tx` signal of SEUC. This signal is the serialized representation of `data_in` parallel input in SEUC transmitter. For each byte transmission, the `Tx_complete` signal is raised while the bytes are sent serially.

Table 4-1 compares our proposed monitor architecture with alternative methods such as TIMBER flip-flop [109] and scan flip-flop [113] in some comparable features. The main advantage of the proposed DC monitor architecture is the employed compact CARRY4 primitive as a delay element rather than large area consuming inverter chains and OR trees. Moreover, the proposed monitor compares advantageously to TIMBER and scan flip-flop since it can detect delay changes in the range of *n* times of 20 psec rather than nanoseconds. Similar to any logic circuit, the input capacitive load of monitors will add a delay to the sensitive nodes. This result as well as area overhead were not clearly describe in [109, 113] due to the large volume of logics employed to configure the architectures. Delay overhead induced by our monitor on SUT was extracted by Static Timing Analyzer tool from Xilinx and depends on its physical distance with the SUT. For example, in our test bench, the SUT of Figure 4-6 has one fanout in the same slice and its net delay increases from 295 psec to 326 psec, or 10.5 % with the DC monitor. Indeed, the monitor

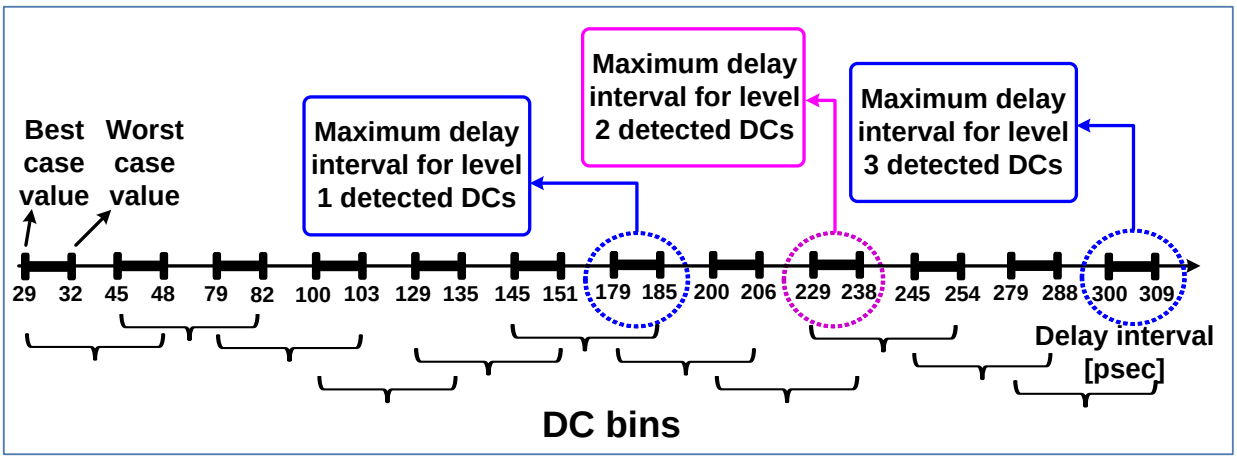


Figure 4-9 : DC bins and maximum bin values for detected *level* 1, *level* 2, and *level* 3 DCs extracted from STA

loads the sensitive node with a delay overhead as small as 31 psec in best-case and as large as 40 psec in the worst-case extracted by the Static Timing Analyzer tool while it is closely placed to the sensitive node. In the case where the monitor is placed as far as possible from the sensitive node, the minimum delay overhead is 87 psec in best-case and the maximum is 99 psec in the worst-case.

4.6.3 Experiments to Detect Cumulative Delay Change (CDC)

Twelve monitors with different threshold delays (DC_{Th}) on the same SUT were used to detect and measure first and cumulative second and third DCs. The delay overhead induced by these monitors on SUT was almost 65 psec in best-case and as large as 81 psec in the worst-case. This SUT is a single net with no logic cone and according to the Static Timing Analyzer (STA), it has a total path delay of 1.36 nsec with a slack of 0.95 nsec at 400 MHz. Delays and therefore DC_{Th} depend on PVT. Variation of DC_{Th} due to PVT was extracted from STA for (slow process-0.95V-85°C) and (fast process-1.05V-0°C) corner cases. Each monitor would detect a DC depending on its DC_{Th} and its corresponding variation. Our experiments on the SUT shown in Figure 4-6 allowed detecting 24 *level* 1 DCs, 43 *level* 2 DCs and 83 *level* 3 DCs. Notice that the locations in *level* 1 DCs table that created a second DC are not included in the *level* 2 DC table. Moreover, the locations in *level* 1 and 2 DC tables that created a third DC are not included in the level 3 DC table.

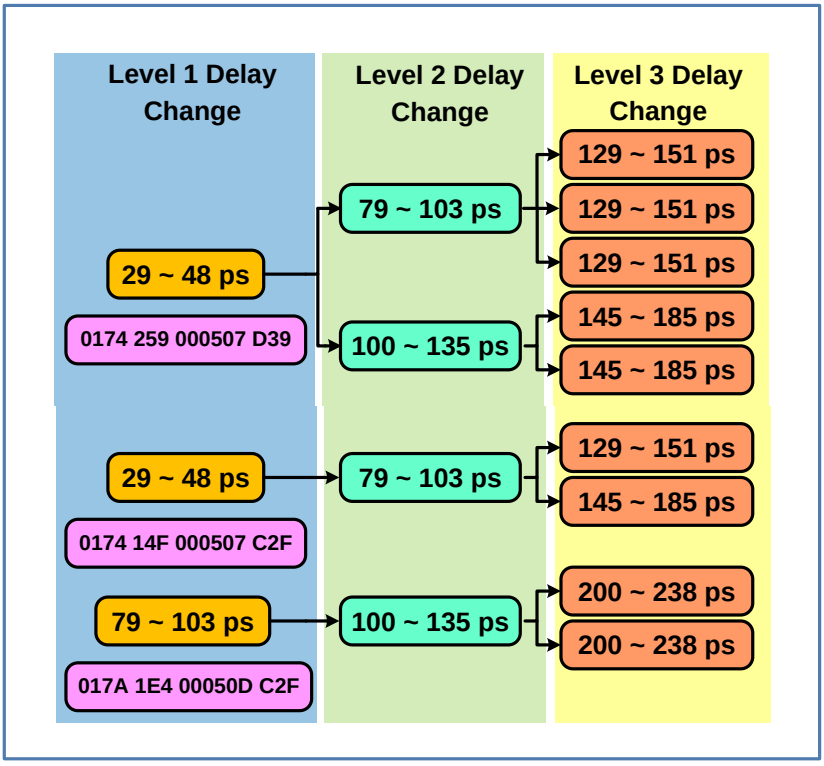


Figure 4-10 : Three sets of experimental results for CDC detection

The twelve monitors, linked to the SUT node in Figure 4-2A, were configured with the DC bins shown in Figure 4-9. The maximum bin value where *level* 1, *level* 2, and *level* 3 DCs were detected is also identified. This means that no DC greater than those values was observed experimentally. The start and end delay values of each horizontal bar in Figure 4-9 were used to configure ADL. They were derived from the best-case and worst-case corners for delay value in each stage of delay element (i.e., carry logics of CARRY4 primitive).

Figure 4-10 presents the interconnection network representation for three of the 24 *level* 1 DCs. Only the fault location for *level* 1 DCs is shown for simplicity. The locations indicated in the first column provide the exact location of the error within a frame [29]. The second column shows four of the 43 *level* 2 detected DCs, and finally, the third column depicts nine of the 83 detected level 3 DCs.

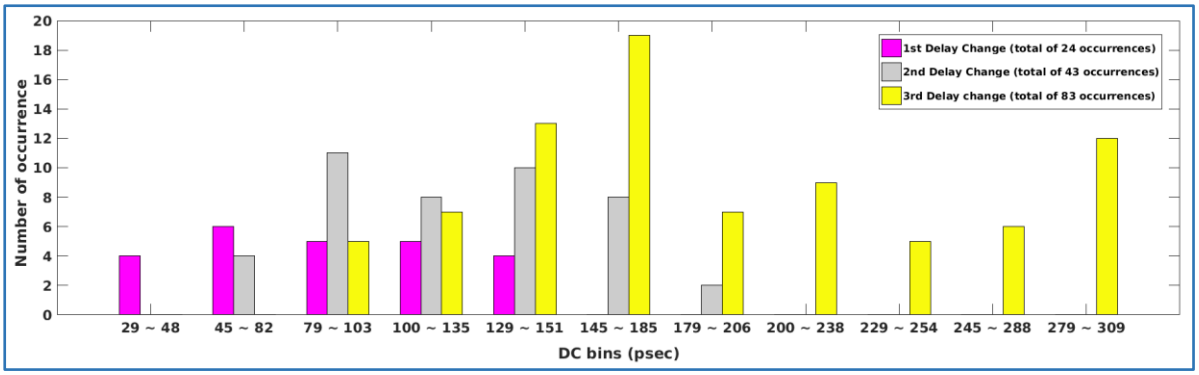


Figure 4-11 : Distribution of all detected DCs by twelve employed monitors with threshold DC values shown as the bins

Table 4-2 : Occurrence of DC increase with DC level

Delay change order	Absolute number of occurrences	Normalized number of occurrences
First DC	24	1
Second DC	49	2.04
Third DC	91	3.79

The histogram of Figure 4-11 presents all 24 *level* 1 DCs, 43 *level* 2 DCs and 83 *level* 3 DCs. These results show that the maximum value of *level* 1 DC detected by our monitor is in the range of 129 ~ 151 psec, which is close to the maximum value of 128 psec obtained experimentally at TRIUMF [32]. Also, the detected *level* 2 DC falls in the range of 179 ~ 206 psec which is in good agreement with the value of 194 psec measured at TRIUMF. It is observed that the probability of occurrence of a DC can increase as the number of DC affecting a node increases with the size of the parasitic network. Indeed, this increase depends on the configurable interconnection network and the design placement in FPGA. Also, we observed a shift in DC level distribution towards higher delay values as the level increases, which is consistent with the fact that *level* 2 DCs

cumulate the effects of *level* 1 DCs, and *level* 3 DCs cumulate the effects of *level* 1 and *level* 2 DCs.

The DC occurrence as a function of DC level is shown in Table 4-2. In this table, all possible second DCs (i.e. those *level* 1 and 2 DCs that create a second DC) and third DCs (i.e. those *level* 1, 2 and 3 DCs that create a third DC) were included to provide a better statistical evaluation of CDC occurrence as the DC detection level increases. A normalization factor is applied by considering that the first DC has an occurrence of 1. For instance, these results show that the probability of occurrence of a second DC after a first DC is 2.04 larger than that for a first DC. In fact, the probability of occurrence increases because SEUs affecting a node increase the size of the parasitic interconnect network.

4.7 Conclusion

Given the importance of routing resources in recent FPGAs, this paper presented a monitor circuit for delay change detection that can be employed as part of an SEU mitigation technique dedicated to preserve the system timing integrity. Post place and route validation and experimental results confirm the functionality of the monitor. The proposed monitor compares advantageously to TIMBER and scan flip-flop since it can detect delay changes in the range of *n* times of 20 psec rather than nanoseconds. The monitor loads the sensitive node with a delay overhead as small as 31 psec in best-case and as large as 40 psec in the worst-case when it is closely connected to the sensitive node. The delay overhead was as small as 87 psec in best-case and as large as 99 psec in the worst-case when the monitor was placed as far as possible from the sensitive node. Further experiments employing several monitors linked to the sensitive node were performed to detect cumulative delay changes. It has been observed that the probability of a delay change occurrence on an SUT line increases as the level of occurrence, first, second or third, increases. This result justify our delay change mitigation strategy of real-time detection of the first delay changes in order to avoid a delay fault caused by a second delay change on the same signal path. This is achieved with a very small impact on the system performance.

4.8 Acknowledgment

The authors would like to thank CMC Microsystems for providing tools as well as CRIAQ and ReSMiQ for their financial support.

CHAPTER 5 ARTICLE 3 : ON THE SUSCEPTIBILITY OF SRAM-BASED FPGA ROUTING NETWORK TO DELAY CHANGES INDUCED BY IONIZING RADIATION

5.1 Overview

The presence of extra combinational delays, also called DCs, in the routing resources of SRAM-based FPGA due to transient ionizing radiation were represented and modeled in circuit level in CHAPTER 3. It was shown that the simulation results are in good agreement with those ones obtained experimentally which confirm the accuracy of the proposed circuit level models for DC generation and propagation in the SRAM-based FPGAs. A delay monitor circuit was proposed in CHAPTER 4 in order to detect and measure the SEU-induced DCs on the routing resources of the SRAM-based FPGAs. To this end, the proposed delay monitor was implemented on the same FPGA that has been employed for the experiments stated in CHAPTER 3. The obtained results were in good agreement with those ones obtained with in-beam experiments and also by circuit level simulations. Also, it was claimed that there is a relation between the level (order) of DC occurrence and the probability to receive more DCs. This chapter intends to present the results on the investigation of the susceptibility of routing interconnection network to delay changes induced by ionizing radiation. Also, the claim that has been stated earlier in CHAPTER 4 is taken into consideration for validation in this chapter. This chapter is the reproduction of a submitted article in IEEE Transactions on Nuclear Science.

– M. Darvishi, Y. Audet, Y. Blaquière, C. Thibeault, and S. Pichette, "On the Susceptibility of SRAM-Based FPGA Routing Network to Delay Changes Induced by Ionizing Radiation," *IEEE Transactions on Nuclear Science*, (Submitted), March 2018.

5.2 Abstract

This paper presents the results of investigations on the susceptibility of routing network in SRAM-based FPGAs exposed to neutron radiation creating single-event upset. A method to configure test circuits mostly with routing resources and few logic resources is presented. Full control over routing resources enables the use of different interconnection types in order to create routing-based oscillators. A method is proposed to route through the 2-D array of switch matrices

inside the interconnection network and to automatically identify the involved programmable interconnection points associated with a node. An experimental setup is proposed to measure delay changes induced by single-event upset to the FPGA routing resources while it is exposed to neutron radiation. The proposed setup requires no external equipment such as manufactured equipments or external instruments for delay change measurement. The experimental results show that our setup is able to measure induced delay changes as low as 5 ps on higher frequency oscillators.

5.3 Introduction

SRAM–based Field Programmable Gate Arrays (FPGAs) have attracted a lot of interest in various applications due to their high digital circuit density and growing performance capability. In addition, reconfigurability in field makes them very attractive for applications in harsh environments such as space and aeronautic [16]. These semiconductor devices are structured in an array of Configurable Logic Blocks (CLB) connected via a programmable routing interconnection network [16], [148].

Recent advances in semiconductor technology allowed integrating programmable logics with very complex systems in a single silicon die. State-of-the-art FPGAs include not only the programmable logic fabric but also hard-core circuits like complex processing systems, and complex interface between the Processor Subsystem (PS) and Programmable Logic (PL) [157]. These new All Programmable System-on-Chip (APSoC) devices have been used extensively in avionic and space applications in recent years [26, 158-161]. The PL part of the APSoC is the FPGA itself and is intended for implementation of high-speed logic and data flow circuits and systems. The PS part contains a microcontroller. Hence, the functionality of any system implemented into an APSoC can be partitioned between PL and PS. Among the APSoC devices, the Xilinx Zynq-7000 fabricated in the Taiwan Semiconductor Manufacturing Company’s 28 nm technology node has been used for radiation effect studies in recent years [161-166]. This type of APSoC is very attractive in the space and aeronautic sector due to its system integration, high configurability, and flexibility.

Routing resources in SRAM-based FPGAs are controlled by SRAM cells that are called configuration bits [17]. Their sensitivity to ionizing radiation has been studied over years [22], [52], [124], [143-145] and showed that in addition to short and open faults, permanent extra

combinational delays can be observed. These extra delays are generated by Single-Event Upset (SEU) as reported in [32], [140]. As determined by circuit-level models and simulations, the root cause of delay changes (DC) is the bit-flip of SRAM-cells controlling the routing resources, mainly found in Switch Matrices (SM). The bit-flip may link an unrouted interconnect to a live interconnect. This phenomenon results in an extra capacitance load added to the live interconnect, and hence delays the arrival of data signals passing through the live interconnect [148]. The impact of ionizing radiation inducing SEU on the interconnection network of SRAM-based FPGAs is a serious matter, given that more than 90% of SRAM configuration bit are dedicated to routings [66, 167].

This paper presents the results of investigations of the likelihood and significance of delay fault occurrence in the routing resources in the programmable logic (PL) of a Zynq-7000 APSoC device due to neutron radiation. We propose a method to configure Ring Oscillators (RO) mostly with routing resources and few logic resources. Full control over routing resources enables the use of different interconnection types in order to create routing-based ROs. The configuration of different ROs is automated using the Xilinx Vivado scripting tool. A method is proposed for traversing SMs inside the interconnection network to automatically identify the involved Programmable Interconnection Points (PIP) associated with an input or output pin of an SM. We also propose an experimental setup to measure DCs as low as 5 ps induced to the routing resources of the Device Under Test (DUT) including the implemented ROs while it is exposed to neutron radiation. Thanks to the proposed setup, no external equipment (e.g., such as manufactured equipments or external instruments) is required for DC measurement.

This paper is structured as follows. Some background information is presented in Section 5.4. An overview of the routing resources in Zynq-7000 APSoC is presented in Section 5.5. A model for SM along with a method to route through it is presented in Section 5.6. The proposed method for configuration of different ROs with routing resources and the procedure for automated design using the Xilinx Vivado scripting tool is discussed in Section 5.7. Experimental setup for in-beam neutron irradiation, hardware implementation of ROs as well as the algorithm to readback the data are presented in Section 5.8. Conclusion and future works are finally drawn in Section 5.9.

5.4 Background

This paper focuses on the susceptibility evaluation of the routing interconnection network in the PL resource in a Zynq-7000 device to SEUs while the device is exposed to neutron radiation. This state-of-the-art APSoC device offers specialized modules such as integrated complex PS. It should be noted that almost 98% of all memory elements in the PL part are configuration bits, of which more than 90% control the routing resources [66, 167]. Routing interconnects in the PL resource are linked through a 2-D array of SMs. An input pin of each SM comprises a set of PIPs where a PIP, a CMOS transistor switch, can be programmably turned on/off to add/remove interconnects. Once an unwanted PIP is activated, a correction mechanism is required to recover the original state of that PIP, such as presented in [143], [168], [34, 169, 170]. Sensitivity evaluation of logic resources in Zynq-7000 APSoC to ionizing radiation was studied in recent years [157, 163-165]. Ionizing radiation effects such as SEU in the memory elements of Zynq-7000 APSoC were presented as an important issue in [165]. The impact of using different system architectures on a Zynq-7000 APSoC in the overall system failure rate was studied in [162, 164]. Several system architectures such as memory organizations and communication schemes were implemented and exposed to proton irradiation. Heavy ions and proton experiments conducted on a Zynq-7000 APSoC showed that the PL and PS parts have different sensitivity to ionizing radiation-induced errors such as SEU [165]. Also, cache memories and BRAMs are very sensitive to SEU where each of them needs a different mechanism for SEU detection and correction [165]. The vulnerability of different types of memory modules, failure rate in memory elements and data have been studied for Zynq-7000 APSoC exposed to ionizing radiation [161-166]. Recent studies involving routing resources in a variety of applications such as clock tuning [171], Time-to-Digital Converters (TDC) [95, 172], Physical Unclonable Functions (PUF) [173], and True Random Number Generators (TRNG) [174] have shown that full control of the delay at the finest granularity between two given points of the circuit is an essential requirement. The placement of circuit elements can be fully controlled by the designer, while routing resources are less controllable. Implementation of logic-based ROs was reported such as ring-oscillator PUFs (ROPUF) [175-180]. Although, these ROs are good to assess the behavior of logic resources against different phenomenon such as environmental changes, supply voltage drop, temperature, and aging effect, they are not suitable for investigation of interconnection network's delay changes in radiation experiments.

5.5 Overview of Routing Resources in Zynq-7000 APSoC

Generic SRAM-based FPGA model, standalone or merged in an APSoC, consists of some fundamental logic cores linked via an interconnection network. There exists a common global model for several families of SRAM-based FPGAs including three types of resources : *logic resources, routing interconnects*, and *switch matrices* [181]. In this paper, we focus on the routing resources and switch matrices that are the roots of the interconnection network.

5.5.1 Logic and Interconnect Tiles Resources

Logic resources are linked via an interconnection network comprised of different interconnection types. Some interconnects are dedicated to specific logics or functions and the rests are global. Interconnects in the network span in horizontal plane traversing the gate array from west to east and in vertical plane from north to south. SMs are employed to link various interconnects and transmit information inside the FPGA.

The topology of a CLB and interconnect (INT) tiles in Xilinx 7-Series FPGAs is shown in Figure 5-1. The planar SM is associated with CLB and has an injective mapping where each input node on the right side is connected to only one node on its left side (in CLB tile with SLICEL). The INT tile consists of one Wilton SM (WSM) where each input node has a multiple mapping to several output nodes and vice versa [182]. A net, such as NetA in Figure 5-1, is made of a list of nodes and represents a logic net. A WSM node can be an input or an output for the data signal that reaches it and is always unidirectional. A WSM input node sends data signal to several outgoing nodes (called *downhill node*) and one of the PIPs connected to an output node is configured to receive data signal from one of its multiple incoming nodes (called *uphill nodes*). A PIP specifies a configurable connection between an SM input and an SM output as depicted in Figure 5-1 [183].

In addition to CLB and INT tiles, other tiles are available in 7-Series FPGAs to make connection to other functional elements such as BRAM, Digital Signal Processor (DSP), Clock Management Tile (CMT) and I/Os. Their DC analysis is out of the scope of this paper. This work focuses on SEU-induced DCs affecting the interconnection network between CLBs.

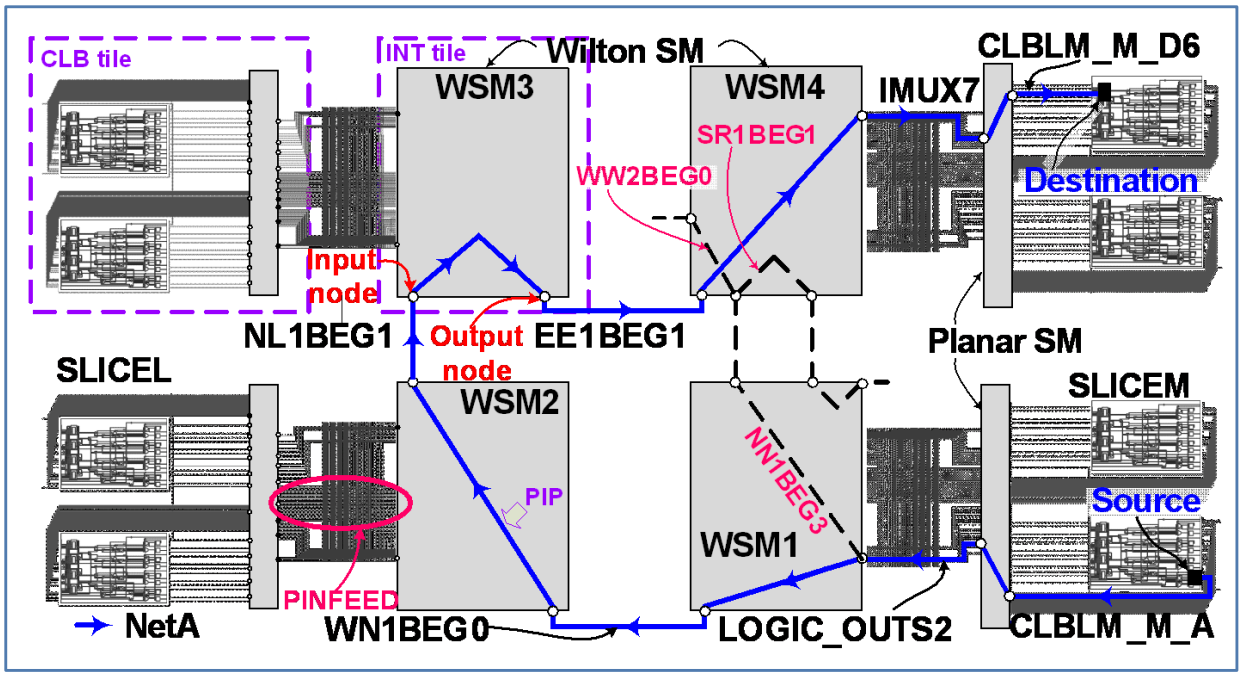


Figure 5-1 : Topology of CLB and INT tiles in Xilinx 7-Series FPGAs extracted by Xilinx Vivado (Each CLB comprises two slices). Logical net NetA connects a source flip-flop to a destination LUT made of seven nodes each made of SINGLE (1L) interconnects

5.5.2 Interconnect Types Available in 7-Series FPGAs

The 7-Series FPGAs generally consist of fifteen types of interconnects for data signal transmission throughout the PL of APSoC device. Interconnects linking the Wilton SMs are categorized as follows :

- **SINGLE (1*L*)** : unidirectional interconnects that span 1 CLB;
- **DOUBLE (2*L*)** : unidirectional interconnects that span 1 or 2 CLBs;
- **HQUAD (4*L*)** : unidirectional interconnects that span 4 CLBs;
- **VQUAD** : unidirectional interconnects that span 6 CLBs;
- **BOUNCEACROSS** : unidirectional interconnects that span 1 CLB only vertically;
- **VLONG** : bidirectional long interconnects that span 20 CLBs vertically;
- **VLONG12** : bidirectional long interconnects that span 12 CLBs vertically;

- **HLONG** : bidirectional long interconnects that span 20 CLBs horizontally;
- **GLOBAL** : homogeneous and unidirectional interconnects that span 20 CLBs vertically and are dedicated to route specific signals (clock, reset, enable, etc.);
- **BENTQUAD** : unidirectional interconnects that bend and span 6 CLBs;
- **PINFEED** : short interconnects that link Wilton SM to planar SM (coming into planar SM);
- **OUTBOUND** : short interconnects that link planar SM to Wilton SM (outgoing from planar SM); some of them also span 1 CLB;
- **BOUNCEIN** : short internal Wilton SM interconnects at some input nodes used to bounce signal;
- **PINBOUNCE** : short internal Wilton SM interconnects at some output nodes used to bounce signal;
- **HVCCGNDOUT** : GND and VCC interconnects to link Wilton SM nodes to logic ‘0’ or logic ‘1’, respectively.

Table 5-1 provides the number of each interconnect’s type connected to a Wilton SM. Four out of a total of 24 OUTBOUND interconnects span one CLB, while the other twenty interconnects link planar SMs to the Wilton SMs. Notice that interconnects of a same type may have different topologies. For example, SINGLE or DOUBLE interconnects that span one and two CLBs respectively, may have a fanout of one or two Wilton SMs, as shown in Figure 5-2.

A logical net, for example NetA shown in Figure 5-1, is made of a list of nodes {Source, CLBLM_M_A, LOGIC_OUTS2, WN1BEG0, NL1BEG1, EE1BEG1, IMUX7 CLBLM_M_D6, Destitation} connecting a flip-flop source to a LUT destination that has been routed with Xilinx Vivado. NetA has seven nodes made of SINGLE (1*L*) interconnect that spans only 1SM. There exists a group of input pins associated with a planar SM at the side of Wilton SM (right side of planar SM for SLICEL and left side of planar SM for SLICEM) that feeds data signal from Wilton SM to planar SM via PINFEED interconnects (Figure 5-1). The dashed interconnects NN1BEG3, WW2BEG0 and SR1BEG1 in Figure 5-1 are examples of undesired interconnects that could be connected to the node *LOGIC_OUTS2*. They can be connected and add a capacitive load to NetA via a bit-flip generated by an SEU on their respective PIP.

Table 5-1 : Types and number of interconnects linked to each WSM in 7-series FPGAs [181]

Interconnect Type	Number of Interconnects Connected to each Wilton SM
DOUBLE	70
SINGLE	68
BOUNCEACROSS	17
VLONG	3
HLONG	3
PINFEED	42
OUTBOUND	24
BOUNCEIN	9
PINBOUNCE	16
GLOBAL	12
HQUAD	17
BENTQUAD	34
VQUAD	18
VLONG12	2
HVCCGNDOUT	2

5.5.3 PIP Notion and Interconnect Coordinate

In 7-Series FPGAs, a PIP is called by the name of interconnect it is connected to and the interconnect coordinates. In addition, depending on the interconnect's tail (the beginning or the end of interconnect), the PIP takes an index of BEG or END. For example, a PIP in the tiles having coordinates X=10 and Y=17, connecting the beginning (BEG) of a DOUBLE (2*L*) interconnect coming from southeast (SE) tile and the beginning (BEG) of a SINGLE (1*L*) interconnect going to northwest (NW), is identified as :

pip INT_R_X10Y17 SE2BEG0 → NW1BEG2

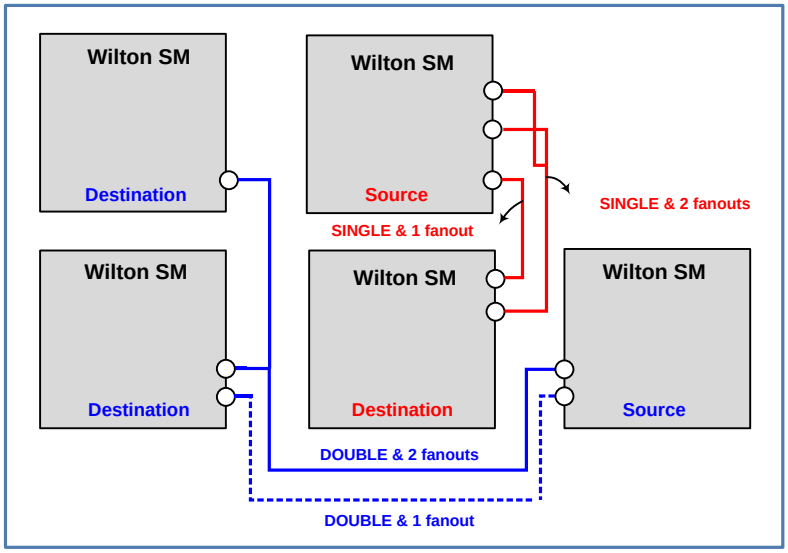


Figure 5-2 : Different topologies of DOUBLE (top) and SINGLE (bottom) interconnects in 7-Series FPGAs

where INT_R_X10Y17 denotes that the PIP belongs to the tile located at coordinate X10Y17. The numbers before BEG denote the interconnects' length they are connecting (2 for DOUBLE interconnect and 1 for SINGLE interconnect). The last number indicates the index in order to distinguish interconnects of a same category.

The outputs of each slice (flip-flop outputs, Mux outputs, or LUT outputs) are denoted as *CLBLx_y_pinname* that are connected to the planar SM. Depending on the source component's location, *x* can be '*M*' or '*L*' representing SLICEM (memory) and SLICEL (logic), respectively. The SLICEL is used to implement only combinational logic function, while the SLICEM can also be configured to implement distributed 64-bit RAM or shift registers. Also, the slice's type is denoted by *y* which can be '*M*', '*L*', or '*LL*' that represent the SLICEM, first SLICEL, and second SLICEL in a CLB, respectively. For example, *CLBLM_M_A* shown in Figure 5-1, means that the output of the first LUT (i.e., *A*) in SLICEM is chosen. The planar SM connects the output pins of slices to the PIPs denoted by *LOGIC_OUT*.

Figure 5-3 shows the parasitic interconnects connected to the NetA depicted in Figure 5-1. The undesired interconnect of *NN1BEG3* is linked to NetA due to the 1st SEU effect on the configuration bit of the PIP in WSM1. This results in an additional capacitive load to NetA and consequently delaying the signal traversing the net. Then, the interconnects of *SR1BEG1* or

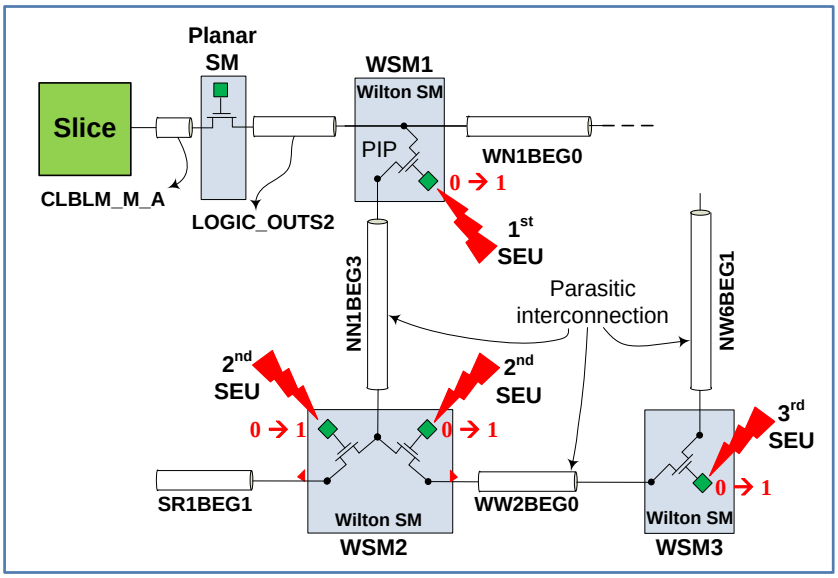


Figure 5-3 : Interconnection of unrouted interconnects to NetA in different WSM levels due to SEU implication for the example in Figure 5-1

WW2BEG0 in WSM2 are connected to WSM1 through a 2nd SEU. Finally, a 3rd SEU links the interconnect of *NW6BEG1* to the precedent parasitic interconnects by affecting the configuration bit of the PIP in WSM3. It is assumed that each SEU affects one PIP at a time.

5.6 Identification of Extra Interconnects Linked to a Logical Net

As mentioned earlier in Section 5.5.2, a bit-flip generated by an SEU on the respective PIP of an interconnection, links a parasitic extra interconnection to the live net (e.g., interconnection of *NN1BEG3* to NetA in Figure 5-1) and a DC is induced to this net. Sensitivity evaluation of different interconnect types in the routing network to SEU and DC generation as the scope of this paper, requires the identification of the respective PIPs associated with the parasitic extra interconnects. Manual PIP identification is a time consuming, tedious, and inaccurate process. Therefore, an automated algorithm is proposed in order to identify those PIPs in different WSM levels associated with a configured net (e.g., NetA in Figure 5-1).

5.6.1 Routing Algorithm for Switch Matrices

It is possible to determine all the PIPs associated with each node of NetA in Figure 5-1 that are connected to an input or output pin of a WSM. A trivial method is to select an input/output pin of

a WSM and manually check the *PIP Junction Properties* in Vivado. This property identifies the PIPs of only one pin of a WSM at a time. It means that, it is not possible to identify the PIPs associated with several pins of a WSM, or the PIPs in different WSM levels simultaneously. This is very time consuming and inaccurate due to possible mistakes in net selection for designs including several nets. Automatic determination of all PIPs associated with each node facilitates the analysis of SEU-induced DCs.

An algorithm is proposed for WSMs that automatically extracts all the PIPs in all WSM levels associated with each pin for any logic net as described in Figure 5-4. In this pseudo-code, the source and destination logic cells are generated and placed with the FPGA floorplanner in `STEP 1`. The notion of logic cell here refers to a slice logic element, such as flip-flop or LUT. Then, a net is routed between the source and destination (`STEP 2`). Starting from the first WSM (`wsm_level = 1`) in `STEP 3` associated with the routed net, a loop is defined in `STEP 4` by considering all the nodes consistent with the routed net connected to a WSM input. In `STEP 5`, all the nodes associated with level 1 WSM are found by calling the `fnode_PIPs` function defined in `STEP 11-18`. Using the non-empty condition on the `node_list`, for each found PIP in level 1 WSM, the PIPs available in the next WSM level are explored and saved. Figure 5-5 shows a partial result for extraction of all PIPs associated with nodes *LOGIC_OUTS2* and *NN1BEG3* available in WSM1 and WSM4 respectively (Figure 5-1) by implementing the pseudo-code of Figure 5-4. The results for higher levels of WSMs are not shown in this figure for the sake of clarity. The PIPs in the left column are those linked to *LOGIC_OUTS2* in WSM1 shown in Figure 5-1, while the PIPs in the right column are those connected to *NN1BEG3* in WSM4.

```
Generate and place Source and Destination logic cell;
Route the net between Source and Destination;
wsm_level = 1;
For each node on the routed net connected to a WSM input
    node_list(wsm_level) = fnode_PIPs(node, pips(node));
    While (node_list(wsm_level) != empty ){
        For each node in node_list(wsm_level)
            node_list(wsm_level +1) = fnode_PIPs (node, pips(node));
    wsm_level ++;}
End

Function fnode_PIPs(node, pips(node)) {
    For ∀downhill pip connected to node {
            If pip not in pips(node)
                put pip into pips(node);
                node = find_next_WSM_input(pip);
                If(node != empty)
                    put node into node_list;}
    return(node_list);
```

Figure 5-4 : Proposed algorithm for WSMs

PIPs in wsm_level =1: (nodes connected to LOGIC_OUTS2)		PIPs in wsm_level = 2: (nodes connected to NN1BEG3)	
WW4BEG0	NW2BEG0	WW4BEG0	LV_L0
WW2BEG0	NR1BEG0	WR1BEG1	WW2BEG0
WR1BEG1	NN6BEG0	NL1BEG_N3	WL1BEG2
WL1BEG_N3	NN1BEG3	NW6BEG0	SW6BEG3
SW6BEG0	NE6BEG0	NW2BEG0	SW2BEG3
SW2BEG0	NE2BEG0	NN6BEG0	SS6BEG3
SS6BEG0	IMUX_L8	NN2BEG0	SS2BEG3
SS2BEG0	IMUX_L40	NE6BEG0	SR1BEG1
SR1BEG1	IMUX_L32	LV_L18	ER1BEG_S0
SL1BEG0	IMUX_L24		
SE6BEG0	IMUX_L16		
SE2BEG0	IMUX_L0		
NL1BEG_N3	ER1BEG1		
BYP_ALT0	EL1BEG_N3		
FAN_ALT0	EE4BEG0		
NW6BEG0	EE2BEG0		

Figure 5-5 : Extracted PIPs connected to LOGIC_OUTS2 and NN1BEG3 interconnects in WSM1 and WSM4

```
set_property FIXED_ROUTE {CLBLM_M_A CLBLM_LOGIC_OUTS12 WN1BEG0 NL1BEG1 EE1BEG1 IMUX7 CLBLM_M_D6} [get_nets netA]
```

Figure 5-6 : Example of a directed routing in Vivado using TCL scripting

5.7 Proposed Architecture for Delay Change Evaluation

The configuration bits exhibit a substantial vulnerability to SEU. This results in an additional capacitive load to a logic net and consequently delaying the signal traversing the net. As more than 90% of configuration bits in most of SRAM-based FPGAs control the routing resources, it is desired to investigate the sensitivity of different types and lengths of interconnects to SEU available in the regular massive interconnection network of the FPGA device. This section presents an architecture based on arrays of ring oscillators (ROs) to evaluate the sensitivity to SEU of each respective interconnect as listed in Table 5-1 in bold style.

Among the fifteen different types of interconnects associated with the PL part of the Zynq-7000 APSoC, six of them cannot be employed to build ROs due to their dedicated role or specific location in the fabric. For example, the GLOBAL interconnects are dedicated to specific signals such as clock, reset, enable. HVCCGNDOUT interconnects are dedicated VCC and GND for TIEOFF logic. The PINFEED and OUTBOUND interconnects located between planar SM and Wilton SM and ROs cannot be built with only these interconnects. BOUNCEIN and PINBOUNCE are extremely short internal Wilton SM interconnects used to bounce signal. The remaining seven interconnects listed in Table 5-2 were used to build seven different ROs. A combination of VLONG, VLONG12 and HLONG interconnects was also used to configure a RO with long interconnects.

Figure 5-7 shows a routing diagram representation of three different sets of ROs implemented to the FPGA. Figure 5-7(a) to Figure 5-7(c) show routing diagrams of horizontal ROs, the BENTQUAD RO, and the vertical ROs, respectively. In this figure, each Wilton SM is shown with a circle (*SM*) and each interconnect is shown with an arrow (*I*). The proposed RO architecture makes use of long routing paths and only two logic components. It is known that logic resources made of LUTs are vulnerable to radiation [32], [140] and their number are minimized in our experiments to increase the delay faults occurrence compared to logic fault due to SEU. Each RO is implemented with only one interconnect type. For example, SINGLE (1*L*) RO type is made with a chain of 1*L* interconnects connected together through consecutive Wilton SMs. Each RO consists of two LUTs and the chain of interconnects. One of the LUTs is configured as an inverter and the other one as a buffer. Two pins are associated with the buffer, cut and enable, in order to turn on or off the oscillation.

Table 5-2 : Characteristics of the implemented ROs to the FPGA

RO Type	Orientation	Number of Wilton SMs in RO	Measured Frequency (kHz)	Delay Resolution (ps)
1L	H	96	4906	41.53
2L	H	67	22750	1.93
4L	H	36	6392	22.47
LONG	H	58	16104	3.86
BENTQUAD	H	124	23541	1.80
BOUNCEACROSS	V	32	29852	1.12
VQUAD	V	51	29784	1.13

The orientation and placement of ROs depends on the orientation of its constitutive interconnects (Figure 5-7). The BENTQUAD interconnects bend and span six CLBs unlike the other horizontal ROs that are straight. Table 5-2 provides the orientation (i.e., *H* for Horizontal and *V* for Vertical) and number of Wilton SMs used to implement each type of RO. The RO configured with BENTQUAD interconnects took more number of Wilton SMs because of its shape and bending within the SMs and it is therefore expected to be more sensitive to SEU. The frequency measurement was performed through a pre-configured Linux scheduler using high resolution timers configured as frequency counters. Each RO has its dedicated counter located on a reference board, i.e. another Zedboard including a Zynq-7000 FPGA, not submitted to radiation (Figure 5-8 (a)). Given the high neutron beam flux during experiments, a sampling rate of 1000 samples/sec was considered for frequency counters over a high resolution in the frequency measurement. Therefore, a resolution of 1 kHz was obtained which translates into a theoretical delay measurement resolution of :

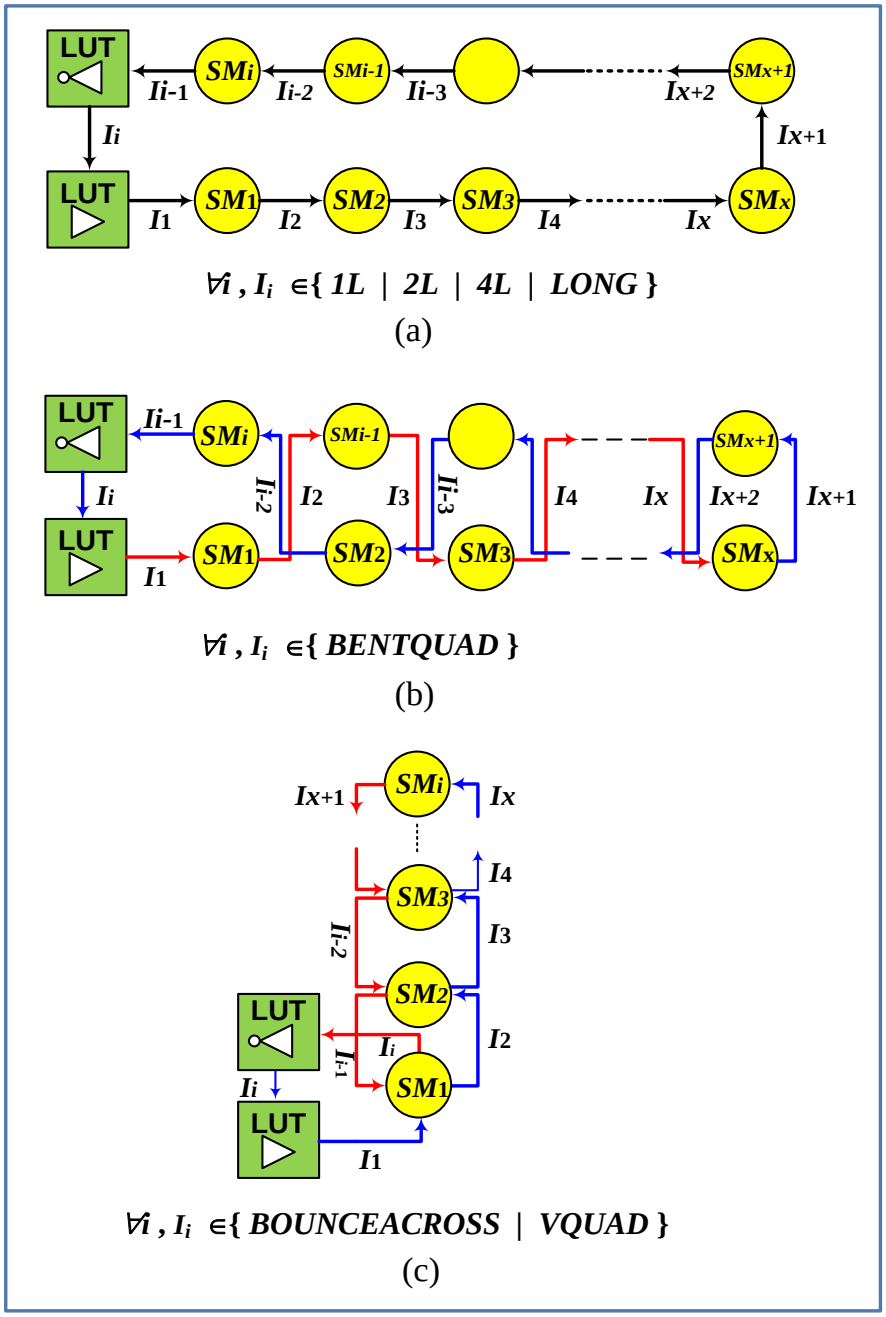


Figure 5-7 : Routing diagram for three different sets of ROs implemented to the FPGA : (a) diagram of 1*L*, 2*L*, 4*L* and LONG interconnects, (b) diagram of BENTQUAD interconnects, and (c) diagram of BOUNCEACROSS and VQUAD interconnects

$$\text{Delay resolution} = \frac{1}{f_n - 1} - \frac{1}{f_n} \tag{5-1}$$

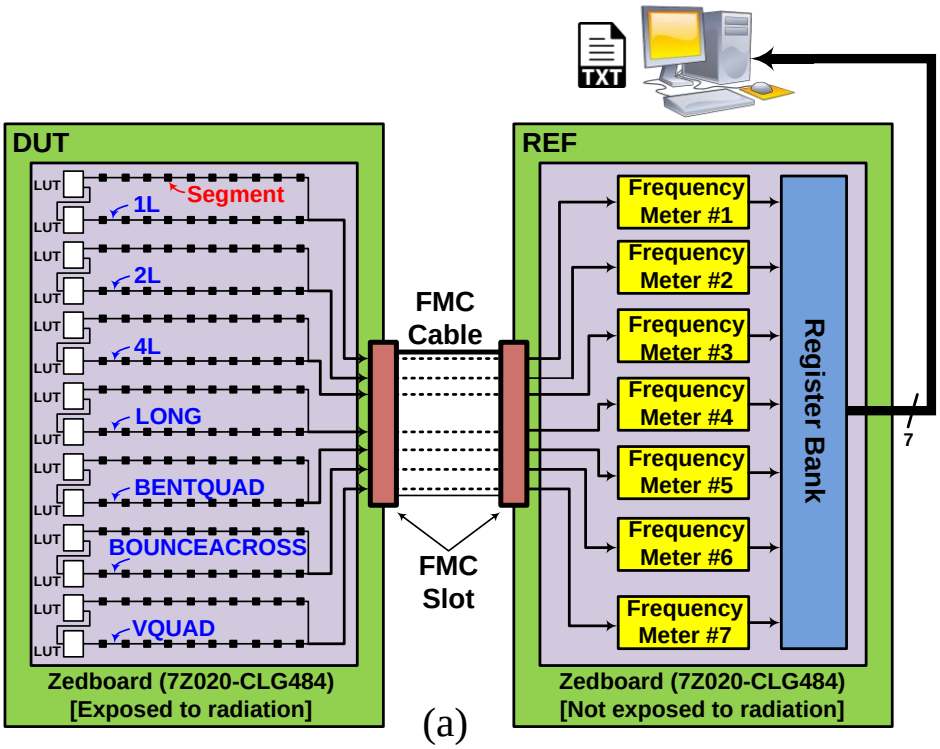
where f_n is the nominal frequency of each RO. The term f_n-1 denotes the minimum decrement of the nominal frequency caused by a DC. Table 5-2 presents the measured nominal frequencies of each RO along with the corresponding theoretical delay resolution. As can be seen in Table 5-2, the delay resolution for 1*L* and 4*L* ROs was not sufficiently small due to their smaller frequencies compared to the other ROs.

5.8 Experiments and Results

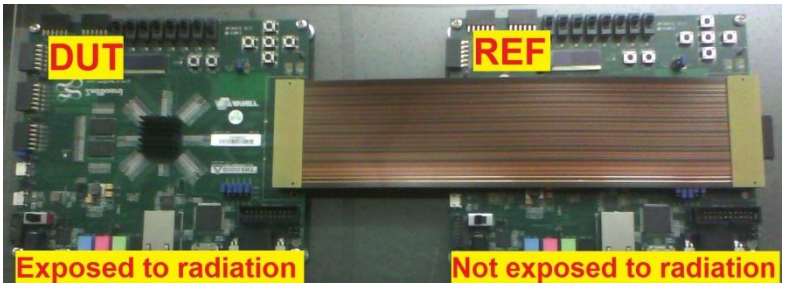
In the experiments, different ROs were implemented on the PL side of ZedBoard Zynq-7000 APSoC (including 7Z020-CLG484 where 7Z020 is the device name and CLG484 is the package name) and their frequencies were measured during run time while the top side of the DUT was exposed to neutron radiation. Frequencies were expected to change due to SEU injection and the extra load that creates delay changes on ROs' routings. Experiments were performed at TRIUMF laboratory in a beam line that provides a high-intensity neutron beam having a similar energy spectrum as the neutron found in the terrestrial atmosphere. The energy spectrum ranges from 10 to 400 MeV and its flux is 5e6 neutrons/cm^2/sec [184]. It should be noted that even at low intensity, some minutes of exposure in neutron beam can be considered as years of operation in high atmosphere.

5.8.1 Setup

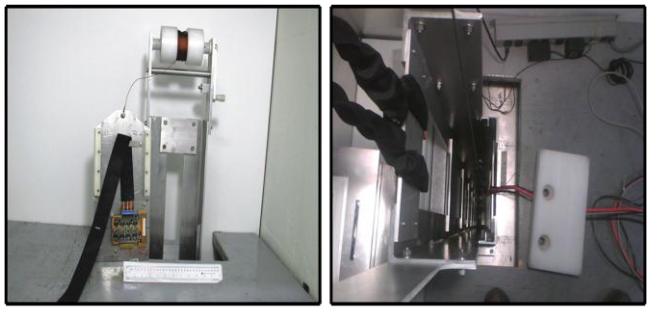
The frequency of implemented ROs is measured by using a dedicated pre-configured Linux scheduler to be used as a high resolution timer. This timer is used as an individual frequency meter for each RO during irradiation run time. In order to protect the frequency meters against radiation, they were implemented on a second ZedBoard that is referred as the reference board.



(a)



(b)



(C)

Figure 5-8 : (a) Diagram of experimental setup including DUT and reference (REF) ZedBoards; (b) Interfacing two ZedBoards via FMC cable; (c) Front and top view of neutron beam shaft at TRIUMF lab

The interface between the two ZedBoards is realized via a single low-pin-count (LPC) FMC slot provided on the ZedBoard. The LPC FMC connector exposes 68 single-ended I/Os that can be configured as 34 differential pairs. This interface spans over two PL I/O banks in 7Z020-CLG484 device. Figure 5-8 (a) shows the diagram of experimental setup prepared for the TRIUMF radiation experiments. Figure 5-8 (b) shows two ZedBoards interfaced via LPC FMC cable ready to be sent to the neutron beam tunnel. Front and top view of the neutron beam shaft are also shown in Figure 5-8 (c). The setup is installed on the beam shaft and is sent to 6m underground where the neutron beam is located.

5.8.2 Results and Discussion

Sixteen experiments were performed at TRIUMF laboratory for various run times. Data acquisition from the reference board was performed in control room. Data corresponding to each RO's frequency was individually saved in a text file using a software routine.

For example, Figure 5-9 shows one set of results obtained for the RO configured with HQUAD interconnects called RO 4L. As can be seen in this figure, the RO frequency decreases over time due to SEU-induced DCs. The run time for this set was almost 16′40″. The histogram of results for one set of RO 4L is shown in Figure 5-10. This histogram shows six overlapped Gaussian distributions, while each distribution corresponds to an oscillating frequency including variations mainly due to jitter. The mean value of each distribution is considered as the RO's frequency during the radiation run time. The mean of the first distribution on the right is the nominal frequency at the beginning of neutron exposure run. The next distribution peak represents the frequency decrement of the RO due to the addition of a parasitic interconnect to the RO's routed net, which creates a DC and decreases the RO frequency.

Gaussian Mixture Model : Histograms of obtained results were matched to Gaussian Mixture Models (GMM). GMM is a parametric probability density function that is represented as a weighted sum of M Gaussian distributions. They are commonly used in parametric modeling of the probabilistic distribution of continuous measurements. A GMM is given by :

$$p\big((x|\lambda)\big) = \sum_{i=1}^{M} w_i g(x|\mu_i\,, \sigma_i\,) \tag{5-2}$$

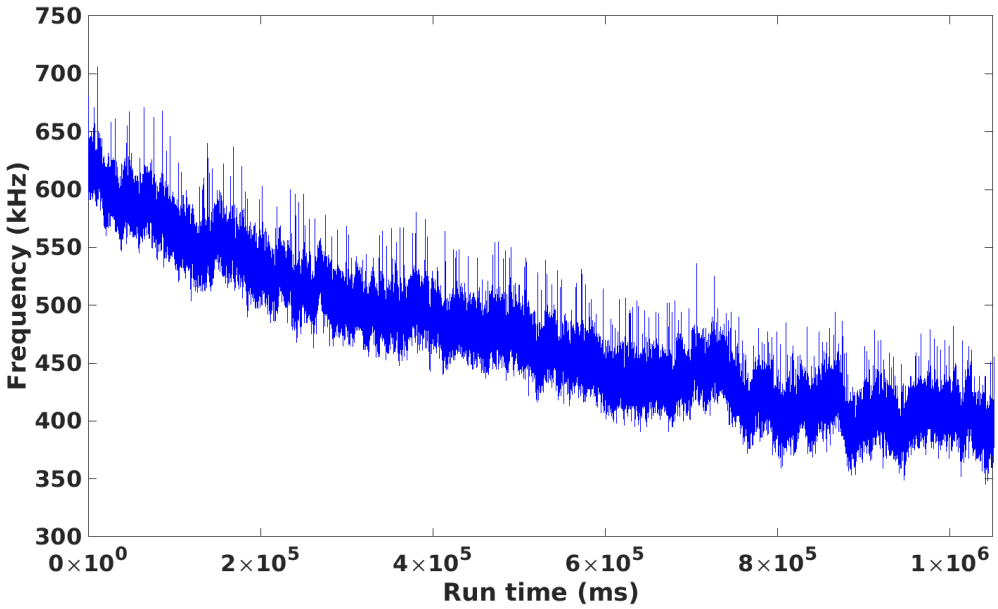


Figure 5-9 : One set of results obtained for the RO 4L configured with HQUAD interconnects. The RO frequency decreases over time due to induced DCs

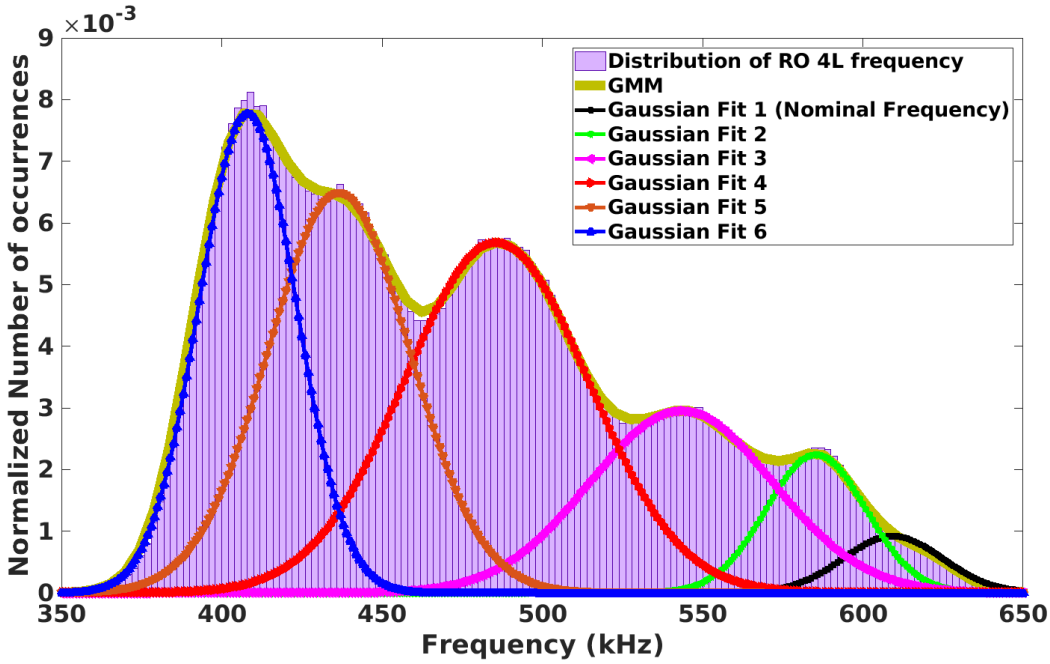


Figure 5-10 : One set of results obtained for the RO 4L configured with HQUAD interconnects with GMM model and separated distributions

where x is a D-dimensional data vector (i.e., measurements), $w_i, i = 1, 2, \ldots, M$, are the weight, and $g(x|\mu_i, \sigma_i)$ denotes the individual Gaussian distribution components. The mixture weights must always satisfy the constraint that $\sum_{i=1}^{M} w_i = 1$. Commonly, a complete GMM is parameterized by all the mean vectors, covariance matrices and weights of individual Gaussian distributions [185]. GMM curve as well as the separated distributions (*Gaussian Fit 1(nominal frequency) to Gaussian Fit 6*) are shown in Figure 5-10.

A database of frequency variations for all ROs in sixteen runs was analyzed to extract DC values generated by SEUs. It should be mentioned that DC was not necessarily observed on all the oscillators during all the runs. Therefore, for those runs where a DC does not occur, only a single distribution exists (i.e., M=1 in Equation (5-2)). The minimum DC value to be experimentally measured with the proposed setup not only depends on the resolution of its corresponding RO (see Table 5-2), yet to the capability of the GMM model to distinct two close DCs in separate Gaussian distributions. The minimum separation factor was extracted by applying the GMM model on two Gaussian distributions when the minimum separation value was swept between 1 ps and 100 ps with steps of 10 fs. Our validation shows that the minimum separation detected by the GMM model was almost 5 ps using the maximum standard deviation of 28.8 kHz observed in our experimental data. The minimum observed DC in the course of sixteen runs in neutron exposure experiments was 8 ps which is consistent with the DC of 5 ps obtained through simulation over PVT variation as shown in Table 5-3, supporting that our data analysis method enables the detection of a small DC occurrence.

Figure 5-11 shows the DC values for all runs of RO configured with BENTQUAD interconnects called RO BTQ, where a DC was observed. The frequency of RO BTQ before neutron exposure is shown in Table 5-2 considering that the board has been reset between each run. In this figure, if similar DC values are repeated, multiple DCs are shown as stacked bars. The values observed in different runs of RO BTQ show a trend in DCs. Tracing the values in horizontal axis shows that a group of DCs can fit in the same category but with a small variation. The reason behind this variation could be a slight difference between the interconnect lengths for a same interconnect type.

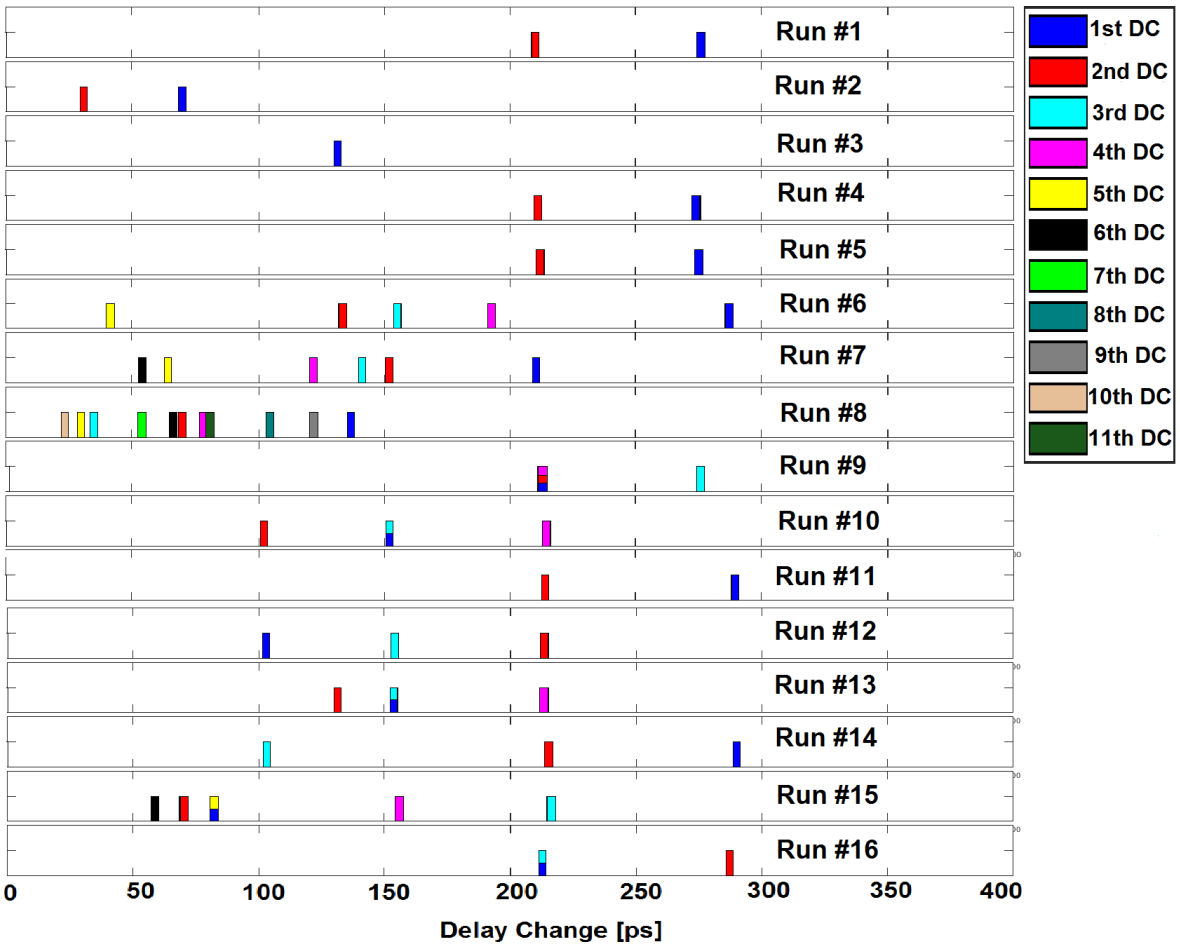


Figure 5-11 : Measured delay change values for all runs of RO BTQ

In order to find a relationship between the DC results obtained experimentally and of the delay created by the different interconnects, delays are extracted from the Xilinx Static Timing Analyzer (STA) tool in Vivado. Parasitic interconnects were added to the RO's routed net with the algorithm presented in Section 5.6.1 and the difference in RO's frequency was measured for all the PIPs and all WSM levels. Table 5-3 gives the extracted DC value corresponding to each interconnect type in one WSM level by considering the process-voltage-temperature (PVT) variations. If an interconnect type falls in multiple DC ranges, it means that there are several topologies available for that type. It is noted that, multiple different parasitic interconnect types can be connected together due to previous SEUs and then might be linked to the RO's routed net with a new SEU resulting in a large DC value. For example, as shown in Figure 5-3, it is possible that the parasitic interconnects *NW6BEG1*, *WW2BEG0*, *SR1BEG1*, and *NN1BEG3* are connected

Table 5-3 : Estimated induced DC value corresponding to each interconnect type

Interconnection Type	Approximate value of DC induction [ps]	Label in Figure 5-12
HVCCGNDOUT	5~20	(1)
PINBOUNCE or BOUNCE IN	21-40	(2)
BOUNCE IN	41-60	(3)
OUTBOUND	61-76	(4)
OUTBOUND or PINFEED	74-89	(5)
1L or 2L	91-114	(6)
2L or 4L	109-127	(7)
4L or BOUNCEACROSS	124-133	(8)
4L or VQUAD	132-141	(9)
VQUAD or BENTQUAD	140-151	(10)
BENTQUAD or VLONG12	161-169	(11)
VLONG12 or VLONG	163-171	(12)
VLONG	191-218	(13)
HLONG or VLONG	216-248	(14)
HLONG	271-284	(15)
HLONG or GLOBAL	281-310	(16)
GLOBAL	332-346	(17)

together via previous SEUs injected to the PIP inside WSM2 and WSM3. Then, a newer SEU injected to the PIP inside WSM1, may link these parasitic network to the RO's routed net. For instance, the DC value in the range of 132~141 ps shown in Table 5-3 could also be induced through two SEUs. To this end, a primarily SEU may link a 2*L* (or 4*L*) interconnect to a PINBOUNCE (or BOUNCEIN) interconnect and a secondary SEU may link this parasitic netwotk to the RO's routed net.

All of DC occurrences for each RO type are shown in Figure 5-12 in the course of 16 runs along with the 17 extracted DC ranges of Table 5-3 for comparison. DCs as small as 8 ps and as large as 364 ps were experimentally observed. The abbreviations of BNC and VQD in Figure 5-12

represent the ROs configured with BOUNCEACROSS and VQUAD interconnects, respectively. It is seen in this figure that the RO BTQ and RO BNC show the highest sensitivity, while the RO VQD and RO 1L show the lowest sensitivity to SEU, although no DC lower than 41 ps could be detected on RO 1L because of its low frequency limitation.

Considering the GMM distribution, the time of DC occurrences were extracted for each run of ROs as shown in Figure 5-13. For each distribution, the individual data points (i.e., frequency values) are added one-by-one to the distribution curve and the distribution error is calculated. If the added data belongs to the distribution, the error will decrease. When adding a new data point increases the error, it means that it does not belong to the current distribution curve and falls into the next distribution. Figure 5-13 shows the time of occurrences for RO BTQ in all run times. The horizontal axis is the time in milliseconds and the vertical axis is the run number. The area labeled with '*No hit*' in the legend is the time before the 1st DC observation. The impact of 1st DCs on the RO's routing net will last until the time that 2nd DCs occur and so on.

The '*Last DC*' label is the time after the last DC occurrence until the end of the run. A trend is observed where when the first DC appears later, chances of having multiple subsequent DCs increases. This result can be explained from the fact that a network of parasitic interconnects is built independently and once the RO is finally connected to it, the probability of getting more DC increases since the parasitic network encompasses several SMs and then more PIPs can be affected by SEUs. The experiments performed at TRIUMF laboratory supports the fact that DCs are induced by configuration bit-flips caused by SEU. The SEU changes the SRAM cell content and links a parasitic interconnect to a live net. Different RO configurations implemented into the FPGA allows obtaining different DC values ranging from almost 8 ps up to 364 ps.

The results of the time of DCs occurrence obtained experimentally for all ROs (presented for one RO in Figure 5-13) can be considered in statistical evaluation and exponential distribution of the time between DCs in a Poisson point process, i.e., a process in which events occur continuously and independently at a constant average rate. Indeed, suppose the DUT is in normal operation at $t = 0$ where no DC is yet induced by SEU (i.e., the areas labeled with '*No hit*' in the legend of Figure 5-13). Consider the first DC is induced at t_1, the second DC is induced at t_2, up to the last DC. The Probability Density Function (PDF) of an exponential distribution can be identified as Equation (5-3).

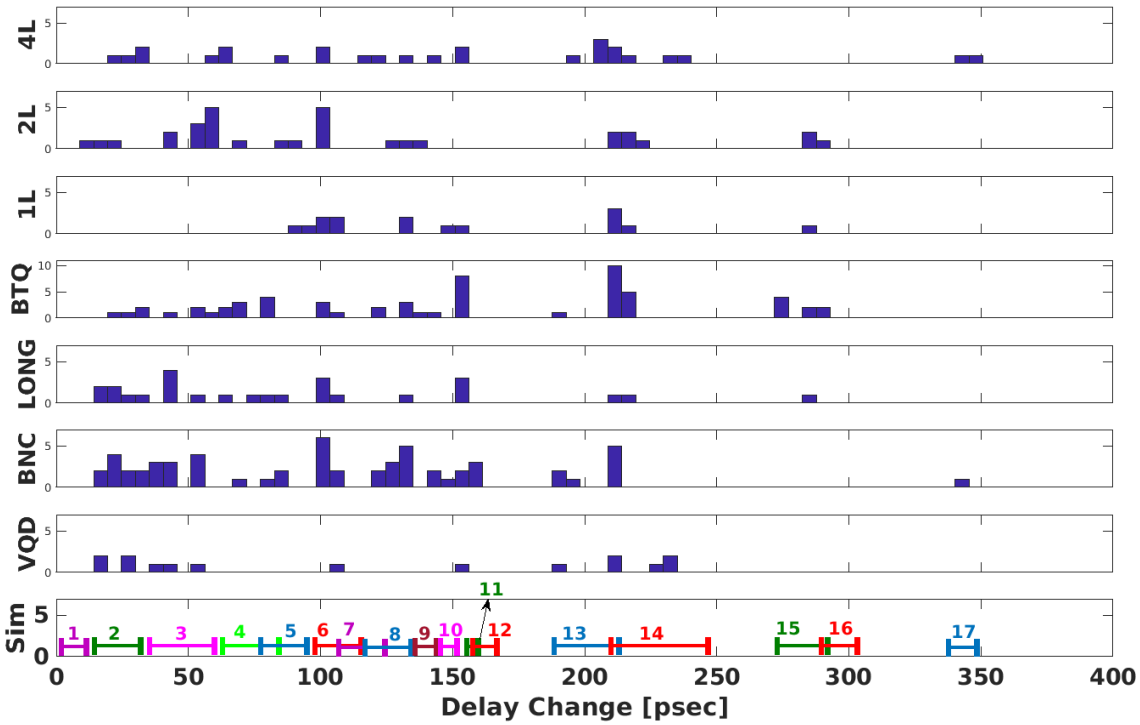


Figure 5-12 : All DC occurrences for each RO type observed in the course of 16 runs along with simulation results

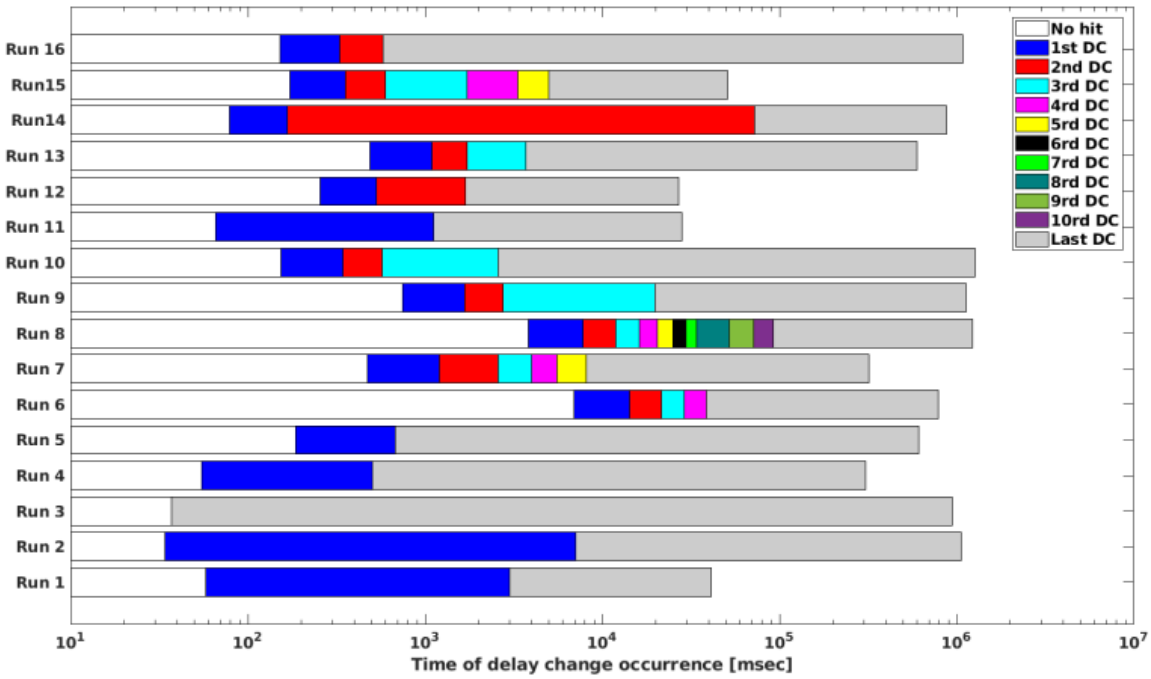


Figure 5-13 : DC time of occurrences for RO BTQ in the course of 16 run times

$$f(t,\beta) = \begin{cases} \frac{1}{\beta} e^{\frac{-t}{\beta}}, & t \geq 0 \\ 0 & , t < 0 \end{cases} \tag{5-3}$$

where β is defined as the mean (average) of the exponential distribution and it is a scalar parameter. The term t is considered as the time interval between a DC occurrence and the precedent DC $(t_i - t_{i-1})$, except for the first DC, that is the time since the beginning ($t = 0$) up to t_1. Those time intervals are generally assumed to be a random number (based on the random nature of SEU injection) that are exponentially distributed. This is known as the exponential fault law, where the fault is intrinsically the induced DCs in our application. Since the well-known term of Mean Time To Failure (MTTF) [186-189] is not an appropriate definition for our application (the system does not necessarily fails due to DC induction), we define these time intervals as Mean Time To Delay Change (MTTDC).

A commonly-used alternative parameterization is to define $\lambda = \beta^{-1}$ that is considered as DC events rate. In this specification, the parameterization involves the "rate" parameter arises in the context of DCs arriving at a rate λ, when the time between DC occurrences has a mean of β.

Table 5-4 provides the mean values ($\beta = \lambda^{-1}$) of DCs occurrence for all ROs within sixteen run times. For each RO type, the number of Wilton SMs that configure the RO (see Table 5-1) is noted in parenthesis. This table is sorted from the most sensitive RO (i.e., shortest mean time to 1st MTTDC) up to the less sensitive RO (i.e., longest mean time to 1st MTTDC). Results obtained for each RO supports the trend that as DCs occur, the probability of getting a subsequent DC increases as shown be the steady decrease of the MTTDC as the order (level) of DC occurrence increases. This trend is also explained from the buildup of an unwanted network of interconnects as the exposure time increases, hence adding more PIPs to the original RO path. It should be noted that during the course of several hours of experiment, no oscillation break down has been observed.

Table 5-4 : Mean values of DCs occurrence for all ROs in the course of sixteen run times

	RO type						
DC level	RO 1L 96	RO 2L 67	RO BTQ 124	RO BNC 32	RO VQD 51	RO LONG 58	RO 4L 36
	Mean Time to DC (β) [ms]						
1st	689	1,502	13,498	16,313	26,555	73,143	173,477
2nd	87	404	7,386	12,020	1,722	40,393	139,188
3rd	37	144	2,896	1,575	69	10,069	106,570
4th	15	88	1,776	1,341		5,056	81,388
5th		64	855	1,167		4,072	11,445
6th			850	1,123		2,535	
7th			718	325		2,096	
8th			376				
9th			144				
10th			27				
11th			7				

5.9 Conclusion and Future Works

This paper has presented a detailed analysis of routing resources in PL part of a Zynq-7000 APSoC that includes an SRAM-based FPGA (7Z020-CLG484) available on a ZedBoard. ROs have been configured using only two LUTs and routing resources as the delay chain implemented at the core of the FPGA. The frequency of ROs has been measured using dedicated timers in the reference board. The DUT have been exposed to neutron irradiation at TRIUMF laboratory. Results obtained experimentally have shown up to eleven DC occurrences. Evaluation of the time of DC occurrence shows a trend when the first DC appears later, chances of having multiple subsequent DCs increases. This result may be explained from the fact that a network of unwanted interconnects is built independently and once the RO is finally connected to it, the probability of getting more DC increases since the unwanted network encompasses several SMs and then more PIPs can be affected by SEUs. The notion of MTTDC was defined in support of mean time to DC occurrence in each RO. The trend shows that as DCs occurred, the probability of getting a subsequent DC increases as shown be the steady decrease of the MTTDC as the order (level) of DC occurrence increases. It is noted that the proposed methodology to build routing-based ring oscillators, the algorithm to identify extra parasitic interconnects linked to a logic net, as well as the experimental setup for delay change measurement can be applied to other FPGA family such as any generation of Xilinx FPGAs compatible to the Vivado design flow.

Providing an SEU emulation tool in order to inject bit-flips to the FPGA and comparing the results with those obtained experimentally would be part of our future work. It is currently a challenge since there is no link between the PL and PS parts of Zynq-7000 APSoC and there are some issues in communication between single-event mitigation tool (SEM) and the processor.

5.10 Acknowledgment

The authors would like to thank the CRIAQ organization that partially funded this project.

CHAPTER 6 GENERAL DISCUSSION

The main purpose of this thesis is the characterization, modeling and validation of the delay changes induced to the routing resources of the SRAM-based FPGAs due to SEU. It was further seen in the literature review that the logic and memory modules in SRAM-based FPGAs are susceptible to SEEs particularly SEU. However, the vulnerability of routing interconnection network to SEU and further implications of delay changes on the signals traversing the affected paths inside the FPGA, to the best of our knowledge, was overlooked in the literature.

In view of this, we have proposed circuit level models for extra combinational delays induced by SEU in SRAM-based FPGAs due to transient ionizing radiation. To this end, circuits involved in delay change generation and propagation have been reverse-engineered using the Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm CMOS technology, similar to the 65 nm triple-oxide technology node used to build Xilinx Virtex-5 FPGA. Circuit level simulation results obtained have been in good agreement with those obtained experimentally at TRIUMF laboratory. Also, the simulations and emulations performed on the I/O blocks (IOB) of the FPGA revealed the reason behind the larger DCs observed at TRIUMF in the ring oscillators that have been directly created by IOBs. It has been shown that the SEU alters the standard or drive of the IOBs. The IBIS model has been employed for the investigation of DC impact on the IOBs.

In the second part of this thesis, a delay monitor circuit has been proposed to detect and measure the observed delay changes. The proposed monitor circuit comprises an adjustable delay line, two flip-flops and an XOR gate. It is advantageous for the compact and simple architecture compared to the existing delay fault detection circuits that have been presented in the literature in CHAPTER 2. The adjustable delay line employed in the monitor design takes advantage of carry chain logics available in most of SRAM-based FPGAs. Appropriate delay tuning at the adjustable delay line and controlling the net delays for monitor’s routings enabled us to detect the induced delay changes with accuracy in the range of picoseconds for Xilinx FPGA. The SEU injection has been performed through the SEU controller IP core supported by most of SRAM-based FPGAs. The detected and measured delay changes by the monitor circuit have been shown to be in good agreement with those obtained experimentally at TRIUMF laboratory and also with the results of the circuit level simulations. In view of this, single delay changes (SDC) ranging from

29 ps to 151 ps have been detected. It was shown that the proposed delay monitor can be considered as a part of a proposed mitigation technique. It means that it is employed in addition to the scrubbing cycle occurring every 7.1 msec approximately in the Virtex-5. According to our observation, SEU created DCs are the probable event. Therefore, our scheme aims at detecting in real time those DCs affecting the most sensitive nodes in order to avoid a failure caused by a second delay change that could happen before the next scrubbing cycle. Moreover, the latest generation of FPGAs show longer scrubbing times, consequent to the gate count increment. It is noted that the proposed delay monitor circuit for delay change detection and measurement could be applied to other types of SRAM-based FPGAs, mainly the state-of-the-art devices.

The extensive investigation of the susceptibility of routing interconnection network in SRAM-based FPGAs to delay changes induced by ionizing radiation has been presented in the third part of this thesis. To this end, we have proposed a method to configure ring oscillators with mostly routing resources and a few logic resources implemented to a state-of-the-art APSoC device including an SRAM-based FPGA. We have also proposed an algorithm to automatically identify the extra parasitic interconnects linked to a logical net due to SEU. An experimental setup for delay change measurement has been proposed and implemented while the board including the ring oscillators has been exposed to a high energy neutron radiation at TRIUMF laboratory. Experimental results have shown that different interconnection types represent different behaviors against induced delay changes. Moreover, it has been shown that the susceptibility of different interconnects to SEU is not the same. For example, it was shown that the ring oscillator configured with BENTQUAD interconnects has shown the observation of up to eleven DCs. The time of delay change occurrence has been measured in the results and the notion of mean time to delay change (MTTDC) has been defined. It has been shown that later is the occurrence of the first delay change to happen, larger is the chance to receive more delay changes. Also, the results obtained have supported the fact that as the level of the delay change occurrence increases, the probability of getting a subsequent DC would increase. This has been shown by the steady decrease of the MTTDC as the order (level) of DC occurrence increases.

It is noted that the configuration of ring oscillators with routing resources is highly constrained with DRC checker in Vivado. It means that increase or decrease of the ring oscillator length may not be achieved as easy as the ring oscillators made of logic resources, e.g. inverters. Hence, the presented ring oscillators in this thesis presented different resolution and frequency based on the

length of delay line that was fine to run the ring oscillator. In addition, the proposed architecture for configuration of ring oscillators with routing resources can be adapted in other types of the APSoC devices including Xilinx SRAM-based FPGAs. Also, the proposed algorithm to identify the parasitic interconnects linked to a logical net and the experimental setup for delay change measurement are extensible and amenable to other types of state-of-the-art APSoC devices.

CHAPTER 7 CONCLUSION AND FUTURE WORKS

7.1 Concluding Remarks

This dissertation addresses the important problem of the effect of cosmic rays on electronic components employed in aircraft avionic system. The increasing demand for utilization of semiconductor devices in avionic systems has presented a substantial vulnerability against cosmic radiations. SRAM-based FPGAs are mainly susceptible to a specific type of SEE, called SEU. Sensitivity evaluation of SRAM-based FPGAs to extra combinational delays caused by SEUs has not been addressed thus far in the literature. Extra combinational delays, also called delay changes, have been observed experimentally for the first time in SRAM-based FPGAs by our research group, when the top side of the device has been exposed to high energy proton beam at TRIUMF laboratory. In this thesis, delay changes observed have been presented and their root cause has been investigated. To this end, the circuit-level model of the delay changes in SRAM-based FPGAs has been proposed which is, to the best of our knowledge, the first work on the modeling of combinational delays in FPGAs. Due to the intellectual property issues, details of the internal circuitry of the FPGA chip are not available. Therefore, circuits involved in delay propagation have been reverse-engineered by performing precise modeling of internal blocks inside the FPGA and executing simulations. Several scenarios of extra combinational delays have been simulated based on the circuit architecture of the FPGA core and routing resources. It has been shown that the main contributions to delay are extra interconnection lines unintentionally connected to the main circuit path via pass transistors activated by SEUs. Moreover, regarding the delay changes affecting the IO blocks of the SRAM-based FPGA, an experimental setup including two ring oscillators inside the FPGA created directly in the IO blocks has also been tested by our research group at TRIUMF. The main reason of longer delay changes observed on the IO blocks due to SEU was unknown at the time of experiments. It was conjectured by our group that the I/O standard or drive might be altered while bombarding the FPGA board. However, no proof has been provided by them to support this phenomenon. In this dissertation, we have strived toward the validation of this hypothesis through circuit level simulations. IBIS models of I/O blocks have been used to compare delays of the primarily implemented design to that of the supported I/O standards and drive strengths in Xilinx Virtex-5 FPGA. Each measurement has been performed for the maximum, typical and minimum levels of the intended

output signal. Simulation results are in good agreement with the experimental results obtained at TRIUMF, and they have supported the I/O standard alteration hypothesis.

The second part of this dissertation has presented the design and experimental validation of a delay monitor circuit for detection and measurement of delay changes caused by SEU in the SRAM-based FPGA. Since in most of the SRAM-based FPGAs more than 90% of the configuration bits control the routing resources, the systems designed on FPGA are particularly vulnerable to interconnection delay changes caused by SEU that affect the configuration memory. The proposed monitor has been considered as part of a mitigation technique dedicated to protect the circuit routing delay integrity while the system has been exposed to the SEUs. Experimental results have shown that the probability of occurrence of a delay change can increase when the order of delay changes affecting a node increases. This increase depends on the configurable interconnection network and the placement of the design in the FPGA. The delay measurements using the proposed monitor have revealed the existence of single delay changes ranging from 29 up to 151 psec. Also, cumulative delay changes in the range of 279 to 309 psec which are the results of an extra interconnection network added by SEUs, have been detected. Measured delay values have been in good agreement with those observed experimentally under proton radiation at TRIUMF laboratory and also the circuit-level simulations and emulations.

Finally, a detailed analysis of routing resources in the programmable logic part of a Zynq-7000 APSoC, that includes an SRAM-based FPGA (7Z020-CLG484) available on a ZedBoard has been presented. To this end, ring oscillators have been configured using only two LUTs and routing resources as the delay chain implemented at the core of the FPGA. The frequency of ring oscillators have been measured using dedicated timers in the reference board that has not been subjected to the radiation. The DUT have been exposed to neutron irradiation at TRIUMF laboratory. Results obtained experimentally have shown up to eleven delay change occurrences on a single ring oscillator. Evaluation of the time of the delay change occurrence has shown a trend when the first delay change appears later, chances of having multiple subsequent DCs would increase. This result can be explained by the fact that a network of parasitic interconnects is built independently. The Mean Time To Delay Change (MTTDC) occurrence in each ring oscillator has been defined. The trend has shown that when delay changes occurred, the probability of getting a subsequent delay change increased.

7.2 Scope for Future Work

Toward the improvement of the objectives achieved in this dissertation, some recommendations for the future work are presented.

The proposed delay monitor circuit has been tested and validated experimentally on Virtex-5 FPGA using the available tools such as Xilinx ISE which exhibits some limitations for the designer. However, modern tools such as Vivado, which supports Virtex-5 and onwards, provide more flexibility for the designer to implement the monitors in the state-of-the-art FPGAs. To this end, it would be beneficial to generate a tool that would automatically tune and add the adjustable delay line of monitors in a design according to a specified slack time of all extracted sensitive nodes in a design. Also, it might be possible to achieve better resolutions for the adjustable delay line by incorporating the programmable interconnection points associated with switch matrices. In addition, the impact of the size of logic cone could be investigated. It has been mentioned that the delay monitor circuit is beneficial for designs with few number of critical paths. However, increasing the design density will increase the number of critical paths and will not be beneficial to incorporate the monitor on all of the critical paths. Hence, further analysis would be interesting to derive a relation between the design densities, number of critical paths and also the numbers of less critical paths, i.e., the paths that may not detect lower DC orders, yet become critical against higher levels of DC. Therefore, a sort of most critical paths reported by this analysis may help to employ the delay monitor circuit only on the nodes that are really necessary.

Regarding the investigations performed on the susceptibility of routing resources to SEU in a Zynq-7000 device, some improvements may be made. Moreover, currently there is a challenge to make a link between the PL and PS parts of Zynq-7000 APSoC for SEU injection purpose and there are some issues in communication between single-event mitigation tool (SEM) and the processor. Therefore, providing an SEU emulation tool in order to inject bit-flips to the FPGA and comparing the results with those obtained experimentally can be part of the future studies.

BIBLIOGRAPHY

[1] G. C. Messenger, "Radiation Hardening of Electronic Systems Invited Paper," *IEEE Transactions on Nuclear Science,* vol. 16, pp. 160-168, 1969.

[2] R. H. Maurer, M. E. Fraeman, M. N. Martin, and D. R. Roth, "Harsh Environments : Space Radiation Environment, Effects, and Mitigation," *Johns Hopkins Apl Technical Digest,* vol. 28, pp. 17-29, 2008.

[3] T. Freeman. Facing up the Secondary Neutrons [Online]. Available : http://medicalphysicsweb.org/cws/article/research/34364

[4] J. H. G. Swift. Mitigating single-Event Upsets, WP395 (v1.0) [Online].

[5] F. Kastensmidt and P. Rech, *FPGAs and Parallel Architectures for Aerospace Applications : Soft Errors and Fault-tolerant Design* : Springer, 2015.

[6] Radiation Hardening [Online]. Available : http://en.wikipedia.org/wiki/Radiation_hardening

[7] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *Device and Materials Reliability, IEEE Transactions on,* vol. 5, pp. 305-316, 2005.

[8] J. L. Autran, S. Semikh, D. Munteanu, S. Serre, G. Gasiot, and P. Roche, "Soft-Error Rate of Advanced SRAM Memories : Modeling and Monte Carlo Simulation," 2012.

[9] R. Edwards, C. Dyer, and E. Normand, "Technical standard for atmospheric radiation single event effects, (SEE) on avionics electronics," in *Radiation Effects Data Workshop, 2004 IEEE*, 2004, pp. 1-5.

[10] Process management for Avionics : Preparation of an Electronic Components Management Plan [Online]. Available : http://www.iec.ch/about/brochures/pdf/technology/avionics.pdf

[11] B. Vibishna, K. Beenamole, and A. K. Singh, "Understanding single-event effects in FPGA for Avionic system design," *IETE Technical Review,* vol. 30, pp. 497-505, 2013.

[12] R. Koga. Single Event Functional Interrupt (SEFI) Sensitivity in EEPROMs [Online]. Available : http://klabs.org/richcontent/MAPLDCon98/Papers/c2_koga.pdf

[13] F. Sturesson. Single Event Effect (SEE) Testing [Online]. Available : http://space.epfl.ch/webdav/site/space/shared/industry_media/08%20SEE%20testing%20%20F.Sturesson.pdf

[14] R. Koga, S. H. Penzin, K. B. Crawford, and W. R. Crain, "Single event functional interrupt (SEFI) sensitivity in microcircuits," presented at the Radiation and Its Effects on Components and Systems, 1997. RADECS 97. Fourth European Conference on, Cannes, 1997.

[15] J. F. Tarillo, N. Mavrogiannakis, C. A. Lisboa, C. Argyrides, and L. Carro, "Multiple Bit Error Detection and Correction in Memory," in *Digital System Design : Architectures, Methods and Tools (DSD), 2010 13th Euromicro Conference on*, 2010, pp. 652-657.

[16] F. L. Kastensmidt, T. Jorge, T. Both, P. Rech, G. Wirth, R. D. L. Reis, *et al.*, "Analysing the Impact of Aging and Voltage Scaling under Neutron-induced Soft Error Rate in

SRAM-based FPGAs," in *ESREF : European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, 2014.

[17] J. J. Rodriguez-Andina, M. J. Moure, and M. D. Valdes, "Features, design tools, and application domains of FPGAs," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 1810-1823, 2007.

[18] S. Liu, M. Boden, D. A. Girdhar, and J. L. Titus, "Single-Event Burnout and Avalanche Characteristics of Power DMOSFETs," *Nuclear Science, IEEE Transactions on*, vol. 53, pp. 3379-3385, 2006.

[19] D. Munteanu, J. L. Autran, and S. Martinie, "Numerical Simulation of Transient Response in 3-D Multi-Channel Nanowire MOSFETs Submitted to Heavy Ion Irradiation," 2011.

[20] M. Allenspach, I. Mouret, J. L. Titus, C. F. Wheatley, Jr., R. L. Pease, J. R. Brews, *et al.*, "Single-event gate-rupture in power MOSFETs : prediction of breakdown biases and evaluation of oxide thickness dependence," *Nuclear Science, IEEE Transactions on*, vol. 42, pp. 1922-1927, 1995.

[21] Xilinx. Virtex-5 Family Overview (Product Specification) - DS100 (v5.1) [Online]. Available : http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf

[22] L. Bozzoli and L. Sterpone, "Self rerouting of dynamically reconfigurable SRAM-based FPGAs," in *Adaptive Hardware and Systems (AHS), 2017 NASA/ESA Conference on*, 2017, pp. 77-84.

[23] Virtex-5 Family Overview, DS100 (ver. 5.0) [Online].

[24] Virtex-5 FPGA User Guide (UG190) ver. 5.4 [Online].

[25] (March 11). *Xilinx Fpga Architecture Innovative On Regarding Excellent In Guest 17*. Available : http://donatz.info/xilinx-fpga-architecture/xilinx-fpga-architecture-innovative-on-regarding-excellent-in-guest-17/

[26] M. Ebrahimi, A. Evans, M. B. Tahoori, E. Costenaro, D. Alexandrescu, V. Chandra, *et al.*, "Comprehensive analysis of sequential and combinational soft errors in an embedded processor," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, pp. 1586-1599, 2015.

[27] B. J. P. Tomas. Introduction to Field Programmable Gate Arrays (FPGAs) [Online]. Available : http://www.ee.unlv.edu/~yingtao/2012_Spring/ECE720/student%20presentations/Introduction_to_Field_Programmable_Gate_Arrays.pptx

[28] FPGA Editor Guide [Online]. Available : http://www.xilinx.com/support/sw_manuals/2_1i/download/fpedit.pdf

[29] K. Chapman. New Generation Virtex-5 SEU Controller [Online].

[30] K. C. L. Jones. SEU Strategies for Virtex-5 Devices (XAPP864) [Online].

[31] F. Brosser and E. Milh, "SEU mitigation techniques for advanced reprogrammable FPGA in space," *Chalmers University of Technology*, 2014.

[32] C. Thibeault, S. Pichette, Y. Audet, Y. Savaria, H. Rufenacht, E. Gloutnay, Y. Blaquière, F. Moupfouma, and N. Batani, "On extra combinational delays in SRAM FPGAs due to transient ionizing radiations," *Nuclear Science, IEEE Transactions on,* vol. 59, pp. 2959-2965, 2012.

[33] P. Graham, M. Caffrey, J. Zimmerman, P. Sundararajan, and E. Johnson, "Consequences and categories of SRAM FPGA configuration SEUs," in *In Proceedings of the International Conference on Military and Aerospace Programmable Logic Devices*, 2003.

[34] H. Asadi, M. B. Tahoori, B. Mullins, D. Kaeli, and K. Granlund, "Soft error susceptibility analysis of SRAM-based FPGAs in high-performance information systems," *IEEE Transactions on Nuclear Science,* vol. 54, pp. 2714-2726, 2007.

[35] Virtex-5 FPGA Configuration User Guide (UG191) [Online].

[36] F. Z. Tazi, C. Thibeault, Y. Savaria, S. Pichette, and Y. Audet, "On Delay Faults Affecting I/O Blocks of an SRAM-Based FPGA Due to Ionizing Radiations," *arXiv preprint arXiv :1409.0736,* 2014.

[37] C. Z. Thibeault, Larry, "AVIO-403, Radiation Tolerant Embedded Systems : Design, Verification and Test Methodologies," École de Technologie Supperieur (ÉTS), Montreal, QC, Canada, Technical Report2014.

[38] D. Munteanu and J. L. Autran, "Modeling and Simulation of Single-Event Effects in Digital Devices and ICs," *Nuclear Science, IEEE Transactions on,* vol. 55, pp. 1854-1878, 2008.

[39] M. Khellah, S. Brown, and Z. Vranesic, "Minimizing interconnection delays in array-based FPGAs," in *Custom Integrated Circuits Conference, 1994., Proceedings of the IEEE 1994*, 1994, pp. 181-184.

[40] P. E. Dodd and F. W. Sexton, "Critical charge concepts for CMOS SRAMs," *Nuclear Science, IEEE Transactions on,* vol. 42, pp. 1764-1771, 1995.

[41] International Technology Roadmap for Semiconductors [Online]. Available : http://public.itrs.net

[42] Y. Song, K. N. Vu, J. S. Cable, A. A. Witteles, W. A. Kolasinski, R. Koga, *et al.*, "Experimental and analytical investigation of single event, multiple bit upsets in poly-silicon load, 64 K×1 NMOS SRAMs," *Nuclear Science, IEEE Transactions on,* vol. 35, pp. 1673-1677, 1988.

[43] Three-dimensional device simulation program manual [Online].

[44] J. Sleight, S. Bangsaruntip, A. Majumdar, G. Cohen, Y. Zhang, S. Engelmann, *et al.*, "Gate-all-around silicon nanowire MOSFETs and circuits," in *Device Research Conference (DRC), 2010*, 2010, pp. 269-272.

[45] P. Dodd, F. Sexton, and P. Winokur, "Three-dimensional simulation of charge collection and multiple-bit upset in Si devices," *IEEE Transactions on Nuclear Science,* vol. 41, pp. 2005-2017, 1994.

[46] P. E. Dodd, "Physics-based simulation of single-event effects," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 343-357, 2005.

[47] P. Roche, J. Palau, G. Bruguier, J. Gasiot, K. Belhaddad, and R. Ecoffet, "SEU response of an entire SRAM cell simulated as one contiguous three dimensional device domain," *IEEE Transactions on Nuclear Science,* vol. 45, pp. 2534-2543, 1998.

[48] P. Roche, J. Palau, G. Bruguier, C. Tavernier, R. Ecoffet, and J. Gasiot, "Determination of key parameters for SEU occurrence using 3-D full cell SRAM simulations," *IEEE Transactions on Nuclear Science,* vol. 46, pp. 1354-1362, 1999.

[49] P. E. Dodd, A. Shaneyfelt, K. Horn, D. Walsh, G. Hash, T. Hill, *et al.*, "SEU-sensitive volumes in bulk and SOI SRAMs from first-principles calculations and experiments," *IEEE Transactions on Nuclear Science,* vol. 48, pp. 1893-1903, 2001.

[50] *Particle Accelerators Around the World*. Available : http://www-elsa.physik.uni-bonn.de/accelerator_list.html

[51] E. Normand and L. Dominik, "Cross Comparison Guide for Results of Neutron SEE Testing of Microelectronics Applicable to Avionics," in *Radiation Effects Data Workshop (REDW), 2010 IEEE*, 2010, pp. 8-8.

[52] A. Lesea, S. Drimer, J. J. Fabula, C. Carmichael, and P. Alfke, "The rosetta experiment: atmospheric soft error rate testing in differing technology FPGAs," *Device and Materials Reliability, IEEE Transactions on,* vol. 5, pp. 317-328, 2005.

[53] C. Carmichael, E. Fuller, J. Fabula, and F. Lima, "Proton testing of SEU mitigation methods for the Virtex FPGA," *Proc. of Military and Aerospace Applications of Programmable Logic Devices MAPLD,* 2001.

[54] F. Faure, R. Velazco, and P. Peronnard, "Single-event-upset-like fault injection : a comprehensive framework," *Nuclear Science, IEEE Transactions on,* vol. 52, pp. 2205-2209, 2005.

[55] K. A. Clark, A. A. Ross, H. H. Loomis, T. R. Weatherford, D. J. Fouts, S. P. Buchner, *et al.*, "Modeling single-event effects in a complex digital device," *Nuclear Science, IEEE Transactions on,* vol. 50, pp. 2069-2080, 2003.

[56] L. W. Massengill, A. E. Baranski, D. O. Van Nort, J. Meng, and B. L. Bhuva, "Analysis of single-event effects in combinational logic-simulation of the AM2901 bitslice processor," *Nuclear Science, IEEE Transactions on,* vol. 47, pp. 2609-2615, 2000.

[57] R. Velazco, A. Corominas, and P. Ferreyra, "Injecting bit flip faults by means of a purely software approach : a case studied," in *Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on*, 2002, pp. 108-116.

[58] P. Fouillat, V. Pouget, D. Lewis, S. Buchner, and D. McMorrow, "Investigation of single-event transients in fast integrated circuits with a pulsed laser," *International journal of high speed electronics and systems,* vol. 14, pp. 327-339, 2004.

[59] P. Civera, L. Macchiarulo, M. Rebaudengo, M. S. Reorda, and M. Violante, "Exploiting circuit emulation for fast hardness evaluation," *Nuclear Science, IEEE Transactions on,* vol. 48, pp. 2210-2216, 2001.

[60] R. Velazco, S. Rezgui, and R. Ecoffet, "Predicting error rate for microprocessor-based digital architectures through C.E.U. (Code Emulating Upsets) injection," *Nuclear Science, IEEE Transactions on,* vol. 47, pp. 2405-2411, 2000.

[61] R. Velazco, S. Rezgui, and H. Ziade, "Assessing the soft error rate of digital architectures devoted to operate in radiation environment : a case studied," *Journal of Electronic Testing*, vol. 19, pp. 83-90, 2003.

[62] V. G. Savani, A. I. Mecwan, and N. P. Gajjar, "Dynamic Partial Reconfiguration of FPGA for SEU Mitigation and Area Efficiency," *International Journal of Advancements in Technology*, vol. 2, pp. 285-291, 2011.

[63] L. Sterpone and M. Violante, "A new reliability-oriented place and route algorithm for SRAM-based FPGAs," *Computers, IEEE Transactions on*, vol. 55, pp. 732-744, 2006.

[64] S. Nomura, M. D. Sinclair, C.-H. Ho, V. Govindaraju, M. de Kruijf, and K. Sankaralingam, "Sampling+ DMR : practical and low-overhead permanent fault detection," in *ACM SIGARCH Computer Architecture News*, 2011, pp. 201-212.

[65] G. L. Smith and L. de la Torre, "Techniques to enable FPGA based reconfigurable fault tolerant space computing," in *2006 IEEE Aerospace Conference*, 2006, p. 11 pp.

[66] F. L. Kastensmidt, G. Neuberger, L. Carro, and R. Reis, "Designing and testing fault-tolerant techniques for sram-based fpgas," in *Proceedings of the 1st conference on Computing frontiers*, 2004, pp. 419-432.

[67] K. Kyriakoulakos and D. Pnevmatikatos, "A novel SRAM-based FPGA architecture for efficient TMR fault tolerance support," in *2009 International Conference on Field Programmable Logic and Applications*, 2009, pp. 193-198.

[68] F. Lima, C. Carmichael, J. Fabula, R. Padovani, and R. Reis, "A fault injection analysis of Virtex FPGA TMR design methodology," in *Radiation and Its Effects on Components and Systems, 2001. 6th European Conference on*, 2001, pp. 275-282.

[69] S. D'Angelo, C. Metra, S. Pastore, A. Pogutz, and G. R. Sechi, "Fault-tolerant voting mechanism and recovery scheme for TMR FPGA-based systems," in *Defect and Fault Tolerance in VLSI Systems, 1998. Proceedings., 1998 IEEE International Symposium on*, 1998, pp. 233-240.

[70] C. Carmichael and C. W. Tseng. Correcting Single-Event Upsets in Virtex-4 FPGA Configuration Memory (XAPP1088) [Online].

[71] J. Heiner, B. Sellers, M. Wirthlin, and J. Kalb, "FPGA partial reconfiguration via configuration scrubbing," in *Field Programmable Logic and Applications, 2009. FPL 2009. International Conference on*, 2009, pp. 99-104.

[72] R. N. Pittman, "Partial Reconfiguration : A Simple Tutorial," MSR-TR 2012-19, 2012.

[73] E. Eto. Difference-Based Partial Reconfiguration, (XAPP290) [Online].

[74] Partial Reconfiguration User Guide (UG702) [Online].

[75] D. Koch, *Partial Reconfiguration on FPGAs : Architectures, Tools and Applications* vol. 153 : Springer, 2012.

[76] C. Kao, "Benefits of partial reconfiguration," *Xcell journal*, vol. 55, pp. 65-67, 2005.

[77] C. Carmichael, M. Caffrey, and A. Salazar. Correcting Single-Event Upsets Through Virtex Partial Configuration (XAPP216) [Online].

[78] E. Stott, P. Sedcole, and P. Y. Cheung, "Fault tolerant methods for reliability in FPGAs," in *2008 International Conference on Field Programmable Logic and Applications*, 2008, pp. 415-420.

[79] R. Glein, B. Schmidt, F. Rittner, J. Teich, and D. Ziener, "A Self-Adaptive SEU Mitigation System for FPGAs with an Internal Block RAM Radiation Particle Sensor," in *Field-Programmable Custom Computing Machines (FCCM), 2014 IEEE 22nd Annual International Symposium on*, 2014, pp. 251-258.

[80] M. B. Tahoori, "Using satisfiability in application-dependent testing of FPGA interconnects," in *Proceedings of the 40th annual Design Automation Conference*, 2003, pp. 678-681.

[81] M. B. Tahoori and S. Mitra, "Automatic configuration generation for FPGA interconnect testing," in *VLSI Test Symposium, 2003. Proceedings. 21st*, 2003, pp. 134-139.

[82] M. Abramovici, J. M. Emmert, and C. E. Stroud, "Roving STARs : an integrated approach to on-line testing, diagnosis, and fault tolerance for FPGAs in adaptive computing systems," in *Evolvable Hardware, 2001. Proceedings. The Third NASA/DoD Workshop on*, 2001, pp. 73-92.

[83] M. Abramovici and C. E. Stroud, "BIST-based test and diagnosis of FPGA logic blocks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, pp. 159-172, 2001.

[84] M. Abramovici, C. E. Stroud, and J. M. Emmert, "Online BIST and BIST-based diagnosis of FPGA logic blocks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, pp. 1284-1294, 2004.

[85] C.-L. Hsu and T.-H. Chen, "Built-in self-test design for fault detection and fault diagnosis in SRAM-based FPGA," *IEEE Transactions on instrumentation and measurement*, vol. 58, pp. 2300-2315, 2009.

[86] A. Benso, S. A. Chiusano, G. Di Natale, P. E. Prinetto, and M. Lobetti Bodoni, "Online and offline BIST in IP-core design," *IEEE Design & Test of Computers*, vol. 18, pp. 92-99, 2001.

[87] M. Abramovici, C. Strond, C. Hamilton, S. Wijesuriya, and V. Verma, "Using roving STARs for on-line testing and diagnosis of FPGAs in fault-tolerant applications," in *Test Conference, 1999. Proceedings. International*, 1999, pp. 973-982.

[88] J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Low overhead fault-tolerant FPGA systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 6, pp. 212-221, 1998.

[89] M. Abramovici and C. E. Stroud, "BIST-based delay-fault testing in FPGAs," *Journal of electronic testing*, vol. 19, pp. 549-558, 2003.

[90] C. Stroud, M. Lashinsky, J. Nall, J. Emmert, and M. Abramovici, "On-line BIST and diagnosis of FPGA interconnect using roving STARs," in *On-Line Testing Workshop, 2001. Proceedings. Seventh International*, 2001, pp. 27-33.

[91] M. Abramovici, C. Stroud, B. Skaggs, and J. Emmert, "Improving on-line BIST-based diagnosis for roving STARs," in *On-Line Testing Workshop, 2000. Proceedings. 6th IEEE International*, 2000, pp. 31-39.

[92] G. Jovanovic and M. Stojcev, "Vernier's Delay Line Time–to–Digital Converter," *A : Appl Math Inform Mech, Scientific Publications of the state University of NOVI PAZAR SER*, vol. 1, pp. 11-20, 2009.

[93] K. Chmielewski, "Multi-vernier time-to-digital converter implemented in a field-programmable gate array," *Measurement Science and Technology*, vol. 22, p. 017001, 2011.

[94] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution," *Metrologia*, vol. 41, p. 17, 2004.

[95] S. Berrima, Y. Blaquière, and Y. Savaria, "A multi-measurements RO-TDC implemented in a Xilinx field programmable gate array," in *Circuits and Systems (ISCAS), 2017 IEEE International Symposium on*, 2017, pp. 1-4.

[96] D. C. Chu, M. S. Allen, and A. S. Foster, "Universal counter resolves picoseconds in time interval measurements," *Hewlett-Packard J*, vol. 29, pp. 2-1, 1978.

[97] M. Fishburn, L. H. Menninga, C. Favi, and E. Charbon, "A 19.6 ps, FPGA-based TDC with multiple channels for open source applications," *IEEE transactions on nuclear science*, vol. 60, pp. 2203-2208, 2013.

[98] J. Kalisz, M. Pawlowski, and R. Pelka, "Error analysis and design of the Nutt time-interval digitiser with picosecond resolution," *Journal of Physics E : Scientific Instruments*, vol. 20, p. 1330, 1987.

[99] E. Bergeron, M. Feeley, M. Daigneault, and J. P. David, "Using dynamic reconfiguration to implement high-resolution programmable delays on an FPGA," in *Circuits and Systems and TAISA Conference, 2008. NEWCAS-TAISA 2008. 2008 Joint 6th International IEEE Northeast Workshop on*, 2008, pp. 265-268.

[100] S. Berrima, Y. Blaquière, and Y. Savaria, "Sub-ps resolution programmable delays implemented in a Xilinx FPGA," presented at the IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, USA, 2017.

[101] J. Kalisz, R. Szplet, J. Pasierbinski, and A. Poniecki, "Field-programmable-gate-array-based time-to-digital converter with 200-ps resolution," *Instrumentation and Measurement, IEEE Transactions on*, vol. 46, pp. 51-55, 1997.

[102] D. M. Santos, S. F. Dow, and M. E. Levi, "A CMOS delay locked loop and sub-nanosecond time-to-digital converter chip," in *Nuclear Science Symposium and Medical Imaging Conference Record, 1995., 1995 IEEE*, 1995, pp. 289-291.

[103] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *Solid-State Circuits, IEEE Journal of*, vol. 35, pp. 240-247, 2000.

[104] C.-S. Hwang, P. Chen, and H.-W. Tsao, "A high-precision time-to-digital converter using a two-level conversion scheme," *Nuclear Science, IEEE Transactions on*, vol. 51, pp. 1349-1352, 2004.

[105] A. H. Chan and G. W. Roberts, "A jitter characterization system using a component-invariant vernier delay line," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, pp. 79-95, 2004.

[106] M.-C. Lin, G.-R. Tsai, C.-Y. Liu, and S.-S. Chu, "FPGA-based high area efficient time-to-digital IP design," in *TENCON 2006. 2006 IEEE Region 10 Conference*, 2006, pp. 1-4.

[107] P. Yen-Lin, K. Ding-Ming, C. Yung-Fa, and W. Cheng-Wen, "Application-Independent Testing of 3-D Field Programmable Gate Array Interconnect Faults," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 22, pp. 207-219, 2014.

[108] A. Panteloukas, A. Psarras, C. Nicopoulos, and G. Dimitrakopoulos, "Timing-resilient Network-on-Chip architectures," in *2015 IEEE 21st International On-Line Testing Symposium (IOLTS)*, 2015, pp. 77-82.

[109] M. R. Choudhury, V. Chandra, R. C. Aitken, and K. Mohanram, "Time-borrowing circuit designs and hardware prototyping for timing error resilience," *IEEE transactions on Computers*, vol. 63, pp. 497-509, 2014.

[110] M. Nicolaidis, "Time redundancy based soft-error tolerance to rescue nanometer technologies," in *VLSI Test Symposium, 1999. Proceedings. 17th IEEE*, 1999, pp. 86-94.

[111] T. Austin, D. Blaauw, T. Mudge, and K. Flautner, "Making typical silicon matter with razor," *Computer*, vol. 37, pp. 57-65, 2004.

[112] D. Ernst, N. S. Kim, S. Das, S. Pant, R. Rao, T. Pham, *et al.*, "Razor : A low-power pipeline based on circuit-level timing speculation," in *Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on*, 2003, pp. 7-18.

[113] S. Valadimas, A. Floros, Y. Tsiatouhas, A. Arapoyanni, and X. Kavousianos, "The time dilation technique for timing error tolerance," *IEEE Transactions on Computers*, vol. 63, pp. 1277-1286, 2014.

[114] M. Sadi, L. Winemberg, and M. Tehranipoor, "A robust digital sensor IP and sensor insertion flow for in-situ path timing slack monitoring in SoCs," in *2015 IEEE 33rd VLSI Test Symposium (VTS)*, 2015, pp. 1-6.

[115] I. Harris and R. Tessier, "Diagnosis of interconnect faults in cluster-based FPGA architectures," in *Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design*, 2000, pp. 472-476.

[116] J. Liu and S. Simmons, "BIST-diagnosis of interconnect fault locations in FPGA's," in *Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on*, 2003, pp. 207-210.

[117] X. Sun, J. Xu, B. Chan, and P. Trouborst, "Novel technique for built-in self-test of FPGA interconnects," in *Proceedings of the 2000 IEEE International Test Conference*, 2000, p. 795.

[118] S. Venkataraman and W. K. Fuchs, "A deductive technique for diagnosis of bridging faults," in *Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design*, 1997, pp. 562-567.

[119] S.-J. Wang and C.-N. Huang, "Testing and diagnosis of interconnect structures in FPGAs," in *Test Symposium, 1998. ATS'98. Proceedings. Seventh Asian*, 1998, pp. 283-287.

[120] S. McCracken and Z. Zilic, "FPGA test time reduction through a novel interconnect testing scheme," in *Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays*, 2002, pp. 136-144.

[121] J. Lach, W. H. Mangione-Smith, and M. Potkonjak, "Runtime Logic and Interconnect Fault Recovery on Diverse FPGA Architectures," in *Military and Aerospace Applications of Programmable Devices and Technologies International Conference*, 1999.

[122] E. S. S. Reddy, V. Chandrasekhar, M. Sashikánth, V. Kamakoti, and N. Vijaykrishnan, "Detecting SEU-caused routing errors in SRAM-based FPGAs," in *18th International Conference on VLSI Design held jointly with 4th International Conference on Embedded Systems Design*, 2005, pp. 736-741.

[123] H. Helstrup, J. Nystrand, S. Martens, B. Skaali, H. Tilsner, J. Wikne, *et al.*, "Irradiation tests of the ALTERA SRAM based FPGA and fault tolerant design concepts," 2003.

[124] P. S. Ostler, M. P. Caffrey, D. S. Gibelyou, P. S. Graham, K. S. Morgan, B. H. Pratt, *et al.*, "SRAM FPGA Reliability Analysis for Harsh Radiation Environments," *Nuclear Science, IEEE Transactions on*, vol. 56, pp. 3519-3526, 2009.

[125] P. Bernardi, M. S. Reorda, L. Sterpone, and M. Violante, "On the evaluation of SEU sensitiveness in SRAM-based FPGAs," in *On-Line Testing Symposium, 2004. IOLTS 2004. Proceedings. 10th IEEE International*, 2004, pp. 115-120.

[126] M. Alderighi, F. Casini, S. D'Angelo, A. Gravina, V. Liberali, M. Mancini, *et al.*, "A preliminary study about SEU effects on programmable interconnections of SRAM-based FPGAs," *Journal of electronic testing*, vol. 29, pp. 341-350, 2013.

[127] S. P. Young, K. Chaudhary, and T. J. Bauer, "Interconnect structure for a programmable logic device," ed : Google Patents, 2002.

[128] S. P. Young, T. J. Bauer, M. Chirania, and V. M. Kondapalli, "Programmable logic block with dedicated and selectable lookup table outputs coupled to general interconnect structure," ed : Google Patents, 2008.

[129] M. Chirania and V. M. Kondapalli, "Lookup table circuit optionally configurable as two or more smaller lookup tables with independent inputs," ed : Google Patents, 2006.

[130] IBIS Open Forum; ©1995-2014 [Online]. Available : www.vhdl.org/ibis/

[131] M. Ceschia, M. Violante, M. S. Reorda, A. Paccagnella, P. Bernardi, M. Rebaudengo, *et al.*, "Identification and classification of single-event upsets in the configuration memory of SRAM-based FPGAs," *IEEE Transactions on Nuclear Science*, vol. 50, pp. 2088-2094, 2003.

[132] M. Wirthlin, E. Johnson, N. Rollins, M. Caffrey, and P. Graham, "The reliability of FPGA circuit designs in the presence of radiation induced configuration upsets," in *Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on*, 2003, pp. 133-142.

[133] P. B. Minev and V. S. Kukenska, "The Virtex-5 routing and logic architecture," *Annual Journal of Electronics, Technical University of Sofia,* vol. 3, pp. 107-110, 2009.

[134] Xilinx. Timing Closure User Guide - UG612 (v14.3) [Online]. Available : http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_4/ug612.pdf

[135] Spectre Circuit simulator [Online]. Available : www.cadence.com/products/cic/spectre_circuit/pages/default.aspx

[136] Taiwan Semiconductor Manufacturing Company. Ltd. *TSMC 65nm Technology*. Available : http://www.tsmc.com/english/dedicatedFoundry/technology/65nm.htm

[137] Xilinx. Virtex-5 FPGA Configuration Users Guide, UG191 (ver. 3.11) [Online].

[138] Virtex-5 FPGA User Guide (UG190) [Online]. Available : www.xilinx.com/support/documentation/user_guides/ug190.pdf

[139] M. Węgrzyn and J. Sosnowski, "Tracing fault effects in FPGA systems," *International Journal of Electronics and Telecommunications,* vol. 60, pp. 92-97, 2014.

[140] F. Z. Tazi, C. Thibeault, Y. Savaria, S. Pichette, and Y. Audet, "On extra delays affecting I/O blocks of an SRAM-Based FPGA due to ionizing radiation," *IEEE Transactions on Nuclear Science,* vol. 61, pp. 3138-3145, 2014.

[141] Xilinx. Virtex-5 FPGA Packaging and Pinout Specification, UG195 (ver 4.8.1) [Online].

[142] R. Giordano, S. Perrella, V. Izzo, G. Milluzzo, and A. Aloisio, "Redundant-Configuration Scrubbing of SRAM-Based FPGAs," *IEEE Transactions on Nuclear Science,* vol. 64, pp. 2497-2504, 2017.

[143] A. M. Keller, T. A. Whiting, K. B. Sawyer, and M. J. Wirthlin, "Dynamic SEU Sensitivity of Designs on Two 28-nm SRAM-based FPGA Architectures," *IEEE Transactions on Nuclear Science,* 2017.

[144] A. M. Keller and M. J. Wirthlin, "Benefits of Complementary SEU Mitigation for the LEON3 Soft Processor on SRAM-Based FPGAs," *IEEE Transactions on Nuclear Science,* vol. 64, pp. 519-528, 2017.

[145] I. Villalta, U. Bidarte, J. Gomez-Cornejo, J. Lázaro, and A. Astarloa, "Estimating the SEU failure rate of designs implemented in FPGAs in presence of MCUs," *Microelectronics Reliability,* vol. 78, pp. 85-92, 2017.

[146] T. Nidhin, A. Bhattacharyya, R. Behera, T. Jayanthi, and K. Velusamy, "Understanding radiation effects in SRAM-based field programmable gate arrays for implementing instrumentation and control systems of nuclear power plants," *Nuclear Engineering and Technology,* vol. 49, pp. 1589-1599, 2017.

[147] M. Caffrey, P. Graham, E. Johnson, M. Wirthlin, and C. Carmichael, "Single-event upsets in SRAM FPGAs," in *Proc. International Conference on Military and Aerospace Programmable Logic Devices,* 2002.

[148] M. Darvishi, Y. Audet, Y. Blaquière, C. Thibeault, S. Pichette, and F. Z. Tazi, "Circuit level modeling of extra combinational delays in SRAM-based FPGAs due to transient ionizing radiation," *IEEE Transactions on Nuclear Science,* vol. 61, pp. 3535-3542, 2014.

[149] S. Huda and J. H. Anderson, "Leveraging Unused Resources for Energy Optimization of FPGA Interconnect," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, pp. 2307-2320, 2017.

[150] F. L. Kastensmidt and L. Carro, "Improving reliability of SRAM-based FPGAs by inserting redundant routing," *IEEE transactions on nuclear science*, vol. 53, pp. 2060-2068, 2006.

[151] E. Chmelar, "FPGA Interconnect Delay Fault Testing," in *ITC*, 2003, pp. 1239-1247.

[152] A. Panteloukas, A. Psarras, C. Nicopoulos, and G. Dimitrakopoulos, "Timing-resilient network-on-chip architectures," in *On-Line Testing Symposium (IOLTS), 2015 IEEE 21st International*, 2015, pp. 77-82.

[153] D. Gomez-Prado, M. Ciesielski, and R. Tessier, "FPGA latency optimization using system-level transformations and DFG restructuring," in *Proceedings of the Conference on Design, Automation and Test in Europe*, 2013, pp. 1553-1558.

[154] A. Tiwari and K. A. Tomko, "Enhanced reliability of finite-state machines in FPGA through efficient fault detection and correction," *IEEE Transactions on Reliability*, vol. 54, pp. 459-467, 2005.

[155] Y. Ichinomiya, S. Tanoue, M. Amagasaki, M. Iida, M. Kuga, and T. Sueyoshi, "Improving the robustness of a softcore processor against SEUs by using TMR and partial reconfiguration," in *Field-Programmable Custom Computing Machines (FCCM), 2010 18th IEEE Annual International Symposium on*, 2010, pp. 47-54.

[156] M. A. Bajura, Y. Boulghassoul, R. Naseer, S. DasGupta, A. F. Witulski, J. Sondeen, *et al.*, "Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs," *IEEE Transactions on Nuclear Science*, vol. 54, pp. 935-945, 2007.

[157] L. A. Tambara, "Analyzing the impact of radiation-induced failures in all programmable system-on-chip devices," 2017.

[158] X. Iturbe, D. Keymeulen, E. Ozer, P. Yiu, D. Berisford, K. Hand, *et al.*, "An integrated SoC for science data processing in next-generation space flight instruments avionics," in *Very Large Scale Integration (VLSI-SoC), 2015 IFIP/IEEE International Conference on*, 2015, pp. 134-141.

[159] X. Iturbe, D. Keymeulen, P. Yiu, D. Berisford, R. Carlson, K. Hand, *et al.*, "On the use of system-on-chip technology in next-generation instruments avionics for space exploration," in *IFIP/IEEE International Conference on Very Large Scale Integration-System on a Chip*, 2015, pp. 1-22.

[160] A. Pérez, L. Suriano, A. Otero, and E. de la Torre, "Dynamic reconfiguration under RTEMS for fault mitigation and functional adaptation in SRAM-based SoPCs for space systems," in *Adaptive Hardware and Systems (AHS), 2017 NASA/ESA Conference on*, 2017, pp. 40-47.

[161] Á. B. de Oliveira, L. A. Tambara, and F. L. Kastensmidt, "Exploring Performance Overhead Versus Soft Error Detection in Lockstep Dual-Core ARM Cortex-A9 Processor Embedded into Xilinx Zynq APSoC," in *International Symposium on Applied Reconfigurable Computing*, 2017, pp. 189-201.

[162] L. A. Tambara, P. Rech, E. Chielle, J. Tonfat, and F. L. Kastensmidt, "Analyzing the impact of radiation-induced failures in programmable SoCs," *IEEE Transactions on Nuclear Science*, vol. 63, pp. 2217-2224, 2016.

[163] I. Villata, U. Bidarte, U. Kretzschmar, A. Astarloa, and J. Lázaro, "Fast and accurate SEU-tolerance characterization method for Zynq SoCs," in *Field Programmable Logic and Applications (FPL), 2014 24th International Conference on*, 2014, pp. 1-4.

[164] L. A. Tambara, P. Rech, E. Chielle, and F. L. Kastensmidt, "Analyzing the failure impact of using hard-and soft-cores in all programmable SoC under neutron-induced upsets," in *Radiation and Its Effects on Components and Systems (RADECS), 2015 15th European Conference on*, 2015, pp. 1-5.

[165] L. A. Tambara, A. Akhmetov, D. V. Bobrovsky, and F. L. Kastensmidt, "On the Characterization of Embedded Memories of Zynq-7000 All Programmable SoC under Single Event Upsets Induced by Heavy Ions and Protons," in *Radiation and Its Effects on Components and Systems (RADECS), 2015 15th European Conference on*, 2015, pp. 1-4.

[166] D. M. Hiemstra, V. Kirischian, and J. Brelski, "Single Event Upset Characterization of the Zynq UltraScale+ MPSoC Using Proton Irradiation," in *2017 IEEE Radiation Effects Data Workshop (REDW)*, 2017, pp. 1-4.

[167] M. Caffrey, P. Graham, E. Johnson, M. W. Byu, and M. Wirthlin, "Single-event upsets in SRAM FPGAs," in *in Proc. International Conference on Military and Aerospace Programmable Logic Devices*, 2002.

[168] I. Villalta, U. Bidarte, J. Gómez-Cornejo, J. Jiménez, and J. Lázaro, "SEU emulation in industrial SoCs combining microprocessor and FPGA," *Reliability Engineering & System Safety*, vol. 170, pp. 53-63, 2018.

[169] C. Carmichael, E. Fuller, P. Blain, and M. Caffrey, "SEU mitigation techniques for Virtex FPGAs in space applications," in *Proceeding of the Military and Aerospace Programmable Logic Devices International Conference (MAPLD)*, 1999, p. C2.

[170] U. Legat, A. Biasizzo, and F. Novak, "SEU recovery mechanism for SRAM-based FPGAs," *IEEE Transactions on Nuclear Science*, vol. 59, pp. 2562-2571, 2012.

[171] T. Polzer, F. Huemer, and A. Steininger, "A Programmable Delay Line for Metastability Characterization in FPGAs," in *Microelectronics (Austrochip), 2016 Austrochip Workshop on*, 2016, pp. 51-56.

[172] P. Chen, Y.-Y. Hsiao, Y.-S. Chung, W. X. Tsai, and J.-M. Lin, "A 2.5-ps Bin Size and 6.7-ps Resolution FPGA Time-to-Digital Converter Based on Delay Wrapping and Averaging," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, pp. 114-124, 2017.

[173] C. Gu, N. Hanley, and M. O'neill, "Improved Reliability of FPGA-Based PUF Identification Generator Design," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 10, p. 20, 2017.

[174] A. P. Johnson, R. S. Chakraborty, and D. Mukhopadyay, "An Improved DCM-Based Tunable True Random Number Generator for Xilinx FPGA," *IEEE Transactions on Circuits and Systems II : Express Briefs*, vol. 64, pp. 452-456, 2017.

[175] M. Barbareschi, G. Di Natale, and L. Torres, "Ring oscillators analysis for security purposes in Spartan-6 FPGAs," *Microprocessors and Microsystems,* vol. 47, pp. 3-10, 2016.

[176] S. Gehrer, "Highly Efficient Implementation of Physical Unclonable Functions on FPGAs," Ph.D. Thesis, Informatic, Technische Universitat Munchen, Germany, 2017.

[177] S. Gehrer and G. Sigl, "Reconfigurable PUFs for FPGA-based SoCs," in *Integrated Circuits (ISIC), 2014 14th International Symposium on*, 2014, pp. 140-143.

[178] F. L. Kastensmidt, J. Tonfat, T. Both, P. Rech, G. Wirth, R. Reis, *et al.*, "Voltage scaling and aging effects on soft error rate in SRAM-based FPGAs," *Microelectronics Reliability,* vol. 54, pp. 2344-2348, 2014.

[179] F. Kodýtek, R. Lórencz, and J. Buček, "Improved ring oscillator PUF on FPGA and its properties," *Microprocessors and Microsystems,* vol. 47, pp. 55-63, 2016.

[180] C.-A. Lefebvre, L. Rubio, and J. L. Montero, "Digital thermal sensor based on ring-oscillators in Zynq SoC technology," in *Thermal Investigations of ICs and Systems (THERMINIC), 2016 22nd International Workshop on*, 2016, pp. 276-278.

[181] Xilinx. 7-Series FPGAs Configurable Logic Block User Guide (UG474) [Online]. Available : https://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf

[182] B. Taj, "Single Event Upset error detection on routing tracks of Xilinx FPGAs," Master's Thesis, Computer and Software Department, McMaster University, Canada, 2013.

[183] S. Berrima, Y. Blaquière, and Y. Savaria, "Sub-ps resolution programmable delays implemented in a Xilinx FPGA," 2017.

[184] TRIUMF. (2017, Fenruary 09). *Neutron Irradiation Facility*. Available : http://www.triumf.ca/neutron-irradiation-facility

[185] D. Reynolds, "Gaussian mixture models," *Encyclopedia of biometrics,* pp. 827-832, 2015.

[186] L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI test principles and architectures : design for testability* : Academic Press, 2006.

[187] I. Herrera-Alzu and M. Lopez-Vallejo, "Design techniques for Xilinx Virtex FPGA configuration memory scrubbers," *IEEE transactions on Nuclear Science,* vol. 60, pp. 376-385, 2013.

[188] Z.-M. Wang, L.-L. Ding, Z.-B. Yao, H.-X. Guo, H. Zhou, and M. Lv, "The reliability and availability analysis of SEU mitigation techniques in SRAM-based FPGAs," in *Radiation and Its Effects on Components and Systems (RADECS), 2009 European Conference on*, 2009, pp. 497-503.

[189] C. Bolchini and C. Sandionigi, "Fault classification for SRAM-Based FPGAs in the space environment for fault mitigation," *IEEE Embedded Systems Letters,* vol. 2, pp. 107-110, 2010.

APPENDIX A – LIST OF PUBLICATIONS AND AWARDS

Journal papers

[J1] **M. Darvishi**, Y. Audet, Y. Blaquière, C. Thibeault, S. Pichette, and F.Z. Tazi, "Circuit Level Modeling of Extra Combinational Delays in SRAM-based FPGAs Due to Transient Ionizing Radiation," *IEEE Transactions on Nuclear Science*, 61(6), pp.3535-3542, 2014.

[J2] **M. Darvishi**, Y. Audet, and Y. Blaquière, "Delay Monitor Circuit and Delay Change Measurement due to SEU in SRAM-based FPGA," *IEEE Transactions on Nuclear Science*, vol. 65, pp. 1-8, (Early Access), DOI : 10.1109/TNS.2018.2828785, April 19, 2018.

[J3] **M. Darvishi**, Y. Audet, Y. Blaquière, C. Thibeault, and S. Pichette, "On the Susceptibility of SRAM-based FPGA Routing Network to Delay Changes Induced by Ionizing Radiation," *IEEE Transactions on Nuclear Science*, March 27, 2018, Submitted.

Conference papers

[C1] **M. Darvishi**, Y. Audet, Y. Blaquière, C. Thibeault, *et al.*, "Circuit Level Modeling of Extra Combinational Delays in SRAM-Based FPGAs Due to Transient Ionizing Radiation," *IEEE Nuclear and Space Radiation Effects Conference (NSREC)*, July 14-18, 2014, Paris, France.

[C2] **M. Darvishi**, Y. Audet, and Y. Blaquière, "A Strategy Toward the Detection of Extra Combinational Delays in SRAM-Based FPGAs Due to Transient Ionizing Radiation," *25th Annual SEE Symposium and Military and Aerospace Programmable Logic Devices (MAPLD)*, May 23-26, 2016, La Jolla, CA, USA.

[C3] **M. Darvishi**, Y. Audet, and Y. Blaquière, "Delay Monitor Circuit for Sensitive Nodes in SRAM-Based FPGA," *IEEE Nuclear and Space Radiation Effects Conference (NSREC)*, July 17-21, 2017, New Orleans, LA, USA.

Poster Sessions

[P1] **M. Darvishi**, Y. Audet, and Y. Blaquière, "Monitor Circuit for Detection of Extra Combinational Delays in SRAM-Based FPGA Due To Transient Ionizing Radiation," *12th International School on the Effects of Radiation on Embedded Systems for Space Applications*, November 7-10, 2016, Montreal, QC, Canada.

[P2] **M. Darvishi**, Y. Audet, Y. Blaquière, and C. Thibeault, "Characterization of Propagation Delays in FPGAs due to Single Event Upsets (SEUs) and Mitigation Techniques," *83e congrès de l'Acfas,* May29, 2015, Université du Québec à Rimouski (UQAR), Rimouski, QC, Canada.

[P3] **M. Darvishi**, Y. Audet, and Y. Blaquière, "Characterization, Modeling and Mitigation of Propagation Delays in SRAM-Based FPGAs due to Single Event Upsets (SEUs) for Avionic Applications," *Journée de l'innovation ReSMiQ,* October, 15, 2015, Polytechnique Montréal, Montréal, QC, Canada.

[P3] **M. Darvishi**, Y. Audet, and Y. Blaquière, "Circuit de détection de délais pour les systèmes sur FPGA exposés aux rayons cosmiques dans les applications avioniques et spatiales," *Journée de l'innovation ReSMiQ,* May, 26, 2017, Polytechnique Montréal, Montréal, QC, Canada.

Awards

[A1] Travel grant for attending IEEE NSREC2014 conference, July 2014.

[A2] ReSMiQ Docrotal Scholarship Award, January 2015.

[A3] Travel grant for attending IEEE NSREC2017 conference, July 2017.