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TOWARDS BRAIN AREA SENSOR WIRELESS NETWORK

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DEDICATION

To my parents

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RÉSUMÉ

De nouvelles approches d'interfaçage neuronal de haute performance sont requises pour les interfaces cerveau-machine (BMI) actuelles. Cela nécessite des capacités d'enregistrement / stimulation performantes en termes de vitesse, qualité et quantité, c'est à dire une bande passante à fréquence plus élevée, une résolution spatiale, un signal sur bruit et une zone plus large pour l'interface avec le cortex cérébral. Dans ce mémoire, nous parlons de l'idée générale proposant une méthode d'interfaçage neuronal qui, en comparaison avec l'électroencéphalographie (EEG), l'électrocorticographie (ECoG) et les méthodes d'interfaçage intracortical conventionnelles à une seule unité, offre de meilleures caractéristiques pour implémenter des IMC plus performants. Les avantages de la nouvelle approche sont 1) une résolution spatiale plus élevée - en dessous du-millimètre, et une qualité de signal plus élevée - en termes de rapport signal sur bruit et de contenu fréquentiel - comparé aux méthodes EEG et ECoG; 2) un caractère moins invasif que l'ECoG où l'enlèvement du crâne sous une opération d'enregistrement / stimulation est nécessaire; 3) une plus grande faisabilité de la libre circulation du patient à l'étude - par rapport aux deux méthodes EEG et ECoG où de nombreux fils sont connectés au patient en cours d'opération; 4) une utilisation à long terme puisque l'interface implantable est sans fil - par rapport aux deux méthodes EEG et ECoG qui offrent des temps limités de fonctionnement.

Nous présentons l'architecture d'un réseau sans fil de microsystèmes implantables, que nous appelons Brain Area Sensor NETwork (Brain-ASNET). Il y a deux défis principaux dans la réalisation du projet Brain-ASNET. 1) la conception et la mise en œuvre d'un émetteur-récepteur RF de faible consommation compatible avec la puce de capteurs de réseau implantable, et, 2) la conception d'un protocole de réseau de capteurs sans fil (WSN) ad-hoc économe en énergie.

Dans ce mémoire, nous présentons un protocole de réseau ad-hoc économe en énergie pour le réseau désiré, ainsi qu'un procédé pour surmonter le problème de la longueur de paquet variable causé par le processus de remplissage de bit dans le protocole HDLC standard. Le protocole ad-hoc proposé conçu pour Brain-ASNET présente une meilleure efficacité énergétique par rapport aux protocoles standards tels que ZigBee, Bluetooth et Wi-Fi ainsi que des protocoles ad-hoc de pointe. Le protocole a été conçu et testé par MATLAB et Simulink.

A partir de la conception du système Brain-ASNET, nous avons choisi la modulation On-Off Keying (OOK) sur une bande de fréquence industrielle, scientifique et médicale (ISM) de 902-

928 MHz comme la meilleure option pour nos exigences d'application. Ayant fait des recherches sur des conceptions d'architecture d'émetteur-récepteur RF ULP de pointe, nous sommes venus avec une nouvelle idée pour la conception de l'architecture de transmetteur RF ULP OOK. L'architecture proposée utilise un oscillateur à anneau multi-phase à verrouillage par injection multi-phase OOK qui, comparé aux émetteurs RF ULP de pointe, fournit un débit de données élevé (plage de 10 Mbits / s) avec un rendement énergétique élevé, tout en consommant une petite aire de silicium.

Pour mettre en œuvre l'idée de Brain-ASNET, l'architecture et la conception entièrement personnalisée d'un système sur puce (SoP) à très faible consommation d'énergie (ULP) sont également présentées. Le frontal analogique (AFE) du SoC utilise un ADP (Analogique-Numérique) ULP à 8 bits conçu et mis en place sur mesure. Le SoC est conçu pour être configurable en tant que puce de nœud de capteur ou en tant que module RF frontal dédié du coordinateur et contrôleur de réseau correspondant. Le SoC est conçu et mis en place, en utilisant les outils de conception de circuits intégrés de Cadence, en exploitant un procédé CMOS de 0.13µm d'IBM. Sa superficie sur silicium est de 1.4 par 1.4 mm^2. Les résultats de simulation post-implantation montrent une bonne efficacité énergétique du protocole de réseau ad-hoc conçu et une faible dissipation de puissance du SoC, en particulier l'émetteur RF ULP proposé. La puce entière, y compris tous les composants intégrés fonctionnels et périphériques, consomme 138µW et 412µW, à 1,2V, configurés dans un réseau synchronisé en tant que nœud de capteur et coordinateur respectivement. L'émetteur ULP OOK RF proposé a une puissance de sortie de –22 dBm qui est en dessous de la limite de puissance ISM. Il dissipe 137µW de puissance à un débit de 2,75Mbps lorsque la tension d'alimentation est de 1,2V. Compte tenu du fonctionnement programmé de chaque nœud de capteur synchronisé, la dissipation de puissance moyenne de l'émetteur du nœud de capteur est aussi faible que 28µW.

Le matériel électronique du coordonnateur et un logiciel d'interface utilisateur en langage Python ont été construits avec l'aide d'un stagiaire de premier cycle. La plate-forme a été testée avec succès avec différents signaux de test. La puce fabriquée a été mesurée et son émetteur RF ainsi que son récepteur ont été testés séparément. Cependant, étant donné que la puce fabriquée n'était pas entièrement fonctionnelle, nous n'avons pas pu la tester en tant que capteur dans un Brain-ASNET en liaison avec le coordinateur et la plate-forme de commande.

ABSTRACT

New high-performance neural interfacing approaches are demanded for today's Brain-Machine Interfaces (BMI). This requires high-performance recording/stimulation capabilities in terms of speed, quality, and quantity, i.e. higher frequency bandwidth, spatial resolution, signal-to-noise, and wider area to interface with the cerebral cortex. In this thesis, we talk about the general proposed idea of a neural interfacing method which in comparison with Electroencephalography (EEG), Electrocorticography (ECoG), and, conventional Single-Unit Intracortical neural interfacing methods offers better features to implement higher-performance BMIs. The new approach advantages are 1) higher spatial resolution – down to sub-millimeter, and higher signal quality – in terms of signal-to-noise ratio and frequency content – compared to both EEG and ECoG methods. 2) being less invasive than ECoG where skull removal under recording/stimulation surgery is required. 3) higher feasibility of freely movement of patient under study – compared to both EEG and ECoG methods where lots of wires are connected to the patient under operation. 4) long-term usage as the implantable interface is wireless – compared to both EEG and ECoG methods where it is practical for only a limited time under operation.

We present the architecture of a wireless network of implantable microsystems, which we call it Brain Area Sensor NETwork (Brain-ASNET). There are two main challenges in realization of the proposed Brain-ASNET. 1) design and implementation of power-hungry RF transceiver of the implantable network sensors' chip, and, 2) design of an energy-efficient ad-hoc Wireless Sensor Network (WSN) protocol.

In this thesis, we introduce an energy-efficient ad-hoc network protocol for the desired network, along with a method to overcome the issue of variable packet length caused by bit stuffing process in standard HDLC protocol. The proposed ad-hoc protocol designed for Brain-ASNET shows better energy-efficiency compared to standard protocols like ZigBee, Bluetooth, and Wi-Fi as well as state-of-the-art ad-hoc protocols. The protocol was designed and tested by *MATLAB* and *Simulink*.

From the Brain-ASNET system design we choose On-Off Keying (OOK) modulation on an Industrial, Scientific and Medical (ISM) frequency band of 902–928MHz as the best option for our application requirements. Having done research on state-of-the-art ULP RF transceiver

architecture designs, we came with a new idea for ULP OOK RF transmitter architecture design. The proposed architecture employs an OOK multi-stage multi-phase injection-locked ring oscillator which compared to its state-of-the-art ULP RF transmitter designs provides high data rate (10-Mbps range) at a high power efficiency, at a small silicon area.

To implement the Brain-ASNET idea, architecture and full-custom design of an Ultra-Low Power (ULP) System-on-Chip (SoC) is also presented. The SoC's Analog Front-End (AFE) utilizes a full-custom designed and laid-out ULP 8-bit Success-Approximation Analog-to-Digital (ADC). The SoC is designed to be configurable as either a sensor node chip or the network coordinator's dedicated RF front-end and corresponding network controller. The SoC is designed and laid-out, using *Cadence IC Tools*, in an IBM 0.13µm CMOS process, with a silicon area of 1.4 by 1.4 mm^2. The post-layout simulation results show good energy efficiency of the designed ad-hoc network protocol and low power dissipation of the SoC, particularly the proposed ULP RF transmitter. The whole chip, including all functional and peripheral integrated components, consumes 138µW and 412µW, at 1.2V, configured in a synchronized network as a sensor node and the coordinator, respectively. The proposed ULP OOK RF transmitter has an output transmit power of –22dBm – below the ISM power limit, and dissipates 137µW of power at a date rate of 2.75Mbps at 1.2V supply voltage. Considering the scheduled operation of each synchronized sensor node, the average power dissipation of the sensor node's transmitter is as low as 28µW.

The coordinator's electronics hardware and a computer user interface software using *Python* language are constructed with assistance of an undergraduate intern. The platform was tested successfully with different test signals. The fabricated chip was measured and its RF transmitter and receiver were separately tested. However, because the fabricated chip was not whole functional, we could not tested it as Brain-ASNET sensors in connection with the coordinator and GUI platform.

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LIST OF SYMBOLS AND ABBREVIATIONS

Abbreviations:

2-D	two-dimensional
3-D	three-dimensional
ADC	Analog-to-Digital Convertor
AFE	Analog Front-End
ALOHA	Additive Links On-line Hawaii Area
AM	Amplitude Modulation
AP	Action Potential
ARQ	Automatic Repeat Request
ASIC	Application-Specific Integrated Circuit
BCI	Brain-Computer Interface
BER	Bit Error Rate
BMI	Brain-Machine Interface
Brain-ASNET	Brain Area Sensor NETwork
BSN	Body Sensor Network
CDMA	Code Division Multiple Access
CMOS	Complementary Metal–Oxide–Semiconductor
CNS	Central Nervous System
CRC	Cyclic Redundancy Check
CSF	Cerebrospinal Fluid
CSMA	Carrier-Sense Multiple Access
DAC	Digital-to-Analog Converter
DLL	Data-Link Layer

DLL	Delay-Locked Loop
ECC	Error-Correcting Code
ECoG	Electrocorticography
EC-PA	Edge-Combining Power Amplifier
EEG	Electroencephalography
ENOB	Effective-Number-of-Bits
ESD	Electrostatic Discharge
FCS	Frame Check Sequence
FDM	Frequency-Division Multiplexing
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FM	Frequency Modulation
FSK	Frequency Shift-Keying
FTSP	Flooding Time Synchronization Protocol
GUI	Graphic User Interface
HARQ	Hybrid Automatic Repeat-Request
HDLC	High-level Data Link Control
IBM	International Business Machines Corporation
IC	Integrated Circuit
iEEG	intracranial Electroencephalography
ILRO	Injection-Locked Ring-Oscillator
ISM	Industrial, Scientific, Medical
LC	Inductor-Capacitor
LEACH	Low-Energy Adaptive Clustering Hierarchy

LFP	Local Field Potential
LLC	Logical Link Control
LMAC	Lightweight Medium Access Control
LNA	Low-Noise Amplifier
LO	Local Oscillator
LTS	Lightweight Tree-Based Synchronization
LV	Low-Voltage
MAC	Media Access Control
MACAW	Multiple Access with Collision Avoidance for Wireless
MICS	Medical Implant Communication Service
MOSIS	Metal Oxide Semiconductor Implementation Service
MRI	Magnetic Resonance Imaging
MUX	Multiplexer
NCU	Network Control Unit
OOK	On-Off Keying
OSI	Open Systems Interconnection
PC	Personal Computer
PCB	Printed Circuit Board
PHY	Physical
PLL	Phase-Locked Loop
PM	Phase Modulation
POR	Power On Reset
QFN	Quad Flat No-leads
RBS	Reference-Broadcast Synchronization

RF	Radio Frequency
RMS	Root Mean Square
RO	Ring Oscillator
RX	Receiver
SAR	Specific Absorption Rate
SAR ADC	Successive-Approximation Register Analog-to-Digital Convertor
SN	Sensor Node
SNDR	Signal-to-Noise Ratio
SoC	System-on-Chip
SYNC	Synchronization
TDM	Time-Division Multiplexing
TDMA	Time Division Multiple Access
TDP	Time-Diffusion Synchronization
TPSN	Timing-sync Protocol for Sensor Networks
TRAMA	Traffic-Adaptive Medium Access
TRX	Transceiver
TX	Transmitter
UHF	Ultra-High Frequency
ULP	Ultra-Low Power
UWB	Ultra Wide-Band
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network
ΔΣ	Delta-Sigma

LIST OF APPENDICES

CHAPTER 1 INTRODUCTION

There are numerous researches currently being done around the world to improve the human quality of life, and particularly those with disabilities. Recording neural signals from the nervous system and body tissues and also ability to stimulate the central nervous system and nerves have made it possible to build different Brain-Machine Interfaces (BMIs) to be utilized as assistive devices for disabled and/or to study and understand living beings nervous systems.

1.1 Project Overview

Our research project aimed at building a new wireless intracortical neural recording system. As part of this work, we performed analysis, design, and implementation of implantable neural recording sensors and of a wireless coordinator that exploits a proposed low-power networking protocol. The overall project objectives were to design and implement ultra-low power application-specific System-on-Chip (SoC), validating the proposed platform based on a wireless network of SoCs comprising multiple sensors, and a coordinator. Meanwhile we came with a couple of ideas to make an energy-efficient Wireless Sensor Network (WSN). As a result, we introduce an ad-hoc network protocol, that we call a modified-HDLC, which solves some common issues with the standard HDLC protocol. The proposed ad-hoc protocol is way more energy-efficient than WSN standard protocols such as ZigBee, Bluetooth, and Wi-Fi and even other highly-cited state-of-the-art ad-hoc protocols. Finally, we talk about our proposed ultra-low power RF OOK transmitter architecture that shows significant improvements over state-of-the-art designs in terms of data rate, power efficiency, etc.

Different methods are used to record neural activities of body tissues and nervous system. Between them, Electroencephalography (EEG), Electrocorticography (ECoG), and, Intracortical Neural Recording are the most conventional methods to record neural activities as electrical signals. Each of these three methods have their own pros and cons. This thesis introduces a novel method that merge and utilized advantages of these three methods, as it will be described later in the current and next chapters. We build a wireless network of multi-channel intracortical neural recording implants that facilitates having wireless intracortical neural recording of the brain over many channels. It makes possible to have a high-spatial resolution recording interface, while it reduces any chance of infection for chronic use and it also makes patient's movement free,

compared to wired interfaces used in EEG and ECoG methods. Meanwhile explaining the novel neural interfacing approach, which we call it Brain Area Sensor NETwork (Brain-ASNET), we focus on three main subjects in this thesis, as briefly described below:

1.1.1 Energy-Efficient WSN Protocols

One of the crucial design challenges to build a robust energy-efficient data network is to choose a proper set of networking protocol layers, whether standard or application-specific. There are many standard protocol sets nowadays that can be difficult to choose between them. Surveys show the majority of application-specific wireless sensor networks, such as Body Sensor Networks (BSN) use their own-defined protocol set to minimize the energy loss where usually standard protocols such as Bluetooth and Wi-Fi are better when a general-purpose programmable BSN sensor module is designed for public market. Researchers have been introducing novel application-specific networking MAC protocols for wireless BSNs in the last few decades, both contention-based and contention-free, from time- and frequency- to code- division multiple access such as TRAMA, Y-MAC, DESYNC-TDMA, LEACH, and, LMAC [1]. Between them, TDMA protocols are the most popular ones for limited centralized networks like BSNs [2]. Since we had an application-specific network (Brain-ASNET) to implement, we researched on protocol design and proposed an energy-efficient ad-hoc network protocol, called modified HDLC, that solves common issues with HDLC standard protocol, and it leads to less implementation complexity and lower power consumption compared to flexible standard protocols as well as state-of-the-art ad-hoc protocols like a highly-cited ad-hoc WSN protocol proposed by Omeni-Toumazou [3]. This will be described in more details in the chapters 2 and 3.

1.1.2 Low-Power Intracortical Neural Recording SoC Design

The design and implementation of a wireless intracortical implant, capable of multi-channel recording from the brain cortex, is a huge multidisciplinary job that requires wide knowledge including nervous system and body tissue biological characteristics, microelectrode fabrication, body-electrode interface characterises, Analog, Mixed-mode, Digital, and, RF integrate circuit and system design and fabrication, data networking and wireless communication, antenna design, and many more. In this project we studied on different state-of-the-art architectures for intracortical-recording implants with focus on ultra-low-power low-voltage SoC design and

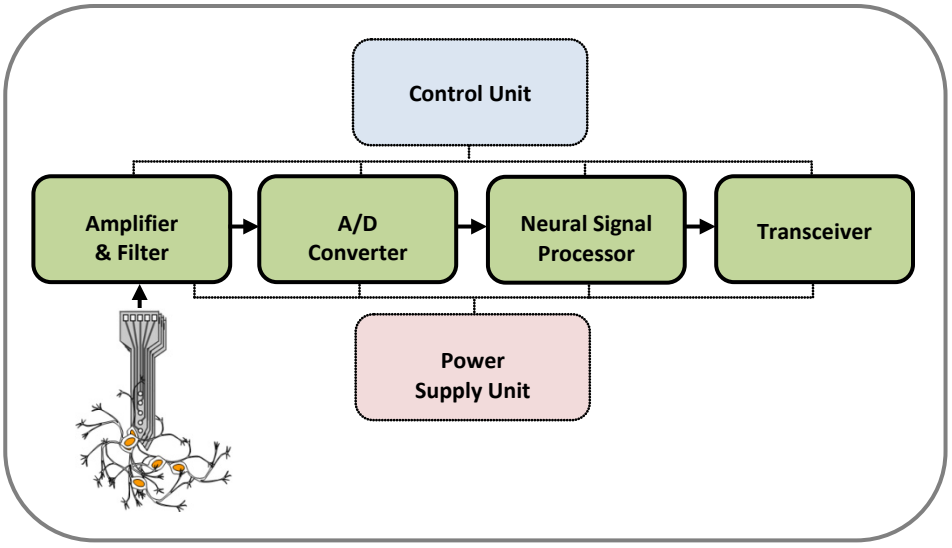

Figure 1.1: Typical architecture of wireless intracortical neural recording sensors

implementation. Figure 1.1 shows a typical wireless intracortical neural recording sensor. There have been numerous researches done (and still in progress) on power-efficient and silicon-area-efficient design of each of the main functional building blocks. Studies show Analog Front-End (AFE) architecture design can be optimized based on the number of recording channels [4]. Successive-Approximation Register (SAR) Analog-to-Digital Convertor (ADC) architecture is one of the best candidates for ultra-low-power AFE design. In this project we focused on the ADC and digital controller designs to minimize the power and silicon area for a preliminary four-channel neural recording sensor. However, as many researches indicate the main power-hungry building block of such wireless microsystems is their wireless RF transceiver, even for short-range communication that is required for limited-size WSNs like BSNs.

1.1.3 Ultra-Low Power Low-Voltage RF Transmitters

Considering that RF transceiver is the main power-consuming building block of an wireless intra-cortical neural recording implant's SoC, it is crucial to employ the most state-of-the-art energy-efficient RF transceiver architecture. In this project, different design aspects of the physical layer for the Brain-ASNET, between the implant sensors and the coordinator, were studied. Therefore, On-Off Keying (OOK) modulation on an Industrial, Scientific and Medical (ISM) frequency band of 902-928MHz was chosen as the best option for our application requirements. We came with a new idea to design a highly energy-efficient OOK RF transmitter for a Mbps-range data

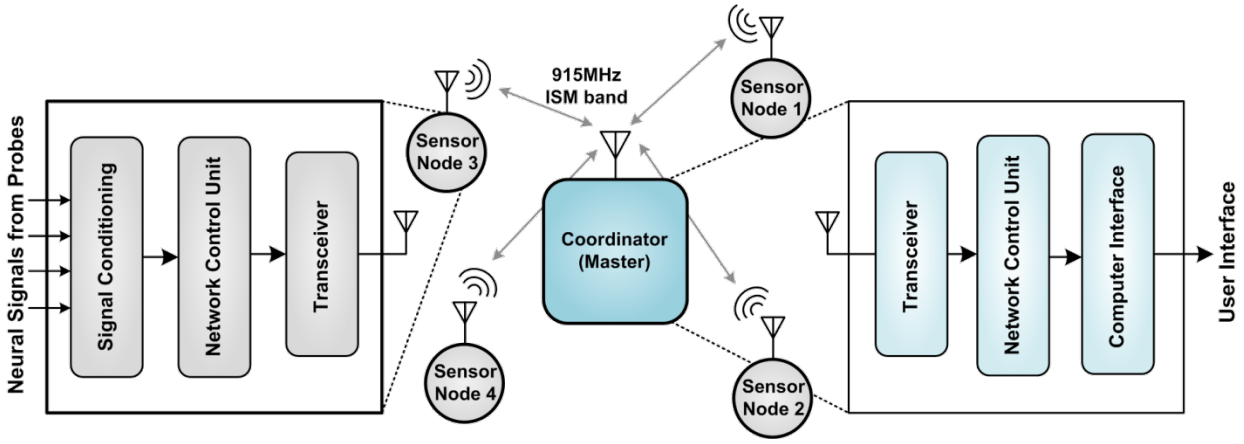

Figure 1.2: The simplified Brain-ASNET, sensor node, and coordinator architectures

rate compared to the state-of-the-art. This architecture employs an OOK multi-stage multi-phase injection-locked ring oscillator which compared to its FSK counterpart is capable of having few tens of times higher data rate (around 20 Mbps). We talk about this proposed architecture, and its chip circuit and layout designs for our application, in the chapter 3.

1.1.4 Project Organization

A successful architecture-, system- and circuit- level design and implementation of the Brain-ASNET requires adoption of the best design options and post analyses to build a robust implementation. There are many tasks to design and implement whole Brain-ASNET system so that it is functional and ready for operation and experiment. As it will be described in details later in chapter 3, for this Master's project, we consider a wireless network consisting of the coordinator and four intracortical neural recording sensors, each sensor with four neural recording input channels. Figure 1.2 shows the simplified network architecture of this Brain-ASNET, including the master coordinator and four slave sensor node simplified architectures. Because of the multidisciplinary nature of design and implementation of Brain-ASNET, many design tasks are required to be done, including the main ones listed below:

Task 1: Network architecture and topology

Task 2: Network DLL, MAC, and, PHY protocol layers

Task 3: Sensor's architecture, system and circuit

3.1: Microelectrode arrays

3.2: Multi-channel analog front-end (including neural amplifiers, ADCs, and, MUXs)

3.3: Digital internal and network protocol controllers (control unit)

3.4: RF transceiver

3.5: Miniature antenna

Task 4: Coordinator and Computer User Interface

In this thesis we performed most of the tasks listed above, with detailed discussion on tasks 2 and 3.4 where we came with new ideas to design and implement the best energy-efficient ad-hoc network protocol and ULP RF transmitter for our specific application, an initial version of a centralized Brain-ASNET.

1.2 Motivation

BMIs demand for high-performance recording/stimulation capabilities in terms of speed, quality, and quantity, i.e. higher frequency bandwidth, spatial resolution, signal-to-noise ratio, and wider area to interface with the cerebral cortex. In this thesis, we talk about the general idea of a novel neural interfacing method which in comparison with EEG, ECoG and conventional single-unit neural interfacing methods offers better capabilities to implement higher-performance BMIs. As the two main challenges in realization of the Brain-ASNET are design and implementation of the power-hungry RF transceiver and WSN protocol, we discuss about our ideas on design of an ULP RF OOK transmitter and an energy-efficient ad-hoc network protocol.

1.3 Basic Principles of Neural Recording Methods

Nowadays, different sciences and engineering techniques are employed in new multi-disciplinary research fields such as biomedical engineering. Neural engineering has introduced Brain Machine Interfaces (BMI) as promising devices for assisting patients with cognitive or sensory-motor disabilities and/or neurological injuries. BMIs were initially introduced to the scientific literature in 1970s by researchers from University of California, Los Angeles (UCLA) [5]. They can be used to control electromechanical devices by processing neural signals recorded from the brain, or to stimulate special parts of the brain like vision and cochlear cortex by signals recorded from electronic devices which function similar to real sensory organs.

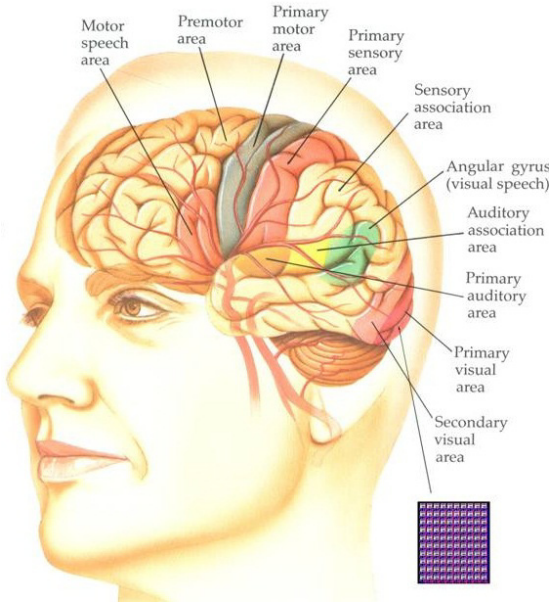

Figure 1.3: The sensory and motor regions discovered on the human cerebral cortex [8]

Because of the electro-chemical nature of neurons and neural systems, electrophysiological methods are the most conventional neural interfacing approaches for recording from and/or stimulation of the brain. For the first time, large-scale electrical neural recording from the brain based on Electroencephalography (EEG) was performed in 1924 [6]. While recorded EEG signals were not informative enough to study severe epilepsy, an invasive method called Electrocorticography (ECoG) was studied by neurosurgeons at the Montreal Neurological Institute in 1950s [7]. Later, Single-Unit Neural Interfacing was employed by researchers to study neural functions and structure of the brain at higher spatial and temporal resolutions. Current researches and available technologies to implement high-performance BMIs are still in their preliminary states.

Neuroscientists believe in the future they would be able to obtain a comprehensive knowledge about the whole structure and functions of the most complicated neural system, the human brain. Figure 1.3 shows the sensory and motor regions discovered on the human cerebral cortex. In fact, the brain is a complicated tissue made of neural cells. Electrochemical signals of the brain activities can be recorded and interpreted to recognize how its complex cellular network works. The specialized cells of the nerves system are called neurons, also known as nerve cells. They basically process and transmit information through chemical and electrical signals from one end to the other end of neuron. The electrochemical transmission across a neuron can described as

follows: 1) There are ion pumps combined with ion channels embedded in the neuron membrane. 2) Intracellular-to-extracellular concentration differences of ions (such as sodium, potassium, chloride, and calcium) can alter the function of voltage-dependent ion channels. 3) If this potential difference changes more than a specific amount, an electrochemical pulse called Action Potential (AP) is generated that causes the same scenario in adjacent ion channels and pump, and like a domino goes along the cell's axon. 4) In the end of neuron, the AP activates synaptic connections with other cells when it arrives [8].

Since research on understanding of functions and structure of the brain and neural system has been begun, different methods to analyze the brain activities have been introduced. These include Electroencephalography (EEG), Singe-Unit Recording & Stimulation, Electrocorticography (ECoG), Magnetic Resonance Imaging (MRI), functional Magnetic Resonance Imaging (fMRI), Computed Tomography (CT), Positron Emission Tomography (PET), Magnetoencephalography (MEG), Nuclear Magnetic Resonance Spectroscopy (NMRS), Single-Photon Emission Computed Tomography (SPECT), Near-InfraRed Spectroscopy (NIRS), and, functional Near-InfraRed Spectroscopy (fNIRS).

These methods can generally be categorized in two: electrophysiological versus neuroimaging techniques. Each of these methods has its own potential benefits. Since the nature of information transmitted between neurons is based on electrochemical signaling, it is more convenient to record neural signal and/or simulate neurons by electrophysiological interfaces. Here we talk about three most conventional electrophysiological neural interfacing methods, i.e. EEG, ECoG, and Single-Unit Neural Interfacing.

- *Electroencephalography*: By placing surface electrodes along the scalp, spontaneous electrical activities of the brain are monitored (Figure 1.4). EEG is usually used for diagnostic applications, generally focusing on spectral content of neural oscillations, also known as brain waves. In the simplest way abnormalities in EEG readings can be diagnosed as epilepsy. However, to diagnose sleep disorders, coma, encephalopathy, and brain death, special diagnostic algorithms and spectral analyses are needed to interpret the results [9].

  Some of the main issues of using EEG to diagnose brain activities include: 1) Low spatial resolution. For example, fMRI can directly display areas of the brain that are active, while EEG requires intense interpretation just to hypothesize what areas are activated by a

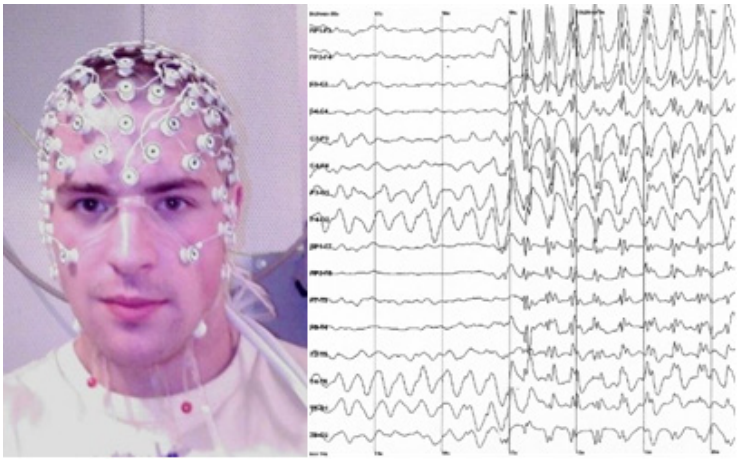

Figure 1.4: A high-density EEG recording with epileptic spikes and wave discharges

particular response [10]. 2) Poor signal-to-noise ratio. EEG measures Local Field Potentials (LFPs) which are results of neural activities of numerous neurons that occur in the cortex, layers below the scalp (Figure 1.5). This requires sophisticated data analysis and relatively large numbers of subjects to extract useful information from EEG. Nevertheless, because EEG is a non-invasive non-expensive electrophysiological monitoring method, it is still preferred over some invasive methods and different researches are being done to obtain better results from EEG.

- *Electrocorticography*: ECoG, also known as intracranial electroencephalography (iEEG), is a type of electrophysiological interfacing with the cerebral cortex using subdural/epicortical surface electrodes placed directly on the exposed surface of the brain (Figure 1.6).

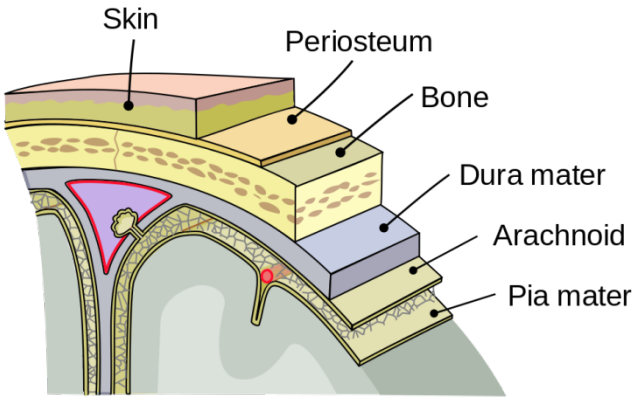

Figure 1.5: The Meninges of the central nerves system [8]

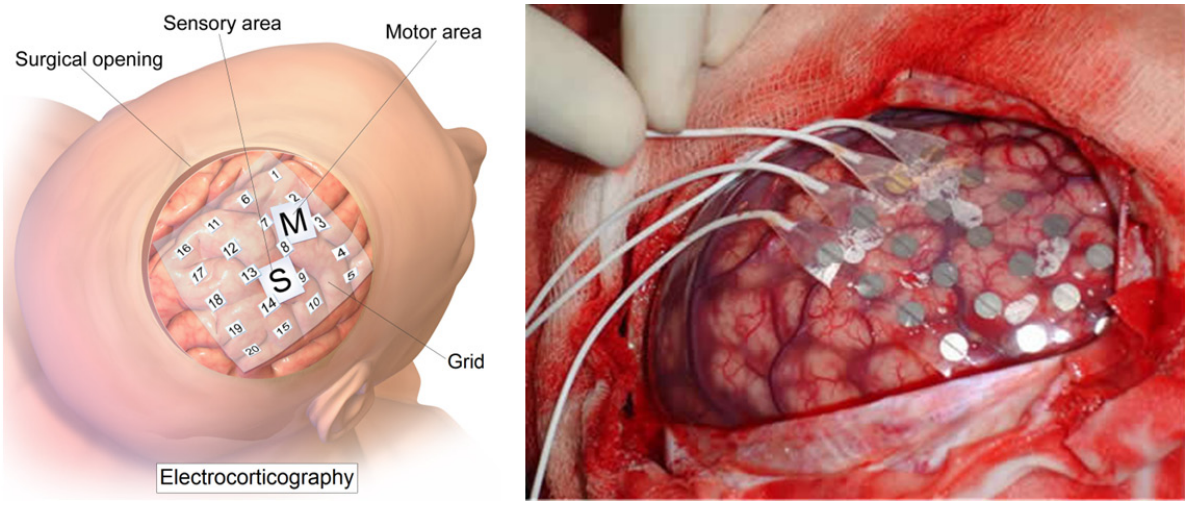

Figure 1.6: ECoG: surface subdural electrodes cover an exposed area of cerebral cortex [14]

Considering the low conductivity of the skull bone (Figure 1.5), LFPs recorded by ECoG have higher quality than that of EEG. A typical adult human EEG signal is about 10μV to 100μV in amplitude when measured from the scalp, and is about 10–20mV when measured by subdural electrodes [11]. ECoG offers a temporal resolution of approximately 5ms and a spatial resolution of 1cm [12]. These LFPs, also known as synchronized postsynaptic potentials, primarily from cortical pyramidal cells, must be conducted through several layers of the cerebral cortex, cerebrospinal fluid (CSF), pia mater, and arachnoid mater before reaching subdural electrodes placed just below the dura mater.

This method requires an surgery to remove the skull that makes it a risky and extremely-invasive procedure, and not popular except for especial cases, like back in 1950s when neurosurgeons used this approach to study severe epilepsy. Recently, researches have introduced an alternative approach instead of invasive ECoG, where similar information can be obtained by integrating EEG and MRI methods [13]. Nevertheless, ECoG has its own benefits and one can follow recent advances on researches relevant to ECoG at International Workshop on Advances in Electrocorticography [14].

- *Single-Unit Neural Interfacing*: This method is to interface with single neurons using a microelectrode system. In the simplest way, the tip of a microelectrode is inserted into a single neuron membrane or is placed adjacent to a single neuron or a population of neurons, so that it can record action potentials, intracellularly or extracellularly, respectively. The microelectrodes need to be fine-tipped, and high-impedance, that are mainly glass micro-

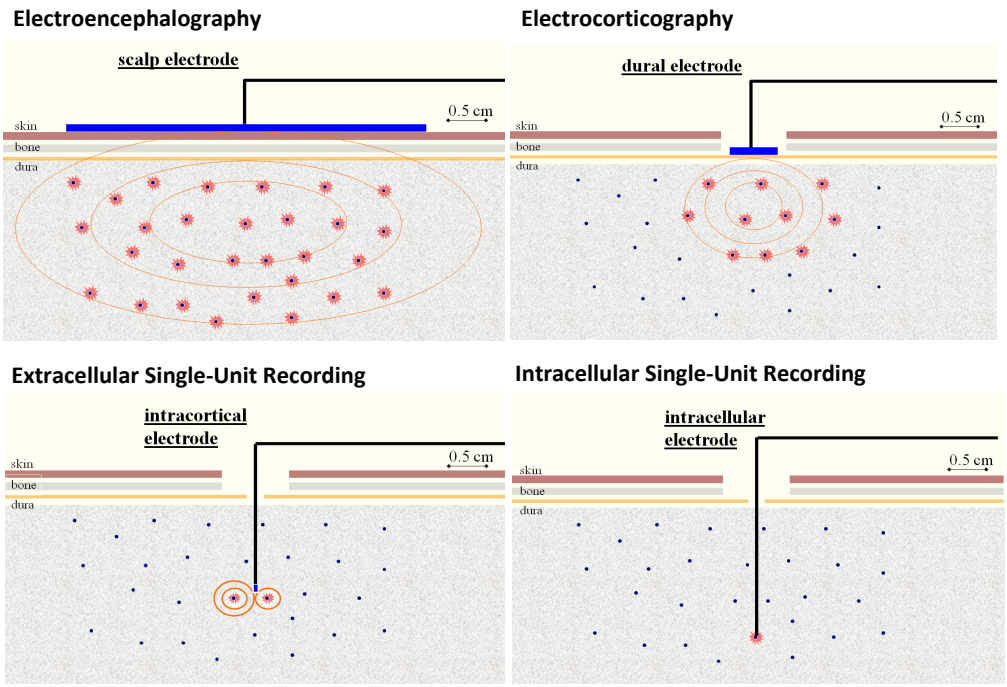

Figure 1.7: Electrophysiological methods to electrically interface with the brain [8]

pipettes or metal microelectrodes [15]. This neural interfacing method is popular in cognitive science studies, where it permits the analysis of human cognition and cortical mapping. It has allowed researchers to discover the role of different parts of the brain in function and behavior. Single-unit neural interfacing is considered in two sub-categories of intracellular and extracellular. Figure 1.7 and Table 1.1 compare these three electrophysiological neural interfacing methods.

Table 1.1: A comparison of converntional electrophysiological methods

Electrophysiological Method	Spatial Resolution	Recorded Signal	Range of Recording	Electrode Type	Electrode Position
EEG	Hundred Thousands of Neurons	Attenuated Compose of LFPs	5 – 20mm	Surface Scalp Electrode	Over Scalp
ECoG	Thousands of Neurons	Compose of LFPs	5 – 10mm	Surface Dural Electrode	Subdural
Extracellular Single-Unit Recording	Tens of Neurons	LFPs & Action Potentials	0.5 – 3mm	Deep Electrode	Extracellular (Under Pia)
Intracellular Single-Unit Recording	One Neuron	Action Potentials	0.05 – 0.35mm	Deep Electrode	Intracellular

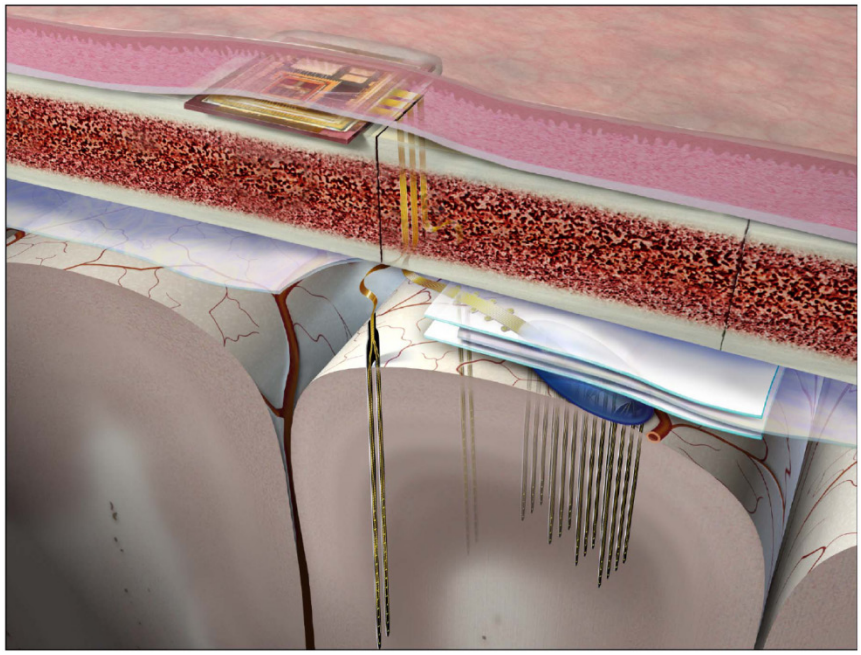

Figure 1.8: A neural microsystem consisting of 2-D and 3-D microelectrode arrays [16]

Since few decades ago, active researches have been started on design and implementation of single-unit neural interfacing systems, and especially microsystems, using 2-D and 3-D microelectrode arrays (Figure 1.8) [16]. This method has been used for BMI and neuro-prosthetic applications like cochlear and retinal implants. Figure 1.9 shows an illustration of a BMI (or more precisely a BCI) by a wireless single-unit neural interfacing implantable microsystem interfacing with a small area of the brain [17].

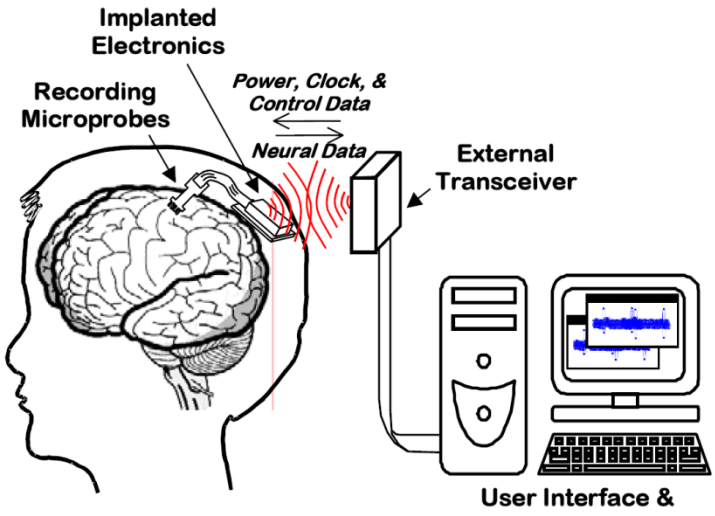

Figure 1.9: A illustration of BCI using wireless single-unit neural recording implants [17]

1.4 Research Objectives and Challenges

Alongside proposing the general idea of Brain-ASNET as a novel neural interfacing approach compared to conventional neural interfacing methods, we determine a few research objectives for this Master's thesis; however, more researches should be done to accomplish the design and implementation of a high-performance Brain-ASNET. The thesis' goals would be:

- Determination of the best network architecture and logical topology, etc. for a limited-sized preliminary version of Brain-ASNET consists of up to seven multi-channel intracortical neural recording-only sensors to record neural signals from different parts of a brain cortex.
- Design of an energy-efficient ad-hoc network protocol for our application-specific network's LLC and MAC protocol layers. The proposed modified-HDLC network protocol is introduced and compared to standard HDLC protocol and state-of-the-art.
- Determination of the best design specifications for the PHY layer of the network, that are based on frequency modulation scheme, data rate, available frequency bands, and practical antenna size for implants, etc.
- An ultra-low power, low-voltage CMOS circuit and system design and fabrication of a SoC that can be configured as either Brain-ASNET sensor's chip (with AFE, controller and RF front end as the functional blocks) or the coordinator's chip (with RF front end, and, a corresponding protocol controller as the functional blocks).
- CMOS design and fabrication of a proposed ULP OOK RF transmitter capable with data rate up to 20Mbps, discussed with detailed analysis, chip circuit and layout design, and simulation and measurement results.
- Construction of the coordinator's electronics hardware and a computer user interface software using Python language is performed with assistance of an undergraduate intern. The platform was tested successfully with test signals.
- The ultimate goal is to have an entire functional Brain-ASNET. That means programming the coordinator and sensors with specified configuration setting from the computer interface, and displaying the recorded signals, on the sensors of all the recording channels,

on the user interface. However, this was not achieved because of time limit and the fact that the fabricated chip not whole functional.

The main challenges in realization of a practical Brain-ASNET will be study and analysis of the most energy-efficient standard protocol or designing of an energy-efficient ad-hoc network protocol to reduce any excessive protocol headers, etc. In addition, the main challenge in design and implementation of neural recording sensor's SoC, with a limited energy source, is the fact that its RF transceiver is the most power-hungry building block (that can consumes more than %90 of power budget for meter-range wireless communication). Utilizing the most power-efficient state-of-the-art option for RF transceiver or designing a new architecture and/or circuit to overcome this challenge is very crucial for our application.

1.5 Contributions

Three contributions can be considered as the main outcomes of this Master's research project, as listed below:

- Brain-ASNET is introduced as a novel approach compared to conventional neural recording methods like EEG, ECoG, and Single-Unit Intracortical Recording. This method allows high-performance recording/stimulation capabilities in terms of speed, quality, and quantity, i.e. higher frequency bandwidth, spatial resolution, signal-to-noise, and wider area to interface with the cerebral cortex which high-performance BMIs demand.
- As it is discussed in details in section 3.2, a new energy-efficient ad-hoc network protocol, called modified HDLC, is proposed in this thesis. This protocol solves some common issues with standard HDLC protocols like variable bit- stuffing/destuffing, and stop flag. The proposed ad-hoc protocol designed for Brain-ASNET shows better energy-efficiency compared to standards like ZigBee, Bluetooth, and Wi-Fi as well as state-of-the-art energy-efficient ad-hoc WSN protocols.
- Lastly we consider our proposed OOK RF transmitter architecture and chip design as a defendable contribution in the research field of ultra-low power, low voltage RF transmitter design, as the results show significant improvement of overall figure-of-merit at high data rates up to 20 Mbps. This will be discussed in the section 3.3.

1.6 Thesis Outline

The subject of this research work shall be “the introduction of Brain Area Sensor Networks, with a proposed energy-efficient ad-hoc protocol, and, a novel ultra-low power OOK RF transmitter architecture and design. The thesis is organized in four chapters and a final conclusion. Following the first chapter introducing our project, goals and challenges, the general proposed idea (the Brain-ASNET) is introduced in details along with some relevant literature review in chapter two. We discuss about architecture-, system- and circuit- level design and implementation aspects in chapter three. Chapter four will present the achieved schematic simulations, post-layout simulations, and, measurement results, followed by a conclusion and potential future works in the last chapter.

CHAPTER 2 PROPOSED GENERAL IDEA, AND, LITERATURE REVIEW

In this chapter we introduce the proposed general idea of Brain-ASNET along with some potential development suggestions and applications. Finally we review some literature about the general idea, wireless sensor networks, their applications, and protocol analysis and design, along with some state-of-the-art WSN protocols and their features.

2.1 Proposed General Idea: Brain Area Sensor Network

Nowadays, researchers demand for informative signals from the brain activities to build high-performance BMIs. EEG as the most conventional electrophysiological monitoring method is fine for BMIs with limited applications [18]. Because recorded EEG signals do not provide enough information about specific parts of the brain, but attenuated Local Potential Fields (LFP) from the whole cortex at a low spatial resolution.

The second most conventional electrophysiological interfacing method, ECoG, makes it possible to record LFPs from the cerebral cortex with higher signal-to-noise ratios and better spatial resolutions as low as one centimetre. This interfacing method also allows to stimulate the brain by surface subdural electrodes. However, this requires a risky, highly-invasive procedure to remove a considerably large area of the skull, and as well patient needs to be under surgery and to be wired to user interface.

Conventional single-unit neural interfacing allows recording from and/or simulation of a population of neurons of a small area of the brain. Temporal and spatial resolutions are better than ECoG results, as accurate as few hundreds of microsecond and few tenths of a millimetre, respectively. In fact, instead of only LFPs, we can also record Action Potentials (AP), which provide more information content about the behaviour of neurons. This interfacing method requires invasively to penetrate a microelectrode array into the brain cortex. With recent advances in wireless intracortical neural interfacing implantable microsystems [17] [18] [19] [20], the recording/stimulation microelectrode array is implanted in the cortex and the electronic microsystem is implanted under the scalp and wirelessly communicates with an external electronic setup. Therefore, the patient has freedom of movement (not under a operation like EEG and ECoG) and infections less likely occur as there are no wires. However, there are still

challenges to implement high-performance wireless BMIs and neuro-prosthetics using a single wireless intracortical implant:

1. As the microelectrode is penetrated into the brain cortex, there are issues for long-term recording/stimulation of neurons. A hypothesis says the chronic inflammatory response around the microelectrode causes neuro-degeneration that decreases the number of neurons it is able to record from [21].
2. The area covered by intracortical microelectrode array is around few millimetres by few millimetres that is very small to deal with the brain whether for recording or stimulation. In neuro-prosthetic applications like retinal implants, researchers have implemented a microelectrode array ($37.6mm^2$) with 1024 stimulation channels [22]. Also, to build an over-100-channel wireless intracortical implant, some researchers [23] [24] have suggested implementing a few microelectrode arrays on a wider area on the cortex all connected to a microsystem implant with long wires; but no physical implementations for in-vivo experiments with this idea have been published in the literature.
3. Even with current technology for wireless intracortical implants that establish a peer-to-peer wireless communication link with an external electronic setup, because of restricted energy sources for this type of implants, it is almost impossible to increase the number of recording channels more than a few tens if the user (neuroscientist or physician) needs to have real waveform of neural signals sensed on microelectrode arrays. The wireless communication between the implant and the external setup can be in either analog or digital schemes; however, most researches prove that digital wireless communication for intracortical implants is superior to its analog counterpart – described in [25]. Neural spikes from the brain cortex have a meaningful frequency spectrum up to a few kHz; thus, to record neural signal containing LFPs and APs, each input channel needs to be sampled at a minimum rate of 10kHz and be digitized with a reasonable resolution – typically around 8 bits. Now, imagine we have only 100 channels to record, digitize, and wirelessly transmit to an electronic external setup; the output data rate would be around 8Mbp without considering protocol overhead for framing the bitstream, etc. This means the implant needs at least 8MHz of frequency bandwidth for wireless communication that is not available at ISM frequency bands lower than 902-928MHz. UWB RF transceivers at

higher ISM frequency bands are popular, but it should be considered that Specific Absorption Rate (SAR) increases by the square of RF frequency. Also, care should be taken not to have a high power consuming implant as it can heat the brain and damage it. Maximum of 1°C temperature increase is acceptable [26]. For these reasons many researchers have tried to reduce the recording output bitstream data rate by different data compression and spike detection methods. We later discuss about it.

Considering the main challenges mentioned above, implementing high-performance BMIs using wireless intracortical implants is not feasible with current technologies, unless we can dramatically decrease power dissipation and output data rate of implants, or, introduce a new way to use wireless intracortical implants on wider area of the cortex and pushing the complexity from the implants to the external setup.

In this thesis, we introduce the general idea of networking wireless intracortical implants for recording from and/or stimulation of the brain. Figure 2.1 show the general idea of networking wireless intracortical implants, called sensor nodes, with the wireless external setup, called the coordinator. We call this network "Brain-ASNET", which stands for "Brain Area Sensor NETwork". In long-term development perspective, one can consider the possibility of connecting this network to the universal network, the Internet, to remotely control an object through a high-performance wireless Brain-Computer Interface (BCI).

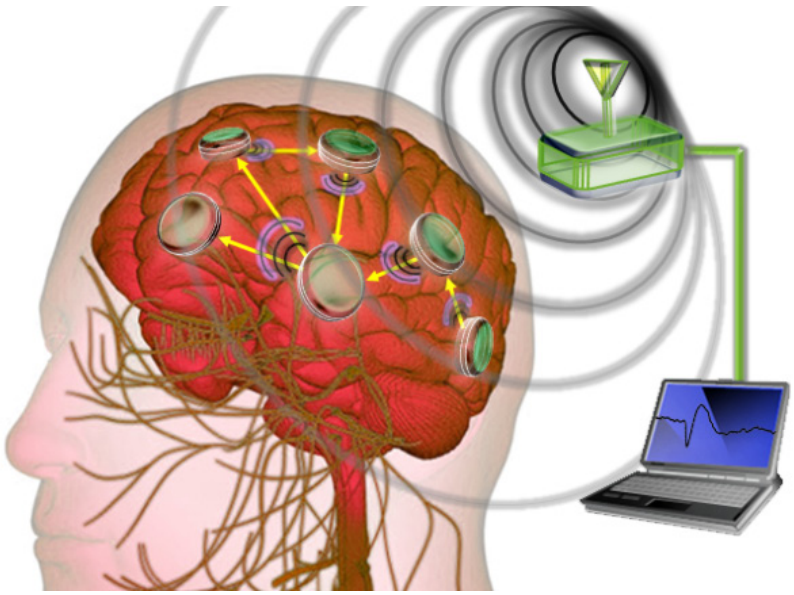

Figure 2.1: An illustration of the proposed Brain-ASNET

2.1.1 Potential Developments and Applications

Here we briefly describe two research categories of neuroscience that can be considered as main applications for the proposed Brain-ASNET:

a) Cognitive science: While non-invasive EEG neural interfacing method does not provide adequate information to study the CNS; instead, invasive ones like ECoG and intracortical neural interfacing, and Brain-ASNET methods provide higher spatial and temporal resolution to allow for information assessing the relationship between brain structure, function, and behaviour. By looking at brain activity at the neuron level, researchers can link brain activity to behaviour, and create neuronal maps describing flow of information through the brain. Evoked potentials provide a method to couple behaviour to brain function. By different stimulating responses, one can visualize what portion of the brain is activated. Therefore, this kind of methods can be used to explore cognitive functions such as perception, memory, language, emotions, and motor control [27].

b) BMIs and Neuro-prosthetics: BMIs and neuro-prosthetics based on wireless intracortical implants have the potential to restore function in patients with paralysis or neurological disease, and many more artificial electrophysiological treatments, such as cochlear and retinal implants. Although there have been issues with long-term use of intracortical implants to build BMIs at the early stages initiated by the BrainGate project [28], some researchers have published data showing good results for long-term intracortical BMIs, e.g. computer control in a patient with Tetraplegia [29].

Considering different possible applications with the proposed neural interfacing approach, various available topologies for data networks, and limited space in the proximity of the brain (or the head and body), we can define a few different network configurations as follows.

1. *Recording-Only Centralized Brain-ASNET*: As a matter of fact, most neural interfaces to monitor the brain activities have a recording-only capability. Because of the limited area that wireless intracortical implants cover, and, no topological change is expected to the network, a star network topology is chosen for the first development phase of Brain-ASNET (Figure 2.2). This will be discussed more in next sections. In this network, all Recording-Only implantable sensor nodes wirelessly transfer their recorded digitized

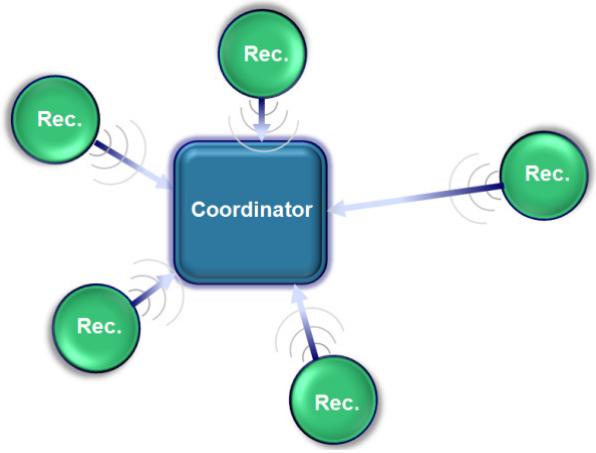

Figure 2.2: Recording-Only Centralized Brain-ASNET

neural signals to the outside of the body to be collected by the coordinator. Still the coordinator can send configuration data packages to each sensor node individually.

2. *Recording-and-Simulation Centralized Brain-ASNET*: In some applications, however, it is necessary to have both recording and stimulation capabilities, simultaneously. For instance, it might be required to stimulate a specific region of the CNS, and immediately record the brain neuronal activities – evoked potentials. In this development design (Figure 2.3), the proposed network is composed of recording and/or stimulation implantable sensor nodes associated with a coordinator outside of the brain.

3. *Recording-and-Simulation Distributed Brain-ASNET*: One of the challenges in implementation of WSNs is the reliability issue. That means, networks should be fault tolerant enough against possible failures in the network structure. In the both centralized

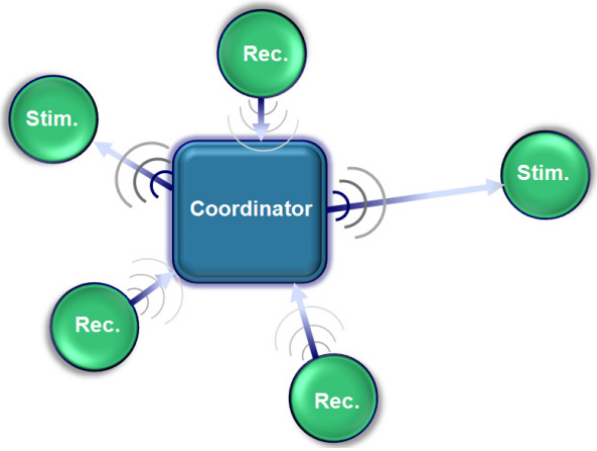

Figure 2.3: Recording-and-Simulation Centralized Brain-ASNET

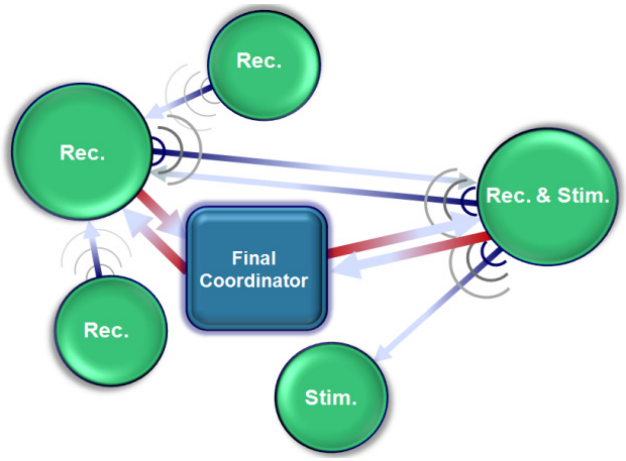

Figure 2.4: Recording-and-Simulation Distributed Brain-ASNET

network structures above, since there is a single gateway between sensor/actuator nodes and the coordinator, any failure in operation of the coordinator may lead to a failure in operation of the whole network, which could be absolutely undesirable in some applications. In contrast, a mesh (or hybrid) network topology essentially offers higher reliability degree for the whole network, compared to the star network topology. As well, we can consider multi-hopping feature for the third network structure, where it most-likely results in higher overall energy efficiency. We can set up a wireless multi-hop node on the skull with more a sensitive/powerful transceiver; then, this node performs like a wireless data relay between the sensor/actuator nodes (implanted in the brain cortex) and the final coordinator (outside the body, connected to the computer). Therefore, the implantable sensor/actuator nodes can be more relaxed in terms of transceiver sensitivity/output power to achieve a wireless transmission in the order of a few meters between implantable nodes, and the coordinator. Figure 2.4 illustrates general idea of the third network structure for the proposed Brain-ASNET.

2.2 Wireless Sensor Networks and their Protocols

Here we discuss about some of the main system-level specifications of a WSN that are required to be carefully chosen and designed when an application specific WSN like Brain-ASNET, with an ad-hoc protocol of its own is desired.

Network Architecture: Network topology is the arrangement of the various elements of a data network, and may be depicted physically or logically. Physical topology refers to the layout of transmission links, the locations of nodes, and the interconnections between the nodes and the links. In contrast, the logical topology is the way that the signals act on the network media, or the way that data passes through the network from one device to the next without regard to the physical interconnection of the devices. Logical topologies are often closely associated with Media Access Control (MAC) methods and protocols. Figure 2.5 shows different possible network topologies; between them the star and the mesh topologies are more conventional in wireless sensor networks. Table 2.1 compares pros and cons of these two network topologies. However, a few literature surveys on wireless body sensor networks indicate that the best network topology for wireless sensor networks with a limited covering space, and minimum necessity for network scalability, like BSNs, is the star topology [2, 30, 31].

PHY Layer: The most basic layer in Open Systems Interconnection (OSI) model of 7-layer protocol stacks is PHY (physical) layer which concerns physical transmission of data in shared medium between all data network nodes. Essential tasks are modulation and demodulation, and, coding and decoding of data received from upper protocol layer Data-Link Layer (DLL) using transceivers in both sender and receiver sides [1, 32]. The most important issue concerning this

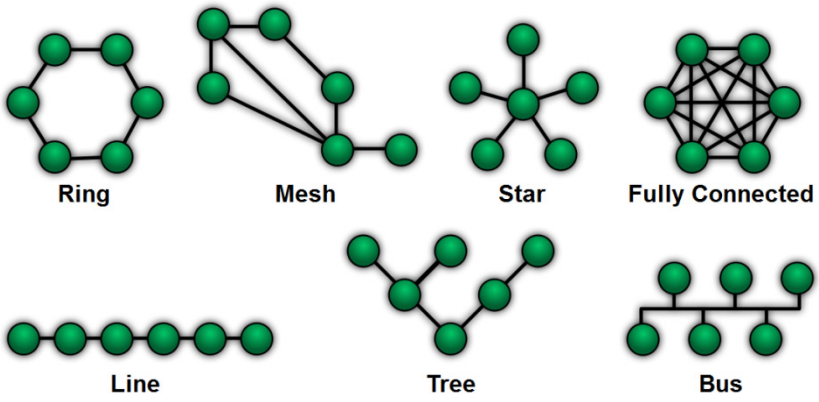

Figure 2.5: Main data network topologies [33]

Table 2.1: A comparison between the popular star and mesh network topologies [31]

Network Topology	Advantages	Disadvantages
Star	Simplicity Simple and cheap slave nodes Low power consumption of slave nodes Low latency and high bandwidth Centralized systems	Dedicated central node Limited spatial coverage Single point of failure Poor scalability, small number of nodes Asymmetric power consumption Inefficient slave-to-slave communication
Mesh	Peer-to-peer communication Very fault tolerant Scalable, many nodes possible Large spatial coverage Medium complexity	Nodes must have same basic functionality Complexity of routing High latency and low bandwidth

layer is to choose appropriate transceiver architecture with low-power consumption and the least implementation complexity, which depends on modulation, coding, correct communication channel modelling, etc.

- *Modulation* In some wireless systems, where data is processed in analog domain, an analog transceiver would essentially be preferred to send and receive analog data. Such transceivers utilize analog modulation schemes of three well-known families AM, FM, and PM. In contrast, many wireless sensor node designs have an analog front end to deal with sensors/actuators, but to utilize benefits of both flexible digital processing and wireless digital transmission, a data converter is used to change signals from analog domain to digital, and vice versa. The digital processing makes feasible powerful data compression, digital pattern recognition, etc; and the digital transmission leads to more robust and higher quality data transmission compared with its analog counterpart. Digital transmitters perform a digital modulation on base-band signals. Figure 2.6 shows different digital modulation schemes families. Analysis shows that for the same signal-to-noise ratio, coherent digital phase-modulation receivers are twice better in bit error rate performance compared with their frequency-modulation counterparts [34]. However, because of synchronization requirement for coherent digital transceivers, they are essentially more complex to be implemented.

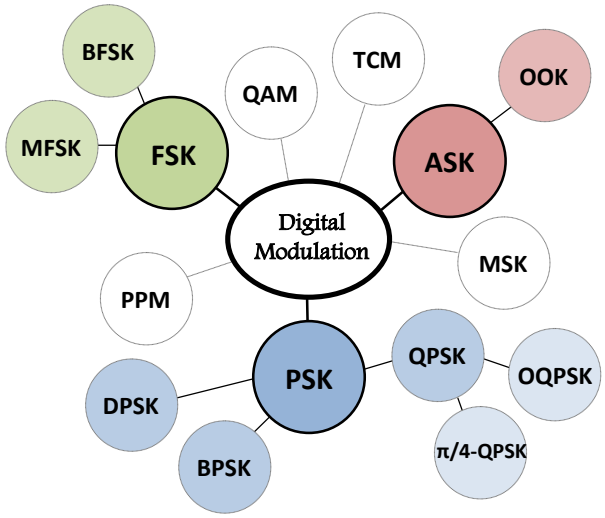

Figure 2.6: The main digital modulation schemes

- *Communication Frequency Allocation* For a practical wireless, RF-based system, the carrier frequency has to be carefully chosen. This carrier frequency determines the propagation characteristics and the available capacity. As well, the choice of a frequency band is an important factor in system design. The range of radio frequencies is subject to regulation to avoid unwanted interference between different users and systems. The most popular freely-accessible RF frequency bands for wireless sensor networks are the Industrial, Scientific, and Medical (ISM) bands (listed in Table 2.2 [2]), and the Medical Implant Communication Service (MICS) band, which is between 402 and 405 MHz, particularly for the implementation of medical implants.

Table 2.2: Industrial, Scientific, and Medical (ISM) frequency bands [2]

Frequency	Comment
13.553 – 13.567 MHz	
26.957 – 27.283 MHz	
40.66 – 40.70 MHz	
433 – 464 MHz	Europe
902 – 928 MHz	Only in the Americas
2.4 – 2.5 GHz	Used by WLAN/WPAN technologies
5.725 – 5.875 GHz	Used by WLAN technologies
24 – 24.25 GHz	

Data-Link Layer: The data-link layer provides the functional and procedural means to transfer data between network entities and might provide the means to detect and possibly correct errors that may occur in the physical layer. When devices attempt to use a medium simultaneously, frame collisions occur. Data-link protocols specify how devices detect and recover from such collisions, and may provide mechanisms to reduce or prevent them [32]. The data-link layer has two sublayers: Logical Link Control (LLC) and Media Access Control (MAC), as described in the following.

- *Logical Link Control* The LLC sublayer sits on top of the packet transmission and reception service offered by the MAC sublayer, and offers its services to the network layer and other higher layers. One of the most important tasks of the LLC sublayer is to create a reliable communication link for packet transmission between neighbouring nodes. This can be broken down into the following main aspects:
    - *Framing* User data is fragmented and formatted into packets or frames, which include the user data and protocol-related information, which includes frame synchronization headers, sender and receiver's addresses, frame check sequences. The format and size of packets can have significant impact on performance metrics like throughput and energy consumption. Essentially, a larger packet size for a given framing overhead leads to achieve a reasonable more energy-efficiency per user bit. On the other hand, larger packets are more susceptible to bit errors if no mechanisms like FEC are applied. However, for the proposed network we prefer to send the whole recording channels sampled data once a data frame is sent to destination. Therefore, no packet size optimization matters here.
    - *Error Control* With the error-control process, we can be confident that the transmitted and received data are identical. Data can be corrupted during transmission. For reliable communication, error must be detected and corrected. The efficiency and energy consumption of the different error-control mechanisms depends on the error patterns (single-bit or burst) on the link.

      Error detection can be categorized in three major types: parity check, cyclic redundancy check (CRC), and checksum check. Parity adds a single bit that indicates whether the number of “1” bits in the preceding data is even or odd.

Parity checking is not very robust, since if the number of bits changed is even, the check bit will be invalid and the error will not be detected. But, CRC is a very efficient redundancy checking technique. It is based on binary division of the data unit, the remainder of which (CRC) is added to the data unit and sent to the receiver. The Receiver divides data unit by the same divisor. If the remainder is zero then data unit is accepted and passed up the protocol stack, otherwise it is considered as having been corrupted in transit, and the packet is dropped. Finally, while Parity checking and CRC is used in the physical layer, checksum is essentially used in the upper layers. Checksum is also on the concept of redundancy.

Error correction may generally be realized in two different ways. Automatic repeat request (ARQ) is an error control technique whereby an error detection scheme is combined with requests for retransmission of erroneous data. Every block of data received is checked using the error detection code used, and if the check fails, retransmission of the data is requested – this may be done repeatedly, until the data can be verified. Forward error correction (FEC), on the other hand, in which sender encodes the data using an error-correcting code (ECC) prior to transmission. The additional information (redundancy) added by the code is used by the receiver to recover the original data. In general, the reconstructed data is what is deemed the "most likely" original data. ARQ and FEC may be combined, such that minor errors are corrected without retransmission, and major errors are corrected via a request for retransmission: this is called hybrid automatic repeat-request (HARQ).

However, to implement the first generation of the proposed network, since it requires real-time monitoring and data transfer correction for our application is not as crucial as for computer networks, we just use CRC error detection scheme, with no error correction. This will be explained more in section 3.2.

- *Media Access Control*: The wireless medium can be shared by multiple network devices; therefore a mechanism is required to control access to the medium. The main function of the MAC sublayer is to decide when a node accesses a shared medium and to resolve any

potential conflicts between competing nodes. Existing MAC protocols can be categorized by the way they control access to the medium. Most MAC protocols fall into either the categories of contention-free or contention-based protocols.

MAC protocols of the contention-free category provide a medium sharing approach that ensures that only one device accesses all resources of the wireless medium at any given time. This category can further be divided into fixed- and, dynamic- assignment classes, indicating whether the slot reservations are fixed (such as TDMA, FDMA, and CDMA) or on-demand (such as Token Bus). This approach eliminates collisions among sensor nodes, exposing a number of desirable characteristics.

Typical protocols of fixed-assignment class are TDMA, FDMA, and CDMA. The Time Division Multiple Access (TDMA) scheme [35] subdivides the time axis into fixed-length superframes, and each superframe is again subdivided into a fixed number of time slots. The time slots are assigned to nodes exclusively and hence the node can transmit in this time slot periodically in every superframe. TDMA requires tight time synchronization between nodes to avoid overlapping of signals in adjacent time slots. In Frequency Division Multiple Access (FDMA) scheme, the available frequency band is subdivided into a number of subchannels and these are assigned to nodes, which can transmit exclusively on their channel. This scheme requires frequency synchronization, relatively narrowband filters, and the ability of receiver to tune to the channel used by a transmitter. Accordingly, an FDMA transceiver tends to be more complex than a TDMA transceiver. In Code Division Multiple Access (CDMA) schemes [36], the nodes spread their signals over a much larger bandwidth than needed basic channel, using different codes to separate their transmissions. The receiver has to know the specific code used by the transmitter; all parallel transmissions using other codes appear as noise. The code management is the big challenge in CDMA scheme. Table 2.3 compares three major fixed-assignment MAC protocols.

Because of low-complexity implementation of TDMA-based MAC protocols, they have been paid more attention. In TDMA-based protocols, a fixed allocation of slots allows nodes to determine precisely when they have to activate their radio for transmission or reception of data. During all other slots, the radio (or even the entire sensor node) can be

Table 2.3: A comparison of three main fixed-assignment MAC protocols

Specifications	TDMA	FDMA	CDMA
Bandwidth Usage	Entire	Entire	Entire
Multipath Reception	Failure	Failure	Good
Protocol Overhead	Long	Low	Medium
Transceiver Complexity	Medium	High	High
Special Issue	Time Synchronization	Sharp Narrowband Filter Freq. Synchronization	Code Assignment Time Synchronization

switched into a low-power sleep mode. Therefore, typical contention-free protocols are advantageous in terms of energy efficiency. With respect to predictability, fixed slot allocations also impose upper bounds on the delay that data may experience on a node, thereby facilitating the provision of delay-bounded data delivery. While these advantages make contention-free protocols desirable choices for energy-conscious networks, they also have some disadvantages. Even though scalability of a sensor network depends on a variety of factors, the design of the MAC protocol affects how well resources are utilized in large-scale networks. Contention-free protocols with fixed slot assignments can pose significant design challenges; that means, it may be difficult to design schedules for all nodes that effectively utilize the available bandwidth when frame and slot sizes are the same for all nodes. This becomes even more pronounced when the network experiences changes in topology, density, size, or traffic characteristics, which may require the reallocation of slots or even the resizing of frames and slots. In networks with frequent changes, these disadvantages proscribe the use of protocols with fixed schedules [1].

In contrast to contention-free techniques, contention-based protocols (such as ALOHA, CSMA, MACAW) allow nodes to access the medium simultaneously, but provide mechanisms to reduce the number of collisions and to recover from such collisions. Contention-based MAC protocols do not rely on transmission schedules, but instead on other mechanisms to resolve contention when it occurs. The main advantage of contention-based techniques is their simplicity compared to most schedule-based techniques. For example, where schedule-based MAC protocols must save and maintain schedules or tables indicating the transmission order, most contention-based protocols do

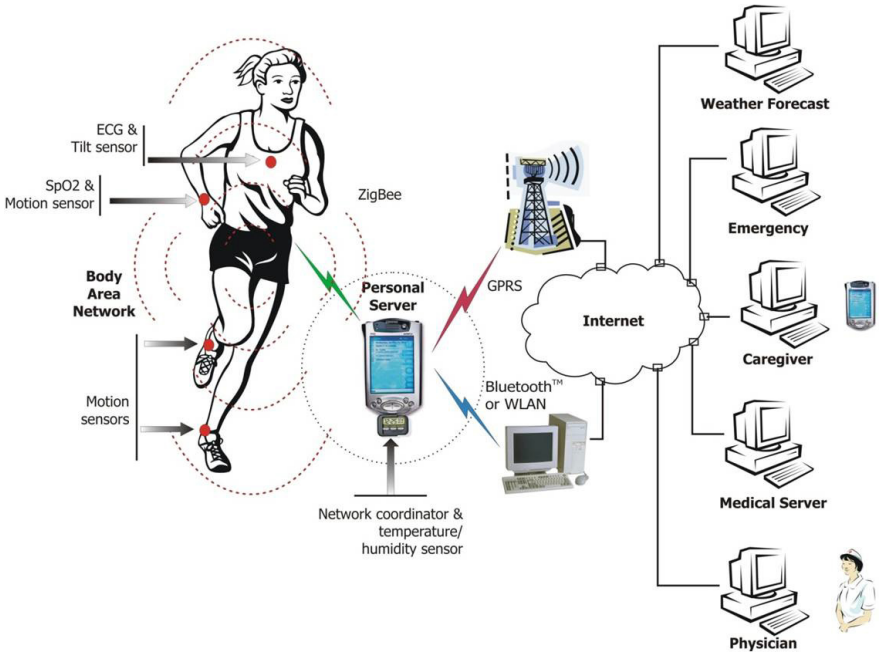

Figure 2.7: A wireless BSN, connected to a local server and the internet [2]

not require to save, maintain, or share state information. This also allows contention-based protocols to adapt quickly to changes in network topologies or traffic characteristics. However, contention-based MAC protocols typically result in higher collision rates and energy costs due to idle listening and overhearing. Contention-based techniques may also suffer from fairness issues, that is, some nodes may be able to obtain more frequent channel accesses than others [32].

One of the most researched types of WSNs with biomedical applications in past decades are Body Sensor Networks (BSN). Figure 2.7 shows general idea of a BSN [2]. While Wi-Fi and Bluetooth are the most popular WSN standard protocols, there have been numerous researches to propose more energy-efficient ad-hoc protocols for different BSNs. Surveys show that many of these ad-hoc protocols are TDMA-based. We review a few of them from the literature, such as TRAMA, Y-MAC, DESYNC-TDMA, LEACH, LMAC.

The Traffic-Adaptive Medium Access (TRAMA) protocol is a contention-free MAC protocol that aims to increase the network throughput and energy-efficiency, compared to traditional TDMA approach. TRAMA reduces the probability of collisions and increases the sleep time and energy savings compared to CSMA-based protocols [37]. Unlike standard TDMA approaches, TRAMA divides time into random-access and scheduled-access intervals. During the random-

access intervals, nodes are awake to either transmit or receive topology information – the length of random-access interval affects the overall duty cycle and achievable energy savings of a node.

Another protocol that uses TDMA-based medium access is Y-MAC. Similar to TDMA, Y-MAC divides time into frames and slots, where each frame contains a broadcast period and a unicast period. Every node must wake up at the beginning of a broadcast period and nodes contend to access the medium during this period [38]. If there are no incoming broadcast messages, each node turns off its radio awaiting its first assigned slot in the unicast period. Each slot in the unicast period is assigned to only one node for receiving data. This receiver-driven model can be more energy-efficient under light traffic conditions, because each node samples the medium only in its own receive time slots. The main drawbacks of the Y-MAC approach are that it has the same flexibility and scalability issues as TDMA (i.e., fixed slot allocations) and that it requires sensor nodes with multiple radio channels.

DESYNC-TDMA [39] is an adaptive TDMA-based protocol that does not require explicit scheduling or time synchronization. This MAC protocol focuses on two shortcomings of traditional TDMA: it does not require a global clock and it automatically adjusts to the number of participating nodes to ensure that available bandwidth is always fully utilized. Desynchronization is a useful primitive for periodic resource sharing in a variety of sensor applications.

The Low-Energy Adaptive Clustering Hierarchy (LEACH) protocol combines TDMA-style contention-free communication with a clustering algorithm for wireless sensor networks. Clustering is a popular approach for sensor networks since it facilitates data aggregation and in-network processing at the cluster head to reduce the amount of data that needs to be transmitted to the base station. While intra-cluster communication is contention-free and interferences among clusters are avoided, communication between the cluster heads and the base station is still based on CSMA. Furthermore, LEACH assumes that all nodes are able to reach the base station, which affects the scalability of this protocol [40].

The Lightweight Medium Access Control (LMAC) protocol is based on TDMA, that is, time is again divided into frames and slots, where each slot is owned by exactly one node. However, instead of relying on a central manager to assign slots to nodes, nodes execute a distributed algorithm to allocate slots [41]. Each node uses its slot to transmit a message consisting of two parts: a control message and a data unit. The fixed-size control message carries information such

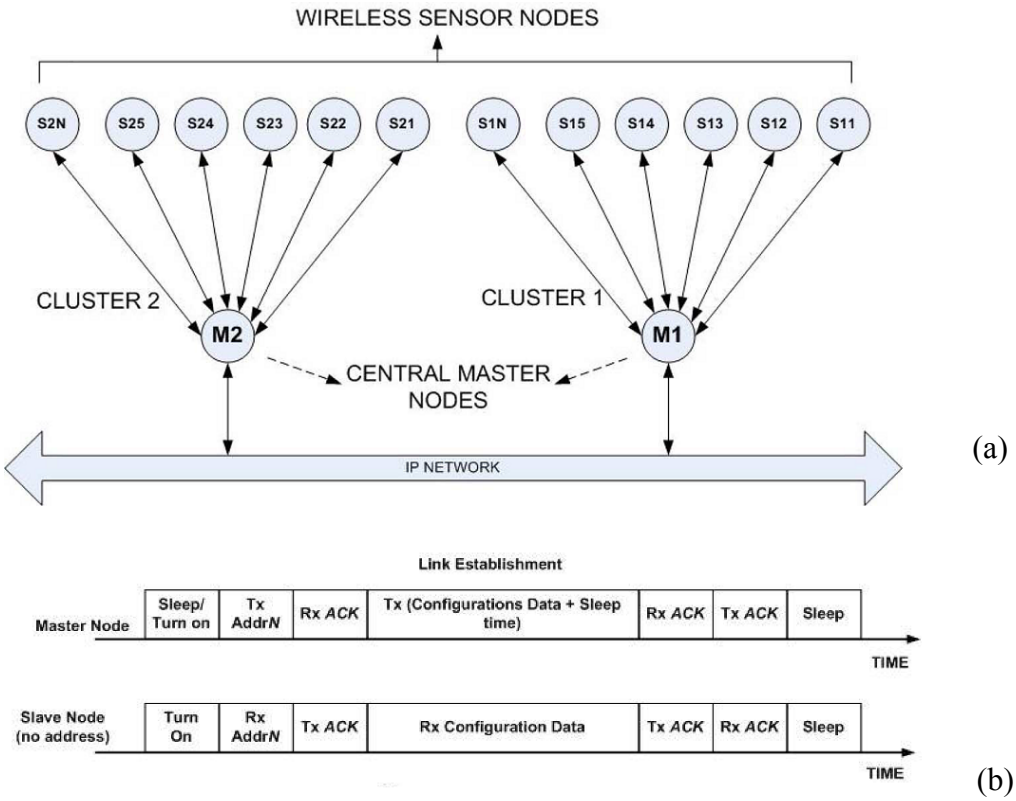

Figure 2.8: Omeni-Toumazou's protocol: a) Clustered topology, b) Link establishment [3]

as the identity of the time slot controller (2 bytes), the distance (in hops) of the node to the base station (1 byte), the address of the intended receiver (2 bytes), and the length of the data unit (1 byte). Thus, the 12-byte overhead can make this protocol energy-inefficient when data payload is in the order of a few ten of bytes.

One of the highly-cited publications on energy-efficient ad-hoc WSN MAC protocol design, particularly for wireless BSNs, is Omeni-Toumazou's work [3]. The protocol's clustered master-slave network topology and its link establishment process are shown in Figure 2.8 a, and, b. Joining a network is centrally managed and all communications are single-hop. To avoid collisions with nearby transmitters, a channel assessment algorithm based on standard listen-before-transmit is used. To handle time slot overlaps, novel concept of a wakeup fallback time is introduced [3]. The protocol is implemented in hardware as part of the Sensium™ ASIC, and measurements show better energy efficiency of this work compared to popular standard protocols: IEEE 802.15.4 (ZigBee), IEEE 802.15.1 (Bluetooth), and, IEEE 802.11 (Wi-Fi).

CHAPTER 3 ARCHITECTURE, SYSTEM AND CIRCUIT DESIGNS

3.1 Brain-ASNET Design and Implementation Aspects

To realize the first version of Brain-ASNET, we have to analyze many design and implementation aspects (Figure 3.1) from system-level design of the network itself, the system-on-chip, sensor and coordinator modules, circuit-level ones, to physical implementation aspects of the network, the ASIC, and a required user interface. The main design and implementation aspect of Brain-ASNET are listed as follows:

A. *System-Level Design*: There are many system-level aspects to be analyzed for the design of the Brain-ASNET, such as network architecture and topology, network protocol and its required layers of this application i.e. DLL, MAC, and PHY, the system design of sensor nodes (and specifically the required SoC as the configurable ASIC), the coordinator and the user interface.

B. *Circuit-Level Design*: For this project, we consider that the coordinator and its interface with the computer do not have energy source restrictions as we design and implement them with available commercial components and connect to power outlet. The implantable sensor nodes, on the other hand, have extremely-restricted energy source. Therefore, the main circuit-level design aspects to implement the SoC are state-of-the-art circuit topology selection or coming with novel designs for the lowest possible power dissipation and the least possible silicon area occupation, with focus on power-hungry and

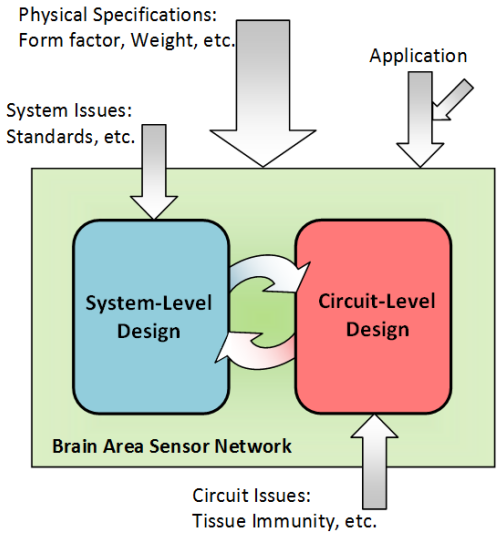

Figure 3.1: General space of design and implementation aspects of Brain-ASNET

area-occupying building blocks, respectively. We evaluated our SoC design complexity and integrated circuitry requirements and chose an IBM 0.13µm CMOS technology through CMC Microsystem and MOSIS available for Canadian academic researchers. This process would be fast enough for RF integrated circuit implementation of our specific application (on 902-928MHz ISM frequency band); and our chip design would be pad-limited which results in less fabrication price in comparison with other CMOS fabrication technologies available through CMC Microsystems.

C. *Physical Implementation*: Many physical design and implementation aspects are required to be studied carefully. These include implantability of the neural-recording sensor-node implant, its microelectrode array and their form factors, miniature high-efficiency antenna design [42, 43], specific absorption rate of the scalp, and other involved tissues [44], biocompatibility of materials [45], microsystem packaging [46], surgery, electrode mounting, and more. However, these topics would demand other research projects around the Brain-ASNET main project of this Master's research thesis.

3.1.1 Sensor Node Design and Implementation

In this section we discuss about analysis and design, and, implementation of implantable sensor nodes with ASIC core, that includes a network control unit custom designed for the proposed network protocol, a RF transceiver, an analog front-end, and other peripheral building blocks.

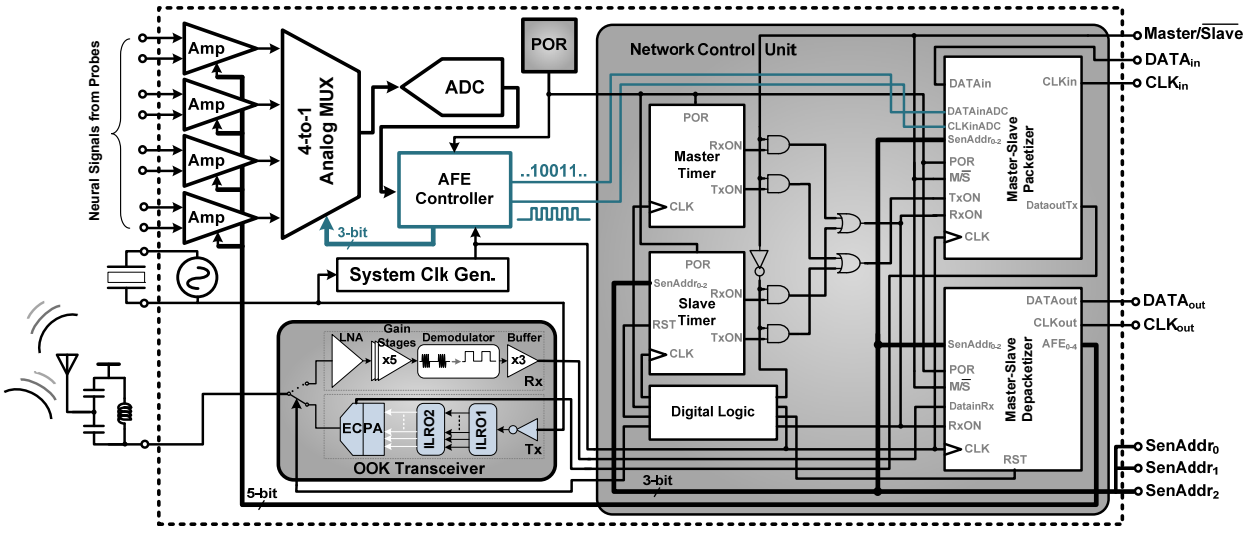

Figure 3.2: The designed sensor-coordinator Brain-ASNET ASIC architecture

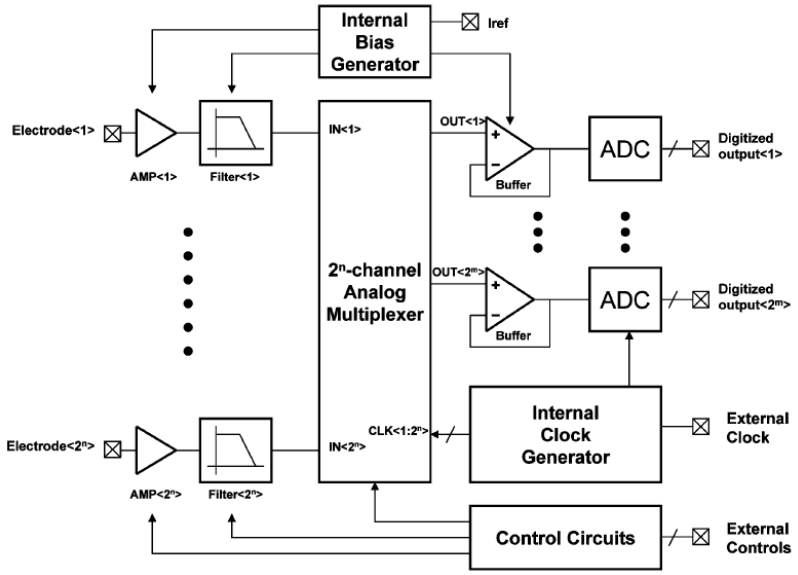

Figure 3.3: General AFE architecture of multi-channel neural recording systems [4]

Because of the energy source restrictions for wireless intracortical implants, our ASIC should be implemented employing ultra low power design techniques. As well, having the least silicon area for the whole SoC design is an important note to take into the consideration.

The SoC includes a full-custom logic designed Network Control Unit (NCU), which is the building block responsible for handling DLL and MAC network protocol layers between sensor nodes and the coordinator. Figure 3.2 shows the architecture of the designed SoC for the proposed system, along with detailed block diagrams of the main functional building blocks. The building blocks in gray, which are the OOK transceiver, the NCU, the Power On Reset (POR) and System Clock Generation, are functional whether when the SoC is configured as a sensor node ASIC or when the SoC is configured as the coordinator's ASIC. The other building blocks, which are AFE part's neural amplifiers, analog multiplexer, ADC and AFE controller, are functional only when the SoC is configured as a sensor node ASIC.

Main challenges to implement a low-power area-efficient AFE with high number of neural recording channels are 1) to design an ultra-low-power, small-area AFE architecture, 2) to chose the proper multiplexing scheme between TDM and FDM, and, 3) to employ state-of-the-art ULP circuit design techniques for neural amplifiers and ADCs. Lot of research has been done to fulfil these tasks individually. Authors in [4] propose a useful AFE design optimization technique where the number of neural amplifiers, ADCs, buffers and the number multiplexing stages becomes important in over-100-channel neural recording microsystems (Figure 3.3).

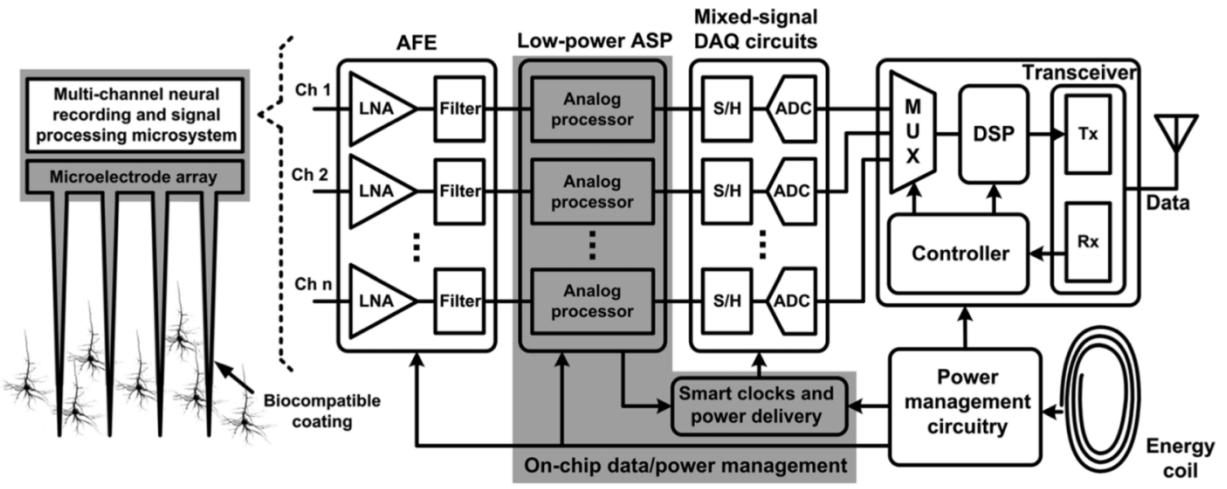

Figure 3.4: A neural-recording AFE architecture with one conventional ADC per channel [47]

Figure 3.4 and Figure 3.5 show two conventional AFE architectures. The former has a dedicated conventional ADC on each of the neural recording channels. If ULP medium-resolution ADCs, like 8–10bit SAR ADCs – that occupy a large silicon area – is used in this AFE architecture, then having high number of recording channels is impractical [47]. The latter AFE architecture presented in [48], on the other hand, uses an ULP small-area delta-sigma (ΔΣ) modulator (with no decimation filter) on each channel, and shifts the digitization process complexity (decimation filtering) to the external side, but at cost of a higher output data rate (because of oversampling). This fact, however, does not have a noticeable effect on power dissipation of wireless RF transceiver of the SoC, if a high-bandwidth RF transceiver (like UWB) is employed.

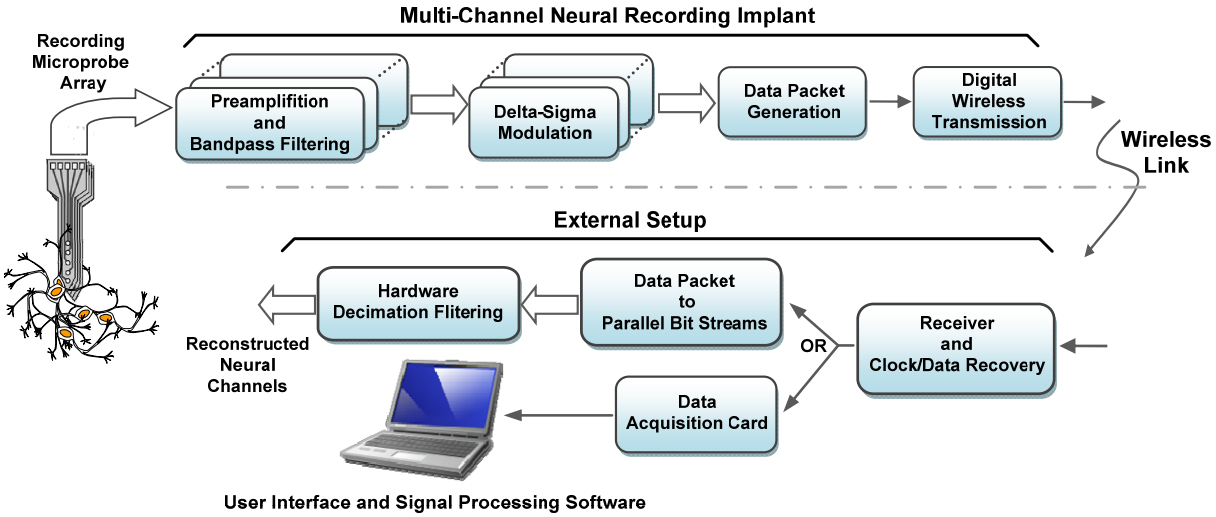

Figure 3.5: A neural-recording AFE architecture with one ΔΣ modulator per channel [48]

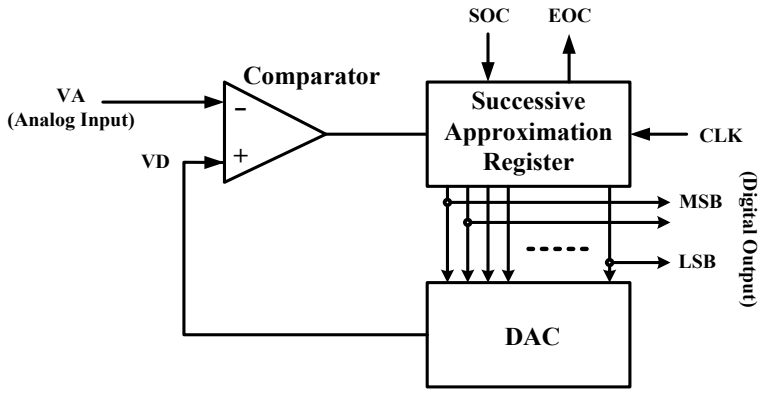

Figure 3.6: The successive-approximation register ADC architecture

Successive-Approximation Register (SAR) ADCs are the best ADC architecture choice for ultra-low power designs [49]. However, SAR ADCs with resolution more than 8 bits usually occupy a considerable amount of silicon area. Selection of a low-power area-efficient neural amplifier is also important in the design of multichannel neural recording implantable microsystems. Because neural amplifiers take considerable amount of silicon area, and our contributions are in other main building blocks of the SoC, we exclude the neural amplifiers for this project's chip tapeout. For this project, having four neural recording channels on each sensor node, we design a highly-linear 4-to-1 analog multiplexer along with an 8-bit SAR ADC as the AFE. A range 3 to 10 KHz is enough to digitize the neural signals. The conversion rate of the ADC is determined based on available system global clock frequency, which itself depends on available crystal oscillator frequency, which a multiplier of it should be somewhere in the 902–928MHz ISM frequency band. We discuss about this later in the section 3.3.

We design an state-of-the-art ultra-low-power 8-bit SAR ADC with minimum ADC offset, gain error, power consumption and required physical silicon area, and, maximum linearity and dynamic range. Figure 3.6 shows design of the SAR ADC architecture. The full-custom designed successive-approximation register logic schematic is shown in Figure 3.7. We design an ULP split-capacitor residue 8-bit Digital-to-Analog Converter (DAC) (Figure 3.8) using low-voltage boot-strap switches. The dynamic comparator structure and its ULP LV dynamic latch designs are shown in Figures 3.9 a and b. The AFE Controller in the sensor node's SoC architecture is responsible for managing the interface between the SAR ADC's multiplexed raw output bitstream and NCU's slave packetizer input.

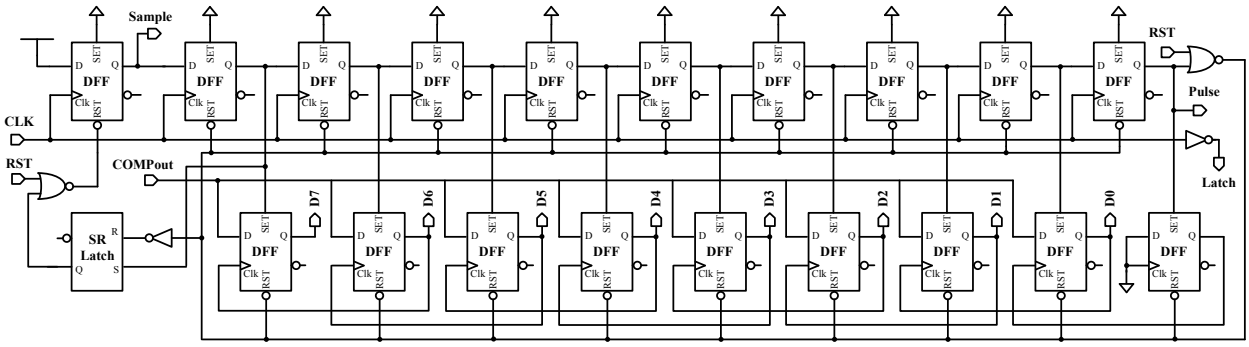

Figure 3.7: The low-power 8-bit SA register design with required timing logic

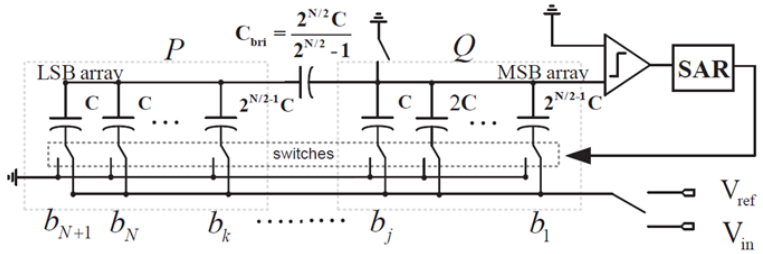

Figure 3.8: The low-power low-voltage Split-Capacitor residue 8-bit DAC design

Higher-frequency wireless RF signals exposed to body tissue are absorbed at higher rates. On the other hand, if a wireless implant has higher output RF transmitter data rate, higher transmission bandwidths are only available at higher ISM frequency bands – which can be less efficient because of RF signal absorption at higher frequencies. Researches show the safest and most energy-efficient available wireless transmission RF bands for biomedical applications are the 402–405MHz MICS (Medical Implant Communication Service) and 902–928MHz ISM bands.

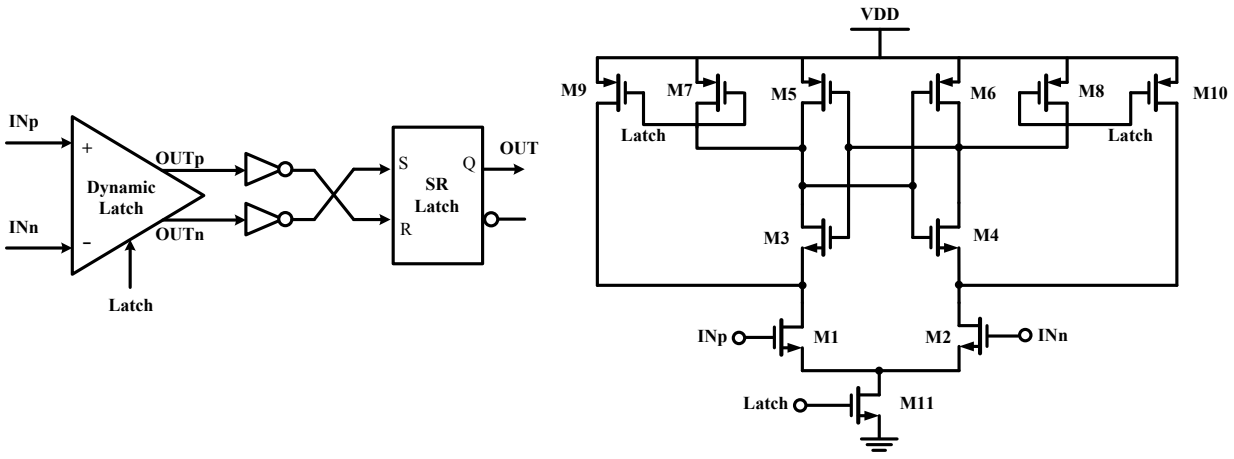

Figure 3.9: Comparator design: a) the logic structure, and, b) its ULP dynamic latch

Table 3.1: Comparison of state-of-the-art neural data reduction systems [50]

		[51]*	[52], [53]	[17], [54]**	[55]***	[56]	[50]
Publication Year		2005	2006, 10	2007, 09	2009	2013	2014
Math. Transform		NA	DWT – *Symmlet4*	NA	NA	WHT	DWT – *Harr*
No. of Channels		32	32	64	16	128	64
Sampling rate (kSps)		20	25	62.5	30	25	20
Resolution		5	10	1	8	8	8
Outgoing Bit-rate (Mbps)		2.5	NA	2	16	NA	3.2
NSE%		NA	NA	NA	0	4.66	1.8
Compression Measures	CR	12.5	62	8	8	63	At least 116
	FR	NA	NA	NA	60	~8	~8
	TCR	NA	NA	NA	480	~504	~903
Feature Size (µm)		0.5	0.5	0.5	0.18	0.18	0.13
Area/Ch. (mm^2)		0.187	0.18	0.3	0.116	0.0128	0.0032
Power/Ch. (µW)		75@3V	94	197@1.8V	96@1.8V	0.65@1.8 V	1.47@1.2V
Details		SD, ADC, Framing	Thresholding and RLE	SD, ADC, Framing	Spike Extraction, Framing	Thresholding and RLE	Spike Extraction, Framing

* Only for spike detection ASIC, ** Only for NPU, *** Only for digital ASIC

Therefore, to increase the number of recording channels on each sensor node, an on-chip data reduction process is required. Many researches on design and implementation of neural signal detection, data compression and reduction systems have been performed and are available in the literature. Table 3.1 compare few of these data compression and data framing digital designs, where in [50] authors claim a novel design with lower power consumption and better silicon area efficiency for a 64-channel intracortical recording system versus one of the most popular counterparts published by Polystim members [55].

3.1.2 Coordinator Design and Implementation

To implement the Brain-ASNET's coordinator, we should consider the same frequency band, modulation, and framing for both sensor node and coordinator RF transceivers designs. That is why, for the first tapeout, we use the same integrated RF transceiver design for the configurable

ASIC. However, since the Brain-ASNET coordinator has not energy source restrictions like the sensor nodes have, we can have shift the power-complexity of the RF communication of network's PHY layer from implantable sensor node's RF transceiver to the external coordinator's RF transceiver. Although analysis shows that a symmetric wireless communication link is the most energy-efficient design, when energy source is restricted on one side, we can use a relaxed low-performance RF transmitter with minimum output power and a relaxed low-performance RF receiver with minimum sensitivity at a desired Bit Error Rate (BER), and use a complex high-performance RF transceiver on the other side to compensate.

Here we also add that, we design the SoC to be configurable, where by setting a specific ASIC pin, called "$\text{Master}/\overline{\text{Slave}}$", to the logic high "1" (on the coordinator's module), the NCU is configured as a master NCU which have the required functions needed for the coordinator's network packetizer and depacketizer. More details are given in section 3.2.

3.1.3 User Interface Design and Implementation

A basic computer user interface is required for the first development phase of Brain-ASNET. We design GUI so that we can occasionally send some configuration data (from the GUI on a PC), to the sensor nodes, that can be used to change different settings on neural recording sensors like neural recording amplifier's gain and bandwidth, etc. The configuration data is digitized by GUI and is packetized by the coordinator's NCU to be wirelessly sent in beacon time slot. Then, it is received on RF front-end and depacketized in NCU of each sensor node. On the other hand, the bitstream received in each sensor node's time slot is depacketized in the coordinator's NCU. If no transmission error is detected, neural signal recorded samples (one bye per each recording channel of sensor node) plus a byte of address and configuration data comes out of coordinator's NCU along with a relevant gated clock. Correspondingly, these sampled data is temporarily stored on the coordinator's USB microcontroller, and then it is sent to the GUI on the PC. GUI demultiplexes the samples, dequantizes them, and displays corresponding analog samples on monitoring windows individually for each sensor node according to its address.

Figure 3.10 illustrates an advanced user interface that we suggest for Brain-ASNET to be considered in the next development phases. There can be a Wi-Fi connection between the coordinator and the PC. This idea is useful if we want to have more freedom of movement for the subject under study or control, while the coordinator can, for example, be mounted on his/her

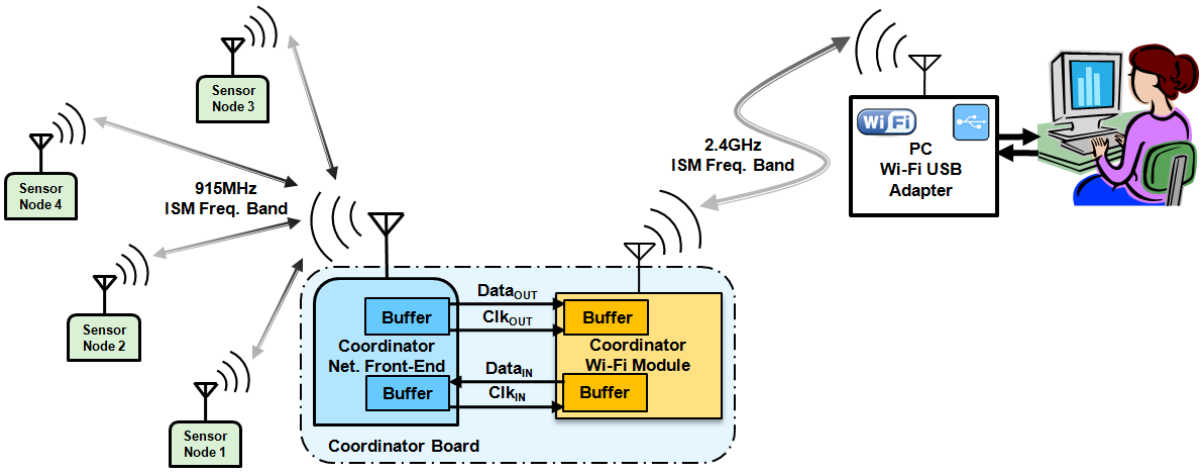

Figure 3.10: A Brain-ASNET with its coordinator wirelessly connected to the user

waist, and wirelessly communicates with sensor nodes on a lower ISM frequency band. The coordinator should also communicate with the computer on a higher ISM frequency band, or it can be Wi-Fi (2.4GHz or 5GHz).

3.2 Ad-hoc Protocol Design for Brain-ASNET

While mesh network topology is conventional for traditional Wireless Sensor Networks (WSN) with scalability and topological changeability, master-slave network architecture, i.e. star logical topology, could dramatically save energy in limited-size WSNs [30]. Table 3.2 summarizes some of the key features of the proposed network and traditional ad-hoc WSNs and Body Sensor Networks (BSN). Figure 3.11 shows the architecture of the proposed network, including a coordinator and four sensor nodes.

Flexible networking standards such as Wi-Fi, Bluetooth, and ZigBee are the most conventional protocols used in ad-hoc WSNs and most of BSNs. Nevertheless, they result in bulky and power hungry systems. Therefore, we have to design an energy-efficient ad-hoc network protocol for our Brain-ASNET application where implantable sensor nodes have severe energy-source restriction. Since significant causes of energy dissipation in WSNs are collisions, idle listening, protocol overhead, and traffic fluctuations, contention-free MAC protocols are preferred over their contention-based counterparts for limited-size WSNs with no expected topological changes and traffic bursts – like body sensor networks [3]. Almost all TDMA-based protocols proposed in the recent decade tend to solve fixed time-slot assignment problem with time-domain multiplexing, but yet utilize the energy-efficiency advantage of such protocols. To give the network capability of scalability usually leads to a large overhead for a TDMA-based protocol. Many energy-efficient TDMA-based protocols have been proposed in the last decade, such as TRAMA, Y-MAC, DESYNC-TDMA, LEACH, LMAC, and the Omeni-Toumazou's protocol, as described in the section 2.2.

Table 3.2: Brain-ASNET vs. Traditional ad-hoc WSNs and BSNs

Attribute	**Network**		
	WSN	**BSN**	**Brain-ASNET**
Energy source	Low	Low	Ultra-low
Self-organizing	Yes	No	No
Architecture	Mesh	Star	Star
Traffic	Burst	Burst	Regular
Applications	*Various*	Healthcare	Prosthetic, BCI
SN form factor	*Medium*	Wearable	Implantable
SN transceiver	m-range, LP	m-range, ULP	cm-range, ULP

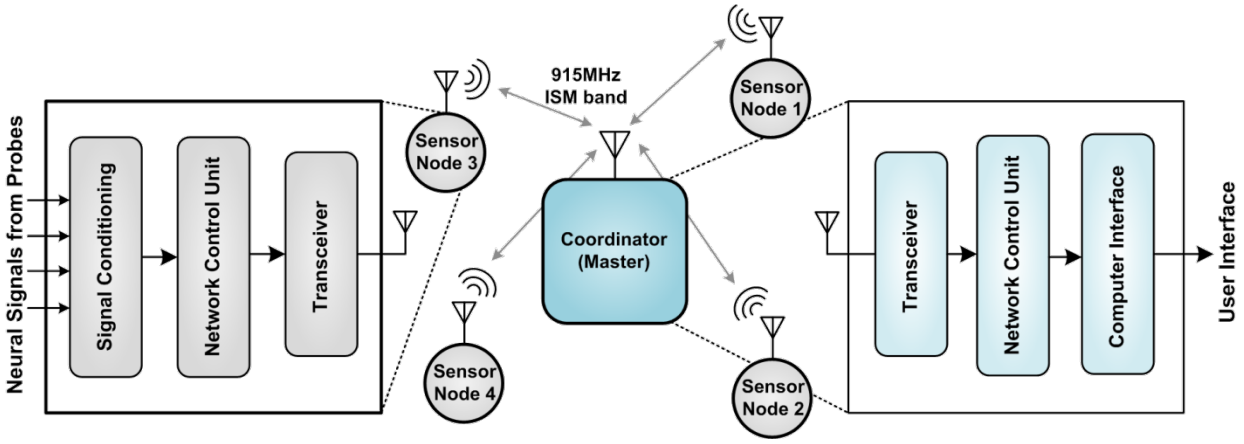

Figure 3.11: The simplified Brain-ASNET, sensor node, and coordinator architectures

But, are these TDMA-based MAC protocols still energy-efficient if the number of network sensor nodes is considerably low, with no expected topological change? No, they are not. In a centralized network like our case study, where all communications are single-hop, using fixed time-slot assignment TDMA-based MAC protocols that avoids any undesired collision and idle listening, results in superb energy efficiency. In this section we propose an ad-hoc energy-efficient network protocol for the first development phase of Brain-ASNET – centralized real-time neural recording-only.

The frame structures of the designed network protocol are similar to that of HDLC standard protocol, other than final flag field and bit-stuffing approach. Figure 3.12 shows the HDLC protocol frame structure [33] versus the proposed modified HDLC one. Because the protocol allows the presence of arbitrary bit patterns (i.e., there are no restrictions on the content of the various fields imposed by the link protocol), there is no assurance that the SYNC patterns (either beacon or sensor-specific) will not appear somewhere inside the frame, which can destroy the network's synchronization. To avoid this problem, a procedure known as bit stuffing is used in standard HDLC protocol. For all bits between the starting and ending flags, the transmitter inserts an extra “0” bit after each occurrence of five “1”s in the frame. In other words, after detecting a starting flag, the receiver monitors the bit stream. When a pattern of five “1”s appears, the sixth bit is examined. If this bit is “0”, it is deleted. If the sixth bit is a “1” and the seventh bit is a “0”, the combination is accepted as a flag. If the sixth and seventh bits are both “1”, the sender is indicating an abort condition. This bit stuffing approach, however, causes a variable frame size and makes necessary to use an ending SYNC pattern to allow receiver to notice when the

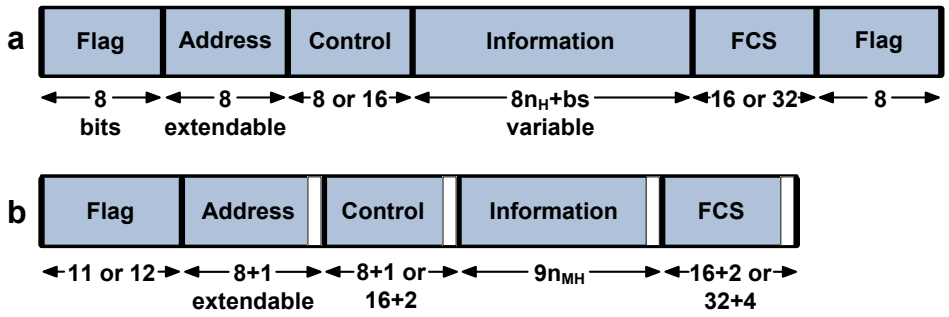

Figure 3.12: Protocol frame structures of a) standard HDLC vs. b) proposed modified HDLC

reception of a frame is completed. This makes the design of this protocol and its corresponding hardware more complex, and it may cause energy inefficiency. To solve this problem, several data encoding techniques such as 6b/8b encoding, 8b/10b encoding, etc. can be utilized to obtain a non-variable size frame. However, these techniques also add implementation complexity, that also means more power dissipation.

Here, we propose a simple, efficient idea to prevent the problem of variable size frame in HDLC protocol caused by its special bit stuffing approach, and, at the same time, to prevent destroying communication synchronization allowing any arbitrary bit patterns in the frame, for which reason HDLC protocol uses its special bit stuffing approach. Choosing a *beacon* SYNC pattern "011111111110" (12-bit), and a *sensor-specific* SYNC pattern "01111111110" (11-bit), and stuffing (attaching) a logic zero at the end of each byte in the whole packet (Address & Control, Data Payload, and FSC fields) except the SYNC field, we obtain a non-variable frame size, with least implementation complexity. The length of protocol frame for HDLC and the proposed modified HDLC are as follows, respectively:

$$L_H = 8\left(n_H + 6\right) + bs \tag{3.1}$$

$$L_{MH} = 9\left(n_{MH} + 5\right) + 2 \tag{3.2}$$

where, n_H, and n_{MH} are the number of bytes of information for HDLC and proposed modified HDLC protocols, respectively, and *bs* is the number of stuffed bits over the various field of the HDLC protocol except the start and end flags (i.e. Address, Control, Information, and FCS); but it is shown just under the Information field for simplicity (Figure 3.12). *bs* is indeed a function of the length of all these fields (i.e. 8(n_H+4)). For large Information field lengths, for example

n_H=n_{MH}=1000, if we consider the worst case of all 1's for all the fields except flags, since for every five consecutive 1's a zero bit is stuffed, therefore the length of protocol frame for HDLC (L_H) to that of the modified HDLC (L_{MH}) is as follows:

$$\eta = \frac{L_H}{L_{MH}} = \frac{8(1000+6)+\lfloor (8(1000+4))/5 \rfloor}{9(1000+5)+2} \cong 1.07 \tag{3.3}$$

where η can be considered as energy efficiency of the proposed protocol to regular HDLC.

The most important problem associated with networks operating by TDMA-based protocols is synchronization issue. In distributed systems, each node has its own clock and its own notion of time. However, a common time scale among sensor nodes is important to identify causal relationship between events in the physical world, to support the elimination of redundant sensor data, and to generally facilitate sensor network operation. Since each node in a sensor network operates independently and relies on its own clock, the clock readings of different sensor nodes will also differ. In addition to these random differences (phase shifts), the gap between clocks of different sensors will further increase due to the varying drift rates of oscillators. Therefore, time (or clock) synchronization is required to ensure that sensing times can be compared in a meaningful way.

Different synchronization protocols have also been developed in the recent decade, which can simply be categorized to three major approaches: one-way, and two-way synchronization message exchange, and receiver-receiver synchronization. Lightweight Tree-Based Synchronization (LTS) [57], Timing-sync Protocol for Sensor Networks (TPSN) [58], Flooding Time Synchronization Protocol (FTSP) [59], Reference-Broadcast Synchronization (RBS) protocol [60], and Time-Diffusion Synchronization (TDP) protocol [61] are examples of such synchronization protocols. These protocols are usually based-on complicated algorithmic processing, which is a strong choice for wide and dynamic wireless sensor networks.

Here, we explain a rather simple, energy-efficient periodical synchronization approach. Similar to all TDMA-based protocols, the proposed protocol is based-on time frames and slots, but their duration can dynamically change if the network loses its synchronization for a while. Time frames and slots of the designed protocol are shown in Figure 3.13.

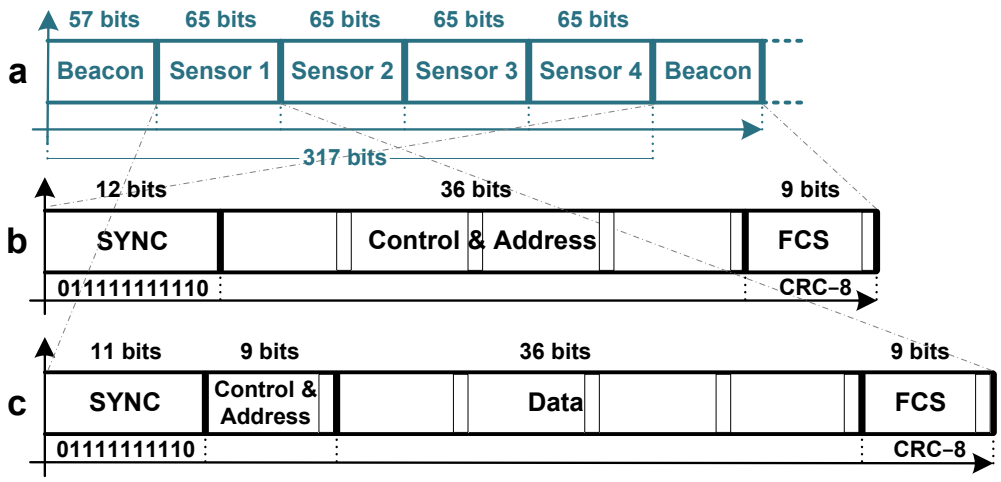

Figure 3.13: The network protocol dedicated design for Brain-ASNET: a) time frame and slots, b) beacon frame structure, and, c) sensor-specific frame structure

In each time frame, a time slot is dedicated to the master (also known as base station or coordinator) to broadcast a beacon (containing configuration information) to its slaves (also known as subscribers or sensor nodes). During this time slot, slaves switch their transceivers on to receiving mode, continuously hunting for a beacon SYNC pattern. Once such a bit pattern is detected, that slave is then synchronized and joined to the network. Hereafter, in each sensor-specific time slots, synchronized slaves wake up in their schedules, based-on their MAC address, and transfer buffered data. If any problem causes the network loses its synchronization, the same procedure is repeated. However, all the different possible states are considered to initialize synchronization in a network for the first time or to resynchronize the sensor node to a synchronized network.

1. *At first, the base station is powered-on, and then a sensor node is powered-on.*

   Upon a sensor node is powered-on, it goes to listening mode and waits to receive a beacon; upon getting synchronized with the base station, it continues its scheduled communication.

2. *At first, sensor nodes are powered-on, and then the base station is powered-on.*

   Just like the previous state, all sensor nodes are in listening mode. After the base station sends a beacon, the sensor nodes become synchronized with the network and start their scheduled communication.

Table 3.3: Protocol design features of Brain-ASNET vs. traditional WSNs and BSNs

Attribute	Network		
	WSN	**BSN**	**Brain-ASNET**
MAC	CSMA	CSMA/TDMA	TDMA
Protocol stack	Bluetooth/ZigBee	Bluetooth/Custom	Custom
MAC address	Dynamic	Dynamic	Hardware
Link establishment	One-by-one	One-by-one	All-at-once
Synchronization	Algorithmic	Periodic	Periodic

3. *In an already synchronized network, a sensor node becomes disconnected for a while.*

   Since the other synchronized sensor nodes might be communicating with the base station, the desynchronized sensor node receiver may receive irrelative data. Therefore, if the beacon SYNC pattern is different from sensor nodes SYNC pattern, the desynchronized sensor node just ignores incoming data until a beacon SYNC pattern is detected.

4. *In an already synchronized network, the base station becomes disconnected for a while.*

   Utilizing the watchdog timer idea in sensor node's timer, if an already-synchronized sensor node does not receive the network beacon for a specific time, it will be reset and go to the listening mode.

Table 3.3 highlights some of key features of the designed protocol for Brain-ASNET, and of conventional protocols for ad-hoc WSNs and BSNs. Table 3.4 compares standard HDLC and the (FCS) field is an error-detecting code calculated from the remaining bits of the frame, exclusive

Table 3.4: The standard HDLC vs. the proposed modified HDLC protocols

Attribute	Protocol	
	HDLC	**modified HDLC**
Variable-rate bit stuffing	Yes	No
Stop Flag (as well as start Flag)	Yes	No
Fixed time slotting	No	Yes
Bit stuffer/destuffer complexity (at TX & RX)	Yes	No
Energy efficiency at large data package sizes	Average	Good

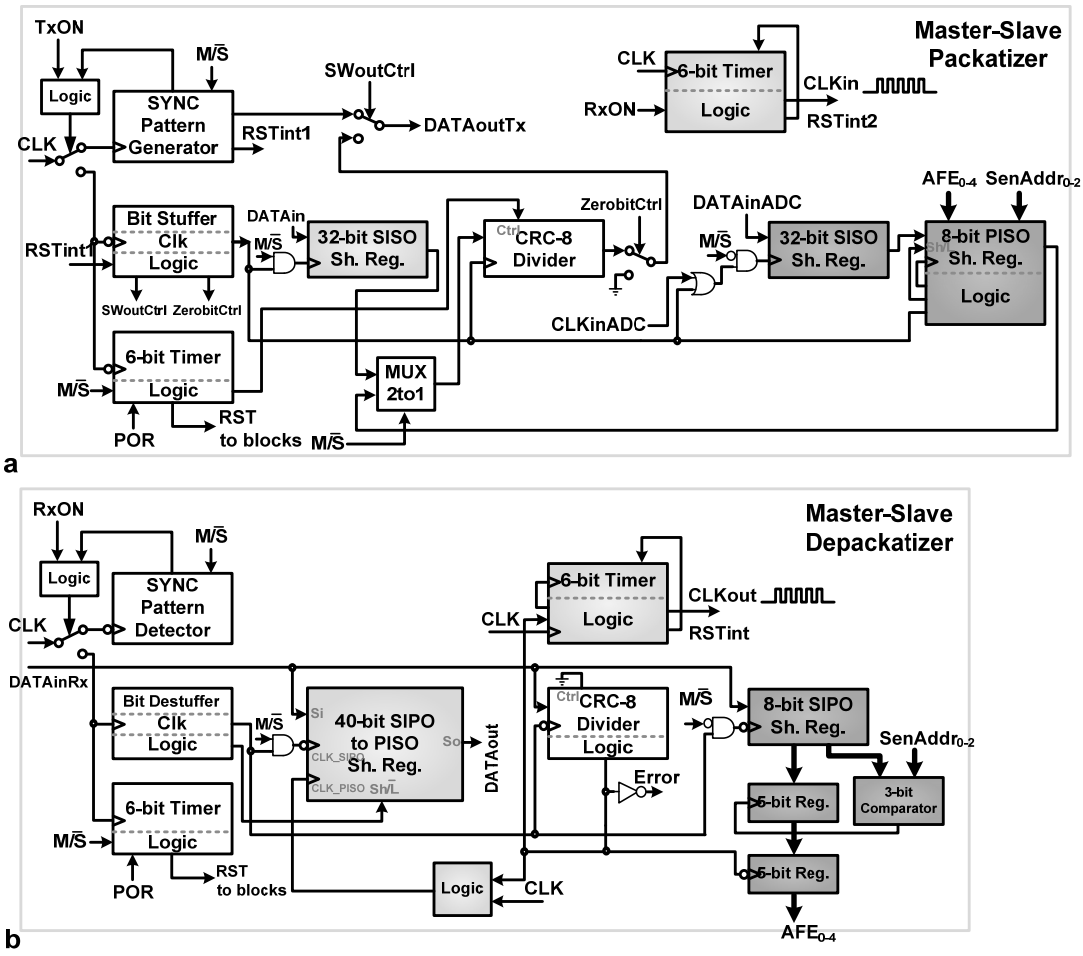

Figure 3.14: NCU logic design a) Master-Slave Packetizer, and b) Master-Slave Depacketizer

of the SYNC field. This code is generated by a CRC-8 divider. We do not want error correction proposed modified HDLC. In the proposed protocol frame structures, frame check sequence in our proposed protocol DLL layer. Thus, we choose CRC-8 as a strong error detection approach compared to other available CRC polynomials such as DARC-8, and ATM-8 [62].

The Network Control Unit (NCU) performs a centrally-managed link establishment of each sensor node, initial synchronization and periodic resynchronization considering all the possible states mentioned above. To do so, each unsynchronized sensor node goes to listening mode after power-on or any transmission failure. To implement the designed protocol packets, both the sensor node and the coordinator require corresponding packetizers. Since the NCU would be configured to be as either only sensor-node's controller, or only coordinator's controller, in fully-costumed design we utilize common blocks between coordinator’s packetizer and sensor node’s one, making a single Master-Slave Packetizer. The same approach is considered to build the

Master-Slave Depacketizer. Figure 3.14 shows the block diagrams of the packetizer and depacketizer. The “ Master/$\overline{\text{Slave}}$” input pin of the SoC configures the NCU to function as coordinator’s NCU or sensor node’s NCU.

For this project, the design of NCU is done based on packetizer design used for peer-to-peer communication protocol, similar to design in [63] for a data-packet checker. We need a pair of packetizer and depacketizer for each sensor node and coordinator, plus required master and slave timers. Since the designs are straightforward and many building blocks between sensor node controller and coordinator controller are identical, a compact configurable master-slave NCU is fully-custom designed. Although a HDL synthesize is more efficient where the size of a digital circuit is large, CMC does not provide access for academic users to standard cell library to have post-layout simulation of analog and synthesized digital building blocks on the same SoC at transistor level.

3.3 ULP RF Transmitter Design for Brain-ASNET

A literature review was done to choose the best modulation scheme to implement ULP RF transmitter and receiver for our wireless implantable sensor nodes. Although Ultra Wide-Band (UWB) wireless transmission allows higher data rates, but implementation of ULP UWB receivers with good performance is not easy with the current technologies. Also, almost all ULP UWB transmitter designs for biomedical applications in the literature are for peer-to-peer communication links, supposing to have a high-performance UWB receiver. OOK and FSK modulations schemes are the best options for our application.

Traditional UHF transmitter architectures are usually based on RF mixer as modulator, Local Oscillator (LO) to generate carrier frequency, and power amplifier which is hardly efficient enough to lead to a low-power energy-efficient design for data rates up to a few Mbps. Conventional UHF LOs employ a power hungry Phase- or Delay- Locked Loop (PLL/DLL) as the frequency multiplier, driven by a crystal oscillator of tens of MHz. Authors in [64] describe the design of an MICS band FSK transmitter based on injection-locking and frequency multiplication. Since the achievable frequency deviation obtained from switching oscillator's crystal shunt capacitor is limited, the maximum effective data rate would be at most up to a few hundreds of kilo hertz. Here, we propose an RF transmitter architecture design with OOK modulation, while a data rate up to 20Mbps can be achieved. The proposed transmitter architecture is shown in Figure 3.15. It is composed of a cascaded multi-phase Injection-Locked Ring-Oscillator (ILRO), which is locked to a crystal oscillator, and an Edge- Combining Power Amplifier (EC-PA) modulated with TX_{IN} generates the output.

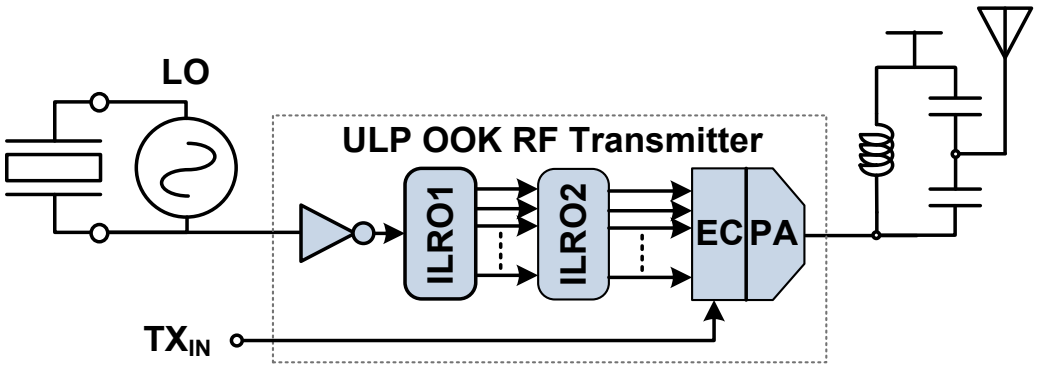

Figure 3.15: The simplified architecture of the proposed ULP OOK RF transmitter

To achieve a multiplied frequency in 902–928MHz ISM frequency band, we check resonance frequency of available commercial miniature-size crystals. Because an even multiple of the crystal's resonance frequency is required to design the first stage ILRO even number of CMOS inverters, we choose an available 44MHz crystal with a multiplication factor of 21 to obtain a 924MHz carrier frequency for the OOK transmitter. An low-power integrated crystal oscillator is designed on the SoC and it is utilized as the transmitter's Local Oscillator (LO), the same as SoC's input clock generator. As discussed in section 3.1.1, neural signal inputs of each channel of sensor nodes are required to sampled at an adequate rate from 3KHz to 10KHz. One cycle of the proposed protocol (in this design) consists of one beacon and four sensor-specific sub packets, totally 317 bits (Figure 3.13). We design a configurable digital frequency divider (÷16 or ÷32) in the System Clock Generation building block of the SoC architecture. Therefore, the AFE ADC's conversion rate, the same as sampling rate for sensor node's input neural signals, can be any of the two options below – inside the desired range of sampling rate of 3–10KHz:

$$f_{samp1} = \frac{f_{LO}}{N_1 \times PL} = \frac{44MHz}{32 \times 317} = 4.338kHz$$
$$f_{samp2} = \frac{f_{LO}}{N_2 \times PL} = \frac{44MHz}{16 \times 317} = 8.675kHz \quad (3.4)$$

where f_{samp} is the sampling frequency of input neural signals (equal to ADC's conversion rate), f_{LO} is the LO frequency, N is the digital frequency division ratio, and PL is the protocol bitstream length. We choose 8.67kHz option as the system's default sampling rate, as it allows a wider frequency content of the input neural signals to be bypass filtered and digitally recorded. Therefore, the sensor node's protocol controller (NCU slave packetizer) output and the coordinator's protocol controller (NCU master packetizer) output have both the same data rate of:

$$f_{NCU\_Data\_OUT} = f_{samp} \times PL = 8.675kHz \times 317bit = 2.75Mbps \quad (3.5)$$

The OOK RF transmitter to be designed should accept an input data rate of 2.75Mbbps. From OOK modulation analysis, a minimum frequency bandwidth of 2.75MHz on an available wireless channel is required. Therefore, 902-928MHz ISM frequency band is selected to satisfy the bandwidth requirement with an efficient miniature-sized RF antenna for the implant, relatively at a lower Specific Absorption Rate (SAR) compared to higher ISM frequency bands.

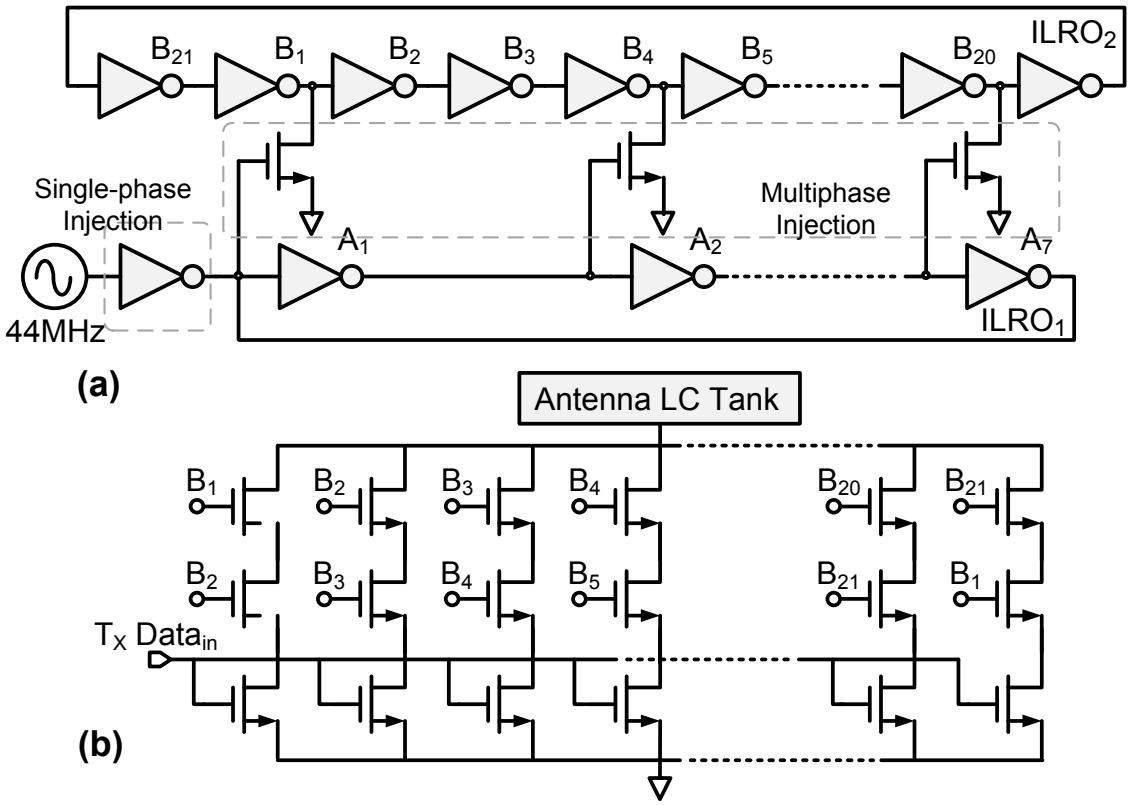

Figure 3.16: Proposed OOK RF TX: a) two-stage multi-phase ILRO, and, b) EC-PA

Figure 3.16 shows the schematic design of the two-stage multi-phase ILRO, where first-stage RO is composed of 7 inverters and second-stage RO has a chain of 21 CMOS inverters. Figure 3.17 shows the edge-combining power amplifier circuit design, in which switched currents of 21 open-drain AND gates (Figure 3.16),

$$TX_{OUT} = TX_{IN} \times \sum \left(B_1 B_2 + B_2 B_3 + \ldots + B_{21} B_1 \right) \tag{3.6}$$

which are multiply outputs of each two next inverters of second-stage RO, are combined. For a robust design to be functional in all process corners, and temperatures care should be taken in the design of each ring oscillator. Since the first ILRO and the local oscillator, and, the second ILRO and first ILRO are phase-locked together, both ILROs should have the same free running oscillation frequency of 44MHz, as below:

$$f_{LO} = f_{ILRO1} = \left(\frac{1}{7 \times 2t_{p1}} \right) = f_{ILRO2} = \left(\frac{1}{21 \times 2t_{p2}} \right) = 44MHz \tag{3.7}$$

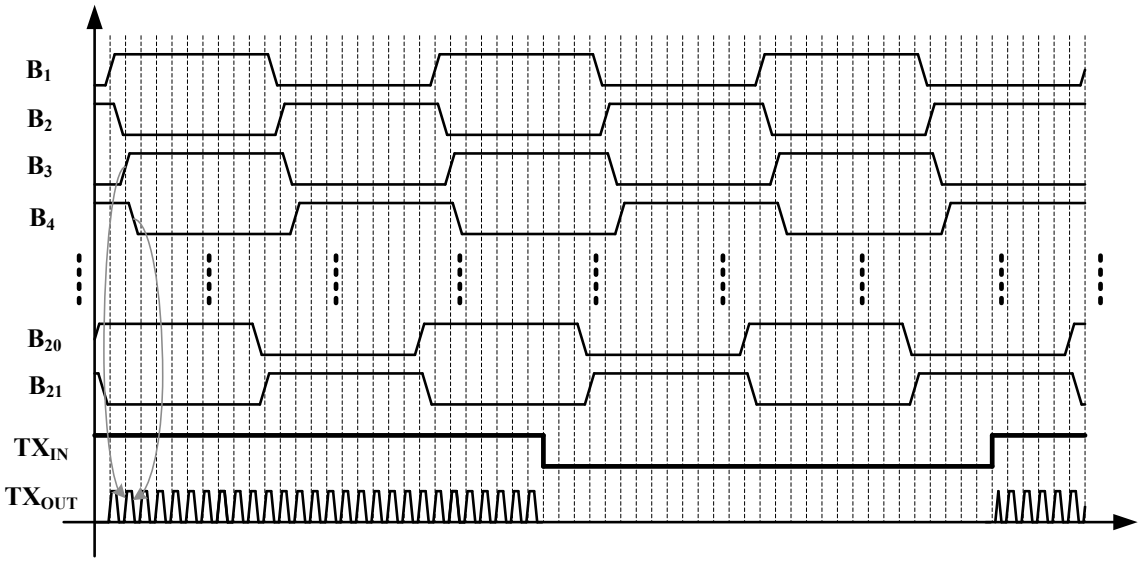

Figure 3.17: The combination of edge pulses, modulated with TX_{IN}

where t_{p1} and t_{p2} are the propagation delays of $ILRO_1$ and $ILRO_2$ CMOS inverters, respectively. A careful symmetrical layout design is required to obtain a carrier frequency with least undesired spurs. Further discussion on the circuit and layout designs and simulation results of the proposed transmitter is presented in chapter 4.

For the RF receiver design, we employ an ultra-low-power, highly-integrated OOK RF receiver architecture *by Lin, et al.* [65], which utilizes a diode-based envelop detector along with two low-pass filters as OOK demodulator. Careful circuit design and layout is required to implement an efficient UHF demodulator in this design. The block diagram of the receiver is shown in Figure 3.18. Having done an analysis on preliminary simulation result for RF gain stages in the IBM 0.13µm CMOS technology, our design requires five gain stages to have enough voltage gain at 902–928MHz frequency band, to achieve appropriate sensitivity for the receiver. The receiver LNA is designed for the maximum power transfer and sensitivity based on the employed matching LC network.

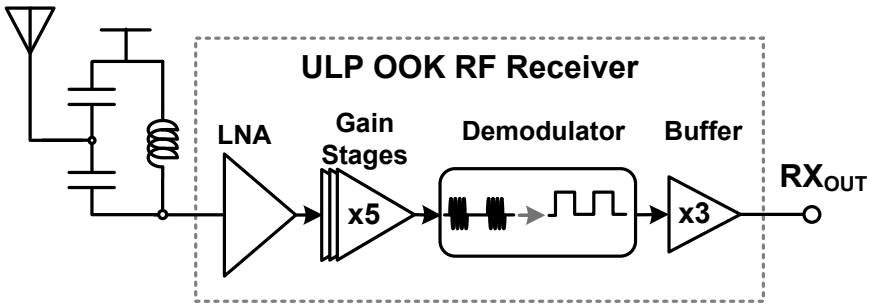

Figure 3.18: The ULP OOK RF receiver architecture designed for the Brain-ASNET ASIC

CHAPTER 4 CHIP LAYOUT, SIMULATION AND MEASUREMENT RESULTS

A first development of Brain-ASNET, studying many design and implementation aspects as described in the chapter 3, was performed. The schematic and post-layout simulations for the multi-channel neural recording sensor node's SoC design and a synchronized Brain-ASNET network of four sensor nodes and the coordinator show good results for designed energy-efficient ad-hoc protocol, ULP OOK RF transmitter, and the whole SoC microsystem, laid-out in IBM 0.13µm CMOS technology.

4.1 Circuit and Layout Designs, and, Simulation Results

The synchronization and data communication functions of the designed protocol, system's AFE linearity performance, and system's transceiver output transmit power, sensitivity, and bit error rate of the designed chip are verified by various post-layout simulations. Monte Carlo analyses, and process corner simulations are also performed to optimize for a robust design for each SoC's building block, and the whole SoC.

The OOK RF transmitter circuit was designed based on a hierarchical architecture as depicted in Figure 4.1 a. Its building block schematics, i.e. TX Component, and TX EC NAND3C circuits are shown in Figure 4.1 b, and, c, respectively. A careful optimized transistor-level design of the RF transmitter to achieve the required output power at its maximum global energy efficiency is performed. Table 4.1 shows the final transistor sizing for the whole OOK RF transmitter design.

Figure 4.2 shows the full-custom design of the integrated transmitter physical layout. To reduce any possible imbalance operation of both injection-locked ring oscillators, all physical interconnections between two successive CMOS inverters should be kept very similar. Therefore, we drew the transmitters ILROs' layouts in a rotating shape to make sure every CMOS inverter sees the same loading. We put the second stage ILRO with 21 inverters in the core of the layout and the first stage ILRO with 7 inverters surrounding the core ring.

The integrated transmitter, designed in IBM 0.13µm CMOS technology, has an output transmit power of –22dBm (less than the ISM maximum power limit regulation of –16dBm), and dissipates 137µW of power at a date rate of 2.75Mbps at 1.2V supply voltage. Considering the

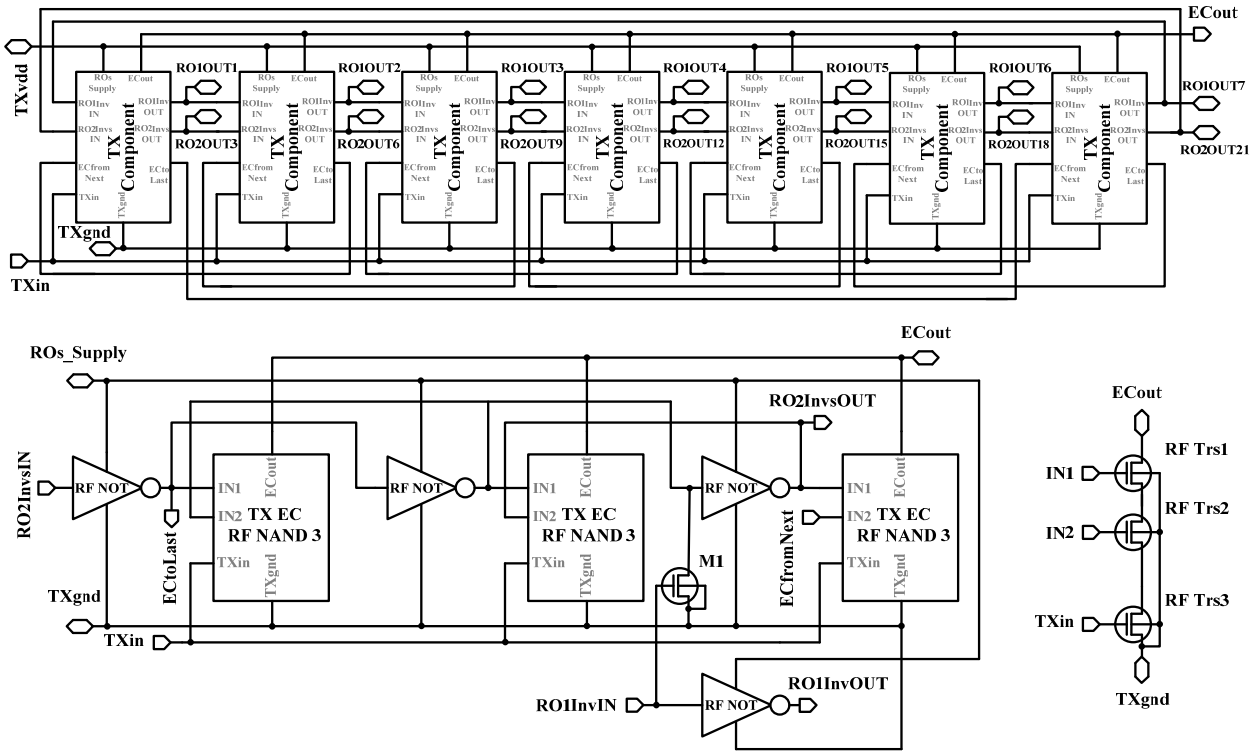

Figure 4.1: The proposed ULP OOK RF transmitter: a) Hierarchical design schematic, b) design schematic of the TX Component, and, c) design schematic of the TX EC NAND3C

scheduled operation of each synchronized sensor node, the average power dissipation of the sensor node's transmitter is as low as 28µW. Figures 4.3 a and b show power spectrum of RF transmitter antenna output when the two-stage ring oscillator is free-running and when it is injection-locked with local oscillator, respectively. This shows how the transmitter output power is degenerated when output frequency is deviated from tuned central frequency of 924MHz

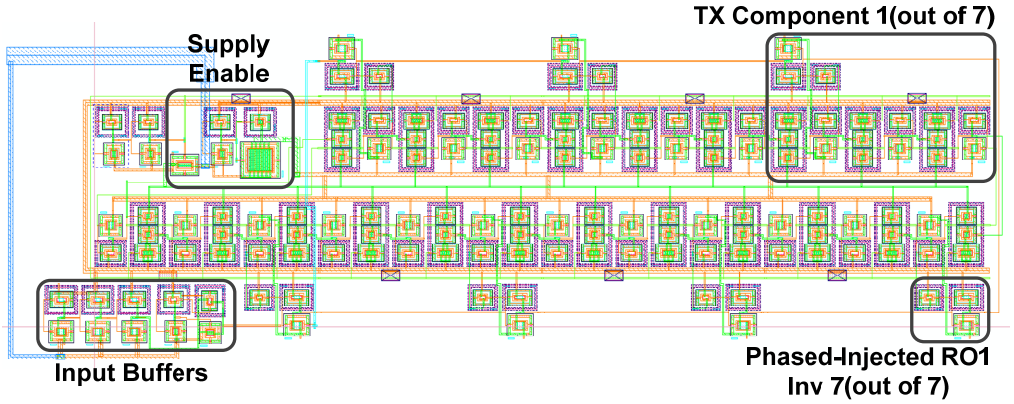

Figure 4.2: Layout design of the proposed ULP OOK RF transmitter

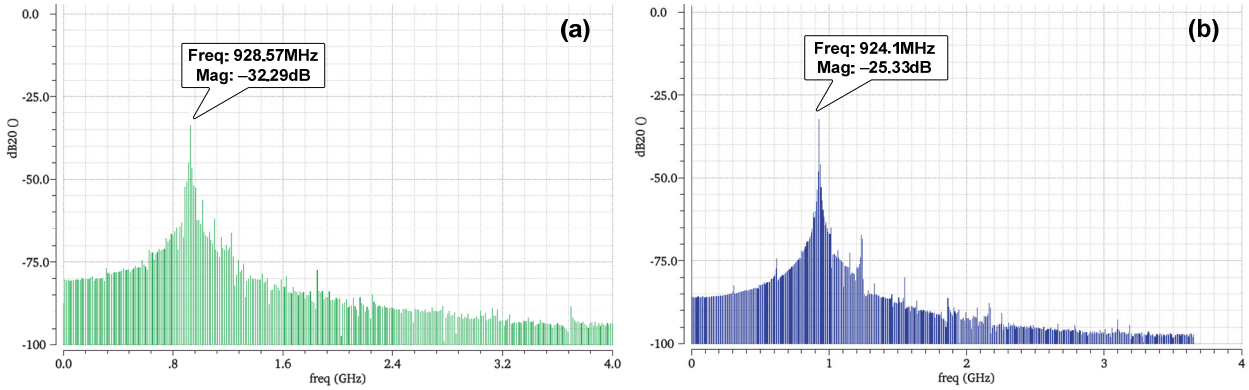

Figure 4.3: Power spectrum of OOK RF transmitter output: a) free-running, b) injection-locked

Table 4.1: Optimized transistor sizing of the designed OOK RF transmitter

RF Transistor Sizing	RO_2NOT		RO_1NOT		TX EC NAND3C			M_1
Nfet or Pfet	N	P	N	P	N	N	N	N
W/L (µm/µm)	$\frac{0.68}{0.54}$	$\frac{1.48}{0.54}$	$\frac{0.68}{1.25}$	$\frac{1.48}{1.25}$	$\frac{1.3}{0.12}$	$\frac{1.3}{0.12}$	$\frac{4.0}{0.12}$	$\frac{0.68}{0.12}$

(=21x44MHz). Also, as seen from the Figures 4.3 a and b, phase noise of the injection-locked transmitter output is much lower than a free-running transmitter, with less spurs around the modulation frequency center of 924MHz. The figure-of-merit (energy consumed per a transmitted data bit) of the proposed ULP OOK RF transmitter shows significant improvement over state-of-the-arts from the literature, as compared in Table 4.2.

Table 4.2: Performance summery of the proposed ULP RF transmitter vs. state-of-the-art

	[66]	[64]	[67]	[68]	[69]	**This Work**
Data Rate	120kbps	200kbps	250kbps	800kbps	1Mbps	**2.75Mbps**
Transmit Power	NA	–17dBm	–16dBm	–4dBm	–12dBm	**–22dBm**
Power Diss.	350μW	90μW	400μW	>10mW	8.9mW	**137μW**
Global Efficiency	NA	22%	6.3%	<4%	0.7%	**4.6%**
Energy per bit	2.9nJ/bit	0.45nJ/bit	1.96nJ/bit	>12nJ/bit	8.9nJ/bit	**0.05nJ/bit**
Modulation	MSK	BFSK	BFSK	BFSK	BFSK	**OOK**
Process	90nm	0.13μm	0.18μm	0.18μm	0.18μm	**0.13μm**

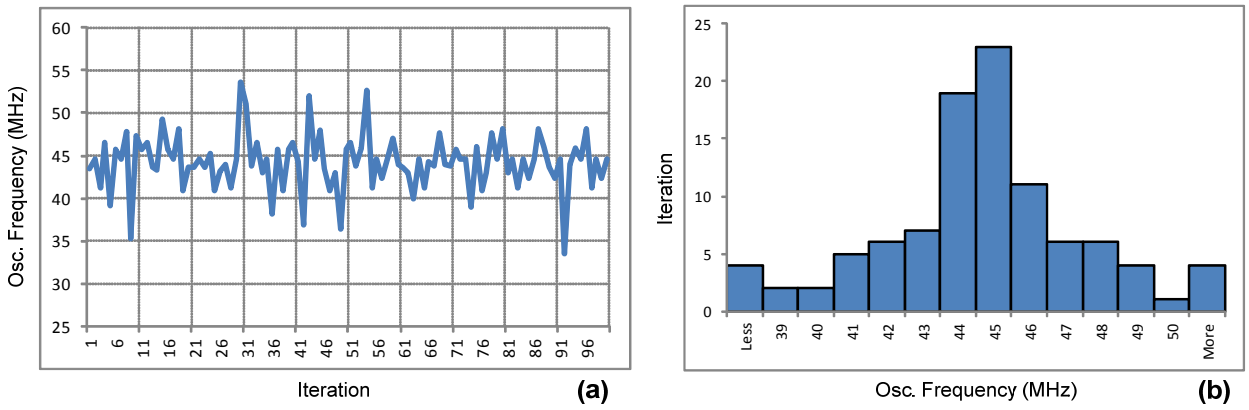

Figure 4.4: Monte-Carlo simulations: a) variations in RO_2 free-running osc. freq., b) histogram

Monte-Carlo simulations are run to check the robustness of our OOK RF transmitter design. Figure 4.4 a shows variations in free-running oscillation frequency of RO_2, by one hundred iterations. Figure 4.4 b shows a histogram of these one-hundred iterations, which is an acceptable distribution around the designed free-running oscillation frequency of 44MHz. In the process of integrated OOK RF transceiver design for this project, we considered just 25dBm of pass loss between 50-Ω antennas of sensor nodes' and the coordinator's identical transceivers. A 44MHz on-chip integrated crystal oscillator is designed to drive transmitter's frequency multiplier for a 924MHz carrier frequency. The same integrated oscillator's output is digitally buffered and divided (by 16 or 32) to generate a global system clock of 2.75MHz for the SoC. As well, we considered in the SoC design to configure SoC to be driven by an external local oscillator, from the Brain-ASNET ASIC pin ExtClk (Appendix A).

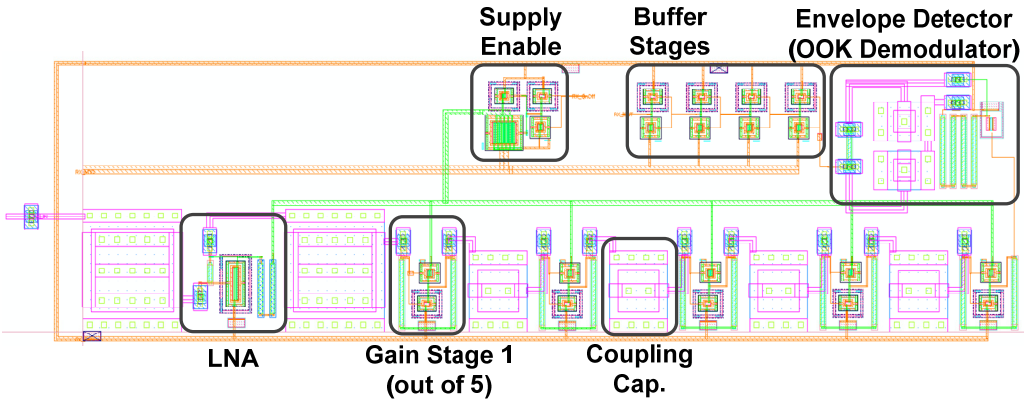

Figure 4.5: Layout design of the ULP OOK RF receiver

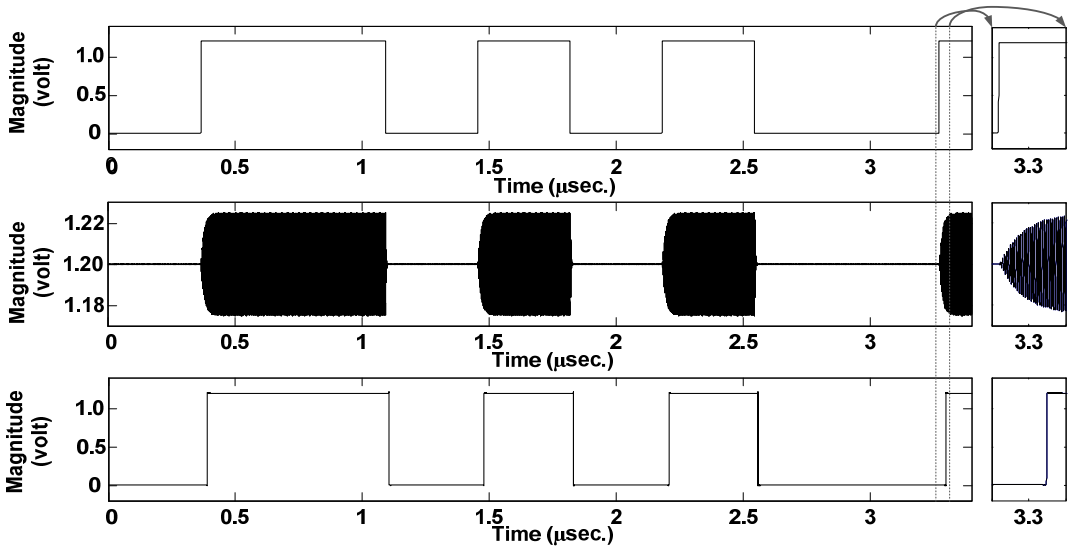

Figure 4.6: Post-layout simulation results of a sensor node's OOK RF transmitter input and antenna output, and the coordinator's OOK RF receiver output, respectively

The integrated OOK RF receiver shows has a sensitivity of –51dBm and consumes around 344µW at an input data rate of 2.75Mbps. The average power dissipation of each synchronized sensor node's receiver is as low as 62µW at 1.2V supply voltage. We implement tapped-capacitor LC matching network using off-chip components. The layout design of the OOK RF receiver is shown in Figure 4.5. Care should be taken in drawing the layout of the receiver, especially for its envelope detector [65]. Figure 4.6 shows post-layout simulation result waveforms of a given data

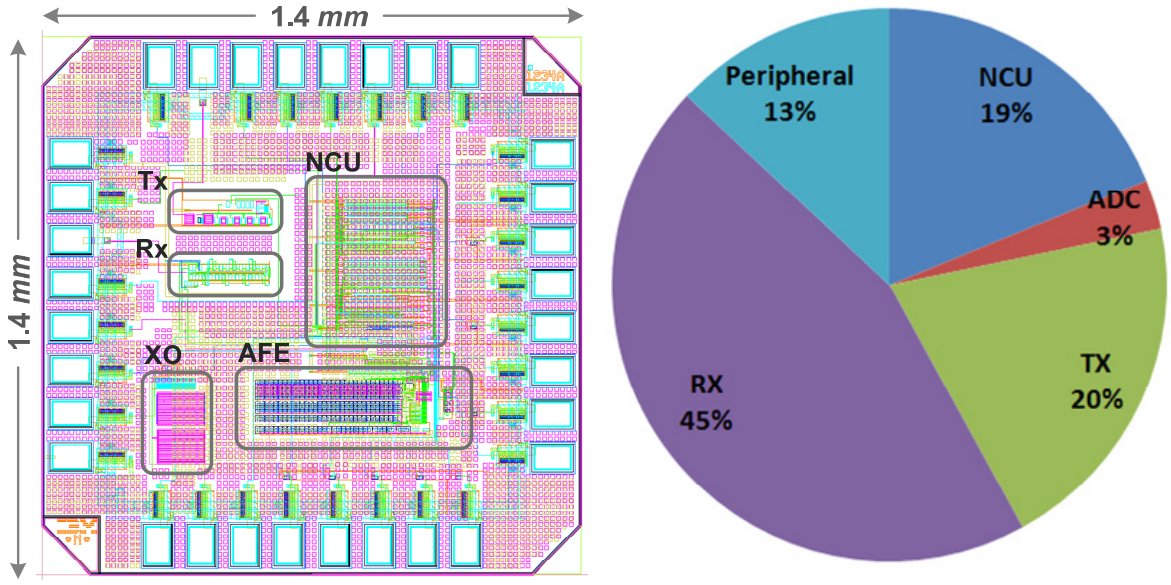

Figure 4.7: Designed Brain-ASNET ASIC: a) chip layout, and b) power consumption chart

Table 4.3: Performance summery of the designed SoC for Brain-ASNET ASIC

Chip total	Power Dissipation, as Sensor	138μW
	Power Dissipation, as Coordinator	412μW
	Die Size	1.4mm x 1.4mm
ADC	Conversion Rate	275kS/s
	Resolution	8 bits
	SNDR (100kHz input)	49.2dB (7.9b ENOB)
	Power Diss.	3.9μW
	FOM $\|P/(Fsx2^{ENOB})\|$	59fJ/conv.-step
	Power Dissipation, avg. in Sensor	0.49μW
NCU	Power Dissipation, as Sensor	26μW
	Power Dissipation, as Coordinator	87μW
Tx	Data Rate	2.75Mbps
	Transmit Power	–22dBm
	Power Diss.	137μW
	Energy per Bit	0.05nJ/bit
	Power Dissipation, avg. in Sensor	28μW
Rx	Data Rate	2.75Mbps
	Sensitivity	–51dBm (s)
	Power Diss.	344μW
	Energy per Bit	0.125nJ/bit
	Power Dissipation, avg. in Sensor	62μW

bitstream, the corresponding RF signals at the transmitter's input on the sensor node side and the receiver's output on the coordinator side.

The SoC layout design, with a silicon area of 1.4x1.4 mm^2, is shown in Figure 4.7 a. The SoC core is buried under top-three metal layers filling required for this IBM 0.13µm CMOS technology.

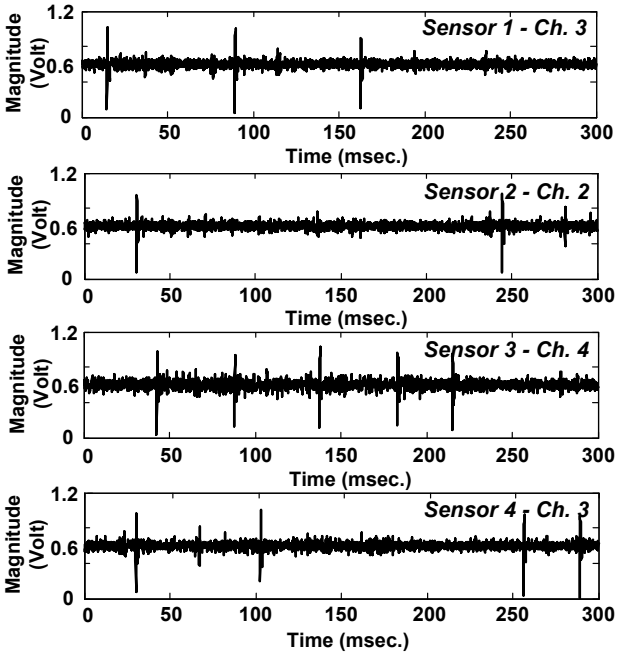

Figure 4.8: Post-layout simulation results of one selected channel of each of four sensor nodes

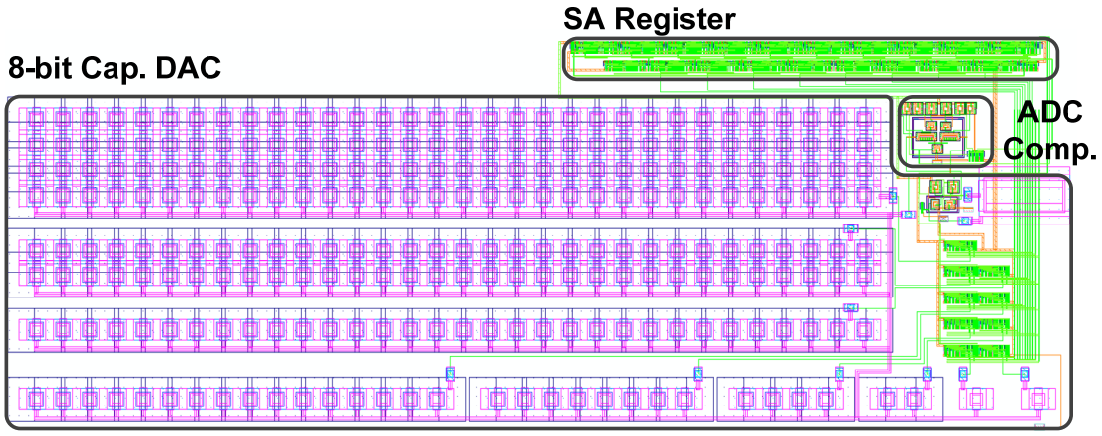

Figure 4.9: Layout design of the ULP 8-bit SAR ADC

You can refer to Appendix A for the SoC layout design, ESD pads, and, pins labels with no top-three metal filling. Figure 4.7 b shows the pie chart of power dissipation of a synchronized sensor node in the Brain-ASNET for this project. Table 4.3 represents detailed performance of the SoC design. Pre-recorded neural signals acquired from auditory cortex of a guinea pig, from the study performed by the authors in [17], were used as inputs of all four sensor nodes. Figure 4.8 shows reconstructed signals from post-layout simulation of the four sensor nodes and the coordinator (integrated RF front-end and NCU parts). Simulation results show that normalized RMS error between the input signals, sampled at ~8.7kS/s, and the reconstructed signals at the coordinator side is ~2%. The ultra-low-power 8-bit SAR ADC was fully-custom designed and laid-out, and evaluated from the post-layout simulation results. Figure 4.9 shows the layout design of the SAR ADC integrated in the SoC. The post-layout simulation results shows a good ADC performance, with a Signal-to-Noise Ratio (SNDR) of 49.2dB at 100kHz input frequency, with an Effective-Number-of-Bits (ENOB) of:

$$ENOB = \frac{SNDR(dB) - 1.76dB}{6.02dB} = 7.88bits\ , \tag{4.1}$$

where it dissipates 3.9µW power at conversion rate of 275kS/s, from a 1.2V supply. In a network synchronized sensor node, its ADC average power consumption is sub-microwatt (0.49µW).

The whole chip, including all functional and peripheral integrated components, consumes 138µW and 412µW, at 1.2V, configured in a synchronized network as a sensor node and the coordinator, respectively. Figure 4.10 compares the designed system power consumption with power

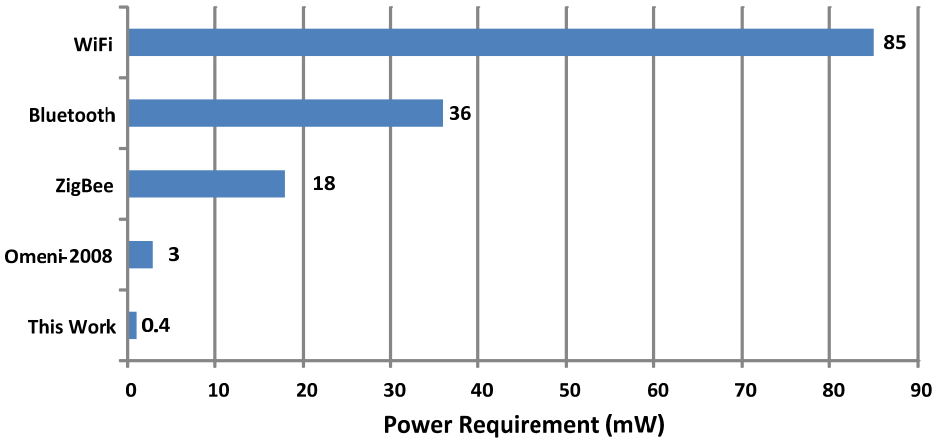

Figure 4.10: Power requirements of this work vs IEEE standards and Omeni-Toumazou's work

requirements for three main IEEE WSN standards, i.e. Wi-Fi, Bluetooth, and ZigBee, as well as highly-cited ad-hoc MAC protocol design by Omeni-Toumazou [3].

Although the comparison may not be considered so meaningful, as the RF communication range and protocol flexibility for all these protocol platforms are different, however it shows how an ad-hoc WSN protocol design can facilitate realization of a sensor network of wireless implants with restricted energy sources, like the Brain-ASNET.

4.2 Implementation and Measurement Results

Figure 4.11 show the micrograph of fabricated chip, packaged with tiny 32-pin QFN packages, available by CMC Microsystems, to minimized both unwanted long wire-boding and IC package

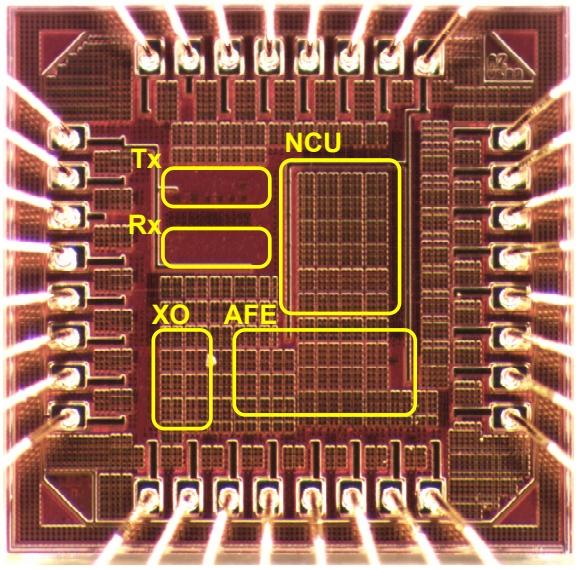

Figure 4.11: A micrograph of the fabricated Brain-ASNET ASIC

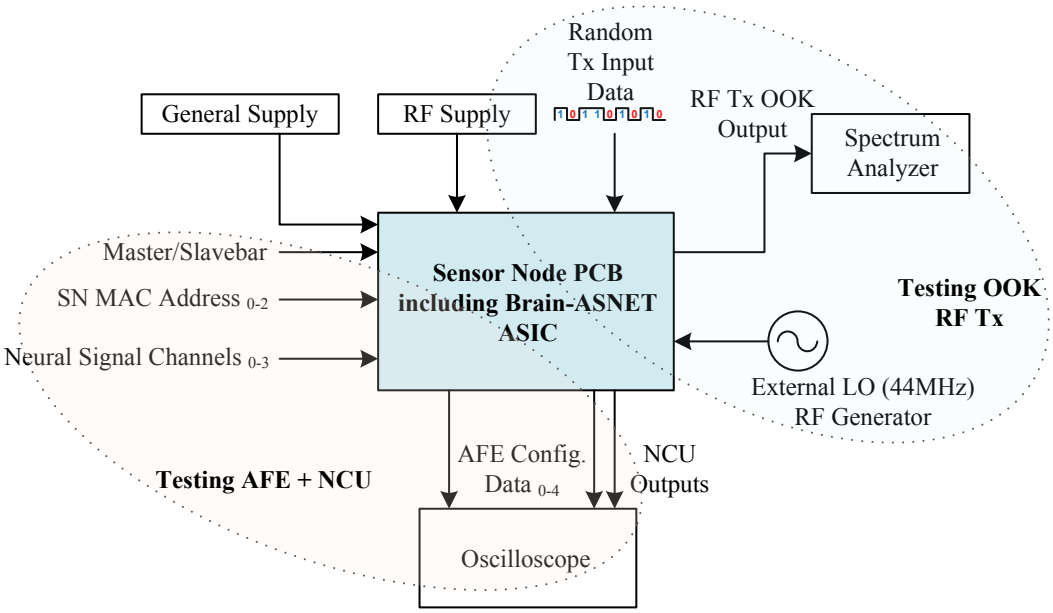

Figure 4.12: Simplified test bench setups used for Brain-ASNET sensor node measurements

pins parasitics. Each sensor node has the fabricated ASIC where all its building blocks are functioning and its NCU is configured in slave mode, plus a 44MHz surface-mounted crystal, center-tapped LC matching tank, RF 915MHz $\frac{1}{4}$–wave antennas, a tiny battery, a commercial 1.2V voltage regulator IC AAT3218IJS, and other required components.

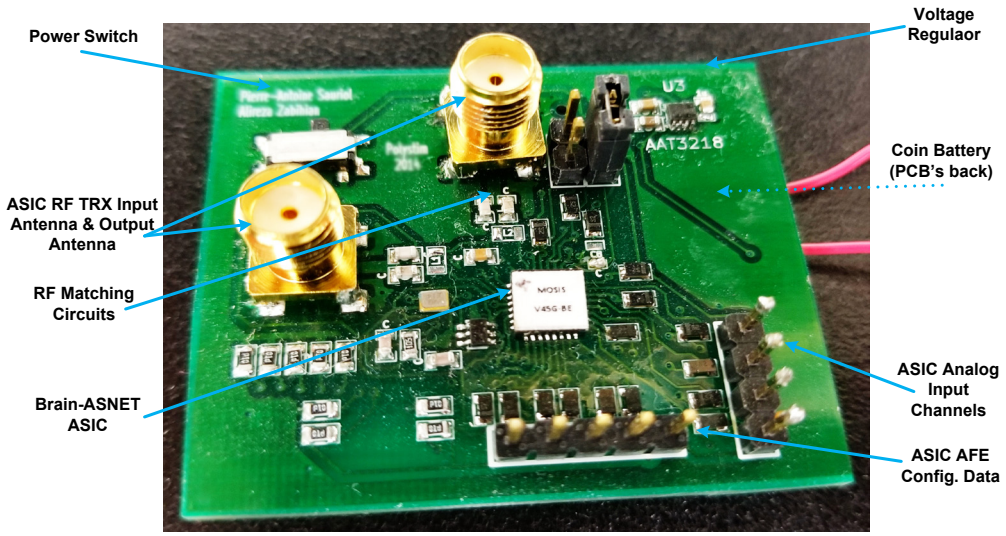

Figure 4.13: A Brain-ASNET sensor node module implemented using the fabricated ASIC

Figure 4.12 shows a simplified diagram of two main test bench setups designed and implemented for measurements of Brain-ASNET sensor nodes. One for low-frequency AFE and NCU parts of the ASIC, and the other for the OOK RF transmitter. These setups were exclusively used to measure and analyze characteristics and functions of the taped-out Brain-ASNET ASIC. Figure 4.13 depicts top side of the designed sensor node module, implemented on a compact PCB to have a preliminary implant with small form factor. This module is real hardware implementation of the core block in Figure 4.12.

The coordinator's electronics hardware and a computer user interface software using *Python* language were constructed with assistance of an undergraduate intern. The coordinator's ASIC NCU output data (consisting of the recorded signal samples along with their corresponding MAC address and configuration packets) comes out with a gated clock, DATAout and CLKout pins (Appendix A), respectively. A synchronized gated clock corresponding with the coordinator's ASIC NCU input data (consisting of configuration and MAC address packets for all the network's sensor nodes) from the computer user interface is also required. All these clock and data signals, plus USB interface controller was implemented by a 8-core microcontroller, on another module interface between the computer USB port and the wireless coordinator of the Brain-ASNET. The platform was tested successfully with different test signals.

Although different measurements were performed to test the Brain-ASNET ASIC using test benches presented in Figure 4.12, but unfortunately, test and measurements of whole Brain-ASNET (that is a wireless network of neural recording implants with expected results) were not successful as we were not able to build a synchronized network of the designed and implemented sensor nodes and the coordinator and computer interface. We investigated all possible sources of error in design and implementation of sensor node PCB and its components, and also test approaches used here. One problem was the fact that the integrated Pierce crystal oscillator did not provide the expected oscillation frequency of 44MHz, but a much lower frequency (around 100kHz). Therefore, measurements of the designed OOK RF transceiver were also not possible, as the transmitter is supplied by ×21 frequency multiplier and tuned and matched only for 902-928MHz ISM frequency band. Although we had considered an external LO to be fed to the ASIC in case the integrated crystal oscillator fails, however we did not find a proper RF signal generator, in the GRM test labs, to provide a clear pulse 44MHz clock signal. Also since this was our first IC design and tape-out experience and we had a PAD limited design, to reduce any

excise tape-out costs, we did not considered other test pad and more configurability to test the proposed OOK RF transmitter at a different frequency other than 902-928MHz ISM frequency band. The analog/mixed-mode and digital parts of the Brain-ASNET ASIC, were tested with an external 500kHz clock, using the test bench shown on the right side of Figure 4.12. The system was partially functional, providing the corresponding sensor-node specific data patterns (including SYNC pattern, fixed zero-bit stuffing at the end of each data byte, etc.), however the sensor nodes AFE-NCU parts were not able to get synchronized with the coordinator NCU and PC interface. As mentioned earlier, since we did not considered test pads for the first tapeout, it was not possible to separately test and characterize the AFE building blocks including analog MUX and SAR ADC. However, this Master's project IC design, tapeout and measurement of a large SoC was a good experience for this student to understand having broken-down design considering test pads is essential for an academic project to be able to better study a large SoC design were analog/mixed-mode, digital, and RF building blocks are compactly integrated.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

In this Master's thesis we presented the proposed general idea of Brain-ASNET, the architecture, system and circuit design of a preliminary development of Brain-ASNET idea along with partial implementation efforts done. Here we review the contributions of our research work and suggest some directions for future work towards an ultimate development of Brain-ASNET. The research works on Brain-ASNET using the proposed energy-efficient ad-hoc network protocol along with design and post-layout simulation results of a SoC as Brain-ASNET sensor node and coordinator ASIC laid-out in an IBM 0.13µm CMOS technology was presented at the IEEE Conference of Neural Engineering [70].

5.1 Summary and Discussion

In the first part of this thesis, we talked about our proposed general idea of Brain-ASNET as a novel neural interfacing method that has some great advantages over conventional neural interfacing methods like EEG, ECoG, and Single-Unit Intracortical Neural Recording. We claimed that the proposed neural interfacing approach provides better recorded signal quality, quantity, and speed, is less invasive than ECoG, and allows free movement of patient where is not possible in EEG and ECoG methods because of surgery and/or connecting wires. A few different network topologies for Brain-ASNETs with recording sensor nodes and/or stimulation actuator nodes were also discussed.

To implement a preliminary version of the Brain-ASNET for this Master's, we gave detailed information on the architecture, system and circuit design and implementation aspects such a WSN. Best design options were analytical chosen, including network topology, MAC, LLC, modulation for wireless communication, frequency band of transmission channel, etc. In section 3.1, we presented the system and circuit design of an ultra-low-power low-voltage SoC that can be configured to be used as ASIC for the Brain-ASNET implantable sensor nodes or as the network coordinator’s dedicated RF front-end and corresponding network controller.

Our proposed energy-efficient ad-hoc network protocol, named modified HDLC, was presented in details in the section 3.2. It was designed and tested by *MATLAB* and *Simulink*, and shows better energy-efficiency compared to standard protocols like ZigBee, Bluetooth, and Wi-Fi as well as state-of-the-art ad-hoc protocols.

Having chosen On-Off Keying (OOK) modulation on an Industrial, Scientific and Medical (ISM) frequency band of 902-928MHz as the best option for our application requirements, we introduced the architecture and circuit design of a novel ULP OOK RF transmitter that employs an OOK multi-stage multi-phase injection-locked ring oscillator. Analytical circuit design and physical layout were presented in the section 3.3 and the chapter 4. In comparison with state-of-the-art, the proposed ULP RF transmitter designed and integrated in the Brain-ASNET SoC provides high data rate (up to 20 Mbps) at a high power efficiency, at a small silicon area. For our design, the ULP OOK RF transmitter has an output transmit power of –22dBm and dissipates 137μW of power at a date rate of 2.75Mbps at 1.2V supply voltage. When synchronized in the Brain-ASNET of four sensor nodes and the coordinator, the average power dissipation of the sensor node's transmitter is as low as 28μW.

The coordinator's electronics hardware and a computer user interface software using Python language are constructed with assistance of an undergraduate intern. The platform was tested successfully with different test signals. The fabricated chip was measured and its RF transmitter and receiver were separately tested. However, because the fabricated chip was not whole functional, we could not tested it as Brain-ASNET sensors in connection with the coordinator and GUI platform.

5.2 Directions for Future Work

The suggestions listed below can be considered for further research on Brain-ASNET project towards next development phases.

- Since there is no need for PLL-DLLs in the architecture of the OOK RF transmitter, its global power efficiency is high between state-of-the-art. However, because of the current design for Edge- Combining Power Amplifier (EC-PA) circuit, where the output is combined of 21 inverters of the second stage injection-locked ring oscillator, cannot provide a higher transmit output power. Analysis on the nature of maximum current drive capacity of the current EC-PA design should be done; and studying different power amplifier classes, a novel EC-PA design can be presented to provide a much higher output power for this OOK RF transmitter.

- Because the maximum data rate of a communication link consisting of this transmitter depends on the nature of ON-OFF Keying transitions speed and corresponding receiver sensitivity and acceptable BER, one can do research on how to reduce the rise and fall times of oscillation in the proposed RF transmitter design. The rise and fall times mainly depend on the amount of inductor and capacitors of the matching network. Because of IC pad and PCB parasitic loadings and the high frequency of oscillation (924MHz in our application), it is not possible to choose any value for the L and C.
- Other network topology and sensor/actuator options, like Recording-and-Simulation Distributed Brain-ASNET, as suggested in section 2.1.1 can be considered for next development phases of Brain-ASNET project.
- As briefly discussed in the section 3.1.1, to increase the number of neural recording channels for each sensor node implant to a practical number, that depends what the current research demands, we should consider integrating an on-chip data compressor unit, with the best design, to the sensor node SoC design.
- For this project, we considered a symmetric wireless communication link having a single RF transceiver design on the ASIC that is similarly functioned for sensor node and the coordinator. Considering severe energy-source restriction in practical design of intracortical neural recording implants, here we suggest designing an asymmetric wireless communication link for the Brain-ASNET's PHY layer between the coordinator and implantable sensor nodes for the next development phase of Brain-ASNET project, as discussed in section 3.1.2. Therefore, an ultra-low-power low-performance relaxed RF transceiver design for the sensor nodes' ASIC, and a high-performance complex RF transceiver design for the coordinator's ASIC are required, that both can be integrated on the same SoC along with other building blocks, as considered in configurable SoC design for this Master's project.
- We did not consider any error correction feature in the DLL layer of the proposed ad-hoc network protocol, but CRC-8 based error detection, that would be enough for the first development phase of Brain-ASNET as mentioned in section 3.2. Therefore, one can add a proper error correction feature in the DLL layer of the proposed modified-HDLC

protocol to make it more general purpose, to use it in WSNs where an error-free correct data transmission is crucial, like computer networks.

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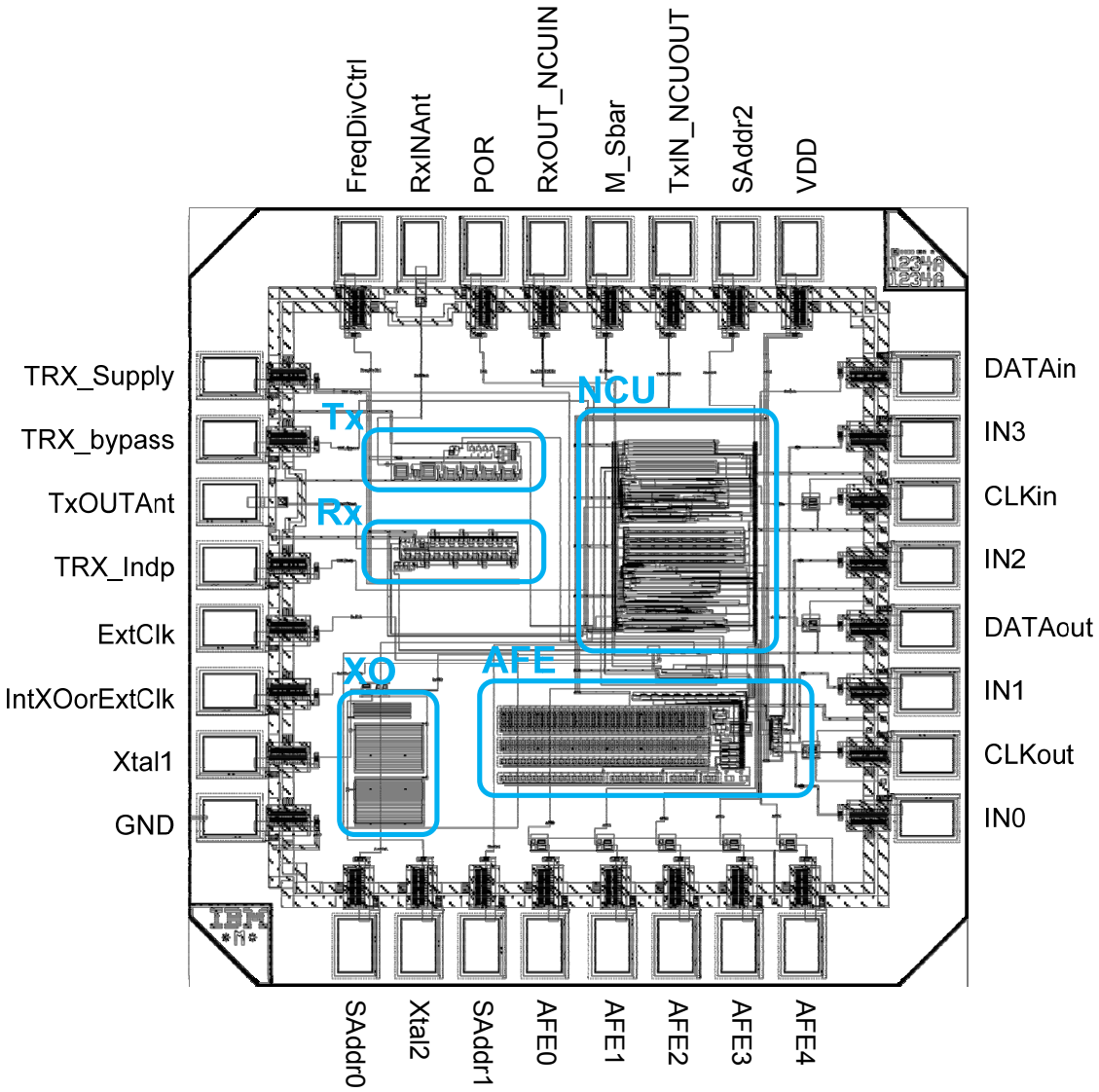
APPENDIX A – BRAIN-ASNET ASIC PIN CONFIGURATION

The pin configuration for the designed sensor-coordinator Brain-ASNET ASIC, along with the chip layout (without three-top-layer metal filling in IBM 0.13µm) is depicted below.



Pin #	Port	Function
1	TRX_Supply	RF transceiver VDD supply
2	TRX_bypass	“1”: transceiver is bypassed, “0”: transceiver is not bypassed
3	TxOutAnt	RF transmitter output connection to antenna
4	TRX_Indp	“1”: transceiver is separated, “0”: transceiver is connected to NCU
5	EXT_Clk	External system clock

6	IntXOorExtClk	“1”: internal Xtal osc. clock is used, “0”: external clock is used
7	Xtal1	External crystal-to-chip pin 1 connection
8	GND	General ground
9	SAddr0	Sensor node MAC address bit0
10	Xtal2	External crystal-to-chip pin 2 connection
11	SAddr1	Sensor node MAC address bit2
12	AFE0	Analog front-end Amp-BPF configuration bit0
13	AFE1	Analog front-end Amp-BPF configuration bit1
14	AFE2	Analog front-end Amp-BPF configuration bit2
15	AFE3	Analog front-end Amp-BPF configuration bit3
16	AFE4	Analog front-end Amp-BPF configuration bit4
17	IN0	Neural recording analog channel0
18	CLKout	NCU gated output clock, when Brain-ASNET chip set as
19	IN1	Neural recording analog channel1
20	DATAout	NCU gated output data, when Brain-ASNET chip set as coordinator
21	IN2	Neural recording analog channel2
22	CLKin	NCU gated input clock, when Brain-ASNET chip set as coordinator
23	IN3	Neural recording analog channel3
24	DATAin	NCU gated input data, when Brain-ASNET chip set as coordinator
25	VDD	General VDD supply
26	SAddr2	Sensor node MAC address bit2
27	TxIN_NCUOUT	“1”: transmitter input (TX separated), “0”: NCU output (for test)
28	M_Sbar	“1”: ASIC set as coordinator, “0”: ASIC set as sensor node (slave)
29	RxOUT_NCUIN	“1”: receiver output (RX separated), “0”: NCU input (for test)
30	POR	Power on reset
31	RxINAnt	RF receiver input connection to antenna
32	FreqDivCtrl	“1”: freq div. = 32 (clk=1.375MHz), “0”: freq div. = 16 (clk=2.75MHz)