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ELECTROLYTE GATED METAL OXIDE TRANSISTORS

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RÉSUMÉ

L'invention du transistor a significativement affectée le progrès technique et scientifique de notre société. Depuis plus de 50 ans, les transistors sont utilisés comme composants actifs dans les circuits électroniques, pour réaliser des amplificateurs ou des interrupteurs par exemple. La plus fascinante des directions futures pour le développement des transistors consiste en leur utilisation dans des dispositifs électroniques flexibles, légers et biocompatibles.

Les oxydes métalliques semi-conducteurs ont été intensivement étudiés au cours des dernières décennies pour des applications dans les transistors, du fait de la grande mobilité de leurs porteurs de charges (~1– 100 $cm^2V^{-1}s^{-1}$), de leur importante transparence optique, de leur stabilité chimique ainsi que de leur faible coût de fabrication. Les oxydes métalliques sont divisés entre les oxydes de transition et ceux post-transition, dépendamment des métaux, qui possèdent différentes configurations électroniques et donc différentes conductivités.

Dans cette thèse, nous allons nous concentrer sur les deux principaux représentants des oxydes métalliques de transition et post-transition, i.e., le TiO_2 et le SnO_2, utilisés comme matériaux de canal dans des transistors utilisant un électrolyte comme diélectrique à la grille. Le TiO_2 et le SnO_2 sont abondants et biointégrables, possèdent une large bande interdite (3-4 eV), et peuvent être utilisés comme canal de transistor pour de nombreuses applications différentes.

Remplacer le diélectrique conventionnel dans les transistors à couche minces par un électrolyte donne l'opportunité de décroître le voltage auquel le transistor est opéré du fait de la haute capacitance de la double couche électrique (autour de 10 $\mu F/cm^2$) qui se forme à l'interface entre l'électrolyte et le semi-conducteur. Cette capacitance élevée permet l'accumulation d'une importante densité de porteurs de charges dans le canal et rend donc possible la transition entre un état isolant et un état semi-conducteur voire métallique. Les transistors utilisant un électrolyte comme diélectrique à la grille (EGTs) peuvent être employés comme éléments de matrice active pour les écrans à faible puissance ou encore intégrés dans des textiles ou d'autres matériaux flexibles. Les EGTs peuvent aussi être utilisés dans d'autres applications prometteuses que sont telles les capteurs chimiques ou biologiques, du fait de leur haute sensibilité aux ions et de leur compatibilité avec les électrolytes aqueux.

Le cœur de cette thèse est dévoué à une meilleure compréhension des mécanismes d'opération d'une importante classe de transistors à couche minces, i.e. les transistors à oxydes métalliques

utilisant un électrolyte comme diélectrique à la grille, afin d'optimiser leurs performances et de développer des agencements géométriques pour permettre d'obtenir des transistors à haute performance. Les EGTs consistent en un canal en oxyde métallique et en une électrode de grille en contact avec un électrolyte. L'application d'un voltage à la grille entraîne la formation d'une double couche électrique au niveau de l'interface entre le canal et l'électrolyte, qui permet de moduler la densité des porteurs de charges dans le canal. Les mécanismes de dopage et la modulation de la densité des porteurs de charges dans les EGTs ont été étudiés par caractérisation électrique des transistors, par voltammétrie cyclique (CV) ainsi que par spectroscopie d'impédance électrochimique.

Des transistors SnO_2 et TiO_2 utilisant des liquides ioniques à la grille ont été fabriqués sur des substrats en silicone. Une méthode de gravure non conventionnelle utilisant le parylène a été utilisée pour étudier le rôle joué par l'extension des interfaces électrolyte/semi-conducteur et électrode/semi-conducteur sur le dopage ainsi que sur les processus de transport des porteurs de charges. Le chevauchement entre les électrodes métalliques et le semi-conducteur, qui est en contact avec l'électrolyte, affecte le processus d'injection des charges. La gravure a entraîné l'augmentation de la densité des porteurs de charges d'un à deux ordres de magnitude dans les deux oxydes métalliques. De plus, les EGTs à SnO_2 ont été fabriqués sur des substrats flexibles en polyimide. Les transistors EGTs à SnO_2 flexibles possèdent de bonnes propriétés électriques lorsqu'ils sont pliés selon différents rayons de courbure et ils pourraient posséder un fort potentiel pour des applications dans le domaine de l'électronique flexible.

Les effets de la structure et de la morphologie des semi-conducteurs sur les performances des transistors ont été étudiés. Dans ce but, des films de TiO_2 poreux à très forte densité ont été fabriqués par traitement à partir d'une solution ainsi que par évaporation par faisceau d'électrons. Les EGTs à TiO_2 faits par évaporation possédaient un courant plus élevé ainsi qu'un ratio on/off plus haut du fait d'une meilleure qualité de la structure. Les effets des gros cations [EMIM] et des petits cations Li^+ sur les mécanismes de dopage ont été étudiés en utilisant deux électrolytes [EMIM][TFSI] et [EMIM][TFSI] mélangé avec un sel de lithium. Les relativement gros cations [EMIM] ne peuvent pas pénétrer à l'intérieur du maillage cristallin du TiO_2. L'intercalation de petits cations comme le Li+ a été rendue possible à la fois dans les films denses et dans les films mésoporeux de TiO_2 par réduction de la vitesse de balayage dans les mesures courant/voltage.

Les mécanismes de transport des charges des transistors utilisant un électrolyte comme diélectrique à la grille ont été étudiés et une corrélation entre la capacitance de la double couche, la densité des porteurs de charges, la mobilité des électrons, la tension seuil et le ratio on/off a été démontrée. Nous pensons que nos transistors à oxydes métalliques utilisant un électrolyte comme diélectrique à la grille sont prometteurs pour de l'électronique flexible, produite sur de grandes surfaces et à faible coût.

ABSTRACT

The invention of the transistor has significantly affected the technological and scientific progress of our society. For over 50 years, transistors have been used as the active components, such as amplifiers or switches, in electronic circuits. The most fascinating future direction for transistor development is towards flexible, lightweight and biocompatible electronics.

Metal oxide semiconductors have been intensively investigated over the past decades for transistor applications, due to their high charge carrier mobility (~1– 100 $cm^2V^{-1}s^{-1}$), high optical transparency, chemical stability and low-manufacturing cost. Metal oxides are divided into transition and post transition oxides, depending on the metals, which possess different electron configurations and, accordingly, different conductivity.

In this Thesis we focus on two main representatives of transition and post transition metal oxides, i.e., TiO_2 and SnO_2, as the channel materials in electrolyte gated transistors. TiO_2 and SnO_2 are abundant and bio friendly, with high band gap (3-4 eV) and can be utilized as transistor channel for many different applications.

Replacing the conventional dielectric in thin film transistors with electrolyte gives the opportunity to decrease the transistor operating voltage due to the high capacitance of the electrical double layer (around 10 $\mu F/cm^2$) that form at the electrolyte/semiconductor interface. This high capacitance allows accumulation of high charge carrier density in the channel thus making possible a transition from an insulating state to semiconducting or metallic one. Electrolyte gated transistors (EGTs) can be utilized as backplanes for low powered displays and integrated into textiles or flexible materials. Other exciting applications of EGTs are chemical sensors or biosensors, due to the high sensitivity to ions and compatibility with aqueous electrolytes.

The core of this thesis is devoted to a better understanding of the operational mechanisms of an important class of thin film transistors, i.e. electrolyte gated metal oxide transistors, to optimize their performance and to develop the appropriate device geometry for high performance transistors. EGTs consist of metal oxide channel and a gate electrode in contact with an electrolyte. The application of a gate electrical bias leads to the formation of an electrical double layer at the channel/electrolyte interface, which permits to modulate the charge carrier density in

the channel. The doping mechanisms and the charge carrier density modulation in EGTs were investigated by transistor electrical characterization, cyclic voltammetry (CV) and electrochemical impedance spectroscopy.

Ionic liquid gated SnO_2 and TiO_2 transistors were fabricated on silicon substrates. Parylene patterning was utilized to investigate the role played by the extension of the electrolyte/semiconductor and electrode/semiconductor interfaces on the doping and charge carrier transport processes. The overlap between the metal electrodes and the semiconductor, which is in contact with the electrolyte, affects the charge injection process. By patterning the charge carrier density was increased on one or two order of magnitude in both metal oxide materials. Moreover, SnO_2 EGTs were fabricated on flexible polyimide substrate. EGT SnO_2 flexible transistors possessed good electrical properties under bending at different radius and could have high potential in flexible electronics.

The effect of structure and morphology of semiconductors on transistor performance was demonstrated. For this purpose, porous and highly dense films of TiO_2 were fabricated by solution processing and by electron beam evaporation. Evaporated TiO_2 EGT showed higher current and higher on/off ratio due to better structural quality. The effect of big [EMIM] and small Li^+ cation on doping mechanisms was investigated by using two electrolytes [EMIM][TFSI] and [EMIM][TFSI] mixed with a lithium salt. The relatively large [EMIM] cation cannot enter the crystal lattice of TiO_2. The intercalation of small cation such as Li^+ was possible both in mesoporous and dense TiO_2 films by decreasing the sweeping rate in current / voltage measurements.

The charge transport mechanism of electrolyte gated transistors was investigated and a correlation between capacitance of the double layer, charge carrier density, electron mobility, threshold voltage and on/off ratio was demonstrated. We believe that our electrolyte gated metal oxide transistors are promising for low cost, flexible and large area electronics.

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LIST OF SYMBOLS AND ABBREVIATIONS

a-GSZO	Amorphous gallium tin zinc oxide
a-HfO_2	Amorphous hafnium oxide
Ag	Silver
AIZO	Aluminum indium zinc oxide
Al_2O_3	Aluminium oxide
ALD	Atomic layer deposition
Au	Gold
AZO	Aluminum zinc oxide
BC-BG	Bottom contacts - bottom gate
BC-TG	Bottom contacts - top gate
BJT	Bipolar junction transistor
C	Capacitance
C gate medium	Cpecific capacitance of dielectric
CB	Conduction band
CdS	Cadmium sulphide
C_{ov}	Overlap capacitance
CV	Cyclic voltammetry
[DEME]-[TFSI] (trifluoromethylsulfonyl)-imide	N,N-diethyl- N-(2-methoxyethyl)- N-methylammoniumbis-
D	Drain electrode
d	Thickness of the insulator
[EMIM][TFSI] bis(trifluoromethylsulfonyl)imide	1-ethyl-3-methylimidazolium

E_g	Band-gap energy
EGT	Electrolyte gated transistors
$E_x(x)$	Electric field
FET	Field effect transistor
f_t	Transit frequency
G	Gate electrode
Ga	Gallium
g_m	Transconductance
HRTEM	high resolution transmission electron microscopy
I_d	Drain current
I_{dsat}	Saturation drain current
IGZO	Gallium tin zinc oxide
I_{off}	Current in off state of transistor
I_{on}	Current in on state of transistor
ITO	Indium tin oxide
IZO	Indium zinc oxide
k	Boltzmann constant
L	Channel length
Li	Lithium
$L_{overlap}$	Width of overlapping electrodes
MeO	Metal oxide
MOCVD	Metal oxide chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field-effect
MPa	Mega pascal

NaOH	Sodium hydroxide
N_t	Total trap density
PANI	Polyaniline
PBS	Phosphate-buffered saline
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene):polystyrenesulfonate
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PI	Polyimide
Pt	Platinum
PVA	Poly(vinyl alcohol)
q	Elementary charge
Q	Mobile charges
R_c	Contact resistance
S	Source electrode
S_3N_4	Trisulfur tetranitride
Sb	Antimony
SnO_2	Tin dioxide
Ta_2O_5	Tantalum pentoxide
TC-BG	Top contacts - bottom gate
TC-TG	Top contacts - top gate
TFT	Thin film transistor
Ti	Titanium
TiO_2	Titanium dioxide
VB	Valence band

V_d	Drain voltage
V_{eff}	Effective voltage
V_g	Gate voltage
V_{th}	Threshold voltage
W	Channel width
WO_3	Tungsten trioxide
WO_4	Orthotungstate
$W_{overlap}$	Length of overlapping electrodes
Y_2O_3	Yttrium oxide
$Zn(OAc)_2$	Zinc acetate
$Zn(OH)_2$	Aqueous ammonia
Zn_2^+	Zinc ion
ZnO	Zinc oxide
ZnO:Li	Lithium - doped zinc oxide
$ZnO•xH_2O$	ZnO hydrate
ZrO_2	Zirconium dioxide
ZrO_x	Zirconium oxide
ZTO	Zinc tin oxide
ε	Vacuum permittivity
ε_s	Permittivity of semiconductor
μ	Charge carrier mobility

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CHAPTER 1 INTRODUCTION

The objectives of this chapter are to give a brief overview of transistor technology as well as the structure and the working principle of thin film transistors (TFT). In particular, I will discuss metal oxides used in this work as semiconductor materials and electrolyte gating principles.

1.1 History of transistors

The first reported transistors were based on field effect. In 1925, the Austro-Hungarian physicist Julius Edgar Lilienfeld patented the operating principles of field effect transistors (FET).[1] The first field effect transistor was patented in 1934 by the German Physicist Oscar Hale.[2] In 1959 scientists from Bell Labs manufactured a metal-oxide-semiconductor field-effect transistor (MOSFET). The first MOSFETs were commercialized in 1963.[3]

Meanwhile, in 1947, the Bell Labs scientists John Bardeen, William Shockley and Walter Brattain invented the point contact transistor, one of the type of bipolar junction transistor (BJT).[4, 5] By means of a simple device, consisting of a paper clip, a small amount of germanium and golden foil, they could amplify an input current by 100 times. In the point contact transistor the low current input terminal is emitter and amplified current output is between base and collector. In 1951 they invented bipolar junction transistor, which is used up till now. In this transistor, the input terminal is base and the amplified current is collected between emitter and collector. In 1956 they were awarded the Nobel Prize in Physics for their “researches on semiconductors and their discovery of the transistor effect”.[6] In 1954, J. Bardeen and W. H. Brattain reported that gaseous ionic species adsorbed on germanium surface causes a change in the surface dipole and hence the conductivity of the germanium, leading to the development of gas sensors.[7] In 1955, their experiment was extended by to the surface of germanium electrodes in contact with aqueous electrolytes. This experiment is often considered as the first example of electrolyte gating.[8]

Early transistors were connected as individual components to other elements like resistors, diodes, capacitors and others on the board to make a circuit. In 1958, to make these circuits boards faster, Jack Kilby proposed the idea that all circuit components can be formed on one semiconductor crystal adding only the interconnections. Later, he fabricated two transistors on

the same silicon crystal leading to the first integrated circuit. Nowadays, it is possible to fit more than a billion transistors on a single crystal. Jack Kilby was awarded the Nobel Prize in Physics for the invention of the integrated circuit in 2000.[6]

The first thin film FET was developed in the RCA laboratory by Weimer in 1961. Polycrystalline cadmium sulphide (CdS) was the material used for the semiconducting thin-film and silicon monoxide, SiO, was the insulator.[9] In 1964, the first metal oxide (MeO) TFT, using evaporated SnO_2 as the semiconductor, was introduced by Klasens.[10] Later, TFTs with SnO_2 deposited by vapor phase reactions were introduced in 1970 by Aoki.[11] Single crystal lithium- doped zinc oxide (ZnO:Li) TFTs hydrothermally grown from solution had a very good electrical properties, such as hall mobility 220 cm^2/Vs.[12]

With the invention of a transistor the techno-science progress was spinned with a new force. In the 1950s the first transistor radio was produced. In 1960, the first fully transistorized portable television appeared. In 1971, the first pocket calculator was fabricated. In 1983, after the invention of the mobile phone, the era of mobile communication began. Today, transistors are facing an explosive evolution towards the light weight, flexible, stretchable and biocompatible electronics for many applications, such as wearable and textile integrated systems [13-17], flexible and rollable displays [18, 19], medical implants [20] and artificial skin [21, 22] among others.

1.2 Thin film transistors

A thin film transistor (TFT) is a transistor where metal contacts and semiconductor material are deposited as thin films. The semiconductor film is separated from the gate electrode (G) by an electrically insulating dielectric. Source (S) and drain (D) electrodes, of given channel width (W) and length (L), inject charges into the semiconductor. TFTs can use several semiconductor materials, such as silicon, compound semiconductors, carbon nanotubes, metal oxides or organic semiconductors.[23-29]

The working principles of TFTs, their characteristics and components will be described below. All transistors components have an influence on the transistor characteristics and should be optimized for different applications.

1.2.1 Working principle of thin film transistors

Figure 1.1 represents the working mechanism of a thin film field effect transistor. A gate electrode, insulator and semiconductor form a capacitor. By applying, for example, a positive voltage, V_g, to the gate, while the source electrode is grounded, negative charge carriers start to accumulate in the channel. When the gate-source voltage exceeds the threshold voltage ($V_g > V_{th}$) the channel becomes conductive.

If a voltage is applied between the drain and the source (V_d), a current starts to flow between the two electrodes (drain-source current, I_d). By gradually increasing V_d, the source-drain current increases till reaching a saturation point, this region is called a linear region due to linear increase of current. When V_d exceeds the effective gate voltage, V_{eff} ($V_d > V_g - V_{th}$), the gate potential gets compensated by the drain potential and the channel is pinched off at the drain. This means that the transistor reaches the saturation regime, where further increase in V_d does not affect I_{dsat}.

Further increase of the V_d will only move the pinch off point closer to the source, thus shortening the channel length. The current will still be flowing from the drain to the source but will not increase, since the depletion region near the drain is lacking the majority charge carriers. The current will be sustained by the carriers injected directly from the electrode. The current flowing in the depletion region is called space-charge limited current and depends only on mobility and not on the charge carrier density. The gate voltage should regulate the distribution of charges within the channel. In the case of short channel devices, the drain field becomes stronger than the gate potential and the gate can not control the current in the transistor. Thus, the space-charge limited current will prevent saturation. So the channel length of transistor should be several times the thickness of dielectric.[30]

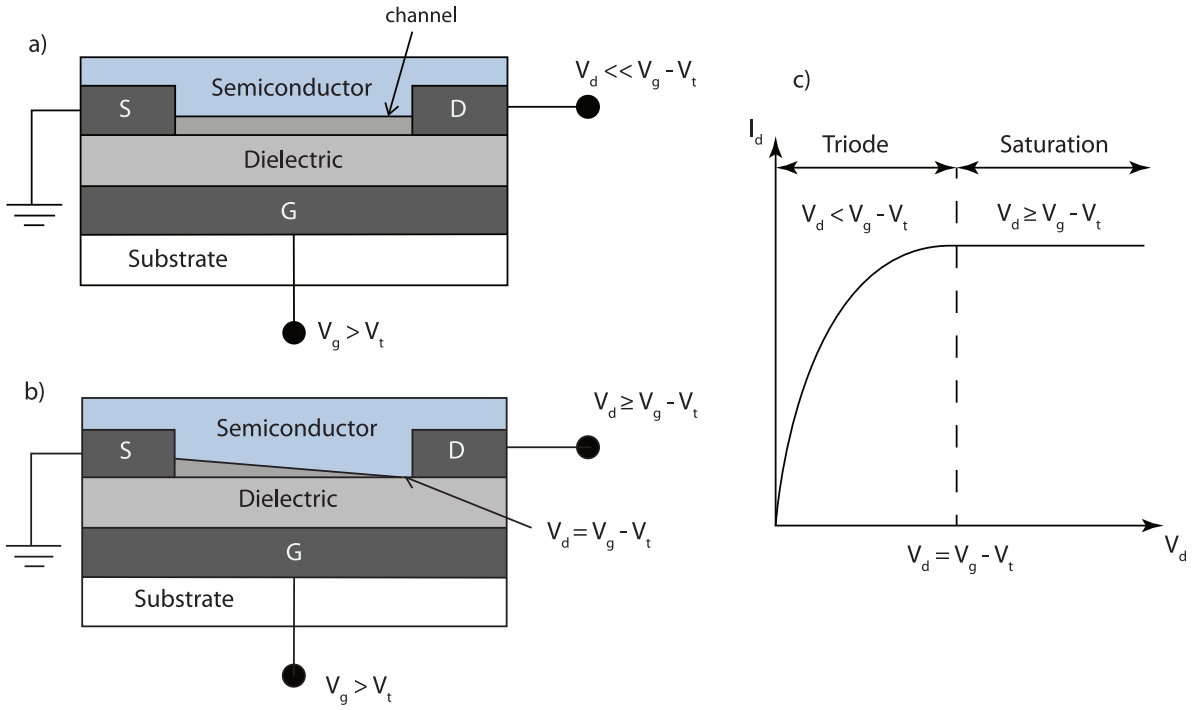

Figure 1-1: Schematic illustration of operating regimes of field effect transistors: (a) linear regime; (b) saturation regime at pinch-off; (c) corresponding current voltage characteristics.

The specific capacitance of the gate insulator is given by the formula :

$C = \frac{\varepsilon k A}{d}$, where ε is the vacuum permittivity, k is the relative permittivity (dielectric constant), A is the area and d is the thickness of the insulator.

Therefore, the mobile charge density can be calculated from the following formula:

$$Q = C(V_g - V_t).$$

This charge density is given when $V_d = 0$. As soon as the drain voltage increases, the charge density will be a function of the distance from the source. The potential will gradually increase from the source to the drain and the charge density can be given as follows:

$$Q(x) = C\left(V_g - V_t - V(x)\right).$$

We can then derive the general formula for the drain current:

$I_d = W\mu Q(x)E_x(x)$, where $E_x(x)$ is an electric field in the direction of x.

Substituting $E_x(x) = \frac{dV(x)}{dx}$ and Q(x) into this formula and integrating over x we get the following relationship:

$$I_d = \frac{W\mu C}{L}\left((V_g - V_t)V_d - \frac{V_d^2}{2}\right).$$

Knowing that in the linear mode $V_d << V_g\text{-}V_t$ and in the saturation mode $V_d = V_g\text{-}V_t$ the above equation can be simplified to the following:

Linear: $I_d = \frac{W\mu C}{L}(V_g - V_t)V_d$,

Saturation: $I_d = \frac{W\mu C}{2L}(V_g - V_t)^2$.

1.2.2 Main characteristics of thin film transistors

The charge carrier mobility describes the efficiency of the charge carrier transport, i.e. how fast carriers can travel through the semiconductor. This parameter can be derived from I_d in the linear and saturation regimes. The charge carrier mobility values in saturation regime tell us about the efficiency of charge carrier transport when channel is formed, while in linear regime channel can be still in formation process. If contacts are ohmic the charge carrier mobility in linear and saturation regimes should be quite similar due to the same amount of charges in both regimes.

Linear : $\mu_{lin} = \frac{L}{WCV_d}\frac{dI_d}{dV_g}$.

Saturation : $\mu_{sat} = \frac{2L}{WC}\left(\frac{d\sqrt{I_{dsat}}}{dV_g}\right)^2$.

The charge carrier mobility in TFT configuration is usually different from intrinsic mobility, which is typically determined by the Hall effect in the bulk material. Charge transport in TFTs occurs in a narrow channel region close to the gate dielectric/semiconductor interface, where different sources of scattering are taking place, such as Coulomb scattering from dielectric charges, surface roughness scattering and others.[31]

The channel current on/off ratio (I_{on}/I_{off} ratio) is the ratio between the channel current in the on state and the current in the off state of the transistor, which is typically extracted from the transfer curves. The off current increases the static power consumption, so minimizing it is important.

Transistors can operate in enhancement (accumulation) or depletion mode. In absence of an applied V_g, enhancement mode transistors are in the off state ($I_d \approx 0$), while depletion mode transistors are in the on state ($I_d \neq 0$) and application of a V_g is needed to turn them off. Enhancement mode transistors decrease the free-running power consumption and are thus preferred for applications in circuits and display technology.

Another important parameter of TFTs is the threshold voltage (V_{th}), i.e. the minimum gate voltage required for a drain source current to flow when the transistor channel is formed. The V_{th} depends on the semiconductor material as well as the type of dielectric, their interface, defect states, impurities and device geometry. [Veres, 2004] The most common methods to determine V_{th} is linear extrapolation from I_d versus V_g curves at low V_d (transfer curves in liner regime) or linear extrapolation from $\sqrt{I_d}$ vs V_g curves at high V_d (transfer curves in saturation regime). When a n type transistor operates in the enhancement mode, V_{th} is positive, and negative in depletion mode of operation. Increasing the gate capacitance can reduce the threshold voltage. At higher capacitance more charges are induced in the channel making it conductive at lower voltages.

The transconductance, g_m, describes how the drain current is modulated by the gate voltage, and it is defined as:

$$\left[g_m = \frac{\partial I_d}{\partial V_g}\right]_{V_d}$$

The transconductance describes the behavior of the transistor at gate voltages above the threshold when the current originates from the drift of charges from source to drain. In the subthreshold regime ($V_g < V_{th}$), the current is mostly originated by diffusion of charges. In this regime the important parameter is subthreshold swing.

The value of subthreshold swing is extracted from the plot of the logarithm of the drain current versus the gate voltage at a constant drain voltage (linear or subthreshold regime). It measures the amount of V_g change required to increase I_d by an order of magnitude in the subthreshold region. The subthreshold swing is represented by the following equation:

$$S = \frac{\partial V_g}{\partial log_{10}(I_d)}.$$

The knowledge of subthreshold swing can give information about the total defect density at the semiconductor dielectric interface.[32] The total trap density, N_t, can be found from the equation:

$N_t = \left[\left(\frac{S\,log(e)}{kT/q} - 1\right)C\right]\frac{1}{q^2\varepsilon_s}$, where, k is the Boltzmann constant, q is the elementary charge, ε_s is the permittivity of the semiconductor and C the dielectric capacitance.[33]

1.2.3 Thin film transistor configurations

Transistor performance significantly depends on the device configuration. The four main transistor configurations are presented in Figure 1.2.

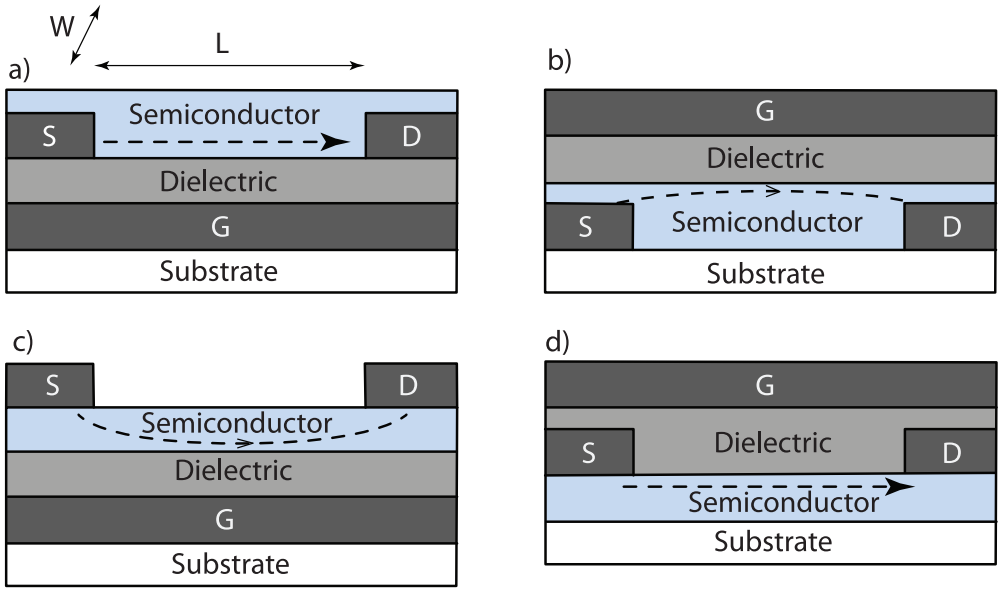

Figure 1-2: Schematic illustration of thin film transistor configurations: bottom contacts - bottom gate (a, BC-BG), bottom contacts - top gate (b, BC-TG), top contacts - bottom gate (c, TC-BG) and top contacts - top gate (d, TC-TG).

In these device configurations, the injected charges travel different distances to reach the semiconductor/dielectric interface, i.e. the region where charge transport takes place. For instance, in the BC-BG and TC-TG configurations charges are injected directly close to the semiconductor/dielectric, whereas, in the BC-TG and TC-BG structures the injected charges must travel through the whole thickness of the semiconductor to reach the channel. Thus, the device configuration can affect the main figures of merit of the transistor, such as the threshold voltage and the charge carrier mobility. For instance, a large surface of the source and drain electrodes

overlapping the gate electrode can result in improved charge injection, leading to a small contact resistance.[34]

1.2.4 The contact resistance and overlap capacitance

Charge exchange (injection and extraction) depends on the workfunction of electrode and the bandgap of the semiconductor. When the workfunction of the electrode is close to the conduction or valence bands of the semiconductor the charges are easily injected and the contacts are called ohmic. A mismatch between the workfunction and the conduction band is called an injection barrier (Schottky barrier). This introduces a resistance to the transistor (contact resistance, Rc). The contact resistance can be significantly larger than the channel resistance depending on the channel length, applied voltage and mobility of the carriers. So, it is especially important to control Rc in short channel devices ($L \leq 5um$) as it dominates over the total resistance and leads to degradation of electrical properties.[33]

The contacts materials in transistors are high work function metals such as Au, Ag, Pt. Conducting polymers, such as PEDOT:PSS, PANI [35-37], graphene and carbon nanotubes, can also be used.[38, 39] The high aspect ratio and 1D structure of carbon nanotubes facilitates charge carrier injection by tunneling and their low density of states provides a lever to further reduce the Schottky barrier height and width.

The overlap capacitance (C_{ov}) is the capacitance between the overlapping parts of source-drain contacts with the gate and it doesn't depend on the applied potential. It can be found by the formula:

$C_{ov} = (L \cdot W)_{overlap} \cdot C_{gate\ medium}$, where $L, W_{overlap}$ is the length and width of overlapping electrodes and $C_{gate\ medium}$ is the specific capacitance of dielectric.

The total capacitance of the transistor is:

$C_{total} = C_{channel} + C_{ov}$, where $C_{channel}$ is a capacitance between gate electrode and channel responsible for transistor operation.[40]

In the case of high-k dielectric materials or electrolytes as a gating media, the total capacitance is high enough that the overlap capacitance becomes negligible. The overlap capacitance directly

influences the transit frequency of transistors, (f_t), which quantifies the speed of the device.[41]

1.3 Electrolyte gated thin film transistors

A high operating voltage (tens of volts) is typically needed in conventional TFTs, due to the low capacitance. Typical dielectric materials, such as SiO_2 (k~3.9) or S_3N_4 (k~7) or others, possess capacitance density in the range of 0.005~0.5 μF cm^{-2}, depending on the thickness and dielectric constant.[42-44] Reducing the thickness of conventional dielectrics to achieve high capacitance can lead to high leakage current and reliability issues. The use of high-k dielectric materials such as ZrO_2 (k~20), Ta_2O_5 (~25), or TiO_2 (~40) can increase the capacitance without significant gate current leakage.[45]

Another way to achieve a high capacitance and charge carrier density modulation is electrolyte-gating [46-49], where the gate dielectric is replaced by an electrolyte. By applying a gate voltage, the electrolyte ions redistribute at the electrolyte/semiconductor interface, forming a thin electrical double layer (EDL). The small thickness of the double layer (~1nm) formed on the electrolyte semiconductor interface leads to high capacitance (typically 1-10 μF/c^2), which allows the transistor to operate at low voltages (less than 2 V).[50, 51]

The mode of operation of electrolyte-gated transistors is mainly governed by one or the two doping processes described below: electrostatic and/or electrochemical.[52, 53] For semiconductors, which are impermeable to ions, the double layer forming at interface with the electrolyte results in a gating mechanism similar to that taking place in field effect transistors (electrostatic, as shown on Figure 1.3a). For semiconductors which are permeable to ions, upon application of gate voltage, ions can have reversible redox reactions on the surface (electrosorption) or ions can enter the film leading to reversible redox reactions (intercalation), thus changing the charge carrier density and hence the conductivity of the film (as shown on Figure 1.3b).[54] It is worth noting that, in real devices, electrostatic and electrochemical doping may occur at the same time.[49, 55]. This faradaic charge transfer is called pseudocapacitance.

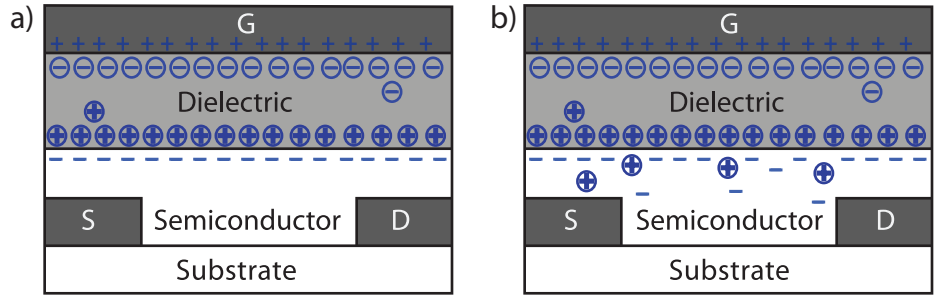

Figure 1-3:Schematic illustration of an electrolyte gated thin film transistors operating in field effect (a) and electrochemical mode (b).

The gate electrode, electrolyte and semiconductor as a second electrode form a capacitor. The electrolytic capacitance depends on the applied potential and frequency. It can be examined by impedance spectroscopy or cyclic voltammetry.[46, 56, 57] The equivalent circuit for such capacitor structure can be modeled as two resistor-capacitor (RC) circuits in series, see figure 1.4. One RC is related to the bulk of electrolyte and another one is related to the double layer.[58] [Yuan, 2010] Each RC circuit has a specific frequency domain and can be identified from the Bode plot (phase angle vs. frequency). At high frequencies (above 100 kHz) there is a bulk capacitive region (polarization of the bulk electrolyte); for the frequency range (10kHz to 1Hz) there is a EDL capacitive region, and below 1 Hz there is a EDL pseudocapasitive region (related to chemical processes on the electrolyte/semiconductor interfaces).

The total capacitor impedance (Z) is the sum of the real part (Z') and imaginary part (Z''):

$Z = Z' + iZ''$, where i is the imaginary unit.

When the electrolyte exhibits capacitive behavior at low frequency and resistive behavior at high frequency, the total impedance depends on the ohmic resistance R and on the electric double layer capacitance C_{EDL}:

$Z = R + i2\pi f C_{EDL,}$ where f is the frequency and C_{EDL} is the capacitance of the electric double layer.

The imaginary part of the impedance is inversely proportional to the capacitance, thus

$C = 1/(2\pi f Z'')$.

The capacitance can also be calculated from cyclic voltammetry, where the integration of

voltametric current over time provides the amount of doping charges Q. And, capacitance can be deduced from the slope of the (linear) plot of the doping charge vs. potential: C= Q/V.

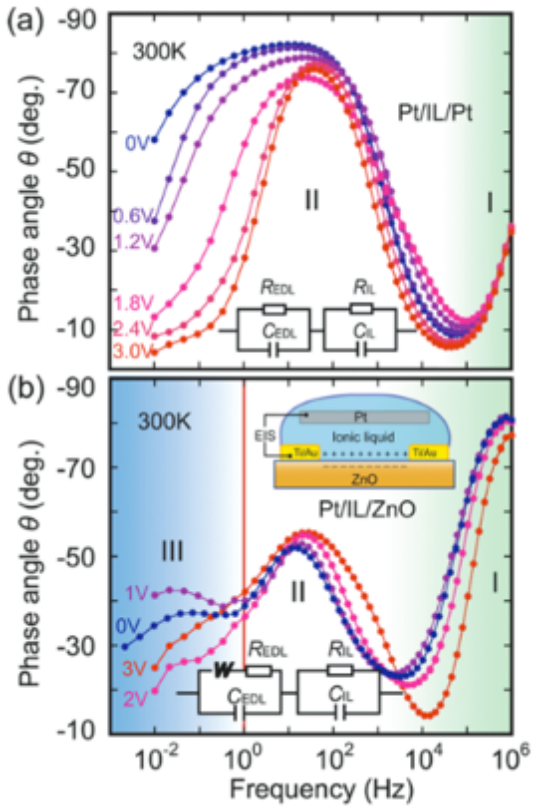

Figure 1-4: Example of the Bode plot (θ-*f*) in Pt/IL/Pt structure. Inset: equivalent electric circuit, two resistor-capacitor (RC) circuits in series. (b) The Bode plot of ZnO EDL transistor. I: bulk IL capacitive region. II: electrostatic EDL capacitive region; III: electrochemical pseudocapacitive region. Reprinted with permission from [58]. Copyright 2010 American Chemical Society.

1.4 Metal oxides (TiO_2 and SnO_2) as semiconductors

Metal oxides (MeO) are among the most popular channel materials in transistors, especially in next generation flexible and transparent transistors, due to their superior electrical properties and high reliability.[46, 59] The more utilized metal oxides in optoelectronic applications are transition and post transition metal oxides. The transition metals exhibit multiple oxidation states. Their compounds in higher oxidation states are strong oxidizing agents, as they tend to accept electrons to reach a stable lower oxidation state.

Electronic structures and charge transport mechanisms of metal oxides are quite different from conventional covalent semiconductors like silicon. CB of silicon formed by sp^3 σ-bonding and VB by sp^3 σ*-antibonding, and the band gap is the energy difference between them. In this case, any structural change will influence the charge transport decreasing the charge mobility. For instance, at a carrier density of 10^{19} cm^3 the electron mobility in a single crystalline and amorphous silicon is around 200 cm^2/Vs and 1 cm^2/Vs, respectively.[60] In metal oxides the band structure is different. The conduction path in crystalline and amorphous covalent semiconductors and post transition MeOs is shown in Figure 1.5.

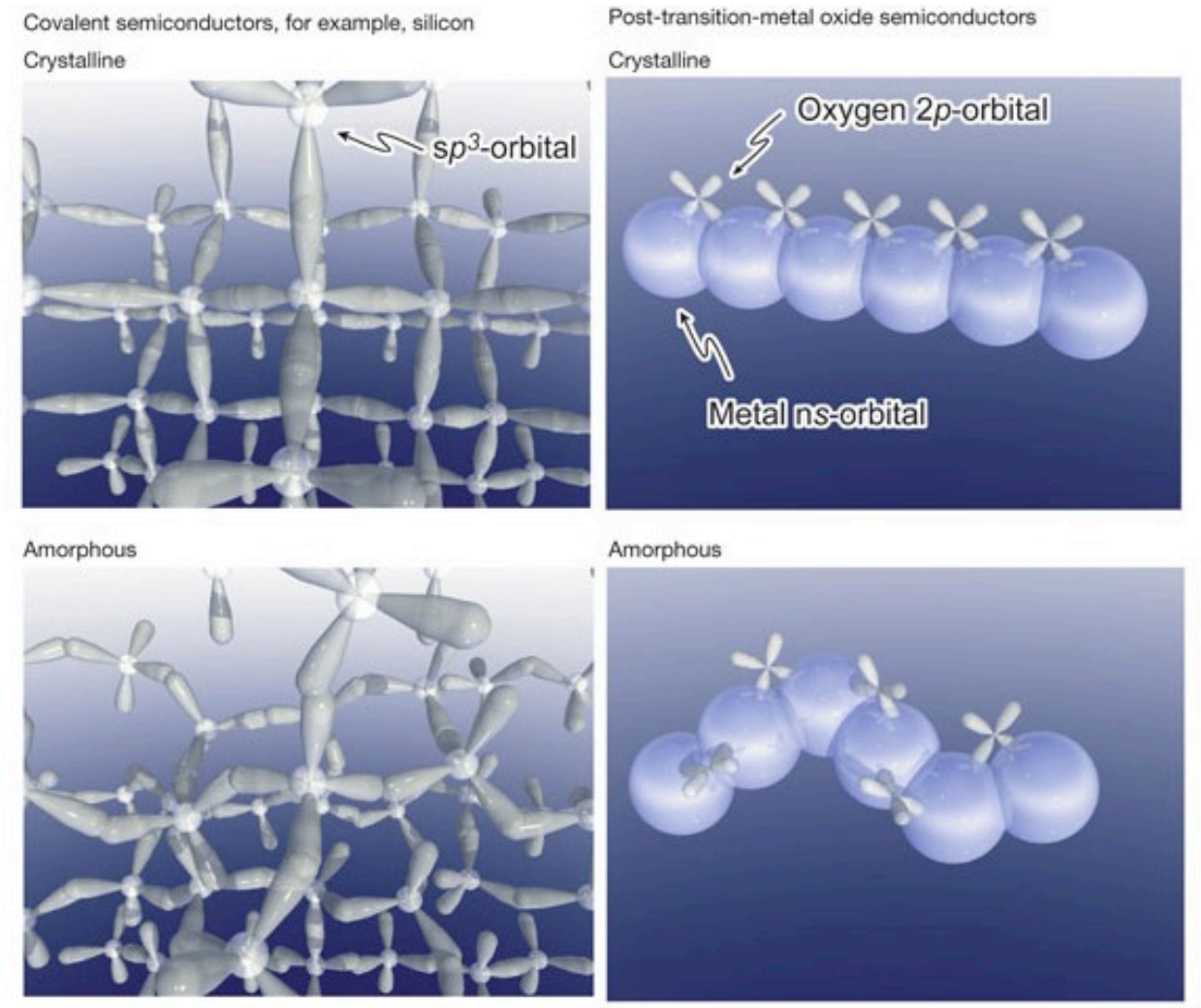

Figure 1-5: Schematic illustration of orbitals for the carrier transport paths in crystalline and amorphous covalent semiconductors and post transition MeOs. a) the band structure in covalent semiconductors, like silicon, consists of overlapping sp^3 orbitals, so structural randomness greatly

degrades the magnitude of bond overlap. b) In post transition oxide semiconductors, spheres represent metal s orbitals (conduction band), the contribution of 2p orbitals (valence band) is small. The spread of metal s orbitals is high and their overlap doesn't significantly affected in amorphous state. Reprinted with permission from[60] © Nature Publishing Group, 2004.

In most metal oxide semiconductors, due to the high electronegativity of O, there are covalent bonds with a strong degree of ionicity. The ionicity creates an electronic structure where 2p orbitals of O form the valence band (VB) and the highest occupied metal orbitals form the conduction band (CB). In the case of transition metals, the conduction band consists of localized d orbitals. In the case of post transition metals, the conduction band consists of delocalized ns ($n \geq 4$) orbitals.[60, 61] The overlap of big s orbitals is insensitive to distorted metal-oxygen-metal bonds in amorphous state.[62] Thus, the charge carrier mobilities of amorphous post transition MeOs can be similar to ones of crystalline.

In this work, I studied the main representatives of binary transition and post transition metal oxides TiO_2 and SnO_2, respectively. They possess similar crystal structures (Figure 1.6) and chemical bonds, and are comparable in electronic band-gap energies ($E_g \approx 3–4$ eV). However, the electronic properties are quite different. The TiO_2 has weak electron conductivity and optical absorption to UV light. While SnO_2 combine electrical conductivity and optical transparency to visible light.[61, 63]

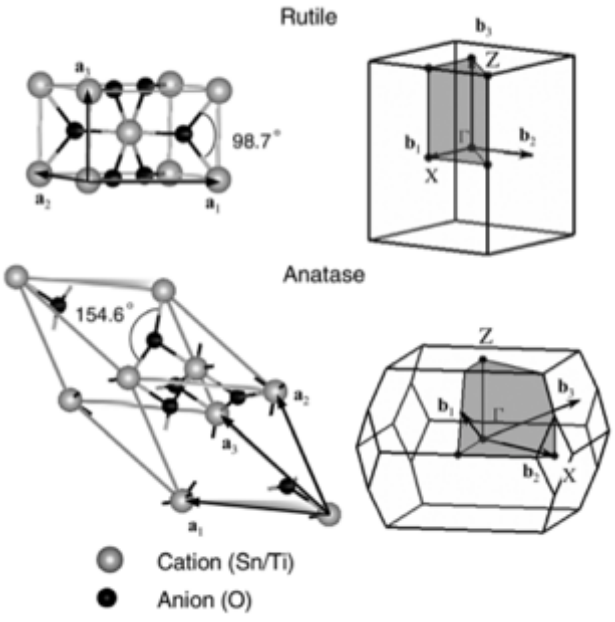

Figure 1-6:The crystalline structures and Brillouin zones of rutile D_{4h}^{14} and anatase D_{4h}^{19}. Reprinted with permission from [61]. © AIP Publishing LLC, 2013.

These differences can be described by their band structure. The VB formed by 2p orbitals of O are the same for all MeOs. The difference of CB, formed by Me cations, with electron configurations $5s^2 5p^2$ for Sn and $3d^2 4s^2$ for Ti gives rise to a single high dispersive CB for SnO_2 and to the several flat dispersed CBs for TiO_2, see Figure 1.7. The overlap of high spread 5s orbitals is responsible for the delocalization of electrons in SnO_2 making the conduction band dispersive and responsible for higher conductivity. While in TiO_2, the electrons are strongly localized in 3d orbitals making the CB flat dispersive. [60, 61]

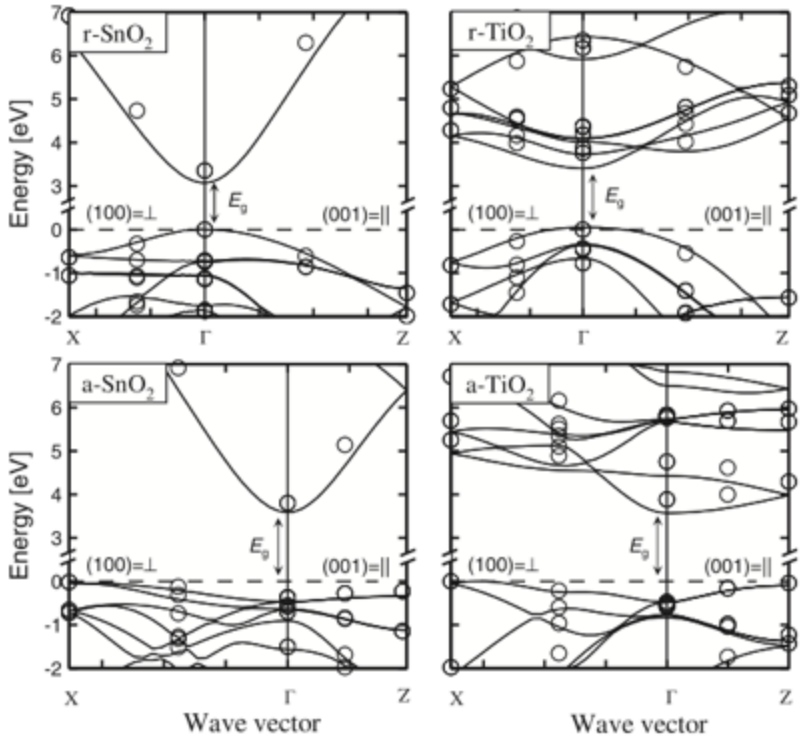

Figure 1-7:Electronic structures of r- SnO_2, r- TiO_2, a- SnO_2, and a- TiO_2 along two main symmetry directions (100) _|_ and (001) ||. Reprinted with permission from [61]. © AIP Publishing LLC, 2013.

1.5 Problem identification

The electrical characteristics of electrolyte-gated transistors depend on the device structure, the effective potential of gate electrode and the doping level of the semiconductor channel.

Understanding the electrical transport mechanisms in electrolyte-gated transistors is an ongoing challenge to design devices with better electronic performance. Moreover, the role played by the extension of the electrolyte/semiconductor and electrode/semiconductor interfaces on the doping and charge carrier transport processes requires deeper investigation. The overlap between the metal electrodes and the semiconductor, which is in contact with the electrolyte, might affect the charge injection process. Another challenge in the fabrication of high performance TFTs for flexible electronics, is the required low processing temperature (150 ºC in the case of polyethylene naphthalate (PEN) substrates, maximum 350 ºC for polyimide (PI) substrates).

1.6 General Objectives

The general objective of this Ph.D. thesis is the design, fabrication, and characterization of metal oxide electrolyte gated transistors based on TiO_2 and SnO_2.

The objective was accomplished by tuning the structure and the morphology of semiconductor materials (SnO_2 and TiO_2) as well as by selecting the appropriate gating media. To control the charge carrier density and understand the doping mechanism in the electrolyte gated TFT, patterning of the semiconductor material with different overlap of source-drain electrodes was implemented. SnO_2 TFTs were also fabricated on PI substrate and their electrical and mechanical properties were investigated to show high performance TFT for applications in flexible electronics.

1.7 Motivation

Environmentally friendly and abundant metal oxides as SnO_2 and TiO_2 are promising transistors channels for flexible displays, medical implants and sensors, wearable electronics etc. Electrolyte gating allows TFTs to work at low voltages, which is critical for bio applications. Fabrication of high performance electrolyte gated TFTs and shedding light on their electrical, electrochemical and mechanical properties make an invaluable contribution to bio and flexible electronics.

1.8 Specific objectives

To achieve the main objective the following specific objectives need to be achieved:

1. *Charge carrier density modulation of metal oxide thin films for electrolyte gated transistors and exploring the doping mechanisms*

By electrostatic and/or electrochemical doping, it is possible to exhibit a transition from insulator to semiconductor or metal like behavior. A high charge carrier density was achieved in TiO_2 and SnO_2 films by electrolyte gating. The fabrication of devices with different surface areas of semiconductor material in contact with the electrolyte and different overlaps with source-drain electrodes helped to tune the electrical properties of devices, to shed light on the charge transport mechanisms and to explore the best device geometry for high performance devices. The doping mechanisms were investigated by Electrical characterization, cyclic voltammetry (CV) and Electrical impedance spectroscopy.

2. *Fabrication of high performance flexible electrolyte gated transistors*

To make metal oxide thin films with good structural and electrical properties, high temperature annealing is needed. So the development of deposition of metal oxide thin films at temperatures of 350°C or lower is required for application in flexible electronics. Electrical and electrochemical characterization of flexible transistors were conducted. Moreover, to show the mechanical stability, electrical characterization of transistors was accomplished after repeating mechanical deformations.

3. *Tuning of the structure and morphology of transistor semiconductors and exploring the effect of ion size in electrolytes on transistors performance*

To explore the effect of structure and morphology of semiconductors on transistor performance, porous solution processed and highly dense evaporated films of TiO_2 were investigated. The relatively large [EMIM] cation cannot enter into the crystal lattice of TiO_2. It was shown that only small cations such as Li^+ can be intercalated through the "zig- zag" rows formed at edge-shared octahedral of the tetragonal form of anatase TiO_2. The effect of big [EMIM] and small Li^+ cations on doping mechanisms was introduced.

1.9 Organization of the work

This thesis is organized into the seven Chapters. Chapter 1 includes an overview of the topics related to the subject of the thesis (thin film transistors, their working principles and characteristics, electrolyte gated transistors and an introduction of metal oxides used in this thesis: TiO_2 and SnO_2), problem identification and objectives of the thesis. Chapter 2 introduces

the state of the art of thin film transistors, in particular metal oxide electrolyte gated transistors. Chapters 3, 4 correspond to two articles of which I was the first author.

Article 1: Tin dioxide electrolyte-gated transistors working in depletion and enhancement mode. (Submitted in ACS Appl. Mater. Interfaces).

Article 2: Photolithographically Patterned TiO_2 Films for Electrolyte-Gated Transistors (Published in ACS Appl. Mater. Interfaces, 8, 14855−14862, 2016).

Chapter 5 is devoted to investigation of effect of different morphology of TiO_2 and cations size in the electrolyte on doping mechanisms of TiO_2 electrolyte gated transistors. (It is a third paper in preparation where I am the first author and it will be submitted soon.)

Chapter 6 is about “General Discussion”.

Chapter 7 contains the conclusions and perspectives on the future work.

Appendix A and B contain all supporting information of articles 1 and 2, respectively.

Appendix C is a list of articles, published during this Ph. D., not included into this thesis.

Appendix D is a list of conferences in which I took part.

CHAPTER 2 LITERATURE REVIEW: METAL OXIDE THIN FILM TRANSISTORS

Metal oxides are attracting enormous interest for TFT technology, due to their electrical, optical and chemical properties.[64, 65] Most of them have a wide band gap, good stability and high charge carrier mobility; they are optically transparent in visible light, making them attractive for transparent TFTs in flat panel displays.[27, 66] Moreover, a lot of metal oxides possess bio-compatible and non-toxic properties making them attractive for bio electronics, such as variety of biosensors.[67] Some oxides have good electrical properties in amorphous state making them the materials of choice for flexible and bendable electronics.[41, 68, 69]

2.1 Vapor processed thin film transistors

The main binary oxides used in TFTs are ZnO, SnO_2 and In_2O_3 due to their good electrical properties, high transparency and biocompatibility. The review of SnO_2 TFTs will be covered in the following paper. ZnO TFTs deposited by radiofrequency magnetron sputtering at room temperature were introduced by Carcia.[70] The influence of different oxygen partial pressure during vacuum deposition on the stoichiometry of the metal oxide film was shown. The highest electron mobility was 40 $cm^2V^{-1}s^{-1}$ and on/off ratio 10^3 for TFTs where ZnO films were deposited at oxygen partial pressure 10^{-6} Torr. The highest on/off ratio 10^6 with electron mobility 1.6 $cm^2V^{-1}s^{-1}$ was achieved for device fabricated at oxygen partial pressure 10^{-5} Torr due to the fewer amounts of oxygen vacancies and so lower conductivity and off current. A depletion mode ZnO transistors with an electron mobility of 23.3 $cm^2V^{-1}s^{-1}$ were demonstrated by Mi. [71] ZnO was deposited by metal oxide chemical vapor deposition and the Al_2O_3 dielectric was deposited by Atomic Layer Deposition (ALD). An on-off ratio of 10^6 and a threshold voltage of -4.8 V were achieved. Lin et al. demonstrated flexible ZnO TFTs where both the dielectric and the semiconductor films were deposited by ALD at 110 °C (Figure 2.1). ALD permits the deposition of defect-free films with minimal defects in the interface at low temperature. The electron mobility was 16.6 $cm^2/V{\cdot}s$ and was increased up to 20 $cm^2/V{\cdot}s$ after passivation of the ZnO layer by TiO_2(3 nm)/Al_2O_3(2 nm) nanolaminate. The passivation layer not only improved the electrical characteristics but also prevented degradation of the transistor properties with time.[72]

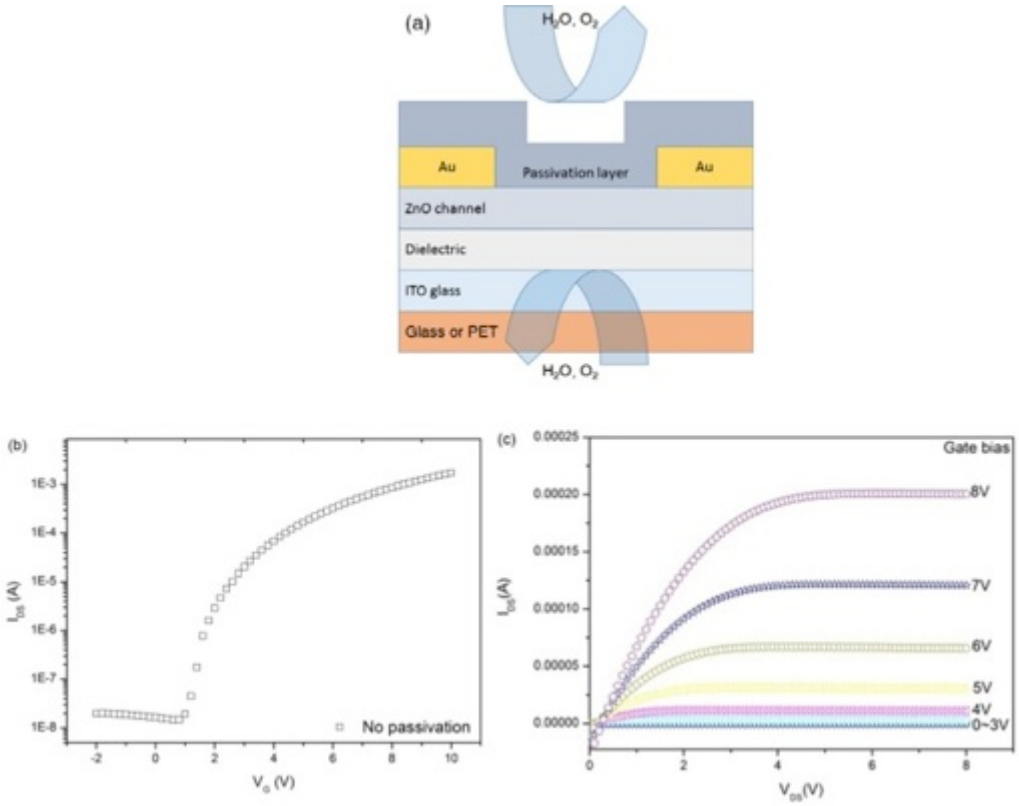

Figure 2-1: (a) Schematic illustration of ZnO transistor; (b) transfer and (c) output characteristics of this transistor without passivation layer. Reprinted with permission from [73]. Copyright © 2015 American Chemical Society

Hosono and colleagues started a new era of ternary and quaternary MeO by synthesizing indium gallium zinc oxide (IGZO) grown by reactive solid-phase epitaxy at room temperature.[74] An electron mobility of 80 $cm^2V^{-1}s^{-1}$ and an on/off ratio of 10^6 was achieved by making use of a-high k HfO_2 dielectric (with dielectric constant 18) and mobility 2 $cm^2V^{-1}s^{-1}$ was achieved using an amorphous aluminum oxide dielectric. Making use of high k dielectric significantly increases the capacitance and charge carrier density in the IGZO leading to high mobility. The layered lattice structure compose of InO_2^- and $GaO(ZnO)_5^+$ stacked along the (001) direction was shown by high resolution transmission electron microscopy (HRTEM), see figure 2.2. It is worth to notice that Ga^{3+} replacing Zn^{2+} in tetrahedral sites maintained the electroneutrality. Moreover, Ga ions formed stronger chemical bonds with oxygen thus suppressing the oxygen vacancy formation. InO_2 worked as a passivation layer, preventing O_2 out-diffusion. Later, the same group published amorphous IGZO transistors on polyethylene terephthalate (PET) films substrate with ITO

electrodes and Y_2O_3 dielectric, where IGZO was also deposited by pulsed laser deposition. An electron mobility of 7 $cm^2V^{-1}s^{-1}$ and an on/off of 10^3 were measured also under bending.[60]

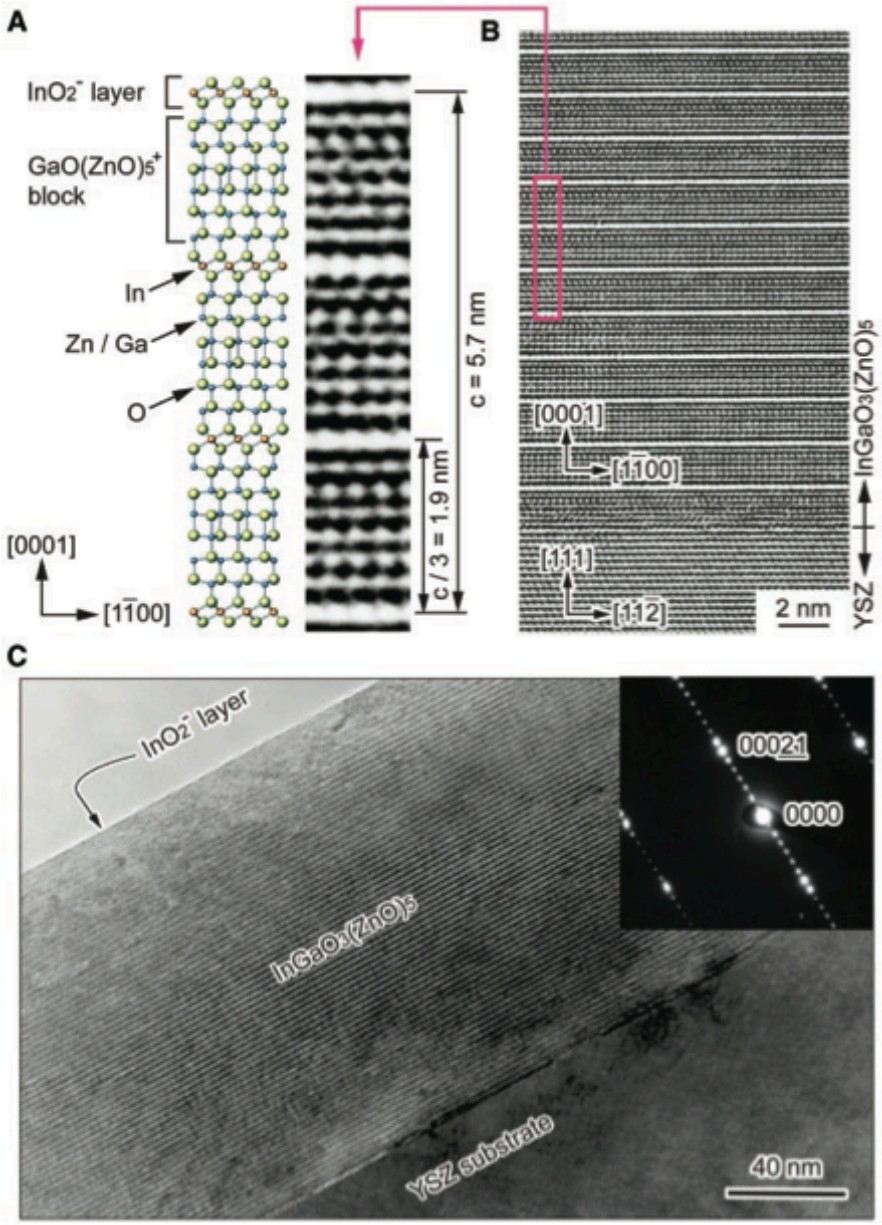

Figure 2-2: Structure of $InGaO_3(ZnO)_5$. (A) Schematic illustration of the crystal structure. A HRTEM lattice image is shown for comparison. (B,C) Cross-sectional HRTEM images of a $InGaO_3(ZnO)_5$ thin film grown by reactive solid-phase epitaxy. Reprinted with permission from [74]. Copyright 2003 The American Association for the Advancement of Science

These works paved the way to the use of different combinations of cations with $(n-1)d^{10}ns^0$ ($n \geq 4$)

electronic configuration like zinc tin oxide (ZTO) [75], indium zinc oxide (IZO) [59, 76, 77], IGZO [60], aluminium zinc oxide (AZO).[78] Multi components compounds easily formed amorphous films, due to the different ionic charges and sizes of each component. Amorphous MeOs attract more and more attention because of their low processing temperatures and a more uniform surface, leading to better electrical characteristics.[79]

Amorphous zinc tin oxide TFTs with good electrical properties (on/off of 10^7, field effect mobility around 5-15 $cm^2V^{-1}s^{-1}$) were introduced by Chiang and others. The zinc tin oxide was deposited by radiofrequency magnetron sputtering. After a high temperature treatment at 600 ºC the mobility values were increased up to 20-50 $cm^2V^{-1}s^{-1}$ and the on/off was higher than 10^7.[75] Amorphous gallium tin zinc oxide (a-GSZO) TFT films were deposited by radiofrequency magnetron co-sputtering using gallium zinc oxide and tin targets at room temperature and at 150 ºC.[80] TFT deposited at higher temperature possess better electrical performances. Higher electron mobility and higher on/off ratio (32 $cm^2V^{-1}s^{-1}$ and 10^{10}) were achieved in indium tin zinc oxide (ITZO) flexible TFTs in comparison with IGZO flexible TFTs (10 $cm^2V^{-1}s^{-1}$ and 10^8).[81] Inverted-staggered bottom-gate TFTs were fabricated on a polyimide film with conventional SiO_2 dielectric. Moreover, 8-inch organic light emitting display (OLED) was fabricated using (ITZO) flexible TFTs, which hindered color video even during the bent.

2.2 Solution processed thin film transistors

Solution processing of metal oxides, such as printing, spin coating and spray pyrolysis opens doors for large area electronics, flexible and printed electronics in ambient condition.[65] Figure 2.3 represents an example of general solution processing for many MeO deposition.[82] The first step is the synthesis of oxide solution by mixing a metal precursor and a solvent. The second step is a pre-annealing to remove the solvent. The third step is an annealing at higher temperature to form the metal oxide layer, which consists of decomposition, hydrolysis, dehydroxilation and crystallization. Hydrolysis is when the metal precursor mixed with solvent; the main intermediate products of this reaction will be radicals of metal hydroxide and other complexes. Then when the annealing temperature is high enough the thermal decomposition of metal hydroxide produce the metal oxide and liberate the water. Different annealing temperatures are needed for different oxides.

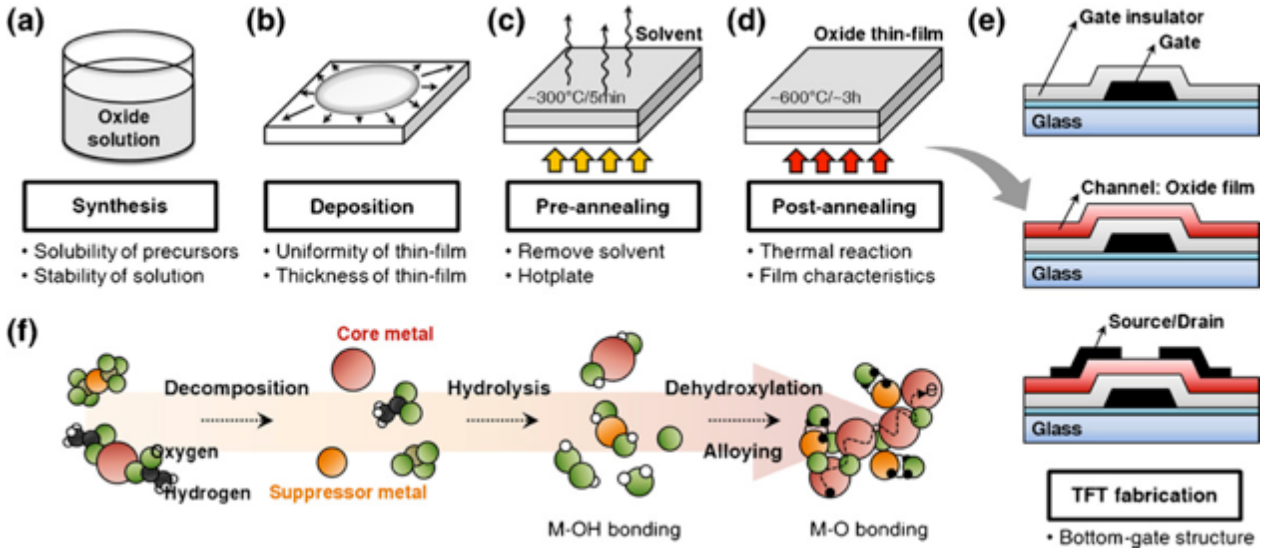

Figure 2-3: Schematic illustration of the solution process for oxide TFTs: (a) Oxide solution was synthesized using metal precursors in solvent. (b) The synthesized oxide solution can be deposited on a substrate by various methods such as spin-coating, printing. (c) The oxide thin film was pre-annealed to remove the solvent and (d) post-annealed to develop an active layer. (e) The bottom-gate top-contact TFT structure was fabricated using solution process. (f) The entire chemical reactions in the oxide solution. Reprinted with permission from [82]. Copyright 2014.

2.2.1 Reduction of the fabrication temperature

The drawback of solution processing is the requirement of the high temperature treatment for hydrolysis and hydroxo-condensation (typically 200-600 °C, depends on the precursor) to form the lattice. The low processing temperature (150°C - 350°C, depending on the substrate) is crucial for applications in flexible electronics, where substrates are not stable at high temperature. Figure 2.4 demonstrates the thermogravimetric analyses of different precursors used for IZO TFTs. The $Zn(NO_3)_2$ precursor shows the decomposition temperature of around 200 °C, hydroxyl and carbon impurities decreased more rapidly, leading to good quality film with high electrical properties.[82] High mobility TFT was fabricated using a mixture of zinc acetate [$Zn(OAc)_2$] and 2-ethanolamine in methoxyethanol as a precursor. Thermogravimetric and differential thermal analyses showed that decomposition of this precursor started at ~190 °C and completed at ~310 °C. An exothermic peak appeared between 300 and 400 °C, revealing the formation of ZnO crystals. The saturation mobility and on/off ratio of the final transistors were 5.25 $cm^2V^{-1}s^{-1}$ and 1.65×10^5, respectively.[83]

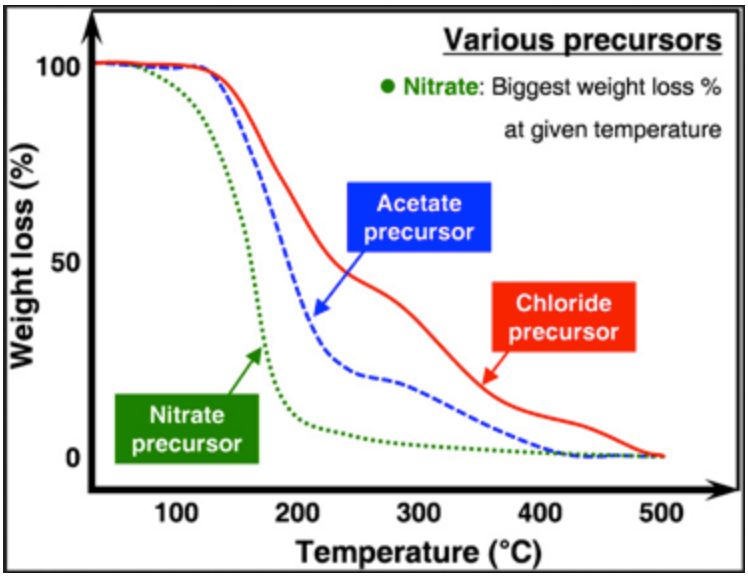

Figure 2-4: Thermogravimetric analysis of different IZO precursors. Reprinted with permission from [82]. Copyright 2010 Creative Commons CC-BY license.

Another way to lower the processing temperature is use of aqueous precursors without organic substances for deposition of ZnO films.[84-86] Meyers introduced aqueous zinc-ammine precursors for low temperature fabrication of spin coated and printed ZnO enhancement mode TFTs. $Zn(NO_3)_2 \cdot 6H_2O$ was dissolved in distilled H_2O with addition of NaOH.[86] Spin coated devices annealed in ambient atmosphere at 150 °C had an electron mobility as high as 1.8 $cm^2V^{-1}s^{-1}$ and on/off ratio as high as 10^6. Printed devices annealed at 300 °C in flowing N_2 possessed higher electron mobility 4-6 $cm^2V^{-1}s^{-1}$ and on/off ratio more than 10^6. Another group introduced ZnO hydrate precursor ($ZnO \bullet xH_2O$) and ammonium hydroxide for the growth of ZnO films for high-performance transistors at temperatures between 80–180 °C.[85] BG-TC transistor configurations with ZrO_x and AlO_x-ZrO_x as dielectric materials were fabricated and had electron mobilities of up to ≈11 $cm^2V^{-1}s^{-1}$. A further reduction of the processing temperature was achieved by replacing thermal annealing with a photo-activation step using UV light. TFT with UV treatment showed electron mobilities of ≈1 $cm^2V^{-1}s^{-1}$ and on/off ratio $>10^4$.

Rim and colleagues showed the effect of high pressure annealing, which help to decrease the fabrication temperature and get high performance transistors. Films annealed in O_2 at 350 °C and 1 MPa pressure had the same crystalline structure and good electrical characteristics as films annealed at low pressure 0.1 MPa at 500 °C.[84]

Besides UV, microwave annealing was used to obtain high performance MeO TFTs at lower temperature.[87, 88] Microwave assisted annealing helps dehydroxylation at lower temperature. Sol gel ZTO TFT had an electron mobility of 0.15 $cm^2V^{-1}s^{-1}$ and an on/off ratio 10^5 after annealing at 350 °C. After microwave assisted annealing at same temperature, an electron mobility of 1.8 $cm^2V^{-1}s^{-1}$ and an on/off ratio 10^6 were observed.[87]

Furthermore, a good approach to decrease the fabrication temperature and to control the charge carrier density is the use of a dual active layer. Dual InZnO(IZO)/AlInZnO(AIZO) TFT with good electrical performance was fabricated at the relatively low temperature of 350 °C. By varying the In/Zn ratio in IZO it is possible to change the charge carrier density in the channel and by varying In/Zn ratio in AIZO the barrier height between IZO and AIZO can be increased, thus decreasing the off current and improving the on/off ratio.[89]

Banger et al. demonstrated a low-temperature method 'sol–gel on chip' hydrolysis to deposit IZO film. Exposure to water of an organic–inorganic alkoxide-based precursors induce the reactions consisting of hydrolysis and condensation and nucleophilic substitution–addition mechanisms. Without hydrolysis, the decomposition temperature of the precursors is 350 °C. The hydrolysis decreased the annealing temperature required to form high quality metal oxide films down to 230 °C. TFTs fabricated at 230 °C using hydrolysis show electron mobility of 7 $cm^2V^{-1}s^{-1}$ and on/off ratio 10^7.[59]

2.2.2 Role of dopant

As was mentioned in 1.3, the higher conductivity in MeO is obtained from cations with electronic configuration $(n-1)d^{10}ns^0$ ($n \geq 4$), such as Zn, In, Sn. For example, by increasing the Indium content the conductivity of InGaZnO was increased resulted to an increase of both the on current (I_{on}) and the off current (I_{off}).[90] High off current is not desirable for real applications. To maintain the desired conductivity it is possible to add an electron suppressor to metal solution.

Kim et al. suggested choosing elements as effective electron suppressors with a low electronegativity and a high standard reduction potential. The element with high reduction potential will reduce the O vacancy. As well oxygen vacancies can be reduced by increasing the electronegativity difference between Me and O. At the same time, the ionic radius of the dopant ion should be smaller than the host one; otherwise it can induce the expansion of the lattice and

increase the amount of oxygen vacancies.[82] Another important parameter is the Lewis acid strength, which defines how easily atoms will accept electrons.[91] The Lewis acid strength has a higher influence than the electronegativity on effective charge and ionic radii. The metal-oxygen bonding strength should be also considered. The bonds between dopant carrier suppressor and oxygen should be stronger than bonds between host ion and oxygen. Some of dopant ions are given in table 2.1.

Table 2-1: Lewis acid strength of elements and their metal-oxide bonding strength. Reprinted with permission from [91]. Copyright 2014 Cambridge University Press.

Elements	Electronegativity	Lewis acid strength	Z/r^2	Bond strength of metal–oxygen (~kJ/mol)
Sr^{2+}	1.004	1.417	1.148	549.5
Ba^{2+}	1.005	1.163	0.901	502.9
Ca^{2+}	1.032	1.593	1.539	589.8
Mg^{2+}	1.208	1.402	2.704	363.2
Y^{3+}	1.209	1.465	2.774	719.6
La^{3+}	1.212	0.852	2.184	799.0
Gd^{3+}	1.272	0.788	2.582	719.0
Sc^{3+}	1.316	1.697	3.830	681.6
In^{3+}	1.445	1.026	4.152	320.1
Zr^{4+}	1.476	2.043	5.408	776.1
Al^{3+}	1.499	3.042	6.584	511.0
Ga^{3+}	1.562	1.167	5.194	353.5
Hf^{4+}	1.568	1.462	5.536	801.7
Ti^{4+}	1.577	3.064	7.207	672.4
Sn^{4+}	1.583	1.617	5.806	531.8
Nb^{5+}	1.771	2.581	8.218	771.8
Sb^{5+}	1.763	3.559	9.131	434.3
Si^{4+}	1.769	8.096	13.717	799.6
Ge^{4+}	1.799	3.059	8.911	659.4
Ta^{5+}	1.881	1.734	8.218	799.1
B^{3+}	1.966	10.709	17.847	808.8
Mo^{6+}	2.025	3.667	11.259	560.2
As^{5+}	2.035	6.220	13.889	481.0
P^{5+}	2.131	10.082	18.491	599.1
W^{6+}	2.132	3.158	11.574	672.0
H^{+}	2.271	1.624	11.111	427.6
Se^{6+}	2.289	9.508	19.133	468.8
Cr^{6+}	2.290	8.203	17.836	429.3
S^{6+}	2.479	21.362	32.450	521.7

Li^{+} was also demonstrated as a carrier suppressor in ZnO. Li doped ZnO was deposited by spray pyrolysis, when the precursor solution sprayed on the heated substrate (400-450 °C in this case). The impressive electron mobility of 85 $cm^2V^{-1}s^{-1}$ and on/off ratio of 10^6 was shown.[92]

2.3 Electrolyte gated thin film transistors

The main advantage of electrolyte-gated transistors is low operating voltage, due to the high capacitance of the electrical double layer at the electrolyte/semiconductor interface.[50, 93-95] Ionic liquids, ion gels, polymer electrolytes, aqueous salt solutions or even water were extensively reported as gating media.[46, 96-98] Interesting research on eight different ionic liquids and their influence on the electrical properties of electrolyte gated ZnO transistors showed that double layers formed faster using ionic liquids with higher ionic conductivity, leading to higher switching speed in transistors.[96] Smaller cations formed denser double layer and showed higher capacitance. Thus, mobility decreased when capacitance were increased. The electron mobility values were in the range of 1.9 - 15.9 $cm^2V^{-1}s^{-1}$. The same work reports improvement of the long term stability of transistors in ambient atmosphere by passivation of the ZnO layer with hexamethyldisilazane (HMDS).

In electrolyte-gated transistors, the high capacitance allows accumulating high charge carrier density in the channel material (up to 10^{14}-10^{15} cm^{-2}) thus making possible the transition of the channel from insulator to semiconductor or even metallic. The doping mechanism in electrolyte gated transistors is a matter of debate. Recently, Xie et al. showed 2D insulator to metal transition (with charge carrier density up to 7×10^{14} cm^2) in the electrolyte gated In_2O_3 thin film transistor by Hall Effect measurements.[94] They fabricated four-point contact electrolyte gated transistor configuration (shown in the figure 2.5a) allowing for transistor and Hall Effect measurements at the same time. [EMI][TFSI]+PS-PMMA-PS ion gel was used as an electrolyte and PEDOT:PSS as a gate electrode. The charge carrier densities were extracted from the gate displacement current and from the Hall Effect measurements. The related mobility values are shown in figure 2.5 b and c. It is worth to note that the charge carrier density and capacitance values extracted by the two approaches are quite similar. Leng et al. investigated doping mechanisms in electrolyte gated transistors.[99] They used single crystal, epitaxial and stoichiometric forms of ITO and WO_3 for comparison. The films were patterned into a long bar with multiple contacts for Hall measurements and only one contact was covered with electrolyte, see figure 2.6. After application of electrolyte gating, Hall effect measurements were done in the gated contact and in the neighboring ones. The measurement showed that ITO devices had mostly electrostatic doping

since there were no difference in Hall resistance for contact one and two others. For WO_3 the situation was different, leading to a conclusion of ion migration from contact 1 to contact 2 and 3.

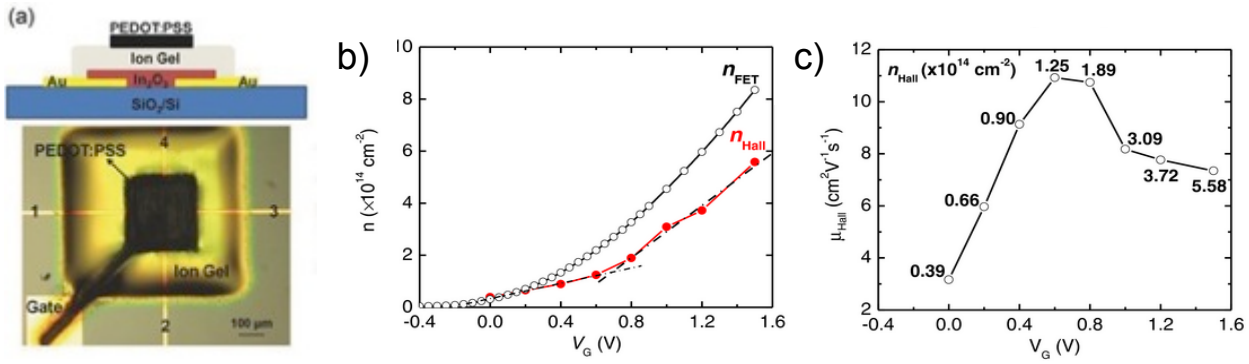

Figure 2-5: a) Schematic illustration and optical image of a van der Pauw ion-gel-([EMI][TFSI]+PS-PMMA-PS)-gated printed In_2O_3 TFT; b) Electron density from Hall effect (n_{Hall}), and from displacement current (n_{FET}) versus V_G. c) Hall mobility (μ_{Hall}) versus V_G; n_{Hall} is labeled for each point. Reprinted with permission from [94]. Copyright 2017 John Wiley and Sons.

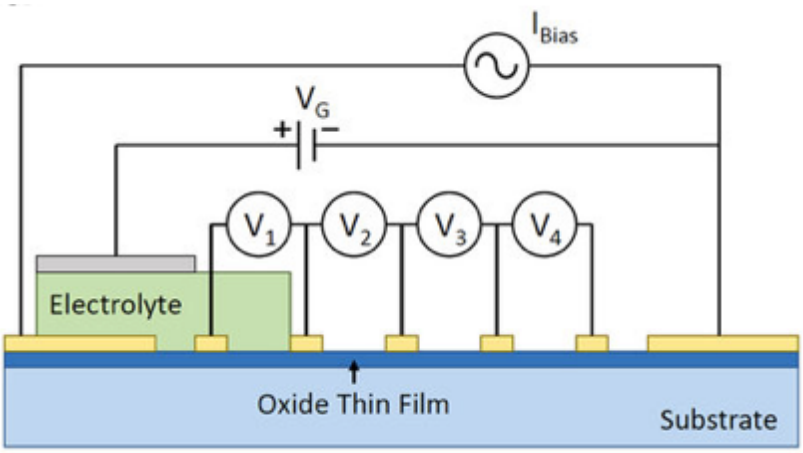

Figure 2-6: Schematic of the device to test for long range effects in oxide thin films away from the area being charged. The gate was a platinum mesh connected to a DC power supply. The spacing of voltage contacts was 300 μm for all devices. Reprinted with permission from [99]. Copyright 2011 American Chemical Society.

The importance of device architecture for electrolyte-gated transistors was shown by Marques [100] comparing planar and top gate configurations of In_2O_3 based transistors. It was shown that top-gate configuration improves electrical characteristics due to reduced electrolyte resistance

and improved electrostatic coupling between gate and channel. Inkjet printed In_2O_3 transistors, using solid polymer electrolyte as a gating media, were demonstrated by Dasgupta et al.[98] In_2O_3 nanoparticles were dispersed in deionized water with low concentrations of an organic base (ethanolamine or piperazine) as a surfactant and printed on already patterned, by e-beam lithography, ITO electrodes. The optical image and device structure are shown in the figure 2.7. The field-effect mobility of such a device was 0.8 $cm^2V^{-1}s^{-1}$. The same group fabricated In_2O_3 inkjet printed TFT using the $InCl_3$ precursor and solid polymer electrolyte.[95] Devices annealed at different temperatures were compared with higher electron mobility values obtained for transistors annealed at 400 °C. For calculation of electron mobility the double layer capacitance was extracted from the impedance spectroscopy at low frequency and increased on 10-20% due to the higher real surface area of electrolyte semiconductor interface.

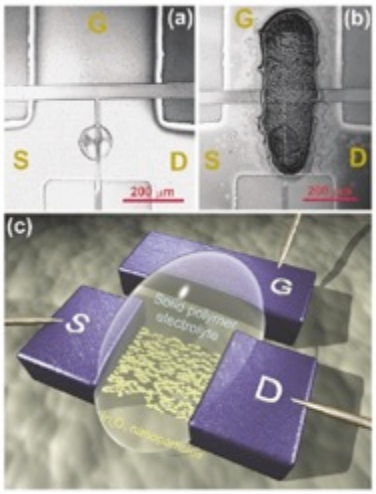

Figure 2-7: Optical images of a typical in-plane In_2O_3 transistor. (a) Patterned (with e-beam lithography) ITO electrodes and a printed drop of In_2O_3 nanoink. (b) The optical image of the same device after printing the electrolyte. (c) A schematic illustration of the device. Reprinted with permission from [98]. Copyright 2011 American Chemical Society.

Water, aqueous salt solutions or aqueous buffer solutions are gating media of choice for biomedical applications. ZnO TFT gated by water and phosphate-buffered saline (PBS) solution was introduced.[97] PBS gated device possessed a bit better electrical properties like on/off ratio of 10^3; while water gated transistors showed on/off ratio of 10^2. They proposed that sodium ions in PBS occupy interstitial sites in ZnO and act as dopants. Furthermore sodium influence on the stoicheometry in the ZnO lattice and induce oxygen vacancies. Later, in 2016, they introduced

low temperature processed water gated ZnO transistors.[101] The influence of different work function gate electrodes on electrical characteristics of water gated transistors was shown. A significant higher drain current and capacitance were observed using the tungsten W gate electrode with the lowest work function (closet one to conduction band of ZnO). More ohmic contact with the W electrode can accumulate more charges in the channel. This effect was explained by the electrochemical dissolution of WO_4 in water under the sweeping of the gate bias. The threshold voltage shift was observed following the gate work function trend.

Aerosol-jet-printed ZnO EGTs making use of [EMI][TFSI]+PS-PMMA-PS ion gel as the electrolyte were demonstrated on flexible polyimide (kapton) substrates.[46] $Zn(OH)_2$ aqueous ammonia solution was used as the ZnO ink and annealed at 250 °C after printing. The transistors showed field-effect electron mobilities of 1.6 $cm^2V^{-1}s^{-1}$, threshold voltages of 1 V and on/off ratio of 10^5. Moreover, transistors demonstrated quite stable properties after bending with a radius 2.5 cm (tensile strength 0.2%) and decrease of drain current by 35% after bending with a radius 0.5 cm (tensile strength 1%). In recent work, sputtered Al doped ZnO (AZO) was used as the material for both source-drain electrodes and channel on a chitosan film used as gating medium.[102] An electron mobility of 8.3 $cm^2V^{-1}s^{-1}$, and an on-off ratio of 10^5 was obtained at an optimized thickness of 30 nm. ZnO TFTs gated with aqueous electrolytes were introduced for environmental and biological sensing by Bandiello.[103] Glucose oxidase was covalently attached through (3-glycidyloxypropyl)-trimethoxysilane (GOPS) to the surface of the ZnO channel. The device was able to detect glucose concentrations between 10^{-4} and 10^{-1} M.

Other biomedical applications of MeO EGT, like synapsis transistors and pH sensors, are gaining a lot of interests. Shao introduced high performance IGZO EGT using sol gel silica as the electrolyte, which was favorable for synaptic behavior emulation.[104] The sol gel silica, annealed at 120 and 300 °C, showed a specific capacitance, measured at 1.0 Hz, of ~3.0 $\mu F/cm^2$ and 0.88 $\mu F/cm^2$, respectively. The saturation field-effect mobility of the devices gated by the silica films annealed at 120 °C was about 6 $cm^2V^{-1}s^{-1}$, and the on/off ratio higher than 10^7.

Liu et al. introduced a solid electrolyte-gated flexible IZO neuromorphic transistor with multiple in-plane gate electrodes for pH sensing application (Figure 2.8).[76] This device operated in dual gate sensing mode and showed a high pH sensitivity of ~105 mV/pH. Another group have also

used the a-IGZO TFT for pH sensing. IGZO was deposited by radiofrequency magnetron sputtering and annealed at 300, 400 and 500°C.[105] Transistors annealed at 500°C temperature showed better performance, with an electron mobility of 27 $cm^2V^{-1}s^{-1}$, a threshold voltage of 0.02V, and an on/off ratio of 10^6. However, better pH sensitivity of 160 mV/pH showed device annealed at 400°C and operated at dual gate (i.e. the transfer characteristics measured by sweeping the one gate voltage with the another gate exposed to the electrolyte) than one gate configuration.

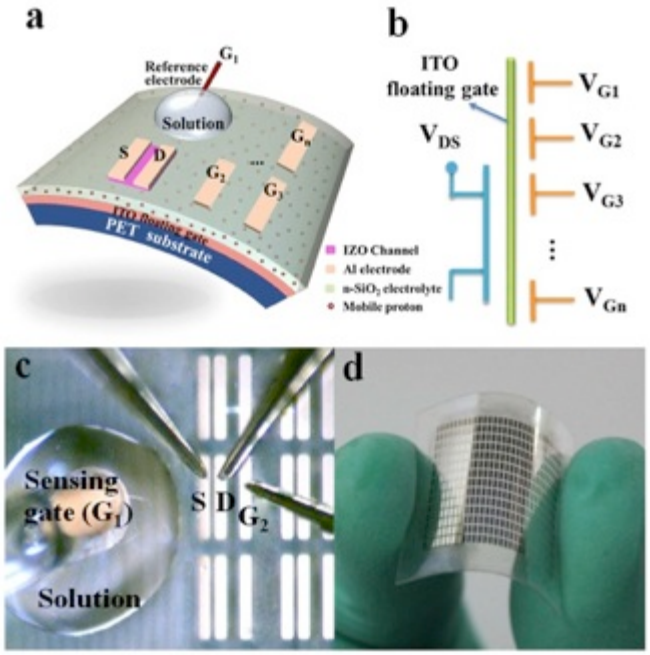

Figure 2-8: Schematic diagram of a flexible IZO-based neuromorphic transistor with multiple in-plane gate electrodes. Reprinted with permission from [76]. Copyright 2015 Creative Commons CC-BY license.

All the above mentioned papers used post-transition metal oxides as the channel materials, where the conduction band is formed by metal s orbitals. Some transition metal oxides (d group metals) are also utilized in EGT. Polycrystalline TiO_2 TFTs with different gating media, such as poly(vinyl alcohol) (PVA), ion-liquid EMIM-TFSI, and ion-gel were demonstrated.[106] The dependence of the concentration of mobile ions in the electrolyte on the performance of transistors was shown. Increasing the NaOH concentration in PVA, V_{th} was decreased while the channel conductance and the off current increased. In ionic liquid and ion gel gated devices the on/off ratio was about 10^4 and the driving voltage was less than 1 V. The authors suggest that an

oxidation reaction probably occurs on the interface between TiO_2 and the electrolyte. TiO_2 TFT slightly doped with Nb using ionic liquid [DEME]-[TFSI] as gating media were introduced. A transition from insulator to metal, with increase of charge carrier density from 10^{13} to 10^{15}, was achieved.[107] The increase of charge carrier density from 10^{13} to 10^{14} and transition from paramagnetic material to ferromagnetism in slightly Co doped TiO_2 ($Ti_{0.90}Co_{0.10}O_2$) by electrolyte gating were shown.[108]

Yang et al. studied the electrolyte gating of VO_2 thin films deposited by radio frequency magnetron sputtering with a V_2O_5 target.[109] Two ionic liquids [DEME][TFSI] (N, N -Diethyl-N -methyl-N -(2-methoxyethyl) ammonium bis (trifluoromethanesulfonyl)imide) and [EMIM][Im] (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide) and two device configurations (planar and vertical, see figure 2.9) were used. The temperature dependence of channel resistance was shown. At room temperature, the VO_2 channel resistance decreased from 109 to 63 kΩ upon application of +2 V gate bias, whereas it slightly increased at -2V. No gating effect was observed at high-temperature (80-110 °C), where VO_2 was in the metallic state.

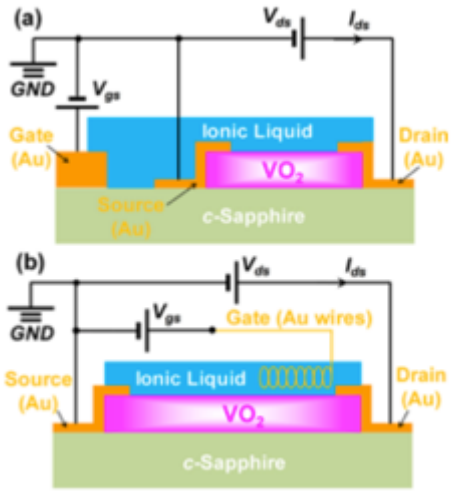

Figure 2-9: Schematic illustration of VO_2 EGT devices with (a) planar gate geometry, and (b) vertical gate geometry. Reprinted with permission from [109]. Copyright 2012 AIP Publishing LLC.

An insulator-to-metal transition by electrolyte gating was also demonstrated in strontium titanate ($SrTiO_3$).[110, 111] Li et al. proposed that, when gate voltage is applied, the imperfection of ordering of cations on the interface of $SrTiO_3$ leads to variations of carrier densities. At rather

high gate voltage (3 V), the formation of percolative paths leads to a metallic behavior. When gating level is low, metallic regions are disconnected and the hoping transport is dominating.[111] In 2010, Ueno et al. tried to understand the doping mechanism in $SrTiO_3$ EGT with polymer electrolyte $KClO_4$-PEO (polyethylene oxide).[108] At applied potential higher than 3.7 V (critical potential) the channel becomes highly conductive irreversibly. Sheet carrier density reached 10^{15} cm^{-2} at 5 V. The possible explanations could be that high electric fields induce the oxygen vacancies at the surface increasing the conductivity. In contrast, below the critical potential, the charging process was attributed to reversible electrostatic processes with a sheet charge carrier density of 10^{14} cm^{-2}. Within this regime, they reached a high electron mobility of 10^4 $cm^2V^{-1}s^{-1}$ at 2 K.

Later, it was proven that during electrolyte gating oxygen migration happens from metal oxide to electrolyte increasing the amount of oxygen vacancies responsible for the increase of conductivity in the VO_2 and TiO_2 channel.[112, 113] The changes in the oxidation state of V were shown by XPS. Moreover it was shown that, in single crystal TiO_2 EGT, formation of oxygen vacancies depends on the TiO_2 facets. To prove the charge carrier modulation more depends on the oxygen migration from TiO_2 to electrolyte, than on electrostatic doping, ionic liquid was saturated with O. This leads to suppression of the gating effect and proved the low influence of the electrostatic doping.

Outlook

A big progress was done in implementing and understanding metal oxide materials. The demonstration of unique electrical properties of post transition metal oxides in amorphous state better than a-Si give rise to potential applications of metal oxide transistors in flexible and transparent electronics. For instance, IGZO transistors, which were commercialized as backplanes for display technology. Decreasing the fabrication temperature of transition metal oxides by choosing the right precursor or post deposition treatment like: Uv light, Microwave or high pressure assisted annealing enable the realization of high performance flexible transistors for biosensing applications. The gap between the performance of vacuum and solution processed metal oxide transistor is falling down opening the door for the large area electronics on a wide range of substrates. Although electrolyte gating doesn't improve the electrical properties of transistors significantly but decrease the operating voltage what is paramountly for biological

applications. The electrical characteristics of some main metal oxide transistors making use of conventional dielectrics and electrolytes are shown in the table 2.2.

Table 2-2 The electrical characteristics of some main metal oxide transistors.

MO	Method of deposition	Dielectric	Treatment temperature, °C	μ, cm^2/Vs	on/off	ref
ZnO	rf magn. sputt. at 10^{-6} Torr	SiO_2	110	40	10^3	70
ZnO	rf magn. sputt. at 10^{-5} Torr	SiO_2	110	1.6	10^6	70
ZnO	MOCVD	Al_2O_3	400	23.3	10^6	71
ZnO	solution processed	ATO(Al_2O_3+ TiO_2)	300	5.25	10^5	83
ZnO	spin coating	SiO_2	150	1.8	10^5	86
ZnO	printing	SiO_2	300	6	10^6	86
ZnO	solution processed	Al_2O_3/ZrO_2	180	11	10^4	85
ZnO	solution processed	Al_2O_3/ZrO_2	UV light	1	10^4	85
LiZnO	spray pyrolysis	ZrO_2	450	85	10^6	92
ZTO	spin coating	SiO_2	350	0.5	10^5	87
ZTO	spin coating	SiO_2	350, microwave assisted	1.8	10^6	87
ZTO	magnetron sputtering	ATO(Al_2O_3+ TiO_2)	300	15	10^7	75
ZTO	magnetron sputtering	ATO(Al_2O_3+ TiO_2)	600	50	10^7	75
a-IGZO	rf magnetron sputtering	SiN_x	RT	6.3	10^8	33
aIGZO	pulsed laser deposition	Y_2O_3	RT	8.3	10^3	60
In_2O_3	aerosol-jet-printing	([EMI][TFSI]) (PS-PMMA-PS)	400	≈ 11	10^6	94
In_2O_3	rf magnetron sputtering	[DEME]-[TFSI]	600			99
In_2O_3	inkjet printing	PVA, KF and deionized water	RT	0.8	10^3	98
In_2O_3	inkjet printing	PVA, KF and deionized water	400	120	10^7	95

ZnO	spray coating	[EMIM][FAP]; [BMIM] [FAP]	390	≈ 10	10^3-10^4	96
ZnO	spin coating	[BMIM] [TFSI]; [EMIM][TFSI]	390	≈ 5	10^3-10^4	96
ZnO	spin coating	[HMIM] [FAP]	390	≈ 16	10^3-10^4	96
ZnO	spin coating	[EMIM][TCB]	390	≈ 2	10^3-10^4	96
ZnO	spin coating	Water	450		10^2	97
ZnO	spin coating	PBS	450		10^3	97
ZnO	spin coating	Water	395	0.2	400	101
ZnO	aerosol-jet-printing	([EMI][TFSI]) (PS-PMMA-PS)	250	1.6	10^5	46
ZnO	spin coating	aqueous (KCl 0.1 M)	450	0.8	10^3	103
AlZnO	rf magnetron sputtering	Chitosan electrolyte		8.3	10^5	102
IGZO	rf magnetron sputtering	silica electrolyte film		5.9	10^7	104
IGZO	rf magnetron sputtering	electolyte	500	27	10^6	105
IZO	rf magnetron sputtering	nanogranual SiO_2 electrolyte		12	10^5	76
TiO_2	spin coating	NaOH+PVA; [EMIM][TFSI]	550		10^4	106
SnO_2 nanowire	vapor–liquid–solid growth	solid SiO_2 electrolyte	900	175	10^5	126
SnO_2 nanowire	vapor–liquid–solid growth	solid SiO_2 electrolyte		102	10^5	130

CHAPTER 3 ARTICLE 1: TIN DIOXIDE ELECTROLYTE-GATED TRANSISTORS WORKING IN DEPLETION AND ENHANCEMENT MODE

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3.2 Abstract

Metal oxides are interesting materials for next generation flexible and transparent electronics due to their electrical properties and reliability. Tin dioxide (SnO_2) is a very promising transparent material that has already found applications in sensing, photovoltaics, optoelectronics and batteries. In this work, we report on electrolyte-gated (EG) polycrystalline SnO_2 transistors both on rigid and flexible substrates. We used as the transistor channel material solution-processed films of SnO_2, both unpatterned and patterned. In the latter case, two different channel geometries were considered (with large and small patterns). Unpatterned transistors, with a channel thickness of about 150 nm, operate in enhancement mode whereas patterned transistors, with channel thicknesses of about 450 nm (small pattern transistors) and about 200 nm (large pattern transistors), operate in depletion mode. We observed operation in enhancement mode also for patterned transistors with low channel thicknesses. We believe that our SnO_2 transistors,

operating at sub-1 V range, are promising for low-cost, transparent, flexible and wearable electronics.

3.3 Introduction

Wide band gap metal oxides, such as ZnO, InZnO, and InGaZnO (IGZO) are promising materials for transparent and flexible transistors.[43, 46, 59, 60, 65, 114] The ideal application of metal oxide transistors is in display technologies, where IGZO-based backplanes have been introduced as an alternative to amorphous Si. In particular, metal oxide electrolyte-gated transistors are attractive for display backplanes because of their high driving current and low operation voltage. While the best performance is in principle achieved with vacuum- deposited materials, solution processing is attractive for flexible and large area electronics applications. One relevant property of these oxides is that their conduction band results from the overlap of large *ns* orbitals of metal cations with $(n\text{-}1)d^{10}ns^{0}$ (where $n \geq 5$, e.g. Sn^{4+}, with an electronic configuration of $(4d)^{10}(5s)^{0}$); this overlap is essentially the same in the crystalline and amorphous phases.[115]

SnO_2, an abundant and low-cost material, is a wide band gap (3.6 eV) oxide that is used, in its doped form, as a transparent conductor and as a solid-state gas sensing material.[116-118] The high electrical conductivity of SnO_2, mostly due to the tendency to form oxygen vacancies, [119, 120] typically leads to transistor operation in depletion mode. SnO_2 thin film transistors (TFTs) were reported by Klasens and later by Aoki.[10, 11] In 1996, Prins demonstrated Sb-doped SnO_2 ferroelectric TFTs with charge carrier concentration of 10^{18} cm^{-3} and electron mobility of 5 $cm^2V^{-1}s^{-1}$. SnO_2 films were obtained by pulsed laser deposition.[121] A much higher electron mobility (about 158 $cm^2V^{-1}s^{-1}$) was achieved in sputtered SnO_2 TFTs, highly doped with Sb.[73] Jang et. al demonstrated solution-processed SnO_2 TFTs with high electron mobility (about 100 $cm^2V^{-1}s^{-1}$) and low operating voltage (<1.5 V).[122] To achieve transistor operation in enhancement mode, essential for applications in display technologies, the intrinsic conductivity of SnO_2 needs to be decreased. Presley et al. achieved enhancement mode operation of SnO_2 TFTs by decreasing the SnO_2 film thickness down to 10-20 nm, achieving a mobility of 0.8 $cm^2V^{-1}s^{-1}$. The electron mobility for transistors working in depletion mode was 2 $cm^2V^{-1}s^{-1}$.[123] SnO_2 TFTs operated in enhancement mode, with an electron mobility around 96 $cm^2V^{-1}s^{-1}$ were later demonstrated by Huang et al.[124] Recently, TFTs based on SnO_2 nanowires and nanobelts have attracted interest

for sensors and transparent electronics.[125-128] Transistors consisting of SnO_2 nanowires doped with Ta showed electron mobility exceeding 100 $cm^2V^{-1}s^{-1}$.[125] In transistors consisting of Sb-doped SnO_2 nanowires, the electron mobility exceeded 500 $cm^2V^{-1}s^{-1}$. Further doping by increasing Sb/Sn ratio led to metallic conductivity.[129]

The charge carrier density in transistor channel materials can be modulated by electrolyte-gating. The high capacitance (typically higher than $\mu F/cm^2$), due to the presence of an electrical double layer at the electrolyte/channel interface, allows transistor operation at low voltages.[48-51, 55] Lightly Sb-doped SnO_2 nanowire transistors, making use of hydrated SiO_2 as solid electrolyte, showed an operating voltage of 1.5 V, with an electron mobility above 100 $cm^2V^{-1}s^{-1}$ and a current on/off ratio around 10^5.[126, 130]

In this work, we report on electrolyte-gated transistors based on solution-processed SnO_2 thin films, fabricated on flexible and rigid substrates. We investigated both unpatterned and patterned transistors, where patterning was achieved using an unconventional photolithography process.[55] Unpatterned transistors worked in in enhancement mode, whereas patterned devices worked in depletion mode. Enhancement mode of operation in patterned devices was achieved by substantially decreasing the thickness of the SnO_2 channel.

3.4 Results and discussion

3.4.1 Transistor fabrication and film characterization

We fabricated patterned and unpatterned SnO_2 EG transistors on SiO_2/Si and flexible polyimide (PI, Polyonics® XF-102) substrates. The latter are good candidates for flexible electronics applications that require processing temperatures up to 350 °C. SnO_2 films were obtained in ambient atmosphere by drop casting of a mixture containing $SnCl_4$ dissolved in methanol and concentrated acetic acid. We carried out a thermal treatment in ambient atmosphere at 450 °C for films on SiO_2 and 350 °C for films on PI. Using a procedure reported elsewhere [55], we prepared two types of patterns on SiO_2 (see Figure S1), one with a geometric area of 0.0025 cm^2 (small patterns, indicated as A) and another with a geometric area of 0.0492 cm^2 (large patterns, indicated as B). For unpatterned devices (indicated as C), the area of the membrane filter soaked in the electrolyte (9 mm × 4 mm = 0.36 cm^2) was taken as the geometric area. The average film

thickness was about 450 nm for patterns A, 200 nm for patterns B and 150 nm for unpatterned devices C. The higher thickness of patterns A and B can be explained by the meniscus-like effect induced by the patterned Parylene. Flexible unpatterned devices on PI (indicated as D), fabricated with the process shown in Figure 3.1 (see also experimental part), had a thickness of about 150 nm.

Unpatterned SnO_2 films on SiO_2, treated at 450 °C, are nanostructured; their cross section confirms that their thickness is about 150 nm (Scanning Electron Microscopy images in Figure S2). These films have a rather smooth surface with a root mean square (rms) roughness of about 1.5 nm (Atomic Force Microscopy images in Figure S2). On the other hand, SnO_2 films on SiO_2 treated at 350° C exhibit roughness values of about 18 nm (Figure S2). The X-ray diffraction (XRD) patterns of the films treated at 450 °C reveal the presence of the tetragonal phase, with crystallites of average size of about 9 nm, as calculated from the Scherrer equation; at 350 °C, both orthorhombic and tetragonal phases are present (Figure S3). XPS shows that the Sn/O ratio is 1/1.75 for films annealed at 450 °C and 1/1.64 for films annealed at 350 °C (Table S1): all the SnO_2 films are oxygen deficient, with the highest deficiency being observed at the lowest temperature.

The evaluation of the charge carrier mobility in EG transistors requires the knowledge of the transistor channel area. For nanostructured materials, the evaluation of the channel surface area is not straightforward. The use of the geometric channel area is likely not correct because it underestimates the active area of the channel and, hence, it leads to the overestimation of the charge carrier density. Assuming that the electrolyte ions completely wet the nanostructured SnO_2 films throughout their depth, a choice for the calculation of the channel surface area is the use of the specific surface area deduced from the Brunauer-Emmett-Teller (BET) analysis.[131] The BET specific surface area of SnO_2 films is 33 m^2/g for samples treated at 450 °C and 58.9 m^2/g for samples treated at 350 °C. By measuring the mass of the films, we deduced values of the surface areas of 0.62 cm^2 for A, 5.3 cm^2 for B, 33 cm^2 for C and 58.9 cm^2 for D (Table S2). On the other hand, the use of the BET specific surface area likely leads to the overestimation of the channel surface area, given that in the channel the SnO_2 film can aggregate in different manners with respect to the powders prepared for the BET analysis. Considering the nanostructured nature of our SnO_2 films, we believe that the values of the surface area deduced by BET analysis constitutes a more realistic estimation. As further investigations are required to assess which

approach is more appropriate for our nanostructured SnO_2 films, we calculated the charge carrier density and mobility values using both the channel surface area deduced from BET and the channel geometric channel area.

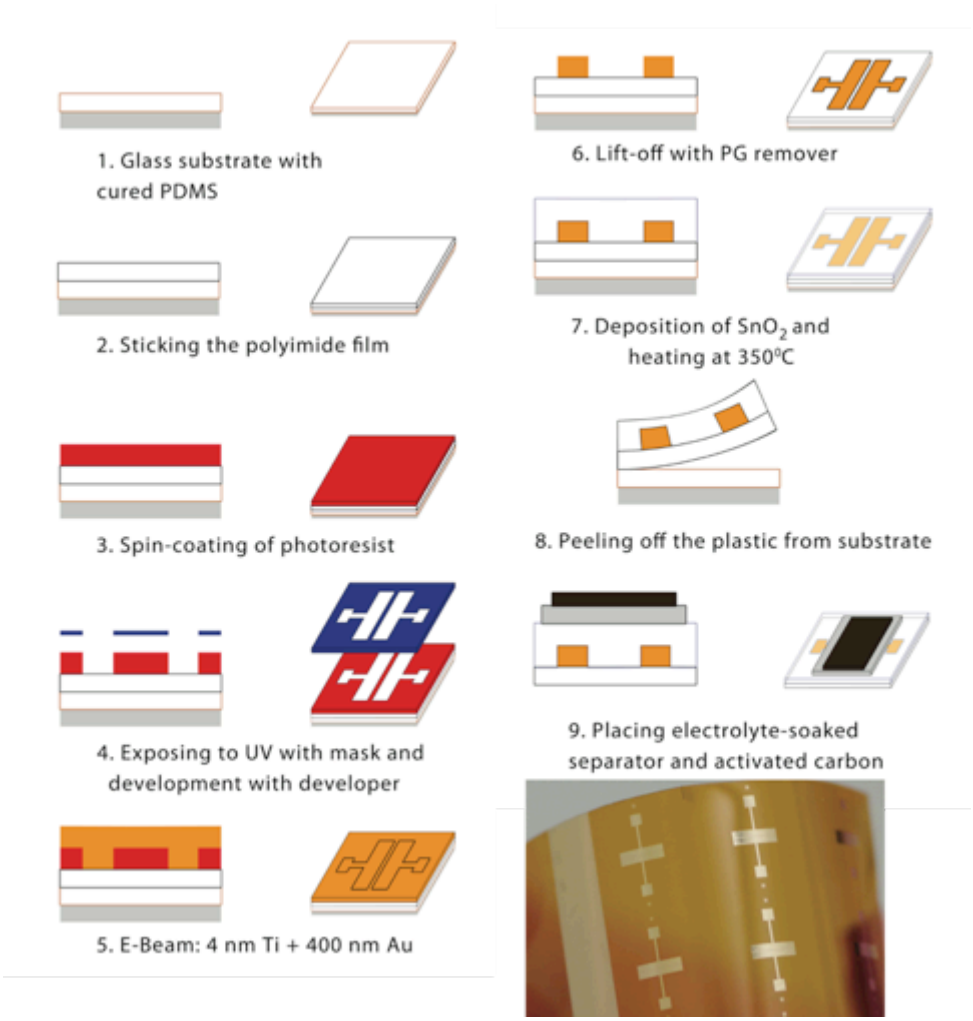

Figure 3-1: Process flow for the fabrication of SnO_2 EG transistors on flexible polyimide substrates and a photo of a final device (unpatterned flexible devices indicated as D). The geometric area of SnO_2 in contact with the electrolyte is 0.36 cm^2, i.e. the area of the Durapore® membrane filter soaked in the ionic liquid [EMIM][TFSI]. The thermal treatment temperature of SnO_2 film was 350 °C.

3.4.2 Electrical characterization of SnO_2 transistors

The characterization of the performance of the different SnO_2 EG transistors (Figures 3.2 and 3.3, Table S2) indicates that all transistors have n-type behavior and can be operated below |1 V|.

Interestingly, we observed that the transistor mode of operation, i.e. depletion vs enhancement, depends on the device geometry and film thickness. Patterned transistors (A and B) operate in depletion mode and typically turn off by applying a bias of about -1 V. The depletion mode of operation is typical of highly conductive SnO_2 transistor channels.[119, 120] We observed a change of the operation mode from depletion to enhancement by decreasing the thickness of the SnO_2 films from 450 nm to 10 nm for small pattern transistors and from 200 nm to 25 nm for large pattern transistors (Figure S4 and Table S2, where devices based on 10 nm-thick films with pattern A are indicated as transistors A1 and devices based of 25 nm-thick films with pattern B are indicated as transistors B1).

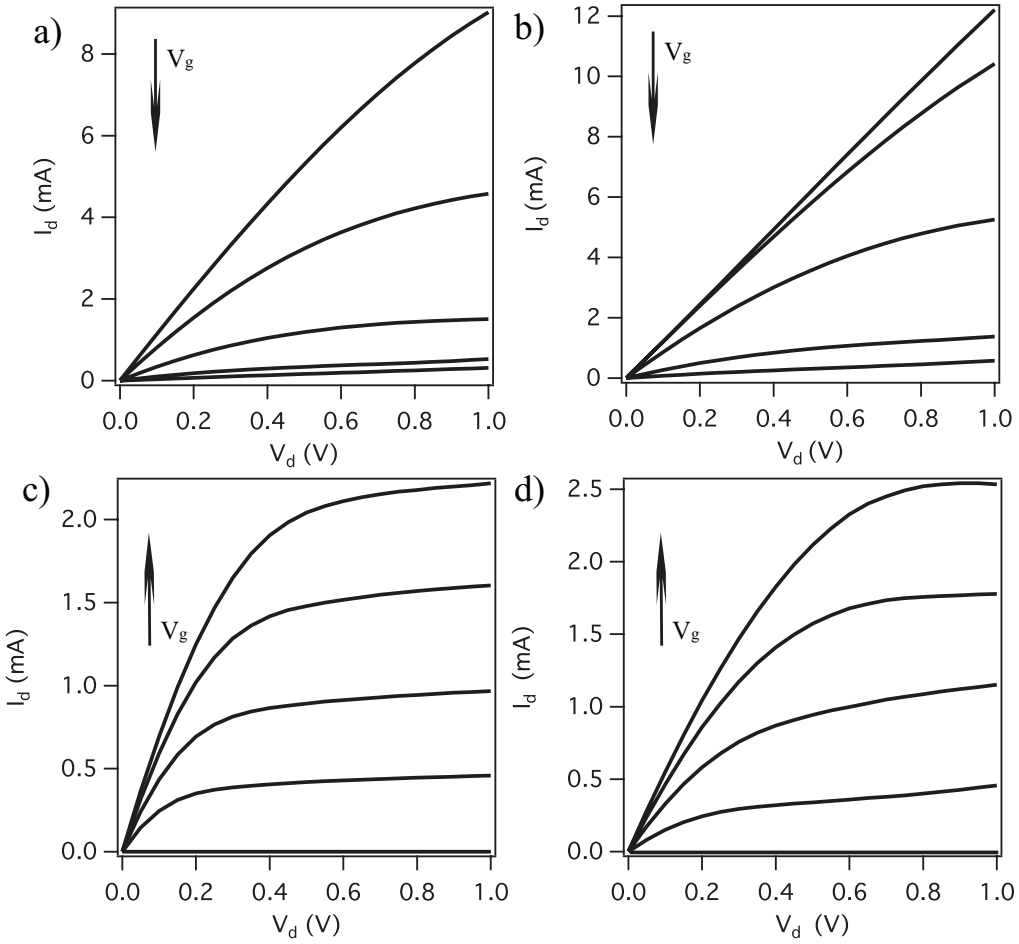

Figure 3-2: Output characteristics of different types of [EMIM][TFSI]-gated SnO_2 transistors (scan rate 50 mV/s). Patterned devices on Si/SiO_2: a) type A and b) type B, with V_g varying from 1 V to -1 V with steps of 0.5V. Unpatterned SnO_2 transistors on Si/SiO_2 and flexible substrates: c) type C and d) type D, at V_g =0V, 0.3V, 0.5V, 0.7V, 1V.

On the other hand, unpatterned transistors (C and D) on SiO_2 and PI substrates operate in enhancement mode. The transition from depletion to enhancement mode of operation is likely associated to a decreased channel thickness, paralleled to an increased resistance of the channel (Figure S5). The on/off ratio (deduced from the transfer characteristics in the saturation regime) is higher for unpatterned devices C and D, operating in enhancement mode, due to their low off current with respect to A and B (Figures S6 and Table S2). As expected, the threshold voltage (V_t), extracted from the transfer curves ($\sqrt{I_d}$ vs V_g) in the saturation regime, is positive for devices operating in enhancement mode and negative for devices operating in depletion mode. The hysteresis is almost negligible in unpatterned devices whereas it is high in patterned ones. This effect is likely due to a poorer contact between the electrolyte membrane and the channel, due to the presence of the photoresist insulator on the Au contacts (Figure S4).

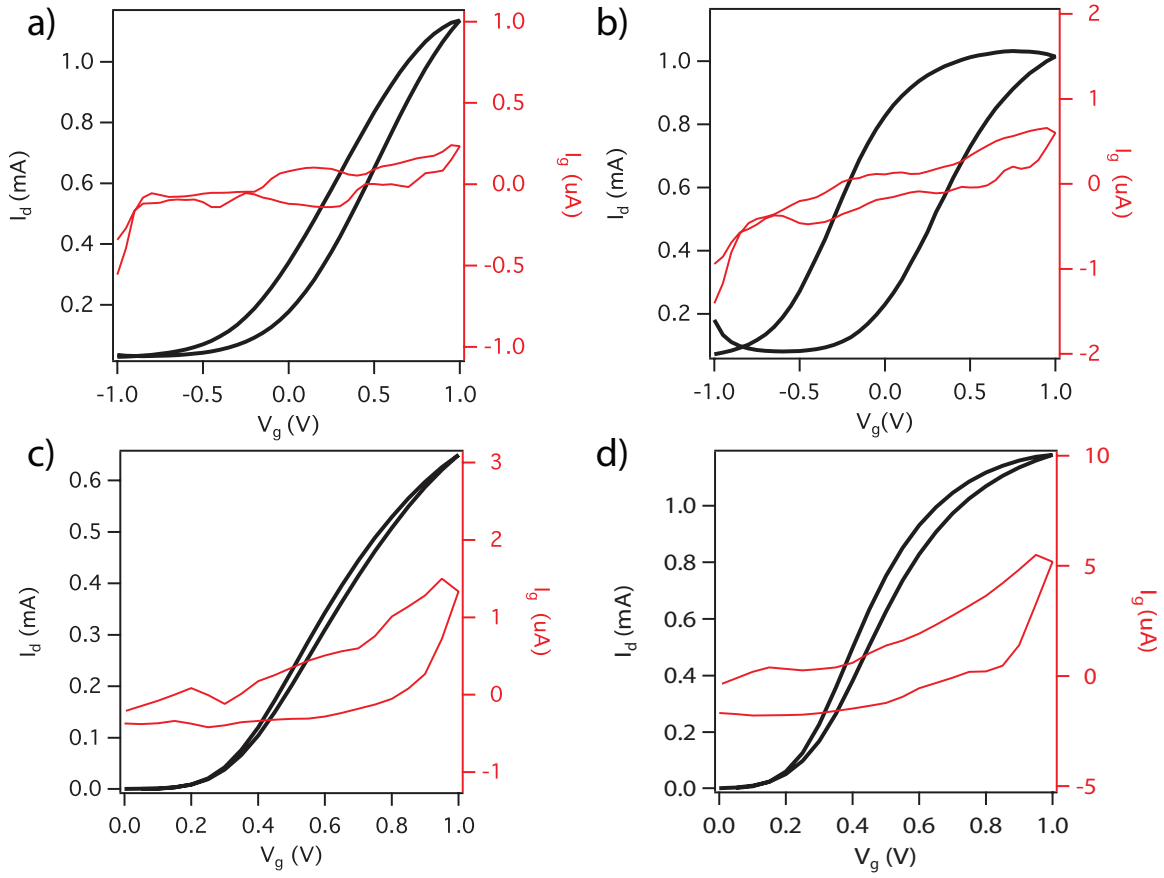

Figure 3-3: Transfer characteristics in the linear regime of [EMIM][TFSI]-gated SnO_2 transistors at V_d=0.2 V. Devices working in depletion mode: a) small pattern A and b) large pattern B. Devices working in enhancement mode: c) unpatterned transistors C and unpatterned transistors D. Scan rate 50 mV/s.

Assuming that for every cation of the electrical double layer at the electrolyte/SnO_2 interface one electron is induced in the SnO_2, we deduce that the doping charge is $Q = \frac{\int I_g dV_g}{r_v}$, where I_g is the gate-source current and r_v is the scan rate of the gate-source potential (Figure 3.3).[132] The charge carrier density, n, is then obtained by $n = \frac{Q}{e\,A}$, where e is the elementary charge and A the surface area of the semiconductor in contact with the electrolyte. For patterned transistors, the charge carrier densities calculated using the BET specific surface area, in the V_g range included between -1 V and 1 V, are ~$9 \cdot 10^{12}$ cm^{-2} (small pattern A) and ~$1.5 \cdot 10^{12}$ cm^{-2} (large pattern B), in agreement with the different extension of the patterning in the two cases. For unpatterned transistors, for 0 V<V_g<-1 V, the charge carrier densities, calculated using the BET specific surface area, are ~$1 \cdot 10^{12}$ cm^{-2} (unpatterned C) and ~$4 \cdot 10^{12}$ cm^{-2} (unpatterned D). On the other hand, the charge carrier densities calculated using the geometric area are ~$2 \cdot 10^{15}$ cm^{-2} (type A), ~$2 \cdot 10^{14}$ cm^{-2} (type B), ~$1 \cdot 10^{14}$ cm^{-2} (type C) and ~$6 \cdot 10^{14}$ cm^{-2} (type D). These results show that the charge carrier density dramatically depends on the method selected to evaluate the surface area (BET analysis vs geometric area).

We evaluated the charge carrier mobility in the linear regime (μ_{lin}) using the relationship: $\mu_{lin} = \frac{L\, I_{d,lin}}{W\, e\, n\, V_d}$, where L is the interelectrode distance, W the electrode width, $I_{d,lin}$ the drain-source current in the linear regime of the transfer characteristics (Figure 3.3). Using the charge carrier density deduced from the BET analysis, for devices working in depletion mode, we extracted values of the electron mobility of 10±2 $cm^2/V \cdot s$ for devices A and 40±10 $cm^2/V \cdot s$ for devices B (see Table S2). For devices working in enhancement mode, we extracted an electron mobility of 45±15 $cm^2/V \cdot s$ for devices C and 25±5 $cm^2/V \cdot s$ for devices D. These values are quite interesting for solution-processed SnO_2 films working in depletion and enhancement mode. The higher electron mobility of devices B and C with respect to devices A is a likely consequence of the lower charge carrier density for large pattern (B) and unpatterned (C) devices. The different charge carrier density and mobility values observed for unpatterned devices C and D are likely due to the lower thermal treatment temperature used for films on flexible substrates, which is expected to lead to a lower degree of crystallization and to the presence of voids and defects (Figure S2 and Figure S3).[120, 133] We obtain similar values of the electron mobility using pseudo capacitance values extracted from cyclic voltammetry (see SI). The electron mobilities deduced using the geometric surface area are 0.04±0.05 $cm^2/V \cdot s$ (type A), 0.4 ±0.2 $cm^2/V \cdot s$ (type

B), 0.6 ±0.2 $cm^2/V·s$ (type C) and 0.16±0.10 $cm^2/V·s$ (type D), which are remarkably lower with respect to the values obtained using the surface area deduced from BET analysis.

3.4.3 Electrochemical characterization of SnO_2 films

We carried out a cyclic voltammetry survey in the transistor configuration of patterned and unpatterned SnO_2 films on Si/SiO_2 and PI substrates in the [EMIM][TFSI] electrolyte (Figure 3.4, Figure S7). The current density in the cyclic voltammetry plots was calculated by normalizing the voltammetric current to the values of the BET surface areas of the SnO_2 films. For the voltammetric experiments, we used a two-electrode configuration, where the SnO_2 film, included between the source and drain electrodes, acted as the working electrode whereas the carbon gate (specific capacitance of about 100 $F·g^{-1}$) acted simultaneously as the counter and quasi reference electrode.[48, 49, 55, 134] Cathodic and anodic redox processes are observable upon scans of the electrode potential in the range between 1 V and -1V vs carbon quasi reference electrode. For patterned devices (A and B), cathodic currents are observable from about 0.5 V to -1 V and anodic currents from -0.7 to 1 V. The anodic activity of patterned devices in the positive potential range correlates with the operation of the corresponding transistors in depletion mode. For unpatterned devices, shoulder-like signatures are observable in the voltammogram from 0 V to -1 V (C and D). Anodic broad peaks are observable at about -0.65 V and -0.4 V for C and D type of transistors, respectively.

For our SnO_2 films in B, C, D configurations (i.e. large pattern and unpatterned devices), the value of the voltammetric cathodic current at -0.5 V vs a carbon reference electrode increases linearly with the square root of the potential scan rate, indicating the diffusion-limited response of these films (Figure S8). On the other hand, a linear dependence of the current with the scan rate is observed for devices of type A (small pattern), suggesting that the electrochemical processes are (pseudo)capacitive in these highly conductive films.[135]

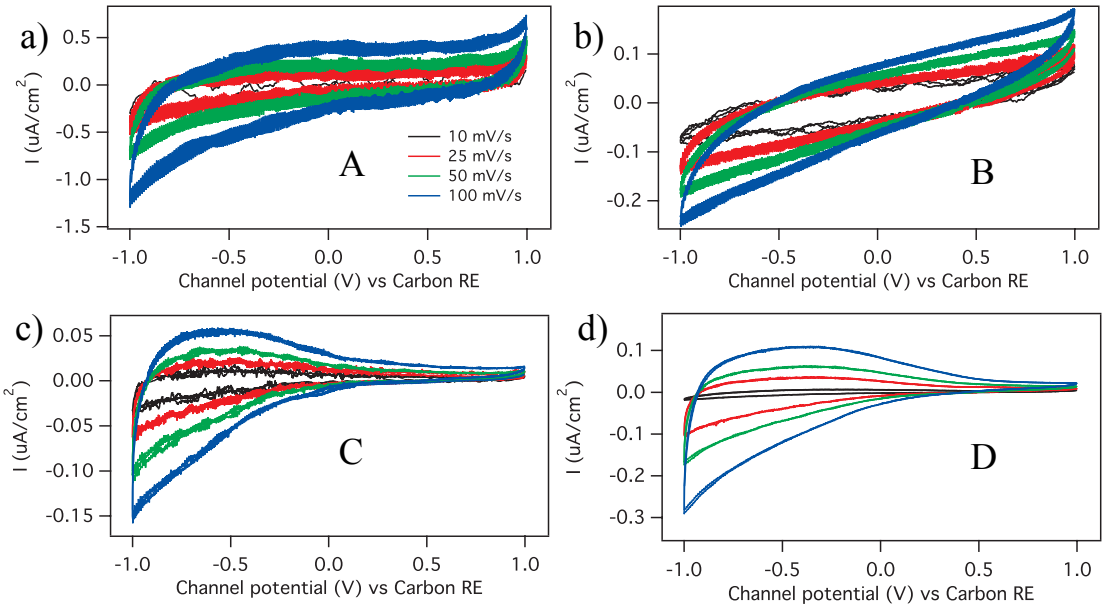

Figure 3-4: Cyclic voltammetry of SnO_2 films in transistor configuration for the patterned and unpatterned devices a) A, b) B, c) C, and d) D (see main text) in the electrolyte [EMIM][TFSI], at scan rates 10, 25, 50, 100 mV/s. The current is normalized to the surface area of the SnO_2 films as deduced using the results of the BET measurements for the specific surface area.

3.4.4 Electrical characteristics under mechanical deformations

We studied the characteristics of SnO_2 flexible EG transistors under bending, to explore their possible applications in flexible electronics. The devices were bent on surfaces with curvature radius (R) of 30 mm and 10 mm.

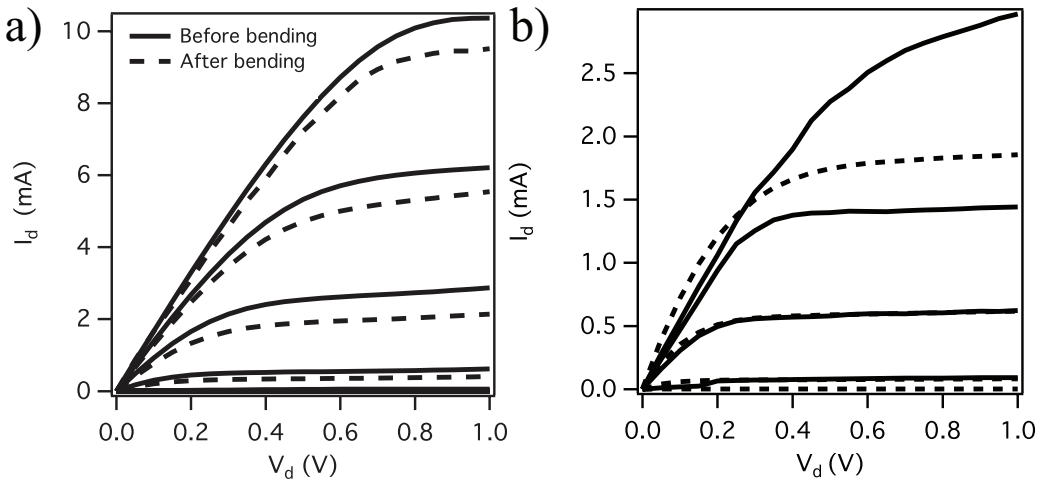

Figure 3-5: Output characteristics of [EMIM][TFSI]-gated SnO_2 transistors on polyimide, under bending at: a) R=30 mm and b) R=10 mm. V_g = 0 V, 0.3 V, 0.5 V, 0.7 V, 1 V. Scan rate 50 mV/s. The thermal treatment temperature of SnO_2 films is 350 °C.

Devices measured before bending and under a first bending at R=30 mm (corresponding to the tensile strain ε=0.002%, where $\varepsilon = \frac{(d_f+d_s)}{2r} \times 100\%$, with d_f the thickness of the film, d_s the thickness of the substrate and r the bending radius[136]) have similar output characteristics (Figure 5). Under bending on a surface with R=10 mm (corresponding to the tensile strain ε=0.125%), devices show a decrease in the transistor current and an increase in the threshold voltage from 0.3 V to 0.5 V (Figure S9). Similar results are obtained after several bending cycles.

3.5 Conclusion

We fabricated, both on rigid and flexible substrates, electrolyte-gated (EG) SnO_2 transistors making use of high surface area activated carbon as the gate electrode and [EMIM][TFSI] as the gating medium. Solution-processed thin films of SnO_2 have been drop casted and photolithographically patterned as transistor channel materials. Unpatterned transistors operated in enhancement mode whereas patterned transistors, characterized by high off currents, operated in depletion mode. The enhancement mode of operation was achieved in patterned transistors only by decreasing the thickness of the SnO_2 films. Values of the electron mobility as high as 45 cm^2/Vs were observed for unpatterned transistors, when the SnO_2 surface area was deduced by the Brunauer-Elmett-Teller analysis. SnO_2 transistors fabricated on flexible polyimide substrates possess good performance, even under bending conditions. Our ongoing work aims at fabricating SnO_2 fully transparent EG transistors, not requiring high temperature thermal treatments, for transparent and flexible applications.

3.6 Materials and methods

3.6.1 Processing of SnO_2

0.45 ml of anhydrous tin (IV) chloride ($SnCl_4$) (Sigma Aldrich #208930) were added to a solution of 50 ml of methanol (CH_3OH) and 0.95 ml of glacial acetic acid (CH_3COOH, Caledon Laboratory Chemicals) inside a N_2 glove box (O_2 and H_2O<5 ppm). The mixture was stirred for 30 minutes to get a clear solution. To obtain thin SnO_2 films (devices A1 and B1), the volumes of $SnCl_4$ and acetic acid (CH_3COOH) were decreased to 4.5 ul and 9.5 ul, respectively.

3.6.2 Flexible transistor fabrication

For the fabrication of flexible transistors, a glass slide was covered with a thin PDMS layer and a PI sheet was attached to it to ensure rigidity during the photolithography process. After patterning of the gold contacts, the SnO_2 solution was drop cast on the substrate, which was heated at 350 °C for 1 h, in ambient conditions. The transistor fabrication was completed by placing, on the top of the SnO_2 channel, a Durapore® membrane filter soaked with the ionic liquid [EMIM][TFSI] electrolyte and an activated carbon gate electrode (6 mm×3 mm×170 μm).

3.6.3 Purification of the ionic liquid

The ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide [EMIM][TFSI] was purchased from IoLiTec Inc. The viscosity of [EMIM][TFSI] is 39.4 mPa·s, at 20 °C and the ionic conductivity 6.63 $mS \cdot cm^{-1}$ (data provided by IoLiTec Inc). Prior to use, [EMIM][TFSI] was purified under vacuum (~10^{-5} Torr), at 80 °C, for about 24 hours and transferred inside the N_2 glove box.

3.6.4 Fabrication of the activated carbon (AC) electrodes

Activated carbon was chosen for its surface area, highly desirable to achieve high current modulation, and it capability to limit undesirable electrochemical reactions (detrimental for device stability).[48, 137] AC gate electrodes consisted of carbon paper (Spectracorp 2050) coated with a suspension containing activated carbon (PICACTIF SUPERCAP BP10, Pica, 28 mg ml^{-1}) and polyvinylidene fluoride (PVDF, KYNAR HSV900, 1.4 mg ml^{-1}) in N-methyl

pyrrolidone (NMP, Fluka, >99.0%). The coating was followed by thermal treatment at 60 °C for 5 hours in vacuum to remove solvent and water traces.

3.6.5 Morphology and structure of SnO_2 films

Film thickness was measured with a stylus profilometer Dektak 150. Scanning Electron Microscopy was performed with a JEOL FEG-SEM, JSM 7600F Scanning Electron Microscope. The structure of the SnO_2 films was investigated by X-ray diffraction with a Bruker D8 diffractometer using a (Cu Kα) beam. X-ray scans were measured every $2\theta = 0.01$ and the time per step was 0.6 sec.

3.6.6 Surface area measurements

Brunauer-Emmett-Teller (BET) single point specific surface area measurements were performed with an Autochem II 2920 Micrometrics, equipped with a TCD detector.

3.6.7 Transistor and electrochemical characterization

Transistor characterization was performed in a N_2 glove box (O_2 and H_2O<5 ppm) using a micromanipulated electrical probe station and a semiconductor parameter analyzer (Agilent B1500A). Electrochemical characterization was performed using a PARSTAT 2273 (Princeton Applied Research) multichannel potentiostat.

3.7 Acknowledgments

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CHAPTER 4 ARTICLE 2: PHOTOLITHOGRAPHICALLY PATTERNED TIO_2 FILMS FOR ELECTROLYTE-GATED TRANSISTORS

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4.2 Abstract

Metal oxides constitute a class of materials whose properties cover the entire range from insulators to semiconductors to metals. Most metal oxides are abundant and accessible at moderate cost. Metal oxides are widely investigated as channel materials in transistors, including electrolyte-gated transistors, where the charge carrier density can be modulated by orders of magnitude upon application of relatively low electrical bias (sub-2 V). Electrolyte gating offers the opportunity to envisage new applications in flexible and printed electronics as well as to improve our current understanding of fundamental processes in electronic materials, e.g. insulator/metal transitions. In this work, we employ photolithographically patterned TiO2 films

as channels for electrolyte-gated transistors. TiO_2 stands out for its biocompatibility and wide use in sensing, electrochromics, photovoltaics and photocatalysis. We fabricated TiO_2 electrolyte-gated transistors using an original unconventional parylene-based patterning technique. By using a combination of electro-chemical and charge carrier transport measurements we demonstrated that patterning improves the performance of electrolyte-gated TiO_2 transistors with respect to their unpatterned counterparts. Patterned EG TiO_2 transistors show threshold voltages of about 0.9 V, ON/OFF ratios as high as 1×10^5, and electron mobility above 1 $cm^2/(V\ s)$.

Keywords: titanium dioxide, electrolyte gating, transistors, ionic liquids, patterning

4.3 Introduction

Electrolyte-gated transistors (EGTs), making use of electrolytes as the gating media, can be operated at low voltage (below 2 V). They are currently investigated for applications in bioelectronics and printable and flexible electronics. EGTs can make use of a large number of electrolytes, including aqueous saline solutions, polymer electrolytes, ionic liquids and ion gels [51, 138], and channel materials, such as organic semiconductors [48, 50, 51, 93, 132, 138-143], metal oxides [46, 49, 58, 95, 96, 112, 126, 144], InN, CdSe, and PbSe.[145-147]

Metal oxides can be used as transistor channels for active matrix displays, injection layers in light-emitting diodes, transparent conductive electrodes and electrode materials for energy conversion and storage.[27, 148] Among metal oxides, TiO_2 stands out for its wide use in solar energy conversion, photocatalysis and electrochromics.[148-150] TiO_2 is a low-cost, abundant and biocompatible material, widely used as white pigment for paper, plastic and food processing. The possible effects on human health of TiO_2 used in food processing and healthcare products are currently under investigation.[151]

Rutile and anatase are common, widely investigated polymorphs of TiO_2.[152] Crystalline and amorphous TiO_2 have been employed as n-type channel material in field-effect and EG transistors.[106, 107, 153-157] Polycrystalline anatase films have been used to explore the effect

of the concentration of electrolyte ions on the working mechanism of EGTs.[106] In EGTs making use of slightly doped epitaxially grown TiO_2 a metal-insulator transition has been observed.[107]

The modulation of the charge carrier density in EGTs can be achieved via different mechanisms, e.g. electrostatic and/or electrochemical, depending on the nature of the channel material and the electrolyte. The formation of electrical double layers (EDLs) at the interface between electrolytes and ion-impermeable semiconductors is at the basis of the electrostatic doping mechanism. Upon application of an electrical bias at the gate electrode, an EDL forms at the electrolyte/semiconductor channel interface. The high capacitance of EDLs (typically in the range of several $\mu F/cm^2$) permits the operation of the transistors at low electrical bias. On the other hand, when semiconductors are permeable to ions, current modulation is achieved by electrochemical doping via reversible charge transfer (Faradaic) processes. EGTs based on nanostructured mesoporous WO_3 films, easily permeated by electrolytes, have been recently reported by some of the authors. Based on electrochemical and transistor device characterizations, the co-existence of at least two contributions to the doping has been proposed: interface-confined electrochemical doping and electrostatic doping.[49]

Despite the impressive progress in the field of EGTs, the role played by the extension of the electrolyte/semiconductor and electrode/semiconductor interfaces on the doping and charge carrier transport processes has not yet been fully investigated. The extent of the overlap between the semiconductor and the electrolyte, in turn in ionic contact with the gate electrode, is expected to affect the charge carrier density in the channel upon doping. The overlap between the metal electrodes and the semiconductor, which is in contact with the electrolyte, might affect the charge injection process. Novel device architectures achieved by patterning the EGT channel represent a crucial tool to control gating (electrolyte/semiconductor) and charge injecting (electrode/semiconductor) interfaces, leading to a better understanding of the fundamentals of injection and doping as well as to improved device performance.[158, 159]

In this work, we report on photolithographically patterned EGTs based on solution-processed nanostructured TiO_2 films. Patterning was achieved using an unconventional photolithography process, based on the use of parylene. We investigated two different patterns. In the former, the TiO_2 film overlaps with a small area at the edges of the source and drain electrodes, while in the latter it overlaps with most of the electrodes' area. By comparing the electrochemical (cyclic voltammetry and electrochemical impedance spectroscopy) and electrical characteristics of patterned films with unpatterned ones, we propose an extended correlation between the extension of electrolyte/metal oxide and electrode/metal oxide interfaces, electrical double layer capacitance, charge carrier density and mobility in TiO_2 nanostructured films.

4.4 Results and discussion

4.4.1 Patterning and Fabrication of the Devices

To pattern TiO_2 films, we used an unconventional photolithography technique based on the use of parylene (Figure 4.1), similar to other processes developed for organic materials.[142] TiO_2 patterning with conventional additive or subtractive photolithography, using lift-off or etching, is not compatible with the conditions commonly required to deposit TiO_2 films. A lift-off process after the thermal treatment required to process TiO_2 films[149] would be rather problematic, due to thermally induced photoresist crosslinking. Similarly, TiO_2 etching would be challenging due to the exceptional TiO_2 chemical stability. A ParyleneC film (1 μm-thick) was deposited on a SiO_2 substrate pre-patterned with Au electrodes (interelectrode distance, L = 10 μm, electrode width, W = 4000 μm, electrode area 4000 μm×600 μm, see Experimental), after spin-coating a surfactant solution (cetyl trimethylammonium bromide, CTAB, 10^{-3} M in H_2O) to facilitate subsequent peel-off. A positive-tone photoresist (MEGAPOSIT^{TM} SPR 220 3.0) was spin coated on the ParyleneC film, exposed through a photomask and developed, thus leaving unprotected ParyleneC over a region including the transistor channel and part of the Au electrodes. The unprotected ParyleneC was removed by oxygen reactive ion etching. After removal of the unexposed photoresist, TiO_2 films were deposited on the patterned ParyleneC by drop casting (see Experimental) and treated first at 40 °C for 30 min, then at 100 °C for 1 hour, to remove the excess solvent. Afterwards, the ParyleneC film was peeled off, leaving the patterned TiO_2 film,

which was treated at 450 °C for 1 hour, in ambient air (see Figure S2c for morphology after Parylene peel off). Two patterns were obtained: one where the TiO_2 film overlapped with the electrode edges (20 μm over each gold electrode) and another one where the TiO_2 film extended over most of the electrodes (about 500 μm over each gold electrode). The TiO_2 geometric area is about 0.0025 cm^2 for smaller patterns, indicated as A, and 0.0492 cm^2 for larger ones, indicated as B. These two different patterns result in a different overlap of TiO_2 film with both the source/drain electrodes and the electrolyte. A final patterning step was performed to protect the Au electrodes with photoresist, to prevent their direct contact with the electrolyte. For the sake of comparison, we also fabricated unpatterned devices, which are indicated as C and have a geometric area of 0.36 cm^2. The average thickness of the TiO_2 films was 3.2 μm±0.7 μm for unpatterned films, 4.4 μm±0.2 μm for films of type B and 6.8 μm±0.7 μm for films of type A, as deduced from 3 samples (for each type of sample, A, B and C) with 8 different measurements on each sample. The higher thickness of the patterns A and B can be explained by a meniscus-like effect induced by the patterned parylene. Device fabrication was completed in a N_2-purged glove box by sequentially placing, on top of the TiO_2 channel, a Durapore® membrane filter (area 0.36 cm^2) soaked in the ionic liquid [EMIM][TFSI] electrolyte and an activated carbon gate electrode (Figure S1 and Experimental). [EMIM][TFSI] is a well-investigated room temperature ionic liquid with low viscosity and high conductivity (see Experimental). The choice of activated carbon for the gate electrode stems from its capability to limit undesirable electrochemical reactions (detrimental for device stability) and its high surface area, highly desirable to achieve high current modulation.[48, 137]

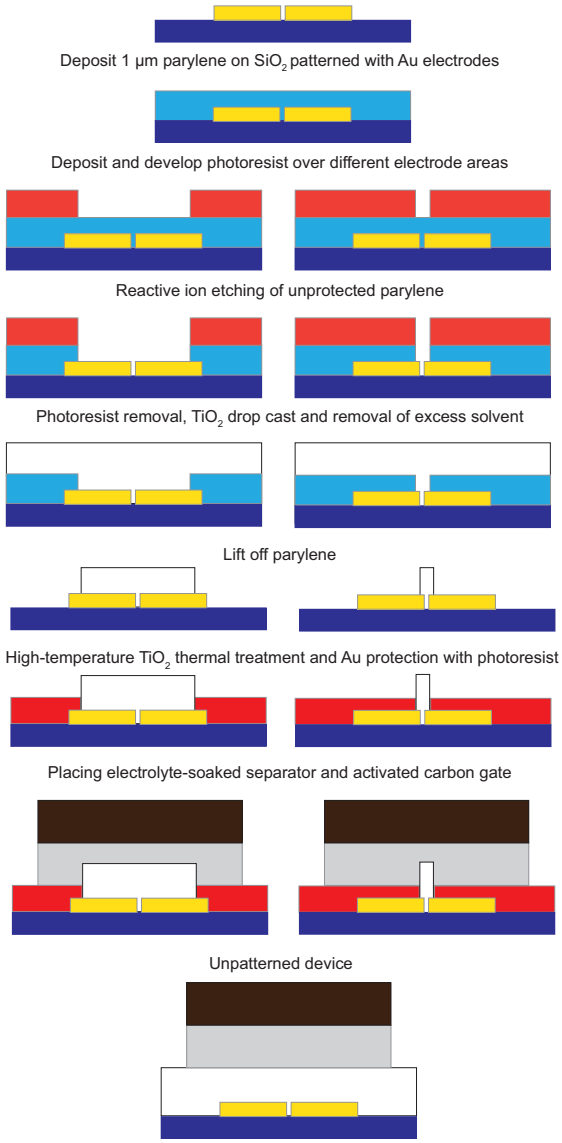

Figure 4-1: Steps for device fabrication including patterning of TiO_2 films with ParyleneC. Two types of patterns were used: covering the transistor channel and overlapping 20 μm over each Au electrode (pattern A, TiO_2 geometric area of 0.0025 cm^2); covering the transistor channel and overlapping about 500 mm over each Au electrode (pattern B, TiO_2 geometric area of 0.0492 cm^2). Unpatterned devices were used for the sake of comparison (sample C, geometric area of 0.36 cm^2). [EMIM][TFSI], soaked in a membrane filter (Durapore®, 9 mm×4 mm×125 μm), is used as the electrolyte. Activated carbon (6 mm×3 mm×170 μm) acts as the gate.

4.4.2 Electrochemical characterization of TiO_2 films

We carried out a cyclic voltammetry (CV) survey on patterned and unpatterned TiO_2 films (structure and morphology shown in Figure S2) in the electrolyte [EMIM][TFSI], to map their redox activity. We used a two-electrode configuration, where the TiO_2 film, included between the source and drain electrodes, acted as the working electrode whereas the carbon gate (specific capacitance of about 100 $F \cdot g^{-1}$) acted simultaneously as the counter and quasi reference electrode.[48, 137, 143]

Cathodic and anodic redox processes are observable upon scans of the electrode potential in the range between -0.5 V and -1.5 V vs. carbon quasi reference electrode (Figure 4.2 and Figure S3). The cathodic current starts to increase at -0.7 V and a shoulder is observable at about -1.2 V. During the anodic scan, a relatively wide anodic peak is observable, located at about -1.25 V. The current density in the cyclic voltammetry plots (Figure 4.2) was calculated by normalizing the voltammetric current (Figure S3) to the values of the surface areas of the TiO_2 films (170 cm^2 for C, 29 cm^2 for B and 2.2 cm^2 for A, see Experimental). It is worth noticing that, for a fixed scan rate, the voltammetric current increases with increasing surface area of the TiO_2 films (Figure S3), whereas the current density follows an opposite trend (sample A has the highest current density and the lowest surface area). The plot of the anodic peak current vs. scan rate (Figure S3) has a quasi linear behavior, thus indicating the pseudocapacitive response of our TiO_2 films.[160]

The pseudocapacitance at the TiO_2 film/electrolyte interface was calculated from the slope of the (linear) plot of the doping charge (deduced by the integration of the voltammetric current over time) vs. potential (see Table S1 for sweeping rate dependence of the pseudocapacitance). With a sweeping rate of 50 mV/s we obtained 0.17 mF for C, 0.070 mF for B and 0.023 mF for A. Considering the surface area of our TiO_2 patterns, these values yielded pseudocapacitance densities of 0.001 mF/cm^2 for C, 0.0024 mF/cm^2 for B and 0.01 mF/cm^2 for A. As expected from the trend of the current density, these results show that the pseudocapacitance density increases with decreasing surface area of the TiO_2 films. This means that, although large surface area films are able to store more charge, small surface area ones (e.g. films of type A) are able to store more charge per unit surface area. This observation can be tentatively explained by considering that the miniaturization of the TiO_2 patterns from sample C to B and A, leads to a condition similar to that of microband electrodes. Here, a rapid edge diffusion at the electrode/electrolyte interface, leading to high voltammetric current densities, is observed (as opposed to commonly encountered

linear diffusion).[160]

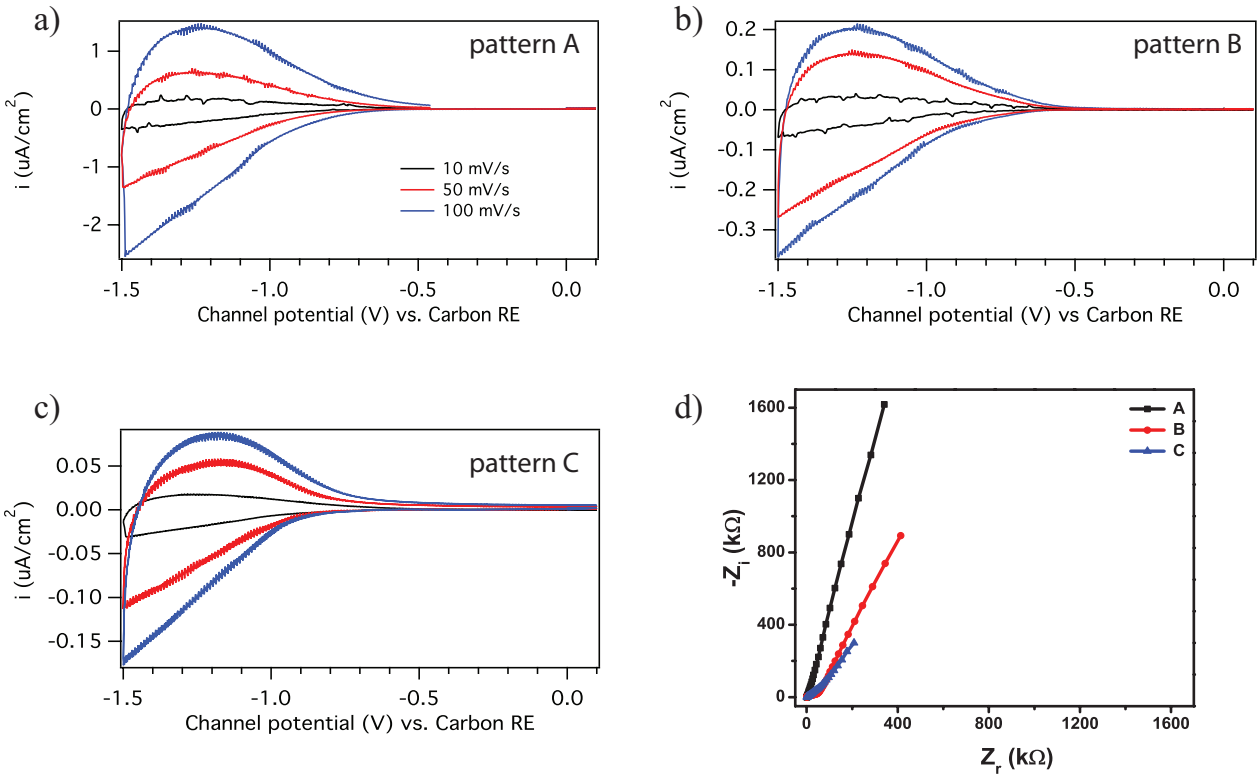

Figure 4-2: Cyclic voltammetry of TiO_2 films of different geometric areas and surface areas (see main text): a) A; b) B c) C, in the electrolyte [EMIM][TFSI], at different sweeping rates (see legend). A TiO_2 film included between source and drain electrodes acts as the working electrode and the carbon gate acts as the counter and the quasi reference electrode. The current is normalized to the surface area of the TiO_2 films in contact with the electrolyte. d) Nyquist plots obtained in transistor configuration using TiO_2 films of different surface areas included between source and drain as the working electrode and carbon as the counter and quasi reference electrode; the measurements were carried out at 1 V vs carbon quasi reference electrode, using [EMIM][TFSI] as the electrolyte.

The cyclic voltammetry response of our TiO_2 films points to a doping mechanism including a pseudocapacitive contribution. A pseudocapacitive contribution has the electrochemical signature of a capacitive one (i.e. linear dependence of the charge stored with the width of the potential excursion). In particular, in pseudocapacitive processes, the charge storage originates from faradaic processes rather than from purely electrostatic ones.[161, 162] In principle, electrochemical doping implies redox processes paralleled by insertion of ions within the bulk of

the material being doped, to ensure the electroneutrality.[163] Nevertheless, for TiO_2 transistors gated by the [EMIM][TSFI], the relatively large size of the [EMIM] cation (whose theoretically deduced radius is 3.5 Å) limits its insertion into the crystal lattice of TiO_2.[164-166] Only small cations such as H^+ and Li^+ can be intercalated through the "zig-zag" rows formed at edge-shared octahedra of the tetragonal form of anatase.[167] In agreement with that, we hypothesize that redox processes responsible for electrochemical doping are confined at the interface between the electrolyte and the high surface area TiO_2 film.[49]

We performed electrochemical impedance spectroscopy (EIS) in the 10 kHz - 0.01 Hz frequency range, at 1 V vs carbon quasi reference electrode, with a perturbation of 10 mV, using the same experimental configuration as in cyclic voltammetry. The Nyquist plots (Figure 2d) show straight lines almost parallel to the imaginary axis that indicate a capacitive behaviour of the TiO_2 films. The capacitance values were calculated taking the imaginary part of the impedance (Z_i) at the lowest frequency (f=0.01 Hz), using the relationship $C=1/(Z_i \times 2\pi \times f)$. The capacitance, extracted from EIS measurements, is higher for films with higher surface area (~0.05 mF for C, 0.017 mF for B and 0.009 mF for A). However, the capacitance density (obtained considering the surface area) decreases with increasing the surface area of the TiO_2 films (~ 0.0045 mF/cm^2 for A, 0.0006 mF/cm^2 for B and 0.0003 mF/cm^2 for C), thus following the same trend as the capacitances deduced from cyclic voltammetry. The phase angle estimated at low frequency is 78° for samples A, 65° for samples B and 55° for C (Figure S4). A phase angle at low frequency of 90° corresponds to a purely capacitive response, whereas a diffusion-controlled process typically gives a Warburg element with a 45° phase angle.[96, 168, 169] This indicates that ion diffusion is faster for films of smaller surface area (A>B>C), in agreement with the microband hypothesis discussed above.

4.4.3 TiO_2 transistors and role of patterning

We performed the electrical characterization of TiO_2 EG transistors making use of films of types A, B and C (Figure 3). The output and transfer characteristics show, as expected, n-type semiconductor behaviour, when the transistors are operated in accumulation mode. It is worth noticing that for patterned TiO_2 films (types A and B) the transistor behaviour could be observed only when the Au electrode pads were protected from a direct contact with the electrolyte prior to measurements. Indeed, the contact between the electrode and the electrolyte adds a capacitive

contribution to the transistor current, due to the formation of electrical double layers at the electrode/electrolyte interface, which prevents an unambiguous interpretation of the drain-source current. The transistor current increases by decreasing the TiO_2 surface area (i.e. the highest current is found for sample A and the lowest for sample C). The values of the transistor ON/OFF ratios (deduced from the transfer characteristics in the linear regime) are about 10^4 for films A, about 10^5 for B, and 10^3 for C (Figure S5). The higher off current found for patterns A (Figure S5) can be tentatively explained as follows. The application of a V_d in electrolyte-gated transistors, even at V_g=0 V, induces a doping in the TiO_2 film in proximity of the electrodes, due to the presence of the electrolyte ions rearranging at the electrically biased electrode interfaces. Upon application of V_d, a certain amount of doping charge is accumulated at the TiO_2/electrolyte interface in patterns A, B and C. In patterns A, the smaller amount of TiO_2 leads to a higher density of doping charge, which in turn leads to a drop of the channel resistance and eventually to a higher off current. The threshold voltage (V_t), as extracted from the linear transfer characteristics (Figure 4.3), is about 0.85 V for films A, 0.95 V for films B and 1.1 V for films C. The difference in threshold voltage is tentatively attributed to the combined effect of the nanostructured nature of TiO_2 and the higher current measured in patterned devices.

We evaluated the charge carrier mobility in the linear regime of the transistors, μ_{lin}, using the following relationship: $\mu_{lin} = \frac{L \times I_{d,lin}}{W \times n \times V_d}$ where L is the interelectrode distance, W the electrode width, $I_{d,lin}$ the drain-source current in the linear region of the transfer characteristics (Figure 3), n the charge carrier density, deduced from $n = \frac{Q}{e \times A} = \frac{\int I_g dV_g}{r_v \times e \times A}$, where Q is the doping charge, e the elementary charge, A the surface area of the semiconductor in contact with the electrolyte, I_g the gate-source current (displacement current, Figure 4.3) and r_v the sweeping rate of the gate potential.[132] The charge carrier density, calculated in the V_g range 0 V - 1.5 V, increases with the decrease of the surface area of the films, being 2.5×10^{12} cm^{-2} for films C, 1.1×10^{13} cm^{-2} for films B and 9.9×10^{13} cm^{-2} for films A. Based on these values, we deduced electron mobilities of 0.55±0.1 $cm^2/V\cdot s$ for films C, 1.2±0.1 $cm^2/V\cdot s$ for B and 0.25±0.05 $cm^2/V\cdot s$ for A, quite interesting values for solution-processed TiO_2 films. The reason of such a large mobility difference for the different patterns is still under investigation. Overall, our results indicate that: i) for a given pattern, the mobility does not significantly depend on charge density (Figure S6), in accordance with the behaviour of EGTs based on organic polymers[140] and ii) the highest

mobility is found for films of type B, thus suggesting that a high charge density, as in the case of films of type A, might have a detrimental effect on charge mobility. Work is in progress to further explore the relationships between pattern size, charge density and charge mobility in films of TiO_2 and other transition metal oxides.

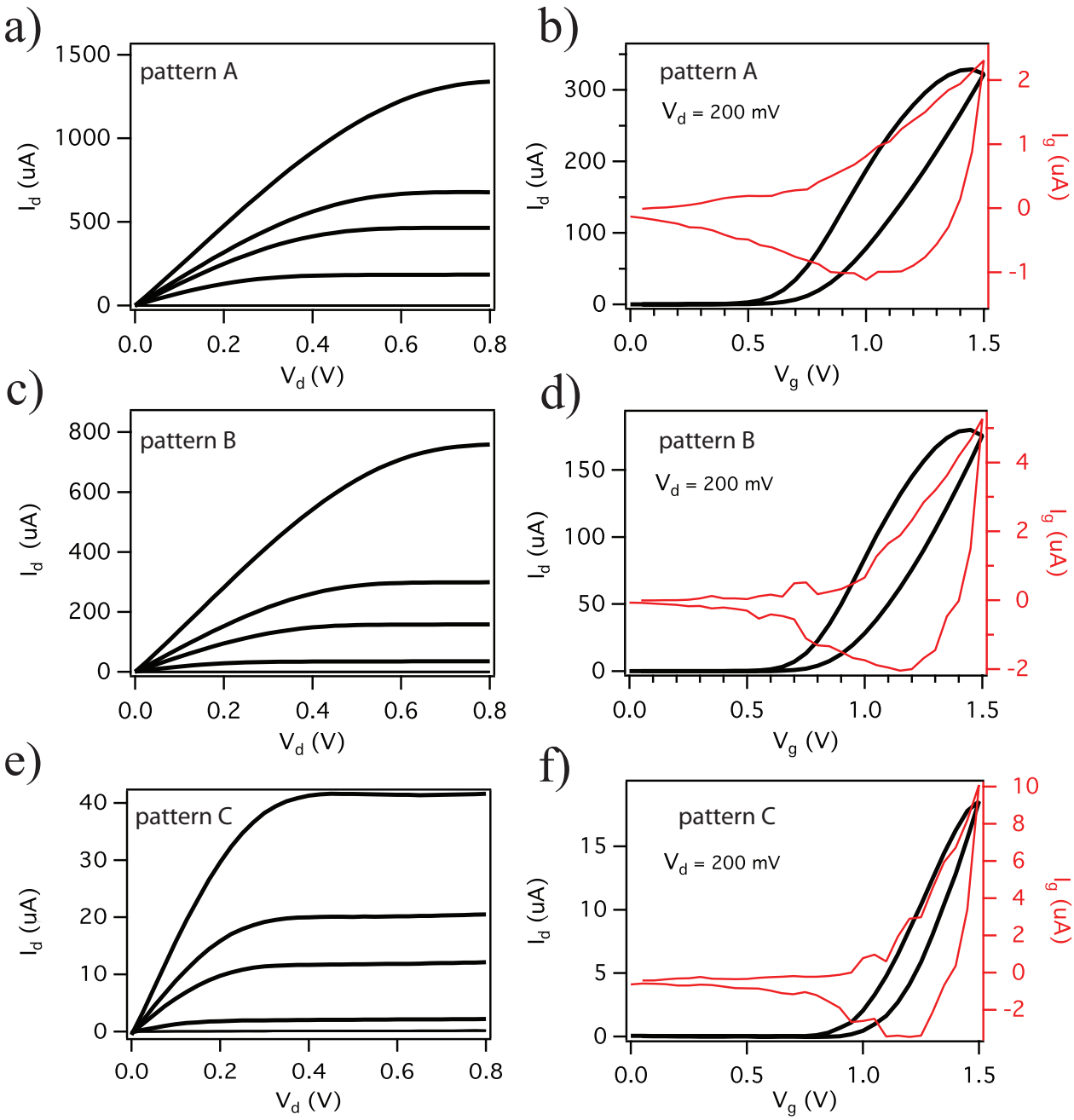

Figure 4-3: Output characteristics at V_g = 0 V, 1 V, 1.2 V, 1.3 V, 1.5 V and transfer characteristics at V_d = 200 mV of [EMIM][TFSI]-gated TiO_2 transistors: a) and b) are for films A; c) and d) for films B; e) and f) for unpatterned films C. The sweeping rate is 50 mV/s.

We also extracted the charge mobility adopting the field-effect approach, based on the knowledge of the pseudocapacitance at the electrolyte/semiconductor interface, as deduced from cyclic voltammetry. The values of the field-effect mobility in the linear and saturation regimes were calculated from the transfer characteristics using the following relationships: $\mu_{lin} = \frac{\partial I_d}{\partial V_g} \cdot \frac{L}{WC_i V_d}$ and $\mu_{sat} = \left(\frac{\partial \sqrt{I_d}}{\partial V_g}\right)^2 \frac{2L}{WC_i}$, where C_i is the pseudocapacitance. Interestingly, the values of the linear and saturation mobility for the same device are similar, likely because of the low contact resistance for the charge injection process in EG transistors.[39, 170] The saturation mobilities are 0.4±0.1 $cm^2/V{\cdot}s$ for films C, 1.4±0.1 $cm^2/V{\cdot}s$ for B and 0.5±0.1 $cm^2/V{\cdot}s$ for A whereas the linear mobilities are 0.6±0.1 $cm^2/V{\cdot}s$ for C, 1.7±0.1 $cm^2/V{\cdot}s$ for B, 0.6±0.1 $cm^2/V{\cdot}s$ for A. These values are similar to those extracted from the charge carrier density and follow the same trend.

4.5 Conclusion

In summary, we have used photolithographically patterned TiO_2 films as the channel material in n-type electrolyte-gated transistors, making use of high surface area activated carbon as the gate electrode and the ionic liquid [EMIM][TFSI] as the electrolyte. Patterning, achieved through the use of a parylene-based technique, improves the capability to control the gating (electrolyte/metal oxide) interface in this class of devices. The transistors operate at about 1.5 V, show mobility above 1 $cm^2/V{\cdot}s$ and ON/OFF ratios as high as 10^5. Patterned devices with large TiO_2/electrodes overlap show the best performance in terms of mobility and ON/OFF ratio, whereas patterned devices with small TiO_2/electrodes overlap show the highest transistor current and the highest charge carrier density, due to the larger specific capacitance. Electrochemical measurements point to a doping mechanism based on electrochemical processes confined at the interface between the electrolyte and the high surface area TiO_2 film. Overall, our results demonstrate that TiO_2 electrolyte-gated transistors are promising for applications in low-voltage electronics, e.g. in glucose sensing, where performance similar to those of graphene EGTs are observed.[103, 171, 172]

Patterned EGTs might also be useful for the study of fundamental physico-chemical processes in nanostructured metal oxides, such as the hypothesis of self-doping, in turn causing an insulator-

metal Mott transition, in nanostructured anatase films employed in photoelectrochemical cells.[149, 173] Ongoing work aims at developing large area deposition techniques for TiO_2, possibly not requiring high temperature thermal treatments, for printable and flexible applications.

4.6 Experimental

4.6.1 Processing of TiO_2

1 g of TiO_2 (a mixture of rutile and anatase in xylene, Sigma Aldrich, #700339) was mixed with 20 ml of dimethylformamide (DMF, Caledon Laboratory Chemicals, purity 98.5%) and 0.4 g of the binder polyvinylidene fluoride (PVDF, Sigma Aldrich). The TiO_2 suspension was stirred in a planetary mixer (THINKY ARM-310) for 30 minutes at 2000 rpm and filtered (0.2 μm filter mesh size) before use. All chemicals used for the synthesis of TiO_2 were used as received.

4.6.2 Purification of the ionic liquid

The ionic liquid 1-Butyl-3-methyl imidazolium bis(trifluoromethylsulfonyl)imide [EMIM][TFSI] was purchased from IoLiTec Inc. Prior to use, it was purified under vacuum ($\sim 10^{-5}$ Torr), at 80 °C, for about 24 hours, as described in the literature,[11] and transferred inside a N_2 glove box (O_2 and H_2O <10 ppm). The [EMIM][TFSI] ionic conductivity is 6.63 $mS \cdot cm^{-1}$ and the viscosity 39.4 mPa·s, at 20°C.[174]

4.6.3 Device Fabrication

Au (40 nm) source and drain electrodes (W/L= 4000/10 μm/μm) with a Ti (5 nm) adhesion layer were patterned on SiO_2/Si substrates by conventional photolithography and lift-off. The patterning of the TiO_2 was performed by unconventional photolithography (see Results and discussion). Device fabrication was completed in a N_2-purged glove box by sequentially placing, on top of the TiO_2 channel, a Durapore® membrane filter (GVHP01300 with a 0.22 μm pore size, area 0.36 cm^2) soaked in the ionic liquid [EMIM][TFSI] and an activated carbon gate electrode (Figure S1 and Experimental). More in detail, EMIM-TFSI was drop casted on the

filter, the wet filter was placed on top of the channel and the carbon gate was placed on the wet filter. We observed good adhesion between the gate and the wet filter.

4.6.4 Fabrication of the activated carbon (AC) electrodes

The AC gate electrode was prepared using carbon paper (Spectracorp 2050) coated with a suspension containing activated carbon (PICACTIF SUPERCAP BP10, Pica, 28 mg ml^{-1}) and polyvinylidene fluoride (PVDF, KYNAR HSV900, 1.4 mg ml^{-1}) in N-methyl pyrrolidone (NMP, Fluka, >99.0%). The coating was followed by thermal treatment at 60 °C for 5 hours in ambient atmosphere to remove solvent and water traces.

4.6.5 Morphology and structure of TiO_2 films

Scanning Electron Microscopy **(**SEM) was performed with a FEI Quanta 450 Environmental Scanning Electron Microscope (FE-ESEM). Atomic Force Microscopy (AFM) was performed in tapping mode with a Digital Instruments Dimension 3100 (Santa Barbara, CA) and a Veeco Nanoscope V controller (Bruker). Tapping mode was performed with a scan rate of 1 Hz using etched silicon cantilevers (ACTA from Applied Nanostructures, Inc.) with a resonance frequency around 300 KHz, a spring constant of 40 N/m and a tip radius <10 nm. All images were acquired with medium tip oscillation damping (20%–30%). The structure of the TiO_2 films was investigated by X-ray diffraction with a Bruker D8 diffractometer using a (Cu Kα) beam. X-ray scans were measured every $2\theta = 0.01$ and the time per step was 0.6 sec.

4.6.6 Surface area measurements

Brunauer-Emmett-Teller (BET) single point specific surface area measurements were performed with an Autochem II 2920 Micrometrics, equipped with a TCD detector. We deduced from the Brunauer-Emmett-Teller (BET) analysis a value of about 57.1 m^2/g for our TiO_2 films. From the weight of the TiO_2 films (0.3 mg for C and, considering the geometric areas and the thickness of the films, 0.051 mg for B and 0.0039 mg for A) we obtained surface areas of 170 cm^2 for C, 29 cm^2 for B and 2.2 cm^2 for A.

4.6.7 Transistor and electrochemical characterization

Transistor characterization was performed in a N_2 glove box (O_2 and H_2O <10 ppm) using a micromanipulated electrical probe station and a semiconductor parameter analyzer (Agilent B1500A). For all devices, the transistor current increased by increasing the time spent in the N_2 glove box after lamination of the electrolyte membrane and the gate electrode.[113, 175] Therefore, the device characteristics were evaluated after stable current values were achieved for patterned devices, i.e. after about one week. Electrochemical characterization was performed using a PARSTAT 2273 (Princeton Applied Research) multichannel potentiostat equipped with impedance modules.

4.7 Acknowledgments

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CHAPTER 5 CHARGE CARRIER DENSITY MODULATION IN DENSELY PACKED AND POROUS POLYCRYSTALLINE TiO_2 FILMS BY ELECTROLYTE GATING

5.1 Abstract

Electrolyte gating permits to modulate the charge carrier density in semiconducting films by several orders of magnitude, upon application of relatively low electrical bias (sub-2 V). We investigated the effect of the size of electrolyte ions on charge carrier density modulation in transistors based on thin films of porous and highly dense polycrystalline TiO_2. The ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide [EMIM][TFSI] and [EMIM][TFSI] mixed with lithium perchlorate were used as the electrolytes, to investigate the effect of relatively large [EMIM] and small Li^+ cations on the device characteristics. The correlation between the electrochemical and electrical characteristics was shown.

5.2 Introduction

The low operating voltage of electrolyte-gated transistors (EGTs), specifically sub-2 V, opens opportunities for applications in printable and flexible electronics. One more advantage of electrolyte gating is a low contact resistance, since polarization of ions in the electrolyte assists the charge carrier injection.[170, 176] EGTs may use a large number of electrolytes including aqueous saline solutions, polymer electrolytes, ionic liquids and ion gels.[51, 54, 163, 177]

Metal oxides are used in a wide range of applications, such as transistors for active matrix displays, transparent conductive electrodes and batteries.[27] Some metal oxides are non-toxic and biocompatible, they also possess good electron-transfer kinetics and adsorption capability for bio sensing applications.[178] Among metal oxides, TiO_2 is a low-cost, abundant material, widely used as a white pigment for medicine, cosmetics, paper and food processing. Moreover it was utilized as a photocatalyst, as an electrochromic material and as a material for Li storage in Li-ion batteries.[149, 150, 179-181]

TiO_2 have been employed as an insulator and as a n-type channel material in field-effect and EGTs.[106, 107, 154-157, 182] Different methods have been used to prepare TiO_2 films, such as magnetron sputtering, electron beam evaporation, pulsed laser deposition or solution processing (e.g. sol-gel).[183-185] Different film deposition techniques lead to different crystal structure, morphology and chemical composition, which significantly affect the electrical properties of the transistors. Polycrystalline anatase TiO_2 films have been used to investigate the effect of concentration of mobile ions on the working mechanism of EGTs.[106] High values of the electron density ($\geq 10^{14}/cm^2$) were achieved in EG transistors based on slightly doped, epitaxially grown, TiO_2 films; a transition from low to high conductivity was demonstrated.[107] Moreover, electrolyte gating induce the transition from paramagnetism to ferromagnetism in co-doped TiO_2 by accumulation of high charge carrier density.[108]

Polarization of an electrolyte upon applied potential induce accumulation or depletion of charges at the semiconductor electrolyte interface. The doping mechanisms can be electrostatic and/or electrochemical.[163] Electrostatic doping is similar to the doping in the field effect transistors where the double layer formed on the electrolyte semiconductor interface. Electrochemical doping is achieved by redox reactions on the surface of the semiconductor or by intercalation of ions within the bulk of the materials resulting in reversible faradaic charge transfer. For TiO_2 gated by [EMIM][TSFI], the relatively large size of the [EMIM] cation of the ionic liquid (theoretically deduced radius of 3.5 Å) leads to surface limited redox reactions, while small cations such as H^+ and Li^+ can be intercalated through the rows formed at the edge-shared octahedra of the tetragonal form of anatase TiO_2.[164, 166]

Investigation of doping mechanisms, influence of ion size and film morphology on charge carrier density is highly important to improve the device performance. In this work, we report on EGTs based on porous solution-processed films and on dense E-beam evaporated films of TiO_2. We compared the electrical characteristics of the transistors obtained upon doping with large $EMIM^+$ cations and small Li^+ cations. The doping mechanisms were investigated by Cyclic Voltammetry (CV) and Electrical Impedance Spectroscopy (EIS).

5.3 Experiments and methods

5.3.1 Processing of TiO_2

Densely packed TiO_2 films were evaporated on Si/SiO_2 in the Thermionics Ebeam evaporator at a pressure of $3 \cdot 10^{-5}$ Torr during the deposition and a growth rate – 0.7 Å/s. The thickness of the evaporated TiO_2 films was estimated by DEKTAK 150 surface profiler and was about 60 nm. Solution processed TiO_2 films were obtained with a method reported in one of our recent publications.[55]

5.3.2 Electrolyte preparation

As the electrolytes, we used the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide [EMIM][TFSI] and a mixture of [EMIM][TFSI] with Lithium perchlorate trihydrate with molar concentration 0.3M per 1 litre of [EMIM][TFSI]. [EMIM][TFSI] was purchased from IoLiTec Inc. [EMIM][TFSI] shows a viscosity of 39.4 mPa·s and an ionic conductivity 6.63 $mS \cdot cm^{-1}$ at 20 °C (data provided by IoLiTec Inc). Lithium perchlorate trihydrate was purchased from Sigma Aldrich. Prior to use, both electrolytes were purified under vacuum ($\sim 10^{-5}$ Torr) at 80 °C, for about 24 hours to remove water and transferred inside a N_2 glove box for device assembling and measurements.

5.3.3 Fabrication of the activated carbon (AC) electrodes

The AC gate electrode was prepared using carbon paper (Spectracorp 2050) coated with a suspension containing activated carbon (PICACTIF SUPERCAP BP10, Pica, 28 mg ml^{-1}) and polyvinylidene fluoride (PVDF, KYNAR HSV900, 1.4 mg ml^{-1}) in N-methyl pyrrolidone (NMP, Fluka, >99.0%). The coating was followed by thermal treatment at 60°C for 5 hours to remove solvent and water traces in ambient atmosphere. The choice of activated carbon for the gate electrode stems from its capability to limit undesirable electrochemical reactions (detrimental for device stability) and its high surface area, highly desirable to achieve high current modulation.[48, 137]

5.3.4 Device Fabrication

Au (40 nm) source and drain electrodes (W/L= 4000/10) with a Ti (5 nm) adhesion layer were patterned on SiO_2 substrates by conventional photolithography and lift-off. Device fabrication was completed in a N_2-purged glove box by placing the electrolyte, consisting of a Durapore® membrane filter soaked in electrolyte, and the activated carbon gate electrode.

5.3.5 Morphology and structure of TiO_2 films

Scanning Electron Microscopy **(**SEM) was performed with a FEI Quanta 450 Environmental Scanning Electron Microscope (FE-ESEM). The structure of the TiO_2 films was investigated by X-ray diffraction with a Bruker D8 diffractometer using a (Cu Kα) beam. X-ray scans were measured every $2\theta = 0.01$, time per step was 0.6 sec. Brunauer-Emmett-Teller (BET) single point specific surface area measurements were performed with an Autochem II 2920 Micrometrics, equipped with a TCD detector.

5.3.6 Transistor and electrochemical characterization

Transistor characterization was performed in a N_2–purged glove box (O_2 and H_2O <10 ppm) using a micromanipulated electrical probe station and a semiconductor parameter analyzer (Agilent B1500A). Electrochemical characterization was performed using a PARSTAT 2273 (Princeton Applied Research) multichannel potentiostat equipped with impedance modules.

5.4 Results and Discussion

Scanning Electron Microscopy images of both evaporated and solution processed TiO_2 films, annealed at 450 °C in ambient atmosphere, are shown in Figure 5-1a and 5-1b. Evaporated films (Figure 5-1 a) are very dense and have a smooth surface with the thickness of ~80 nm. While the solution processed films are porous with thickness of ~3 um. The X-ray diffraction (XRD) patterns of the films reveal the presence of anatase phase for evaporated films and mixture of anatase and rutile for solution processed films (Figure 5-1c). Solution processed films structure and morphology were introduced in our previous studies.[55]

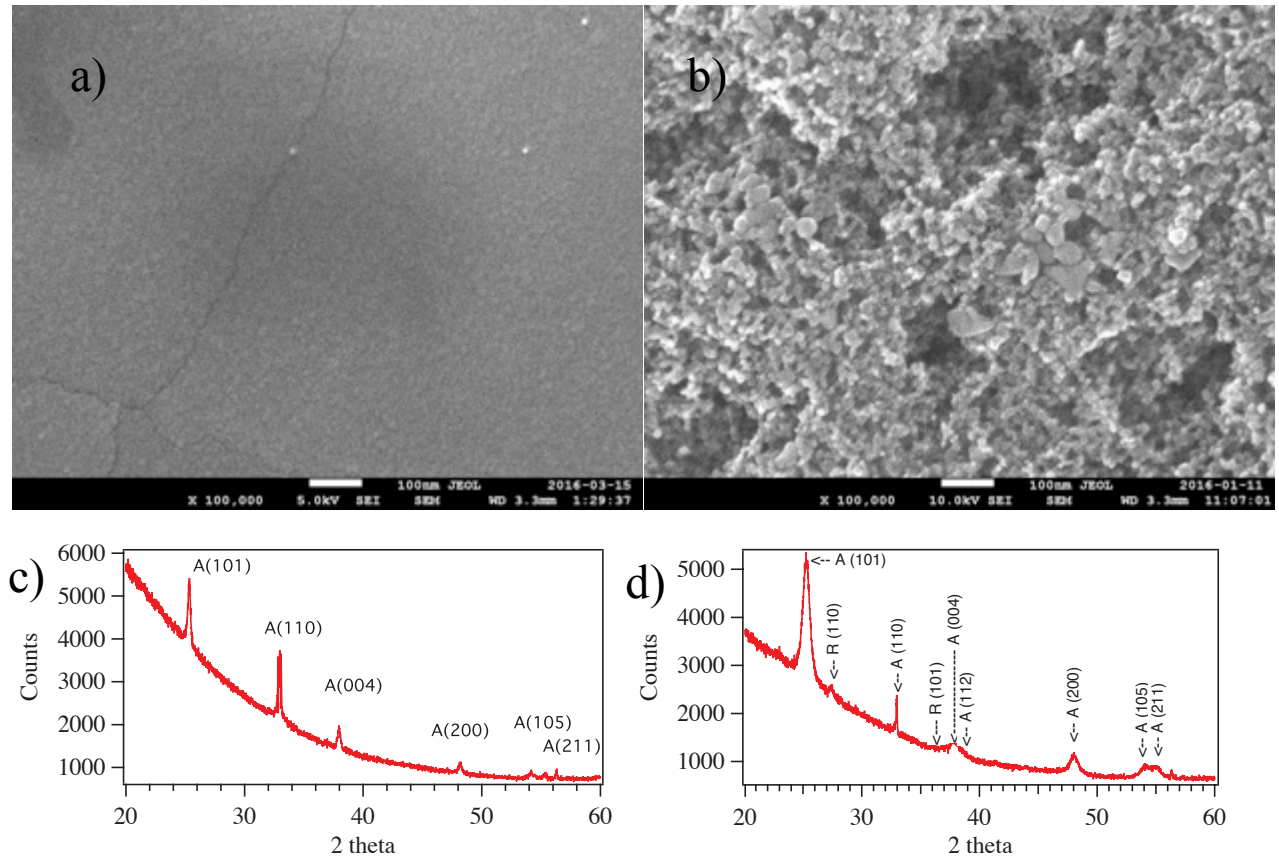

Figure 5-1: Scanning electron microscopy and X ray diffraction images of (a,c) Ebeam evaporated and (b,c) solution processed TiO_2 films on Si/SiO_2 annealed at 450 C.

Transistors making use of evaporated and solution processed films of TiO_2 gated with [EMIM][TFSI] will be henceforth named A and B, respectively. Transistors making use of evaporated and solution processed films of TiO_2 gated with ([EMIM][TFSI] + lithium perchlorate) will be henceforth named C and D, respectively.

All transistors show n-type semiconductor behaviour and work below 1.5 V. The output and transfer characteristics of EG transistors of types A and B are shown on Figure 5-2. Evaporated TiO_2 TFTs with [EMIM][TFSI] as gating medium (type A) possess higher ON current and better ON/OFF ratio around 10^4, while solution processed [EMIM][TFSI] gated TFTs (type B) showed ON/OFF ratio around 10^2. The threshold voltage (V_t), as extracted from the $I_d^{1/2}$ vs V_g (saturation transfer characteristics at V_d =1V (Figure 5-2), is about 1.2 V for films A, and 1 V for films B.

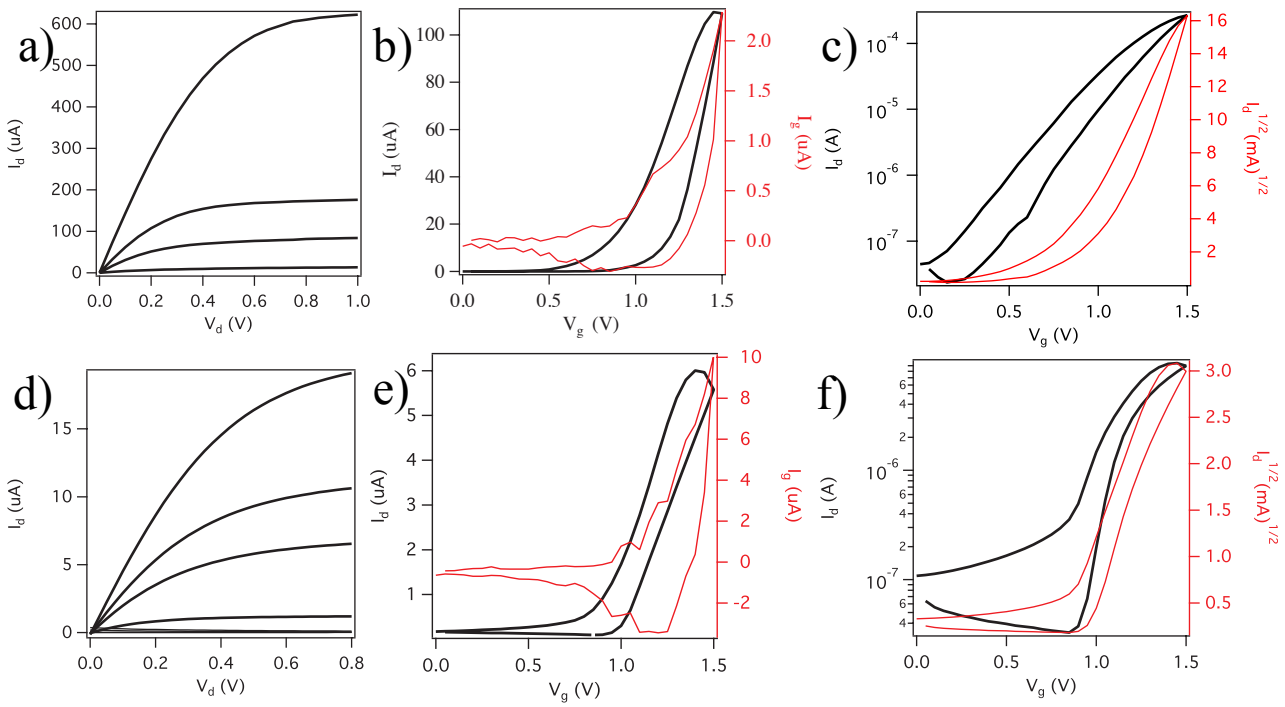

Figure 5-2: (a,d) Output characteristics at V_g = 0 V, 1 V, 1.2 V, 1.3 V, 1.5 V and (b,e) transfer characteristics at V_d = 200 mV; (c,f) transfer characteristics at V_d = 1V of [EMIM][TFSI]-gated TiO_2 transistors: a), b), c) are for evaporated TiO_2 devices (type A); d), f) and e) for solution processed TiO_2 devices (type B). The scan rate is 50 mV/s.

We evaluated the charge carrier density in the linear regime of the transistors, from the displacement current using the formula: $n = \frac{Q}{eA} = \frac{\int I_g dV_g}{r_v eA}$, where Q is the doping charge, e the elementary charge, A the geometric surface area of the semiconductor in contact with the electrolyte, I_g the gate-source current in the linear region of the transfer characteristics and r_v is the scan rate of the gate potential.[141]

The charge carrier density, calculated in the V_g range 0 V - 1.5 V, decreases with the increase of the surface area of the films, being 1.9×10^{14} cm^{-2} for type A and 6.4×10^{12} cm^{-2} for type B. It can be explained that the surface of porous films of TiO_2 is much higher and during the cathodic scan, a higher amount of positive ions can be displaced towards the TiO_2 surface, to counterbalance the injected electrons. Moreover, the hydroxyl group in the solution-processed films and interfacial defects can trap the electrons, thus decreasing the charge carrier density. The current density was calculated by normalizing the current to the values of the geometric surface

area (the area of filter soaked in the electrolyte) of 0.4 cm^2 for highly dense films of type A devices and surface area deduced from Brunauer-Emmett-Teller (BET) analysis (about 57.1 m^2/g) was 170 cm^2 for porous films of type B devices.[55]

We carried out a cyclic voltammetry survey on devices type A, the CV for devices type B was shown for comparison to map their redox activity (see Figure 5-3). We used a two-electrode configuration, where the TiO_2 film, included between the source and drain electrodes, acted as the working electrode whereas the carbon gate (specific capacitance of about 100 $F \cdot g^{-1}$) acted simultaneously as the counter and quasi reference electrode.[48, 49, 137]

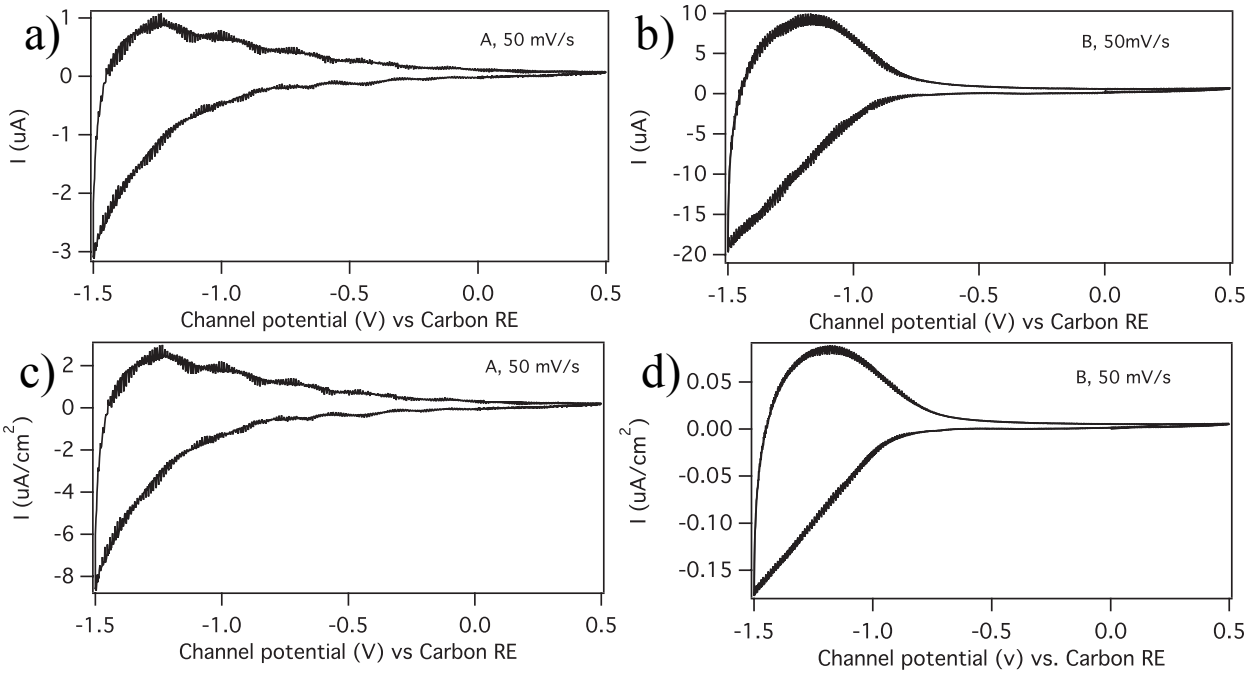

Figure 5-3: Cyclic voltammetry of evaporated TiO_2 films of devices type A (a,c) and solution processed TiO_2 devices (type B) (b,d). A TiO_2 film included between source and drain electrodes, acts as the working electrode and the carbon gate acts as the counter and the quasi reference electrode. For (c,d) the current is normalized to the surface area of the TiO_2 films in contact with the electrolyte. The measurements were carried out at scan rate 50 mV/s using [EMIM][TFSI] as the electrolyte.

Cathodic and anodic redox processes are observable upon scans of the electrode potential in the interval between -0.3 V and -1.5 V vs. carbon quasi reference electrode for device A and between

-0.5 V and -1.5 V vs. carbon quasi reference electrode for device B. While the voltammetric current was higher for solution processed TiO_2 films (type B), the current density was higher for evaporated films (type A).

The sharp increase of the cathodic current starts at -0.8 V for A and at -0.7 V for B. During the anodic scan, a relatively wide anodic peak is observable for both devices, located at -1.25 V. The current density in the cyclic voltammetry plots was calculated by normalizing the current to the values of the surface areas of the TiO_2 films. The values of the current density decrease with the increase of the TiO_2 surface area (samples A has the highest current density and the lowest surface area).

From the cyclic voltammetry measurements, we deduced the pseudocapacitance at the TiO_2 film/electrolyte interface, by calculating the slope of the (linear) plot of the doping charge (deduced by the integration of the voltammetric current over time) vs. potential. The capacitance is 0.33 mF for A and 0.17 mF for B; the specific pseudocapacitance was 0.82 mF/cm^2 for A and 0.001 mF/cm^2 for B. These results show that evaporated films of devices type A are able to store more charge per unit surface area, compared to solution processed samples B, that is in agreement with deduced charge carrier density from displacement current.

We performed Electrochemical impedance spectroscopy (EIS) in the 0.01 Hz-10 kHz frequency range, at 1 V vs carbon quasi reference electrode, with a perturbation of 10 mV, using two electrode configuration. The Nyquist plot is shown on figure 5-4; the straight lines almost parallel to the imaginary axis indicate a capacitive behaviour of both TiO_2 films. However, the phase angle estimated at low frequency is -68° for samples A, and -55° for samples B. This indicates that ion diffusion has a more significant effect on the doping process for porous films with larger surface area.

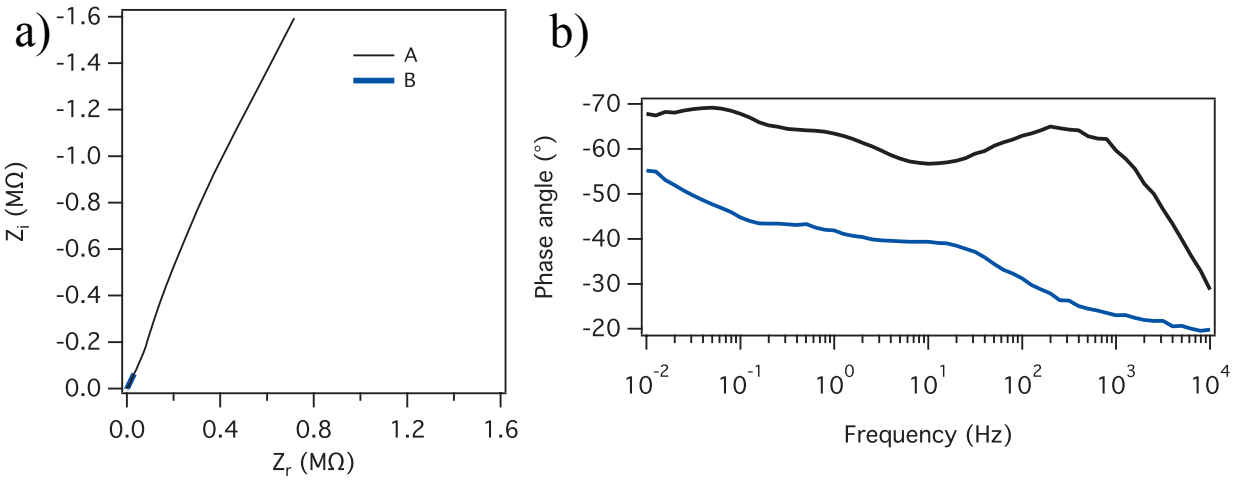

Figure 5-4: Nyquist plots obtained in transistor configuration using dense (A) and porous (B) films of TiO_2 included between source and drain as the working electrode and carbon as the counter and quasi reference electrode. (b) Phase angle vs frequency of the same devices. In samples A the film has a geometric surface area of 0.4 cm^2, in samples B the BET surface area is of 170 cm^2. The measurements were carried out at 1 V vs carbon quasi reference electrode, using [EMIM][TFSI] as the electrolyte.

We investigated the influence of small Lithium cation in electrolyte on electrical properties of TiO_2 transistors. Lithium salt was mixed in room temperature ionic liquid [EMIM][TFSI] with concentration of 0.3 M.[186] The output and transfer characteristics of dense evaporated TiO_2 TFTs with [EMIM][TFSI] + Lithium perchlorate as gating medium (type C) are shown on Figure 5-5. To allow more Li^+ cations to intercalate into TiO_2 films and to dope it, [187] we changed the sweeping rate by increasing the duration of the sweep such as 50mV/s; 50 mV/30s and 50 mV/60s. It is known that interstitial Li is a donor with a reaction: $TiO_2+x(Li^++e^-) \leftrightarrow Li_xTiO_2$. [188] As seen from output curves at scan rate 50 mV/s there is a non omhic charge carrier injection, figure 5-5a. By changing the sweeping rate from 50 mV/s to 50 mV/30s and to 50 mV/60s the on/off ratio was improved with shift of V_{th} from 0.6 V to 1V and to 1.1V, respectively. The threshold voltage was deduced from the transfer curves in linear regime. The charge carrier density n for device C was around 9.6×10^{14} cm^{-2} at 50 mV/s, 1.9×10^{14} cm^{-2} at 50 mV/30s and 8.4×10^{13} cm^{-2} at 50 mV/60s, as deduced from the displacement current. The charge carrier density, calculated in the V_g range 0 V - 1.5 V, decreases with the increase of the sweep

time. Increasing the sweep duration, more Li^+ cations intercalated through the TiO_2 crystal lattice probably inducing the interface states, which traps electrons thus increasing the threshold voltage and decreasing the charge carrier density. The charge carrier mobility in the linear regime (μ_{lin}) was extracted using the relationship: $\mu_{lin} = \frac{L\, I_{d,lin}}{W\, e\, n\, V_d}$, where L is the interelectrode distance, W the electrode width, $I_{d,lin}$ the drain-source current in the linear regime of the transfer characteristics and n the charge carrier density. The charge carrier mobilities for the device C at 50 mV/s was 0.004 $cm^2V^{-1}s^{-1}$; at 50 mV/30s n was 0.06 $cm^2V^{-1}s^{-1}$; at 50 mV/60s n was 0.12 $cm^2V^{-1}s^{-1}$.

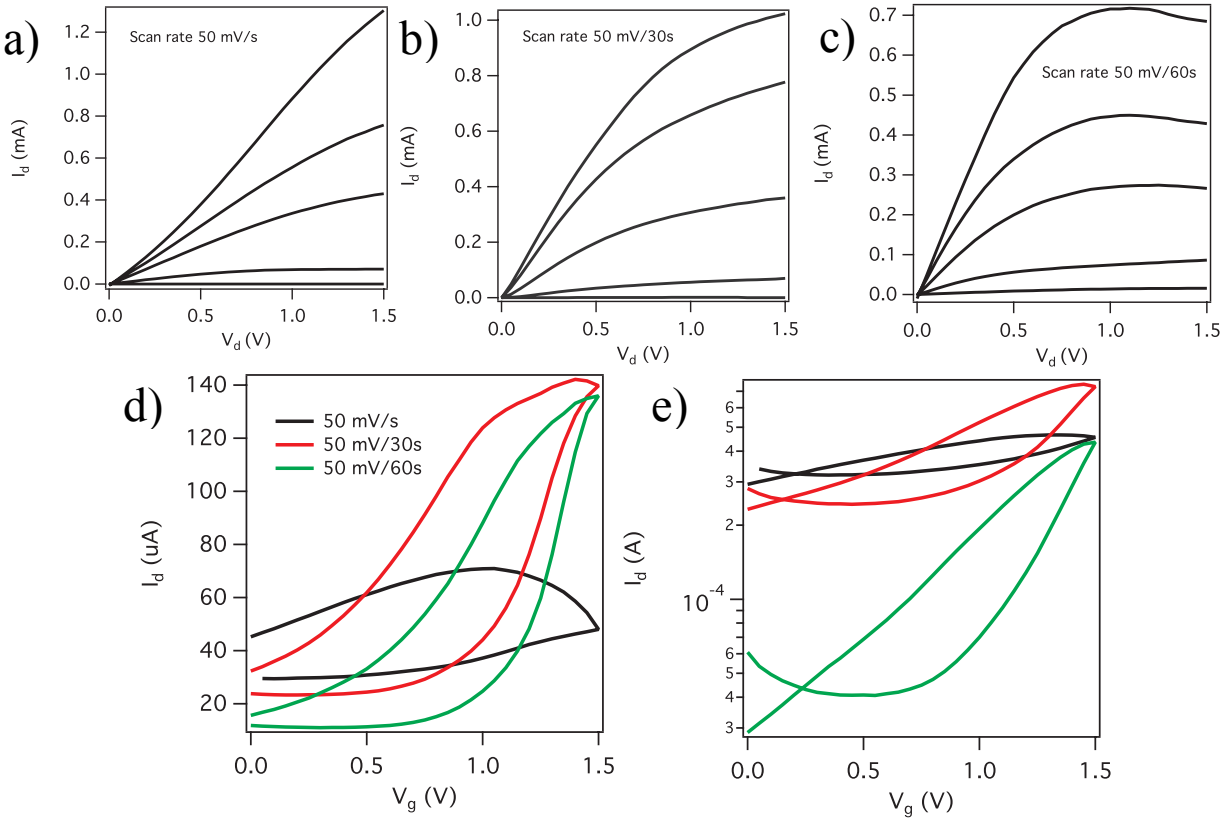

Figure 5-5: Output characteristics at V_g = 0 V, 1 V, 1.2 V, 1.3 V, 1.5 V at sweeping rate (a) 50 mV/s; (b) 50 mV/30s and (c) 50 mV/60s. (d) Transfer characteristics at V_d = 200 mV; (e) transfer characteristics at V_d = 1V of evaporated TiO_2 TFTs with [EMIM][TFSI] Lithium perchlorate as gating medium (device C).

The output and transfer characteristics of porous solution processed TiO_2 TFTs using a mixture of [EMIM][TFSI] and Lithium perchlorate as gating medium (type D) are shown on Figure 5-6.

As in device C, changing the sweeping rate from 50 mV/s to 50 mV/30s and to 50 mV/60s the on/off ratio improved for device D from 10^2 to 10^3 and then to 10^4, respectively. The threshold voltage V_{th} shifted to more positive values: 0.9 V at 50 mV/s to 1V at 50 mV/30s and to 1.2V at 50 mV/60s was also observed. The charge carrier density n, deduced from the displacement current, was ≈3.4 ×10^{12} cm^{-2} at 50 mV/s, ≈5.8 ×10^{11} cm^{-2} at 50 mV/30s and ≈ 1.4 ×10^{11} cm^{-2} at 50 mV/60s. Like in transistors based on evaporated TiO_2, the charge carrier density decreases by increasing the duration of the sweep. The electron mobility, in the linear regime, for the device D was 0.27 $cm^2V^{-1}s^{-1}$ at 50 mV/s, 2.7 $cm^2V^{-1}s^{-1}$ at 50 mV/30s and 33 $cm^2V^{-1}s^{-1}$ at 50 mV/60s. For both devices C and D we found a decrease of charge carrier density and increase of mobility upon intercalation of Li^+. Intuitively, we can explain the observed increase of the electron mobility and decrease of charge carrier density by the filling of the traps on the electrolyte/semiconductor interface.

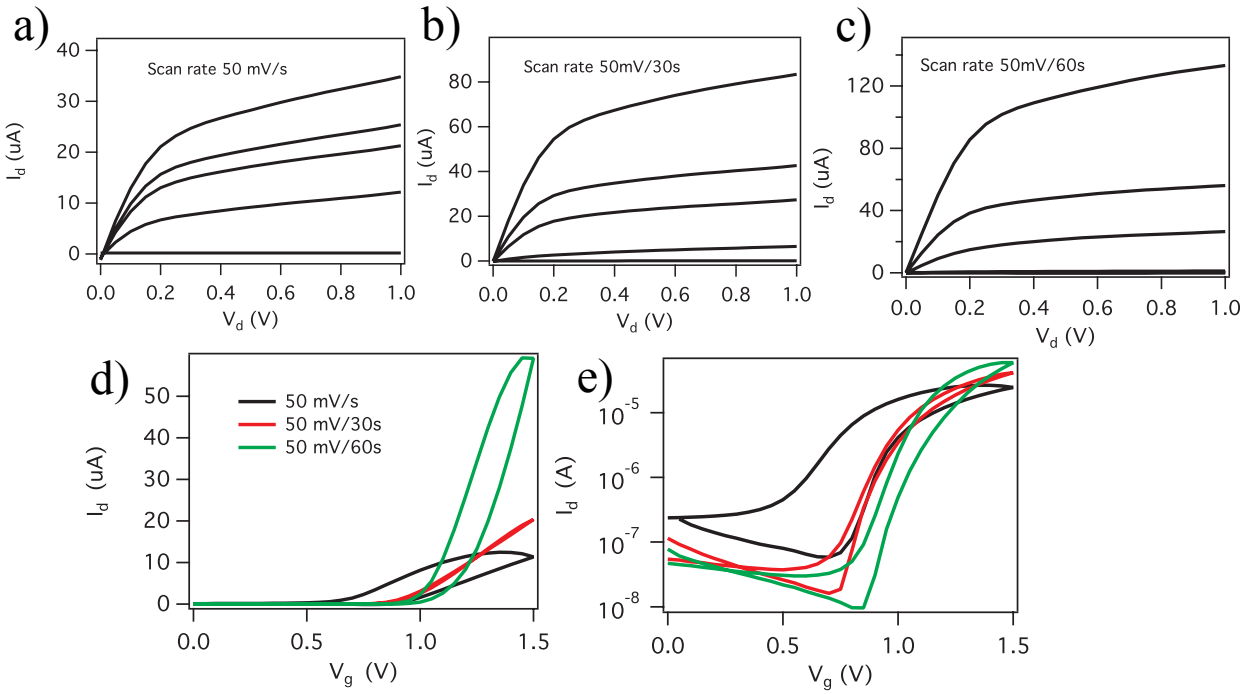

Figure 5-6: Output characteristics at V_g = 0 V, 1 V, 1.2 V, 1.3 V, 1.5 V at sweeping rate (a) 50 mV/s; (b) 50 mV/30s and (c) 50 mV/60s. (d) Transfer characteristics at V_d = 200 mV; (e) transfer characteristics at V_d = 1V of porous solution processed TiO_2 TFTs with [EMIM][TFSI] Lithium perchlorate as gating medium (device D).

We performed a cyclic voltammetry survey for evaporated devices type C and solution processed devices type D using [EMIM][TFSI] / Lithium perchlorate mixture (Figure 5-7).

The voltammetric current and the current density (see Figure 5-3) were higher for evaporated TiO_2 (device type C), than for solution processed TiO_2 (device type D). For device C, cathodic and anodic redox processes are observable upon scans of the electrode potential in the interval between 0 V and -1.5 V vs. carbon quasi reference electrode and for device D between 1.5 V and -1.5 V vs. carbon quasi reference electrode. For device C, the sharp increase of cathodic current starts at -1 V. During the anodic scan, a relatively wide anodic peak is observable for both devices, located at -0.8 V. For device D there are two peaks of cathodic current, one at -0.15 and second one at -1.25 V. During the anodic scan, a relatively wide anodic peak is observable for both devices, located at -0.7 V and at 1.5 V. The current density in the cyclic voltammetry plots was calculated by normalizing the current to the values of the surface areas of the TiO_2 films.

From the cyclic voltammetry measurements, we deduced the pseudocapacitance at the TiO_2 film/electrolyte interface, by calculating the slope of the (linear) plot of the doping charge (deduced by the integration of the voltammetric current over time) vs. potential. The capacitance is 0.11 mF for C and 0.0022 mF for D; the specific pseudocapacitance normalised by the area is 0.27 mF/cm^2 for C and 0.00027 mF/cm^2 for D. These results show that dense film of device type C are able to store more charge per unit surface area, compared to porous samples D, that is in agreement with deduced charge carrier density from displacement current.

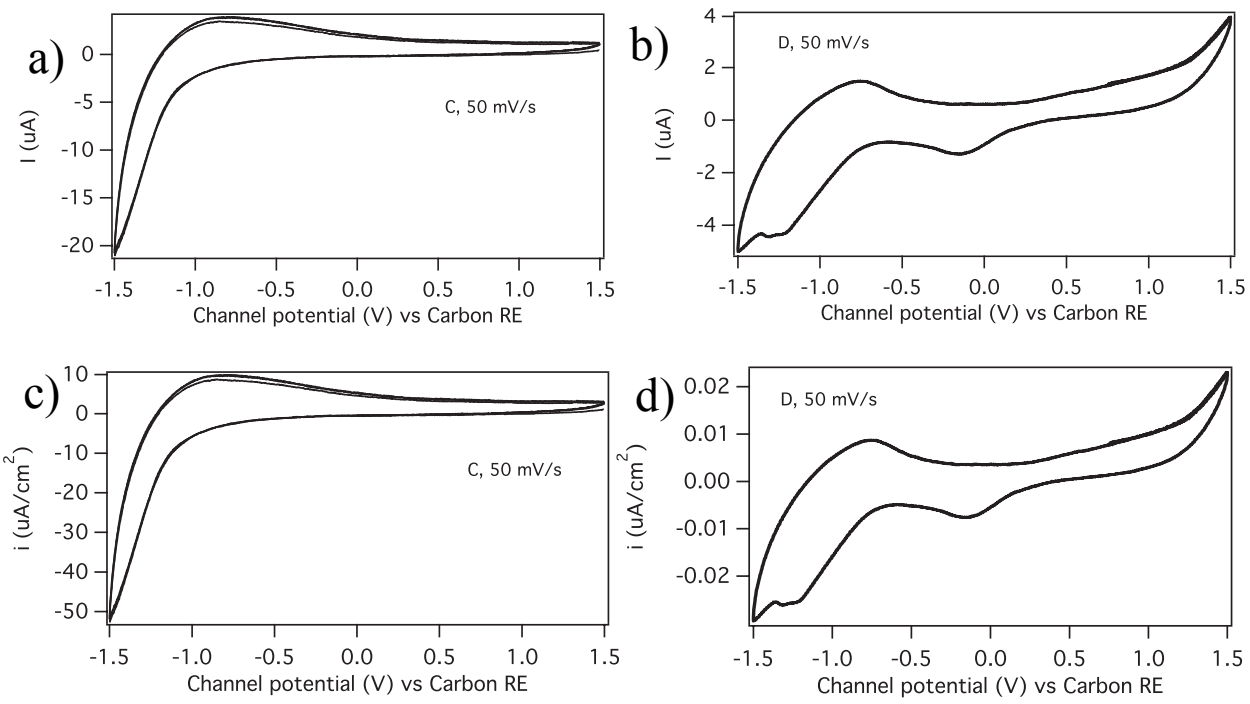

Figure 5-7: Cyclic voltammetry of TiO_2 films for devices type C (a,c) and D (b,d). A TiO_2 film included between source and drain electrodes acts as the working electrode and the carbon gate acts as the counter and the quasi reference electrode. For (c,d) the current is normalized to the surface area of the TiO_2 films in contact with the electrolyte. The measurements were carried out at scan rate 50 mV/s using [EMIM][TFSI]+Lithium perchlorate as the electrolyte.

5.5 Conclusion

EG n-type transistors based on porous and dense polycrystalline TiO_2 films making use of high surface area activated carbon as the gate electrode and the ionic liquid [EMIM][TFSI] and [EMIM][TFSI] with lithium perchlorate as the electrolytes were demonstrated. Our transistors operate at sub 1.5 V conditions. EGTs based on evaporated TiO_2 with [EMIM][TFSI] as a gating medium show higher current and better on/off ratios as high as 10^4. The electrical properties of EGTs based on porous solution processed films of TiO_2 can be improved by using a [EMIM][TFSI] /lithium perchlorate mixture as an electrolyte. The on/off ratio increases (from 10^2 to 10^3 and then till 10^4) and the electron mobility increases from 0.27 $cm^2V^{-1}s^{-1}$, to 2.7 $cm^2V^{-1}s^{-1}$ and to 33 $cm^2V^{-1}s^{-1}$) with increase of sweep duration from 50mV/1s to 50mV/30s and to

50mV/60s, respectively.

Besides shedding light on the doping mechanisms in EGTs with different morphology of TiO_2, our work paves the way to a more widespread use in electronics of a low cost, abundant and biocompatible material such as TiO_2. Moreover, since TiO_2 is an electrochromic material after intercalation of Li^+ [185] this results can be useful for the development of the electrochromic switch for smart windows.[189]

CHAPTER 6 GENERAL DISCUSSION

Electrolyte gating is a good approach to achieve transistor operation at low voltages and to add sensing species directly to the electrolyte for biological sensing applications. Although the interest in electrolyte-gated devices raised over the past decades, there is a lack of clear understanding of the device working mechanisms, including charge carrier density modulation, electrochemical doping and electrical double layer formation.

Investigation of charge carrier density modulation in materials with different electrical properties allows to explore the doping and charge transport mechanisms in transistors. In this thesis, I focused on the binary metal oxides TiO_2 and SnO_2 as transistors channel materials. These two oxides, based on metals with different electron configurations, possess different intrinsic electrical conductivity, which makes them interesting for investigation of electrical and electrochemical properties under electrolyte gating.

The device geometry and the size of the electrolyte ions play a primary role on doping mechanisms and charge carrier density modulation. Patterning of the semiconductor channel material on limited areas above the source-drain electrodes, instead of deposition it all over the substrate, leads to a decrease of parasitic currents and to an increase of the charge carrier density in the channel, by accumulating a high amount of charges in more confined area. Patterning of metal oxide electrolyte gated transistors is useful for the study of fundamental physico-chemical processes in nanostructured metal oxides, such as electrostatic and/or electrochemical doping leading to an insulator-metal transition.

Moreover, high charge carrier density can be achieved by forming a more densely packed electrical double layer at the electrolyte/semiconductor interface using gating media with small ions, such as Li^+ or H^+, rather than bulky ions typical of ionic liquids. Furthermore, small ions can intercalate through the semiconductor and dope it. Thus, electrical characteristics of metal oxide EGTs can be affected by patterning the transistor channel, varying the channel thickness and choosing the appropriate electrolyte.

EGTs of binary oxides are valuable tools to understand the device working mechanism and the effect of processing parameters on device performance. This will pave the way to a wider use of complex oxides based on these metals. For example, binary ZnO and their ternary, quaternary

oxides are quite well investigated materials in EGTs. InGaZnO is widely investigated and is nowadays used for production of displays backplanes. However, there is still lack of knowledge for binary, ternary or quaternary oxides based on Sn, which could be used instead of the rarer In and Ga. Even though the use of a liquid electrolyte is not appropriate for display technology, a solid electrolyte can be an alternative choice, keeping the advantages of electrolyte gating.

While the best device performance is in principle achieved with vacuum-deposited materials, solution processing is attractive for flexible and large area electronic applications. Thus, one of the goals of this has been was to improve the electrical properties of solution processed metal oxide transistors and to show their potential application for flexible electronics. Moreover, transistors based on the more intrinsically conductive semiconductors, like SnO_2, mostly work in depletion mode of operation. By using solution processing we were able to were able to fabricate SnO_2 transistors working in the enhancement mode, which is very important for applications in display technologies.

CHAPTER 7 CONCLUSION AND RECOMMENDATIONS

We fabricated solution processed SnO_2 and TiO_2 electrolyte-gated transistors operated at voltages lower than 1.5 V, making use of high surface area activated carbon as the gate electrode and the ionic liquid [EMIM][TFSI] as the gating medium. Using a parylene-based patterning I studied the influence of the extension of the electrolyte/semiconductor and electrode/semiconductor interfaces on the doping and charge carrier transport processes. I showed that the doping mechanism is likely based on electrochemical processes confined at the interface between the electrolyte and the high surface area metal oxide film.

Solution processed thin film SnO_2 transistors were fabricated on both rigid and flexible substrates. Unpatterned transistors were operated in enhancement mode. An average electron mobility of about 45 cm^2/Vs and on/off 10^4- 10^5 were obtained. Patterning of the semiconductor channel material on limited areas above the source-drain electrodes increases the conductivity of the film, leading to transistor operating in depletion mode with high off current. The enhancement mode of operation was achieved in patterned transistors only by decreasing the thickness of the SnO_2 films using diluted precursor solutions. Flexible SnO_2 transistors on polyimide substrates with good performance, even under bending conditions at bending radius (R)=30 mm, with linear electron mobility as high as 30 cm^2/Vs and on/off 10^4; under bending at R=10 mm, linear electron mobility decreased to 15 cm^2/Vs.

Electrolyte gated TiO_2 transistors work in enhancement mode. Patterned devices with large TiO_2/electrodes overlap show the best performance in terms of mobility, i.e. above 1 $cm^2/V{\cdot}s$ and on/off ratio as high as 10^5. Patterned devices with small TiO_2/electrodes overlap show the highest transistor current and the highest charge carrier density, due to the larger specific capacitance.

I compared transistors based on solution processed porous and dense evaporated polycrystalline TiO_2 films making use of the ionic liquid [EMIM][TFSI] and [EMIM][TFSI] with lithium perchlorate as the electrolytes. EGTs based on evaporated unpatterned TiO_2 with [EMIM][TFSI] as a gating medium show higher current and better on/off ratio with respect to analogous solution processed devices. The electrical properties of EGTs based on porous solution processed films of TiO_2 can be also improved by gating with a mixture of [EMIM][TFSI] and lithium perchlorate as a gating medium. The mobility values increase from 0.27 $cm^2V^{-1}s^{-1}$ to 33 $cm^2V^{-1}s^{-1}$ by decreasing

the sweeping rate from 50mV/s to 50mV/60s.

Overall, our results demonstrate that TiO_2 electrolyte-gated transistors are promising for applications in low-voltage electronics, e.g. in bio and environmental sensing. The availability of a variety of TiO_2 nanostructures enables to achieve extraordinary large surface areas, as well as unique chemical, physical, and electronic properties. For instance, it is possible to fabricate EGTs with TiO_2 nanofibers to increase the surface area. Another opportunity would be to change the device geometry, for instance using bottom gated or planar configuration to allow functionalization of the TiO_2 surface for sensing applications. Moreover, since TiO_2 shows electrochromic properties upon intercalation of Li^+, our results are promising for the development of an electrochromic switch for smart windows applications. We believe that use of UV treatment or microvawe-assisted annealing will help to decrease the fabrication temperature for TiO_2 transistors on flexible substrate. Furthermore, fabrication of metal oxide transistors using aqueous electrolytes will be attractive for biomedical applications. We have already fabricated TiO_2 transistors gated with aqueous PBS solution.

Fabrication of fully transparent SnO_2 EG transistors, not requiring high temperature thermal treatments, is highly attractive for printable, transparent and flexible electronics. Deposition of transparent electrodes, with properties similar to like ITO but indium-free, together with deposition of transparent solid electrolyte, will allow fabrication of fully transparent SnO_2 EGTs with potential applications in smart windows and display technology. The choice of the right precursor and/or fabrication of ternary or quaternary metal oxide based on Sn are very attractive to decrease the deposition temperature and to obtain high performance devices.

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APPENDIX A – SUPORTING INFORMATION FOR THE ARTICLE 1

Tin dioxide electrolyte-gated transistors working in depletion and enhancement mode

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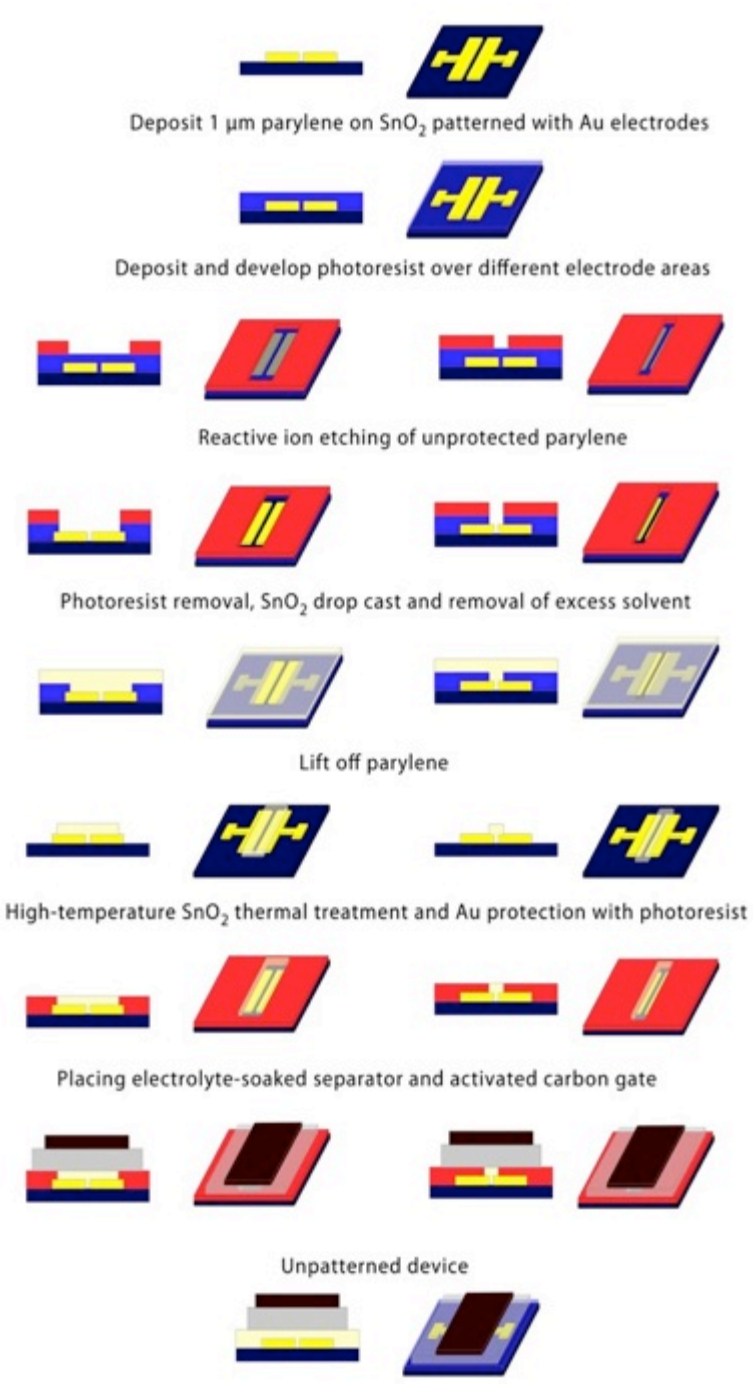

Figure S1. SnO_2 transistor fabrication on SiO_2/Si substrates (samples A, B, C). The geometric area of the SnO_2 in contact with the electrolyte is 0.0025 cm^2 for patterns A, 0.0492 cm^2 for patterns B and for 0.36 cm^2unpatterned devices C. The Au (40 nm) source and drain electrodes (W/L= 4000/10 µm/µm) with a Ti (4 nm) adhesion layer were patterned by conventional photolithography and lift-off. The ionic liquid [EMIM][TFSI] is used as the electrolyte and activated carbon as the gate electrode.

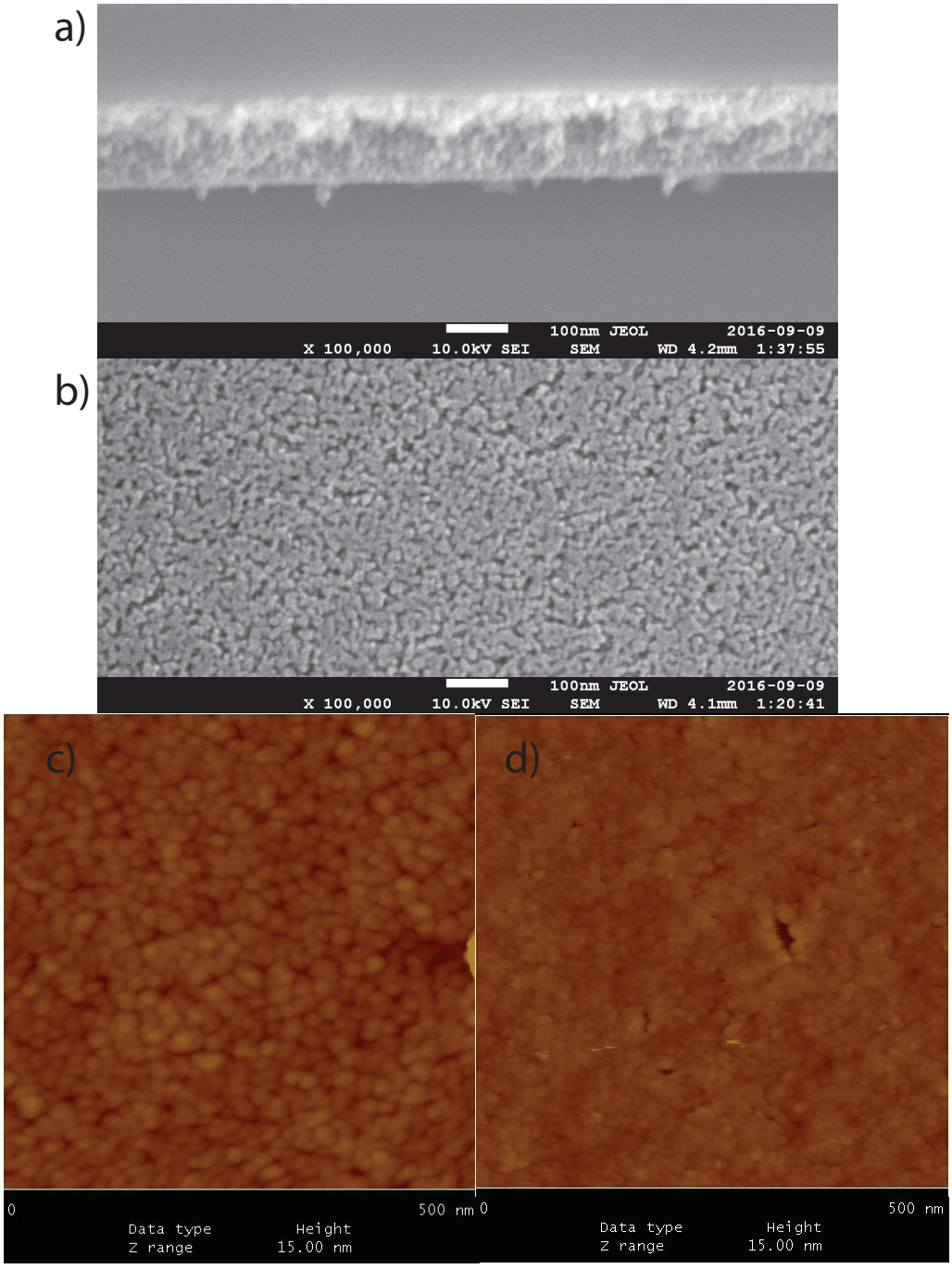

Figure S2. (a and b) High-magnification Scanning Electron Microscopy images of SnO_2 films treated at 450 °C; (c) Atomic Force Microscopy images of SnO_2 films annealed at 450 °C (the rms roughness in this image is 0.8 nm; the roughness for 30 um × 30 um-sized images is 1.5 nm) and (d) at 350 °C (the roughness in this image is 0.3 nm; the roughness for 30 um × 30 um-sized images is 18 nm).

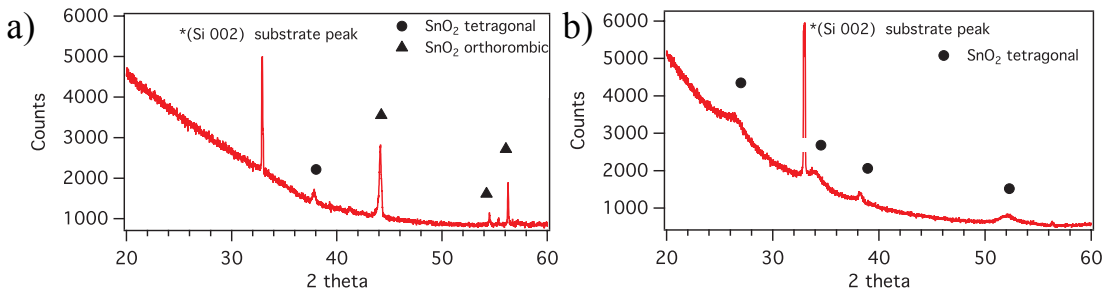

Figure S3. X-ray diffraction (XRD) patterns of SnO_2 films on SiO_2/Si substrates thermally treated in ambient atmosphere at a) 350 °C and b) 450 °C.

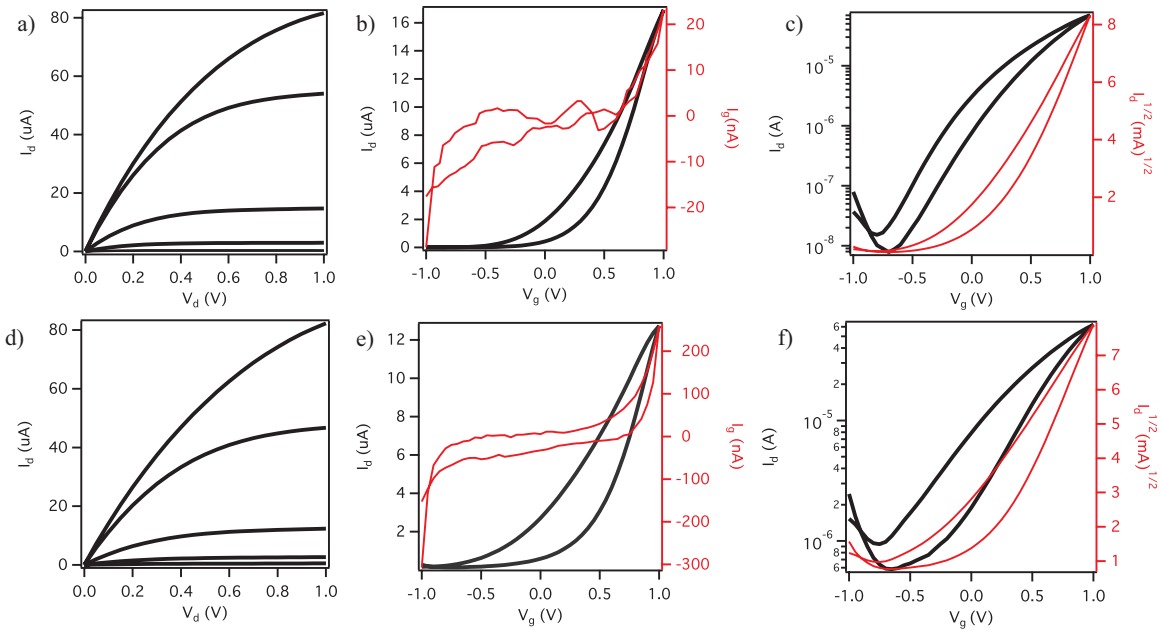

Figure S4 Output (**a** and **d**, at V_g = 0 V, 0.3 V, 0.5 V, 0.7 V, 1 V) and transfer characteristics in saturation (**b** and **e**, at V_d=1 V) and in the linear regime (**c** and **f**, at V_d=0.2 V) of [EMIM][TFSI]-gated SnO_2 transistors for devices A1 (**a, b, c**) and B1 (**d, e, f**). The thickness of SnO_2 films for transistors A1 (**a, b, c**) is ca. 10 nm whereas for transistors B1(**d, e, f**) is ca. 25 nm. Scan rate 50 mV/s.

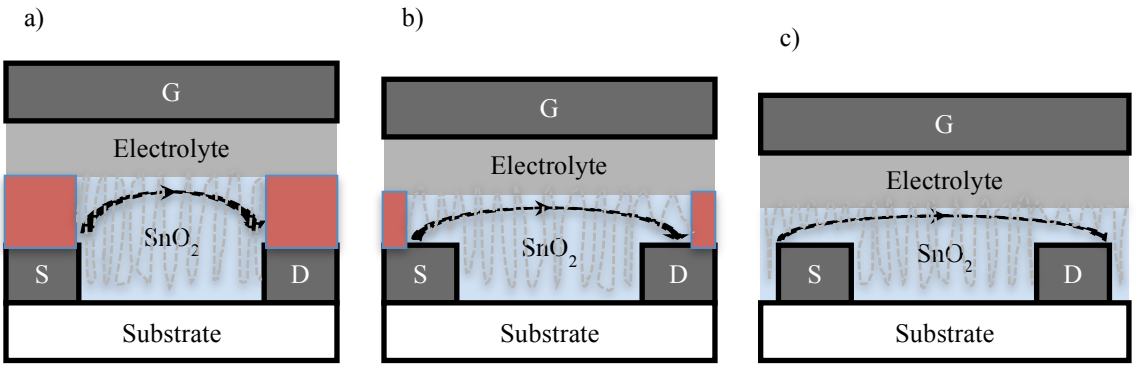

Figure S5. Schematic of SnO_2 transistors on SiO_2/Si substrate: a) patterned device A (geometric area of SnO_2 in contact with [EMIM][TFSI] is 0.0025 cm^2 whereas surface area using BET is 0.62 cm^2); b) patterned device B (geometric area 0.0492 cm^2 and BET area is 5.3 cm^2); c) unpatterned transistor C (geometric area 0.36 cm^2, BET area 33 cm^2).

Assuming that the ions of the electrolyte penetrate through the total depth of the SnO_2 thin film, we were interested in gaining insight into the surface area of the films. Therefore, we deduced the surface area of SnO_2 thin films using the Brunauer−Emmett−Teller (BET) method: the BET specific surface area of SnO_2 films treated at 450 °C is 33 m^2/g whereas at 350 °C is 58.9 m^2/g. The density of the films $d = \frac{mass}{thickness \cdot geometric\ area}$ (considering that the mass of the powder obtained from the film is of 0.0001 g) was therefore d = 0.0001 g/(0.000015 cm · 0.4 cm^2) = 16.6 g/cm^3. Using the geometric areas and thickness of SnO_2 films we found the weight of the films for patterned transistors A = 16.6 $g/cm^3 \cdot 0.000045$ cm·0.0025 cm^2 = 0.0000019 g; for B = 16.6 $g/cm^3 \cdot$ 0.00002 cm·0.0492 cm^2 =0.000016 g. Therefore, using the BET analyses, we deduced that the surface area for A is 0.0000019 g·33 m^2/g = 0.000062 m^2 =0.62 cm^2, for B = 0.000016 g·33 m^2/g=0.00053 m^2 = 5.3 cm^2 and for C = 0.0001 g·33 m^2/g=0.0033 m^2 = 33 cm^2; for D = 0.0001 g·58.9 m^2/g=0.00589 m^2 = 58.9 cm^2.

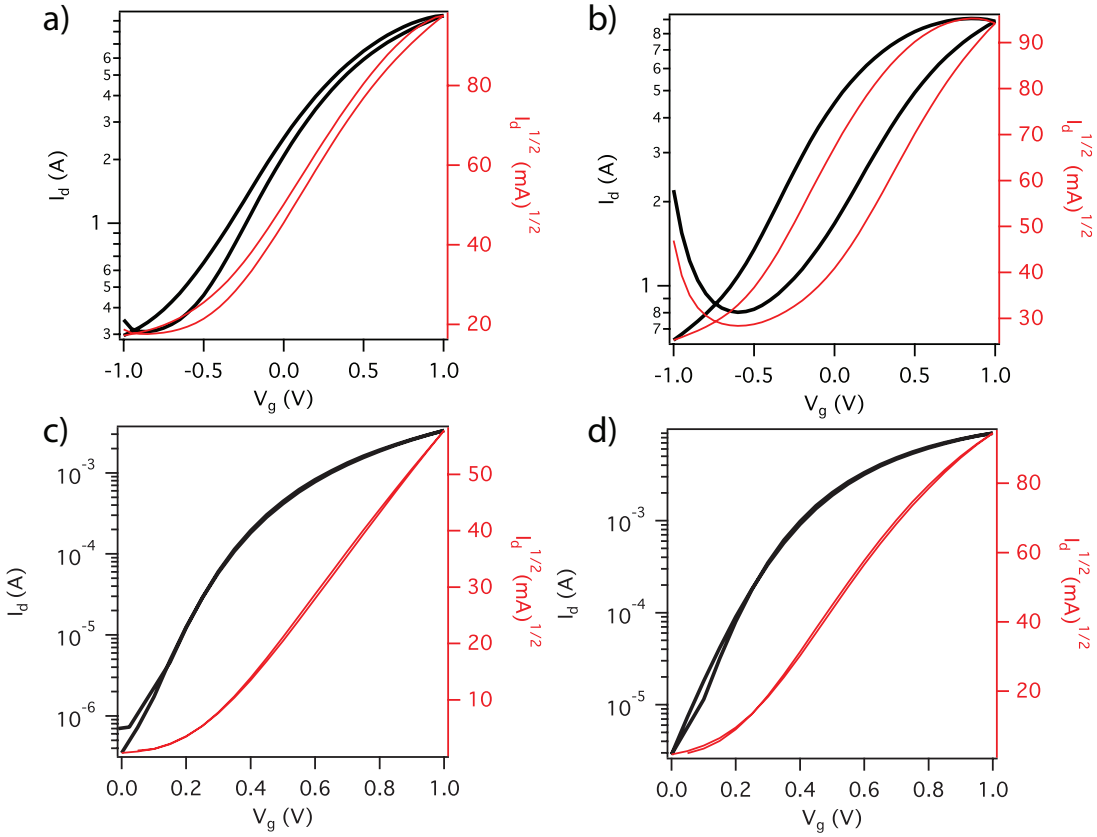

Figure S6. Transfer characteristics in saturation regime (V_d = 1 V) of [EMIM][TFSI]-gated SnO_2 transistors at for devices a) A, b) B, c) C and d) D. The scan rate is 50 mV/s.

Electron mobility using the pseudocapacitance values deduced from cyclic voltammetry We extracted the electron mobility from the transfer characteristics in the linear and saturation regimes, using the relationships: $\mu_{lin} = \frac{\partial I_d}{\partial V_g}\frac{L}{WC_iV_d}$ and $\mu_{sat} = \left(\frac{\partial\sqrt{I_d}}{\partial V_g}\right)^2 \frac{2L}{WC_i}$, where we used the pseudocapacitance (C_i) extracted from the cyclic voltammetry. The capacitance extracted for unpatterned films is 0.014 mF (unpatterned C) and ~0.085 mF (unpatterned D) for the voltage range 0 V<V_g< -1 V. For patterned devices, the values of the capacitance are 0.0013 mF (small patterns A) and 0.0031 mF (large patterns B) for 1V<V_g< -1 V. The capacitance density (obtained considering the BET surface area) changes as follows: ~0.002 mF/cm^2 for A, 0.0006 mF/cm^2 for B, 0.0004 mF/cm^2 for C and ~0.0025 mF/cm^2 for D.

The linear mobility is 6.5 ± 3 cm^2/(V s) for devices A and 20 ± 5 cm^2/(V s) for B, whereas it is 40 ± 10 cm^2/(V s) for devices C and 20 ± 5 cm^2/(V s) for D. The saturation mobility is 8.5 ± 3 cm^2/(V s) for devices A, 30 ± 5 cm^2/(V s) for B, 90 ± 10 cm^2/(V s) for C and 40 ± 5 cm^2/(V s) for D. The linear mobility calculated using the charge carrier density and the paseudocapacitance are quite similar. The fact that the saturation mobility values are higher than the linear ones is probably due to the presence of a Schottky barrier at the Au/SnO_2 interface (the work function of Au is 5.1 eV whereas the conduction band of SnO_2 is located at ca. 4.4 eV). The linear electron mobility extracted using the geometric area is 0.02±0.05 cm^2/V·s for films A, 0.2±0.1 cm^2/V·s for B, 0.6±0.2 cm^2/V·s for C and 0.2±0.05 cm^2/V·s for D. The saturation mobility is 0.03 ± 0.05 cm^2/(V s) for devices A, 0.3 ± 0.1 cm^2/(V s) for B, 1.5 ± 0.1 cm^2/(V s) for C, and 0.3 ± 0.1 cm^2/(V s) for D.

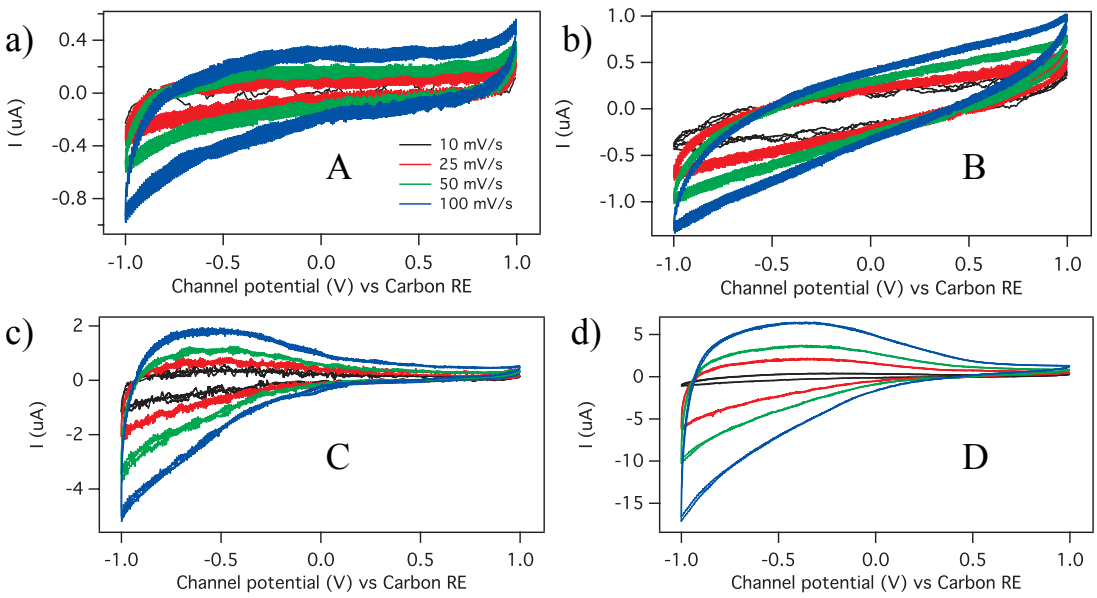

Figure S7. Cyclic voltammetry in transistor configuration (see main text) of SnO_2 films for the devices: a) A; b) B; c) C; d) D in the electrolyte [EMIM][TFSI], at scan rates of 10, 25, 50, 100 mV/s.

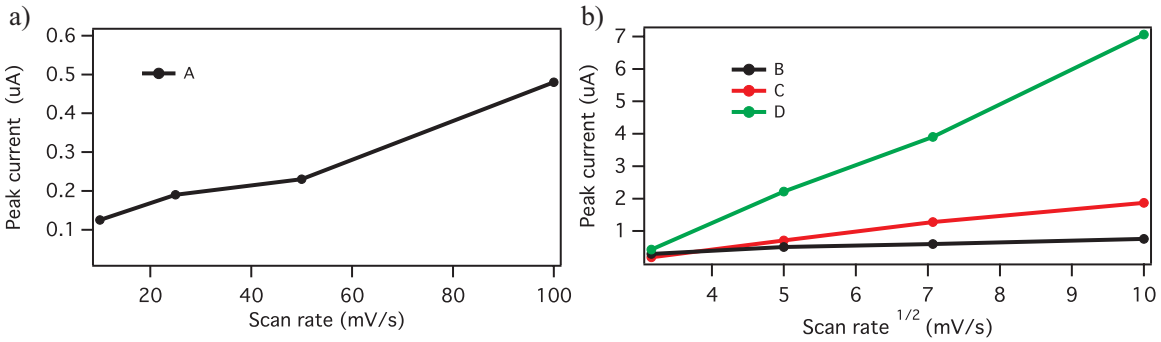

Figure S8. Dependence of the voltammetric current of the cathodic signature (located at about -0.5 V vs carbon quasi reference electrode) on the potential sweep rate for samples A (a); B, C, D (b). The lines are guides to the eye.

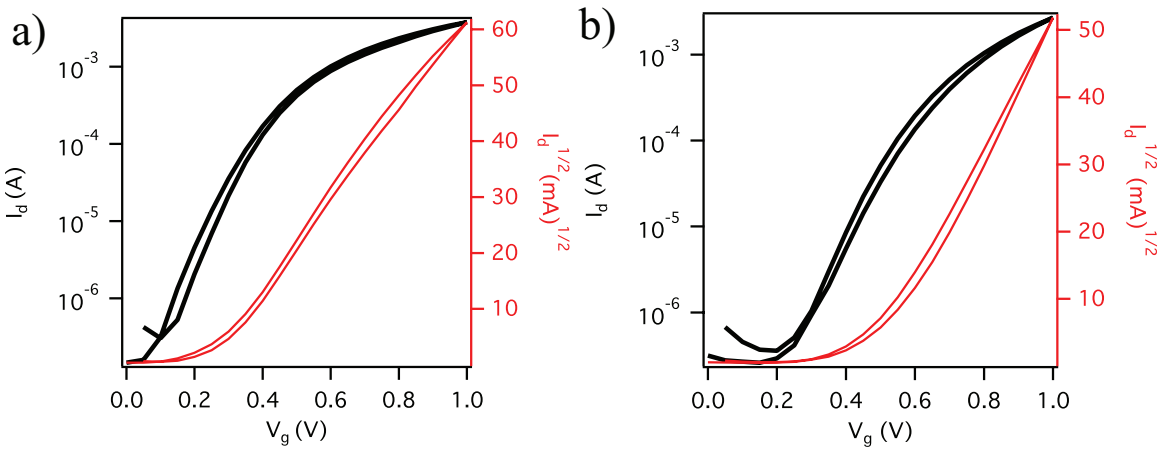

Figure S9. Transfer characteristics of [EMIM][TFSI]-gated SnO_2 transistors on polyimide substrates. Linear regime (V_d=0.2 V) a) before bending and b) under bending, at R=10 mm. Saturation regime (V_d=1 V) c) before bending and d) under bending at R=10 mm. Scan rate 50 mV/s.

Table S1

Name	BE	Identification	At. %	
			Annealed at 450 °C	Annealed at 350 °C
C1s	285.0	C-C	15.6	8.7
	286.7	C-O, C-O-C	2.7	1.6
	288.9	O-C=O	1.0	1.6
O1s	530.9	Sn-O in SnO_2	37.4	42.8
	532.3	7.1 Adsorbed OH or Sn-OH, C=O	17.2	14.4
	533.3	C-O	4.7	4.6
Sn3d5/2	487.0	Sn^{4+} in SnO_2	21.4	26.2

Table S2. Electrical characteristics of SnO_2 electrolyte-gated transistors with different channel thickness.

"Dep." stands for depletion mode of operation and "En." for enhancement mode of operation.

	A	**A1**	**B**	**B1**	**C**	**D**
Thickness (nm)	450	10	200	25	150	150
Surface area deduced from BET analysis (cm^2)	0.62		5.3		33	58.9
$n\times10^{12}$ (cm^{-2}) (from the BET surface area)	9	-	1.5	-	1	4
μ_{lin}, $cm^2/(V\cdot s)$ (deduced using the BET surface area)	10±2	-	40±10	-	45±15	25±5
$n\times10^{14}$ (cm^{-2}) (from geometric area)	20	1	2	1.6	1	6
μ_{lin}, $cm^2/(V\cdot s)$ (deduced using the geometric area)	0.04±0.05	0.01 ±0.02	0.4 ±0.2	0.01±0.002	0.6 ±0.2	0.16 ± 0.1
on/off	~10	~10^4	~10	~10^2	~10^4	~10^4

V_{th} (V)	-0.45	0.2	-0.25	0.15	0.3	0.3
Mode of operation	Dep.	En.	Dep.	En.	En.	En.

APPENDIX B – SUPPORTING INFORMATION FOR THE ARTICLE 2

Photolithographically patterned TiO_2 films for electrolyte-gated transistors

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ACS Appl. Mater. Interfaces, 8, 14855−14862, 2016.

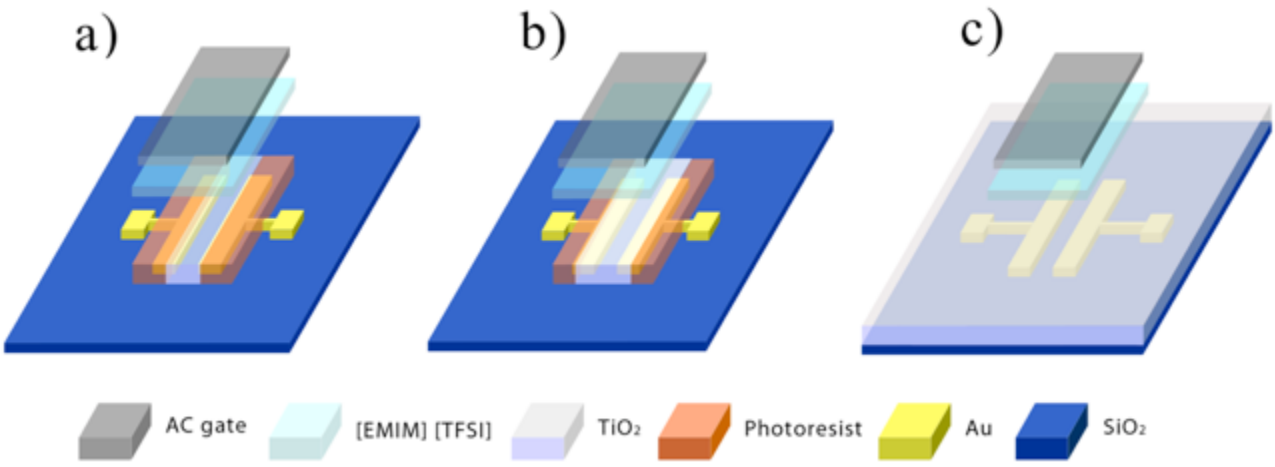

Figure S1. Device structures of [EMIM][TFSI]-gated TiO_2 transistors with pattern A (a), pattern B (b) and unpatterned, C (c). During patterning of TiO_2 transistor channel, care was taken to ensure that the ionic liquid did not overlap the top of the Au contacts to limit parasitic capacitances

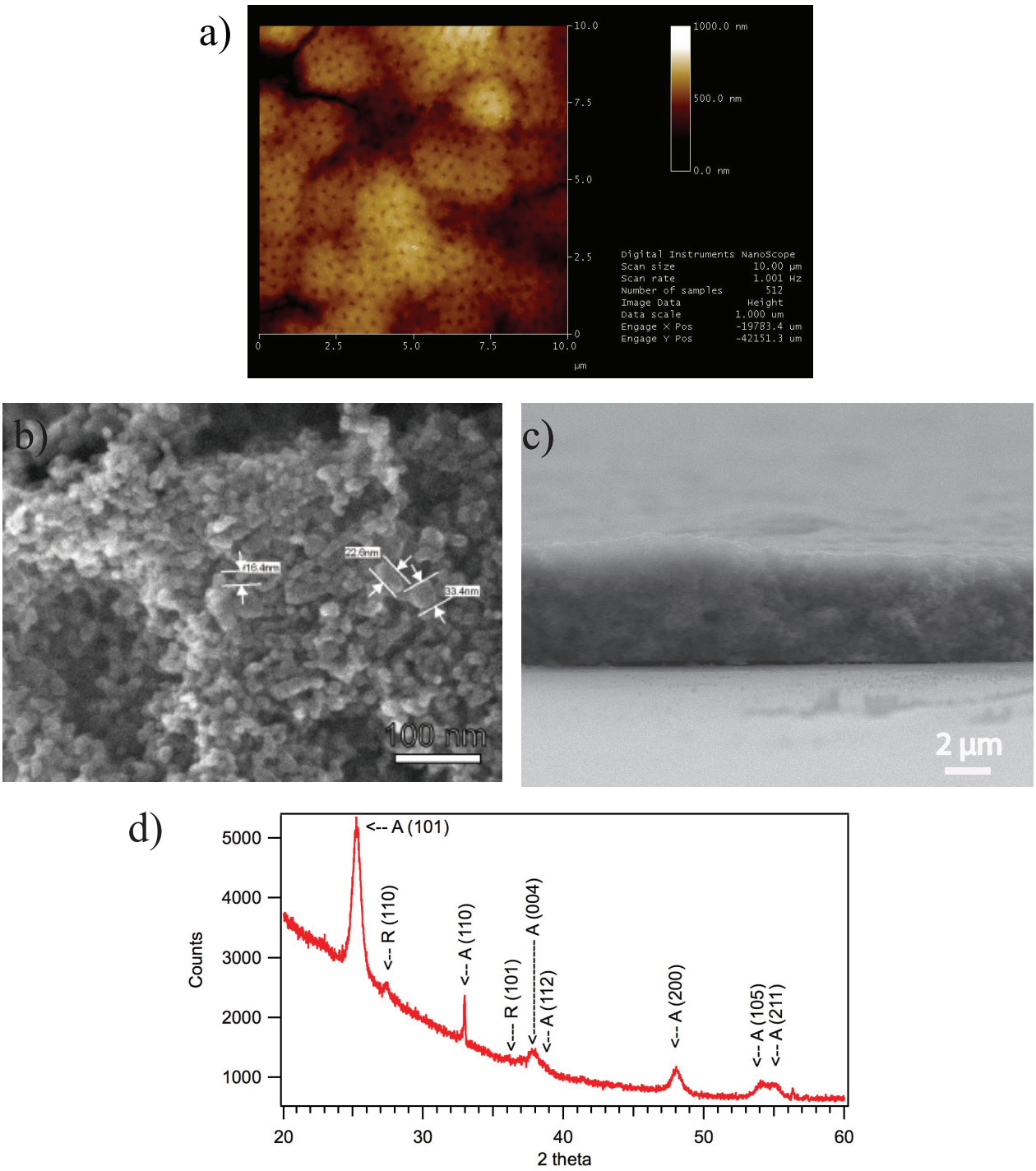

Figure S2. TiO_2 films investigated in this work: a) Atomic Force Microscopy image (10 µm x 10 µm); b) high-magnification Scanning Electron Microscopy image, 5 kV; c) Scanning Electron Microscopy image of the TiO_2 film edge after Parylene peel-off, 10 kV; d) X-ray Diffraction pattern (symbol A indicates peaks attributable to the anatase phase whereas symbol R indicates peaks attributable to rutile).

The structure and morphology of the drop-cast TiO_2 films were investigated by Atomic Force Microscopy (AFM, Figure S2 a) Scanning Electron Microscopy (SEM, Figure S2 b and c) and X-ray diffraction (XRD, Figure S2 d). AFM images give a rms of 120 ± 10 nm. SEM images show that TiO_2 films consist of particles about 15-40 nm-sized. XRD patterns show that our TiO_2 films are polycrystalline. As expected, the TiO_2 films include both anatase (ca. 92% as deduced from the Spurr and Mayers relationship) and rutile phases.[1] The average crystallite size calculated from the half width at half maximum of the peak A (101) (Figure S2 c) by the Debye-Scherrer relationship is 14 nm ± 5 nm.

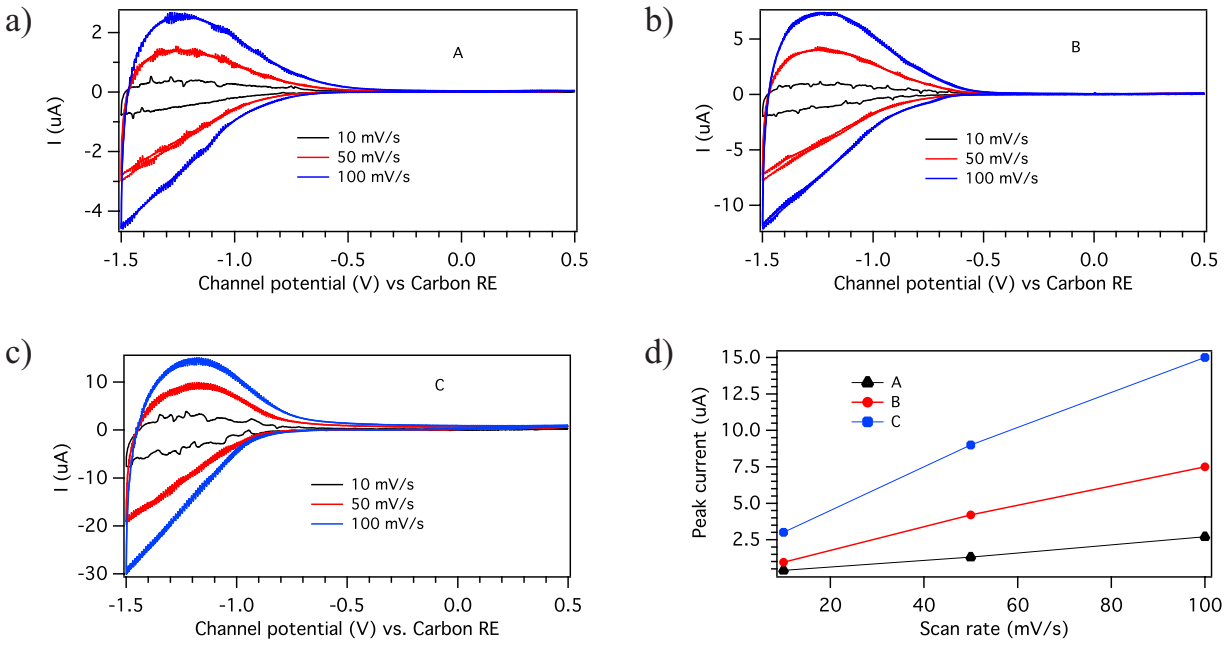

Figure S3. Cyclic voltammetry studies in transistor configuration of TiO_2 films of type A (a), B (b), and C (c) (see main text for the meaning of A, B, C). TiO_2 films included between the source and drain electrodes acted as the working electrode whereas the carbon gate acted as the counter and the quasi reference electrode. Dependence of the voltammetric current of the anodic peak (located at about 1.25 V vs carbon quasi reference electrode) on the electrode potential sweep rate for samples A, B and C (d), (coefficient of determination R^2 is 0.99). The electrolyte was the room temperature ionic liquid [EMIM][TFSI].

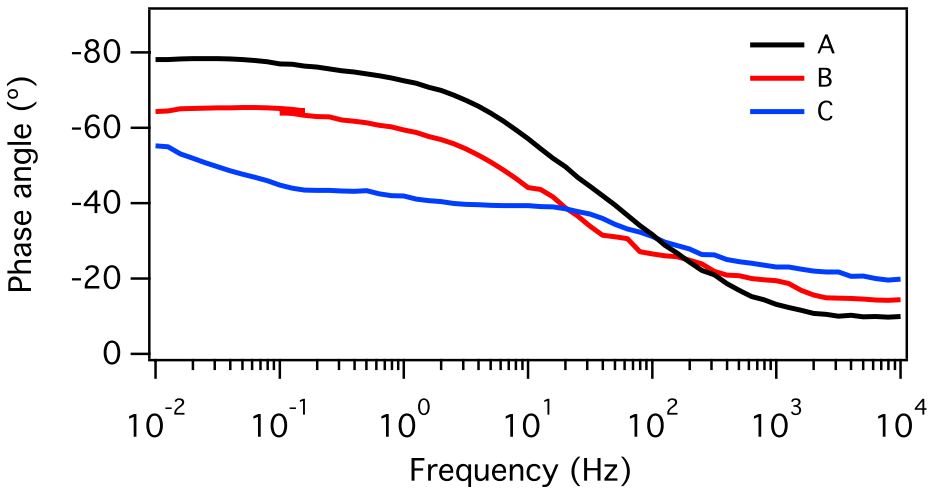

Figure S4. Phase angle vs frequency plot obtained using the TiO_2 thin film included between the source and drain electrodes as the working electrode and the carbon gate as the quasi reference electrode, at 1 V vs carbon quasi reference, for samples A, B and C. The electrolyte was [EMIM][TFSI].

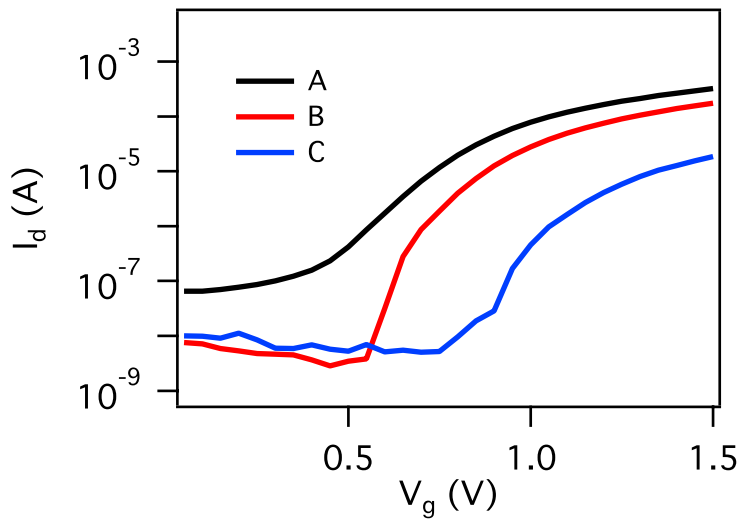

Figure S5. Transfer characteristics in the linear regime (V_d = 200 mV) for the [EMIM][TFSI]-gated TiO_2 transistors investigated in this work (for the meaning of A, B, C see main text).

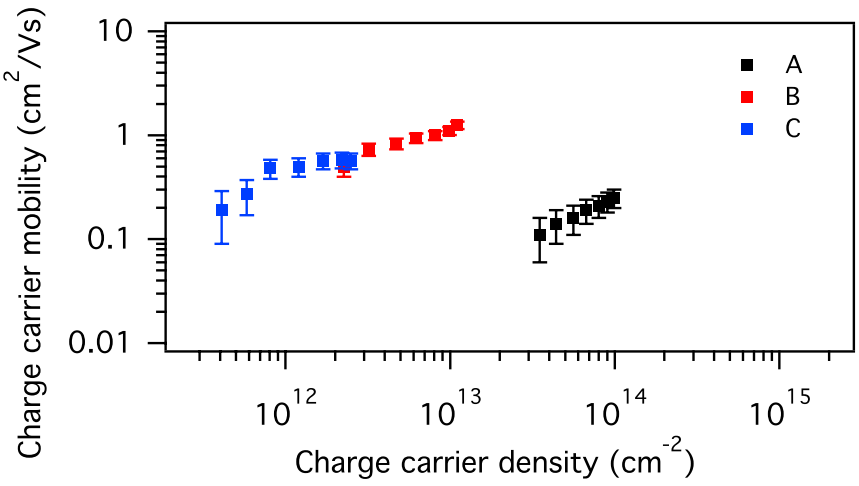

Figure S6. Charge carrier mobility vs charge carrier density. The charge carrier density was extracted increasing the $|V_g|$ extreme of integration during transfer curves obtained in the linear regime. Intervals of $|V_g|$ values considered are: 0-0.9 V, 0-1 V, 0-1.1 V, 0-1.2 V, 0-1.3 V, 0-1.4 V, 0-1.5 V, for the three types of films investigated in this work: A, B, C (see main text for the meaning of the symbols A, B and C).

Table 1: Sweep rate dependence of the capacitance for of TiO_2 films (patterns A, B, and C).

	Pattern A Capacitance (mF/cm^2)	*Pattern B Capacitance (mF/cm^2)*	*Pattern C Capacitance (mF/cm^2)*
Scan rate 10 mV/s	*1.4×10^{-2}*	*2.8×10^{-3}*	*1.6×10^{-3}*
Scan rate 50 mV/s	*1.0×10^{-2}*	*2.4×10^{-3}*	*1.0×10^{-3}*
Scan rate 100 mV/s	*9.8×10^{-3}*	*2.0×10^{-3}*	*7.6×10^{-4}*

References

(1) Spurr, R.; Myers H. Quantitative Analysis of Anatase-Rutile Mixtures with an X-Ray Diffractometer. *Anal. Chem*. **1957**, *29*, 761–762.

APPENDIX C – LIST OF PUBLICATIONS IN POLYTECHNIQUE MONTREAL NOT INCLUDED TO THE THESIS

[1] Valitova I, Amato M, Mahvash F, Cantele G, Maffucci A, Santato C, Martel R and Cicoira F, Carbon nanotube electrodes in organic transistors. Nanoscale, (5) 4638, 2013.

[2] Coppedè N,* Valitova I,* Mahvash F, Tarabella G, Ranzieri P, Iannotta S, Santato C, Martel R, Cicoira F, Titanyl Phthalocyanine ambipolar thin film transistors making use of carbon nanotube electrode, Nanotechnology, 25(48) 485703, 2014.

[3] Z. Yi, L.G. Bettini, G. Tomasello, P. Kumar, P. Piseri, I. Valitova, P. Milani, F. Soavi, F. Cicoira, Flexible conducting polymer transistors with supercapacitor function, J. Polym. Sci. Part B: Polym. Phys. 55, 96-103 , 2017.

* - Authors are equally contributed.

APPENDIX D – PARTICIPATION IN THE CONFERENCES

1. “Photolithographically Patterned Metal Oxide Electrolyte-Gated Transistors” Materials Research Society (MRS) Fall Meeting and Exhibit, 2016, Boston, Oral presentation.

2. “Charge carrier density modulation in polycrystalline TiO_2 electric double layer transistors” Materials Research Society (MRS) Fall Meeting and Exhibit, 2015, Boston, Poster presentation.