UNIVERSITÉ DE MONTRÉAL

DIFFERENTIAL INTEGRATOR PIXEL ARCHITECTURE FOR DARK CURRENT COMPENSATION IN CMOS IMAGE SENSORS

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DIIFFERENTIAL INTEGRATOR PIXEL ARCHITECTURE FOR DARK CURRENT COMPENSATION IN CMOS IMAGE SENSORS

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DEDICATION

To my family

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RÉSUMÉ

Le Capteur d'Image CMOS (CIS) est rapidement devenu la technologie dominante dans les marchés de l'imagerie. Il y a des avantages sur les technologies avec CCD tels que la faible consommation de puissance et les faibles coûts. . La technologie CMOS APS s'est améliorée au cours des dernières décennies et propose une alternative viable à la technologie CCD pour de nombreuses applications. Néanmoins, les capteurs d'image CMOS APS ont un niveau plus élevé de courant d'obscurité que les capteurs CCD. Plusieurs techniques ont été développées pour améliorer la performance du capteur d'image en termes de courant d'obscurité qui limite sévèrement la gamme dynamique et la sensibilité des capteurs d'image.

Il existe différentes approches pour réduire le courant d'obscurité. L'approche idéale, mais coûteuse, consiste à modifier le procédé de fabrication par améliorant la photosensibilité du pixel ou de réduire le courant de fuite. Cependant, certaines architectures de circuits peuvent être utilisées pour réduire ou compenser le courant d'obscurité sans modification de procédé, cette alternative fait l'objet de ce mémoire.

Dans cette thèse, un circuit amplificateur différentiel multi-branche est proposé pour compenser l'effet de courant d'obscurité d'un capteurs d'image CMOS. Afin d'obtenir une application de détection à faible courant de noirceur, un interrupteur de type T avec un faible courant de fuite est utilisé. La nouvelle configuration de multiple-input multiple-output amplificateur différentiel présente l'avantage de réduire considérablement les courants d'obscurité femto-ampères des photodiodes. L'objectif étant d'améliorer la sensibilité et la gamme dynamique des pixels des capteurs d'image CMOS. Un prototype est conçu à partir du procédé de fabrication CMOS standard 0.18 µm de TSMC.

ABSTRACT

CMOS Image Sensor (CIS) rapidly became the dominant technology over Charge-Coupled-Device (CCD) in imaging markets. It has many advantages over CCDs such as low power and low cost which is highly desirable for imaging-enabled mobile devices. CMOS Active Pixel Sensor (APS) technology has improved during the last decades and suggests a viable alternative for many applications with CCD technology. Nonetheless, CMOS APS image sensors have higher dark current level than CCD sensors. Several techniques have been developed to improve the performance of image sensor in terms of dark current which severely limits the dynamic range and the sensitivity of image sensors.

There are different approaches to reduce the dark current. The ideal but expensive approach is to modify the fabrication process by enhancing the photosensivity of the pixel or reducing the leakage current. However, some circuit and layout techniques reduce or compensate the dark current of standard CMOS processes which is the method considered in this work.

In this thesis a multi-branch differential amplifier circuit is proposed to compensate the effect of dark current in CMOS image sensors. In order to obtain a low level sensing application, a T-type switch with low leakage current is used. The new configuration of multiple-input multiple-output differential amplifier has the advantage of compensating the femto-ampere dark currents of photodiodes. The objective is to improve the sensitivity and the dynamic range of active pixel CMOS image sensors. A prototype is designed and simulated in a standard CMOS 0.18 µm fabrication process from TSMC.

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ABREVIATIONS

CMOS	Complementary Metal-Oxide-Semiconductor
ADC	Analog to Digital Converter
APS	Active Pixel Sensor
CCD	Charge Coupled Device
CIS	CMOS Image Sensor
CDS	Correlated Double Sampling
CMC	Canadian Microelectronics Corporation
TSMC	Taiwan Semiconductor Manufacturing
CMOS	Complementary Metal Oxide Semiconductor
DFF	D flip-flops
DC	Direct Current
FD	Floating Diffusion
SR	Shift Register
SF	Source Follower
DPS	Digital Pixel Sensor
DR	Dynamic Range
FF	Fill Factor

FPN	Fixed Pattern Noise
EHP	Electron-Hole Pair
IC	Integrated Circuit
MOS	Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
PPS	Passive Pixel Sensor
fF	Femto Farad
nF	Nano Farad
pF	Pico Farad
fA	Femto Ampere
nA	Nano Ampere
pA	Pico Ampere
Si	Silicium
SiO2	Silicon Dioxyde
SNR	Signal to Noise Ratio
S/H	Sample and Hold
QE	Quantum Efficiency
CTIA	Capacitive Transimpedance Amplfier
TG	Transmission Gate
STI	Shallow Trench Isolation

PPD	Pinned Photodiode
DPS	Digital Pixel Sensor
IREV	Reverse-biased junction leakage current
GIDL	Gate-Induced Drain Leakage
DSM	Deep Submicron
MIM Cap	Metal-Insulator-Metal Capacitor
SUB	Sub-Threshold
RMS	Root Mean Square
PSD	Power Spectral Density
STD	Standard Deviation
A/D	Analog to Digital Converter

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INTRODUCTION

CMOS imaging sensors are taking over the imaging sensor market mainly due to their low cost and low power consumption and compactness [1]. Charged Coupled Device (CCD) imagers were the dominant technology in last two decades due to their image quality and flexibility. CCDs do not allow system on a chip with ancillary circuits such as signal processors, and analog-to-digital converters (ADCs) while CMOS imagers have provided system on a chip, low-power, and cost effective imaging systems. Recent advances in CMOS imaging sensor fabrication process such as PIN photodiodes and backside illumination have considerably bridged the gap between CMOS and CCD sensors.

Compared to CCD image sensors, CMOS image sensors have higher dark current and high level of fixed pattern noise [2]. The dark current is the leakage current of reverse-biased photodiode which destroys the imaging performance especially under low illumination [3]. A large dark current in the photodiode array of a CMOS imager limits the sensor's dynamic range considerably by reducing the signal swing. The expected dynamic range value for CMOS image sensors is about 54dB which assesses the ability of a sensor to properly image both high lights and dark shadows in a scene. Also, the dark current prevents the sensor from taking images at low illumination levels. Several techniques have been proposed to reduce or compensate dark current. The differential dark current compensation technique cannot effectively reduce the dark current due to different reverse bias voltage on photodiodes in each pixel which leads to non-uniformity in pixel array [3, 4]. Previous work has shown the significant effect of varying the reverse bias voltage across the photodiode [5]. In [6] multiple- input multiple-output differential amplifier with negative feedback integrator is implemented. The feedback on a differential architecture fixes the integrating nodes of photodiodes to a constant voltage which leads to a more uniform dark current within the pixel array [4]. Therefore, the uniform dark current can be cancelled by subtracting a dummy (dark) pixel output from an illuminated pixel. However, the multiple-input multiple-output differential technique proposed in [6] cannot sense low illumination levels which needs dark current compensation in the femto-ampere range.

Motivation

The motivation of this work is to reduce the effect of dark current on CMOS image sensors. The implemented design should have the ability to manage and compensate for small values of dark current in the femto-ampere range. In order to reduce the effect of dark current which reduces the dynamic range of an image sensor, the new configuration of multiple-input multiple-output differential amplifier with advantage of managing the femto-ampere dark currents of photodiode is proposed in this work.

Objective

The main objective of this work is to design a circuit which compensates the effect of dark current in CMOS image sensors. Dark current severely limits the performance of image sensors in terms of dynamic range and sensitivity. In this work, a pixel architecture designed in a standard TSMC CMOS 0.18 μm process is designed and simulated at the post-layout level in order to prove its effectiveness in reducing the effect of dark current.

Thesis Organization

This master's thesis is organized as follows: In Chapter one, a brief overview on CMOS image sensor and their dark current characteristics is presented. Then, MOS switches and their leakages are described.

Chapter 2 is dedicated to the design of a pixel structure of a CMOS image sensor intended to eliminate the effect of dark current. The differential structure for compensating the dark current effect which was proposed in [6] is first introduced. Then, a new architecture for compensating the dark current effect with ability of sensing low illumination levels is proposed.

Chapter 3 presents the pre-layout and post-layout simulation results using a row array of pixels.

Finally, the thesis is concluded and future improvements are suggested.

CHAPTER 1 IMAGE SENSOR CHARACTERISTICS AND DARK CURRENT

1.1 Image Sensors

An image sensor comprises a two-dimensional array of pixels. Each pixel consists of a photodetector which converts incident light into photocurrent. The electrical circuits process and store the photocurrent into a readable electrical signal. The electrical signal is read out of the pixel array and digitized by an analog-to-digital converter (ADC). The Array size of a digital image sensor can be as large as tens of megapixels for high-end applications, while individual pixel sizes can be as small as 2 by 2 μm [7].

Solid-state image sensors are the main building blocks of digital imaging devices; they are well suited for low-cost, compact and digital video cameras due to their advantages, such as weight, size, cost and power consumption.

Two main solid-state image sensor technologies are presented in this Chapter: CCD (Charged Coupled Devices) and CIS (CMOS Image Sensors).

1.2 CMOS Image Sensors

Standard Complementary Metal-Oxide Semiconductor (CMOS) technologies have some advantages over CCD technology, such as low power and low cost, which is highly desirable for mobile devices.

Figure 1.1.b shows the architecture of CMOS image sensor which consists of an array of pixels. By scanning vertically one row of the array can be addressed and by scanning horizontally, a single pixel out of the selected row can be addressed. Therefore, an individual pixel can be selected randomly and sent to the output amplifier. The structure of this readout mechanism allows a random access to all individual pixels in the array which is similar to SRAM and DRAM memory structures [8].

Three basic classifications of pixel structures in CMOS image sensors are: Passive pixel sensor (PPS), Active pixel sensor (APS) and Digital pixel sensor (DPS).

1.2.1 Passive Pixel Sensor (PPS)

The simplest structure of CMOS image sensor is PPS which has only one transistor per pixel. The selected signals of columns by means of column decoder are transferred to the output amplifier. PPS has small pixel size and high fill factor but suffers from very poor signal to noise ratio (SNR) and low readout speed. The mismatch between small photodiode capacitor and large vertical and horizontal bus capacitors, add a large noise value to readout signal (poor SNR). To eliminate this noise effect, a column amplifier is added to the column lines of the array as shown in Figure 1.1.b.

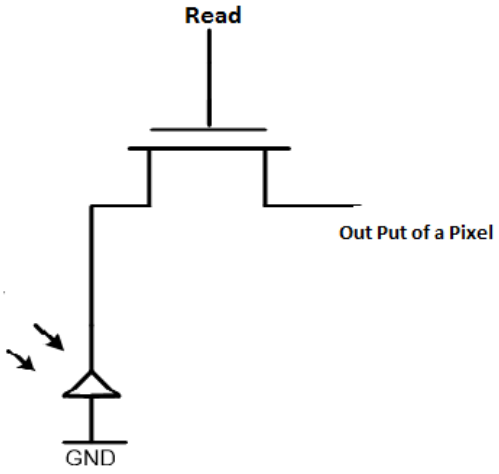

Figure 1.1.a pixel structure of PPS

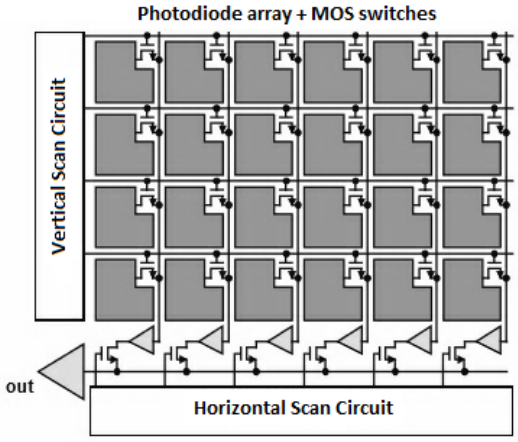

Figure 1.1.b structure of CMOS PPS[8]

1.2.2 Active pixel sensor (APS)

Almost all CMOS designs today use active pixels sensor structure. Each pixel consists of three transistors (3T pixel) where one transistor works as buffer or amplifier. Complex CMOS pixel designs which include more transistors (4T and 5T) have been used to add noise reduction and shuttering functions [9]. The simpler structure with less number of transistors has a better fill factor. Although the fill factor of a CCD sensor remains much higher than the 3T CMOS sensor.

In APS configuration only the mismatch effect of horizontal column capacitance has been removed but there is still noise in readout signal from large column capacitance which is connected to photodiode capacitor. In order to solve this problem every pixel gets its own amplifier as shown in Figure 1.2.b.

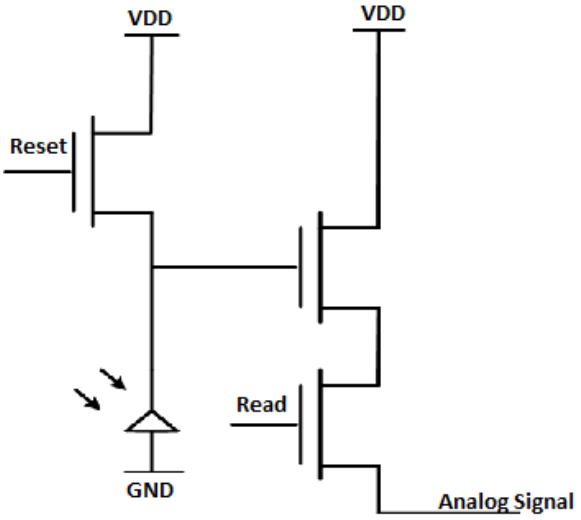

Figure 1.2.a pixel structure of APS

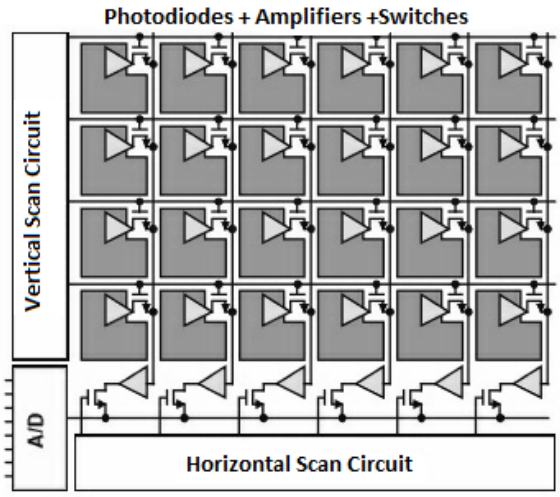

Figure 1.2.b structure of CMOS APS [8]

1.2.3 Pinned Photodiode Active Pixel Sensor (APS)

The most popular pixel sensor architecture is Pinned photodiode (PPD) APS. The idea is coming from buried channel CCD to increase the sensitivity and reduce the dark current. The schematic of PPD APS is shown in Figure 1.3.

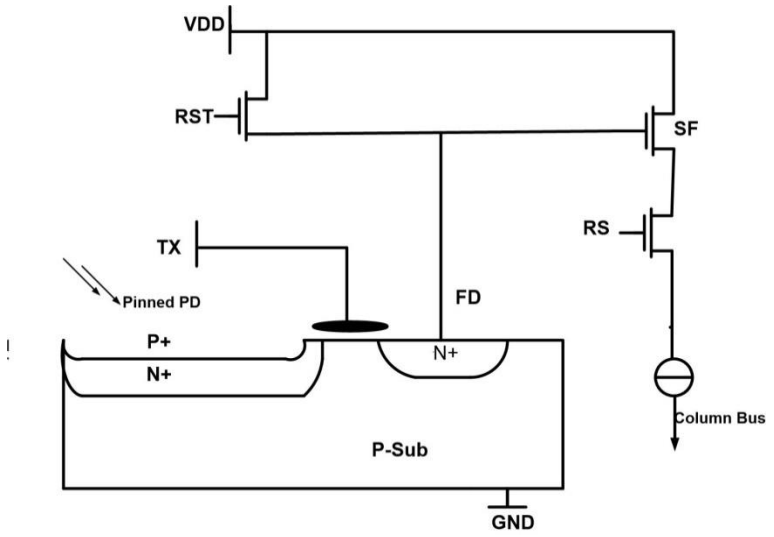

Figure 1.3. Pixel structure of a Pinned Photodiode APS [9]

The pinned photodiode pixel consists of a photo sensing element which is a pinned diode (p+-n+-p), where the n+ region (floating diffusion) is pulled away from the silicon surface in order to reduce the surface defect noise such as dark current [10]. The pixel consists of four transistors (4T) including a transfer gate (TX), reset transistor (RST), source follower (SF), and row-select (RS) transistor. The transfer gate separates the floating diffusion (FD) from the photo sensing part. Timing diagram for pixel readout of the pinned photodiode APS is shown in Figure1.4. First, the TX gate and RST switches are turned on at the same time, and floating diffusion node is reset to high voltage (V_{DD}) and the pinned photodiode fully depletes the photodiode. By starting the integration after turning off the TX and RST, the photo generated electrons are stored in the n+ region of the device. During the pixel readout, the floating diffusion is first reset to V_{DD}. The reset voltage may now be readout for true correlated double sampling. Then the transfer gate is turned on, and the whole generated charges from photosensing element are transferred to the floating diffusion node. Also this voltage is readout through correlated double sampling and decreases the noise. The Pinned photodiode APS has good sensitivity to the blue light and has low dark current.

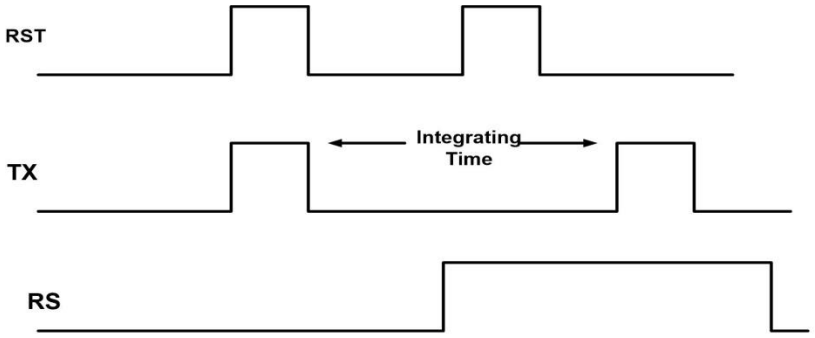

Figure 1.4. Readout timing diagram of PPD APS

1.2.4 Digital Pixel Sensor (DPS)

In DPS architecture each pixel has its own analog-to-digital converter (ADC) and the pixel output is a digital signal. Since ADCs are close to the generated signals of each pixel, it has higher SNR and faster read-out speed. Also the fill factor of DPS is significantly smaller than the traditional architecture. Existence of ADC in each pixel increases the fixe pattern noise of this structure which is caused by the mismatch between individual pixels [11].

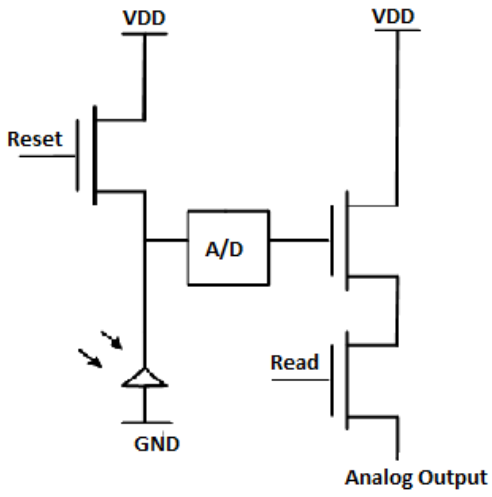

Figure 1.5.a pixel structure of DPS

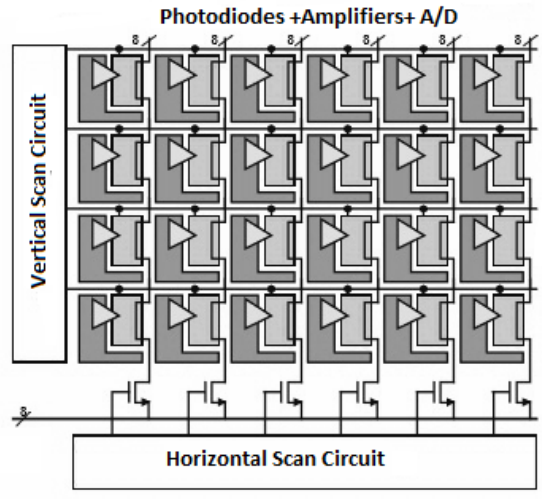

Figure 1.5.b structure of CMOS DPS [8]

1.3 Image Sensor Characteristics

Various parameters establish the advantages, disadvantages and performances of image sensors. Main characteristics of image sensors are defined in this chapter.

1.3.1 Fill Factor

Fill factor (FF) defines as the ratio of the light sensitive area of pixel to the pixel total area.

$$FF = (A_{act} / A_{pix}) \times 100\% \quad (1.1)$$

where :

A_{act} is the photodiode active area (light sensitive area)

A_{pix} is the total area of the pixel

In order to increase the fill factor of image sensor, the circuitry in a pixel should take up as little space as possible and the photosensitive area should take maximum space as possible. Higher fill factor increases the dynamic range and the sensitivity of the pixel.

By placing an array of microlenses on top of the sensor, the fill factor is improved. Furthermore, microlenses have a limited minimum size and can only be used in the visible part of the electromagnetic spectrum. The more effective way to increase the fill factor is by backside illuminating the sensor which improves the capture of incoming photons by 60% to over 90% [12, 13].

1.3.2 Quantum Efficiency

The most important factor to define image sensor performance is Quantum efficiency (QE). QE is the ratio of the number of collected electron-hole pairs (EHP) to the number of incident photons. This parameter describes its response to different wavelengths of light. QE is the ratio of detected signal charge per pixel to the number of incident photons:

$$QE(\lambda) = N_{det}(\lambda) / N_{inc}(\lambda) \quad (1.2)$$

where:

$N_{det}(\lambda)$ is detected signal charge per pixel of wavelength λ

$N_{inc}(\lambda)$ is number of incident photons of wavelength λ

QE depends on the design, particularly on the pixel geometry and on the fill factor.

1.3.3 Dynamic Range

One of the major limitations on image sensor's performance is dynamic range (DR) which is the ability of recording both bright and dark extremes. It's defined as the ratio of the maximum non-saturating voltage signal (the light level just below the system saturation) to the smallest detectable input signal (the light level just above the dark noise) over the desired image capture-time period.

Dynamic range expresses as:

$$DR = 20\ log\frac{V_{max}}{V_{min}} \tag{1.3}$$

where:

V_{max} is the maximum non-saturating signal

V_{min} is the minimum detectable signal

Increasing dynamic range by increasing the saturation level needs larger full well capacity. Increasing the full well capacity is rather difficult because of the restriction in the pixel size and reset voltage swing. Therefore, the most straightforward approach to increase the dynamic range is to decrease the dark noise level. There are also ways to control the saturation level by multi exposure or logarithmic pixel response [12, 14, 15].

The dynamic range of the human eye is around 90dB, high-end CCDs have a dynamic range of more than78dB and CMOS sensors have dynamic range of about 54dB [15]. In general, a CCD sensor has a better dynamic range than CMOS image sensor because CMOS imagers suffer from the high read-noise and non-uniformity.

1-4 Dark Current

1-4-1 Dark Current in Image Sensors

In low light conditions, dark current becomes a major part of the noise in image sensors. The total dark current in the pixel of image sensor depends on pixel type, pixel size and fabrication process. It also depends on the design and technology factors such as, silicon defect density, temperature and electric field of photo-sensing element.

Generation rate of dark current in image sensors mainly depends on silicon surface and bulk defect density where they result from impurities in depleted bulk silicon or surface SiO-SiO_2 interface. These imperfections introduce a path which allows valance electrons to sneak to the conduction band adding to the signal measured in the pixel. These energy states which are located in forbidden gap are called dangling bonds. The density of these surface states is determined by the quality of the fabrication process. The dark current generation due to surface impurities is more than the one generated by bulk defects. An efficient way to reduce the current density is to use low-temperature hydrogen annealing as proposed in [9, 14].

1-4-2 Dark Current in P-N Junction Photodiode

The major part of dark current in image sensors is coming primarily from the photodiode current in the absence of illumination.

A photodiode can operate in two modes: photoconductive mode (reverse biased) or photovoltaic mode (zero biased). Dark current and the current due to the shunt resistance are two major currents in the photodiode. In photovoltaic mode, the dominant current which is diffusion current determines the shunt resistance. The shunt resistance may approximately double for every 6 ºC decrease in temperature which is the slope of current voltage curve of photo diode when V=0. An ideal photodiode has a shunt resistor of infinite while actual values are about 10 to 1000 MΩ. In photoconductive mode, the drift current becomes the dominant current which is known as dark current and approximately doubles for every 10 ºC increase in temperature [7, 11].

Applying a higher reverse bias will decrease the junction capacitance and increase the amount of dark current. Also dark current is affected by the photodiode material and the size of the active

area. Therefore, the dark current depends on the device physics, the silicon process and it is a strong function of temperature.

Total photodiode current which is composed of photo current and dark current:

$$I_{total} = I_{dark} + I_{Due\ to\ Light} \tag{1.4}$$

$$I_{total} = I_o\left(e^{V_D/V_T} - 1\right) + I_{Due\ to\ Light} \tag{1.5}$$

where I_{dark} is the photodiode current in the absence of illumination, $I_{Due\ to\ Light}$ is the photo-generated current, V_D is the bias voltage of the photodiode, V_T is the thermal voltage and I_o is the reverse saturation current. With large values of revered bias voltage, the dark current becomes reverse saturation current (I_o).

$I_{Due\ to\ light}$ includes every electron-hole pair (EHP) created within the depletion region (W) and within a diffusion length away from the depletion region which are swept by the electric field [16]:

$$I_{Due\ to\ light} = (-qA)\,(L_N + L_P + W)\,G_L \tag{1.6}$$

Therefore:

$$I_{total} = I_o\left(e^{V_D/V_T} - 1\right) + (-qA)\,(L_N + L_P + W)\,G_L \tag{1.7}$$

where q is the electrical charge, G_L, the generation rate per volume and time (EHP/cm-3-s) and, A, the cross sectional area of the device. L_P and L_N are the lengths of the n and p-type materials respectively within a diffusion length from the depletion region given by:

$$L_{N,P} = \sqrt{2\,D_{N,P}\tau_{N,P}} \tag{1.8}$$

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_b}} \tag{1.9}$$

where $D_{n,p}$ is the diffusion constant, $\tau_{n,p}$ is the life time of the minority-carriers, ε_s is the permittivity of the silicon, ε_s is the dielectric constant, V_{bi} is the built in potential (bias voltage) and N_b is the doping density (p or n depending on the dopant).

The photodiode current is in opposite direction of the diffusion current. Therefore, as shown in Figure 1.6, illuminating the photodiode with optical radiation shifts the I-V curve to negative values by the amount of the photocurrent ($I_{Due\ to\ light}$).

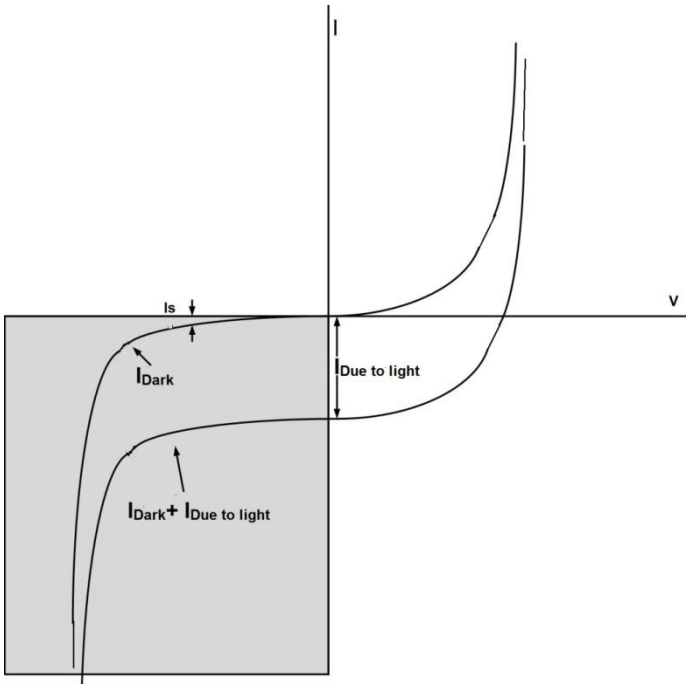

Figure 1.6. I-V Characteristic curves of a Photodiode under reverse bias – gray region (the upper curve is taken in the dark and the other curve is taken under illumination)

Figure 1.7. shows dark current generation mechanism in simple PN junction:

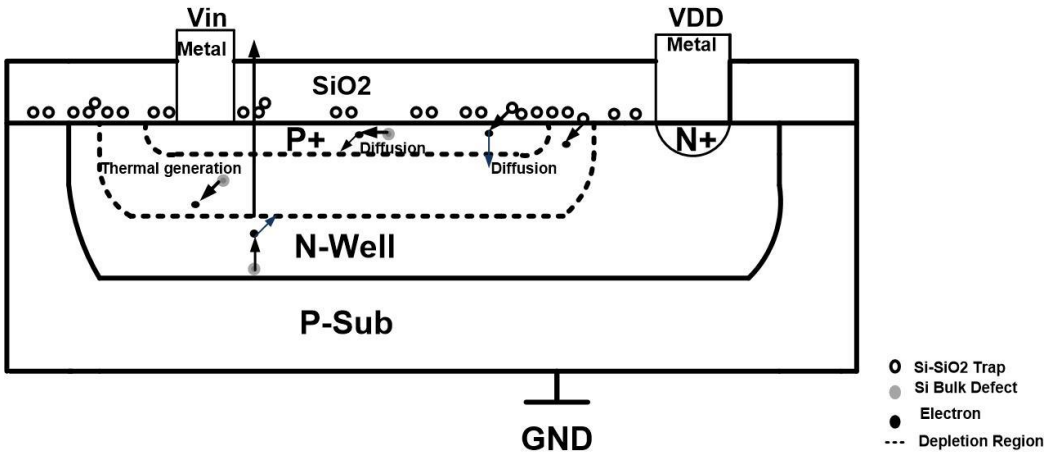

Figure1.7.Dark current generation mechanism in simple P+/N-well photodiode [13]

Since the N-well is connected to V_{DD} and P+ is considered as V_{in} node in Figure 1.7. , the P+/NW junction is the only active junction. More specifically, only carriers generated by P+/NW diode will be collected as useful information, while the other carriers gathered by the NW/P-sub diode would be swept to the power supplies.

1-4-3 Dark Current Reduction in CMOS Image Sensor

Since the dark current has bad effect on CMOS image sensors performances in the terms of sensitivity and dynamic range, many efforts have been done in order to reduce its effect. Considerable efforts have been made for reducing the dark current by physical modification of the photodetector, such as adding a photogate to the photodiode, adding an n+ reset ring structure [17], surrounding the pixel by a p-well [18] and burying the source follower transistor [19].

Shrinking the feature size technology increases the resolution of image sensors by decreasing the pixels size. Meanwhile, it brings new challenges where using shallow trench isolation (STI) beyond the 0.18um technology significantly and increases the dark current. In deep submicron technologies, STI is used to isolate pixels and components in the pixel from each other. The STI boundaries may have higher defect densities than the substrate, creating a higher density of energy states in forbidden gap between the STI boundaries and the silicon along the Si-SiO_2

interface. In order to reduce the dark current due to STI effect, it is possible to increase the distance between photodiode and STI at the expense of losing the fill factor of pixel. The APS 4T structure which includes pinned photodiode has less dark current than pixel with a p-n junction photodiode. In PPD structure, the heavily doped p+ pinning layer significantly reduces the dark current by completely shielding the depletion region of photodiode from touching the bar Si-SiO_2 interface.

The most effective way to reduce the dark current is to decrease the depletion width of the photodiode, but small depletion width leads to lower QE. PPD has high QE while having less significant dark current than p-n junction photodiode. However, the pinned photodiode (PPD) based 4-T pixel has some disadvantages, such as a low dynamic range associated with the small well capacity and requires modification of the typical CMOS fabrication process whit additional cost.

Dark current random noise of sensor is mainly reduced by replacing the standard surface mode transistor n-MOS amplifier in the pixel with buried channel source follower. Therefore, the sensor dark current noise in terms of 1/f noise will be reduced by burying the source follower transistor [14].

Reset noise is a dark current random noise which is coming from reset transistor and is modeled as a resistor with thermal noise in ON mode of the reset switch. This thermal noise is sampled and held in the photodiode capacitor after the transistor is OFF. In order to reduce the reset noise voltage, photodiode capacitance (C_{PD}) should be as large as possible. Since the image performance is reduced by increasing the C_{PD} value, mostly the image sensors suffer from the reset noise. Recent researches prove that by using the so called soft reset technique, reset noise of 3T pixel could be reduced [20]. In 4T-PPD pixel, the reset noise also could be reduced by using a correlated double sampling CDS structure [14].

1-5 Noise Associate with Dark Current in CMOS Image Sensors

Dark current generates two types of noise: dark current non-uniformity from pixel to pixel, Fixed Pattern Noise (FPN), and temporal noises (reset noise, flicker noise (1/f) and dark shot noise).

1-5-1 Fixed Pattern Noise (FPN)

Two main sources of FPN are: dark current inside the pixel and mismatches due to in-pixel or column level transistors. Pixel-level FPN which is due to transistor parameters mismatches can be eliminated by Correlated Double sampling (CDS) circuits while the mismatch due to column transistors are eliminated in the digital domain during the image processing procedures [14].

1-5-2 Dark Current Shot Noise

Part of electron-hole generation of photo-sensing elements in the absence of illumination which depends on temperature is called dark current shot noise. Dark current shot noise is the dominant source of noise in low light illumination.

$$V_{Shot} = \frac{\sqrt{qI_{dark}\, t_{int}}}{C_{PD}} \tag{1.10}$$

where I_{dark} is the average of dark current. The term t_{int} is the integration time. C_{PD} is photodiode capacitance.

The dark current shot noise can be reduced by lowering the temperature, careful pixel layout, a proper transistor size and bias setting [10].

1-5-3 Reset Noise

This noise originates from thermal noise of the reset switch which is often implemented by an NMOS transistor and known as KTC, expressed by

$$V_{RST} = \sqrt{\frac{KT}{C_{PD}}} \tag{1.11}$$

Where K is Boltzmann's constant (k =1.38E-1023 J/K) and T is the temperature in Kelvin and C_{PD} is photodiode capacitance.

1-5-4 1/f Noise

1/f noise is due to lattice defects at the interface of the Si-SiO_2 channel of MOS transistor which is mainly due to the source follower in CMOS image sensors pixel. This noise depends on the gate oxide capacitance, the width and the length of the transistor. Ways to reduce 1/f noise include increasing the size of transistor, reducing the power supply or burying the source follower transistor.

1-6 Leakage in MOSFET

In CMOS image sensor structure different MOS switches are used for different purposes which are described in this chapter. Leakage from switches can add large distortion effect in readout signal. First, different sources of leakage in MOSFET structure are reviewed then, switches and their leakages are presented.

Over the past decades, MOSFET size has been scaled down continuously. Channel length of MOSFETs have been reduced from several micrometers to tens of nanometers in modern integrated circuits. Small size MOSFETs, below few tens of nanometers bring some problems. They need very low supply voltages and have poorer electrical properties like higher leakage currents, and lower output resistance.

Non-ideal behavior of CMOS switches due to leakage current in OFF operation mode is described in this chapter. The main sources of MOSFET leakage currents in deep submicron (DSM) process circuits are: Sub-threshold conduction current (I_{SUB}), gate direct tunneling current (I_G), gate-induced drain leakage current (I_{GIDL}) and reverse-biased junction leakage current (I_{REV}) as shown in Fig. 1.8. Amongst all the leakage current components, sub-threshold leakage is the most dominant component [21, 22]. Various techniques have been developed for reducing the sub-threshold leakages in MOSFET transistors.

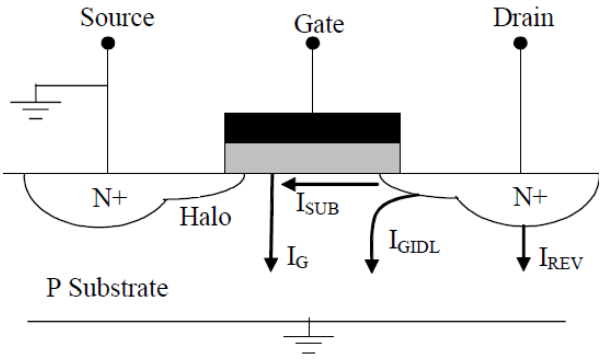

Figure 1.8. Leakage current components in an NMOS transistor [22]

1-6-1 Reverse-biased junction leakage current (IREV)

The leakage through the source or drain to substrate of the reverse-biased diodes when a transistor operates in OFF mode is called reversed-bias junction leakage. The magnitude of junction leakage depends on the area of the drain or the source diffusion and the density of leakage current is determined by the process technology [23].

1-6-2 Gate-Induced Drain Leakage (GIDL)

Gate-induced drain leakage (GIDL) is caused by band to band-tunneling in the drain region underneath the gate which is very sensitive to the gate oxide thickness, the drain concentration, the lateral doping gradient, and the applied drain-to-gate voltage [22]. When the gate is at zero or negative voltage and the drain is at the supply voltage level, there can be a dramatic increase of avalanche multiplication and band-to-band tunneling. Minority carriers underneath the gate are swept to the substrate, creating GIDL current. GIDL is defined as:

$$I_{GIDL} = AE_s \times e^{-B/E_s} \tag{1-12}$$

$$A = \frac{q^2 {m_r}^{1/2}}{18.л.h^2 {E_{gap}}^{3/2}} \tag{1-13}$$

$$B = \frac{л\, {E_{gap}}^{3/2}\, {m_r}^{1/2}}{2\sqrt{2}.q.h} \tag{1-14}$$

E_{gap} is the direct energy gap of silicon (~1.12 eV), h is 1/2 π times the Planck's constant, m_r = 0.2 m0 (a silicon effective mass), E_s is the vertical electric field at the silicon surface, and q is the electronic charge which is equal to 1.6 E-19 C. Thinner oxide T_{ox} and higher supply voltage V_{dd} increase GIDL. GIDL is also referred to as surface band-to-band tunneling leakage [23, 24].

1-6-3 Gate Direct Tunneling (I_G)

The gate direct tunneling leakage flows from the gate through the "leaky" oxide insulation to the substrate. The magnitude of I_G decreases exponentially with the gate oxide thickness and the supply voltage. The high-K gate dielectric reduces direct tunneling current and is required to control this component of the leakage current for low standby power devices [25].

1-6-4 Sub-threshold Leakage (I_{SUB})

Sub-threshold leakage is the current from source to drain when the MOSFET is in OFF mode and this current is due to diffusion of minority carriers in the MOSFET channel when the $V_{gs}$is less than the threshold voltage [21]. I_{SUB} is calculated using the following formula:

$$I_{SUB} = \mu_0 C_{ox}\left(\frac{W}{L}\right)(V_T)^2\, e^{1.8}\, e^{\frac{V_{gs}-V_{th_0}-\eta V_{ds}-\gamma V_{sb}}{nV_T}}\left(1- e^{-|V_{ds}|/V_T}\right) \quad (1.15)$$

where W and L are the width and length of transistor, C_{ox} *i*s the gate oxide capacitance, μ is the carrier mobility, γ is the linearized body effect coefficient, η is the is the drain-induced barrier lowering (DIBL) coefficient, V_T is the thermal voltage and n is the sub-threshold swing coefficient.

The magnitude of the sub-threshold current is a function of the temperature, supply voltage, device size, and the process parameters, such as threshold voltage (V_{th}) which plays the dominant role.

By shrinking the size of the technology V_{th} of the transistor is decreased [26]. The threshold voltage depends on four parameters: V_{SB}, doping, process and temperature.

$$V_{TN} = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\varphi_F|} - \sqrt{|2\varphi_F|}\right) \quad (1.16)$$

where V_{T0} is the threshold voltage for zero substrate bias, $2\varphi_F$, the surface potential, $V_{SB,}$ the source to body substrate bias.

In addition to parameters optimization, changes in circuit configuration were presented for reducing the sub-threshold leakage current, such as stack effect, dual and multi-threshold voltage techniques [27, 28].

From the above discussion, we see that I_{SUB}, I_{REV} and I_{GIDL} increase with V_{DB}. Since the transistor gate must be at a high potential with respect to the source and substrate for this current to flow, the I_G is not a component of the OFF current. Among the three components of I_{OFF}, I_{SUB} is clearly the dominant component [29].

Figure 1.9 shows the leakage current contributions of OFF mode MOSFET in different deep submicron (DSM) technologies and it shows the dominant of sub-threshold leakage in larger technologies [30]

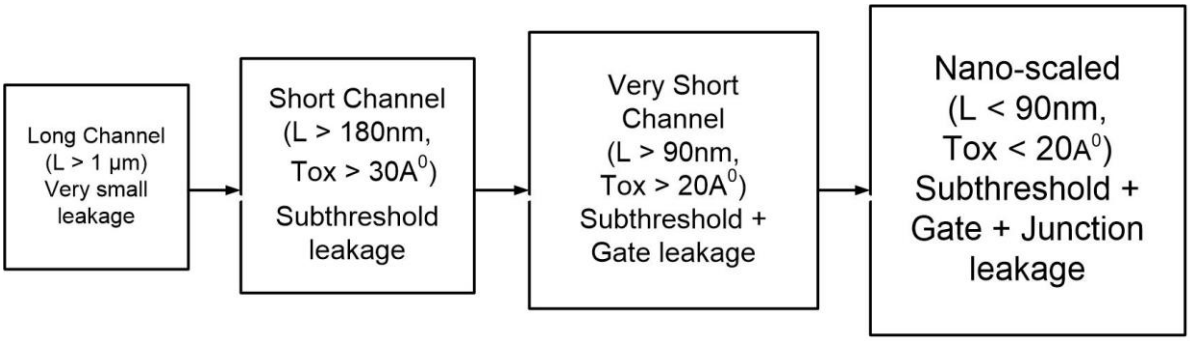

Figure 1.9. Leakage in different bulk technologies [31]

1-7 Summary

This chapter presented a brief overview of CMOS image sensors. The important characteristics of image sensors, especially the dark current, have been described. Different technics of reducing the dark in CMOS image sensor were reviewed. At the end of the chapter leakage current in MOSFET has been explained. In the next chapter, the new CMOS image sensor structure will be proposed for compensating the dark current effect by considering the effect of MOSFET's leakage on operation of the proposed circuit.

CHAPTER 2 DESIGN OF AN IMAGE SENSOR PROTOTYPE

In this chapter the leakage of MOSFET switches is thoroughly described by simulating and analyzing a sample-and-hold circuit. Then, the structure for compensating the effect of dark current in CMOS image sensors is presented. Afterward, optimization techniques for eliminating the leakage current effect of CMOS switches in the proposed design are described. At the end a subtractor circuit is introduced for subtracting the output of a dummy pixel form a pixel being readout to complete the dark current compensation circuit.

2-1 MOS Switches

2-1-1 Sample-and-Hold Circuit

In this section, we compare and analyze the leakage sources in Transmission Gate (TG) switch by simulating a sample-and-hold circuit.

A simple sample-and-hold circuit is composed of a MOS switch and a hold capacitor. This circuit is suffering from some non-idealities behavior which makes the capacitor voltage to discharge during the hold mode due to MOSFET leakages, clock feedthrough and charge injection effects. As it is shown in Figure 2.1, the TG switch is used instead of a single MOS switch in order to reduce the effect of channel charge injection and clock feedthrough.

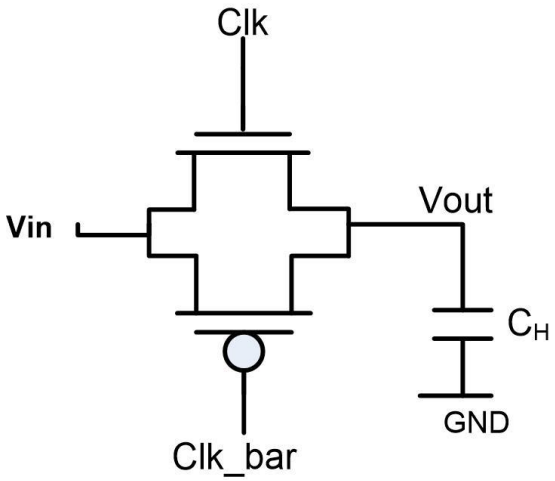

Figure 2.1 Sample-and-Hold circuit

The leakage current of the switch discharges the capacitor to input signal V_{in}, V_{DD} or V_{SS} values during the hold mode of S/H operation. This distortion could be reduced by increasing the capacitor value or decreasing the sampling time of the switch.

Figure 2.2 shows the distortion in the voltage of hold capacitor which is discharged during the hold mode due to different sources (V_{in} , V_{DD} or V_{SS}). Figure 2.2.b and c show the S/H output which has junction leakages respectively through V_{DD} and V_{SS} and Figure 2.2.d shows the S/H output which has the sub-threshold leakage and discharges the capacitor to V_{in} value during the hold mode.

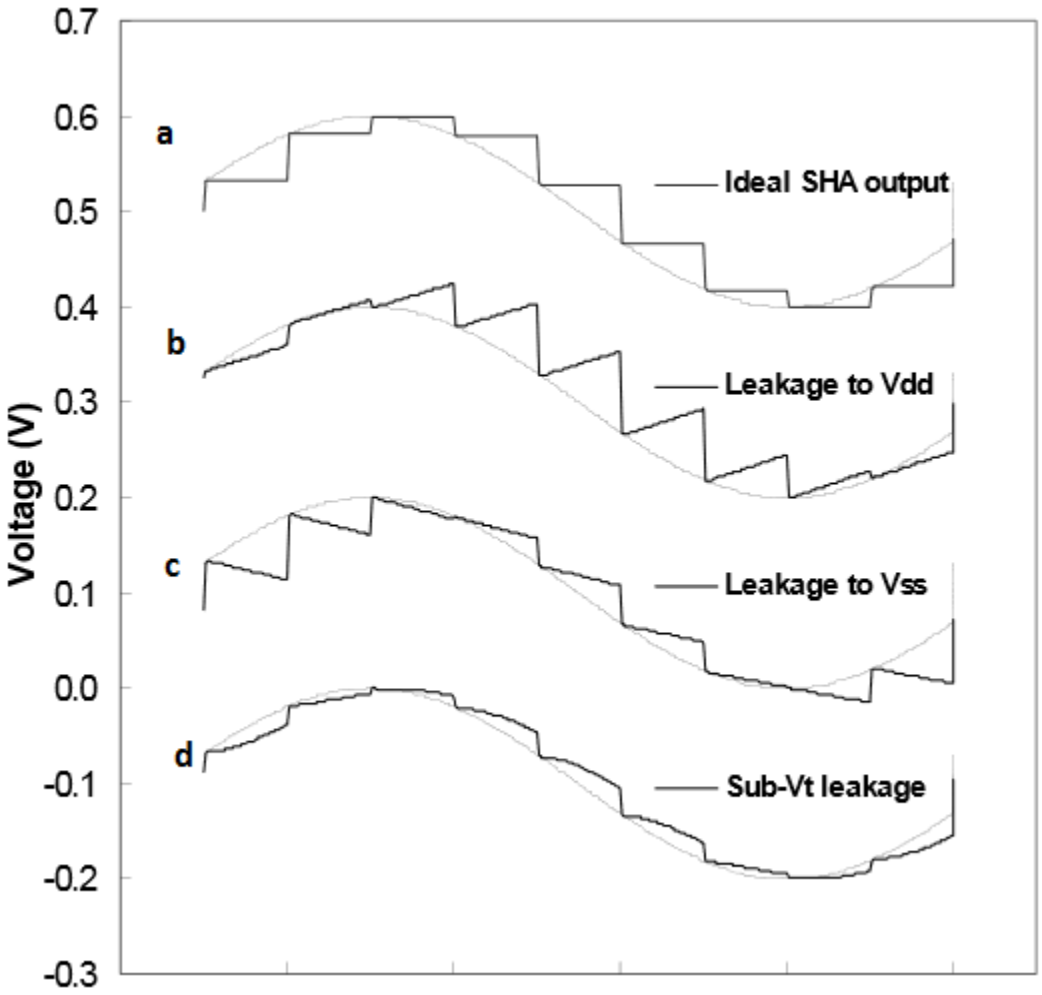

Figure 2.2. Sample-and-Hold output with various leakages [32]

As mentioned before, the dominant leakage of a switch is the sub-threshold current which discharges the capacitor to the input signal value [32]. We are going to show this fact by simulating the circuit of Figure 2.3. This circuit is simulated with an input sine wave (Amp= 0-1 V, f=1 Hz) and hold capacitors in the atto, femto, pico and nano Farad ranges.

Figure 2.4,5,6,7 show the distortion in the output of a sample-and-hold circuit due to the sub-threshold leakage current. By comparing the graphs in the Figures 2.4,5 and 2.6,7, we see that for femto and atto values of the hold capacitor the sub-threshold leakages current is significant but for larger values of the hold capacitor (pico and nano Farad) the sub-threshold leakage is negligible.

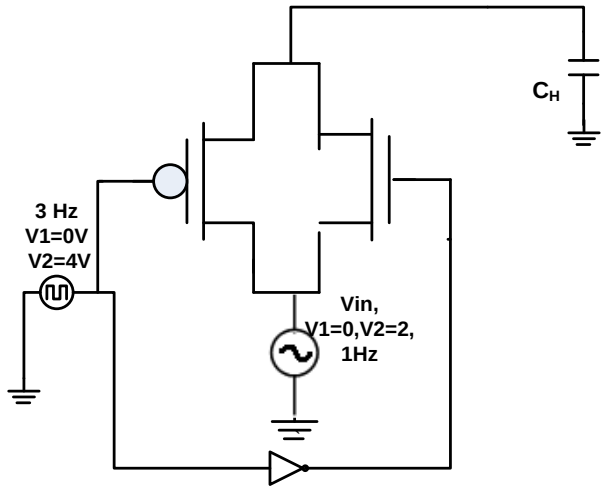

Figure 2.3. Simple-and-Hold circuit

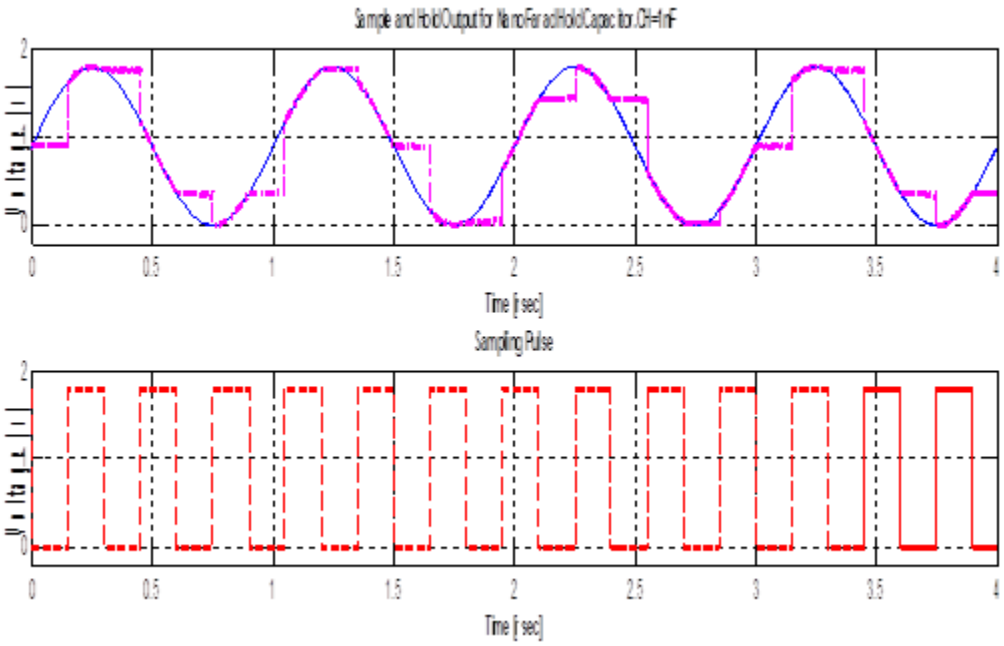

Figure 2.4. Sample-and-Hold output for Nano Farad hold capacitor.C_H=1nF

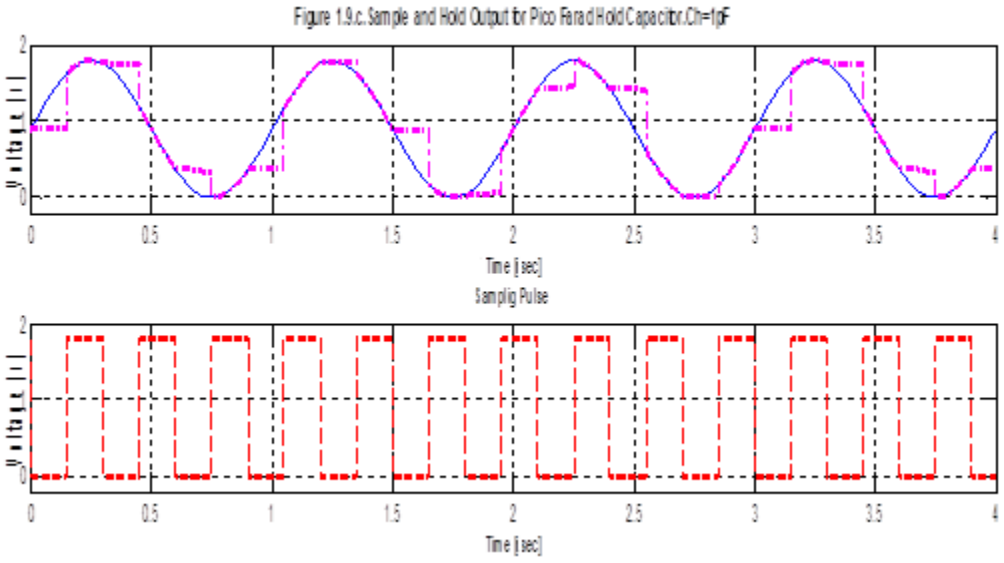

Figure 2.5. Sample-and-Hold output for Pico Farad hold capacitor.C_H=1pF

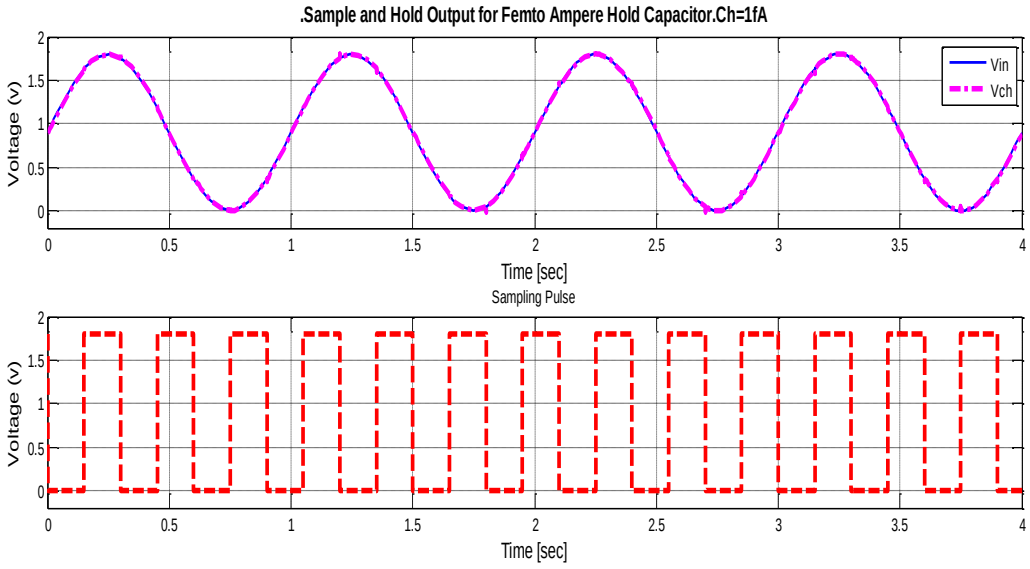

Figure 2.6. Sample-and-Hold circuit for Femto Farad hold capacitor,C_H=1fF

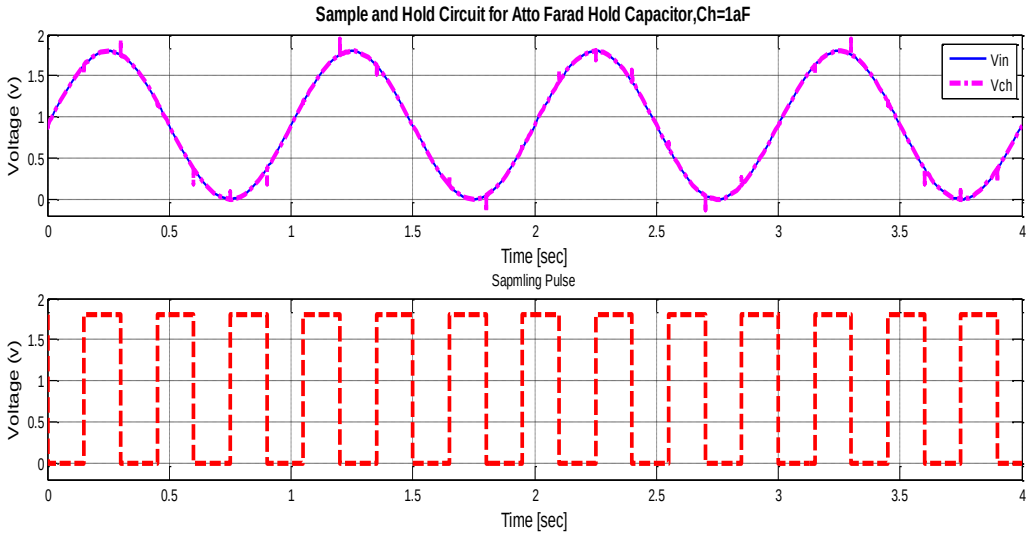

Figure 2.7. Sample-and-Hold circuit for Atto Farad hold capacitor, C_H=1aF

The clock feedthrough of S/H circuit which is shown in Figure 2.8 has been calculated according to equation (2.1). The equation shows that the value of the clock feedthrough depends on the clock amplitude and the hold capacitor values [33]. Clock feedthrough error appears as glitches at the edge of clock pulses.

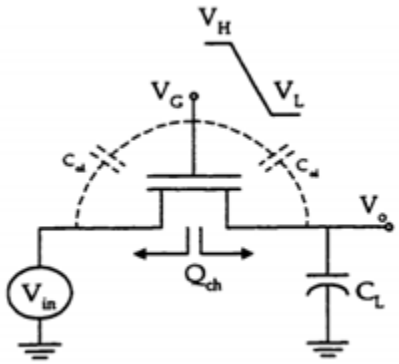

Figure 2.8. Calculating feedthrough effect in simple Sample-and-Hold circuit (MOS Switch)

$$\Delta V_0 = \frac{C_{ol}}{C_{ol}+C_L}(V_H - V_L) \qquad (2.1)$$

By comparing Figures 2.4,5,6. and 7, we find the small clock feedthrough effect by using a TG switch. The output graphs show significant clock feedthrough effect on circuits with smaller hold capacitors. For example Figure 2.7. shows clock feedthrough errors due to using atto farad range while Figure 2.4 and 2.5 show negligible effect of clock feedthrough error for nano and pico farad range of hold capacitor.

To analyze the operation of a S/H circuit, the switch is modeled as a high resistor in OFF mode and a low resistor in ON mode. It means that the sample-and-hold circuit could be modeled by a simple RC circuit as it is shown in Figure 2.9.

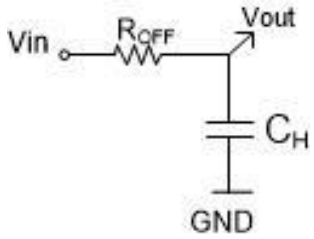

Figure 2.9. Simple RC circuit which models the S/H circuit

The values of R_{ON} and R_{OFF} of a simple TG switch is deduced by simulating the configurations below.

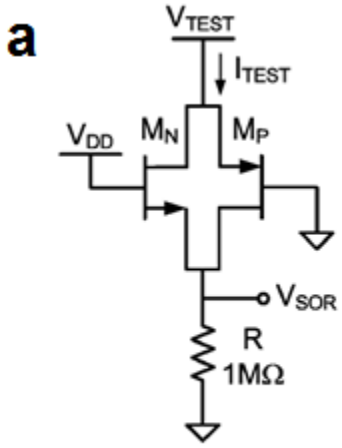

Figure 2.10.a. Configuration for calculating R_{ON}

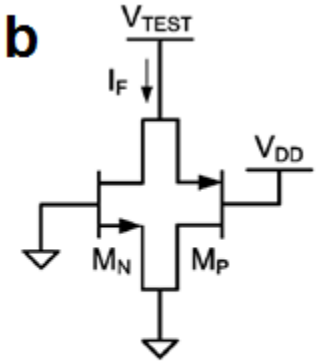

Figure 2.10.b. Configuration for calculating R_{OFF}

The R_{OFF} of the TG switch is extracted from Figure 2.11. By sweeping the VTEST voltage source and measuring the current I_F, the value of about 0. 2TΩ is obtained for R_{OFF}.

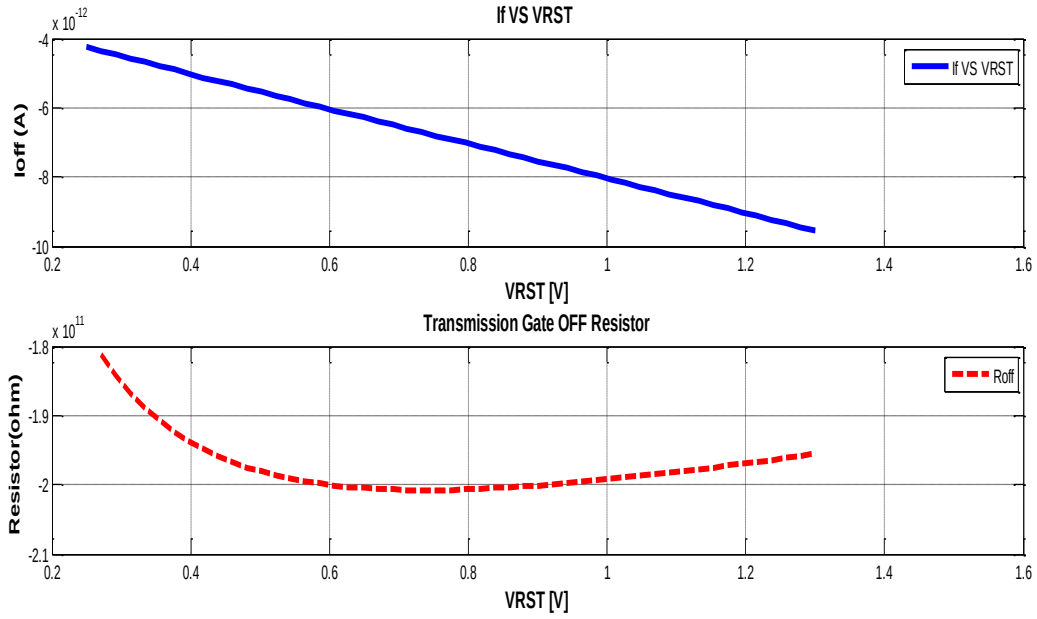

Figure 2.11. OFF resistor of TG

As shown in Figure 2.6 and 2.7, in OFF mode the output of the switch tries to follow the input signal value. Since the $R_{OFF}$with the value of TΩ range makes the capacitor to charge with time constant which equals to $R_{OFF}C_H$ (<1ms) and 1000 times less than hold time (1sec). Thus, the capacitor voltage is discharged by the input source (*Vin*) due to sub-threshold leakage of the switch during the hold time .For nano Farad values of the capacitor, the constant time is τ =RC>100s which is quite larger than the hold time. So there is no distortion in the output voltage during the hold time as it is shown in Figure 2.4. Figure 2.5. shows a little effect of sub-threshold leakage which affects the hold voltage mode of pico farad capacitor while it doesn't have effect on nano Farad capacitors. Figure 2.12 shows this effect by scaling Figures 2.4 and 2.5. Red circles in Figure 2.12 shows the effect of sub-threshold voltage on pico and nano Farad hold capacitors.

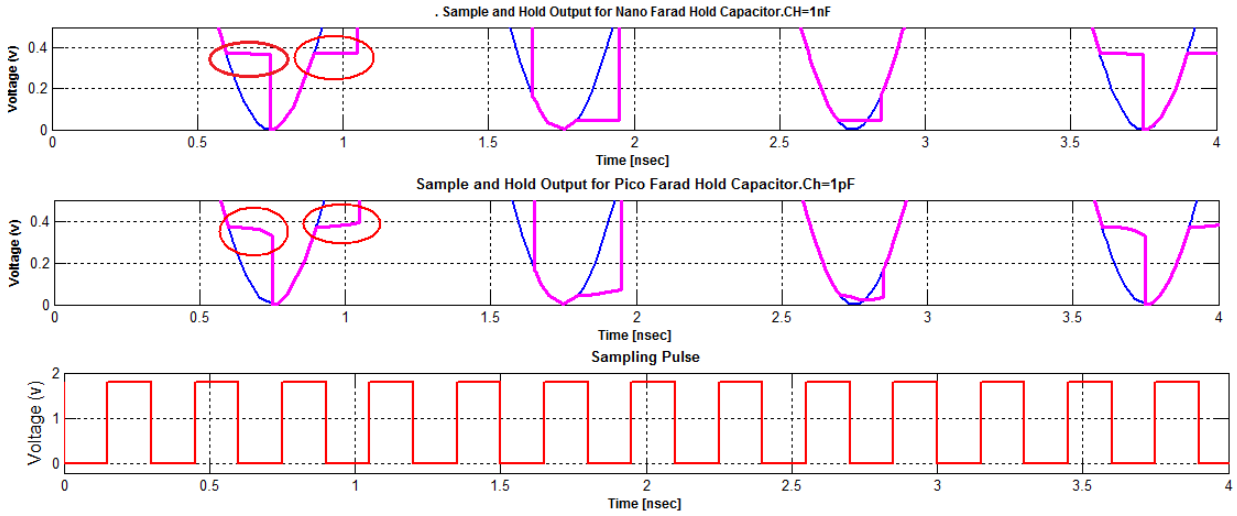

Figure 2.12 Comparison of the sub-threshold leakage effect of single MOS switch on Nano and Pico Farad hold capacitors

The charge injection effect in the output could be reduced by decreasing the fall time and rise time of the clock pulse feeding MOSFETs' gates.

2-2 Proposed Circuit Reducing the Effect of Dark Current in CMOS Image Sensor

In this section a circuit for compensating the effect of dark current in CMOS image sensor is proposed. Since differential architecture could not efficiently compensate the non-uniformity noise effects, a feedback configuration which fixes the integrating node of photodiodes and makes uniformity dark current noise is implemented. Pixel architecture is presented and optimized for low level sensing illuminations and number of pixels is expanded for a row of pixel array.

2-2-1 Capacitive Transimpedance Amplfier (CTIA)

A simple integrator circuit is shown in Figure 2.15. which is known as a Capacitive Transimpedance Amplfier (CTIA) [6, 34].

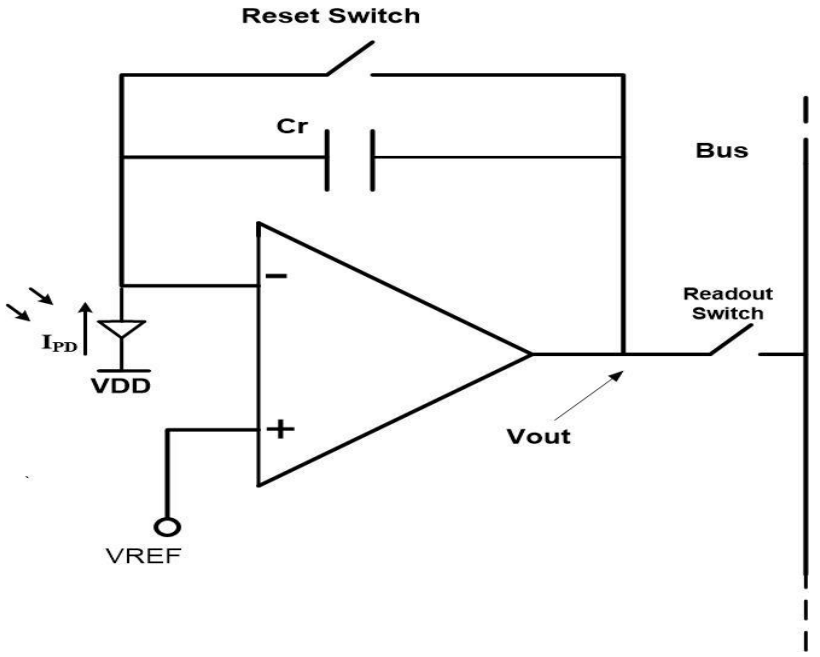

Figure 2.13. Capacitive Transimpedance Amplfier (CTIA)

The circuit is used to convert the photodiode current to voltage. The integrator circuit consists of an amplifier, an integrating capacitor (C_r) located in the negative feedback loop and a reset switch transistor in parallel to the capacitor. Also a readout switch is shown in the figure which is connected to the bus line of the pixel array column.

As mentioned in chapter one, a photodetector produces a current proportional to the amount of incident light which is modeled by a DC current source (I_{PD}). The traditional P+/N-well photodiode is used. Also N-well/P-sub photodiodes could be used by switching to complementary configuration. The typical circuit model of a photodiode is shown in Figure 2.16.

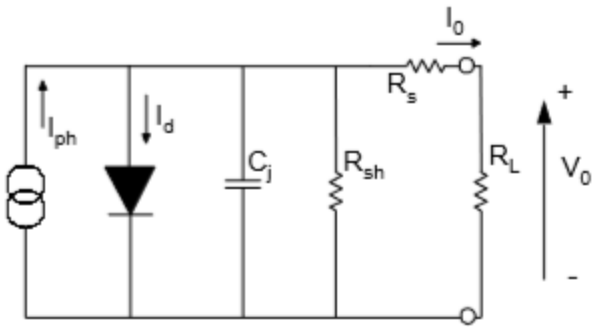

Figure 2.14. The PN junction: A junction capacitance (Cj) and a shunt resistance (R_{Sh}) are in parallel with the other components. Series resistance (R_S) is connected in series with all components in this model

CTIA circuit is operating in "reset" and "integrating" modes. By closing the reset switch, the integrating capacitor is discharged and the op-amp acts as a buffer amplifier. As a result, the output will be equal to V_{REF}value; the non-inverting and inverting input of the op-amp:

$$V_{REF} = V^+ = V^- \tag{2.2}$$

The integration phase starts after opening the reset switch. Constant current from the photodiode (I_{PD}) integrates across C_r. Due to feedback and the large amplifier gain, the integration node (inverting input) and the non-inverting input of the op-amp will remain equal to V_{REF}. Equation (2.3) determines the total charge of the capacitor during the integration mode. t_{int} is the elapsed time from the start of the integration phase.

$$Q = I_{PD} \Delta t = C_r \, (V_{REF} - V_{Out}(t_{int})) \tag{2.3}$$

Therefore the output voltage of the op-amp during the integration time can be given as

$$V_{Out}(t_{int}) = V_{REF} - \frac{I_{PD} \times t_{int}}{C_r} \tag{2.4}$$

So, the output voltage in the integrating time has a negative slope which depends on the intensity of the photodiode current.

The output of the integrator circuit is shown in Figure 2.17.

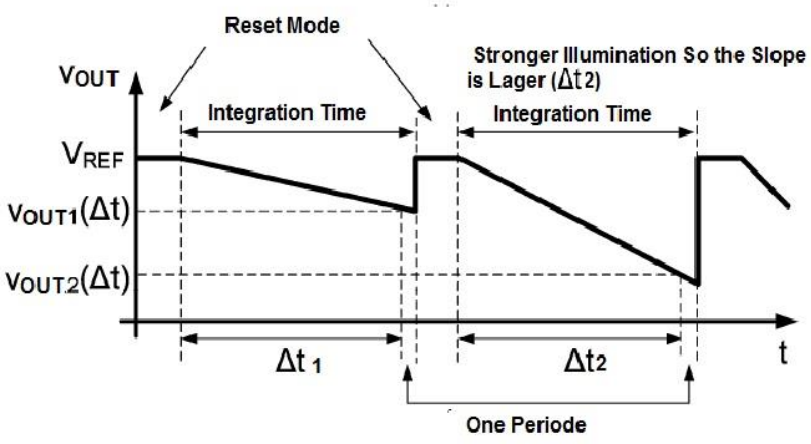

Figure 2.15 Integrator circuit output [35]

A circuit using two integrators and two photodiodes is shown in Fig. 2.18. One of the photodiodes is sensitive to the light and generates photo-current and dark-current. The other photodiode is shielded from the light and has only dark current at its output. The circuit is operating in "reset" and "integrating" modes as simple integrator circuit. The output voltage of each op-amp is equal to the simple integrator circuit described before:

$$V_{Out1}(t_{int}) = V_{REF} - \frac{(I_{Dark})}{C_r} t_{int} \quad (2.5)$$

$$V_{Out2}(t_{int}) = V_{REF} - \frac{(I_{Dark} + I_{photo})}{C_r} t_{int} \quad (2.6)$$

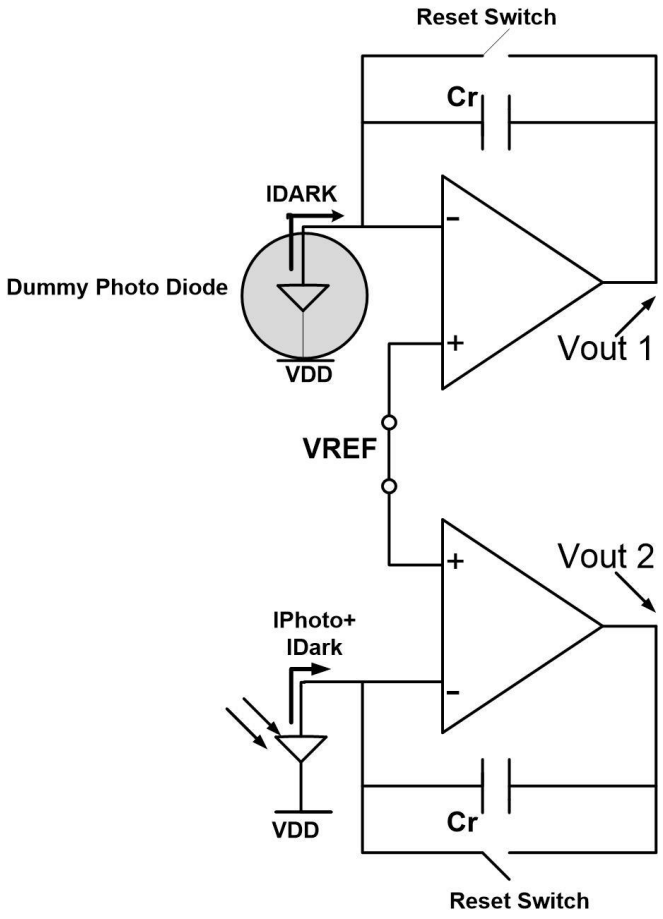

Figure 2.16. CTIA interface [36]

In order to decrease the number of transistors in each pixel so that the fill factor is increased, the structure of the two amplifiers in Figure 2.18. can be modified into the more compact amplifier presented in Figure 2.19.

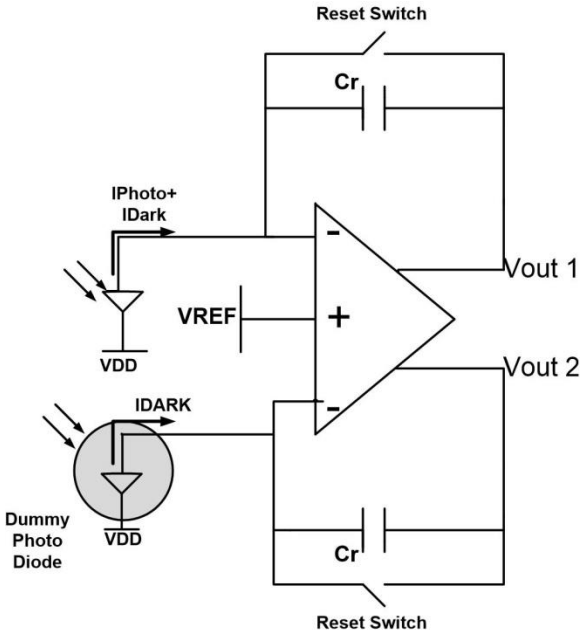

Figure 2.17. Double-Input Double -Output CTIA

The new amplifier has one non-inverting and two inverting inputs as well as two outputs. In Figure 2.19, V_{out2} depends on the photo and dark current of the photodiode ($I_{PD}=I_{Dark}+I_{Photo}$) while V_{out1} depends only on the photodiode dark current ($I_{PD}=I_{Dark}$). By subtracting V_{out1} from V_{out2} in the integrating phase, the output voltage becomes less dependent on the photodiode dark current:

$$V_{Out2}(t_{int}) - V_{Out1}(t_{int}) = \frac{(I_{Dark}+I_{photo}) - (I_{Dark})}{C_r} t_{int} = \frac{I_{photo}}{C_r} t_{int} \qquad (2.7)$$

The number of integrators can be expanded to the number of pixels in a row and leads to a new configuration being a multiple input/output integrator circuit. The symbol of the multi-branch CTIA is shown in Figure 2.20.

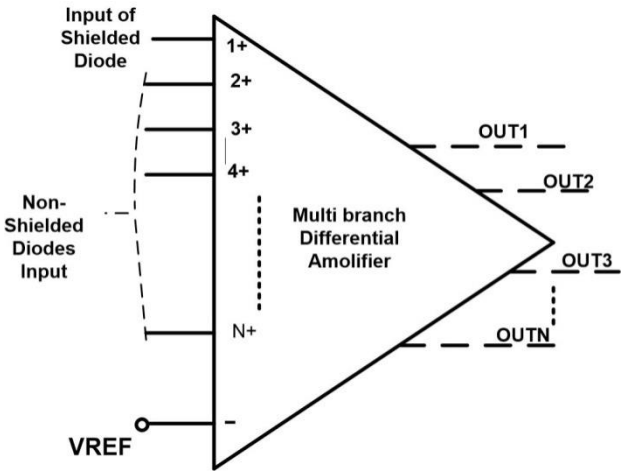

Figure 2.18. Multi-Branch differential amplifier [6]

2-2-2 Leakage Current Reduction of Reset Switch

As explained in the first section of this chapter, leakage current from MOSFET switches could have distortion effect on the output of the circuit especially when the switches are in OFF mode. The effect of this leakage is seen during the charge of the hold capacitor in the sample-and-hold circuit. In the proposed circuit, off transistor leakage of MOSFET has an effect on the accumulated charge in the capacitor of the integrator circuit.

When using a single MOS or CMOS transmission gate (TG) as the reset switch in the integrator circuit, the small dark current of the photodetector cannot build any voltage across the capacitor. This is because often the leakage current of the OFF reset switch exceeds the dark current value of the photodiode. When the capacitor starts charging during the integration mode, the built up voltage on the capacitor increases the V_{DS} voltage of OFF Switch which creates the leakage current in OFF reset switch during the integration time. This leakage is trying to discharge the capacitor. . The discharge happens in a smaller time constant than the time needed for the capacitor to charge with the dark current of the photodiode.

As mentioned before, the sub-threshold leakage is the dominant leakage current contribution in MOSFETs which is a current flowing from drain to source when the MOSFET is in OFF mode. The leakage current and photodiode dark current directions are shown in Figure 2.21.

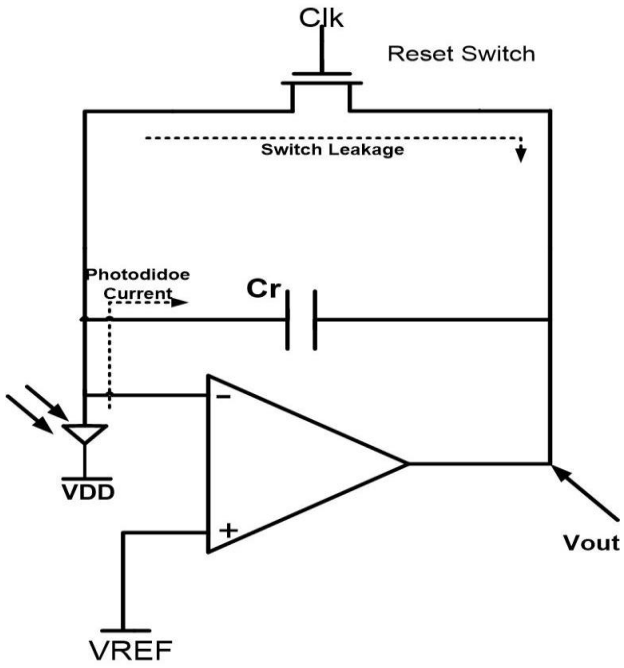

Figure 2.19. Leakage of CTIA circuit with NMOS reset switch

Various techniques have been presented to reduce sub-threshold leakages in MOSFET transistors. In the integrator circuit, a T-type circuit is used as a reset switch for reducing the sub-threshold leakage current of the switch by putting the V_{ds} of the MOS to zero [35]. As shown in Fig. 2.22, in the T-type switch configuration, the single NMOS switch is replaced by two NMOS switches in series and one NMOS switch connected between a V_b voltage source and the node between NM1 and NM3. Voltage V_b is set close to the integrating node voltage, V_{REF} value. During the integration mode where NM1 and NM3 switches are OFF and NM2 is ON, the node between NM1 and NM3 switches is pulled to V_b through the ON resistor of NM2 transistor. Since the drain of NM1 is connected to V_b, drain-source voltage of NM1 is close to zero and the leakage of NM1 approaches zero. Therefore, the leakage current of the T-type switch is greatly reduced.

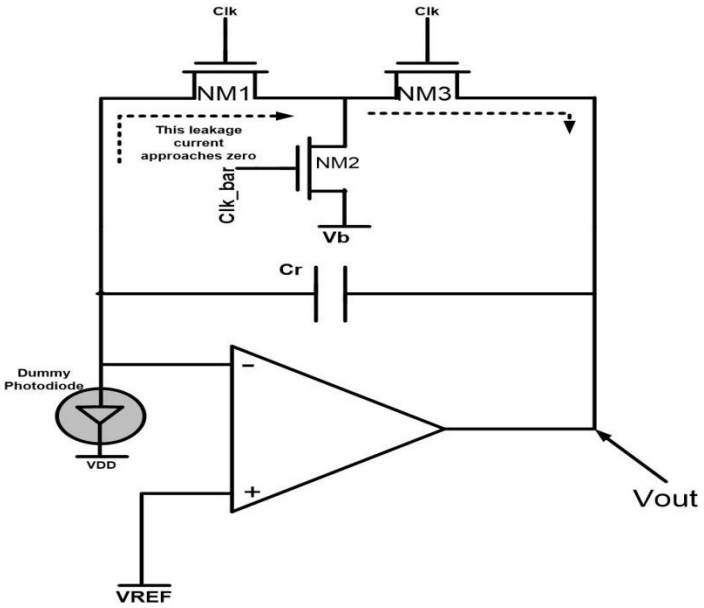

Figure 2.20. CTIA circuit with T-type reset switch

During the circuit reset mode, NM1, NM3 are ON and NM2 is OFF. By using the TG switches instead of NM1 and NM3 in the T-type configuration, the channel feed through effect of the switch could be reduced. Also stacking NM1 and NM3 by putting few transistors in series with NM1 and NM3 leads to a smaller drain source voltage for the transistors. Therefore, according to (1.15), with a smaller V_{ds}, the sub-threshold leakage flowing through the stacked-series transistors will be reduced [37]. Since the design aims at reducing the number of transistors in a pixel, the simple configuration of the T-type switch with three transistors was considered.

The leakage current of the single MOS switch is in the range of pico-amperes while the leakage current of the T-type switch can be below 1 fA [35, 37-39].

2-3 Actual Implementation

The multi-branch differential amplifier for compensating the effect of dark current in CMOS image sensors is presented in [6]. The dummy pixel and the non-shielded pixel of the multi-branch amplifier are shown in Fig. 2.23. In the dummy pixel of the circuit, the capacitor cannot be charged using the small dark current value of the photodetector during the integration time (when the TG switch is OFF) because the time constant responsible for charging the capacitor

through the OFF switch of path 2 is smaller than the time needed to charge the capacitor via the photodiode dark current. Also in the non-shielded pixel of Fig. 2.23, the capacitor is discharged through the OFF resistor of the TG switch (through path 1) while being charged by the photodiode current. In the proposed architecture, the TG switch in the non-shielded pixel is replaced by a T-type switch with a smaller leakage current. The replaced switch doesn't prevent the capacitor from being charged by the photodiode dark current since the switch leakage is less than the photo diode dark current. However, replacing the TG switch by the T-type switch in the dummy pixel cannot solve the switch's leakage problem because in this configuration, the drain-source voltage of the transistors in the T-type switch is not equal to zero during the integrating mode of the circuit. From Fig. 2.22, we found that an effective low-leakage T-type switch can be implemented only when it is placed in the feedback path of the circuit. Therefore, the configuration of the shielded dummy pixel should be modified to a new structure with feedback.

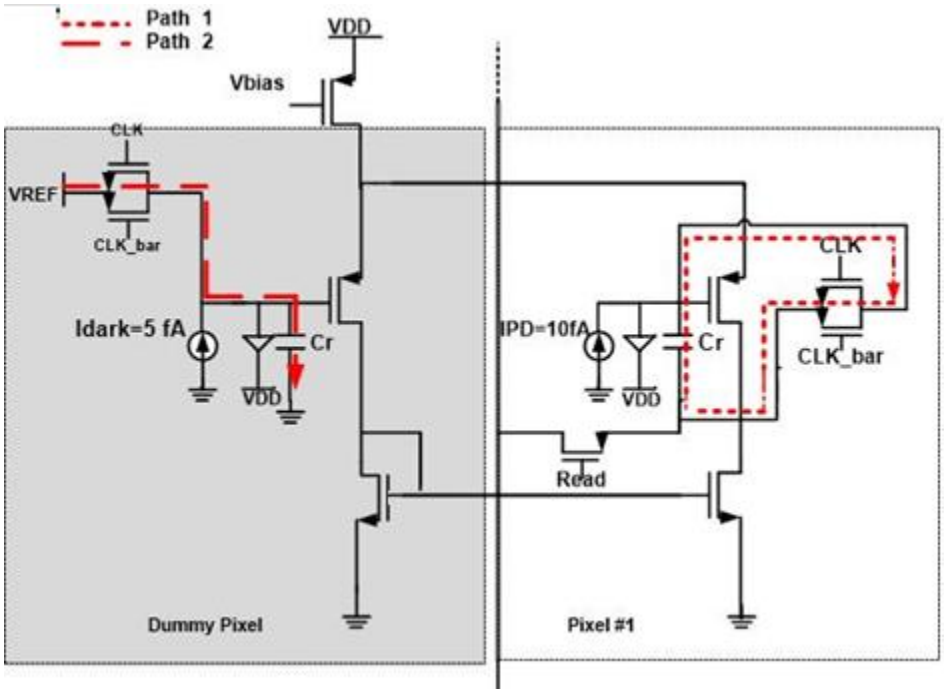

Figure 2.21. Dark current compensation circuit of [6]

Changing the configuration of the circuit in [6] leads to a new structure of multiple-input multiple-output integrator which is shown in Fig. 2.24. In proposed design, one dummy pixel is shared with an entire row of pixels and its dark current is subtracted from the output voltage of each pixel in a row. Therefore, the subtractor circuit gives an output voltage where the

contribution of the photodiode dark current has been greatly reduced. The subtractor circuit is implemented in a column amplifier at the bottom of the pixel array. Implementing a complete differential amplifier in each pixel reduces the fill factor and increases power consumption. The proposed solution is achieved by implementing multiple-input multiple-output differential amplifier; the amplifiers would have one non-inverting and a several inverting inputs as shown Fig. 2.24. The number of inverting inputs is equal to the number of pixels in a row plus a dummy pixel. Unlike the previous configuration, the new setting provides constant voltages across the reset T-type switch.

Since the photodiode has fixed depletion region width due to the feedback configuration, photodiode capacitance (C_{PD}) has a constant value. Each photodiode is modeled with a current source in parallel with a constant photodiode capacitor.

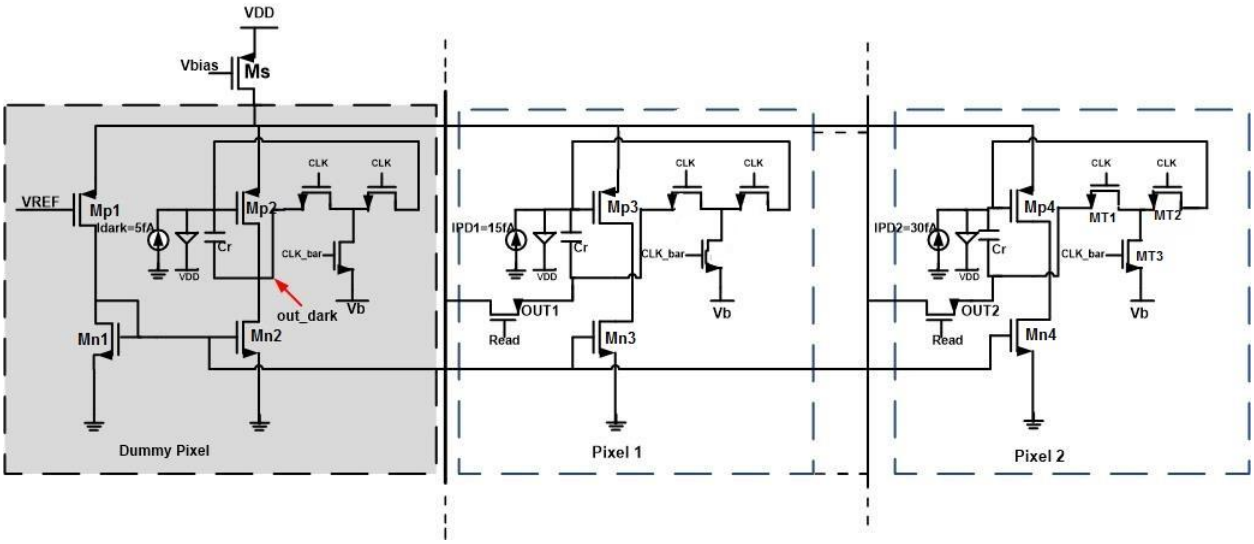

Figure 2.22. Multiple-Input Multiple-Output Differential Capacitive Transimpedance Amplifier.

Table 2.1. Parameter values of the circuit of Figure 2.24.

Parameters	Value
$(W/L)_N$	(0.5 µm /0.18 µm)
$(W/L)_P$	(0.5 µm /0.18 µm)
$(W/L)_T$	(0.5 µm /0.18 µm)
$(W/L)_s$	(0.5µm/0.18 µm)
I_{Dark}	0.5fA
I_{PD1}	15fA
I_{PD2}	50fA
V_{DD}	3.3V
V_{bias}	2.3V
V_{REF}	2 V
V_b	1.915 V
C_r	30 Ff
Clk	0-3.3V (PW=30 ms, T=40 ms)

2-4 Subtractor Circuit

Subtractor circuit is used for subtracting non-dummy pixels' output from dummy pixel. The schematic of a subtractor circuit is shown in Fig 2.25 which has a symmetrical structure [40]. The bias current of the circuit is obtained by M1 and M2 which operate as a current mirror source. The subtractor circuit has three inputs and one output. The three inputs are V_{BG1}, V_{BG2} and V_x. Since M1 and M2 operate as current mirror source, I_1 and I_2 are equal. M3 and M4 are driven by the constant current I_1 while M5 and M6 are driven by the constant current I_2. The gates of M3 and M4 are connected to V_{BG1} and V_{BG2} respectively. V_{BG1} is chosen to be larger than V_{BG2}. The gate of MOS transistor M6 connects to the constant voltage which keeps M6 in saturation region. The drain of MOS transistor M5 is the output of the subtraction circuit. Since M8 and M9 forms the current mirror circuit, $I_{D4}=I_{D5}$. From $I_1=I_2$, we get $I_{D3}=I_{D6}$. Based on the

relationships between the gate to source voltages and the drain currents, we can easily find that the output voltage of the subtraction circuit is given by the following equeation:

$$V_{sub} = V_x - (V_{BG1} - V_{BG2}) \quad (2.8)$$

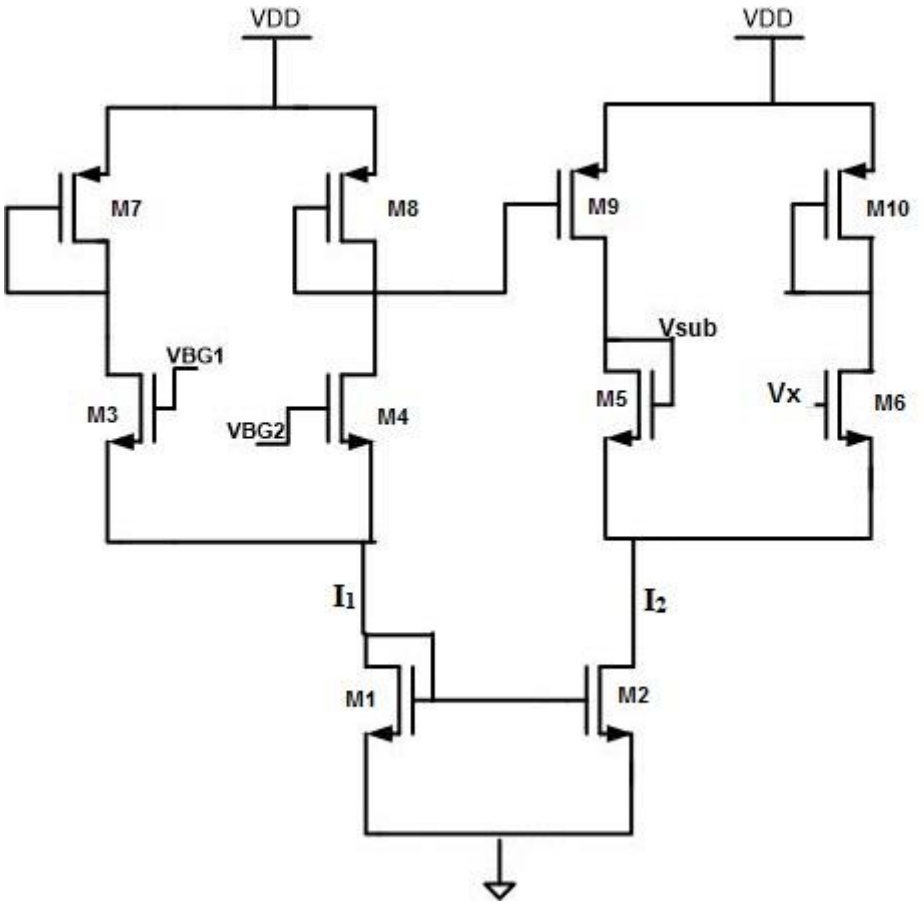

Figure2.23 Subtractor circuit [40]

Table 2.2 shows the parameter values of subtractor circuit:

Table 2.2 Parameter values of subtractor circuit:

$(W/L)_{(7,8,9,10)}$	(0.6µm/0.18µm)
$(W/L)_{(1,23,4,5,6)}$	(0.5µm/0.18µm)
V_{DD}	3.3V
V_x	2V

2-5 Summary

In the chapter a new architecture for compensating the effect of dark current in CMOS image sensors has been proposed. The proposed design which is presented in Figure 2.24 has the ability to sense low level illuminations by compensating dark current. It employs T-type switches which have reduced OFF transistor leakage current than regular MOS or TG switches.

CHAPTER 3 POST-LAYOUT SIMULATIONS AND RESULTS

In this chapter layout and post-layout simulation of designed structure is presented. Also Monte Carlo simulation has been done in order to analyze the effect of manufacturing process on the proposed design.

3-1 Simulation Results

3-1-1 Simulation result with three pixels

Simulation results of the circuit in Fig. 2.24, are presented in Fig. 3.1. According to equation (2.5), the graph shows that during the integration time the output voltage of each pixel has a slope which depends on the total photodiode current (I_{PD}=I_{Dark} +I_{Photo}). During the reset mode, the output is forced to V_{REF} because of the differential amplifier configuration. The integration and reset times are both selected to be 30ms and 10ms respectively.

All photodetectors in Fig. 2.24 are modeled by constant current sources [6, 15]. In this simulation, the current of the dummy pixel is set to I_{Dark} =0.5 fA (Table 3.1) and the photodiode current of the other pixels are chosen to be I_{PD1} =15 fA and I_{PD2} =50 fA. The integrating capacitor (C_r) is chosen to be 30fF.

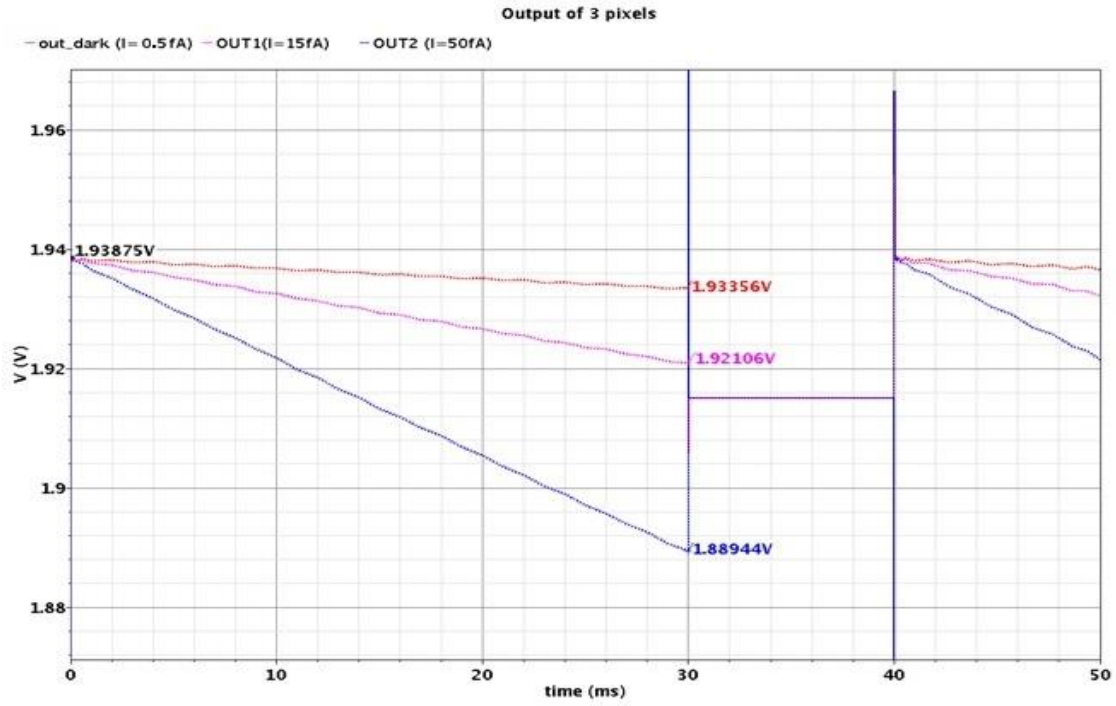

Figure 3.1. Pixels' output for Idark=0.5fA, I_{PD}=15fA and I_{PD}=50 fA

V_{bias} and V_{REF} values in the circuit of Figure 2.24 are set to 2.3V and 2V to keep all transistors in the active region. V_b is set to 1.915V in order to minimize the leakage current of reset switch. The supply voltage of the circuit is V_{DD}=3.3V.

By increasing the number of pixels in a row, the bias voltage of the current source transistor (M_S) should be decreased in order to feed the current to all branches in multi-branch differential amplifier.

By subtracting the output voltage of dummy pixel from the output voltage of each pixel, the output dependency on the photodiode dark current is greatly reduced as demonstrated by (2.7). The voltage subtracting circuit is implemented in column amplifier level.

3-1-2 Estimating the precision of the subtractor circuit

The subtractor circuit in Figure 2.25 is used to subtract the output voltage of two pixels.Figure 3.2 shows the output of dummy pixel and the output of pixel 2 with a photodiode current of 30fA

of Figure 2.24. Also the output of the subtractor circuit which subtracts the output of two pixels is shown in Figure 3.2.

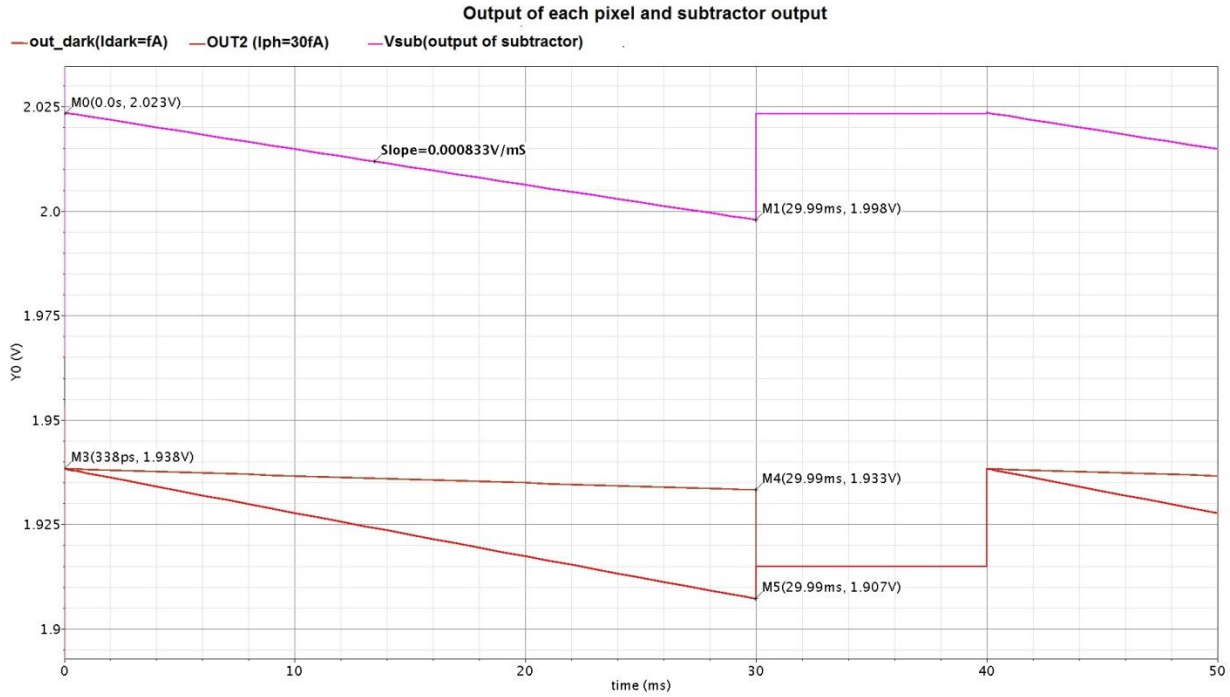

Figure 3.2 Subtractor circuit output, subtracting the dummy pixel output with I_{Dark}=0.5 fA from the output of pixel 2 with I_{PD}=30 fA.

In Figure 3.3, the output of the subtractor circuit in Figure 3.2 is compared to the output of a mathematical subtraction performed by Cadence graphic tools in order to estimate the precision of the subtractor circuit.

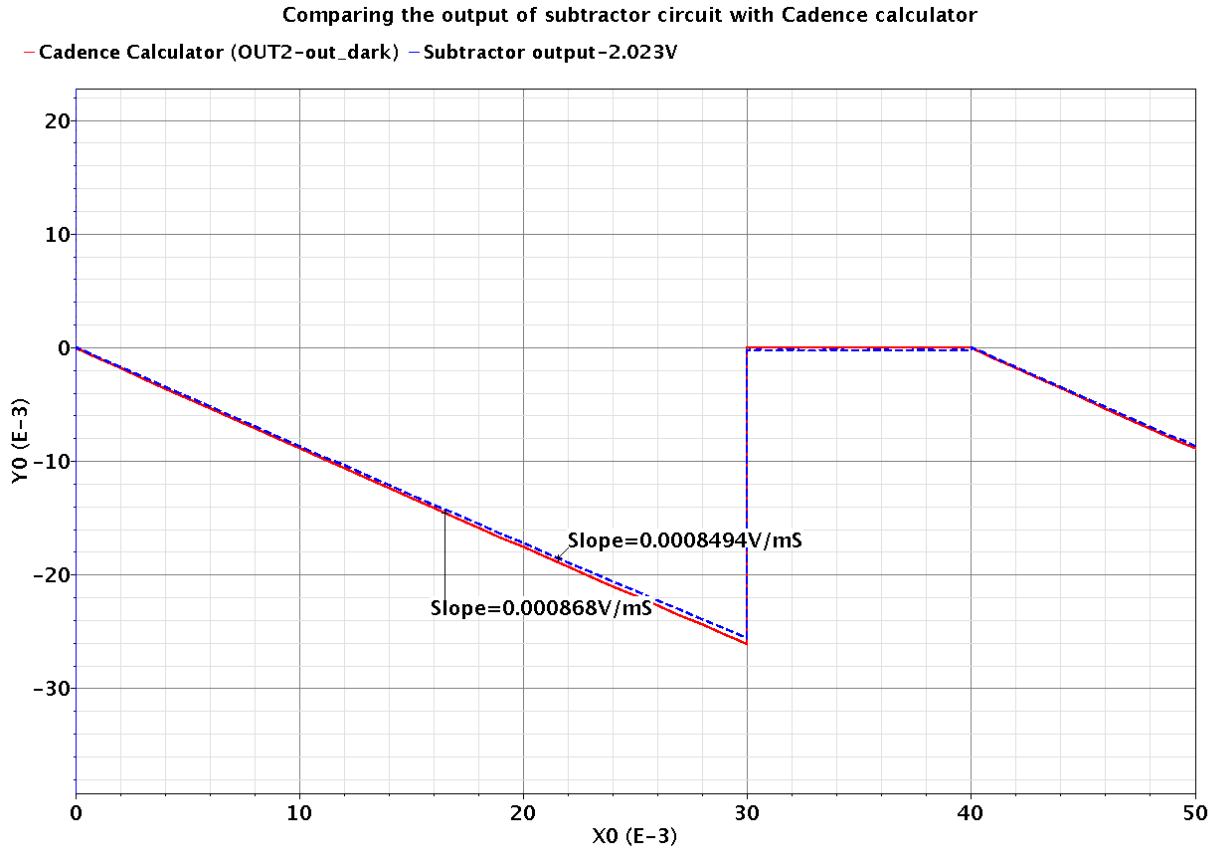

Figure 3.3 Comparing the output of the subtracting with Cadence graphic tools with the output of the subtractor circuit, (subtracting the dummy pixel output with Idark=0.5 fA from the output of the pixel 2 with IPD=30 fA).

As shown in this figure, the output using Cadence calculator and the output of the subtractor are nearly the same (The difference between the slopes of two outputs is about 2.14%).

3-2 Comparing the results of different switches

The circuit in Figure 2.24 is simulated to compare the results of three types of switches: TG, ideal switch and T-type switch. As shown in Figure 3.4, the output with TG (or single MOS switch) during the integrating time is not linear with a negative slope while the outputs with a T-type switch and the ideal switch have negative slopes which follow equation (2.5).

The TG switch as mentioned above destroys the output voltage considerably since the leakage current of the reset switch exceeds the dark current of photodiode. The leakage current of the TG switch is in the range of pico-ampere. This is larger than the photodiode dark current value

which is in femto-ampere range. Simulating the circuit with a T-type switch compared to an ideal switch leads to an error of less than 0.4% at the output.

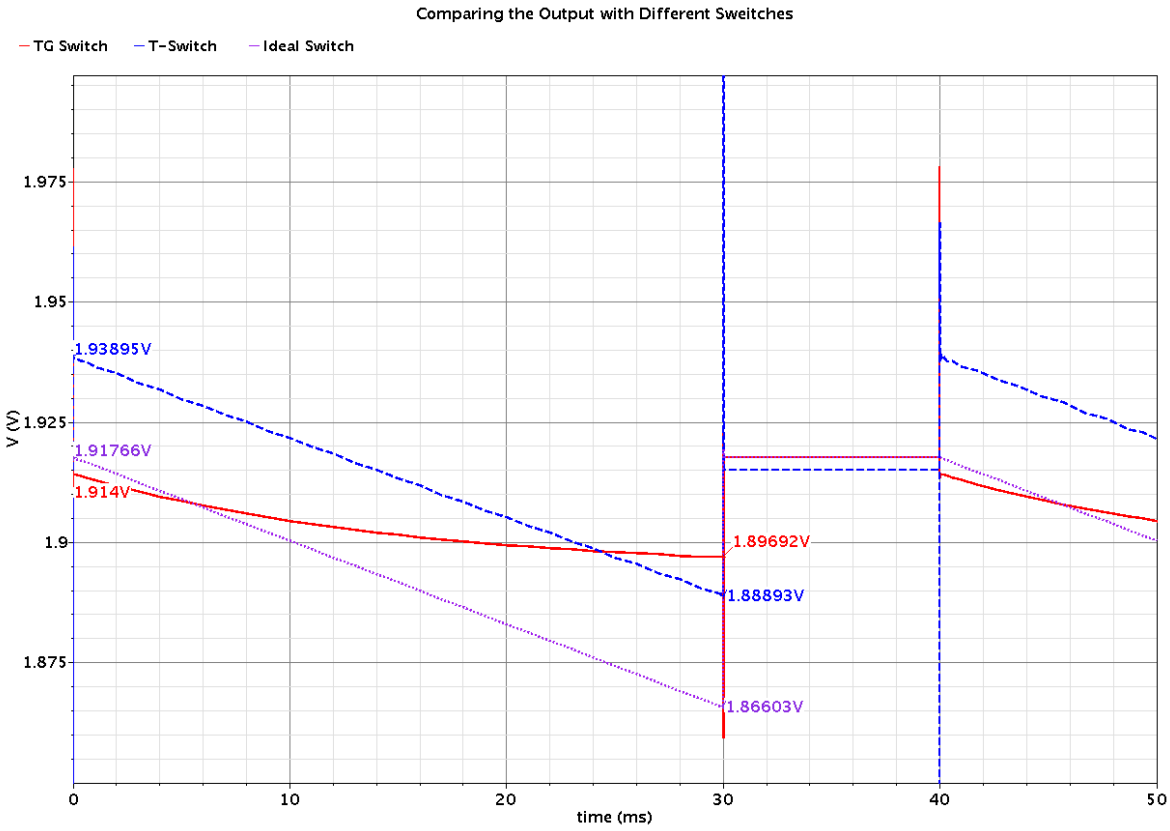

Figure 3.4. Output of a pixel with IPD =50 fA for the three types of switch

3-3 Dynamic Range

The dynamic range (DR) is the ratio of the maximum non-saturating voltage signal (the light level just below the system saturation) to the smallest detectable input signal (the light level just above the dark noise) in given image capture-time period.

The maximum non-saturated signal is measured by varying a current source as a photodiode current from femto- to pico-ampere range until the output saturation is obtained. In this

condition, the measured output swing is 1.903V for photodiode current of 2.5 pA according to Figure 3.5.

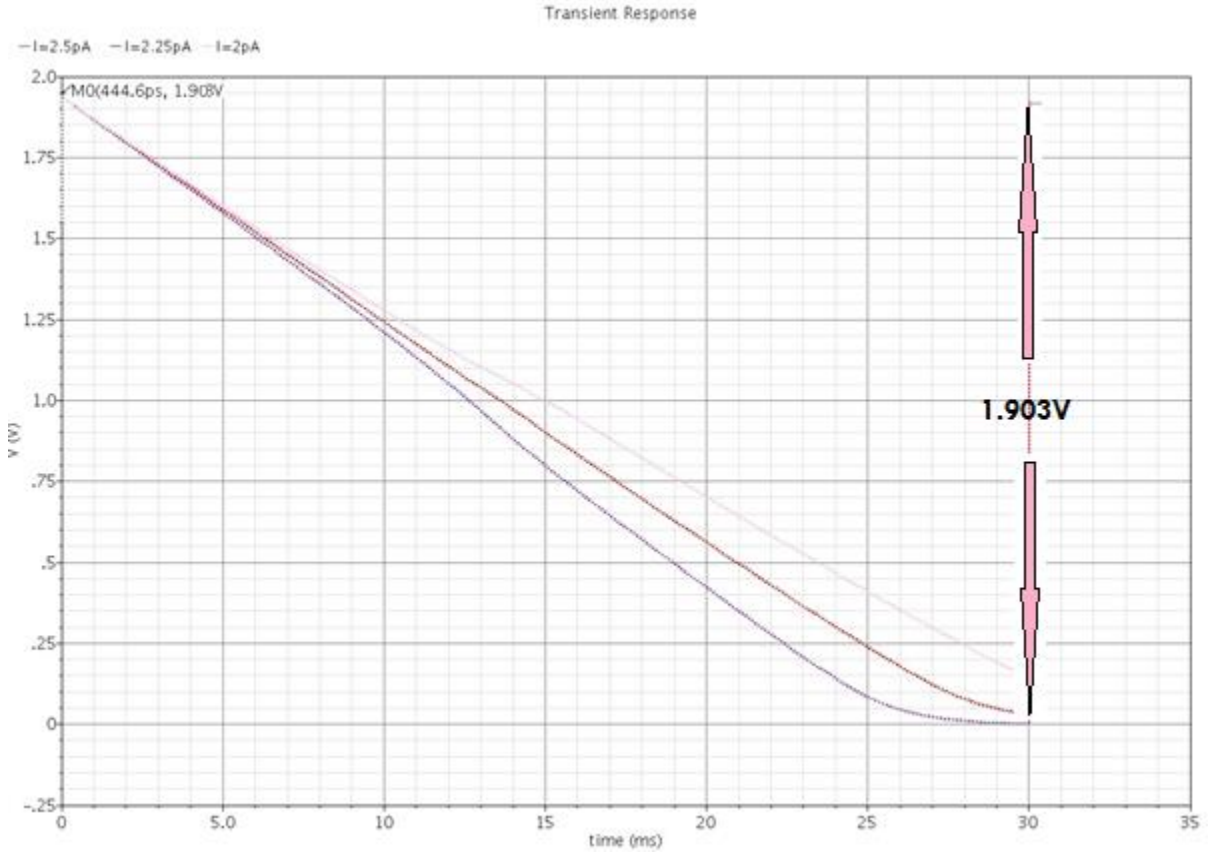

Figure 3.5 Maximum non-saturated output voltage of the pixel

Minimum output signal is evaluated considering the noise floor which is composed of the shot noise generated by the dark current, the flicker noise of the input transistor and the reset noise which is known as KTC noise.

Total rms noise value is calculated by using the following equation:

$$\langle V_{rms-total} \rangle = \sqrt{V_{shot}^2 + V_{1/f}^2 + V_{KTC}^2} \tag{3.1}$$

Flicker noise is caused by traps near Si/SiO2 interface that randomly capture and release carriers. The typical value of the flicker noise for PMOS transistors is equal to 2.28 e-28 c^2/m^2 which is negligible compared to other noise components [41].

During the integration phase, the dominant noise is the shot noise due to the dark current and the photocurrent. Assuming that the photodiode capacitance is constant over the integration period, with a PSD (Power Spectral Density) of shot noise given by

$$S_{In}(f)=q\,(i_{photo}+i_{Dark})\ A^2/Hz \tag{3.2}$$

If photodiode shot noise is modeled as a white Gaussian noise process, by integrating the photodiode current in C_{PD}, the following equation for the noise voltage of C_{PD} can be obtained [42, 43]:

$$\frac{d(v_{Cn})}{dt}=-\frac{I_n(t)}{C_{PD}} \tag{3.3}$$

$$v_{Cn}(t_{int})=-\frac{\int_0^{t_{int}} I_n(\tau)d\tau}{C_{PD}} \rightarrow v_{cn}^2(t_{int})=\frac{\int_0^{t_{int}} I_n^2(\tau)d\tau}{C_{PD}^2} \tag{3.4}$$

$$v_{cn}^2(t_{int})=\frac{q\,(i_{dark}+i_{photo})}{C_{PD}^2}t_{int} \tag{3.5}$$

where I_n is the current shot noise, C_{PD} is the photodiode capacitor which is typically equal to 27fF, v_{cn} is C_{PD} noise voltage, q is the electronic charge which is equal to *1.6 E-19* C, t_{int} is the integration time which is 30ms and i_{dark} is equal to 0.5fA (Table 3.1).

where :

$$V_{Shot}=\sqrt{v_{cn}^2(t_{int})=}=\sqrt{V_{dark}^2+V_{photo}^2} \tag{3.6}$$

$$V_{Shot\_dark}=\sqrt{V_{dark}^2}=\frac{\sqrt{qI_{dark}\,t_{int}}}{C_{PD}}=0.57\ e\text{-}4V \tag{3.7}$$

I_n is also integrated trough the C_r (integrating capacitor of Figure 2.4) which has negligible output noise voltage compared to the output noise voltage due to integrating of I_n trough the C_{PD}.

The value of KTC at T= 300K noise is equal to:

$$V_{KTC} = \sqrt{KT/C_r} = 3.69\,e\text{-}4V \tag{3.8}$$

where C_r is the integrating capacitor in Figure 2.24 which is equal to 30fF, K is Boltzmann constant and T is the temperature in Kelvin.

The value of the dark current shot noise is equal to:

$$\langle V_{rms} \rangle = \sqrt{V_{shot}^2 + V_{KTC}^2} = 3.72e\text{-}4V \tag{3.9}$$

The DC Gain of the differential amplifier is about 24dB as shown in Figure 3.6.

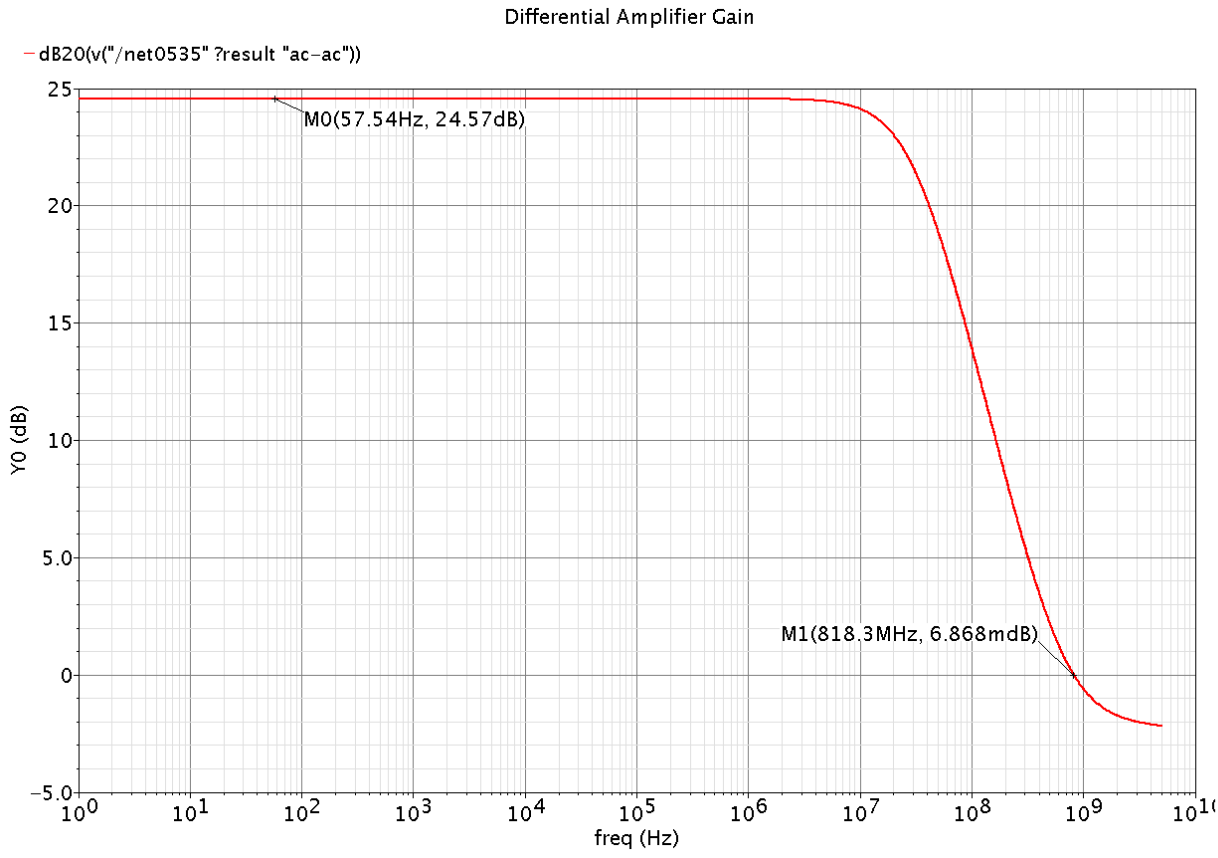

Figure 3.6 Differential amplifier gain

Therefore the value of the output noise voltage due to the input noise with amplifier gain of 24db is equal to:

$$V_{N\_out} = V_{N\_in} \times DC_{gain} = 3.72e\text{-}4 \times 10^{(24/20)} = 0.004173V \quad (3.10)$$

Therefore the value of the dynamic range is equal to:

$$20log \frac{Vmax}{Vmin} = 20log \frac{1.903}{0.004173} = 53.17dB \quad (3.11)$$

3-4 Layout Design

The fill factor and pixel size are the most important factors in designing the pixel of image sensors. Dedicating a small pixel area to the circuit part leads to a smaller pixel size and a higher fill factor while the remaining area of the pixel is occupied by the photo sensing element.

The smallest size transistors have been chosen in order to decrease the pixel size. Capacitor as a circuit element is an important component to optimize in the layout design in order to reduce the pixel size. Finally, the photodiode area size is chosen to get a reasonable fill factor above 50%.

3-4-1 Capacitor

In CMOS technologies, several different types of capacitors are available: MIM capacitors, p-n junction capacitors, Polysilicon-Insulator-Gate capacitors, transistors connected in a capacitor configuration, etc. Newer technologies with smaller feature sizes and a greater number of metal layers allow for greater capacitance densities [44]. Polysilicon capacitors were ignored because of the already existing polysilicon gated transistors in the pixel. A transistor in a capacitor configuration (source and drain shorted) gives a good capacitance per area ratio but gives a non-linear output since C_{gs} varies depending on the region of operation of the transistor and the temperature fluctuation. Capacitors that utilize the MOSFET gate oxide have the highest capacitance density that can exceed 6fF/μm^2 with recent technologies. For a pn junction capacitor, the process variations can cause a device mismatch generated by the fluctuations of the doping concentration and the doping profile [44]. MIM cap technology offers a capacitance density of around 1fF/μm^2 which is much less than MOS capacitor but it has a good linear response. Insertion transistors underneath a MIM cap are forbidden following the design rules especially for high frequency applications [Appendix A]. So using a transistor capacitor can save

more area. Besides, the linear response of the MIM caps with respect to temperature variation makes them more useful than transistor capacitors.

3-4-2 Metal-Insulator-Metal Capacitor (MIM Cap)

MIM cap is formed by two parallel metal plates in square shape. The top metal, CTM, forms the upper electrode and metal 5 forms the lower electrode. M6 is used to connect the CTM layer to the circuit. By using CTM as the top plate of the capacitor the thickness of the dielectric layer between the two electrodes is reduced in comparison with using M6 as a top plate layer. This helps to increase the total capacitance. The effective capacitance per unit area of the MIM cap is around lfF/μm^2 for the TSMC 180 nm technology [45].

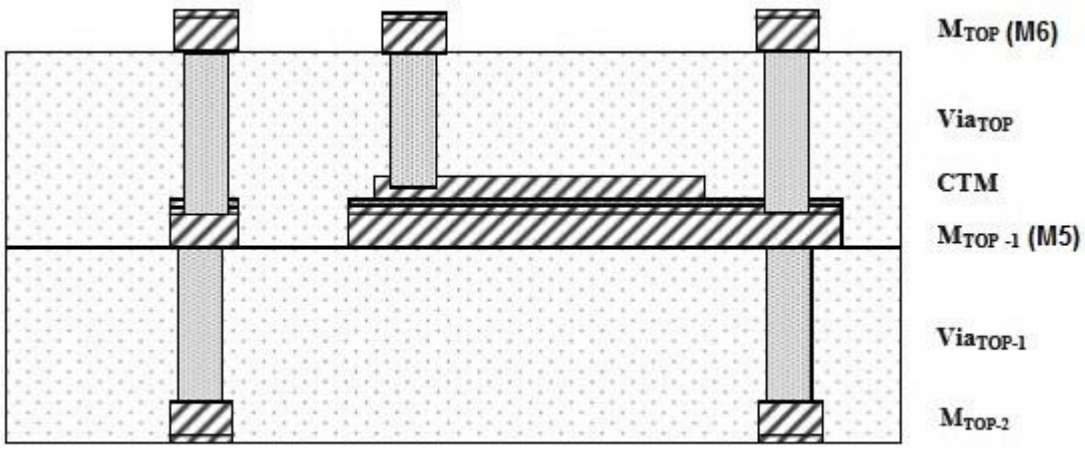

Figure 3.7. Cross section view of a MIM Cap [46]

The capacitance value of a MIM capacitor C_{M1M} can be computed by (3.13)

$$C_{MIM} = \frac{A_P \varepsilon_0 \varepsilon_I}{t_i} \tag{3.12}$$

where A_p is the area of one of the plates, ε_0 is the permittivity in vacuum, ε_i and t_i are the relative permittivity and thickness of the dielectric, respectively.

Equation (3.13) expresses the ideal value of C_{M1M}. Although, some of the electric fields called fringing fields go through the air instead of the dielectric and increases the apparent area of the plates which is proportional to the thickness of the dielectric. Since for a MIM capacitor, a thin oxide is used as its dielectric, it makes vertical dimension to be much less than the dimensions of its plates, this problem is usually neglected [47].

Figure 3.8 shows the equivalent circuit model of a MIM capacitor between Port 1 and Port 2 used in the Spectre simulator for TSMC 180 nm CMOS technology. In this model, $R_{M1M,s}$ and $L_{M1M,s}$ are the parasitic resistance and inductance in the electrodes, $C_{MIM,ox}$ is the oxide capacitance between the bottom plate of the MIM capacitor and the substrate, and $R_{MIM.sub}$ and $C_{MIM.sub}$ are the silicon substrate resistance and capacitance, respectively [46].

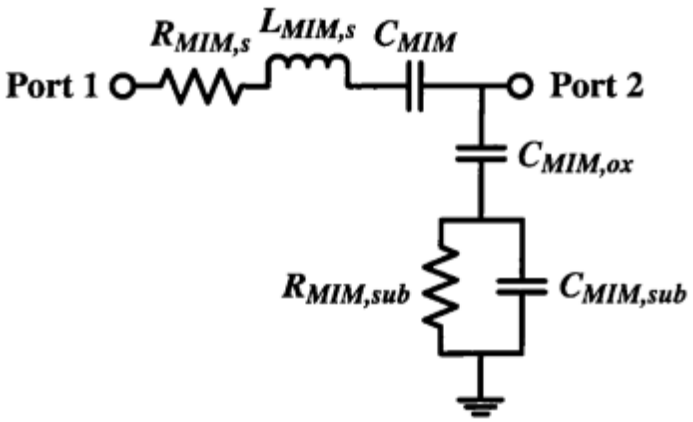

Figure 3.8. Equivalent circuit model of a MIM capacitor between Port 1 and Port 2 used in the Spectre simulator for the TSMC 0.18 um CMOS technology [46]

In order to decrease the pixel size and consequently increase the fill factor, MIM cap is put on top of the circuit part of a pixel. As mentioned in the design rules of TSMC 180nm, metal routing under the CTM layer is allowed since the application of image sensor is not a high frequency application and it does not require a high frequency signal isolation metal layer under the capacitor bottom metal layer.

3-4-3 Photodiode

P+/N-well photodiode has been used in this design. To prevent the photodiode from latch up effect, a substrate layer around the photodiode could be used. Since surrounding the photodiode with a p-substrate layer increases the pixel size, in this design, a common substrate between the photodiode and NMOS transistors is considered.

Dark Current and capacitor values of the photodiode are calculated using model parameter values of P+/N-Well in TSMC 180nm process.

Table 3.1. TSMC 0.18μm CMOS model parameters of the photodiode

Parameter Name	Parameter Value	
	Area	Perimeter
Junction Capacitance, C_D	1.000266×10^{-3} F/m^2	2.0402547×10^{-10} F/m
Dark Current, I_s	8.38×10^{-6} A/m^2	1.24×10^{-11} A/m

Since the square area and perimeter area of the photodiode are equal to $A_D = 27.70$ μm^2 and $P_D = 21.6$ μm, the junction capacitance and dark current of the photodiode are calculated as below:

$$C_D = A_D \times (1.000266\times 10^{-3}) + P_D \times (2.0402547\times 10^{-10}) = 32.12495238\ fF \quad (3.13)$$

$$I_s = A_D \times (8.38 \times 10^{-6}) + P_D \times (1.24 \times 10^{-11}) = 0.5\ fA \quad (3.14)$$

Therefore, the total dark current value of the P+/N-well photodiode with a chosen area size in the layout design (28.14μm^2) is in the range of 0.5fA.

3-5 Pixel Layout

Figure 3.9 shows the pixel layout and an addition part circuit which is needed for dummy pixel. The capacitor is put in top of the non- photosensing part of the pixel and the size of each pixel is $9\times9\mu m^2$.

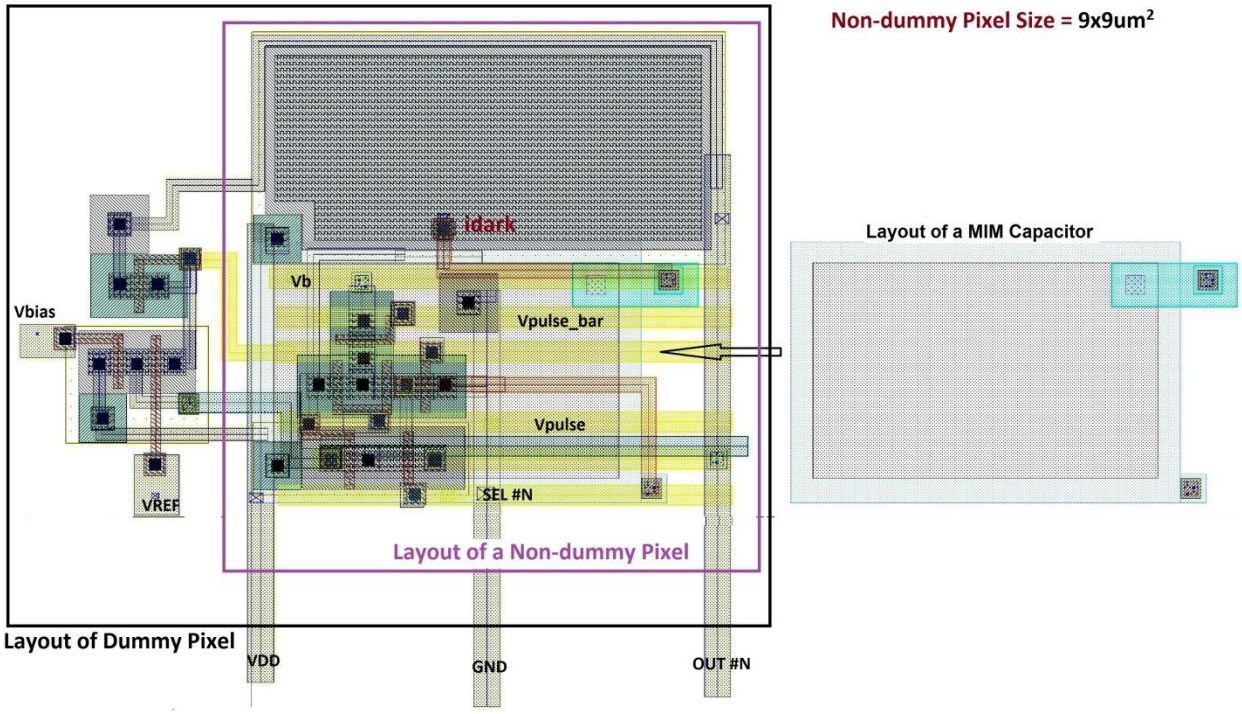

Figure 3.9 Pixel layout

Table 3.2 Characteristics of the pixel circuit

Number of transistors per pixel	5
Photo sensing Area	28.14 μm^2
Active Pixel Size	81 μm^2
Fill Factor	34.7%
Minimum transistor channel Length	0.18 µm

Table 3.2 Characteristics of the pixel circuit (Continue)

Minimum transistor channel Width	0.15 µm

N-well or P-substrate guard ring could also be used around the whole circuit of each transistor in the design in order to prevent the latch up effect.

3-6- Shift Register

The implementation of the readout control signals is explained is this section. Row selection or column selection control signals are done using shift registers or decoders. In this design a column shift register is used to readout the signals of a row in the pixel array.

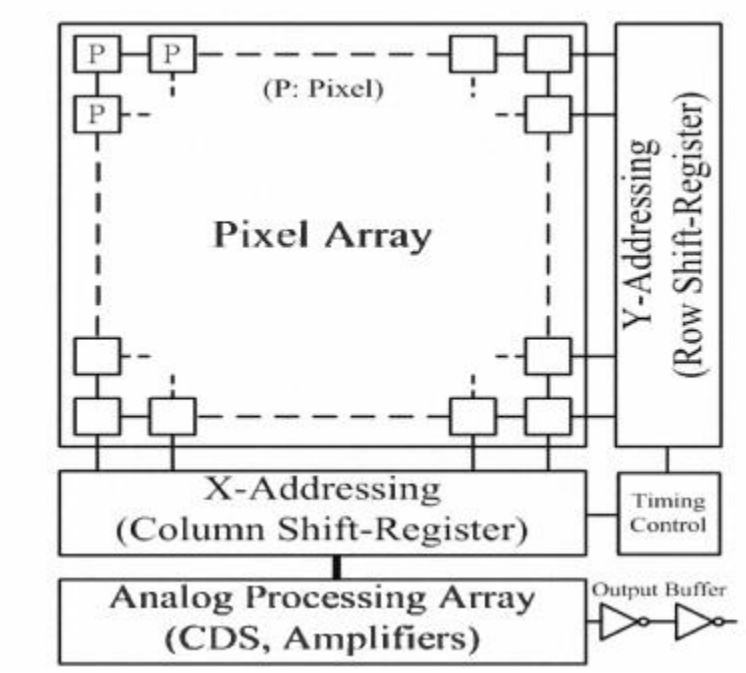

Figure 3.10. Structure of a CMOS Image Sensor

3-7 Circuit Simulation with Ten Pixels Including the Shift Register

The readout circuit symbol of ten pixels in a row is shown in Figure 3.11.

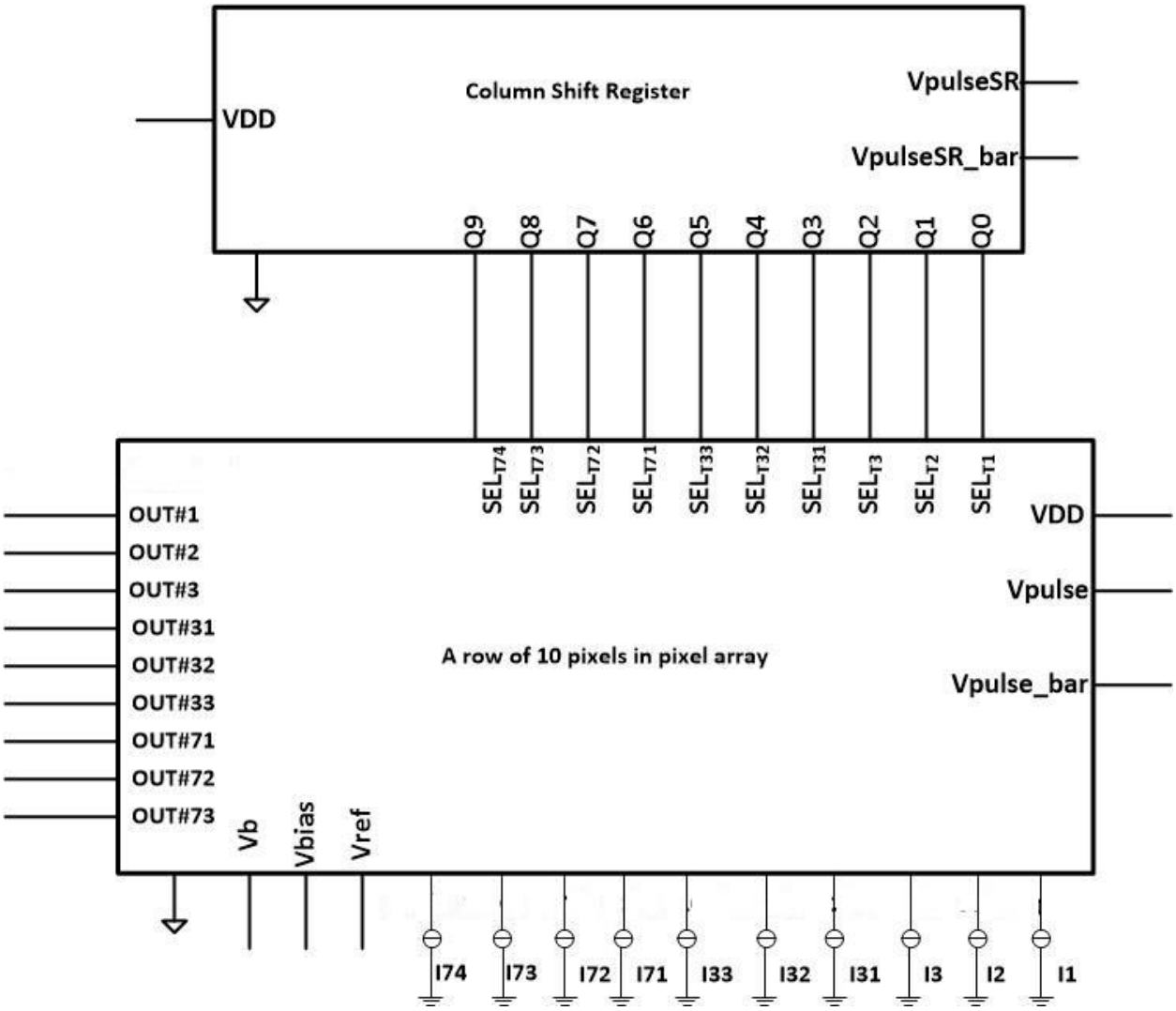

Figure 3.11. Layout schematic symbol of 10 pixels out of a row of 100 pixels with readout circuit

By increasing the number of pixels in a row, the gate biased of the current source transistor (M_S) should be decreased in order to feed the current to all branches in multi-branch differential amplifier.

Table 3.3 Parameters of the circuit in Figure 3.11

V_{DD}	3.3 V
$V_{pulse} = V_{pulse\_bar}$	0-3.3V (PW=30ms, T=40ms)
$V_{pulseSR} = V_{pulseSR\_bar}$	0-3.3V (PW=1ms, T=2ms)
IN	0-3.3V (PW=20ms, T=20.5ms)
V_{bias}	1.85 V
V_b	1.783 V
V_{REF}	1.9 V
$I_{D3,33,73}$	50Fa
$I_{D2,32,72}$	15Fa
$I_{D1,31,71}$	0.5fA

The post layout simulation of Figure 3.12 is given in the following section. The slopes of readout signal of 9 pixels out of 100 pixels show the output of pixels with a specific value of a photodiode current.

Slopes around 0.17, 0.57 and 1.6 V/S respectively represent the output of the pixels with photodiode currents of $I_{D1,31,71} = 0.5fA$, $I_{D2,32,72} = 15fA$ and $I_{D3,33,73} = 50fA$.

3.8 Analysis of the Parasitic Effect

By increasing the design size and decreasing the technology size, the impact of parasitic elements becomes more important.

In this design, pixels with more distance from the dummy pixel could be affected by parasitic elements such as added capacitance and resistance due to circuit interconnections. In order to see these effects, the simulation of a row of 100 pixels was performed by assuming the same photodiode current in each pixel.

Figure 3.12 shows post-layout simulation results of the output of the farthest and the closest pixel from the dummy for the same photodiode current. It demonstrates that there is no effect of parasitic elements in this design.

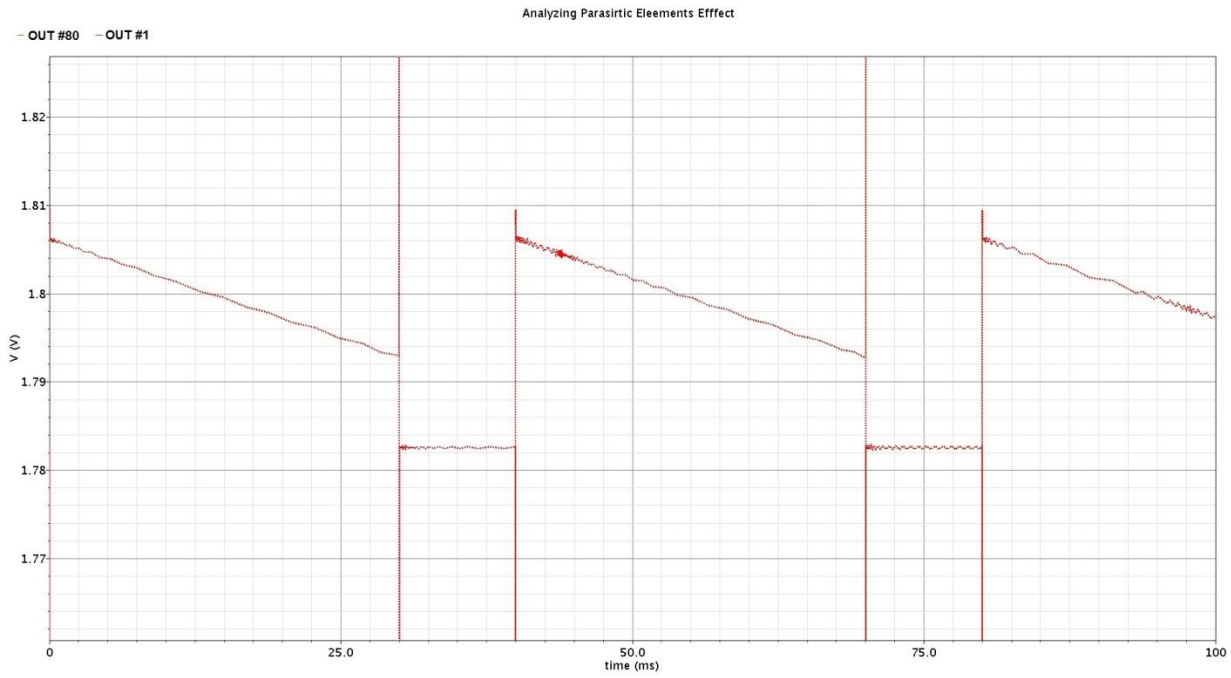

Figure 3.12 Comparison the output of the first and 80th pixel out of 100 pixels for IPD value of 15fA

3-9- Switch Leakage

The leakage current of the reset switch has been decreased by using the T-type switch configuration. However, there is still a leakage current contribution from the T-switch which

could have some effect at the amplifier output. To evaluate the value of the T-switch leakage, the output of the circuit is measured without the photodiode. As shown in Figure 3.13, the value of the leakage current is in the range of 2.01fA which is calculated by (3.16).

$$I_{Leak}=\frac{(V_{Out}(t_2)-V_{Out}(t_1))\times C_r}{t_2-t_1}=\frac{(1.8403-1.847)\times 30fF}{100mS}=\ 2.01\text{fA} \qquad (3.15)$$

The output of the pixel with photodiode currents of 1fA and 10fA is also shown in order to compare the slopes. The value of the T-switch leakage is however compensated by the dummy pixel since the dummy pixel has the same T–switch configuration.

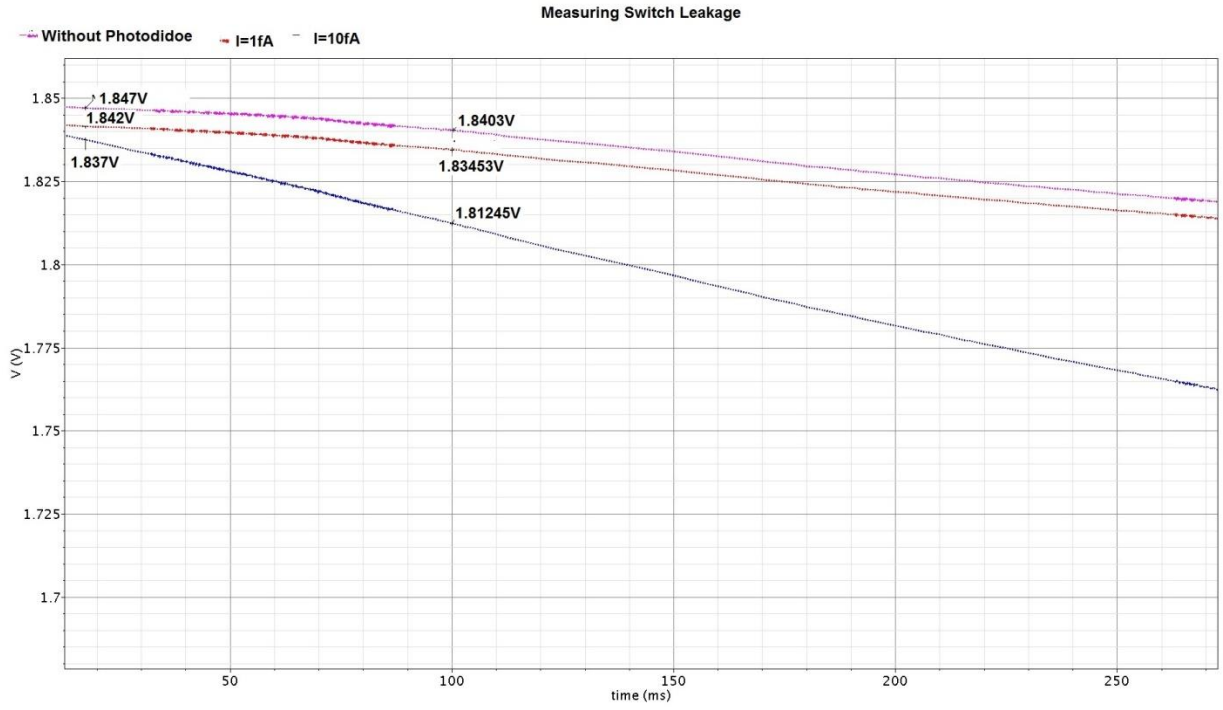

Figure 3-13 Measurement of the T-Switch leakage current

Figure 3.14 shows the pixel output after a long exposure time. By increasing the V_{DS} value of NM3 in Figure 2.22 due to the capacitor charging by photodiode current or the leakage current of NM3, the leakage current of NM3 is increased and leads to capacitor charging in opposite direction. Therefore, the output saturation voltage level depends on the photodiode current value.

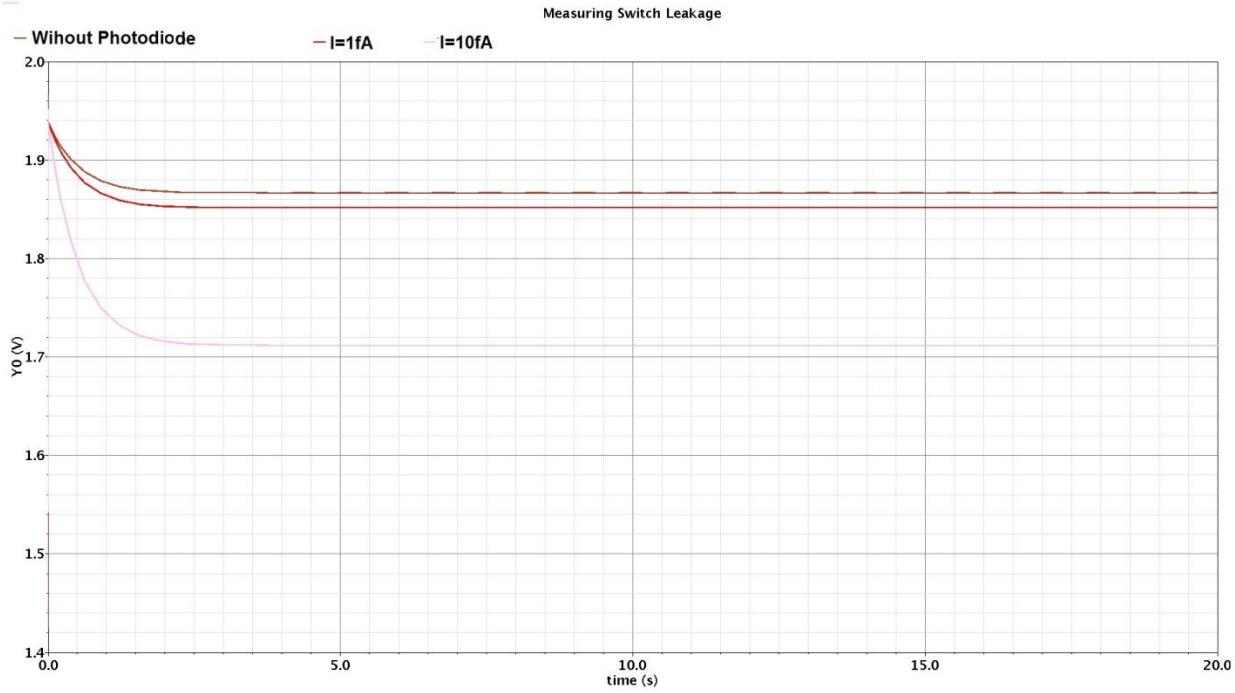

Figure 3.14 Output of Pixels in long exposure time

3-10- Monte Carlo Simulation

In this part, two different sources of variation are distinguished and analyzed: process variations and temperature variations. The process variations are due to variations in manufacture conditions. The most effective parameters of transistors which affect the circuit operation are V_{th}, W and L. Temperature variations affect the behavior of the circuit due to MOSFET parameters change such as V_{th}.

3-10-1 Process Variation

The physical deviation of the manufacturing processes such as the implantation dose and the energy can generate variations in the device structure and the doping profile. These variations together with the temperature drift affect the electrical behavior of the devices in a circuit.

Devices and interconnects have variations in film thicknesses, lateral dimensions, and doping concentrations [48]. The parameters of individual transistors are classified as inter-die and intra-die variations.

Table 3.4 shows the MOSFET parameters and relevant process steps that directly influence each of those parameters [49].

Table 3.4 MOSFET parameters and their relevant process steps

Device Parameter	Relevant Process Step
μ	Ion implantation, diffusion, annealing, stress
C_{ox}	Gate Oxide Formation
W,L	Etching, lithography
V_{th}	Ion implantation, gate oxidation, annealing, etching, lithography

3-10-2 Analyzing the Effect of Process Variations in the Designed Structure

The effect of process analysis of Monte Carlo simulation in the leakage current of the reset switch is described in this part. As discussed before, the subthreshold leakage current of the MOSFET in the OFF mode is calculating using the equation:

$$I_{SUB} = \mu_0 C_{ox}\left(\frac{W}{L}\right)(V_T)^2\, e^{1.8}\, e^{\frac{V_{gs}-V_{th_0}-\eta V_{ds}-\gamma V_{sb}}{nV_T}}\left(1 - e^{-|V_{ds}|/V_T}\right) \quad (3.16)$$

Three different process parameter distributions are supported by Spectre: Gaussian, uniform and Lognormal. Gaussian distribution is used since it's defined in the design library kits of TSMC 180nm CMOS process for MOSFET parameters variation.

Due to variation of $\beta = \mu_0 C_{ox}\left(\frac{W}{L}\right)$ and V_{th} parameters of the current source MOSFET (M_s in Figure. 2.24) in each iteration, the current of M_s is changed according to (3.17). Therefore, the current of all branches of the differential amplifier which are fed by the current source transistor

will be changed. . In order to keep all the MOSFETs in the saturation region and ensure the same current in each branch, all voltages of all nodes in the circuit vary at each iteration.

Figure 3.15 shows the output voltage of a pixel with I_{PD}=30fA in Figure 2.24 for 10 iterations in the process variations analysis:

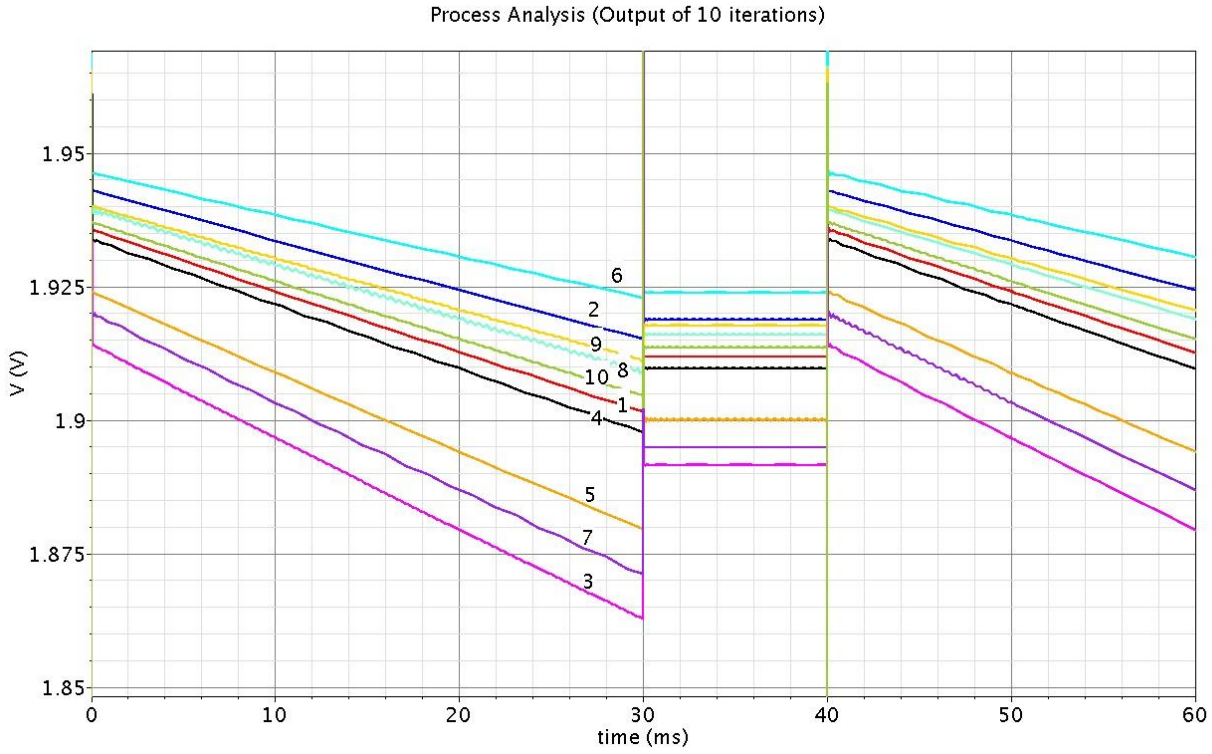

Figure 3.15 Output of a pixel of Figure 2.24 for 10 iterations

As seen, different slopes exist due to different values of V_{ds} of M_{T2} in Figure 2.24. The differences between the drain (V_p) and the source (V_x) voltages of M_{T2} are presented in Figure 3.16 for each iteration (all simulations were done for a pixel current of I_{PD}=30 fA).

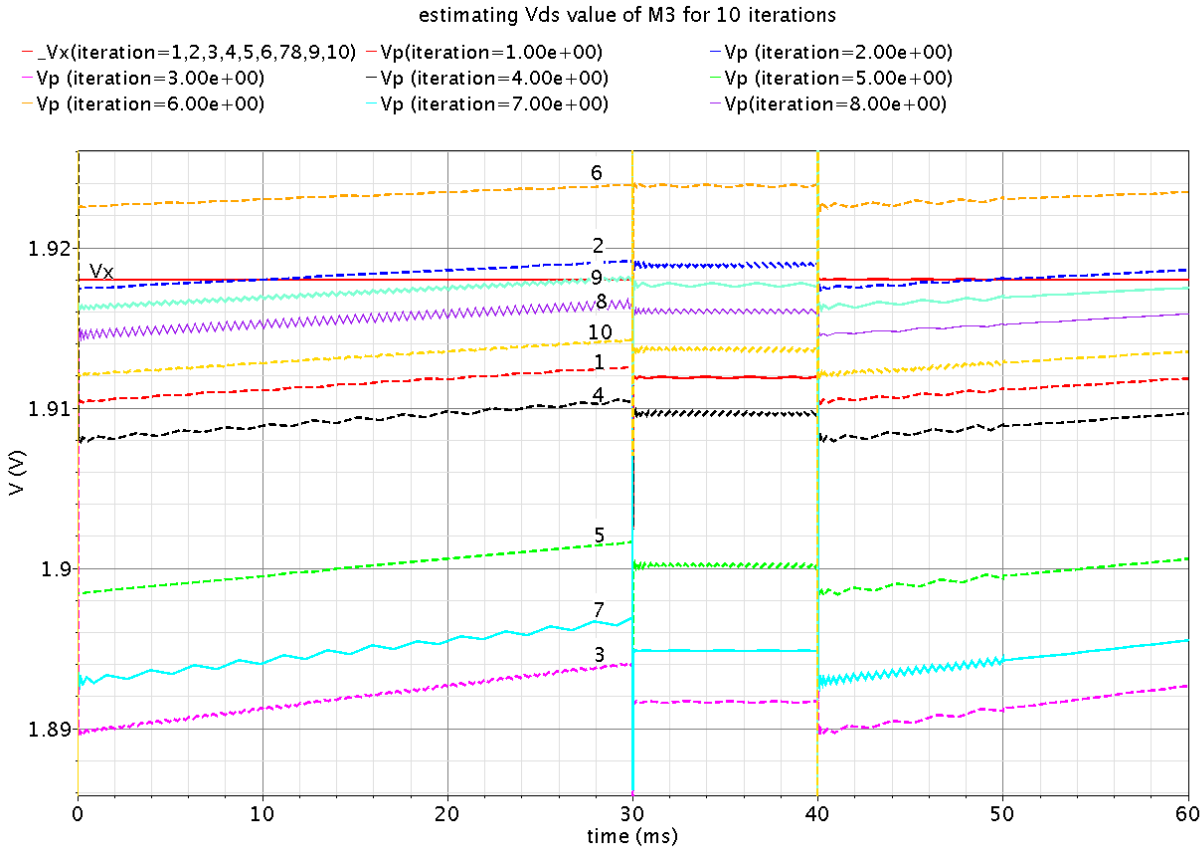

Figure 3.16 Vds values of MT2 for 10 iterations

With higher values of V_{ds} for M_{T2}, the leakage current of the reset switch is increased. Therefore, the output slope is higher due to the integration of both the leakage current of the reset switch and the dark current of the photodiode. As shown in Figure 3.16, in iteration 6, V_p is more than V_x, therefore V_{ds} has negative value. In this iteration since the V_{ds} value is negative, the leakage current of M_{T2} is in reverse direction of the photodiode current and makes smaller slope than iteration 1 with the same $|V_{ds}|$ value.

Figure 3.17 a,b shows V_{th} and β values for each iteration for NMOS and PMOS transistors in the circuit.

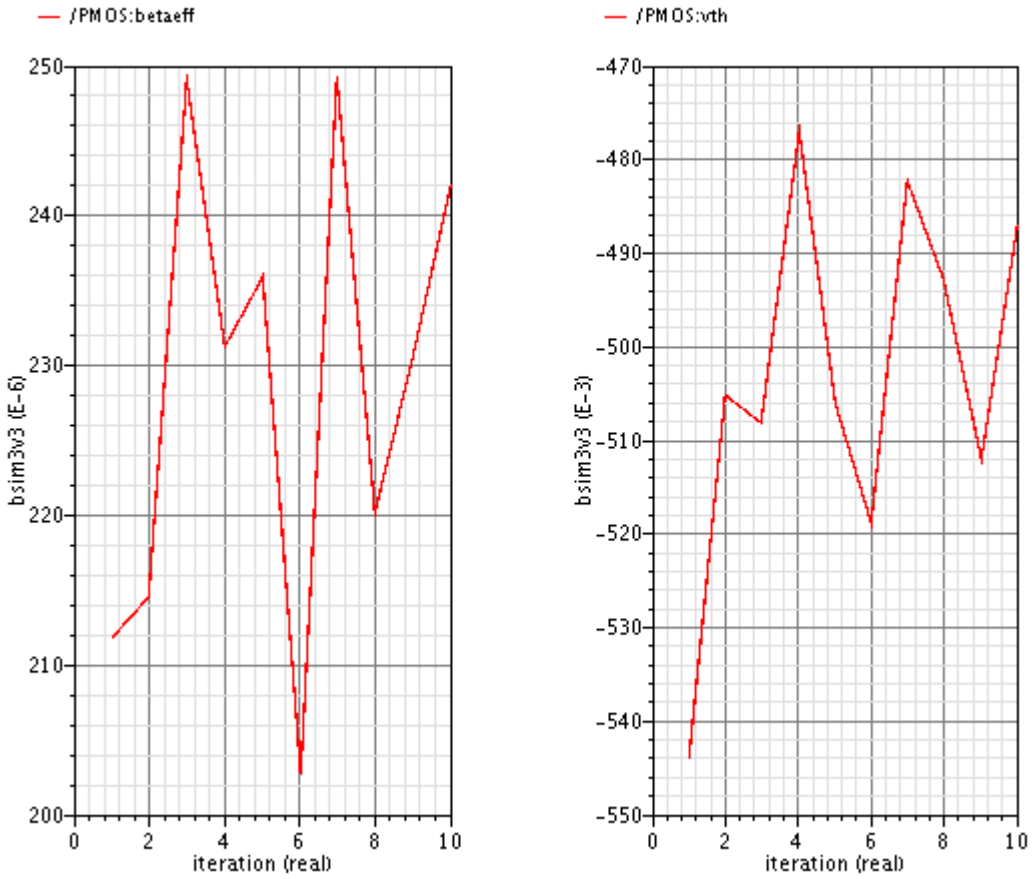

Figure 3.17.a V_{th} and β variation in 10 iterations for PMOSs

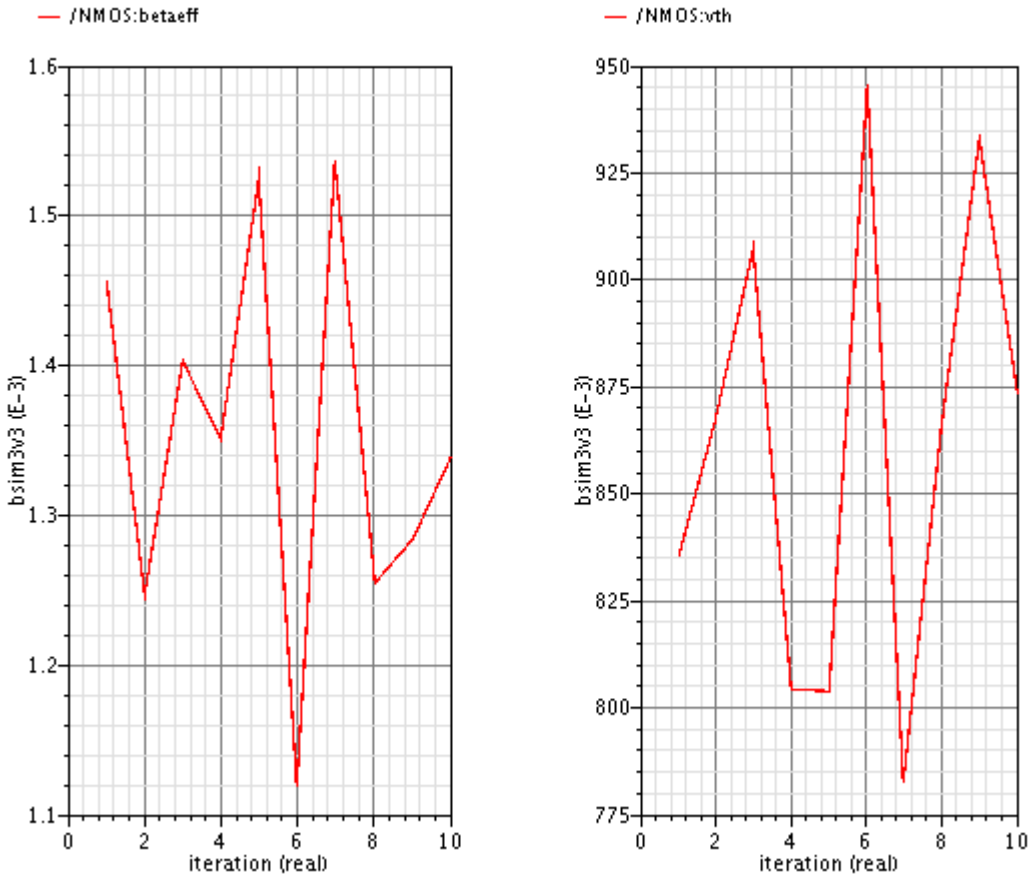

Figure 3.17.b. V_{th} and β variation in 10 iterations for NMOSs

Since M_S in Figure 2.24 has a constant value of V_{SG}, variation of V_{th} and β parameters gives different values of the bias current for each iteration. With higher value of $\beta \times (Vsg - V_{th})$ for M_S, the bias current gets larger. Iteration 5 has the highest bias current value while iteration 6 has the minimum bias current as shown in Figure 3.18. Also Figure 3.18 shows the current of M_S, M_{P1} and M_{p4} of Figure 2.24. It shows how the current of M_S is divided between M_{P1} and M_{P4} which exist in two different branches of differential amplifier. Since the gate voltage of M_{P1} is 2V and gate of M_{P4} is less than 2V due to offset effect of differential amplifier, Current of M_{P1} is smaller than M_{P4} with smaller V_{SG} voltage value.

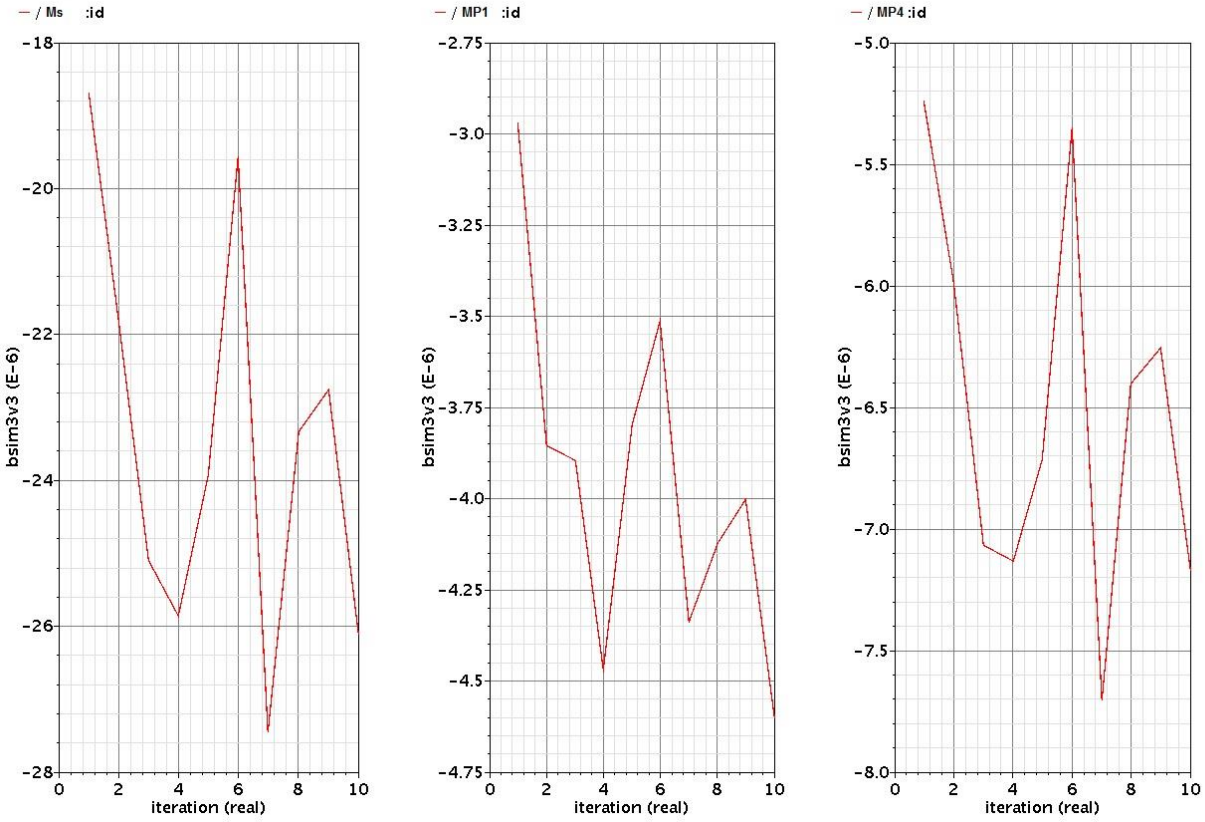

Figure 3.18 Bias current of Ms and branches of differential amplifier (Mp1 and Mp4)

Since in each iteration, branches get different values of bias current, M_{P1} with constant gate voltage tries to justify its source voltage by following (3.17). Due to different values of V_{th} and β for Mp_1 and bias current of MOSFET, the source voltage of Mp_1 and Mp_4 get different values in each iteration. Also the gate voltage of Mp_4 gets different values in each iteration. This voltage affects V_{ds} value of M_{T2} and changes the leakage current value of reset switch in each iteration.

Table 3-5 *β, Vth* of MOSFETs and slope value of a pixel output with I_{PD}=30fA for 10 iterations.

		1	2	3	4	5	6	7	8	9	10
PMOS	β (Vcm^{-1})	2.055E-4	2.085E-4	2.421E-4	2.25E-4	2.292E-4	1.968E-4	2.426E-4	2.141E-4	2.242E-4	2.357E-4
	Vth(V)	-0.6937	-0.6527	-0.6603	-0.6246	-0.6575	-0.6684	-0.6324	-.6416	-0.6628	-0.6356
NMOS	β (Vcm^{-1})	1.725E-3	1.494E-3	1.694E-3	1.6E-3	1.804E-3	1.345E-3	1.825E-3	1499E-3	1.542E-3	1.605E-3
	Vth(V)	0.5057	0.5327	0.5584	0.5026	0.4911	0.5648	0.4875	0.5283	0.5630	0.5411
	Slope (V/mS)	0.001132	0.000933	0.001709	0.00120	0.00148	0.000782	0.00161	0.001	0.000955	0.001132

The following histogram shows the distribution of leakage current for many iterations by displaying the slope value of the subtractor output for 75 iterations.

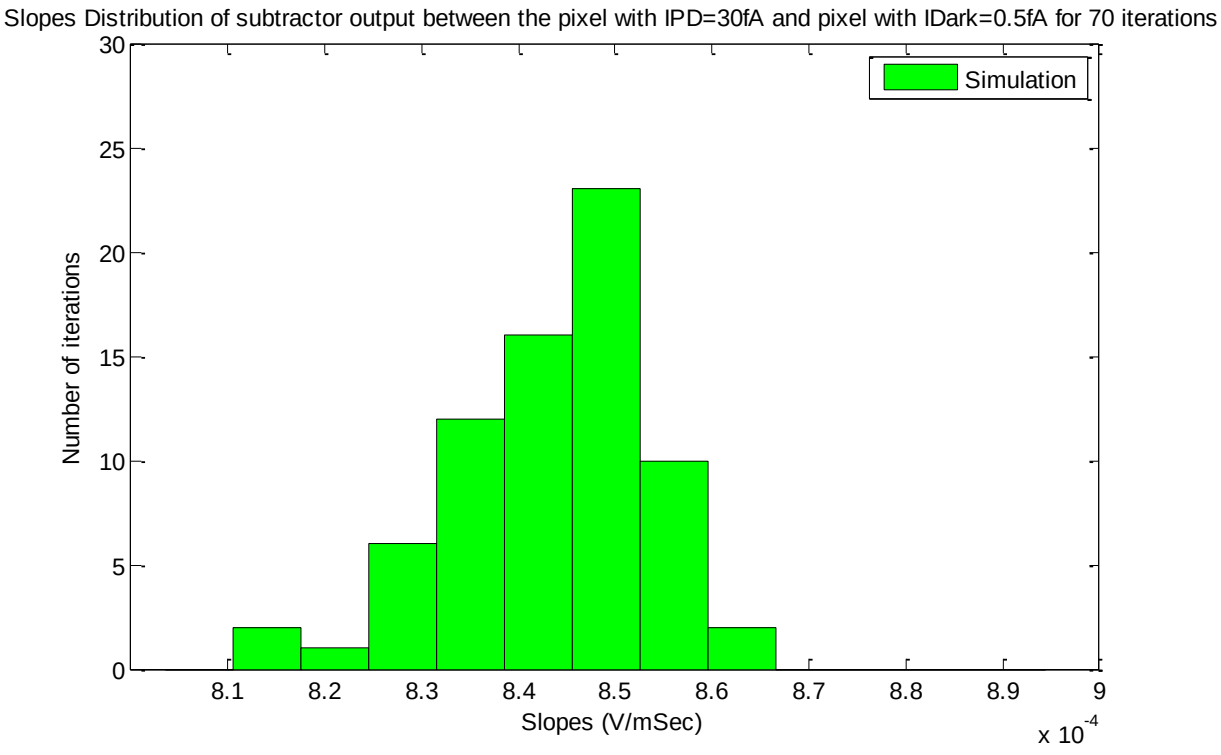

Figure 3.19 Slopes of subtractor output which subtract the output of dummy pixel from the pixel with IPD=30fA for 70 iterations

The values are compared with the slope of 0.0008666 V/mS which is the output slope of the subtractor that subtracts dummy pixel output with I_{dark}=0.5fA from the pixel output with I_{PD}=30fA for the designed pixel with minimum MOSFET size.

The standard deviation (STD) and the mean value of the histogram are 1.2604e-05 V/mS and 8.4275e-04 V/mS respectively. The mean value of histogram is near to the output slope of Figure 3.3.

3-10-3 Operating Temperature

By sweeping the temperature from -40 Celsius to 60 Celsius, the leakage current of reset switch is increased as shown in Figure 3.20.

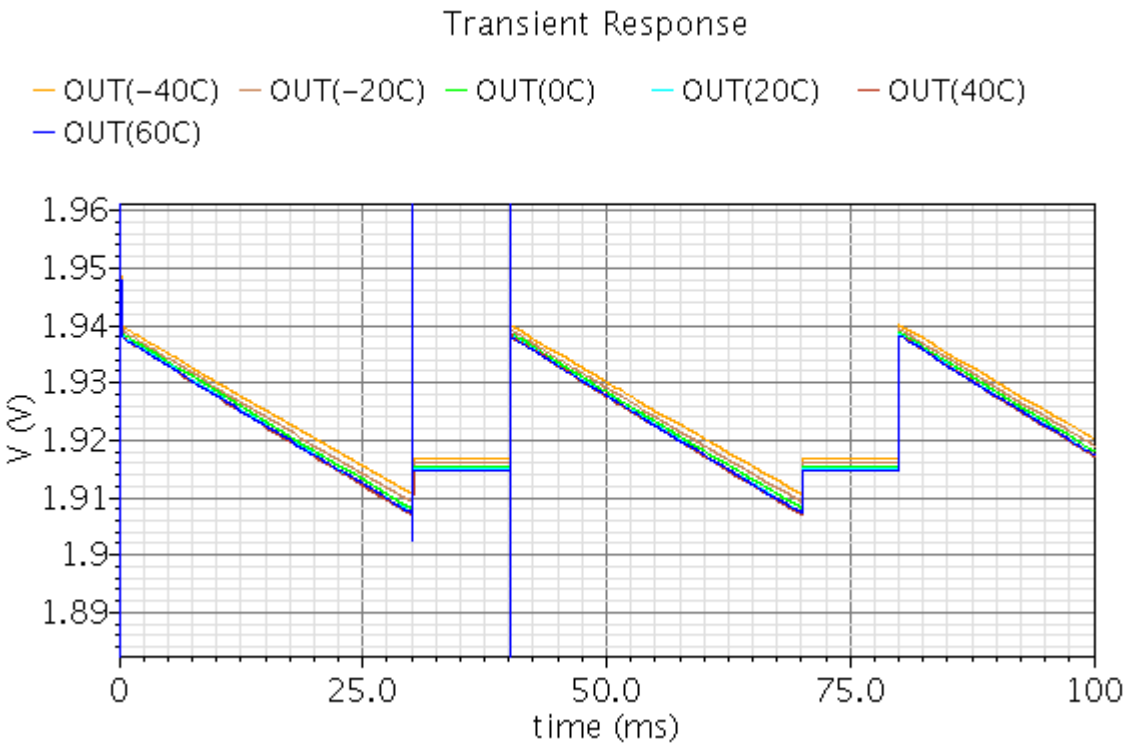

Figure 3.20. Pixel output with IPD=30fA for different temperatures

Table 3-6 Output slope of a pixel with I_{PD}=30fA of Figure 2.24 for different temperatures

T (^{o}K)	233	253	273	293	313	333
Slope (V/mS)	0.000978	0.001010333	0.0010266	0.0010376666	0.0010453333	0.0010306666

Also the voltage of drain (V_x) and source (V_p) of M_{T2} is shown in Figure 3.21 for different temperatures:

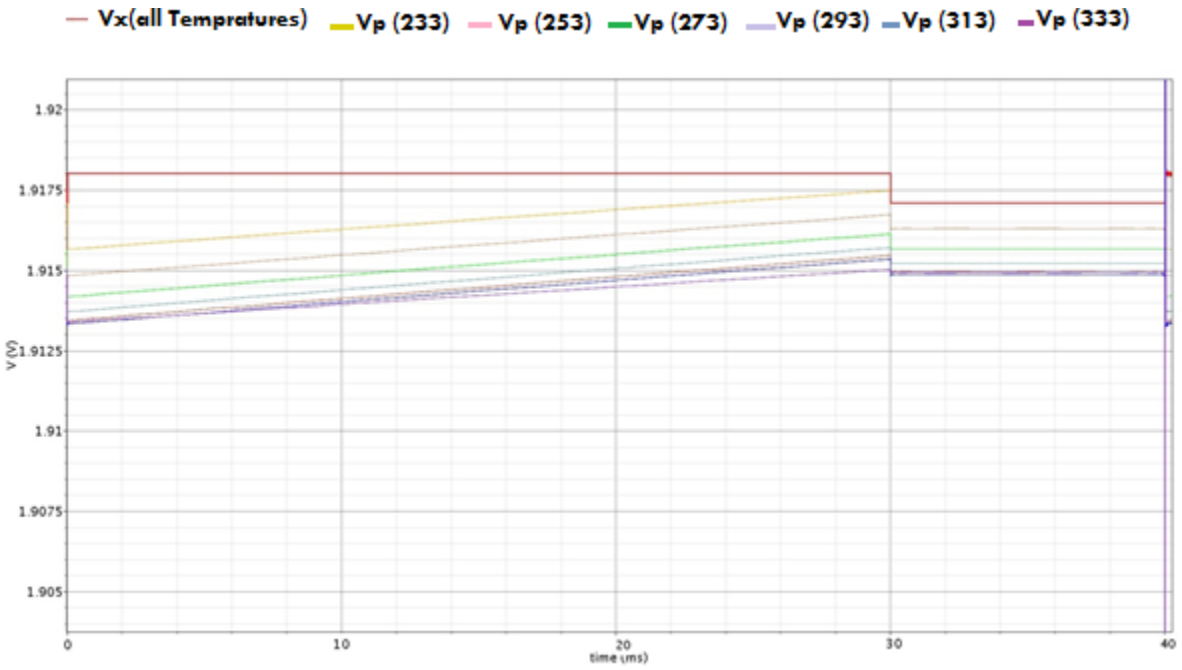

Figure 3.21 Estimating Vds value of MT2 for different temperatures

As shown in the figure, the value of V_{ds} increases 0.0002V per 20 Kelvin increasing in the temperature.

3-11 Summary

In this chapter, post layout simulation of the implemented circuit for dark current compensation has been presented. Also the operation of the proposed circuit with different switches has been analyzed. The structure with reset switch with leakage current value of less than 2fA is implemented. The output of 100 pixels in a row for analyzing the effect of parasitic elements in the large design has been compared. Finally, Monte Carlo and temperatures variations simulations have been performed in order to see their effect on our design especially on the leakage current of the reset switches. The results show process variation doesn't have much negative effect in the circuit operation while temperature has more effect in the circuit operation which increases V_{ds} value by 0.0002V per 20 Kelvin.

CONCLUSION AND FUTURE WORK

CMOS image sensors have the ability of on-chip signal processing, low cost and low power consumption. However, CMOS imagers have higher dark current when compared to CCDs which prevents it from being a prevailing technology for high-end applications. It is well known that the dark current is mainly generated from the interface defects that are located in the vicinity of the shallow trench isolation (STI) and in the depletion region of the photodiode at the Si/SiO_2 interface. There have been many efforts to reduce the dark current of CIS pixels. Some methods are implemented by process modification such as pinned photodiode and others reduce the dark effect without any process modification such as using n+ ring reset. In this thesis we proposed an Active Pixel Sensor (APS) architecture without any process modification which compensates the effect of the dark current. The proposed technique enables a low-level sensing application for image sensor, by increasing the dynamic range and improving the linearity. Desired dynamic range which is achieved by this structure is 53dB.

In this dissertation several new ideas/contributions have been proposed:

- A new multi input/output differential amplifier structure has been proposed in order to compensate the dark current effect in CMOS image sensors. The goal is to design a pixel circuitry having a small footprint to keep a reasonable fill factor for a small pixel size.

- T-type switch has been used as a reset switch of the APS structure in order to reduce the leakage current. Therefore, the new configuration of multiple-input multiple-output differential amplifier has the advantage of carefully managing the femto-ampere dark currents of photodiode.

- The leakage current of different types of switches has been compared and measured by simulating the proposed configuration with a sample and hold circuit structure.

-The design has been optimized and extended for a large number of pixels in a row.

-All simulations have been verified by post-layout simulation which considers the effect of parasitic capacitors and resistors. Also the post-layout simulation for 100 numbers of

pixels in a row shows that parasitic elements don't have effect even on the operation of the pixel which has the farthest distance from the dummy pixel.

-Process and temperature variation has been done which is related to manufacturing and environment effects. As shown in the results, process variation doesn't have much negative effect in the circuit operation while temperature has more effect in the circuit operation.

Future work could be achieved in following areas:

- In small technologies (130nm) gate leakage of MOSFET is the main leakage which is larger than the dark current value of the photodiode current and destroys the operation of the circuit. Different circuit architectures will be required.

-T-switch configuration does not work for smaller technologies. Since T-switch configuration could reduce the leakage current of reset switch by few hundred of femto-amperes, it could not eliminate the whole leakage current for smaller technologies which also includes leakage current from the gate of MOSFET. Also proposed structure with 0.18um CMOS could not eliminate the whole leakage current of reset switch. The leakage current of reset switch of proposed configuration is calculated in Figure 3.13.

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APPENDIX A-DESIGN RULES OF MIM CAPACITOR TOP METAL [46]

CTM.I.3

No ViaTPO_1 under CTM region are allowed.

Suggestion:

Metal routing under MIM is allowed. Nonetheless, to place routing metal under MIM, it is strongly recommended to add a high frequency signal isolation metal layer under CBM. Customer should refer to TSMC PDK for better accuracy.

CTM.I.4

Recommended: Designer needs to take care of the impact of the noise coupling if any circuit or routing is put under MIM.

APPENDIX B-CODE FOR HISTOGRAM GRAPH

```
%
%
% Histogram for Estimating slopes Distribution of a pixel for 70 iteration of
Monte Carlo Process Simulation in Cadence
%
clear all
clc

slopes = [

0.0007810666 0.00081491 0.00082633 0.0008333 0.00083066 0.0008316 0.0008393
0.000825 0.00084166 0.00083366 0.000832 0.000835 0.000838 0.00084033 0.000848
0.0008383 0.00082733 0.0008506 0.00084833 0.000858 0.000848 0.0008496
0.0008496 0.000851 0.0008507 0.0008508 0.0008512 0.000839 0.000838 0.000842
0.000845 0.000847 0.000846 0.000843 0.000846 0.0008533 0.0008543 0.0008503
0.000864 0.000850 0.000857 0.000844 0.000857 0.0008282 0.000816233 0.0008223
0.00084533 0.00083666 0.00083433 0.0008426666 0.000844 0.00084433 0.000854
0.0008416 0.000846666 0.000836666 0.000854 0.000861 0.000831 0.000833
0.0008476 0.000856333 0.000852 0.000844 0.000849 0.000852 0.000844 0.000851
0.00085133 0.000852 0.00083866 0.000857 0.000854
]';



 stdv= std (slopes);
 mn=mean(slopes);
figure(1)
% nbins = ;
xvalues1_5 = 0.1e-03 : 0.007e-3 : 1e-3;
%subplot(2,1,1)
hist(slopes,xvalues1_5)
legend('Simulation')
title(' Slopes Distribution of subtractor output between the pixel with
IPD=30fA and pixel with IDark=0.5fA for 70 iteration
 ')
xlabel('Slopes (V/mSec)')
ylabel('Number of iterations')
axis([0.8e-3 0.9e-3 0  30])
h = findobj(gca,'Type','patch');
display(h)
set(h(1),'FaceColor','g','EdgeColor','k');
datacursormode on
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APPENDIX C-DESIGN SUBMISSION PROCESS

I had plan to submit my design for fabrication through CMC (Canadian Microelectronics Corporation) on August 2014, but CMC announced that the run has been postponed to November since they didn't have enough numbers of applicants for the run. Also the run of November has been postponed in two times and they are still waiting for more applicants to go for fabrication for TSMC 180 nm technology. The following email shows that my design has been accepted by CMC for fabrication.

10/21/2014 Print

Subject:	1401CF - Formal Allocations Delayed
From:	Sarah J. Neville (neville@cmc.ca)
To:	1401CF@cmc.ca;
Cc:	fab@cmc.ca;
Date:	Friday, October 17, 2014 10:11 AM

Good afternoon,

Applications have been reviewed by our Peer Review Committee for 1401CF and all applications were successful. We are withholding formal allocations however as this run is currently undersubscribed and we are awaiting for more researchers to join. Once we have reached the minimum requirements for this run, we will:

- Confirm allocated design dimensions
- Design Deadline (currently scheduled for December 3, however could shift into January 2015).

If you require additional information, or have any questions, please feel free to contact us.

Regards,

Sarah

Sarah J. Neville

This email is the discussion that I have with CMC after postponing the run:

From: Marzieh mehri <m_mehri65@yahoo.com>
Sent: Tuesday, November 11, 2014 10:21 AM
To: Sarah J. Neville
Reply To: Marzieh mehri
Subject: Re: TSMC 180nm

Since I will graduate during this year, the problem is timing . The submission deadline for this technology which was in August has been cancelled (I was supposed to share my chip with a student in August). The November deadline also has been deferred and I'm not sure if I could provide experimental results by end of my graduation with this technology run.

Thank you,
Marzieh

On Tuesday, November 11, 2014 6:57 AM, Sarah J. Neville <Neville@cmc.ca> wrote:

Just one question, can you please let us know what made you decide to withdraw – was it timing? Or something else?

Thanks,
Sarah

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From: Marzieh mehri [mailto:m_mehri65@yahoo.com]
Sent: Tuesday, November 11, 2014 9:52 AM
To: Sarah J. Neville
Subject: Re: TSMC 180nm

Here is the list of postponed Runs which has been announced by CMC (August which is also differed Run is not shown in the figure):