UNIVERSITÉ DE MONTRÉAL

HIGH-ACCURACY DIGITAL TO ANALOG CONVERTER DEDICATED TO SINE-WAVEFORM GENERATOR FOR AVIONIC APPLICATIONS

MASOOD KARIMIAN-SICHANY
DÉPARTEMENT DE GÉNIE ÉLECTRIQUE
ÉCOLE POLYTECHNIQUE DE MONTRÉAL

MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION
DU DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES
(GÉNIE ÉLECTRIQUE)
MAI 2013

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Ce mémoire intitulé:

HIGH-ACCURACY DIGITAL TO ANALOG CONVERTER DEDICATED TO SINE-WAVEFORM GENERATOR FOR AVIONIC APPLICATIONS

présenté par : KARIMIAN-SICHANY Masood
en vue de l'obtention du diplôme de : Maîtrise ès Sciences Appliquées
a été dûment accepté par le jury d'examen constitué de :

M. SAVARIA Yvon, Ph.D., président
M. SAWAN Mohamad, Ph.D., membre et directeur de recherche
M. THIBEAULT Claude, Ph.D., membre

To my mother,

for her inimitable love and patience

To my son, Amirali

ACKNOWLEDGEMENTS

I give my deepest thanks to God who guides me in such a wonderful way, instructs me whatever I understand, and helps me through inspiring people with whom I grow. Among those people, I am always thankful to my parents for their love and devotion. I cherish them.

It has been my honor to study and work in Montreal Polytechnique and Polystim laboratory. I would like to express my appreciation and respect to my supervisor, Professor Mohamad Sawan for his continuous support, guidance, and encouragement. This Master thesis could never have been completed without his help and advice.

I am also grateful to the members of the examining board of my Master thesis, Prof. Yvon Savaria and Prof. Claude Thibeault, for their feedbacks on this Master thesis and also on my progress in AVIO402 project during all these years.

During my program, I have been supported by postdoctoral fellows of Polystim laboratory. I would like to acknowledge Dr. Ali Naderi who technically supported and contributed in this work. My gratitude also goes to Dr. Saeid Hashemi for his invaluable help and encouragement. Moreover, I wish to thank Mrs. Marie-Yannick Laplante for her office support, Réjean Lepage for network and software administration, and all other students and technicians of Polystim, in particular Mona Safi-Harb, Amine Miled, Guillaume Simard, Faycal Mounaim, Sami Hached, Genevieve Massicotte, and Laurent Mouden for their support and providing friendly environment. I am sincerely grateful to my friend, Madjid Mokhtari, for his encouragement and heartfelt friendship.

I am truly indebted to my undergraduate teacher, Professor Saeid Sadri, and I would like to express my special thanks to him for his prodigious influence on my understanding methodology.

I would like to acknowledge financial support from Natural Sciences and Engineering Research Council of Canada (NSERC), Bombardier aerospace, Thales Canada Inc., MITACS, Consortium for Research and Innovation in Aerospace in Quebec (CRIAQ), and the products and services provided by Canadian Microelectronic Corporation, and Polystim neurotechnologies laboratory.

Last but not least, I want to thank my wife and my son for their being with me, support, and sacrifice during all these years.

RÉSUMÉ

De nos jours, malgré les avancées remarquables de la microélectronique, les systèmes avioniques emploient essentiellement des technologies vieillissantes afin de répondre aux normes de sécurité exigeantes des systèmes avioniques. La nouvelle génération d'avionique modulaire intégrée (AMI) des More Electric Aircrafts (MEA), nécessite des architectures de réseaux stables et fiables, employant des modules électroniques intégrables modernes qui restent à être conçus et développés. Suivant cette tendance, une interface générique intelligente pour capteurs (Smart Sensor Interface - SSI), dédiée aux capteurs de position avionique est proposée dans ce mémoire. Le circuit intégré SSI fera partie d'un réseau de capteurs AFDX amélioré et est composé de signaux d'excitation et de modules d'acquisition de données. Les efforts de conception sont concentrés sur l'unité de génération de signaux d'excitation (Excitation Signal Generation - ESG) de la SSI.

En tant que lien entre le réseau AFDX et les capteurs de déplacement, l'unité ESG doit générer des signaux sinusoïdaux précis, d'une fréquence allant de 1.5 kHz à 10 kHz. En respectant la programmation de l'interface, nous démontrerons qu'une architecture de générateur de signaux basée sur la mémoire est la seule option qui réponde aux objectifs du design.

Le design d'un convertisseur numérique-analogique (CNA) basé sur le principe du sur-échantillonnage et faisant partie du chemin ESG est également présenté dans ce travail. Ce CNA est le noyau d'un générateur de signaux sinusoïdaux versatile conçu pour le système SSI proposé. Un taux d'échantillonnage élevé est utilisé dans ce CNA, de façon à obtenir un rapport signal sur bruit (Signal to Noise Ratio - SNR) élevé. Une analyse de l'impact d'une implémentation carrée et non-carrée de la matrice de sources de courant (Current Source Array - CSA) sur la performance de la séquence de commutation est présentée. Il sera démontré que la considération de tels impacts conduit à la conception de CNA plus précis. Une séquence de commutation optimale pour la taille du CSA conçu, sera introduite. Afin de réduire la taille des plots d'entrées et de sorties de la puce, un convertisseur de données série à parallèle haute-vitesse est inclu dans le CNA. Ainsi, les données d'entrée peuvent être envoyées de façon sérielle à un registre à décalage et appliquées de façon interne au noyau du CNA. Le CNA a été fabriqué sur une puce d'une dimension de 1.2×1.2 mm^2 fabriqué avec la technologie IBM CMOS 0.13µm et est alimenté

avec une tension de 1.2 V. Générant un courant d'onde sinusoïdale ayant une valeur crête de 1023 µA, le CNA proposé permet d'obtenir un SNR plus élevé que 84 dB dans la bande passante Nyquist DC à 20 kHz.

ABSTRACT

Today, despite the astonishing advances in the field of Microelectronics, avionics systems are mostly employing older technologies to guarantee the level of reliability required by stringent safety standards of avionic systems. Toward the new generation of Integrated Modular Avionics (IMA) in More Electric Aircrafts (MEA), reliable and stable network architecture which employs modern integrated electronic modules must be designed and developed. In this trend, a generic Smart Sensor Interface (SSI) for avionics displacement sensors will be proposed in this Master thesis. The integrated SSI circuit will be part of an improved AFDX sensor network and consists of signal excitation and data acquisition paths. The design efforts of this Master thesis will focus on the Excitation Signal Generation (ESG) unit of the SSI.

As a link between AFDX network and displacement sensors, the ESG unit should generate pure and accurate sine-waveform with variable frequency between 1.5 kHz and 10 kHz. Respecting the programmability of the interface, it will be shown that a memory-based signal generator architecture is the only choice which supports the design objectives.

As part of the ESG path, the detailed design of a 10-bit interpolating digital to analog converter (DAC) will also be presented in this work. The DAC is the core of a versatile sine-waveform generator unit designed for avionics SSI. High-speed sample rate will be used in this segmented current steering DAC in order to achieve a high Signal to Noise Ratio (SNR). In the module level design of the DAC, the impact of square and non-square implementation of the current source array (CSA) on the performance of the switching sequence is introduced. It will be shown that considering such impacts will lead to the design of more accurate DACs. An optimum switching sequence for the designed CSA size will be designed and introduced. In order to reduce the I/O pads of the chip, high-speed serial to parallel converter will be included in the DAC. Thus the input data can be serially sent to the input shift register and internally applied to the DAC core. The DAC was fabricated on 1.2 × 1.2 mm^2 chip fabricated using IBM 0.13µm CMOS technology, operating with a supply voltage of 1.2 V. Sourcing a sine wave current with a peak of 1023 µA, the proposed DAC is able to achieve a SNR better than 84 dB in the Nyquist bandwidth of DC to 20 kHz.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS AND SYMBOLS

Abbreviations:

ACS	Avionics Computer System
ADN	Aircraft Data Network
AFDX	Avionics Full Duplex Switched Ethernet
AFDXES	AFDX End System
ARINC	Aeronautical Radio, Incorporated
ASIC	Application-Specific Integrated Circuit
ASP	Analog Signal Processor
CAN	Controller–Area Network
CMOS	Complementary Metal-Oxide-Semiconductor
CSA	Current Source Array
CSDAC	Current-Steering Digital to Analog Converters
DAM	Data Acquisition Module
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ES	End System
ESG	Excitation Signal Generator
FAA	Federated Avionic Architecture
FBW	Fly-By-Wire
FCC	Flight Control Computer
FCS	Flight Control System
FPGA	Field Programmable Gate Array
IMA	Integrated Modular Avionics
ISS	Integrated Sensing System
LRU	Line Replaceable Unit
LSB	Least Significant Bit
LVDT	Linear Variable Differential Transformer
MEA	More Electric Aircraft
MEMS	Micro-Electro-Mechanical Systems
MOS	Metal-Oxide-Semiconductor

MSB	Most Significant Bit
MTBF	Mean-Time Between Failure
NCAP	Network Capable Application Processor
NMOS	N-type Metal-Oxide-Semiconductor
OSR	Over Sampling Ratio
PMOS	P-type Metal-Oxide-Semiconductor
RTC	Remote Terminal Cluster
RVDT	Rotary Variable Differential Transformer
SCSDAC	Segmented Current-Steering Digital to Analog Converters
SD	Standard Deviation
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SSI	Smart Sensor Interface
TAI	Transducer Analog Interface
TEDS	Transducer Electronic Data Sheet
TIM	Transducer Interface Module
TMI	Transducer Measurement Interface
TRL	Technology Readiness Level

CHAPTER 1

INTRODUCTION

1.1 Project overview

This research has been performed in the content of a three years collaborative research and development project (AVIO402) which includes analysis, design, and implementation of several solutions to improve the actual devices interconnection in aircrafts such as sensor and actuator interfaces to data buses. These subjects are key issues related to the technological development plan of industrial partners, Thales Canada Inc. and Bombardier Aerospace Inc., for next generation avionic systems. This topic also represents one of the main priorities of the Consortium for Research and Innovation in Aerospace in Quebec (CRIAQ), which supports this project partially. The overall program objective consisted in 1) development of new sensor/network interface and new position sensors for avionic applications, 2) development of less-wired solutions for safety-critical data communications, and 3) study on frequency selection and EMC/EMI for civil airborne wireless communication systems [1].

High channel count sensor and actuator devices are needed to tackle a growing number of functions in aircrafts. With traditional avionics technology, connecting these devices results in bulky wiring bundles. The stringent safety standard of avionic systems requires redundant installation of all components on board, which further exacerbates the situation. Moreover, in new avionic systems, communications between devices across different application domains are also needed, which drastically increases information flow within the aircraft. Wiring bundles and demand for a much higher communication bandwidth raise serious challenges requiring the development of new avionic data buses [2,3].

The main project tackled solutions to build new avionic systems being able to meet stringent requirement in flight safety-critical operations, such as flight control. The research consisted of

three complementary parts: 1) autonomous sensor and actuator/network interfaces, 2) safety-critical data buses, and 3) frequency selection for wireless communications on board aircraft. Each of these main subjects has been resulted in an appropriate architecture to facilitate reliable interconnection and interoperation [1].

The operation of Fly-By-Wire (FWB) flight control systems relies heavily on position sensors for detecting pilot controls, actuators displacement, and control surfaces movement. The sensors currently used in most such systems are fully analog and passive based on electromagnetic principle or more specifically the Rotary/Linear Variable Differential Transducer (R/LVDT) technique [4,5,6,7]. It is therefore of great interest to connect sensors to high performance standard digital avionics data buses and to render them intelligent, autonomous, and situation-aware. In responding to these technological challenges, this project aimed at developing a new avionics communication network allowing a reduction of the complexity of cabling by adopting a smaller wire-count solution, using data buses with higher overall throughput than current systems. Digital interfaces were also developed to connect legacy position sensors and actuators to data buses. Furthermore, MEMS (Micro-Electro-Mechanical Systems) and photonic technologies have been explored to develop new lightweight, contactless, and highly reliable position sensors for replacing the current state of the art in order to provide enhanced performance while reducing the cost of deployment and maintenance. Based on the research results, the Avionics Full Duplex Switched Ethernet (AFDX) has been proposed as a baseline network architecture. This would achieve a solution for avionics data networks combining throughput, architecture adaptability, and secure and safe digital data stream with reliable time determinism, bounded latency, guaranteed bandwidth, and fault tolerance suitable for safety-critical applications. The adoption of this architecture facilitated the integration of low cost and/or legacy avionics data buses. The AFDX provided also means to connect avionics subsystems to other segments within an Aircraft Data Network (ADN) [1].

There are several standards such as [2] that outline the environmental constraints and test procedures of airborne equipments. The outcome of this project is being validated with a widely adopted standard in aerospace industry for new technology assessment, namely the Technology Readiness Levels (TRLs). More specifically, the development of sensor/network interfaces and safety-critical data buses should reach TRL4 (prototypes validation in the laboratory) [8]. This approach allows the project to be seamlessly integrated into engineering development processes

of the supporting industrial partners facilitating transfer to industry. The research work is split into the following three areas [1].

1.1.1 Sensor/network interfaces and new position sensors

As shown in Figure 1.2, a sensing system is basically composed of one or more sensors and/or actuators, an interface block, and a data processor. A sensor network includes a group of sensing systems which are connected together through a communication infrastructure. If the sensor and the interface block are implemented in a single housing, the resulting module is called a *smart sensor*. This module usually includes an analog front-end, an analog to digital converter (ADC), and a bus interface. By integrating all these components in one chip, an "integrated smart sensor" is obtained [9,10,11].

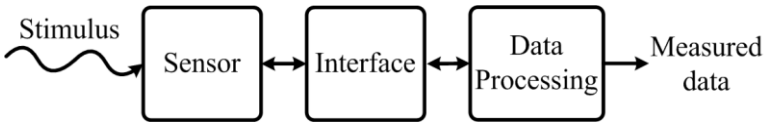


Figure 1.1: General diagram of a sensing system

The objective of the research on this theme aims specifically at making autonomous smart sensors to replace existing position sensors in flight control systems. The proposed Smart-Sensor Interface (SSI) will be designed and implemented with state-of-the-art CMOS technologies. Also, special attention has to be paid to the reduced-interconnection complexity. It must fit all types of proposed position sensors in this project. For solutions capable of replacing existing position sensors, this project also aims at developing novel, cost effective, and reliable devices for absolute angular position measurement of rotational components based on photonics and MEMS technologies. The new sensors should be compatible with the digital interfaces and be interchangeable with other sensors relevant to this project [1,10].

1.1.2 Safety-critical avionics data network

The project proposes a dual-protocol multi-rate avionics data bus with AFDX/ARINC 664 as the baseline network architecture and ARINC 825 as the framework for the field bus. The main objectives related to this theme include the establishment of system architecture, the development

of applications of AFDX switch and end systems (ES), interfacing to the main network and the field buses, the development of cross-domain communications mechanisms, and the integration of sensors/actuators with flight computational units via the new data network. Considering that AFDX standard tackles only few explicit reliability aspects, the integration of reliability features is studied elegantly to match the needs of flight safety-critical applications. In particular, to characterize, analyze, and evaluate the level of performance and criticality of various functionalities, fault models are built. Based on this characterization, issues like architecture and modes of operation including maintenance and fault containment will be addressed [1].

1.1.3 Frequency selection for safety-critical wireless communication systems

The objective of this theme is to propose a solution for the avionics wireless data bus. The radio-frequency hardware implementation of such a system should maximize immunity to intentional and unintentional emitters present in the environment and at the same time, minimize disturbances to other aircraft systems, as well as ground equipments. As with the currently available technology, it is extremely difficult to build wireless avionics networks which can meet the stringent requirements for flight safety-critical systems alone, the emphasis is placed on the property of determinism with guaranteed bandwidth and bounded latency. Such a system offers a means for backing up wired data buses, constituting an emergency system in case the wired communications with critical terminals are totally lost, and hence, it further enhances the safety level of avionics data networks. To achieve the objective, research will be carried out on the identification of frequency bands of operation causing the least EMC/EMI issues [1].

1.1.4 Project organization

The adopted architecture and communication standards are key points for the successful system development. Ultimately, the choice of communication standards may be driven more by factors such as life cycle costs, maintainability, upgradability, expandability, compatibility, and certification. They also determine the architecture with which sensors, actuators, and other electronic components interconnect and interoperate. To meet these criteria, the architecture in Figure 1.2 has been proposed for the new avionics data network addressed in this project [1].

As shown in Figure 1.2, the AFDX is the backbone of the network and all sub-systems are connected via AFDX End Systems. Sensors and actuators, as well as Transducer Interface Module (TIM), are geographically close to each other within each Remote Terminal Cluster (RTC). The components in a RTC are connected to a field bus, e.g. ARINC 825, and communicate with the AFDX network via a Network Capable Application Processor (NCAP), composed of a data concentrator and an AFDX ES, through which the data flow over the field-bus. The Flight Critical Computer (FCC) can be a single computational component or a partition of a central computational unit in an Avionics Computer System (ACS) [1,12,13].

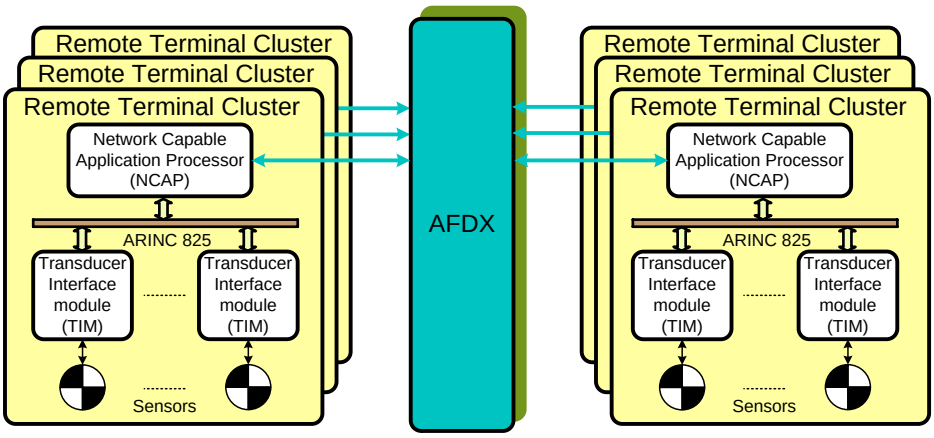


Figure 1.2: System architecture of avionics data network in AVIO402 project

Due to its multidisciplinary nature, this project required a joint effort of the co-applicants having expertise in different areas and a close collaboration and coordination with the supporting organizations at every stage of the project. More specifically, this project consisted of eight tasks:

Task 1: Smart sensors interface (SSI) which is the subject of this Master thesis

Task 2: Generic network interface wrapper

Task 3: Photonic position sensor

Task 4: MEMS position sensor

Task 5: Network architecture, cross-domain communications, adaptation to flight control applications, and QoS enhancement

Task 6: Development of AFDX ES applications, integration of field-bus and RTOS, and system level testing

Task 7: Reliability modeling, architecture for fault handling, and fault management at both hardware and software levels

Task 8: Frequency selection for wireless communications on board aircraft, aspect EMC/EMI

1.2 Motivation

Employing high speed, high throughput data bus structures and new sensor technologies in avionics sensor networks forces using a universal, reliable, and flexible interface which should reduce the interconnection complexity of the network. The development of sensor technology has resulted in new types of sensors with increasing accuracy and reliability, smaller size and lightweight, contactless, less power consumption, and simplified integration possibility with electronic circuits. In order to use different sensor technologies at the same time, a SSI circuit with an adaptive front-end is essential. With regard to capabilities of state-of-the-art CMOS technologies, it is of great interest to construct a fully integrated sensor interface [1,11].

It has been shown that IEEE-1451 (smart transducer interface standard [12,13]) can be used in aerospace field to reduce wiring and complexity [14,15]. The proposed architecture of the SSI in AVIO402 is shown in Figure 1.3 in which the SSI is part of a TIM introduced in IEEE-1451. The TIM is connected to a field bus such as the Controller Area Network (CAN) and communicates with the AFDX network via a Network Capable Application Processor (NCAP) [16]. The SSI is used for activating and signal conditioning of different position sensors. The proposed modular architecture can also handle a diversity of sensors and actuators, as well as the digital interfaces within an avionics system. In fact, the SSI module should be designed as a generic bridge that easily adapts to a wide range of sensors, actuators, and other modules and to a pair of field bus such as ARINC825 [17].

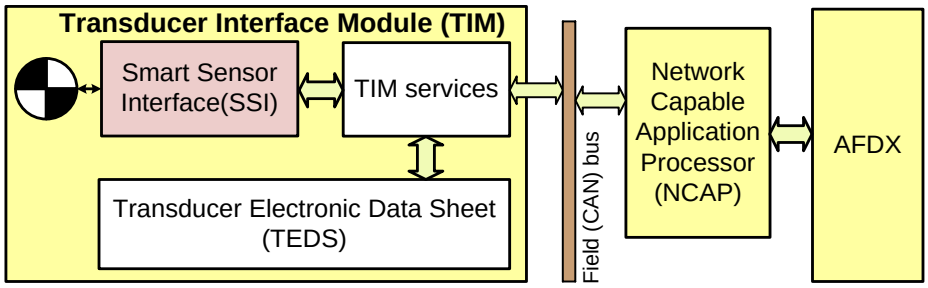


Figure 1.3: Architecture of modified AFDX network along with the SSI

The proposed architecture of the SSI is shown in Figure 1.4 which consists of different signal paths, from sensor to network and vice versa. The sensor output feeds forward throughout an analog signal processing scheme and then is digitized using a high precision analog to digital converter and a ratio-metric unit. Afterward, the sensor data is forwarded to TIM services through Transducer Measurement Interface (TMI). The feedback path generates the excitation signal for sensors based on the amplitude and frequency information provided by the incoming data from network and adapts its level to the operating range of the sensors [1,17,16].

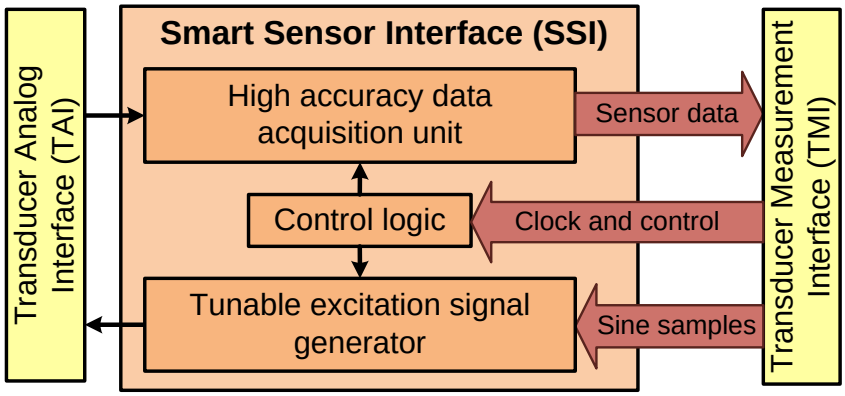


Figure 1.4: Architecture of the proposed SSI

The Excitation Signal Generator (ESG) path links the avionics AFDX network and the position sensors. With reference to the specifications of legacy R/LVDT position sensors, it generates a sinusoidal signal with voltage levels adapted for actuating the sensors.

Considering the circuit complexity of the SSI, in this Master thesis we have focused on the design, implementation, and characterization of the ESG unit. Although there are several solutions for low-frequency sinusoidal waveform generation, a new architecture for the ESG unit should be carefully designed in order to adhere to the requirements of the proposed SSI block

diagram. The new ESG should be programmable and can be integrated with other blocks within the SSI. Before proceeding to the literature review and design of the ESG, basic principles of displacement sensors and their interfacing requirements are described.

1.3 Basic principles of displacement sensors

The increasing applications of sensor networks and sensing devices have resulted in numerous implementation techniques. In aircrafts and avionics systems, various types of sensors and actuators are employed in order to prepare critical data for Flight Control Computers (FCC). Therefore, reliable, precise, accurate, and highly-sensitive sensors with a very long Mean-Time Between Failures (MTBF) are required to meet stringent safety standards for avionic applications. R/LVDT displacement sensors are based on Variable Differential Transformer technique and operate wear-free. They exhibit excellent linearity and resolution, possess long lifetime, and measure over a large spectrum. Hence, they perfectly comply with avionic safety standards and are widely used in flight data acquisition and servo control [2,4,11].

To clarify the terminology, *position* of an object is its linear or angular coordinate with respect to a selected reference. In contrast, *displacement* means the specific linear or circular movement of an object from one position to another. In other words, a displacement is measured by sensing the amount of motion of an object with reference to its own prior position rather than to another reference [11].

With respect to the quality and the performance of displacement sensors, they are employed to measure not only the displacement, but also some other stimuli such as force and pressure. In these cases, the stimulus should be first converted to displacement and then accurately measured by a variety of R/LVDT sensors. As an example of pressure sensing, the pressure variation could change the position of a diaphragm. Using an R/LVDT sensor, the displacement of the diaphragm can be then converted into an electrical signal representing pressure [11,18].

In order to benefit the level of performance of R/LVDTs, a highly accurate and precise sensor interface circuit is a vital requirement in the navigation of air vehicles. In this section, the physical structure and operation principles of R/LVDTs as well as the architecture of the interface circuit are briefly described.

1.3.1 LVDT and RVDT inductive sensors

The Variable Differential Transformer (VDT) technique is based on the magnetic flux coupling between two or three coils which can be altered by a moving ferromagnetic core. The coils are arranged as one primary and two equally spaced, identical secondary ones. Upon exciting the primary coil with a sine waveform current and depending on the position of the core, an AC voltage is induced in the secondary coils. The core is connected to the object whose displacement is to be measured. The amount of core displacement can be extracted from the secondary signals. The sensors which use this technique are also called variable-reluctance transducers because the movable core alters the reluctance of the flux path [11].

The LVDT and RVDT electromechanical transducers use the VDT technique and are considered as magnetic or inductive type displacement sensors. When the primary coil is excited, the carrier signal is induced in the secondary coils with the same frequency contents as the excitation signal. Therefore, a pure sine wave excitation signal eliminates harmonics in the transformer and prevents errors. The movement of the ferromagnetic core within the flux path is modulated over the amplitude of the carrier signal of the secondary coils. As shown in Figure 1.5, the mechanically actuated core is coaxially inserted into a cylinder structure on which the coils are wound. The core does not physically touch the coils and thus there is no or very little friction. Being designed on the same principles as LVDT, the RVDT is capable of measuring angular displacement by using a rotary core [11,18].

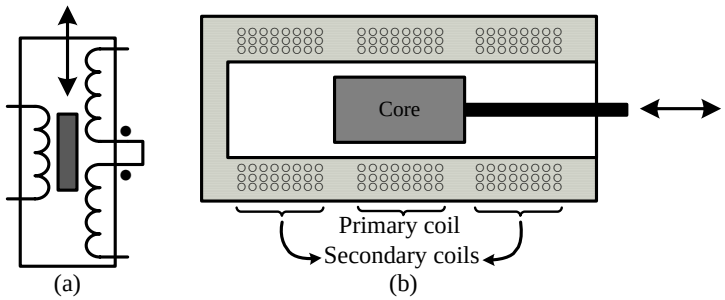


Figure 1.5: (a) LVDT electrical diagram (b) LVDT physical cross section

In general, the two secondary coils are connected in opposite phase. So, the output of the sensor is the difference between the individual secondary voltages. Assuming fully symmetrical secondary coils, as long as the core is held in the magnetic center of the sensor, the summation of

the two output voltages remains zero. Any movement of the core toward the endings of the cylinder unbalances the secondary voltages which results in a non-zero output. In fact, the movement of the core alters the reluctance of the flux path that results in variation of the induced voltage. Hence, the amplitude and phase of the output signal represent the displacement and its direction, respectively. Obviously, the displacement information is valid in the linear operating range of the sensor [11].

The following advantages discriminate the R/LVDTs from other types of displacement sensors: (1) the penetration of any nonmagnetic material in the magnetic field generated by the primary coil, results in no loss of accuracy; (2) to be used in harsh environments and corrosive situation, R/LVDTs can be coated with inert material. Such coating does not affect the measurement; (3) as a desirable mechanical feature, there is no or very little friction or wear resistance; (4) magnetic and mechanical hysteresis is negligible; (5) in theory, the sensitivity of the sensor is infinitesimal; (6) the output impedance is very low; (7) the mechanical structure is solid and robust and they can measure over a large spectrum of displacement; (8) these transducers are static sensors. This means that their response is not a function of time [2,11,18,19].

With respect to the above-mentioned advantages, there are a variety of applications for these rugged and versatile sensors. They are employed in jet engines and hot-slab mills in order to measure force and pressure [18]. In Idaho National Engineering Laboratory (INEL), the LVDT is used to measure the elongation of the nuclear fuel rod which is an indication of critical heat flux [20]. In medical applications, authors of [21] directly placed a LVDT over the hand vein to measure the variation of its diameter (ranging from 0.8 mm to 1.4 mm) due to norepinephrine infusion. An example of a different exploitation, LVDT is used in a horticultural study in order to measure the variation of the diameter of pepper plants [22]. In addition, these transducers are widely employed in aircrafts and avionics systems including flight controls, thrust reversers, steering feedback, and landing gear [3,18,23,24,25].

1.3.2 LVDT and RVDT interfacing

Considering Figure 1.1, any interfacing circuit should be faithful to both the sensor and the data processing module. With regard to the infinitesimal sensitivity of R/LVDTs, the resolution of the

sensing system is determined by the specifications of the interfacing electronics. Thus, the design of an interface for R/LVDTs sensors is more challenging compared to other types of sensors [11].

R/LVDTs are classified as passive sensors. This means that an external source of energy is required for the operation of the sensor. Therefore, any R/LVDT interfacing circuit should include two major modules: (1) an Excitation Signal Generator (ESG); (2) a Data Acquisition Module (DAM). The ESG output should drive the sensor with a sine waveform of proper frequency and amplitude. On the other hand, the sensor output should be conditioned by front-end circuit and the DAM in order to be compatible with data processing system [11,25].

For proper excitation of primary coil, a stable sine wave generator is required in the ESG. The advantage of sinusoidal excitation signal is that proper filtering increases the achievable Signal to Noise Ratio (SNR). Nevertheless, generation of sine waveform needs more complex circuit and consumes higher power in comparison with square-wave or pulse signals. The frequency of the sine is determined by the movement speed. To accurately extract movement data, the sine frequency (the carrier frequency for amplitude modulated data) should be at least 10 times higher than the highest possible movement speed of the sensing stimulus [11]. Thus, different applications impose various sine frequencies. As a result, the adjustability of the excitation frequency is a preliminary consideration in the design of a generic SSI. According to the key features of most R/LVDT sensors and general specifications of commercially available R/LVDT signal conditioners, the sine wave output of the ESG should cover the frequency and amplitude range of 1 kHz to 20 kHz and 1 V_{rms} to 10 V_{rms}, respectively. The maximum required excitation current is 20mA [9,26,27,28,29].

In the data acquisition path of the interface, the sensor output might be too weak and noisy with undesirable interference signal components. Therefore, the analog front-end must have a very low noise figure and should be linear for the wide dynamic range of sensor output signal. High order low pass filter with a sharp cut-off knee is also needed to discriminate the data from the carrier signal. A high-resolution and high-accuracy ADC should then digitize the sensor output signals for further processing [1].

1.4 Research objectives and challenges

Keeping the SSI architecture of Figure 1.4 in mind, the following goals have been considered in this work:

- First and foremost, the frequency and amplitude of the excitation signal should be determined via the TMI. This feature guarantees the configurability of the SSI. The acceptable frequency and amplitude range for most of the Legacy R/LVDT sensors varies from 1 kHz to 10 kHz and from 1 V_{rms} to 7 V_{rms}.
- The proposed ESG should be designed based on CMOS technologies in order to make the integration of the SSI possible.
- To support one of the essential goals of the main project, the number of input/outputs between ESG and the TMI should be minimized. This feature not only decreases the required wiring connections, but also facilitates the integration of the SSI and the TMI.
- In order to drive legacy R/LVDT position sensors, the final output of the ESG should provide sufficient drive capabilities. In addition, the acceptable range of excitation signal amplitude of most legacy sensors is not fully attainable in nanometer CMOS technologies. Thus, additional circuitry should be considered in the last stage of the ESG.
- To minimize the power consumption, the designed ESG must maximize the power efficiency. Since the excitation signal is better to be of current type, this feature can be achieved by current-mode designing of main blocks.

Established goals and objectives confront with various challenges in the design, implementation and integration procedures. Any ESG architecture and specification should comply with the SSI and support the required systematic specifications. Therefore, more parameters must be taken into account in the design of ESG. Moreover, with reference to the low frequency operation of the ESG, smoothing filters may need large capacitors and/or resistors which either are not available in CMOS technologies or may impose very large or unacceptable die area.

Proper operation of data acquisition unit is tied to the accuracy and purity of the sine-wave excitation signal. Hence, the accuracy and precision of the ESG output along with the

programmability of the frequency and amplitude is yet another challenge which should be tackled in the systematic and circuit level designs.

The last challenge that faces this design is the incorporation of low voltage circuits in nanometer CMOS technologies with the required high voltage amplifier blocks as the last stages of the ESG. Achieving this goal imposes the usage of some off-chip blocks in order to drive the sensors with appropriate signal level.

1.5 Contributions

In view of the objectives that are considered and the mentioned challenges, the following contributions have been made:

- A new ESG unit has been designed which can be integrated along with a data acquisition unit in order to constitute a system-on-chip SSI module for the avionics applications. The proposed ESG architecture is fully compatible with the TIM services and configurable through the TMI block in the improved AFDX network. The whole SSI module is to be used as an important part in next generation avionics data networks which facilitate the transition of a Federated Avionic Architecture (FAA) to an Integrated Modular Avionics (IMA).
- Moreover, in chapters 3 and 4, a new parameter in the design of Segmented Current-Steering Digital to Analog Converters (SCSDAC) has been introduced. According to the simulations the performance of the switching sequence in SCSDACs depends on the physical realization of Current Source Array (CSA). To further investigate this effect, a new programmable CSA chip has been designed, laid out and submitted for fabrication. Provided that the measurement results confirm the simulation results, the choice of switching sequence should be based on the aspect ratio of the CSA. In this case, further investigation is needed to design a generic efficient sequence for specific ratios between the length and the width of the laid out CSA.

1.6 Thesis outline

The development of a programmable excitation signal generator unit within a SSI module for avionics applications shall be the subject of this work. The Master thesis is organized in four chapters and a conclusion. Following this brief introduction, the specifications of the desired smart-sensor interface as well as literature review will be presented in chapter two. Chapter three discusses the ESG design procedure in system and circuit levels. Additional details along with simulation and measurement results have been provided in chapter four. The conclusions and outcome drawn from this research are explained in the final chapter which also includes some future directions for circuit designs and system-level integration.

CHAPTER 2

BACKGROUND ON EXCITATION SIGNAL GENERATION AND R/LVDT INTERFACING

2.1 Introduction

The purpose of this chapter is to review the published articles and commercial interfacing solutions and excitation signal generation methods for R/LVDT displacement sensors. This brief survey as well as fundamentals of R/LVDTs presented in chapter one, help the readers to better understand the topic of this Master thesis.

In the first step, the benefits and challenges of smart and integrated sensing systems will be discussed. To cover our application, we have then focused on commercially available solutions which can drive legacy displacement sensors and demodulate their outputs. Several papers with the same topic will also be presented. Afterwards, the published methods of excitation signal and sine waveform generation will be discussed. Finally, with reference to our selected architecture for realization of the ESG, the design of the Current-Steering Digital to Analog Converters (CSDAC) will be reviewed.

2.2 Integrated sensing systems

Since the late 1970s when the Fly-By-Wire (FBW) flight control systems came into use, the aerospace industry has evolved toward designing More Electric Aircrafts (MEA) instead of relying on conventional hydraulic, mechanical, and air/pneumatic avionics systems. The MEA approach has improved the efficiency, reliability, and maintainability of avionics systems. It has also resulted in lighter aircrafts which can lead to reduced fuel consumption in a highly competitive market [30,31].

In support of this trend, Integrated Sensing Systems (ISS) has been developed in order to miniaturize, reduce the cost, size, power consumption, and weight of the sensor systems. Sensing,

signal conditioning, analog to digital conversion, bus interfacing, and data processing are main functions of any ISS. Hence, the ISS may include the sensor, amplifier, Analog to Digital Converter (ADC), buffer, and bus interface. To further improve the quality of the system, built-in self-testing, auto-calibration, and data evaluation modules can be integrated in ISS. Depending on the integration compatibility of the sensor and the allowance of the technology, different levels of integration are expected which are shown in Figure 2.1 [9]. On the other hand, a set of smart transducer interface standards named IEEE-1451, have been developed to standardize different solutions for connecting sensors and actuators to instrumentation systems [12,13].

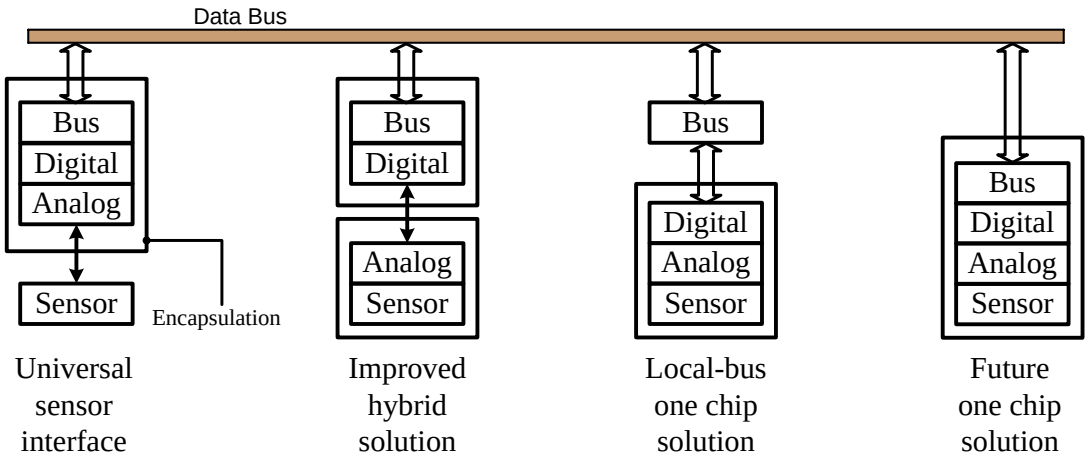


Figure 2.1: Several types of integrated sensing systems

ISS is associated with numerous benefits and challenges. Sharing of multifunction modules, common module production, canceling the effects of cable and wire impedances, and employing mature technologies in robust and reliable designs are major strong points of this design methodology. Moreover, ISS facilitates the succession of integrated modular avionics and reduces the amount of equipment installed on the aircraft. At the same time, it increases the efficiency of communication between coupled functions. However, there are some challenges in the top-down and bottom-up ISS design approaches. The high cost of integration will be reasonable only in case of mass production. In other words, the size of the market determines the level of integration of sensing systems. Another negative aspect is that the integration must be consistent with the required level of redundancy in order to maintain the desired reliability. Also,

the parasitic electrical effects on the sensing elements should be carefully taken into account [9,32,33,34].

2.3 L/RVDT integrated interfacing

Using discrete electronic components and designing Application Specific Integrated Circuit (ASIC) are two traditional solutions to interface L/RVDT sensors [35]. With respect to Figure 2.2, the system and circuit level designs of the ESG and the DAM should be consistent and uniform in any integrated interface solution (will be referred as SSI in this Master thesis) for L/RVDT sensors. Besides, the specifications of each module should be determined with regard to those of the other module. In other word, the required performance of each module depends on the desired characteristics of the whole interface as well as the specifications of the other module. As an example, generation of a highly-precise, high-SNDR sine waveform in the ESG decreases the order of filter in the DAM.

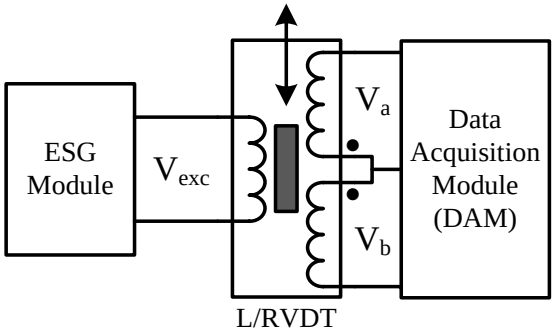


Figure 2.2: L/RVDT interface modules

In a fully integrated SSI, the integrability of the ESG and the DAM is the most important requirement. Another obligation is that the frequency and amplitude of the excitation signal must be set by the TMI which is part of the TIM introduced in IEEE-1451 [16]. Since the TMI is a digital block, the proposed design of the ESG should be able to receive the sine waveform parameters through a digital signal. Considering the commercial displacement sensors and respecting the AVIO402 demands, the ESG must generate a sine waveform in the frequency range of 1 kHz and 10 kHz with an accuracy of 1%. Since the information bandwidth is rather small in L/RVDTs, multiple measurements can be performed in the desired frequency range.

Thus, 30 different excitation frequency channels have to be covered by ESG. In the DAM, sensor output signals should be conditioned, filtered and averaged for further analog or digital signal processing. Moreover, each sensor channel should be filtered from the other channels to avoid cross talk between neighbor sensing systems [1,26,28,29].

Interfaces designed by fully analog electronics, suffer poor long-term performance, comprise many components, and are hard to adjust. They also lack the communication with computers and microcontrollers. Programmable digital and mixed-signal circuits are used in newer interfaces. Drumea et al. [36] have used MSP430F149 microcontroller (MCU) produced by Texas Instruments, to bring together data conversion blocks, timer, digital memory, and PWM module. On-chip 12-bits ADC, comparator, timer, Universal Synchronous-Asynchronous Receiver-Transmitter (USART), as well as ultralow-power consumption, and built-in memory make it a powerful target for this application. One of the timers can generate a pulse-width modulated (PWM) signal which is filtered to produce a sine waveform. This stable 5 kHz sine signal is then buffered by two external operational amplifiers to source the required excitation current to the primary coil of the sensor. A discrete differential amplifier is then used to apply the sensor output signals to the ADC of the MCU. Using external DAC and/or RS232 interface, the displacement value can be sent to other systems. This interface electronics has been fabricated on a two layer PCB with 50 x 40 x 20 mm dimensions. Although the interface precision is reported to be ±0.3% with a calibrated algorithm, it has been only connected to a special LVDT built by Research Institute for Hydraulics and Pneumatics. A fixed sine frequency and no measured data on the quality of the sine is another weak point of this report. On the other hand, this MCU cannot be integrated with the TMI and the TIM services which further limit our design strategy.

STM32F103RC MCU from STMicroelectronics is used by Wang et al. in [35] in order to design an intelligent acquisition module for differential transformer position sensors. In this architecture, a sine-wave memory inside the MCU sequentially sends the sine samples to the on-chip 12-bits DAC. Two off-chip operational amplifiers filter and buffer DAC output and excite the sensor. Sensor output signals are then amplified or attenuated (depending on the signal level) and applied to the MCU through a matching circuit. In addition to the sine-wave generator and signal acquisition units, the MCU realizes signal processing, calculation, calibration, and communication modules. Although [35] is a complete L/RVDT interface and the authors have claimed that it generates pure sine-wave, no measurement result has been reported. Besides, it has

the same drawback as [36] in integrating MCU in the NCAP in order to centralize interface control module. Nevertheless, the idea of using a digital sine-sample memory has been used in our design which will be discussed in chapter 3.

In another similar approach, PCI1716 card from Advantech is configured as a powerful data acquisition module for L/RVDT sensors in [37]. It can receive 16 single ended or 8 differential channels. The complete data acquisition system contains the PCI1716, the PCLD-8710 wiring terminal board, and an Industrial PC (IPC). The PCI card includes 16-bits ADC, 1024 samples FIFO, 32 digital inputs and outputs, and 2 analog output channels with 20mA driving capability. 0.01 mm is the best achieved precision in this user-friendly and software programmable interface, however, it is not a proper solution for avionics application due to the cost, non-integrability, size, and required wiring connections.

Canu et al. [38] have presented a versatile input interference for avionic computers. Their general interface solution fills the requirements of four types of most common input and outputs of avionic computers: (1) discrete Input Vdd/Open; (2) Discrete Ground/Open; (3) L/RVDT acquisition; (4) ARINC429 receiver. Drastically decreasing the complexity of I/O boards, it results in more flexible interface boards that occupy less physical area in avionic computers. Unfortunately, this generic solution only interfaces L/RVDTs to the computer and cannot generate the excitation signal or perform any data processing scheme.

There are few commercially available signal conditioner subsystems for L/RVDTs. Analog Devices single chip solutions, AD598 and AD698, convert sensor signals to an accurate unipolar or bipolar DC voltage proportional to the physical displacement. Both chips need a few external passive components to set the signal conversion gain and excitation signal (V_{exc}) frequency and amplitude [39,40]. They can drive the sensor primary coil with an excitation sine in the frequency range of 20 Hz to 20 kHz and up to $24V_{rms}$. Total harmonic distortion of the sine is claimed to be -50 dB. Being set by external resistors and capacitors, the amplitude and frequency of the excitation signal as well as the gain of the chip will be fixed and cannot be programmed. Moreover, any inaccuracy or temperature drifts of passive components cause amplitude and frequency distortion in V_{exc} and output voltage. The outputs of AD598 and AD698 are calculated based on Eqs. (2.1) and (2.2), respectively.

$$\frac{V_a - V_b}{V_a + V_b} \tag{2.1}$$

$$\frac{|V_a - V_b|}{V_{exc}} \tag{2.2}$$

where V_{exc} is the excitation voltage and V_a and V_b are secondary voltages of the L/RVDT, as shown in Figure 2.2.

In Eq. (2.1), it is assumed that $(V_a + V_b)$ is a fixed value which should be measured and used as a parameter in the design procedure. However, this term is proportional to the V_{exc}. Thus, any variation of excitation voltage will cause nonlinearity in the displacement measurement. In the AD698, the direction of the displacement cannot be detected because of using the absolute difference value between sensor outputs in the numerator of Eq. (2.2). Consequently, AD598 and AD698 cannot be employed in our application due to their non-integrability and non-programmability.

Several manufacturers produce different models of L/RVDT signal conditioner units which perform excitation, amplification, demodulation, signal modification, and readout [27,41,42,43]. Table 2.1 summarizes the specifications of these models. They can be employed in many industrial instrumentation applications to excite various L/RVDTs and detect their output signals. However, there are many incompatibilities in using them within avionics systems. They are not compatible with IEEE-1451 since they cannot be configured by a centralized control block. The excitation signal frequencies are also limited and cannot be digitally controlled. Additionally, the outputs are in the form of analog voltage and/or current signals. No analog to digital convertor has been provided in these products. Non-integrability and large physical dimensions are other factors which makes them improper for our application. Nonetheless, the presented specifications clarifies and justifies our selected objectives and design parameters stated in chapter one.

In summary, any solution for avionic sensing system and its building blocks should be integrable and programmable in order to be used in IMA systems. With respect to the development of sensor network architectures in MEAs, it must also be versatile and compatible with a centralized control system and/or network gateways. In the rest of this chapter, we will focus on the different methods used in design and realization of a sine waveform generator as the core of the ESG.

Table 2.1: Specifications of commercial L/RVDT signal conditioners

Brand and Model		Line power	Detected Output	Excitation Signal			
				Waveform	Frequency	Amplitude	Current
Measurement Specialties	ATA 2001	115/220 VAC (50 ~ 400Hz)	● Unipolar (0 ~ 10 VDC) ● Bipolar (0 ~ ±10 VDC) ● Current (4 ~ 20 mA)	PWM shaped sine	2.5, 5, 10 kHz[1]	0.5 or 3.5 V_{rms}	Up to 45 mA_{rms}
	IEM 422	115/220 VAC	Current (4 ~ 20 mA)	Sine	2.5, 5, 10 kHz[1]	0.5 or 3.5 V_{rms}	Up to 25 mA_{rms}
	LDM 1000	10 ~ 30 VDC	● Unipolar (0 ~ 10 VDC) ● Bipolar (0 ~ ±5 VDC) ● Current (4 ~ 20 mA)	Sine	2.5, 5, 10 kHz[1]	1 or 3 V_{rms}	Up to 25 mA_{rms}
	LiM 420	18 ~ 30 VDC	Current (4 ~ 20 mA)	Sine	2.5 kHz	3.5 V_{rms}	Up to 20 mA_{rms}
	LVM 110	±12 or ±15 VDC	● Unipolar (0 ~ 10VDC) ● Bipolar (0 ~ ±10VDC)	Sine	2.5, 5, 8, 10 kHz[1]	3 V_{rms}	Up to 20 mA_{rms}
	MP 2000	100 ~ 240 VAC (47 ~ 63Hz)	● Unipolar (0 ~ 10VDC) ● Bipolar (0 ~ ±5VDC) ● 5-digits digital display	Not specified[2]	2.5, 3.3, 5, 10 kHz[1]	1 or 3 V_{rms}	Up to 25 mA_{rms}
	PML 1000	90 ~ 265 VAC (50 ~ 60Hz)	● Unipolar (0 ~ 10VDC) ● Current (4 ~ 20 mA) ● 5-digits digital display	Not specified[2]	2.5 or 5 kHz[1]	1 or 3 V_{rms}	Up to 25 mA_{rms}
AA-Lab Systems	A-308	±7 ~ ±18 VDC	● Unipolar and Bipolar (0 ~ ±10VDC)	Low-distortion Sine	20 Hz to 20 kHz[3]	3 ~ 20 V_{rms}	40 mA_{rms}
	A-308 DIN	+9/-14 VDC +16/-28 VDC	● Unipolar and Bipolar (0 ~ ±10VDC) ● Current (4 ~ 20 mA)	Low-distortion Sine	930 Hz to 10 kHz[3]	3 ~ 20 V_{rms}	40 mA_{rms}
Everight Sensors	S1A	15 ~ 30 VDC ±15 VDC	● Unipolar (0 ~ 10 VDC) ● Bipolar (0 ~ ±10 VDC) ● Current (4 ~ 20 mA) ● Current (0 ~ 20 mA)	Low-distortion Sine	1, 3, 5, 10 kHz[1]	1.5, 3, or 4.5 V_{rms}	Not specified[2]
Macro Sensors	LVC 2500	10 ~ 30 VDC	● Unipolar (0 ~ 10 VDC) ● Bipolar (0 ~ ±10 VDC) ● Current (4 ~ 20 mA)	Low-distortion Sine	3, 5, 10 kHz[1]	3 V_{rms}	Not specified[2]
	MMX Series	15 ~ 30 VDC	● Unipolar (0 ~ 10 VDC) ● Current (4 ~ 20 mA)	Not specified[2]	2.5 kHz	1 ~ 3 V_{rms}	Not specified[2]

[1] Switch selectable
[2] In the online datasheet
[3] With component change

2.4 Sine wave generation methods

Considering the overall performance of the SSI, sinusoidal signal is the most efficient waveform to excite an L/RVDT sensor. Contrary to square, periodic exponential and quasi-sine waveforms, a pure sine wave has only one dominant frequency component. Exciting the L/RVDT with a sine-waveform induces the same frequency component in the signal spectrum of the sensor outputs. This characteristic decreases the order of the low pass filter in both ESG and DAM. The desired 14-bits resolution in the DAM of our SSI necessitates the design of a high-accuracy sine-wave generator in the ESG. The generator block should cover 1 kHz to 10 kHz frequency range.

According to the research papers and commercial products, sine-wave generators are based on three different techniques, namely: (1) Analog oscillator; (2) Non-linear circuits; (3) DSP[1] and memory-based. The choice of the architecture depends on the desired signal quality. In oscillators, a tunable component sets the frequency. Covering a limited frequency-tuning range, they are highly affected by temperature variation and component tolerances. Non-linear circuits usually transform a triangular wave to a sine by utilizing a nonlinear-transfer function. They cover a wider frequency range but are perturbed by temperature changes. In integrated realizations, the process variations of semiconductor devices and mismatches further decrease the accuracy and precision of the oscillators and non-linear solutions [44]. Both techniques are not programmable and thus, cannot be involved in our application.

DSP and memory-based architectures are mixed-signal circuits which employ DSP, digital memory, microcontroller, or digital logic circuitry along with a DAC to generate an arbitrary waveform. As depicted in Figure 2.3, the samples of the expected waveforms are stored in a digital or analog memory. Depending on the shape of the signal, an addressing algorithm reads out one stored sample in each clock cycle and applies it to the DAC for conversion to an analog equivalent. The clock rate and the number of retrieved samples in each cycle determine the frequency of the output signal. A filter, amplifier, and/or matching circuit follow the DAC to improve the quality of the signal. A DSP or MCU can be used to implement the clock module, the memory address controller, and the digital memory. This method is widely used in Arbitrary

[1] Digital Signal Processor

Function Generators (AFG) and Arbitrary Waveform Generators (AWG) [45,46]. The large required physical size of the memory and other digital blocks is the drawback of this technique.

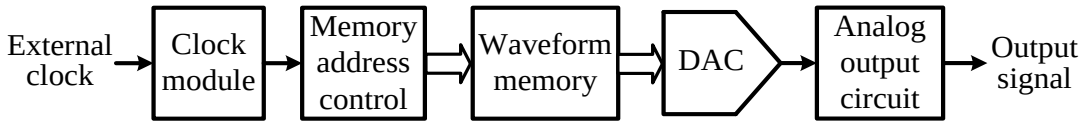


Figure 2.3: block diagram of mixed-signal waveform generators

In 2009, Yang et al. have designed a hybrid architecture to generate quadrature sine waveforms in seven orders of frequency range from 1 mHz up to 10 kHz [44]. To cover the range of 100 Hz to 10 kHz which overlaps our application, they have used a resistor-chain DAC (RCDAC). It includes a resistor-chain followed by a track-and-hold circuit and a g_m-C biquadratic low pass filter with selectable cutoff frequencies. The resistor-chain is a voltage divider with 33 different taps which are representing analog samples of a half-cycle sine waveform. Therefore, the chain could create a set of 64 samples of a complete cycle of a sine. An overall SFDR[2] of -50dB is expected from the 64x OSR[3]. A clock divider divides the 10 MHz master clock (f_{clk}) frequency by an integer number, *M*, to control the DAC switches. Synchronously with the clock and consecutively, tap voltages are conducted to the DAC output in order to form the sine wave. The output frequency (f_{out}) can be calculated using Eq. (2.3).

$$f_{out} = \frac{f_{clk}}{64M} \tag{2.3}$$

The authors of [44] used the RCDAC as an analog memory to avoid the large physical area needed for a digital memory. The matching between resistors and the on resistance of the switches are the most important factors affecting the linearity and performance of this architecture. To achieve a high linearity, 1000 same-size resistors were utilized in the chain to form unequal resistances between taps. Simple NMOS transistors are used as switches which simplify the control logic. Occupied 1 mm^2, the design is fabricated in 0.5µm CMOS process. Contrary to the design objective (-50dB) a THD of less than -44dB (0.6 %) across the entire frequency range has been reported.

[2] Spurious Free Dynamic Range

[3] Over Sampling Ratio

The notable drawback of the analog memory is that upon fabrication of the chip, no calibration will be possible. Moreover, the large number of resistors results in higher power dissipation in the chip. Furthermore, to have higher SFDR, larger number of taps and thus, more resistors are required which increases the complexity of the design. Additionally, the on-resistance of the NMOS switches depends on the tap voltage and negatively affects the linearity of the RCDAC.

In brief, the idea of saving the samples in a memory is a proven solution for generating a sine waveform, but an analog memory is not suitable for our application where the SSI is linked to a digital architecture including digital memories. As the most important block in memory-based sine wave generators, a review on DACs will be presented in the rest of this chapter.

2.5 Digital to Analog converter architectures

As shown in Figure 2.3, integrated DAC is the most important block in the memory-based sine waveform generators. On the other hand, a more accurate and precise DAC generates a purer sine wave with higher SNDR. The purity and perfection of the sine wave further results in higher SNDR of the sensor output signal and increases the accuracy of the sensing system.

Baker, Razavi, and Kester discussed the fundamentals and popular architectures of integrated DACs. Differing in complexity level, DAC circuits are implemented in three different technologies; voltage-mode, current-mode, or charge redistribution mode. In terms of the architecture, resistor string, R-2R ladder, current steering, or switched capacitor could be used to convert binary-weighted digital data to an analog value [47,48,49]. D/A converters can also be divided in Nyquist-rate, interpolating, and oversampling categories. In narrower bandwidth and lower frequency applications, higher update rates can be used to increase the accuracy and relax the requirements of the anti-aliasing filter which follows the DAC. In wide band applications, Nyquist-rate conversion method is used to avoid the high clock frequency needed for oversampling [50].

Resistor strings architectures, depicted in Figure 2.4, are very simple and have a guaranteed monotonicity. But in N-bit DAC, the matching between 2^N resistors has a significant role in the linearity merit. Besides, the power dissipation and physical area required for the resistors must be

balanced. Assuming that the summation of the errors of all resistors is zero, the maximum Integral Non-Linearity (INL) of this DAC type is calculated using Eqs. (2.4) and (2.5) [47].

$$LSB = \frac{V_{REF}}{2^N} \tag{2.4}$$

$$|INL|_{max} = \frac{1}{2} LSB \times 2^N \times (\%\, matching) \tag{2.5}$$

where N is the number of digital input bits, and *%matching* is the maximum deviation of the resistances from the desired value. Therefore, achieving maximum INL of 0.5LSB in a 10-bit DAC needs a matching of better than 0.09% among 1024 integrated resistors! The output node is connected to 2^N switches in the simple resistor string type. Hence, a large parasitic capacitor is expected in this node which limits the frequency of the DAC output. The resistance of switches is another design challenge and should be minimized to achieve a high performance. The impact of this factor is more critical in binary switch array resistor string (Figure 2.4(b)).

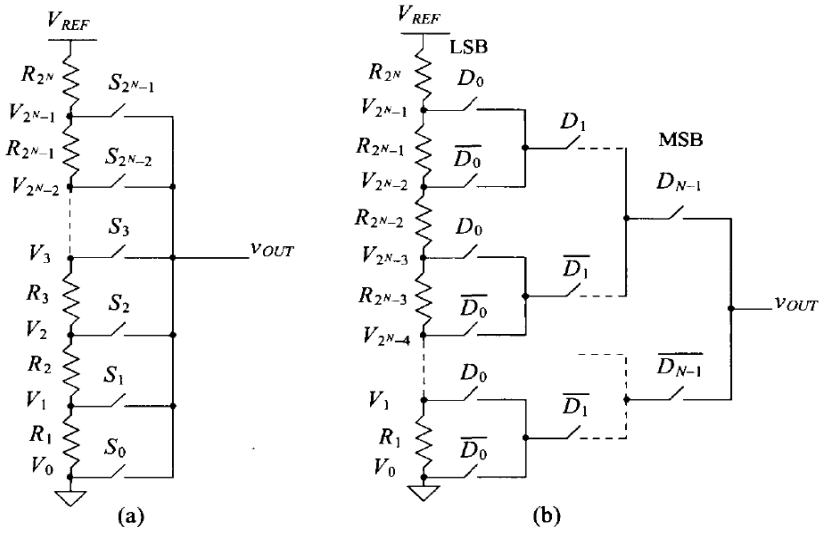


Figure 2.4: (a) Simple resistor string DAC (b) Resistor string with binary switch array [47]

R-2R ladder, shown in Figure 2.5, is another common DAC type which uses only two different resistors, includes less number of resistors, and has lower noise level comparing to resistor string. Although R-2R ladder has slower conversion speed in comparison with resistor string, it can be used in current-mode configuration as well (inverted mode) [49]. However, in this architecture, all the resistors should be matched and the resistance of switches is a crucial design parameter which should be minimized or compensated [51].

Figure 2.6 shows the circuit diagram of binary-weighted charge-scaling DAC. The capacitance, C, is the unit capacitor representing the LSB and is used in forming larger capacitors corresponding to other data bits. The output voltage is a function of V_{REF} and the division between capacitors. The accuracy and precision of the DAC depends on the available capacitors in the targeted CMOS technology. Similar to resistor string architecture, there is a large parasitic capacitance at the non-inverting input of the buffer that limits the resolution of this DAC. Careful layout techniques and schemes must be employed to overcome process variations. Split arrays are also introduced to avoid very large non-integrable capacitors [47].

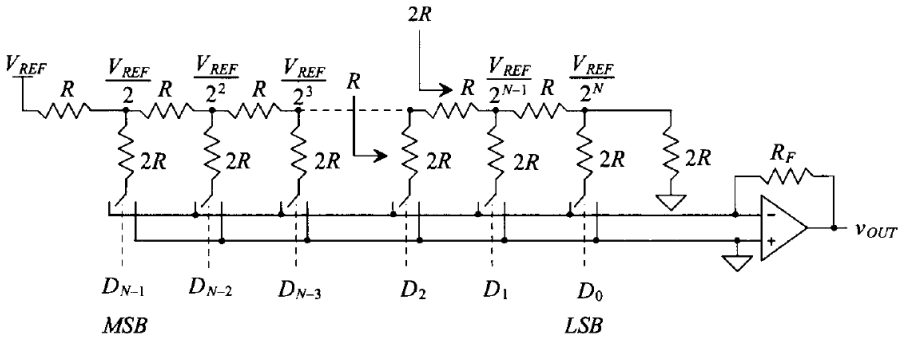


Figure 2.5: R-2R ladder DAC architecture [47]

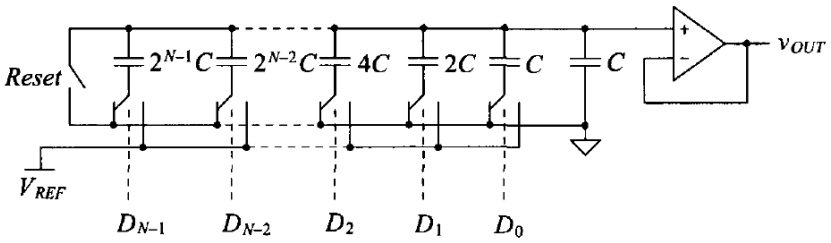


Figure 2.6: Binary-weighted charge-scaling DAC architecture [47]

In the current-mode R-2R ladder DAC, a voltage is converted to current. But in Current-Steering DAC (CSDAC), current sources are the very basic stage of the conversion. In this architecture, precision current sources steer their currents to the load through the switches, controlled by input data bits. Two configuration of this type is shown in Figure 2.7 where (a) includes a set of similar current sources and in (b) binary-weighted values are used. Digital encoder or decoder blocks

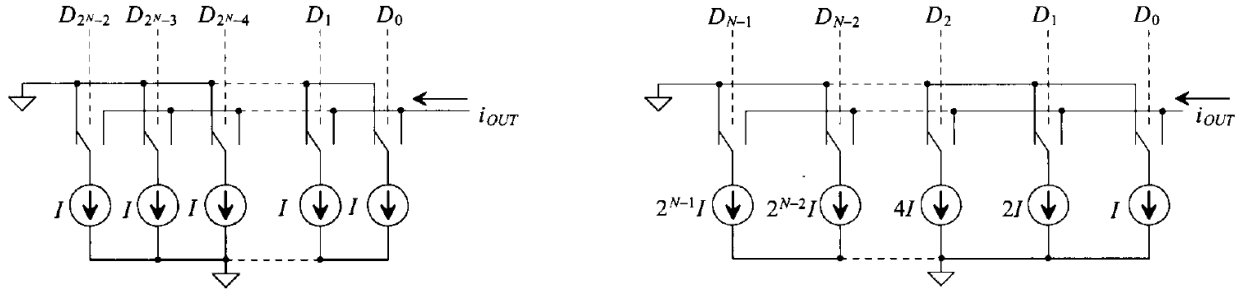
might be used in order to convert input data to appropriate format. Switch control blocks and timings should be carefully designed to prevent conversion error [47].

Comparing with 2^N sources in the thermometer coded CSDAC, the binary-weighted type contains N sources for an N-bit converter. The disadvantage of binary-weighted CSDAC is the large glitch at output in response to higher bit transitions. The worst glitch occurs when the MSB[4] changes and causes the maximum DNL that is defined in the following Eq. (2.6) [47]:

$$|DNL|_{max} = (2^N - 1) \times |\Delta I|_{max} \tag{2.6}$$

Formulated in Eq. (2.7), the INL in both architectures is a function of N and the maximum current error due to mismatch [47].

$$|INL|_{max} = 2^{N-1} \times |\Delta I|_{max} \tag{2.7}$$



(a) (b)

Figure 2.7: Current steering DAC (a) Thermometer code, (b) Binary-weighted code [47]

To overcome drawbacks of both current steering DAC implementations, a combinational topology has been introduced that is called *segmented CSDAC*. In this solution, binary-weighted CSDAC is employed for implementing LSB part which results in less number of current sources. To benefit the advantage of lower DNL, the MSB part is designed using thermometer code structure. An example of this architecture for a 7-bits CSDAC is shown in Figure 2.8 [49].

The transformer nature of the L/RVDTs demands for sine wave current instead of voltages for excitation. Hence, we focused on CSDACs which has an inherent high-current drive capability and thus, no output buffer is needed [47]. Furthermore, the compatibility of CSDACs with high speed applications facilitates the usage of the oversampling techniques. Additionally, low-cost

[4] Most Significant Bit

and high performance 0.13µm CMOS technology enables the designer to achieve a high level of matching which is required among current source transistors in CSDAC architecture.

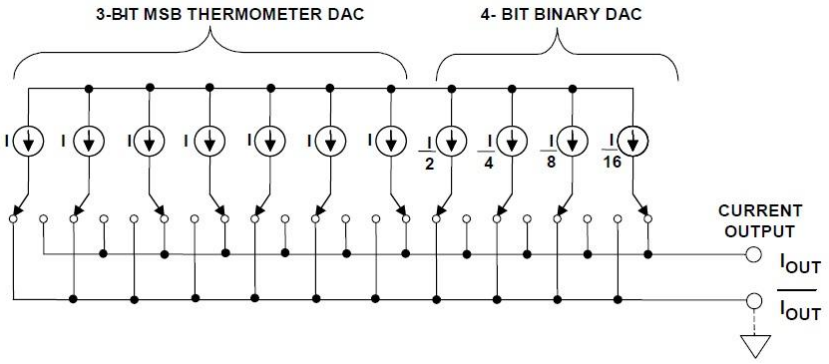


Figure 2.8: Segmented current steering DAC [49]

2.5.1 State of the art of current-steering DACs

Although CSDAC architecture is widely employed in the high-speed data converter applications, there is no limitation in using it for generating low frequency signals. In the binary-weighted CSDAC architecture, the arrangement of Current Source Array (CSA) results in high glitches, non-monotonic behavior, and differential nonlinearity (DNL). So, in high-accuracy applications, fully thermometer-decoded or segmented arrangement is often used to implement the whole or the most significant bits of the current-steering DAC. In this arrangement, increments of input code switch on the unary current sources one after another and steer their current into the output load. The above solution improves all such degrading factors but the drawback is increasing layout complexity, active area, and power consumption [52,53,54,55,56,57,58,59].

As CSDACs rely on the generation of currents proportional to the binary/unary weights, large array of current sources are required in high resolutions. The implementation of such current sources on silicon with adequate accuracy is challenging due to the process variations and/or different interfacing conditions raised by various interconnections. Thus, random mismatch between the laid-out and fabricated current sources are expected that increases both DNL and INL in the DAC. Therefore, depending on the effective DAC resolution, the INL yield put a high bound on the mismatch among current sources in the array. Apart from the major considerations in the architectural level design, maximum tolerable mismatch error along with the process variation profile of the selected technology should be considered in the sizing of current source transistors.

Reducing such an error which is often referred to as random error in the literature, implies using large-sized transistors that constrains the size of the CSA. In addition to the random error, there are other sources for errors such as temperature variation, power supply voltage drop along the array, limited output resistance of the sources, mechanical stress over the die, layout issues, and technology related imperfections. The generated errors due to these factors are known as systematic errors. The larger the dimensions of the CSA, the higher the impact of the systematic errors on the DAC performance. The accumulation of random and systematic errors forms the overall error which affects the static and dynamic performances of the DAC. In fact, for a DAC structure with minimized error in its CSA elements, as different number of current sources switch on in response to the DAC input, their global error may be accumulated. This results in increase of the INL. Authors have introduced distributed scheme to reduce such error while implementing current sources. In this scheme each source is mainly split to 4 or 16 parallel sources which are distributed in the CSA. Moreover, a variety of switching sequences have been developed in order to further reduce such an effect. Choice of efficient switching sequence implies known or predicted gradient of the systematic error [52,53,58,59].

An accurate switching strategy may also be developed based on the measurements of a test chip. Although it is costly and depends on the size of CSA, applying such technique can practically minimize the accumulation of gradient errors in the DAC [53]. Another approach is to accurately tune the current sources after fabrication, [60], which is not feasible for all technologies and requires extensive efforts at layout stage. Authors have also introduced DAC designs consisting of extra circuitry capable of measuring the error of each source locally and post-fabrication programming of the efficient switching sequence based on the outcomes [61]. Growth of active area and complicated routing are the major drawbacks of this method. Nevertheless, in DAC circuits using conventional methods, switching sequence is designed based on linear and quadratic components of the gradient error. Among other approaches, the symmetrical, hierarchical symmetrical, INL bounded, and Q^N rotated walk sequences are often used [53,58,62,63,64].

Authors in [62], whom are followed by other successors such as in [63], have assumed a physically square-pattern of $M \times M$ (rows by columns) for distribution of the current sources. They have compared several different switching sequences with reference to their impact on the INL and have proposed an optimized sequence. With this assumption, the size of the current

source transistors added to the empty space between them in *x* and *y* directions should be equal while laying out the CSA. This means that, both the width and length of the transistor should be the same (that causes a limitation in the circuit level design) or large distances should be considered between transistors with unequal length and width (results in larger die area) [58].

In implementation of thermometer-decoded current steering DACs, large number of current sources, configured by large transistors, is often used. This is to reduce the mismatch between sources [57,65]. Besides, the binary-weighted current sources of segmented DACs are mainly distributed throughout the unary source array. This results in modifying the uniformity of the CSA in the DAC architecture [53]. These will further exacerbate the impact of gradient errors on the performance of the DAC. Hence, the efficiency of the switching sequence must be characterized in accordance with the dimensions of the laid-out CSA. To the best of our knowledge, this effect was not ever considered in the researches.

From this review we can conclude that a correlation is expected between the physical implementation of the CSA and the proper switching sequence. Choice of distribution pattern for current sources and switching sequence may play significant role in drawing the design strategy for the targeted DAC structures. In the context of this Master thesis, we will design a 10-bit CSDAC as the core of the ESG. During the design procedure, the impacts of the physical size of the CSA will be considered, simulated, and measured as a new parameter in the realization of the CSDAC.

2.6 Conclusion

In this chapter, an overview of the integrated sensing systems is presented. The application of this concept for interfacing R/LVDT displacement sensors, the requirements of such an interface, and the commercially available solutions were also discussed. As one of the two main modules of R/LVDT sensor interface, sine waveform generation methods compared. With reference to our application, the memory-based sine wave generation technique is selected for implementation. Finally, the state of the art of the CSDAC which can be used in this application was introduced. The next chapter is dedicated to the design procedure in the system and circuit level. We will first review the block diagram of the ESG, clarify the design parameters, and determine the I/O requirements. Then, the CSDAC circuit structure will be presented.

CHAPTER 3

THE ESG ARCHITECTURE AND DAC DESIGN

3.1 Introduction

In order to validate the fully integrated design of the SSI in AVIO402, it is required to individually design, implement, verify, and validate the main modules and building blocks of the SSI. Referring to Figure 1.4, we will focus on the design of the integrated ESG in this work. Upon individual design and validation of the SSI modules, the integrable parts of the ESG and the DAM will be integrated in one single chip [1].

Obviously, the specification of the ESG contributes in the overall performance of the SSI. Thus, system level analysis of the SSI should be also considered in setting the requirements of the ESG module. With respect to the whole SSI architecture presented in chapter one and according to the outcomes of the reviewed literature, the memory-based sine waveform generation method has been approved for implementing the ESG. This method meets all the desired specification and characteristics. As shown in Figure 2.3, a DAC has been employed at the heart of this architecture. With regard to the impacts of the static and dynamic performance of the DAC on the overall specification of the ESG module, a 10-bit DAC was designed. In this chapter, the design procedure of the suitable DAC architecture is presented.

In Section 3.2, the system level structure of the ESG and the required specifications are described. CSDAC specification and its design procedure are explained in Sections 3.3. Then, in Section 3.4, the design of the DAC will be discussed in circuit and layout level. Section 3.4.2 presents the main contribution of this work which is the impact of physical implementation of the current source array (CSA) on the performance of the switching scheme in CSDAC architecture.

Finally, layout design challenges of CSDACs will be explained which will be followed by the conclusion.

3.2 The ESG requirements and block diagram

3.2.1 ESG design requirements

Low-count of I/O connections, integrability with DAM, programmability of the frequency and amplitude of the excitation signal, and supporting the required accuracy and resolution of the SSI are design requirements of the ESG module [1]. Design specifications of the ESG module and its internal stages should be concluded from the SSI design parameters and system level analysis. Figure 3.1 indicates the system level diagram of the SSI and its connection to the sensor and digital interface controller.

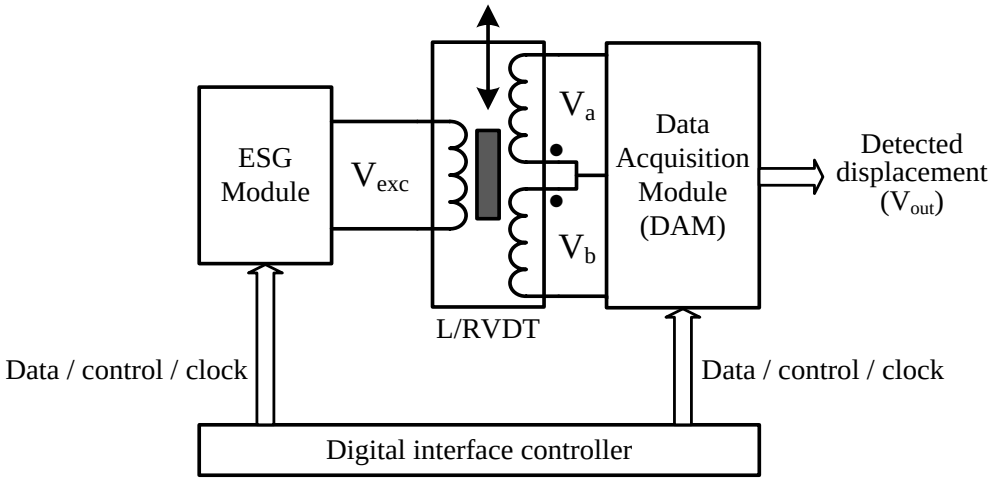


Figure 3.1: System level diagram of the SSI [1]

According to the SSI design requirements in [1,66], displacement of the core of the sensor must be converted to a 14-bit digital value and be available at the output of the DAM with a maximum latency of 2 mSec. As stated in chapter 1, V_{exe} provides the carrier signal for the L/RVDT and the displacement of the core is modulated over the amplitude of V_a and V_b. In order to detect the displacement, sensor output signals are then demodulated and digitized in the DAM. The maximum bandwidth of V_{out} is assumed to be 500 Hz which impose a Nyquist frequency of 1

kHz. With reference to the theory of sampled data systems, Signal to Noise (quantization noise of the converter) Ratio (SNR) of V_{out} can be calculated using Eq. (3.1) [49].

$$SNR = 6.02N + 1.76\ dB \tag{3.1}$$

where N is the number of bits of Analog to Digital Converter (ADC) embedded within DAM. Given the Nyquist sampling frequency of f_s, the SNR is measured over the Nyquist bandwidth (DC to $f_s/2$). Thus, V_{out} must meet the SNR of 86.04 dB in the bandwidth of 500 Hz. If higher sampling frequency than Nyquist is used in the ADC, a process gain will be added to Eq. (3.1) which is formulated in Eq. (3.2) and improves the SNR in the desired bandwidth.

$$SNR = 6.02N + 1.76\ dB + 10\log\left(\frac{f_s}{2\times BW}\right) \tag{3.2}$$

where f_s is the oversampling frequency, BW represent the maximum bandwidth of the signal, and the SNR is calculated over the signal bandwidth (DC to BW) [49].

On the other hand, the noise level of V_a and V_b contributes in the final SNR of Vout. This contribution depends on the architecture of the DAM. Hence, accurate model of the DAM is needed to analyze this contribution. Given an ideal sensor model, system level analysis of the DAM shows minimum required SNR of 84 dB for V_{exe} over the bandwidth of 10 kHz [1]. Based on Eq. (3.2), using oversampling ADC and digital filtering in the DAM relaxes the required SNR of the excitation signal.

System level considerations and requirements impose several design obligations on the ESG that are listed in Table 3.1. Moreover, the I/O connections of the ESG should be minimized in order to be proper for avionic applications.

Table 3.1: ESG design objectives

Design objectives	**Required range**	**Details**
Excitation frequency	1 ~ 10 kHz[1]	• Frequency accuracy: 1% • Number of channels: 30[2] • Programmable by digital interface controller
Excitation amplitude	1 ~ 7 V_{rms}[1]	• ESG output should be matched with sensor input
Output SNR	84 dB	• Measured over DC to 10 kHz

[1] Based on Honeywell L/RVDT used in avionics applications [26].

[2] This implies maximum displacement data bandwidth of 80 Hz [1].

3.2.2 Proposed ESG block diagram

With reference to the reviewed literature, the memory-based sine-wave generator is the only method which supports the frequency and amplitude programmability of the sine-wave. Figure 3.2 shows the proposed detailed block diagram of the ESG which is based on this method.

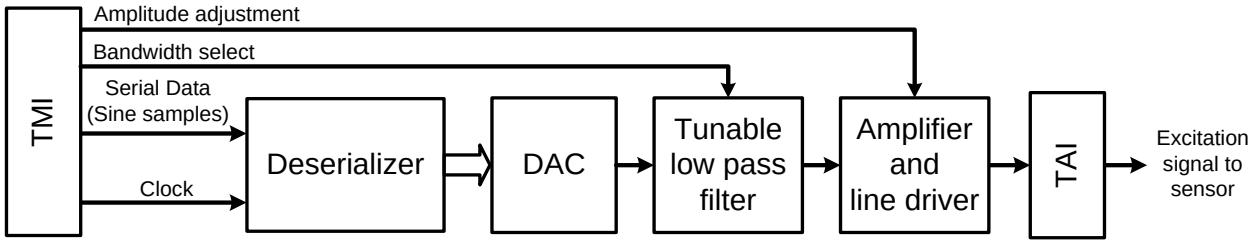


Figure 3.2: Proposed ESG architecture

In Figure 3.2, TMI is part of digital interface and provides digital signals, commands, and clocks needed by ESG. Introduced in IEEE-1451, Transducer Analog Interface (TAI) is the physical interface between the transducer and the signal conditioning functions [12]. TMI and TAI are beyond the scope of this work.

In order to reduce the I/O connections between TMI and the ESG, a serial data line has been considered for transferring the data to the ESG. Thus, a Deserializer is used that includes a shift register and a latch. Deserializer is responsible for serial reception, preserving, and parallel transmission of the digital sine samples to the DAC. These processes are in synchronization with a clock signal generated in digital interface. In fact, data are serially entered in a shift register with a higher clock frequency than sample rate. The contents of the shift register should be then loaded into a latch which keeps the data for the digital to analog conversion. The clock frequency of the latch is equal to the update rate of the input data. Required resolution and SNR of the sine waveform determine the size and contents of the digital lookup table memory (located within TMI) which keeps sine samples as well as the length of the shift register and latch.

High speed DAC converts the digital latched samples to its analog equivalent and generates an accurate analog sine waveform. It is designed based on current steering architecture to support higher update rates which improves the SNR of the excitation signal. Depending on the sample rate (update rate) of the digital data at the input of the DAC and the number of digital sine samples in one complete cycle, different sine frequencies will be generated at the output of the

DAC. It goes without saying that resolution, accuracy, precision, linearity, and speed of the DAC considerably affect the ESG performance in this architecture. The parameters of the DAC will be discussed in later sections.

The DAC output is pulse amplitude modulated with a modulation frequency equal to sample rate. Consequently, the spectrum of the DAC output signal is repeated at multiples of the sample frequency. Depending on the desired signal bandwidth and the sample rate, an appropriate analog anti-aliasing Low Pass Filter (LPF) should be used after the DAC. Rejection of the repeated spectra and sufficient attenuation of the harmonics of the fundamental frequency are the main responsibilities of this LPF. With regard to the adjustable excitation signal frequency (1 kHz to 10 kHz), the cut-off frequency of this filter must be separately tuned for any sine wave frequency. However, the design of the LPF can be simplified by selecting few switch-selectable cut-off frequencies based on the frequency distance between the fundamental frequency and the first harmonic. The TMI provides the control command for selecting the cut-off frequency of the LPF.

The filtered signal should be amplified or buffered in order to be matched with the primary coil of the sensor. Adjustability of the amplitude of excitation signal is one of the objectives of this project. Therefore, variable gain amplifier must be used whose gain can be adjusted by the digital interface via TMI. Linearity of the amplifier plays a significant role in the overall SSI performance. Generation of large amplitude excitation signal requires high power supply voltages which cause serious restriction on integration of all blocks. Hybrid technologies might be needed to integrate the ESG into one chip.

In the block diagram of Figure 3.2, achieving SNR of 84 dB for the excitation signal is the responsibility of the DAC and anti-aliasing filter. Eq. (3.1) formulates the effect of quantization noise and implies a minimum resolution of 14 bits on the DAC in favor of providing such a high SNR. However, higher update rate than Nyquist as well as using appropriate LPF could result in the same SNR with lower DAC resolution.

In theory, the filter has a roll off of 6 dB per octave for each pole. Although the design of high order integrable LPF in the targeted frequency range is very challenging (due to the large size of capacitors and inductors), lower order active filters with switch-selectable cutoff frequencies and few off-chip components can be integrated in the full-custom SSI chip. Additionally, the LPF should attenuate the level of harmonic components of the fundamental sine frequency and reject

the repeated spectra of the excitation signal at multiples of the sample rate frequency. The power of harmonics of the fundamental frequency reduces the SNDR of the excitation signal. Eq. (3.3) formulates the SNDR.

$$SNDR = 10log\left(\frac{P_S}{P_N+P_D}\right) \tag{3.3}$$

where P_S is the fundamental signal power, P_N is the in-band noise power, and P_D is the sum of the power of first five harmonics [49].

In the semi-custom stage of the AVIO402, the most challenging internal block must be designed, fabricated and validated. This validated block should then be integrated with other blocks as the full-custom SSI. Regarding the impacts of DAC parameters on the ESG and SSI performance, we will focus on the design of DAC and deserializer in this work. Since the design of the filter is beyond the scope of this work, in-band SNR improvement of the LPF is not discussed in this Master thesis. We have selected high speed CSDAC architecture based on the reviewed literature.

According to Eq. (3.2), the process gain of oversampling increases the expected SNR, however, the drawback of high sample rate is the size of lookup table which keeps the ideal sine samples. It has been assumed that sufficient memory space is available in digital interface. On the other hand, quantization uncertainty defines a maximum limit for the sample rate. This parameter is shown in Figure 3.3 for an ideal 3-bit DAC. To calculate this limit, the DAC resolution and Full Scale (FS) must be known.

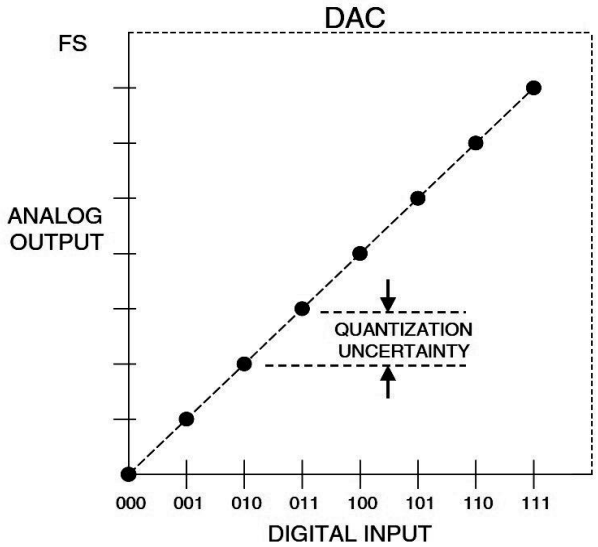


Figure 3.3: Transfer function of an ideal 3-bits DAC [49]

The quantization uncertainty of an ideal N-bit DAC can be calculated:

$$Quantization\ uncertainty = \frac{FS}{2^N} = LSB \tag{3.4}$$

where N is the number of bits, FS is the output full scale, and LSB is the weight of the least significant bit of the DAC. Considering the LSB of the DAC, the sample period ($\frac{1}{f_s}$) must be long enough that one LSB variation happens in the ideal sine waveform. This concept is visualized in Figure 3.4 where the ideal 1 kHz sine wave with full scale amplitude of FS is depicted along with the reconstructed wave form. As can be seen in Figure 3.4, two successive steps have the maximum voltage difference (step voltage) at the mid-scale of the reconstructed sine signal. We use this fact to calculate the maximum sample rate of the DAC as a function of its LSB.

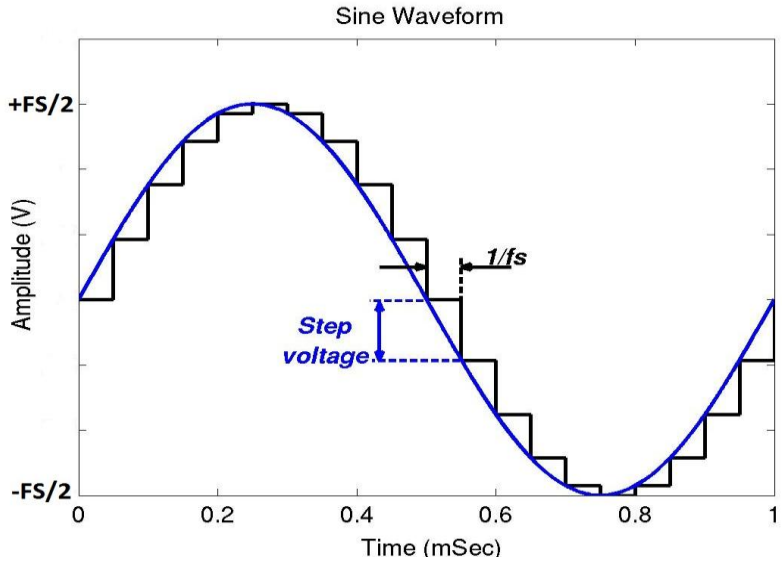


Figure 3.4: Ideal 1 kHz sine wave versus reconstructed output signal of DAC

For sample rate of f_s and sine frequency of f_{sine}, minimum step voltage can be calculated using Eqs. (3.5) and (3.6).

$$\left\{\left(\frac{FS}{2}\right) * Sin\left[2\pi f_{sine}\left(t + \frac{1}{f_s}\right)\right]\right\} - \left\{\left(\frac{FS}{2}\right) * Sin(2\pi f_{sine} t)\right\} \geq LSB \tag{3.5}$$

$$\left\{\left(\frac{FS}{2}\right) * Sin\left[2\pi f_{sine}\left(t + \frac{1}{f_s}\right)\right]\right\} - \left\{\left(\frac{FS}{2}\right) * Sin(2\pi f_{sine} t)\right\} \geq \frac{FS}{2^N} \tag{3.6}$$

Given the maximum step voltage at the mid-scale (t = 0) which is shown in Figure 3.4, it is needed that:

$$\left\{\left(\frac{FS}{2}\right) * Sin\left[2\pi f_{sine}\left(\frac{1}{f_s}\right)\right]\right\} \geq \frac{FS}{2^N} \tag{3.7}$$

$$f_s \leq \frac{2\pi f_{sine}}{asin\left(\frac{1}{2^{N-1}}\right)} \tag{3.8}$$

where *asin* is the inverse sine function. The number of samples needed for reconstructing sine signal is therefore:

$$Number\ of\ samples\ per\ sine\ cycle = \frac{f_s}{f_{sine}} \tag{3.9}$$

Adopting maximum sample rate to generate 1 kHz sine signal, we will need 32170 bits of memory to keep the sine samples. To generate higher sine frequencies with the same number of sine samples per cycle, higher sample rates can be adopted. According to Eqs. (3.2), (3.8), and (3.9), Nyquist sampling and oversampling parameters are listed in Table 3.2 for 10-bit DAC. These parameters are calculated at the beginning, middle, and end of the targeted frequency range. It is also possible to use a constant oversampling frequency and reconstruct different number of sine samples in order to cover the whole frequency range. The choice between fixed f_s or constant number of sine samples depends on the design strategy of the digital interface.

Table 3.2: Sampling parameters for 10-bit DAC

Excitation signal frequency	**Nyquist sampling**			**Oversampling**		
	f_s (kHz)	No. of samples[1]	SNR[2] (dB)	f_s[3] (MHz)	No. of samples[1]	SNR[2] (dB)
1 kHz	20	20	61.96	3.217	3217	84.02
5 kHz	20	4	61.96	16.085	3217	91.01
10 kHz	20	2	61.96	32.17	3217	94.02

[1] Per one sine cycle

[2] Calculated from DC to 10 kHz using Eq. (3.2)

[3] Maximum sample rate for the resolution of 10-bits

Using steep roll off LPF with high stop band rejection relaxes the sample rate of the DAC. Therefore, there is a tradeoff between the order of the LPF on one hand and the sample rate and resolution of the DAC on the other hand.

Considering the above mentioned facts and figures, a 10-bit CSDAC is proposed and destined for fabricating in the semi-custom stage of ESG design. Measurement learning and achievements

determine the final design architecture of the ESG for the full-custom stage. In the rest of this chapter, the design flow, schematic capture, and layout implementation of the 10-bit CSDAC with very high oversampling capability are discussed.

3.3 The CSDAC architecture, specifications, and design procedure

Digital to analog converters reconstruct an analog signal from N-bit digital samples. Therefore, DAC output signal is quantized and can only represent 2^N voltage or current values (assuming a fixed reference). N is the resolution of the DAC and the N-bit digital input may be expressed in different formats among which binary is the most popular. The reconstructed signal in time and frequency domain is shown in Figure 3.5 where f_c is the sample rate. As a matter of fact, output signal of the DAC is a pulse-modulated signal and has a Sinc function equivalent in frequency domain. Images of the fundamental frequency of the output are also repeated at multiples of the sample frequency. According to the sampling theorem, the sample rate should not be less than Nyquist frequency which is twice the maximum expected frequency component in the reconstructed signal [49].

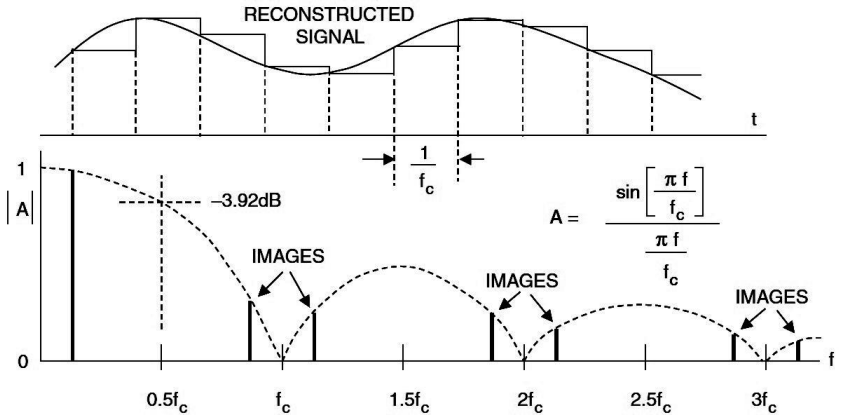


Figure 3.5: DAC sinc(x) roll off [49]

DACs can be divided into three categories: (1) Nyquist rate DACs in which sample rate is equal to Nyquist rate; (2) Interpolating DACs that use a higher sample rate than Nyquist; (3) Oversampling DACs which use higher sample rate than Nyquist along with a noise shaping modulator. We have aimed to a high sampling rate, interpolating CSDAC in this work [49].

As discussed in chapter 2, CSDAC architecture is used in high-accurate and high-speed data converter systems. Additionally, submicron CMOS technologies offer fast and low power solution with the possibility of System on Chip (SoC) design. In fact, CMOS technologies not only provide the required infrastructure to achieve expected performance of the CSDAC, but also facilitate the implementation of some of other blocks in the ESG (low pass filter in Figure 3.2) and the SSI in order to integrate the whole system within one chip [59].

Conceptual, block, and circuit diagram of a general N-bit, binary-weighted, CSDAC is shown in Figure 3.6. Weighted current sources are transistors (M_{CS}) which mirror multiples of the reference current and steer their currents to the load via switch transistors (M_{SW}). Sources with higher currents are built by using a number of unit current sources in parallel. To achieve the best matching among current mirrors, the mirroring transistors must be designed as a Current Source Array (CSA). The output resistance of an ideal current source is infinite. Depending on the desired performance, cascode transistors (M_{Casc}) might also be used in series with M_{CS} to increase output resistance of each source. M_{Casc} and M_{CS} are biased by stable bias circuit. High speed switches are controlled by the input data through switch driver circuit. Any logical "one" at the N-bit binary input word adds the current of its corresponding current source to the load [48,49].

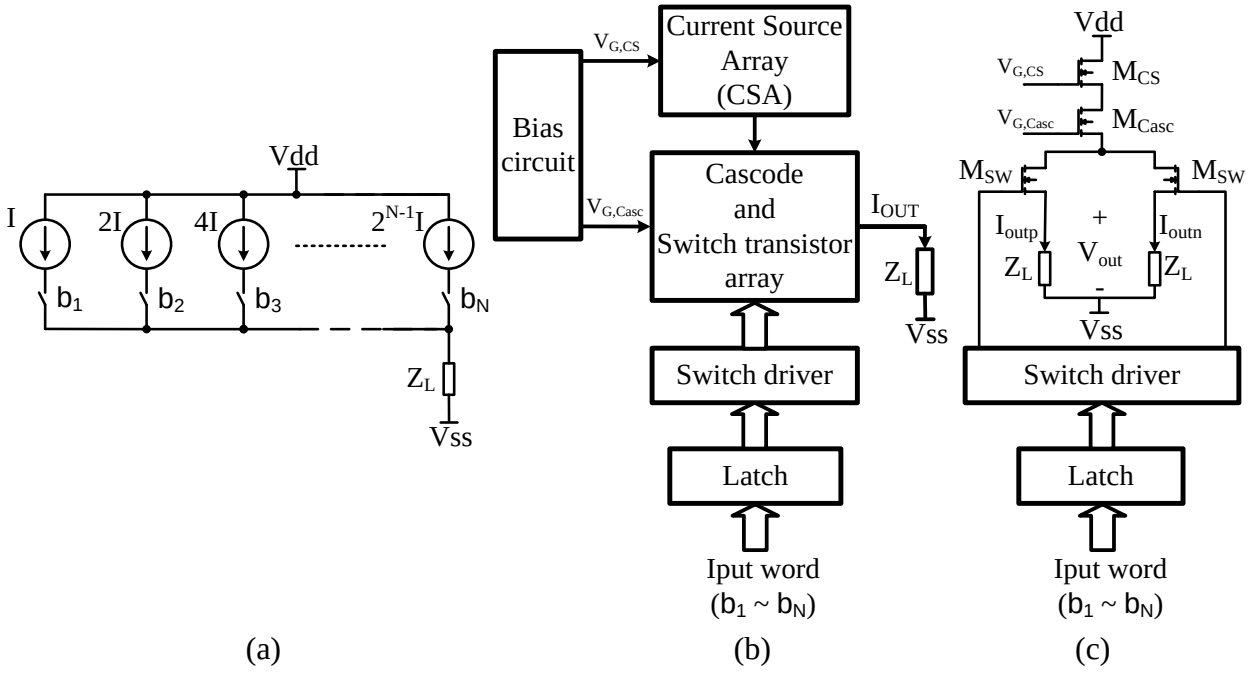
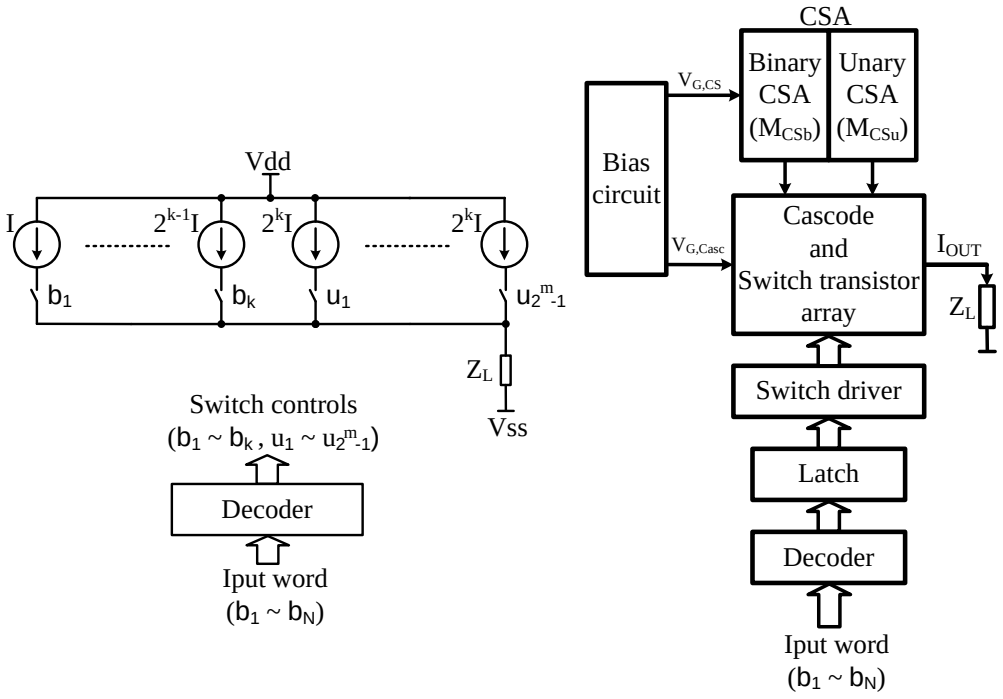


Figure 3.6: Binary-weighted CSDAC; (a) Conceptual diagram, (b) General block diagram, (c) Circuit diagram

In order to decrease DNL of binary-weighted current sources, CSDAC can be segmented into binary-weighted and thermometer-decoded sections. This architecture is shown in Figure 3.7. In this architecture k-bit of LSB and m-bit of MSB are designed using binary-weighted and unary-weighted implementations, respectively. A decoder is needed to convert m-bits binary MSB to the equivalent thermometer code. Increasing the number of unary current sources (m) improves the DNL of the DAC; however, more die area is needed. Hence, there is a tradeoff between DNL and the area which will be discussed later in this chapter [59,67].



(a) (b)

Figure 3.7: Segmented CSDAC architecture; (a) Conceptual diagram, (b) General block diagram

Mismatch among current sources can be reduced by sizing the transistors [65]. Splitting unary transistors (M_{CSu}) and spreading them across the CSA further reduce the error of each source. Moreover, the sequence of switching on current sources of the CSA contributes in the accumulation of the mismatch errors. Switching scheme, splitting transistors and using a switching sequence, is another design parameter of segmented CSDACs [53,59,62].

There are many DAC specifications that defined in [49] and can be grouped as static, dynamic, environmental, and optimization parameters [59]. The most important specifications of each group are listed in Table 3.3. Specified parameters of this work are shown as desired value.

Table 3.3: Most important specifications of CSDACs with desired values in this work

Group	Specification	Desired value	Unit
Static	Resolution	10	bits
	Full Scale Range (FSR)	–	V or A
	INL	0.5	LSB
	DNL	0.5	LSB
	INL yield	–	%
	Accuracy	–	%, ppm, dB, or LSB
	Monotonicity	monotonic	–
Dynamic	Sample rate	Variable	Hz
	Output frequency range	1 ~ 10	kHz
	SNR	84	dB
	SNDR	–	dB
	THD	–	dB
	Glitch impulse	–	pV-Sec or mV-nSec
	SFDR	–	dB
	Settling time	–	nSec
	Noise	–	V_{rms}, V_{p-p}, or dB
	Input feedthrough	–	–
	Slew rate	–	V/µSec
Environmental	Power supply[1]	1.2	V
	Load resistance	–	Ω
	Digital input level	1.2	V
	Technology[2]	0.13 µm CMOS	–
Optimization	Power consumption	–	mW
	Chip area	–	mm^2

[1] Limited by the technology

[2] Being Supported by CMC Microsystems, lower fabrication price, multiple run per year, and accurate transistor models are the features of standard CMOS 0.13 µm technology that makes it well-suited to our work [68,69,70].

Due to the importance of INL and DNL in this work, their definitions are stated below:

> "Integral nonlinearity is the maximum deviation, at any point in the transfer function, of the output voltage level from its ideal value—which is a straight line drawn through the actual zero and full scale of the DAC" [49].

> "Differential nonlinearity is the maximum deviation of an actual analog output step, between adjacent input codes, from the ideal step value of +1 LSB, calibrated based on the gain of the particular DAC. If the differential nonlinearity is more negative than –1 LSB, the DACs transfer function is non-monotonic" [49].

Despite the discrimination made in Table 3.3 among static and dynamic performance of a DAC, the static linearity of the DAC (INL and DNL) is reflected in the dynamic specifications. For example large INL and DNL result in higher noise and distortion in the output signal and tremendously decrease the SNR and SNDR of the DAC. Consequently, we will more focus on the improvement of the linearity of the CSDAC in this work.

In terms of circuit realization, the CSDAC includes both analog and digital blocks. Thus, analog and mixed-signal design flow should be followed in system and block level [68]. The design phase of CSDAC should be completed in the following three levels [49,59]:

1. Architectural level to determine segmentation and required matching among current sources
2. Module level to choose appropriate switching scheme
3. Circuit level to design digital blocks and determine the size of all transistors

Upon design completion of the functional circuits, a floorplan is needed to generate the layout of each block. All verified layouts will be then put together in the system level. Verification of the completed CSDAC layout in different design corners is the last step in the design procedure.

3.4 CSDAC design phase

With reference to the discussions of Section 3.3 and to achieve higher linearity, segmented CSDAC (SCSDAC) was selected in this work. In this Section, the circuit and layout design procedure will be stated. This SCSDAC is designed based on the requirements which are stated in Section 3.2 and listed in Table 3.3, separately.

The decoder in Figure 3.7 has an important role in generating synchronous unary and binary outputs. In fact, it must insert a latency equalizer between the k-bit LSB of the input word and the output binary counterpart. The equalizer should have the same delay as the decoder and synchronizes all output bits ($b_1 \sim b_k$, $u_1 \sim u_{2^m-1}$). Moreover, the decoder needs a significant

physical area which increases by the increase of unary bits (m). On the other hand, the TMI, Figure 3.2, contains the lookup table of the sine samples. Since in the final stage of our project all the SSI sub-modules should be integrated together and in order to avoid the complications of the decoder in the circuit and layout level, the decoder block is eliminated in this work. Therefore, the binary and unary input bits of the SCSDAC are serially received by the Deserializer. Depending on the segmentation, each input data sample is composed of $k + 2^m - 1$ bits.

Based on the above discussion, Figure 3.8 shows the general block diagram of the proposed SCSDAC. CLK_p is the sample rate of the SCSDAC and CLK_s is the bit rate of serial input data. Before loading data into the latch, all serial bits must be pushed into the shift register and settled. Eq. (3.10) states the relation between the frequencies of CLK_p and CLK_s:

$$f_{CLK_s} > \left\{\left[(k + 2^m - 1) \times f_{CLK_p}\right]\right\} \tag{3.10}$$

where *k* and *m* are the number of binary and unary-weighted input bits, respectively. Depending on the segmentation, the shift register should support high bit-rate (f_{CLK_s}) corresponding to the maximum sample rate of 32.17 MHz in Table 3.2.

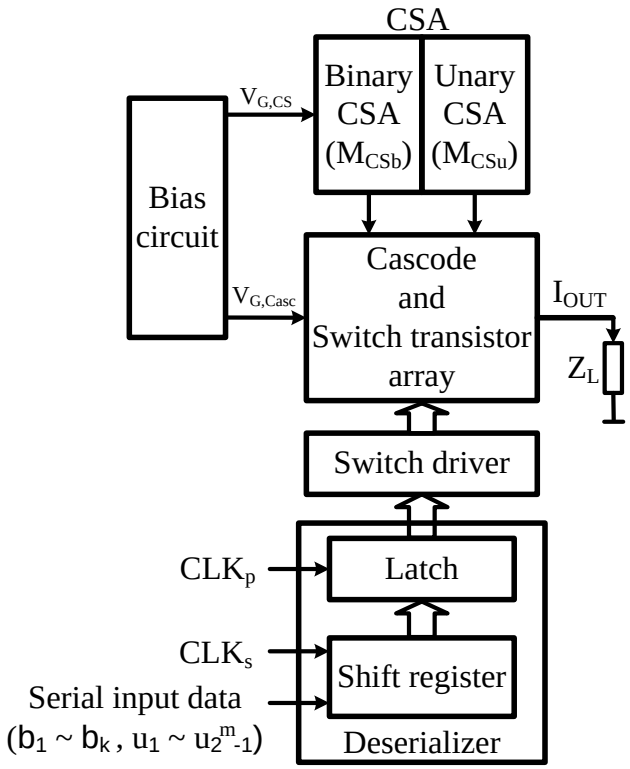


Figure 3.8: General block diagram of the proposed segmented CSDAC

3.4.1 Architectural design

More detailed view of the proposed SCSDAC is depicted in Figure 3.9 where M_1 and M_k are the LSB and MSB current sources of the binary segment, respectively. The other $2^m - 1$ transistors belong to the unary segment and each of them provides the same amount of current. Assuming I_u is the unit current in M_1 (LSB current) and considering the sizing relation among all M_{CS}, the current of the MSB binary branch and each unary branch are $2^{k-1} \times I_u$ and $2^k \times I_u$, respectively.

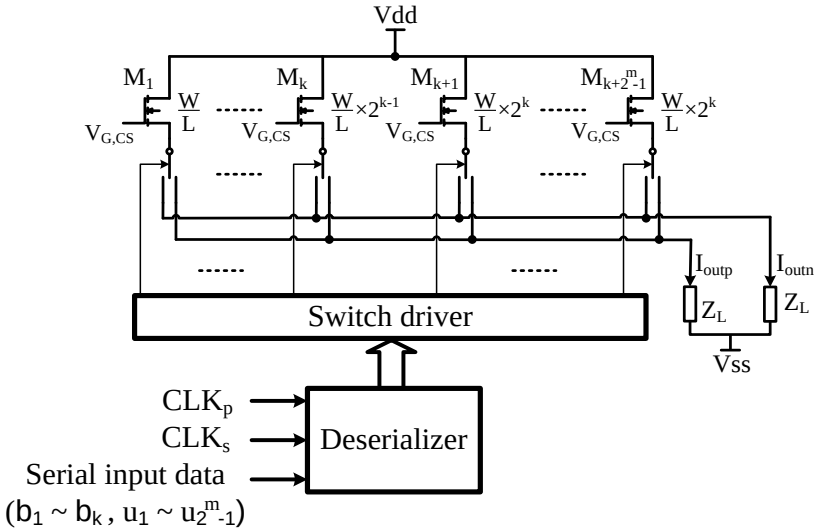


Figure 3.9: Architectural diagram of the SCSDAC

To improve matching among all transistors and to simplify the circuit layout, multiple numbers of paralleled unit transistors (M_1) are used in implementing each M_{CS}. Consequently, $2^{k+m} - 1$ unit transistors are needed to implement SCSDAC. As an example, the proposed 10-bit CSDAC in this work requires 1023 very well matched unit transistors. Such a large number of matched transistors needs a large die area which is one of the major drawbacks of this DAC architecture. Interestingly, total number of M_{CS} is constant for binary-weighted, thermometer-decoded, and segmented CSDAC architectures. Nevertheless, thermometer-decoded CSDAC occupies more area comparing to its binary-weighted counterpart. This is due to employing the decoder and switching scheme techniques which will be discussed later in Section 3.4.2. So, the higher the *m*, the lower the DNL and the larger the die area.

In the first step of the design procedure, the number of binary and unary bits (segmentation) as well as the maximum tolerable mismatch between M_{CS} transistors will be determined. The former

is a matter of tradeoff between die area and linearity (INL and DNL) while the latter depends on the required INL and accuracy of the SCSDAC. Hence, the specific objectives of architectural design phase are the selection of *k*, *m*, and relative Standard Deviation (SD) of unit current matching $\left(\frac{\sigma(I_u)}{I_u}\right)$ [59]. Discussed in [58], random and systematic errors contribute in the current mismatch among M_{CS} transistors and thereupon the INL and DNL. First, the random mismatch effects and consideration will be explained and formulated. The impacts of systematic errors and mismatch compensation methods will be discussed in Sections 3.4.2 and 3.4.3.

In [47], the DNL and INL are related to the maximum mismatch error of the unit current source. Mathematical illustration is as follow:

$$I_j = I_u \pm \varepsilon_j \qquad for\ j = 1,2,3,\dots,2^N - 1 \tag{3.11}$$

where I_j is the current of the j[th] source, I_u is the unit current, ε_j is the mismatch error, and *N* is the total number of bits. If the DAC has to be designed for maximum INL of INL_{Req}, then:

$$|\varepsilon|_{max,INL} = \frac{INL_{Req}}{2^{N-1}} \tag{3.12}$$

where $|\varepsilon|_{max,INL}$ is the maximum tolerable mismatch error of all sources which results in INL_{Req}. This maximum error is independent of the implementation type of the CSDAC. However, the maximum tolerable error to achieve DNL_{Req} depends on the implementation type. For binary-weighted CSDAC:

$$|\varepsilon|_{max,DNL} = \frac{DNL_{Req}}{2^{N-1}} \tag{3.13}$$

While for the fully thermometer-decoded CSDAC:

$$|\varepsilon|_{max,DNL} = DNL_{Req} \tag{3.14}$$

In Eqs. (3.12-14), the worst case INL and DNL are calculated for $2^N - 1$ current sources.

Similarly, if Gaussian mismatch error distribution is assumed among $2^N - 1$ current sources, the maximum SD of the INL will be the same for both binary-weighted and thermometer-decoded CSDACs. It can be formulated as a function of the SD of unit sources [71].

$$\sigma_{INL,max} = \frac{1}{2}\sqrt{2^N - 1}\,\sigma_\varepsilon \cong 2^{\frac{N}{2}-1}\sigma_\varepsilon \tag{3.15}$$

where $\sigma_{INL,max}$ is the maximum SD of the INL, and σ_ε is the SD of the unit current source. As an example, σ_ε must be $\frac{1}{32}$ LSB to have an σ_{INL} of 0.5 LSB in the targeted 10-bit DAC. The maximum SD of DNL for binary-weighted $(\sigma_{DNL,max,b})$ and thermometer decoded $(\sigma_{DNL,max,u})$ CSDAC can also be calculated:

$$\sigma_{DNL,max,b} = 2^{\frac{N}{2}}\sigma_\varepsilon \tag{3.16}$$

$$\sigma_{DNL,max,u} = \sigma_\varepsilon \tag{3.17}$$

In [65], the relation of the transistor size and the accuracy of the current is illustrated.

$$A_{tr} \propto \frac{1}{(\sigma_\varepsilon)^2} \tag{3.18}$$

where $A_{tr}$is the unit transistor area and σ_ε is the SD of unit current. Eqs. (3.15-18) provide the segmentation basis of CSDAC. Based on these relations, authors in [67] listed the SD of INL and DNL as well as area requirements for different INL values in 10-bit binary-weighted and thermometer-decoded CSDACs. The requirements are summarized in Table 3.4 in which σ and A_{unit} are the SD of unit current and the minimum needed area for obtaining $DNL = 0.5\ LSB$ in a thermometer-decoded CSDAC. Since we replaced the decoder of Figure 3.7 with a deserializer, $A_{DES}$is reported in this table as the physical area of the 10-bit shift register and latch.

Table 3.4: Binary and unary-weighted 10-bit CSDAC requirements [67]

Specification	**Binary weighted**	**Unary-weighted**[1]
INL	16σ	16σ
DNL	32σ	σ
Area (INL=0.5 LSB)	$256A_{unit}$	$256A_{unit}$
Area (DNL=0.5 LSB)	$1024A_{unit}$	A_{unit}
Deserializer area	A_{DES}	2^9A_{DES}

[1] Unary-weighted and thermometer-decoded are equivalent terms

Eq. (3.18) implies the use of larger unit transistors for getting lower variance of unit current and higher DAC accuracy. Therefore, the chip area is mostly dominated by the size of the CSA. Acquiring high-speed performance results in small size switch transistors, but the chip area is significantly increased as a result of large number of M_{Casc}, M_{SW}, and switch driver in unary

implementation as well as the area overhead due to the interconnect lines. As listed in Table 3.4, the area of the digital deserializer should be taken into account in segmentation of a CSDAC.

Along with increasing DAC linearity, the THD of the DAC output is decreasing for unary-weighted DAC realization. This fact is due to the reduction of glitch energy for smaller step sizes in unary-weighted comparing with binary-weighted CSDAC type [67]. Hence, the main challenge in the design of SCSDAC is the tradeoff between the chip area on one hand and the THD and linearity on the other hand.

Despite the fact that the chip area does not impose any limitation on this work, die area is tried to be optimized. Using the methodologies presented in [59,67], we determined maximum number of 4-bits in the binary-weighted segment. Thus, 6-bits will be implemented as unary-weighted in the proposed SCSDAC. Obviously, assigning more bits to the unary segment improves the DNL, however, the area will be tremendously increased.

Relative SD of the unit current source is the other specification which should be determined in this phase of the design. Based on the assumption of Gaussian random mismatch distribution, the percentage of DACs falling within certain bounds around a mean value can be found by using Eqs. (3.15-17). The major DAC parameter to be calculated in this way is the *INL yield* which is the ratio of the number of DACs with smaller INL than INL_{Req} to the total number of DACs [52,71]. Depending on the design technology, Monte Carlo simulation must be performed to accurately calculate INL yield. To avoid long simulation time, Bosch et al developed a formula in [52,72] in order to estimate relative SD as a function of INL yield and DAC resolution.

$$\frac{\sigma(I)}{I} \leq \frac{1}{2C\sqrt{N}} \quad with \quad C = inv\_norm\left(0.5 + \frac{yield}{2}\right) \tag{3.19}$$

where $\frac{\sigma(I)}{I}$ is the relative SD of the unit current source, *inv_norm* is the inverse cumulative normal distribution, and *N* is the DAC resolution. Using Eq. (3.19), achieving INL yield of 99.7%, 50%, and 10% needs relative SD of 0.5%, 1.3%, and 1.9%, respectively [72]. Regarding to the high accuracy level of the SCSDAC, high INL yield of 99.7% is selected in this work. This implies a relative SD of 0.5% for each unit current source.

In [65], it is expressed that $\frac{\sigma(I)}{I}$ is inversely proportional to the gate overdrive voltage ($V_{GS} - V_{th}$) and gate area ($W \times L$) of M_{CS}. Exact illustration is unique for each technology. Respecting

this relation, large gate area compensates random mismatch caused by process variations. Furthermore, the gate overdrive voltage should be kept as high as possible to ensure that threshold voltage does not dominate the relative SD. Otherwise, larger gate area will be needed to achieve desired matching [52,53,54,57,59].

3.4.2 Module design

Switching scheme is another design parameter of unary-weighted CSDAC in which large number of similar current sources is distributed in CSA. In order to compensate the systematic mismatch errors among these sources, careful switching scheme must be designed at the module level design phase. There are two components related to switching scheme: (1) Splitting current source transistors (M_{CS}) and spreading them across the CSA; (2) Developing an appropriate switching sequence for switching on/off different current sources in the CSA according to the digital input data. Although the relative SD of random mismatch error is minimized in architectural design of the CSDAC, accumulation of the cell errors degrades the INL [58,59].

First of all, the systematic mismatch error distribution and the impact of error accumulation on the INL should be illustrated. As a matter of fact, INL and DNL are used to define the deviation of data converter's real transfer function from the ideal one. Eq. (3.11) expresses the current of the j^{th} current source of a CSA in the unary-weighted CSDAC with 2^N -1 elements. The INL and DNL of a CSDAC implemented by the fully unary CSA, can then be derived as follows:

$$INL_{CSDAC} = \max\{|INL(k)|\} \cong \max\left\{\left|\sum_{j=1}^{k} \varepsilon_j\right|\right\} \tag{3.20}$$

$$DNL_{CSDAC} = \max\{|DNL(k)|\} \cong \max\{|\varepsilon_k|\} \tag{3.21}$$

where *k* determines the number of switched on sources for a given input code and equals to the N-bit digital input code ($1 \leq k \leq 2^N - 1$). INL(*k*) and DNL(*k*) represent the resulted nonlinearities for that input. Thus, in addition to individual error of each source (ε), the total number (*k*) and the accumulated error of the switched-on sources affect the INL. Considering that "ε" can be of a negative or a positive value, appropriate switching sequence can prevent the accumulation of errors and may improve the INL. In contrast, the DNL does not depend on the number of activated current sources and therefore, it is not affected by the switching sequence of the CSA [58].

The systematic errors in a CSA can be approximated using first and second order of a Taylor series expansion around the center of the array. This expansion represents linear, quadratic, and joint gradients over the CSA that can be expressed by Eqs. (3.22), (3.23), and (3.24), respectively.

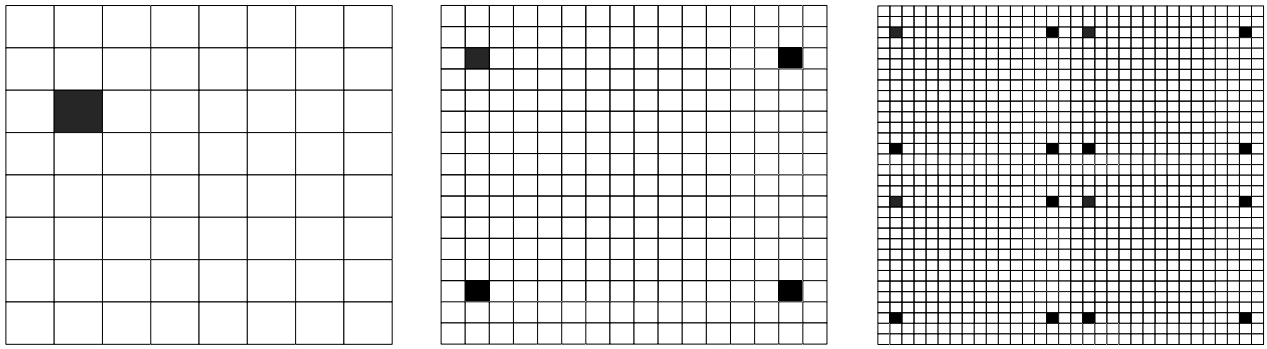
$$\varepsilon_l(x,y) = (g_l \times \cos\theta \times x) + (g_l \times \sin\theta \times y) \tag{3.22}$$

$$\varepsilon_q(x,y) = g_q \times (x^2 + y^2) - a_0 \tag{3.23}$$

$$\varepsilon(x,y) = w * \varepsilon_l(x,y) + \varepsilon_q(x,y) \tag{3.24}$$

where *x* and *y* are the coordinates of each source in the CSA. θ and g_l are the angle and the slope of the linear gradient component of the error, while a_0 and g_q are technology dependent parameters. The θ may vary randomly, but the maximum linear error occurs when θ is equal to 45º or 135º. "*w*" specifies the ratio of the linear to the quadratic gradient error in the joint error and for simplicity has been set to 1 in this paper [53,58,62].

Considering Eqs. (3.22-24), both components of a switching scheme tend to average the systematic and graded errors. While splitting unary transistors averages the systematic mismatch errors, proper switching sequence reduces the accumulation of averaged error. Based on Eqs. (3.20,21), splitting M_{CS} units improves both INL and DNL, however, switching sequence can only ameliorate the INL. Figure 3.10(a) shows an example of an 8×8 unary CSA where each M_{CS} is implemented as 1 unit. This unit has been split into 4 and 16 parallel units in Figure 3.10(b) and (c), respectively. Parallel units are symmetrically laid out across the CSA. Although this technique averages the error of each unit, the making interconnections needs large area and complicated layout. Due to these complications, each M_{CS} is divided into 4 parallel elements in this work.



(a) (b) (c)

Figure 3.10: Splitting unary M_{CS} in an 8×8 CSA; (a) No split; (b) Split by 4; (c) Split by 16

As can be inferred from Figure 3.10, the physical size of the CSA is determined by the size of M_{CS} transistors and the choice of switching scheme. Nevertheless, the CSA has been analyzed as an square in the literature. In general, the array is distributed in physical dimensions of $X_a \times Y_a$ such that:

$$Y_a = r \times X_a \tag{3.25}$$

where X_a and Y_a are the length and width of the laid-out CSA and r is the ratio between them. Clearly, a CSA with square distribution pattern is an especial case of Eq. (3.25) in which $r = 1$. For an $M \times M$ (rows by columns) array of current sources, the geometric positions (x and y) of each M_{CS} in the array are listed as below:

$$x \in \left\{-1, \left(-1 + \frac{2}{M-1}\right), \left(-1 + \frac{4}{M-1}\right), \dots, \left(1 - \frac{2}{M-1}\right), 1\right\} \tag{3.26}$$

$$y \in \left\{-r, \left(-r + \frac{2r}{M-1}\right), \left(-r + \frac{4r}{M-1}\right), \dots, \left(r - \frac{2r}{M-1}\right), r\right\} \tag{3.27}$$

Thus, to validate the performance of each sequence, a more accurate model of the gradient errors for the targeted CSA should be developed [58].

A variety of switching sequences have been designed and developed for SCSDACs [53,58,62,63,64]. Simulations by MATLAB were performed to show the dependency of switching sequence performance to the dimensions of the CSA. To highlight this relation, the effects of other factors in the design of switching protocol such as higher order gradient errors, different ratios of linear to quadratic errors, splitting current sources, and non-zero-average error profiles have not been discussed in this paper. Moreover, in order to evaluate the performance of each sequence, the maximum accumulated error is considered as a representation for the INL of the DAC.

Here, square and non-square distribution patterns for implementing a given CSA structure are considered. Different normalized distributions of simulated joint gradient error for a 16×16 array of current sources are depicted in Figure 3.11. The distribution in a square-implemented CSA is shown in Figure 3.11(a), while Figure 3.11(b) and (c) show the distribution for the same CSA, implemented using non-square patterns. These two values are selected as an example. The array dimensions are also normalized in the x and y directions in Figure 3.11. The linear and quadratic components of joint error are calculated such that to result in a zero-mean normalized joint gradient error [62]. Figure 3.11 reveal that different accumulated errors can be expected from the

given array with a unique switching strategy, depending on the implied distribution array whether to be square or non-square.

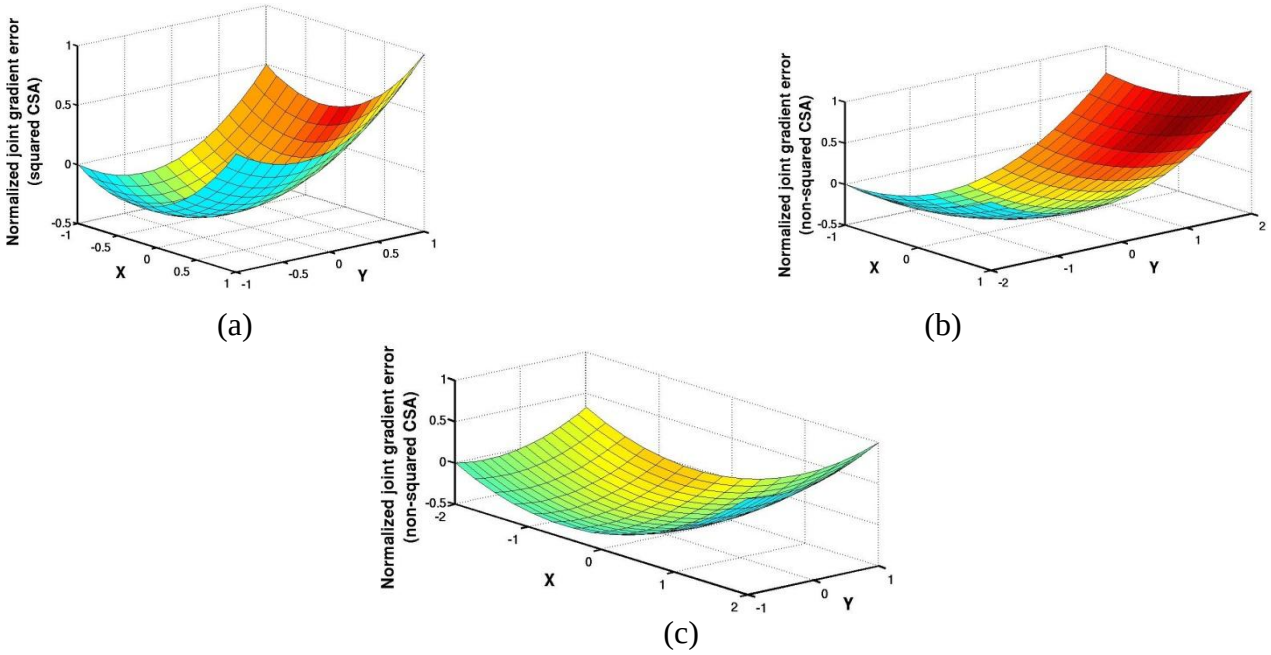


Figure 3.11: Normalized distribution of joint gradient error for a 16×16 CSA; (a) Square CSA ($r = 1$); (b) Non-square CSA ($r = 2$); (c) Non-square CSA ($r = 0.5$) [58]

Optimized switching sequences are mainly selected in a symmetrical manner or based on experimental measurements of test chips implemented with the same process. The evaluation criteria of the different switching sequences are the minimization of the accumulated gradient error in the applied distribution pattern for the current sources. Various sequences of the well-known symmetrically-designed row-column switching scheme for a single row of the array is shown in Figure 3.12(a, b, c) in which the numbers show the order of both row and column activation. To deliver its current to the DAC output, each element of the CSA is switched on according to its row-column addresses in the 16×16 matrix [62]. On the other hand, in the Q^2 random walk sequence [53], the CSA is divided into 16 regions, whereas each region contains 16 elements. In this sequence, current sources are switched on sequentially as per the order shown in Figure 3.12(d). These sequences are used to show the impact of the CSA dimension and related gradient error distribution on the performance of the DAC.

15 13 11 9 7 5 3 1 2 4 6 8 10 12 14 16

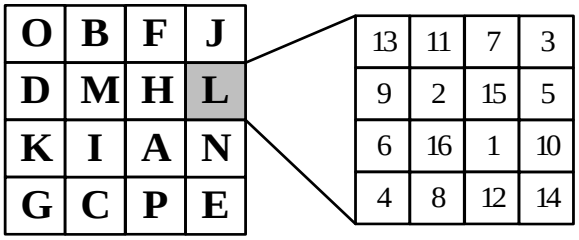
(a)

14 10 6 2 1 5 9 13 15 11 7 3 4 8 12 16

(b)

15 11 7 3 1 5 9 13 14 10 6 2 4 8 12 16

(c)



(d)

Figure 3.12: Switching sequences for a 16×16 CSA; (a) Symmetrical sequence (b) Hierarchical-symmetrical sequence (Type A) (c) Hierarchical-symmetrical sequence (Type B) (d) Q^2 random walk sequence [58]

The results of MATLAB simulations for different sequences have been tabulated in Table 3.5. The presented data are the maximum accumulated error achieved by simulating the activation order of 0 to 256 current source units simultaneously based on different sequences. Being corresponded to the INL, these data are the summation of normalized errors presented in Figure 3.11.

Table 3.5: Maximum Accumulated Error in 16×16 CSA

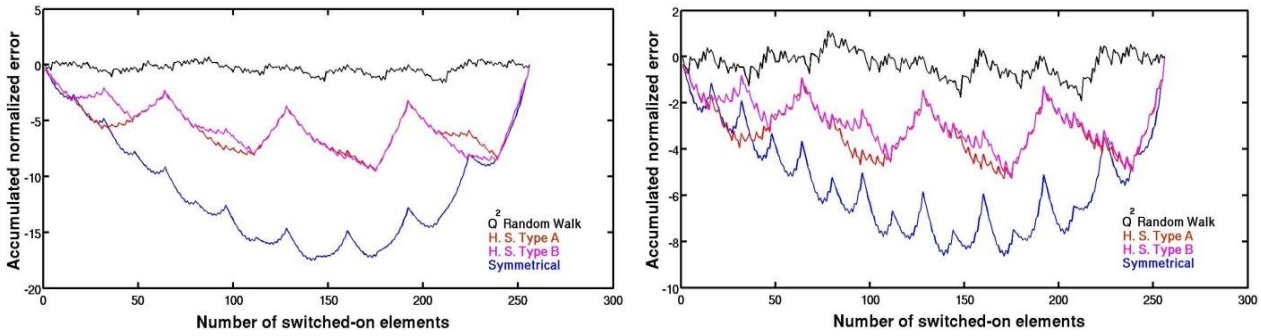
Simulated sequences	**Accumulated normalized error**		
	Squared CSA Figure 3.11(a)	**Non-Squared CSA Figure 3.11(b)**	**Non-Squared CSA Figure 3.11(a)**
Symmetrical	17.54	26.84	8.63
H. S.[1] (Type A)	9.48	13.70	5.29
H. S. (Type B)	9.50	13.80	5.20
Q^2 random walk	1.59	1.61	1.91

[1]. Hierarchical Symmetrical

According to the results in Table 3.5, the performance of each sequence is a function of physical realization of the CSA. E.g. when Q^2 random walk sequence is used, the accumulated error is increased by almost 20% in non-square patterns. While in symmetrical sequences, the error is significantly reduced when the CSA is implemented using the pattern of Figure 3.11(c) and is increased when implementation as of Figure 3.11(b) is considered. There is no properly related

discussion provided in literature to be used for the justification of the outcomes. It should be noted that inaccurate gradient error interpretations may lead to unexpected test results [58].

Figure 3.13 compare accumulated error for different number of switched-on current sources in the 16×16 CSA. Here, the same gradient error distributions and switching sequences as tabulated in Table 3.5 are considered. These graphs further reveal that the accumulation of the gradient error corresponds to the dimensions and the geometry of the CSA, as well as the physical position of every element in the array. Therefore, this effect should be considered as an integrated part of the strategy for implementing a current steering DAC with a given INL. As seen in Figure 3.13, the Q^2 random walk shows the best performance among the basic sequences which were considered in our simulations. However, erroneous gradient error interpretation may unlikely lead to the selection of inappropriate sequence when well-optimized sequences are being compared [58].



(a) (b)

Figure 3.13: Accumulated normalized error in 16×16 CSA;
(a) Square CSA; (b) Non-square CSA $(r = 0.5)$

In brief, in absence of reliable data on the behavior of the CSA against the random and systematic error patterns, the switching sequence efficiency may be somehow estimated using the learning obtained from the distribution of the laid-out CSA. Otherwise, test results may not be satisfactory as they unexpectedly lack accuracy. Thus, adequate sequence for each DAC should be exclusively designed based on the size of the transistors, process characteristics, and the arrangement of the CSA. This implies a recursive approach for the optimum sequence with the consideration of physical arrangements of the current source transistors [58].

In addition to the switching scheme, layout design techniques can also be employed to reduce systematic mismatch errors. In this regard, adding dummy devices to avoid edge effects,

providing wide power/ground lines to eliminate voltage drop across chip, and using cascode transistor (M_{Casc}) to increase output resistance of the unit source are adopted in this work.

One of the advantages of using deserializer instead of decoder is that the switching sequence can be changed after fabrication of SCSDAC. As part of the proposed block diagram in Figure 3.8, the position of input data in the shift register is shown in Figure 3.14. At any cell of this register, a logical high switches on corresponding current source in the unary or binary-weighted segments. b_i and u_i notations represent binary-coded and thermometer-coded input data. The SCDAC is segmented into 4-bits of binary and 6-bits of unary format. In this case, the CSA includes 63 unary sources each of which are split into 4 parallel units and results in 16×16 array of similar transistors. In fact, the order of serial data bits determines the unary sources that will be switched on. Hence, the switching sequence might be further optimized based on the test results.

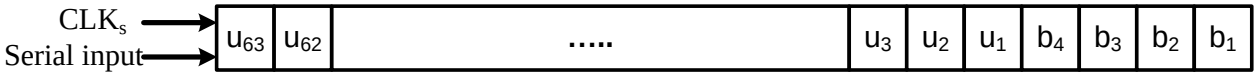


Figure 3.14: The position of input data in the shift register

Nevertheless, MATLAB simulations were done to find optimized symmetrical switching sequence after sizing unit transistor in unary segment of proposed SCSDAC. In these simulations, normalized linear and quadratic gradient mismatch error with an average of zero was taken into consideration. The accumulated error for different symmetrical sequences of 63 unary sources were simulated and compared. Table 3.6 illustrates the selected sequence which resulted in the lowest accumulated error. Highlighted cell is used for the bias transistor.

Table 3.6: Selected switching sequence in this work

38	22	26	41	b	25	21	37
6	53	57	10	9	56	52	5
14	61	49	2	1	48	60	13
45	30	18	34	33	17	29	44
47	32	20	36	35	19	31	46
16	63	51	4	3	50	62	15
8	55	59	12	11	58	54	7
40	24	28	43	42	27	23	39

3.4.3 Circuit design

In this phase, the circuit of the SCSDAC will be designed. It includes: (1) Bias and unit current values; (2) The size of M_{CS}, M_{Casc}, M_{SW}, and transistors in digital blocks; (3) Output resistance of each unit source; (4) Proper switch driver circuit. Both static and dynamic performance should be taken into account in design procedure [59]. With regard to the specific application of this work, the main concern is the accuracy and linearity in low frequency signal generation. However, dynamic performance should be optimized for the maximum sample rate mentioned in Table 3.2.

In terms of static performance, the SCSDAC must be designed for optimized behavior against random and systematic mismatch errors. At first, unit current, INL yield, gate overdrive voltage of M_{CS}, and size of transistors are determined to minimize the effects of random errors. To reduce the impacts of systematic errors, increasing output resistance of each source, setting the poles of the frequency response, and using layout design techniques have to be considered [59,73].

Figure 3.15 depicts details of the SCSDAC. Four LSBs and six MSBs are implemented in binary and unary segments, respectively.

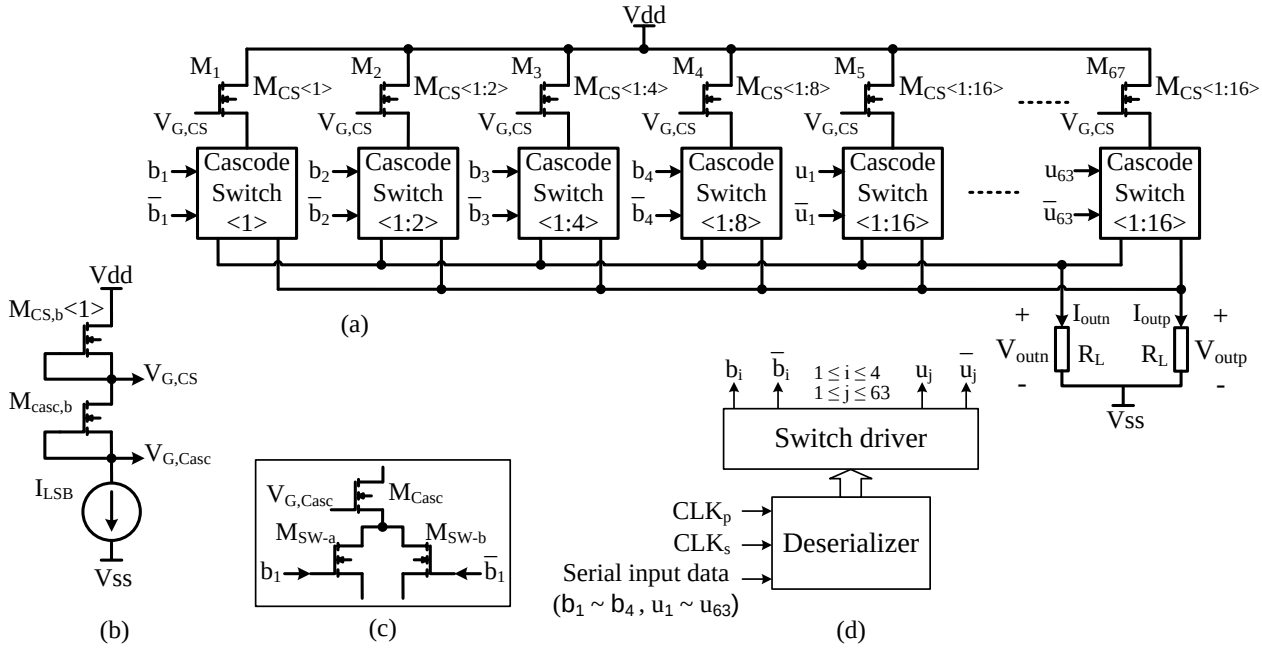


Figure 3.15: Detailed diagram of the proposed SCSDAC;
(a) DAC core; (b) Bias circuit; (c) Cascode and switch cell; (d) Deserializer and switch driver;

In Figure 3.15(a), the current in M_1 branch represents the unit current (I_{LSB}). Other current source branches are composed of several unit sources in parallel. The number of paralleled elements is shown in angle brackets. One M_{Casc} and two M_{SW} form a cascode-switch cell in the M_1 branch, shown in Figure 3.15(c). This cell is also repeated in higher order branches. Bias voltages of all M_{CS} and M_{Casc} transistors are provided by bias circuit in Figure 3.15(b) which is a stable β-multiplier reference circuit. Switch driver has to generate two on/off commands for $M_{SW\text{-}a}$ and $M_{SW\text{-}b}$. In order to prevent glitches at the drain node of M_{CS} and M_{Casc}, at least one of the two switches should be on at any time. The synchronization between on/off commands of each branch is the major challenge in the design of switch driver shown in Figure 3.15(d) [47,59].

Using large M_{CS}, the unit current source is forced to meet the criteria in Eq. (3.19). That is:

$$\frac{\sigma(I_{LSB})}{I_{LSB}} \leq 0.5\% \tag{3.28}$$

Additionally, unit current is related to the Full-Scale current (I_{FS}) or swing voltage (V_{swing}) [59].

$$I_{LSB} = \frac{V_{swing}}{2^N \times R_L} \tag{3.29}$$

$$I_{LSB} = \frac{I_{FS}}{2^N} \tag{3.30}$$

where R_L is the load resistor. Considering, the cascode and switch transistors in M_1 branch:

$$V_{SD,CS} + V_{SD,Casc} + V_{SD,SW} + V_{swing} = V_{dd} \tag{3.31}$$

where $V_{SD,CS}, V_{SD,casc}, V_{SD,SW}$ are the source-drain voltages of current source, cascode, and switch transistors, respectively. Eq. (3.31) reveals that higher V_{swing} restricts the headroom of the bias voltage of M_{CS} and M_{Casc} ($V_{GS} - V_{th}$). Higher gate overdrive voltage is preferred to reduce the mismatch effects due to threshold voltage variations. Thus, lower V_{swing} should be selected or the DAC output must be virtually connected to ground by using a current buffer shown in Figure 3.16. Moreover, switch transistors should remain in saturation for the maximum output voltage.

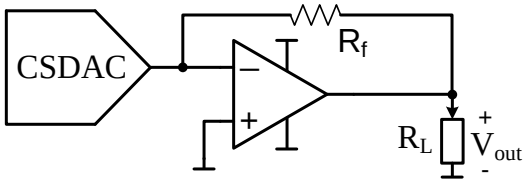


Figure 3.16: Current buffer

Finite output impedance of current sources is an important source of systematic and graded errors. In [48,59,73], analyses have been performed to characterize this phenomenon. Assuming ideal current sources in the SCSDAC of Figure 3.15(a):

$$I_{outp} = \left(I_{LSB} \times \sum_{i=1}^{4} 2^i \times b_i\right) + \left(2^4 \times I_{LSB} \times \sum_{j=1}^{63} u_j\right) = X \times I_{LSB} \qquad (3.32)$$

where X is the digital input code, I_{LSB} is the unit current value. However, output impedance is a finite value which is reducing as output signal frequency increases. Ideal and non-ideal circuit models are shown in Figure 3.17, where $R_{out}(X)$ is the input-dependent equivalent impedance of the switched-on current sources, $I_{loud,i}$ and $I_{loud,ni}$ are ideal and non-ideal load currents.

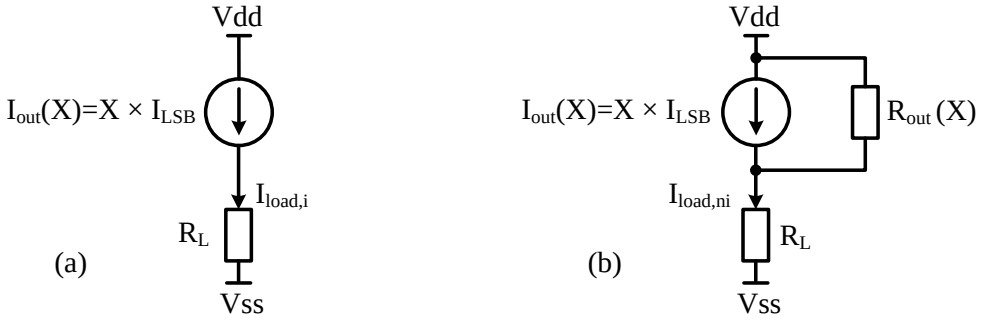


Figure 3.17: CSDAC model: (a) Ideal current sources; (b) Non-ideal current sources

In [48], the impact of non-ideal current sources on the INL is formulated:

$$INL = \frac{R_L\left(2^N - 1\right)}{4 \times R_{out,LSB}} \qquad (3.33)$$

where N is the number of bits and $R_{out,LSB}$ is the finite output impedance of LSB current source. Two poles are formed by the capacitors at drain nodes of M_{CS} and M_{Casc}. In lower output frequencies series combination of M_{Casc} and M_{SW} results in a very high $R_{out,LSB}$. As frequency increases, the effects of these two poles appear as decrease of $R_{out,LSB}$. To overcome this problem, the poles must be moved toward higher frequencies. This can be done by using layout techniques and smaller size transistors. However, M_{CS} has to be a large transistor to reduce mismatch and displacement of its pole which is dominant, is not possible. Hence, careful attention should be paid in designing the layout of M_{Casc} drain node.

There is also another tradeoff between $R_{out,LSB}$ and I_{LSB}. While higher I_{LSB} improves SNR [73], increasing I_{LSB} degrades $R_{out,LSB}$; since it is inversely proportional to the $r_{o,M_{CS}}$ and $r_{o,M_{Casc}}$. In

addition, larger channel length (L) of MCS results in higher $r_{o,M_{CS}}$ and higher $R_{out,LSB}$. In terms of dynamic performance, limited $R_{out,LSB}$ affects dynamic performance. According to [73]:

$$SFDR \cong 20log\left(\frac{R_{out,LSB}}{R_{load}}\right) - 6(N-2) \quad (3.34)$$

In the applications that SFDR matters, Eq.(3.34) can be used in adjusting $R_{out,LSB}$.

In the design of the latch and switch driver, perfect synchronization required between complementary switch commands ($b_i/\bar{b}_i$ and $u_i/\bar{u}_i$) for ameliorating dynamic performance. Such synchronization reduces digital input signal and clock feedthrough to the output node [59].

Considering all the constraints and tradeoffs, the designed parameters are tabulated in Table 3.7. Monte-Carlo simulations were also performed to ensure the relative SD of the I_{LSB} and INL yield.

Table 3.7: Designed parameters of the proposed SCSDAC

Parameter			**Designed specification**	**Unit**
Definition		**Symbol**		
Output frequency range		f_{out}	1 ~ 10	kHz
Sample rate		f_s	< 3.2	MHz
Technology		–	CMOS 0.13µm	–
Power supply		V_{dd}	1.2	V
Resolution		N	10	bit
Unary-segment		–	6	bit
Binary segment		–	4	bit
Unit current		I_{LSB}	1	µA
Full scale current		I_{FS}	1023	µA
Output resistance		R_L	100	Ω
Full scale swing		V_{swing}	102.3	mV
Switching scheme		–	Splitting M_{CS} by 4	–
		–	Sequence of Table 3.6	–
Switch driver structure		–	Non-overlapping clock generator	
M_{CS}	Width	W_{CS}	16	µm
	Length	L_{CS}	18	µm
M_{Casc}	Width	W_{Casc}	1.2	µm
	Length	L_{Casc}	0.5	µm
M_{SW}	Width	W_{SW}	0.2	µm
	Length	L_{Casc}	0.2	µm

[1] Based on Monte-Carlo simulations

3.4.4 Layout design

Although smaller blocks must be designed first in hierarchical design methodology, both top-down and bottom-up design strategies are necessary in schematic and layout design of the targeted SCSDAC. After generation of sized circuits, schematic simulations, and design optimization, layout of all blocks are individually generated using Cadence Virtuoso Layout XL. The floorplan is outlined with reference to the estimated area for main building blocks. Shown in Figure 3.18, the CSA is tried to be laid out at the center of the die. To be far from digital blocks, the bias circuit is placed at the top of the chip. Separate power supply pads are considered for different blocks. The switch driver is placed very close to cascode and switch array to improve the synchronization of switch commands [59]. Since the parasitic capacitor at drain node of M_{Casc}, tremendously degrades output resistance of the current source, M_{Casc} and M_{SW} should be very close to reduce metal connection between them. Wide power and ground lines and dummy elements in the CSA have to be used to ameliorate the linearity. On-chip decoupling capacitors are also used to get more stability [69,70,74]. Layout view of SCSDAC is shown in Figure 3.19.

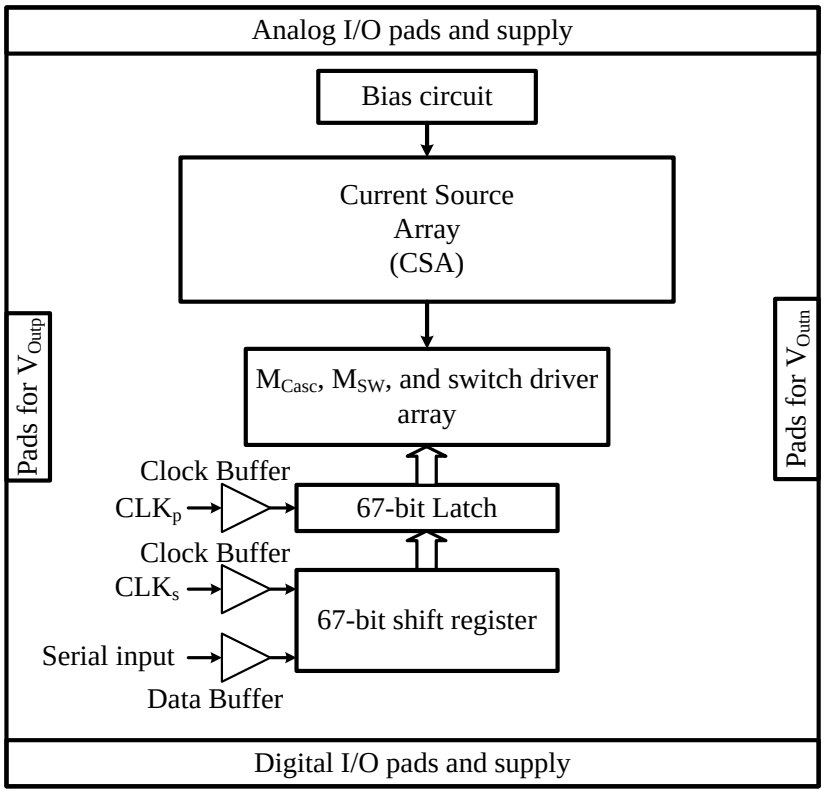


Figure 3.18: SCSDAC floorplan

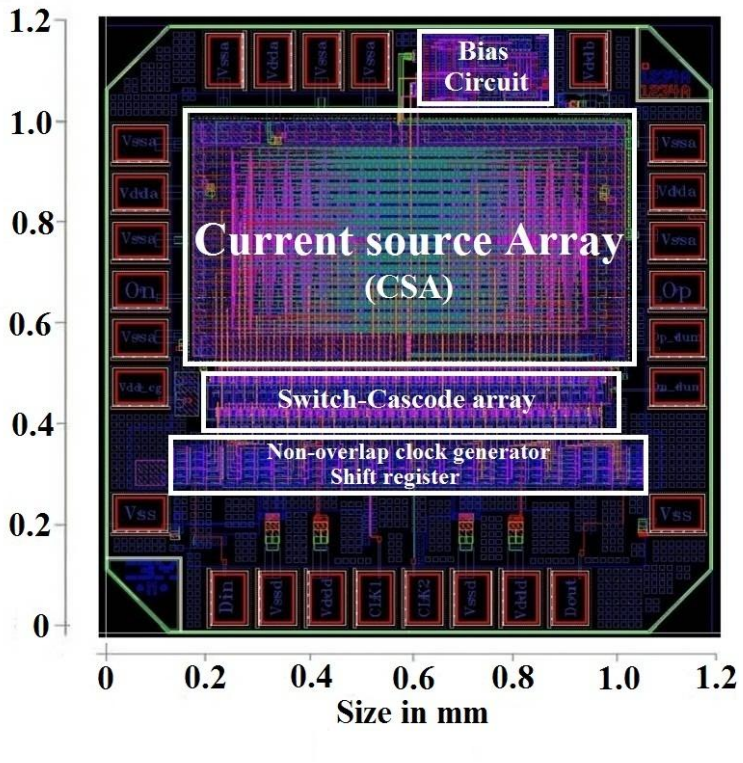


Figure 3.19: Designed layout of the SCSDAC

3.5 Conclusion

In this chapter, complete design procedure of a 10-bit SCSDAC dedicated to excitation signal generator path of a smart sensor interface was presented. This DAC is part of the ESG which was systematically designed. The design specifications were extracted from the system level architecture and requirements of the ESG. Based on the desired parameters, the SCSDAC was hierarchically designed in four individual stages: (1) in architectural level, DAC was segmented into binary-weighted and thermometer-decoded sections; (2) in module level, proper switching scheme was discussed and the impacts of CSA size on the performance of switching sequences were introduced; (3) in the circuit level, the transistors are sized based on the required static and dynamic performance; (4) layout floorplan and challenges is explained as the last stage of the design. In the next chapter, the testing and measurement techniques for digital to analog converter will be described which will be followed by simulation and measured results of the fabricated chip.

CHAPTER 4

SIMULATION AND MEASUREMENT RESULTS

4.1 Introduction

The proposed SCSDAC was designed, simulated, and fabricated in IBM-PDK CMOS 0.13µm technology. The complete schematic and layout design procedure and considerations were presented in chapter 3. In addition to the design steps which are defined in the literature, the impact of physical implementation of the CSA on the linearity of the CSDAC is also introduced as a new design consideration.

In this chapter, detailed simulation and measurement results of the individual building blocks and the whole chip are presented. General basis and techniques of testing DACs are reviewed in Section 4.2. Then, schematic and post-layout simulation results are discussed in Section 4.3 which is followed by measurement achievements in Section 4.4.

4.2 DAC testing techniques

Considering the specifications of the DAC, listed in Table 3.3, two test setups are required for measuring static and dynamic parameters. Precision multimeter with current and voltage measurement capability is the most important equipment in the static DAC testing while a high-speed oscilloscope and a spectrum analyzer are needed in dynamic testing of DAC performance. Figure 4.1 illustrates the static and dynamic test bench setup in this work. In static testing, after latching any input code (67-bit of data corresponding to a 10-bit binary word) in the deserializer block of the proposed SCSDAC, the differential output current should be precisely measured. The output current can be converted to voltage by using two high-precision load resistors. Proper input codes must be sequentially and periodically applied to the deserializer in order to measure

the dynamic specifications of the generated analog signal by the SCSDAC. Shown in Figure 4.1(b), high-speed oscilloscope and spectrum analyzer are used to measure time and frequency domain specifications. Here, level shifter block is required to convert the digital high voltage level of the FPGA platform into 1.2 V which is the standard supply voltage in IBM 0.13µm CMOS process.

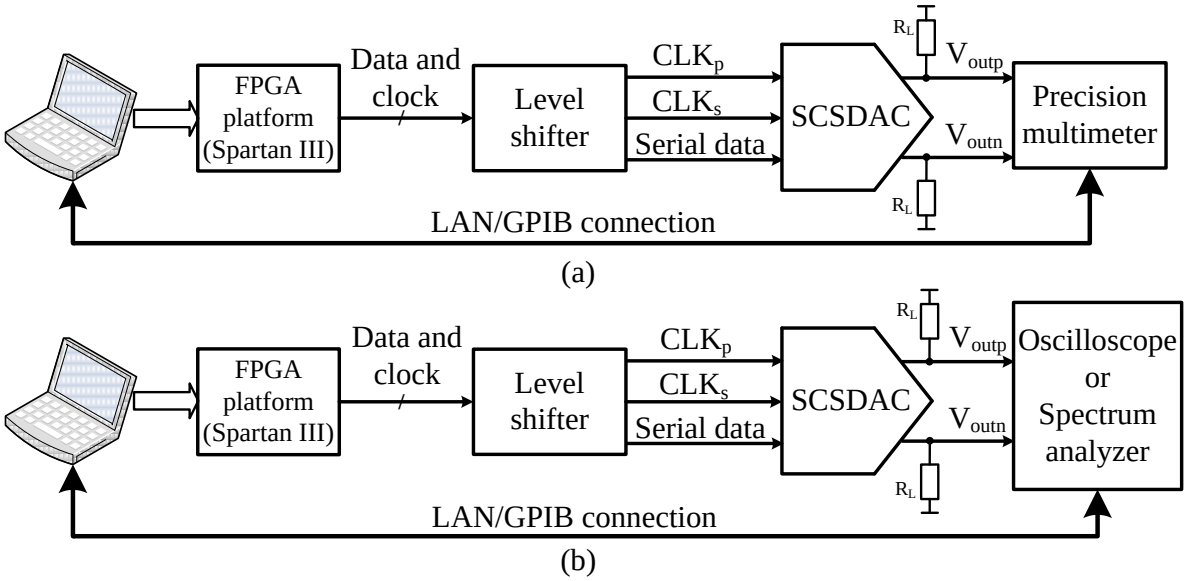


Figure 4.1: Test bench setup for DAC measurement; (a) Static testing; (b) Dynamic testing

4.2.1 Static specification measurement

Monotonicity, offset error, gain error, and INL are the most important specifications which represent the static accuracy of DAC [49]. If DAC output increases or hold its value for an increasing digital input data, the DAC will be monotonic. The DNL can be used as an indication of monotonicity. In CSDACs, offset error is the output voltage corresponding to all "0"s code.

$$V_{OS} = V_{all\ zero} \tag{4.1}$$

where V_{OS} is the offset voltage and $V_{all\ zero}$ is the DAC output for all "0"s code.

In an ideal CSDAC, the outputs for all "0"s code and all "1"s code are zero and $V_{FS} - V_{LSB}$, respectively. The line which connects these two end-points is the ideal transfer function and its slope is the ideal gain of the DAC. The slope of the measured transfer function indicates the real

gain. Deviation of real gain from ideal expected gain is the gain error. V_{OS} must be cancelled in calculating gain error.

$$Gain\ error\ (\%) = 100 \times \left[\frac{V_{all\ one} - V_{OS}}{V_{FS} - V_{LSB}} - 1\right] \tag{4.2}$$

where $V_{all\ one}$ is the DAC output for all "1"s code, and V_{FS} is the full scale output current which is equal to $2^N \times V_{LSB}$. The offset and gain errors are shown in Figure 4.2 [49].

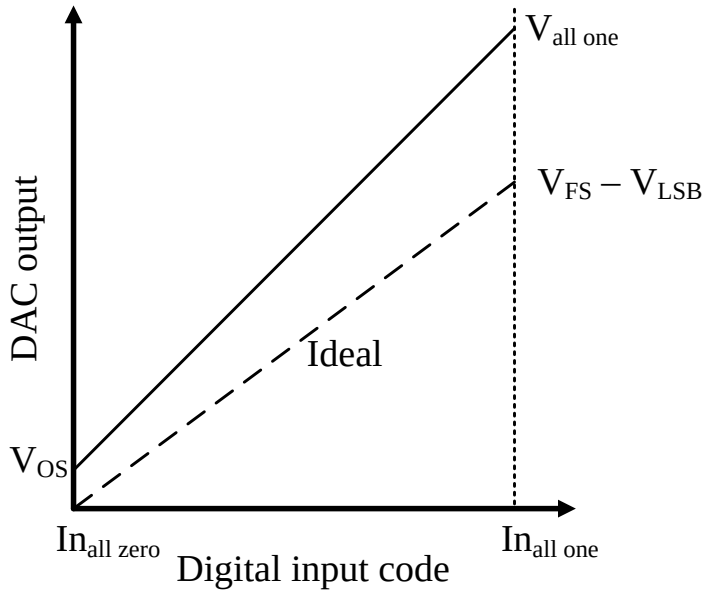


Figure 4.2: Offset and gain errors in CSDAC

The linearity of the DAC is measured based on the real transfer function. In general, calculation of DNL and INL is a time consuming procedure since all combinations of the input code must be applied to the DAC and the corresponding output is measured. In binary segment of the SCSDAC where the error of each bit does not affect the error of other bits, *superposition* can be used in order to reduce the number of test cases for measuring linearity. In contrast, superposition cannot be applied to the unary-weighted segment. Therefore, all of the MSB input code combinations must be generated by the FPGA platform in Figure 4.1 [49]. The DNL and INL at any input code can be calculated using Eqs. (4.3-4).

$$DNL_n = V_n - V_{n-1} - V_{LSB} \qquad for\ 1 \le n \le 2^N - 1 \tag{4.3}$$

$$INL_n = \sum_{i=1}^{n} DNL_i \tag{4.4}$$

4.2.2 Dynamic specification measurement

Settling time and glitch impulse area are the most important time-domain dynamic specifications of the DACs. Maximum sample rate of the DAC should be considered in dynamic testing. Settling time is defined as the transition time from the output of all "0"s code to the output of all "1"s code. The error band can be defined in terms of LSB or a percentage of the full scale. Glitch impulse area is defined as the sum of the area of four glitches happened in the worst case transition of the DAC output. The above-mentioned parameters are shown in Figure 4.3. Wideband high-speed oscilloscope must be used in measuring glitch area and settling time [49].

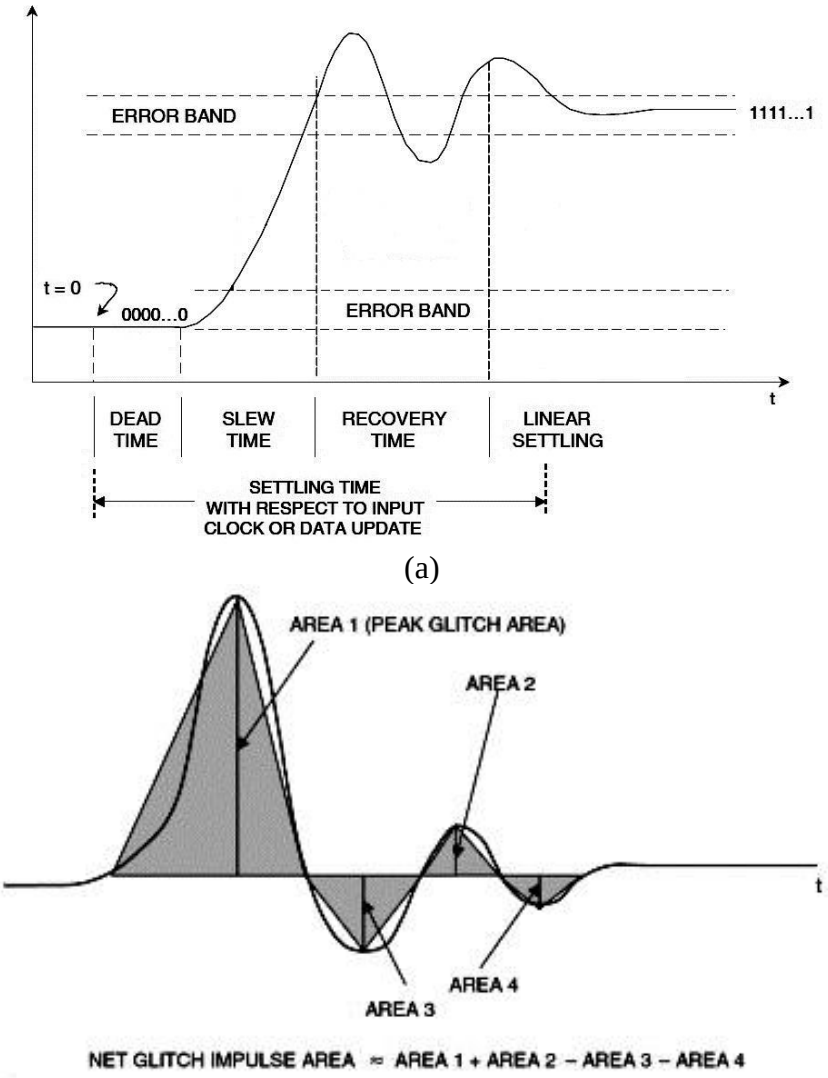


Figure 4.3: Time-domain dynamic specifications; (a) Settling time; (b) Glitch impulse area [49]

In the frequency domain, SNR, THD, SFDR, and SNDR are the most important specifications which characterize the distortion of the output signal of a DAC. Here, periodic samples of single tone sine wave signal are needed to be consecutively applied to the DAC. Thus, a word generator or arbitrary digital waveform generator can be employed. The generated analog output is then analyzed using a spectrum analyzer whose input dynamic range is higher than the full scale range of the DAC. The resolution bandwidth (RBW) of the spectrum analyzer should be set to minimum in order to resolve the fundamental frequency and harmonics. In this case, the process gain of the analyzer should be calculated in the characterization of the DAC. Depending on the sample rate, several harmonics may fall back inside the Nyquist bandwidth due to aliasing. Being defined in the literature, the SNR, THD, SFDR, and SNDR are described in Figure 4.4 and Eqs.(4.5-7) [49].

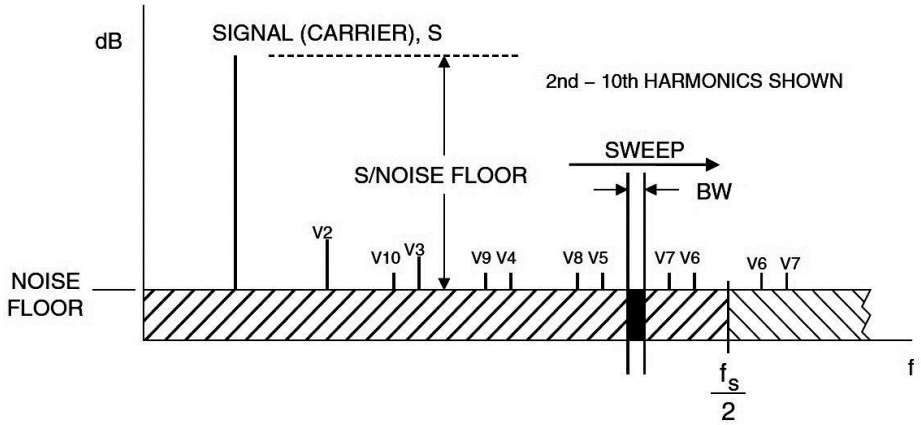


Figure 4.4: Frequency spectrum of DAC output [49]

$$SNR = S/Noise\ floor - 10log_{10}\left(\frac{f_s}{2\times BW}\right) \tag{4.5}$$

where *S/Noise floor* is the noise floor level comparing with signal level and is expressed in dBc, f_s is the sample rate, and BW is the resolution bandwidth of the spectrum analyzer.

$$THD = 20log_{10}\left[\sqrt{(10^{-V2/20})^2 + (10^{-V3/20})^2 + \cdots + (10^{-V6/20})^2}\right] \tag{4.6}$$

where *V2* to *V6* are the power level of the first 6th harmonics with respect to the signal level and expressed in dBc. THD can also be defined for different number of harmonics and is measured for the full scale output signal.

$$SNDR = 20log_{10}\left[\sqrt{(10^{-SNR/20})^2 + (10^{-THD/20})^2}\right] \tag{4.7}$$

In order to eliminate the correlation between the output frequency and the quantization noise, it is crucial that the sample rate be a non-integer multiple of the output frequency. With this assumption, the SFDR is the power of the worst spurious component with reference to the power of fundamental frequency component and expressed in dBc. If the spur level is compared with the full scale fundamental power, SFDR will be shown in dBFS (dB Full Scale) [49].

4.2.3 Simulation result characterization

While the specifications of measurement equipments have significant role in characterization of the fabricated SCSDAC, precise test bench setup as well as accurate Discrete Fourier Transform (DFT) algorithm is essential measurement solution in analyzing schematic and post-layout simulation results. Considering the hierarchical architecture of the design, each building block and the complete SCSDAC chip must be simulated and verified in circuit and layout levels. In the Analog Design Environment (ADE) in Cadence simulator, ideal sources are available to power up the chip and generate the input/output signals for the DAC. Using these sources, the schematic and layout of major building blocks of the SCSDAC can be verified. However, serial input data and the two clock signals (refer to Figure 3.15) should be generated using VerilogA coding in the chip level simulations.

In addition, DFT analysis is needed for extracting the power spectrum of the DAC output signal and measuring dynamic performance in circuit and layout level. Although DFT and other mathematical functions are available in the Cadence Calculator, the generated signal can be better analyzed using MATLAB functions. Therefore, the output signal must be sampled in Cadence environment and sent to MATLAB for further verification. Figure 4.5 depicts the simulation test setup. To avoid very long simulation time of the whole SCSDAC, the data should be captured from the minimum length of transient analysis in Cadence and then processed in MATLAB.

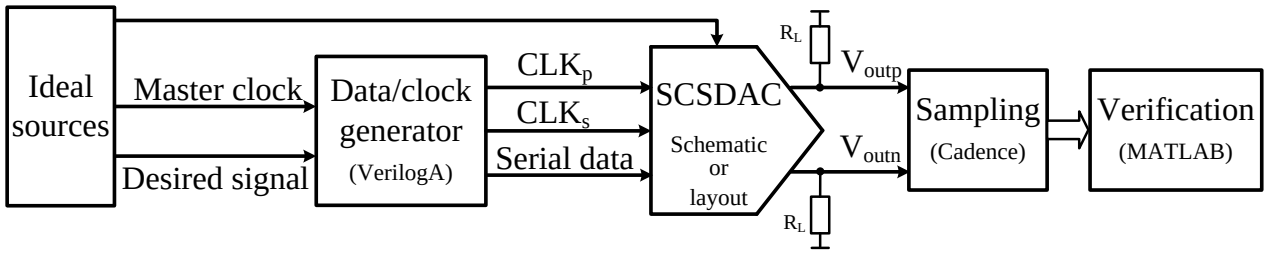


Figure 4.5: Test bench setup for DAC simulation

To accelerate calculation of the DFT in MATLAB, Fast Fourier Transform (FFT) algorithm might be employed. However, FFT prerequisites impose several limitations on the choice of the output frequency and the number of sampled data captured in Cadence. For an N-point DFT:

$$X(k) = \frac{1}{N} \sum_{m=0}^{N-1} x(m) e^{\frac{-j2\pi mk}{N}} \qquad for\ 0 \leq k \leq N-1 \tag{4.8}$$

where $x(m)$ is the time domain sampled signal, N is the number of DFT points, and $X(k)$ is the DFT of the $x(m)$. DFT values for $0 \leq k \leq \frac{N}{2}$ are corresponding to the frequency range from zero to $\frac{f_s}{2}$, where f_s is the sample rate. Thus, the width of each frequency bin is $\frac{f_s}{N}$ and therefore, larger N results in higher resolution in frequency domain. On the other hand, N must be a power of two in FFT routines and the number of samples in time domain should be equal to the number of FFT points. Furthermore, sampled signal must be periodic. This means that if two set of samples are repeated one after another, there should be no phase discontinuity in the signal. Otherwise, spectral leakage aberrations will appear in the FFT output. Hence, the signal must be windowed before being applied to the FFT calculator, if the samples are unknown or non-periodic. Additionally, fundamental frequency component of the signal must be a prime number multiple of the width of each frequency bin.

$$f_{in} = M \times \frac{f_s}{N} \tag{4.9}$$

where M is a prime number. A non-prime value of M concentrates the noise at the harmonics of f_{in}. Thereupon, lower SFDR is resulted [49].

4.3 Simulation results

In this section, the schematic and post-layout simulation results of the main building blocks of the proposed SCSDAC will be presented. Considering the design phases which were explained in Chapter 3, the LSB current source and the whole DAC circuit were simulated in order to verify and validate the design.

Based on the designed transistor sizes reported in Table 3.7 the complete circuit diagram of the LSB current source is shown in Figure 4.6. In this circuit, each of the ten nodes plays a significant role in the overall performance of the SCSDAC. Referring to Figure 3.15, using

parallel unit transistors in higher order current sources will result in 1023 LSB sources. Therefore, both system and circuit level design criteria should be taken into account in evaluating the performance of the LSB source.

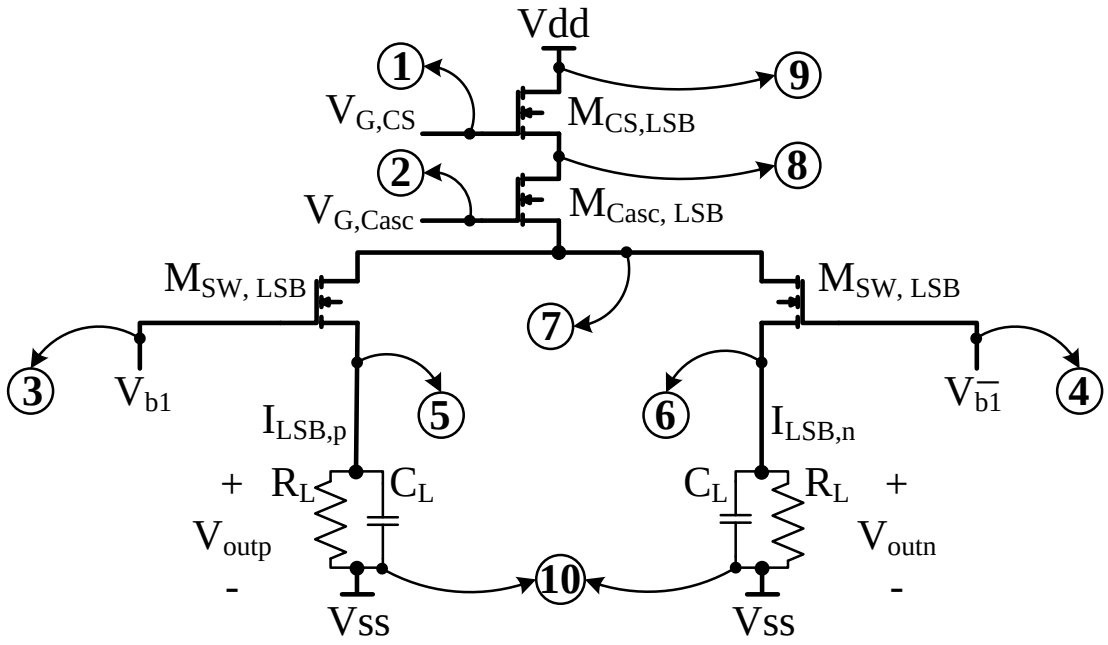


Figure 4.6: LSB current source

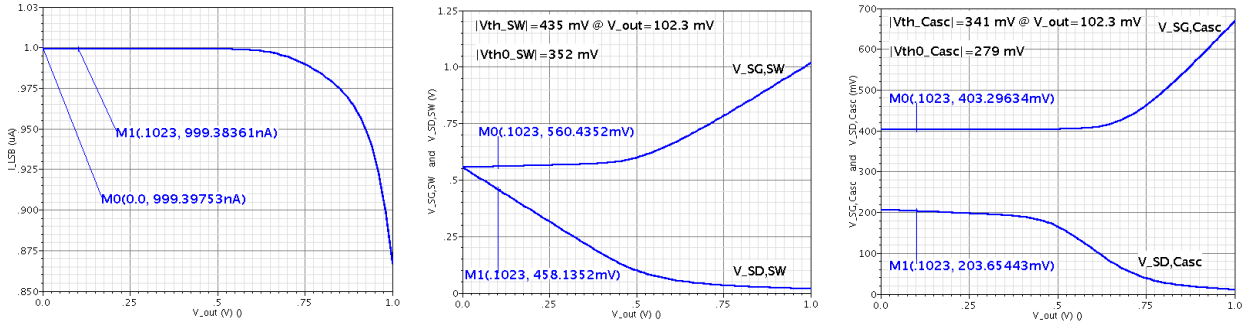
Driven by $V_{G,CS}$ and $V_{G,Casc}$, nodes 1 and 2 are the common gate nodes for all of the M_{CS} and M_{Casc} transistors, respectively. Nodes 3 and 4 provide on/off commands for the switch transistors and are driven by V_{b1} and its complementary voltages. Nodes 5 and 6 are the differential outputs which are common for all sources and are connected to the load resistor and capacitor (R_L and C_L). 7 and 8 are the most critical nodes in this circuit in terms of dynamic performance. The parasitic capacitors should be minimized at these nodes. Power supply and ground connections are provided through 9 and 10 nodes. While 10 is an off-chip node, very low resistance path should be designed in the layout in order to guarantee uniform distribution of V_{dd}.

According to design aspects presented in Chapter 3, the main objectives of the LSB current source is to generate an accurate LSB current of 1 µA with: (1) guaranteed operating point in the saturation region for all transistors; (2) minimized random and systematic error; (3) high output resistance; (4) minimized glitch impulse area and input feedthrough; (5) high switching speed.

4.3.1 Transistor operating regions

Although higher V_{swing} is desired, increasing V_{out} pushes the M_{SW} and M_{Casc} toward the triode region. Referring to Figure 4.6, increasing V_{out} (V_5 or V_6) reduces V_{SD} of M_{SW} and slightly decreases I_{LSB}. Then the current mirror functionality of the circuit tries to keep I_{LSB} constant by increasing V_7. Thus, the $V_{SG,SW}$ slightly increases. Further increasing V_{out} more reduces $V_{SD,SW}$ and changes the operating region of M_{SW} (depending on $V_{th,SW}$). If V_{out} is increased more, the same situation will happen for the M_{Casc} that should be prevented in the design. Considering the supply voltage of 1.2 V and simulation results in IBM 0.13 µm CMOS technology, the maximum V_{out} for which all the transistors are in the saturation region is almost 410 mV. It should be noted that the body of PMOS transistors in Figure 4.6 is connected to V_{dd} in order to use the same NWELL for the M_{SW} and M_{Casc} and reduce the parasitic capacitors at node 7. This imposes variability of V_{th} due to the body effect in M_{SW} and M_{Casc}.

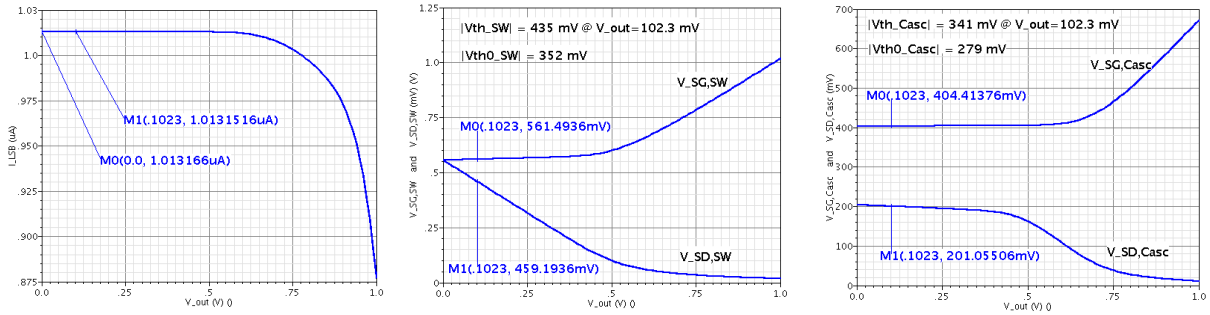
Additionally, Eq. (3.28) defines another constraint on the I_{LSB} which is slightly varying with the variations of V_{out}. Moreover, it must be noticed that pushing transistors more into the saturation region results in higher bandwidth which is desired in dynamic performance of the SCSDAC. On the other hand, maximum V_{out} is equal to R_L multiply by I_{FS}. This implies that R_L and/or I_{FS} must be increased to increase V_{out}. While increasing R_L degrades the linearity based on Eq. (3.33), augmenting I_{FS} needs larger M_{CS}. In Figure 4.7, the variations of I_{LSB}, $V_{SG,SW}$, $V_{SD,SW}$, $V_{SG,Casc}$, and $V_{SD,Casc}$ are depicted versus V_{out}.



(a) (b) (c)

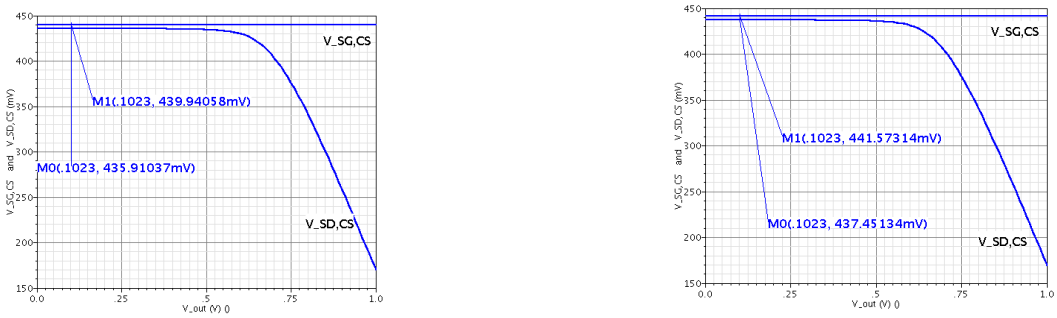
Figure 4.7: V_{out} effects (ideal bias) (a) I_{LSB}; (b) V_{SG} and V_{SD} of M_{SW}; (c) V_{SG} and V_{SD} of M_{Casc};

While the results in Figure 4.7 are obtained using an ideal reference current, Figure 4.8 shows the same results with the designed bias circuit. Figure 4.9 indicates these curves for M_{CS}.



(a) (b) (c)

Figure 4.8: V_{out} effects (designed bias) (a) I_{LSB}; (b) V_{SG} and V_{SD} of M_{SW}; (c) V_{SG} and V_{SD} of M_{Casc};



(a) (b)

Figure 4.9: $V_{SG,CS}$ and $V_{SD,CS}$ versus V_{out} (a) ideal bias; (b) designed bias;

As discussed above, there is a tradeoff between V_{swing}, linearity, bandwidth, and the size of current source transistors. With reference to the full scale current of 1023 µA, we have used load resistor of 100 Ω to achieve 102.3 mV full scale output voltages. The results in Figure 4.7 and Figure 4.8 guarantee the saturation of transistors. Variations of V_{th} of all transistors in different corners are tabulated in Table 4.1.

Table 4.1: Threshold voltage of transistors in LSB current source

Voltages	**Transistors**	**Simulated corners**				
		tt	**ss**	**sf**	**fs**	**ff**
V_{th0} (mV)	M_{CS}	229.6	250.7	207	247.5	201.3
	M_{Casc}	279	296.3	262	292	256
	M_{SW}	352	356.7	350.6	350.4	344
V_{th}[1] (mV)	M_{Casc}	341	361.6	321	355.7	313
	M_{SW}	435	434.5	438.3	428	432

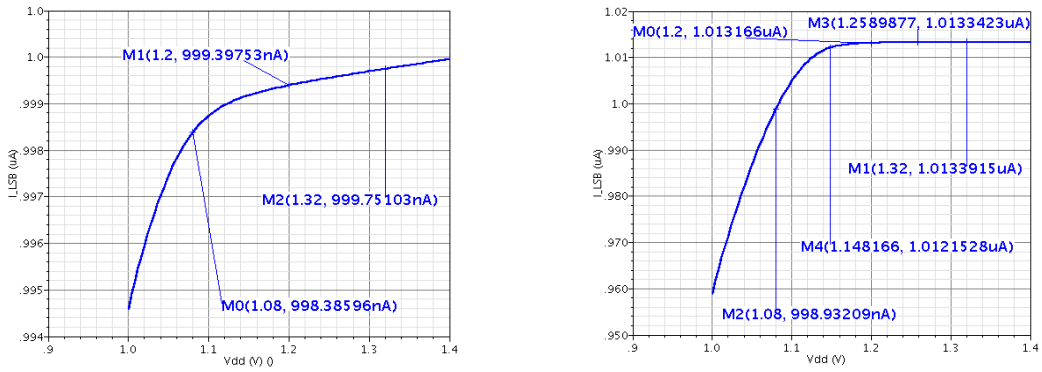
[1]. Threshold voltages are calculated for V_{out} = 102.3 mV

4.3.2 Output current precision

Monte Carlo simulation and intentional alteration of circuit parameters were used to evaluate the robustness of the design and the precision of the output current in LSB and full scale levels. Simulating random and systematic error among CSA was the specific objective of this analysis. In this regard, the impacts of any change in V_{dd}, size of all transistors, and the resistance of the V_{dd} distribution path were studied. This investigation is done for both cases of using an ideal reference current or the designed bias circuit.

In the previous section it was shown that by changing V_{out} from 0 to 102.3 mV, the precision of I_{LSB} is $\pm 0.69 \times 10^{-3}$ % and $\pm 0.71 \times 10^{-3}$ % for ideal and design bias circuits, respectively.

The aberration of I_{LSB} as a result of ± 10 % variation in V_{dd} is shown in Figure 4.10. In the worst case, I_{LSB} is reduced by 0.1 % and 1.4% using ideal or designed bias circuit, respectively. In order to keep the I_{LSB} variations below 0.1 % using biased circuit, the V_{dd} should be maintained between 1.15 V and 1.25 V.

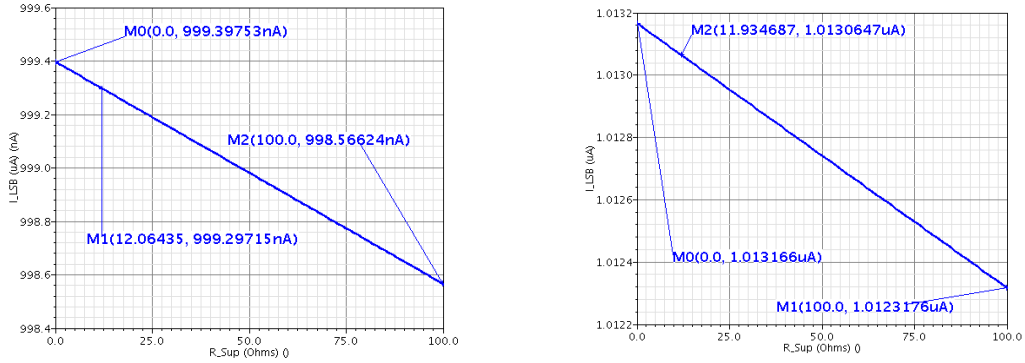


(a) (b)

Figure 4.10: I_{LSB} aberrations due to V_{dd} (a) ideal bias; (b) designed bias;

An important challenge in the layout design of the SCSDAC is the resistance of V_{dd} distribution path. A variable resistor is placed in series with M_{CS}, in order to simulate this phenomenon. As depicted in Figure 4.11, larger V_{dd} path resistance reduces the I_{LSB} and increases the power dissipation of the chip. It is shown that a 100 Ω resistance reduces the I_{LSB} by 0.083 % or 0.098 % depending on the type of bias circuit. Accordingly, the metal path resistance should be less than 12 Ω in order to keep the I_{LSB} variations below 0.01 %. The resistance of the V_{dd} path

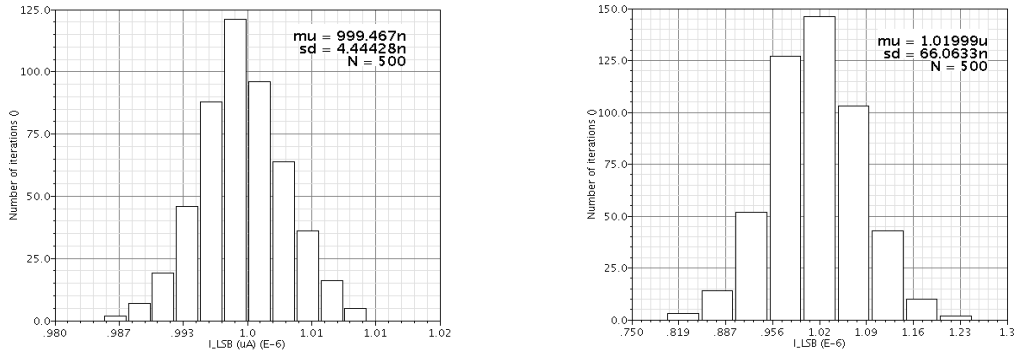
depends on the type, length, and width of the metal layer and can be calculated using technology parameters [69].



(a) (b)

Figure 4.11: I_{LSB} reduction due to resistance of V_{dd} path (a) ideal bias; (b) designed bias;

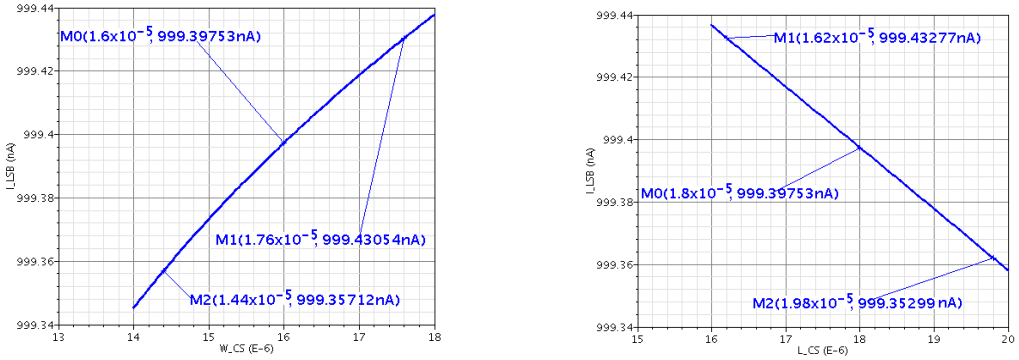
Monte Carlo simulations were done on the LSB current source and the results are shown in Figure 4.12 for 500 iterations. Using an ideal reference current, the relative SD of the I_{LSB} is almost 0.4 % which is better than requirements in Eq. (3.28). This metric is 6.5 % when designed bias circuit is employed. In fact, the reason for such a difference is that the process and mismatch variations are also applied to the bias circuit in Monte Carlo simulations. Thus, the reference current is changing which exacerbates the SD of the I_{LSB}. Nevertheless, since the INL is measured with reference to a straight line drawn through the actual zero and full scale of the DAC [49], Figure 4.12(a) represents the behavior of the LSB current source against process variations. On the other hand, Although selecting large gate area of M_{CS} results in higher precision in I_{LSB}, it will impose large CSA area and more layout limitations in meeting the design rules of the technology [69].



(a) (b)

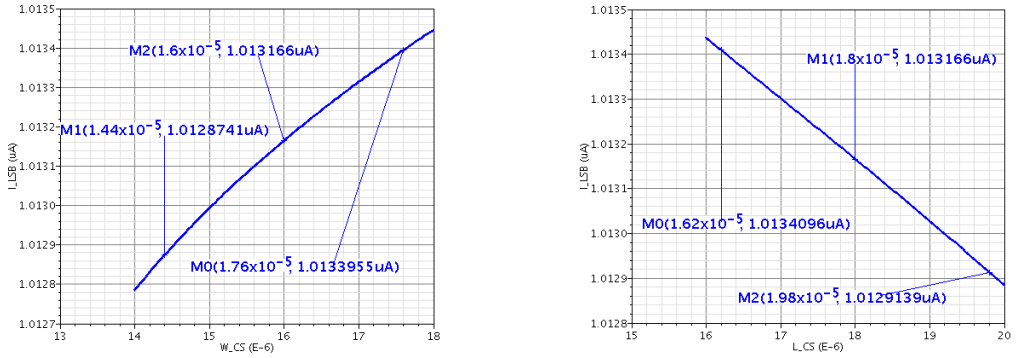
Figure 4.12: I_{LSB} reduction due to resistance of V_{dd} path (a) ideal bias; (b) designed bias;

In the next step, degradations of I_{LSB} with ± 10 % change in width and length of M_{CS}, M_{Casc}, and M_{SW} are simulated and the results are shown in Figure 4.13 to Figure 4.16. These impacts on the precision of I_{LSB} are summarized in Table 4.2.



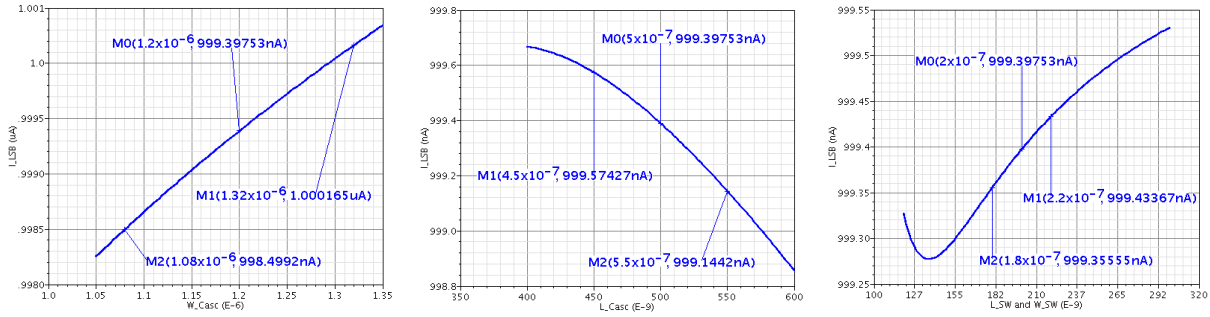
(a) (b)

Figure 4.13: I_{LSB} aberrations due to size of M_{CS} with ideal bias circuit (a) W_{CS}; (b) L_{CS};



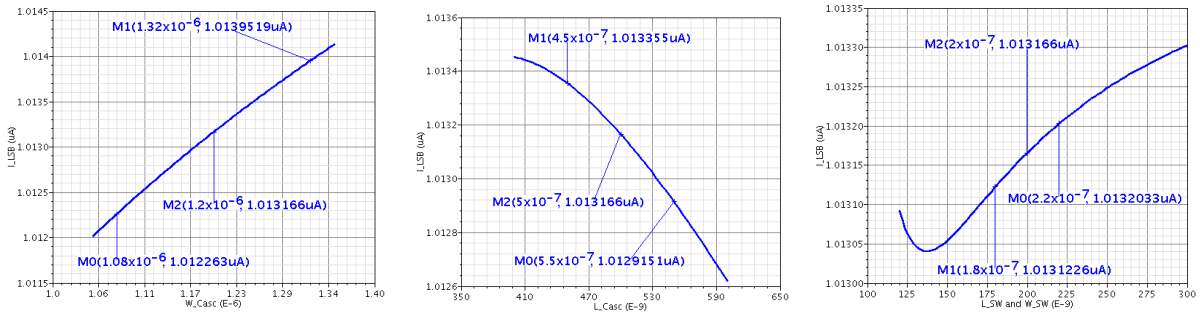
(a) (b)

Figure 4.14: I_{LSB} aberrations due to size of M_{CS} with designed bias circuit (a) W_{CS}; (b) L_{CS};



(a) (b) (c)

Figure 4.15: I_{LSB} variations with the size of M_{Casc} and M_{SW} using ideal bias circuit (a) W_{Casc}; (b) L_{Casc}; (c) W_{SW} and L_{SW};



(a) (b) (c)

Figure 4.16: I_{LSB} variations with the size of M_{Casc} and M_{SW} using designed bias circuit (a) W_{Casc}; (b) L_{Casc}; (c) W_{SW} and L_{SW};

Table 4.2: Simulation results of impacts of circuit parameters on precision of I_{LSB}

Parameter				**Precision of I_{LSB} (%)**	
Description	**Typical value**	**Maximum variation** [69]	**Simulated variation range**	**Ideal bias**	**Designed bias**
Power supply (V_{dd})	1.2 V	N/A	1.08 ~ 1.32 V	0.1	1.4
Output voltage (V_{out})	–	N/A	0 ~ 102.3 mV	0.69×10^{-3}	0.71×10^{-3}
Resistance of V_{dd} path	–	N/A	0 ~ 100 Ω	83×10^{-3}	84×10^{-3}
Width of M_{CS}	16 µm	± 0.047 µm	14.4 ~ 17.6 µm	4.04×10^{-3}	28.8×10^{-3}
Length of M_{CS}	18 µm	± 0.022 µm	16.2 ~ 19.8 µm	4.45×10^{-3}	24.9×10^{-3}
Width of M_{Casc}	1.2 µm	± 0.047 µm	1.08 ~ 1.32 µm	89.9×10^{-3}	89.1×10^{-3}
Length of M_{Casc}	0.5 µm	± 0.022 µm	0.45 ~ 0.55 µm	25.3×10^{-3}	24.7×10^{-3}
Width and length of M_{SW}	0.2 µm	± 0.022 µm	0.18 ~ 0.22 µm	4.2×10^{-3}	4.3×10^{-3}

In order to evaluate the precision of I_{LSB}, the width and length of transistors are changed by ± 10 % in this work. Based on the facts and figures of Table 4.2, L_{Casc} variation results in the worst degradation in I_{LSB}. However, not only the simulated range is more than twice the predicted variation during fabrication, but also the contribution of this error in the whole mismatch among LSB sources is very low.

4.3.3 Output resistance of current sources

The output impedance of the LSB current source is also simulated and studied in this work. Theoretically, larger channel length, shorter channel width, smaller I_{DC}, and lower gate overdrive voltage increase the output resistance of a MOS transistor [47]. Larger R_{out} improves the INL and the SNDR of the DAC but decreases the bandwidth if large channel length is used. Considering the LSB current source shown in Figure 4.6, the equivalent capacitors at nodes 7 and 8 determine the poles of the frequency response of R_{out}. The equivalent circuit is shown in Figure 4.17. C_{CS} and C_{CSW} indicate the equivalent capacitors at nodes 7 and 8.

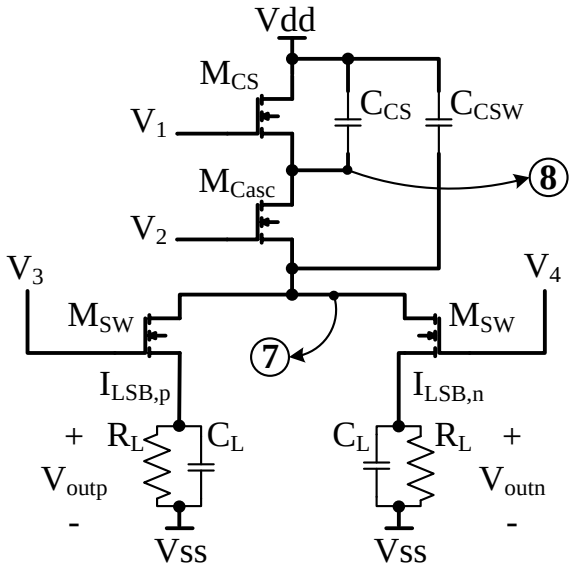
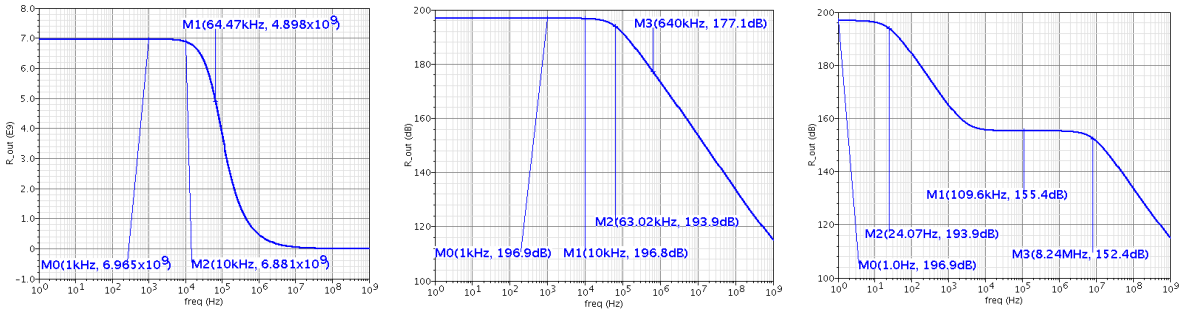


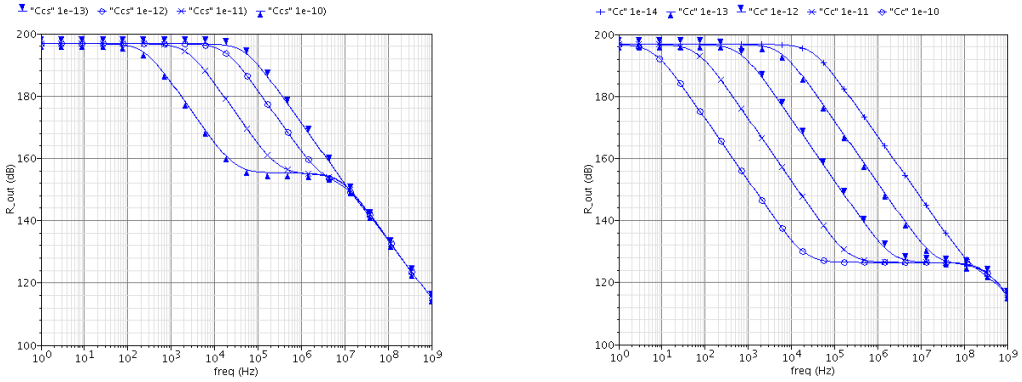
Figure 4.17: Equivalent circuit of LSB current source

Considering the size of M_{CS} and the layout connections from CSA to switch-cascode array in the floorplan shown in Figure 3.18, C_{CS} is expected to be much larger than C_{CSW} and create the dominant pole in the R_{out} frequency response [57]. Figure 4.18(a) and (b) show the plot of R_{out} in frequency domain in linear and logarithmic scales up to 1 GHz. Since these curves are acquired from schematic view, the impacts of layout connections are not simulated. Therefore, the effects of C_{CS} and C_{CSW} are not discriminated. In Figure 4.18(c) an intentional 1 nF capacitor is added in parallel with C_{CS} in order to highlight the position of the poles. In order to simulate the effect of different number of parallel current sources, parametric simulation were performed using different values of C_{CS} and C_{CSW}. The results are shown in Figure 4.19.



(a) (b) (c)

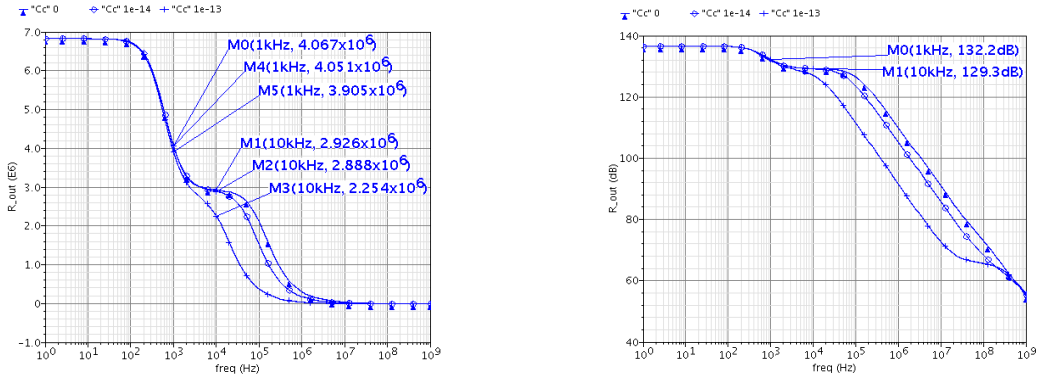
Figure 4.18: R_{out} of LSB source (a) linear scale; (b) logarithmic scale; (c) C_{CS} = 1nF



(a) (b)

Figure 4.19: R_{out} of LSB source for various (a) C_{CS}; (b) C_{CSW};

Figure 4.19(b) confirms the importance of reducing C_{CSW} in obtaining high R_{out}. The output resistance of the proposed SCSDAC is the lowest when all of the 1023 LSB sources switch their current into the output node. The overall R_{out} of this condition is depicted in Figure 4.20 where the resistance at 1 kHz and 10 kHz are shown for C_{CSW} values of 0, 10 fF, and 100 fF.



(a) (b)

Figure 4.20: R_{out} of full scale output for various C_{CSW} (a) linear scale; (b) logarithmic scale;

Careful layout considerations were taken into account to minimize the parasitic capacitors which are in parallel with C_{CSW} and C_{CS}. The layout view of the M_{SW} and M_{Casc} are shown in Figure 4.21 [57]. In this solution, there is no metal connection between the drain of M_{Casc} and the source of M_{SW}. Nonetheless, using the parasitic extracted view of this layout cell in the simulations slightly increase C_{CSW} and C_{CS}. The resulted deflection on Rout is shown in Figure 4.22.

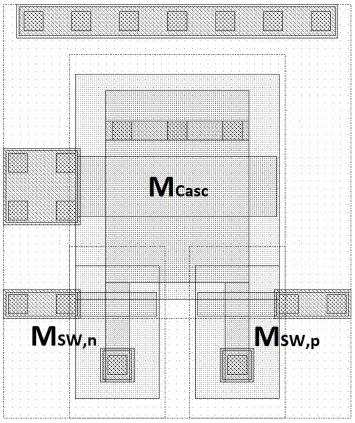
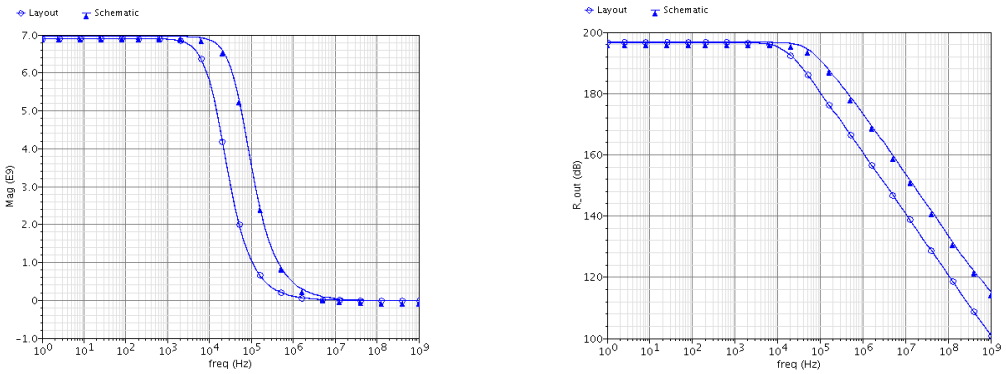


Figure 4.21: Layout of the LSB switch and cascode transistors



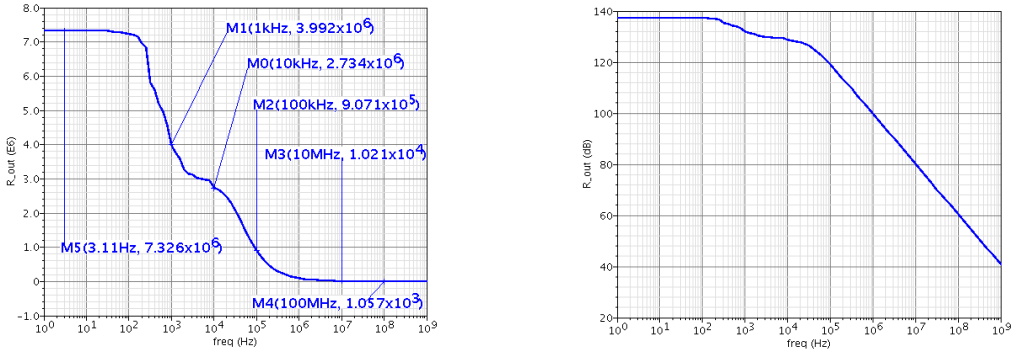
(a) (b)

Figure 4.22: R_{out} of LSB source in layout and schematic (a) linear scale; (b) logarithmic scale;

Although R_{out} of LSB cell is still very high in Figure 4.22, paralleling the sources and chip level parasitic capacitors will further reduce the overall R_{out} of the proposed SCSDAC. In the next step, 1023 parallel LSB sources were simulated using the layout cell of Figure 4.21. As can be seen in Figure 4.23, R_{out} is almost twice smaller than parallel equivalent of 1023 sources at 10 kHz.

According to Eq. (3.33), output resistance of LSB cell must be less than 51 kΩ to guarantee an INL of 0.5 LSB. Based on the results of Figure 4.23, the contribution of R_{out} in the INL of the

proposed DAC can be neglected. Moreover, no significant reduction of R_{out} is observed with changing V_{out}, W_{CS}, and W_{Casc}.

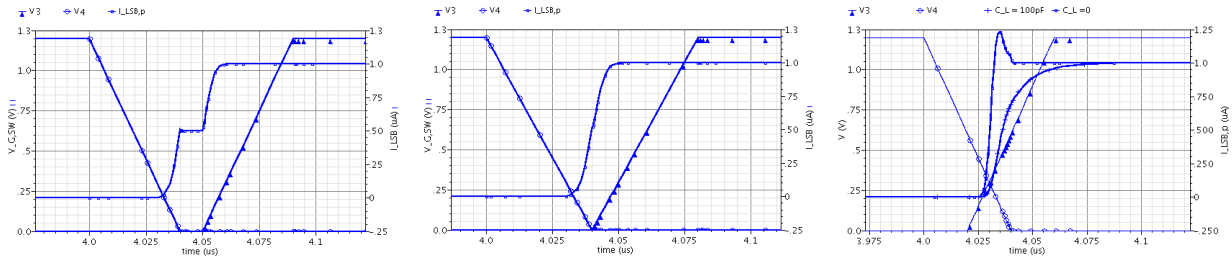


(a) (b)

Figure 4.23: R_{out} of SCSDAC for full scale output using layout cell
(a) linear scale; (b) logarithmic scale;

4.3.4 Transient analysis

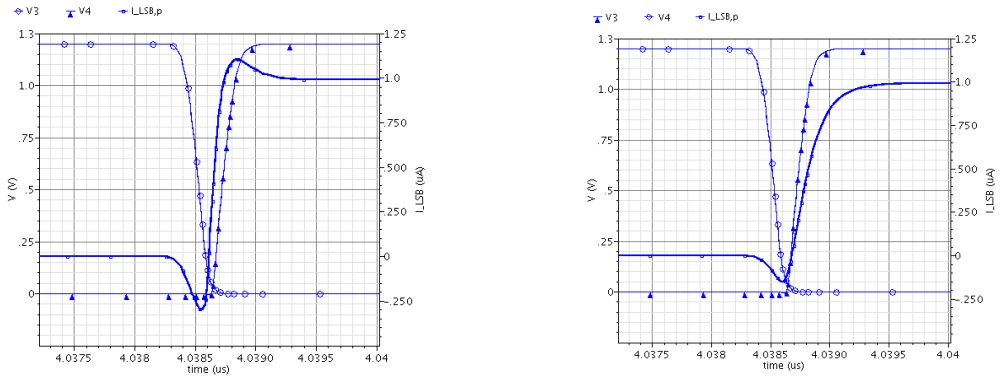
The main role of using two switch transistors is to avoid switching of currents in each source. Referring to Figure 4.6, proper nonoverlapping switch control commands (nodes 3 and 4) are required to prevent charging and discharging of equivalent capacitors at nodes 7 and 8. Ideal switch commands are used to simulate the resulted transient response imperfection which is shown in Figure 4.24. In low frequency applications, appropriate load capacitor (C_L) eliminates the generated glitch. Depicted in Figure 4.24(c), the drawback of using C_L is longer settling time.



(a) (b) (c)

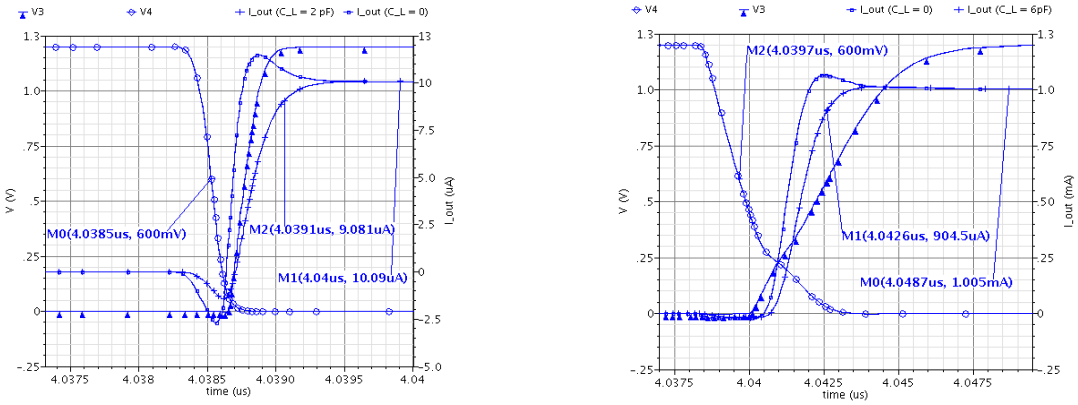
Figure 4.24: Effect of switch commands on I_{LSB}; $t_{overlap}$ = (a) 10 nSec; (b) 0 Sec; (c) -20 nSec;

Simulation results of the designed nonoverlapping switch driver circuit is shown in Figure 4.25 for C_L = 0 and C_L = 2 pF. Considering the design specifications in Table 3.2, maximum update period is almost 311 nSec. In the worst case, the settling time should be shorter than 5% of the update period (15.55 nSec) [49]. Furthermore, the maximum sine wave current step at the output of the DAC is almost 10 µA ($10 \times I_{LSB}$) for the maximum update rate, based on Eqs. (3.5) and (3.6). The simulation results of Figure 4.26 shows that the settling time of this DAC is less than 1 nSec in making a smooth transition (C_L = 2 pF) from zero to 9.08 µA. This settling time is referenced to the 50% of the switch command. Using C_L = 6 pF, the settling time is 2.9 nSec for full scale transition. The results in Figure 4.26 reveal that adopting higher load capacitors will further reduce the glitch impulse without affecting the switching speed required in this work.



(a) (b)

Figure 4.25: Effect of designed switch driver circuit on output step of I_{LSB}; (a) C_L=0 ; (b) C_L=2 pF;



(a) (b)

Figure 4.26: Effect of designed switch driver circuit on output step of (a) 10µA; (b) I_{FS};

4.3.5 Overall post-layout simulation results

As the last step in post-layout simulations, a test bench was provided to generate appropriate digital data corresponding to 128 different samples in a complete sine waveform. The digital data was then serially sent to the input shift register of the SCSDAC synchronous with a serial clock. After sending each digital input word (Figure 3.14) to the SCSDAC, update clock loads it to the input latch and consequently the DAC output alters. The update clock frequency is set to 1.28 MHz in order to generate 10 kHz sine wave. Lower update rates results in lower sine frequencies. To minimize the time of transient post-layout simulation, highest update rate is selected to achieve Figure 4.27. The update rate and sufficient number of samples per each sine cycle should be selected with regard to the specifications of the measured output signal of the DAC. Although higher number of samples per sine cycle generates a very smooth analog sine, larger memory is needed to save the digital words and higher serial and update clock frequencies will be inevitable.

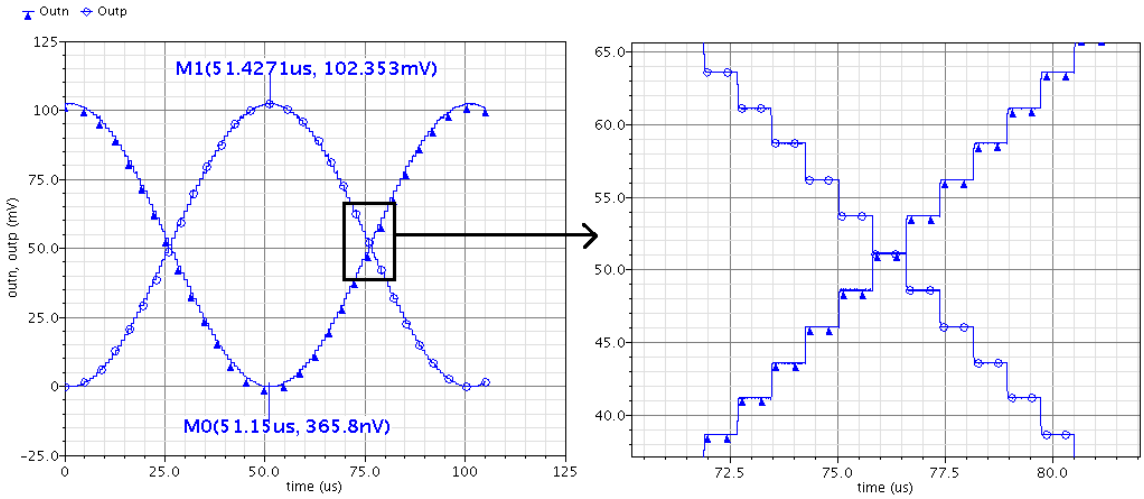


Figure 4.27: Sine wave of 10 kHz generated in post-layout simulation (update rate = 1.28 MHz)

In order to extract the transfer function of the designed SCSDAC, all of the 1024 possible inputs are generated and applied to the extracted view of the layout. As a result the differential outputs of the DAC traversed the full scale output range which is shown in Figure 4.28. Careful examination of these curves indicates the monotonicity and accuracy of the analog output signal of the DAC. An update rate of 4 MHz is applied to the DAC in this simulation which is significantly higher than the desired oversampling rate mentioned in Table 3.2.

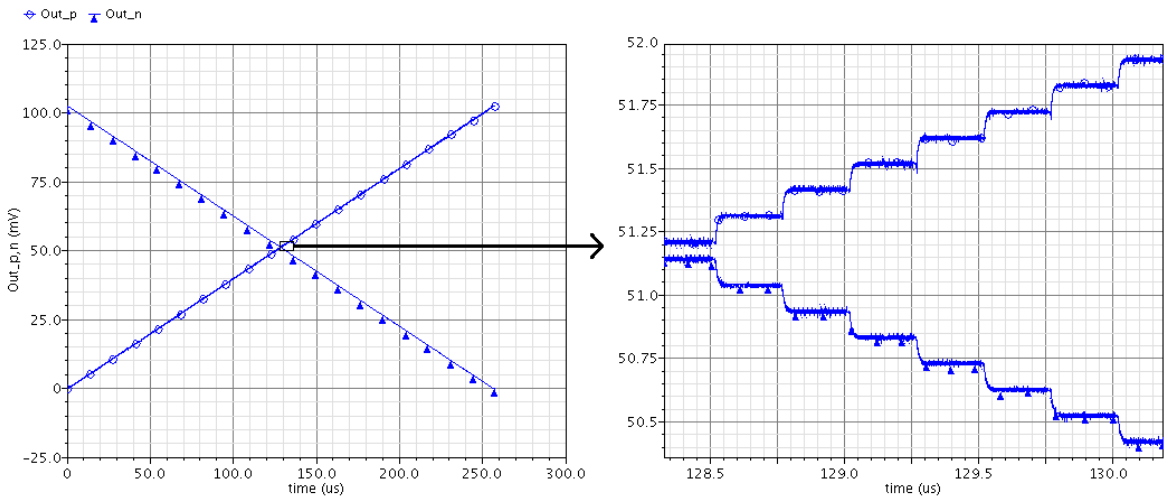


Figure 4.28: DAC transfer function captured in post-layout simulation (update rate = 4 MHz)

4.3.6 General discussion on simulation results

With regard to the presented simulation results, there are several tradeoffs that should be carefully considered in the circuit-level design stage of the SCSDAC:

1- Although PMOS transistors are slower than NMOS, they are more robust against noise. Thus, better SFDR and higher R_{out} is expected when PMOS is used in the CSDAC. Besides, the output node can be referred to the ground by using PMOS transistors.

2- Higher I_{LSB} is desired to increase the output voltage swing, but it results in lower R_{out}.

3- Using switches with larger channel length significantly increases $R_{out.}$ However, it decreases the switching speed and the bandwidth of the DAC. Smaller L_{SW} reduces the input signal feedthrough and the power consumption and also needs smaller size transistors in the switch driver circuit.

4- Glitch impulse area can be reduced by using smaller size transistors; however, large transistors are essential in reducing the effect of process variation.

5- Although higher overdrive voltage of the M_{CS} and M_{Casc} minimizes the random error caused by the variations of V_{th}, it is limited by the voltage headroom of the technology.

6- Synchronization of switch commands is very important with respect to dynamic performance, but it imposes high level of layout completion.

4.4 Measurement results

The designed SCSDAC is fabricated in a total die area of $1.2 \times 1.2\, mm^2$ using the IBM 130nm CMOS technology provided by CMC Microsystems [68]. Photomicrograph of the fabricated chip is shown in Figure 4.29. NCAP capacitors and wide metal wiring are used at different segments of the V_{dd} and bias voltage distribution paths. At the output and V_{dd} nodes of the DAC, wide thick metal connections are used in order to minimize the power dissipation. Beta-multiplier bias circuit with on-chip resistor is included in the design to generate reference voltages for the M_{CS} and M_{Casc} transistors. The choice of on-chip resistor prevents possible oscillation. A fast start-up circuit is also implemented in the bias circuit to avoid unwanted operating points. Fast edge-triggered flip flops are employed in designing the deserializer.

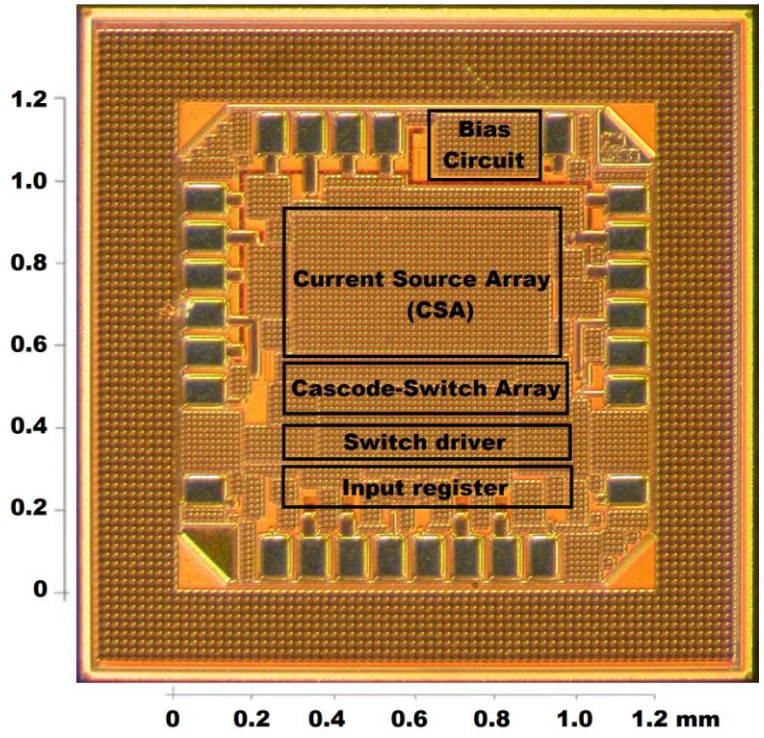


Figure 4.29: Photomicrograph of the designed SCSDAC

Despite the careful design strategy in system and circuit level, the chip could not be successfully tested. Nonetheless, detailed test and measurement were done over the chip in order to locate the problem. In the rest of this chapter, a discussion is provided to justify the malfunction and compare measurement results and post-layout simulation results of the chip.

4.4.1 Verification and validation of the chip

Verification and validation plan of the fabricated SCSDAC included the following steps:

1- Visual and ohmic tests in order to check the internal connections through I/O pads.

2- DC performance evaluation by applying the supply voltage to the chip in order to measure the supply current of the chip, DC voltages of I/O pads, and the output current corresponding to all "1"s and all "0"s input codes.

3- Full static characterization of the SCSDAC by individually applying all input data combinations to the serial input synchronous with clock signals.

4- Full dynamic characterization of the SCSDAC by applying various test patterns to the serial input synchronous with clock signals.

5- Yield measurement and analysis by following the previous steps for all packaged chips and fabricated dice.

The resistance and p-n junctions between various pads were measured and compared with the expected values based on the detailed schematic analysis of the chip. Upon completion of this step, different blocks of the SCSDAC are powered up by different power supplies via separate pads. After inspecting the DC voltages of all I/O pads, all "1"s and all "0"s input combinations are entered in the chip by applying sufficient number of clock pulses to CLK_S and CLK_P pads while the input serial data pad was connected to V_{dd} and ground, respectively. The results are summarized in Table 4.3.

Table 4.3: Results of DC performance verification of the fabricated chip

Test condition	**Post-layout simulation results**			**Measurement results**		
	I_{outp} (µA)	**I_{outn} (µA)**	**I_{SS}[1] (µA)**	**I_{outp} (µA)**	**I_{outn} (µA)**	**I_{SS}[1] (µA)**
All "0"s input	1.93×10^{-3}	1023.5	1210	$\approx 1 \times 10^{-1}$	1023.2	≈ 1400
All "1"s input	1023.5	1.93×10^{-3}		1023.2	$\approx 1 \times 10^{-1}$	

[1] Average DC supply current of the chip.

4.4.2 Problem location and justification

In spite of successful results in the ohmic and DC tests, the output current was not proportional to the input bit stream generated by the FPGA platform during static characterization. Further investigation and testing revealed that the input data is not correctly pushed into the input shift register. Functional block diagram of the SCSDAC is depicted in Figure 4.30 which includes the circuit diagram of the shift register. In order to obtain high speed serial input data transfer, minimum sized, edge-triggered, D-type flip flops are used in designing this shift register. All of the flip flops are triggered by the rising edge of the CLK_S signal. For the testability purposes, the output of the last flip flop is set as an output signal in the designed chip.

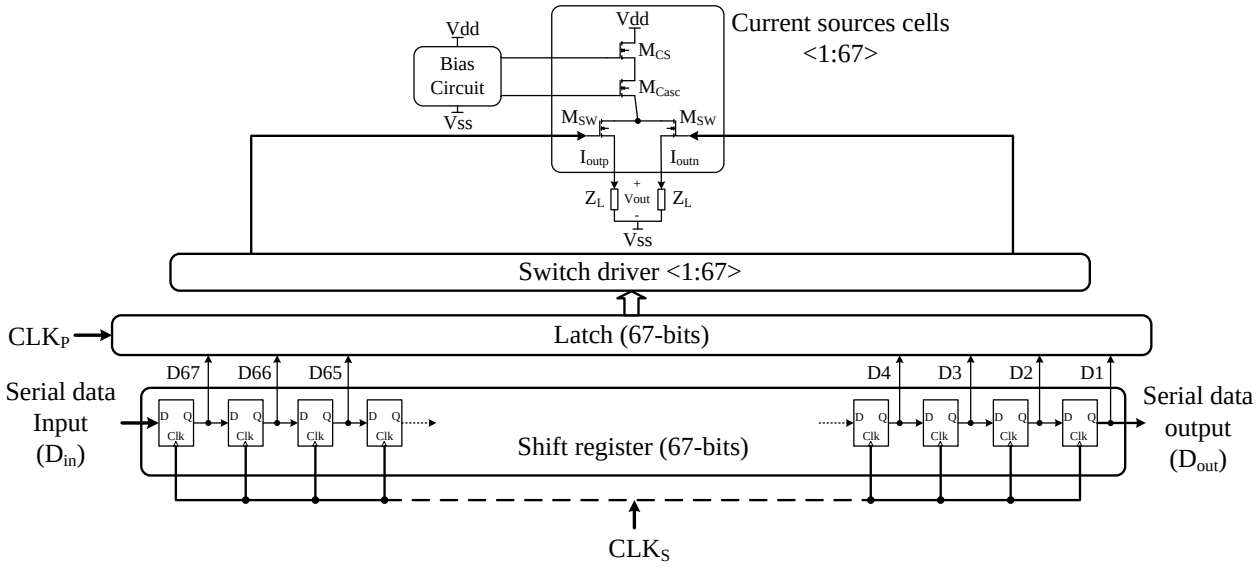


Figure 4.30: Functional block diagram of the designed SCSDAC

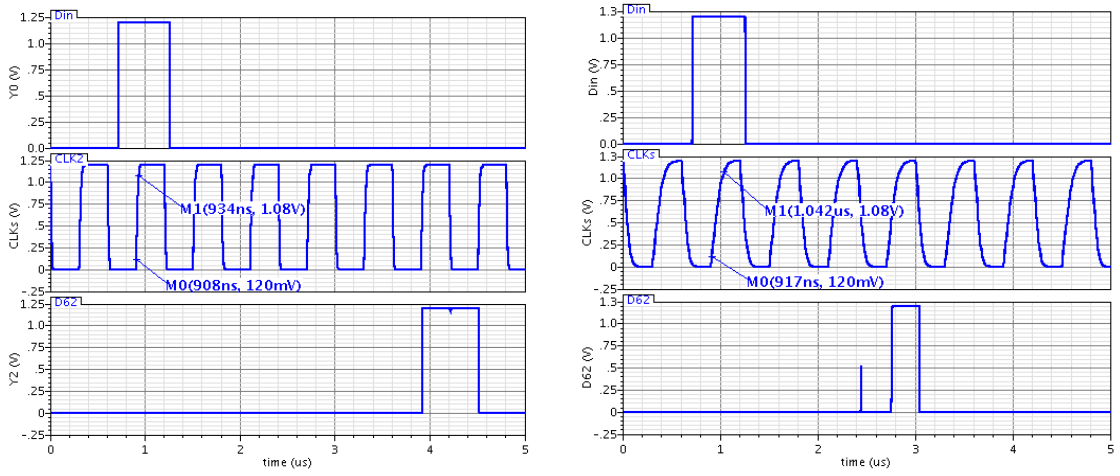
Assuming proper timing and synchronization between serial data input and the CLK_S, one bit of the input stream will be shifted from D67 toward D1 position at each rising edge of the CLK_S. Therefore, 67 rising edge of clock are needed to completely load one input word to the shift register. This word should then be loaded to the 67-bit latch by applying a rising edge to the CLK_P. To verify this function, a repeating input data stream is applied to D_{in}. In this stream, D1 bit is high-level and the other bits are low-level. While it was expected to receive the "1" at D_{out} after 67 rising edge of CLK_S, the output appeared sooner than expected. By using a function generator as the source of the CLK_S signal and reducing the rise time, the number of required

clock edges to forward D_{in} to D_{out} are listed in Table 4.4. Different number of pulses for each rise time shows the instability of the performance of the shift register. Even the fastest rising edge of the clock did not result in a correct functionality.

Table 4.4: Measured test results of the input shift register

t_r (nSec)	No. of rising clock edges for reaching D_{in} to D_{out}
100	18 ~ 20
50	35 ~ 37
20	59 ~ 62
10	65 ~ 66
5	66 ~ 67

The same test pattern was also used in post-layout simulation of the chip with variable rise and fall time of the CLK_S. Post-layout simulation results are presented in Figure 4.31 where the output of D62 flip flop is shown for two different clock rise and fall times of 6 nSec and 125 nSec. D62 is selected to reduce the time required for post-layout transient analysis. Although the data is correctly reached to D62 after 6 rising edge of CLK_S in Figure 4.31(a), it is corrupted in Figure 4.31(b). This problem could be due to the speed of the flip flops and the effects of parasitic capacitors in the clock distribution path. As a matter of fact, during long rise time of the clock several bits of the register are shifted. Moreover, the data is shifted in the falling edge of the clock. Further analysis and simulations on a single flip flop confirmed the detected problem.



(a) (b)

Figure 4.31: Post-layout simulations showing data shift from D_{in} to D62
(a) t_r = 6nSec; (b) t_r = 125nSec;

According to [75], this problem can also be caused by clock skew which is the time difference in the arrival of the clock at different flip-flops. In fact, a racing happens between the data and the clock. This racing depends on the architecture of the clock distribution path and the delay of the logic gates (used in the implementation of each flip flop in the shift register). As a consequence, the serial data can pass the shift register during a shorter time than expected. With reference to the guidelines given in [75] and our observation during the test of this chip, an appropriate clock distribution network should be designed in order to overcome this problem. In this network, proper clock skew should be guaranteed among the 67-bit input shift register of the deserializer. In addition, the delay of the digital gates and the clock path should be carefully analyzed to prevent unwanted racing between data and the clock.

4.5 Conclusion

In this chapter, the verification and validation strategy of the proposed SCSDAC were presented in simulation and measurement level. The testing methods and important static and dynamic specifications of a DAC were also discussed and explained. Lack of appropriate clock distribution network and the complexity of the input shift register disturbed accurate functionality of the input shift register and prevented correct data conversion process. However, consistent schematic and post-layout simulation results approve the design and confirm the required level of accuracy.

CHAPTER 5

GENERAL CONCLUSIONS AND FUTURE WORK

This Master thesis was concerned with conceptual design and partial implementation of a generic smart sensor interface for avionics applications. In this chapter, the contributions of this work will be reviewed and several directions will be suggested for future research work.

5.1 Summary and discussion

In the first part of this Master thesis, the system level block diagram of the ESG module was proposed in accordance with the overall SSI structure and the L/RVDT sensor requirements. We argued that the memory-based signal generator architecture supports the desired system level specifications. This means that the digital samples of a sine-waveform which are stored in a digital memory should be popped sequentially and sent to a DAC synchronous with a variable clock frequency. It was shown that the output signal of the DAC must be filtered and amplified in order to be applied to the sensor as excitation signal. In fact, this ESG architecture is used in modern arbitrary signal generators; however, we adopted the block diagram to be compatible with the SSI and the improved AFDX sensor network architecture.

To extract the ESG design requirements, detailed system-level analysis of the SSI were presented in Section 3.2. With reference to the displacement sensor specifications and the model of the data acquisition unit of the SSI, we concluded the basic necessities of the proposed ESG block diagram. As the main building block of the ESG module, the requirements of the DAC were extracted in Section 3.2. We showed that high-speed 10-bit DAC is needed to convert the digital samples of a sine-wave to equivalent analog value. Based on demonstrated theoretical analysis, a SNR of 84 dB is achievable when an update rate of almost 3.2 MHz is used to generate the sine-waveform in the desired frequency range of 1 kHz to 10 kHz. We also stated that the high update rate of the DAC relaxes the design of the anti-aliasing low pass filter which is used after the DAC. To meet the desired DAC specifications and supported by the outcomes of the literature

survey (Section 2.5), we selected segmented current-steering DAC (SCSDAC) architecture. We argued the choice of segmented type of CSDACs which significantly improves the linearity of the DAC.

As the heart of this Master thesis, we explained and discussed the design procedure of the SCSDAC in Sections 3.3 and 3.4. Based on the most important specifications of the CSDAC which were summarized in Table 3.3, we discussed the three phases (architectural, module, and circuit level) of the SCSDAC design. While we determined the segment sizes and the required matching between current sources, the switching scheme was introduced in the module level phase. Many solutions have been proposed to increase the linearity and accuracy of this DAC type. Nonetheless, we found no published work in which the impacts of the size of Current Source Array (CSA) on the efficiency of the switching sequence have been considered. Hence, we analyzed and simulated such impacts in Section 3.4.2 as the main contribution of this work. We argued that the size of the CSA and the arrangement of the current source transistors in the layout-level must be considered in designing the most efficient switching sequence. In fact, it was shown that there is a significant correlation between the physical implementation of the CSA and the proper switching sequence. Choice of distribution pattern for current sources and switching sequence may play significant role in drawing the design strategy for the targeted DAC structures. Therefore, we followed a recursive approach corresponding to the laid out CSA in order to design the optimum sequence in this work. The derived sequence was introduced in Table 3.6. Some of the results of this work have been published in [58]. In the last phase of the design procedure, the transistor-level circuit and layout design challenges were explained in Sections 3.4.3 and 3.4.4.

In Chapter 4, schematic and post-layout simulations were presented. It was shown that post-layout simulations validate the design. Thus, an excellent accuracy and linearity were expected from the design. However, as a result of a problem in clock distribution path of the input shift register, we were not able to fully test the fabricated chip and characterize its performance. The details of locating this problem and its reason were discussed in Section 4.4.2. We also showed that same problem can be seen in the post-layout simulation if the rise and fall edges of the serial clock prolonged enough. However, the measurement results of the fabricated chip for all “0”s and all “1”s input combinations are within acceptable vicinity of the simulation results.

5.2 Directions for future work

As discussed in Chapter 4, we faced a problem in clock distribution path of the input shift register. The main possible future work is a thorough survey on the architectures and solutions for clock distribution in high density integrated digital circuits. A new shift register can be designed and laid out along with the designed SCSDAC.

In Section 3.2, we presented the architecture of a memory-based ESG which includes DAC, low pass filter, amplifier, and line driver. As a result of importance and complexity of the DAC, the rest the thesis was dedicated to the SCSDAC design. Based on the achievements of this work, an integrated low pass filter and amplifier can be designed and tested with the DAC. This is an interesting system on chip design which can be used in the SSI.

As we explained in Chapter 1, the SSI includes a data acquisition module and an ESG. With reference to the achievements in the design and implementation of the data acquisition unit, integration of complete SSI will be a challenging work that improves the overall performance. The results of such work will comply with the main objective of the AVIO402 project.

In Chapter 3, we introduced the impacts of the square and non-square CSA implementation on the efficiency of the switching sequence in CSDACs. Respecting this design criterion, we designed a non-square CSA with the possibility of employing various switching sequences. In order to further study this phenomenon, it is desirable to design a programmable integrated CSA which can be formed in square or non-square patterns. No major work has been done on this issue and it can boost our understanding of the above-mentioned impacts.

REFERENCES

[1] Guchuan Zhu, Mohamad Sawan, and Ali Naderi, "System Architecture: Data Networks and Smart Sensors for Safety-Critical Avionics Applications," Electrical Engineering, Montreal Polytechnique, Montreal, QC, System Architecture 2012.

[2] RTCA, *Environmental Conditions and Test Procedures for Airborne Equipment*. Washington DC, USA, RTCA DO-160F: RTCA, Inc., 2007.

[3] Ian Moir and Allan Seabridge, *Aircraft systems: Mechanical, electrical, and avionics subsystems integration*. West Sussex, England: John Wiley & Sons Ltd, 2008.

[4] Edward Herceg, *Handbook of measurement and control; an authoritative treatise on the theory and application of the LVDT*. Camden, New Jersey, United States: Schaevitz Engineering, 1976.

[5] Anno Yoo, Seung-Ki Sul, Dong-Cheol Lee, and Cha-Seung Jun, "Novel Speed and Rotor Position Estimation Strategy Using a Dual Observer for Low-Resolution Position Sensors," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2897-2906, December 2009.

[6] Wei Quan and K. Shida, "A Full-Range Space Angular Position Sensor Based on Multifunctional Method," in *5th IEEE Conference on Sensors (ICSENS)*, Daegu, Korea, 2006, pp. 1195-1198.

[7] R. Wegener, F. Senicar, C. Junge, and S. Soter, "Low Cost Position Sensor for Permanent Magnet Linear Drive," in *7th International Conference on Power Electronics and Drive Systems. PEDS '07.*, Bangkok, 2007, pp. 1367-1371.

[8] Assistant secretary for research and engineering. (2011, April) Office of the Under Secretary of Defense for Acquisition, Technology, and Logistics. [Online]. http://www.acq.osd.mil/ddre/publications/docs/TRA2011.pdf

[9] Gerard C. M. Meijer, *Smart Sensor Systems*. Chippenham, Wiltshire, Great Britain: John Wiley & Sons, Ltd, 2008.

[10] Yamu Hu and Mohamad Sawan, "CMOS Front-end Amplifier Dedicated to Monitor Low Amplitude Signal from Implantable Sensors," *Analog IC and Signal Processing Journal*, vol. 33, no. 1, pp. 29-41, 2002.

[11] Jacob Fraden, *Handbook of Modern Sensors: physics, designs, and applications*. Newyork, United States: Springer-Verlag, 2004.

[12] D. Wobschall, "IEEE 1451—a universal transducer protocol standard," in *IEEE Autotestcon*, September 2007, pp. 359-363.

[13] E. Y. Song and Lee Kang, "Understanding IEEE 1451-Networked smart transducer interface standard - What is a smart transducer?," *IEEE Instrumentation & Measurement Magazine* , vol. 11, no. 2, pp. 11-17, April 2008.

[14] R.L. Oostdyk, C.T. Mata, and J.M. Perotti, "A Kennedy Space Center implementation of IEEE 1451 networked smart sensors and lessons learned," in *IEEE Aerospace Conference*, Big Sky, MT , 2006.

[15] L.H. Eccles, "The need for smart transducers: an aerospace test and evaluation perspective," *IEEE Instrumentation & Measurement Magazine*, vol. 11, no. 2, pp. pp.23,28, April 2008.

[16] J.-Ph. Tremblay, Y. Savaria, G. Zhu, and C. Thibeault, "A System Architecture for Smart Sensors Integration in Avionics Applications," *SAE International Journal of Aerospace*, vol. 5, no. 1, pp. 189-195, October 2012.

[17] Saeid Hashemi, Masood Karimian, jinying Zhang, Ali Naderi, and Mohamad Sawan, "Generic Architecture for a Self-Powered Smart Sensor Interface in Avionic Application," in *Aerospace Electronics and Avionics Systems Conference*, Phoenix, Arizona, USA, 2012.

[18] Keith Antonelli et al., "Displacement Measurement, Linear and Angular," in *The Measurement, Instrumentation and Sensors Handbook*. USA: CRC Press, 1999, ch. 6.

[19] R. W. Borek, A. Pool, and D. Bosman, *Basic principles of flight test instrumentation engineering*, Second edition ed. Essex, England: Advisory Group for Aerospace Research and Development (AGARD), 1994.

[20] J. R. Wolf, "The Linear Variable Differential Transformer and its uses for in-core fuel rod behavior measurements," in *International colloquium on irradiation for reactor safety programmes*, Petten, Netherlands, 1979.

[21] Assem O. Alradi and S. George Carruthers, "Evaluation and application of the linear variable differential transformer technique for the assessment of human dorsal hand vein alpha-receptor activity," *Clinical Pharmacology & Therapeutics*, vol. 38, no. 5, pp. 495-502, November 1985.

[22] M. Cohen, R. Savé, C. Biel, and O. Marfà, "Simultaneous measurements of water stress with LVDT sensors and electrotensiometers: application in pepper plants grown in two types of perlites," in *II International Symposium On Sensors in Horticulture*, Greve, Denmark, 1998, pp. 193-200.

[23] Edward A. Stephenson, "Aircraft flight data recorder data acquisition system," 4656585, April 07, 1987.

[24] Cary R. Spitzer, *The Avionics Handbook*. USA: CRC Press LLC, 2001.

[25] Jon S. Wilson, *Sensor Technology Handbook*. Burlington, MA, USA: Elsevier Inc., 2005.

[26] Honeywell Inc., *Sensing and Control Product Catalog (TM08)*. Golden Valley, MN, USA: Honeywell international Inc., March 2008.

[27] Measurement Specialties. (2012, October) LVDT/RVDT Signal Conditioning. [Online]. http://www.meas-spec.com/position-sensors/position-sensor-instrumentation/lvdt-rvdt-signal-conditioning.aspx

[28] Measurement Specialties. (2012, September) AC RVDTs. [Online]. http://www.meas-

spec.com/position-sensors/rotary-displacement-sensors/ac-rvdts.aspx

[29] Active Sensors. (2012, September) RVDT position sensors. [Online]. http://www.activesensors.com/products/rvdt-position-sensors

[30] A. Boglietti, A. Cavagnino, A. Tenconi, and S. Vaschetto, "The safety critical electric machines and drives in the more electric aircraft: A survey," in *35th Annual Conference of IEEE on Industrial Electronics (IECON)* , Porto, Portugal, Nov. 2009, pp. 2587-2594.

[31] Collinson R.P.G., *Introduction to Avionics Systems*, 3rd ed. Maidstone, Kent, UK: Springer, 2011.

[32] B.A. Rich, P.J. Lehnerd, and J.A. Gracia, "Benefits and challenges of integrated sensor systems," in *IEEE National Aerospace and Electronics Conference (NAECON)*, vol. 1, Dayton, OH, May 1995, pp. 352-358.

[33] R. Szkody, "Integrated sensor system-demonstration results," in *18th Digital Avionics Systems Conference* , vol. 1, St Louis, MO, Nov. 1999, pp. 3.B.3-1 - 3.B.3-8.

[34] T. J. Redling, "Integrated flight control systems: a new paradigm for an old art," *IEEE Aerospace and Electronic Systems Magazine*, vol. 16, no. 5, pp. 17-22, May 2001.

[35] L. Wang, X. Wang, and Y. Sun, "Intelligent Acquisition Module for Differential Transformer Position Sensor," in *International Conference on Intelligent System Design and Engineering Application (ISDEA)*, vol. 1, Changsha, China, Oct. 2010, pp. 878-883.

[36] A. Drumea, A. Vasile, M. Comes, and M. Blejan, "System on Chip Signal Conditioner for LVDT Sensors," in *First Electronics Systemintegration Technology Conference*, vol. 1, Dresden, Germany, September 2006, pp. 629-634.

[37] J. Fan et al., "Application of LVDT sensor data acquisition system based on PCI-1716," in *IEEE International Conference on Computer Science and Automation Engineering (CSAE)*, vol. 3, Shanghai, China, June 2011, pp. 548-552.

[38] A. Canu, D. Faura, P. Toillon, M. Gatti, and Ph. Benabes, "A versatile input interface for avionic computers," in *IEEE/AIAA 30th Digital Avionics Systems Conference (DASC)*, Seattle, WA, USA, October 2011, pp. 7A3-1 - 7A3-11.

[39] Analog Devices. (2012, september) AD598(LVDT signal conditioner) datasheet. [Online]. http://www.analog.com/static/imported-files/data_sheets/AD598.pdf

[40] Analog Devices. (2012, October) AD698(Universal LVDT signal conditioner) datasheet. [Online]. http://www.analog.com/static/imported-files/data_sheets/AD698.pdf

[41] Macro Sensors. (2012, October) [Online]. http://www.macrosensors.com/index.html

[42] AA Lab Systems. (2011, May) [Online]. http://www.lab-systems.com/index.html

[43] Alliance Sensors Group. (2012, October) Everight Sensors. [Online]. http://www.everightsensors.com/LVDT_Signal_Conditioner/LVDT_Signal_Conditioner.shtml

[44] Chao Yang and A.J. Mason, "Fully Integrated Seven-Order Frequency-Range Quadrature Sinusoid Signal Generator," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 10, pp. 3481-3489, October 2009.

[45] Tektronix Inc. (2012, November) "XYZs of Signal Generators". [Online]. http://www.tek.com/landing-page/signal-generator-tutorial-support-0

[46] Frequency Devices Inc. (2012, October) SPPOSC Series Oscillators. [Online]. http://www.freqdev.com/products/osc/spposc.pdf

[47] R. J. Baker, *CMOS: Circuit design, layout, and simulation*, 3rd ed., S. K. Tewksbury and J.E. Brewer, Eds. Hoboken, New Jersey, USA: Wiley-IEEE Press, 2011.

[48] B. Razavi, *Principles of Data Conversion System Design*. Piscataway, New Jersey, USA: IEEE Press, 1995.

[49] W. Kester, *The Data Conversion Handbook*. USA: Analog Devices, 2005.

[50] M. Gustavsson, J.J. Wikner, and N. Nick Tan, *CMOS Data Converters for Communication*. USA: Kluwer Academic Publishers, 2002.

[51] D. Marche, Y. Savaria, and Y. Gagnon, "An Improved Switch Compensation Technique for Inverted R-2R Ladder DACs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 6, pp. 1115-1124, June 2009.

[52] A. van den Bosch, M.A.F. Borremans, and M. Steyaert, "A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 315-324, March 2001.

[53] G.A.M. Van Der Plas, J. Vandenbussche, W. Sansen, M.S.J. Steyaert, and G.G.E Gielen, "A 14-bit intrinsic accuracy Q2 random walk CMOS DAC," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1708-1718, December 1999.

[54] K. O'Sullivan, C. Gorman, M. Hennessy, and V. Callaghan, "A 12-bit 320-MSample/s current-steering CMOS D/A converter in 0.44 mm2," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1064- 1072, July 2004.

[55] J. Deveugele and M.S.J. Steyaert, "A 10-bit 250-MS/s binary-weighted current-steering DAC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 320- 329, February 2006.

[56] L. Da-Huei, L. Yu-Hong, and T.H. Kuo, "Nyquist-Rate Current-Steering Digital-to-Analog Converters With Random Multiple Data-Weighted Averaging Technique and Rotated Walk Switching Scheme," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 11, pp. 1264-1268, November 2006.

[57] P. Palmers and M.S.J. Steyaert, "A 10–Bit 1.6-GS/s 27-mW Current-Steering D/A Converter With 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 11, pp. 2870-2879, November 2010.

[58] Masood Karimian, Saeid Hashemi, Ali Naderi, and Mohamad Sawan, "Impact of gradient error on switching sequence in high-accuracy thermometer-decoded current-steering

DACs," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, Korea (South), 2012, pp. 1279-1282.

[59] J. Vandenbussche, G. Gielen, and M. Steyaert, *Systematic Design of Analog IP Blocks*. Dordrecht, Netherlands: Kluwer Academic Publishers, 2003.

[60] T. Chen and G.G.E. Gielen, "A 14-bit 200-MHz Current-Steering DAC With Switching-Sequence Post-Adjustment Calibration," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2386-2394, November 2007.

[61] T. Zeng and D. Chen, "New sequence switching and layout technique for high-speed high-accuracy current-steering DACs," in *Proceedings of the IEEE 2009 National Aerospace & Electronics Conference (NAECON)*, Dayton, OH, July 2009, pp. 256-259.

[62] Y. Cong and R.L Geiger, "Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays,"" *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 7, pp. 585-595, July 2000.

[63] Ko-Chi Kuo and Chi-Wei Wu, "A Switching Sequence for Linear Gradient Error Compensation in the DAC Design," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 8, pp. 502-506, August 2011.

[64] D.H. Lee, Y.H. Lin, and T.H. Kuo, "Nyquist-Rate Current-Steering Digital-to-Analog Converters With Random Multiple Data-Weighted Averaging Technique and QN Rotated Walk Switching Scheme," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 11, pp. 1264-1268, November 2006.

[65] M.J.M. Pelgrom, A.C.J. Duinmaijer, and A.P. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433- 1439, October 1989.

[66] F. Gansmandel, F. Clement, and P. Molaret, "CRAIQ project AVIO402/ NSERC CRD smart sensors," Thales Canada Inc., Montreal, ARA-R&D-10-0049, Rev: NC, June 2010.

[67] Chi-Hung Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *Solid-State Circuits, IEEE Journal of* , vol. 33, no. 12, pp. 1948-1958, December 1998.

[68] (2013, January) CMC Microsystems. [Online]. http://www.cmc.ca/

[69] IBM Microelectronics Division. (2010, November) CMOS8RF (CMRF8SF) Design Manual. Technology document.

[70] IBM Microelectronics Division. (2010, November) CMRF8SF Model Reference Guide. Technology document.

[71] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 33, no. 12, pp. 1959-1969, December 1998.

[72] A. Van den Bosch, M. S. J. Steyaert, and W. Sansen, "An Accurate Statistical Yield Model For CMOS Current-Steering D/A Converters," in *IEEE International Symposium on*

Circuits and Systems (ISCAS), Geneva, Switzerland, May 2000, pp. IV-105-108.

[73] J. J. Wikner and N. Tan, "Influence of Circuit Imperfections on the Performance of DACs," *Analog Integrated Circuit and Signal Processing*, vol. 18, no. 1, pp. 7-20, January 1999.

[74] Alan Hastings, *The Art of Analog Layout*, 2nd ed.: Prentice Hall, July 2005.

[75] E.G. Friedman, "Clock distribution networks in synchronous digital integrated circuits," *Proceedings of the IEEE*, vol. 89, no. 5, pp. pp.665,692, May 2001.