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IR-UWB AND OFDM-UWB TRANSCEIVER NODES FOR COMMUNICATION AND POSITIONING PURPOSES

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DEDICATION

To my beloved parents, sisters, wife and daughter
For their endless love, encouragment and support

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Résumé

Ultra-wideband (UWB) a suscité l'intérêt de chercheurs et de l'industrie en raison de ses nombreux avantages tels que la faible probabilité d'interception et de la possibilité de combiner la communication des données de positionnement dans un seul système. Il existe plusieurs UWB couche physique (PHY) présentées initialement à la norme IEEE qui convergent en deux propositions principales: des porte-UWB ou Orthogonal Frequency-Division Multiplexing (OFDM-UWB), et à court d'impulsion porteuse à-UWB ou Impulse Radio-(IR-UWB).

Une des plus grandes tâches difficiles pour les chercheurs est de nos jours la conception d'émetteurs-récepteurs UWB optimisés qui satisfont à des conditions rigoureuses, dont la simplicité caractéristiques large bande, à faible coût et de conception. Des études antérieures ont montré que les récepteurs à conversion directe basée sur Wave-radio interféromètre (WRI) circuits représentent un bon candidat pour les applications UWB. Circuits IRG ont plusieurs avantages tels que l'exploitation à large bande, à faible coût et la simplicité. Des travaux antérieurs sur l'IRG circuit, cependant, a enquêté sur le circuit de l'IRG sur la base du concept de porteuse unique signaux (par exemple, les signaux sinusoïdaux). L'objectif de ce projet est de fournir les résultats de conception, de simulation, de mise en œuvre et le test d'un émetteur-récepteur WRI basé sur ce que peut être utilisé comme un nœud ou un pico-réseau dans un détecteur sans fil / réseau de données. Nous allons passer par les étapes de conception et de mise en œuvre de propositions UWB deux: IR-UWB et OFDM-UWB. Pour la proposition porteuse à nous concentrer sur la conception et la mise en œuvre de l'émetteur-récepteur en intégrant les

opérations de transmission / réception dans un prototype unique, alors que pour la proposition des porte-nous concevoir et mettre en œuvre l'émetteur-récepteur avec le circuit de l'IRG dans le récepteur seulement utilisé en tant que convertisseur abaisseur directe.

Résultats expérimentaux, de simulation et d'analyse ont été obtenus et sont présentés dans cette thèse.

La mise en œuvre de l'(IR-UWB) et (OFDM UWB-) émetteurs-récepteurs utilisant une nouvelle conception de Wave Radio-interféromètre (WRI) comme un circuit convertisseur abaisseur directement dans un canal réaliste UWB est présenté. Selon les spécifications IEEE 802.15.3a standard, un code MATLAB a été utilisé pour générer le modèle de canal pour des simulations et des mesures. Le même code représentant la réponse impulsionnelle du canal a été importé vers un émulateur de canal radio à imiter le comportement du canal sans fil pour les mesures en laboratoire. Une étude analytique de l'outil de taux d'erreur (BER) des deux émetteurs-récepteurs est prévu. En outre, pour les émetteurs-récepteurs proposés opérant dans la gamme de fréquences (3,1-4.1GHz), une étude comparative entre plusieurs modèles de canaux standard (CM1) et (CM4) est présentée pour chaque scénario. Le but de cette étude est de montrer meilleurs et les pires scénarios de rendement par rapport à des cas l'émetteur-récepteur proposée dans un canal réaliste décoloration aidé avec les résultats analytiques. En outre, différentes configurations de transmission / réception des antennes ont été envisagées, notamment à une seule entrée à sortie unique (SISO), une seule entrée multiple-sortie (SIMO) et à entrées multiples-sorties multiples (MIMO). Pour chaque

configuration, nous offrons la même étude comparative des modèles de canaux CM1 et CM4. Les résultats de simulation, d'analyse et de mesure de démontrer que les implémentations d'émetteur-récepteur les deux ont le même ordre de diversité. Toutefois, l'IR-UWB émetteur-récepteur présente une moyenne de 2 dB rapport signal sur bruit (SNR) de perte par rapport à la même configuration du nombre de transmettre et de recevoir des antennes UWB OFDM pour émetteur-récepteur. Cela est dû à la propagation par trajets multiples immunité héritée avantage dans les systèmes OFDM. En outre, les deux spectacles émetteurs-récepteurs sont analysés en considérant IQ dégradations de canal. Utilisation ± 0.5 dB et ± 9^{o} que les déséquilibres d'amplitude et de phase, respectivement, il se trouve que OFDM UWB-récepteur est plus sensible aux erreurs de décodage en raison de la sensibilité élevée de sous-porteuses gigue de phase. En outre, les résultats obtenus démontrent que BER WRI-UWB émetteurs-récepteurs peuvent fournir des résultats comparables à la performance BER typiques émetteurs-récepteurs UWB. La formulation analytique fourni sert comme une limite supérieure sur la performance attendue de l'IRG BER-UWB systèmes. Plage de mesure a été limitée par la simulation et les outils de mesure. Une méthode de synchronisation filaire a été utilisé pour éviter l'expertise de synchronisation unique ne sont pas couverts dans cette thèse.

Abstract

Ultra-wideband (UWB) technology has attracted interest from both researchers and the industry due to its numerous advantages such as low probability of interception and the possibility of combining data communication with positioning in a single system. There are several different UWB physical layer (PHY) proposals originally submitted to IEEE which converged into two main proposals: carrier-based UWB or Orthogonal-Frequency Division Multiplexing (OFDM-UWB), and short-pulse carrierless-UWB or Impulse-Radio (IR-UWB).

One of the biggest challenging tasks for researchers nowadays is the design of optimized UWB transceivers that would satisfy rigorous conditions, among which wideband characteristics, low-cost and design simplicity. Previous studies have shown that direct-conversion receivers based on Wave-Radio Interferometer (WRI) circuits represent a suitable candidate for UWB applications. WRI circuits have several advantages such as wideband operation, low cost, and simplicity. Previous works on WRI circuit, however, investigated the WRI circuit based on the concept of single-carrier signals (i.e., sinusoidal signals). The objective of this project is to provide the design, simulation, implementation and testing results of a WRI-based transceiver that can be utilized as a node or a piconet in a wireless sensor/data network. We will go through the design and implementation steps for both UWB proposals: IR-UWB and OFDM-UWB. For the carrierless proposal we will focus on designing and implementing the transceiver by integrating the transmitter/receiver operations in a single prototype, while for the carrier-based proposal we will design and implement the transceiver with

the WRI circuit in the receiver only utilized as a direct downconverter.

Experimental, simulation and analytical results have been obtained and are presented in this thesis.

The implementation of the (IR-UWB) and (OFDM-UWB) transceivers employing a novel design of Wave-Radio Interferometer (WRI) circuit as a direct down-converter in a realistic UWB channel is presented. According to IEEE 802.15.3a standard specifications, a MATLAB code has been used to generate the channel model for simulations and measurements. The same code representing the channel impulse response has been imported to a radio channel emulator to imitate the wireless channel behavior for the laboratory measurements. An analytical investigation of the bit-error-rate (BER) performance of both transceivers is provided.

Also, for the proposed transceivers operating in the frequency range (3.1–4.1GHz), a comparative study between standard channel models (CM1) and (CM4) is presented for each scenario. The aim of this study is to show best vs. worst case performance scenarios for the proposed transceiver in a realistic fading channel aided with analytical results.

Further, different configurations of transmit/receive antennas have been considered including single-input single-output (SISO), single-input multiple-output (SIMO) and multiple-input multiple-output (MIMO). For each configuration, we provide the same comparative study for channel models CM1 and CM4. Simulation, analysis and measurement results demonstrate that both transceiver implementations have the same diversity order. However, IR-UWB transceiver shows an average 2dB signal-to-noise

ratio (SNR) loss compared to the same configuration of the number of transmit and receive antennas for OFDM-UWB transceiver. This is due to the multipath immunity inherited advantage in OFDM systems. In addition, both transceiver performances are analyzed considering IQ channel impairments. Using ±0.5dB and $\pm 9^{o}$ as amplitude and phase imbalances, respectively, it's found that OFDM-UWB transceiver is more susceptible to decoding errors due to subcarriers high sensitivity to phase jitter. Also, the obtained BER results demonstrate that WRI-UWB transceivers can provide comparable BER performance results to typical UWB transceivers. The analytical formulation provided serves as an upper bound on the expected BER performance of WRI-UWB systems. Measurement range was limited by simulation and measurement tools. A wired synchronization method was used to avoid unique synchronization expertise not covered in this thesis.

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LIST OF SIGNS AND ABBREVIATIONS

CPW	Co-planar waveguide
I	In-phase
LUT	Look-up-table
MHMIC	Monolithic hybrid microwave integrated circuit
Q	Quadrature
ADC	Analog-to-digital converter
ADS	Advanced Design System
AWGN	Additive white Gaussian noise
BER	Bit error rate
BPSK	Binary phase shift keying
BPSM	Binary phase spectrum modulation
CRLH	Composite right/left-handed
DAC	Data access component
DSP	Digital signal processing
DS-UWB	Direct-Sequence UWB
DUT	Device under test
EVM	Error-vector-magnitude
FCC	Federal Communications Commission
FMCW	Frequency modulation continuous wave
FPGA	Field programmable gate arrays

GMAC	Giga multiply-accumulate
GPS	Global positioning system
IF	Intermediate frequency
IP	Intellectual property
ISI	Inter symbol interference
I-UWB	Impulse UWB
LEs	Logic elements
LO	Local oscillator
MB-OFDM	Multiband orthogonal frequency-division multiplexing
Mbps	Mega bit per second
MB-UWB	Multiband Ultra wide band
MC-UWB	Multicarrier Ultra wide band
MIR	Multi(six)-port impulse radio
MMIC	Monolithic microwave integrated circuit
M-PSK	M-ary phase shift keying
Msps	Mega symbol per second
NF	Noise figure
PAM	Pulse amplitude modulation
PCS	Personal communication system
PPM	Pulse position modulation
PPM	Pulse position modulation
PR	Pseudo random

PSD	Power spectral density
PSM	Phase spectrum modulation
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
QPSM	Quaternary phase spectrum modulation
RF	Radio frequency
SDR	Software defined radio
SIW	Substrate integrated waveguide
TFMA	Time-frequency multiple access
TSDF	Timed synchronous data flow
U-NII	Unlicensed National Information Infrastructure
UWB	Ultra-wideband
WPAN	Wireless personal area network
WRI	Wave-Radio Interferometer

CHAPTER 1 INTRODUCTION

1.1 Research overview

Wireless communication has become the most important communication mean and its use has increased dramatically over the last decade, due to the high demand on communication systems capable of providing easier connectivity anywhere and anytime with high data transfer rates. On the other hand, wireless systems are now used for computer networking and internet access in addition to voice/video communications. Moreover, the emphasis has shifted from providing fixed voice services to general wireless digital services that allow a wide variety of applications [1]-[6]. As a consequence of this growth, the need to develop new higher-capacity and highly reliable communication systems is increasing and driving research work to develop more integrated services, providing higher data rates and more universal interface for a variety of applications.

Among the new emerging communication technologies, Ultra-wideband (UWB) technology has attracted interest from both researchers and the industry due to its numerous advantages such as low probability of interception and the possibility of combining data communication with positioning in a single system. Since applications targeted for UWB need to satisfy stringent design requirements, the goal of improving the inherent UWB transceivers design was the main focus of researches during the last few years [7].

On the other hand, previous research works indicated that direct-conversion receivers have numerous advantages over their heterodyne counterparts when used for UWB applications. Those advantages include reducing circuit complexity and allowing a higher level of circuit integration than conventional heterodyne receivers [7]. Direct conversion receivers based on the Wave-Radio Interferometer (WRI) (commonly know in the literature by Multi-port circuits) have been proposed [8] as multimode or software receivers operating with digital signal processors (DSPs) programmed for a number of modulation schemes. The utilization of WRI circuit in homodyne receivers has been realized in several variants including mixers, modulators, demodulators and antennas [7].

Although previous research efforts tackled the implementation of homodyne transceivers for several technologies and frequency bands [9]-[12], none of these works considered testing these transceivers in realistic channel conditions. Also, those studies were limited in considering Impulse-Radio (IR) UWB standard only when homodyne transceivers were designed for communication and positioning application [13]. Moreover, as higher capacity and data throughput is nowadays a driving force for more research work, another deficiency found in previous works is the lack of considering multiple-transmit and receive antenna configurations. Taking into account all these factors, this thesis builds a frame work that considers implementing an UWB homodyne transceiver using IR and Orthogonal-Frequency Division-Multiplexing (OFDM) modulation schemes that can be applied in communication or positioning applications.

1.2 Research problem

With the continuous increase in demand of higher throughput, low-cost wireless devices and more strict access to the available spectrum, previous research on WRI circuits of homodyne transceivers focuses on the improvement of transmitters and receivers on the component level. In this thesis we alleviate these challenges by adopting new modulation schemes like OFDM and multiple-antenna configurations on the transmitter and receiver sides.

In the present research project, the main goal is to develop a comparison and design efficient transceiver nodes using IR-UWB and OFDM-UWB standards. These transceiver nodes can be utilized for communications, tracking and positioning or short-range radar imaging. The most general objectives and specifications in a transceiver design for such applications are mainly controlled by parameters, such as cost, size, simplicity and power efficiency. To achieve these objectives, WRI circuit is used as an RF front-end for the transceivers. Furthermore, this study provides a realistic benchmark of both transceivers performance in UWB wireless channel. To achieve that, IEEE802.15.3a UWB standard channel is re-generated for simulation and emulation in the lab environment. Below, the main contributions in this thesis are addressed with emphasis on tackled challenges and their solutions.

1.3 Thesis objectives and contributions

The most important feature of a WRI circuit is the ability to perform accurate phase discrimination both in low radio frequency (RF) and millimeter wave frequency range. The phase discrimination capability is feasible over a wide bandwidth as long as the

WRI circuits cover the wideband frequency range.

For an UWB signal occupying an absolute bandwidth of more than 500 MHz, the implementation of wideband radio devices appears to be a unique challenge. Previous studies, investigating WRI circuit considering sinusoidal signals, have shown that WRI circuit has several advantages such as wideband operation, low cost, and simplicity. The entire 3.1–10.6-GHz UWB band can be covered with one or two WRI circuits fabricated with low cost integrated circuit chips. The WRI technology for UWB applications is therefore promising and this project will originally study this topic.

Consequently, the objectives of this research are as follows:

- As known, the use of WRI circuit as a digital modulator/demodulator was achieved previously by integrating ready system components to implement the WRI circuit. For the proposed carrierless UWB system, we introduce a design and implementation of a dual-layer fully fabricated WRI circuit in the lab.
- Compared to the previous WRI circuit, the newly fabricated WRI circuit combines both functions of modulation and demodulation on the same circuit, which translates to lower cost and size.
- Another feature of the new WRI circuit is its dynamic range which extends to approximately double the dynamic range of the prior design due to the used of the log-power detectors.
- Implementation for an OFDM-UWB system in an emulated wireless channel with WRI circuit utilized for direct downconversion.

- Implementation considering a realistic UWB channel based on IEEE802.15.3a channel model with a receiver using WRI circuit for direct downconversion.
- Simulation and implementation for different variants of transmit/receive configurations of the transceiver; *i.e.*, SISO, SIMO and MIMO. Implementing these variants using the channel emulator in the lab assumed uncorrelated fading statistics between different channels.
- Providing analytical bit-error-rate (BER) expressions to benchmark IR-UWB and OFDM-UWB transceivers performance.

In this project, a novel WRI circuit operating in the range (3.1-4.1 GHz) is designed, fabricated and utilized in test bench platforms considering IR-UWB and OFDM-UWB standards. Based on research work done previously on WRI technology [14], it can be concluded that the entire 3.1 GHz to 10.6 GHz UWB band can be covered with one or two integrated circuit chips. The testing platforms adopt quasi-symmetric receiver and transmitter architecture (using WRI circuits to digitally modulate and demodulate the input impulse phase spectrum in accordance with FCC UWB bandwidth). In the IR-UWB transceiver, digital baseband data is modulating the phase spectrum of the input pulse using the fabricated WRI circuit, while for OFDM-UWB it's used to modulate the OFDM subcarriers. Then, modulated signals undergo an additive white Gaussian noise (AWGN) channel and a realistic channel fading based on IEEE802.15.3a standard using the channel emulator.

Some of the modulation and demodulation algorithms are developed in field-programmable gate array (FPGA) using digital signal processing (DSP) techniques.

Analytical, simulation and experimental results for both implementations are obtained and presented in this thesis.

1.4 Thesis outline

Based on this focus, this dissertation is arranged in six chapters. The current chapter presented the research overview, definition of the research problem, thesis objectives, and contributions. Chapter 2 will present the necessary background for UWB technology, WRI circuits and the IEEE802.15.3a UWB standard channel used to emulate the wireless channel behavior in the test bench. In Chapter 3, the newly fabricated WRI circuit is introduced where we show its S-parameters and phase response results. Chapter 4 covers detailed results of the IR-UWB transceiver utilizing the fabricated WRI circuit. Chapter 5 provides details on the OFDM-UWB transceiver results. Finally, conclusions and future works are summarized in Chapter 6.

CHAPTER 2 UWB AND WRI CIRCUIT BACKGROUND

2.1 Introduction

As the communication systems are moving towards the wireless media, the need for efficient new wireless technologies and more optimized design for transceiver systems are pushing. In fact, some efficient promising wideband techniques like ultra-wideband (UWB) have been proposed, but the problem associated with them is how to provide efficient means of modulation and demodulation either on the baseband or the radio frequency domains. Besides that, a paramount challenge for UWB receiver systems is how to mitigate the wideband fading channel scenarios. In this chapter, a brief introduction of UWB technology considering its different modulation schemes IR and OFDM is introduced. Then, previous research accomplishments on WRI circuit are summarized with emphasis on different applications of the circuit. Finally, IEEE802.15.3a UWB channel model used in this work to emulate the wireless channel during simulation and lab measurements is presented.

2.2 Review of ultra-wideband (UWB) technology

Ultra-wideband (UWB) technology has attracted considerable attention in both short-range wireless communication and radio frequency (RF) location sensing applications. Major advantages of this technology include fine time resolution, resistance to multi-path, low probability of interception, potentially low complexity and low cost, and the possibility of combining data communication with positioning in a single system [14]-

[18].

A UWB signal is currently defined as a signal with an instantaneous fractional bandwidth (B_f) greater than 0.20. The fractional bandwidth can be determined in (2.1) [19].

$$B_f = 2\frac{f_H - f_L}{f_H + f_L} \tag{2.1}$$

where f_L is the lower frequency and f_H is the higher frequency -3dB points in the signal spectrum, respectively. Also, according to the Federal Communications Commission (FCC) report on UWB [20], a signal is recognized as UWB if the signal occupies 500MHz (or more) bandwidth at -10dB emission points regardless of the fractional bandwidth value. The radiation limit mandated by FCC for indoor UWB applications is maximum power output of -41.3dBm/MHz between 3.1GHz and 10.6GHz. Figure 2-1 shows the spectral mask mandated by the FCC for unlicensed UWB communications. Spectral mask of some existing radio standards, such as global positioning system (GPS) and personal communication system (PCS) are also shown in Figure 2-1 for comparison purposes.

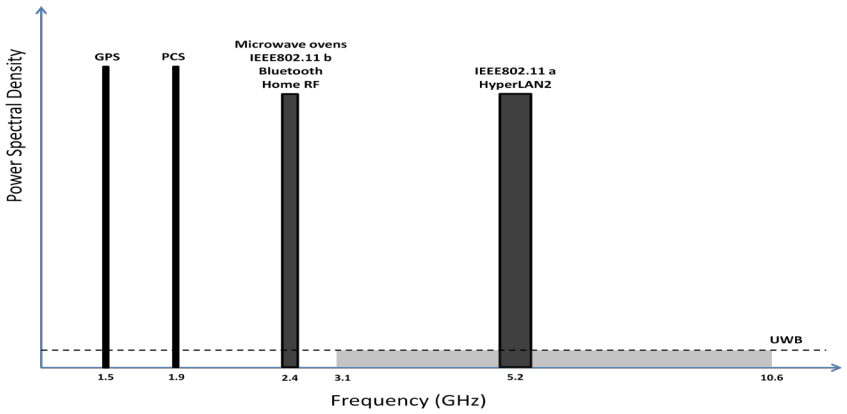

Figure 2-1: FCC spectral mask for unlicensed UWB communications and a comparison with other radio standards [21].

Current UWB systems can be primarily categorized into carrierless and carrier-based UWB. Carrierless UWB, also known as Impulse-Radio UWB (IR-UWB) utilizes very short pulse in transmission. Common choices of modulation scheme in IR-UWB communication include pulse position modulation (PPM), pulse amplitude modulation (PAM), and pulse shape modulation [22]. In above modulation methods, data information is conveyed either in position, amplitude or shape of a pulse. In this category, one of the leading proposals during UWB standardization activities is known as Direct-Sequence UWB (DS-UWB) [23]. In the DS-UWB system, as shown in Figure 1-2, the 3.1- to 10.6-GHz band is divided into a low band from 3.1 to 4.9 GHz and an optional high band from 6.2 to 9.7 GHz. The bandwidth of the high band is twice the bandwidth of the low band, resulting in shorter time-domain pulses in the high band. The 4.9- to 6.1-GHz band is purposely neglected to avoid interference with IEEE 802.11a devices operating in the 5-GHz unlicensed national information infrastructure (U-NII) bands. Each piconet of the DS-UWB operates in one of the two bands, and

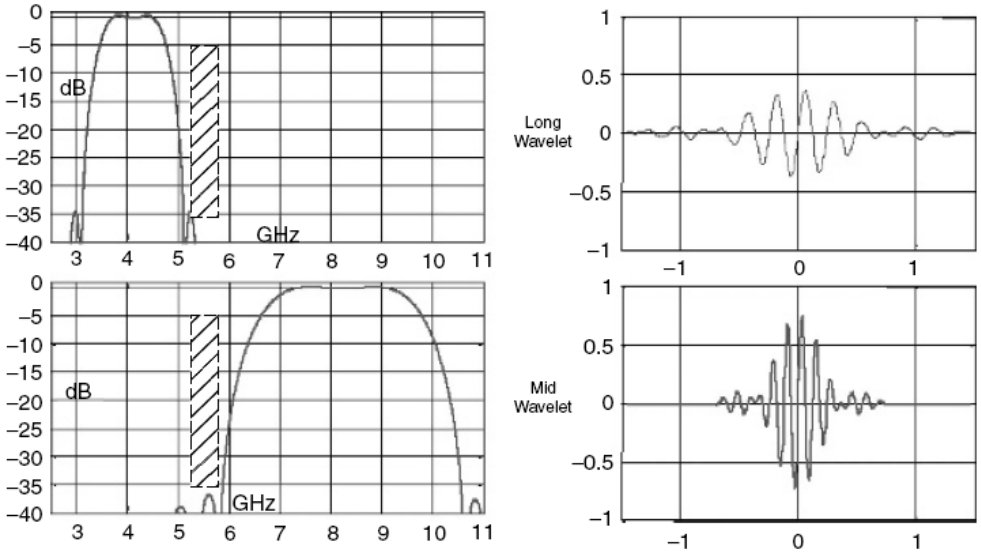

Figure 2-2: Frequency and time response of the two basic channels in the DS-UWB proposal [19].

piconets in the same band are separated by code-division multiplexing. The basic coverage cell, referred to as a picocell, has a nominal coverage range of about 10 m. A network operating within that range is referred to as a piconet.

Carrier-based UWB, however, uses multiple simultaneous carriers in transmission. Common forms of carrier-based UWB exist such as Multicarrier UWB (MC-UWB), Multiband UWB (MB-UWB). In this category, the leading proposal for the IEEE 802.15.3a is Multiband OFDM (MB-OFDM). The MB-OFDM system uses the OFDM technique in the UWB 3.1- to 10.6-GHz unlicensed bands. Following this approach, the spectrum is divided into 15 bands each of width 528 MHz. In each band, a 128-point OFDM system using QPSK modulation is implemented to limit the required precision of mathematical operations and make digital implementation at ultrahigh sampling rates feasible. Figure 2-3 gives an overview of the MB-OFDM proposal. The 15 bands in the

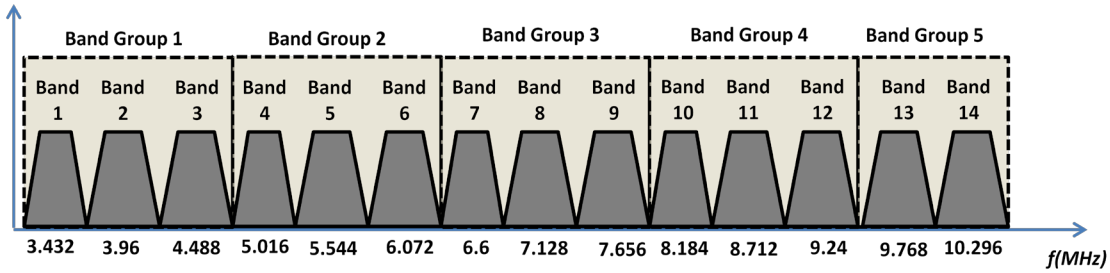

Figure 2-3: Frequency bands, groups of frequencies, within each group of the MB-OFDM approach to UWB communications in 3.1- to 10.6-GHz unlicensed UWB bands proposed to the IEEE 802.15.3a WPAN standard [19].

3.1 − 10.6 GHz unlicensed UWB spectrum are divided into five groups of 528-MHz bands. Group 1 is the most desirable because group 2 interferes with U-NII bands and IEEE 802.11a devices, and higher groups have smaller coverage areas. Each physical piconet is implemented in a band group and several logical piconets share a band group using different time-frequency multiple access (TFMA) codes.

Other research and development activities on UWB include UWB channel characteristics, UWB antennas, and generation of UWB waveforms, etc. More detail can be found in [8], [12] and [18].

2.3 Review of Wave-Radio Interferometer technology

The Wave-Radio Interferometer (WRI) was first used on microwave measurement to obtain the complex reflection coefficient of a device under test (DUT) [24]. The complex ratio of the device connected at one input ports of a WRI circuit can be determined by observing signal powers at the remaining four output ports which is called test ports. Figure 2-4 shows the diagram of a WRI circuit used for this kind of microwave measurement.

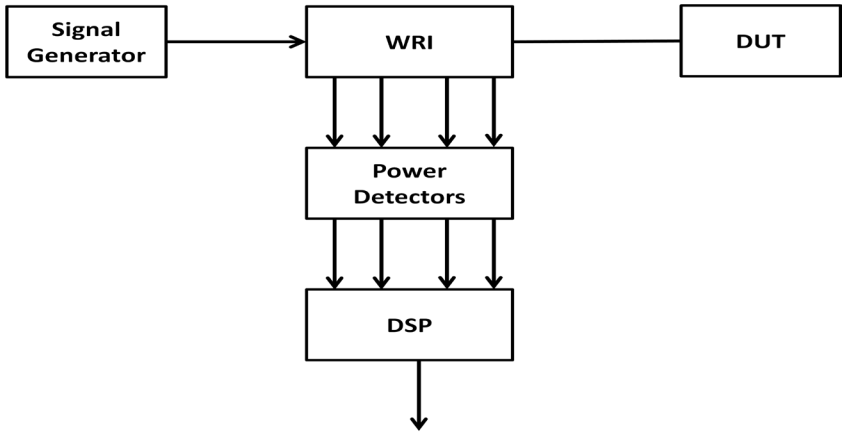

Figure 2-4: WRI reflectometer for microwave measurment.

One of the benefits of WRI-based measurement technique is that these power observations at the test ports are from locations other than the position of interest. This feature can be utilized to avoid violating of uniformity using a uniform transmission line or waveguide at the interface between the WRI circuit and the DUT. Other methods of observing the signal (e.g.,via probes, etc.) at the position of interest also violates unfortunately the uniformity.

The concept of calculating the complex ratio of an incoming signal and a known local oscillator (LO) signal by using the WRI was then applied to communication receivers [12]–[16]. From a communication receiver point of view, the amplitude and phase information embedded in the complex ratio can be used for demodulating phase or amplitude modulated signals. In [12]–[16], the WRI technology was reported as a direct conversion receiver operated with sinusoidal signals at millimeter-wave and radio frequencies (RF). The WRI receivers, shown in Figure 2-5, directly demodulate the data information carried on a single carrier using quadrature-phase shift keying (QPSK), quadrature amplitude modulation (QAM), etc. Standard direct conversion usually uses

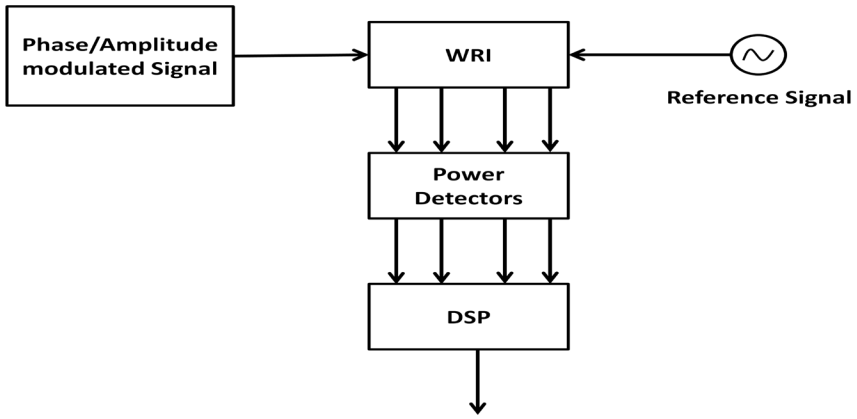

Figure 2-5: WRI direct conversion receiver.

two quadrature (Q) carrier paths to do the direct conversion without intermediate frequencies (IF), i.e., the in-phase (I) and quadrature signal are separated at RF stage [25]. The previously reported WRI-based direct conversion receivers, however, use only one carrier and separates I and Q signals by signal processing after the four outputs at base band stage. This direct conversion or demodulation feature of a WRI circuit was applied to software defined radio (SDR) platform by utilizing the flexibility of signal processing at base band. As candidate SDR receiver architecture, the WRI-based configurable receiver architecture, shown in Figure 2-6, can demodulate several modulation schemes such as QPSK and QAM. Detail investigations of WRI SDR applications can be found in [16]-[18].

Besides the WRI based receivers, a direct quadrature phase shift keying modulator based on WRI technology was recently introduced for a single carrier signal [13]. The modulator is composed of a WRI circuit, a switch matrix and open and short terminations. A conventional QPSK modulator employs heterodyne architecture which requires two intermediate frequency (IF) mixers, in-phase and quadrature-phase carriers,

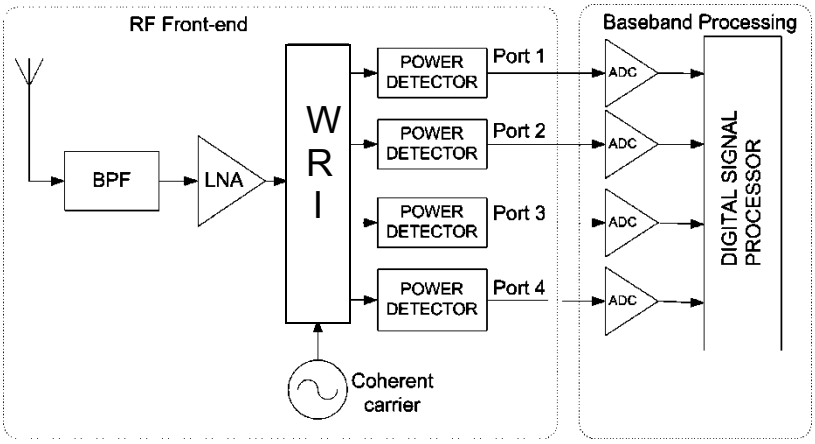

Figure 2-6: WRI Based SDR receiver architecture.

and an RF upconversion section. Compared with a heterodyne modulator, this direct QPSK modulator eliminates the need for IF modulation and RF upconversion, consequently reducing power consumption and circuit complexity. The WRI-based modulator, due to its lack of nonlinear elements, can be scaled dimensionally and operates from RF to millimeter wave frequency ranges, which is not the case with some other direct modulators [26], [27]. Also, extendibility to M-ary phase shift keying (M-PSK) is possible because the architecture allows a variety of terminations to be applied to its ports.

As an alternative to standard frequency modulation continuous wave (FMCW) radar sensor, the WRI-based radar was also investigated in [22]-[23]. Range information and Doppler frequency contained in the vector of complex ratio of the transmitted and received signal can be found using WRI phase/frequency discriminator.

Several fabrication technologies have been used for WRI circuits. The work in [16] demonstrated a WRI module fabricated using monolithic hybrid microwave integrated circuit (MHMIC). The MHMIC WRI module was used as a front-end for QPSK

demodulator operating between 26–28.5 GHz (in Ka band). Moldovan [22] demonstrated a WRI circuit fabricated in metal blocks using machined WR-10 waveguides. The WRI circuit was used at 94GHz (in W band) as the front-end module of collision avoidance radar. Xu [28] implemented a WRI junction operating at 24GHz using substrate integrated waveguide (SIW) structure. SIW structure benefits the design and development of low-cost millimeter-wave integrated circuits by allowing the integration of planar and non-planar structures on the same planar platform [29]. Another example of WRI using integrated circuits operating at wide bandwidth between 0.9GHz to 5GHz is given in [19]. A recent study [30] showed a WRI circuit adopting a composite right/left-handed (CRLH) transmission line for its key components. A direct advantage is that dual bands 3.96GHz and 7.39GHz can be covered by the proposed WRI front-end.

The UWB WRI-based transceiver systems presented in this thesis provides comparative implementation studies of IR and OFDM modulations. Both implementations considers different configurations of transmit and receive antennas. Those implementations will also be tested in realistic fading environment by emulating IEEE802.15.3a channel model presented in the following section.

2.4 IEEE802.15.3a UWB channel model

The IEEE802.15.3a channel model was first introduced based upon the measurements in [31]. The statistical channel model was also provided in the same work. It has been adopted as a channel standard for wireless high speed data communications for UWB applications. One of the proposed physical-layer modulations, MB-OFDM in [32],

implemented this channel model and showed that it can support up to 480Mbps. Due to some limitations in the model such that it is designed for indoor residential and office environment only with a restriction of less than 10m between the transmitter and receiver, another comprehensive channel model was introduced [33]. This channel model, IEEE 802.15.4a has been primarily been considered for low data rate UWB applications (< 1Mbps), such as sensor networks. However, as indicated in [31], it is not restricted to these applications only, and can also be used for high speed UWB applications. The research work in [34] provides a great reference for comparison between these models. In the following, we will present the statistical modeling of the IEEE 802.15.3a standard channel model [35], which is used to generate the channel impulse response employed in the simulations and the test bench.

The channel impulse response can be represented by

$$h_i(t) = X_i \sum_{l=0}^{L} \sum_{k=0}^{K} \alpha_{k,l}^{i} \delta\left(t - T_l^i - \tau_{k,l}^{i}\right) \tag{2.2}$$

where $\alpha_{k,l}^{i}$ is the multipath gain coefficient, with i referring to the impulse response realization, l to the cluster number, and k to the arrival within the cluster. T_l^i represents the delay of the l^{th} cluster for the i^{th} channel realization, while $\tau_{k,l}^{i}$ is the delay of the k^{th} multipath component relative to the l^{th} cluster arrival time for the same channel realization. The large-scale shadowing statistics for the i^{th} channel realization are represented by log-normal distribution, represented by X_i in equation (2.2). After comparing different probability distributions to the measurement data, the small-scale

amplitude statistics were modeled as log-normal distribution rather than Rayleigh distribution, which is used in the original Saleh-Valenzuela model.

The distributions of the cluster and ray arrival times are given by

$$p(T_l / T_{l-1}) = \Lambda e^{-\Lambda(T_l - T_{l-1})}, \qquad l > 0 \tag{2.3}$$

$$p(\tau_{k,l} / \tau_{(k-1),l}) = \lambda e^{-\lambda(\tau_{k,l} - \tau_{(k-1),l})}, \quad k > 0 \tag{2.4}$$

where Λ is the cluster arrival rate, and λ is the ray arrival rate, i.e., the arrival rate of a path within each cluster. The behaviour of the (averaged) power delay profile is [35]

$$\mathrm{E}\left[\left|\alpha_{k,l}^{i}\right|^2\right] = \Omega_0 e^{-\left(\frac{\Gamma_l}{\Gamma}\right)} e^{-\left(\frac{\tau_{k,l}}{\gamma}\right)} \tag{2.5}$$

which reflects the exponential decay of each cluster, as well as the decay of the total cluster power with delay.

In order to use the model, several of the above parameters need to be defined, which helps relate the model to actual measurements. Table II in [32] provides some target parameters for various line-of-sight and non-line-of-sight (NLOS) channels. The parameters of the model were found through an extensive search, which attempted to match the important characteristics of the statistical channel model output to the characteristics of actual measurements. The important channel characteristics include the mean excess delay, the root-mean square (RMS) delay spread, the mean number of paths within 10 dB of the peak, and the mean number of paths, which capture 85% of the channel energy. A channel realization generated for this model is shown in Figure 2-7.

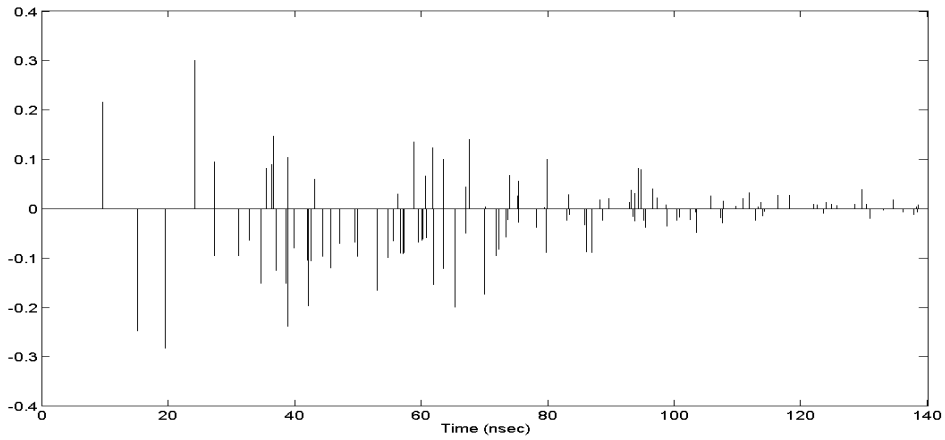

Figure 2-7: An IEEE 802.15.3a channel model realization.

There are four main IEEE MB-OFDM UWB channel models proposed by the IEEE 802.15.3a Task Group, accounting for the four typical multipath scenarios of UWB systems. Namely CM1 with a line-of-sight (LOS) scenario with a distance between the transmitter and receiver reaching up to 4 m; CM2 non-line-of-sight (NLOS), with a separation from 0 to 4m, CM3 non-line-of-sight (NLOS), with a separation from 4 to 10m, and CM4 proposed to fit the channel with a rms delay spread of 25ns representing an extreme NLOS multipath channel. In this thesis and in the following chapters, we consider the CM1 and CM4 for system performance analysis between best vs. worst case scenarios.

Take note that in order to test both UWB transceiver implementations; an emulated channel is used in both simulation and measurement results. Those obtained results are based on simulating IEEE 802.15.3a channel model and not a real-time wireless channel.

2.5 Conclusion

In this chapter an overview of the general requirements and challenges of wireless communication transceiver design were introduced, and new trends in the field were presented. The different UWB standard proposals were presented along with a description of the main characteristics concerning their channel allocation, bandwidth requirements and the definition of UWB technology. Then, the OFDM technique was briefly highlighted upon for its importance and hence practicality for the use in wireless systems. In addition, previous research accomplishments on WRI circuit are summarized with emphasis on different applications of the circuit. Finally, IEEE802.15.3a UWB channel model used in this work to emulate the wireless channel during simulation and lab measurements is presented.

CHAPTER 3 WRI TRANSCEIVER CIRCUIT

3.1 Introduction

The development of the proposed IR-UWB and OFDM-UWB transceivers mandated the design and fabrication of an RF front-end which satisfy low-cost, high-performance and versatility requirements. This chapter presents the design and implementation of a new transceiver based on the WRI circuit topology. This transceiver has the advantage of combining both functions of transmission and reception for an impulse UWB signal over the design frequency range (3.1-4.1 GHz). In order to clarify the concept principle, a brief description of the WRI operation as a single operation circuit, (i.e., a modulator in the transmitter side and a demodulator in the receiver side) will be provided, then the circuit design, challenges and implementation steps carried for the new WRI transceiver will be presented.

3.2 Modulator WRI

A review of traditional implementations of the WRI is presented in [16]. The proposed transceiver in this work adopts the new WRI architecture introduced in [17], whose block diagram is shown in Figure 3-1. It is composed solely of power dividers/combiners (PDC) and phase shifters (PS), whereas earlier architectures required hybrid couplers in addition. A typical test bench utilizing WRI circuit for the transmitter and the receiver is shown in Figure 3-2. The transmitter in the test bench shown in Figure 3-2 consists of a wave-radio circuit, a switching matrix and open/short circuit terminations. The modulator WRI shown operates as follows. Port 1 is fed with a

monocycle pulse signal which is routed to ports 3, 4, 5, and 6 through the different branches of the wave-radio circuit. The switch matrix is controlled by DSP techniques, which present either a short circuit (S) or an open circuit (O) termination at ports 3 to 6 according to the modulation criteria given in Table 3.1, where ΔΦ represents the phase difference between ports 1 and 2. Port 2 subsequently outputs the digitally modulated signal which acquires different phase states depending on the terminations applied at ports 3 to 6.

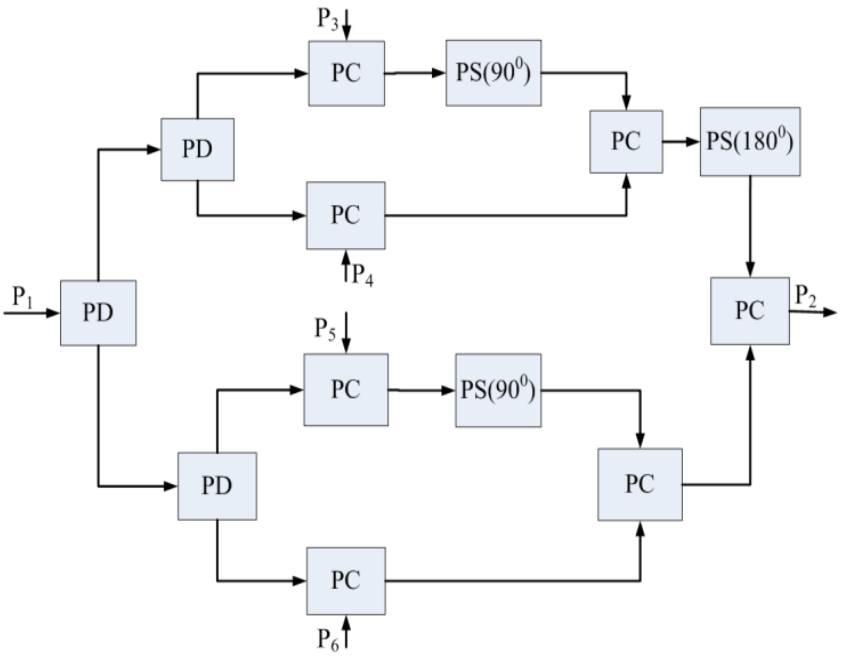

Figure 3-1: WRI architecture using power combiners/dividers (PDC) and phase shifters (PS).

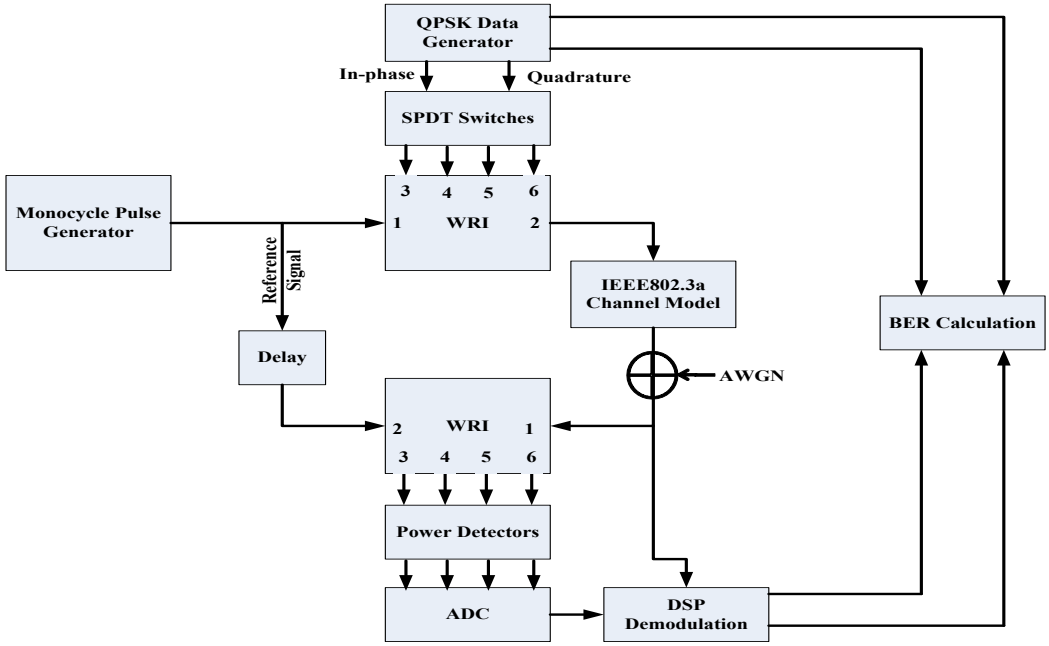

Figure 3-2: Typical test bench employing separate WRI circuits for the modulation and demodulation functions.

Table 3.1: Open and short circuit terminations criteria for the four QPSK modulation states.

Modulation State	Port Number				$\Delta\,\Phi$	I	Q
	3	4	5	6			
1	O	O	O	S	0^0	0	0
2	O	O	S	O	90^0	0	1
3	O	S	O	O	180^0	1	1
4	S	O	O	O	270^0	1	0

3.3 Demodulator WRI

The receiver in the test bench shown in Figure 3-2 is composed of the same wave-radio circuit structure, with the exception that inputs and outputs are acquired from

different ports as shown in Figure 3-3. Ports 1 and 2 are fed with the modulated and reference signals, respectively. Ports 3 to 6 simultaneously provide four signals to the power detectors. The output signals from power detectors are then sampled and digitally processed at baseband for demodulation.

The determination of the received symbol is obtained by determining the minimum power available at ports 3 to 6. Then with the aid of proper digital signal processing algorithms, demapping of the transmitted symbol can be achieved efficiently.

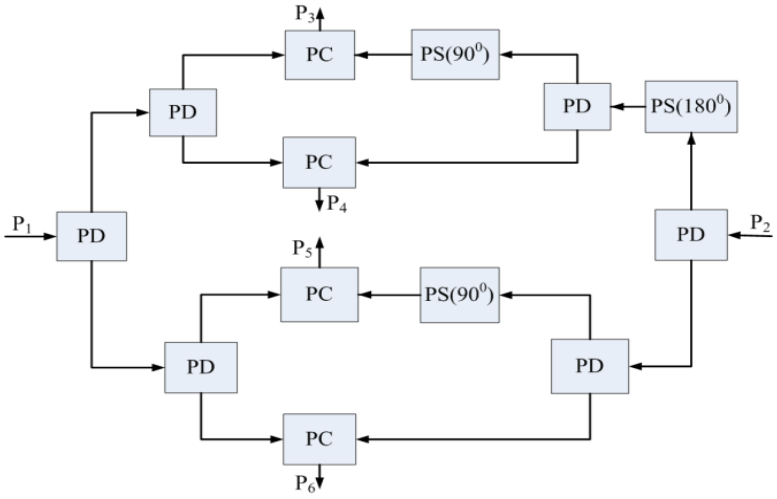

Figure 3-3: WRI with the same architecture used as a modulator (note the arrow directions compared to Figure 3-1).

3.4 Simulation of WRI

As shown in [36], the transfer function between port 1 and port 2 of the WRI circuit can be derived and expressed as follows:

$$H = 0.707 \times e^{-j(4\varphi + 2\theta + i.90^0)}, \quad i = 0, 1, 2, 3 \tag{3.1}$$

where φ is the phase change of the power divider/combiner branch, θ is the phase change of the transmission line, i represents the i^{th} configuration of four different

termination configurations. For a single carrier at frequency f_c, phase values are constant. The value of $(4\varphi + 2\theta)$ is the unwanted total phase change of the components and the transmission lines. It can be designed to be discrete multiple of 360º in order to eliminate the phase variation of the modulated signal.

An ideal WRI circuit simulation model was first developed in the environment of Matlab-Simulink [37]-[39]. According to the S-parameters of the components used in the WRI circuit, the mathematical relationships between two inputs and four outputs of the WRI circuit are depicted using the Simulink model editor. The model simulating an ideal WRI circuit is shown in Figure 3-4.

Using the complex numbers for the above model is straightforward because an S-parameter at a frequency point is a vector including both amplitude and phase. The model eliminates the frequency variable. Thus it is a frequency-independent model. This infers that the phasor representation of a signal must be used to implement a system simulation based on this model. For an M-ary phase shift keying signal, its phasor representation can be written using Euler's theorem as follows [40]:

$$s(t) = \mathrm{Re}\left\{\sqrt{\frac{2E}{T}}\right\} e^{j\omega_0 t} e^{j\emptyset_i t}, \quad 0 \leq t \leq \mathrm{T},$$

$$i = 1, \ldots, M \qquad (3.\text{Error! Bookmark not defined.})$$

where the phase term, $\phi_i(t)$, will have M discrete values, typically given by:

$$\emptyset_i(t) = \frac{2\pi}{M}, \quad i = 1, \ldots, M \qquad (3.2)$$

The parameter E represents the symbol energy, T the time duration and ω_0 the carrier frequency. When the modulated signal and the carrier signal (reference signal) in such a

complex notation are fed into the WRI circuit model, the constantly rotating aspect of the unmodulated carrier will be removed. Only information-bearing phasor will be calculated by this model. The Simulink model, given in Figure 3-4, is thus useful for analyzing WRI circuit-based transceiver at the systems level. Similarly, signal processing algorithms for WRI circuit-based system can be easily tested in Simulink using the WRI circuit model given in Figure 3-4.

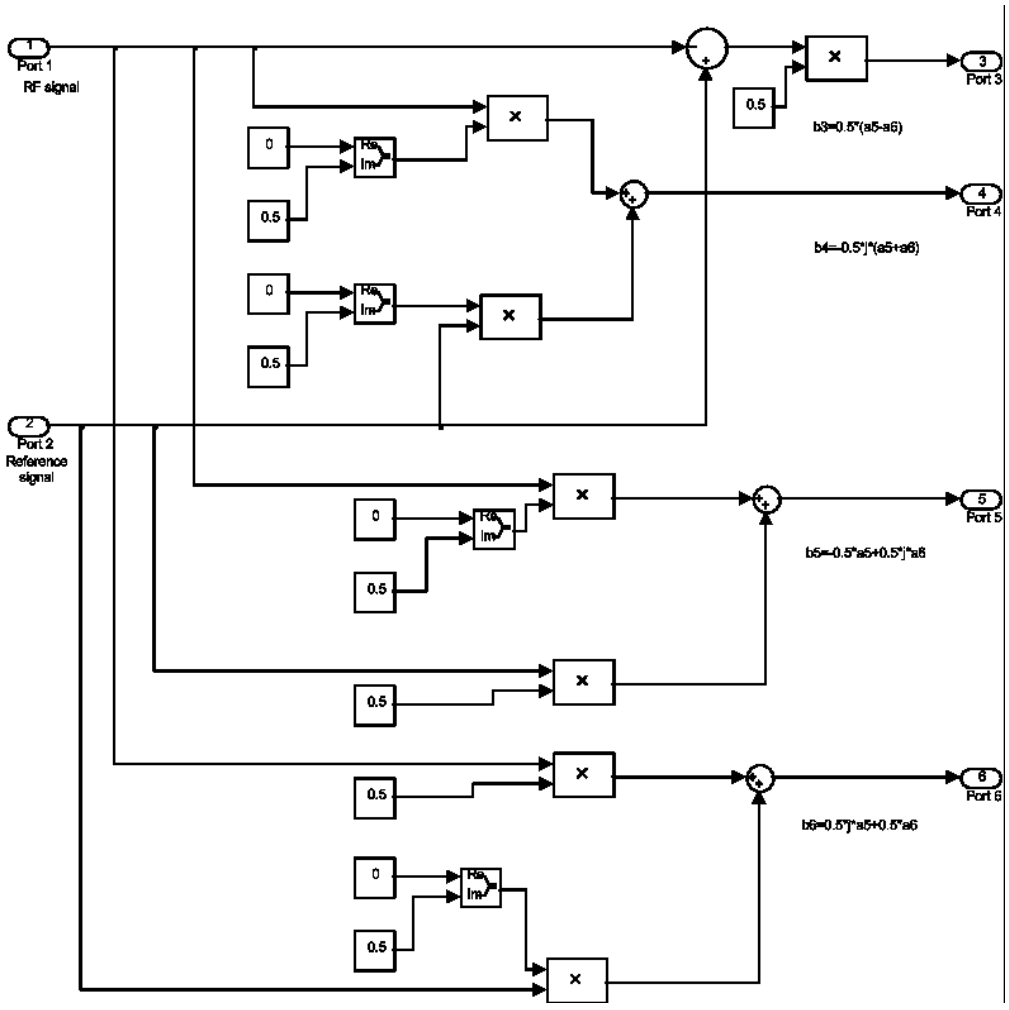

Figure 3-4: WRI circuit model in Simulink.

Then, an equivalent ideal WRI circuit is simulated within Advanced Design System (ADS) software. In the simulation, a WRI circuit model was implemented based on the structure shown in Figure 3-1. The schematic of the modulator simulation is shown in Figure 3-5. The power divider/combiner was simulated using ideal S-parameters. Under different termination configurations, the output waveforms of the various QPSK modulation states were obtained and are shown in Figure 3-6. They agree with the results derived from (3.1).

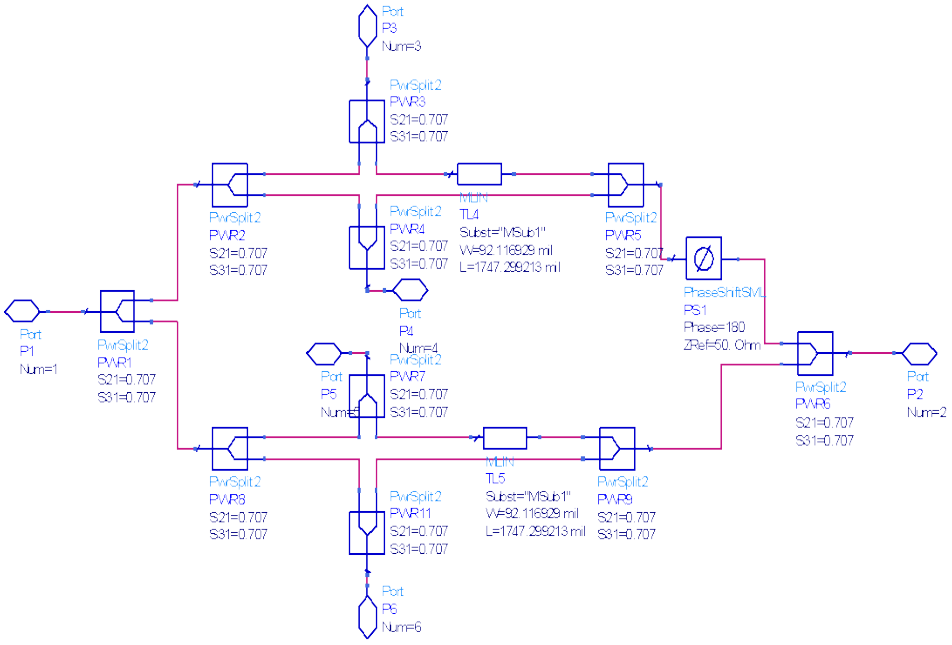

Figure 3-5: Schematic of WRI circuit in ADS.

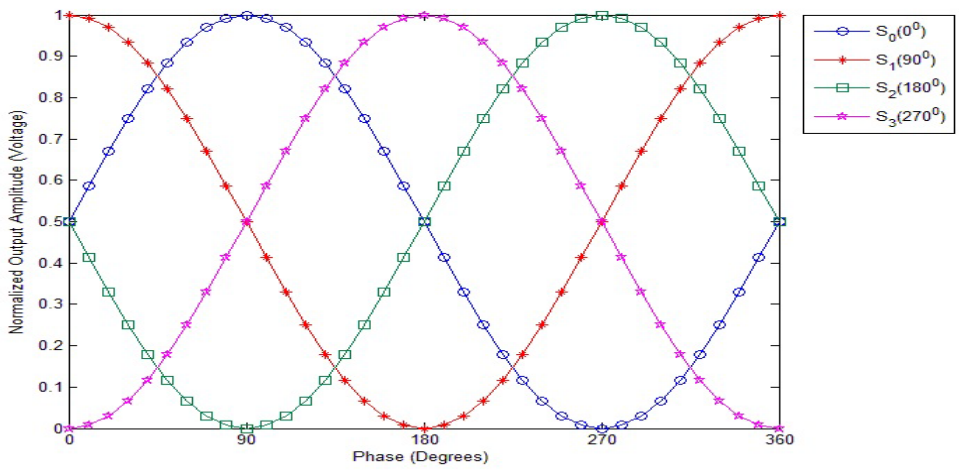

Figure 3-6: WRI normalized output voltages vs. phase difference between the input and reference signals at any frequency within the operating channel.

A more realistic simulation was performed using the measured S-parameters of the fabricated WRI in order to study the effect of phase and amplitude imbalances. The simulated WRI used in the test bench set up has a maximum amplitude imbalance of ±0.3 dB and phase imbalance of ±3 degrees.

An I-Q impairment analysis is done by sweeping the amplitude imbalance between -0.3 dB to 0.3 dB and the phase imbalance between -3º to 3º. The simulation results show that the phase difference ranges from -11.3º to 11.4º and the amplitude difference ranges from 0.3dB to 2.3dB. The impaired I-Q constellation points are presented in Figure 3-7 and compared with the ideal points.

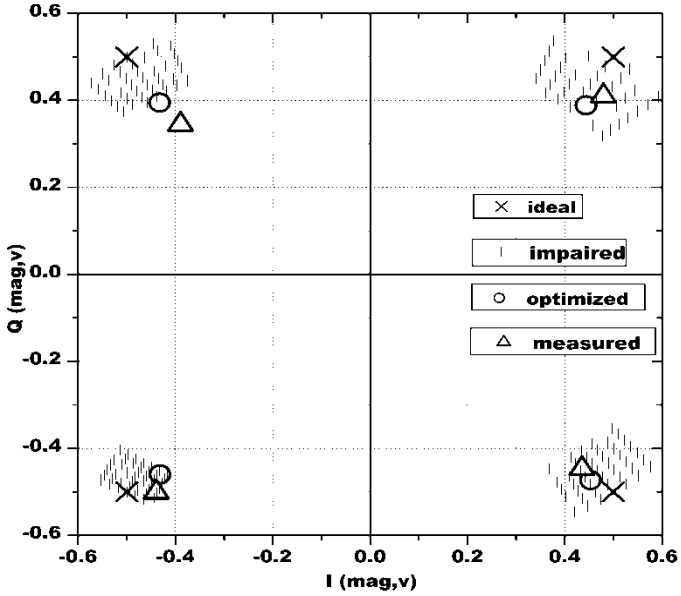

Figure 3-7: Comparison of I-Q constellations obtained by varying phase and amplitude.

An error vector analysis is further done to quantify WRI circuit performance in terms of magnitude and phase errors. The figure of merit, Error-Vector-Magnitude (EVM), is the unsigned scalar distance between the end points of reference phasor and actual or measured phasor [41]. EVM is defined in (3.4) as a percentage of the peak signal level, usually defined by the constellation's corner stage (Figure 3-8).

$$Error\ vector\ magnitude = \frac{average\ error\ magnitude}{peak\ signal\ magnitude} \times 100\% \qquad (3.3)$$

The fabricated WRI used in the test bench has a typical amplitude imbalance of ±0.50dB and phase imbalance of ±9º. The error vector magnitude (EVM) analysis is done by sweeping the amplitude imbalance between -0.5 dB to 0.5 dB and the phase imbalance between -9º to 9º. The combined effect of amplitude and phase imbalance is simulated and presented in Figure 3-9. The results show that at 3.6 GHz there is less than a 2º phase difference from the ideal case. The EVM is as low as 14.5% which indicates that this modulator can achieve acceptable phase modulation accuracy. Note that the contribution to EVM by the phase and amplitude imbalance can be reduced by optimal design method described in the following text.

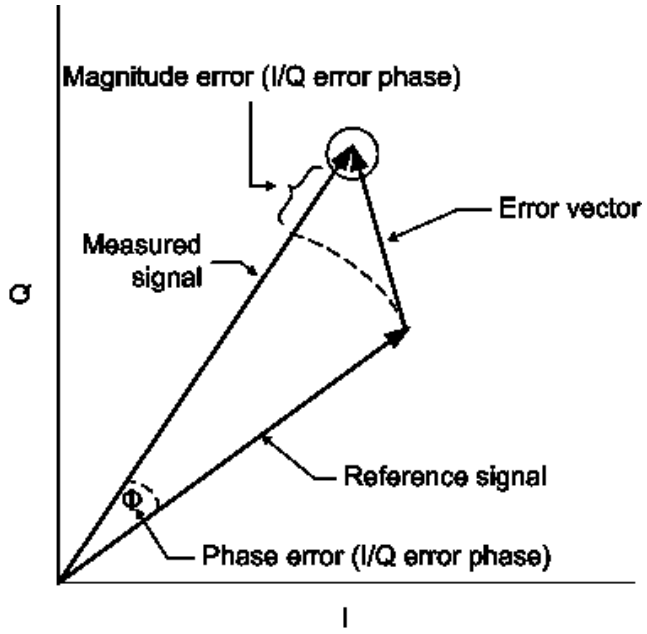

Figure 3-8: Error Vector Magnitude.

When the WRI circuit is fabricated, its modulation performance can be analyzed using error vector analysis. With both magnitude and phase values associated, EVM is effective for analyzing or troubleshooting the effect of phase and amplitude imbalance existing in a WRI modulator.

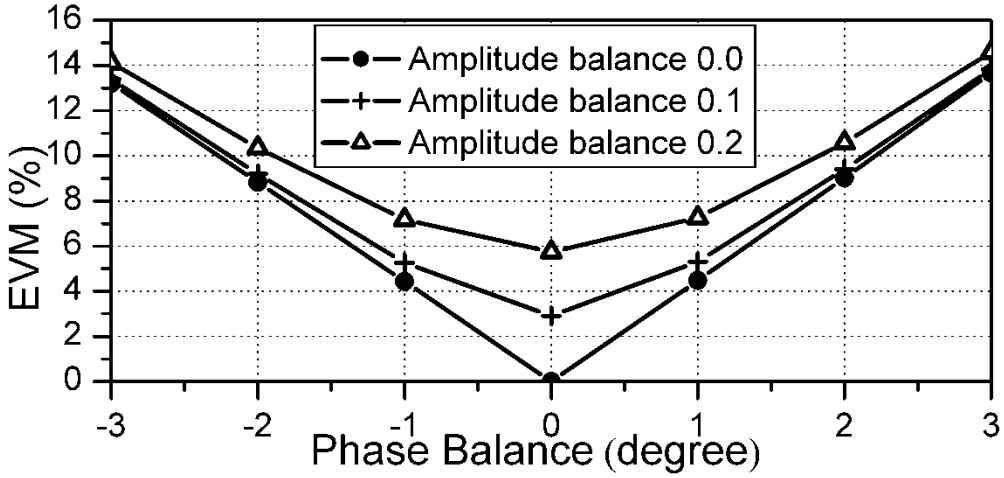

Figure 3-9: Combined effect of amplitude and phase imbalance.

To overcome the I-Q impairment, an optimization process was designed according to (3.1). Lengths of transmission line connecting cables are specified as parameters to be optimized under the goal of minimizing both the phase and amplitude errors. During the optimization process two different search methods, gradient and random, were used for better accuracy. The WRI circuit design was modified using the optimal lengths and simulated again. The optimized I-Q constellation is compared with ideal and impaired points in Figure 3-7. Note that the contribution to the I-Q impairment by the phase and amplitude imbalance can also be reduced by calibration algorithms used in receiver processing [42].

In order to verify the amplitude and phase balance of the optimized WRI circuit, S-

parameter measurements were carried out between port 1 and 2 of the circuit. Different combinations of open and short circuit terminations were applied to ports 3 to 6 manually. The output signal constellation, derived from measuring S_{21} data, is compared with simulated and ideal points in Figure 3-7. A phase difference from 0.8º to 4.5º and

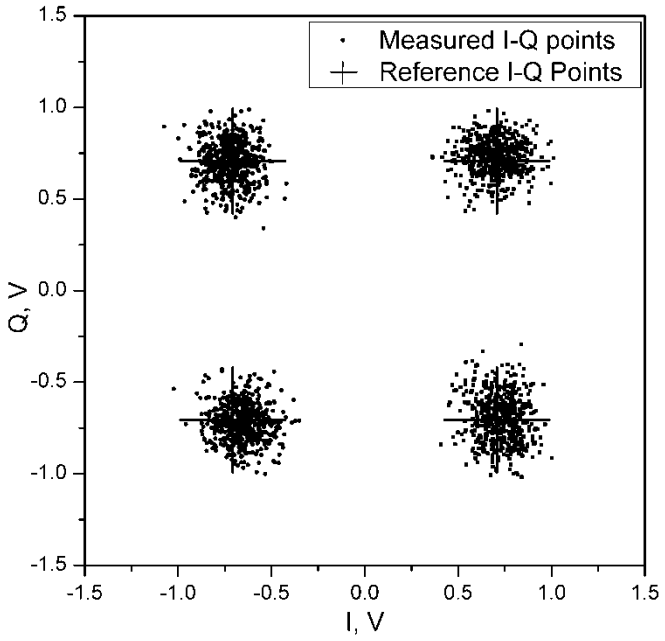

Figure 3-10: Measured constellation of output modulated signal.

an amplitude difference from 0.5 dB to 2.7 dB were achieved, which shows close correlation with the previous optimized result.

The WRI circuit was further measured with commercial microwave switches and a digital data generator. The data generator provides two rectangular pseudo random sequences. One sequence is for in-phase (I) channel and the other is for quadrature (Q) channel. These modulating sequences were used to switch opens and shorts onto ports 3-6. Each sequence is at a symbol rate of 10 Msps. Thus a data rate of 20 Mbps was

achieved using this modulator. It is noted that the data rate was selected in accordance with the available equipment. Normalized constellation of the modulated signal was measured and shown in Figure 3-10. During this measurement campaign, the carrier signal had a frequency of 3.6 GHz and 12 dB signal-to-noise (SNR) ratio.

3.5 Transceiver WRI

In previous works, the WRI was employed as one of two variants. At the transmitter side, it was used only as a modulator, while at the receiver side it was used only as a demodulator. In order to cope with the requirements of current and future wireless technologies employed either for localization or communication purposes, we initiate here the idea of not only integrating on the same board but also *merging* within the same WRI the transmitter and receiver operations.

Based on the operation requirements of the wave-radio interferometer as a modulator/demodulator in the transmitter/receiver, the design of the WRI transceiver can be obtained as follows.

First, in order to operate as a modulator while in the transmission mode, we must apply to ports 3 to 6 short circuit (S) or open circuit (O) terminations according to the criteria defined in Table 2.1. Secondly, in the receiver mode, and to operate as a demodulator, a power detector is required also at ports 3 to 6. These two configurations may be accommodated by the use of a single-pole triple-throw (SP3T) switch at each of these ports. However, due to some practical aspects, such as switching speed, isolation between the switched ports and required Transistor-Transistor Logic (TTL) switching control voltages, the choice settled on using a single-pole quad-throw (SP4T) switch

(Hittite's SP4T HMC345LP3E). The resulting switching circuit, which is replicated at each of the ports P3 to P6 of the WRI circuit, is shown in Figure 3-11. Its four switching ports are labeled RF1 to RF4. RF1 is an internal port terminated by a 50 Ω resistor to avoid undesired reflections. RF2 is the receiver port, which is connected to a demodulating detector.

RF3 and RF4 are the transmitter ports, which are respectively connected to a short and open circuits provided by open-ended transmission lines, where the short circuit is achieved by an extra quarter-wavelength section.

Previous implementations of the WRI demodulator used Schottky diodes for power detection. While these diodes are well known for their fast switching speeds and low forward voltage dropping, yet they suffer from low dynamic range capabilities. We have therefore selected a logarithmic-detector (Analog Devices AD8317), which is capable of accurately converting an RF input signal amplitude (i.e. power) to a corresponding decibel-scaled output voltage. This detector can be seen in Figure 3-11 at RF2 of the SP4T switch.

The implementation of the WRI transceiver required the design and fabrication of two substrate layers, one for RF and another one for DC. The layout of the RF layer, which is essentially constituted of the wave-radio circuit with the SP4T switch circuit shown in Figure 3-11 at ports 3 to 6, is shown in Figure 3-12. This layer was designed considering a central carrier frequency of 3.6 GHz. As mentioned earlier, to provide more design flexibility by controlling these switches using the FPGA board, Hittite's SP4T switch has been used since its controls (CTLA and CTLB in Figure 3-11) operates

using 0/+5 voltages. Also, this switch provides high isolation and low insertion loss at its RF ports. Both (RF and DC) layouts have been fabricated on Rogers RT/Duroid 5870 with relative permittivity (ε_r = 2.33), thickness of 31mils and a loss tangent of 0.0012. This substrate was chosen to allow large separation between transmission lines on the RF layer to avoid any cross coupling effects.

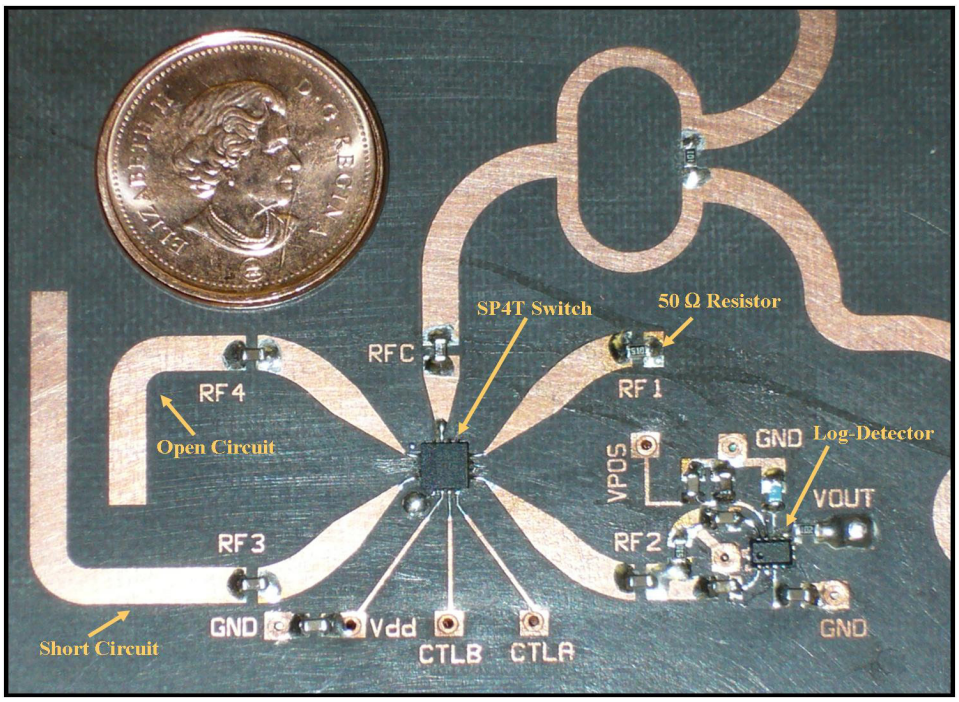

Figure 3-11: The core of the WRI transceiver.

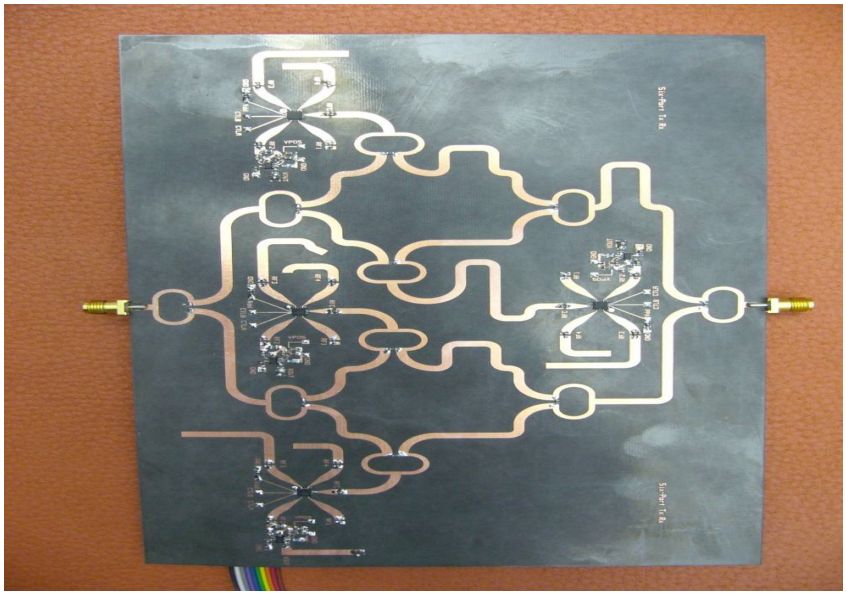

Figure 3-12: Fabricated RF layer of the WRI transciever.

In order to test the dynamic range capability of the log-detector in the lab, an experimental testing was conducted were the input signal power was varied and the corresponding output signal value is measured. The AD8317 log-detector tested in the lab provided a dynamic range extending from -55 dBm to +5 dBm, corresponding approximately to the double of the dynamic range offered by a Schottky power detector. These two surface-mount chips have been also used for their wideband characteristics, which is mandatory for UWB based applications. The layout of the DC layer, which is connected to the RF layout using vias, is given in Figure 3-13. This layer provides the interface to the FPGA board for control purposes. Further details about the design, fabrication and testing of the WRI transceiver can be found in [43].

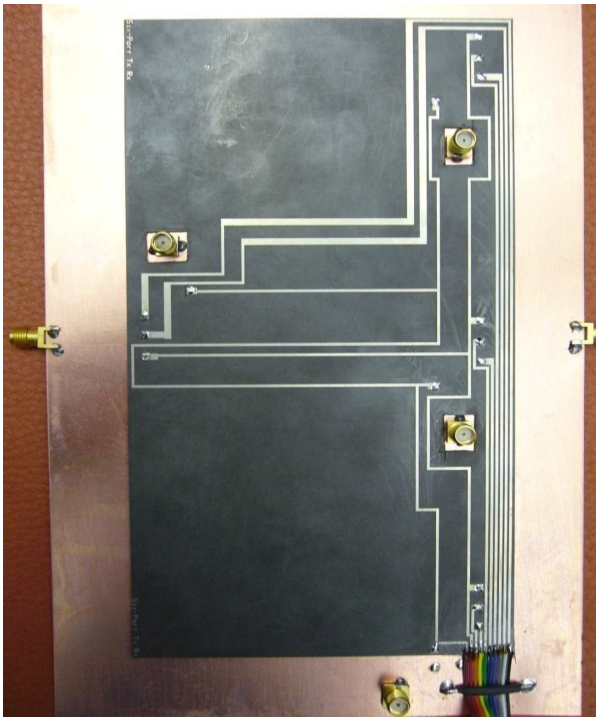

Figure 3-13: Fabricated DC layer of the WRI transceiver.

3.6 Design and fabrication challenges

The initial stage of the design of the RF layer was based upon the optimization of the Wilkinson power divider/combiner design. The first implementation of the Wilkinson power divider/combiner suffered from cross coupling between the two λ/4 sections of the Wilkinson PD/PC and the following branches of transmission lines. Hence, by redesigning and testing a new layout of the Wilkinson, after adding extra spacing between the λ/4 sections and the following transmission lines, the cross-coupling problem was eliminated. The final design for the optimized Wilkinson is shown in Figure 3-14.

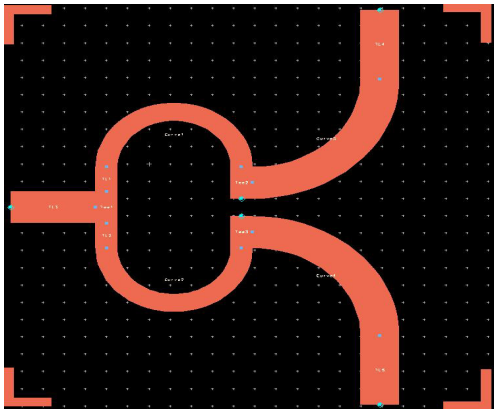

Figure 3-14: Optimized design for the Wilkinson PD/PC.

The second encountered challenge was the proper length choice of the extension transmission lines connecting ports 3, 4, 5 and 6 to their corresponding SP4T switches. Since the basic operation of providing a certain phase shift for the output pulse rely basically on the vector addition/subtraction of the signals reflected from these ports, these lengths have been carefully chosen in order to provide the same phase drift between the common port of the Wilkinson PD/PC and port RFC of the SP4T switch in Figure 3-11.

The third challenge was finding the best compromise between reducing the size of the RF layout of the designed prototype, and choosing the proper distance between the 90^{o}, 180^{o} phase shift extra length transmission lines and the surrounding components on the layout in order to avoid any cross coupling that might occur.

The fourth challenge was properly designing and aligning both the RF and DC layers, and choosing the proper locations for the VIAs that connect both layers so that puncturing wouldn't cause any malfunction in the required operation of any layer.

Figure 3-15 shows a capture of the final design for both layers in Advanced Design System (ADS).

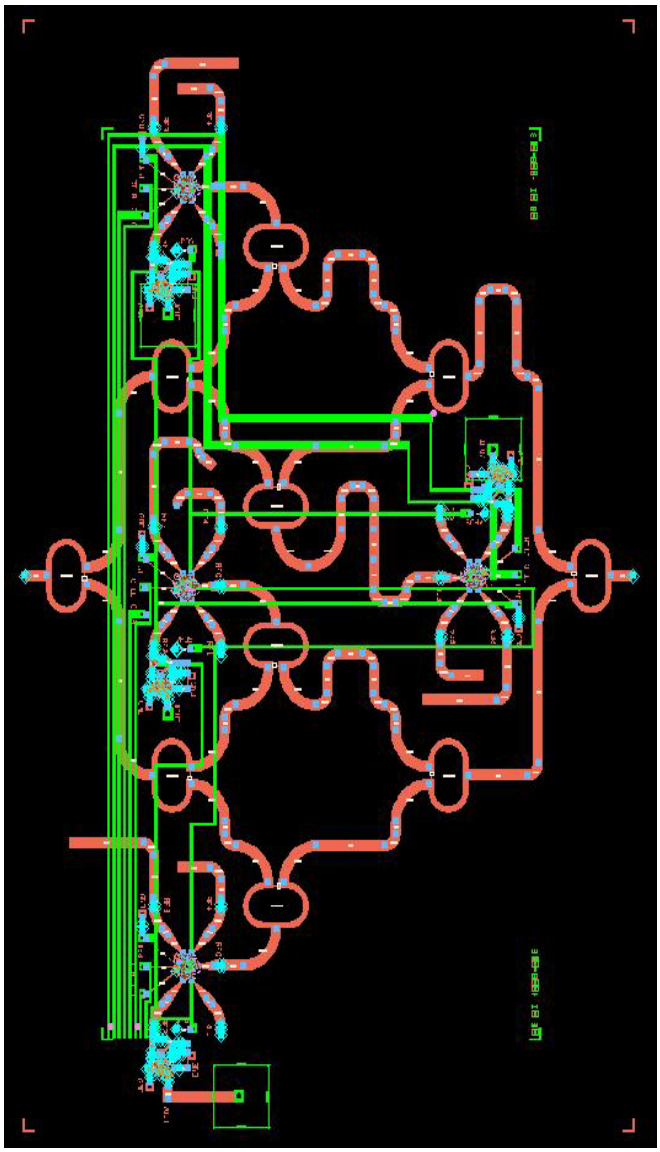

Figure 3-15: A picture showing both layers RF and DC of the WRI transceiver.

3.7 WRI Transceiver Design Features

Compared to the previous design of the Wave-Radio Interferometer as a direct QPSK digital modulator/demodulator in [44], the newly designed WRI transceiver has the following advantages

1. The new design for the WRI transceiver combines both functions of the modulator and demodulator in the same prototype. This in consequence translates into smaller size and lower cost prototype.

2. The new design of the WRI transceiver is based upon the design and fabrication of both RF and DC layers in the lab, while the one in [40] relies totally on ready system components.

3. As a demodulator, the design in [40] utilized Schottky diodes as power detectors. However, the newly designed WRI transceiver employs log-detectors for this purpose. As mentioned earlier, these detectors are well recognized for their wide dynamic range which is almost double the one provided by Schottky diodes. This is mandatory; especially for systems destined to work in UWB standards were signal emissions have very low power levels.

4. Isolation between the transmitter and receiver is inherent by the isolation capabilities of the SP4T switch. This is due to the fact that both functionalities are obtained using the same circuit structure. Therefore, the expected isolation between the transmitter and receiver in this scenario can be measured by the achieved isolation between the switch common port and its output ports. As shown in Figure 3-16, a minimal isolation value of 27dB is measured along the

design frequency range. During measurements, similar values were obtained between all ports of the SP4T switch.

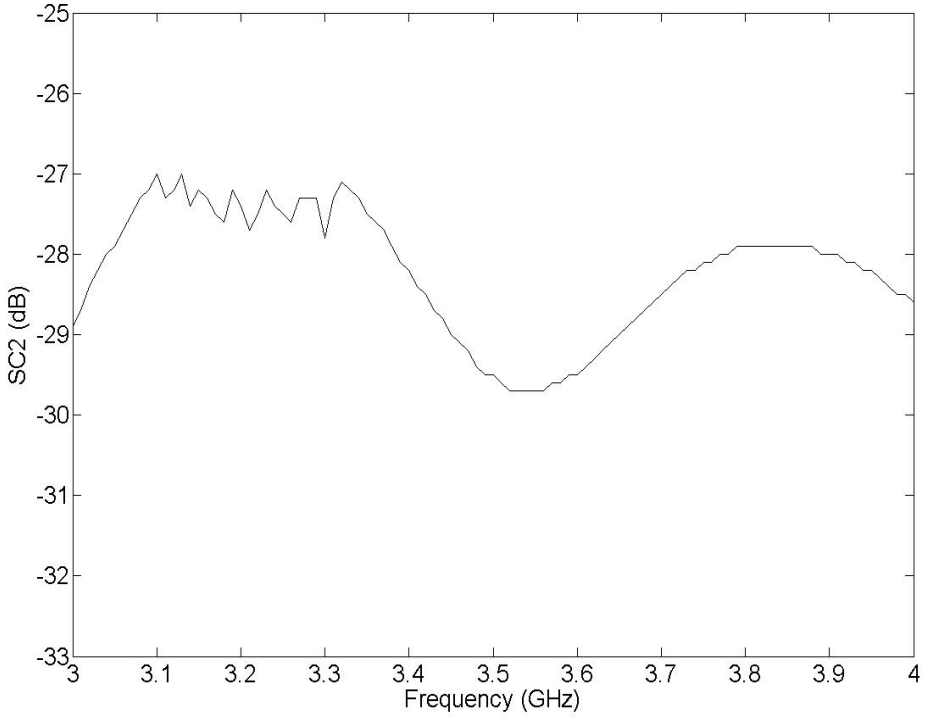

Figure 3-16: Measured isolation result between the common port of the SP4T switch and output port 2.

Since that the whole process of designing and fabricating the WRI transceiver was performed in the lab, redesigning a compact version of the transceiver can be achieved by changing the fabrication technology, such as MHMIC or MMIC fabrication technologies.

3.8 S-Parameters Test Bench

One vital factor that affects the BER performance of the intended transceivers is the amplitude and phase imbalance of the designed WRI circuit. Therefore, a S-parameters study was conducted to verify the amplitude and phase response of the fabricated circuit.

The test setup used for the WRI transceiver is shown in Figure 3-16. An EP1S80B956C6 Altera FPGA board controls the SP4T switches based on the input in-phase (I) and quadrature (Q) components of the original data stream. Corresponding to the criteria defined in Table 3.1, a very high speed integrated circuit hardware description language (VHDL) program configures the FGPA board, changing the switch positions between RF ports 3 or 4 on each of the WRI ports 3 to 6 according to the desired modulation state at the output. The Agilent 33250A Waveform Generator is used as a 20 MHz clock generator for the FPGA board. The S-parameters of the WRI transceiver are measured by the Anritsu 37369D Vector Network Analyzer (VNA).

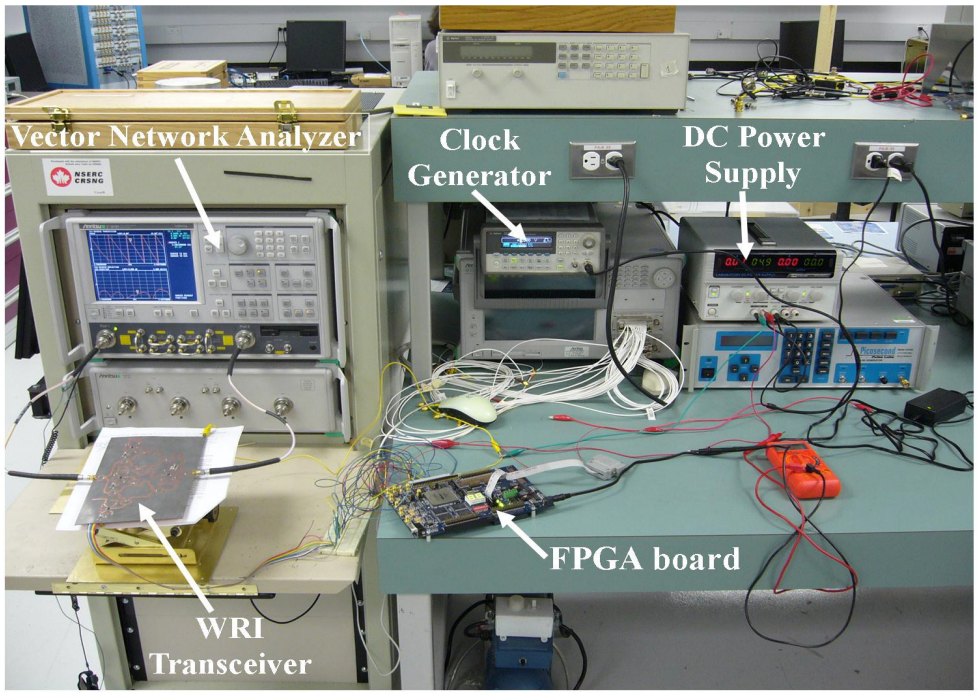

Figure 3-17: WRI transceiver S-parameters test setup.

Using the pre-described test setup, the following S-parameter results for the WRI transceiver were obtained. Figure 3-18 shows the input reflection coefficient (S_{11}) for the transceiver. Along the entire bandwidth of 3.1 to 4.1 GHz, the transceiver maintains an S_{11} below -15 dB. Moreover, the minimum return loss is obtained approximately at the design frequency (3.6 GHz). The forward transmission coefficient (S_{21}) for the WRI transceiver is shown in Figure 3-19. In this figure we can see clearly S_{21} confined within the range of -4 to -9 dB throughout the 3 to 4 GHz bandwidth spectrum. This loss is incurred as a result of the use of the Wilkinson power divider, in addition to the loss caused by the SP4T switches at ports 3 to 6 of the transceiver. As shown in [40], a

power amplifier with reasonable gain can be easily cascaded into the system to compensate that loss and provide the desired gain at the output. For example, Centellax high power amplifier (UA1L30VM) can be used which has a typical gain of 30 dB along approximately 30 GHz of bandwidth (0.01-30 GHz). In general, close agreement between simulation and measured results can be observed in these two figures. The small deviation between simulation and measurement may be due errors in the VNA calibration.

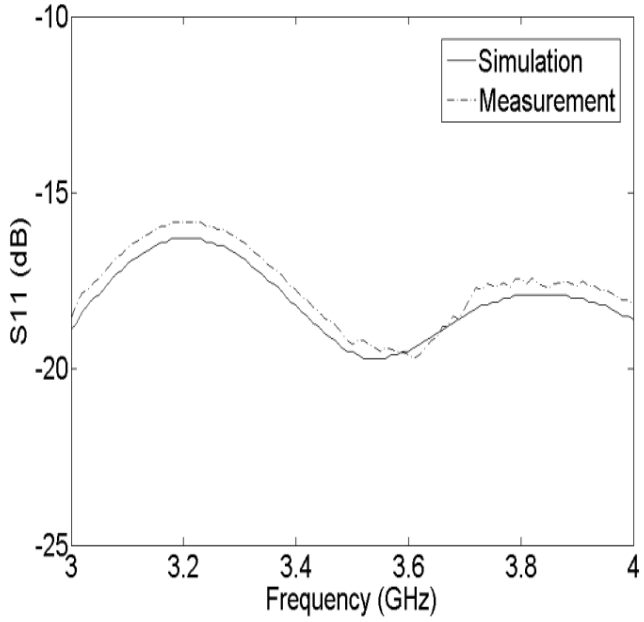

Figure 3-18: Simulated vs. measured S_{11} of the WRI transceiver.

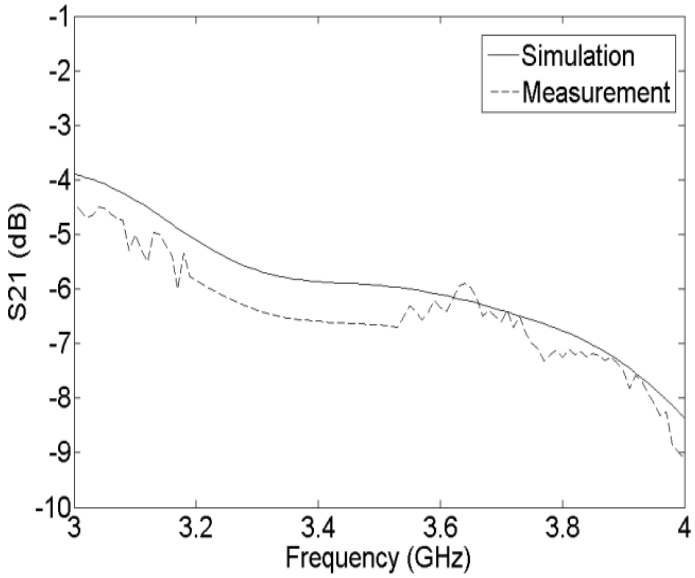

Figure 3-19: Simulated vs. measured S_{21} of the WRI transceiver.

Figure 3-20 and Figure 3-21 show the phase response for the forward transmission coefficient (S_{21}) of the WRI transceiver. In Figure 3-20, it is observed that for the modulation states 1 and 3, at the design frequency of 3.6 GHz, the expected phase shifts of 0^o, and 180^o, respectively, can be obtained. Moreover, Figure 3-21 shows that at the same frequency, the expected phase shifts of 90^o and 270^o are obtained for the modulation states 2 and 4, respectively. These two figures also exhibit close agreement between measured and simulation results, with a small discrepancy not exceeding 9^o. The phase difference between the simulation and measurement curves can be returned to the inaccuracies during the layout fabrication process. This small phase drift is not expected to affect the detector decision except for small signal-to-noise ratios (SNRs) when the location of the received symbols is very close to the decision regions

boundaries. At that time only, this small phase shift may cause a phase rotation, and hence will lead to an error decision. This phase error can be estimated, and then corrected using a PLL circuit or other phase noise cancellation techniques.

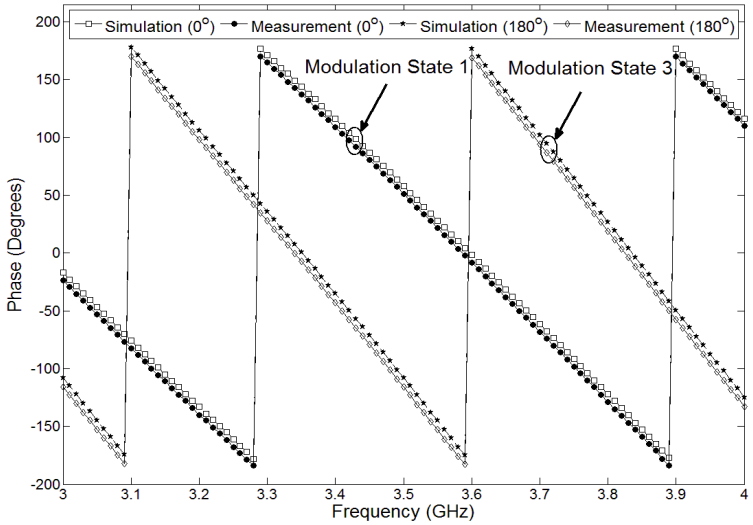

Figure 3-20: Simulated vs. measured S_{21} phase response for the WRI transceiver for modulation states 1 and 3.

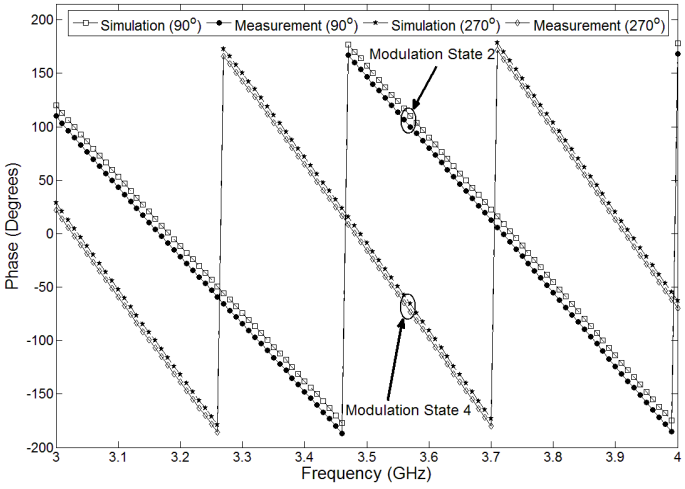

Figure 3-21: Simulated vs. measure S_{21} phase response for the WRI transceiver for modulation states 2 and 4.

3.9 Conclusion

In this chapter, the operational concept of utilizing WRI circuit as a modulator and demodulator was discussed. Also, a newly designed and fabricated dual-layer WRI transceiver circuit has been introduced. Then, design steps, fabrication challenges and features were presented. In order to enhance circuit characteristics, an optimization process was adopted. Following this optimization process, a test bench to verify the S-parameters of the fabricated circuit was developed. The obtained results demonstrate that the fabricated circuit has an acceptable return loss and linear phase response along the design frequency range of 3.1 - 4.1 GHz. This fabricated circuit constitutes the main component that will be used to build up both standard UWB transceiver nodes as will be discussed in the next two chapters.

CHAPTER 4 IR-UWB TRANCEIVER

4.1 Introduction

One of the main two proposals of UWB technology is carrierless-UWB or IR-UWB. It relies on the use of extremely short duration pulses (nanoseconds) instead of continus waves to transmit the information. This pulse directly generates a very wide instantaneous bandwidth signal with a very low duty cycle. Since this UWB approach covers a wide spectrum of applications, it has been under great interest of development from researchers [43, 44].

Building upon aforementioned advantages of WRI circuit, in this chapter, using the fabricated WRI circuit in Chapter 3, we present the IR-UWB transceiver development steps including signal generation, test-bed implementation procedure and obtained simulation and measurement results.

4.2 Methods of generating UWB waveforms

One way of generating UWB signals is to use very sharp signal transitions in time followed by a band-pass filter (Figure 4-1) [45]. Sharp signals can be a step function or narrow rectangular pulse. Sharp signal transitions and extremely narrow pulses act like extremely wideband energy sources, which are then shaped by the desired band-pass filter. This method is a simple and effective method of generating UWB signals. It is

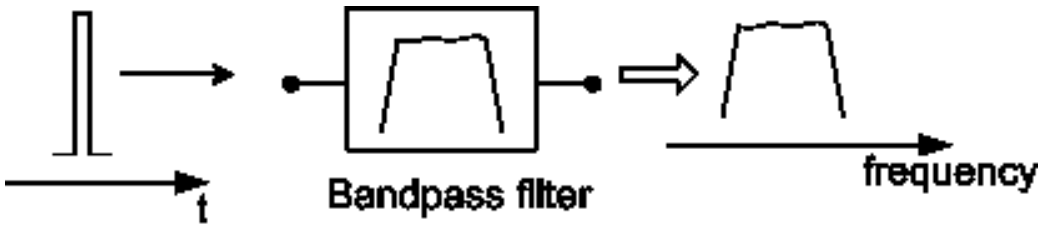

Figure 4-1: A method of UWB pulse generation.

appropriate for certain kinds of UWB systems. However, the method lacks the finesse to precisely shape and position UWB signal energy in the frequency spectrum.

UWB signals can also be generated using precision signal design method. Figure 4-2 shows an example of this method. In this approach, we can synthesize UWB signals with precision in both the signal shape and its placement in the frequency spectrum. To that end, signals can be shaped at base band and then shifted in frequency to the desired location in the spectrum using heterodyning technique. Band shaping is much easier to accomplish at base band than at higher radio frequencies.

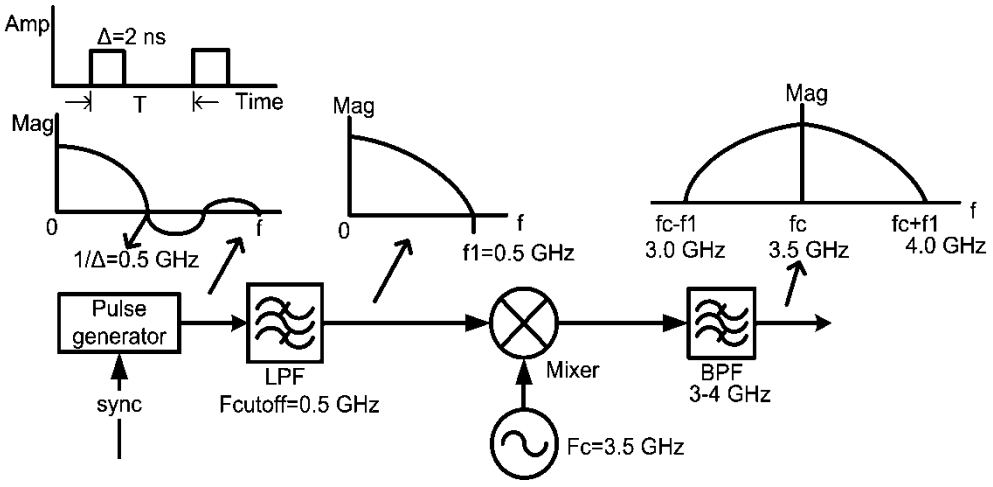

Figure 4-2: UWB pulse precision generation method.

Another approach to generate UWB signals is Fourier Series-Based pulses generation [46]. In this approach, an UWB signal is generated in the frequency domain by summing harmonics of the desired signal instead of generating the signal by a single high-power in the time domain. The Fourier series is normally used to decompose periodic signals into sinusoids as described in (4.1).

$$x(t) \approx \sum_{n=1}^{N} \left[a_n \cdot \cos(n\omega_0 t) + b_n \cdot \sin(n\omega_0 t) \right] \approx \sum_{n=1}^{N} c_n \cdot \cos(n\omega_0 t - \phi_n) \qquad (4.1)$$

where ω_0 is the fundamental angular frequency related with signal repetition interval T as $\omega_0 = 2\pi / T$. The Fourier series in (4.1) can be used in reverse to synthesize a periodic signal. Thus, generating a periodic pulse train can be done by finding the Fourier series expansion of the pulse train to be produced and then generating and transmitting each sinusoidal component of the expansion. A separate oscillator produces each harmonic component of Fourier series expansion and the sum of all the oscillators will reproduce the desired periodic pulses. Only finite terms of Fourier series can be used because of finite number of oscillators. The DC component should not be included in the waveform generation because an antenna cannot transmit the DC component. With these constraints, we can synthesize a desired pulse train from the truncated Fourier series expansion approximately.

For other UWB proposals, such as multi-band orthogonal frequency-division multiplexing (MB-OFDM), instead of using impulse principle, the MB-OFDM UWB signals consists of the parallel transmission of several signals that are modulated at different carrier frequencies occupying the correct spectrum allocation.

4.3 Pulse generation in the test bench

In the experiment of the proposed platform, the precision signal design method was adopted to generate the impulse UWB signal. The pulse signal in the chosen channel (3–4 GHz) is generated using a rectangular pulse generator, a low pass filter, an upconverter, and a band pass filter shown in Figure 4-2. The pulse generator generates a

rectangular pulse train at a repetition frequency of 25 MHz. The width of each pulse is 2 ns. The generated pulse train and its spectrum are shown in Figure 4-3 and Figure 4-4, respectively. A low pass filter with 500 MHz cut-off frequency is used to filter out frequency points beyond 500 MHz of the rectangular pulse spectrum. The upconverter operates at a center frequency of 3.5 GHz and it converts the portion of the rectangular pulse signal spectrum to a signal spectrum occupying 1-GHz bandwidth between 3–4 GHz. Figure 4-5 shows the spectrum of the generated UWB signal.

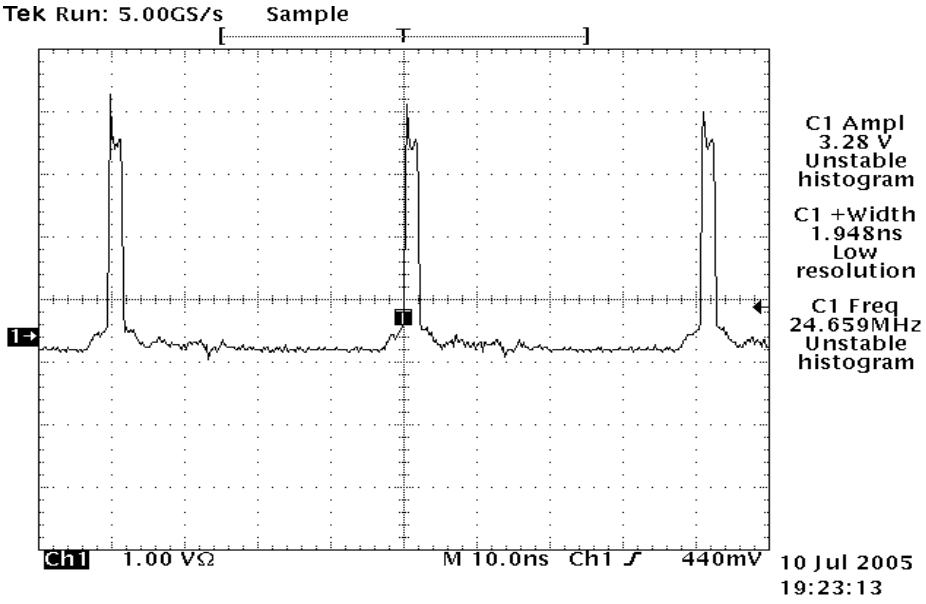

Figure 4-3: Generated pulse train in the time domain [22].

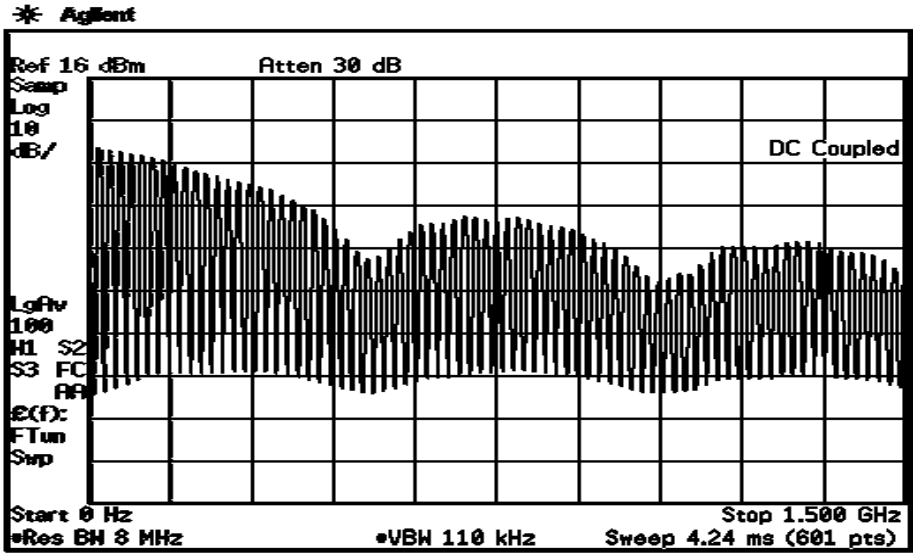

Figure 4-4: Generated pulse spectrum before upconversion [22].

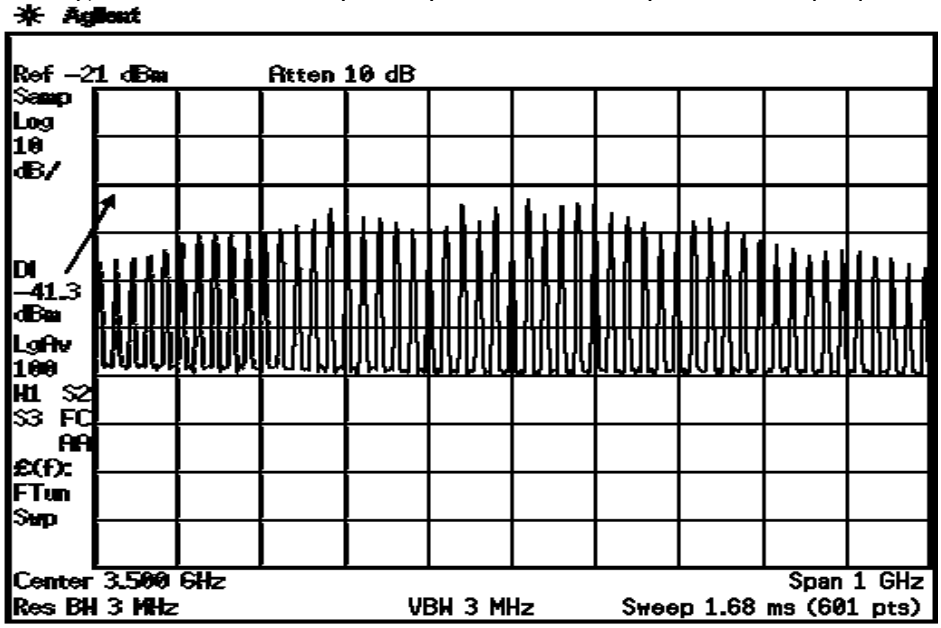

Figure 4-5: Generated pulse spectrum after upconversion [22].

4.4 IR-UWB test bench implementation

During this study, the WRI BER was the primary parameter of concern. The test bench used for the BER measurement in the lab is shown in Figure 4-6. The pattern pulse generator Anritsu ME522A transmitter was used to provide the input for both WRI transceivers shown in the figure. In fact, the input signal will act as the required input pulse for the WRI transceiver when it is in its transmission mode, while it will represent the reference signal for the other WRI transceiver which will be operating in its receiving mode. The input pulse duration was adjusted to 10 nsec, with a maximum pulse repetition frequency of 20 MHz. To control both WRI transceivers, the following modifications have been made to the VHDL program.

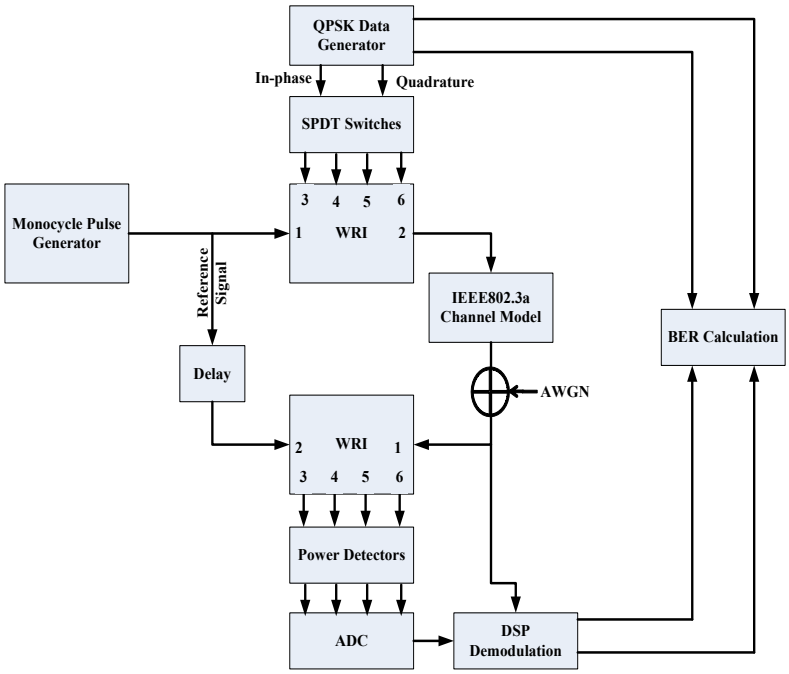

Figure 4-6: IR-UWB SISO test bench employing WRI circuits for the modulation and demodulation functions.

Based upon a control pin on the FPGA board, the VHDL program will arrange for one of the WRI circuits to operate in its transmission mode, while the other will be set to its receiving mode and vice versa. When any WRI circuit is set to operate in its transmission mode, this will initiate control signals from the FPGA board to alternate the SP4T switch position between RF ports 3 and 4 (Figure 3-11). On the other hand, when the WRI transceiver is operating as a receiver, the FPGA board will trigger the SP4T switch position to RF port 2, and will activate the Log-Detector through its VPOS TTL activation VIA (Figure 3-11).

As previously mentioned, in order to define the modulation state, we need to determine which Log-Detector has a minimum at its output port for every pair of the I and Q data streams. Hence, the output ports of the Log-Detector for the WRI transceiver operating in its receiving mode are connected to Analog Devices AD8564 Comparator. This comparator will provide a TTL output that can be fed to the FPGA board, which will help to determine the minimum port, (i.e. modulation state), and regenerate the I and Q data streams for BER measurement purposes. Furthermore, using the modified VHDL program, the FPGA board was configured to transform the regenerated I and Q streams into a single output stream which was compared to a synchronized replica of the transmitted stream using Anritsu ME522A receiver equipment. Figure 4-7 shows the test setup used for BER measurements of the WRI transceiver.

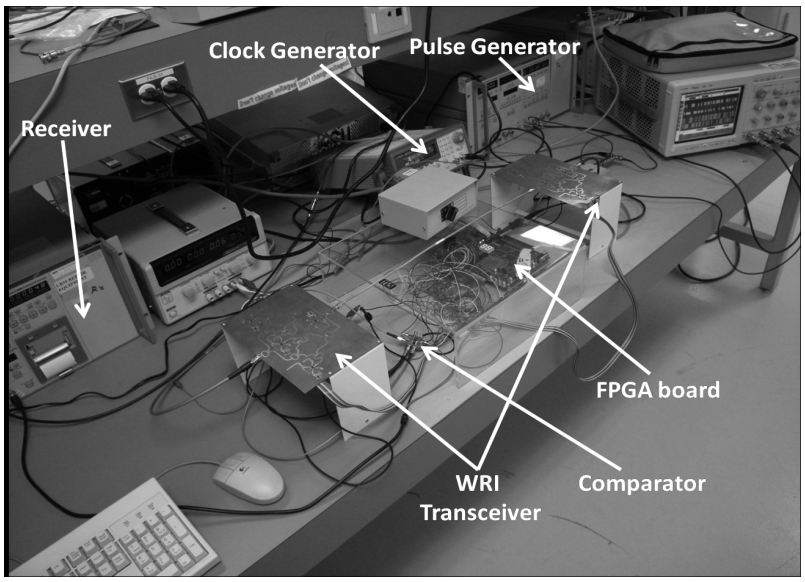

Figure 4-7: IR-UWB transceiver test setup.

The UWB wireless channel based on IEEE802.15.3a standard is resembled in the test bench by EB Propsim C8 Channel Emulator. The generated channel model using MATLAB is exported to the emulator, with the input of one of its RF interfaces connected to port 2 (output) of the transmitter WRI, while the output of the interface has been connected to port 1 (input) of the receiver WRI. The 100MHz RF bandwidth limitation of the emulator dictated a maximum pulse bandwidth of 100MHz. This pulse has been upconverted using 5 of Hittite's (HMC170C8) surface mount mixers with LO frequencies of 3.15, 3.25, 3.35, 3.45 and 3.55GHz generated using Wiltron synthesized sweep generator. Hence, a signal with a total bandwidth of 500MHz has been created and transmitted over the wireless channel.

We have also considered in this study the implementation of multiple transmit/receive antenna configurations of the same transceiver. The reason being is to

explore how the addition of multiple antennas at the transmitter, receiver or both sides will affect the coverage range, the data rate, the diversity order obtained and the system performance in terms of its BER. Furthermore, it is expected that utilizing the richness of the channel model can lead to a transceiver that can be used not only for high-speed communications, but also for localization and ranging.

It has been reported that for multiband UWB systems, adding more antennas in the transmitter, receiver or both sides simultaneously will generally enhance the coverage range, data rate and BER [47].

The SIMO and MIMO implementations of the IR-UWB transceiver are shown in Figure 4-8 and Figure 4-9, respectively. For those implementations, two WRI circuits are used in the receiver with joint combining using DSP demodulation. Synchronization is maintained between the transmitter, channel emulator and the receiver using the reference signal.

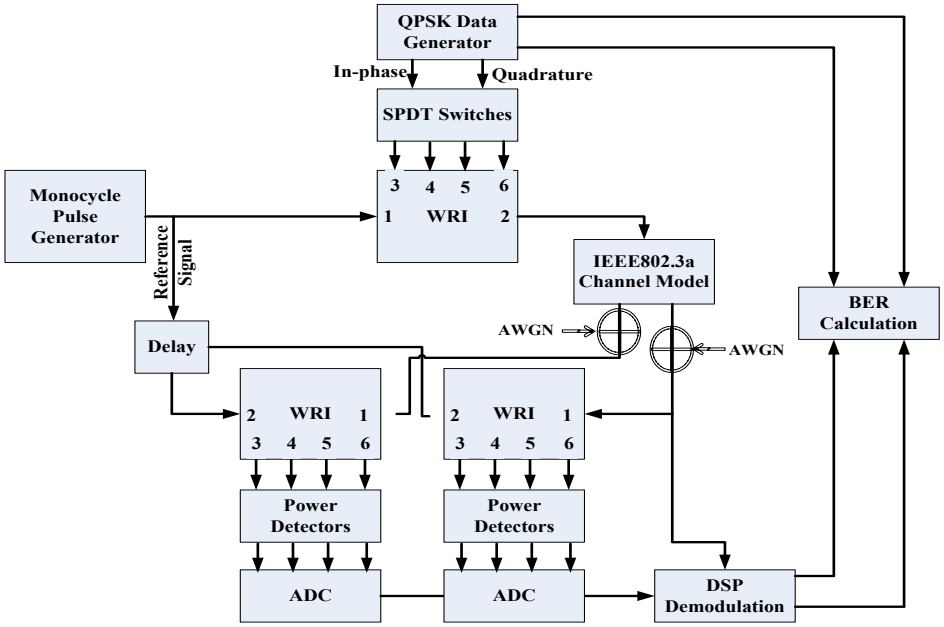

Figure 4-8: Block diagram of the IR-UWB test bench of the SIMO (1x2) transceiver.

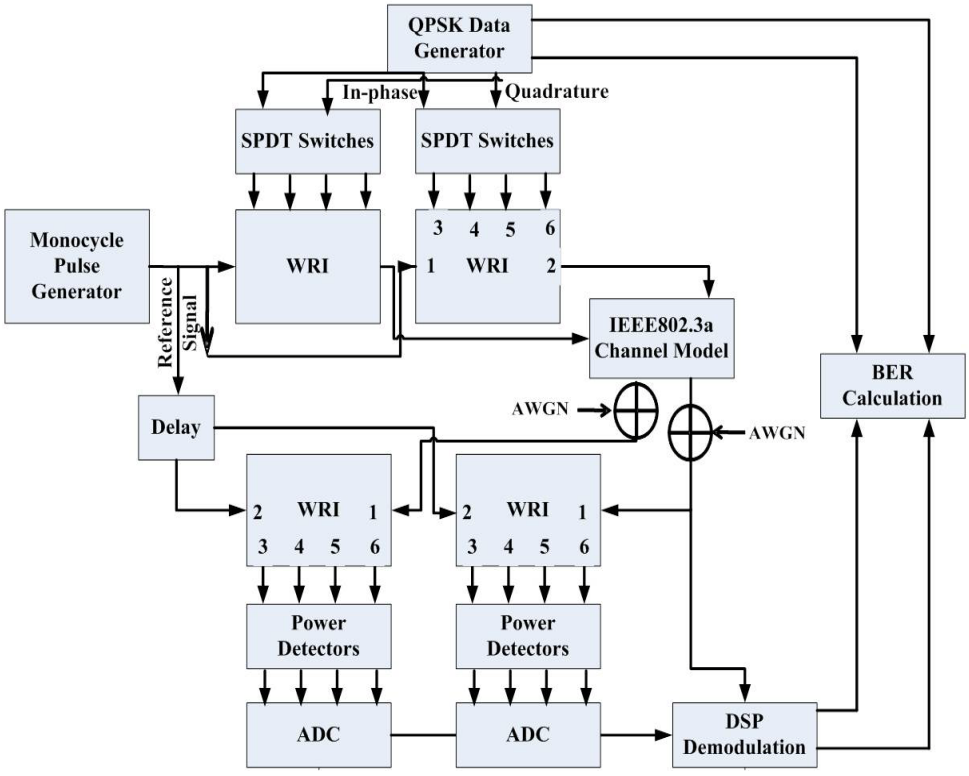

Figure 4-9: Block diagram of the IR-UWB test bench of the MIMO (2x2).

4.5 Demodulation algorithm

Based on the above results, a demodulation algorithm were implemented on a field-programmable gate-arrays (FPGAs) DSP platform. The adoption of FPGA digital signal processor in the proposed UWB platform is for the purpose of increasing the flexibility of the system and adapting it to software defined radio (SDR) needs. In addition, using design-ready intellectual property (IP) functions provided with the DSP platform significantly shortens the implementation time. Figure 4-10 illustrates the basic functions of the demodulation algorithm for the modulated signal.

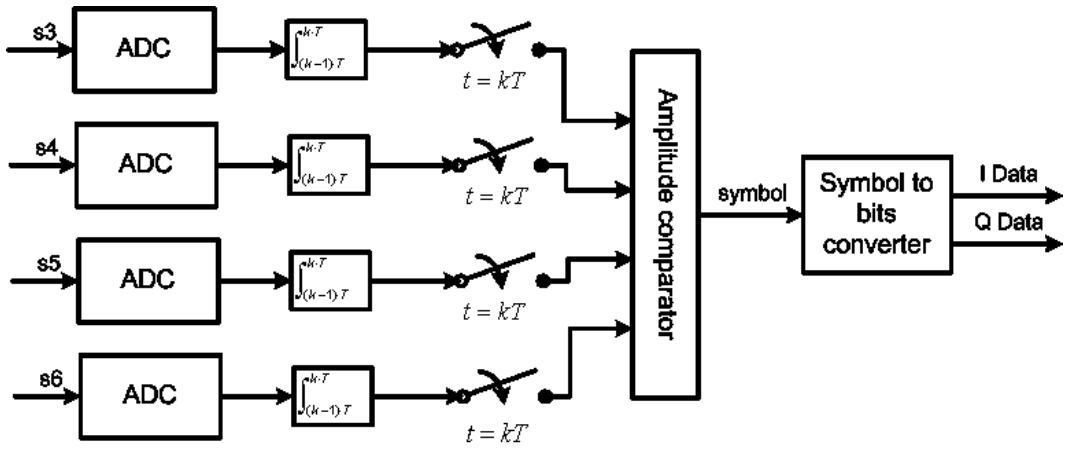

Figure 4-10: Illustration of demodulation algorithm for WRI circuit output ports.

Four output signals are sampled by analog-to-digital converters. Then samples are integrated over the pulse repetition period (T). At the clock times of $t = kT$, a comparison of accumulator output is done and the port with minimum amplitude is determined. If the amplitude of s_3 is minimum, symbol (0) is given. And the rest symbol (1, 2, and 3) can be deduced by analogy. Symbol (1) is corresponding to the minimum amplitude present at port 4. Symbol (2) is corresponding to the minimum

amplitude present at port 5. Symbol (3) is corresponding to the minimum amplitude present at port 6. Each symbol is then mapped to binary data and separated into I and Q channel. The symbol to bits converter can be realized according to the truth table shown below (Table 4.1.).

Table 4.1: Truth table of symbol to bits converter.

Inputs				outputs	
D_0	D_1	D_2	D_3	I	Q
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

It is assumed that only one input of the converter has a value of 1 at any given symbol time. The converter can be implemented with OR gates whose inputs are determined directly from the truth table. Output I is equal to 1 when the input digit is 1 at D_2 or D_3. Output Q is equal to 1 when the input digit is 1 at D_1 or D_3. These conditions can be expressed by the output Boolean functions in (4.2) and the bit converter can be implemented with two OR gates [48].

$$\begin{aligned} I &= D_2 + D_3 \\ Q &= D_1 + D_3 \end{aligned} \tag{4.2}$$

Based on the above results, demodulation algorithms were implemented on a field-programmable gate-arrays (FPGAs) DSP platform. The FPGA DSP platform includes analog-to-digital converters, digital I/O interface, and a Stratix EP1S80 FPGAs device [49]. The Stratix EP1S80 FPGAs device is in density of 79,040 logic elements (LEs).

Each LE contains a four-input look-up-table (LUT), which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carries chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode [50]. The DSP blocks in the Stratix devices run at 333 MHz to provide data throughput performance of 2.67 Giga multiply-accumulate (GMAC) operations per second per DSP block. The FPGA device (EP1S80) on the platform includes 22 DSP blocks which can provide a combined throughput of up to 58.6 GMAC per second [51].

The above algorithms were first built using graphical-based design-entry methods. Then the design is converted to a device programming image by the assembler of the development tool (Quartus II [52]) so that the FPGA device can be configured with the desired algorithm. As an example, Figure 4-11 shows part of the design schematic of the demodulation algorithm.

Besides the above algorithms, baseband clock management is necessary for symbol synchronization. The involved clock signals include analog-to-digital converter (ADC) sampling clock, symbol clock, an external clock signal synchronizing the data generator, a trigger signal synchronizing pulse generator, and internal clock signals of FPGA device. These clock signals having different frequencies are derived from a single clock source, an 80 MHz oscillator on the DSP platform. Using phase-locked loops functionality built in the FPGA system blocks, clock signals having desired frequencies are synthesized at PLL output ports using scaling factors.

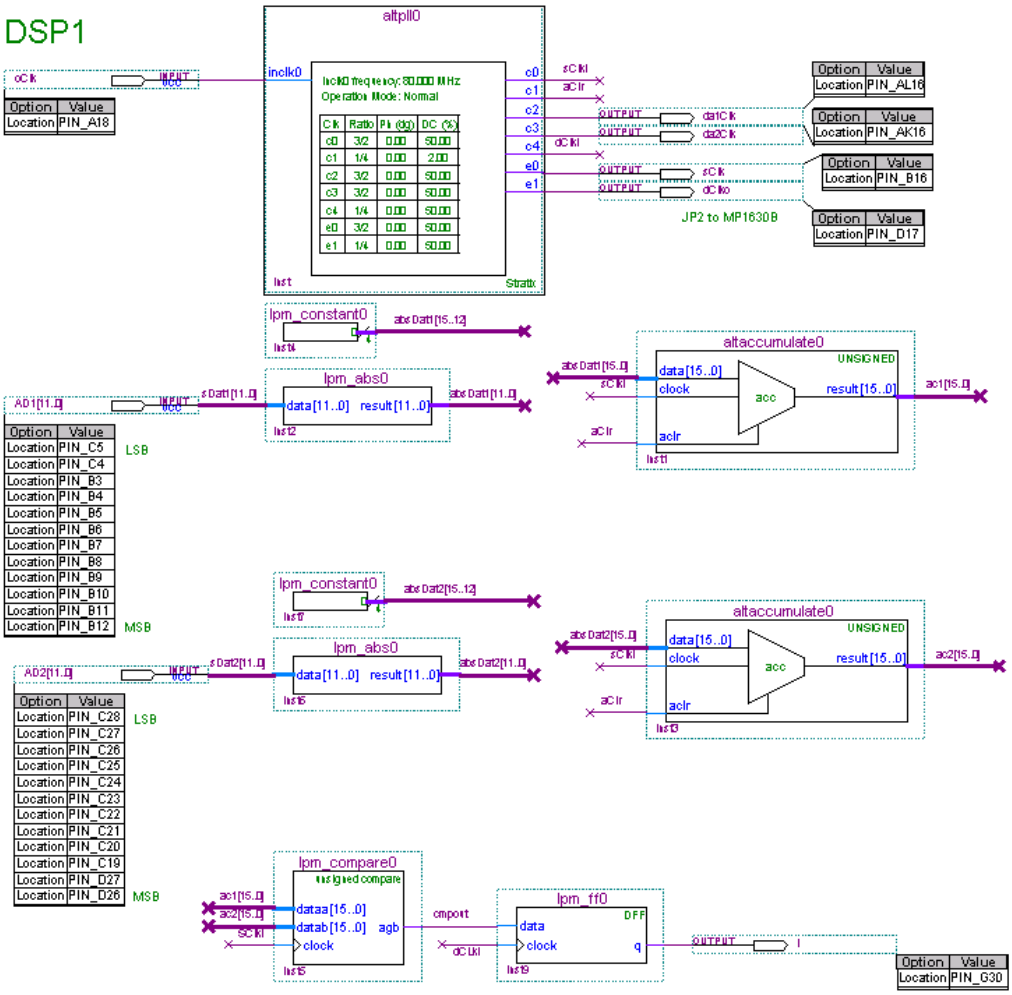

Figure 4-11: FPGA implementation of demodulation algorithm.

4.6 Synchronization algorithm

One of the practical issues considered when implementing the IR-UWB test bench is the realization of synchronization. In order to demodulate the received signal, the received pulse signal and a reference signal are coherently processed in the WRI demodulator circuit. This implies that a reference signal must be synchronized to the receive signal using a certain method. During simulation and experimental study of the IR-UWB system, the reference signal is derived from the transmitted pulse signal using a power divider. A certain length of transmission line is inserted into the reference signal path to match the receiving signal path delay. In future developments of the platform, this synchronization will be accomplished using an algorithm based on WRI circuit output signals. An investigation has been done on the output signals of WRI circuit under non-synchronization situations, i.e., an existing arbitrary delay exists between

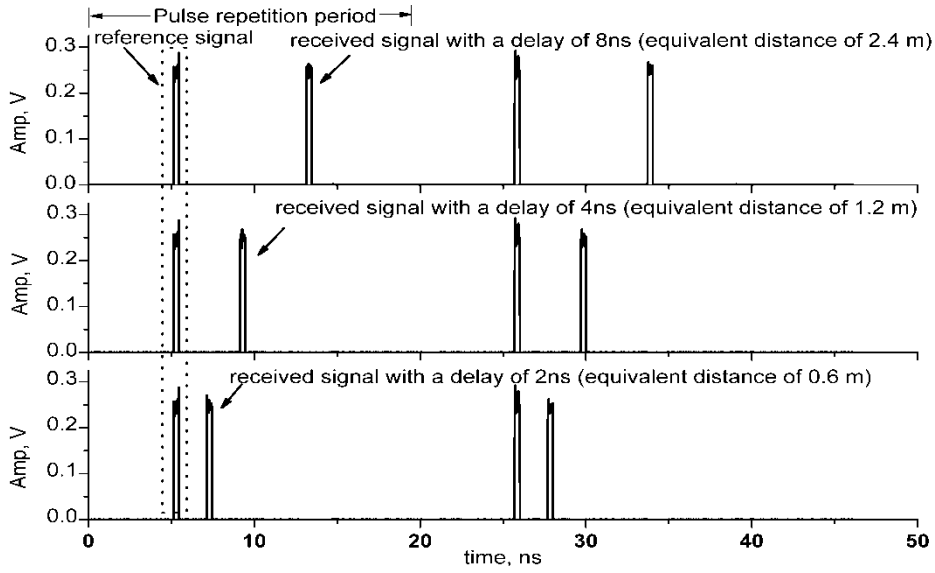

Figure 4-12: Simulated output signals for three different delays.

reference and received signals. The purpose is to find the delay by observing signals at outputs of the WRI circuit.

System simulation has been carried out with practical parameters over IEEE802.15.3a channel. A pulse signal occupying a frequency band from 3.1 to 4.1 GHz is used for simulation. Its fractional bandwidth is 0.28. The width of each pulse is 5 nsec. The pulse repetition period is 50 nsec. The simulation focuses on the time delay and doesn't include the power decay factor. Figure 4-12 shows the output signals for three different delays between reference and received signals. Within a pulse repetition period, the output signal is a waveform with two pulses. The simulation results show that the time difference between two pulses is equivalent to the propagation delay between reference pulse and the received pulse. The propagation delay can be easily converted to a free space distance between transmitter and receiver. Since the output signal can be thought as a pattern for a certain delay, a pattern recognition algorithm [53] was intuitively used to estimate delay values.

A proof-of-concept experiment was done to verify this function. In the experiment, two input ports of a WRI circuit are fed respectively with a reference signal and a delayed received signal. WRI output signals are measured when the delay in receive path is changed using three different cables with lengths of 6, 11, and 14 feet, respectively. Those were chosen because they correspond to the expected delays of the IEEE802.15.3a channel models. It is readily seen in Figure 4-13 that within a pulse repetition period the measured time difference between two voltage peaks is equivalent to the length of cable. This equivalence can be verified using equation (4.3).

$$delay = \frac{l}{(c/\sqrt{\varepsilon_r})} \tag{4.3}$$

where l is the length of cable, $\boldsymbol{c = 3 \times 10^8}$ is the speed of light in free space, $\varepsilon_r = 2.03$ is the known dielectric constant of the material of used cables. The small deviation caused by connectors between cables is neglected.

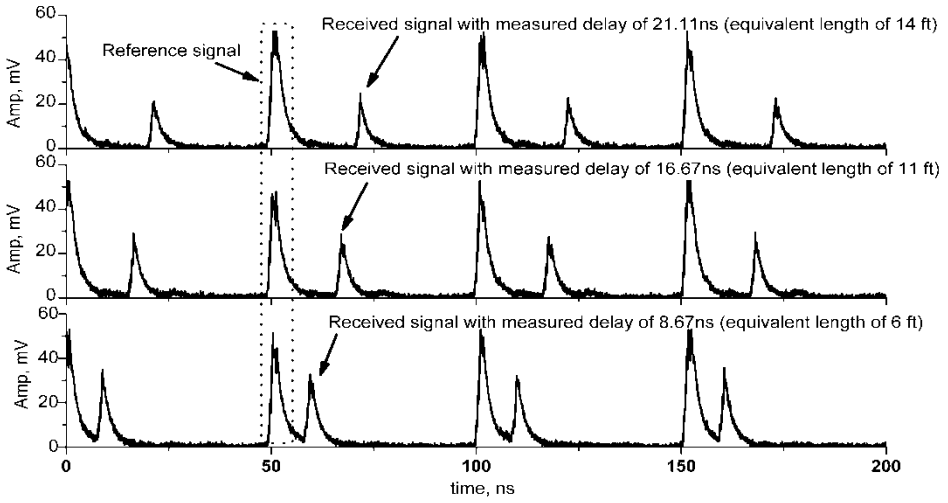

Figure 4-13: Measured signals for three different delays.

Based on the above results, a synchronization algorithm can be developed to facilitate the generation of a reference pulse, at the receiver, acquiring and synchronizing to the transmitted signal. The algorithm based on recognition of WRI circuit output signal pattern may provide a simple solution for this IR-UWB system.

4.7 BER performance analysis

The average BER of a QPSK system is given by

$$P_b = \int_0^\infty Q\left(\sqrt{\overline{\gamma_b}}\right) f_h(\overline{\gamma_b}) d\overline{\gamma_b} \tag{4.4}$$

where $f_h(x)$ corresponds to the pdf of the random variable h which represents the channel fading statistics and the function $Q(x)$ is defined by $Q(x) = 1/\sqrt{2\pi}\int_x^\infty e^{-t^2/2}\,dt$. $\overline{\gamma_b}$ is the average signal-to-noise ratio (SNR). For evaluating the asymptotic BER behavior, P_e can be upperbounded by

$$P_b \leq \frac{1}{\sqrt{2\pi}}\int_0^\infty \frac{1}{\sqrt{\overline{\gamma_b}}} e^{-\overline{\gamma_b}/2} f_h(x)dx \tag{4.5}$$

where this bound follows from $Q(x) \leq 1/\sqrt{2\pi}\, e^{-x^2/2}/_x$.

To simplify the analysis and since there is no exact closed-form solution to the distribution of h available in the literature, we will use an approximation of the exact pdf $f_h(x)$. The exact pdf will be replaced by an approximate pdf $f_{app}(x)$ based on a minimum mean-square error (MSE) criterion that satisfies

$$MSE = E[f_h(x) - f_{app}(x)]^2. \tag{4.6}$$

By solving the above least-squares problem numerically using Gauss-Newton method, the best fit for the exact distribution $f_h(x)$ is found to be an N-component mixture of Gamma distributions which can be written as [54]

$$f_\gamma(x) = \sum_{n=1}^N \gamma_n \frac{e^{-x/\theta_n} x^{k_n-1}}{\Gamma(k_n)\theta_n^{k_n}} \quad ; \quad x \geq 0 \tag{4.7}$$

where $\sum_{n=1}^N \gamma_n = 1$. The parameters k_n and θ_n are positive for all values of n and $\Gamma(x) = \int_0^\infty \mathrm{e}^{-\mathrm{t}}\mathrm{t}^{\mathrm{x}-1}\mathrm{dt}$ is the Gamma function.

By replacing $f_h(x)$ by $f_\gamma(x)$ in (4.4) we get

$$P_b \leq \frac{1}{\sqrt{2\pi}}\sum_{n=1}^N \gamma_n \frac{\Gamma(k_n-\frac{1}{2})}{\Gamma(k_n)(\theta_n\overline{\gamma_b})^{\frac{1}{2}}(1+\frac{\theta_n\overline{\gamma_b}}{2})^{k_n-\frac{1}{2}}} \tag{4.8}$$

which can be approximated for sufficient large values of SNR by

$$P_b \approx \frac{1}{\sqrt{\pi}} \sum_{n=1}^{N} \gamma_n 2^{k_n - 1} \frac{\Gamma(k_n - \frac{1}{2})}{\Gamma(k_n)} (\theta_n \overline{\gamma_b})^{-k_n} \ . \tag{4.9}$$

4.8 Simulation and measurement results

The WRI circuit was simulated using the ideal circuit model shown in Figure 3-4. Based on the characteristics of the logarithmic power-detector, an ideal power detector is also modeled in Simulink and shown in Figure 4-14.

When the rectangular pulse train is fed into the model, four output signals show pulsed amplitude profiles which vary according to the phase difference. For a certain phase difference, each output signal has a pulsed voltage which occurs only at the pulse duration.

Figure 4-15 show the simulated output signals at ports 3–6 for modulation state 0. At this modulation state, the phase difference $\Delta\theta$ at each frequency is equal to 0º. As shown port s_3 has minimum amplitude and port s_5 has maximum amplitude. At ports 4 and 6, output signals amplitudes have median values. Results for the other three modulation states were also obtained and are shown in Figure 4-16 to Figure 4-18, respectively.

It is readily seen that s_4 is minimum when modulation state is 1, s_5 is minimum when modulation state is 2, and s_6 is minimum when modulation state is 3. Hence, during a symbol period, all output ports have non-zero pulse amplitudes except for one port (corresponding to the modulation state) which has zero pulse amplitude.

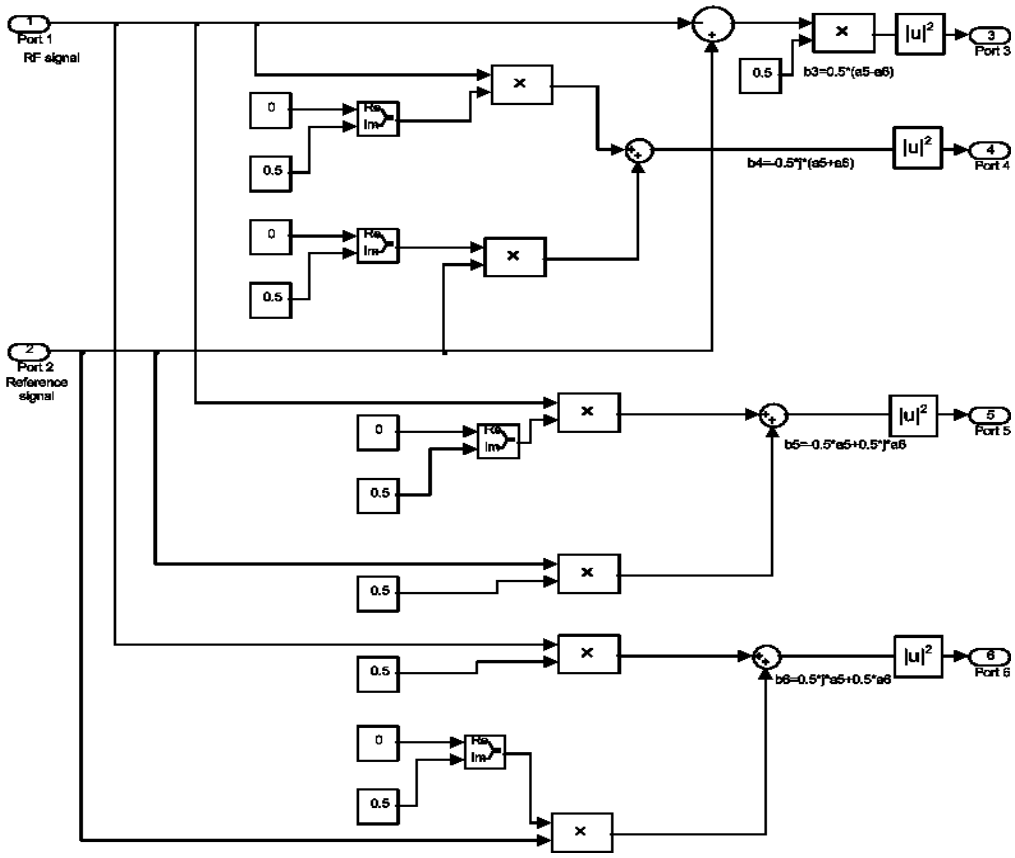

Figure 4-14: An ideal log-detector model in Simulink.

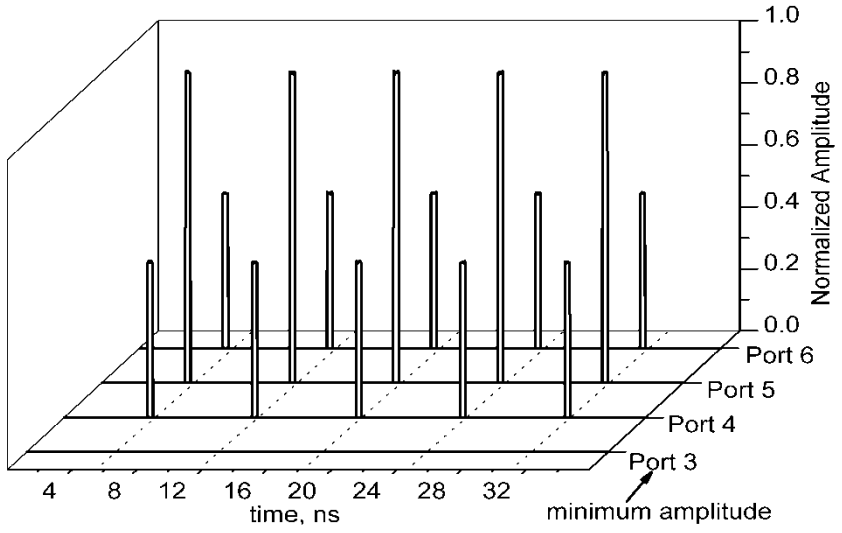

Figure 4-15: Signals simulated at ports 3 to 6 of demodulator for modulation state 0.

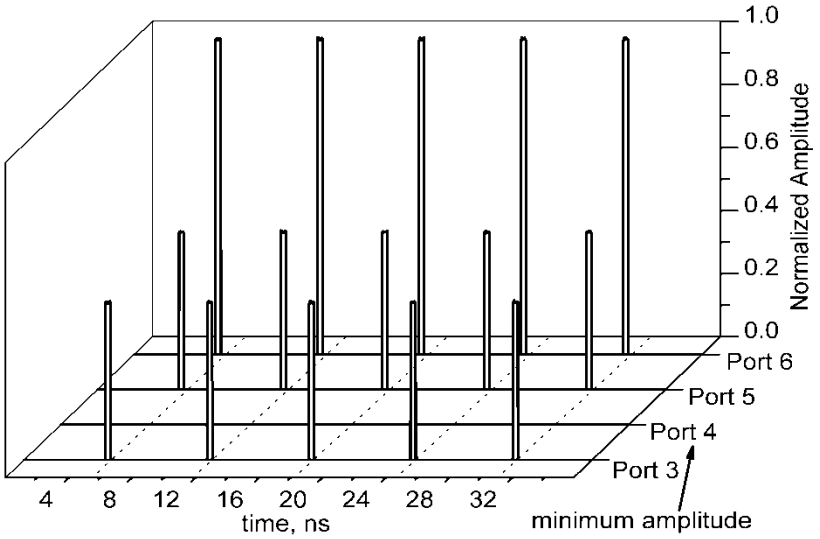

Figure 4-16: Signals simulated at ports 3 to 6 of demodulator for modulation state 1.

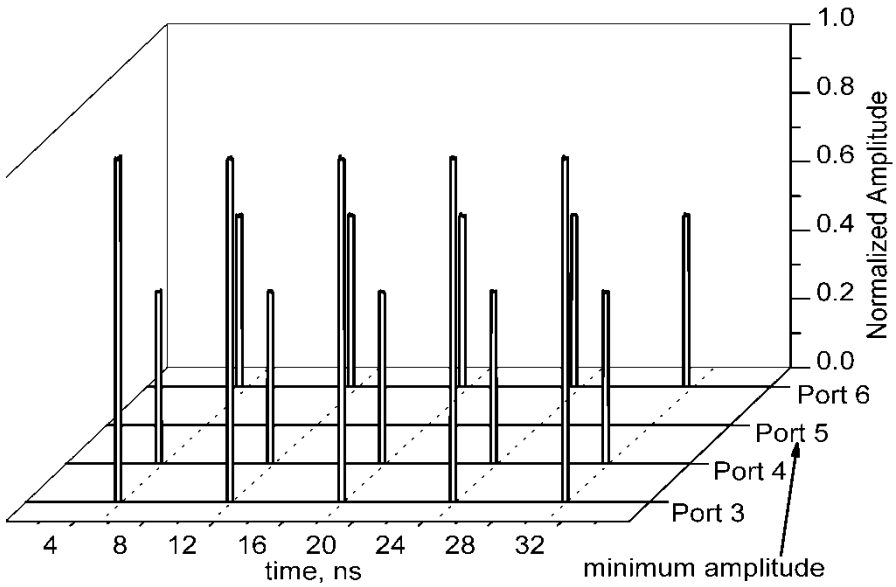

Figure 4-17: Signals simulated at ports 3 to 6 of demodulator for modulation state 2.

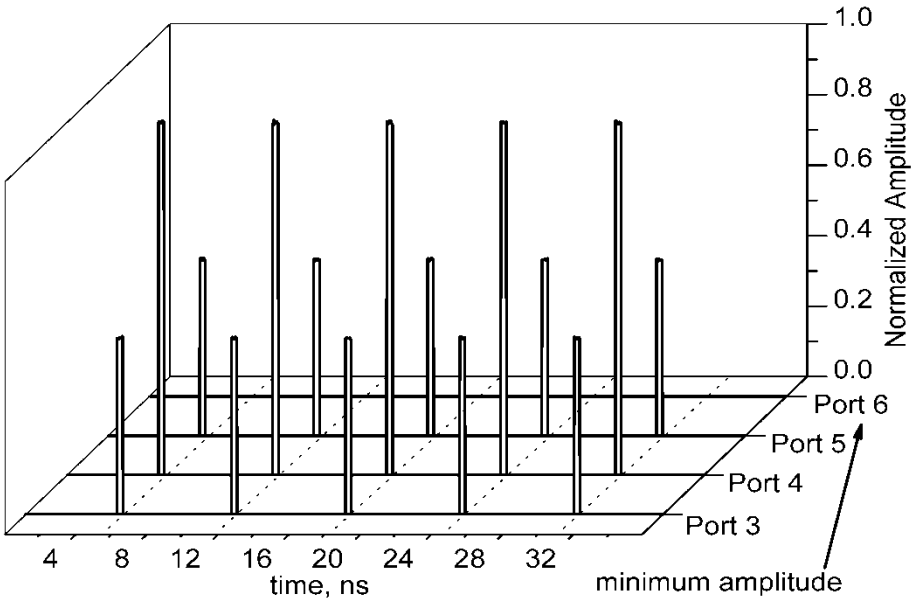

Figure 4-18: Signals simulated at ports 3 to 6 of demodulator for modulation state 3.

The simulation and measurement results considered a 15 dB range of signal-to-noise ratio (SNR) due to simulation time, and implementation limitations. For an AWGN channel, BER measurement results curve compared to both, simulation and theoretical curves are shown in Figure 4-19. Similar results for the BER were reported in [55], where an architecture based upon power dividers and hybrid couplers was used for the WRI circuit. As can be seen in the figure, a good agreement between the measurement and theory curves is obtained.

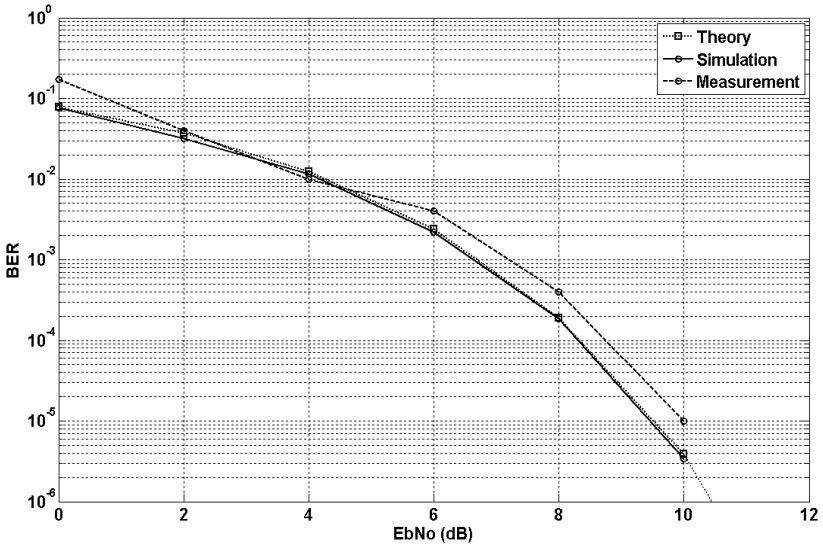

Figure 4-19: BER theory, simulation and measurement curves comparison.

The BER performance of the IR-UWB transceiver is considered in IEEE802.15.3a channel models CM1 and CM4. The system considered a total bandwidth of 500MHz. The arrival rates Λ and λ and the decay factors Γ and γ of the cluster and ray, respectively, follow the parameter values used in [56]. For the purpose of demonstration, the numerical results are obtained in the two extreme channels: CM1 and CM4.

For IR-UWB transceiver, an extensive numerical analysis to verify the accuracy of the approximations is performed for the two channel models. For the gamma-mixture approximation, numerical results showed that increasing the number of components in the mixture (N in eq. (4.7)) beyond three results only in a marginal decrease in the MSE. Consequently, to keep the analysis simple, a 3-component mixture of gamma distribution is used for channel modeling.

For the IR-UWB transceiver, simulation, analysis and measurement results are compared in Figure 4-20. Small discrepancy is observed between simulation and analysis results obtained from equation (4.9) due to the approximations used. Closer agreement can be obtained by considering more components in the channel approximate distribution in (4.7). Further, equation (4.9) clearly demonstrates the system diversity order to be equal to k_n especially at high SNR values.

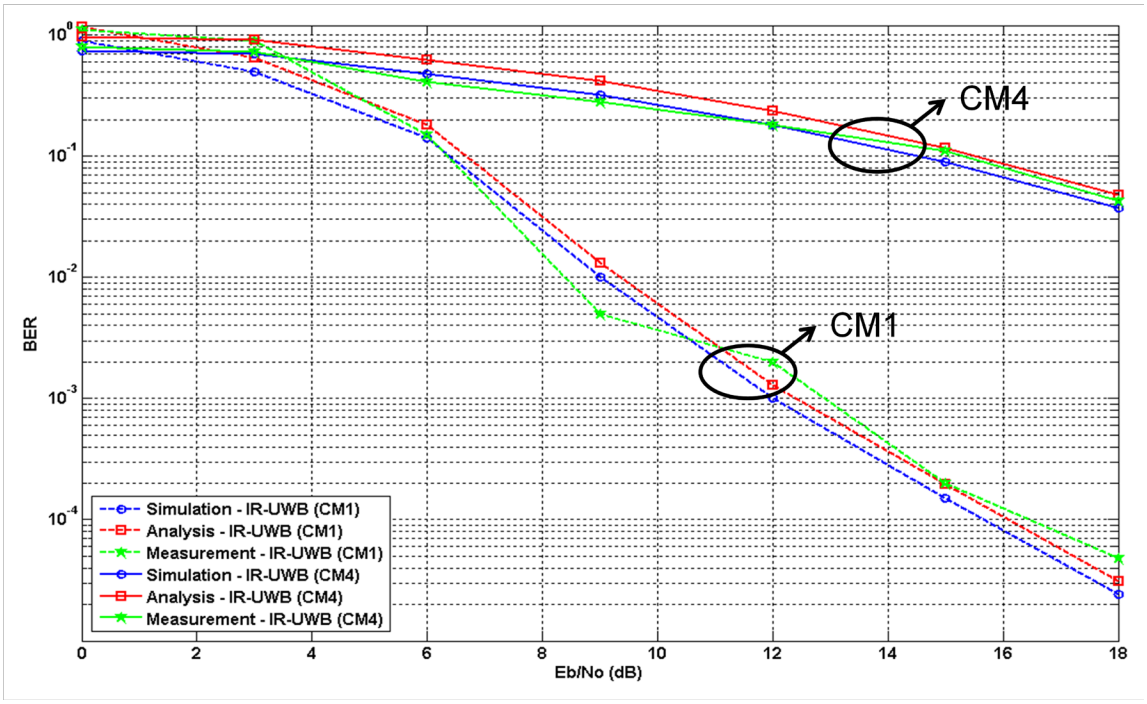

Figure 4-20: IR-UWB transceiver simulation, analysis and measurement results for CM1 and CM4.

Also, in the following figures, the BER performance of the prescribed transceivers is verified by simulation and measurement results for SISO, SIMO and MIMO test bench. The IEEE802.15.3a standard channel parameters where chosen to emulate the best vs. worst case scenarios of fading in an indoor environment (CM1 vs. CM 4 in [57]). The

worst case model represents an extreme non-line of sight (NLOS) multipath channel with 25 nsec RMS delay spread and 41 multipath components having values 10 dB below the power level of the strongest component. The considered modulation format is QPSK, where the total bandwidth of the pulse transmitted is 500 MHz and the rate of transmission is 20 MHz to relax the requirements for the external sampling clock. As shown, Figure 4-21 and Figure 4-22 illustrate the obtained results for IR-UWB transceiver for CM1 and CM4, respectively. BER performance gains resulting from the additional diversity and the enhanced energy captured are evident in the SIMO (1x2) and MIMO (2x2) systems compared to the transceiver in the SISO case [58]. For example, considering CM1 of the IR-UWB transceiver at a BER of 10^{-5}, the MIMO system with 2 branches at the receiver outperforms its SIMO counterpart by about 2.2 dB. This can be due to both, the diversity gain (frequency and time since combining is performed over five consecutive QPSK symbol periods), and the extra power gain in addition. Furthermore, those figures show that simulation and measurement curves follow the same diversity order with good agreement between them.

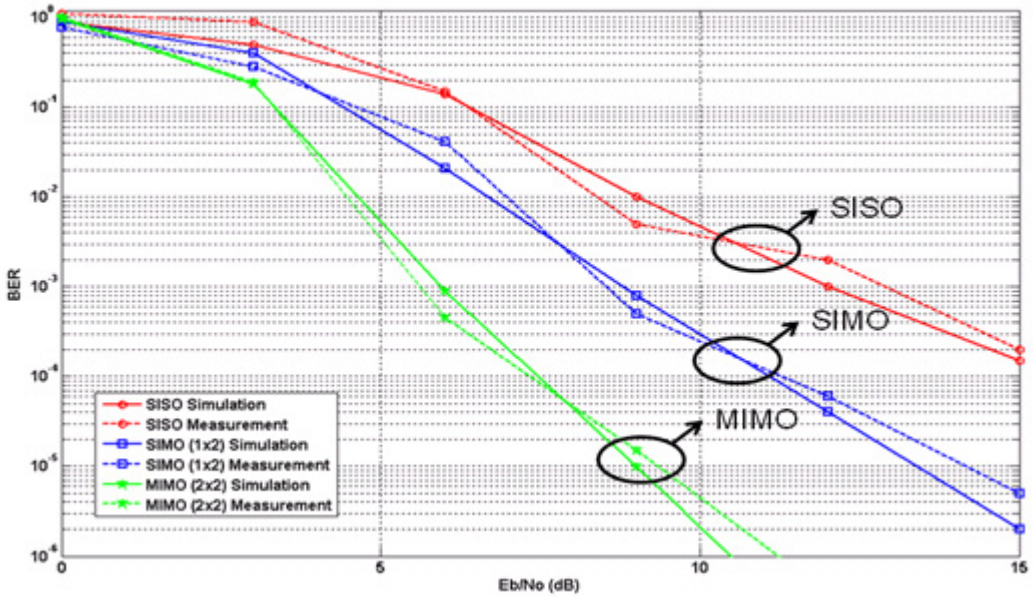

Figure 4-21: SISO, SIMO (1x2) and MIMO (2x2) BER simulation and measurement results of IR-UWB transceiver for CM1.

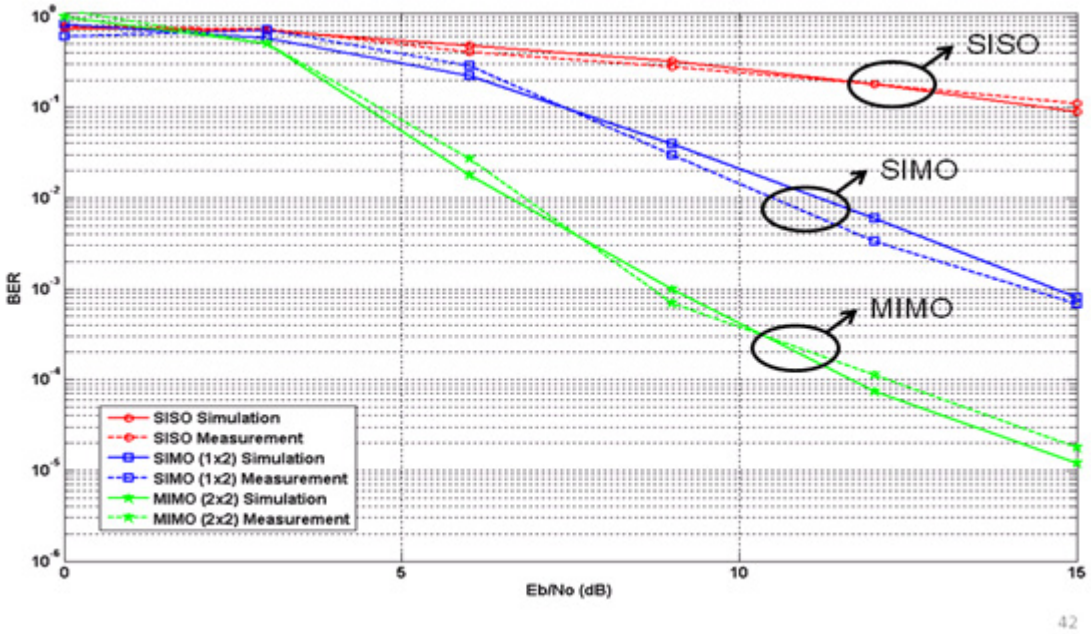

Figure 4-22: SISO, SIMO (1x2) and MIMO (2x2) BER simulation and measurement results of IR-UWB transceiver for CM4.

Furthermore, in order to have more realistic perspective of the transceiver performance, amplitude and phase imbalances of ±0.5dB and ±9^{o} [59] are considered in this study, respectively. An IQ impairment analysis was performed by sweeping the amplitude imbalance between -0.5 to 0.5 dB and the phase imbalance between -9^{o} to 9^{o}. The impaired IQ channels are compared with the ideal ones obtained from simulations in Figure 4-21 and Figure 4-22 for CM1 of IR-UWB. As seen in Figure 4-23, IR-UWB exhibits a maximum loss of 1.5dB from the ideal case. This can be overcome by an optimization process to minimize the phase imbalance of the designed transceiver circuit [60].

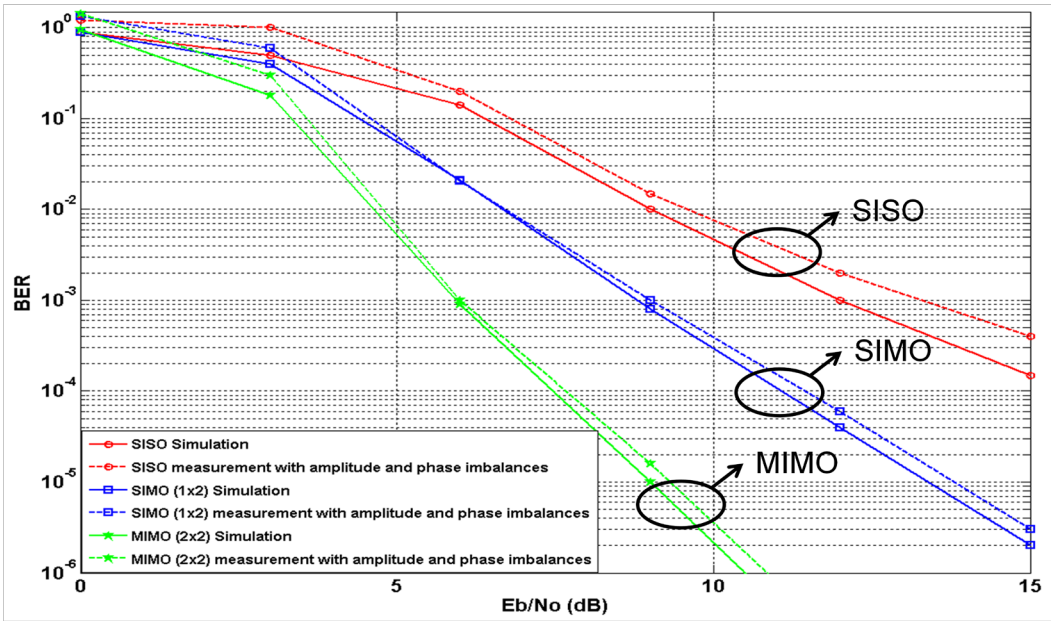

Figure 4-23: SISO, SIMO (1x2) and MIMO (2x2) BER results of IR-UWB transceiver for the ideal case and with amplitude and phase imbalances for CM1.

Also, Figure 4-24 shows the obtained output signal constellations for various SNR values. After the addition of white noise and experiencing the standard channel fading, the output constellations are presented in Figure 4-24 (a)-(d) for 2, 6, 8, and 10 dB SNRs, respectively. It is found that the output constellation is stable, and remains focused even if the errors appear because of the comparator circuit, whose output voltage can have only two distinct values. Otherwise, if the errors appear, the output signal constellation presents a rotation to the left or right of 90^{o} multiples and "the image" of the output constellation is the same. Therefore, errors appear in the demodulated signal and the BER rises up.

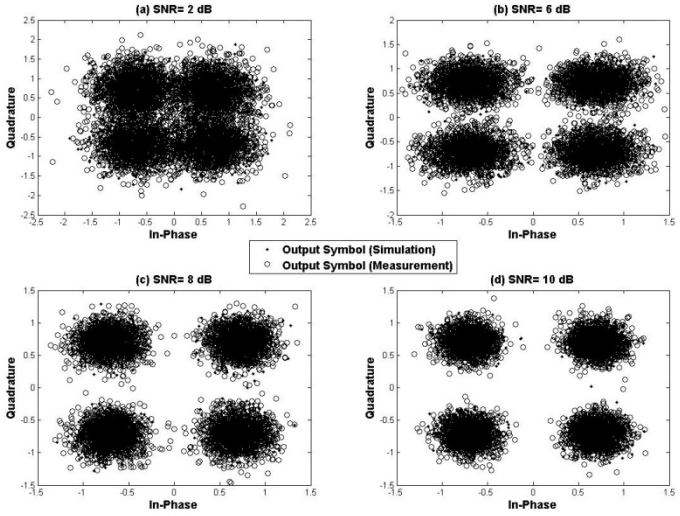

Figure 4-24: Output measured and simulated signal constellations for different signal SNRs.

For the test bench, the maximum power level of the RF input signal is set after measurement to be +5 dBm along the variant SNR values. The dynamic range of the WRI transceiver was found to be significantly, if not exclusively, dependent on the Log-

Detector dynamic range. Therefore, this WRI transceiver is a robust QPSK demodulator according to the dynamic range of the input QPSK signal.

It is worth to mention that the maximum data rate with an acceptable BER for the new WRI transceiver would greatly depend upon the SP4T switching characteristics. As addressed in [61], the maximum supported switching speed for the used SP4T switch is 50 nsec, which correspond to a maximum data rate of 40 Mbps. Large BER degradation was encountered when the data rate was increased above that bound due to this switch limitation.

4.8 Conclusion

This chapter introduced the IR-UWB WRI transceiver circuit, where pulse generation, different configurations of transmit and receive antennas for transceiver test bench were discussed. The concept of operating the transceiver as one node capable of performing modulation and demodulation functions is presented. Then, briefly, the simple synchronization algorithm used within the test bench is provided. Following that, an upperbound expression for the BER of the transceiver is derived to benchmark the expected measurement and simulation results. Later, obtained analysis, simulation and measurement results are compared where close agreement is found between them. In general, all curves maintain same diversity order with inferior performance for measurement results due to measurement and synchronization error. Considering amplitude and phase imbalance case, results indicate that around 1.5dB BER performance loss is encountered compared to the ideal case.

CHAPTER 5 OFDM-UWB TRANSCEIVER

5.1 Introduction

With the higher demand of data throughput, new emerging wireless technologies moved toward more sophisticated modulation schemes. OFDM is considered as one of these most promising schemes. Among the applications that adopt OFDM, Wireless USB, WiFi and Bluetooth release 4.0. Since UWB is one of the important short range wireless communication technologies, studying OFDM for UWB systems has been of great interest for research community recently.

Many previous works in the literature considered utilizing the WRI circuit in IR-UWB systems. However, in this thesis we present the first implementation results of an OFDM-UWB system utilizing the WRI circuit as a direct downconverter. For a carrier-based OFDM-UWB system, in the following, the procedure for the design and implementation of a transceiver employing the WRI circuit will be discussed.

The idea was initiated based on the fact that WRI circuit can be used as amplitude and phase detector to extract the in-phase (I) and quadrature (Q) components of the signal at the front end of the communication receiver. This will be employed to initiate the same study for the WRI circuit for an UWB OFDM signal.

As a first approach, the system will be simulated then implemented with an AWGN channel. Then, since the implemented transceiver is targeted to work for UWB applications, transceiver performance will be verified in a realistic UWB channel. Hence, in the following stage, the channel impulse response based upon IEEE 802.15.3a will be generated, and used in both simulation and implementation in order to test the

transceiver. Also, the ability of the WRI circuit to extract the in-phase and quadrature components under such channel impairments will be investigated.

The study performed in [62] only considered a two paths Rayleigh fading channel with a delay spread of 0.23μsec. Comparing the studied channel model in [63] with the one implemented based upon IEEE802.15.3a standard which includes 25 nsec RMS delay spread and 41 multipath components, we will examine the effect of different amplitude and phase imbalances of the WRI circuit and the effect of that on the system's total BER.

The IEEE802.15.3a channel model is generated using MATLAB, and then used in ADS to simulate the whole system. In order to improve the system BER performance by using spatial diversity, we will propose later a transceiver implementation for SIMO and MIMO systems.

5.2 Implementation challenges and limitations

The first encountered problem is the limited bandwidth supported by the channel emulator. According to the operation manual, the maximum RF bandwidth supported is 100MHz. Since, according to the FCC regulations an UWB signal must occupy a total bandwidth of 500MHz or above, the adopted solution is based on transmitting the OFDM symbol over 5 non-overlapping sub-bands each with a bandwidth of 100MHz. Then, the transmitted OFDM UWB signal is formulated by summing the upconverted OFDM symbols over the center frequency for every sub-band and transmitting the resulting signal.

On the other hand, we are constrained by the clock speed of the A/D and D/A converters. The A/D converter available on the FPGA board has an internal clock speed of 125MHz, while the D/A has a 165MHz one. In order to overcome this obstacle, an external signal generator will be used to generate the clock that drives both converters. The clock speed will be chosen as 200MHz or above to maintain a baseband OFDM symbol bandwidth of 100MHz.

In order for the proposed system to be as closer as possible to a realistic MB-OFDM system we will take the following measures

- Instead of implementing a 128 point FFT algorithm for a total bandwidth of 528MHz which means a 4.125MHz bandwidth for each subband, a 32 point FFT algorithm is implemented for every 100MHz subband which corresponds to a 3.125MHz. The reason behind this is that the emulated channel model was simulated and tested for an MB-OFDM system with 4.125MHz subband bandwidth, and by reducing the number of subcarriers for our system, we are also ensuring at the same time that the subband bandwidth in our implementation will be as much similar as possible to the original system. Hence, this means that we should expect a great resemblance between the channel effect in the original system and our system.
- Based upon a comparison between the original system implementation and our system, we propose the following system parameters for both the simulations and the implementation

Table 5.1: Comparison between the parameters of the MB-OFDM and implemented OFDM-UWB systems.

The Parameter	MB-OFDM System	Proposed System
Number of subcarriers(N)	128	32
Subcarrier spacing	528MHz/128=4.125MHz	100MHz/32=3.125MHz
QPSK symbol period	1/528MHz=1.89nsec	1/100MHz=10nsec
OFDM symbol useful duration	128x1.89nsec=242.4nsec	32x10nsec=320nsec
Cyclic prefix duration	0.25x242.4nsec=60.6nsec	0.25x320nsec=80nsec
Total duration of one OFDM symbol	242.4+60.6+9.5=312.5nsec (9.5nsec guard interval)	320+80=400nsec

Using the proposed system with the IEEE802.15.3a channel model which has an average RMS delay spread of 14.18nsec and a coherence bandwidth of 4.5MHz, we can observe that the proposed system is expected to have immunity toward multipath fading. For this indoor UWB system with N x 1 QPSK symbol period >>> delay spread, the channel for the proposed system can be described as underspread. The expected data rate assuming that all the 32 subcarriers will be used to transmit data (sending 32 QPSK symbols every 400nsec) will be 80Msps or 160Mbps.

5.3 OFDM-UWB test bench implementation

Figure 5-1, Figure 5-2 and Figure 5-3 show the block diagrams for the transceivers implementing the SISO, SIMO and MIMO emulated wireless channels, respectively. According to OFDM-UWB system standards, the total operating bandwidth is 528 MHz divided over several sub-bands. The number of these sub-bands has been chosen carefully to provide a compromise between immunity to multipath fading and system complexity. Hence, a 128-point IFFT/FFT modulation was considered. In the proposed system, a limitation imposed by the channel emulator, is that the total RF bandwidth of the channel is 100MHz. To overcome this obstacle, instead of implementing a 128-point FFT algorithm for a total bandwidth of 528MHz, a 32-point FFT algorithm is implemented to provide the best resemblance between the channel encountered in the standard and the one in the proposed transceiver.

In the simulations and measurements, the transceiver considered a system operating with an instantaneous bandwidth of 100 MHz, divided into 32 tones with an OFDM symbol period of 400 nsec (containing 40 samples), of which 80 nsec is a cyclic prefix corresponding to 8 samples. The frequency spacing between the carriers is 3.125 MHz. With all the sub-carriers carrying data, this will give a total symbol rate of 80 Msps or an equivalent bit rate of 160 Mbps. The modulation format for each tone is QPSK.

Since an UWB signal must occupy a total bandwidth of 500MHz or above, the proposed transmitter sends the same OFDM symbol over 5 non-overlapping sub-bands each with a bandwidth of 100MHz. Then, the transmitted OFDM-UWB signal is

formulated by summing the upconverted OFDM symbols over the center frequency for every sub-band and transmitting the resulting signal.

The receiver operation is based upon a well-known technique for the direct extraction of the In-phase (I) and Quadrature (Q) components of an RF modulated signal [64]. The WRI module can be used for direct translation of the I and Q signals from the RF to the baseband without any mixer and without any intermediate frequency. The technique for the extraction of I and Q signals from the output signals of the WRI module with the knowledge of the WRI structure and of the I, Q signal statistics has been discussed in [65]. We consider the same simple technique given in [66], which shows that an appropriate combination of the power levels of the four power detectors of the WRI module is used to calculate the I and Q components of the OFDM signals in time domain.

The I and Q channels are fed later to an analog to digital converter, which produces a 12-bit word taking samples at a maximum rate of 250 Msps (external clock is used). Using a simple VHDL program, the functions serial to parallel and cyclic prefix removal are obtained, and then employing the FFT function from Altera on the FPGA board, a 32-point FFT algorithm has been implemented.

The module following the FFT, which is a channel equalization block, is implemented using Altera's DSP builder library function for equalization. Finally, QPSK de-mapping can be achieved using Altera's DSP builder library function for constellation mapping/de-mapping. After obtaining five consecutive demodulated QPSK symbol versions, these will be combined to provide a final output.

It is worth to mention that maintaining synchronization is mandatory between the local oscillators in the transmitter, channel emulator and the receiver. This can be accomplished by using the same LO signal for the mixer in the transmitter and the channel emulator using RFLO port on its RF interface. This port allows the use of external signals for the internal upconversion circuit of the channel emulator.

For testing purposes, a simple synchronization method is adopted. The delay caused by the channel model can be accounted for by transmitting a single-tone pilot-like signal through the channel and measuring the delay caused by the channel. Then, during the system implementation, a cable with an appropriate length will be used to account for that delay in order for the LO signal used in the receiver mixer to be synchronized with the one at the transmitter.

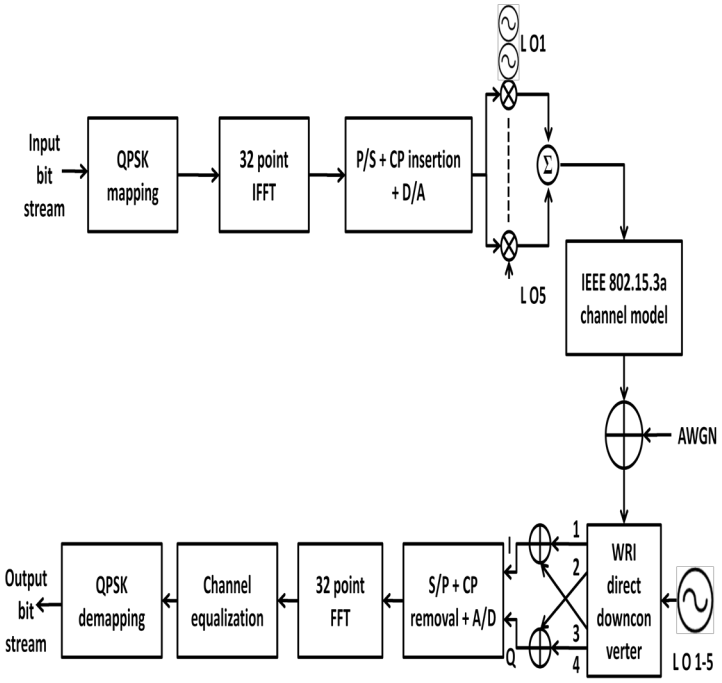

Figure 5-1: Block diagram of the OFDM-UWB test bench of the SISO transceiver.

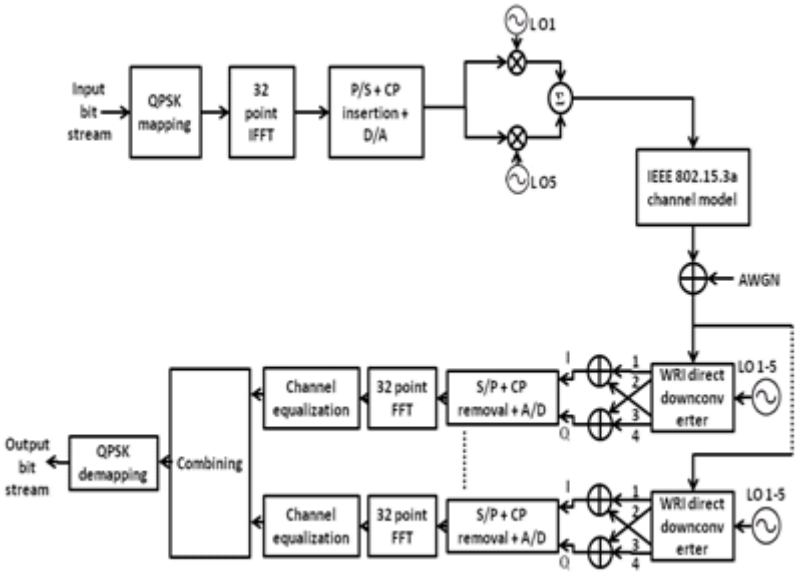

Figure 5-2: Block diagram of the OFDM-UWB test bench of the SIMO (1x2) transceiver.

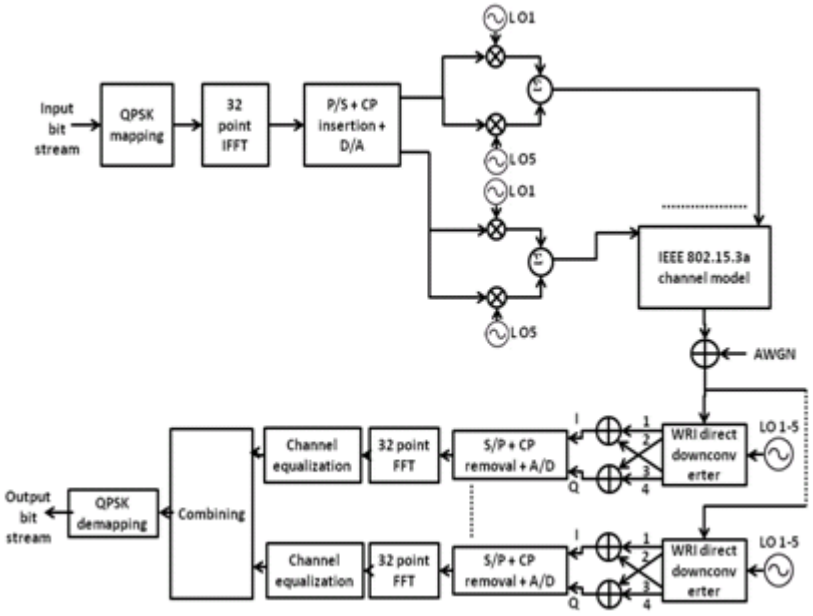

Figure 5-3: Block diagram of the OFDM-UWB test bench of the MIMO (2x2) transceiver.

In the test bench setups shown above all system components where implemented in baseband excluding the local oscillators, the following filters and the WRI circuit which are implemented in passband.

5.4 BER performance analysis

Assume a data sequence $\{c_{0,i}, c_{1,i}, \dots, c_{n,i}, \dots, c_{N-1,i}\}$ with the OFDM symbol index i and the subcarrier index n $(n = 0,1, \dots, N-1)$ as the input into the system, where N is the number of subcarriers. The transmitted symbols are assumed to be independent and identically distributed (i.i.d.) with a symbol energy E_s. With E_b representing the bit energy, two bits form a quadrature phase-shift keying (QPSK) symbol in the system; *i.e.,* $E_s = 2E_b$. Transmitted OFDM symbols are generated using a point inverse discrete Fourier transform (IDFT). The useful OFDM symbols with duration T_s are pre-appended by a cyclic prefix (actually zero-trailing) with duration T_C to mitigate Inter-symbol Interference (ISI) and appended by a guard interval with duration T_G to ensure a smooth transition between two consecutive OFDM symbols.

The output of the IDFT is given by [67]

$$x_i(\mathrm{t}) = \frac{1}{T_s} \sum_{n=0}^{N-1} c_{n,i}\ g(t - i\acute{T}_s\ )\ e^{((j2\pi n(t - i\acute{T}_s\ ))/T_s)} \qquad (5.1)$$

where $\acute{T}_s = T_c + T_s + T_G$ is the duration of the transmitted OFDM symbol, and $g(t)$ is the rectangular pulse. The transmitted signal $x(\mathrm{t}) = \sum_{i=-\infty}^{\infty} x_i(t)$ travels through UWB channel and the received signal $r(\mathrm{t})$ is the sum of the channel output, $y(\mathrm{t})$, and the additive white Gaussian noise (AWGN), $n(\mathrm{t})$

$$\mathrm{r(t)} = y(t) + n(t) = \sum_{i=-\infty}^{\infty} y_i(t) + n(t) \tag{5.2}$$

where

$$y_i(\mathrm{t}) = x_i(\mathrm{t}) * \mathrm{h(t)} = \frac{1}{T_s} \sum_{n=0}^{N-1} c_{n,i} \sum_{l=0}^{L} \sum_{k=0}^{K} \alpha_{k,l}\, \mathrm{g}(t - iT_S - T_l^{'} - \tau_{k,l}) \times$$

$$e^{((j2\pi n(t - iT_S - T_l - \acute{\tau}_{k,l}))/T_S)} \tag{5.3}$$

is the channel output corresponding to OFDM symbol $x_i(t)$, and $*$ denotes the convolution operation. The channel, the transmitted symbols, and the AWGN are assumed mutually independent.

The demodulated signal in the subcarrier m during the ith OFDM symbol period can be defined as

$$\hat{c}_{m,i} = \int_{i\acute{T}_s + T_c}^{i\acute{T}_s + T_c + T_S} r(t) e^{-j2\pi(f_{t,m})(t - i\acute{T}_s)}\, dt \tag{5.4}$$

where $f_{t,m}$ is the transmitter carrier frequency corresponding to the subcarrier m. By substituting (5.2) into (5.4), we have

$$\hat{c}_{m,i} = \int_{i\acute{T}_s + T_c}^{i\acute{T}_s + T_c + T_S} y_i(t)\, e^{((-j2\pi m(t - i\acute{T}_S))/T_S)} dt + \sum_{\iota \neq \imath} \int_{i\acute{T}_s + T_c}^{i\acute{T}_s + T_c + T_S} y_{\acute{\imath}}(\mathrm{t}) \times$$

$$e^{((-j2\pi m(t - i\acute{T}_S)/T_S)} dt + \int_{i\acute{T}_s + T_c}^{i\acute{T}_s + T_c + T_S} n(t)\, e^{((-j2\pi m(t - i\acute{T}_S)/T_S)} dt$$

$$\triangleq A_{m,i} + \hat{c}_{m,i}^{ISI} + n_{m,i} \tag{5.5}$$

where $A_{m,i}$ contains the useful information related to the ith OFDM symbol and the intercarrier interference (ICI), $\hat{c}_{m,i}^{ISI}$ results from the inter-symbol interference (ISI) from adjacent OFDM symbols, and $n_{m,i}$ is modelled as zero-mean complex Gaussian random variable with variance N_0.

In order to define an expression for the system BER, the variance of the fading, ICI and ISI terms in (5.5) must be defined [68].

In [69], the terms σ_H^2, σ_c^2, and σ_S^2 represent the variance terms of the fading, ICI and ISI, respectively are defined as a function of T_l^i, $\tau_{k,l}^{\ i}$ which are the arrival times in Poisson processes with rates Λ, λ and decay factors Γ, γ. Based on (5.5), those variances will be separated in terms of different values of Λ, λ, Γ, and γ which are dependent on each channel model.

Beside the fading and the interference terms, the received symbol is also affected by AWGN $n_{m,i}$ whose variance is N_0. Thus the average SNR per QPSK symbol can be defined as

$$\overline{\gamma_s} \triangleq \frac{E_s\,\sigma_H^2}{\sigma_C^2 + \sigma_S^2 + N_0}. \tag{5.6}$$

Since the energy per bit $E_b = (1/2)E_s$, the average SNR per bit is

$$\overline{\gamma_b} = \frac{1}{2}\overline{\gamma_s}. \tag{5.7}$$

Since the system employs QPSK modulation, the average BER, denoted as P_b, is determined through the average symbol error rate P_s as $P_b = P_s$, where P_s is determined by averaging symbol error rate over the fading statistics. Hence, we have

$$P_s(h) = Q\left(\sqrt{2\rho}\right) \tag{5.8}$$

where h is a vector representing the fading terms associated with $\hat{c}_{m,i}$, $Q(.)$ is the well-known Q-function, defined as $Q(x) = 1/\sqrt{2\pi}\int_x^\infty exp^{(-(t^2)/2)}\,dt$. In (5.8), ρ is defined as

$$\rho = \|h\|^2 \frac{E_b}{\sigma_Z^2} \tag{5.9}$$

where $\sigma_z^2 = \sigma_C^2 + \sigma_S^2 + N_0$ is the variance used in the average SNR expression, and $\|.\|$ is the Frobenius norm. The remaining task is to determine the probability density function (PDF) of the random variable ρ. The average symbol error rate then is given by [70], [71]

$$P_{s=} \int_0^\infty f_\rho(x) Q\left(\sqrt{2x}\right) dx. \tag{5.10}$$

Note that when ρ is a chi-square random variable with $2d$ degrees of freedom, its PDF is [71]

$$f_\rho(t) = \frac{1}{(d-1)!(\overline{\gamma_\rho})^d} t^{d-1} e^{-t/\overline{\gamma_\rho}}, \quad t \geq 0 \tag{5.11}$$

where $\overline{\gamma_\rho} = E[\rho]$ is the expectation of ρ. Thus the average symbol error rate is [5]

$$P_s = p^d \sum_{k=0}^{d-1} \binom{d-1+K}{K} (1-p)^k \tag{5.12}$$

where

$$p \triangleq \frac{1}{2}\left(1 - \sqrt{\frac{\overline{\gamma_\rho}}{1+\overline{\gamma_\rho}}}\right). \tag{5.13}$$

From [72], it has been shown that $\overline{\gamma_\rho} = \overline{\gamma_b}$ the average SNR per bit. Hence, from (5.10) and (5.11), the average BER reduces to

$$P_b = \frac{1}{2}\left(1 - \sqrt{\frac{\overline{\gamma_b}}{1+\overline{\gamma_b}}}\right). \tag{5.14}$$

5.5 Simulation and measurement results

The simulation and measurement results considered a 18dB range of signal-to-noise ratio (SNR). The IEEE802.15.3a standard channel parameters where chosen to emulate

the best vs. worst case scenarios of fading in an indoor environment (CM1 vs. CM4 in [73]). The worst case model represents an extreme non-line of sight (NLOS) multipath channel with 25 nsec RMS delay spread and 41 multipath components having values 10 dB below the power level of the strongest component. The considered modulation format is QPSK, where the total bandwidth of the pulse transmitted is 500 MHz and the rate of transmission is 80 MHz.

The BER performance of the OFDM-UWB transceiver is considered in IEEE802.15.3a channel models CM1 and CM4. The system considered a total bandwidth of 500 MHz. The duration of the useful OFDM symbol, and the cyclic prefix are 320 nsec, 80 nsec, respectively. The arrival rates Λ and λ and the decay factors Γ and γ of the cluster and ray, respectively, follow [74]. For the purpose of demonstration, the numerical results are obtained in the two extreme channels: CM1 and CM4.

Figure 5-4 illustrates the OFDM-UWB transceiver performance comparison between CM1 and CM4 using simulation, analysis and measurement results. As shown, the average BER increases as the severity of the channel increases; *i.e.*, CM1 is the least severe channel with the lowest average BER while CM4 is the most severe channel with the highest average BER when compared at the same SNR. Good agreement between simulation and analysis results obtained from equation (5.14) is observed.

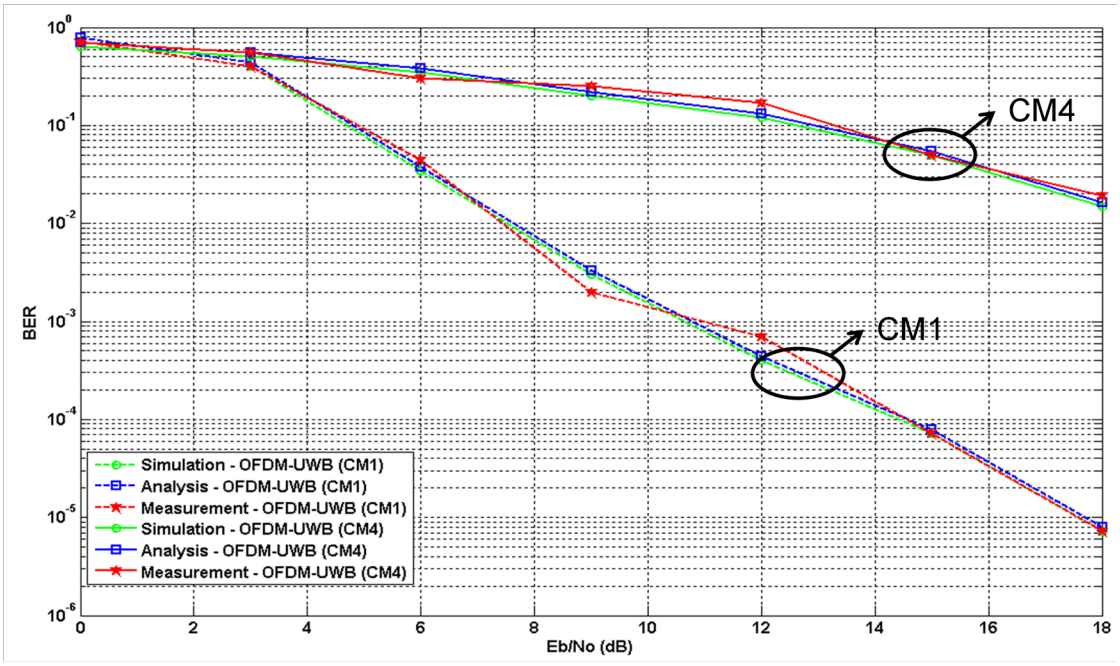

Figure 5-4: OFDM-UWB transceiver simulation, analysis and measurement results for CM1 and CM4.

In the following figures, the BER performance of the prescribed transceivers is verified by simulation and measurement results. As shown, Figure 5-5 and Figure 5-6 illustrate the obtained results for IR-UWB, OFDM-UWB transceivers for CM1 and CM4, respectively. BER performance gains resulting from the additional diversity and the enhanced energy captured are evident in the SIMO (1x2) and MIMO (2x2) systems compared to the transceiver in the SISO case. For example, considering CM1 of the OFDM-UWB transceiver at a BER of 10^{-5}, the MIMO system with 2 branches at the receiver outperforms its SIMO counterpart by about 3.2 dB. This is due to both, the diversity gain (frequency and time since combining is performed over five consecutive QPSK symbol periods), and the extra power gain in addition. Furthermore, those figures show that simulation and measurement curves follow the same diversity order with good agreement between them.

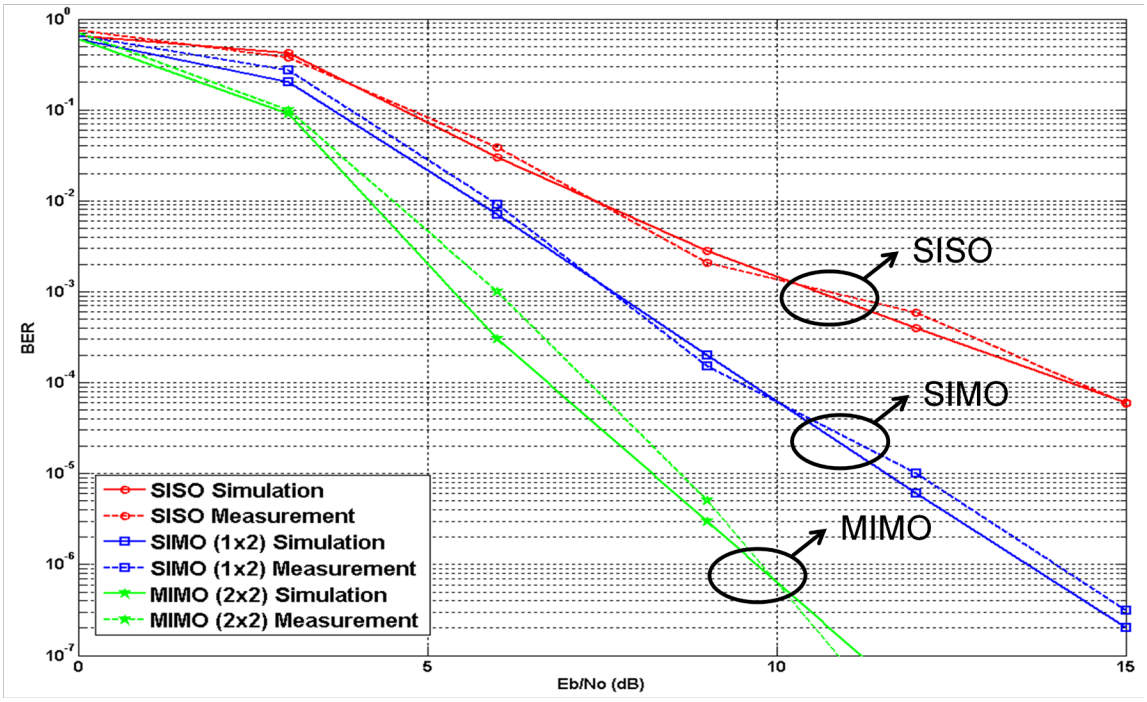

Figure 5-5: SISO, SIMO (1x2) and MIMO (2x2) BER simulation and measurement results of OFDM-UWB transceiver for CM1.

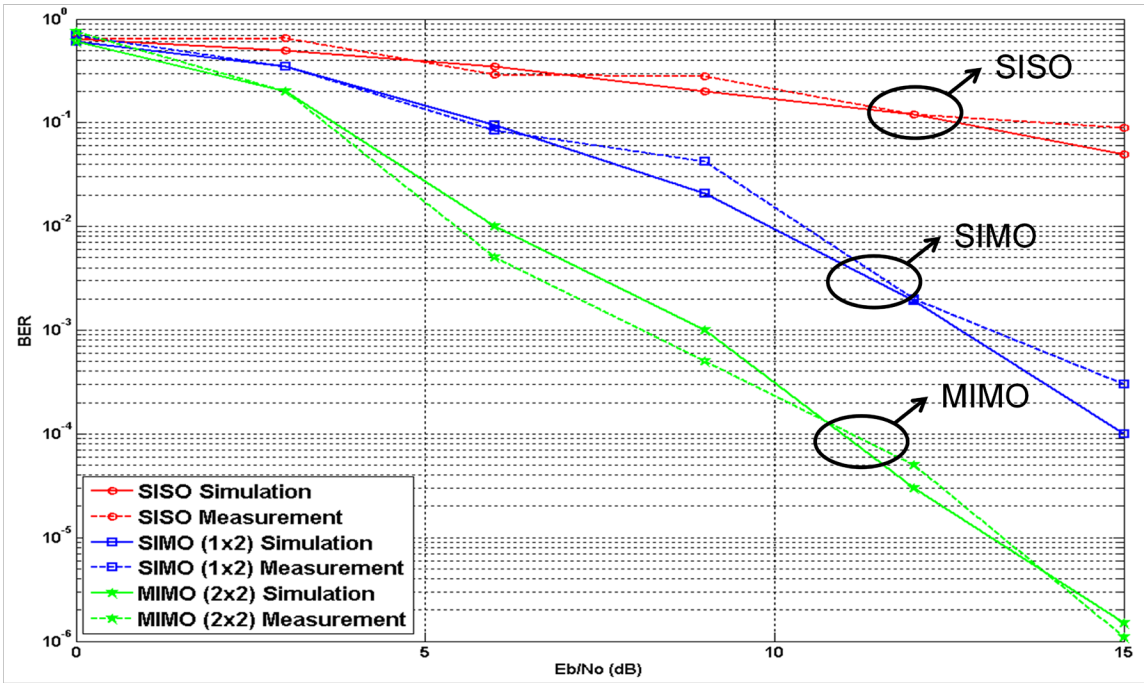

Figure 5-6: SISO, SIMO (1x2) and MIMO (2x2) BER simulation and measurement results of OFDM-UWB transceiver for CM4.

In those results, small discrepancy is encountered due to the imperfect synchronization, which may be compensated by employing stronger synchronization techniques. Some of these errors are due to measurements inaccuracy where we can observe some points of the measurements curves outperform analysis or simulations. In general, these points are within 1dB of an average represented by the simulation curve. Also, in Figure 5-7 and Figure 5-8 the performance of IR-UWB and OFDM-UWB transceivers is compared for CM1 and CM4 with different configurations of transmit and receive antenna numbers. Both figures indicate that OFDM-UWB transceiver outperforms the IR-UWB counterpart with an average of 2dB [76]. This difference is a direct result of using OFDM modulation which provides strong immunity against multipath fading in this highly scattering channel.

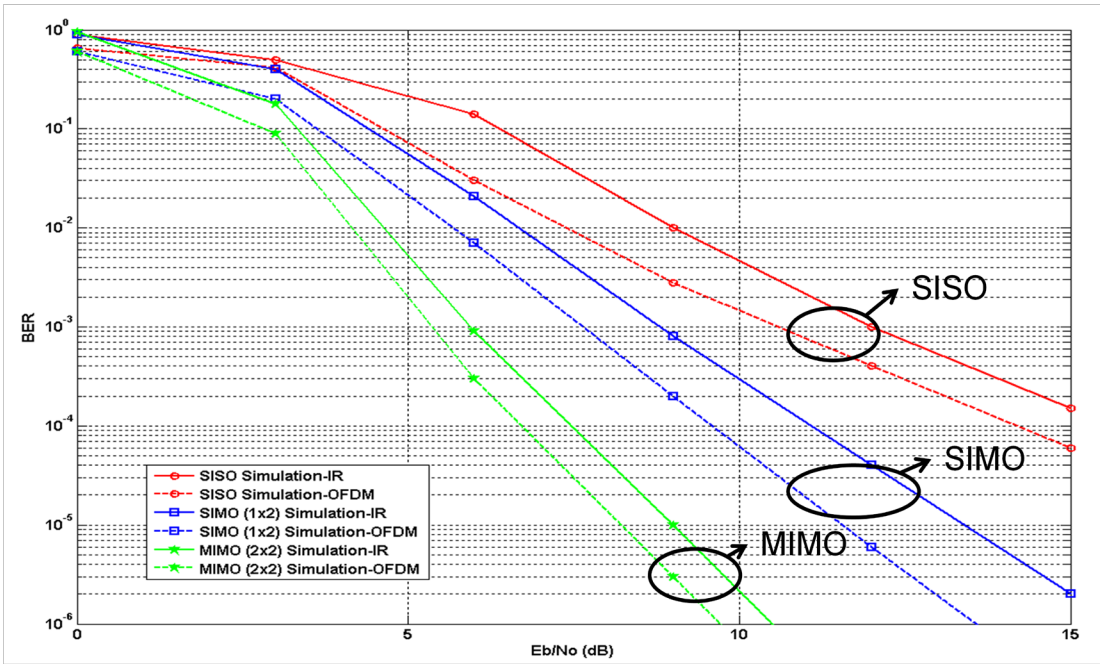

Figure 5-7: SISO, SIMO (1x2) and MIMO (2x2) BER simulation and measurement results of IR-UWB and OFDM-UWB transceivers for CM1.

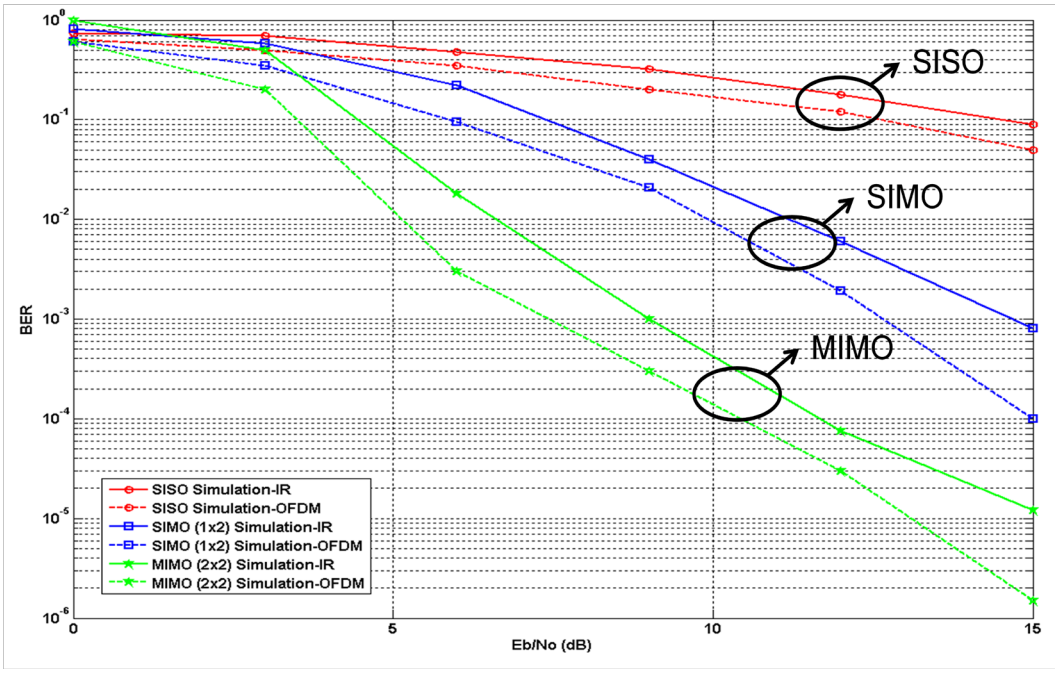

Figure 5-8: SISO, SIMO (1x2) and MIMO (2x2) BER simulation and measurement results of IR-UWB and OFDM-UWB transceivers for CM4.

Furthermore, in order to have more realistic perspective of the transceiver performance, amplitude and phase imbalances of ±0.5dB and ±9^{o} [77] are considered in this study, respectively. An I-Q impairment analysis was performed by sweeping the amplitude imbalance between -0.5 to 0.5 dB and the phase imbalance between -9^{o} to 9^{o}. The impaired I-Q channels are compared with the ideal ones obtained from simulations in Figure 5-5 and Figure 5-6 for CM1 of the OFDM-UWB test bench. As seen in Figure 5-9, OFDM-UWB system exhibits a maximum loss of 2.7dB. This is due to OFDM subcarriers high sensitivity for phase imbalances. This can be overcome by an optimization process to minimize the phase imbalance of the designed transceiver circuit [78].

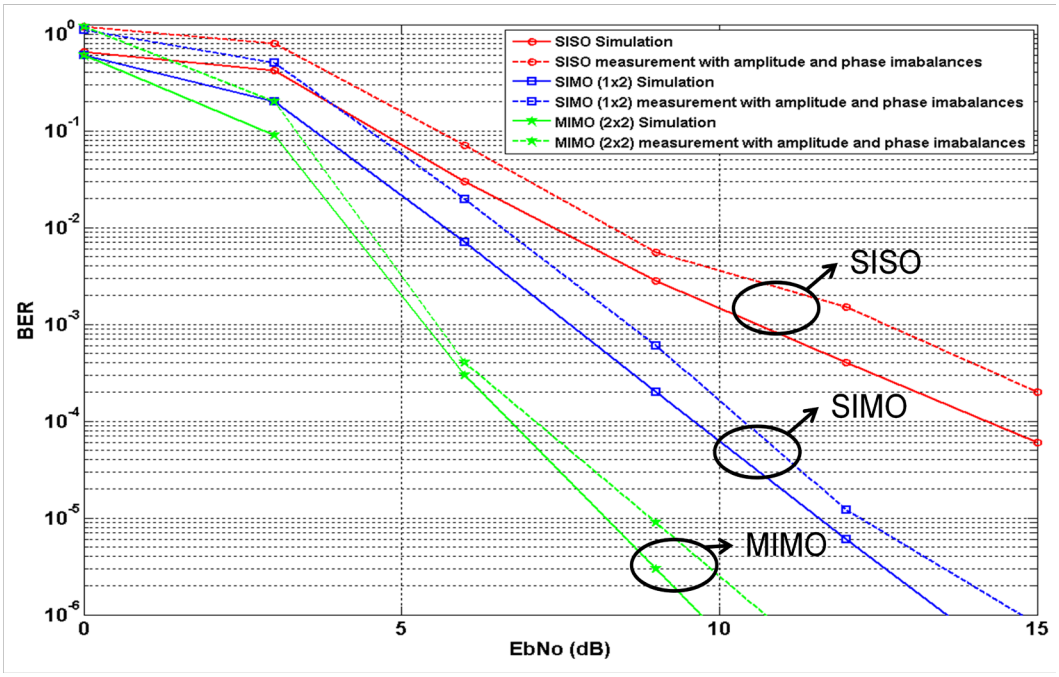

Figure 5-9: SISO, SIMO (1x2) and MIMO (2x2) BER results of OFDM-UWB transceiver for the ideal case and with amplitude and phase imbalances for CM1.

By comparing the obtained results with the ones reported in [79] for an MB-OFDM system of a conventional UWB transmitter and receiver system, big similarities are observed. Considering the results of the uncoded system, in small SNR values, system results for CM1 and CM4 are almost the same. However, in high SNR values the BER results of CM4 is worst compared to CM1 by around 1.5dB.

5.6 Comparison between UWB systems

In this section, the implemented IR-UWB and OFDM-UWB systems are compared with other conventional UWB systems from a more qualitative viewpoint.

- As for transceiver architectures, other UWB systems usually include a circuit controlling timing or shape (depends on modulation scheme) at transmitter end

and a correlation circuit at the receiver end. The implemented transceivers adopt a quasi-symmetric architecture (using WRI circuits for both modulation and demodulation).

- The new fabricated WRI circuit provides the means to realize both transmit and receive operations within the same transceiver node. Hence, the work in this thesis provides a benchmark for a self-reliant transceiver prototype that can be utilized for communication or positioning purposes.
- A common UWB receiver is based on a correlation circuit which consists of a multiplier and an integrator [75]. The single output from the correlation circuit is then used for bit detection. In the implemented test benches, the wide-band WRI circuit combined with DSP techniques equivalently realizes the correlation function. Its four output signals make subsequent signal processing easier. The complexity of more outputs is also traded off by realizing both UWB communication and positioning functions on a single hardware [76].

5.7 Conclusion

This chapter introduced the first implementation of an OFDM-UWB WRI transceiver, where different configurations of transmit and receive antennas for the transceiver test bench were considered. The concept of operating the transceiver as one node capable of performing modulation and demodulation functions using OFDM modulation is presented. Following that, an expression for the BER of the transceiver is verified against different UWB channel models. Then, system simulation and measurement parameters used are described, with emphasis on testing equipment limitations. Analysis,

simulation and measurement results for different number of transmit and receive antennas demonstrate that OFDM-UWB outperforms IR-UWB by 2dB considering the ideal scenario. However, when considering amplitude and phase imbalances, the reverse's encountered due to OFDM subcarriers high sensitivity to phase jitter.

CHAPTER 6 CONCLUSIONS AND FUTURE WORK

6.1 Conclusion

A double layer wave-radio interferometer (WRI) circuit has been exploited as a direct down-converter in an IR-UWB and OFDM-UWB transceiver over a realistic UWB channel. Different number of transmit and receive antennas for the proposed transceivers are considered to verify its BER performance. Also, best vs. worst case scenarios were studied by employing IEEE802.15.3a standard CM1 and CM4 to emulate the fading channel. A Good agreement is observed between obtained simulation and measurement results of the implemented transceivers.

By comparing IR-UWB and OFDM-UWB modulation schemes, it is observed that the later provides an average 2dB SNR enhancement for the same BER. Also, the results show BER performance improvement with the use of an extra branch at the receiver, due to joint diversity and power gains. However, OFDM-UWB modulation shows less immunity to amplitude and phase imbalances when compared to its IR-UWB counterpart. An average SNR loss of 2.7dB is encountered for OFDM-UWB transceiver as a result of subcarriers sensitivity to abrupt phase changes.

Also, an analytical framework for the BER performance of both OFDM-UWB and IR-UWB WRI-based transceivers is presented over IEEE802.15.3a indoor wireless channel. This frame work is based on proposing convenient approximating distributions for the energy captured over these channels. The proposed approximations result in simple pdf expressions with acceptable levels of accuracy over the entire range of parameters. These approximations are useful in evaluating the BER performance and

they capture the diversity orders that can be achieved over the IEEE 802.15.3a channel model. The analysis also provides an insightful understanding of the system performance in the standard channel model considering best and worst scenarios (CM1 and CM4). Furthermore, a brief comparison with other UWB systems was also given.

In addition, this work demonstrates the benefit of utilizing WRI based transceivers. Those transceivers possess the advantage of having simpler architecture compared to traditional ones. Furthermore, their passive mixing and relatively low fabrication cost features make them an ideal candidate for WPAN transceivers front end design.

Major contributions are summarized as follows:

- For the proposed carrierless UWB system, we introduce a design and implementation of a dual-layer fully fabricated WRI circuit in the lab.
- The newly fabricated WRI circuit combines both functions of modulation and demodulation on the same circuit, which translates to lower cost and size.
- The new WRI circuit has a dynamic range that extends to approximately double the dynamic range of the prior design due to the use of log-power detectors.
- First time implementation for an OFDM-UWB system in an AWGN and emulated wireless channel with WRI circuit utilized for direct downconversion.
- First time implementation considering a realistic UWB channel based on IEEE802.15.3a channel model with a receiver using WRI circuit for direct downconversion.
- First time simulation and implementation for different variants of

transmit/receive configurations of the transceiver; *i.e.*, SISO, SIMO and MIMO using WRI-based transceiver.

- Provided a simplified analysis framework to benchmark obtained simulation and measurement results.
- Simplified synchronization method based on WRI circuit output signals has been implemented.

6.2 Future Work

Due to time limitations, in the future, and in order to realize the fabrication of the transceiver node, the fabricated double-layer WRI circuit, DSP demodulation techniques can be designed using a suitable integrated circuit method to be integrated on a small size chip. An improved synchronization algorithm for the developed platform can also be realized. Further, the potential capability of realizing both UWB communication and positioning functions using a single transceiver node can be further studied. The anticipated transceiver node performance can be investigated through other UWB standard channels such as IEEE802.15.4a developed for ultra-low power wireless sensors. Finally, an investigation of the IR-UWB and OFDM-UWB transceivers performance using antennas should be conducted since no simulation, measurement or analysis studies in this work considered that scenario.

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