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MINIATURIZATION TECHNIQUES OF SUBSTRATE INTEGRATED WAVEGUIDE BASED ON MULTILAYERED PRINTED CIRCUIT BOARD PLATFORM

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DÉDICACE

To my parents
To Guangyu

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RESUMÉ

Le guide d'ondes intégrées au substrat (GIS) est une structure à ondes guidées qui présente des avantages avec un facteur de qualité Q élevé et une excellente isolation ligne à ligne. La technique GIS a été largement utilisé dans la construction de composants passifs, tels que coupleurs, diviseurs, filtres, et déphaseurs. Certains dispositifs actifs ont également été développés avec facteur Q élevé et résonateurs en technologie GIS. En comparant à d'autres types de lignes de transmission planaire, le facteur de qualité Q important du GIS est une embouchure pour son intégration avec d'autres circuits classiques. Les techniques de miniaturisation du SIW sont donc devenues une urgence.

Le travail dans cette thèse commence par l'examen et la discussion des techniques de miniaturisation existantes pour GIS, y compris les (ridge substrate integrated waveguide, RSIW), intégrés sur substrat à demi-mode (HMSIW) et les (folded substrata integrated waveguide, FSIW). L'impédance et la constante de propagation des lignes basées sur ces techniques de miniaturisation sont calculées en utilisant la méthode de résonance transversale (transverse resonant method, CRT). Bien que ces paramètres puissent être obtenus par des méthodes de simulation EM, un calcul rapide sera utile pour l'optimisation de la conception en utilisant l'analyse paramétrique. Une préoccupation particulière est axée sur la relation entre la constant d'atténuation et les paramètres géométriques. Les dimensions optimisées de chaque GIS miniaturisés sont proposés en se basant sur l'analyse paramétrique. Les paramètres de transmission de ces lignes de SIW miniaturisés peuvent être extraire en utilisant la méthode à double ligne.

Sauf HMSIW, toutes les autres techniques de miniaturisation mentionnées ci-dessus pour la mise en œuvre de la plateforme multicouche. Parmi les techniques de fabrication diverses qui sont en mesure de fournir des substrats multicouches, le circuit imprimé multicouche est utilisé dans la conception des circuits rapportés dans cette thèse. On croit que les avantages du circuit GIS sont importants dans les applications à ondes millimétriques, bien que la conception pourrait limiter la fréquence de fonctionnement. Plus précisément, le substrat Rogers R6002 est utilisé dans toutes nos conceptions pour prouver les concepts étudiés dans ce travail. Une étape

principale pour l'utilisation de la technologie GIS est de développer des transitions à haute performance et des interconnexions entre les circuits intégrés sur substrat, d'autres types de lignes de transmission, d'autres circuits intégrés ou les monter en surface sur des substrats multicouches. Dans ce travail, une nouvelle transition entre une ligne micro-ruban et le GIS dans un environnement de conception sur substrat multicouche est présenté. Afin d'obtenir une réponse large bande et à faible perte, la transition est composé d'un GIS coniques et une ligne micro-ruban fuselé, modélisé et conçu en tenant compte à la fois d'adaptation d'impédance et du champ. L'impédance caractéristique et la longueur d'onde guidée calculée en utilisant des formes fermée basée sur une méthode transversale de résonance et aussi sont utilisés pour développer notre procédure de conception. La large bande passante effective est obtenue en deux exemples développés dans ce travail, qui sont validés par les résultats simulés et mesurés. Trois autre transitions, y compris une transition micro-ruban à GIS, une transition TFSIW-à-SIW et une transition SIW-à GIS, sont conçus sur un substrat en deux couches et ont une bonne corrélation entre la simulation et la mesure.

Plusieurs composants passifs sont conçus et fabriqués en utilisant les techniques de miniaturisation mentionnés ci-dessus et les transitions proposées. Une procédure de conception d'un anneau hybride TFSIW est présentée et discutée en référence aux paramètres calculés des lignes de transmission TFSIW en utilisant TRM. La bande passante par rapport à la perte de retour pour les quatre ports et l'isolation entre les ports isolés est de 12,7%, inférieur à -20 dB. La perte d'insertion et de la différence de phase sont -3,7 dB et 1800 ± 30, respectivement, à la fréquence centrale. Deux circuits à jonction six ports basé sur la technique HMSIW sont proposés et mis en œuvre sur une bande de fréquence de 22 GHz à 26 GHz. Deux jonctions à cinq ports sont conçues sur la base technique de TFSIW à la fréquence centrale de 26 GHz. Les deux utilisent deux jonctions de couplage dans le plan H. Encore une conception compacte a atteint 23% de bande passante à la discordance résiduelle inférieure à -20 dB et une autre conception à une bande passante plus large que 43% en ajoutant une transition conique.

Le GIS donne une très bonne solution pour intégrer une antenne réseau de guide d'ondes à fente et son réseau d'alimentation dans un substrat planaire. Cette structure hautement intégré et compact peut non seulement réduire la taille du système entier, mais aussi améliorer le rendement du système. Cependant ce type d'antenne est connu avec une bande de fréquence très limitée, ce qui devient encore plus grave dans la conception basée sur GIS en raison de sa hauteur réduite du

guide d'ondes. Il a été constaté que certaines structures GIS miniaturisé peuvent non seulement réduire la taille du circuit, mais aussi améliorer quelques fonctionnalités, telles que la l'impédance et la bande passante. Un réseau d'antenne 4 × 4 basé avec la technique RSIW est proposé avec une bande passante de 8,8% facilement réalisable. Avec le réseau d'antenne à slot 2 × 4 proposé TFSIW large fente, la taille de l'antenne est réduite de 40% et l'impédance la bande passante (-10 dB) est de 5,6%. Plusieurs réseaux RSIW sont conçus avec des réseaux d'alimentations différentes, fabriqué sur un substrat Rogers de deux couches et comparées avec les spécifications, telles que le gain à haut débit, diagramme de rayonnement et la perte d'isertion. Un meilleur design parmi ces réseaux d'antennes intégré à un duplexeur GIS dont les centres de deux bandes de passage sont de 25,5 GHz et 26,5 GHz respectivement. Une expérience est menée avec une paire d'antenne de réception qui est placés sur le plan de polarisation croisée pour tester le facteur de perte à polarisation croisée.

Afin d'accélérer l'utilisation de la technique GIS pour plus application, nous étudions l'accordabilité du GIS chargé avec des diodes semi-conductrices sur le dessus. Le déphaseur accordable est un appareil micro-ondes important pour des nombreuses applications. Les dispositifs semi-conducteurs sont souvent utilisés dans des circuits planaires pour changer la phase et / ou l'amplitude d'un signal RF qui les traversent. Dans ce travail, nous présentons deux plates-formes de conception de déphaseur GIS à 26 GHz, à savoir un déphaseur en ligne et un déphaseur de réflexion, pour le réglage de la phase du GIS en continu et en numérique, respectivement. Les diodes sont chargées sur le dessus du GIS par quelques fentes transversales ouvertes sur le mur large du GIS. La plage d'accord, la phase et l'amplitude des deux déphaseurs en ligne de type SIW et la réflexion sont étudiées grâce à la corrélation entre la simulation et de mesure. Les résultats mesurés sont en accord avec les réponses calculées à partir des modèles équivalents et les modèles EM. Un déphaseur mis au point par un unique varactor à un déphasage de plus de 25 ° sur une bande passante de 30%. La variation de déphasage est inférieure à 2,2 ° sur la bande. Le déphaseur de 180 ° de type réflexion a un décalage de phase mesurée supérieure à 180 ° sur une bande passante de 13% et la variation de la perte d'insertion est -3,8 ± 0,87 dB dans une bande passante de 15,3%.Un levier de 360 ° en phase est conçue en cascade avec deux déphaseurs à 180 °. Le déphaseur de phase à 360 ° est utilisée comme un modulateur de phase dont le contrôle de la tension du signal est générée à partir d'une entrée I / Q.

Le récepteur multiport à conversion directe est une solution prometteuse pour les applications de MMW. Beaucoup d'architectures ont été proposées pour la construction des composants clés du récepteur à une jonction six ports ou cinq ports. Une simulation numérique est précédée pour étudier l'impact des terminaux non-idéal pour la phase et l'amplitude du récepteur de six ports. Basé sur la conclusion tirée de cette étude, un six ports GIS à jonction est composé de quatre coupleurs 3dB est construit dans un substrat Rogers à une seule couche. Un système émetteur-récepteur est proposé des dispositifs proposés et conçu dans ce travail, y compris :

- Un modulateur de phase qui est contrôlé par une séquence de tension d'entrée converti du signal I / Q;

- Deux antennes RSIW large fente, avec l'un est placé sur le plan de polarisation croisée de l'autre;

- Un duplexeur GIS et un BPF GIS;

- Une jonction de six ports dont les quatre sorties sont connectées avec des détecteurs de puissance RF et les circuits décodeur analogique;

- Un groupe d'emballage des circuits intégrés qui sont montés en surface sur le substrat et connecté avec SICs par guide d'ondes coplanaires à la masse (GCPW).

Simulations ADS en enveloppe de l'émetteur-récepteur proposées sont réalisées avec des modèles de différents niveaux, en commençant par les modèles des composants idéaux fournis dans l'ADS et enfin remplacer les modèles idéaux par d'autres plus réalistes obtenus dans les simulations et les mesures EM.

ABSTRACT

Substrate integrated waveguide (SIW) is a guided-wave structure that enjoys the benefits of a high quality factor (Q) and an excellent line-to-line isolation. SIW technique has been widely used in building passive components, such as couplers, dividers, filters, and phase shifters. Some active devices have also been developed with high Q SIW resonators. Comparing to other types of planar transmission lines, the big form factor of SIW is a bottleneck for its integration with other conventional integrated circuits. Miniaturization techniques for SIW therefore become very urgent.

The work in this dissertation starts with reviews and discussions of existing miniaturization techniques for SIW, including ridge substrate integrated waveguide (RSIW), half-mode substrate integrated waveguide (HMSIW) and folded substrata integrated waveguide (FSIW). The impedance and propagation constant of the transmission lines based on these miniaturization techniques are calculated using transverse resonant method (TRM). Although these parameters can be extracted from full wave electromagnetic (EM) simulations, a fast computation would be helpful in the design and optimization by using parametric analysis. One particular concern focuses on the relationship between attenuation constant and geometric parameters. Optimized dimensions of each miniaturized SIW are suggested based on the parametric analysis. The transmission line parameters of these miniaturized SIW transmission lines can be extracted from experiments using dual-line method.

Except HMSIW, all other miniaturized techniques mentioned above need multilayer platform for implementation. Among various fabrication techniques which are able to provide multilayered substrate, low-cost multilayer printed circuit board (PCB) is used in the design of the circuits reported in this dissertation. It is believed that the advantages of SIW circuits are important in millimeter wave applications, although the design might limit the operating frequency. Specifically, Rogers substrate R6002 is used in all our designs for proving the concepts investigated in this work. One principal step for using the SIW technology is to develop high-performance transitions and interconnects between substrate integrated circuits (SICs) and other types of transmission lines or circuits embedded in or surface mounted on the multilayer substrates. In this work, a novel transition between a microstrip line and an SIW in a multilayer substrate design environment is presented. In order to achieve a low-loss broadband response, the transition, consisting of a tapered or multi-sectional ridged SIW and a tapered microstrip line, is modeled and designed by considering both impedance matching and field matching. Characteristic impedance and guided wavelength calculated by using closed-form expressions based on a TRM are used to develop design procedures.

Effective broad bandwidth is obtained in two examples developed in this work, which are validated with simulated and measured results. Another three more transitions, including a microstrip-to-SIW transition, a TFSIW-to-SIW transition and an SIW-to-SIW transition, are designed in a two-layer substrate and have good correlation between the simulations and measurements.

Several passive components are designed and fabricated utilizing the miniaturization techniques mentioned above and the proposed transitions. A design procedure of a T-type folded substrata integrated waveguide (TFSIW) hybrid ring is presented and discussed with reference to the calculated parameters of TFSIW transmission lines using TRM. The bandwidth with reference to the return loss at all four ports and isolation between isolated ports is 12.7%, less than -20 dB. The insertion loss and phase difference are -3.7 dB and $180° \pm 3°$, respectively, at the center frequency. Two six-port junction circuits based on the HMSIW technique are proposed and implemented over a frequency band from 22 GHz to 26 GHz. Two five-port junctions are designed based on TFSIW technique with the center frequency of 26 GHz. Both junctions make use of coupling in H-plane. One more compact design has achieved 23% bandwidth with residual mismatch less than -20 dB and another design has a bandwidth as wide as 43% by adding a tapered transition .

SIW provides a very good solution to integrate a waveguide slot array antenna and its feeding network in a planar substrate. This highly integrated and compact structure can not only reduce the whole system size but also enhance the system yield. However, this type of antenna is known for suffering from a very limited frequency bandwidth, which becomes even more serious in SIW-based design because of its reduced waveguide height. It was found that some miniaturized SIW structures can not only reduce the size of the circuit but also have some features improved, such as impedance bandwidth. A 4×4 slot array antenna based on RSIW technique is proposed and an 8.8% bandwidth is easily achieved. With the proposed 2×4 TFSIW slot array antenna, the size of the antenna is reduced by 40% and the impedance bandwidth (-10 dB) is 5.6%. Several RSIW arrays are designed with different feeding networks, fabricated in a two-layer Rogers substrate and compared with specifications, such as broadband gain, radiation pattern and return loss. The best design among these array antennas is integrated with an SIW diplexer whose centers of two passing bands are 25.5 GHz and 26.5 GHz, respectively. An experiment is conducted with a pair of receiving antennas which are placed on the cross-polarized plane to each other for testing the cross-polarization loss factor.

In order to accelerate the usage of SIW technique into more applications, we study the tunability of SIW loaded with semiconductor diodes on the top. Tunable phase shifter is an important microwave device in many applications. Semiconductor devices are often used

in planar circuits to change the phase and/or amplitude of a radio frequency (RF) signal passing through them. In this work, we present two design platforms of SIW phase shifter at 26 GHz, namely an inline phase shifter and a reflection-type phase shifter, for tuning the phase of SIW continuously and digitally, respectively. The diodes are loaded on top of the SIW through some transverse slots opened on the broad wall of the SIW. The tuning range, phase and magnitude imbalance of both inline SIW phase shifter and reflection type SIW short termination are investigated through the correlation between the simulation and measurement. Measured results are in agreement with responses calculated from equivalent models and EM models. An inline phase shifter tuned by single varactor has a phase shift larger than 25° over a 30% bandwidth. The variation of phase shift is less than 2.2° within the band. The 180° reflection-type phase shifter has a measured phase shift more than 180° over a bandwidth of 13% and the variation of insertion loss is -3.8 ± 0.87 dB within a bandwidth of 15.3%. A 360° phase shifter is designed by cascading two proposed 180° phase shifters. The 360° phase shifter is used as a phase modulator whose control voltage is generated by an analog encoder circuit and an input I/Q signal.

Multiport direct conversion receiver is a promising solution for millimeter-wave applications. Many architectures have been proposed for building the key component of the receiver, a six-port or five-port junction. A numerical simulation is proceeded for studying the impact of the non-ideal terminations to the phase and magnitude imbalance of the six-port receiver. Based on the conclusion drawn from this investigation, an SIW six-port junction that is composed of four 3 dB couplers is built in a single layer Rogers substrate. A transceiver system is proposed using all devices introduced and designed in this work, including

- A phase modulator that is controlled by a sequence of voltage converted from input I/Q signal;
- Two RSIW slot array antennas, with one is placed on the cross-polarized plane of the other;
- An SIW diplexer and an SIW band pass filter;
- A six-port junction whose four outputs are connected with RF power detectors and analog decoder circuits;
- A group of packaged integrated circuits which are surface mounted on the substrate and connected with surrounding SICs through grounded coplanar waveguide (GCPW).

Advanced Design System (ADS) envelop simulations of the proposed transceiver are performed with models of different levels, starting with the ideal component models provided in ADS and finally replacing the ideal models with more realistic ones obtained in EM simulations and measurements.

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BER	Bit Error Rate
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CFSIW	C-Type Folded Substrate Integrated Waveguide
CMOS	Complementary Metal Oxide Semiconductor
CPS	Coplanar Strip
CPW	Coplanar Waveguide
DAC	Data Access Component
EBG	Electromagnetic Band Gap
EME	Electric-Magnetic-Electric
ESD	Electrostatic Discharge
FDD	Frequency Domain-defined Device
FDTD	Finite-Difference Time-Domain
FEM	Finite Element Method
FMCW	Frequency Modulation Continuous Wave
FSIW	Folded Substrate Integrated Waveguide
FSS	Frequency Selective Surface
GCPW	Grounded Coplanar Waveguide
HMSIW	Half-Mode Substrate Integrated Waveguide
IF	Intermediate Frequencies
LHM	Left-Handed Medium
LO	Local Oscillator
LTCC	Low Temperature Co-Fired Ceramic
MEMS	Micro Electro Mechanical Systems
MHMIC	Monolithic Hybrid Microwave Integrated Circuit
MIC	Microwave Integrated Circuit
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
mmW	Millimeter-Wave
MOM	Metal-Oxide-Metal
MOM	Method of Moments
mW	Microwave

PA	Power Amplifier
PBG	Photonic Band Gap
PCB	Printed Circuit Board
PEC	Perfect Electric Conductor
PLF	Polarization Loss Factor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RSIW	Ridge Substrate Integrated Waveguide
SDR	Software Defined Radio
SIC	Substrate Integrated Circuit
SiP	System In Package
SIW	Substrate Integrated Waveguide
SoC	System On Chip
SOLT	Short Open Load Through
SPN	Six-Port Network
SR	Spiral Resonator
SRR	Split Ring Resonator
SWF	Slow-Wave Factor
TEM	Transverse Electromagnetic
TFSIW	T-Type Folded Substrate Integrated Waveguide
TLM	Transmission Line Matrix
TRL	Through Reflect Line
TRM	Transverse Resonant Method
TSV	Through Silicon Via
TWV	Through Wafer Via
UWB	Ultra-Wide Band
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer

CHAPITRE 1

Introduction

With the increasing technical and performance requirement on wireless systems for communication and sensor applications, high-density microwave (mW) and millimeter-wave (mmW) system integration techniques have been under intensive development. Generally, a high-performance system involves high-quality analog passive components, active devices and even digital parts. A number of hybrid integrated circuit design concepts have been proposed to enhance the integration at system level. The performance of the guided-wave structures is crucial for the designs of critical mmW and sub-millimeter wave systems, subsystems and devices such as power amplifiers (PAs), filters, phased antenna arrays and low noise amplifiers. Because the microstrip line exhibits extremely low quality factor (Q-factor) and poor line-to-line isolation in mmW applications, existing millimeter wave integrated circuit technologies rely heavily on slotline, coplanar strip (CPS) and coplanar waveguide (CPW) transmission line components. However, these transmission lines still suffer from some limitations, especially for future millimeter and submillimeter applications. Problems can be summarized as follows.

- It is difficult to accurately model these lines because of the leakage radiation, surface wave propagation and box mode-coupling. Some unwanted propagation modes can be excited.
- These lines suffer from a poor Q-factor which can limit the performance of related subsystems, such as reducing selectivity of filters, increasing insertion loss and higher heat dissipation and noise temperature.
- A poor line-to-line isolation gives a low directivity to directional couplers. A high cross-talk increases the interaction between devices. Coupling between on-wafer calibration standards increases measurement uncertainty.
- Low package density results in larger chip size and more chip costs.

It is well known that non-planar components have lower loss and thus higher Q against their planar counterparts. A hybrid approach that integrates both planar and non-planar circuits within a single platform is attractive for a compact and high-performance design. However, transitions from nonplanar circuits to planar ones are rather complicated especially when the operating frequency goes to mmW band or even higher. Rectangular waveguides are commonly used in low-loss microwave and mmW circuit designs. Metallic rectangular wave-

guides have much lower current densities, compared to conventional slotlines, CPS and CPW lines. Moreover, because the propagating fields are contained within an enclosed structure, there is no leakage of electromagnetic energy. As a result, this type of guided-wave structure enjoys the benefits of having a high Q-factor and excellent line-to-line isolation. Substrate integrated waveguide (SIWs), also known as laminated waveguide or post-wall waveguide, have been therefore proposed and investigated from 1990s, theoretically and practically. An SIW is a type of rectangular waveguide synthesized in a substrate, which is composed of two rows of metallized via-holes or grooves connected with two metal plates on the top and bottom sides. The operating mechanism of an SIW is quite similar to a classic rectangular waveguide. The Q-factor of an SIW is smaller than a classic air-filled metal rectangular waveguide because of the dielectric filling and volume reduction. In the past decade, the advanced SIW technology has attracted much attention from the researchers all over the world. A brief review of SIW technique in the aspect of analysis methods, passive and active components and antenna designs is given below,

Till now, very few numerical methods were developed and published for SIW structures to achieve a high computational efficiency. A hybrid method that combines method of moments (MOM) and cylindrical eigenfunction expansion was presented by Wu et Kishk (2008). A boundary integral-resonant mode expansion (BI-RME) method was applied by Bozzi *et al.* (2006) for the analysis of lossless SIW. This algorithm was improved by Bozzi *et al.* (2008) for the modeling of lossy SIW interconnects and components. Although these algorithms have high efficiencies in analyzing some specific problems, most analysis of SICs is usually performed in full wave electromagnetic (EM) simulation softwares, such as Ansoft High Frequency Structure Simulator (HFSS) and Computer Simulation Technology (CST) which use finite element method (FEM) and finite-difference time-domain (FDTD) method, respectively. EM analysis of all designs presented in this work is conducted by Ansoft HFSS.

The most basic and important SICs are passive devices such as filters, phase shifters, power dividers, directional couplers, hybrids, multiport junctions and coupling matrix. The Y- and T- type SIW junctions or power dividers were firstly proposed by Germain *et al.* (2003). Some designs were reported for achieving a high isolation between two outputs by adding resistors either using Wilkinson concept (Zhang et Wu (2008)) or magic Tee concept (Sarhadi et Shahabadi (2010)). By cascading directional couplers and power splitters (Moldovan *et al.* (2006)), the inputs and outputs of a multiport junction (or power divider) are kept in a single substrate layer. Another low-loss solution of multiport power divider was achieved by using a center-fed probe and a current probe array distributed in a radial cavity as input and outputs, respectively, (Song *et al.* (2008)). The coupling in a 3-dB SIW coupler can be implemented through a window on the shared narrow wall in a single-layer design (Liu *et al.*

(2005)) or an opening on the shared broad wall in a multilayer platform. Other types of couplers included an SIW hybrid ring (Che *et al.* (2006)) and a magic Tee (He *et al.* (2010)) which is a hybrid circuit composed of both SIW and other planar lines. The phase of an SIW can be constantly shifted by adjusting the physical broadside dimension, such as shifting the location of the synthesized sidewall (Cheng *et al.* (2007)), or changing the equivalent broad wall width by using composite right/left handed structure (Ali *et al.* (2009)). Tunable phase shifter is getting more and more attractive because of its application in phased array antenna where the phase of the transmission path needs to be continuously changed. The tunability on phase of an SIW can be achieved either by filling SIW with a tunable material, such as ferrite (Bray et Roy (2004)), or loading SIW with voltage controllable semiconductor components (Sbarra *et al.* (2009)). Filter is an important component in passive category. The same as the standard metallic waveguide filter, the coupling between cavities is usually implemented by inserted metal posts, iris on the sidewall or opening on the top wall. Several miniaturization techniques for SIW filter design have been proposed by using complementary split ring resonator (Zhang *et al.* (2010)) or manipulating the SIW cross section in a multilayer platform (Wu *et al.* (2010b)). SIW resonators are often used in the designs of active devices, such as voltage controlled oscillator (VCO) and mixer. With the improvement on assembling techniques, it is possible to develop high performance RF switch and power detector using SIW with integrated diodes or transistors in the future.

SIW can be used not only to build passives and actives but also to make planar antenna or antenna arrays. Because of its advanced features related to loss and narrow-beam or shaped-beam forming, waveguide slot array antenna is very attractive for RF and mmW applications. Roughly one quarter of the publication of SIW is for antenna design, which shows SIW antenna is one of the most important applications of SIW technique (Wu *et al.* (2010a)). It is very convenient to fabricate slot radiating elements on the broad wall of an SIW because of its feature as a printed circuit. From 1998, Hirokawa *et al.* had a series of publications on the parallel plate waveguide slot array antenna which uses reflection canceling slot pairs as the radiating elements and SIW structure for building the feeding networks. Both longitudinal slot (Yan *et al.* (2004a)) and transverse slot (Lai *et al.* (2009))on the broad wall of an SIW can be used as radiating element of a linear polarized SIW slot array . A nonlinear polarized SIW slot antenna array can be designed by rotating the slots (Chen *et al.* (2007)) on the broad wall. Besides the printed slot on the broad wall, SIW can also provide feeding network through slots to other types of radiating elements, such as antipodal linearly tapered slot (Hao *et al.* (2005a)), vivaldi antenna (Yang *et al.* (2007)), microstrip patch (Huang *et al.* (2004)), dielectric resonator (Hao *et al.* (2006)), yagi antenna (Zhang et Wu (2008)) and printed dipoles (Yu *et al.* (2009)). Not only limited to slot array antenna, SIW can also be

used to design other types of antennas, such as leakage antenna (Deslandes et Wu (2005b); Weitsch et Eibert (2007)), using opened waveguide itself as radiating element (Clenet *et al.* (2006)), H-plane sectoral horn antenna (Yamamoto (2006)), and horn antenna covered with SIW cavity frequency selected surface (SIWC-FSS) (Luo *et al.* (2007)).

With the increasing demand of wireless communications and radar applications in connection with the system size and cost, there have been persistent efforts to simplify the structure of RF front-end module or transceiver module. Among various choices for the transceiver systems, direct conversion strategies have been widely used for their unique advantages to reduce circuit complexity and allow for a higher level integration compared with other conventional heterodyne structures. The key component of such a direct conversion receiver is a multiport junction, either six-port (Tatu *et al.* (2001)) or five-port (Neveux *et al.* (2004)). Multiport junction can be built with various techniques, such as monolithic microwave integrated circuit (MMIC), miniaturized hybrid integrated circuit (MHMIC) (Tatu *et al.* (2003)), complementary metal oxide semiconductor (CMOS) (Chang *et al.* (2006)) and printed circuit board (PCB) (Xu *et al.* (2006)). The six-port can be designed with different transmission lines, including microstrip line, waveguide (Moldovan *et al.* (2004)) and SIW (Xu *et al.* (2006)). Most applications for six-port direct conversion receiver focus on the transceiver systems for K-, Ka-, V- or W- band high speed data transmission, communication or radar sensor. A multiport junction with tunable or switchable terminations can also be used to build an external modulator. A six-port QPSK modulator was presented in (Zhao *et al.* (2006)). The modulator can be extended for more modulation schemes if more impedances values are implemented by the terminations (Luo et Chia (2008)). This reflection-type modulator has been widely used in the design of a vector modulator (McPherson et Lucyszyn (2001)). Since the key parts in both the multi-port direct conversion receiver and the reflection-type modulator are passives which could be built using high-Q SIW couplers and dividers, SIW technique provides a solution of this type of transceiver for mmW applications.

Approaches for designing transition from SIW to other planar circuits in a single-layer substrate were presented previously, including the microstrip-to-SIW transition and the CPW-to-SIW transition (Deslandes et Wu (2001, 2005a)). The conductor loss of a classic rectangular waveguide increases with the reduction in the height of substrate (Pozar (1998)).

$$\alpha_c = \frac{R_s}{a^3 b \beta k \eta}(2b\pi^2 + a^3 k^2) \quad N_P/m \tag{1.1}$$

where R_s is the surface resistance of the metallic walls, a and b are the width and the height of the waveguide, $\eta = \sqrt{\mu/\varepsilon}$ is the intrinsic impedance of the material-filled waveguide, β is the propagation constant, and $k = \omega\sqrt{\mu\varepsilon}$ is the wavenumber of the material-filled waveguide

region. When the dielectric substrate for filling an SIW is relatively thin, for instance thinner than one tenth of the central working wavelength (λg), the conductor loss will dominate the total loss of a waveguide. From this point of view, a thicker substrate is preferred in order to yield a low-loss component in the design of substrate integrated circuits (SICs) which is against the requirement for having a low loss microstrip line. One way to overcome the contradiction is to use a grounded coplanar waveguide (GCPW) which is more compatible with the thick substrate (Deslandes et Wu (2005a)). Another solution of this problem is to create SICs in a multilayer substrate.

In order to satisfy the single mode condition, it is typical to set up the SIW width as 0.7 wavelength (λg) at the center operating frequency. SIW inherits this feature from the standard waveguide. Compared to a standard metallic waveguide, the width of an SIW is reduced by $\sqrt{\varepsilon_r}$ times because of the substrate filling. Since SIW is an enclosed structure, two SIW structures can be arranged side-by-side even without a space for isolation. In spite of these two features, the width of an SIW is still much larger than that of other planar transmission lines. This drawback of SIW circuits becomes more pronounced when a thin substrate is used. When the substrate thickness is reduced in mmW applications, the size of microstrip line and stripline circuits can be scaled down at the same rate. However, the SIW width always remains the same because the cut-off frequency of its dominant mode (TE_{10}) is only related to its broadside dimension. On the other hand, with the performances of microwave and RF integrated circuits based on semiconductor processes greatly improved in the past years, system-in-package (SiP) or system-on-chip (SoC) solutions have been more and more applied at the system level design. The difference of volume/size is even larger when an original SIW is compared with those planar circuits designed with lumped element schemes. Therefore, the miniaturization technique of SIW circuits is an essential aspect that determines whether SIW technique can be used in size-restricted wafer-based IC design.

Because of the reasons mentioned above, the primary objective of this work aims to investigate the miniaturization techniques for SIW in multilayer platform. The remainder of the dissertation is organized as follows.

In Chapter 2, the existing miniaturization techniques for SIW are reviewed and discussed. There are several available SIW miniaturization techniques, including ridge substrate integrated waveguide (RSIW), half-mode substrate integrated waveguide (HMSIW) and folded substrata integrated waveguide (FSIW). Among these techniques, RSIW and C-type folded substrata integrated waveguide (CFSIW) are directly derived from miniaturizing the standard rectangular waveguide. HMSIW and T-type folded substrata integrated waveguide (TFSIW) techniques were proposed specifically for SIW structures, which have an extremely small ratio of height to width and the conductive sheets can easily be patterned in fabrication.

In this chapter, impedance and propagation constant of these miniaturized SIW transmission lines are calculated using transverse resonant method (TRM). One particular concern focuses on the relationship between the attenuation constant and the geometric dimensions of these structures. Optimized dimensions for each structure are suggested based on simulated parametric analysis. A set of transmission lines are fabricated and corresponding transmission parameters are extracted with dual-line method.

From the investigation in the first chapter, we find that multilayer platform is required for most miniaturized SIW structures. Considering the fabrication conditions available in our lab, laminated Rogers substrates are used as a multilayered platform for our designs to prove the concepts. One principal step for using the SIW technology is to develop high-performance transitions and interconnects between SICs and other types of transmission lines or circuits embedded in or surface mounted on the multilayer substrates. The limitations of the process add more challenges to this work. In chapter 3, various transitions from (miniaturized) SIWs to other planar circuits on either a single layer substrate or multilayer PCBs are studied. Some passive devices, including a TFSIW hybrid ring, two HMSIW six-port junctions and two five-port junctions, are designed and measured using the miniaturized SIW and corresponding transitions proposed in Chapter 2 and 3. The design procedures of these devices are summarized. All simulated results are compared with the measurements. It is found that some of these designs have not only reduced circuit size but also a better performance on operating bandwidth.

In Chapter 4, RSIW and TFSIW are adopted in the design of slot array antenna. Although waveguide slot array antenna is attractive for RF and mmW applications, this type of antenna is hard to be assembled with other integrated circuits. SIW provides a solution to build a slot waveguide array antenna in planar substrate. The feeding network for the array antenna can be tightly integrated with the antenna in a single substrate. This highly integrated and compact structure can not only reduce the whole system size but also enhance the system yield. The proposed TFSIW and RSIW slot array antennas present additional improvements on both reduced antenna size and broader impedance bandwidth. Several array antennas with different feeding networks are fabricated in a two-layer Rogers substrate. The broadband gain, radiation pattern and return loss of these antennas are all measured. Several SIW filters and one diplexer are designed using SIW cavity filter technique. A radio frequency (RF) frond-end is then composed of one of the proposed antennas and the SIW diplexer. The polarization loss factor of such the proposed dual-antenna system is measured with two identical array antennas which are placed perpendicular to each other.

In Chapter 5, we investigate the tunability of SIW for its usage in more applications. Fixed phase shifter is an important microwave device in many applications. Semiconductor

devices are often used in planar circuits to change the phase and/or amplitude of a RF signal passing through them. In this chapter, varactor diode and pin diode are selected as the control devices for tuning the phase of SIW continuously and digitally, respectively. The diodes are loaded on top of the SIW through some transverse slots opened on the broadside wall of the SIW. The tuning range, phase and magnitude imbalance of both inline SIW phase shifter and reflection type SIW short termination are investigated through the correlation between simulations and measurements. Two phase shifters, having a tuning range of 180° and 360°, respectively, are implemented with varactor diodes and reflection-type architecture. In the last section of this chapter, the 360° phase shifter is used as a phase modulator whose phase is changed with the control voltage generated from the input I/Q signal.

In Chapter 6, a numerical simulation is firstly designed for studying the impact of the non-ideal termination to the phase and magnitude imbalance of the six-port receiver. Based on the conclusion drawn from this investigation, an SIW six-port junction that is composed of 3-dB four couplers is built in a single layer Rogers substrate. The six-port junction is used to build a transceiver system which includes the six-port junction designed in this chapter, the phase modulator proposed in Chapter 5 and the RF frond-end designed in Chapter 4. The frequency range of this transceiver system is selected at 26GHz. The center frequencies of the transmitting and receiving path are 25.5 GHz and 26.5 GHz, respectively. Each of them has a 500 MHz bandwidth. Selecting this frequency band is partly limited by the multilayer PCB fabrication tolerance of our in-house fabrication. On the other hand, 26 GHz is also in a typical frequency band used by Local Multipoint Distribution Service (LMDS), which normally cover the frequency bands 26 GHz $\sim$ 29 GHz and 31.0 GHz $\sim$ 31.3 GHz. A series of envelop simulations of the proposed transceiver are performed in Advanced Design System (ADS) with models of different levels. The simulations start with ideal component models provided in ADS and end with much more realistic models obtained in EM simulations and measurements.

The contributions of the work presented in this dissertation are summarized in the last chapter. Although multilayer PCB is the one platform used in this work, it is possible that the conclusions and designs in this dissertation can be used in other type of platforms.

CHAPITRE 2

Miniaturization Techniques of Substrate Integrated Waveguide Circuits

2.1 Introduction

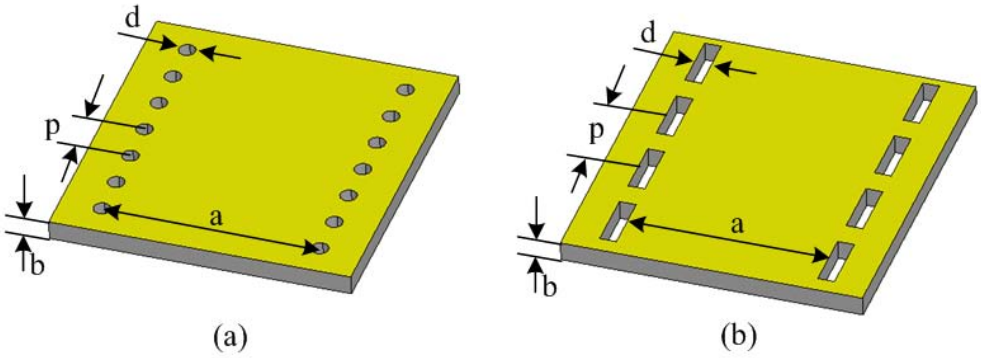


Figure 2.1 Substrate integrated waveguide.

In the beginning of an SIW circuit design, the width of an SIW to be used needs to be calculated with a given dielectric constant of substrate (ε_r) and the center operating frequency. In an SIW shown in Figure 2.1(a), the value of the width (a) is also affected by the pitch between two adjacent posts (p) and the diameter of each single post (d). The cut-off frequencies for TE_{10} mode and TE_{20} mode in an SIW have been formulated by Cassivi *et al.* (2002). The width (a) of an SIW is usually made $0.7\lambda g$ at the operating frequency in practical applications, which is $1.4\backsim1.5$ times of the cut-off frequency. Since the sidewalls of an SIW are composed of rows of periodic conductive posts, metallized via holes or grooves but an ideal conductive surfaces, an effective width (a') of an SIW needs to be calculated using the formulations in (Cassivi *et al.* (2002)) or (Yan *et al.* (2005)). A substrate-filled rectangular waveguide, which has perfect metallic sidewalls and whose width equals to a', can then be used instead of the original SIW in order to simplify the modeling (Cassivi *et al.* (2002)). The sidewall of an SIW can also be synthesized by a row of plated rectangular slots which is shown in Figure 2.1(b). The advantage of using rectangular slots is that the equivalent width of the SIW can be directly measured from the distance between two opposite slots. Ideal perfect electrical boundary is usually used in initial design in order to make the simulation more computationally efficient. The perfect electrical boundary can be directly replaced by two rows of rectangular slots whose distance between each other equals to the width of waveguide

used in the ideal model. Therefore, the rectangular slots are used in all the designs proposed in this dissertation.

Pursuing a lower cost is one of the most important tendencies for neoteric electrical industrial development. A product made on a large piece of substrate obviously has a high cost. This is why the operating frequency of civilian products keeps getting higher. Not only there are more available frequency spectrum resources and lower power consumption, but also a smaller substrate is required by an electrically small circuit. In the designs of SIW circuits, the difficulty on miniaturization is primary on its broad side dimension.

One intrinsic drawback of the conventional waveguide-type devices is their huge size. As to the size or volume of an SIW, there are two pros we should mention. (1) It is a widely-used technique to reduce the cut-off frequency of a rectangular waveguide by filling the waveguide with dielectric substrate, partly or entirely. The size of an SIW has already been reduced by a factor of $1/\sqrt{\varepsilon_r}$ comparing with the conventional rectangular waveguide filled with air. (2) Being different from a transmission lines having an open structure like a microstrip line, the space between two adjacent waveguides for isolation can be saved because of their close structures. Unfortunately, even taking the above two advantages into consideration, the size of SIW circuits is still too large in some integrated circuits.

Moreover, when the operating frequency goes higher, the physical thickness of the substrate becomes thinner to avoid using an electric-thick substrate. The real dimensions of transmission lines, such as microstrip line and stripline, can be scaled down proportionally. However, the waveguide circuits have different laws. In a single-mode waveguide transmission line, the cut-off frequencies of the TE_{10} mode (the dominant mode) and TE_{20} mode (the first high order mode) acts as the high bound and the low bound of the operating frequency range. The same as in a conventional air-filled rectangular waveguide, the cut-off frequencies of these two modes do not depend on the thickness of the substrate in an SIW. They are only proportional to the dielectric constant of the substrate filling the waveguide. $1/\sqrt{\varepsilon_r}$ is the maximum compress ratio to be achieved by using substrate filling technique. This drawback on circuit size gets more pronounced in high-frequency applications, where a thin substrate is used.

In order to use SIW circuits in more integration circuits, except more innovative structures and better electromagnetic performance, SIW miniaturization techniques are an urgent topic under study to break the $1/\sqrt{\varepsilon_r}$ limitation. f_c' is the cut-off frequency of a miniaturized SIW with the same broad side dimension. The miniaturization of the SIW circuits includes two aspects. One is to reduce the longitudinal waveguide length along the wave propagation direction. It can be implemented by introducing some slow-wave structures in SIW designs, such as placing periodic vertical irises in the SIW or using electromagnetic band gap (EBG)

conductive plane as top or bottom broad wall of the SIW. This topic is beyond the scope of this research. The waveguide miniaturization discussed in this research focuses on reducing the width (a) of an SIW on the plane perpendicular to wave propagation. This miniaturization equals the reduction of the cut-off frequency of TE_{10} mode in an SIW with a fixed width (a). In following sections, some waveguide miniaturization techniques will be studied in SIW structures, including ridge substrate integrated waveguide (RSIW), half mode substrate integrated waveguide (HMSIW), and folded substrate integrated waveguide (FSIW).

A compress ratio α is defined for evaluating the capability of the miniaturization techniques introduced in this chapter.

$$\alpha = \frac{f_c'}{f_c} \tag{2.1}$$

where f_c is the cut-off frequency of an ordinary (original) SIW whose broadside dimension is a.

2.2 Ridge SIW

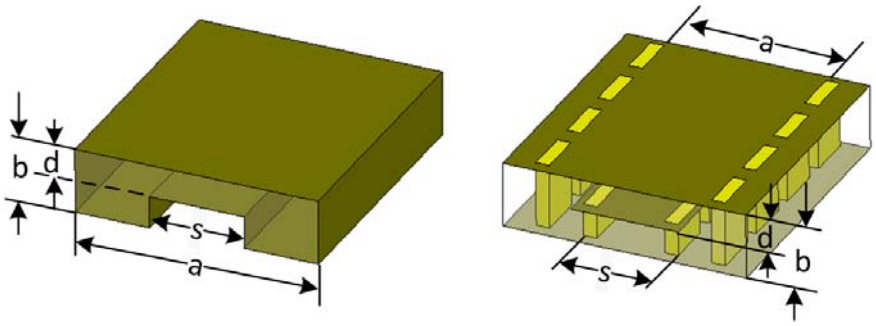


Figure 2.2 Ridge substrate integrated waveguide.

A ridge waveguide is made of a uniform rectangular waveguide with one or two ridges over its broad walls. A ridge waveguide implemented by conductive posts in multilayered substrate is shown in Figure 2.2. The cut-off frequency of a ridge waveguide can be changed by adjusting width s and height d of the ridge without altering outer dimensions of the waveguide a and b. The cut-off frequency, quality factor and characteristic impedance of an air-filled ridge waveguide can be obtained by solving the transverse resonant equation of the dominant mode (Marcuvitz (1986)).

2.2.1 Characteristic impedance

As has been well documented, the characteristic impedance of a transmission line can be defined in three ways : power-current definition $Z_{PI} = 2P_t/(\Pi^*)$, voltage-current definition $Z_{VI} = V/I$, and power-voltage definition $Z_{PV} = (VV^*)/(2P_t)$, where P_t is a time-averaged power transmitted through a cross-section. $*$ denotes the complex conjugation. Such three definitions equal to each other only for a pure transverse electromagnetic (TEM) transmission line. For a quasi-TEM transmission line such as microstrip line or a non-TEM transmission line such as rectangular waveguide or ridged waveguide, the values of a different definition are not unique because of the arbitrary definition of voltage or current.

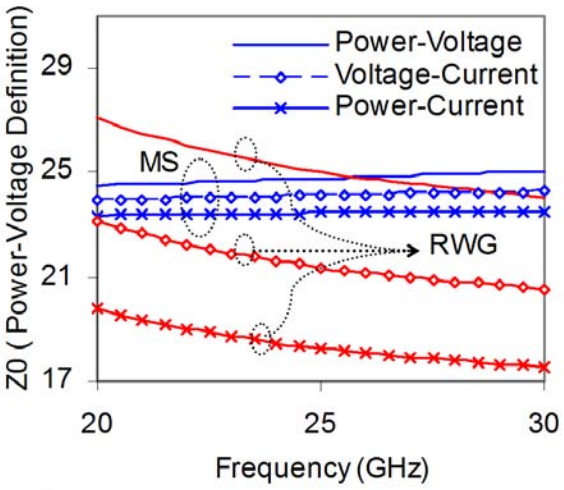


Figure 2.3 Characteristic impedance of three definitions.

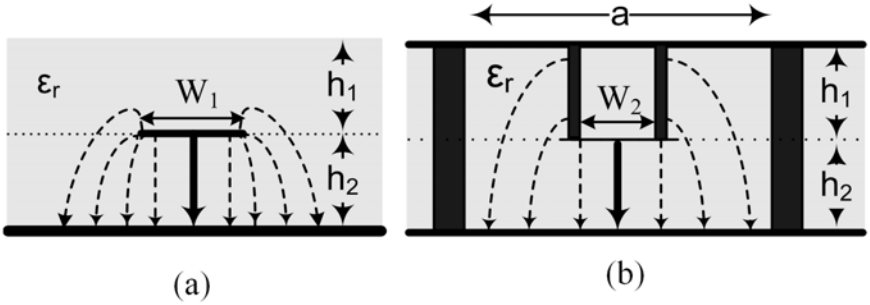


Figure 2.4 Field distribution and integration path of (a) microstrip line and (b) ridged waveguide.

The characteristic impedances of above three definitions are plotted in Figure 2.3. In this figure, the width of microstrip line equals to the width of the gap in ridged waveguide,

that is $W_1 = W_2$ in Figure 2.4. With the power-voltage definition, the impedance curves of microstrip line and ridged waveguide have a cross point within the frequency band of interest. It is probably because the port voltages of these two structures have the same integration paths which are shown with black bold arrows in Figure 2.4. On the other hand, the current definitions of the two structures have more ambiguity. The characteristic impedance with power-voltage definition is therefore used in our design because of its compatibility with microstrip line and ridged waveguide under this circumstance.

2.2.2 Closed-form expressions of TRM

Cutoff wavelength and characteristic impedance are the most important parameters of a (ridged) waveguide for design purposes, especially those of dominant mode. Many studies have been documented on calculating these parameters. A power-voltage definition of impedance of a single-ridge waveguide based on a variational technique was introduced by Utsumi (1985). Spectral domain analysis and magnetic field integral equation (MFIE) were used to analyze ridged waveguide in (Kitazawa et Mittra (1984); Sun et Balanis (1993)). Finite element method for both single and double ridged waveguide was presented by Helszajn et McKay (1998); McKay et Helszajn (1999). Comparing these full-wave methods, transverse resonance method has advantages on computational efficiency and reasonable accuracy, as long as the dimensions of the structures are within a valid range. It gives analytic approximate expressions of characteristic impedance and guided wavelength. Cohn (1947); Chen (1957); Hoefer et Burton (1982) gave the closed-form expressions of characteristic impedance in voltage-current definition. Hopfer (1955) gave the expressions of characteristic impedance in power-voltage definition.

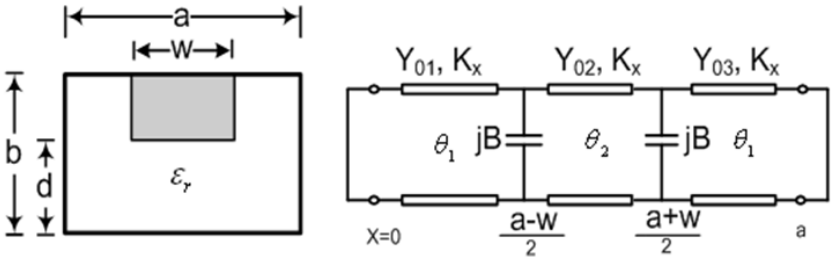


Figure 2.5 Equivalent circuit of a ridged waveguide.

Approximated formulations for a single ridge substrate integrated waveguide are derived below using TRM. An equivalent circuit is indicated in Figure 2.5. The admittances on plane $X = 0$, where the metallic side wall of the ridge waveguide is, equal to zero, which gives the characteristic equation as follows.

$$-\cot\theta_1 + \left(\frac{Y_{02}}{Y_{01}}\right)\tan\theta_2 + \frac{B}{Y_{01}} = 0 \tag{2.2}$$

where

$$Y_{01} = \frac{k_c}{\omega\mu_0}\left(\frac{1}{b}\right) \quad , \quad Y_{02} = \frac{k_c}{\omega\mu_0}\left(\frac{1}{d}\right) \tag{2.3}$$

and

$$\theta_1 = \frac{\pi(a-w)}{\lambda_c} \quad , \quad \theta_2 = \frac{\pi w}{\lambda_c} \tag{2.4}$$

k_c is the cutoff number which is related to the cut-off wavelength λ_c by $k_c = \frac{2\pi}{\lambda_c}$. $\frac{B}{Y_{01}}$ represents the discontinuity on either side of the ridge. One approximation of $\frac{B}{Y_{01}}$ in the case of the single ridge waveguide is in (Marcuvitz (1986)).

$$\begin{aligned}\frac{B}{Y_{01}} \approx\ & 4\left(\frac{b}{a}\right)\left(\frac{a}{\lambda_c}\right)\left[\ln\csc\left(\frac{\pi d}{2b}\right) + \frac{Q_2\cos^4\frac{\pi d}{2b}}{1+Q_2\sin^4\frac{\pi d}{2b}} + \right. \\ & \left. \frac{1}{16}\left(\frac{b}{\lambda_g}\right)^2\left(1-3\sin^2\frac{\pi d}{2b}\right)^2\cos^4\frac{\pi d}{2b}\right]\end{aligned} \tag{2.5}$$

where $Q_2 = \frac{\lambda_g}{\sqrt{\lambda_g^2 - b^2}} - 1$ and λ_g is the guided wavelength which is given by

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon - \left(\frac{\lambda_0}{\lambda_c}\right)^2}} \tag{2.6}$$

One closed-form approximation for the cutoff wavelength of the dominant mode in the single ridge waveguide is in (Sun et Balanis (1993)).

$$\begin{aligned}\frac{a}{\lambda_c} =\ & \frac{a}{2\sqrt{\varepsilon}(a-w)}\left[1 + \frac{4}{\pi}\left(1 + 0.2\sqrt{\frac{2b}{a-w}}\right)\left(\frac{2b}{a-w}\right)\right. \\ & \left.\ln\csc\left(\frac{\pi d}{2b}\right) + \left(2.45 + 0.2\frac{w}{a}\right)\left(\frac{wb}{d(a-w)}\right)\right]^{-\frac{1}{2}}\end{aligned} \tag{2.7}$$

These equations provide good initial values of variables in Equation 2.2, and it can then be solved using an iterative method. This representation agrees with full wave numerical methods within 1% provided that $0.01 \le \frac{d}{b} \le 1$, $0 \le \frac{b}{a} \le 1$, and $0 \le \frac{w}{a} \le 0.45$.

The average power flow at infinite frequency applicable to a single ridge waveguide is Hopfer (1955).

$$\begin{aligned} P_t(\infty) &= \left(\frac{\varepsilon E_0^2 d^2}{2\pi\eta_0}\right)\left[\left(\frac{d}{b}\right)\left(\frac{b}{a}\right)\left(\frac{2ma}{\lambda_c}\right)\ln\csc\left(\frac{\pi d}{2b}\right)\cos^2\theta_2+\frac{\theta_2}{2}\right. \\ &\quad \left.+\frac{\sin 2\theta}{4}+\left(\frac{d}{b}\right)+\left(\frac{\cos\theta_2}{\sin\theta_1}\right)\left(\frac{\theta_1}{2}-\frac{\sin 2\theta_1}{4}\right)\right]\left(\frac{a}{b}\right)\left(\frac{b}{d}\right)\left(\frac{\lambda_c}{a}\right) \end{aligned} \tag{2.8}$$

where $\eta_0 = \sqrt{\dfrac{\mu_0}{\varepsilon_0}}$ is free space wave impedance. The power flow at finite frequency is then given by

$$P_t(\omega) = P_t(\infty)\left(\frac{\lambda_0}{\lambda_g}\right) \tag{2.9}$$

$E_0 = \dfrac{V}{d}\left(\dfrac{V}{m}\right)$ is the peak electric field intensity at the center of the waveguide, the power-voltage definition of characteristic impedance of a single ridge waveguide is then given by the definition

$$Z_{pv}(\infty) = \frac{V(\infty)V^*(\infty)}{P_t(\infty)} \tag{2.10}$$

Taking above equations into Equation 1.1,

$$\begin{aligned} Z_{pv}(\infty) &= \frac{\dfrac{\pi\eta_0 d^2}{2\varepsilon}\left(\dfrac{b}{a}\right)\left(\dfrac{d}{b}\right)\left(\dfrac{a}{\lambda_c}\right)}{\left[\left(\dfrac{d}{b}\right)\left(\dfrac{b}{a}\right)\left(\dfrac{4a}{\lambda_c}\right)\ln\csc\left(\dfrac{\pi d}{2b}\right)\cos^2\theta_2\right.} \\ &\quad \left.+\frac{\theta_2}{2}+\frac{\sin 2\theta_2}{4}+\left(\frac{d}{b}\right)\left(\frac{\cos\theta_2}{\sin\theta_1}\right)^2\left(\frac{\theta_1}{2}-\frac{\sin 2\theta_1}{4}\right)\right] \end{aligned} \tag{2.11}$$

The impedance of a ridge waveguide at finite frequency can then be derived from the quantity at infinite frequency and dispersion factor $\dfrac{\lambda_g}{\lambda_0}$.

$$Z_{pv}(\omega) = Z_{pv}(\infty)\left(\frac{\lambda_g}{\lambda_0}\right) = Z_{pv}(\infty)\frac{1}{\sqrt{\varepsilon-\left(\dfrac{\lambda_0}{\lambda_c}\right)^2}} \tag{2.12}$$

Characteristic impedance in power-current can be obtained with the following relationship

$$Z_{pi}(\infty) = \frac{Z_{vi}^2(\infty)}{Z_{pv}(\infty)} \tag{2.13}$$

2.2.3 Parametric analysis

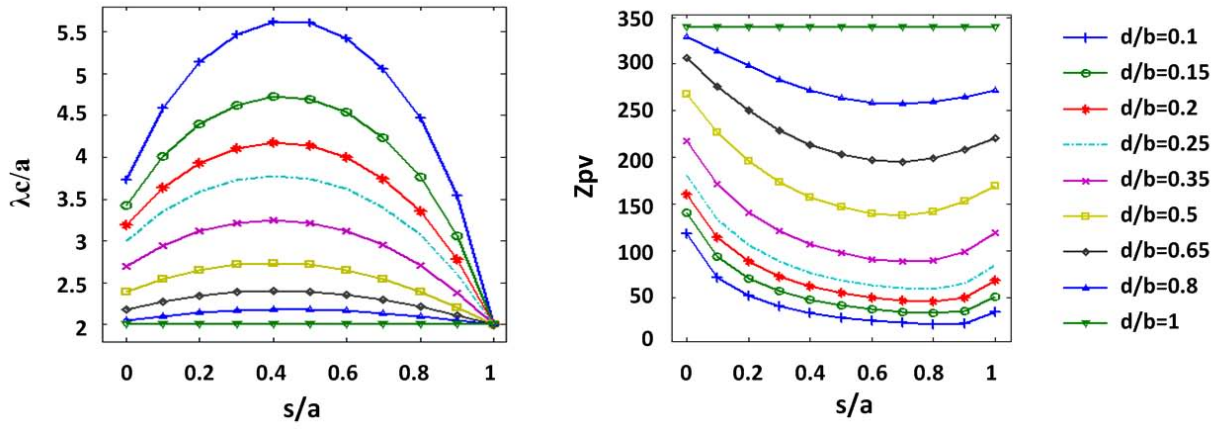


Figure 2.6 Cut-off wavelength and characteristic impedance of a ridge waveguide.

The curves of cut-off frequencies are parabolic when the ratio s/a is swept between 0 and 1. The maximum cut-off wavelength is obtained when the ratio of ridge width to waveguide width (s/a) is around $0.45 \sim 0.5$. Another ratio d/b can also affect the cut-off frequency monotonously. The smaller the ratio d/b is, the lower cut-off frequency of the ridge waveguide has. Moreover, the characteristic impedance of a ridge waveguide is also a function of the ratio s/a and d/b, as shown in Figure 2.6.

The relationship between cut-off frequency, quality factor and the ratios of d/b and s/a in a RSIW is shown in Figure 2.7. The RSIW simulated in this example has $a = 0.6$ mm, $b = 0.12$ mm and the filling substrate has dielectric constant $\varepsilon_r = 9.0$. A ridge waveguide with a higher ridge (large d/b) has a larger cut-off frequency (Figure 2.7(a)) and smaller characteristic impedance. A high Q factor can be achieved when the height of RSIW is increased (the same as SIW) or a large value of ratio d/b is used when the total height of the RSIW is fixed. This conclusion is always true in SIW-type structures because the conductive loss, the dominant part of the total loss in these wave-guiding structures, increases quickly when the height of the waveguide drops.

In a RSIW, the compression ratio α is primarily determined by two ratios, s/a and d/b. The two ratios are fundamentally limited by fabrication condition. The ratio s/a is limited by

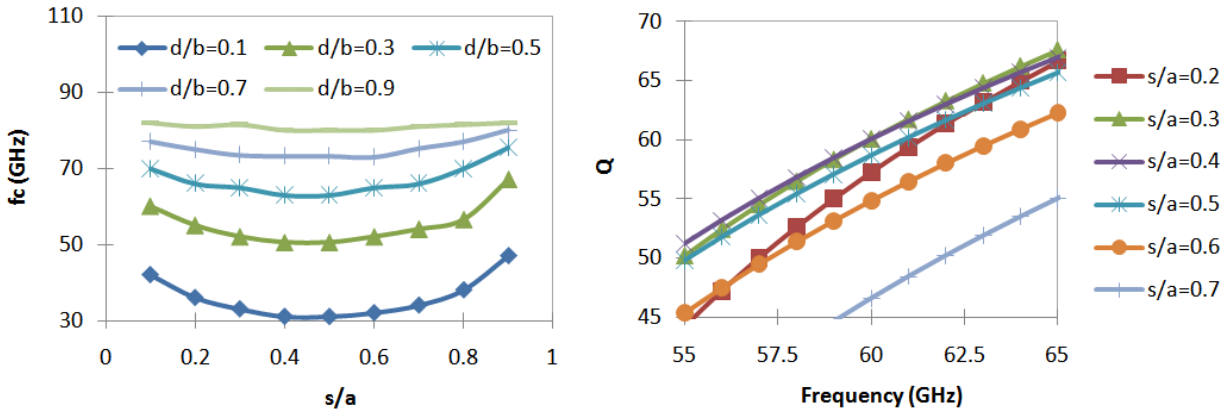


Figure 2.7 Cut-off frequency and quality factor of a ridge waveguide changing with dimensions.

the pitch between two adjacent posts or via holes. The ratio b/d is limited by the minimum thickness of substrate layer and the maximum number of layers that can be stacked in the process.

To achieve an optimized design having both small physical size and high Q factor, there are certain rules to follow in choosing the value of the two ratios :

1. For s/a, a value between the range $0.4 \sim 0.5$ is always used for obtaining a smaller compression ratio and a higher Q factor, as shown in Figure 2.7(b).
2. For d/b, there is a trade-off between the compression ratio and the Q factor. A larger value of d/b yields a smaller compression ratio and unfortunately a lower Q factor as well.

2.3 Folded SIW

From the cross sections shown in Figure 2.8, a transversely folded waveguide or simply folded waveguide can be classified into two types according to the way in which they are folded, namely, (a) and (c) are C-type; (b) and (d) are T-type. A 4-layered C-type folded waveguide, as shown in Figure 2.8(c) was first proposed as a standard waveguide miniaturization technique by Owens for low frequency applications in (Owens (1986)). This technique is especially suitable for the waveguide whose width is much larger than its height, which is exactly a basic feature of SIW. In 2004, a 2-layered C-type folded waveguide shown in Figure 2.8(a) was proposed by Kim et Lee (2004) for conventional rectangular waveguides in microwave and RF applications. In 2005, a 2-layered T-type structure in Figure 2.8(b) was proposed for the miniaturization of an SIW for the first time (Grigoropoulos et Young

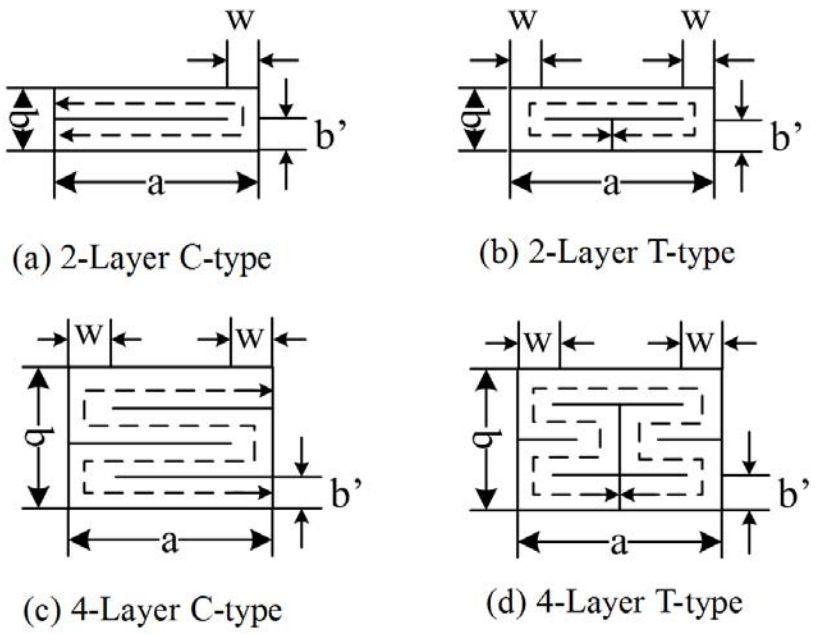


Figure 2.8 Cross sections of folded substrate integrated waveguide.

(2004)). Subsequently, two folding approaches as described in Figure 2.8(a) and (d) were also implemented with SIW in multilayered substrates (Grigoropoulos *et al.* (2005); Sanz Izqueirdo *et al.* (2006)). Except for filters (Grigoropoulos *et al.* (2005); Kim *et al.* (2006)), a 2-layered C-type FSIW was also applied in the design of a slot antenna (Sanz Izquierdo *et al.* (2005)). Similar folding scenario was also used in the design of compact resonators and filters (Hong (2006)).

The solid lines in Figure 2.8 represent conductive surfaces. Over these cross sections, the transverse modes supported in each type of FSIW can be expanded along an approximated path represented by the dash lines shown in Figure 2.8. The electric walls at the end of the path set up the boundary conditions with regard to these transverse modes. An equivalent length a' can be used for calculating the cut-off frequency of the transverse modes. With the equivalent length a', the compression ratio α of an FSIW is defined as

$$\alpha = \frac{a'}{a} \tag{2.14}$$

where a is the real physical broad side dimension of the FSIW.

In Figure 2.9, dispersion characteristics of the dominant mode in the four types of folded waveguides are compared with that of conventional or original unfolded SIW. All these four FSIWs and SIW have the same physical broad side dimension a and the same substrate filling. It is clearly observed that the cut-off frequencies of these dominant modes are almost

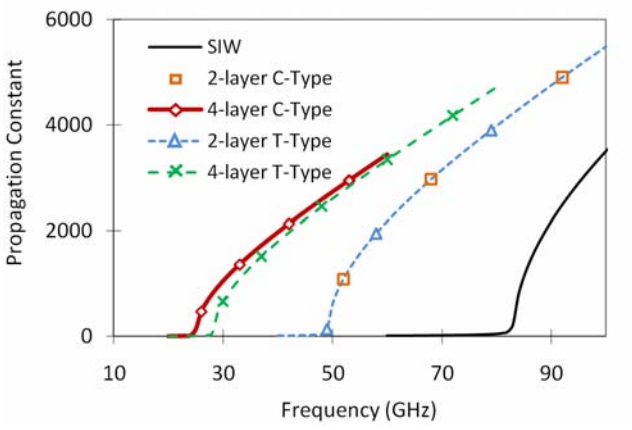


Figure 2.9 Dispersion characteristics of the FSIWs.

inversely proportional to the number of folds. Theoretically, both C-type and T-type FSIW can be folded many times for achieving a better compression ratio α. In practice, the number of such a fold is however limited to 2 or at most 4 because of the inherent loss problem and design as well as fabrication complexity. Because of a large conductor loss caused by the metal strips inserted, the loss performance of FSIW usually gets worse when the number of fold increases.

Similar to the cut-off condition that should be satisfied in a standard rectangular waveguide, a folded waveguide becomes cut-off when its equivalent width a' is close to a half wavelength. In (Grigoropoulos *et al.* (2005)), the fundamental modes in a folded metallic waveguide were analyzed. Transverse resonant method (TRM) can also be used to estimate the propagation constant of all folded waveguides (Marcuvitz (1986)).

2.3.1 T-folded SIW

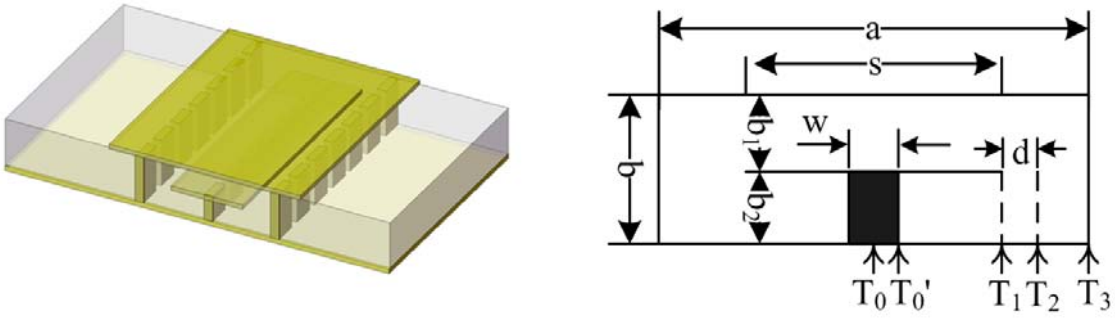


Figure 2.10 3D layout and dimensions of a TFSIW structure.

The 3D layout of a TFSIW structure and all dimensions in its cross section are shown in Figure 2.10. All designs and discussions in this chapter are based on $b_1 = b_2 = b/2$, that is the two laminated substrate layers have the same thickness. T_0, T_0', T_1 and T_2 are the locations of some planes which will be used later in equivalent models.

The analysis of characteristic parameters and the deduction of the equivalent model of a TFSIW can be referred to some previous works on T-septum waveguide and ridged waveguide (Mazumder et Saha (1987); Zhang et Joines (1987); Marcuvitz (1986); Sharma et Hoefer (1983)). Full-wave methods, such as the integral eigenvalue equation solved by using Ritz-Galerkin method and transmission line matrix (TLM) method, were used to calculate the propagation constant and impedance of a T-septum waveguide.

Attenuation constant

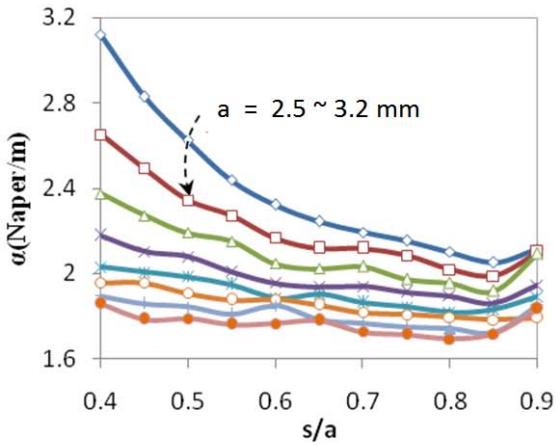


Figure 2.11 Attenuation variation with a and s/a in a TFSIW, extracted from HFSS.

The attenuation constant α of a T-septum waveguide was calculated by Zhang et Joines (1987). To our best knowledge, there is no published discussion on the attenuation of a TFSIW. On the other hand, the unexpected loss is the most important factor which limits the development of this miniaturization technique. Besides the material parameters, the attenuation of a TFSIW is also a function of the width a, height b and the aspect ratio of the septum s/a. Similar as in an SIW case, a larger substrate thickness can give TFSIW circuits a smaller conductor loss, which is the primary source of the loss in SIW-type structures. Once a substrate is chosen, b is fixed. The choice of width a is mainly limited by satisfying the single mode condition, which will be discussed later in this section. Therefore, a designer can suppress the total loss of a TFSIW by choosing a proper value of s/a within the range (0, 1).

As shown in Figure 2.11, we analyze the attenuation constant of a TFSIW when a and s/a are adjusted. The attenuation constant is extracted by using HFSS at a fixed frequency (26 GHz). In this simulation, the material is Rogers 6002 with the loss tangent $\delta = 0.002$ and the height of each substrate layer $b_1 = b_2 = 10$ mil. The metal is copper with the conductivity $\sigma = 5.8 \times 10^7$ S·m^{-1}, the surface roughness is about 1 μm and the metal thickness is roughly 12 μm. As it can be found from Figure 2.11, when value of s/a is within the range $[0.7, 0.8]$, the total attenuation of the TFSIW stays on a relatively low level. It is different from the conclusion by Zhang et Joines (1987), that a smaller s/a always gives a smaller attenuation in a T-septum waveguide. On the other hand, the propagation constant of a TFSIW is proportional to s/a, so a TFSIW with s/a in this range will have a better quality factor.

Phase constant

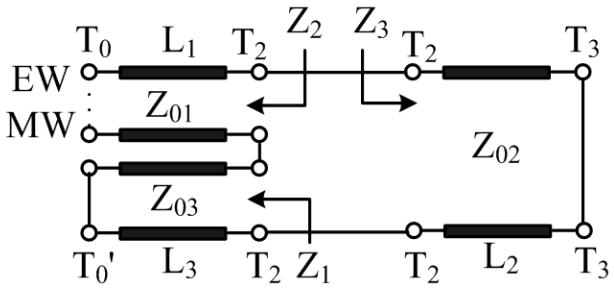


Figure 2.12 Equivalent circuit for a half TFSIW.

The propagation constant for a T-septum waveguide can be estimated using the transverse resonance method (TRM). Similarly, TRM can also be used to calculate the phase constant of a TFSIW. The circuit in Figure 2.12 was firstly introduced as an equivalent circuit of an E-plane bifurcation (Marcuvitz (1986)). When a short circuit is added at plane T_3, this model can be used to solve the phase constant of a TFSIW using TRM. Input impedances of three arms Z_1, Z_2 and Z_3, looked at plane T_2, can be calculated using equations below.

$$Z_1 = jZ_{01}\tan(\frac{s-w}{2} + d) * k_x \tag{2.15}$$

$$Z_2 = \begin{cases} jZ_{02}\tan(\frac{s}{2} + d) * k_x & T_0 \text{ is electric wall} \\ -jZ_{02}\tan(\frac{s}{2} + d) * k_x & T_0 \text{ is magnetic wall} \end{cases} \tag{2.16}$$

$$Z_3 = jZ_{03}\tan(\frac{a-s}{2} - d) * k_x \tag{2.17}$$

where d is the distance from the edge of the septum to a reference plane used in the equivalent

circuit of a bifurcation discontinuity. The value of d can be solved by following equation.

$$\frac{2\pi d}{\lambda g} = \frac{2b}{\lambda g}(\frac{1}{2}\ln 2 + \frac{1}{2}\ln 2) + S_1(\frac{2b}{\lambda g}, 0, 0) - 2S_1(\frac{b}{\lambda g}, 0, 0) \tag{2.18}$$

and

$$S_1(x, 0, 0) = \sum_{n=1}^{\infty}(\sin^{-1}\frac{x}{n} - \frac{x}{n}) \tag{2.19}$$

$$\therefore d = \frac{\ln 2b}{\pi} + \frac{1}{k_x}\sum_{n=1}^{\infty}\sin^{-1}(\frac{bk_x}{n\pi} - 2\sin^{-1}\frac{bk_x}{2n\pi}) \tag{2.20}$$

and

$$2Z_{01} = Z_{02} = 2Z_{03} \tag{2.21}$$

Z_{01}, Z_{02} and Z_{03} are characteristic impedances of the transmission lines. k_x is the wave number of the transverse mode. d is a dimension deciding the location of the plane T_2 shown in Figure 2.10.

According to the theory of TRM, the summation of the impedances looked at plane T_2 must equal to zero. This gives the equation for finding the phase constant β.

$$Z_{01} + Z_{02} + Z_{03} = 0 \tag{2.22}$$

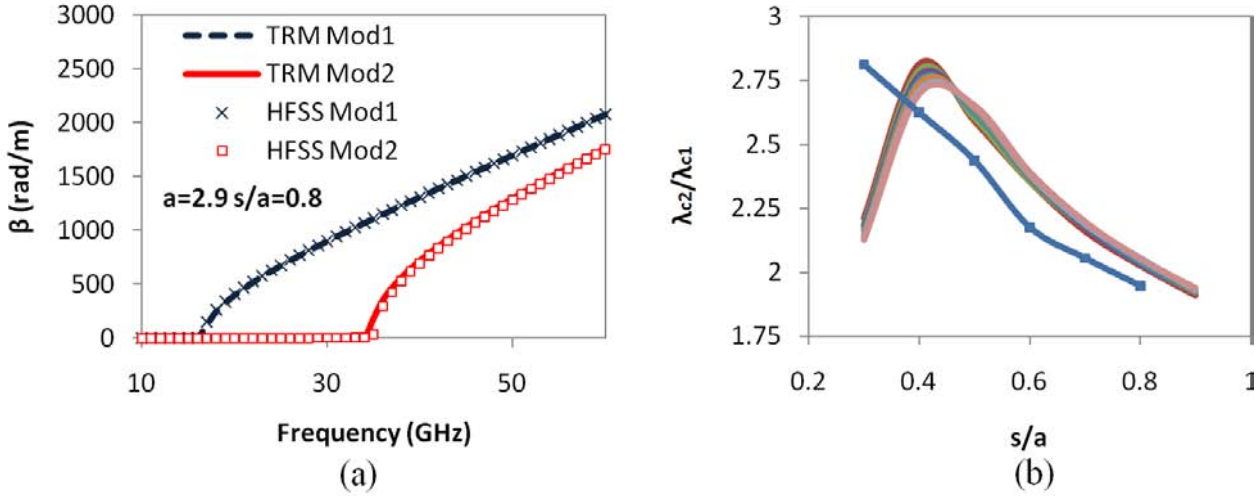


Figure 2.13 (a) Phase constants of TFSIWs solved by TRM and HFSS. (b) The line with markers is the BW of the RSIW, when $a = 3.8$ mm. The lines without marker are the BW of the TFSIWs, when $a = 2.9$ mm and $b_1 = b_2 = 0.254$ mm.

When T_0 is a magnetic wall, the first solution to Equation 2.22 corresponds to the domi-

nant mode in a TFSIW. When T_0 is an electric wall, the first solution to Equation 2.22 is the first high order mode in a TFSIW. In Figure 2.13(a), the phase constants of these two modes solved by this method are compared with results obtained from HFSS.

Bandwidth (BW) of a TFSIW which is defined as $\lambda_{c1}/\lambda_{c2}$, where λ_{c1} and λ_{c2} are cutoff wavelengths of the dominant mode and the first high order mode, is calculated when a and s/a are adjusted. As shown in Figure 2.13(b), the BW of a TFSIW is sensitive to s/a but the absolute value of a. Again, the TFSIWs are compared with the RSIW mentioned in Part 2.3.1 (attenuation constant). As shown in Figure 2.13(b), when $s/a > 0.4$, the TFSIW has a larger BW than that of the RSIW which has the same s/a.

Impedance

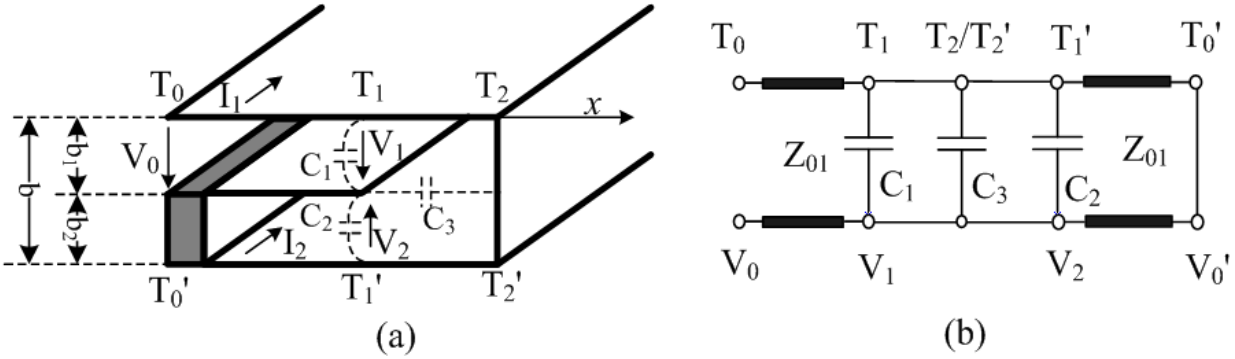


Figure 2.14 Equivalent circuits for calculating the voltage-current defined impedance of a TFSIW.

The characteristic impedance of a waveguide or an SIW is not well defined; however, the concept of impedance is still helpful in waveguide or SIW circuit design. The power-voltage defined impedance of a T-septum waveguide was calculated by Zhang et Joines (1987). In this chapter, we use an equivalent circuit to make a quick calculation of the voltage-current defined impedance of a TFSIW. The discontinuity on plane T_1T_1' can be regarded as two capacitors C_1 and C_2 shown in Figure 2.14(a). The impact of the gap between the edge of the septum and the side wall of the TFSIW can be represented by capacitor C_3. The equivalent circuit of a transverse cross-section in a TFSIW is then given in Figure 2.14(b). In order to obtain the voltage-current defined impedance, we need to calculate the total longitudinal current in the TFSIW. On plane T_0T_0', we assume the voltage from the top wall to the septum is V_0. Since the voltage along the wall of the waveguide cosinusoidally decreases, the voltage

between the up plate and septum at point $x = l$ is

$$V_1(l) = V_0 \cos 2\pi l/\lambda_{c0} \tag{2.23}$$

where λ_{c0} is cutoff wavelength of the TFSIW. The longitudinal current density on the up plate of TFSIW is

$$J_1(l) = \frac{V_1(l)}{b_1\eta} = \frac{V_0}{b_1\eta}\cos 2\pi l/\lambda_{c0}, \quad \text{where} \quad \eta = \sqrt{\frac{\mu_0}{\varepsilon_0\varepsilon_r}} \tag{2.24}$$

and the current on the top plate can then be calculated by an integration of current density in the upper plate along the transversal direction

$$\begin{aligned} I_1 &= 2\int_0^{\frac{s}{2}} J_1(l)\mathrm{d}l & (2.25)\\ &= \frac{2V_0}{b_1\eta}\int_0^{\frac{s}{2}} \cos 2\pi l/\lambda_{c0}\mathrm{d}l & (2.26)\\ &= \frac{V_0\lambda_{c0}}{b_1\eta\pi}\sin \pi s/\lambda_{c0} \end{aligned}$$

In the lower layer substrate, the voltage between the T-septum and the lower plate $V(l)$ and the current density on the lower plate $J(l)$ can be derived in the same manner.

$$\begin{aligned} V_2(l) &= \frac{V_2 \sin(l-\frac{w}{2})2\pi/\lambda_{c0}}{\sin(\frac{s-w}{2})2\pi/\lambda_{c0}} & (2.27)\\ J_2(l) &= \frac{V_1(l)}{b_2\eta} & (2.28) \end{aligned}$$

where V_2 is the voltage on plane $\mathrm{T_1T_1'}$ in the lower substrate layer. The longitudinal current I_2 on the bottom plate of TFSIW is then expressed as.

$$\begin{aligned} I_2 &= 2\int_{\frac{w}{2}}^{\frac{s}{2}} J_2(l)\mathrm{d}l & (2.29)\\ &= 2\int_{\frac{w}{2}}^{\frac{s}{2}} \frac{1}{b_2\eta}\frac{V_2\sin(l-\frac{w}{2})2\pi/\lambda_{c0}}{\sin(\frac{s-w}{2})2\pi/\lambda_{c0}}\mathrm{d}l & (2.30)\\ &= \frac{2V_2}{b_2\eta\sin(s-w)\pi/\lambda_{c0}}\frac{\lambda_{c0}}{2\pi}\left[-\cos(l-\frac{w}{2})2\pi/\lambda_{c0}\right]\Big|_{\frac{w}{2}}^{\frac{s}{2}} & (2.31)\\ &= \frac{V_2\lambda_{c0}}{b_2\eta\pi}\tan\left[\frac{(s-w)\pi}{2\lambda_{c0}}\right] & (2.32) \end{aligned}$$

Since the total current on the two plates equals to each other, $I_1 = I_2$

$$V_2 \tan\left[\frac{(s-w)\pi}{2\lambda_{c0}}\right] = V_0 \sin(\frac{s}{2}\frac{2\pi}{\lambda_{c0}}) \tag{2.33}$$

V_2 can then be expressed by V_0 as follows

$$\therefore \qquad V_2 = V_0 \frac{\sin(\frac{s\pi}{\lambda_{c0}})}{\tan\left[\frac{(s-w)\pi}{2\lambda_{c0}}\right]} \tag{2.34}$$

The discontinuity on plane $\mathrm{T_1T_1'}$ can be regarded as an E-plane bifurcation. In (Marcuvitz (1986)), the discontinuity of an E-plane bifurcation can be equivalent to two shunt capacitors which have been indicated as C_1 and C_2 in Figure 2.14, the normalized susceptance of the capacitors is

$$\frac{B_1}{Y_0} = \frac{B_2}{Y_0} = \frac{b}{b_2}\tan\frac{2\pi d}{\lambda g} = 2\tan\frac{2\pi d}{\lambda g} \tag{2.35}$$

The electric field strength on the capacitors is then expressed as

$$E_{C1} = \frac{V_1}{b_1} = \frac{V_0}{b_1}\cos(\frac{s\pi}{\lambda_{c0}}) \tag{2.36}$$

$$E_{C2} = \frac{V_2}{b_2} = \frac{V_0}{b_2}\frac{\sin(\frac{s\pi}{\lambda_{ca}})}{\tan\left[\frac{(s-w)\pi}{2\lambda_{c0}}\right]} \tag{2.37}$$

The displacement currents on two capacitors are then derived as follows

$$I_{C1} = \frac{V_0\lambda_{c0}}{\pi\eta h}\frac{B_1}{Y_1}\cos(\frac{s\pi}{\lambda_{c0}}) \tag{2.38}$$

$$= \frac{V_0\lambda_{c0}}{\pi\eta h}\frac{B_1}{2Y_0}\cos(\frac{s\pi}{\lambda_{c0}}) \tag{2.39}$$

$$I_{C2} = \frac{V_0\lambda_{c0}}{\pi\eta h}\frac{B_2}{Y_2}\frac{\sin(\frac{s\pi}{\lambda_{c0}})}{\tan\left[\frac{(s-w)\pi}{2\lambda_{c0}}\right]} \tag{2.40}$$

$$= \frac{V_0\lambda_{c0}}{\pi\eta h}\frac{B_2}{2Y_0}\frac{\sin(\frac{s\pi}{\lambda_{c0}})}{\tan\left[\frac{(s-w)\pi}{2\lambda_{c0}}\right]} \tag{2.41}$$

The impact of the lateral part between plane $\mathrm{T_1T_1'}$ and plane $\mathrm{T_2T_2'}$ can be regarded as

capacitor C_3. Because of the reduced height of the TFSIW, we assume the voltage on the wall between T_1T_1' and T_2T_2' all approximately equal to V_1. The displacement current of C_3 can be calculated as follows.

$$I_{C3} = \int_0^{\frac{a-s}{2}} \frac{V_1}{\eta} \frac{\mathrm{d}l}{\sqrt{l^2 + (\frac{b}{2})^2}} + \int_{-\frac{b}{2}}^{\frac{b}{2}} \frac{V_1}{\eta} \frac{\mathrm{d}l}{\sqrt{l^2 + (\frac{a-s}{2})^2}} \tag{2.42}$$

$$= 2\frac{V_1}{\eta}\left[\ln\left(\frac{a-s}{2} + \sqrt{(\frac{a-s}{2})^2 + (\frac{b}{2})^2}\right) - \ln\frac{b}{2}\right] + \frac{V_1}{\eta}\left[\ln\left(\frac{b}{2} + \sqrt{(\frac{b}{2})^2 + (\frac{a-s}{2})^2}\right) - \ln\left(-\frac{b}{2} + \sqrt{(\frac{b}{2})^2 + (\frac{a-s}{2})^2}\right)\right] \tag{2.43}$$

As introduced by Sharma et Hoefer (1983), the voltage-current defined impedance of the TFSIW at infinite frequency Z_∞ can be calculated based on this equivalent model as follows.

$$Z_\infty = \frac{V_0}{I_1 + I_2 + I_{C_1} + I_{C_2} + I_{C_3}} \tag{2.44}$$

$$Z_{VI} = \frac{Z_\infty}{\sqrt{1 - (\frac{f_C}{f})^2}} \tag{2.45}$$

The voltage-current defined impedance at a specific frequency f can then be calculated using Equation 2.45, where f_C is the cutoff frequency of the TFSIW. When a and s/a are adjusted, an example in Figure 2.15 shows the comparison of the impedance calculated with the closed-form formulations and Ansoft HFSS. The TFSIW is in a substrate which has $b1 = b2 = 0.254$ mm and $\varepsilon_r = 2.94$.

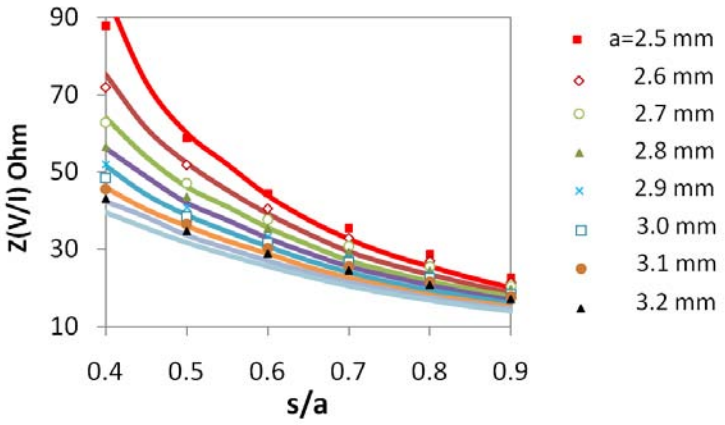


Figure 2.15 Voltage-current defined impedance of TFSIW : solid lines are from HFSS and markers are from equivalent circuit.

2.3.2 C-folded SIW

The propagation constant of a C-folded SIW can also be solved with TRM by using an equivalent circuit shown in Figure 2.16

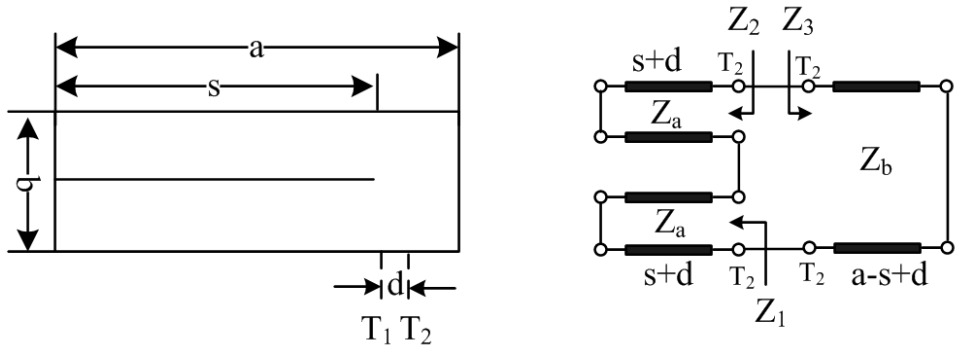


Figure 2.16 Equivalent circuit of a C-folded SIW.

Similar as Equations 2.15, 2.16 and 2.17, the input impedance on plane T_2T_2' can be expressed as

$$Z_{in}^1 = jZ_1 \tan(s+d)k_x \tag{2.46}$$

$$Z_{in}^2 = jZ_1 \tan(s+d)k_x \tag{2.47}$$

$$\begin{aligned} Z_{in}^3 &= jZ_2 \tan(a-s-d)k_x \\ &= 2jZ_1 \tan(a-s-d)k_x \end{aligned} \tag{2.48}$$

where d is the same variable given in Equation 2.20. By making the summary of these impedances on plane T_2T_2' equal to zero, we then have the equation for solving the propagation constant in an C-folded SIW

$$\tan(s+d)k_x + \tan(a-s-d)k_x = 0 \tag{2.49}$$

An example in Figure 2.17 shows the comparison of the impedance calculated with the closed-form formulations and Ansoft HFSS. The TFSIW is in a substrate which has $b1 = b2 = 0.254$ mm and $\varepsilon_r = 2.94$.

2.4 Half-mode SIW

Half-mode substrate integrated waveguide (HMSIW) was proposed by Hong *et al.* (2006). The 3D view of an HMSIW transmission line is shown in Figure 2.18(c). This technique

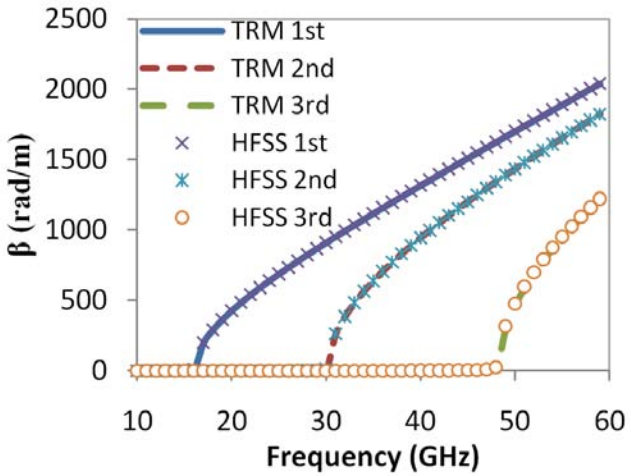


Figure 2.17 Comparison of propagation constant of a C-folded SIW calculated with TRM and HFSS.

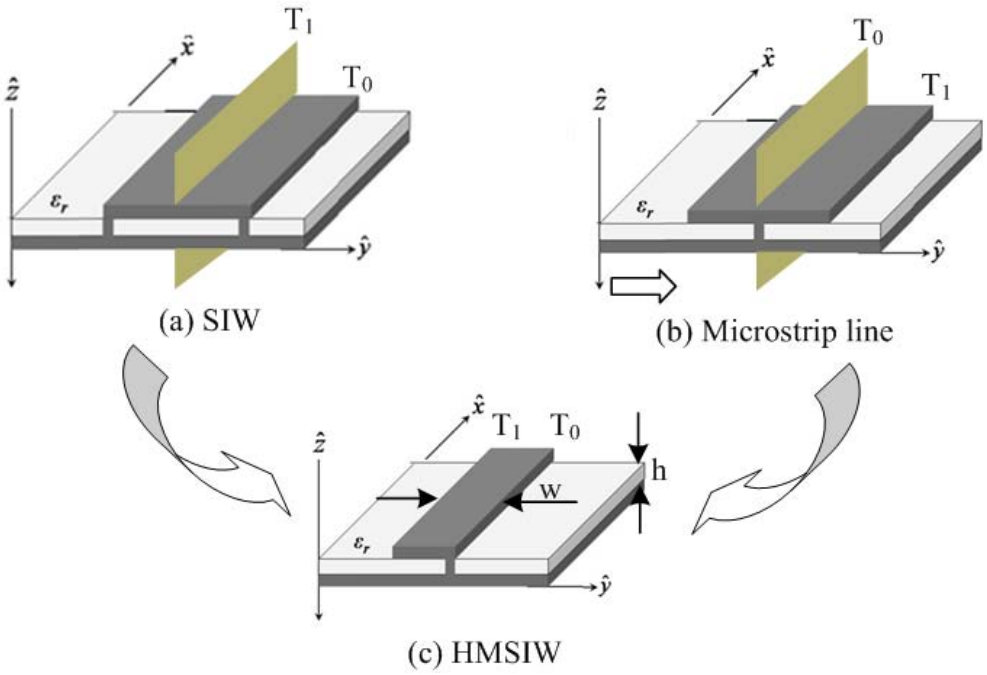


Figure 2.18 The relationship between SIW, microstrip line and HMSIW.

has successfully been used for designing compact power dividers, filters, antennas and 3-dB couplers. The relationship between SIW, microstrip line and HMSIW can be depicted in Figure 2.18. First of all, an HMSIW can be considered as one half of an SIW as shown in Figure 2.18(a). The dominant mode in a rectangular waveguide at the symmetric plane along the propagation direction is equivalent to a magnetic wall. In an SIW structure, the ratio

of width w to height h is usually very large when an SIW is cut into two half waveguides along the center plane, the resulting open aperture between the top and bottom planes is thus very close to a magnetic wall. The dominant mode in such a structure is just like one half of the dominant mode TE_{10} in a complete SIW. In the area close to the aperture, the field is out-diffused a little bit to satisfy its boundary conditions.

On the other hand, an HMSIW can also be regarded as a half of microstrip line, which is terminated by a short-circuited plane in the middle, as shown in Figure 2.18(b). The first higher order mode of the microstrip line has been demonstrated to be an efficient leaky-wave line source. Usually a electric wall is inserted in middle plane of a microstrip line to suppress the dominate mode (quasi-TEM mode). Interestingly, the working mechanism of a half microstrip line excited by its first high-order mode is exactly the same as that of an HMSIW. However, the propagation constant of the line needs to be designed in different area for different applications. For a microstrip leaky wave antenna, the propagation constant of the line should be designed in the radiation area while, as a wave-guiding structure, the propagation constant of a HMSIW needs to be kept away from that area. However, because of their similar working mechanism, the physical and numerical models for analyze these two structure can be the same. In (Lee (1986)), TRM was used to analyze high-order modes propagating along a microstrip line and the working mechanism of a microstrip leaky-wave antenna. In our work, we also use the TRM to analytically solve the propagation constant of an HMSIW.

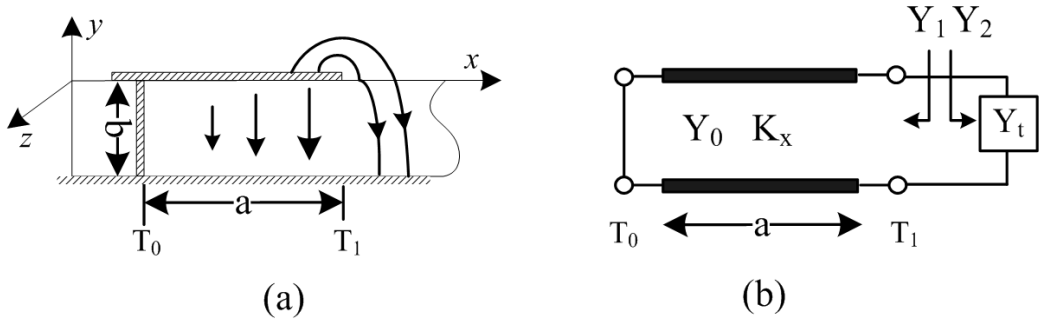


Figure 2.19 Cross-section and transverse equivalent circuit of an HMSIW.

The cross-section of an HMSIW is shown in Figure 2.19(a). The transverse resonance equivalent circuit of this network is shown in Figure 2.19(a), where Y_t is a terminating admittance to represent the boundary condition at the edge of the metal strip (plane T_1). Γ_1 and Γ_2 are input admittance of the equivalent circuits on the left and right sides of plane T_1

respectively. Γ_1 can be deduced simply from the transmission line theory

$$\Gamma_1 = \begin{cases} -e^{-jk_x a}, & \mathrm{T}_0 \text{ is short-circuited plane} \\ -e^{-jk_x a + j\pi}, & \mathrm{T}_0 \text{ is open-circuited plane} \end{cases} \tag{2.50}$$

$$\Gamma_2 = e^{-j\chi} \tag{2.51}$$

The transverse resonance equation of this network is

$$\Gamma_1 \Gamma_2 = 1 \tag{2.52}$$

The relationship between the equivalent admittance χ and the transverse resonance wave number k_x can be expressed as

$$\chi - k_x a = \pm n\pi, n = 1, 3, 5 \ldots \tag{2.53}$$

where $n = 1$ is used for calculating the wave number of the dominate mode in the HMSIW and $n > 1$ can be used to calculate the high order modes. The transverse wave number k_x is then can be solved. The desired longitudinal propagation wave number can then be calculated as

$$(k_z)^2 = \varepsilon_r (k_0)^2 - (k_x)^2 \tag{2.54}$$

For a thin substrate, an analytic formulation of χ has been given in Kuester *et al.* (1982).

$$\chi = 2 \arctan\left(\frac{k_z}{k_x} \tanh \triangle\right) - f_e\left(-\frac{k_x}{k_0}\right) \tag{2.55}$$

$$\triangle = \frac{k_z b}{\pi}\left\{\left(\frac{1}{\varepsilon_r} - 1\right)[\ln(jk_x b) + \gamma - 1] + 2Q_0(-\delta_\varepsilon) - 2Q_0(-\delta_\mu)\right\} \tag{2.56}$$

$$f_e\left(-\frac{k_x}{k_0}\right) = \frac{2k_x b}{\pi}\left\{\frac{1}{\varepsilon_r}[\ln(jk_x b) + \gamma - 1] + 2Q_0(-\delta_\varepsilon) - \ln 2\pi\right\} \tag{2.57}$$

$$\delta_\varepsilon = \frac{\varepsilon_r - 1}{\varepsilon_r + 1} \tag{2.58}$$

$$\delta_\varepsilon = \frac{\mu_r - 1}{\mu_r + 1} = 0 \tag{2.59}$$

$$Q_0(t) = \sum_{m=1}^{\infty}(t^m \ln m), \quad |z| < 1 \tag{2.60}$$

By using the above formulations, we firstly analyze an HMSIW over the V band and compare dispersion curves of the first two modes through Ansoft-HFSS simulations as plotted in Figure 2.20. The curves of the dominant mode generated between HFSS and TRM match

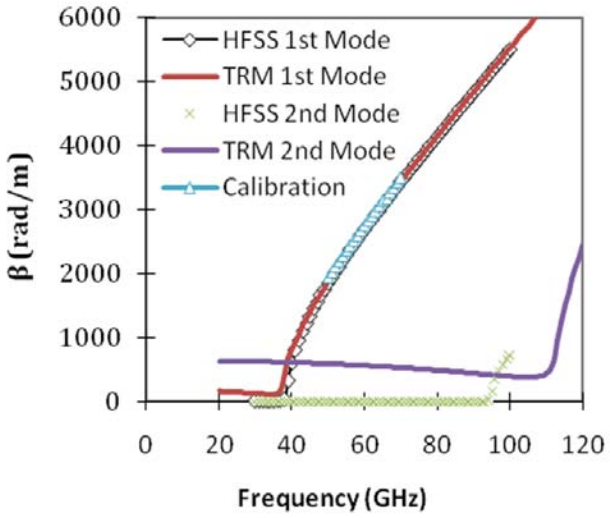


Figure 2.20 Dispersion curves of the first two modes in an HMSIW.

with each other very well. As for the difference with respect to the first high order mode, it may be caused by the approximation that we considered in the derivation of integral formulation in TRM.

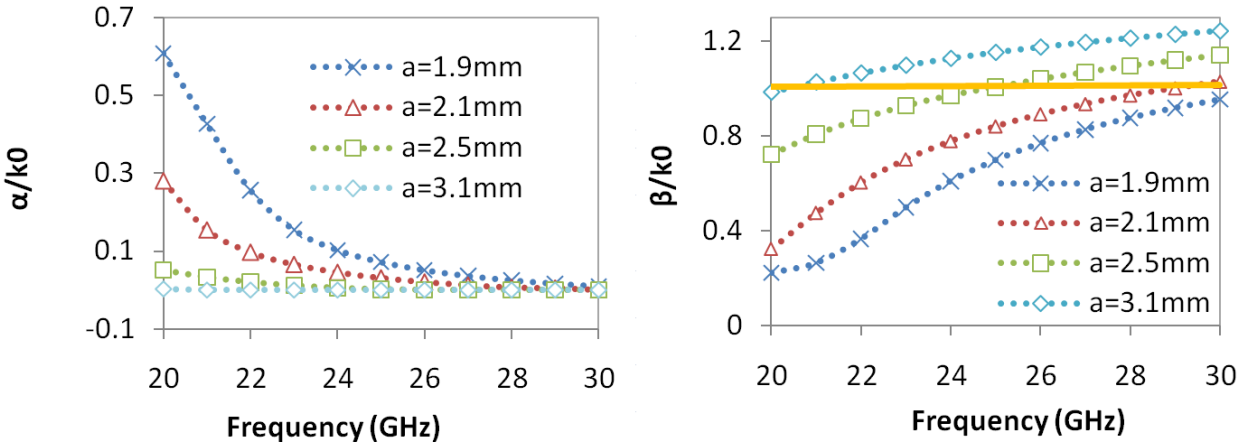


Figure 2.21 The propagation constant of an HMSIW leaky wave antenna in Xu *et al.* (2008b).

We can also analyze the HMSIW leaky-wave antenna proposed by Xu *et al.* (2008b). The propagation constant is shown in Figure 2.21. According to the conclusions in (Lee (1986)), in order to make the HMSIW structure work as a leaky wave antenna, the phase constant curves should be located below the orange horizontal line, which means the width of the HMSIW should be at least 1.9 mm in this case. On the contrary, when the propagation constant is in

the region above that dash line, the wave will be guided (or bounded) in an HMSIW like in a normal transmission line. By using the quick TRM analysis, we can identify the different working ranges of an HMSIW.

2.5 Comparison of miniaturized SIW transmission lines

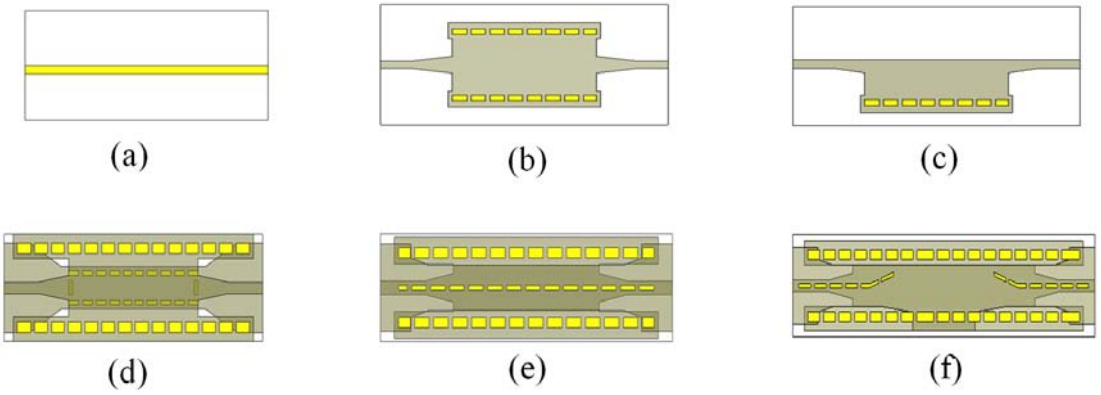


Figure 2.22 Transmission lines based on various miniaturization techniques and their transitions to microstrip lines, (a) microstrip line, (b) SIW, (c) HMSIW, (d) RSIW, (e) TFSIW, (f) CFSIW.

In order to compare characteristics of the three different techniques and four different structures introduced above, a group of SIW transmission lines are implemented and analyzed. The ideal models of these lines are shown in Figure 2.22. In practical models for fabrication, all vertical metal walls are implemented by using rows of plated via hole which are connected with metal strips at the top and bottom. The substrate used is Rogers 6002, $\varepsilon_r = 2.94$ and $\tan\delta = 0.0012$. Among them, the SIW and HMSIW are constructed in a single layer substrate ($h = 10$ mil) while the other three SIWs are made in a double layer substrate ($h = 20$ mil). The broad side dimension and compression ratio of each line are listed in Table 2.1. The FSIWs achieve the highest compression ratio. Transitions from all these SIWs to microstrip lines are designed for experiments in (Deslandes et Wu (2001)). A calibration technique with two transmission lines of different length is used to extract propagation constants and S-parameters of the lines, (Xu et Wu (2005)). The simulations are conducted by using Ansoft HFSS within $24 \sim 28$ GHz. We also did the measurement of these transmission lines. However, the extracted transmission line parameters have fluctuations within the testing frequency band. We believe that it is mainly caused by the reliability and reciprocity of the fabrication. Since the loss of the transmission lines which are designed for

parameter extraction using dual-line method is not proportional to their length. Therefore, we only show the Q of these lines which are extracted from simulations with dual-line method in Figure 2.23. The performance of all these transmission lines are summarized in Table 2.2. According to the simulation and our experience, the RSIW and TFSIW are two good candidates which make a good tradeoff between the size of the circuit and performance of the design. Therefore, a lot of designs proposed in the following chapters are based on these two miniaturization techniques.

	SIW	HMSIW	RSIW	C-FSIW	T-FSIW
a(mm)	5	3	3.5	2.9	2.9
α	1	0.6	0.7	0.58	0.58

Tableau 2.1 Broad side dimension and compression ratio of each miniaturized SIW.

	Substrate layer	Compression ratio	Symmetric	Loss in practice
SIW	1		yes	small
HMSIW	1	large	no	large
RSIW	2	medium	yes	medium
TFSIW(2 folds)	2	large	yes	medium
CFSIW(2 folds)	2	large	no	large

Tableau 2.2 Comparison of different miniaturization techniques.

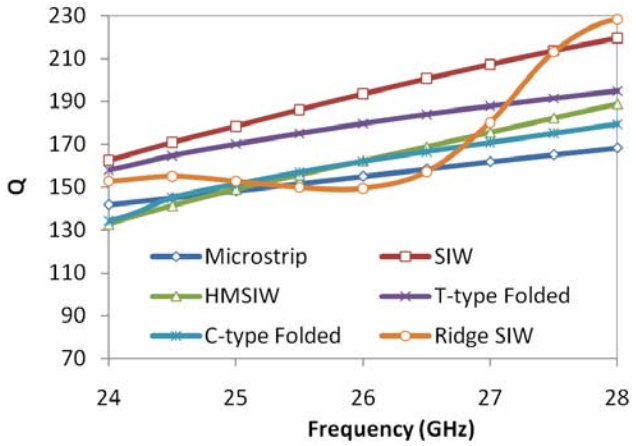


Figure 2.23 Quality factor Q of an SIW and miniaturized SIWs extracted from HFSS simulations by using TRL numerical calibration.

The conclusions listed in the table are drawn based on the simulation results. However, the performance of these lines and related designs such as transitions are tightly related to the

tolerance and process one can achieve in fabrications. The fabrication issues which cannot be accurate modeled and estimated in the simulations and the errors in alignment and stack-up can directly cause the failure of the design. An example will be given in next chapter to show the impact of the fabrication, specifically multilayered fabrication, on the performance of the design.

2.6 Other SIW miniaturization techniques

The slow-wave structure can be classified as 1D, 2D and 3D structures. 1D slow-wave structure is implemented along the direction of wave propagation by placing periodic irises inside the SIW Liu *et al.* (2005). 2D slow-wave structure, such as using periodic EBG cells patterned conductive planes as the top and bottom walls of the SIW Hao *et al.* (2005b), can both change the cut-off frequency and be used to minimize both the length and width of an SIW .

Metamaterial slab loaded waveguide

One artificial surface used in waveguide minimization is the perfect magnetic conductors (PMCs) built with left-handed medium (LHM) or negative magnetic permeability structures printed on dielectric substrates and inserted inside the waveguides. According to the location of metamaterial slabs, there are two different ways to produce equivalent PMCs to make wave propagate below cut-off frequency.

In (Yang *et al.* (1999)), metamaterial slabs with artificial perfect magnetic conductors (complex surfaces) were stuck on the sidewalls inside the waveguide. The PMCs are constructed with a photonic band gap (PBG) structure. By using the equivalent transmission line model, the cross section of a regular rectangular waveguide can be looked as two pairs of cascading half cut-off wavelength transmission line terminated with short circuits. The artificial PMCs change the terminations of two transmission lines from perfect electric conductors (PECs) to PMCs. Therefore, the E-field distributed in the cross section is close to TEM mode when the resonant condition of the PBG structure is satisfied. In this circumstance, even the working frequency is below the cur-off frequency of the original rectangular waveguide, TEM wave can propagate in this waveguide.

In another approach, a dielectric slab with an artificial negative magnetic permeability structure on its one side or both two sides is inserted into the symmetry plane of the waveguide. A hollow waveguide below the cut-off frequency is interpreted as an equivalent of negative permittivity material, while resonant elements on a dielectric slab represent a negative magnetic permeability structure. In a rectangular waveguide filled with double negative metamaterial, which means the rectangular waveguide works below the cut-off frequency and

it has a frequency selective surfaces (FSS) printed on a dielectric slab placing in its symmetry plane, waves of certain band below the cut-off frequency can propagate.

Different configurations have been published to be used to construct the FSS. Marques *et al.* (2002) proposed broadside-coupled split ring resonators (SRRs) printed on both sides of a dielectric substrate. A high miniaturization ratio can be obtained by loading the SRRs with lumped capacitor (Hrabar *et al.* (2005)). Except SRRs of different shapes (Marcuvitz (1986)), spiral resonators (SRs) and dipoles (Lubkowski *et al.* (2006)) can also be used as resonant elements for making an FSS. Larger miniaturization ratios can be obtained by introducing more turns in the spiral structure and reducing the gap between the dipole and the waveguide. High density of the resonator elements can give a steep slop between the passband and stopband.

There are some disadvantages when using this approach to minimize the size of the waveguide. This approach uses resonators to construct the FSS, therefore, the insertion loss of the guided wave structure is large and the bandwidths of related circuits are very narrow. Using some nonresonant type of metal materials may alleviate the two problems. 1) The responses of the waveguide and bandpass or bandstop filters have some ripples in the passband. The number of ripples is related to the number of resonator in the direction of propagation. Decreasing the size of resonators causes the continuous medium approximation to be more accurate and alleviates the problem of high ripples. 2) Although increasing the number of array elements provides steeper slopes of bandpass characteristics, but this high selectivity is at the cost of larger physical dimensions and higher insertion loss.

The resonators used in this approach are vertical structures printed in a thin dielectric surface vertically placed in the symmetrical plane of the waveguide ; therefore, for the SIW structures fabricated in multilayered substrate, there is no much flexibility of making a specific resonator by only using horizontal planar strips and vertical via holes.

Slow wave surface

Another approach to minimize the waveguide is to employ the slow wave characteristic of the electromagnetic band gap (EBG) structure. EBG structures are periodic structures, which can be constructed with a piece of dielectric substrate with periodic metallic patterns printed on the top and a metal ground plane backed on the bottom. There are one or multiple frequency band gaps on the patterns where no substrate mode can exist. An EBG surface shows a high impedance property or known as the magnetic conductor surface within the stopband, in which wave propagation of electric and magnetic energies are separated. This unique high-permittivity property has been applied to improve the performance of antenna designed by suppressing surface wave mode.

Another important application of EBG structures is to use their slow-wave characteristic in design of phase shifters. This slow wave property has been used in circuits' miniaturization. When using EBG structure on the top and bottom surfaces of a rectangular waveguide, the cut-off frequency of such an EBG waveguide is shifted to a lower frequency band because of the slow-wave effect of the high-permittivity surfaces. In (Shelkovnikov et Budimir (2007)), the EBG surface is constructed with an array of small metal patches printed on top connected the ground on the bottom by metal plated via-posts on a thin dielectric substrate. The width of the EBG waveguide is 20% smaller than the conventional dielectric filled waveguide. In (Wu et Tzuang (2003)), an electric-magnetic-electric (EME) surface is used as a slow-wave medium and the width of the synthetic SIW is 62% smaller than the conventional SIW. The drawback of this waveguide miniaturization approach is that all known methods for enhancing the slow-wave factor (SWF) or the normalized phase constant of the EBGs lead to an increasing attenuation constant and decreasing bandwidth.

2.7 Conclusion

In this chapter, we review and discuss various SIW miniaturization techniques. Some of them are based on manipulating the cross sections of the synthesized waveguide, such as RSIW and FSIW. The others are based on creating artificial boundaries, such as HMSIW and those techniques mentioned in Section 2.6. There are many factors we need to consider in selecting a specific miniaturization technique for an integrated circuit design, such as the substrate platform and form factor to achieve. The HMSIW has a fixed compression ration around 0.5 and the structure can be built on a single layer substrate but the asymmetric structure may cause the design complexity. Both RSIW and FSIW need multilayer substrate platform for implementation. The compression ratio of these schemes is tunable by adjusting the physical dimension of the inner metal strip or posts. The FSIW has the potential to achieve a better compression ratio. But both RSIW and TFSIW need to be implemented with blind via holes or buried via holes. This might be an issue in fabrication and the cost of fabrication might also increase.

CHAPITRE 3

SIW Transitions and Passives in Multilayer Substrate

3.1 Introduction

Transitions are fundamental circuits for providing the interconnects between various waveguiding structures. The designs of transitions can have strong impacts on the performance of the entire system. On the other hand, limited by I/O connections provided by the commercial measurement equipments, the new proposed structures usually need to be converted into some conventional microwave structures, such as microstrip line, or connect with standard connectors, such as coaxial line connectors. Although there is more freedom we can use when the design is in a multilayer platform, the design also becomes much more complicated when the field is transferred in three directions. In this chapter, we focus on the applications of the miniaturized SIW techniques which have been investigated in the previous chapter. All structures introduced in the previous chapter are waveguide or SIW type structures, which means we are not able to measure them directly. Many transition designs from SIW to microstrip line and grounded coplanar waveguide (GCPW) have been published. However, there are not much reports on the transition designs from SIW-type circuits to those conventional planar lines in multilayer platform. In the first section of this chapter, several transitions are proposed, fabricated and tested in two- or three- layer structures.

Microstrip line is the most widely used planar structure in multilayer substrate ; it is critical to design a high-performance SIW-to-microstrip transition, where the microstrip line could be on any layer of the substrate. An SIW-to-microstrip transition is firstly introduced in this chapter. The transition involves a tapered or multisection ridge waveguide and a tapered transmission line. Closed-form expressions of characteristic impedance and guided wavelength of a ridge waveguide are given using transverse resonance method (TRM). Parameters of three ridge SIWs are calculated and compared with a commercial full-wave software. A design procedure is given from the view of transmission line impedance matching. Simulation results of two examples are compared with measurement results and a conclusion is drawn in the end.

TFSIW is a structure which has been used in many designs in our work. The wide dimension of the waveguide can be reduced by 40% by using this structure in a multilayer substrate. The transitions from TFSIW to other types of structures, such as microstrip line and SIW, are then necessary. However, the designs for these transitions are more complicated

than those between single layer structures. The field distribution of the dominate mode in TFSIW is not uniform in the two layers because of the folding. Some complex structures need to be adopted to keep a smooth mode transformation in the design of these transitions. Section 3.2.2 and Section 3.2.3 present two examples of TFSIW transition designs.

An SIW-to-SIW transition in a two-layer PCB is demonstrated. The design is fabricated in our own workshop. Some fabrication issues are discussed based on the comparison of the simulation and measurement. The design of such a kind of transitions provides a possibility to dramatically reduce the size of the system design by separating the design into different layers. Those designs with E-plane coupling can also be implemented if the fabrication process is reliable and reciprocal.

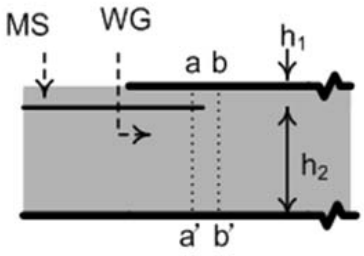
In the last three sections of this chapter, some new passive circuits are proposed and measured, including an HMSIW six-port junction, a TFSIW hybrid ring and a TFSIW 5-port ring. The design methodologies of these miniaturized passive circuits are investigated. These designs are all fabricated and tested. From the correlation between the simulations and measurements, we conclude that the design of multilayer circuit based on our own fabrication process is satisfying in most designs. However, some special design rules and technique are adopted in order to have a more reliable and repeatable fabrication.

3.2 SIW transitions

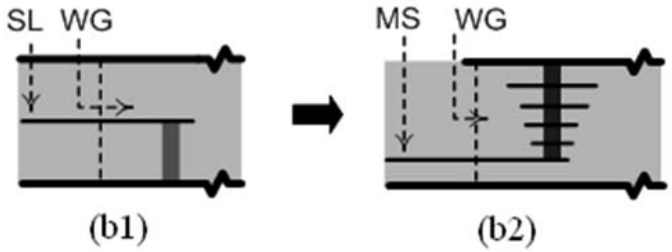
3.2.1 SIW-to-microstrip transition

An SIW-to-microstrip transition has been proved effective on a single layer substrate (Deslandes et Wu (2001)). On a thick substrate, such a transition is subject to a large radiation loss, which may lead to a strong coupling to its neighboring integrated circuits. In order to have an accurate prediction of entire structure response, related circuits should be analyzed together with the transition using electromagnetic modeling package. If an SIW-to-microstrip transition with negligible radiation is used instead, the overall design task can be reduced by carrying out simulation for each functional block in a separate manner.

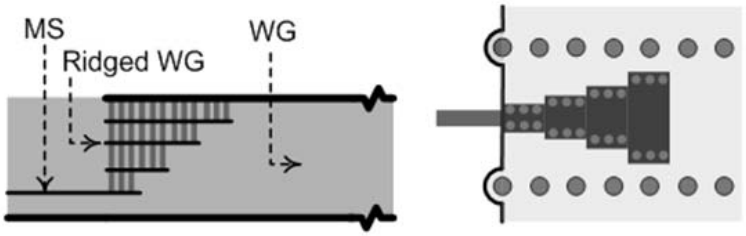
Several studies have been reported on the SIW-to-microstrip transitions in multilayer substrate. In (Rong *et al.* (1999)), the field was directly coupled from an SIW to a tapered microstrip line which was inserted into the waveguide. No connection among different layers was required. However, this coupling type of transition requires similar vector distributions of electric fields on two cross sections, a-a' and b-b' as shown in Figure 3.1(a). The transform ratio $\alpha = h_1/h_2$ cannot be a large value under this condition. In another proposed SIW-to-stripline transition (D'Orazio et Wu (2006)), a stripline ended with a shorted via was inserted into an SIW, as shown in Figure 3.1(b1). The design can further be developed to an



(a) Coupling type of transition.



(b) Probe type of transition.



(c) Ridge waveguide type of transition.

Figure 3.1 Structures of SIW-to-microstrip transitions.

SIW-to-microstrip transition. Some metal pads can be added in the surrounding area of the shorted via to provide a matching mechanism. This probe type of transition is similar to the probe coupled coaxial-to-waveguide transition as studied in (Huang et Wu (2003)). However, it is difficult to derive a general equivalent circuit for this structure and the multisection impedance matching theory cannot be used to guide the design directly, which makes this transition not a good approach from the design point of view.

Simultaneous field matching and impedance matching are important for a transition design. Two general problems in an SIW-to-microstrip transition design are 1) a large difference between the characteristic impedance values of a microstrip line and a rectangular waveguide, and 2) a field mismatching between SIW and microstrip line, especially when the microstrip line is not located on the same plane as the top of the SIW. One of the widely used clas-

sic waveguide-to-microstrip transitions is related to the ridged waveguide (Moochalla et An (1984)).

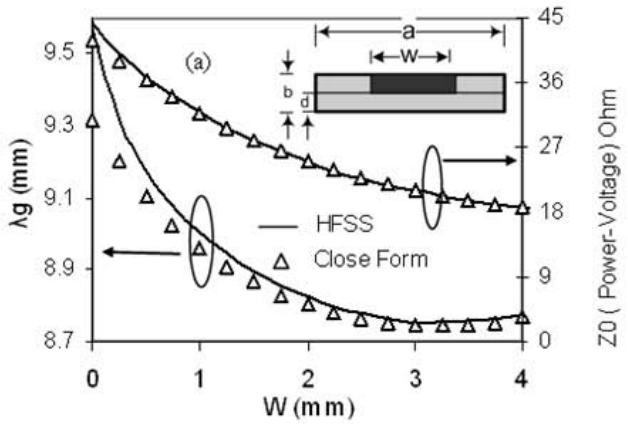
There are two advantages to use a ridged waveguide as either functional microwave circuits or transition : 1) the cut-off frequencies of the dominant mode and the first higher order mode of a ridged waveguide are widely separated compared with a conventional rectangular waveguide ; 2) value of the characteristic impedance of a ridged waveguide is between that of a regular rectangular waveguide (usually 377 Ohm for an air-filled rectangular waveguide) and that of a coaxial or stripline structure (usually 50 Ohm).

A ridged waveguide has one more advantage when it is used to create a transition between waveguide devices and microstrip type circuits. The characteristic impedance of a ridged waveguide is changed with depth and width of the ridge. Cross-sections of a microstrip line and a substrate integrated ridged waveguide on a 2-layer substrate are shown in Figure 2.4. The metallic ridge, as shown in Figure 2.4(b), can be implemented by using rows of metallized via-holes or grooves in multilayer substrates. Electric fields on the cross sections are described by the dash lines with arrows. The field between the metal strip and ground plane in Figure 2.4(a) looks similar to the field distributed between the gap and ground in Figure 2.4(b), especially when the ratio $a/2(h_1 + h_2)$ and a/W_2 are large and the fields are more concentrated in the center part.

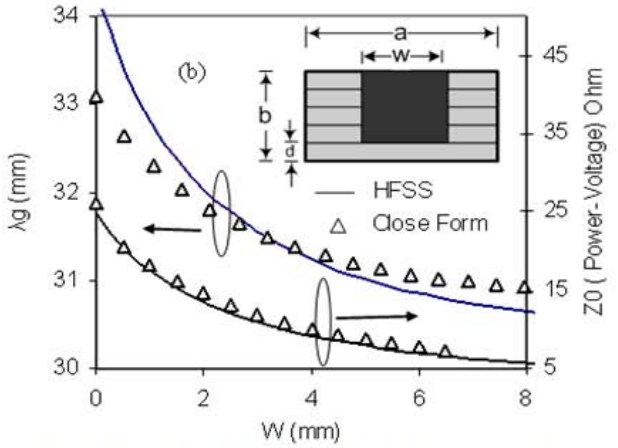
Based on the above consideration, a tapered ridged substrate integrated waveguide and a tapered microstrip line are synthesized between a microstrip line and an SIW in our proposed SIW-to-microstrip transition. The field matching and characteristic impedance matching therefore have a good balance at the junction. The ridged waveguide extends the edge of its ridge over the tapered microstrip line. The multisection impedance matching theory for general microwave transmission lines is proved to be able to provide a good guide in a design of this ridged waveguide type transition between SICs and microstrip line circuits.

Although the field distribution is a more natural way to describe the matching where there are discontinuities in microwave circuits, it cannot be used directly in design. The field and dispersion information should further be quantified as a frequency-dependent value, such as the characteristic impedance. A transition design can be divided into numerical analysis including several simpler transmission lines if the characteristic impedance definitions for these lines are compatible. The closed-form expressions derived in Chapter 2 are applied here for calculating the characteristic impedance and guided wavelength of three ridged SIWs which are used in the later design. Comparison between the approximate results calculated using closed-form expressions and those obtained using a commercial finite element method (FEM) package HFSS are plotted in Figure 3.2.

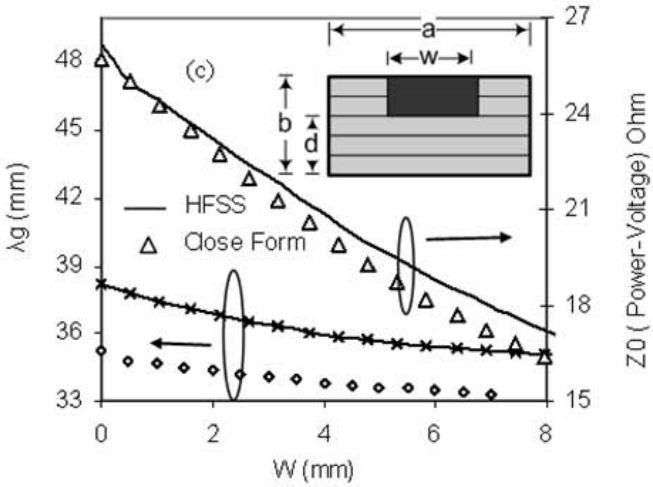
When using a ridged waveguide structure to design a transition between an SIW and



(a) a=6.88mm, b=0.508mm, d=0.254mm, ε_r =2.33;



(b) a=22mm, b=1.27mm, d=0.254mm, ε_r =2.94;



(c) a=0.762mm, b=1.27mm, d=0.254mm, ε_r =2.94;

Figure 3.2 Characteristic impedance (P/V) and wavelength.

a microstrip line, it is believed that a field matching and an impedance matching could be satisfactorily achieved when two conditions are met : $W = W_1 = W_2$ and $Z_{MS} = Z_{RSIW}$. For example, a ridged waveguide shown in Figure 3.2(a) can be used to design a transition between an SIW, which has the same outer dimension as this ridged waveguide, and a microstrip line, which may be sandwiched between two substrates. In order to find the best initial solution to this problem, characteristic impedance curves for the ridged waveguide and corresponding microstrip line, $W_1 = W_2$, are plotted in Figure 3.3. The line with rectangle markers is related to the impedance of a ridged substrate integrated waveguide with respect to W_2 and the other is for the impedance of a microstrip line regarding W_1. Values in Figure 3.3 are calculated at 25 GHz. Then the cross-point P_1 is the optimized solution that we figure out and it can be a good initial value of W_1 and W_2.

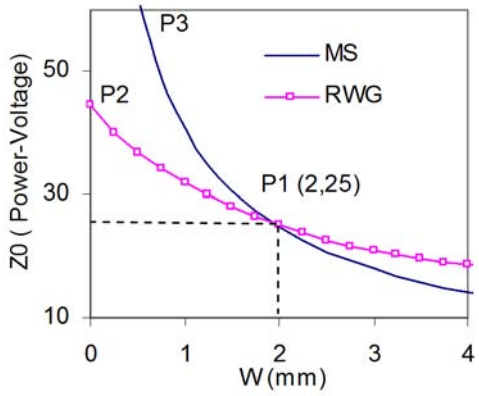


Figure 3.3 Power-voltage defined characteristic impedances of a microstrip line and a ridged SIW.

Two examples are carried out in this study to present the proposed transition between SIWs and microstrip lines in multilayer substrates. All circuits were fabricated using normal multilayer PCB technique. The metallic walls of ridge for the waveguide inside the structure are constructed by three thin metal grooves. These grooves are connected with a triangular metal sheet sandwiched between both substrates. The top and bottom of the waveguide are connected with two rows of via-hole arrays. Different types of tapers can be fabricated by changing the positions of via-holes or grooves. When the width of the grooves t, the radius of vias r and the distance between two neighboring grooves or vias d shown in Figure 3.2(c) are small enough, the leakage of field can be ignored. After taking an equivalent dimension transformation introduced in (Cassivi *et al.* (2002)), the approximate formulations of TRM derived in Section 2.2 are still useful.

Example 1

A back-to-back two-layer transition is designed and fabricated. Both substrates used in the process are Rogers 5870, $\varepsilon_r = 2.33$, $\tan\delta = 0.0012$ and $h_1 = h_2 = 10$ mil, which means the transform ratio equals to 1. According to the approach for finding the solution of an initial design introduced above, the SIW-to-microstrip transition can be modeled and designed in the following three steps.

Step 1 The width of waveguide is decided by the cut-off frequency k_c of the SIW since cut-off frequency of the ridged waveguide section is always lower.

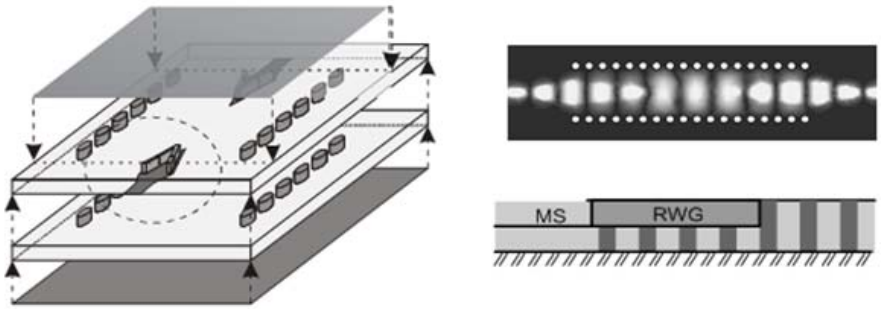
Step 2 With the help of the characteristic impedance curves plotted in Figure 3.3, an initial value for W_1 and W_2 can be found at P_1.

Step 3 A tapered microstrip line is then extended on one side to transfer the microstrip line from P_1 to P_3 to match any interconnection line. A tapered ridged waveguide is extended on the other side, from P_1 to P_2, where the ridged waveguide become a rectangular waveguide, as shown in Figure 3.3.

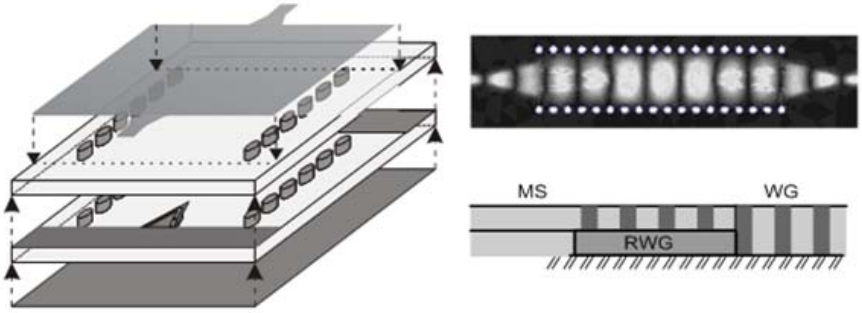
In this study, we gave two designs by putting the ridged waveguide in different substrate layer to implement two transitions. Which to be used is decided by the layout of the microstrip line circuits to be connected with the SIW. For transition 1 shown in Figure 3.4(a), the microstrip line is placed between two layers with a ground at the bottom of the entire substrate. For transition 2 shown in Figure 3.4(b), the microstrip line is put on the top of the whole substrate with the ground sandwiched between two substrate layers. The 3D configurations, side section view and top view of field propagation of the final transition designs are drawn in Figure 3.4(a) and (b) respectively. All design parameters are listed in the caption.

Compared to the final optimized dimension of the designs, the dimensions obtained using the above procedure proved good initial dimensions for both two designs. As shown in the field distributions, the lengths of both ridged SIW triangular taper and microstrip triangular taper are around one guided wavelength. It is because the first null of the reflection coefficient for a triangular tapered line occurs at $\beta L = 2\pi$. The value of the guided wavelength also has been approximately calculated using the formations of TRM.

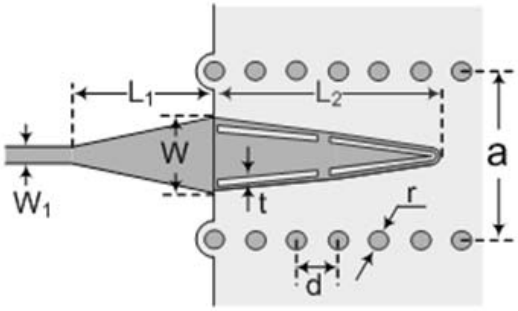
A through reflect line (TRL) calibration is used to measure the circuit with an HP8510 network analyzer and a Wiltron test fixture. Simulated and measured results of the transition are compared in Figure 3.5. A bandwidth of 14.5% at 15 dB return loss is obtained from 23.2 GHz to 27.1 GHz. The insertion loss is better than -1.5 dB within the pass band of interest. The length of one single transition is around 16.5 mm and the total length of the back-to-back transition is 43 mm.



(a) Transition 1



(b) Transition 2



(c) Top view

Figure 3.4 Configuration of a back-to-back two-layer transition. Design parameters are : Transition 1 : $L_1 = 5.46$ mm, $L_2 = 8.61$ mm, $W = 3.154$ mm, $t = 0.254$ mm, $d = 1.58$ mm, $a = 6.88$ mm, $W_1 = 0.711$ mm, $r = 0.3937$ mm ; Transition 2 : $L_1 = 5.46$ mm, $L_2 = 8.35$ mm, $W = 3.754$ mm, $t = 0.254$ mm, $d = 1.58$ mm, $a = 6.88$ mm, $W_1 = 0.711$ mm, $r = 0.3937$ mm.

Example 2

Theoretically, following the above procedure, an SIW-to-microstrip transition with any transform ratio can be easily made. The field is gradually transferred from a quasi-TEM mode for a microstrip line buried in the substrate to the TE_{10} mode of an SIW filled with

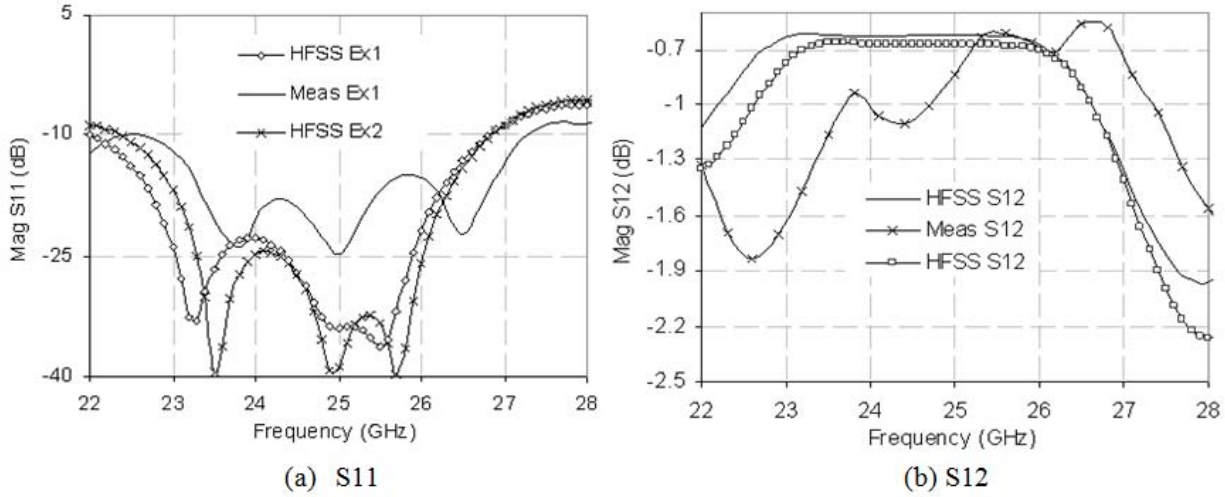


Figure 3.5 Simulated and measured S11 and S12 of two 2-layer back-to-back transitions.

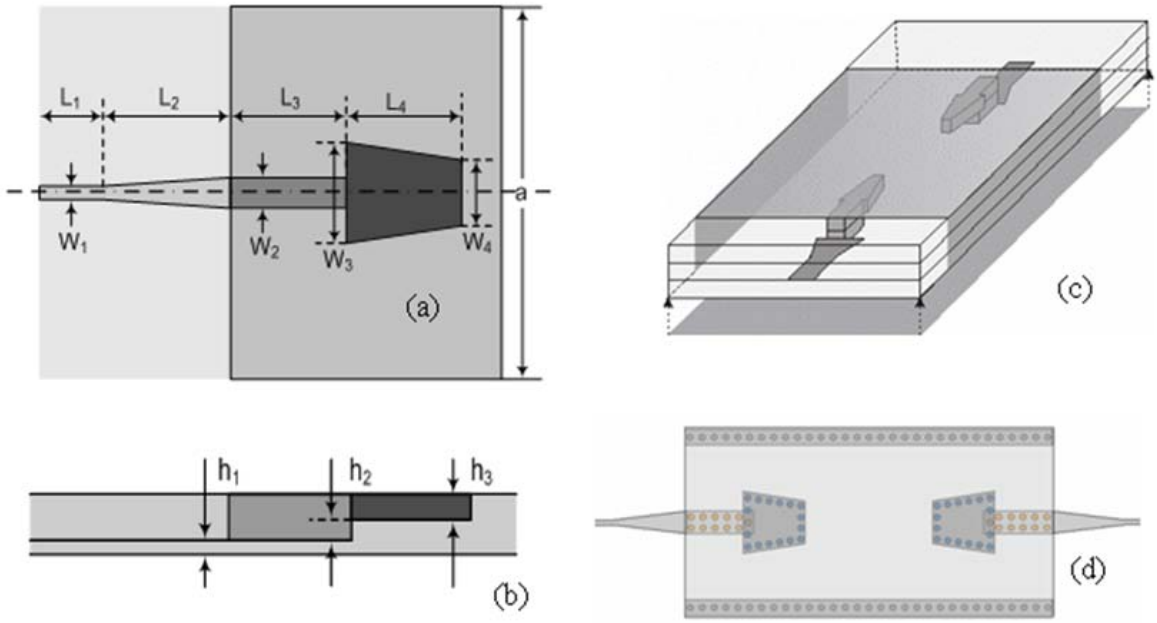


Figure 3.6 Configuration of a 3-layer back-to-back transition. Design parameters are : $L_1 = 2.5$ mm, $L_2 = 10$ mm, $L_3 = 7.5$ mm, $L_4 = 7.5$ mm, $W_1 = 0.64$ mm, $W_2 = 1.8$ mm, $W_3 = 6$ mm, $W_4 = 4$ mm, $h_1 = 0.254$ mm, $h_2 = 0.508$ mm, $h_3 = 0.508$ mm, $a = 22$ mm.

a multilayer substrate. However, the length of the transition is around one wavelength. And the length of the transition is related to the transform ratio α, a larger transform ratio value usually needs a longer transition length, which may be too long for the applications that have

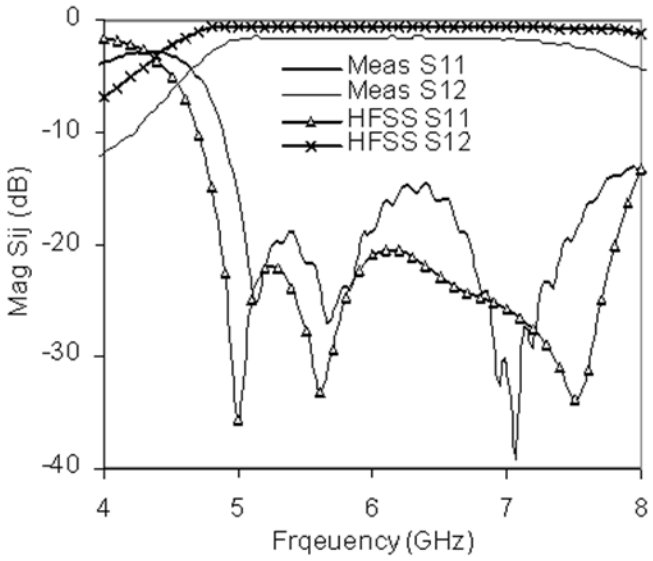


Figure 3.7 Simulation and experimental results of a three-layer back-to-back transition.

strict requirements on size. The total length of the transition can be shortened by using other type of taper such as an exponential taper or multisection tapers which are synthesized with more layers.

A C-band back-to-back transition is designed on a three-layer substrate as a multisection impedance transformer. The substrate is Rogers 6002, $\varepsilon_r = 2.94$ and $\tan\delta = 0.0015$. The thickness of two upper layers is 20 mil and, for the last layer on the bottom, the height of substrate is 10 mil. The transform ratio from the top of an SIW to the layer supporting the microstrip line is $\alpha = 4$. Three dimensional configuration and parameters of the transition are given in Figure 3.6. The ridges in the transition can be made using one single groove in Figure 3.6(c) or some via-hole arrays in Figure 3.6(d). The former is used in our design for simplicity. Figure 3.7 shows the simulated and measured results. As shown in Figure 3.6(b) and (c), length of the ridged waveguide part of such a transition should be longer than 30 mm if using triangular taper matching. Using the 2-step ridged waveguide impedance matching circuits, total length of the ridged waveguide part is 15 mm.

This transition provides an effective way to integrate an SIW with buried microstrip line circuits on a multilayer substrate. The integration of low-loss SICs becomes attractive in more performance-demanding microwave integrated circuit (MIC) or monolithic microwave integrated circuit (MMIC) applications using the multilayer substrate technologies.

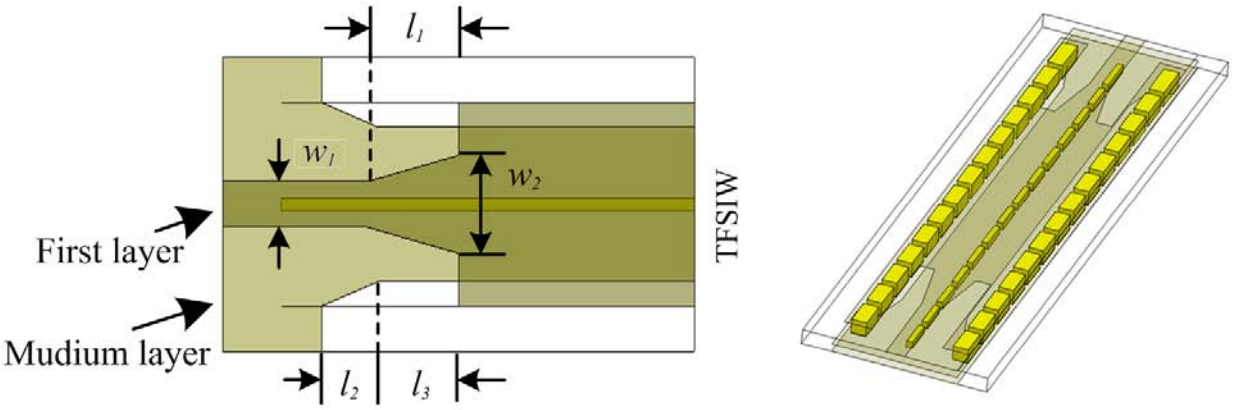


Figure 3.8 Design layout of the microstrip-to-TFSIW transition.

3.2.2 Microstrip-to-TFSIW transition

A microstrip-to-TFSIW transition (Figure 3.8) is designed for measurement purpose in many design examples introduced in this thesis. This transition is from a TFSIW to a microstrip line in the upper layer only, which means the ground of microstrip line is sandwiched between two substrate layers. The extended sidewalls of the TFSIW connect the ground of the microstrip line with a metal plate at the bottom of the substrate. The impedance matching theory cannot be used in this design because of the complexity of the structure. A broadband matching is achieved by adjusting the dimensions of the microstrip parameters, l_1, w_1, and w_2, and the parameters of ground, l_2 and l_3. Based on the dimensions listed in Table 3.1, the simulated return loss of a back-to-back microstrip-to-TFSIW transition is lower than -25 dB within the frequency band $22 \sim 30$ GHz, as shown in Figure 3.9.

In practice, some plated via holes are placed in the lower layer below the mirostrip line and close to the edge of circuit. By doing this, when a test fixture clips the substrate in a measurement, a solid connection between the ground of the fixture and the ground of microstrip line in middle of the substrate can be established. However, a TRL calibration with a set of kits having the same transitions can remove the so-caused reflection in an even better way.

Unit : mm	w_1	w_2	l_1	l_2	l_3
	0.65	1.4	1.95	1.2	1.7

Tableau 3.1 Dimensions of the microstrip-to-TFSIW transition.

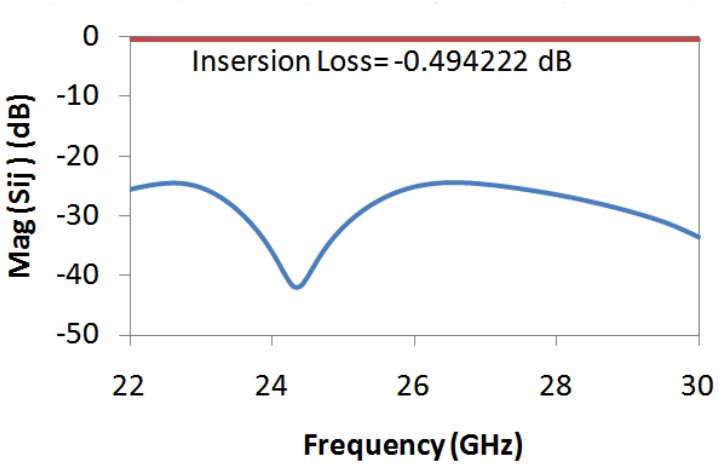


Figure 3.9 Simulated S-parameter of a back-to-back microstrip-to-TFSIW transition.

3.2.3 TFSIW-to-SIW transition

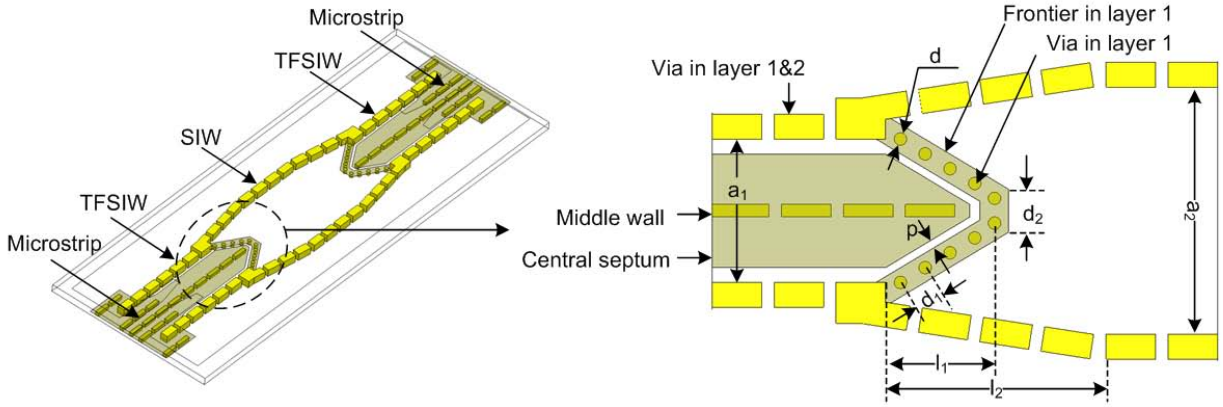


Figure 3.10 Layout and dimension of a TFSIW-to-SIW transition.

This section gives an example of transition from a TFSIW to an SIW, both of which are in a double layer substrate as shown in Figure 3.10. The difficulty in such a transition design comes from several differences between these two structures, the field distribution (as shown in Figure 3.11), the geometry size, the propagation constant and the characteristic impedance. A straightforward way for obtaining such a transition is to decompose the design into two, (1) a transition from TFSIW to RSIW and (2) another transition from RSIW to SIW. Although such a design can be expected to have a broad bandwidth performance, it will also be very cumbersome. It is well known that a tapered transition is usually a quarter wavelength long, therefore a design with two tapers will be as long as one wavelength. In this

section, we give a very compact design of such a transition.

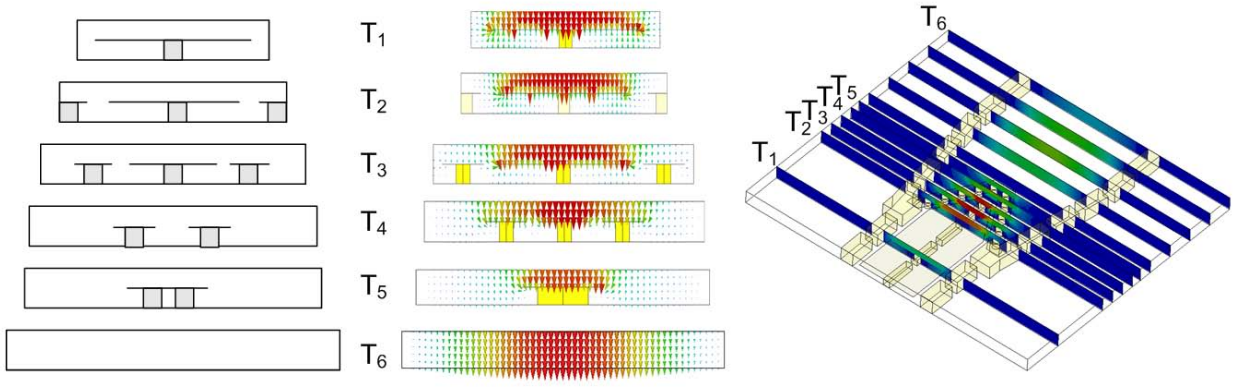


Figure 3.11 Field distribution in a TFSIW-to-SIW transition.

The layout of the proposed back-to-back TFSIW-to-SIW transition is shown in Figure 3.10. A pair of TFSIW-to-microstrip line transitions proposed in the previous section are added into the circuit for measurement purpose. The dimensions of a single transition are given in the top view of the layout shown in Figure 3.10. In Figure 3.11, a serial of cross sections have been made along the transition. T_1 is within the TFSIW and T_6 is within the SIW. In T_2, T_3, T_4 and T_5, the width of the central septum is gradually decreased and a pair of obstacles in lower layer get close to the middle wall at the same time. In the lower layer, the frontier in layer 1 synthesized by a row of plated via holes plays an important role for the field of TFSIW transforming into a RSIW type, instead of directly into an SIW type. This taper not only helps the field transformation from TFSIW to RSIW type in the lower layer but also assists the field changing from RSIW to SIW type in the upper layer.

Unit : mm	a_1	a_2	p	d	d_1	d_2	l_1	l_2
	2.9	5	0.15	0.25	0.58	0.87	2.2	4.45

Tableau 3.2 Dimensions of a TFSIW-to-SIW transition.

The dimensions of an optimized design is given in Table 3.2. Except those dimensions for defining the plated vias, such as d, p, d_1 and d_2, there are two primary variables for tuning the reflections, the length of the taper in the lower layer l_1 and the length of the waveguide taper l_2. By observing an H-plane filed distribution, we can conclude that the value of l_2 is about a half wavelength and the value of l_1 is around a quarter wavelength. The gap width p is the minimum trace to trace tolerance we can use in fabrication. As shown in Figure 3.12, the measured S-parameters match the simulations quite well. There is still some difference when

the reflection is lower than -20 dB, which is probably caused by the error in the fabrication and calibration.

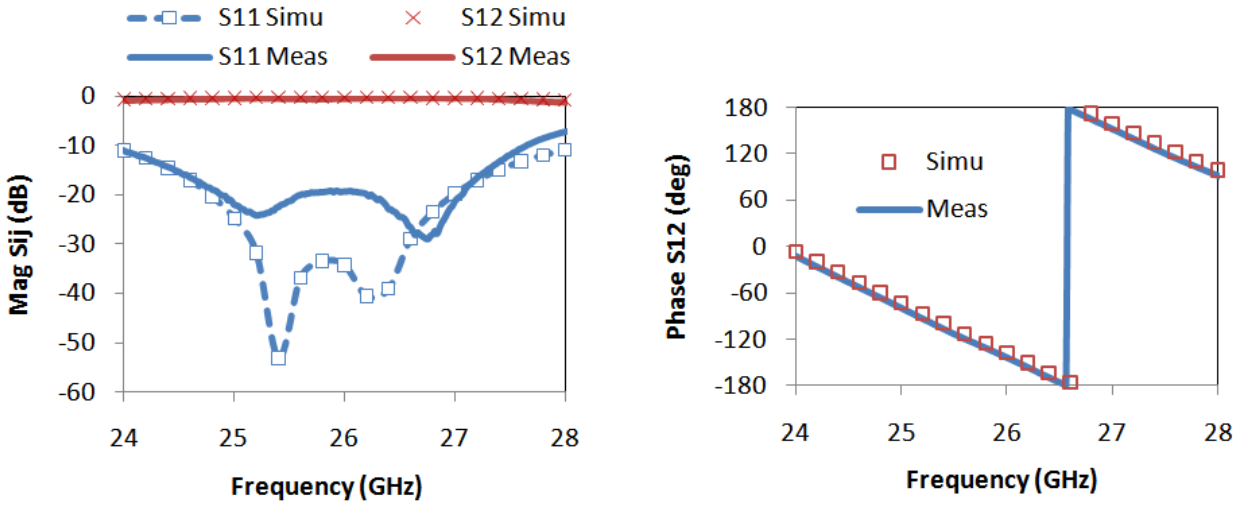


Figure 3.12 Simulated and measured S-parameter of a TFSIW-to-SIW back-to-back transition.

3.2.4 SIW-to-SIW transition

Compared with the conventional air-filled metal waveguide, one advantage of SIW circuits is that it is easy to be integrated in planar circuits. A design of SIW based on multilayer technique can make this predominance more pronounced. When the functional components in a large design are separated in different substrate layers, the size of the entire design can be drastically reduced. Moreover, the overall performance of the design can be improved because of the shorter connections and less loss on the routing. This is based on the assumption that a connection between layers can provide the same bandwidth and reflection performance as a transition in a single layer does. A reliable and broad bandwidth transition between SIWs in different layers is a very important feature which can determine the performance of the entire design.

As shown in Figure 3.13, an SIW transition is designed and fabricated in our own workshop. Two SIWs in different layers are coupled with each other through a large aperture on their broad walls. The design of the transition can be regarded as a two pole filter. The field distribution is shown in Figure 3.14. In order to get an optimized design, the dimension of the apertures l_2 and l_3 and the distance from the center of the aperture to the short plane of the waveguide d need to be tuned first to locate the first pole around the center frequency.

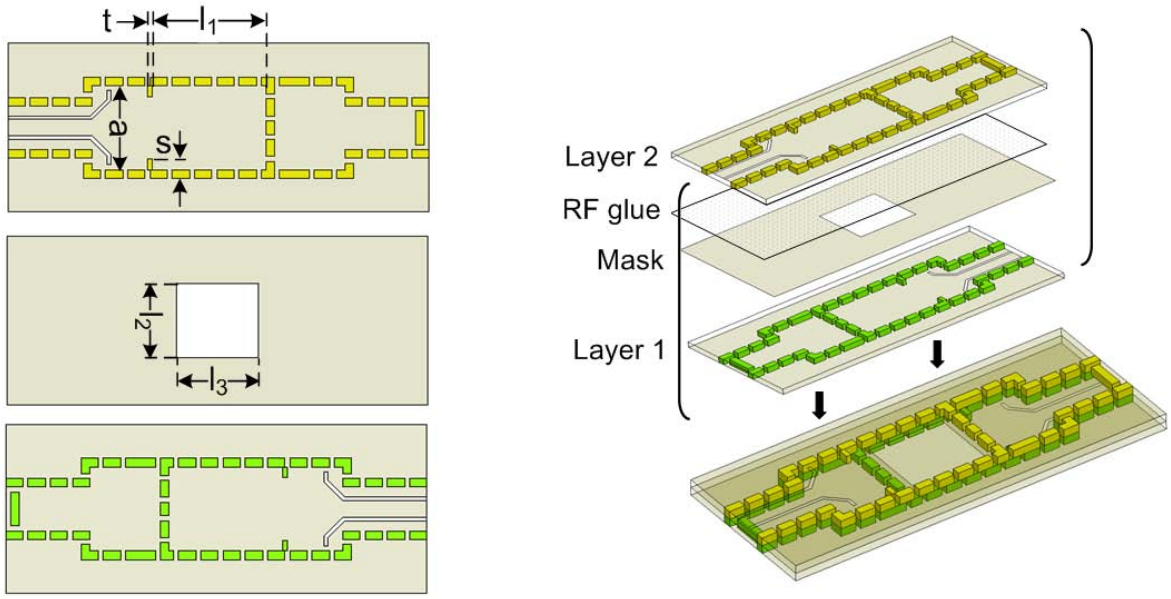


Figure 3.13 Layout of an SIW transition in a two-layer substrate.

Then two pairs of inductive slots are added into the structure which provides another pole of the reflection. The location l_1 and the length s of the slots can be tuned for a good reflection within a broad bandwidth. The dimensions of the final optimized design are listed in Table 3.3.

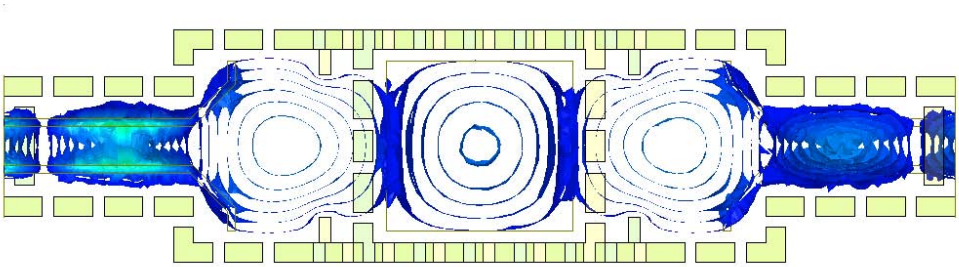


Figure 3.14 Filed distribution of an SIW transition in a two-layer substrate.

Unit : mm	l_1	l_2	l_3	d	s	t
	6.75	4.4	4.8	6.75	0.65	0.3

Tableau 3.3 Dimensions of an SIW-to-SIW transition.

Unlike the multilayer fabrication based on semiconductor technique or co-fired ceramic technique, we used a thin layer of RF glue to stick multiple substrate layers together. This

process can create a thin gap between different layers and block the direct electric contact between them. Although a proper pressure can decrease the final thickness of the glue to $1 \sim 2$ um, we are concerned that it can degrade the performance. Therefore, we did the experiment with and without the layer of RF glue. The two SIWs shown in Figure 3.13 are fabricated individually at first, the middle mask with the coupling aperture is made on both the two substrates, at the bottom of the upper layer and on the top of the lower layer. The two substrate layers are then stacked together and fixed with a pair of screws beside the SIWs. A metal gasket is used to add an extra pressure above the region of the aperture. In the second experiment, we use the RF glue to assemble two layers together. Two experiment results and corresponding simulation results are all compared in Figure 3.15. As we can see in these two figures, when the two layers are mechanically connected without the RF glue, the insertion loss of the transition decreases to about 0.5 dB at 26 GHz. The level of the worst reflection within the interested frequency band is below -25 dB. If we consider the fabrication tolerances and measurement errors, the experiment result has a good coincidence with the simulation, for both magnitude and phase. The difference between two simulations of the transition with and without RF glue is not obvious. However, the difference of these two cases in experiments are quite obvious as we can observe from Figure 3.15. In order to get this result, a pressure is added at the aperture area, which means the degeneration of the performance is mainly caused by the gap between two substrate layers.

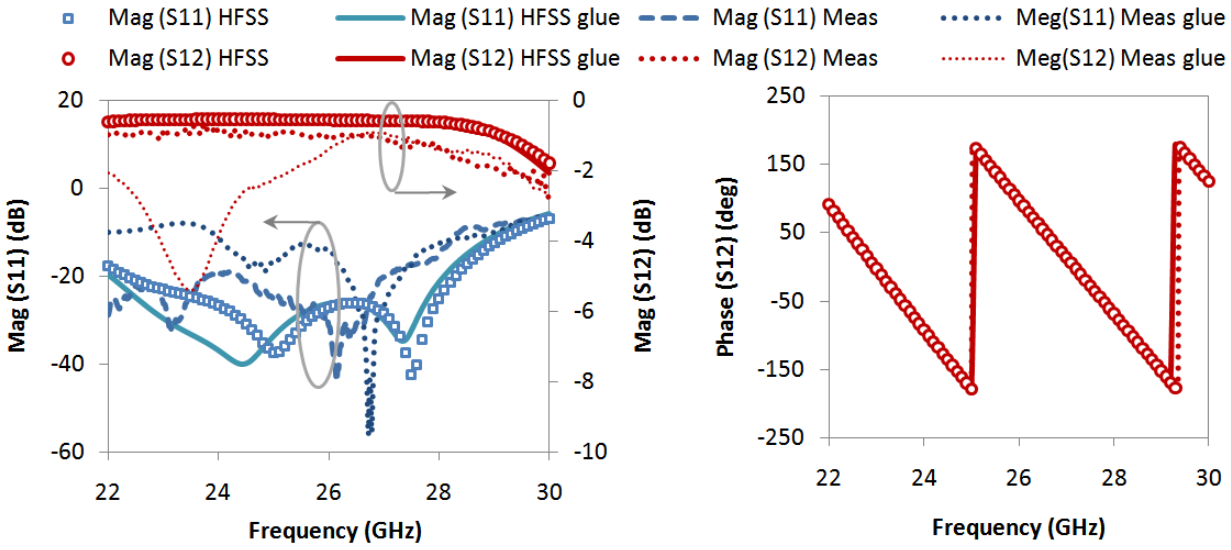


Figure 3.15 Simulation and measurement of an SIW transition in a two-layer substrate.

From this experiment, we conclude that when the electric connection between layers can be guaranteed, an SIW-to-SIW transition can easily have a 25% bandwidth of reflection low

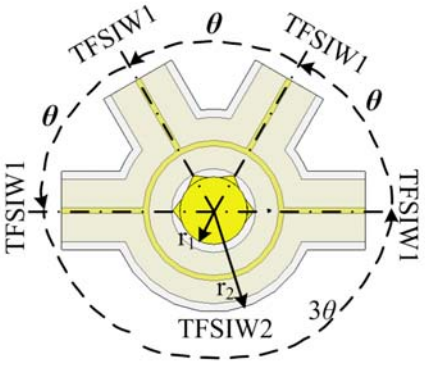
than -20 dB. An even wider bandwidth can be expected if more inductive slots are used while the insertion loss is increased simultaneously. However, the performance of the transition will get worse when the electric connection between different layers cannot be established, for example when a layer of RF glue is used in our mutilayer fabrication process. This problem needs to be considered when we conduct the multilayer SIW circuit design. When the pattern of the plated via holes in two layers are the same, it is highly recommended that we drill and plate these via holes together after the substrates have been stacked up.

3.3 TFSIW hybrid ring

A T-septum waveguide is proposed for achieving a better bandwidth and impedance performance as a ridged waveguide does. TFSIW, a scenario proposed as a miniaturization technique for reducing the broadside dimension of SIW (Grigoropoulos et Young (2004)), can be looked as a T-septum waveguide that is implemented in a double-layered substrate. Corresponding to another type of the folded SIW, i.e. C-type folded waveguide (CFSIW) (Grigoropoulos *et al.* (2005)), an SIW with horizontally symmetric septa is generally called T-type folded SIW. Different from the T-septum waveguide, a TFSIW is fabricated using a printing and via-hole technique in planar substrate. The thickness of the septum can be treated as infinitely thin. The sidewalls and the horizontal partition walls are formed by rows of via holes or plated slots. The structure of TFSIW is very suitable for multilayer substrate technologies. In this section, the propagation constant and characteristic impedance of TFSIW structures are analyzed on the basis of their equivalent circuits. To demonstrate the circuit applications, the design procedure of a proposed TFSIW hybrid ring is presented and discussed with reference to the calculated parameters. Simulation results of the designed coupler ring circuit are compared with measurement results.

Hybrid ring is an important component which has many applications in mixer and phase shifter design. A high isolation H-plane hybrid ring has been designed based on the SIW technique (Che *et al.* (2006)). It is well known that the distance between arms are $\lambda_g/4$ and $3\lambda_g/4$, respectively, where λ_g is the wavelength at the center frequency. However, because of a large broadside dimension of the SIW, the distance between adjacent arms has to be extended from $\lambda_g/4$ to $5\lambda_g/4$ (Che *et al.* (2006)). When the design is conducted using TFSIW structure, there is no such sacrifice because of the half reduced broadband dimension. The total size of the hybrid ring based on TFSIW is then much smaller than its counterpart based on the SIW technique. In this section, we will use the parameters calculated in section 2.3.1 to design a TFSIW hybrid ring.

A schematic of TFSIW hybrid ring is given in Figure 3.16. The theory for designing such



	TFSIW1	TFSIW2
a	2.9 mm	2.5 mm
s	2.3 mm	1.9 mm
w	0.2 mm	0.2 mm
Z	23 Ohm	31.5 Ohm
λ_g	8.7 mm	10.1 mm

Figure 3.16 TFSIW hybrid ring and dimensions of the initial design.

a coupler is classical and quite straightforward, which can be summarized as follows : 1) the impedance of TFSIW2 is $\sqrt{2}$ times of the TFSIW1 ; 2) the distance between adjacent arms is θ and the long distance between the two opposite arms is 3θ, where θ equals to $\lambda g/4$. Furthermore, two additional rules need to be considered : 1) to keep the two TFSIWs working under single mode condition ; 2) to suppress the loss by choosing proper values of a and s/a. According to the conclusion drawn in Part 2.3.1 (Attenuation constant) of Section 2.3.1, the ratio s/a of the two TFSIWs should be kept within the range $[0.7, 0.8]$.

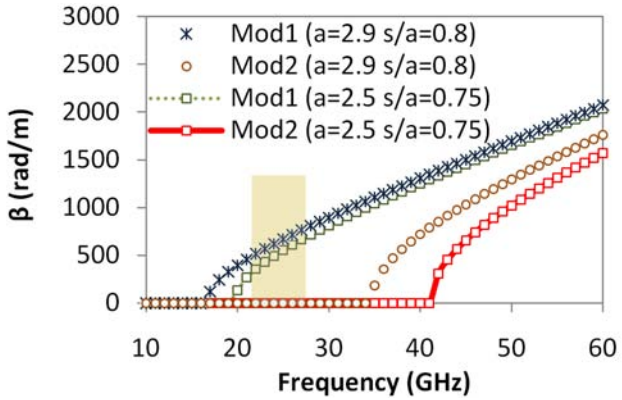


Figure 3.17 Dispersion curves of the dominant mode and first high order mode in TFSIW1 and TFSIW2.

A procedure for designing a TFSIW hybrid ring is as follows.

Step 1 Use the formulations in Equation 2.44 to make a table of impedance where a is adjusted around a half width of normal SIW and s/a is within $[0.7, 0.8]$.

Step 2 In the table obtained in step 1, find two numbers and one is around $\sqrt{2}$ times of the other. In our design, Z_1 and Z_2 are set up as 23 Ohm and 31.5 Ohm, respectively, corresponding to $s_1/a_1 = 0.8$, $a_1 = 2.9$ mm and $s_2/a_2 = 0.75$, $a_2 = 2.5$ mm.

Step 3 Verify the single mode condition by drawing the dispersion curves of the dominant mode and the first high order mode in TFSIW1 and TFSIW2 as shown in Figure 3.17. The yellow region is the frequency band of the hybrid ring to be designed.

Step 4 Calculate the wavelength of TFSIW2 λ_{g2} at center frequency using the phase constant solved in step 3. The inner and outer radius of the ring can be obtained by using Equations 3.1 and 3.2, where a_2 is the width of the TFSIW2 obtained in step 2.

$$r_1 = \frac{3\lambda_{g2}}{4\pi} - \frac{a_2}{2} \tag{3.1}$$

$$r_2 = \frac{3\lambda_{g2}}{4\pi} + \frac{a_2}{2} \tag{3.2}$$

In our design, λ_{g2} of the TFSIW2 given in Figure 3.16 is 10.2 mm, then the initial values of r_1 and r_2 are 1.18 mm and 3.68 mm, respectively.

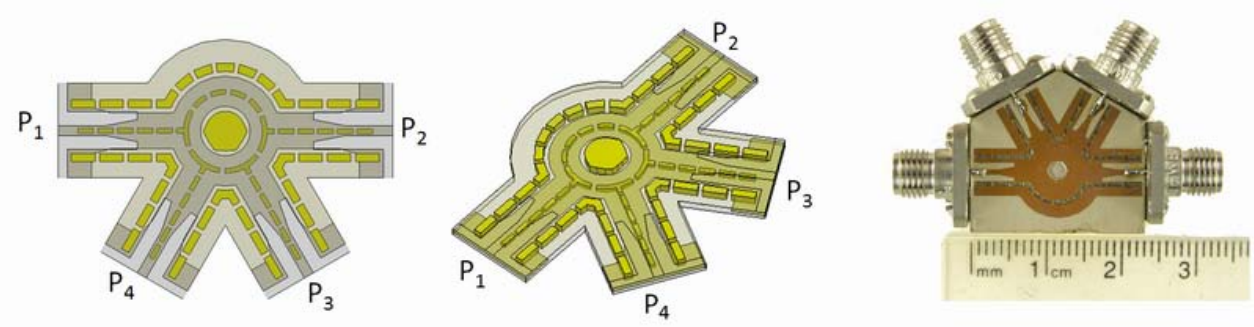


Figure 3.18 Top view, 3D view and picture of fabricated hybrid ring.

Following the above-described steps 1-4, an initial design of the proposed TFSIW hybrid ring can be obtained without any full wave simulation. A fine tuning is required based on the initial design. After a fine tuning in our design, most dimensions of the TFSIW1 and TFSIW2 remain the same as in the initial design, except $r_1 = 1.23$ mm and $r_2 = 3.72$ mm. A transition from microstrip line to TFSIW is designed for measurement purpose. In order to enhance the bandwidth and improve the return loss of the design, some mechanisms can be involved at the junctions connecting the arms and the ring. It can be metal posts (Che *et al.* (2006)) or simply changing the shape of the inner conductor which is used in our design.

The top view, 3D view and final fabricated circuit of the hybrid ring are given in Figure 3.18. The total size of the layout is 16.5×21.2 mm^2. The full wave simulation results of the hybrid ring with microstrip line to TFSIW transitions are given in Figure 3.19. The bandwidth with reference to the return loss at all four ports and isolation is 12.7% (24.1 $\sim$ 27.3

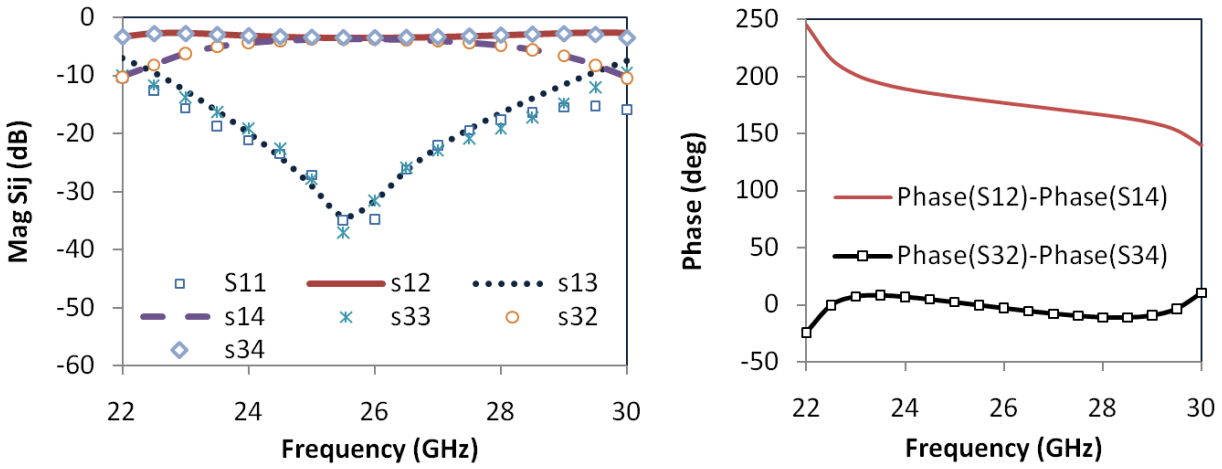


Figure 3.19 Simulation results of the TFSIW hybrid ring.

GHz), less than -20 dB. The insertion loss is 3.7 dB at the center frequency (26 GHz) and better than 4.3 dB within the above broadband. The phase difference between S12 and S14 is $180° \pm 3°$ at the center frequency and $180° \pm 10°$ within the band ($24.1 \sim 27.3$ GHz).

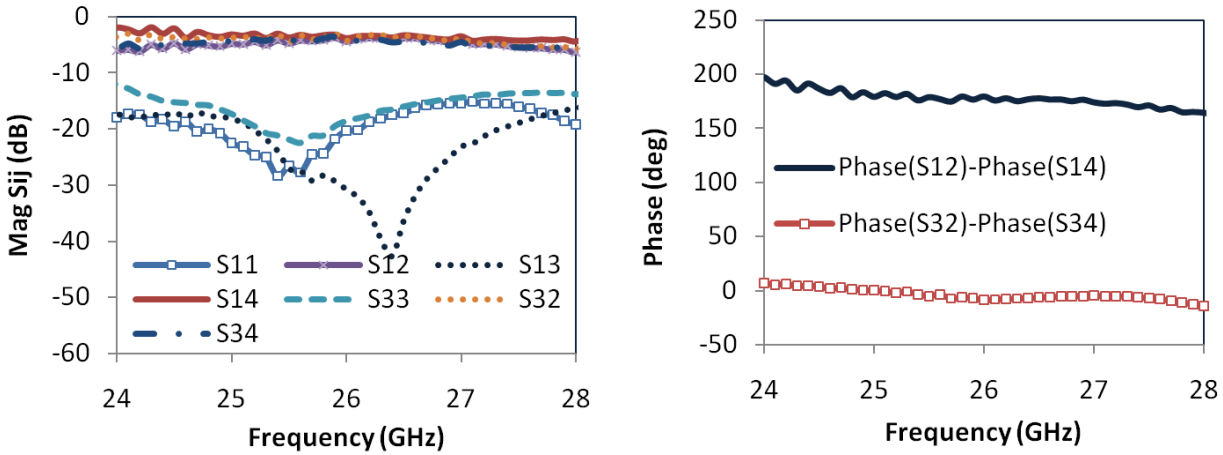


Figure 3.20 Measurement results of fabricated TFSIW hybrid ring.

The proposed TFSIW hybrid ring is fabricated in our own lab using a multilayer PCB technique. All vertical walls are constructed by plated slots cut by laser. Two substrates are stuck together using high-frequency glue which effect is not considered in simulation. Four K-connectors are soldered for measurement. Limited by our in-house fabrication accuracy, especially the alignment for substrate laminating, the measured results of the fabricated

circuit are shifted by 2.1 GHz as shown in Figure 3.20. Within the band 27.6 $\sim$ 28.8 GHz, the isolation between isolated ports and the return loss at each port are better than 20 dB and 15 dB, respectively. At the center of this band, the insertion loss of S12 and S14 are 4.7 dB and 4.9 dB, including the effect of the K-connectors which are not involved in simulation. It is believed that the performance of the circuit can be improved with a better fabrication condition. For in-phase mode, the phase imbalance and magnitude imbalance are 12% and 8%, respectively. The phase imbalance and magnitude imbalance of the out-of phase mode are 18% and 14%, respectively.

3.4 HMSIW six-port

A six-port junction circuit is a passive interferometer device which mainly consists of several couplers and power dividers. Six-port junctions based on various design techniques such as microstrip line, stripline, metallic waveguide and SIW, have been studied over the past ten years. In this section, we propose, design and demonstrate two six-port junction circuits for K-band direct-conversion transceiver system based on the HMSIW technique. The two junctions are studied and implemented with different architectures according to the requirement of some specified design. One six-port junction with four couplers is utilized to provide a high isolation suitable for the use as a reflection type I/Q modulator. In order to simplify the design without affecting the circuit function, a phase shifter in this six-port junction is moved to the end of two arms of the junction. The other six-port alternative circuit suitable for the design of a direct-conversion receiver is examined and implemented with a more common architecture which is comprised of three couplers and one power divider. Theoretical and experimental results are presented and discussed.

Three types of components are required for the design of a six-port junction, a T-junction, a directional coupler and a 50 Ohm load for the terminal matching. Each part is designed separately and implemented by using the HMSIW technique. All HMSIWs used in each section are kept with the same width to guarantee a smooth connection between every two parts in a later assembling process. Design of necessary HMSIW/SIW-to-microstrip transitions is carried out by following up a previous work (Liu *et al.* (2007)).

To keep the design in a symmetric manner, we use an SIW as the input arm. Two splitting arms are implemented using the HMSIW sections. A circular conductive post is put inside of the junction for creating a matching condition. The primary parameters for tuning are the radius of post r, the location of post L_1, the length of transition L_2, and the depth of bend L_3. The insertion loss of an optimized design is depicted in Figure 3.21. The phases over the two arms are completely synchronized.

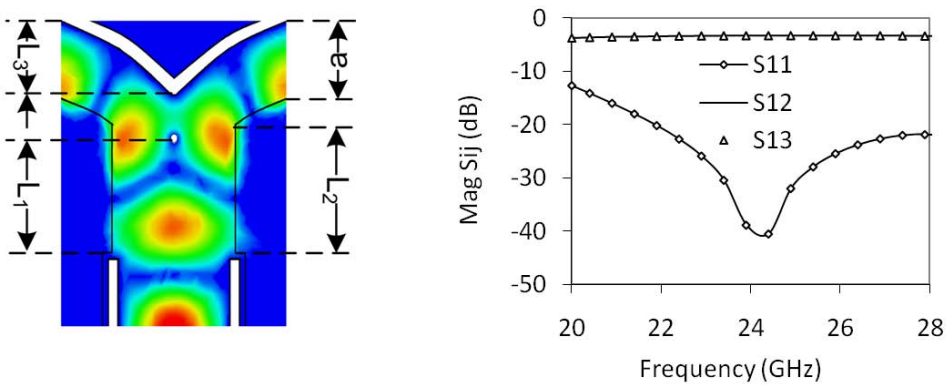


Figure 3.21 HMSIW T-junction : $a = 3.3$ mm, $r = 0.18$ mm, $L_1 = 4.89$ mm, $L_2 = 5.53$ mm, and $L_3 = 3.21$ mm.

50 Ohm termination

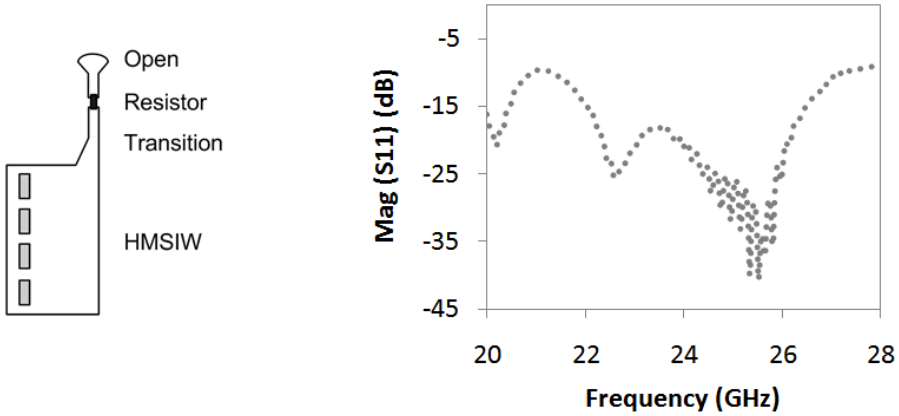
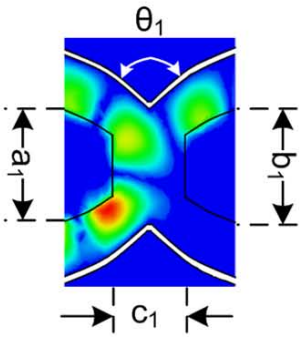


Figure 3.22 Measurement of a 50 Ohm termination to an HMSIW.

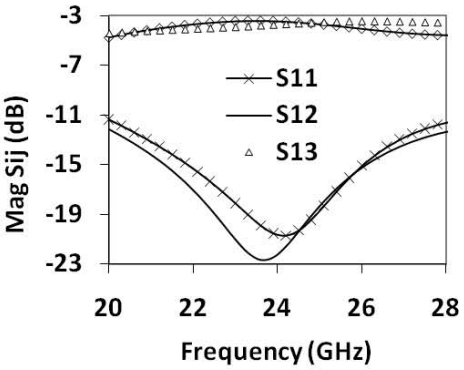
A traditional way in making a matching termination for a waveguide type structure is to add an absorber at the end of the waveguide. However, this method is no longer convenient for an SIW structure because of the assembling problem. In this chapter, we make use of a transition to transfer the HMSIW to a microstrip line which is terminated with a surface mounted 50 Ohm resistor. It can achieve a return loss better than -15 dB from 22 GHz to 26.5 GHz, as shown in Figure 3.22.

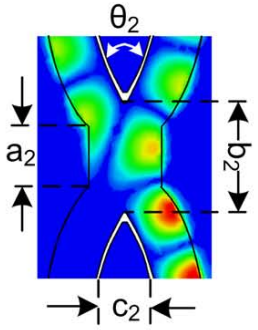
Directional coupler

Two HMSIW coupler designs are described in Figure 3.23. The performance of those couplers is optimized by changing the dimensions of coupling portion a, b, c as well as the

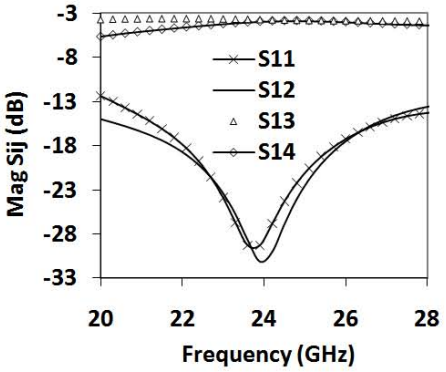


(a) Coupler 1



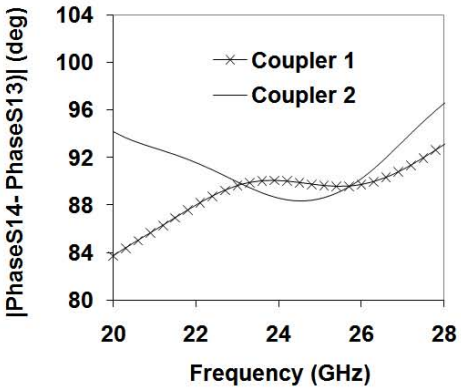


(b) Coupler 2



(mm)	C1	C2
a	3.69	3.73
b	6.48	4.93
c	5.13	6.88
θ	105°	62°

(c)



(d)

Figure 3.23 (a) and (b) present, respectively, return loss and insertion loss in each arm of the optimized couplers. (c) is the dimensions of the couplers. (d) gives the phase difference between the direct arm and the coupling arm.

angle of arm θ. The six-port junctions designed in this work are expected to operate within the frequency band of $23 \sim 25$ GHz. In order to reduce the circuit size as much as possible, the arms of the couplers are bent. Simulated S-parameters of two couplers are shown in Figure 3.23.

Two six-port junctions are integrated with the building components that we have discus-

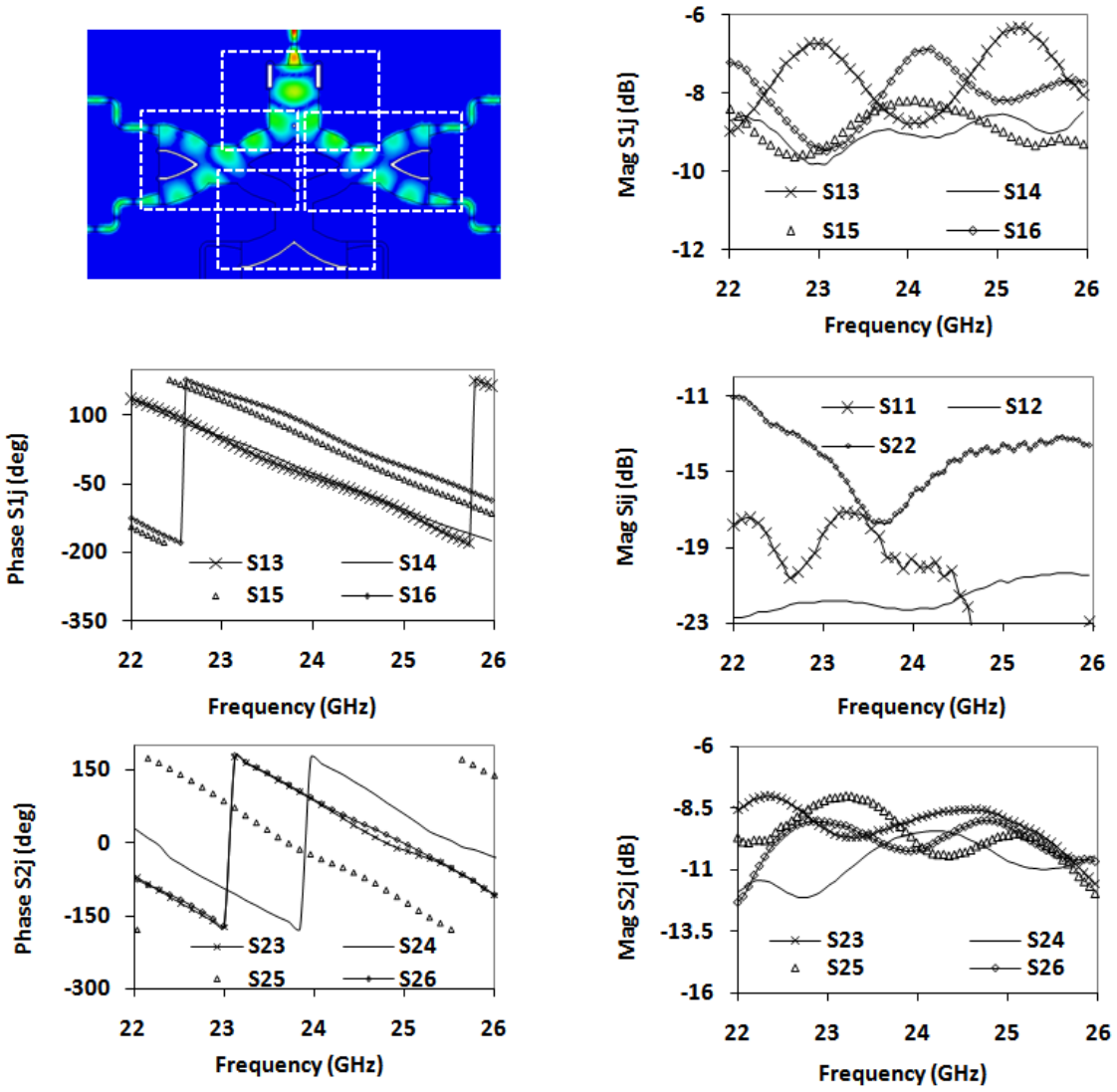


Figure 3.24 Six-port junction of a direct-conversion demodulator.

sed and designed. The field distributions of the junctions are illustrated in Figure 3.24 and Figure 3.25. The six-port junction in Figure 3.24 is for the demodulator used in a direct-conversion receiver while the six-port junction in Figure 3.25 is developed for modulator in the form of a reflection-type transmitter. For clarity, the components designed in the previous section are enclosed in rectangles drawn on the layouts. In order to reduce the circuit size, there are some overlaps between adjacent component parts. The final size of junction 1 in Figure 3.24 is 33 mm $\times$ 56 mm and the size of junction 2 in Figure 3.25 is 31 mm $\times$ 56 mm. Measured S-parameters of the two six-port junctions are also given in Figure 3.24 and Figure 3.25. Junction 1 has a better performance on both the transmission coefficients and the

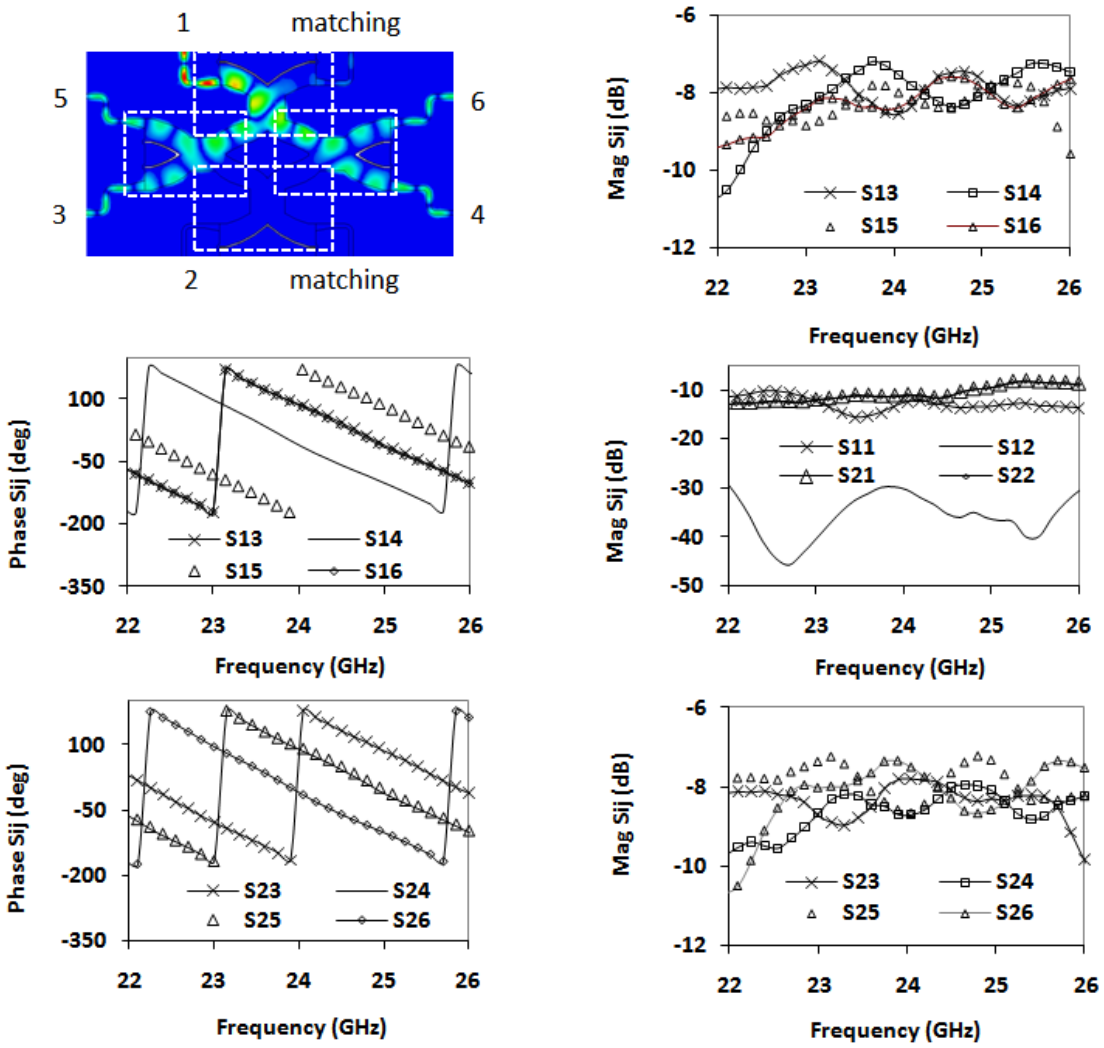


Figure 3.25 Six-port junction for a reflection-type transmitter.

isolation (S12). All the designs have used Rogers 6002 substrate with $\varepsilon_r = 2.94$ and $h = 0.254$ mm. A through-reflect-line (TRL) calibration has been used to remove discontinuities caused by the connectors. The results are measured with an HP8510 network analyzer within the frequency band from 22 GHz to 26 GHz.

3.5 TFSIW five-port junction

A symmetric 5-port junction is utilized in two important microwave applications. A reflectometer topology proposed by Riblet et Hansson (1981) comprising a matched symmetrical five-port waveguide junction and a directional coupler, was proved capable to satisfy the op-

timum performance criteria of the reflectometer for measuring the reflection coefficients of a device under test. Many versions of the five-port junction have been implemented using microstrip line (Kim *et al.* (1984)), stripline (Hansson et Riblet (1983)) and metallic waveguide structures. The bandwidth of the microstrip line and stripline design can be as high as 76% (Yeo et Choong (2001)) which is very suitable for making a broadband reflectometer.

Another application attracted much more attention in the past decade is the multi-port homodyne demodulator in a direct conversion receiver or transceiver (Li *et al.* (1995)), where a passive six- or five- port junction functions as a passive mixer together power detection diodes. For millimeter wave applications, waveguide devices are always preferred because of their high quality factor. Although the bandwidth of waveguide devices is usually less than 50% in order to follow the single mode condition, a device which can cover a full waveguide bandwidth (from $1.1f_c$ to $1.8f_c$, where f_c is the cut-off frequency of the waveguide) is still good enough for a direct conversion receiver in millimeter wave band. A five-port waveguide junction has five rectangular waveguides connected to a central cylinder cavity at $2\pi/5$ angular intervals. Except the design proposed by Riaziat et Zdasiuk (1985), most waveguide junctions are coupled in E-plane. This is because an H-plane junction is too bulky and cumbersome. In this section, we demonstrated, designed and fabricated two five-port junctions based on TFSIW technique for 26 GHz direct conversion receiver applications. The two junctions are both coupled with each other in H-plane.

Several adjusting mechanisms have been used to broaden the bandwidth of a waveguide junction without ruining its symmetry. A segment of tapered waveguide can function as a transition between the central cavity and each standard waveguide arm in either E-plane (Cullen et Yeo (1988)) or H-plane (Riaziat et Zdasiuk (1985)) coupled waveguide junctions. Riblet (1983) inserted inductive diaphragms in waveguide arms which gave a more compact design than the tapered waveguide. Yeo et Qiao (1994) combined several adjustment elements in one design : five inductive diaphragms at the joints, a metallic rod at the center of the cavity and a layer of dielectric sleeve surrounding the metallic rod for creating an oversized cavity.

In this section, the proposed SIW five-port junctions are H-plane coupled because an E-plane coupled junction is unpractical for SIW technique, in which the thickness of substrate needs to be equal to the broadside dimension of waveguide. In order to make the design more compact, we exploit the TFSIW structure in this design. TFSIW is a good candidate for creating a miniaturized SIW design and it has a high compression ratio close to 2. Limited by the structure characteristics, metallic post and tapered waveguide are utilized as the adjustment elements to improve the matching.

The proposed five-port junctions are designed in a two-layer substrate, both of which are

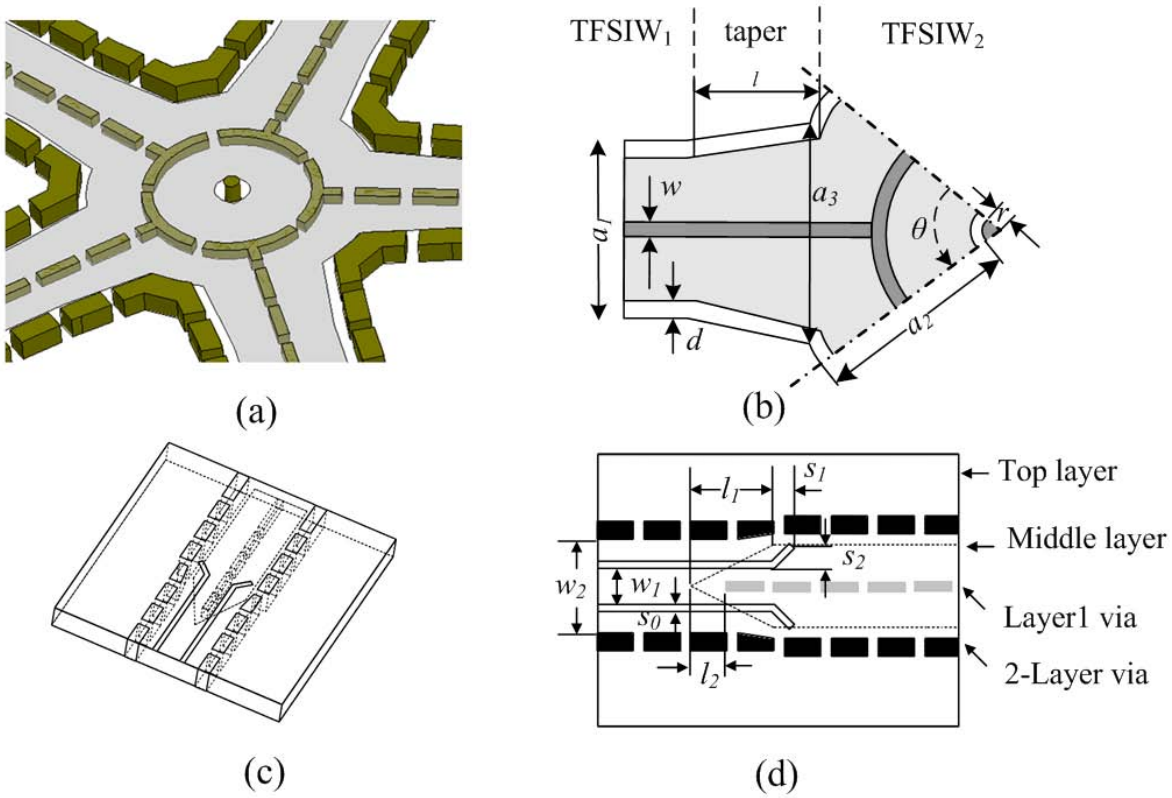


Figure 3.26 3D layouts of (a) an untapered five-port junction with (c) a TFSIW-to-MS transition in upper layer, and (b) a tapered five-port junction with (d) a TFSIW-to-MS transition in lower layer.

RT/Duroid 6002 with thickness 0.254 mm, dielectric constant $\varepsilon_r = 2.94$, and loss tangent $\delta = 0.002$. The broadside dimension of TFSIW is first decided by the single mode condition and minimum loss criteria. Loss and compression ratio need to be compromised when the width (d) of the septum between two layers is selected. Each adjacent pair of ports can be considered to be connected by a transmission line of electrical length d and characteristic admittance Y.

Unit : mm	a_1	a_2	a_3	w	d	l	r
untapered	2.9	3.08	2.9	0.2	0.3	0	0.23
tapered	2.9	3.27	3.23	0.2	0.3	2.1	0.23

Tableau 3.4 Dimensions of the tapered and untaperd five port junctions.

Two TFSIW five-port junctions (Figure 3.26(a) and (b)) are designed in this work. Because of the symmetry, only 1/5 of the design layout with all dimensions is shown in Figure 3.27. All values related to dimensions are listed in Table 3.4. The untapered junction

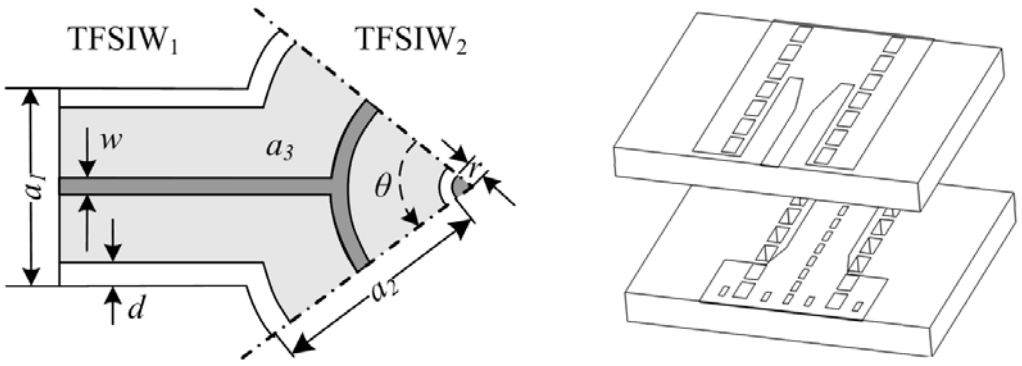


Figure 3.27 1/5 layout of the five-port junction with all dimensions.

(Figure 3.26(a)) is more compact and easier to be designed. There are only two independent adjustment elements : the radius (r) of the central post and the width (a_2) of the TFSIW$_2$ (Figure 3.27). In order to improve the bandwidth performance, a segment of taper is added into the second design (Figure 3.26(a)) and the width (a_3) and length (l) of the taper are adjustable. It can be observed from Table 3.4 that the width (a_3) is very close to the width of the TFSIW$_2$ (a_2), and the taper length (l) is approximately equal to the averaged value of the quarter wavelengths of TFSIW$_1$ and TFSIW$_2$ (2.11 mm).

As shown in Figure 3.26(c) and (d), two different TFSIW-to-microstrip line transitions are designed and connected with two five-port junctions, respectively, for our measurement purpose. In Figure 3.26(c), the microstrip line is on top of the upper layer and its ground is between two substrate layers. The ground is connected to the bottom of the circuit using plated slots. In Figure 3.26(d), the junction design is reversed so that the vertical septum of the TFSIW is in the upper layer. A segment of tapered microstrip line is inserted into the TFSIW, the depth of the taper and the location where the vertical septum of TFSIW ends is two elements for adjusting the matching. It is verified by Ansoft HFSS simulations that both transitions have return loss lower than -20 dB in the full waveguide bandwidth.

The simulation and measurement results of both designs are compared in Figure 3.28. The residual mismatch below -20 dB is from 22.8 GHz to 28.8 GHz for the untapered design and from 20 GHz to 31 GHz for the tapered design. Although the untapered design has a smaller bandwidth (23%), it has covered the full bandwidth of our receiver. The bandwidth of the tapered design is 43%. Within these bands, the phase differences $\Delta\phi = \arg(S_{13}/S_{12}) = \arg(S_{15}/S_{14})$ between the adjacent and non-adjacent arms are around $120^\circ \pm 5^\circ$.

Both five-port junctions with their transitions to microstrip lines are fabricated in our in-house workshop. A TRL microstrip line calibration is conducted for removing the reflection

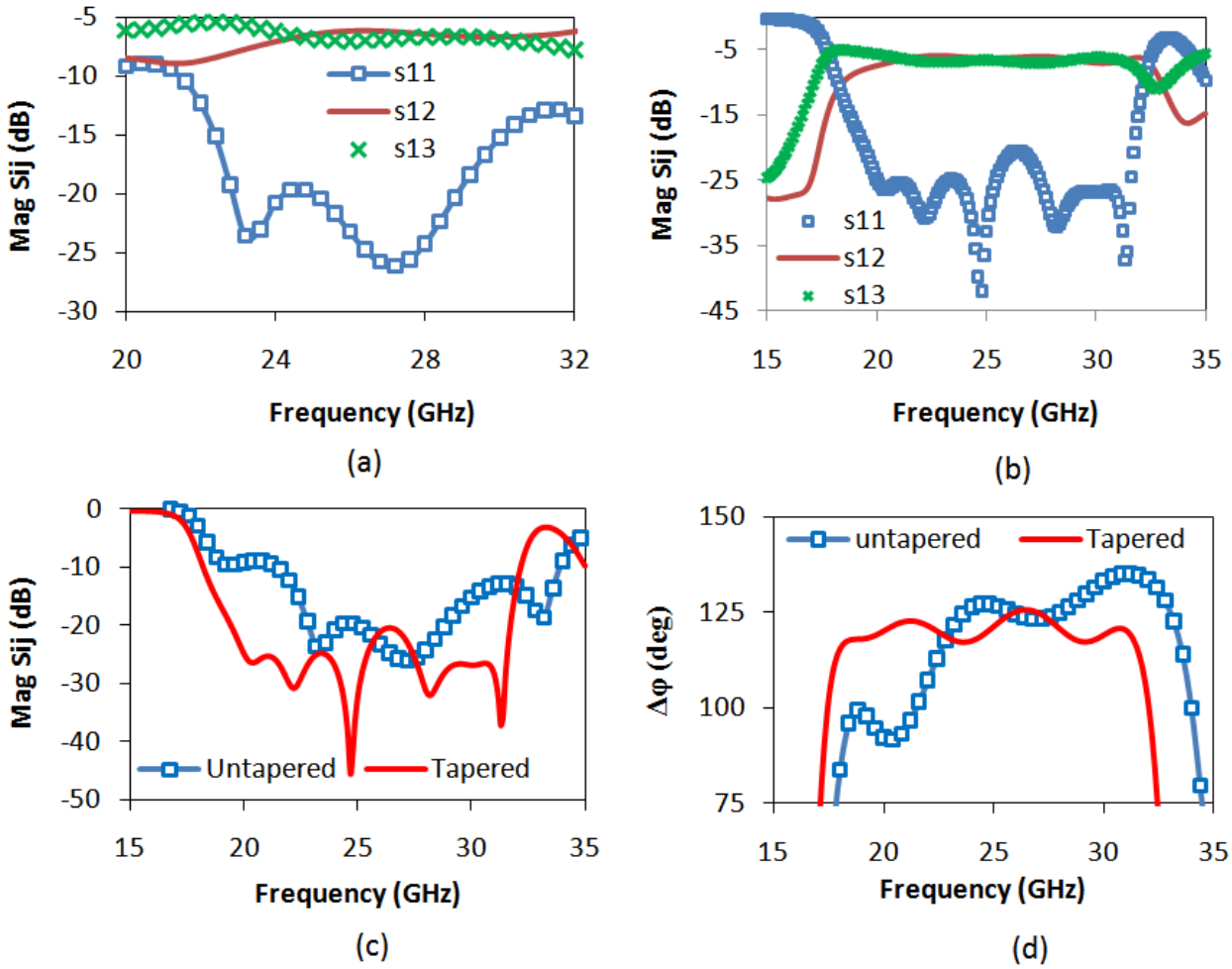


Figure 3.28 Simulated reflection coefficients of (a) untapered and (b) tapered five-port junctions, (c) the comparison of their reflection and (d) phase differences .

between the connectors and microstrip lines. In Figure 3.29(a), the phase differences $\Delta\phi 1$ ($\arg(S_{13}/S_{12})$) and $\Delta\phi 2$ ($\arg(S_{15}/S_{14})$) are within $110° \pm 10°$. In Figure 3.29(b), the junction has residual mismatches less than -20 dB from 25.4 GHz to 28.3 GHz. Within this band, the unbalance of the transmission coefficients from one port to its adjacent port and non-adjacent port is lower than 1.7 dB. Field distributions in the upper layer and lower layer of the tapered five-port TFSIW junction are illustrated in Figure 3.30.

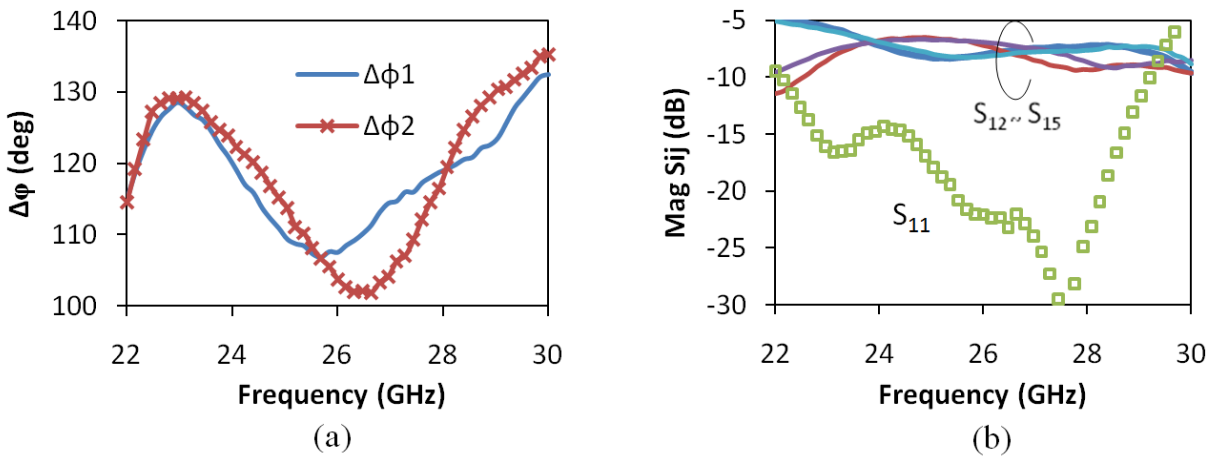


Figure 3.29 Measurements of (a) phase difference and (b) reflection coefficients of the untapered five-port junction.

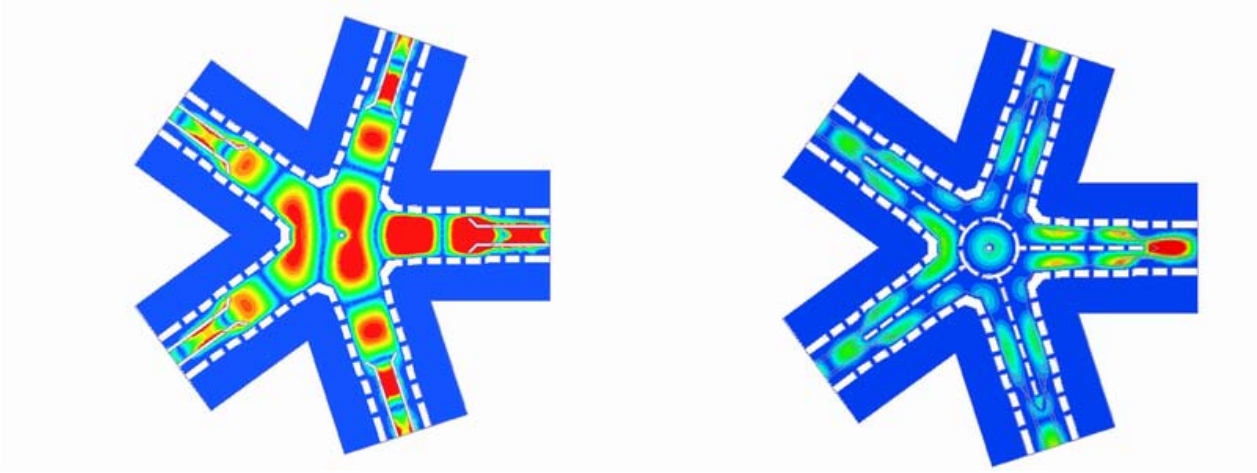


Figure 3.30 Field distributions in the upper layer (a) and lower layer (b) of the tapered five-port TFSIW junction with TFSIW-to-GCPW transitions.

CHAPITRE 4

Substrate Integrated Waveguide Front-End

4.1 Introduction

Waveguide slot array antenna has found a wide range of applications in radar and communication systems because of its excellent performance in connection with high-power handling capacity, low loss, high efficiency and etc. Among different types of waveguide slot arrays, resonant arrays with longitudinal shunt slots on the broad walls have additional advantages of low cross polarizations. On the other hand, an SIW can easily be integrated with other planar circuits in a mass production process and it also has a relatively high-quality factor (Q) compared with its planar counterparts. Therefore, the use of the SIW technique for the design of slot array radiating structures will combine the above-mentioned advantages, thus allowing the development of low-cost, mass-producible, high-performance integrated waveguide antenna systems (Yan *et al.* (2004b); Deslandes et Wu (2005b); Li et Wu (2008); Deslandes et Wu (2006)).

However, a waveguide slot array antenna suffers from a very limited frequency bandwidth. This becomes even much more pronounced for SIW slot antenna. First of all, the height of an SIW is usually less than 1/5 of a full-height conventional waveguide height. In addition to small waveguide height and dielectric filling effect, the mutual coupling between slots becomes stronger. These factors lead to a much narrower frequency bandwidth that is usually around 3% or less. Ridge waveguide presents a solution to the frequency bandwidth enhancement of a waveguide slot array antenna. A design based on normal ridge waveguide can yield 7% or even more frequency bandwidth (Wang *et al.* (2006); Kim et Elliott (1988)).

Apart from the frequency bandwidth issue, the broadside dimension of an SIW is much larger than other types of planar transmission lines, such as microstrip line and coplanar waveguide. Some specialized miniaturization techniques have been proposed in reducing the broadside dimension as well as the volume of SIW circuits. They are ridge SIW (RSIW), T-type folded SIW (TFSIW), C-type folded SIW (CFSIW), half-mode SIW (HMSIW) and some slow-wave structures composed of artificial boundaries, as discussed in previous chapters. Most of these techniques have successfully been used in miniaturized slot array antenna design. In (Lai *et al.* (2009)), two HMSIW linear array antennas with transverse slots were designed in X-band and Ka-band. The band broadening effect of RSIW has also been discussed in (Che *et al.* (2008)). A single slot antenna fed by CFSIW was proposed by Sanz-Izquierdo

et al. (2005). In (Sanz Izquierdo *et al.* (2005)), an X-band 2×2 slot array antenna was designed in a two-layer substrate. Two parallel TFSIWs are fed by an SMA connector through an SIW-to-TFSIW Y-junction and a coaxial line-to-SIW transition. Recently, a 75 GHz 4-element linear slot array (Henry *et al.* (2009)) was designed based on TFSIW technique and fabricated using photo-imageable thick-film technique. Limited by the fabrication tolerance, the measured results of the two designs do not have a good coincidence with simulations.

This chapter is organized as follows. There are three important components in a waveguide slot array antenna design : wave guiding structure, feeding network and radiation elements. Therefore the details of these components used in our designs are discussed in the following three sections. Two waveguiding structures, i.e. TFSIW and RSIW, are firstly compared in Section 4.2.1. All kinds of three-port junctions (dividers), transition among SIW, TFSIW, RSIW and microstrip line, and two different designs of feeding network for our final antenna array are investigated in Section 4.2.2. Equivalent circuit of shunt slot on TFSIW and single linear arrays fed by TFSIW and RSIW are modeled in Section 4.2.3. In Section 4.2.4, four slot array antennas based on the TFSIW and RSIW techniques, including a 2×4 TFSIW array, a 4×4 RSIW slot array antenna slot array, and two 4×8 arrays which have different feeding network, are then designed, manufactured and measured. The size of the proposed TFSIW array antenna is reduced by 40% compared to the regular SIW design and the impedance bandwidth (-10 dB) is 5.6%. A 4×4 slot array antenna based on ridge SIW and T-type folded SIW techniques easily achieves an 8.8% bandwidth and has a size-reduced broadwall at the same time. Two 4×8 RSIW array antennas with different feeding network are compared in the last section of this chapter. In order to separate the receiving channel from the transmitting one, an SIW diplexer with 40 dB isolation is designed in Section 4.3. The design of the diplexer starts from two three-pole Chebyshev filters. In order to increase the isolation between receiver and transmitter, one more introduced transmission zero is generated in each isolated frequency band. In the last section of this chapter, an experiment is designed with two proposed slot array antennas and the SIW diplexer for testing 1) the isolation between receiving and transmitting channels and 2) the isolation between two cross-polarized antennas.

4.2 SIW slot array antenna

4.2.1 Waveguiding structures : TFSIW and RSIW

RSIW and TFSIW are two miniaturized SIW structures which are both based on multilayer substrate technique. The physical layout and cross section with dimensions of RSIW and TFSIW are shown in Figure 4.1. The two structures are designed in a two-layer substrate.

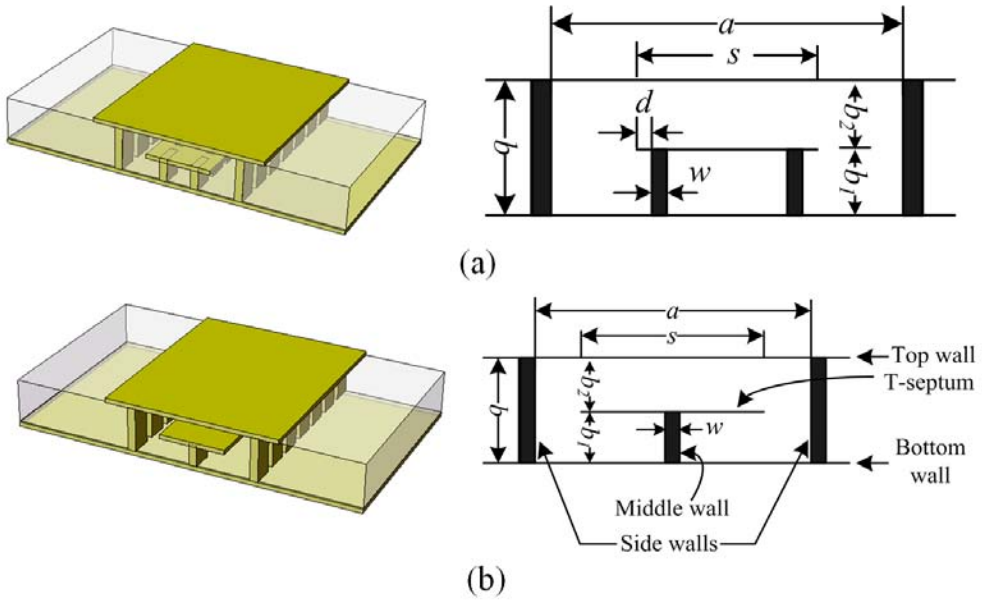


Figure 4.1 Physical layout and cross section of (a) RSIW and (b) TFSIW.

Both layers are made of RT/Duroid 6002 with thickness $b_1 = b_2 = 10$ mil, dielectric constant $\varepsilon_r = 2.94$, and $\tan\delta = 0.002$.

In practice, vertical metal walls in SIW-type structures are all implemented with drilled rows and plated slots. In Figure 4.1(a), two metal strips of width d, extend from the two sides of the ridge to protect the plated slots in fabrication process. The width s of the conductive plate between two substrates is 2.3 mm and the thickness of the middle wall w is 0.2 mm. The dimensions of all vertical slots, including width tt, length ll and interval hh, are classified into two groups. For those slots going through both two substrate layers, such as the sidewalls of RSIW and TFSIW and the short circuits at the end of four RSIWs, we have $tt_1 = 0.5$ mm, $ll_1 = 1$ mm and $hh_1 = 0.3$ mm. And for other slots only in the lower substrate layer, such as the wall of the ridge in the RSIW and the interval in the TFSIW, we have $tt_2 = 0.254$ mm, $ll_2 = 1$ mm and $hh_2 = 0.254$ mm. With the so-calculated air/slot ratio (hh/tt), no formulation is used to deduce the effective width Cassivi *et al.* (2002) of RSIW and TFSIW. Their width, denoted as a in Figure 4.1, is measured with the inner sides of two corresponding slots.

According to the conclusions in Chapter 2, the dimensions of RSIW and TFSIW need to be carefully chosen to achieve an optimized design having both small physical size and high Q factor. The RSIW width is a half of broadside wall dimension a, and aspect ratio s/a of the T-septum in the TFSIW is in the range of $0.7 \sim 0.8$. Geometrical dimensions of the two structures used in this work are listed in Table 4.1. The circuits in later sections are

Unit : mm	a	$b_1 = b_2$	s	w	d
RSIW	3.8	0.254	2.1	0.254	0.254
TFSIW	2.9	0.254	2.3	0.2	
SIW	5	Single Layer=0.254			

Tableau 4.1 Design dimensions of RSIW and TFSIW.

all composed of the RSIW and TFSIW. The two waveguiding structures are compared with a normal SIW and the measured attenuation and propagation constants are illustrated in Figure 4.2. The SIW has the maximum broadside dimension and the largest attenuation as well. The RSIW has the minimum attenuation and medium size broadwall. This structure is then finally used in the designs of antennas for our system.

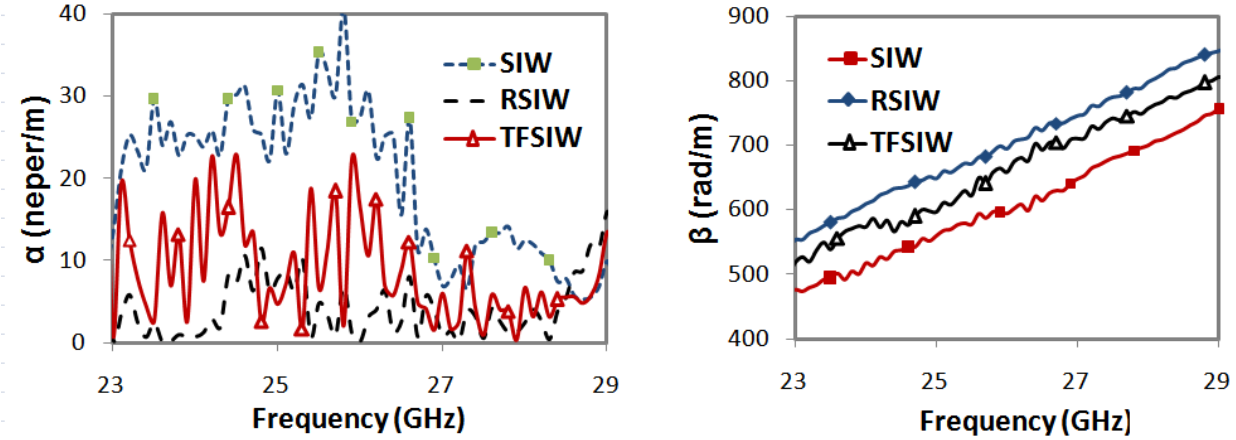


Figure 4.2 Measured attenuation (α) and propagation constant (β) of SIW, TFSIW and RSIW.

4.2.2 Feeding network : transition, junction and divider

In a standing-wave slot array antenna, the waveguide with slot radiators can be fed from one term through a 1-to-n power splitter, where n is the number of the linear array. It can also be excited by another feeding waveguide. The radiating waveguide and feeding waveguide are coupled with each other through some slots on their shared broad wall. In each approach, the feeding network has some impact on the radiation preformation and operating bandwidth of the slot radiator and hence the entire array, and this increases the complexity of the antenna synthesis and design. This impact in the later approach gets even more critical when height-reduced waveguide is used, which is the case in the designs based on SIW technique. A typical

width to height ratio in SIW is around $5 \sim 10$, which is much larger than 2. And 2 is the value normally used in an air-filled metal waveguide design. Therefore almost all published SIW-type slot array antennas use the first approach in their feeding network design, despite of the fact that multi-layer SIW structure is easily fabricated with a high precision. In this chapter, all the feeding networks are designed at one terminal and in the same layer.

The antennas used in our transceiver system are connected with single-layer SIW filters. Power dividers from SIW to various waveguiding structures need to be designed as feeding networks. In this section, a few transitions and three-port junctions are designed and the feeding networks of antenna array can be composed of these parts. Also, transitions from microstrip line to various waveguiding structures are also required for the purpose of testing each antenna individually.

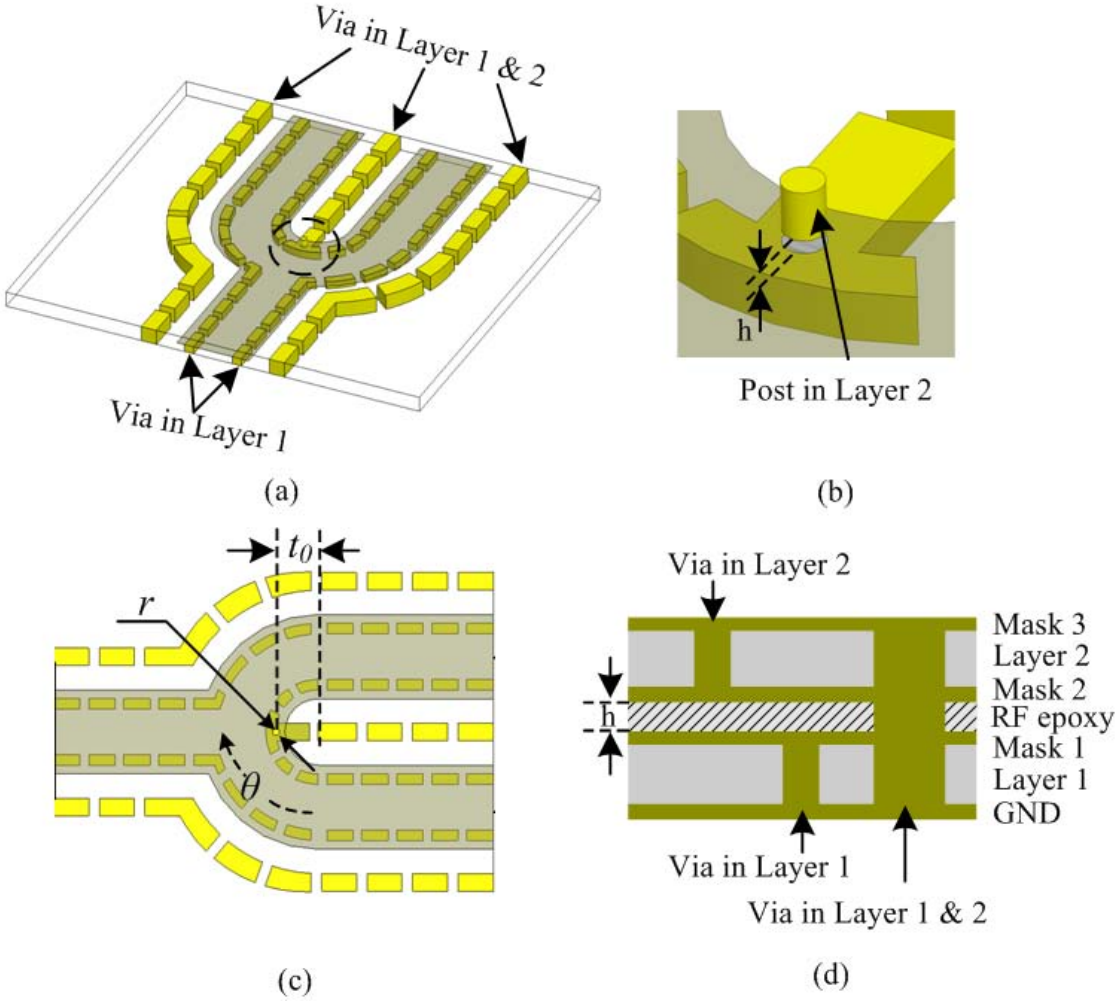


Figure 4.3 (a) Physical and (c) design layout of RSIW Y-junction ; (b) 3D view of inductive post ; (d) substrate layer stack-up.

Y-junction is widely used in various microwave network designs for the purpose of splitting one microwave signal into two. Since the waveguiding structures used in our designs are TFSIW and RSIW, their Y-junctions are firstly investigated. A 1-to-n feeding network is then constructed by cascading several Y-junctions in a recursive manner. Inductive post is often used in the design of waveguide and SIW Y-junctions and T-junctions.

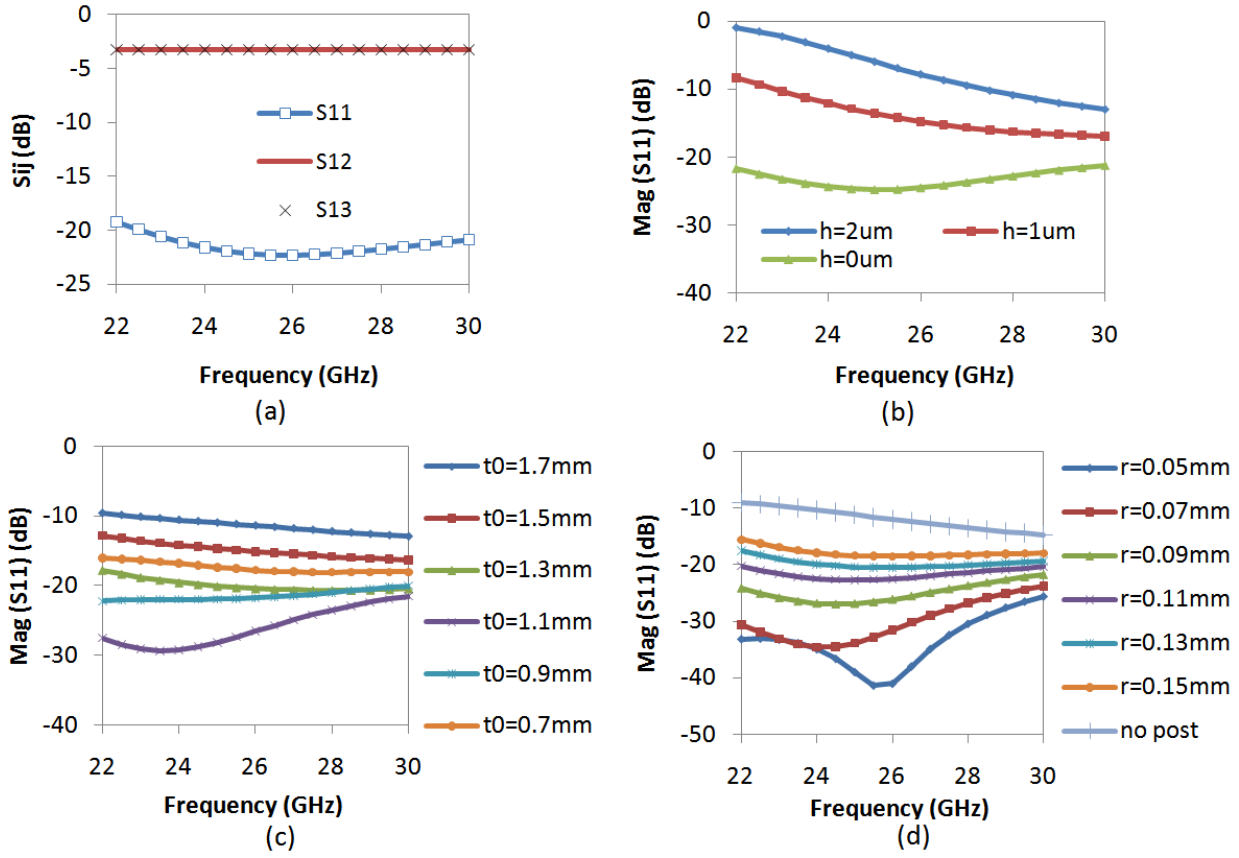


Figure 4.4 (a) S-parameters of optimized RSIW Y-junction; (b) S-parameters of RSIW Y-junction with and without electric connection between the inductive post and the middle metal mask. Parametric analysis, (c) location and (d) radius of inductive post.

In Figure 4.3(a), a RSIW Y-junction is composed of three RSIW and two 90 degree turns. An inductive post in the upper layer is used for tuning the reflection at the common port. From the parametric analysis in Figure 4.4(c) and (d), it is shown that the reflection at the common port can be effectively tuned by changing the location and radius of the post. The fabrication tolerance is approximately 1 mil and the minimum diameter of the post we can make is about 10 mil (r=0.125 mm). From the perspective of fabrication, the tolerance is enough for obtaining an optimized design which reflection is between -20 dB $\sim$ -25 dB. A small radius which is not tolerable in fabrication is needed for a better reflection lower than

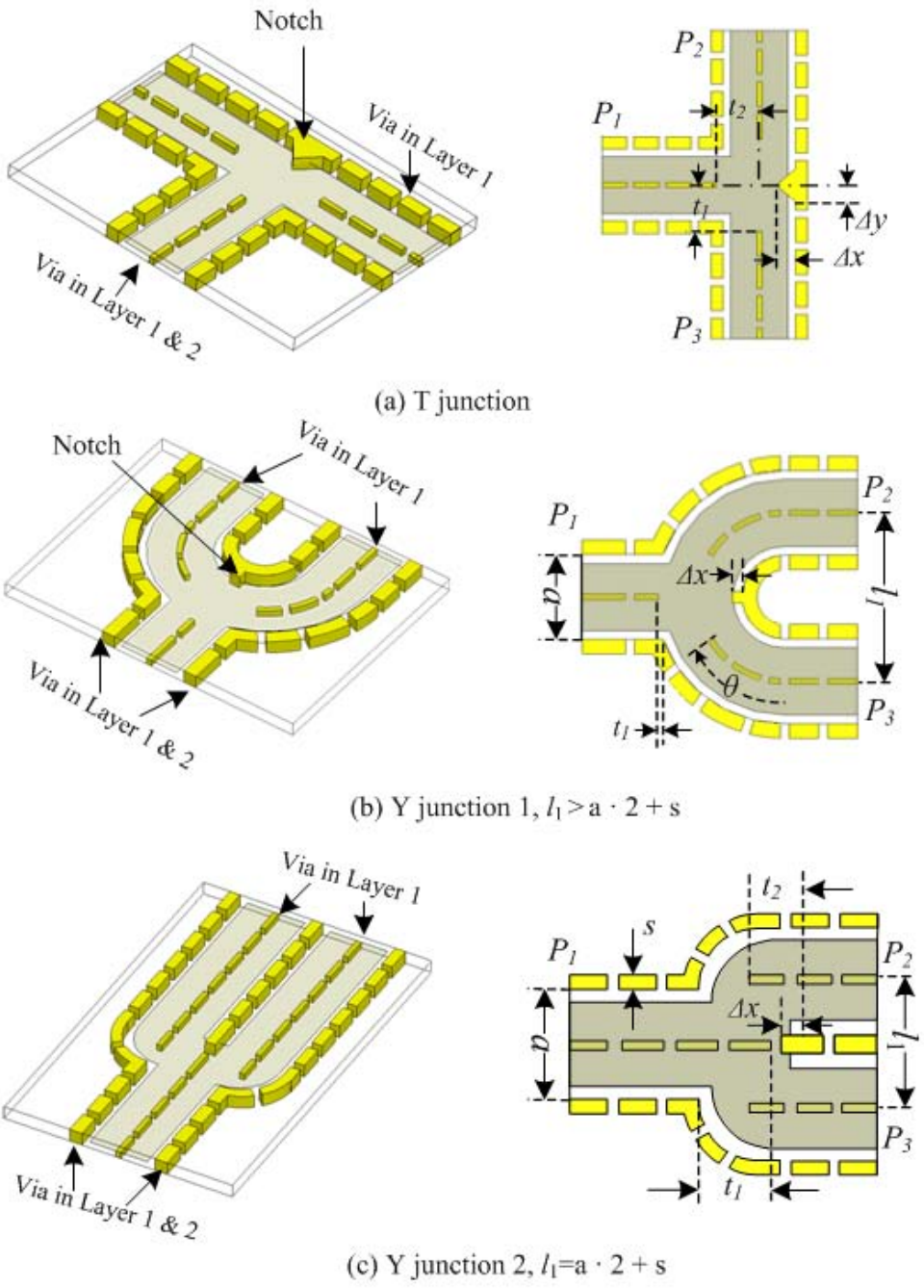


Figure 4.5 Physical and design layout of TFSIW three-port junctions.

-25 dB. Moreover, there is a small gap between the post and the middle metal layer is caused by the fabrication process we used in our own workshop and this can lead to the failure of this Y-junction design. A layer stack-up of a two-layer substrate is shown in Figure 4.3(d). In our in-house workshop, for building a two-layer PCB for high frequency applications, the processing techniques, including drilling, plating and mask making, are adapted in a

certain sequence. All masks and slots through only one substrate are first processed. The two substrate layers are then stitched together using a layer of high-frequency glue. The slots through both layers, such as the sidewalls of the waveguide, are then drilled and plated. A proper pressure is added onto the substrate layers and the final thickness of the high-frequency glue is around 1 $\sim$ 2 micron. Although it is very small thickness, it can cause a large decrement of inductance in the equivalent circuit of this fine inductive post. A simulation is conducted with a gap between the post (via only in layer 1) and the middle metal layer (on mask 2). As shown in Figure 4.4(b) and (d), even with a 1 um gap, the response of the entire design is almost the same as when there is no post at all. Instead of using the post, a notch can also be used as an inductive interference to improve the reflection at the common port. But notches with finite thickness all involve two capacitors in its equivalent circuit, which makes the best reflection we can achieve is still around 20 dB. For these reasons, we didn't use this Y-junction in the design of feeding networks for the antenna array. Instead, a combination of TFSIW Y-junctions and transitions from TFSIW to RSIW provides a good feeding network to RSIW linear arrays.

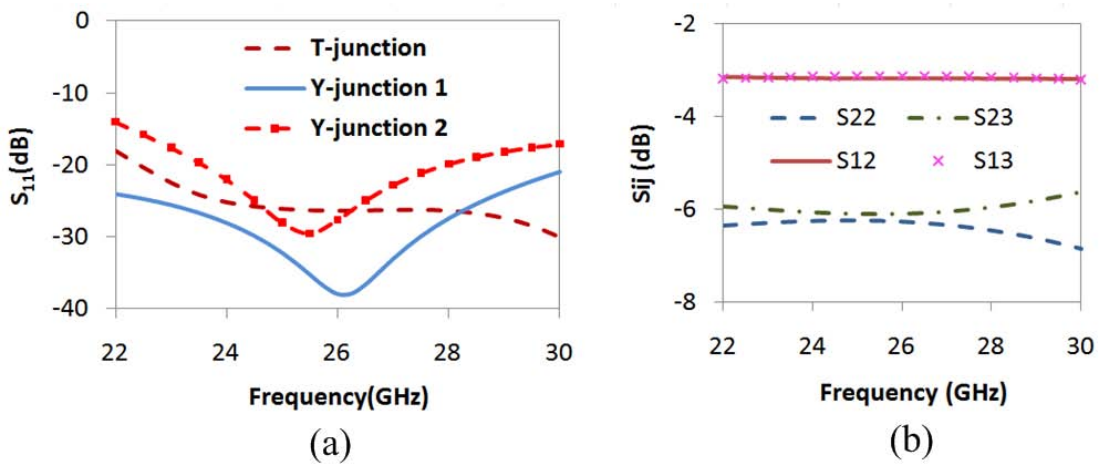


Figure 4.6 Simulation results of TFSIW Y-junction.

A TFSIW three-port junction can be designed in a similar way. A TFSIW T-junction and two Y-junctions have been illustrated in Figure 4.5. The septums of three arms in the lower layer are disconnected in the central area of the junction for the waveform transformation. The reflection at Port 1 can be tuned by changing the length of the septums inserted into this area, such as t_1, t_2 and θ. An inductive notch also helps to improve the performance of a junction, the same as what is usually performed in normal waveguide design. The S-parameters of the three optimized junctions are compared in Figure 4.6(a). The expected frequency band of the feeding network is from 25 GHz to 27 GHz. Y-junction 1 has a reflection lower than -25 dB

within the interested frequency band. It is used in the later design of the feeding network. The insertion loss and other S-parameters of Y-junction 1 are shown in Figure 4.6(b). The Y-junction 2 is also used in the design of a 2×4 TFSIW array antenna whose two linear arrays are placed side by side. All primary dimensions of three junctions in Figure 4.5 are listed in Table 4.2

Unit : mm	
T Junction	$t_1 = 1.85$, $t_2 = 1.75$, $\Delta x = 0.769$, $\Delta y = 0.659$
Y Junction 1	$t_1 = 0.159$ $\theta = 16.52$, $\Delta x = 0.33$, $l_1 = 5.77$
Y Junction 1	$t_1 = 1.7$, $t_2 = 1.15$, $\Delta x = 0.45$, $l_1 = 3.3$

Tableau 4.2 Dimensions of TFSIW T- and Y- junctions.

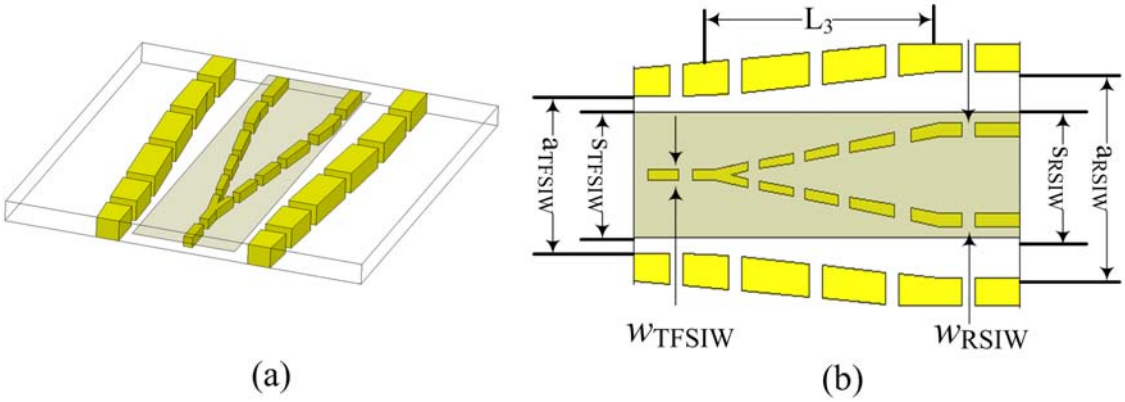


Figure 4.7 Physical and design layout of the TFSIW-to-RSIW transition.

In order to feed a RSIW using a TFSIW, a tapered TFSIW-to-RSIW transition (Figure 4.7) is used between the broadband feeding network and each linear 1×4 RSIW slot array antenna. Since the values of a, s and w in the TFSIW and the RSIW are different, they are adapted by a half wavelength tapered line. These values are listed in Table 4.2. The length of tapered lines L_3 is 5 mm. The return loss within the simulated frequency band is lower than -20 dB.

In the design of a Y junction shown in Figure 4.8, the input is an SIW and the outputs are two TFSIWs with interval $d = 2 \times a_{SIW}$, therefore angle $\theta = 60°$. The field of the dominate mode in a TFSIW is symmetric. In the design of TFSIW Y-junction shown in Figure 4.9(a), the angle α is used to tune the volume of the joint of input and output TFSIWs. The length difference of the inner and outer half of an output TFSIW can compensate the phase imbalance of the fields in the lower layer at the joint so that the field distribution of each output is symmetric. However, in the design of SIW-to-TFSIW junction shown in

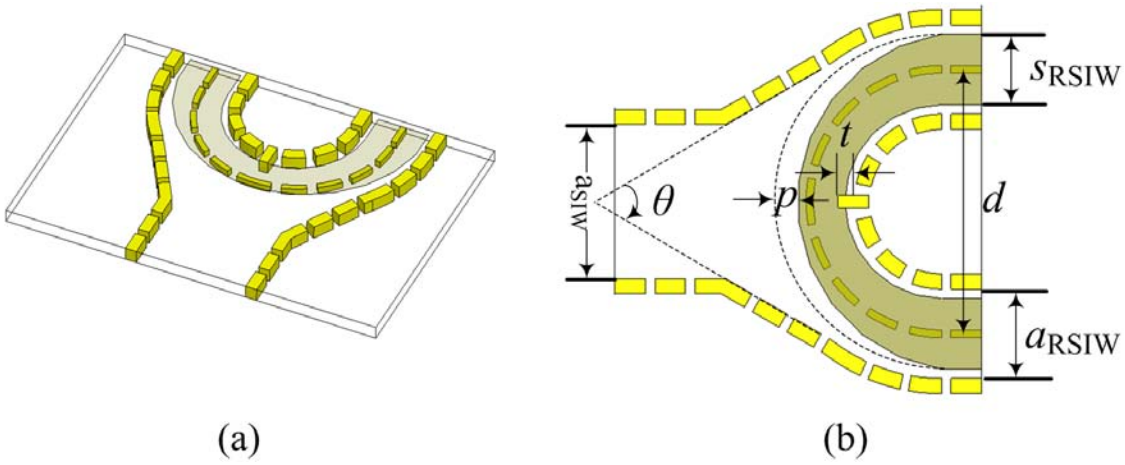


Figure 4.8 Physical and design layout of the TFSIW-to-SIW junction.

Figure 4.9(b), the field in the lower layer at the joint are off-phase, a much bigger phase imbalance versus the above design of TFSIW Y-junction. In the final optimized design, the septum between two substrate layers is trimmed on one side so that the fields in two halves of the TFSIW have different equivalent propagation constants. The differences of path length and propagation constant in the two halves compensate the phase imbalance at the joint, so that a symmetric field of TFSIW is achieved at the output. The width of the trimmed septum p is adjusted for optimization and an inductive notch is also used for turning the reflection coefficient at the input SIW port. The optimized design has a return loss lower than -20 dB from 23 GHz to 30 GHz which is more enough for the later design of feeding network.

In Figure 4.10, two different feeding networks are designed for a 4×4 slot array antenna. The input and output of the network are specified as SIW and RSIW respectively. As mentioned in the previous section, because TFSIW T-junction is easier to fabricate than its RSIW counterpart based on the multilayered substrate technique in our fabrication, TFSIW is used as a translation in the design in Figure 4.10(a). The power splitting is implemented by TFSIW three-port junctions and TFSIW is converted into SIW and RSIW at the input and output. The performance of the feeding network is good enough for our antenna design, but it also seems clumsy, therefore we have another design shown in Figure 4.10(b).

The second design is a direct SIW-to-RSIW 1-to-4 power divider. The phase at output P_2 and P_5 has a 180° difference to those at output P_3 and P_4, therefore the following linear antenna arrays need to be flipped to their own symmetric axis in order to keep the phases of all radiators. According to the theory of the 4-way waveguide splitter, the width of the translation waveguide in the middle should be different from the input and output ones, therefore the widths of RSIWs in this design, one vertical and four horizontal, are different,

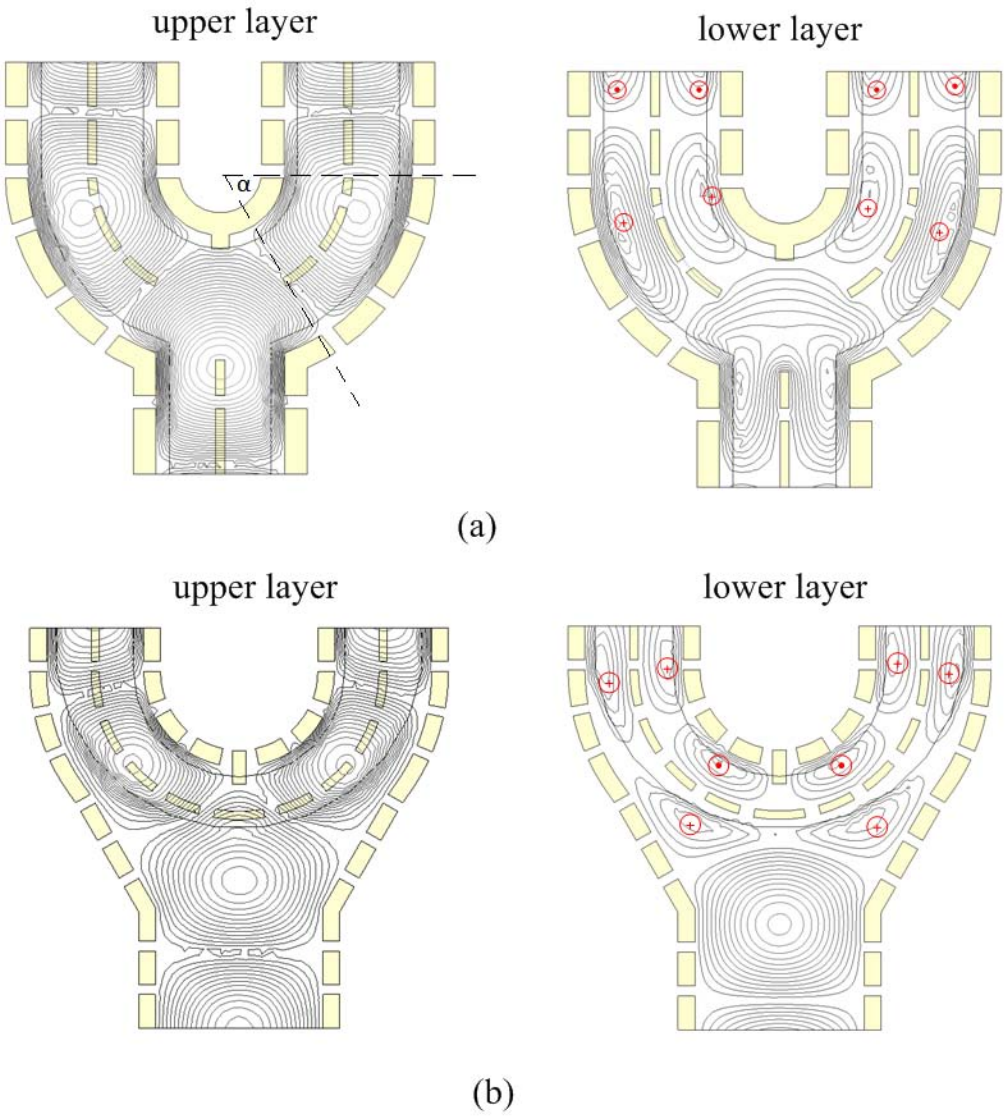


Figure 4.9 Field distribution of TFSIW junctions, (a) TFSIW Y-junction and (b) SIW-to-TFSIW Y-junction.

$a_1 = 4.8$ mm, $a_2 = 3.9$ mm and $s_1 = s_2 = 1.9$ mm. The equal division of the power in four paths are also adjusted by the phase tuning notches indicated in Figure 4.10. The total length of the second design is 11.3 mm which is just one half of that of the first design 23.2 mm, however it suffers from a very limited bandwidth which is caused by in-line phase tuning.

The insertion loss and reflection at SIW input, the phase from input to four outputs and phase difference at P_2 and P_3 are all plotted in Figure 4.11 and Figure 4.12. The reflection at the input of the first design is all below -20 dB within the entire frequency band, and the phase difference at P_2 and P_3 is always kept around 5°. In the second design, the -20

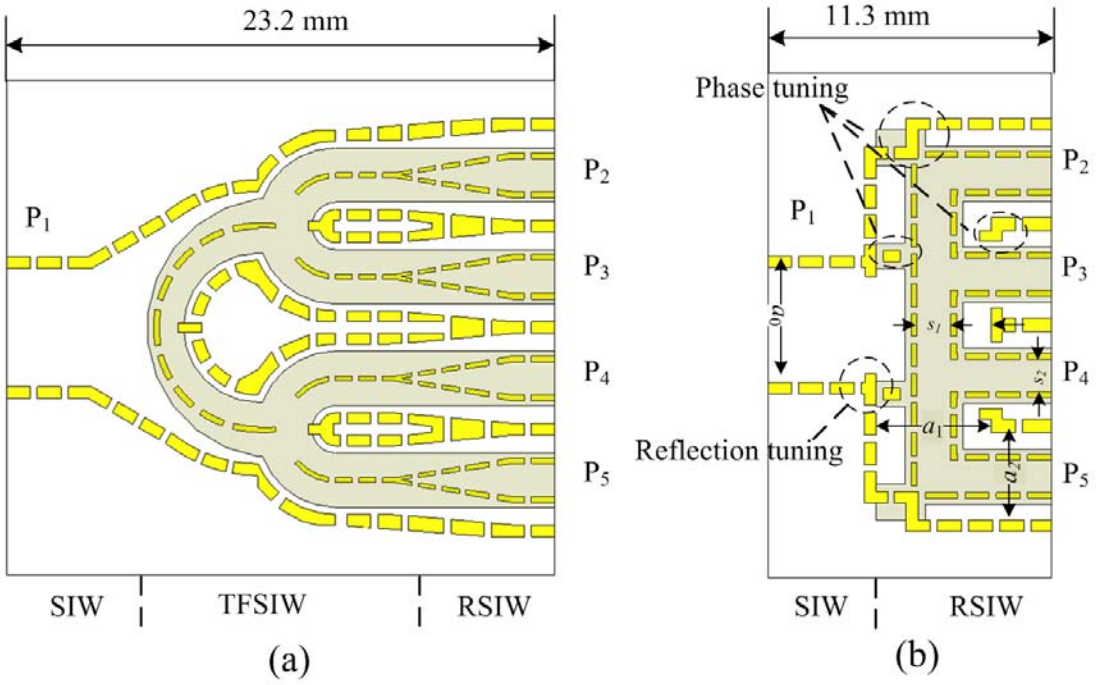


Figure 4.10 Two feeding networks for 4×4 RSIW slot array antenna : (a) SIW-TFSIW-RSIW and (b) SIW-RSIW.

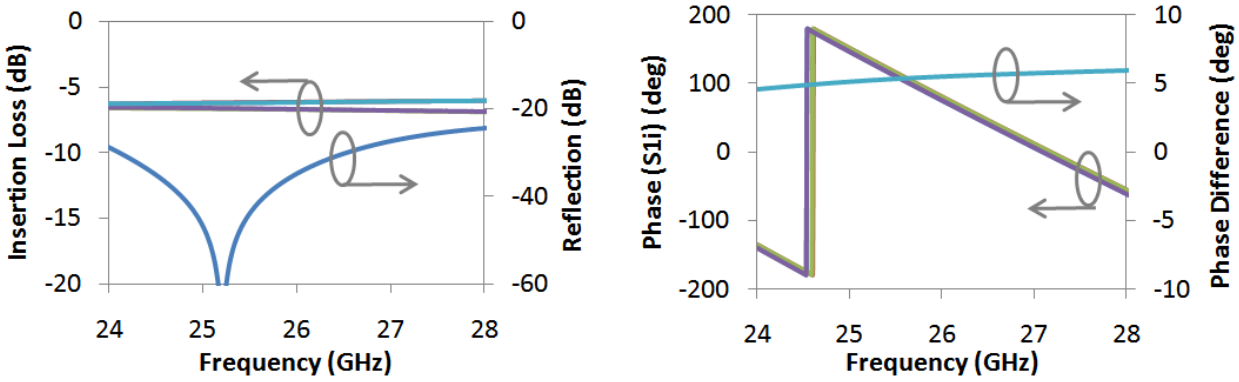


Figure 4.11 Response of a 1-to-4 long feeding network.

dB bandwidth is less than 2 GHz at the center frequency, the same bandwidth of the 180° phase difference between P_2 and P_3. A 2 GHz bandwidth is required, considering the system specification and the tolerance of fabrication. Hence the first design is adopted in our design of the slot array antenna.

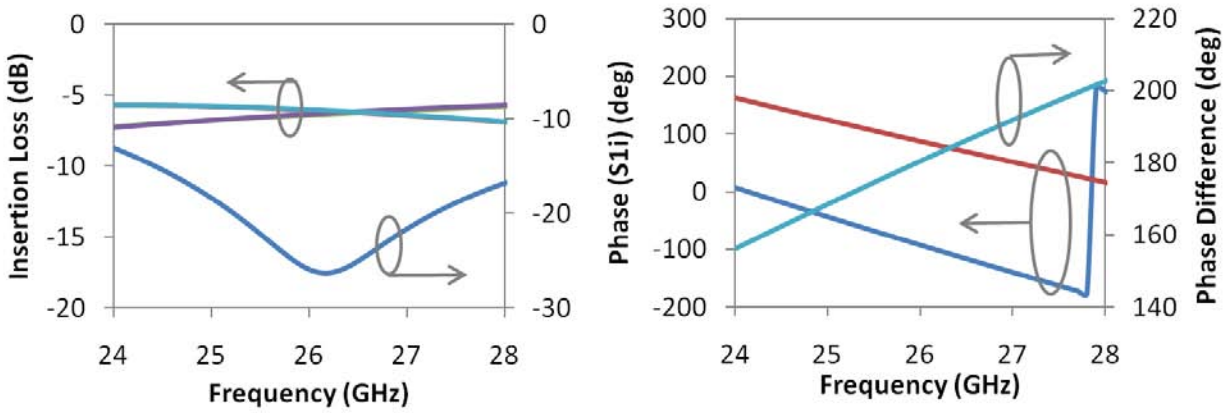


Figure 4.12 Response of a compact 1-to-4 long feeding network.

4.2.3 Equivalent circuit of radiation element

The analysis of a longitudinal slot array in a full-height ridge waveguide was completed by Kim et Elliott (1988). When the height of the waveguide is reduced, however, the classical MoM (method of moments) formulations become less accurate (Stern et Elliott (1985)). The height of a single layer used in this work is 10 mil, i.e. 1/10 of the full height. The classical analytical methods are no longer valid. In this work, we deploy Ansoft HFSS to optimize the proposed antenna array. The width of the slot is usually chosen between 1/10 and 1/30 of the resonant length. On the other hand, a wide slot can improve both the impedance bandwidth and the power-handling capacity of a slot antenna. However, the symmetry and polarization of the radiation pattern can also be deteriorated when the slot is too wide. This section is to investigate 1) the equivalent model of a single shunt slot on TFSIW or RSIW, and 2) the equivalent active admittance of slot in a TFSIW or RSIW linear array.

A longitudinal slot on the broadside of a TFSIW or RSIW can be represented by a single shunt admittance or a T network as shown in Figure 4.13. When the S-parameters of the equivalent circuit are obtained in simulation and measurement, the value of the equivalent admittance can then be solved with Equation 4.1 and Equation 4.2. The value of Y_3 is given in Equation 4.5.

$$\frac{Y_1}{Y_0} = \frac{1+S_{11}}{-2S_{11}} \tag{4.1}$$

$$\frac{Y_2}{Y_0} = \frac{2S_{12}}{(1-S_{11}+S_{12})(1-S_{11}-S_{12})} \tag{4.2}$$

$$\frac{Z_2}{Z_0} = \frac{(1+S_{11}-S_{12})}{(1-S_{11}+S_{12})} \tag{4.3}$$

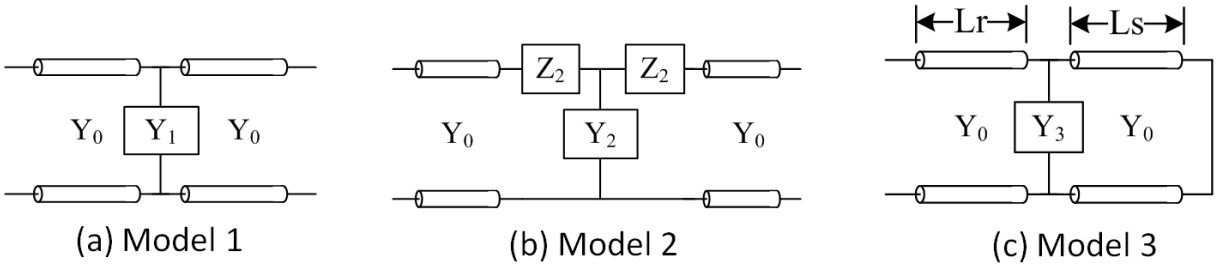


Figure 4.13 Equivalent model of a single shunt slot, (a) two-port single shunt admittance model, (b) two-port T-network model, and (c) single-port single shunt admittance model.

Single slots on RSIW and TFSIW used in our design extracted with these models are compared in Figure 4.14 and Figure 4.15, respectively. The extracted equivalent admittances of a TFSIW-fed slot are also compared with the values extracted from the measured S-parameter. The correlation between these curves shows that the single admittance model is still valid for slots used in our design.

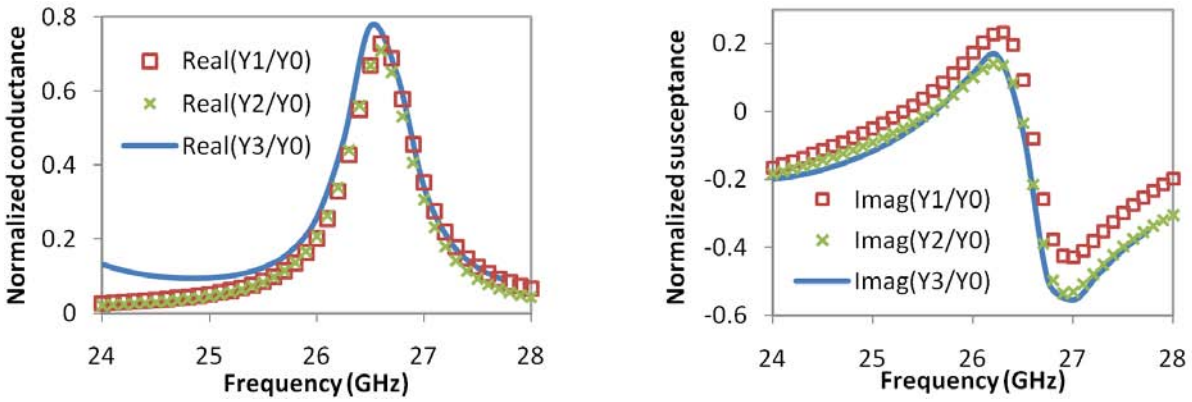


Figure 4.14 Simulated and measured normalized admittance Y_0 of a shunt slot on RSIW.

Mutual coupling between radiators can cause difficulties when the classic theory of the waveguide slot array antenna is applied in an SIW-type antenna design. It becomes more severe in our designs based on TFSIW and RSIW because of a more compact structure. The impact of mutual coupling can be investigated by extracting an equivalent active admittance of the radiator in a linear array. Assuming that the equivalent active admittances of uniform slots are the same, a linear slot array can be represented by an equivalent circuit shown in Figure 4.16.

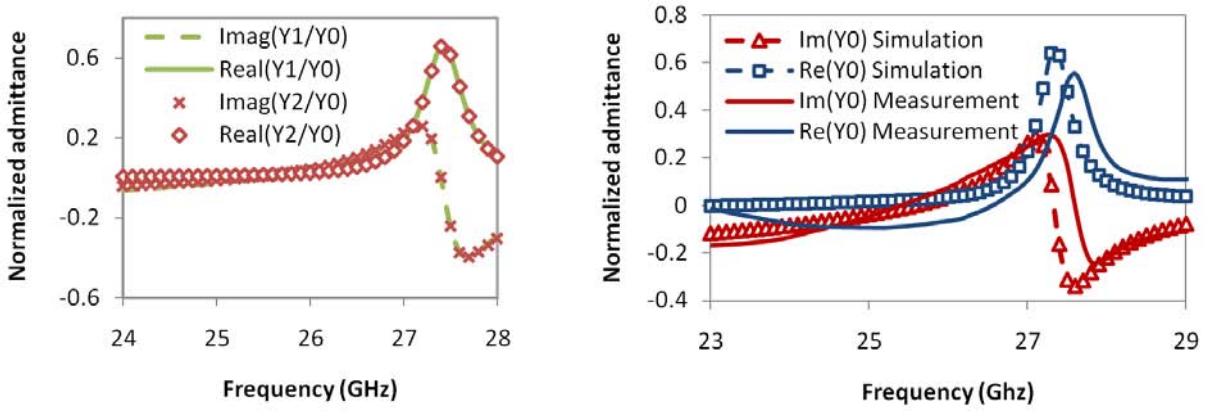


Figure 4.15 Simulated and measured normalized admittance Y_0 of a shunt slot on TFSIW, slot length $l_s = 3.35$ mm, slot width $w_s = 0.4$ mm and slot shift $x = 0.25$ mm.

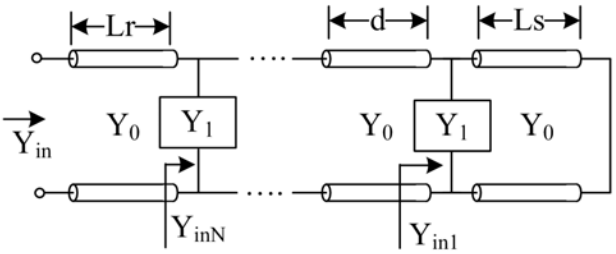


Figure 4.16 Equivalent model of a linear slot array (Wang *et al.* (2006)).

$$
\begin{aligned}
Y_{in1} &= -j\cot\beta L_s + Y \\
Y_{in2} &= \frac{Y_{in1} + j\tan\beta d}{1 + jY_{in1}\tan\beta d} \\
&\vdots \\
Y_{inN} &= \frac{Y_{in(N-1)} + j\tan\beta d}{1 + jY_{in(N-1)}\tan\beta d} \\
Y_{in} &= Y_{in(N+1)} = \frac{Y_{inN} + j\tan\beta L_r}{1 + jY_{inN}\tan\beta L_r} \\
also, \quad Y_{in} &= \frac{1 - S_{11}}{1 + S_{11}}
\end{aligned}
\tag{4.4}
$$

where $Y_{in1} \ldots Y_{inN}$ are normalized input admittance before each radiation slot. Y is the normalized equivalent admittance of one slot radiator. When the reflection coefficient at the input is obtained through simulation or experiment, the normalized active admittance can

be extracted from simulated S-parameter in an iterative manner.

For a single slot, we have

$$\begin{aligned} Y_{in1} &= -j\cot\beta L_s + Y \\ Y_{in} &= \frac{Y_{in1} + j\tan\beta L_r}{1 + jY_{in1}\tan\beta L_r} \\ \therefore \quad Y &= \frac{\Gamma(1+\cot\beta L_s\tan\beta L_r) + j(\cot\beta L_s - \tan\beta L_r)}{1 - j\Gamma\tan\beta L_r} \end{aligned} \tag{4.5}$$

The normalized active admittances of a TFSIW and RSIW linear array extracted with above formulations are shown in Figure 4.17 and Figure 4.18, respectively. As shown in Figure 4.17, when $N = 1$, the equivalent active admittance is the self admittance of a slot resonating at 27.5 GHz. When more slots are added into the array, the resonant frequency of the equivalent active admittance finally converges to f_0. From these figures, we can conclude that it tends to converge towards a frequency point when the number of the radiators are larger than 3, which means the mutual coupling between adjacent 3 radiators can have impact on the equivalent resonance of the radiator.

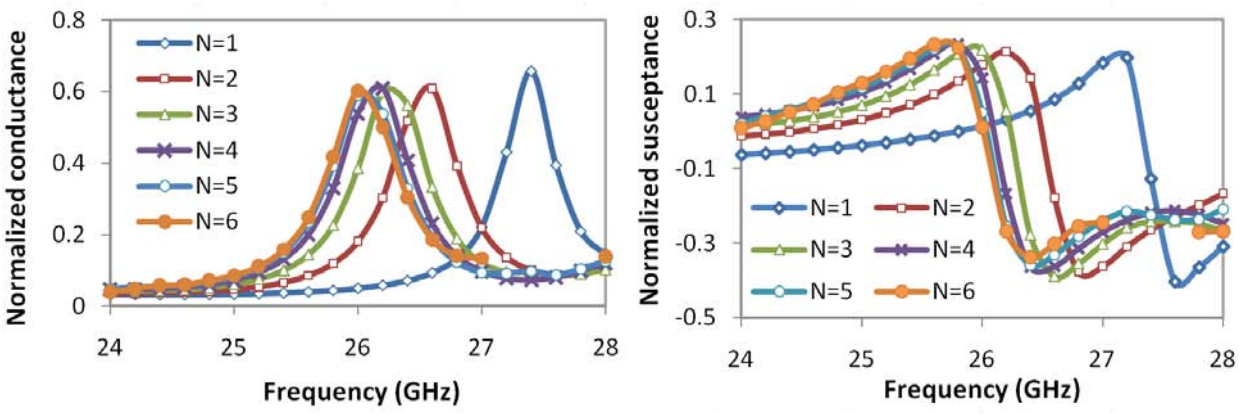


Figure 4.17 Normalized active admittance of equivalent shunt slots in a linear N-element array of a TFSIW.

4.2.4 Slot array antenna

This section presents the design of three slot array antennas based on RSIW and TFSIW techniques, (1) a 2×4 TFSIW slot array antenna, (2) a 4×4 RSIW slot array antenna, and (3) an 8×4 RSIW slot array antenna.

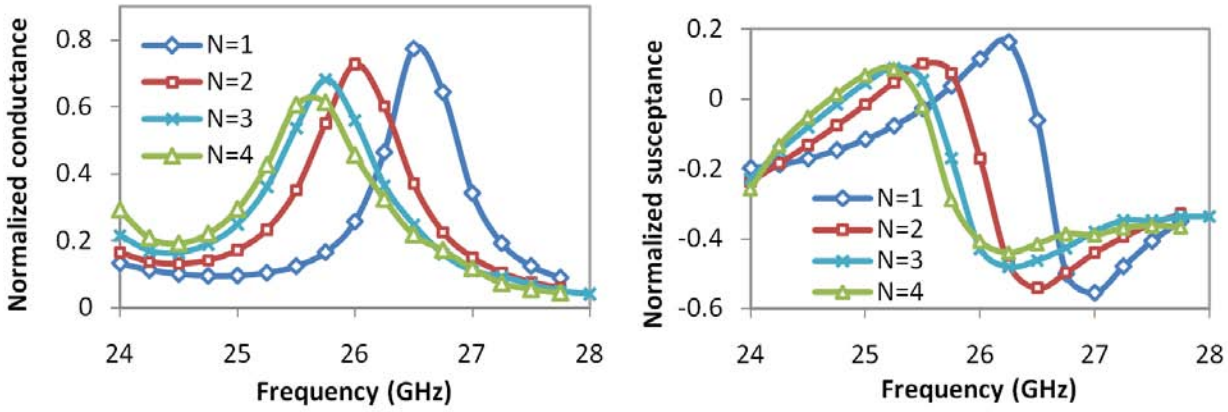


Figure 4.18 Normalized active admittance of equivalent shunt slots in a linear N-element array of a RSIW.

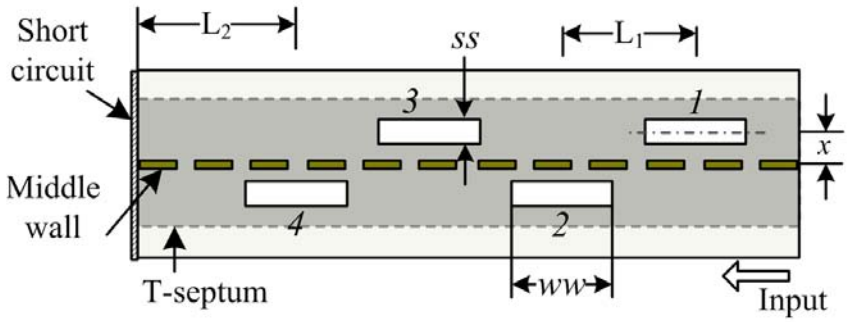


Figure 4.19 Geometrical layout of the linear TFSIW slot array antenna, $x = 0.25$ mm, $w = 0.4$ mm, $L_1 = 4.25$ mm, $l = 3.35$ mm, and $L_2 = 5.325$ mm.

TFSIW slot array antenna A linear TFSIW slot array with 4 uniform radiating elements, having the same size and shift to the center line, is shown in Figure 4.19. The shift of each slot x is 0.25 mm and the length of each slot l is 3.35 mm. At the center frequency f_0 (26 GHz), the resonant length l_s of a single slot with the same shift is 3.85 mm, which is $0.44 \times \lambda_g$ and λ_g (= 8.7 mm) is the guided wavelength of the TFSIW. Therefore, the length of each slot in the final design is $0.385 \times \lambda_g$ or $0.87 \times l_s$. The normalized magnitude of electric field E_x in four slots is shown in Figure 4.20. Because of the strong couple between slots, the excitations on slots are $0.68 : 1 : 1 : 0.68$ from slot $1^{\#} \sim 4^{\#}$, respectively. The simulated E- and H-plane radiation patterns of the 1×4 linear arrays are displayed in Figure 4.21. The H-plane sidelobe level is lower than -22 dB and the backlobe level is lower than -11 dB.

The proposed 2×4 array is then made by assembling the optimized linear array with the

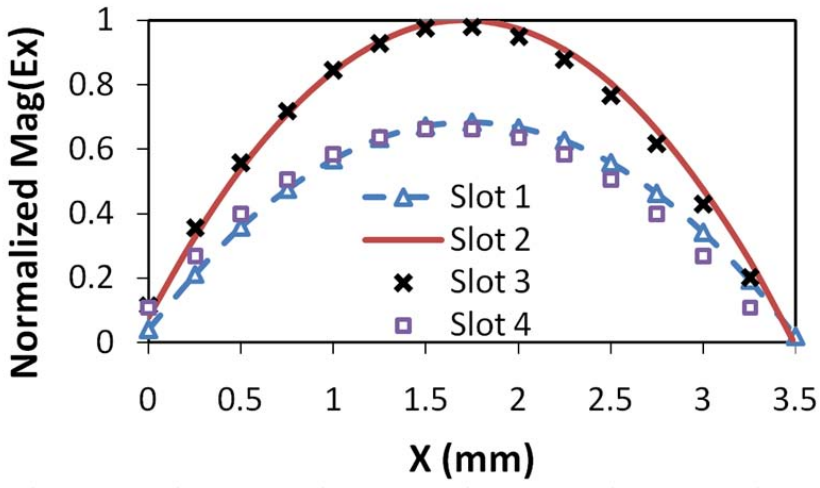


Figure 4.20 Normalized magnitude of electric field E_x in four slots of one linear array.

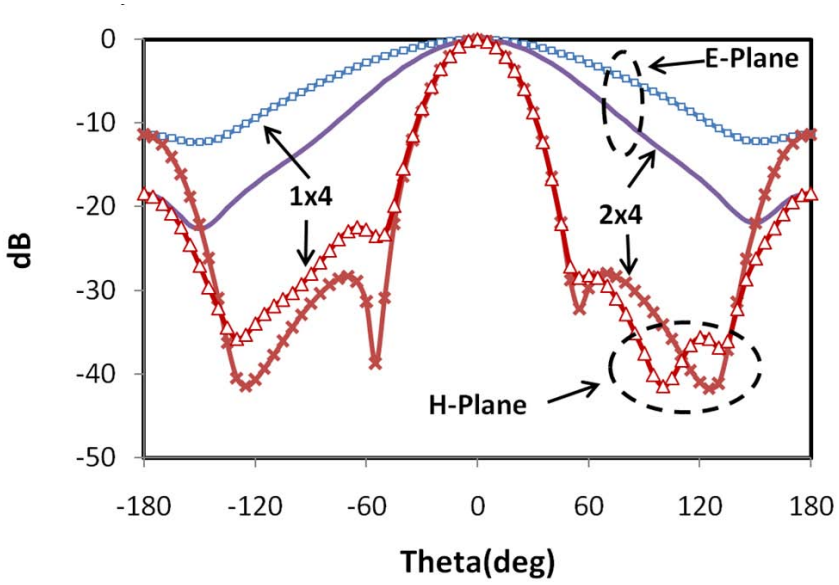


Figure 4.21 Simulated radiation pattern of 1×4 and 2×4 TFSIW slot array antenna.

proposed TFSIW Y-junction. A microstrip line-to-TFSIW transition is used for our measurement purpose, whose dimensions were given in (Ding et Wu (2009)). For achieving a highly compact design, two linear arrays are put side by side in this design. The interval D defined in Figure 4.22 is 3.3 mm ($0.28 \times \lambda_0$). Although the E-plane radiation patterns are sacrificed a little for getting a compact design, as shown in Figure 4.21, the half-power beamwidth of the E-plane radiation pattern is reduced from 124° of the 1×4 array to 37° of the 2×4 array. The back lobe levels for both E-plane and H-plane are decreased by 7 dB.

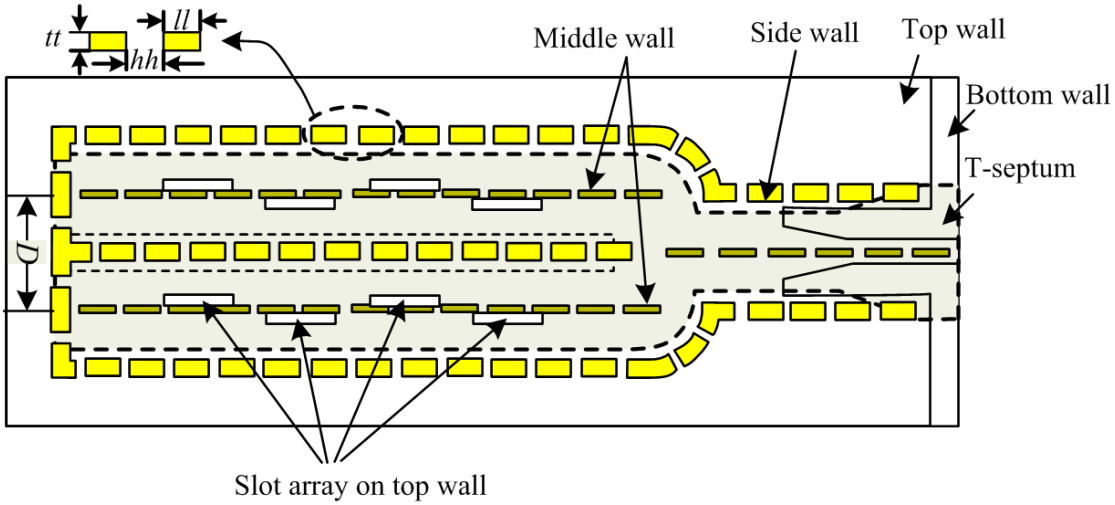


Figure 4.22 Design layout of 2×4 TFSIW slot antenna array.

Figure 4.22 is the final design layout of the proposed 2×4 TFSIW slot array antenna. The dimensions of all vertical slots, including width tt, length ll and interval hh, are therefore classified into two groups. For those slots going through both two substrate layers, we have $tt_1 = 0.5$ mm, $ll_1 = 1$ mm and $hh_1 = 0.3$ mm. And for other slots only in the lower substrate layer, we have $tt_2 = 0.254$ mm, $ll_2 = 1$ mm and $hh_2 = 0.254$ mm. The gaps between neighboring slots are small enough such that no effective width of the TFSIW needs to be calculated when the ideal metal walls are replaced with rows of artificial plated slots (Xu *et al.* (2008a)). The inner surfaces of the rectangular slots can be directly used as the equivalent sidewalls of the SIW.

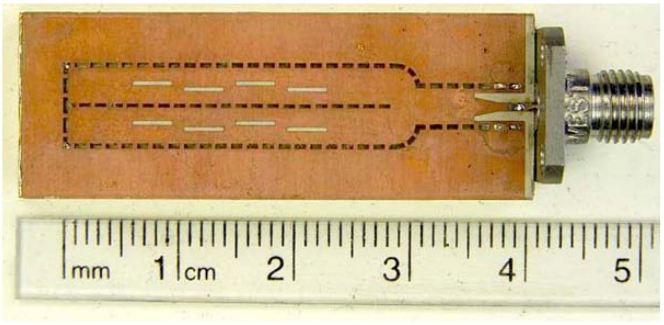


Figure 4.23 Physical picture of 2×4 TFSIW slot array antenna.

The photograph of the fabricated antenna is shown in Figure 4.23. The size of the entire antenna with surrounding margin is 38.9×7.13 mm^2. The width of this antenna is reduced

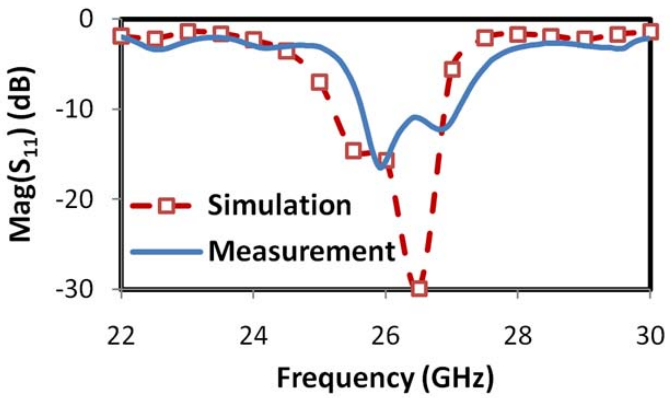


Figure 4.24 Simulated and measured reflection coefficients of the 2×4 TFSIW array antenna.

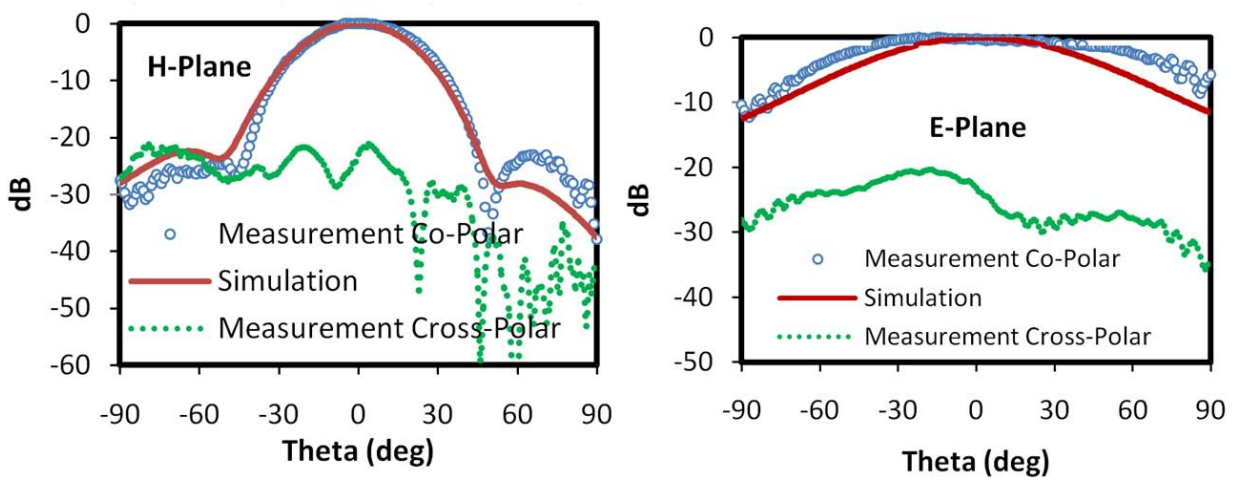


Figure 4.25 Simulated and measured co-polarizations, and measured cross polarizations of H-plane and E-plane at 26 GHz.

by 40% compared with the design based on the standard SIW technique. The measured reflection coefficients are compared with the simulated results in Figure 4.24. Due to the fabrication and substrate parameter tolerance, the measured -10 dB frequency band is shifted to 25.63 $\sim$ 27.05 GHz against the simulated range of 25.25 $\sim$ 26.85 GHz. The measured impedance bandwidth is 5.46%. Simulated and measured E-plane and H-plane radiation patterns are shown in Figure 4.25. The radiation pattern and gain are measured in a compact-range anechoic chamber with 1° azimuth angle and elevation angle resolution. The side lobe level of H-plane is below -20 dB at the center frequency (26 GHz) in both simulation and measurement. The measured cross polarizations in both E-plane and H-plane are lower than -20 dB. The simulated radiation efficiency is 84.62% and the measured broadband gain at 26

GHz is 10.9 dBi in Figure 4.26.

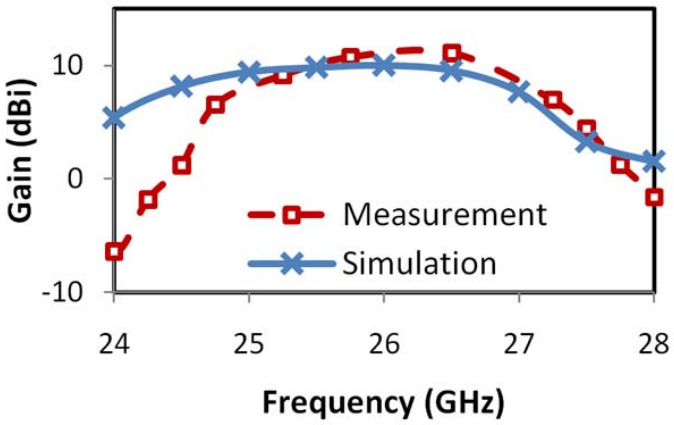


Figure 4.26 Simulated and measured broadband gain.

4 × 4 RSIW slot array antenna A linear RSIW slot array with 4 elements, shown in Figure 4.27, is designed at first. The width and length of each slot are ss and ww. The offset of slots is dd. The length between two adjacent slots is L_1. L_2 is the distance from the center of the last slot to the short circuit which is at the end of the RSIW. Good initial designs of relative 2×4 and 4×4 arrays are easily completed by simply assembling the feeding network and the optimized linear array. The final design is then obtained after a fine-tuning based on the initial designs. The optimized dimensions of each 1×4 RSIW slot array are listed in Table 4.3. The interval between two adjacent linear arrays, denoted as D in Figure 4.28, is 4.3 mm.

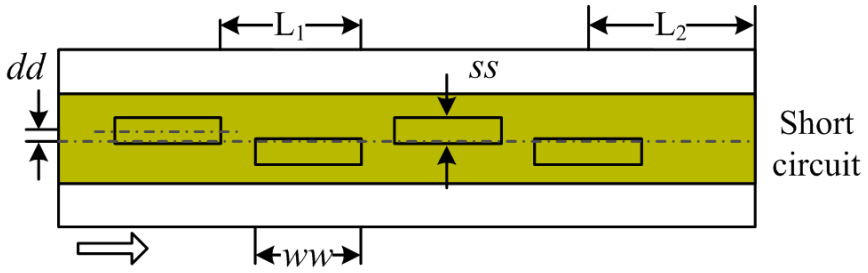


Figure 4.27 Design layout of the linear RSIW slot array antenna.

A top view of the layout of the proposed 4×4 RSIW slot array antenna is shown in Figure 4.28. The center frequency of the antenna is designed at 26 GHz. Connected with the RSIW slot array, denoted as part (e) in Figure 4.28, several transitions and power dividers

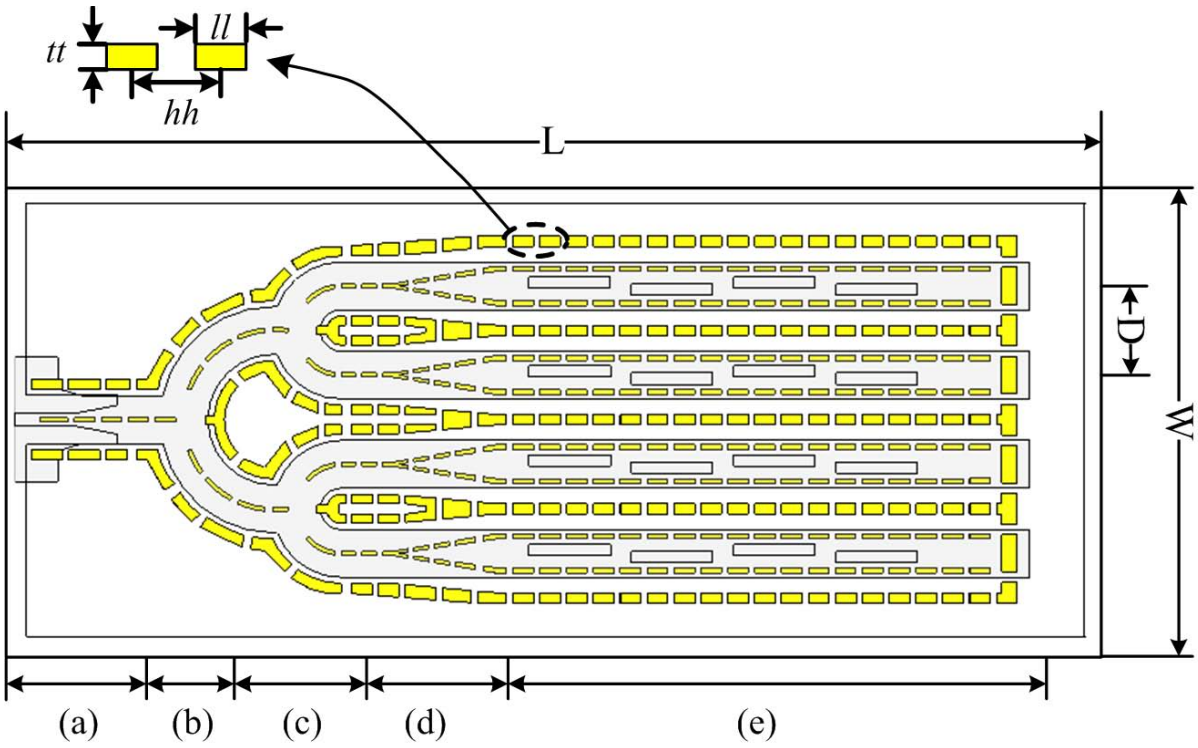


Figure 4.28 Design layout of the 4×4 RSIW slot antenna array.

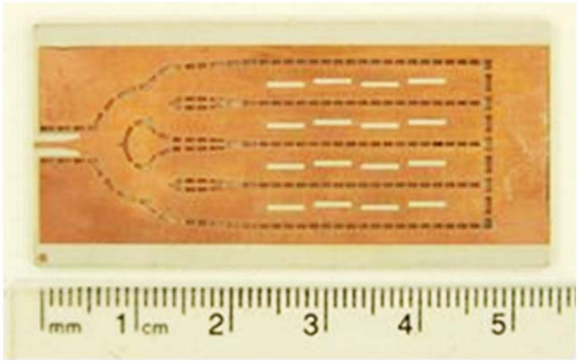


Figure 4.29 Physical picture of the 4×4 RSIW slot array antenna.

are used to construct the feeding network. They are (a) one microstrip-to-TFSIW transition, (b) and (c) two TFSIW junctions, and (d) one TFSIW-to-RSIW transition.

The photograph of the fabricated antenna is shown in Figure 4.29. The size of the entire antenna with surrounding margin is 54×21 mm^2. All simulations are conducted with Ansoft HFSS.

The measured return loss is compared with its simulated counterpart in Figure 4.30. Due

Unit : mm	dd	ss	L_1	ww	l_2	D
	0.175	0.55	4.95	3.95	4.075	4.3

Tableau 4.3 Dimensions of each linear 1×4 RSIW slot array antenna.

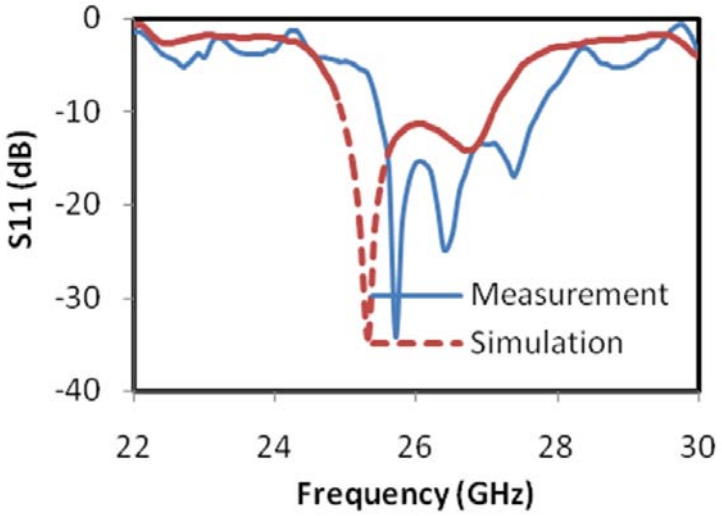


Figure 4.30 Simulated and measured return loss of the 4×4 RSIW array antenna.

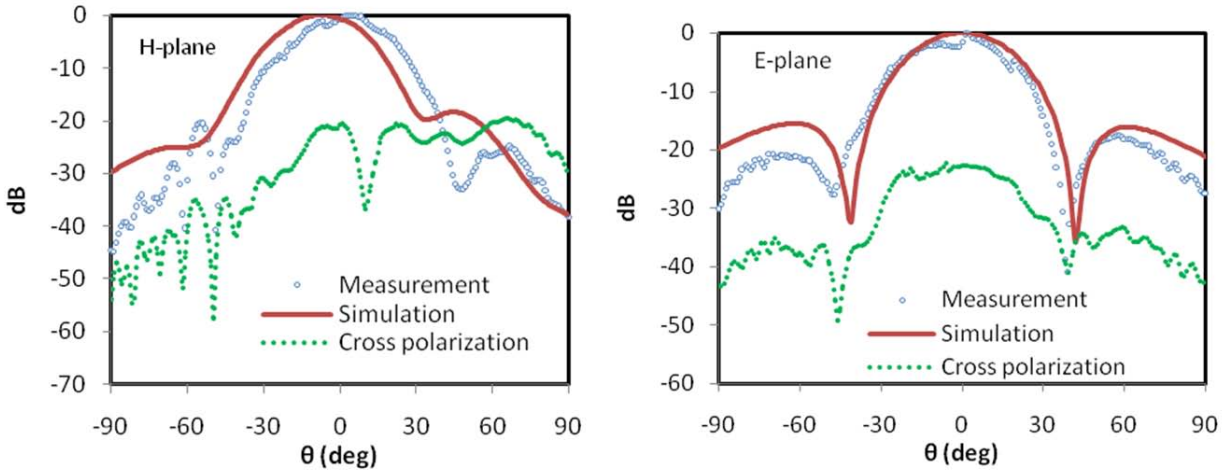


Figure 4.31 Simulated and measured co-polarization and measured cross polarization of H-plane and E-plane at 26 GHz.

to the limited fabrication and substrate parameter tolerance, the measured frequency band (< -10 dB) is shifted from $24.85 \sim 27.05$ GHz against the simulated range of $25.45 \sim 27.75$ GHz. The measured frequency bandwidth (10 dB return loss) is about 8.8%, which is much

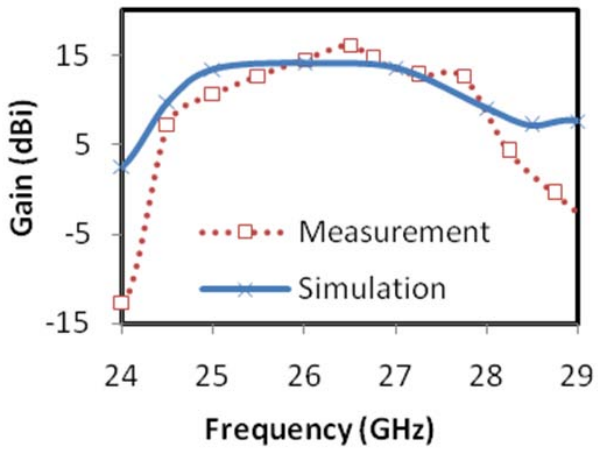


Figure 4.32 Simulated and measured broadband gain of the 4×4 RSIW array antenna.

larger than the designed performances 2.7% in (Li et Wu (2008)) which was based on the conventional SIW technique. Simulated and measured E-plane and H-plane radiation patterns are also shown in Figure 4.31, respectively. In the measurements, the side-lobe is lower than -18 dB in E-plane and -20 dB in H-plane. Compared with a 4×4 slot array antenna based on the SIW technique (Li et Wu (2008)), the level of side-lobe in E-plane is lowered by more than 5 dB and the cross-sectional size of the entire array antenna is reduced to 80%. As shown in Figure 4.32, except a very small frequency shift, the measured broadband gain is well consistent with the simulated result. The gain at the designed center frequency (26 GHz) is 14.5 dBi.

8×4 RSIW slot array antenna Two antennas are used in our transceiver system. Because the designed antenna in the previous section has both broad bandwidth and high cross-polarization, we double the number of the linear array to increase the broadband gain. The new antenna can be regarded as two 4×4 array antennas that are assembled side by side via an SIW-to-TFSIW junction. The layout of the designed antenna is shown in Figure 4.33. The total size of the antenna is 56×38 mm^2.

The radiation patterns of the E-plane and H-plane of the fabricated array antenna are shown in Figure 4.34. The radiation patterns are plotted at two center frequencies of the upper link 25.5 GHz and down link 26.5 GHz, respectively. The cross-polarization at 26.5 GHz is below -30 dB in both H-plane and E-plane radiation patterns. This can provide a good isolation between the modulated signal and carrier received from two antennas which are placed perpendicularly to each other. The reflection of the antenna is measured and compared with the simulation in Figure 4.35. The 10 dB bandwidth is about 9%, from 25.3

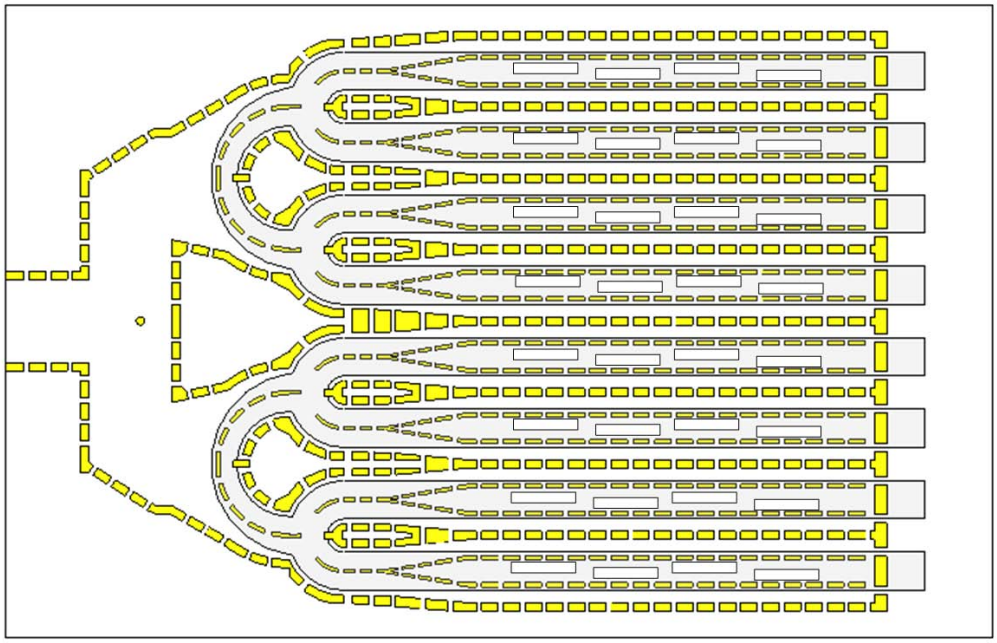


Figure 4.33 Design layout of 8×4 RSIW slot array antenna.

GHz to 27.7 GHz. The working frequency band is shifted with about 300 MHz which is within the normal range of our fabrication tolerance.

The broadband gain from 22 GHz to 30 GHz are plotted in Figure 4.36. Two standard waveguide horn antennas are used in the gain measurement. Each of them only covers a half of the interested frequency band. The results of two measurements are merged in Figure 4.36 and indicated with dots of different colors. Since the size of the antenna is doubled compared with the previous design of the 4×4 array, the gain of the antenna is about 3 dBi higher.

4.3 SIW diplexer

In the past decades, the continued development of microwave and millimeter wave technologies has spurred their applications in telecommunication, guidance, navigation, telemetry, detection, remote control, military and medical systems. Ever-increasing system capacity makes the spectrum resources more and more strained. Designs of passive components in RF front-end circuits become crucial on pursuing high performance such as high frequency selectivity, low insertion loss, flat group delay and large power handling. Microwave filter is a two-port network which is frequency selective. One of the promising features of an SIW device is its high quality factor comparing to its planar counterparts. Therefore, SIW technique has been widely applied in the designs of cavity filters and diplexers. Generally speaking, SIW filters can be synthesized following the classic design methodologies and procedures for

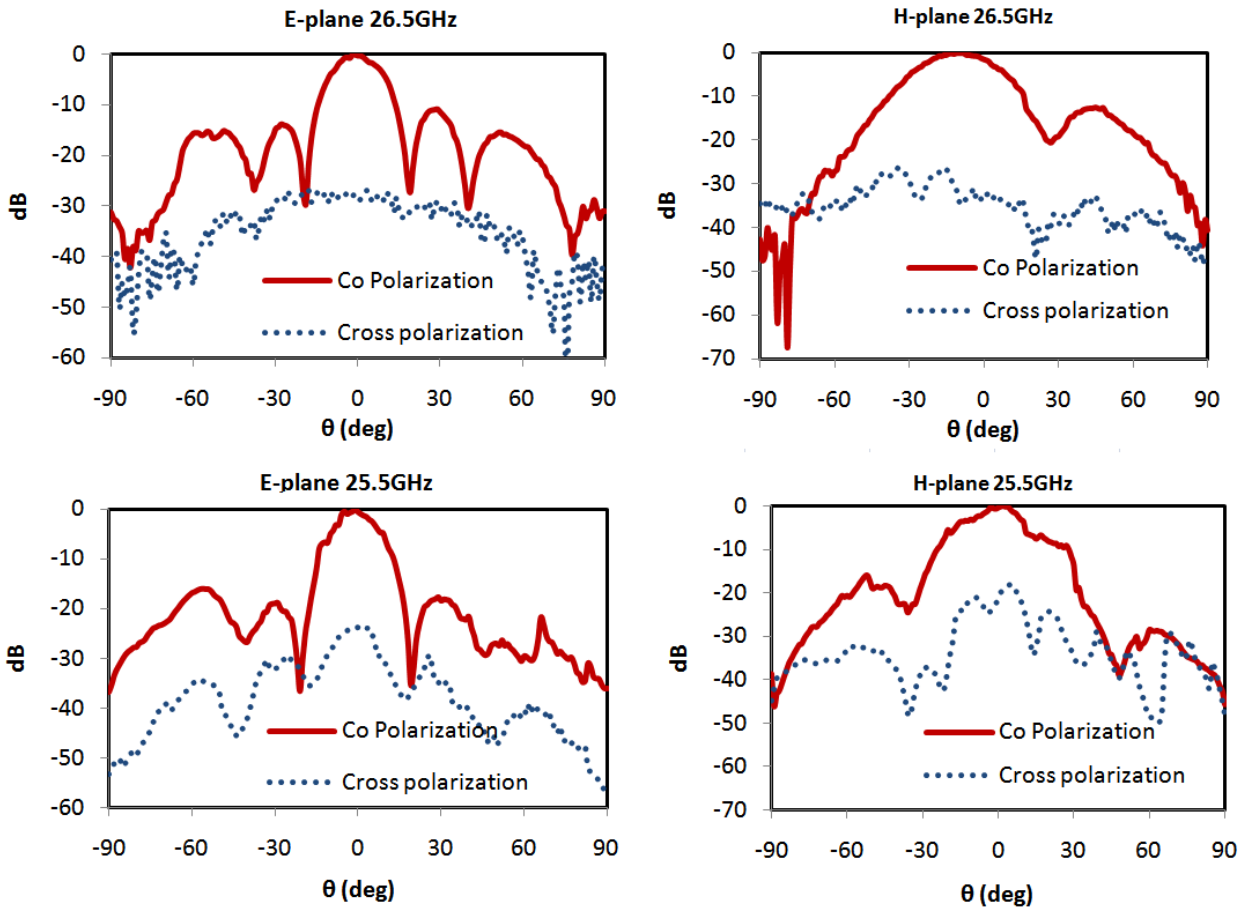


Figure 4.34 Measured E- and H- plane co- and cross- polarization radiation patterns of 8×4 RSIW slot array antenna at 25.5 GHz and 26.5 GHz.

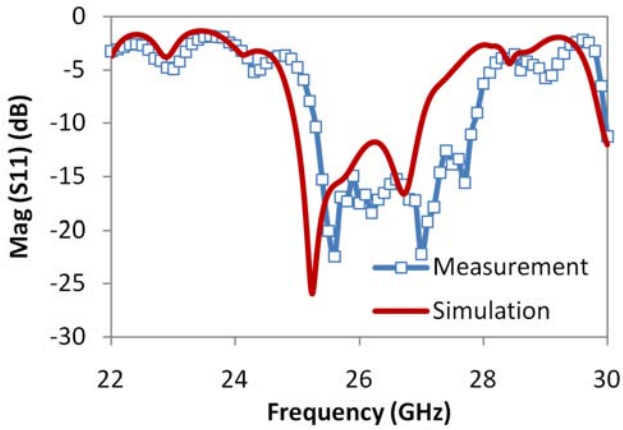


Figure 4.35 Simulated and measured return losses of 8×4 RSIW slot array antenna .

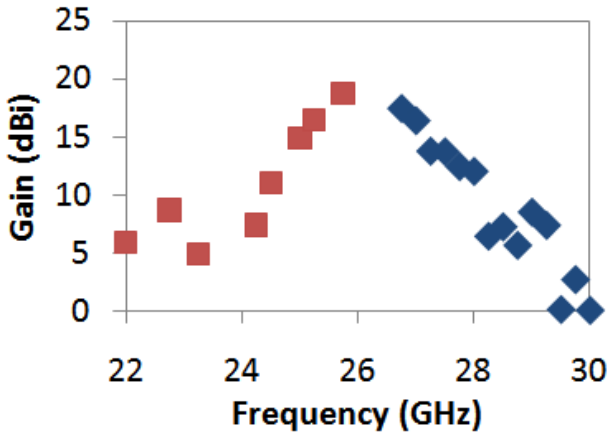


Figure 4.36 Measured broadband gain of 8 × 4 RSIW slot array antenna.

the normal waveguide filters, although there are still some differences between them. The sidewalls of an SIW are rows of plated vias or slots. In order to alleviate the computational burden, these sidewalls are usually modeled as perfect electric conductor (PEC) during the design process. They have to be replaced by vias or slots equivalently after the design is completed and all specifications are satisfied. Secondly, the thickness of the iris in H-plane, whose impact on the device performance usually cannot be ignored, depends on the geometry of the obstacle used to form the sidewalls. The irises on the broad walls of SIWs in multilayer designs can be simply ignored because of the small thickness of the metal layer.

A diplexer is a three-port device which is connected the transmitter and receiver to a single antenna in electronic and communication systems. Two signals can be separated in different approaches (1) by using directional coupler or circulator in which case the two signals do not need to be of different frequencies and (2) by using frequency selective devices such as filters when the frequencies of two signals are usually different. Different types of discontinuities have been used in the SIW filter designs, such as metal post, H-plane iris and slots on the top metal layers. Cavity is a common structure used in the design of filter designs and SIW diplexers (Hao *et al.* (2005c); Han *et al.* (2007); Tang *et al.* (2007); Chen *et al.* (2005)). Since waveguide is a band pass device by nature, all diplexers proposed in these publications consist of a power divider (or a waveguide junction) and two band pass filters (BPFs). In order to enhance the isolation and selectivity of the filters, transmission zeros need to be added to have a sharp slope from passband to stopband. In the design of a diplexer for communication systems, the filters need to be more selective on one side, therefore the transmission zero need to be asymmetrically located. The generalized Chebyshev filters can arbitrarily place transmission zeros in the stopband. The transmission zeros can be added into its response in various ways, such as extracted pole technique (Rhodes et Cameron (1980)),

adding cross coupling between non-adjacent resonators (Levy (1976)), asymmetric iris (Arndt *et al.* (1990)), or other propagating/evanescent mode (Rosenberg et Hagele (1994)).

The specifications used in our diplexer design are given in Table 4.4

	Start Freq (GHz)	Stop Freq (GHz)	BW (MHz)	Isolation (dB)
Filter for Tx	25.3	25.7	400	-40
Filter for Rx	26.3	26.7	400	-40

Tableau 4.4 Specification of BPFs in the design of diplexer.

We firstly design the BPF for each channel with three-pole Chebyshev filters, whose optimized coupling matrix are given as follows.

For transmitter :

$$M_{Tx} = \begin{bmatrix} 0 & 1.2621 & 0 & 0 & 0 \\ 1.2621 & 0 & 1.2455 & 0 & 0 \\ 0 & 1.2455 & 0 & 1.2455 & 0 \\ 0 & 0 & 1.2455 & 0 & 1.2621 \\ 0 & 0 & 0 & 1.2621 & 0 \end{bmatrix} \tag{4.6}$$

For receiver :

$$M_{Rx} = \begin{bmatrix} 0 & 1.2719 & 0 & 0 & 0 \\ 1.2719 & 0 & 1.2793 & 0 & 0 \\ 0 & 1.2793 & 0 & 1.2793 & 0 \\ 0 & 0 & 1.2793 & 0 & 1.2719 \\ 0 & 0 & 0 & 1.2719 & 0 \end{bmatrix} \tag{4.7}$$

The design procedure of a Chebyshev filter implemented by thick inductive irises in a rectangular waveguide has been well described in many publications, for example (Shamsaifar (1992)). The irises are used as impedance inverters and the transmission lines between two irises are half wavelength resonators. The design procedure is briefly summarized as follows.

Step 1 : Using M_{ij} calculates impedance inverters K_{ij}

The value of the impedance invertors in Figure 4.37 can be calculated by the elements of

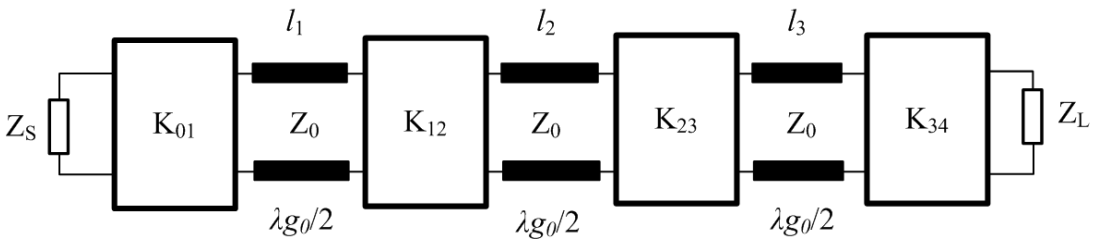


Figure 4.37 Model of bandpass filter with cascaded impedance invertors and transmission line resonators.

coupling matrix as follows.

$$K_{01} = \sqrt{\frac{\pi\omega}{2}}\left(\frac{\lambda g_0}{\lambda_0}\right) M_{1S} \tag{4.8}$$

$$K_{ij} = \sqrt{\frac{\pi\omega}{2}}\left(\frac{\lambda g_0}{\lambda_0}\right) M_{ij},\ where\ i,j = 1,2,3 \tag{4.9}$$

$$K_{34} = \sqrt{\frac{\pi\omega}{2}}\left(\frac{\lambda g_0}{\lambda_0}\right) M_{3L} \tag{4.10}$$

where λg_0 and λ_0 are the wavelengths in substrate and free space, respectively, and the lengths of the transmission line resonators $l_1 = l_2 = l_3 = \lambda g_0/2$.

Step 2 : Using impedance inverter values K_{ij} calculates equivalent susceptances χ_1 and χ_2

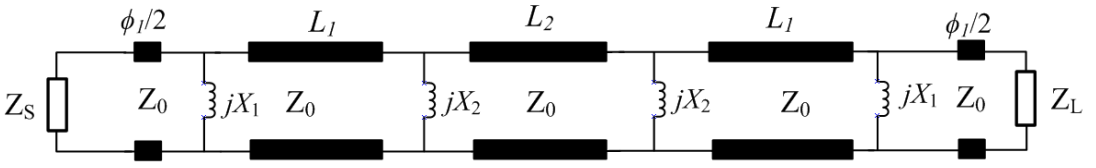


Figure 4.38 Model of bandpass filter with shunt inductors and revised transmission line resonators.

An iris with finite thickness can be modeled by a shunt inductor and a pair of transmission lines on its both sides, as shown in Figure 4.38. The normalized susceptance χ of the inductor and the electric length of the transmission lines ϕ between irises can be expressed by the

normalized impedance of the K invertor as follows.

$$\frac{\chi}{Z_0} = \frac{K_{ij}/Z_0}{1-(K/Z_0)^2} \tag{4.11}$$

$$\phi = -\arctan(2\chi/Z_0) \tag{4.12}$$

And the lengths of the transmission line resonators need to be revised as

$$L_1 = l_1 + \phi_1/2 + \phi_2/2 \tag{4.13}$$

$$L_2 = l_2 + \phi_2/2 \tag{4.14}$$

Step 3 : Find the dimension of inductive irises which can be equalized with the same susceptances χ_1 and χ_2

To simplify the design procedure, we fix the iris thickness as d shown in Figure 4.39. Only the widths of the iris d_1, d_2 and the lengths of the resonators S_1 and A need to be deduced from the equivalent susceptance of the iris which we obtained in Step 2. The conversion, from the equivalent sustenance to the physical dimensions of an iris, usually is achieved through a parameter extraction based on the curve fitting of S-parameters. The S-parameters of an iris are firstly calculated by either analytic formulations or full-wave EM applications. By comparing so-calculated S-parameters with another result calculated from the equivalent circuit of the iris, the equivalent susceptance and a small phase offset which represents the finite thickness of the iris can then be extracted.

When d is fixed:
X_1 -> d_1, ϕ_1
X_2 -> d_2, ϕ_2
L_1, ϕ_1 -> S_1
L_2, ϕ_2 -> A

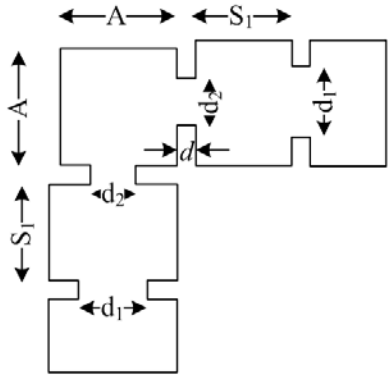


Figure 4.39 Conversion from the equivalent circuit to physical dimension of an iris.

The distance between two outputs of the diplexer needs to be large enough so that the following devices of the transceiver can be put between them. Therefore we replace the middle cavity of a conventional in-line filter with a corner cavity as shown in Figure 4.39. Two irises

on the corner cavity are on its symmetric plane, the cavity can be designed following the same procedure of the in-line filter design. Two Chebyshev filters for the transmitter and receiver are so designed, shown in Figure 4.40, respectively. In these two figures, the S-parameters calculated from the coupling matrix (with the quality factor of 400) are compared with those obtained from an Ansoft HFSS simulation.

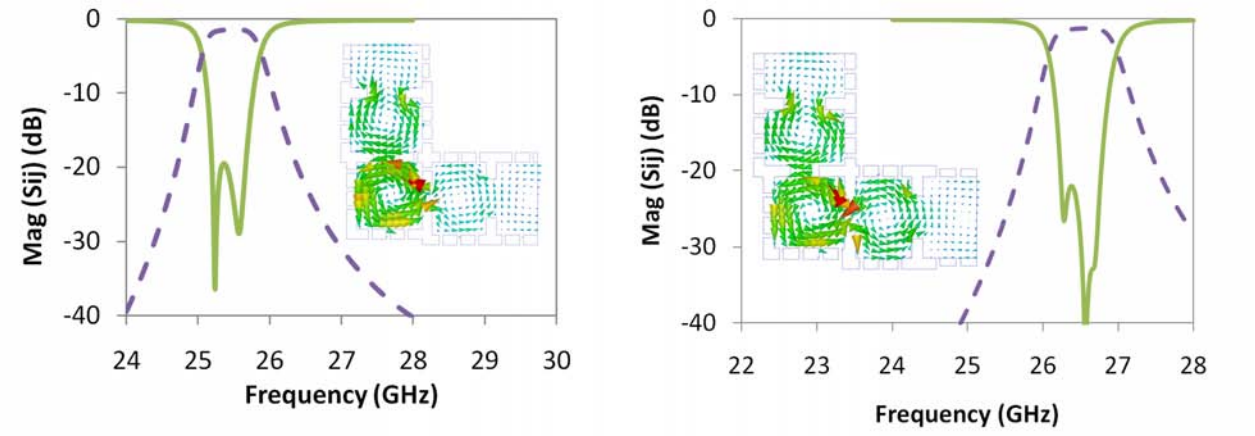


Figure 4.40 Initial design of 3-pole filters for transmitter and receiver respectively.

If these two filters are used in our design of the diplexer, the transmitter and receiver channel cannot have the expected isolation (40 dB). Therefore, additional transmission zeros need to be added into the responses of the two filters, such as by adding transmission zeros in the stopband where the isolation needs to be improved. The mutual coupling matrixes of a three-pole filter can be written as follows,

$$M = \begin{array}{c|ccccc} & S & 1 & 2 & 3 & L \\ \hline S & 0 & M_{1S} & 0 & 0 & 0 \\ 1 & M_{1S} & M_{11} & M_{12} & M_{13} & 0 \\ 2 & 0 & M_{12} & M_{22} & M_{23} & 0 \\ 3 & 0 & M_{13} & M_{12} & M_{33} & M_{3L} \\ L & 0 & 0 & 0 & M_{3L} & 0 \end{array} \tag{4.15}$$

where the mutual coupling between resonators 1 and 3, M_{13}, can be either positive or negative. The sign of this coefficient decides whether the frequency of so-caused transmission zero is higher or lower than the passband (Hagensen (2010)). As proposed by Guglielmi *et al.* (1995), a transmission zero can appear in a BPF's stopband when the high order modes around the irises can be coupled with each other. When the two irises on adjacent side walls of a corner cavity have an offset to the symmetric plane and get closer to each other, a transmission

zero on the right-hand side of the passband can then be generated. The frequency of the transmission zero can be tuned by changing the location of the irises, i.e. variable t indicated in Figure 4.41. When two irises get closer to each other, the coupling between them become larger and the transmission zero also moves closer to the passband. However, the coupling so-caused is still not large enough to have the required steep stopband performance. In Figure 4.41, when the variable t changes between 0 mm to 0.6 mm, the obtained transmission zeros of the transmitter filter are all higher than 28 GHz. Since adjusting the location of the iris only cannot provide sufficient coupling that we need, other techniques need to be adopted here to improve the edge steepness between the passband and stopband. Moreover, for the receiver filter, we need the transmission zero on the left-hand side of the passband which cannot be implemented by adjusting the location of the irises.

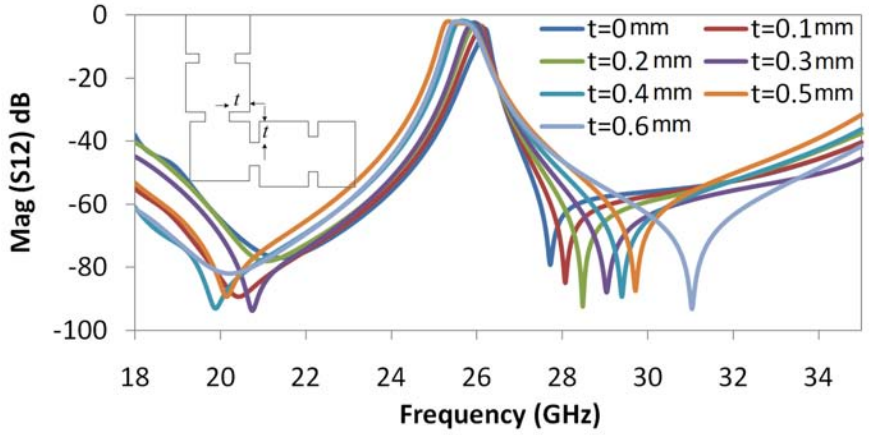


Figure 4.41 Transmission zero changing with the location of the irises.

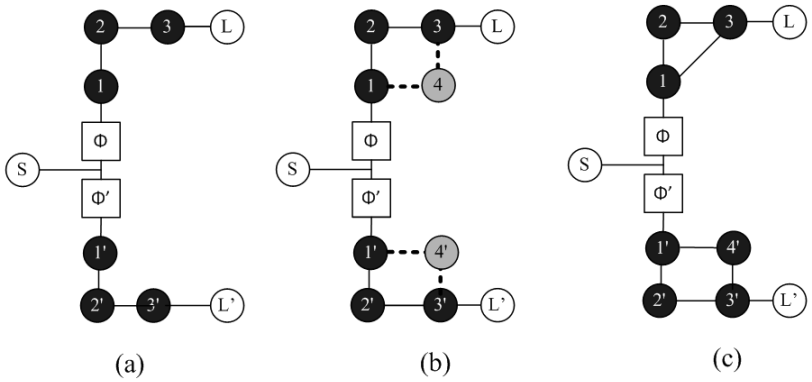


Figure 4.42 Topologies of two diplexers composed of (a) Chebyshev bandpass filter and (b) generalized Chebyshev bandpass filter.

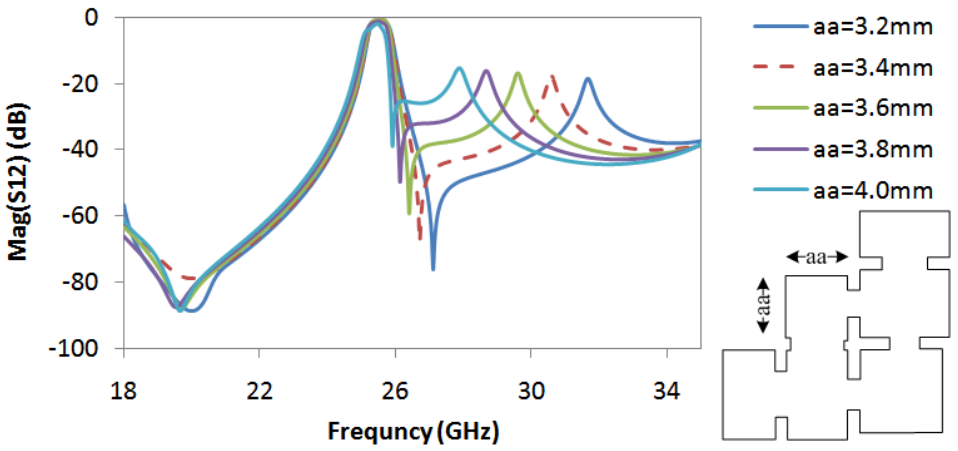


Figure 4.43 Transmission zero of transmitter filter changing with *aa*.

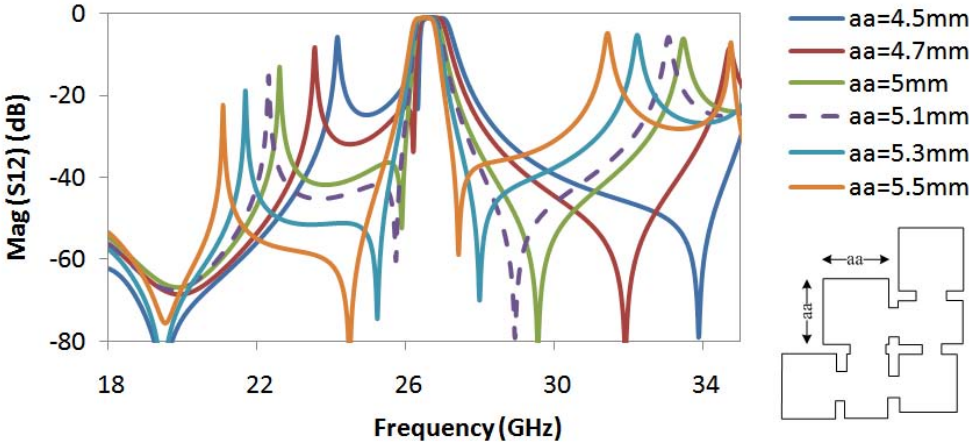


Figure 4.44 Transmission zero of receiver filter changing with *aa*.

In order to have a transmission zero at an arbitrary place, we add a square cavity (4 and 4′) between the first and third resonators, as shown in Figure 4.42(b). The two non-resonant nodes are both square cavities and each has two irises coupled with resonators 1 and 3. It is found that the transmission zero can be efficiently tuned by the side length of this additional cavity. In the transmitter filter, the length of the third cavity is reduced from 3.78 mm to 3.37 mm and the side length of the cavity (3.47 mm) is close to the length of the third cavity. For these two reasons, the two cavities (3 and 4) can be regarded as one large rectangular cavity whose overall resonant frequency is very close to that of cavity 1. The circuit model of the filter can be simplified as three cavities having a positive mutual coupling between every two cavities, as shown in Figure 4.42(c). As summarized by Thomas (2003), when the all mutual couplings between three cavities are inductive, the transmission zero will be located

above the passband. Moreover, the location of the transmission zero above the passband can be tuned by the side dimension of the forth cavity (aa) as shown in Figure 4.43.

In the receiver filter, there is at least one transmission zero needed on the left-hand side of the passband. It is also implemented by adding an additional cavity between the original first and third cavities as shown in Figure 4.42(b). The side dimension of the added cavity is 5.14 mm in the optimized design, which corresponds to a resonance at 22 GHz. The response of the filter has two transmission zeros located on different sides of the passband. The transmission zeros can also be changed by adjusting the length of the side dimension aa. As shown in Figure 4.44, when aa is increased, both two transmission zeros shift to the lower frequencies.

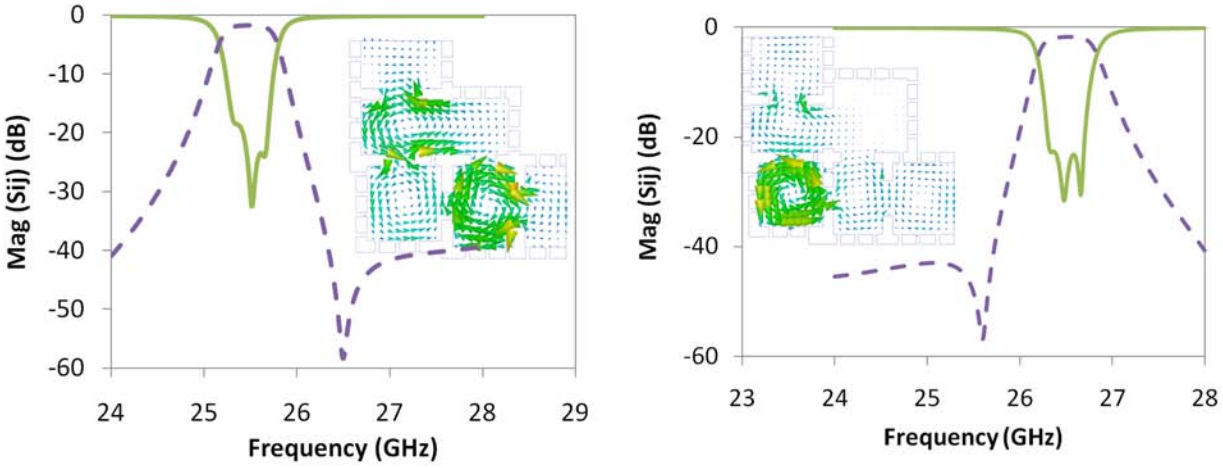


Figure 4.45 Optimized filters for transmitter and receiver.

The response of two optimized filters is plotted in Figure 4.45. The proposed diplexer is composed of two optimized filters and an SIW T-junction as shown in Figure 4.46. The location and width of the iris on the common port and the lengths of two arms connected with filters are variables used in the optimization of diplexer. The final layout and dimensions of the diplexer and GCPW-to-SIW transitions at the three ports are shown in Figure 4.46. The simulation (using Ansoft HFSS) and measurement results are compared in Figure 4.47. In simulations, the return loss at the three ports are all below -20 dB. The minimum insertion loss for transmitter and receiver filters are -1.91 dB and -2.21 dB, respectively. Considering the diameter of the laser beam in our micro-fabrication is about 4 mil, we shift all edges toward interior for 2 mil in the fabrication. In measurements, the minimum insertion loss in the two passbands are -2.98 dB and -3.63 dB respectively. The return loss at the antenna port (S_{11}) and transmitter port (S_{22}) are both less than -15 dB within the passbands. The isolation

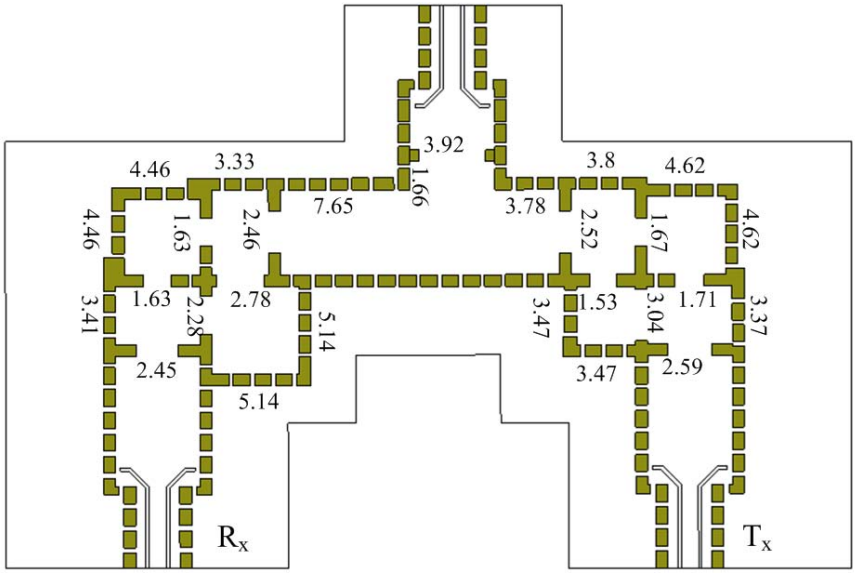


Figure 4.46 Layout and dimensions of diplexer.

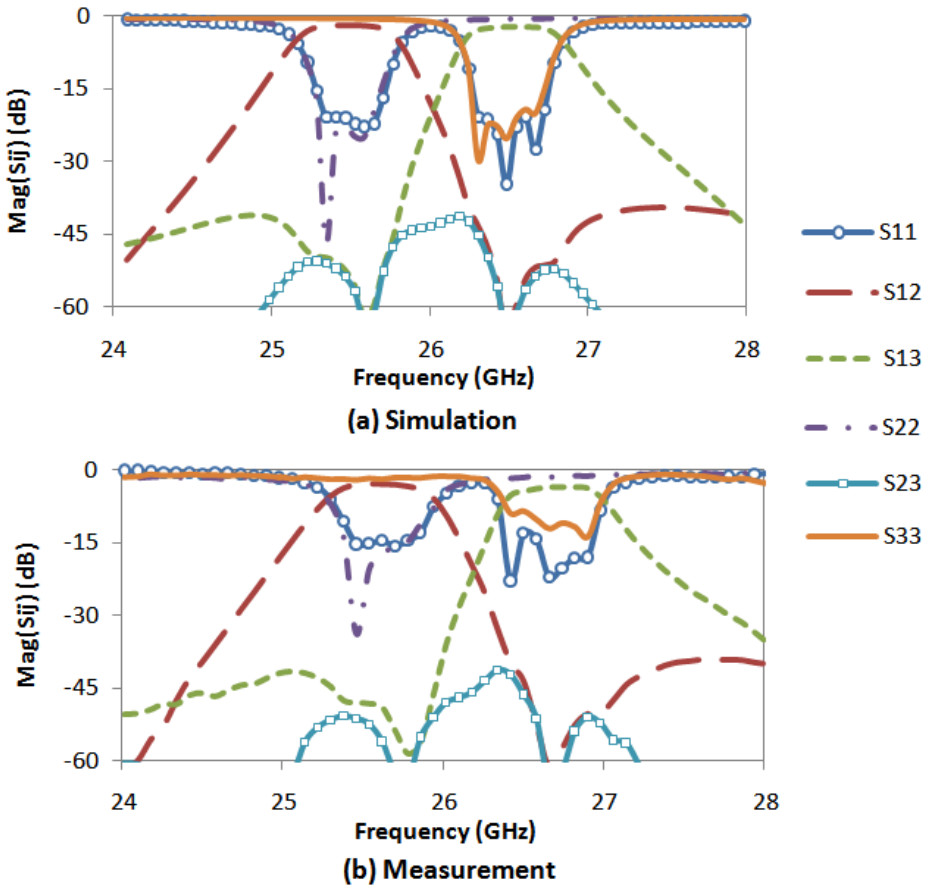


Figure 4.47 Simulation and measurement of diplexer.

between the transmitter and receiver filters is lower than -40 dB in both the simulation and measurement results.

4.4 Dual-antenna measurement

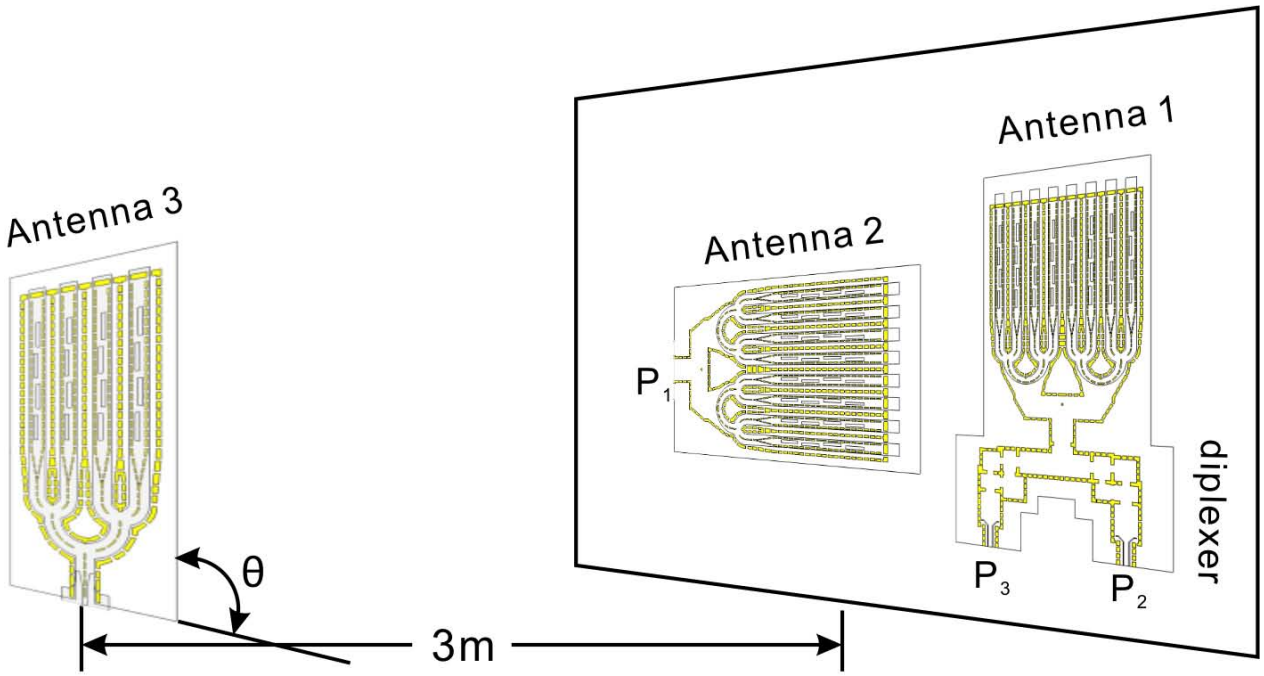


Figure 4.48 Setup of dual antennas.

In order to simplify the system structure, two same antennas need to be used in a transceiver system. One is for the transceiver and the other is to receive the carrier when the system works in the receiver mode. An experiment is conducted for the purpose of testing (1) the isolation between the uplink and downlink channels and (2) the isolation between transceiver antenna and carrier antenna. In the experiment, the three antennas are placed as shown in Figure 4.48. Antennas 1 and 2 are perpendicularly fixed. Antenna 1 for transceiver is vertically positioned and connected with the SIW diplexer designed in the previous section. Antenna 2 for receiving the carrier is horizontally positioned. The outputs of the antennas P_1, P_2 and P_3 are for receiving carrier, Tx channel and Rx channel, respectively, and they are connected with Agilent power detectors in the experiment. Another antenna 3 gets an input signal from a microwave signal generator and transmits this source to the other two antennas. Antenna 3 can be placed either vertically or horizontally so that only one of two receiver antennas is on its co-polarization direction and the other is on the cross-polarization direction.

The distance between the source antenna and two receiver antennas is 3 meters. The path loss between two antennas can be calculated with the Friis transmission loss equation.

$$Loss(dB) = 10\log\left(\frac{4\pi d}{\lambda}\right)^2 \tag{4.16}$$

where the path length d is the distance between the two antennas. The calculated path loss at 26 GHz for 3 meters is about 70 dB. The expected received power can then be estimated with the equation below.

$$P_{in} = P_{out}(dBm) - G_T(dBi) - G_R(dBi) - PathLoss(dB) - OtherLoss(dB) \tag{4.17}$$

where the other loss includes the insertion loss in the filters and connectors, which is around $4 \sim 5$ dB in total. The output level of the signal generator is set as 10 dBm. The results of two measurements when θ is 0° and 90° are plotted in Figure 4.49. Because of the fabrication error, both Tx and Rx channels are shifted upward by 500 MHz. The parameters read at 26 GHz (for Tx channel) and 27 GHz (for Rx channel) are listed in Table 4.5. From this table, the isolation between the carrier antenna and the transceiver antenna is about 23 dB. The isolation between the Tx channel and the Rx channel is larger than 45 dB. When the input of transmitter P_2 is 10 dBm, the output P_1 of antenna 2 is lower than -52 dBm.

Frequency (GHz)	θ	P_1(dBm)	P_2(dBm)	P_3(dBm)
26	90°	-53	-36	-68
26	0°	-34	-63	-64
27	90°	-59	-69	-39
27	0°	-34	-62	-62

Tableau 4.5 Power received in a dual-antenna measurement.

4.5 Conclusion

In this chapter, we design and measure a front-end which is composed of a 4×8 SIW slot array antenna and an SIW cavity diplexer. The design is integrated on a two layer Rogers substrate. The antenna is feeding through a network made by RSIW and TFSIW. A 9% (-10 dB) impedance bandwidth covers two passbands of the following SIW diplexer. The antenna has a 15 dBi broadband gain within the two passbands of the diplexer. Two extra transmission zeros, each introduced in one passband of the diplexer, provide a 40 dB isolation between two passbands. Two such 4×8 linear polarized antennas are orthogonally placed for testing the polarization isolation loss. A 23 dB isolation between the two antennas is

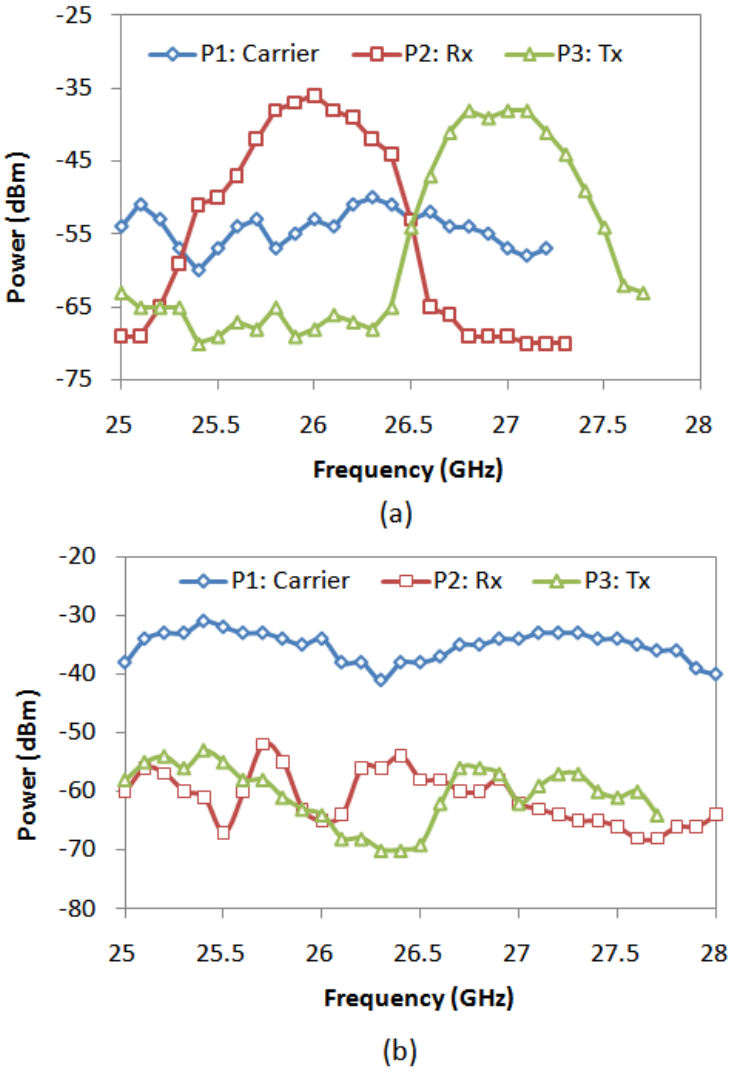


Figure 4.49 Dual antenna measurement, (a) $\theta = 90°$, (b) θ=0°.

good enough for a dual antenna transceiver system, in which they are for transmitting of the modulated signal and carrier signal, respectively.

CHAPITRE 5

Electronically Tuned Substrate Integrated Waveguide Phase Shifter and Modulator

5.1 Introduction

Most applications of SIW circuits are still limited in the design and development of passive components, antennas or antenna arrays. In order to expedite the usage of SIW technique into more applications, it is imperative to develop SIW devices with new features such as tunability. Phase shifter is an important microwave device in many applications. Semiconductor devices are often used in planar circuits to change the phase and/or amplitude of a RF signal passing through them. Compared with other techniques available to the design of a tunable phase shifter such as micro electro mechanical system (MEMS), ferrite and ferroelectric materials, a varactor tuned phase shifter has advantages in terms of extremely fast tuning speed, easy assembling and controlling, small size and low power consumption.

The phase of an electronically tuned phase shifter can be changed continuously or discretely, which are called analog phase shifter and digital phase shifter, respectively. From the perspective of the design structure, a phase shifter can be classified into two groups, inline type and reflection type. A digital inline SIW phase shifter was implemented by inserting two PIN diodes into the substrate as switchable shorted posts (Sellal *et al.* (2008)). The phase of the transmission coefficient was digitally tuned by switching the diodes on and off. The tuning step of the phase between two states was about 15°. A 360° reflection-type phase shifter was composed of a 3 dB coupler and two SIW shorts (Sbarra *et al.* (2009)). Each short termination was continuously tuned by two varactors loaded through the slots on the top metal layer.

Several different technologies have been used in the design of phase shifter, such as ferrite, ferroelectric thin film, semiconductor diode, MEMS, varactor diode and etc. All these techniques have both advantages and shortcomings. The factors need to be considered for selecting a proper technique for a specific phase shifter design include cost, reliability, power handling capacity, switching speed, DC power consumption, size, linearity and the complexity for fabrication. Integration, switching speed and RF loss are the essential issues to be considered in our application. Our original objective is to use a tunable device to control an SIW phase shifter digitally, so that a six-port SIW I/Q vector modulator can be implemented by using a combination of some 3 dB couplers and tunable terminators. This idea was propo-

sed and demonstrated in the previous designs for some lower-frequency and microstrip-based applications. Therefore, a tunable SIW termination is first designed by using a PIN diode of semiconductor technique in section Section 5.3. However, the termination implemented by PIN diode-loaded SIW has a limited accuracy on phase shifting and unsatisfactory magnitude flatness. Hence, a flip-chip varactor diode is used in all designs of different phase shifter from Section 5.2. In this chapter, an inline phase shifter and reflection-type phase shifter are designed using SIW technique and both of them are controlled by varactor diodes. The varactor diodes in these two design platforms are assembled in different manners. The design layout and correlation between the results of equivalent circuit model, EM model and measurements are discussed.

5.2 Diode loaded onto SIW

One way to load a semiconductor device to an SIW is to directly insert the component into the substrate (Sellal *et al.* (2008)). Such a design has stringent requirements on substrate removal and component assembling. Moreover, the EM modeling of such a hybrid circuit is still a challenging work and usually has a lower accuracy compared with the design techniques presented in this work, where devices are loaded from outside or on the surface of an SIW.

5.2.1 Diode loaded with line transformation

The most straightforward way to connect a packaged or bondable semiconductor device with an SIW is to transform the SIW to another classic planar transmission line, such as microstrip line or coplanar waveguide (CPW). The device can then be assembled on those lines using the conventional assembling techniques and analyzed with the established equivalent circuits and modeling methodologies.

In this work, a short termination (Figure 5.1) is needed in the design of a reflection-type phase shifter. Instead of a typical 50 Ohm line of microstrip or CPW, the SIW is directly transformed to a transmission line whose dominant mode is a quasi-TEM mode, similar to a parallel-plate transmission line. The characteristic impedance Z_t of this line is about 20 Ohm. The reason why we choose this low impedance line is that a design with a smaller value of Z_t has a larger maximum tuning phase shift (Lin *et al.* (2007)).

As shown in Figure 5.1, the short termination is implemented simply by inserting two longitudinal slots along the side walls of SIW. A pair of transversal slots are used at the start of line transformation for improving the matching. The central metal piece is electrically separated from the other metallic parts on the top, which makes the assembling of diodes more convenient. The control voltage can be added to the diodes through a fine line connected from

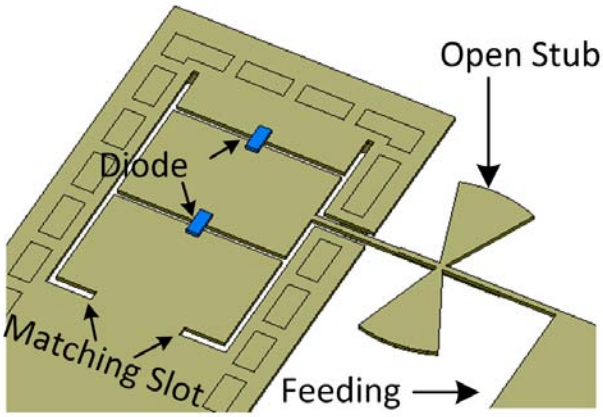


Figure 5.1 Proposed dual-varactor tuning short termination with feeding circuit.

the side. The butterfly stub on the fine line is for establishing an open boundary condition at the junction.

5.2.2 Diode loaded through slot

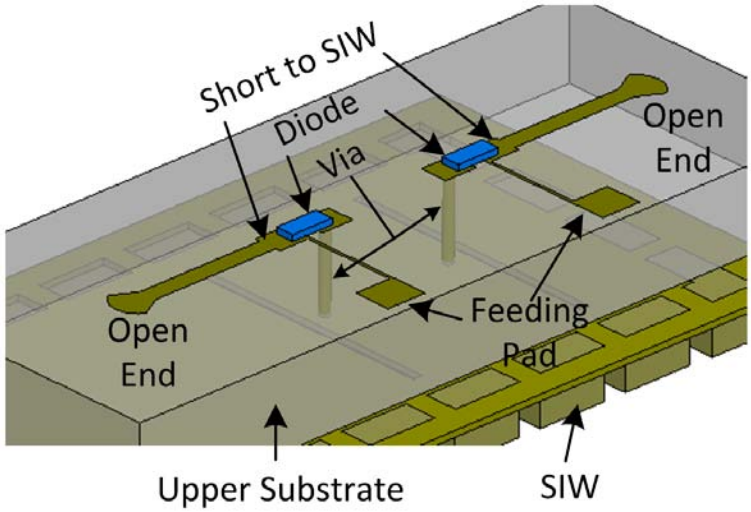


Figure 5.2 Isolating DC from ground using a substrate layer.

A semiconductor device can also load an SIW through a slot which is opened in the top metal layer (Sbarra *et al.* (2009)). Unlike other conventional planar transmission lines, a waveguide or a waveguide-type device, such as an SIW, has a closed structure. There is no path electrically separated from the ground for DC signal. When loading an SIW through a slot, we need to avoid a direct contact between the SIW and both pads of the diode. In (Sbarra *et al.* (2009)), an isolation was provided by a substrate located between the diode

and the SIW. As shown in Figure 5.2, one pad of the diode directly connected with the SIW through a via-hole and the other pad was RF shorted to the ground with a microstrip butterfly stub. However, this design of isolation brings more parasitic effects and the fabrication is also complicated.

In this work, we use a bondable chip capacitor as the DC block between the SIW and one pad of the varactor chip (Microsemi MV39002-P2715), as shown in Figure 5.3. To balance the height of two sides, a metal block with the same thickness is placed under the other pad. Since the value of chip capacitor, 50 pF in our design, is much larger than the value of the varactor and the equivalent capacitance of the slot, it can be ignored in the EM modeling of the RF path. A bonding wire connects the chip capacitor and a feeding pad for adding the control voltage. Therefore, the DC signal is electrically separated from the ground by the chip capacitor. In the next section, an inline phase shifter is designed and fabricated with the control element, a varactor diode, assembled in this way. From the comparison between simulation and measurement, it is observed that this assembling method provides a convenient and stable DC voltage to the varactor and also an ignorable parasitic effect in the EM modeling of the RF path.

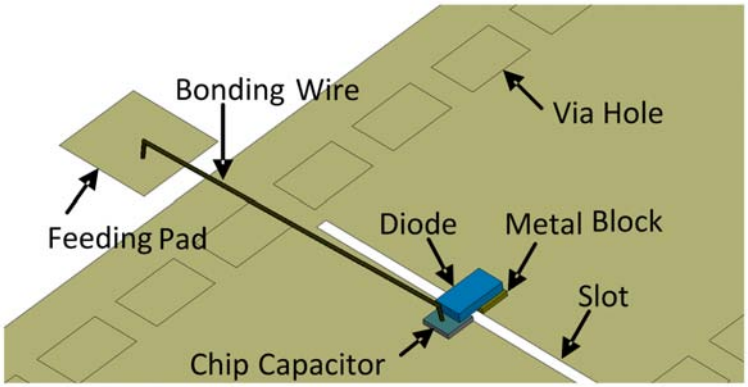


Figure 5.3 Chip capacitor as the DC block between varactor and SIW.

5.3 PIN diode-tuned SIW termination

An SIW short termination tuned by four PIN diodes are shown in Figure 5.4. The design of matching layout is discussed in the next section. In this section, we focus on the performance of termination loaded by PIN diodes. The diode we use here is MA4AGBLP912 of M/A-COM, a low series resistance and low capacitance GaAs PIN diode in beamlead package. The equivalent circuits of this diode with the forward and reverse biases are given in Figure 5.4. The diode with the reverse bias can be looked as a capacitor and an inductor in series, whose

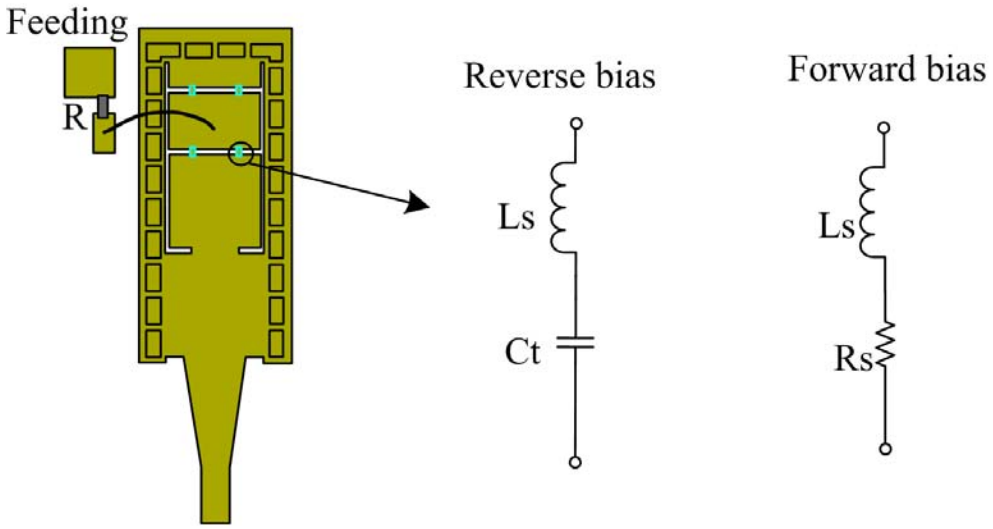


Figure 5.4 PIN diode-tuned SIW termination and equivalent circuits of the PIN diode with forward and reverse biases.

values are experimentally extracted $C_t = 28.5$ fF and $L_s = 0.07$ nH. A forward biased PIN diode can be modeled with a resistor and an inductor in series whose values are $R_s = 4\ \Omega$ and $Ls = 0.07$ nH. The capacitor represents the total reversed capacitor and the inductor is from the packaging effect. Four PIN diodes are placed across the gap and connected in parallel. A wire bridge is used to add the biasing of the PIN diodes to the middle of the rectangular pad. A surface mounted resistor is used for the purpose of limiting the current when the diode is forward biased.

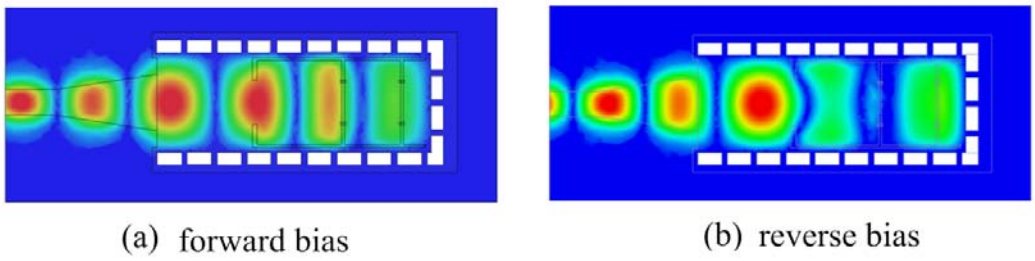


Figure 5.5 Field distribution of SIW termination with PIN diode forward biased and reverse biased.

Ansoft HFSS is used in the design of such a structure in Figure 5.4. The equivalent elements of the diode are assigned as boundary conditions on a rectangle and placed on the SIW for representing the PIN diode in a full-wave simulation. Simulated field distributions in the SIW termination when the diodes are forward biased and reverse biased are shown in

Figure 5.5. To verify the effectiveness of such a simulation, the designed SIW termination is fabricated. The measured S-parameter is compared with simulation results in Figure 5.6. The values of elements in the equivalent models are so-extracted from the measurement and simulation correlation. It is observed that the simulation has a satisfying accuracy when the equivalent elements are assigned with proper values.

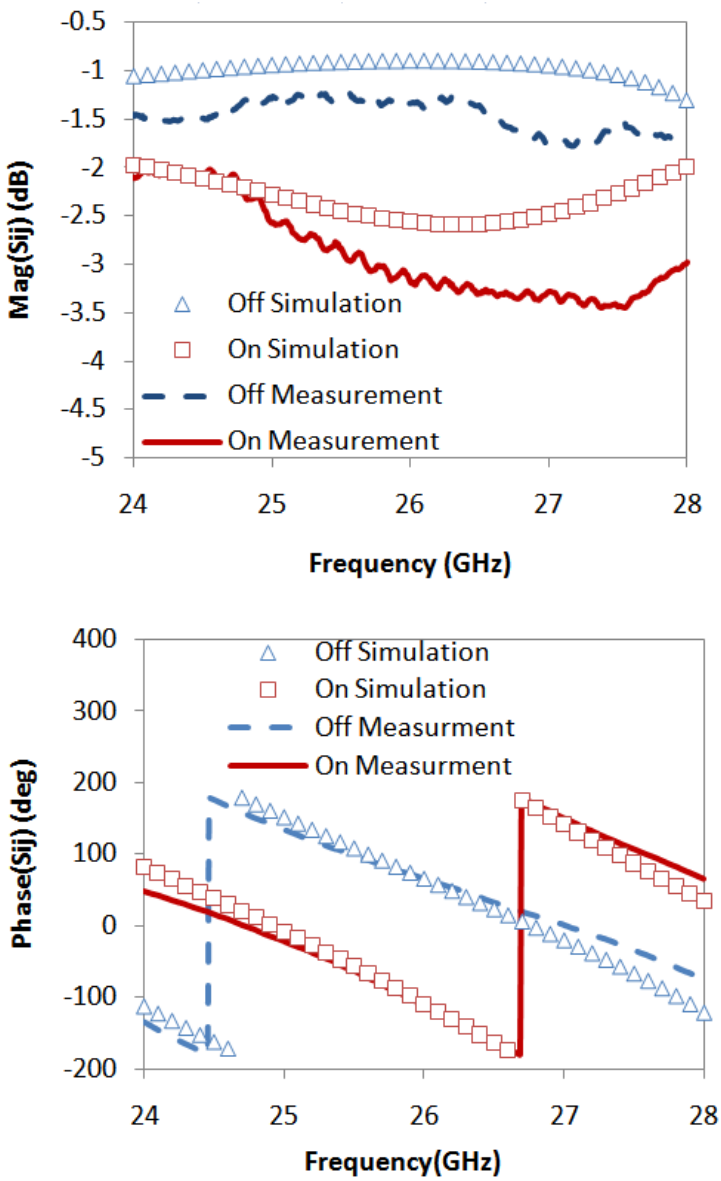


Figure 5.6 Comparison of simulation and measurement of PIN diode-tuned SIW termination.

Since a PIN diode has only two states and there is no other tuning scheme in the designed structure, the tolerances requirement is rigorous to obtain the two states with designed phase shifts. Some parametric analysis is conducted to investigate the impact of the device and

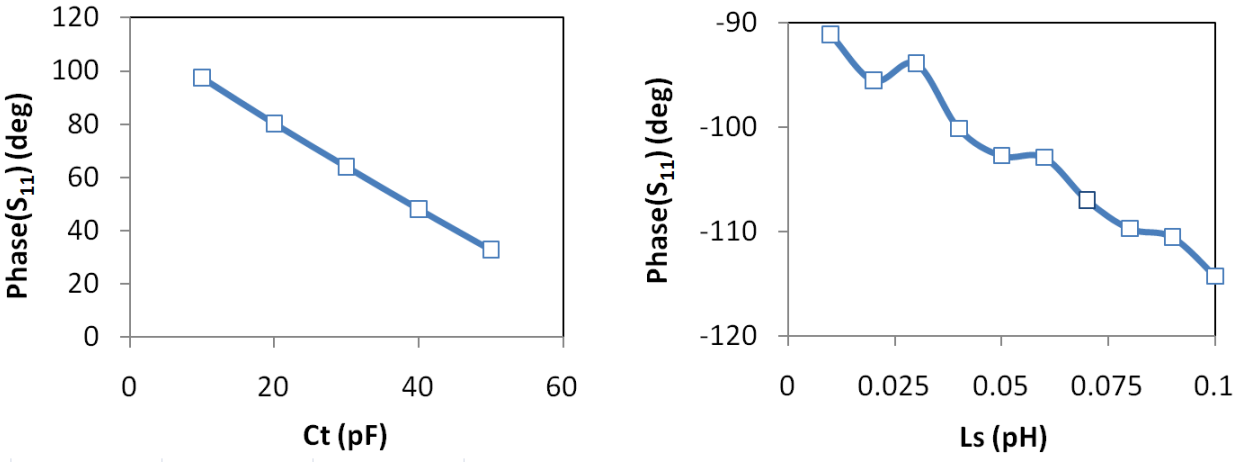


Figure 5.7 Phase of reflection in SIW termination changing with equivalent elements of PIN diodes, total capacitance C_t and package inductance L_s.

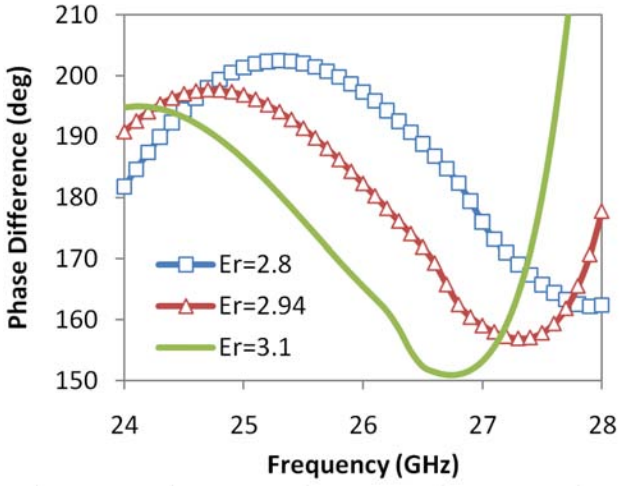


Figure 5.8 Phase of reflection in SIW termination changing with the dielectric constant of substrate.

substrate tolerance on the phase shift between the two states. Figure 5.7 shows the change of the phase of reflection when the total capacitance and package inductance of the PIN diode are adjusted within the tolerated range given in the datasheet. A phase shift larger than 50° and 25° are observed when C_t and L_s are changed within the range [10 pF $\sim$ 30 pF] and [0.01 pH $\sim$ 0.1 pH], respectively. This values of C_t and L_s can vary between individual components and it is an absolute and unpredictable phase error between simulation and experiment. Furthermore, the tolerances of the dielectric constant of substrate can also affect the accuracy of the design. The substrate used in the design is Rogers Duriod 6002 and the

range of dielectric constant in specification is ±4%. The phase difference between the two states changing with the effective dielectric constant of substrate is plotted in Figure 5.8. From this figure, we can conclude that a 20° phase error might be caused by the variation of the dielectric constant. By observing the parametric analysis shown in Figure 5.7 and Figure 5.8, we decide to look for another phase shifter design with a more flexible tuning scheme. Different from a diode with only two states, a varactor tuned phase shifter has a successive tunability and therefore is a more suitable candidate for our design.

5.4 Varactor-tuned inline phase shifter

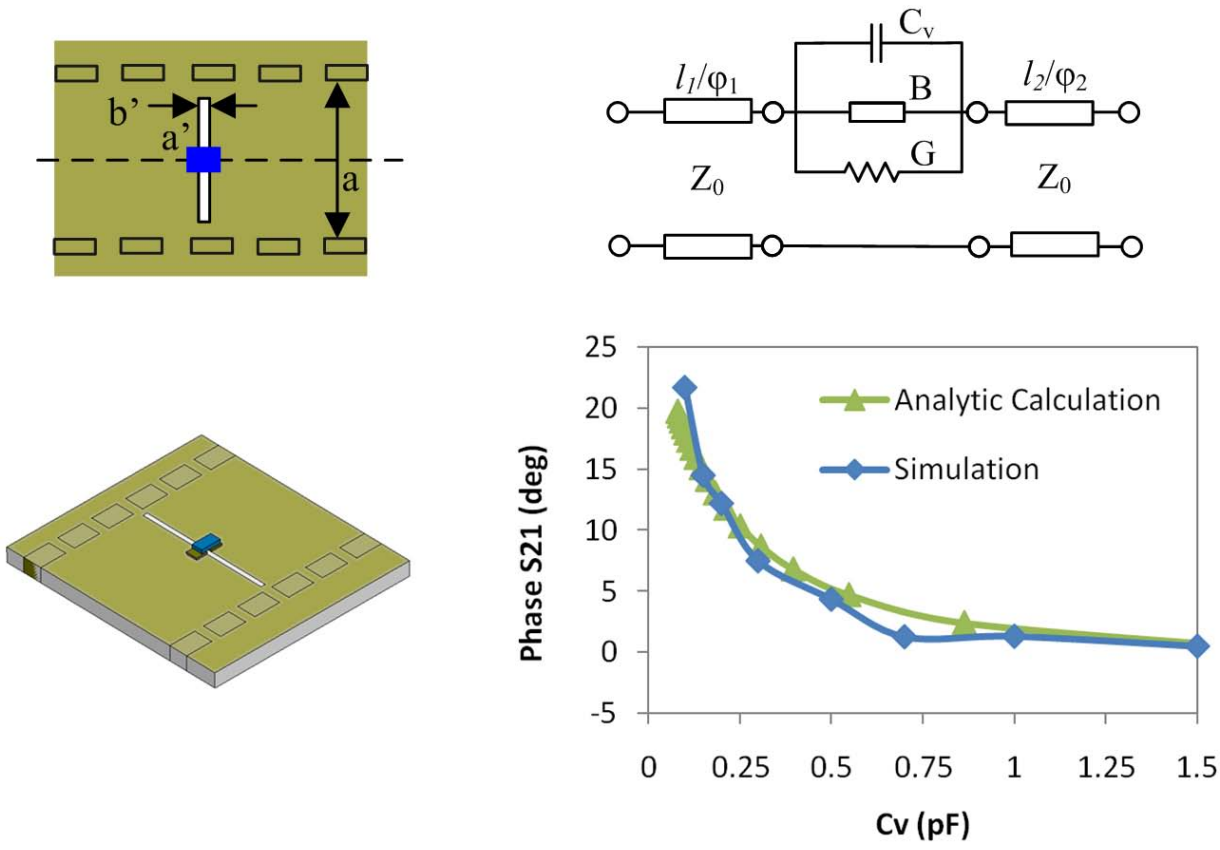


Figure 5.9 Equivalent circuit of an SIW loaded by a varactor diode through a slot and phase shift of S_{12} calculated using EM model and equivalent circuit model : $a = 5$ mm, $a' = 4.57$ mm, and $b' = 0.167$ mm.

An inline phase shifter can be obtained by simply loading SIW with a varactor diode through a transversal slot on the top. The equivalent circuit of such a design is shown in Figure 5.9, where a is the width of SIW, a' is the length of slot and b' is the width of slot.

The varactor is in parallel with the equivalent circuit of the slot, and they both connect the SIW in series. The capacitance of the varactor can be calculated using the following equation.

$$C_v(V) = \frac{C_j(0)}{(1 + V/\Phi)^\gamma} \tag{5.1}$$

where C_j is the junction capacitance when control voltage is 0 V, Φ is the built in potential (1.2 V for the varactor is used in our work) and γ is the tuning slope. The normalized admittance of the slot $\tilde{G} + j\tilde{B} = Y_0 \cdot (G + jB)$ can be evaluated by Equation 26 and Equation 33 in Oliner (1957), where Y_0 is the characteristic admittance of SIW. Transmission coefficient T can be calculated with Equation 5.2 and phase shift $\Delta\Phi$ is defined in Equation 5.3. When C_v is tuned from 0.09 pF to 1.8 pF, the calculated phase shift is correlated with the EM simulation results obtained from HFSS, as shown in Figure 5.9.

$$T(C_v) = \frac{2}{2 + Y_0/(G + jB + j\omega C_v)} \tag{5.2}$$

$$\Delta\Phi = |\angle T(C_{vmin}) - \angle T(C_{vmax})| \tag{5.3}$$

The tuning range of phase shift can be quickly evaluated using this equivalent model when we choose an appropriate varactor product for our design.

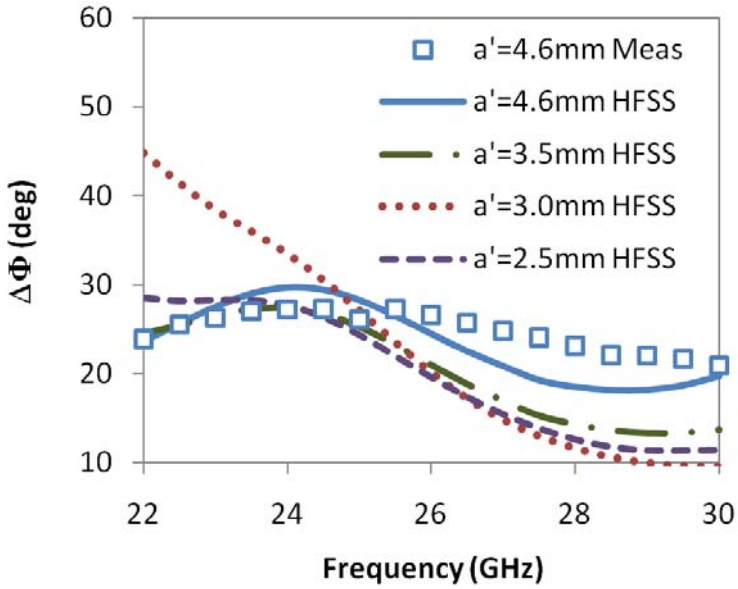


Figure 5.10 Chip capacitor as the DC block between varactor and SIW.

The resonant frequency of the transverse slot (f_s) should be designed far below the working frequency band of the SIW in order to eliminate unexpected radiation from the slot. The

frequency performance of phase shift $\Delta\Phi$ changing with the length of slot a' is shown in Figure 5.10. It is observed that resonant frequency f_s moves upward to the working frequency band when the length of slot a' becomes smaller. Meanwhile, the flatness of phase shift $\Delta\Phi$ within the entire frequency band degrades, whereas the tuning range of $\Delta\Phi$ may increase at some frequency points. Since the flatness of $\Delta\Phi$ is one of the most important specifications in the design of a phase shifter, we use the maximum value of $a' = 4.6$ mm in our design. A larger tuning range of an inline phase shift can be achieved by cascading more tuning elements with half wavelength spacing.

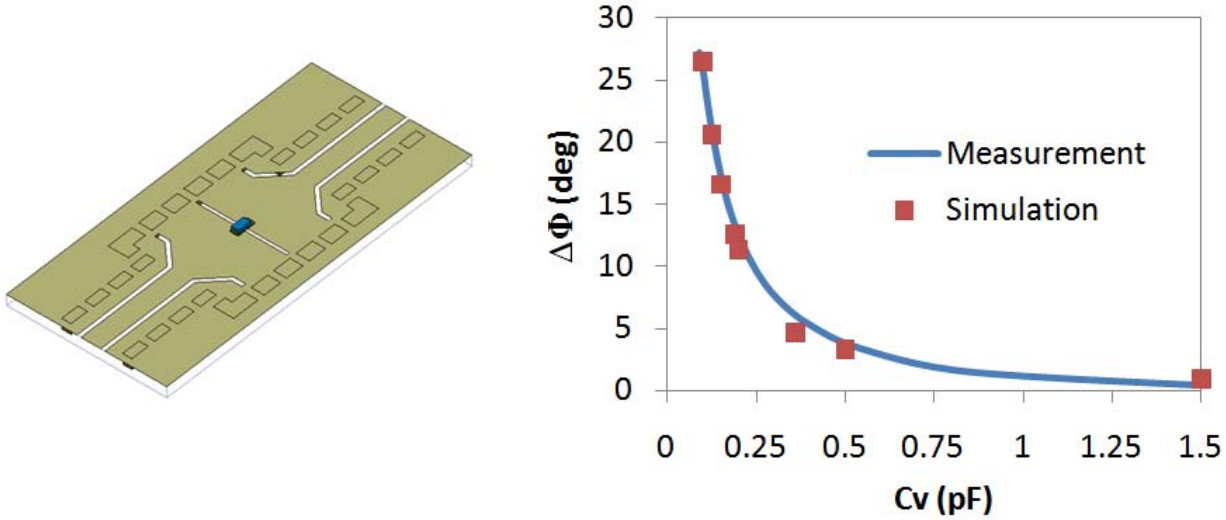


Figure 5.11 Simulation and measurement correlation of phase shift $\Delta\Phi$.

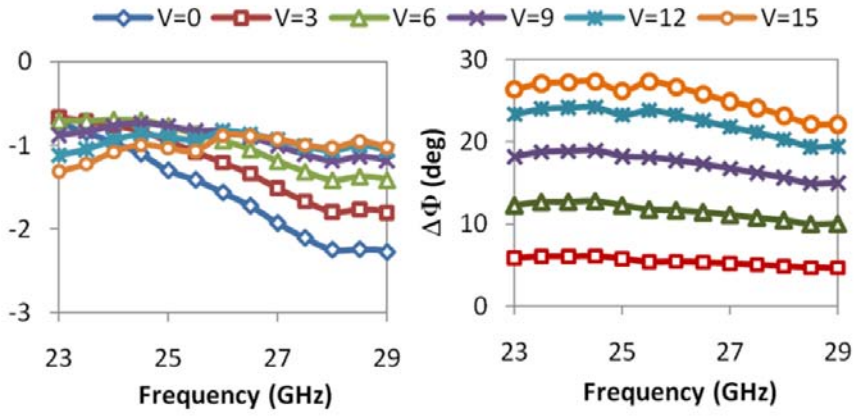


Figure 5.12 Measured insertion loss and $\Delta\Phi$ of the inline SIW phase shifter.

An SIW inline phase shifter is designed and fabricated with a pair of transitions from SIW

to grounded coplanar waveguide (GCPW) as shown in Figure 5.11. Measured phase shift $\Delta\Phi$ changing with the control voltage of varactor diode is correlated with the simulations of HFSS. The control voltage of varactor is adjusted from 0 V to 15 V in our experiment, while the capacitance of varactor in our simulation changes from 1.8 pF to 0.09 pF. In the simulation, the varactor is modeled as a rectangle placed on the slot and assigned a lumped LRC boundary condition. Measured frequency performance of the insertion loss and phase shift is shown in Figure 5.12. The phase shift is $24.8° \pm 2.2°$ and the insertion loss is 1.09 ± 0.17 dB in a 30% bandwidth.

5.5 Varactor-tuned reflection-type phase shifter

A typical reflection-type phase shifter is composed of a 3 dB coupler and two short terminations which are controlled by tuning elements. The performances of the phase shifter, including maximum tuning range of phase shift and variation of insertion loss and phase shift, are all related to the performance of the termination. In this section, we first study some designs of short terminations which are controlled by single or dual varactor diodes. Based on the optimized design of a dual-varactor tuned short termination, two SIW reflection-type phase shifters are fabricated and tested.

5.5.1 Single-varactor tuned SIW termination

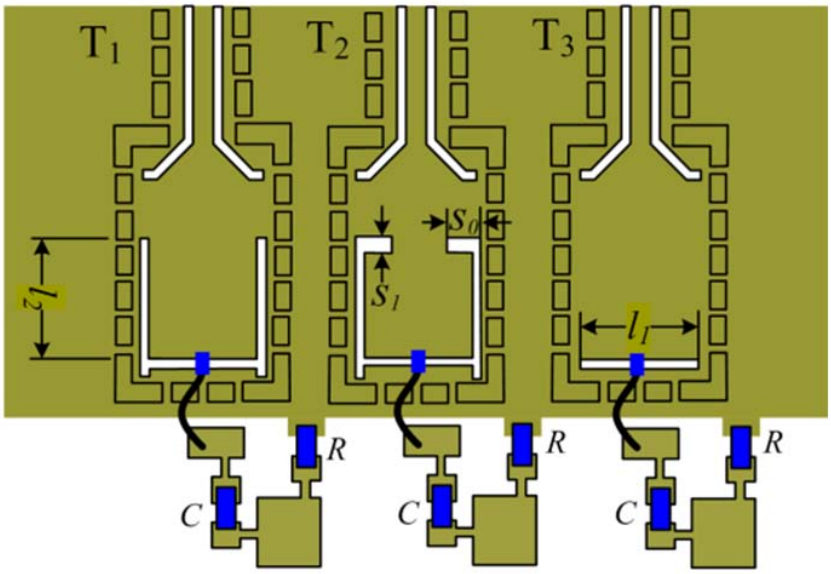


Figure 5.13 Three single-varactor controlled short terminations to SIW, $l_1 = 4.67$ mm, $l_2 = 4.47$ mm, $S_1 = 0.25$ mm and $S_0 = 1.15$ mm.

In order to find an optimum design of short termination whose reflection coefficient has both a large phase shift and a flat frequency performance, three different short terminations (T_1, T_2 and T_3) are fabricated and tested (Figure 5.13). Different from the SIW is directly shorted in T_3, the SIWs in T_1 and T_2 are both transformed to parallel plate-type transmission lines and then shorted with synthesized metal walls. Length l_1 of the slot under the varactor is 4.6 mm, the same value as used in the previous inline phase shifter. Phase shift $\Delta\Phi$ of reflection coefficient Γ is defined as $|\angle\Gamma(C_{vmin}) - \angle\Gamma(C_{vmax})|$.

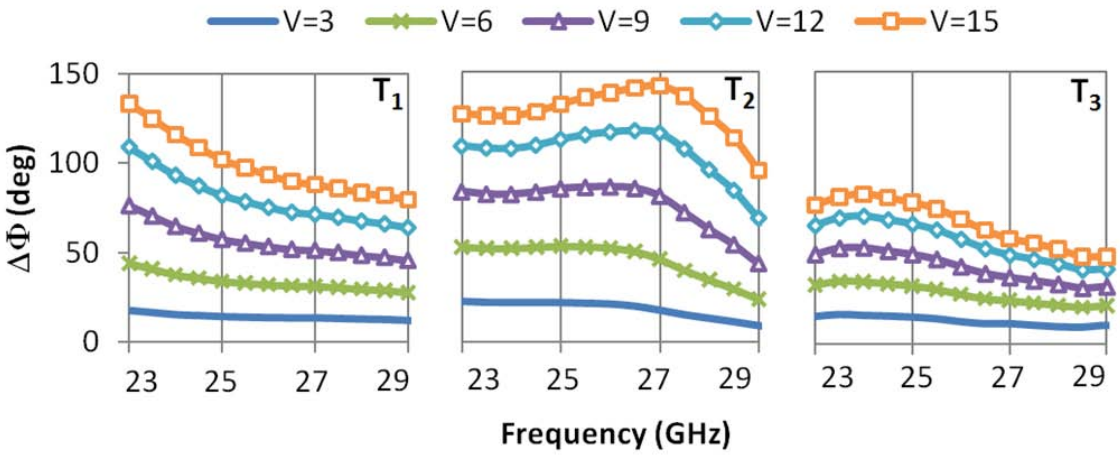


Figure 5.14 Measured phase shift of reflection coefficient changing with control voltage of the varactor.

Measured phase shifts $\Delta\Phi$ of the three terminations are compared in Figure 5.14. T_3 has the smallest average phase shift of 65° within the band compared to 100° of T_1 and 120° of T_2. In T_2, a pair of transversal slots are used at the start of line transformation for improving the flatness and the tuning range of phase shift in the band. The variation of phase shift within a frequency band can be measured by the standard deviation (SD) which is defined by

$$\mathrm{SD} = \sqrt{\frac{\sum(\Delta\Phi - \bar{\Phi})^2}{n-1}} \tag{5.4}$$

where n is the number of frequency samples and $\bar{\Phi}$ is the average phase shift within the band. As shown in Figure 5.15, both T_2 and T_3 have a phase shift variation less than 15° in the band $23 \sim 29$ GHz, while T_2 has the minimum standard deviation, less than 5° when the interested frequency band is limited in a smaller range $25 \sim 27$ GHz. Since termination T_2 has the largest tuning range and the flattest frequency performance of phase shift, it is selected in the following design of dual-varactor controlled phase shifter which is aimed to

have a phase shift of 180° within the interested band.

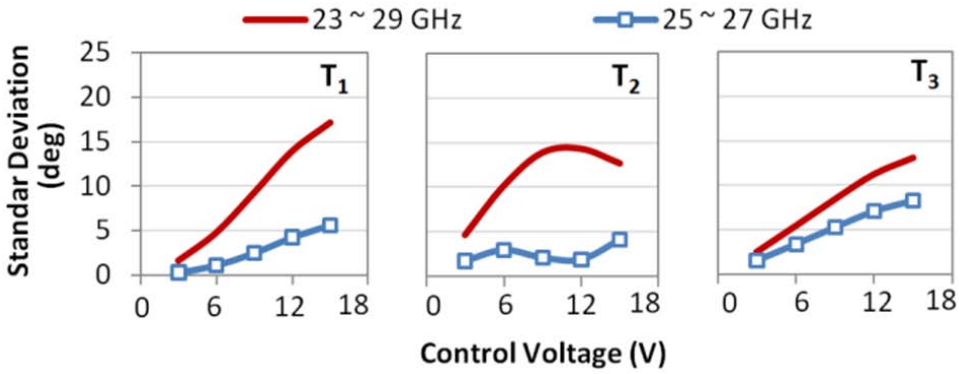


Figure 5.15 Standard deviation of measured phase shift of reflection coefficient.

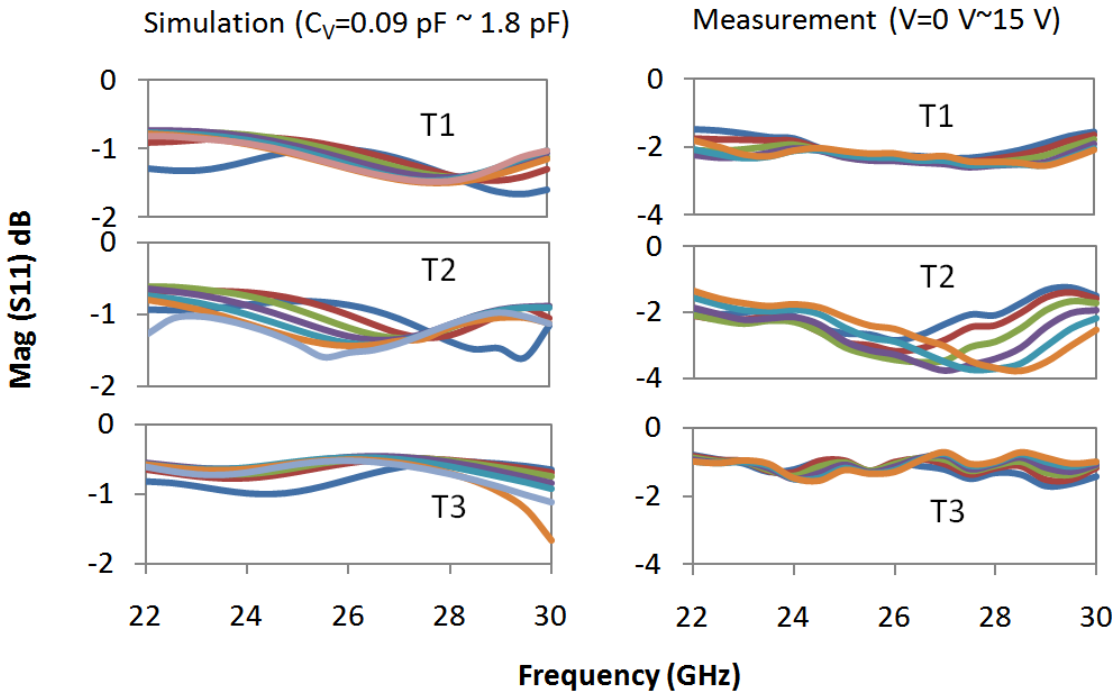


Figure 5.16 Simulated and measured magnitude of reflection coefficient.

A good correlation between the simulated and measured magnitudes of the three terminations in Figure 5.16 shows that the simulation tool can provide a reliable and accurate estimation in the design. Although, compared with T_1 and T_3, T_2 has a relatively large fluctuation within the interested frequency band, it is still within our tolerable range.

5.5.2 Dual-varactor tuned SIW termination

Because of the parasitic effect, the minimum capacitance of the varactor diode used in this work is about 0.09 pF. This limits the tuning range of the phase shift of all terminations in Figure 5.13 less than 180°. A commonly used technique for extending the tuning range of a reflection termination is to connect two varactors in series with certain distance, normally the quarter wavelength. The tuning range of the phase shift can be doubled in the best scenario.

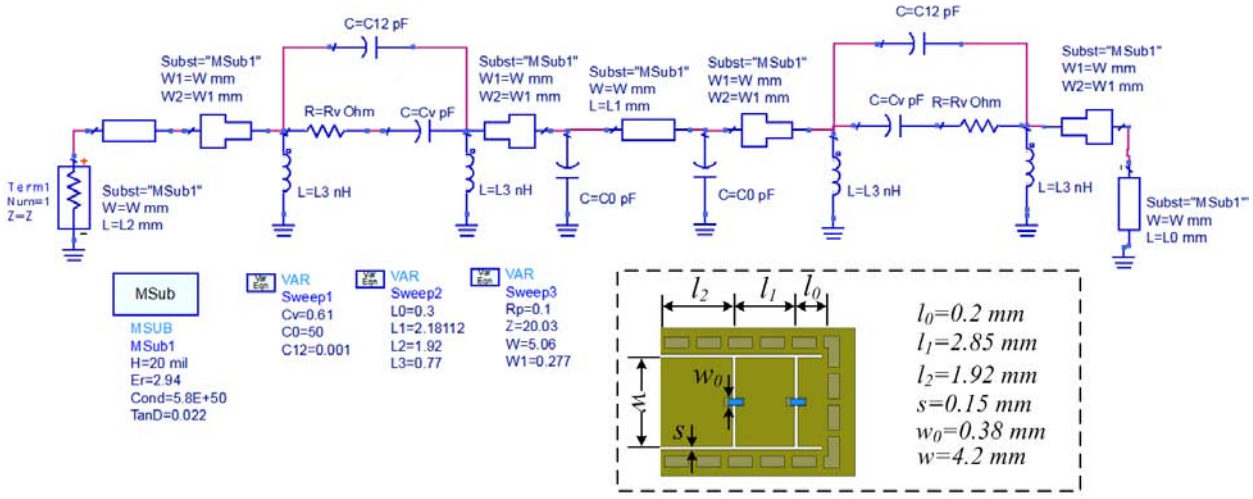


Figure 5.17 Equivalent circuit of a short termination with two varactors.

The layout of a dual-varactor tuned short termination without matching slots is shown in Figure 5.17. Since the dominant mode is quasi-TEM mode, this termination can be modeled by an equivalent circuit model as shown in Figure 5.17. The transmission lines are modeled by microstrip lines TL_0, TL_1 and TL_2 whose widths are a little larger than the physical dimension w because of the fringe effect. Microstrip steps are used between the microstrip lines and transversal slots so that the current discontinuity in the area where varactors are assembled can be taken into consideration. The slots under the varactors are modeled as π-networks, consisting of L_3 and C_{12} in Figure 5.17. The separated block between two slots has a large capacitance to the ground which is denoted as C_0.

Except capacitor C_v, resistor R_v is connected in series in order to model the loss caused by the varactor. The impedance of the termination at the input of the circuit is the characteristic impedance of the SIW which value is 20 Ohm, so that the equivalent circuit simulation results can be compared to a full wave simulation where the input is defined as a “wave port”. The distance between two varactors l_1 is around a quarter wavelength of the dominant mode.

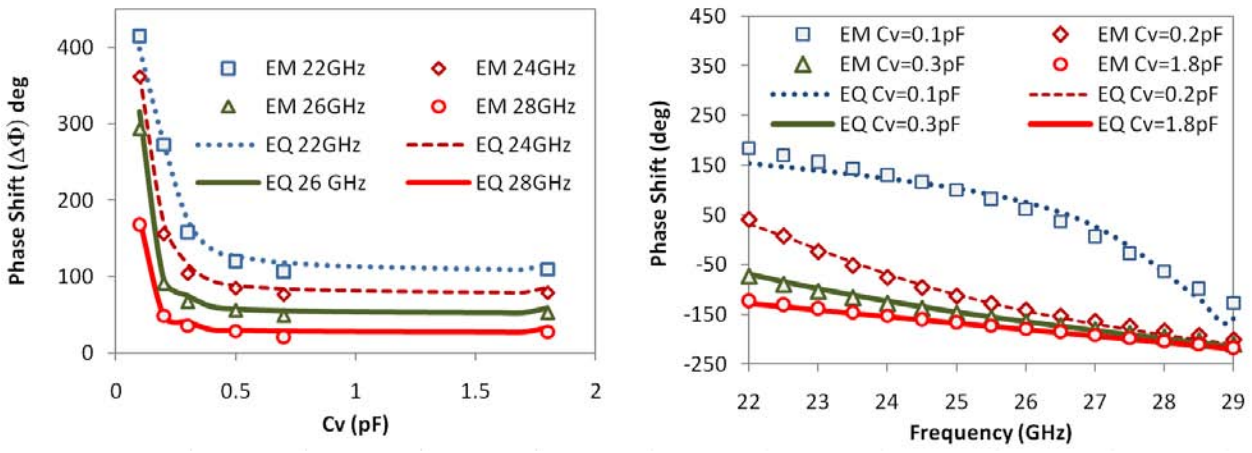


Figure 5.18 Comparison of EM simulation and equivalent circuit model simulation of a short termination with two varactors.

When the control voltages of the two varactors are adjusted from 0 V to 15 V simultaneously, the frequency performance of phase shift of the reflection coefficient is calculated using the equivalent circuit and correlated with the simulation results of HFSS in Figure 5.18. The phase of reflection coefficient changing with the capacitance C_v of the varactor is also compared. The results in Figure 5.18 show that the equivalent circuit can be used to estimate the response of the proposed dual varactor-tuned SIW short termination.

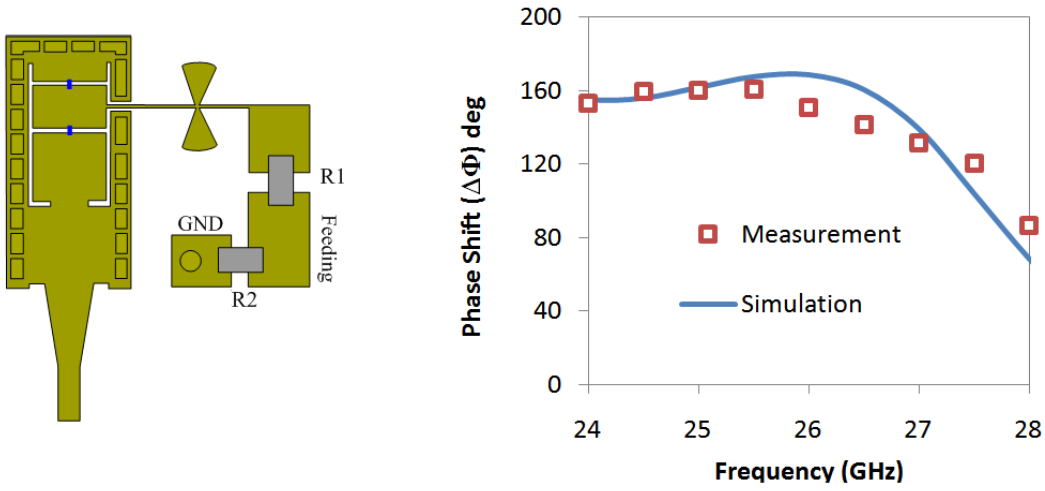


Figure 5.19 Layout, simulation and measured maximum phase shift of a dual varactor-tuned SIW short termination.

An optimized design of the proposed dual-varactor tuned short termination with a microstrip-to-SIW transition is fabricated and tested. In the layout shown in Figure 5.19, two resistors

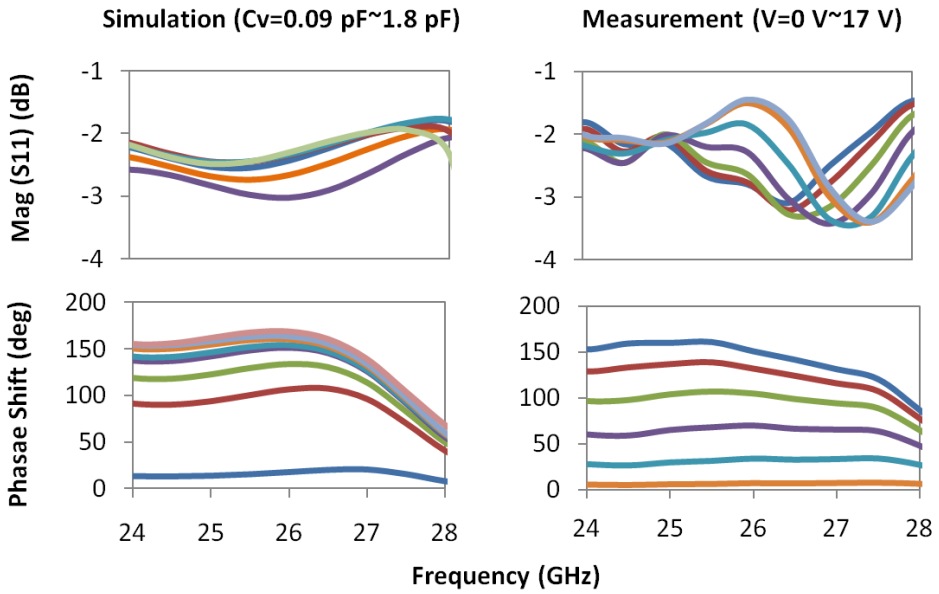


Figure 5.20 Simulation and measured results of a dual varactor-tuned SIW short termination changing with the control voltage.

$R_1 = 10$ MOhm and $R_2 = 1$ KOhm are both used for protecting the varactor. Measured and simulated maximum tuning ranges of the phase of reflection are also given in Figure 5.19. Within our interested frequency band of 25 GHz to 27 GHz, the maximum phase shift is below 180°. The measured S-parameters are compared with the simulation in Figure 5.20.

5.5.3 Varactor tuned reflection type SIW phase shifter

A 3 dB H-plane SIW coupler is designed with Rogers R6002 substrate, and the substrate thickness is 20 mil, which dimensions are shown in Figure 5.21(a). By using two stages at the bifurcation part, the -10 dB bandwidth of the coupler covers the entire frequency band and reflection is less than -20 dB when the frequency is higher than 24 GHz. In the simulated results shown in Figure 5.22, the signal magnitude at transmitted and coupled ports is -3.3 ± 0.6 dB and the phase difference at ports 3 and 4 is $90° \pm 5°$ from 23.6 GHz to 30 GHz. The design of the SIW short termination is also refined base on the design shown in the previous section. The distance from the short plane at the end of the SIW to the first slot and the distance between two slots are both important variables for obtaining the maximum tuning range. The dimensions of the final design of the termination are given in Figure 5.21(b).

A reflection-type phase shifter is then designed by loading two ports of the coupler with optimized short terminations obtained in the previous section. The other two ports of the

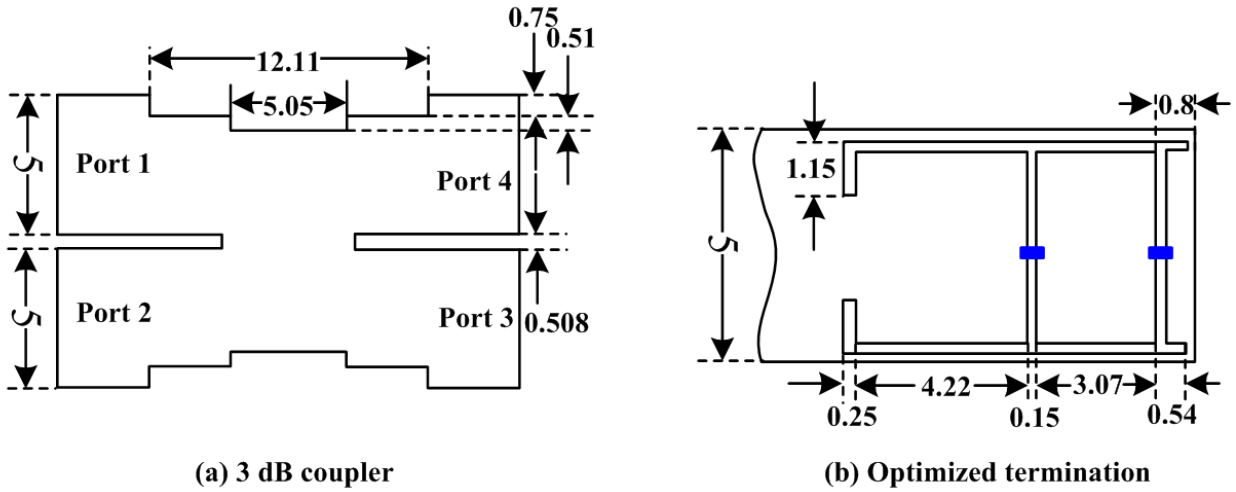


Figure 5.21 Layout dimension of final phase shifter design.

coupler are connected with SIW-to-GCPW transitions for testing purpose. The layout of the proposed phase shifter with a biasing circuit for adding control voltages to varactors is shown in Figure 5.23(a). The control voltage of the varactors is added onto the separated rectangles through two fine lines. After a TRL calibration with a set of GCPW calibration kits, the reference planes of the measurement are still on GCPW and 5 mm away from the edge of the circuit. The correlation of phase shift between simulation and measurement is larger than 180° for all frequency points lower than 27 GHz, as shown in Figure 5.23(b). In Figure 5.24, the simulations are compared with the full measurement results, including return loss, insertion loss and phase shift. The curves in the figures of simulations represent results obtained with discrete values of capacitance C_v ranging from 0.09 pF to 1.8 pF. The curves in the figures of measurements correspond to the results when the control voltage is adjusted from 0 V to 16 V with a spacing of 2 V. The maximum variation of the measured insertion loss is -3.8 ± 0.87 dB and the return loss is lower than -10 dB within a 15.3% bandwidth (from 24 GHz to 28 GHz).

Another 360° phase shifter is designed by cascading two 1800° phase shifters together, as shown in Figure 5.25(a). In order to feed the varactors, four separated pads of the terminations are all connected together and with a biasing pad beside the phase shifter with bonding wires. The S-parameter of the phase shifter is measured from 0 V to 15 V with a step of 1 V. All the measured S-parameter files are merged into an MDIF file for an ADS S-parameter simulation with interpolation function. A parametric simulation with the tuning voltage changing from 0 V to 15 V with a step of 0.5 V is conducted in ADS with an S-parameter interpolation. All S-parameters, including the real measured data and those obtained with interpolation,

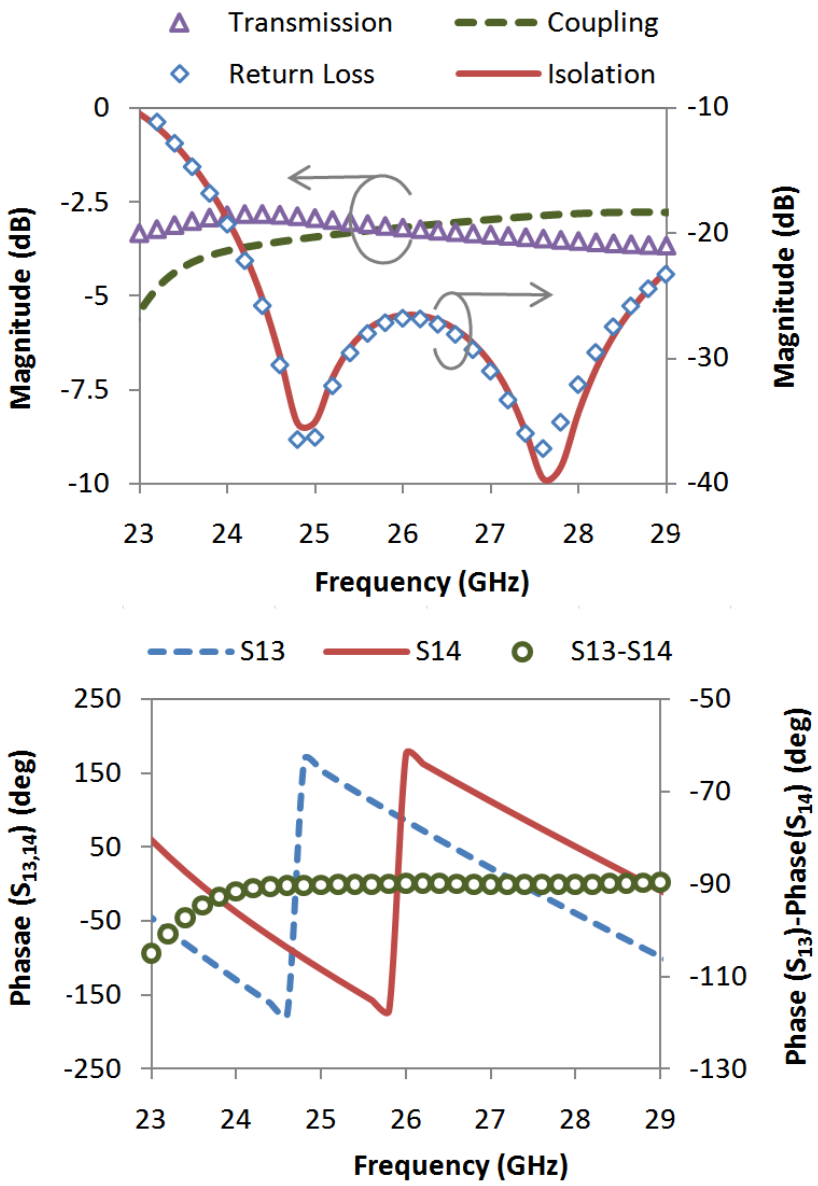


Figure 5.22 HFSS simulation of a 3 dB H-plane SIW coupler.

are plotted in Figure 5.25(b). The correctness of this simulation provides a solution to an envelope simulation with the real experiment data of the proposed phase shifter.

The measured frequency response of the phase shift is plotted at control voltages 3 V, 6 V, 9 V, 12 V, 15 V, as shown in Figure 5.26(a). The tuning range is larger than 360° from 23.5 GHz to 26.5 GHz. The phase and magnitude at 26 GHz changing with the control voltage are also given in Figure 5.26(b). It is found that the changing of the phase shift is quite linear and the variance of the magnitude is less than ±0.5 dB within the tuning range.

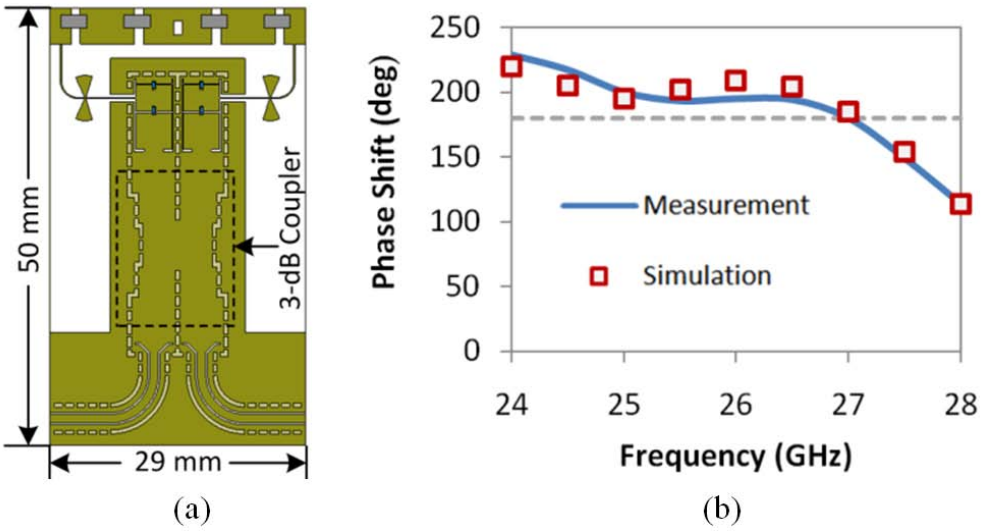


Figure 5.23 (a) Layout and (b) simulation and measurement correlation of the 180° reflection-type SIW phase shifter.

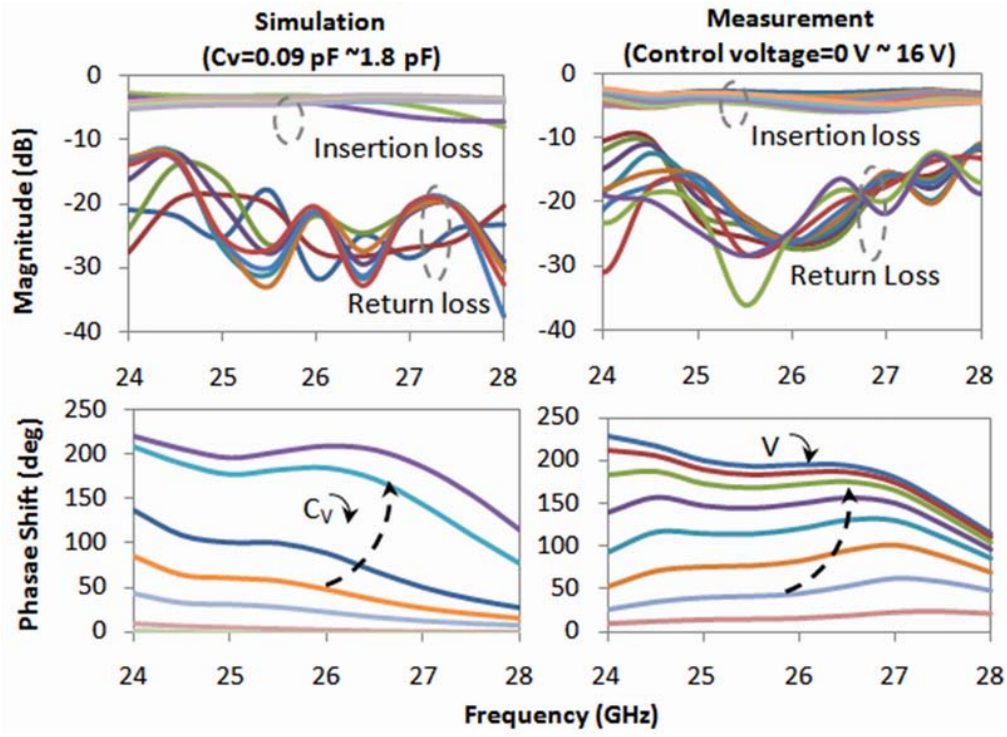


Figure 5.24 Simulated and measured S-parameters of the 180° reflection-type SIW phase shifter changing with control voltage.

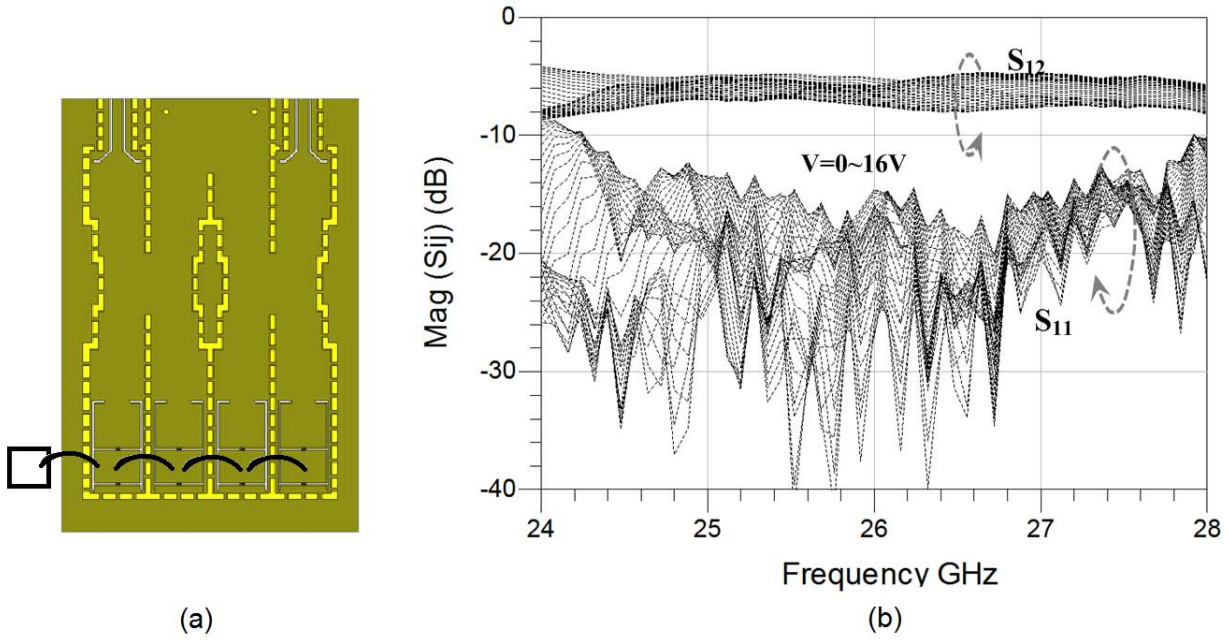


Figure 5.25 (a) Layout. (b) Measured S-parameter of the 360° reflection-type SIW phase shifter.

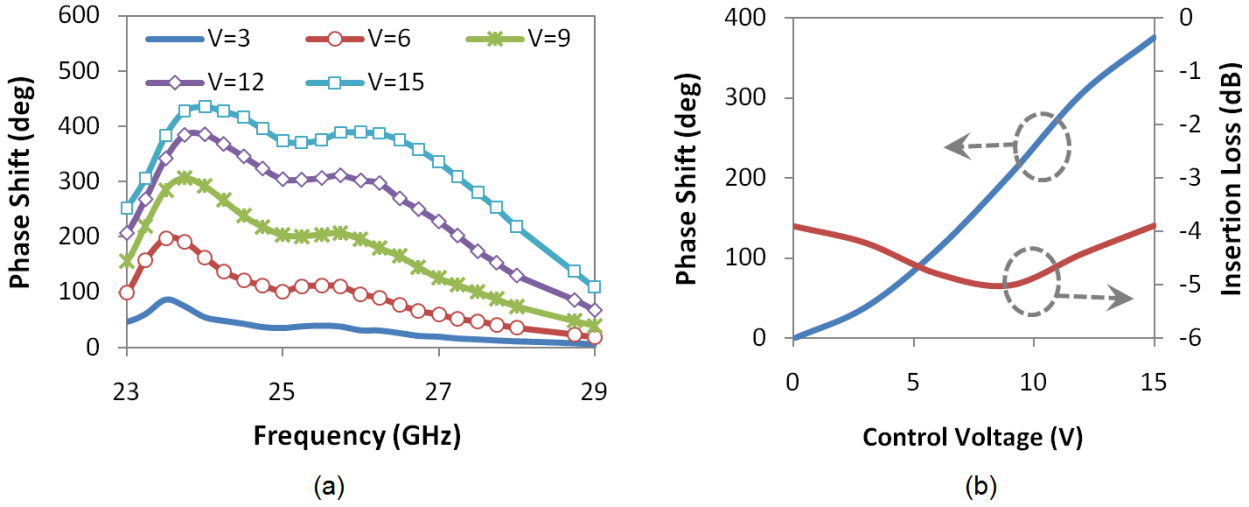


Figure 5.26 (a) Frequency-dependent performance of phase shift changing with control voltage. (b) Phase shift and insertion loss changing with control voltage at 26 GHz.

5.6 QPSK modulator

The 360° phase shifter designed in the previous section can be used as a phase modulator when the reflection coefficient Γ is changing with a voltage which is controlled by the I/Q

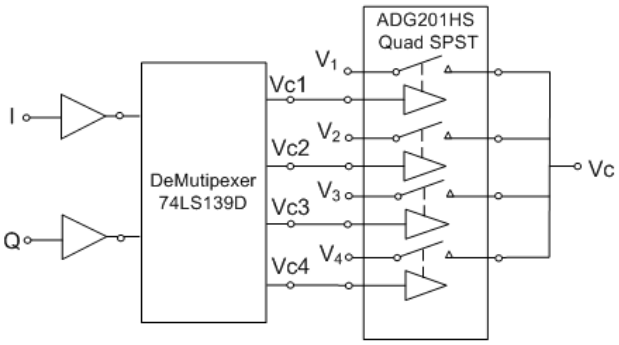


Figure 5.27 Block diagram of encoder.

signal.

The control signal of the modulator can be generated by an encoder shown in Figure 5.27. The baseband I/Q signal input into a demultiplexer whose logic table is listed in Table 5.1.

I	Q	V_{c1}	V_{c2}	V_{c3}	V_{c4}
0	0	H	H	H	L
1	0	H	H	L	H
0	1	H	L	H	H
1	1	L	H	H	H

Tableau 5.1 Logic table of the I/Q signal input.

The outputs of the de-multiplexer, V_{c1}, V_{c2}, V_{c3} and V_{c4}, are control signals of a following quad single pole single throw (SPST) switch array. For each I/Q input, only one output of the de-multiplexer is of low level and able to trigger one of the four switches. The inputs of the switch array are four different voltage levels, V_1, V_2, V_3 and V_4, and the output V_c equals to one input when the corresponding switch is turned on by the I/Q signal. The output V_c is used to control the 360° phase shifter designed in the previous section, the phase shift of the phase shifter will be 0°, 90°, 180° and 270° when V_c equals to V_1, V_2, V_3 and V_4, respectively.

An ADS simulation of the encoder circuit is shown in Figure 5.28. The input I/Q signals of are compared with the output control voltage V_c in Figure 5.29(a). V_1, V_2, V_3 and V_4 equal to 0 V, 5.7 V, 8.8 V and 11.6 V, respectively, and these values are determined by checking the phase shift curve shown in Figure 5.26. The symbol rate of the input I/Q signal is 1 Mbit/s which is the same as the output V_c, as shown in Figure 5.29(b).

The measured waveform and spectrum of the output of the encoder are given in Figure 5.30. In the experiment, limited by the measurement range of the oscilloscope, the levels of $V_1 \sim V_4$ are set as 1 V, 2 V, 3 V and 4 V, respectively.

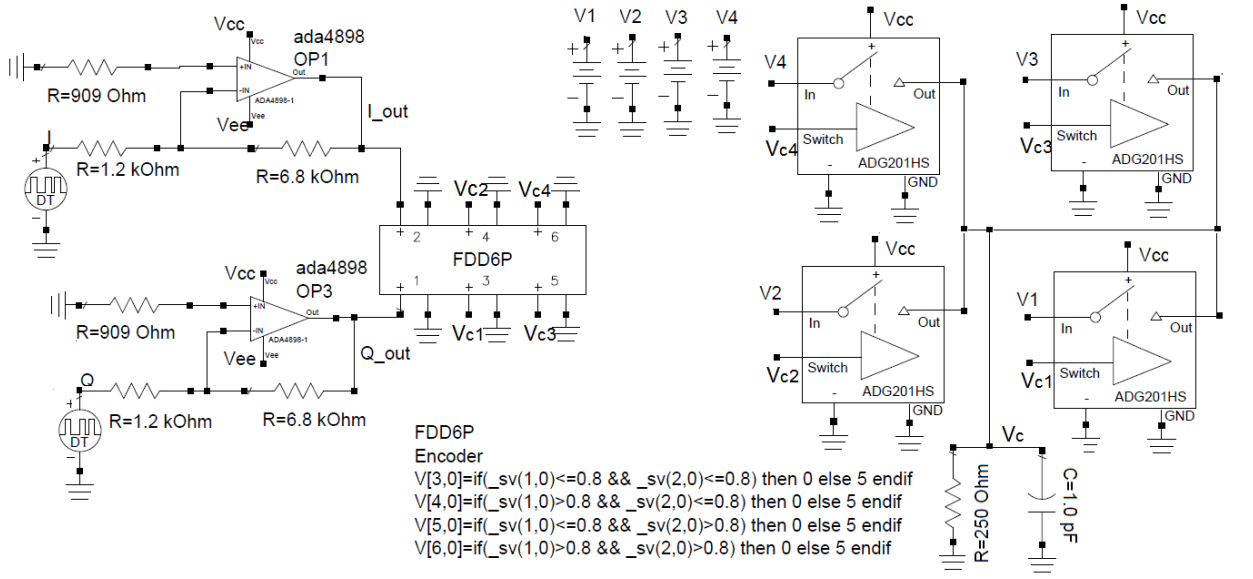


Figure 5.28 ADS simulation of encoder.

When two adjacent ports are loaded with terminations $\Gamma = \gamma e^{j\phi_1}$, the S-parameter of a 3 dB coupler becomes as follows

$$\begin{bmatrix} b_1 \\ b_7 \end{bmatrix} = \begin{bmatrix} 0 & -j\Gamma \\ -j\Gamma & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_7 \end{bmatrix} \tag{5.5}$$

where Γ is the reflection coefficient of the termination. If two such couplers are cascaded with each other, the S-parameter of the 360° phase shifter is then changed into

$$[S] = \begin{bmatrix} 0 & -\Gamma^2 \\ -\Gamma^2 & 0 \end{bmatrix} \tag{5.6}$$

As shown in Figure 5.31, the incoming wave of the modulator is generated by signal generator $a_1 = Ae^{j\phi_0}$, where A is the amplitude and ϕ_0 is the phase of the local oscillator (LO) signal, then the output at port P_2 is $b_2 = -A\Gamma^2 e^{j\phi_0} = -A\gamma^2 e^{j(\phi_0+2\phi_1)}$. Carrier leakage means that the local oscillator signal leaks to the RF output through transmitter. It can cause the degradation in the signal constellation and undesired RF loss at the local oscillator frequency. The carrier leakage might be caused by the finite isolation between the input and isolated ports of the coupler. The coupler used in our design has an isolation as high as 20 dB within the frequency we are interested, as shown in Figure 5.22, therefore the LO leakage caused by the isolation of the coupler can be ignored. Another source for carrier leakage of reflection type modulator is unideal terminations loaded to the coupler. Ideally, the values

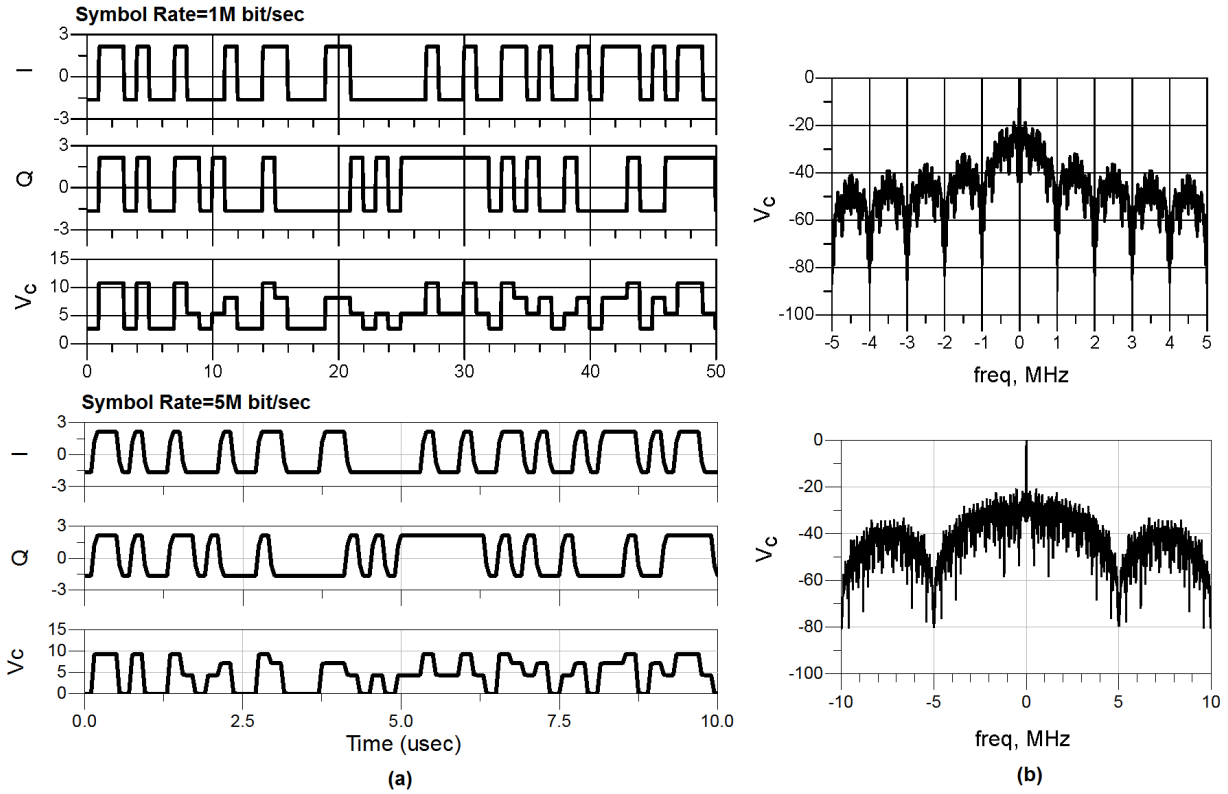


Figure 5.29 Simulated waveform of encoder.

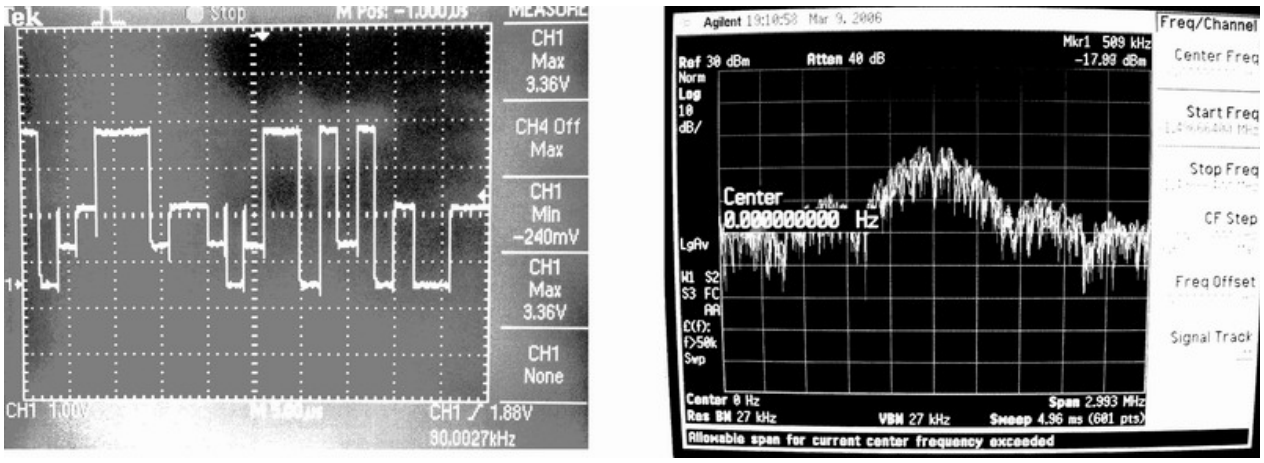


Figure 5.30 Measured waveform and spectrum of encoder output.

of Γ of the fours states in a QPSK modulator should be located in the four quadrants and symmetric to the original point. However, because of the magnitude and phase error of the

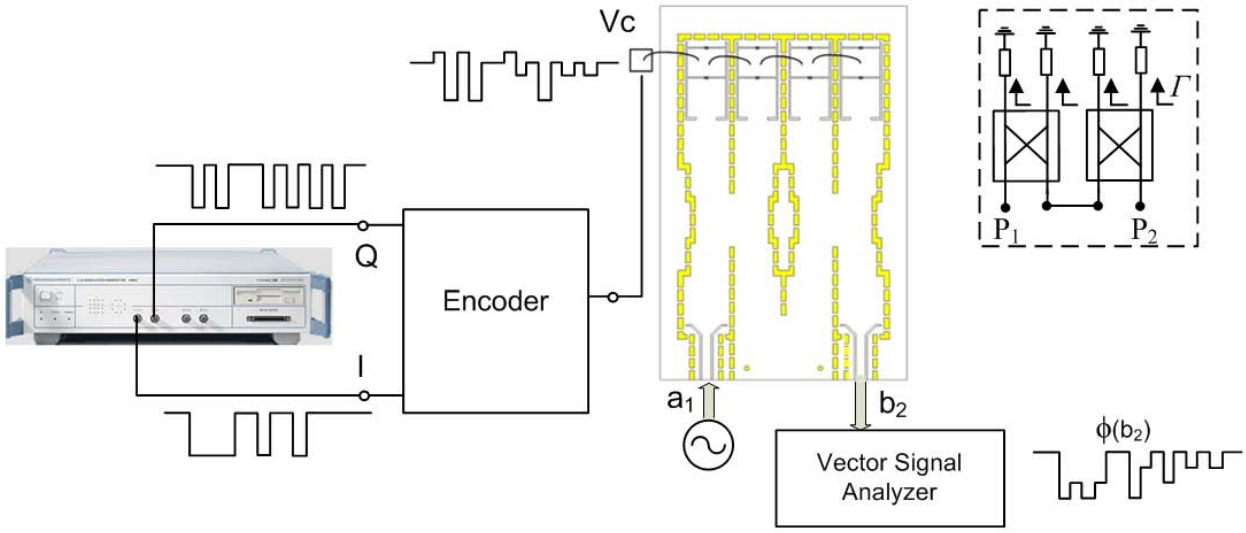


Figure 5.31 Experimental setup of 360° phase shifter modulator.

360° phase shifter modulator, the center of the four points will have an offset to the original point.

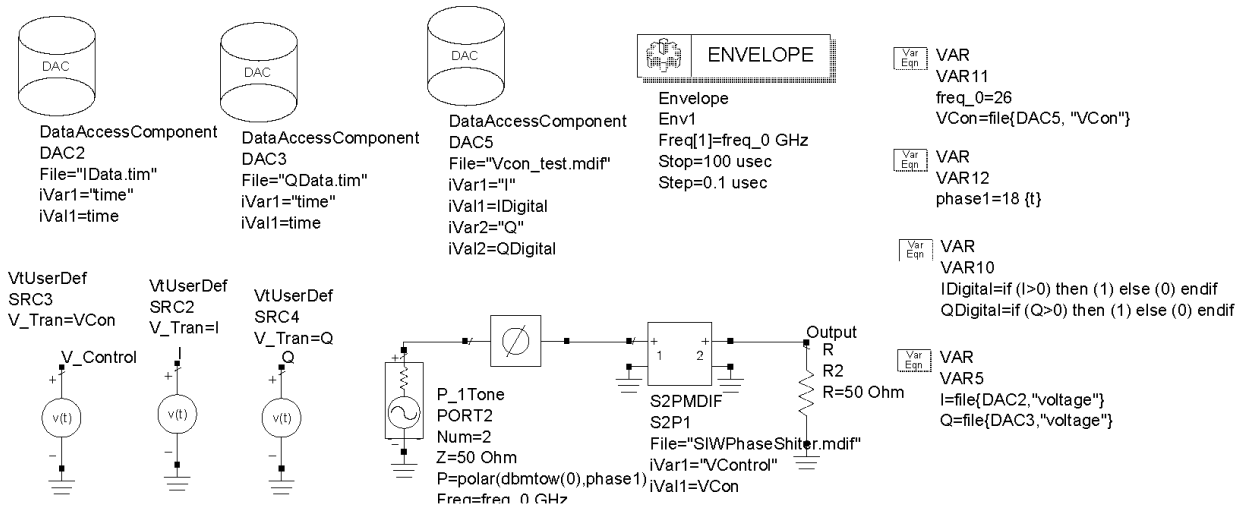


Figure 5.32 Envelop simulation of 360° phase shifter modulator.

It is difficult to have an analytical expression of the reflection coefficient Γ of an SIW short termination loaded with two varactors, as shown in Figure 5.17. An ADS simulation of the 360° phase shifter modulator is shown in Figure 5.32. The 360° phase shifter modulator is

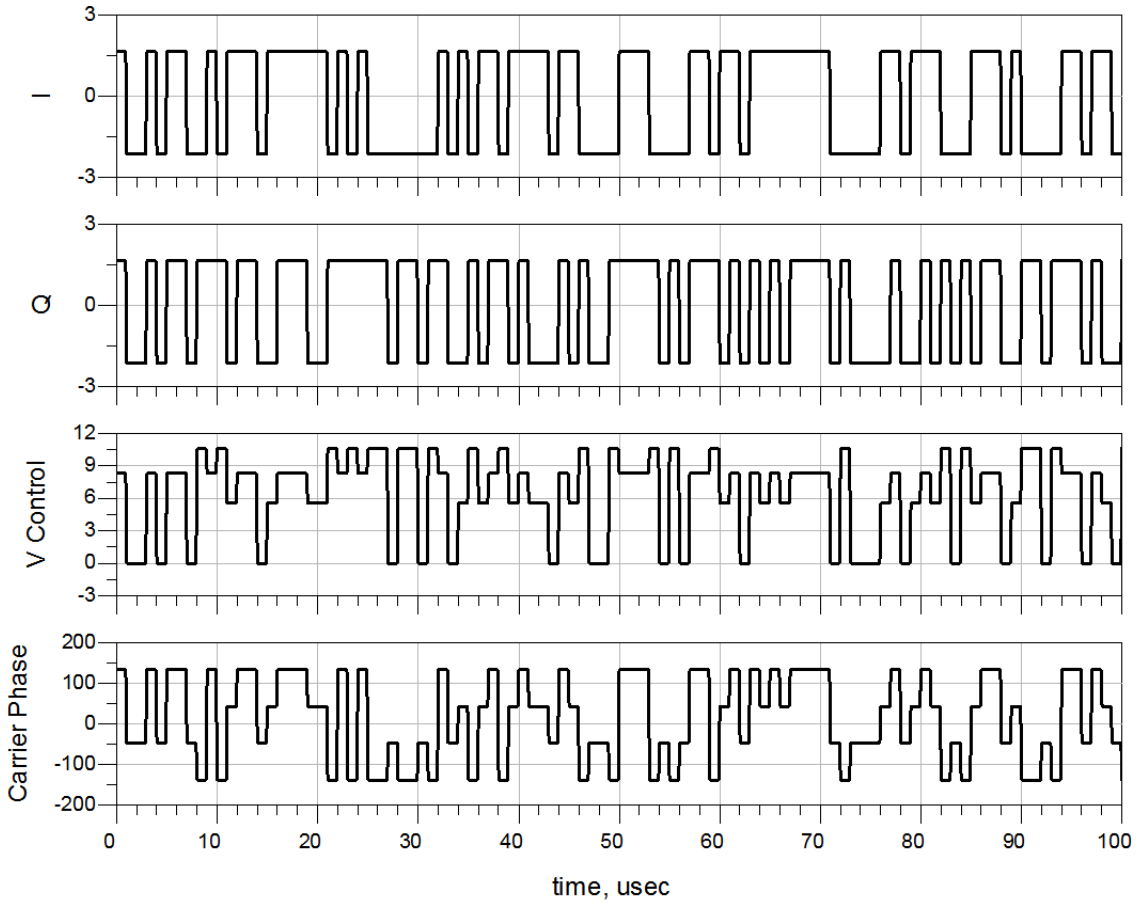


Figure 5.33 Simulated waveforms and phase of modulated signal.

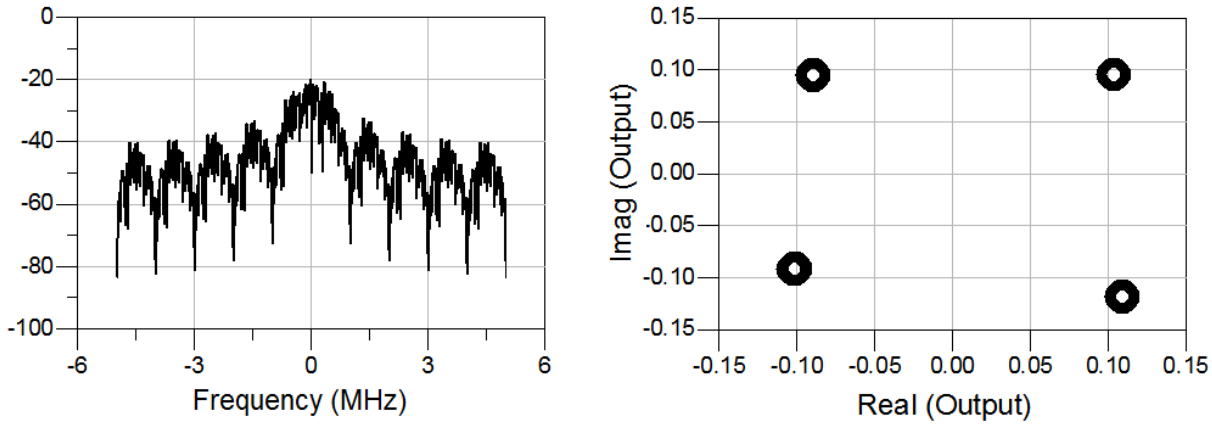


Figure 5.34 Simulated spectrum and constellation of 360° phase shifter modulator.

modeled by a set of S-parameters measured at 1 V, 2 V, ..., 15 V. Therefore, the impact of the error of phase and magnitude of the non-ideal terminations is considered in the simulation. The time domain I/Q signal and control signal are generated from the simulation shown in Figure 5.28 and their waveforms are compared with the phase of the modulated signal in Figure 5.33. The simulated spectrum and constellation are shown in Figure 5.34.

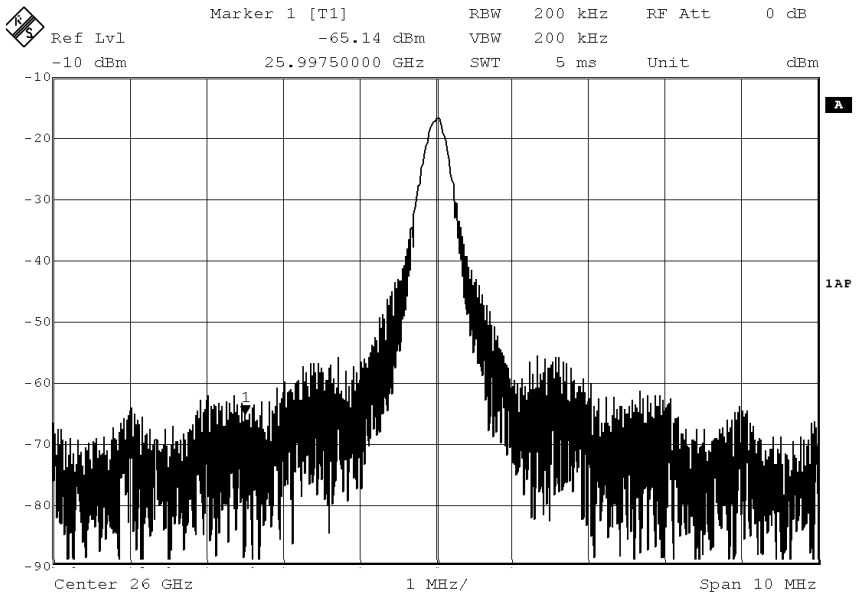


Figure 5.35 Measured spectrum of 360° phase shifter modulator.

An experiment, as shown in Figure 5.31, is conducted for testing the spectrum (Figure 5.35), constellation (Figure 5.36) and EVM (Figure 5.37) of the modulated signal of the 360° phase shifter modulator. The data rate used in the experiment is 500 Kb/s. The signal analyzer is R&S FSQ40 whose minimum sweep speed is 5 ms. The peak in the spectrum actually is the carrier leakage at the LO frequency, which is 26 GHz in the experiment. The overall EVM of the modulator is 15.25%. The root-mean-squared (RMS) magnetite error is 1.8%, which is primarily caused by the magnitude variation of the reflection-type phase shifter. This variation is ±1.2 dB at the experiment frequency. The phase error is 9.09°, which might be caused by the fluctuation of the control voltage generated by the encoder. As shown in Figure 5.26, the phase shift changes with the control voltage, nonlinearly. When the control voltage increases, the phase shift changes even faster. The output of the encoder is supposed to stay constant in one signal state, however this constancy degenerates when the symbol rate increases or the input voltage levels of the switch array get very high. When the four voltage levels output from the encoder are 0 V, 5.5 V, 8.3 V and 10.5 V, the output of the encoder starts to have some fluctuation in each time slot. A ±0.2 V variance on control

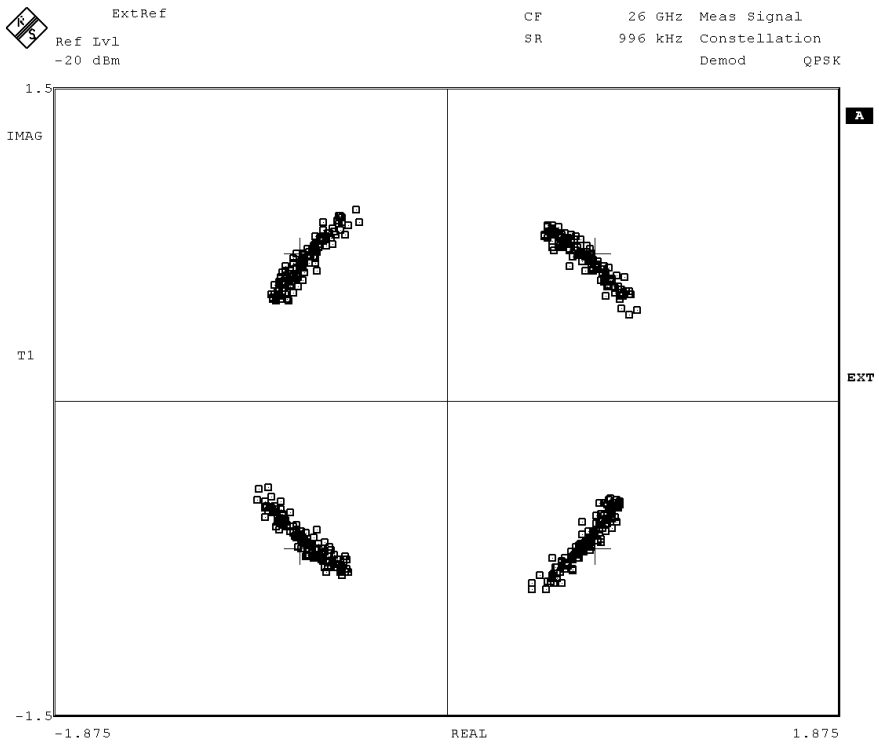


Figure 5.36 Measured constellation of 360° phase shifter modulator.

IFOVLD
Ref Lvl
-20 dBm
CF 26 GHz
SR 1 MHz Symbol/Errors
Demod QPSK

Error Summary			
Error Vector Mag	15.25 % rms	35.10 %	Pk at sym 473
Magnitude Error	1.88 % rms	5.50 %	Pk at sym 769
Phase Error	9.09 deg rms	-20.62 deg	Pk at sym 473
Freq Error	-118.33 kHz	-118.33 kHz	Pk
Amplitude Droop	0.53 dB/sym	Rho Factor	0.9749
IQ Offset	0.03 %	IQ Imbalance	1.07 %

Figure 5.37 Measured EVM of 360° phase shifter modulator.

voltage can cause ±10° on the phase shift.

5.7 Conclusion

To conclude this chapter, we study the features of some electronically tuned SIW phase shifters from different perspectives, such as control component, tuning range and shifter

architecture. Both PIN diode and varactor diode are used as control components for digital tuning and continuous tuning, respectively. From the architecture point of view, the reflection-type phase shifter has a much larger tuning range than the inline-type one. A design with two control components connected in series can further broaden the tuning range. The tuning range and the frequency performance of the phase shift can be varied with different designs of termination. A 180° tuning range is finally achieved with a reflection-type architecture and four varactor diodes. Two such phase shifters are cascaded together to achieve a 360° tuning range in a 12% bandwidth. A phase modulator is implemented with such a 360° phase shifter whose control voltage is adjusted by an external encoder circuit. The performance of the proposed phase modulator is then simulated in ADS and correlated to the measurements.

CHAPITRE 6

SIW Six-Port Receiver

Six-port network (SPN) was first used for microwave measurement to obtain the complex reflection coefficient of a device under test. Since 1990s, SPNs have been investigated as an alternative of standard frequency modulation continuous wave (FMCW) radar sensor and direct conversion receiver for demodulating signal in different formats, such as binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), and quadrature amplitude modulation (QAM) schemes. In the past ten years, SPNs were implemented in various applications using different fabrication technologies and design approaches, such as RF front-end for QPSK demodulator in Ka-band by using miniaturized hybrid microwave integrated circuit (MHMIC), frond-end module for W-band collision avoidance radar by using machined WR-10 waveguide, Ka-band software defined radio (SDR) receiver by using SIW structure, a transceiver for Ultra-wideband (UWB) radio system (Tatu *et al.* (2001, 2002); Moldovan *et al.* (2004); Chang *et al.* (2006); Zhao *et al.* (2006); Xu *et al.* (2006); Lim *et al.* (2007); Wang *et al.* (2007)).

In those previous studies, SPNs have been demonstrated to be an excellent candidate of modulator and demodulator for both communication and radar systems. In a six-port direct conversion receiver (Tatu *et al.* (2001, 2002, 2005); Moldovan *et al.* (2004); Xu *et al.* (2006)), the in-phase (I) and quadrature (Q) signal can be directly separated in the RF portion without any intermediate frequencies (IF) conversion and amplification which are usually required in the heterodyne receiver. Similarly, a system comprising a six-port network, a switch matrix and some open and short terminations can be used as a single-carrier QPSK modulator instead of two IF mixers, I/Q carriers, and RF up-conversion section in a conventional modulator of the heterodyne architecture. Combined with the base-band signal processing functions, the transceiver system based on the SPN technique has more flexibility to process signals of different modulation formats. The system, especially the RF portion, is simplified, which has a great significance when the operating frequency goes into mmW and beyond. The power consumption and the overall cost of the system will be significantly reduced. Because there are fewer linear components in the system, the dimension of circuits is scalable which can alleviate the overhead of system design. Without any serious problems from the linearity caused by active components, the six-port transceiver systems proposed in this chapter will have more predominance on bandwidth, error tolerance and power capacity.

A series of six-port radio architectures were proposed for the development of low-cost and

high-efficient direct-conversion software-defined transceivers, which are now becoming more favorable in the community than their mixer-based counterparts, because of their attractive performances on power consumption, linearity and system noise as well as design and manufacturing costs (Moldovan *et al.* (2004); Xu *et al.* (2005); Tatu *et al.* (2002); Wang *et al.* (2007)). A six-port junction circuit is a passive interferometer device which mainly consists of several couplers and power dividers. Six-port junctions based on various design techniques, such as microstrip line, stripline, metallic waveguide and SIW, have been studied over the past ten years.

A general waveguide type T-junction does not have a high isolation between two splitting arms as a Wilkinson power divider does. Generally, it is not a serious problem in a through-type design such as six-port junction in the design of a direct conversion receiver because it is assumed that only few outgoing waves at each port are able to be reflected back into the six-port junction. A successful example for using T-junctions as power dividers to construct a six-port junction was given in (Xu *et al.* (2005)). From the functionality point of view, all these three architectures can be used in a six-port receiver design.

6.1 Six-port Junction

6.1.1 S-parameter matrix of SIW six-port junction

Theory for using six-port network as a direct conversion receiver has been discussed in (Li *et al.* (1995, 1996); Hentschel (2005))s. As it has been concluded in (Xu (2007)), there are three types of architecture for building a six-port junction, namely,

A 3 couplers + 1 power splitter (Tatu *et al.* (2001)) ;

B 2 couplers + 2 power dividers + 90° phase shifter (Xu *et al.* (2005)) ;

C 4 couplers + 1 phase shifter (Moldovan *et al.* (2004)).

Six-port junctions of type A have been widely used in the microstrip line and stripline design. This architecture has two principal advantages compared with the other two techniques : 1) no phase shifter is used, which makes the structure simpler and 2) the wider bandwidth. In addition, a high-isolation between input and output can be provided by using a Wilkinson power divider that is convenient to be integrated based on the microstrip and stripline techniques.

The S parameter matrix of an ideal Wilkinson power divider is given in Equation 6.1. The S-parameters of type A and B six-port junctions which are composed of the Wilkinson power divider have already been derived in (Xu (2007)).

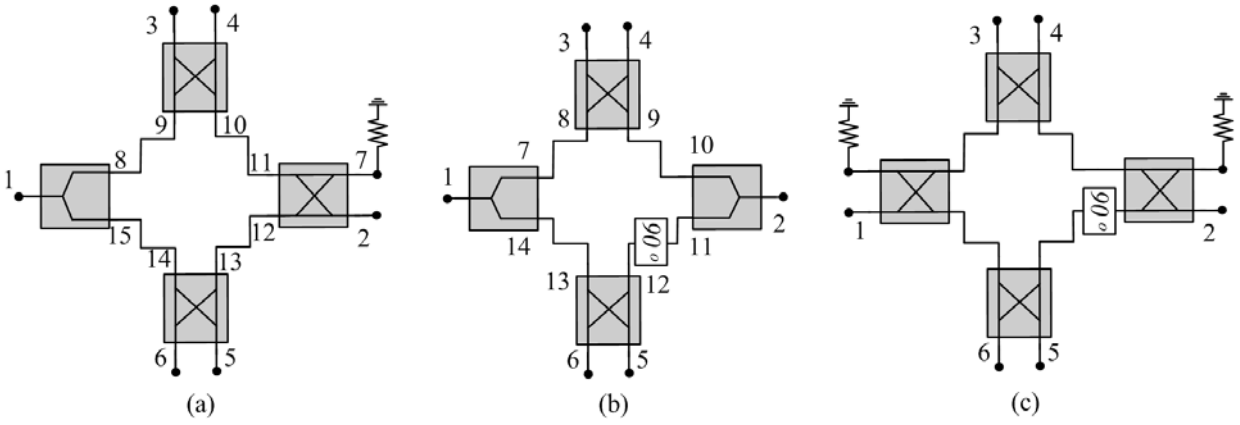


Figure 6.1 Block diagram of three six-port architectures.

$$[S_1] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \tag{6.1}$$

In a three-port waveguide junction, a lossless network, the return loss of two output ports and the isolation between them are not zero any more. In general, the S parameter matrix of a waveguide junction can be expressed as Equation 6.2.

$$[S] = \begin{bmatrix} 0 & \frac{-j}{\sqrt{2}} & \frac{-j}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} & -\frac{1}{2} & \frac{1}{2} \\ \frac{-j}{\sqrt{2}} & \frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{6.2}$$

To get the S parameter of a six-port junction, we number all ports of each part, including the inner connected ones, as shown in Figure 6.1. The incident wave and reflected wave at each port are defined as a_n and b_n, $n = 1, 2, \ldots 15$.

$$\begin{bmatrix} b_3 \\ b_9 \\ b_{10} \\ b_4 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \begin{bmatrix} a_3 \\ a_9 \\ a_{10} \\ a_4 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} a_{10} + ja_9 \\ a_4 + ja_3 \\ a_3 + ja_4 \\ a_9 + ja_{10} \end{bmatrix} \tag{6.3}$$

$$\begin{bmatrix} b_7 \\ b_{11} \\ b_{12} \\ b_2 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \begin{bmatrix} a_7 \\ a_{11} \\ a_{12} \\ a_2 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} a_{12} + ja_{11} \\ a_2 + ja_7 \\ a_7 + ja_2 \\ a_{11} + ja_{12} \end{bmatrix} \tag{6.4}$$

$$\begin{bmatrix} b_5 \\ b_{13} \\ b_{14} \\ b_6 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \begin{bmatrix} a_5 \\ a_{13} \\ a_{14} \\ a_6 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} a_{14} + ja_{13} \\ a_6 + ja_5 \\ a_5 + ja_6 \\ a_{13} + ja_{14} \end{bmatrix} \tag{6.5}$$

$$\begin{bmatrix} b_1 \\ b_8 \\ b_{15} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-j}{\sqrt{2}} & \frac{-j}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} & -\frac{1}{2} & \frac{1}{2} \\ \frac{-j}{\sqrt{2}} & \frac{1}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_8 \\ a_{15} \end{bmatrix} = \begin{bmatrix} -\frac{j}{\sqrt{2}}a_8 - \frac{j}{\sqrt{2}}a_{15} \\ -\frac{j}{\sqrt{2}}a_1 - \frac{1}{2}a_8 + \frac{1}{2}a_{15} \\ -\frac{j}{\sqrt{2}}a_1 + \frac{1}{2}a_8 - \frac{1}{2}a_{15} \end{bmatrix} \tag{6.6}$$

From Equation 6.3 to Equation 6.6, the reflected and incident waves at the inner ports ($n = 8, 9, \ldots 15$) can be expressed by those of the outer ports ($n = 1, 2, \ldots 7$).

$$\begin{aligned} b_8 = a_9 &= -j\tfrac{a_1}{\sqrt{2}} + j\tfrac{a_3}{2\sqrt{2}} + \tfrac{a_4}{2\sqrt{2}} - \tfrac{a_5}{2\sqrt{2}} - j\tfrac{a_6}{2\sqrt{2}} \\ b_9 = a_8 &= -\tfrac{a_4}{\sqrt{2}} - j\tfrac{a_3}{\sqrt{2}} \\ b_{10} = a_{11} &= -\tfrac{a_3}{\sqrt{2}} - j\tfrac{a_4}{\sqrt{2}} \\ b_{11} = a_{10} &= -\tfrac{a_2}{\sqrt{2}} - j\tfrac{a_7}{\sqrt{2}} \\ b_{12} = a_{13} &= -\tfrac{a_7}{\sqrt{2}} - j\tfrac{a_2}{\sqrt{2}} \\ b_{13} = a_{12} &= -\tfrac{a_6}{\sqrt{2}} - j\tfrac{a_5}{\sqrt{2}} \\ b_{14} = a_{15} &= -\tfrac{a_5}{\sqrt{2}} - j\tfrac{a_6}{\sqrt{2}} \\ b_{15} = a_{14} &= -j\tfrac{a_1}{\sqrt{2}} - j\tfrac{a_3}{2\sqrt{2}} - \tfrac{a_4}{2\sqrt{2}} + \tfrac{a_5}{2\sqrt{2}} + j\tfrac{a_6}{2\sqrt{2}} \end{aligned} \tag{6.7}$$

Therefore, the reflected waves at all outer ports can be expressed by the following matrix

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} -a_3 + ja_4 + ja_5 - a_6 \\ a_3 + ja_4 - a_5 + ja_6 \\ -a_1 + a_2 + a_3/2 - ja_4/2 + ja_5/2 - a_6/2 + ja_7 \\ ja_1 + ja_2 - ja_3/2 - a_4/2 + a_5/2 + ja_6/2 + a_7 \\ ja_1 - a_2 + ja_3/2 + a_4/2 - a_5/2 - ja_6/2 + ja_7 \\ -a_1 + ja_2 - a_3/2 + ja_4/2 - ja_5/2 + a_6/2 + a_7 \end{bmatrix} \tag{6.8}$$

Assuming port 7 is well matched, the S parameter of the six port junction in Figure 6.1(a) is then given as :

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 0 & 0 & -1 & j & j & -1 \\ 0 & 0 & 1 & j & -1 & j \\ -1 & 1 & \frac{1}{2} & -\frac{j}{2} & \frac{j}{2} & -\frac{1}{2} \\ j & j & -\frac{j}{2} & -\frac{1}{2} & \frac{1}{2} & \frac{j}{2} \\ j & -1 & \frac{j}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{j}{2} \\ -1 & j & -\frac{1}{2} & \frac{j}{2} & -\frac{j}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix} \tag{6.9}$$

In the same way, we can have the S-parameter of the type B six-port as follows :

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 0 & 0 & -1 & j & j & -1 \\ 0 & 0 & j & -1 & 1 & j \\ -1 & j & 0 & -j & \frac{1+j}{2} & -\frac{1+j}{2} \\ j & -1 & 0 & -j & \frac{1+j}{2} & \frac{1+j}{2} \\ j & j & \frac{1+j}{2} & \frac{1+j}{2} & -1 & 0 \\ -1 & 1 & -\frac{1+j}{2} & \frac{1+j}{2} & -\frac{1+j}{2} & \frac{1+j}{2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix} \tag{6.10}$$

Since no power divider is used, the S-parameter of type C six-port will be formulated below, no matter it is implemented by microstrip or waveguide.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 0 & 0 & j & 1 & j & -1 \\ 0 & 0 & 1 & j & j & 1 \\ j & 1 & 0 & 0 & 0 & 0 \\ 1 & j & 0 & 0 & 0 & 0 \\ j & j & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix} \tag{6.11}$$

We can rewrite the S-parameters of the six port junctions in Equations 6.9, 6.10 and 6.11 as follows

$$\begin{bmatrix} [B_1]_{1\times 2} \\ [B_2]_{1\times 4} \end{bmatrix} = \begin{bmatrix} [0]_{2\times 2} & [S_{12}]_{2\times 4} \\ [S_{21}]_{2\times 4} & [S_{22}]_{4\times 4} \end{bmatrix} \begin{bmatrix} [A_1]_{1\times 2} \\ [A_2]_{1\times 4} \end{bmatrix} \tag{6.12}$$

where $[A_i]$ and $[B_i]$, $i = 1, 2$, are the incident wave and reflected wave.

When the type A and type B six-ports are implemented using waveguide-type structure, such as SIW, the sub matrix $[S_{22}]$ becomes nonzero. In simulation, all values of the load impedance, R_i (i=1, 2 ... 6) , are 50 Ω, which means all ports are matched. However, in an application of a six-port receiver, four ports, such as $P_3 \sim P_6$ in Figure 6.2(a), are connected with power detectors, which usually have limited matching. The phases from two inputs P_1 and P_2 to four outputs are important specifications that determine the performance of

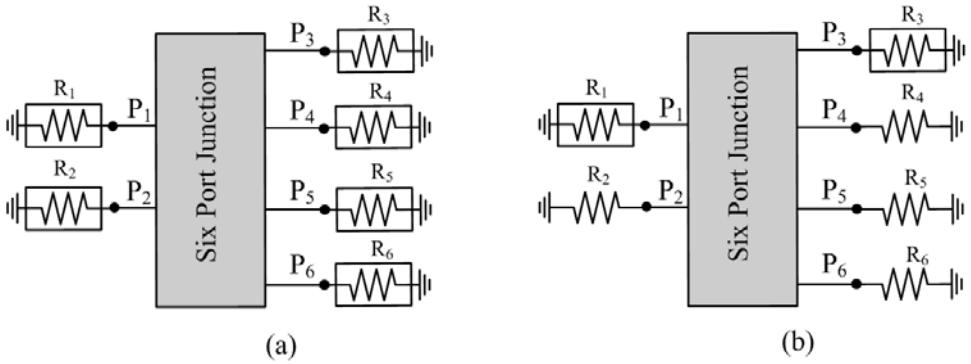


Figure 6.2 Setup for simulation(a) and measurement(b) of six-port junction.

the demodulation of the receiver. The phase in three different types of six-port junctions is plotted in Figure 6.3 when the load impedance $Z_3 = Z_4 = Z_5 = Z_6$ are swept from 25 Ω to 50 Ω, which represents the reflection caused by the load mismatch changing from -10 dB to perfectly matched. Each curve shown in Figure 6.3 is the phase normalized to its ideal value. For example in the figure for type A six-port junction, the four curves are defined as follows :

$$\begin{aligned}
\text{Curve} \quad 1 \quad &: \quad \text{Phase}(S_{32}) - \text{Phase}(S_{31}) - 180 \\
\text{Curve} \quad 2 \quad &: \quad \text{Phase}(S_{42}) - \text{Phase}(S_{41}) \\
\text{Curve} \quad 3 \quad &: \quad \text{Phase}(S_{52}) - \text{Phase}(S_{51}) - 90 \\
\text{Curve} \quad 4 \quad &: \quad \text{Phase}(S_{62}) - \text{Phase}(S_{61}) + 90
\end{aligned}$$

As shown in Figure 6.3, only when $[S_{22}]$ is zero in the type C six-port junction, the overall phase from input to output can be independent with the mismatch at four outputs. For the type A and B six-port junctions, the phase variance can be as large as 12° and 20°, respectively, when the reflection at port $P_3 \sim P_6$ is increased up to -10 dB.

A vector network analyzer (VNA) usually only has two or four ports. When the number of the device under test (DUT) is less than the port account of the testing instrument, the S-parameter of the device can be accurately measured with various calibration methods. However, when the DUT has a higher port count, some approximation needs to be adopted to get its S-parameters. A very common solution to this problem is to connect the ports under test with the instrument and terminate other ports with match loads. For example, in order to measure S_{31}, ports P_1 and P_3 are connected with a VNA which has already been calibrated with standard calibration kits using short-open-load-through (SOLT) method. Other four ports P_2, P_4, P_5 and P_6 are connected with 50 Ω load, as shown in Figure 6.2(b). For the

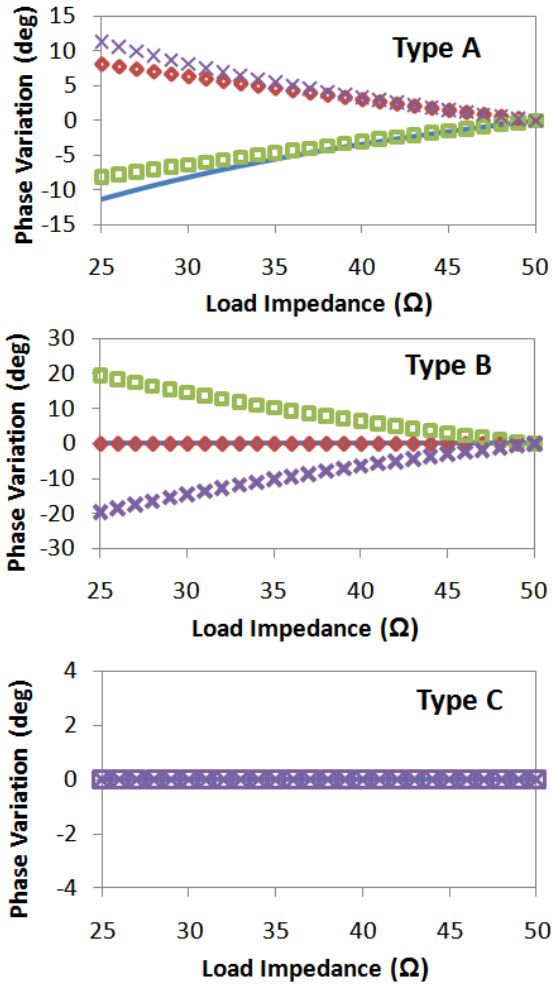


Figure 6.3 Phase variation with load impedance.

type A and type B six-port junctions, the measured phases of S_{31}, S_{41}, S_{51} and S_{61} can have some error when $[S_{22}]$ is zero. Some numerical experiments are adopted to investigate the impact of nonzero $[S_{22}]$ on the measured phases of four channels. For example, the simulation results of the type A waveguide-type six-port junction are shown in Figure 6.4. The figure is obtained after 8 measurements of S_{ij}, $i = 3, 4, 5, 6$ and $j = 1, 2$. In each measurement, only P_i and P_j are perfectly matched, the other four ports are loaded with a termination which impedance is swept between 25 Ω and 50 Ω. The obtained curves are very close to the results shown in Figure 6.3.

6.1.2 Design and measurement of SIW six-port junction

In a waveguide type six-port junction, the power splitter can be implemented by a Y-type three-port waveguide junction. A typical SIW Y-type three-port junction is shown in

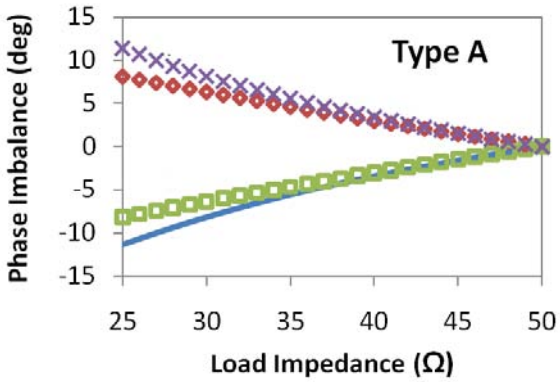


Figure 6.4 Phase variation with load impedance in measurement.

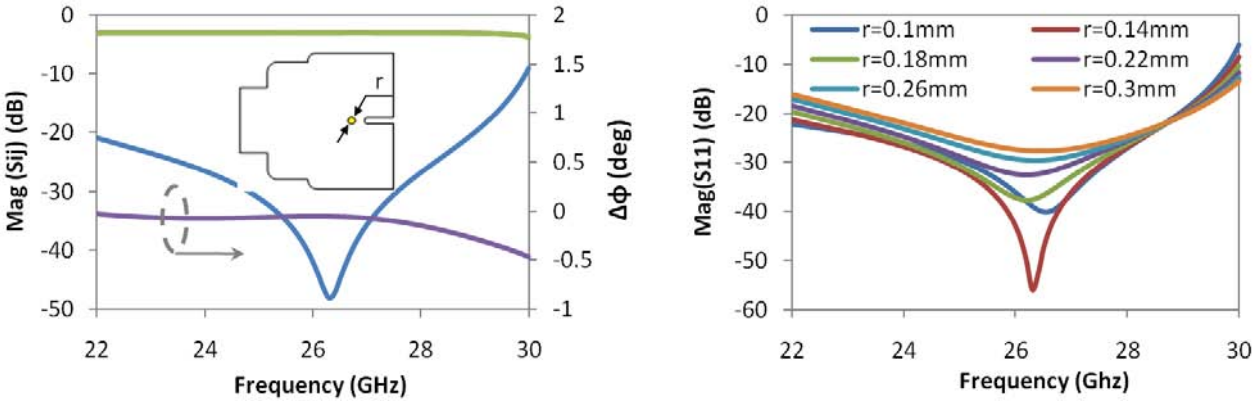


Figure 6.5 S-parameters of SIW Y-junction and parametric analysis of metal post radius.

Figure 6.5. A metallic post and several steps are used at the input port for having a better return loss. The simulated return loss is less than -20 dB from 22 GHz to 29 GHz. The phase $\Delta\phi$ and magnitude imbalance of S_{21} and S_{31} are less than $\pm 0.5^\circ$ and ± 0.1 within the full simulation frequency band. The parametric analysis in Figure 6.5 shows that the structure is not sensitive to the radius of the post with the available fabrication tolerance. A 3 dB coupler can be implemented as shown in Figure 6.6. The coupling coefficient and return loss at all ports can be tuned by the dimensions of the steps. In an optimized design shown in Figure 6.6, the return loss of all ports is less than -20 dB from 24.2 GHz to 30 GHz. The magnitude and phase imbalance are ± 1 dB and $\pm 1.72^\circ$, respectively, from 22.7 GHz to 30 GHz.

A type A and a type C six-port junctions can be composed of the optimized designs of 3-port SIW junction and 3 dB SIW coupler above. The layout of two six-port junctions are shown in Figure 6.7. A GCPW-to-SIW transition is used at each port for testing purpose.

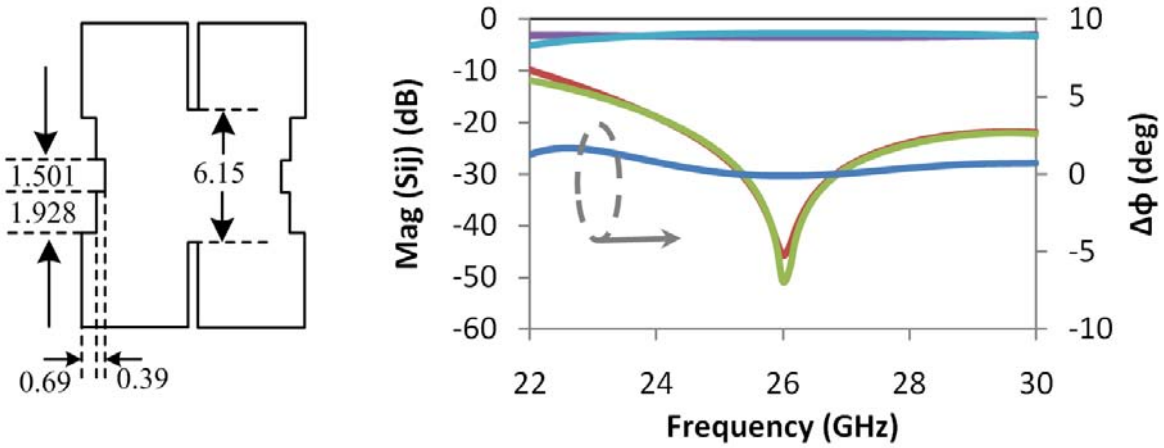


Figure 6.6 Layout and S-parameter of SIW 3 dB coupler.

The matching load at extra ports, P_7 and P_8, is implemented by covering the GCPW with a layer of RF absorber. For measurement, the return loss of such termination is between -10 dB $\sim$ -15 dB. Because of the impact of the reflection at ports $P_3 \sim P_6$ on the phase of these channels, we select the type C six-port junction in our design to minimize the phase error from simulation to measurement and real application. A 90° phase shifter needs to be placed in the arm between P_2 and P_5. The phase shifter can be implemented by offsetting one input from the central plane by 45° as shown in Figure 6.7(b). Another way to set offset is to add a folded line at each joint of two couplers. The length of the folded line l can be easily tuned and the 90° phase difference can be implemented by satisfying $l_2 - l_1 = 45°$.

The simulated and measured return losses at port P_1 and P_2 and the isolation between them are compared in Figure 6.8. From the comparison, both S_{11} and S_{12} have a good correlation between the simulation and the measurement. The isolation between two input ports P_1 and P_2 is higher than 20 dB within the entire interested band. The designed structure is fabricated on a single layer Rogers 6002 substrate with 20 milthickness. For testing the circuit, each port of the six-port junction is assembled with an end launch connector. In the measurement, the VNA is firstly calibrated with a set of through-reflection-line (TRL) calibration kits. The accuracy of the calibration can degenerate with the number of wearing the connectors. The measured S_{22} has a higher level compared to the simulated value and it might be caused by a bad connection in the calibration or measurement. However, the measured S_{22} is still lower than 10 dB within the entire band, which is good enough for our application.

Other important goals for the design of a six-port junction are the magnitude balance and phase shift in different channels. The simulated and measured magnitudes of S_{ij}, $i = 3, 4, 5, 6$

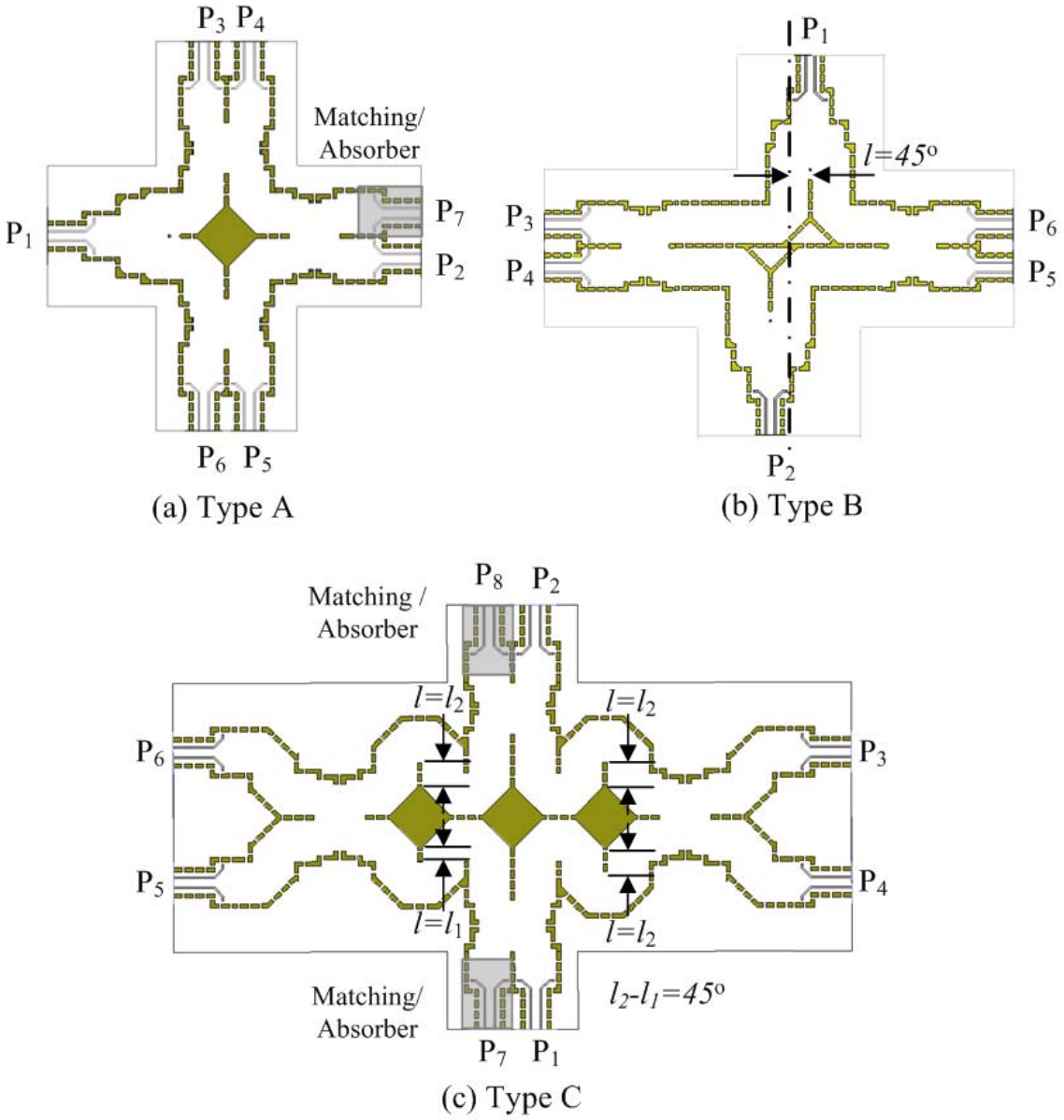


Figure 6.7 Layout of type A and type C SIW six-port junctions.

and $j = 1, 2$ are given in Figure 6.9 and Figure 6.10. The measured magnitude and phase of all S_{ij} are -7.9 dB $\pm$ 1.2 dB and $-3.5° \pm 8.5°$.

6.2 Simulation of SIW phase modulator and direct conversion receiver

In the previous chapters and sections, we have designed various SIW passive devices in a single-layer or double-layer Rogers' substrate. In this section, we try to build a transceiver system using the devices which are designed in the previous chapters and section. All devices

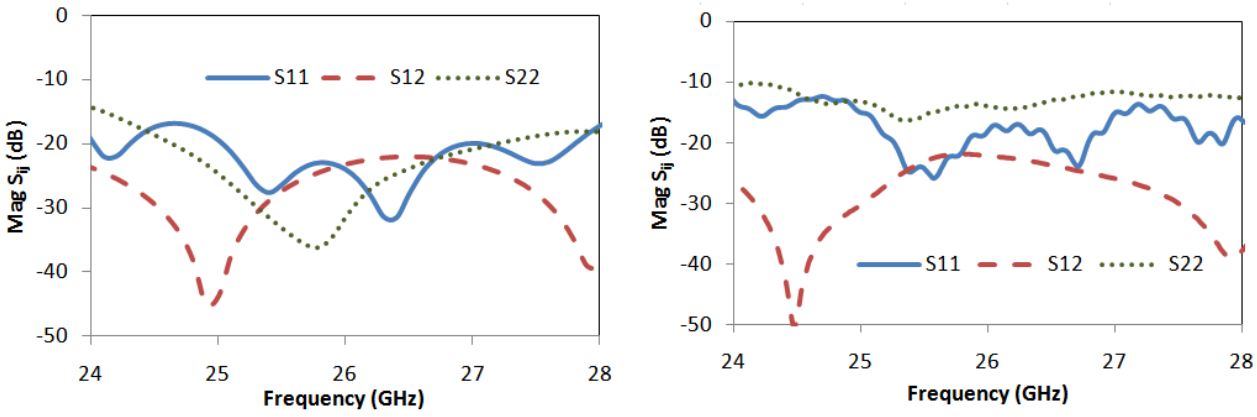


Figure 6.8 Simulated and measured return loss and isolation of inputs.

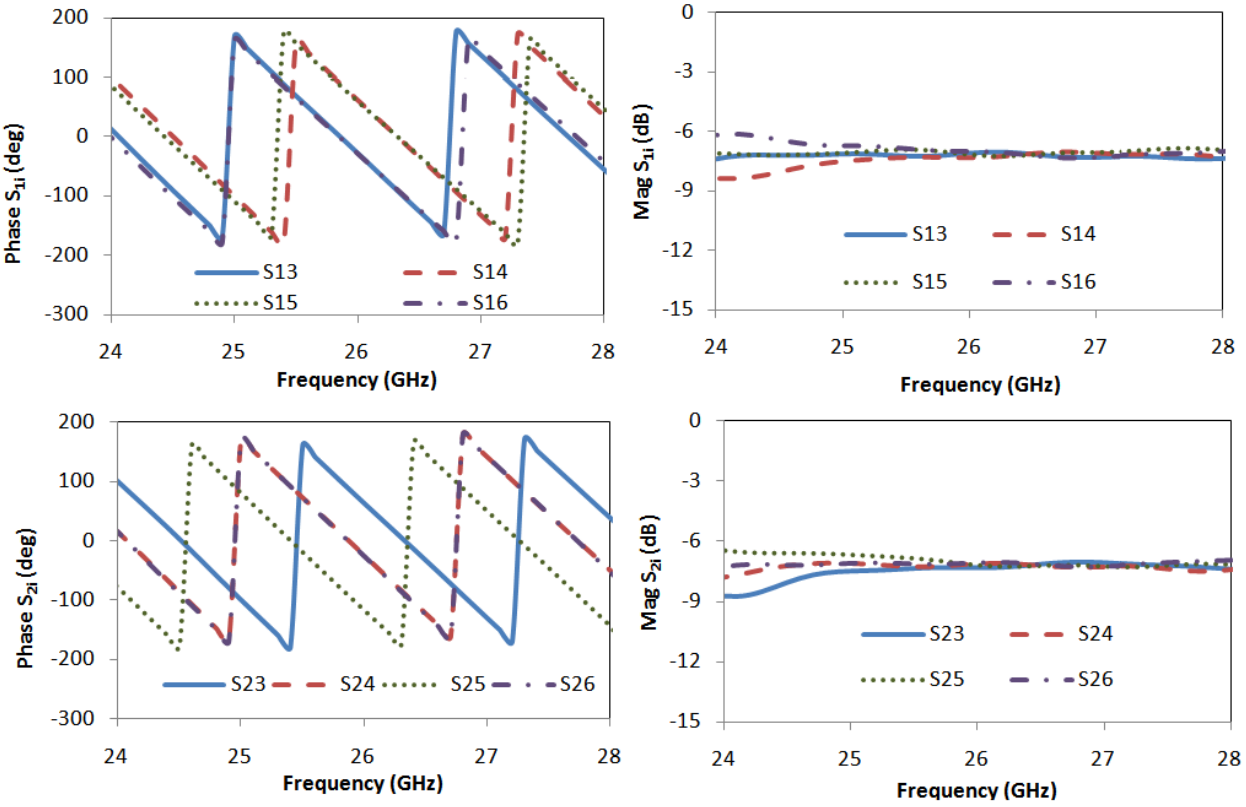


Figure 6.9 Simulated S-parameter of type C SIW six-port junction.

are designed in a Rogers substrate platform which is either a single-layer of 20 mil thickness or a double-layer substrate with 10 mil thickness of each single layer.

Many analytical studies and simulations of six-port receiver system have been reported

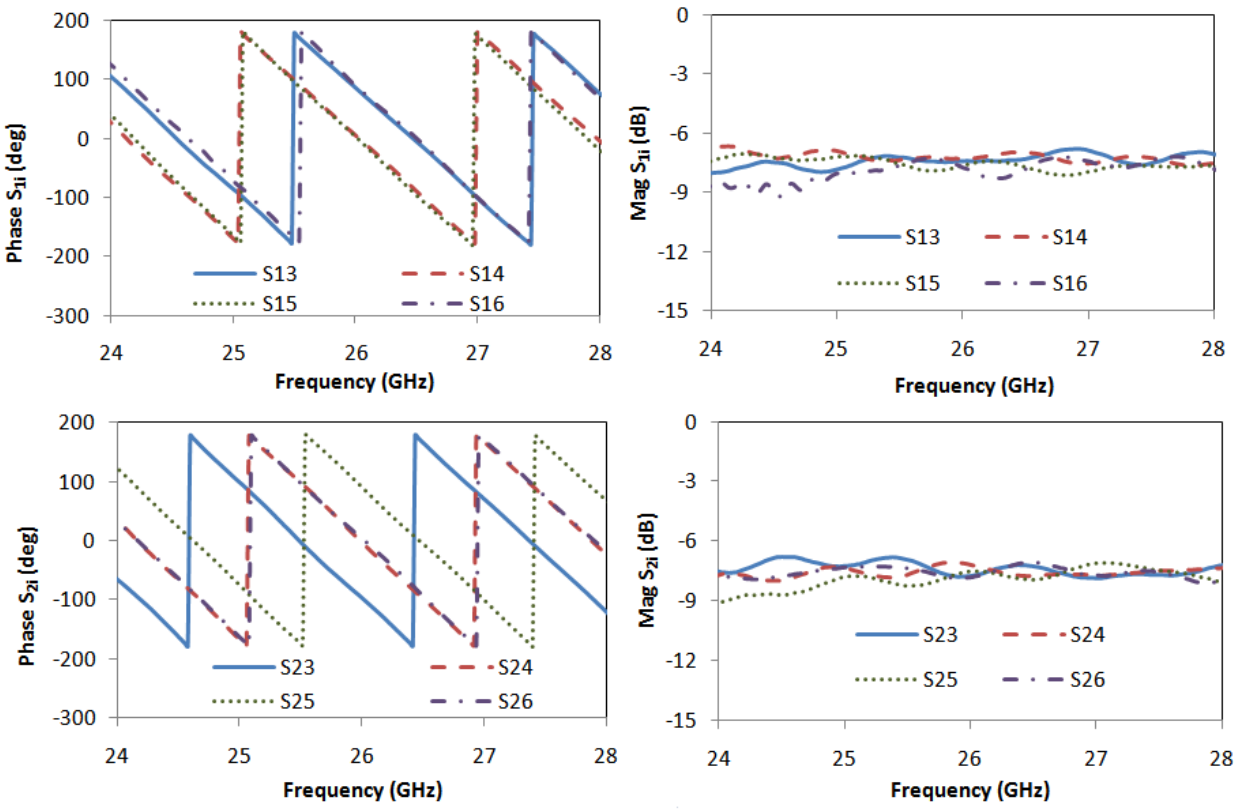


Figure 6.10 Measured S-parameter of type C SIW six-port junction.

In previous publications. In (Xu (2007)), the theory of a six-port receiver was analyzed in detail. Tatu *et al.* (2002) presented an ADS simulation of this type of receiver, in which the measurement focused on the input and output waveforms, constellation of demodulated signal, and frequency component. In this section, we employ an ADS envelop simulation to analyze the proposed receiver and transmitter. In the proposed system, there are conversions of digital, analog, and RF signal. To build such a mixed signal simulation of entire system in ADS, some special skills are adopted. In this section, we first discuss the test result of power detector. Then curve fitting is utilized to build a model of the test result, which is reused in another following simulation. We develop a theoretical model of system with a modulator and a demodulator, connected with each other. Following that process, we replace the simulated result with the measured result in the major components of modulator and demodulator, and simulate the system again. In the end, we connect the system with other components, such as antenna, diplexer, and various active devices to complete the whole system building.

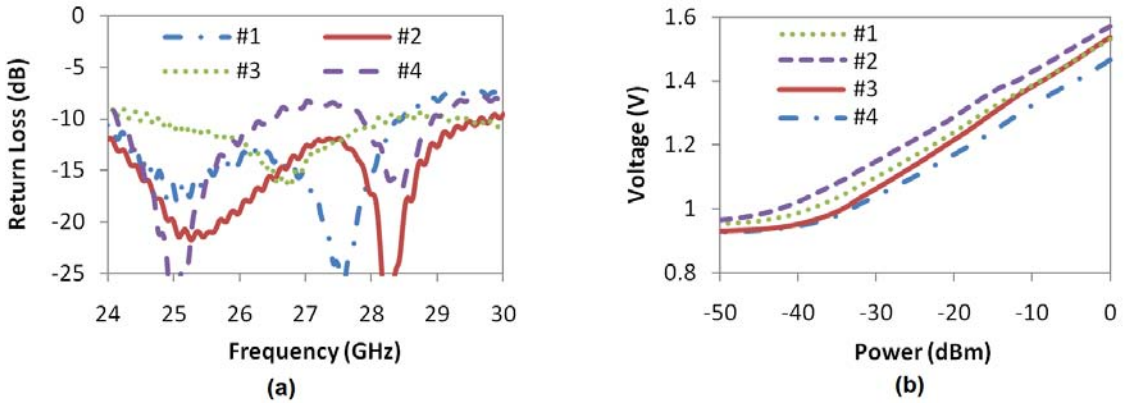


Figure 6.11 Measured return losses and power-voltage curve of detectors.

6.2.1 ADS model of RF power detector

To use the six-port junction as a demodulator in direct conversion receiver, four output ports of the six-port junction, P3, P4, P5 and P6, need to be connected with RF power detectors to convert the RF power into DC voltages. The detector used in the experiment is Hittite logarithmic detector HMC662LP3E, which has a wide dynamic range up to 28 GHz. Four detectors are surface mounted on GCPW in a single layer Roger R6002 substrate, which height is 20 mil. The return loss of each detector is about -5 dB without any matching tuning circuit. In order to improve the return loss at the interested frequency point, a small piece of substrate with a metal stub on top is loaded onto the GCPW at the input of each power detector. The return loss of the detectors No. 1, 2, and 3 is decreased to less than -10 dB at the interested frequency point, i.e. 26.5 GHz, as shown in Figure 6.11(a). The return loss of No. 4 detector is about -10 dB, a little worse than the others. Therefore, the output voltage is lower than others in the curves of output voltage changing with the input RF power for four detectors, as shown in Figure 6.11(b). It is observed that the power-voltage curves of four detectors have a good linearity when the input power is within the range of -40 dBm to 0 dBm. The output voltage levels have a maximum 0.1 V difference which might be caused by the performance difference of the devices themselves, the return loss of the RF ports and other factors during the assembling process. This voltage difference among four ports can be corrected by a potentiometer circuit shown in Figure 6.12.

In order to simulate the six-port demodulator subsystem, a true logarithmic amplifier is used in an ADS simulation for modeling the functionality of RF detector, to convert RF power to a DC voltage. The power-voltage curve of a detector is firstly measured and then saved in a module called ‘Data Access Component’ (DAC), as shown in Figure 6.13. Three parameters of the model for a logarithmic amplifier, including number of stages, stage gain

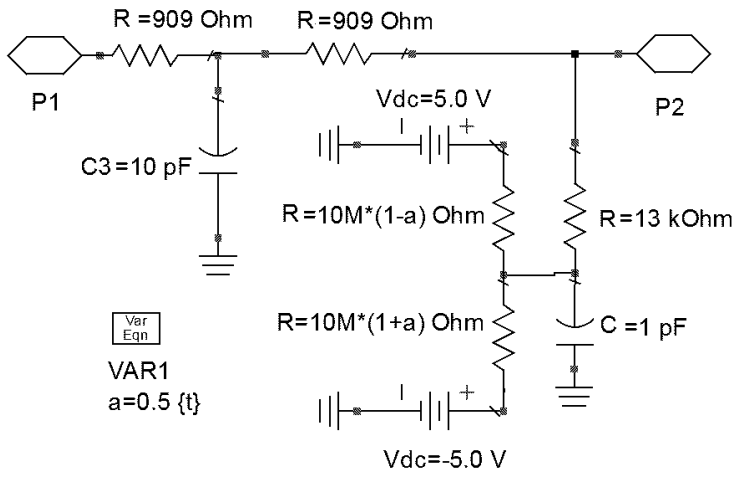


Figure 6.12 Low pass filter and potentiometer circuit connected to output of detector.

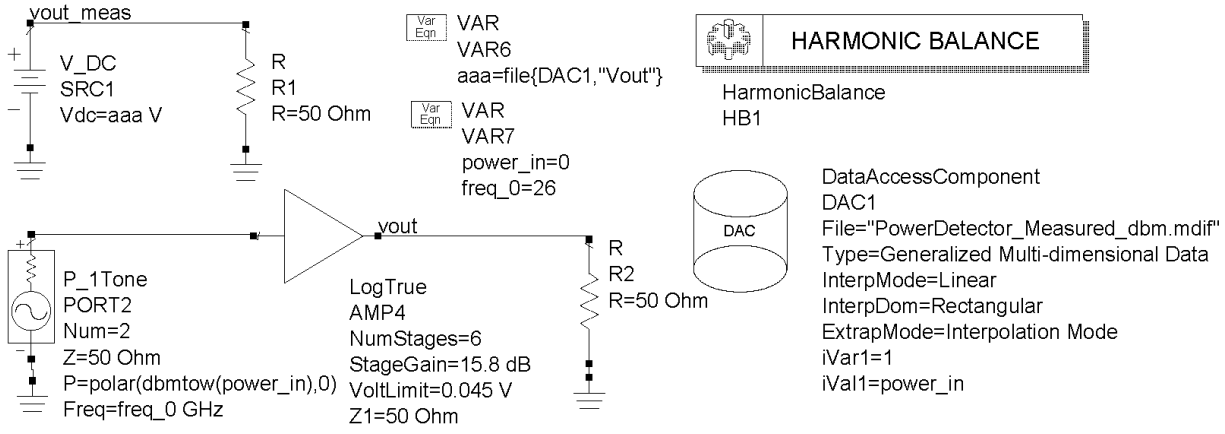


Figure 6.13 ADS model of logarithmic detector.

and voltage limit, are adjusted in order to obtain a good matching between the simulated and measured power-voltage curves. One example of the measurement and simulation correlation of the power detector is shown in Figure 6.14.

In the experiment shown in Figure 6.15, we measure the DC voltage at four outputs changing with the phase difference of the two inputs. A RF source $A\cos(\omega_c t)$ is equally split into two by a power divider. One of them directly inputs to one port of the six-port junction P_1. Another path is connected with a tunable phase shifter and then the signal input into another port of six junction P_2.

The normalized outputs of simulated and measured DC voltage of the four detectors are shown in Figure 6.16. The minimum values of four outputs are shifted by 90°. The curve is

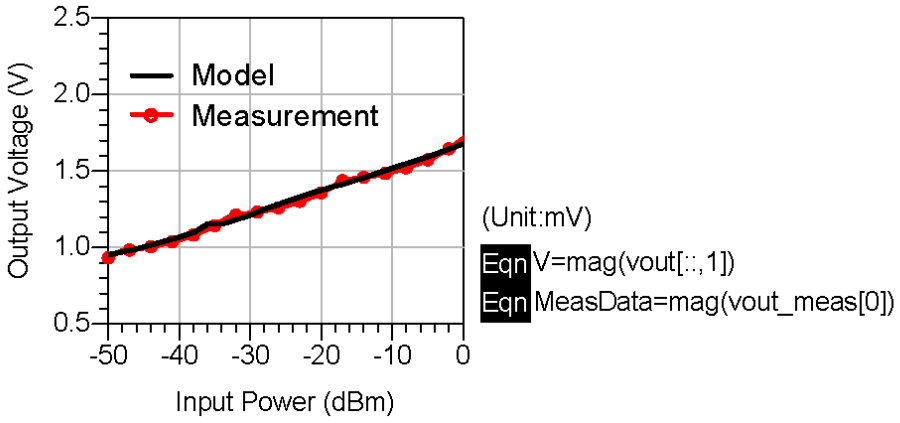


Figure 6.14 Measured and simulated power-voltage curves of logarithmic detector.

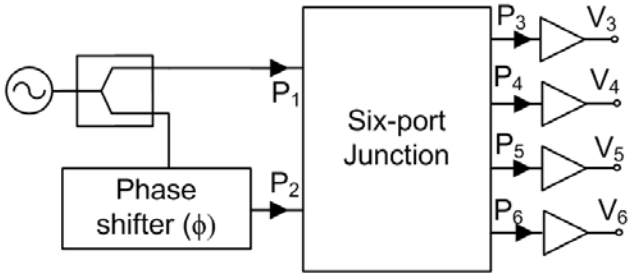


Figure 6.15 Experiment for testing the detected DC voltage changing with the phase difference.

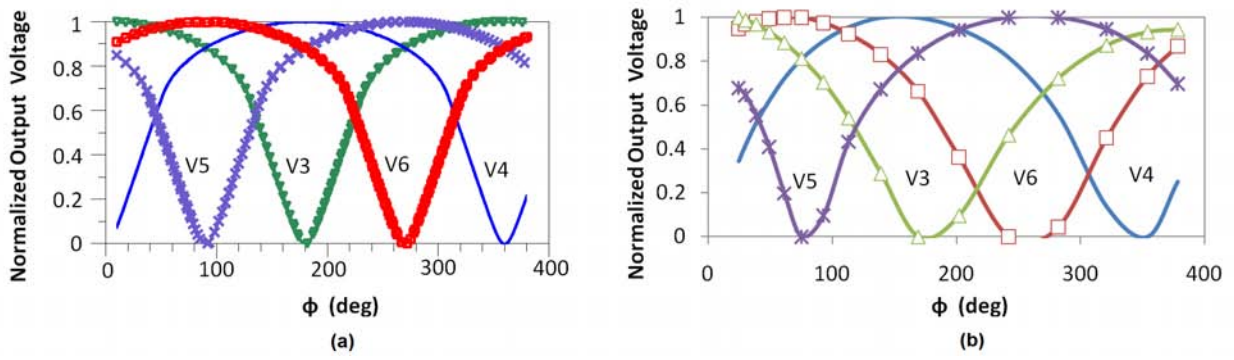


Figure 6.16 (a) Simulated and (b) measured normalized DC voltages changing with phase difference between two inputs.

obtained with the input power equals to -15 dBm. When the input power is changed between -40 dBm $\sim$ 0 dBm, similar curve can be obtained.

6.2.2 ADS simulation of ideal phase modulator and six-port quadrature demodulator

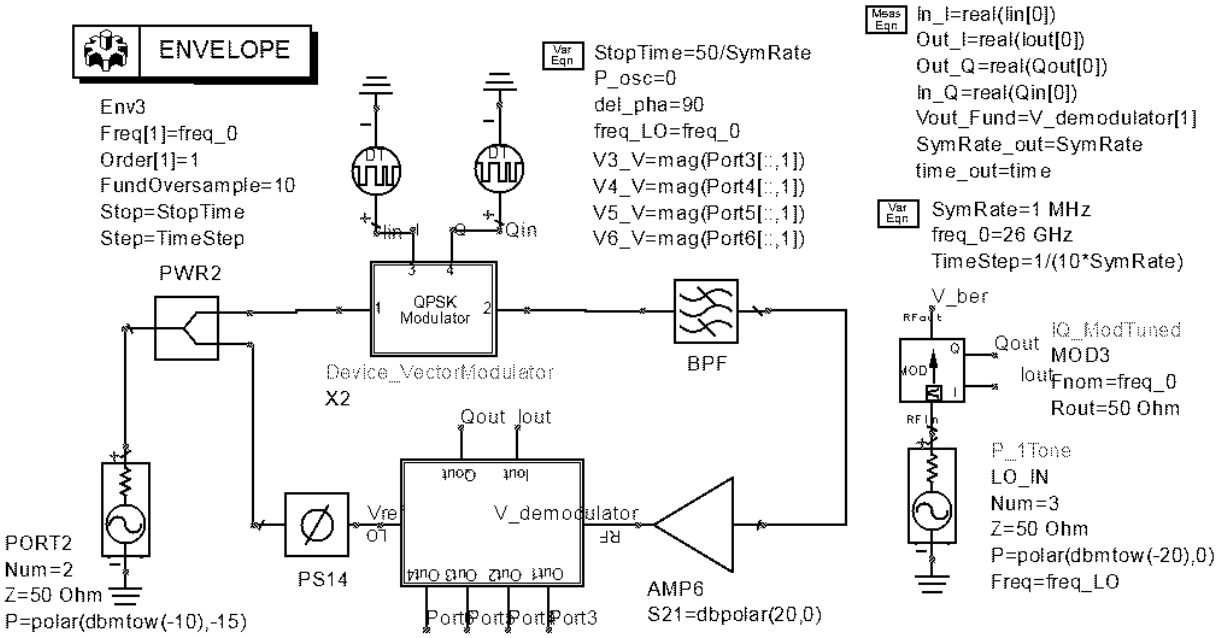


Figure 6.17 ADS simulation of ideal phase modulator and six-port quadrature demodulator.

The first ADS simulation we perform here is a transceiver system envelop simulation. The simulation setup is shown in Figure 6.17. In this simulation, a phase modulator is connected with a six-port demodulator directly, without any air link between them. All components and subsystems used in this simulation are composed of the ideal models provided in ADS. The models of demodulator and modulator are shown in Figure 6.18 and Figure 6.19, respectively. A phase shifter is used between the RF source and the second input of the demodulator for the purpose of phase synchronization. The six-port in the demodulator is composed of four 3-dB couplers and three fixed phase shifter. All four power detector model use the same model obtained in the previous section. The I/Q signal can be demodulated by comparing the output voltages of two detectors. The modulator has four paths and each of them has a fixed value phase shifter, an attenuator and two voltage controlled switches. The control voltage is determined by the value of I/Q signal through the frequency domain defined device (FDD) in ADS. For each state, only one path is turned on and the signal passing through

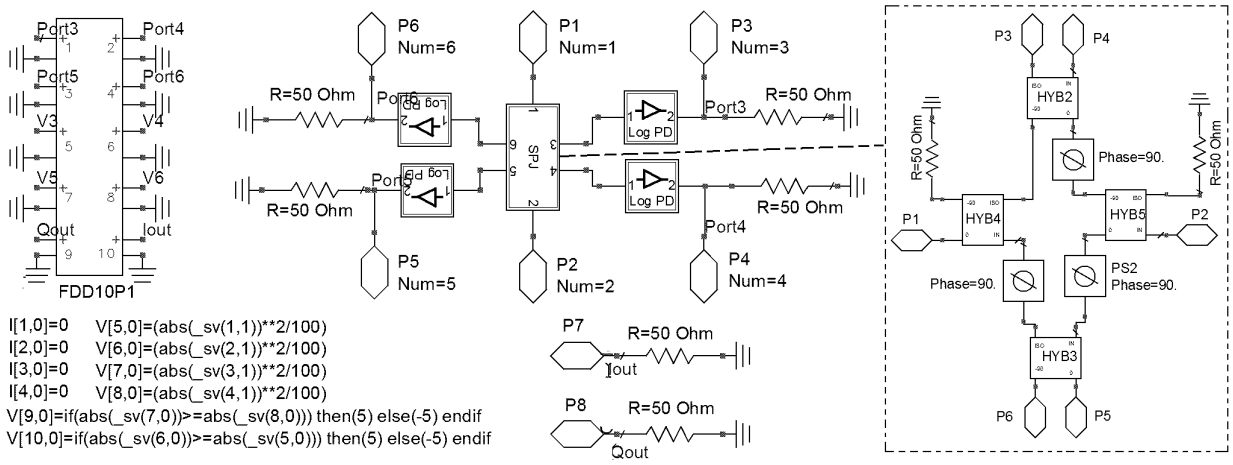


Figure 6.18 Ideal model of six-port quadrature demodulator.

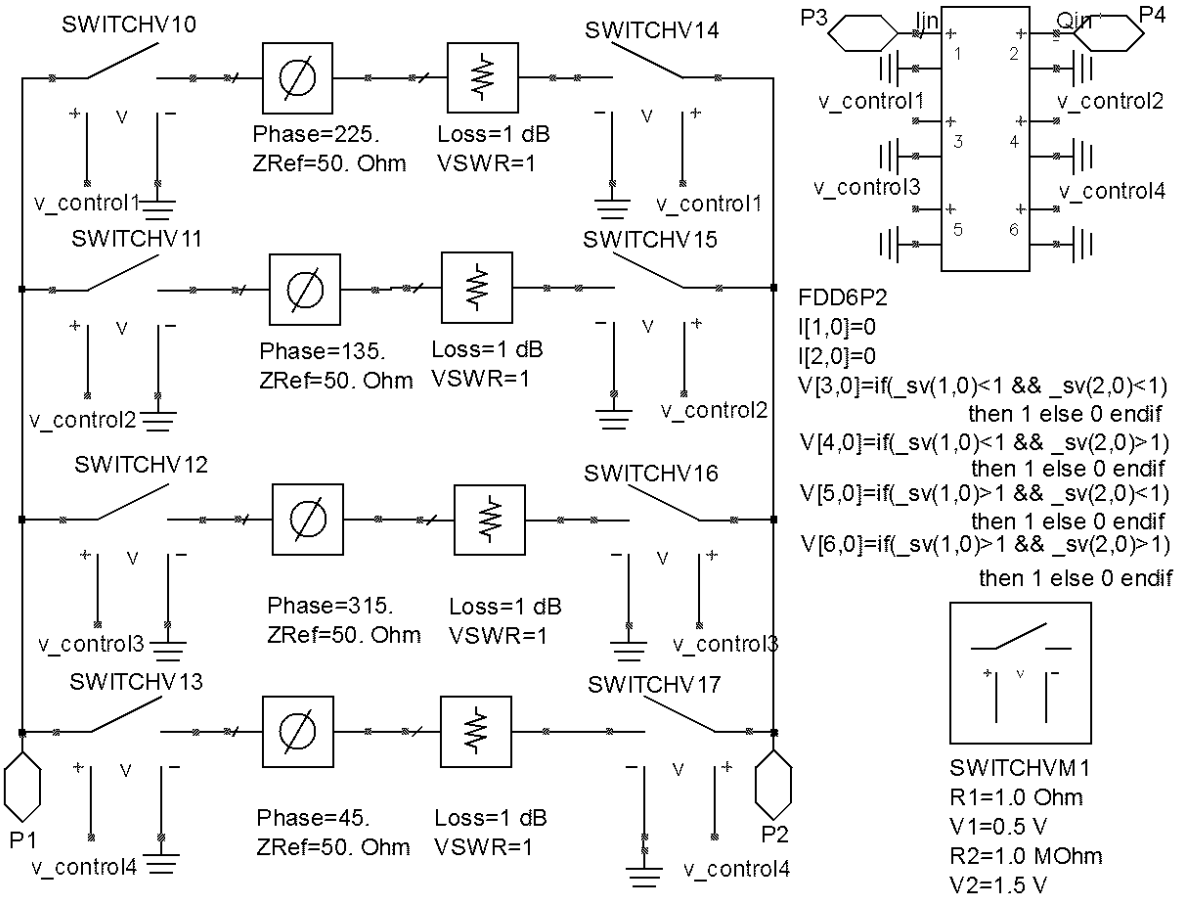


Figure 6.19 Ideal phase modulator.

will be shifted by a fixed phase value, 45°, 135°, 225° or 315°.

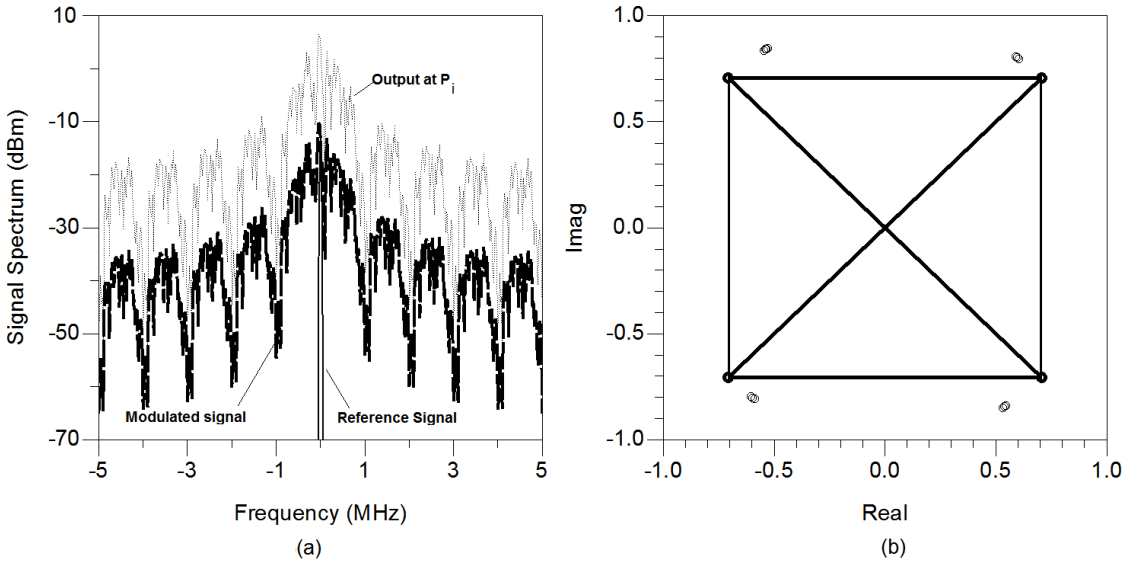


Figure 6.20 Spectrum and constellation of phase shifter modulator.

The spectrum of the modulated signal and reference signal is given in Figure 6.20(a). The spectrum of the output of the RF power detector is also shown in this figure. Two constellations of the modulated signal and the output I/Q signals are shown in Figure 6.20(b). The waveforms at four outputs of the power detectors are shown in Figure 6.21 with the corresponding input and output I/Q signals.

6.2.3 ADS simulation of SIW phase shifter modulator and SIW six-port demodulator

The second simulation is also carried out for a phase modulator connected with a six-port demodulator as shown in Figure 6.22. Different from the previous simulation, we use measured data and simulation model instead of the ideal model so that the simulation results are closer to the realistic results. The phase modulator proposed in the previous chapter is used here as a phase modulator. The model of the modulator is a set of measured S-parameters when the control voltages are adjusted from 0 V to 15 V, with 1 V for each discrete sampling step. In order to use this model in an envelope simulation in ADS, we need to express the control voltage of the phase modulator as a function of the input I/Q signals. The I and Q signals are generated by the simulation of the encoder shown in Figure 5.28 of Chapter 5 and recorded in files 'Idata.tim' and 'QData.tim', respectively. The files are used to assign value of two voltage control sources by using DAC, as shown in Figure 6.22. At each sampling point, the

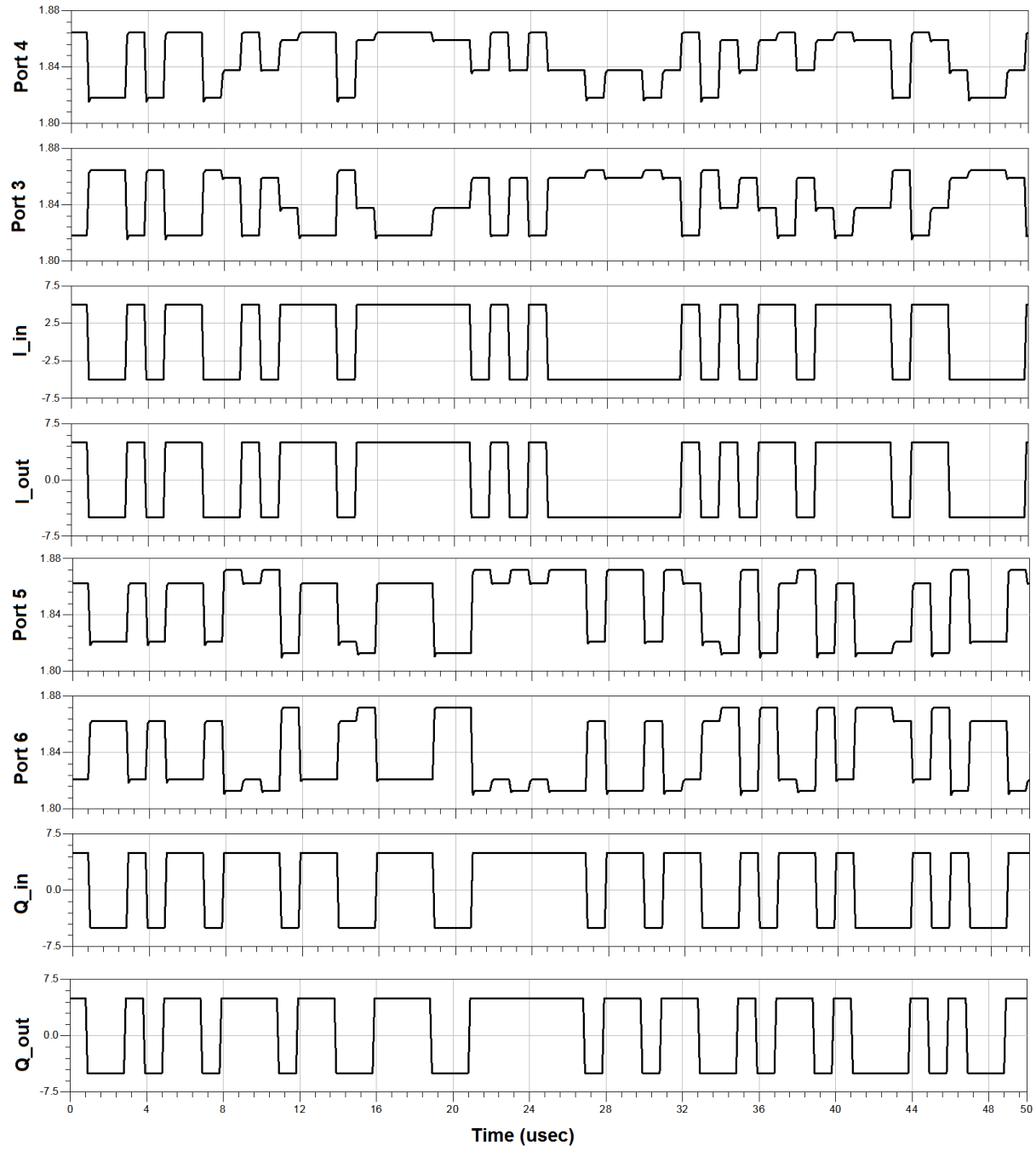


Figure 6.21 Waveform of phase shifter modulator.

control voltage of the phase modulator is then decided by the I/Q signals and a mapping table in another DAC 'Vcon_test.mdif', which is as follows :

```
1        VAR I(1)= 0
2        VAR Q(1)= 0
```

```
3          BEGIN BLOCK1
4          % Indextest(1) Vcon(real)
5          1   0
6          END
7
8          VAR I(1)= 1
9          VAR Q(1)= 0
10         BEGIN BLOCK1
11         % Indextest(1) Vcon(real)
12         1   5.55
13         END
14
15         VAR I(1)= 0
16         VAR Q(1)= 1
17         BEGIN BLOCK1
18         % Indextest(1) Vcon(real)
19         1   10.57
20         END
21
22         VAR I(1)= 1
23         VAR Q(1)= 1
24         BEGIN BLOCK1
25         % Indextest(1) Vcon(real)
26         1    8.
27         END
```

The topology of the demodulator used in this simulation is similar to the one shown in Figure 6.18. However, instead of using theoretic models of the coupler and dividers, the model of the six-port junction used in this simulation is an S-parameter in touchtone format. The S-parameter file is generated by a full wave simulation software Ansoft HFSS. Since the reference signal and the modulated signal are generated by the same RF source, carrier recovery problem can be simplified to a phase synchronization. This problem will be discussed more in the following section, which can be easily implemented by inserting a phase shifter and a tunable attenuator between the RF source and the input of the six-port. The waveform in time domain of the four outputs of the power detectors are given with the corresponding input and output I/Q signals, as shown in Figure 6.23. The bit error rate (BER) of the demodulator is about 10^{-6} when the Eb/No is at a level of -11 dB, as shown in Figure 6.24(a).

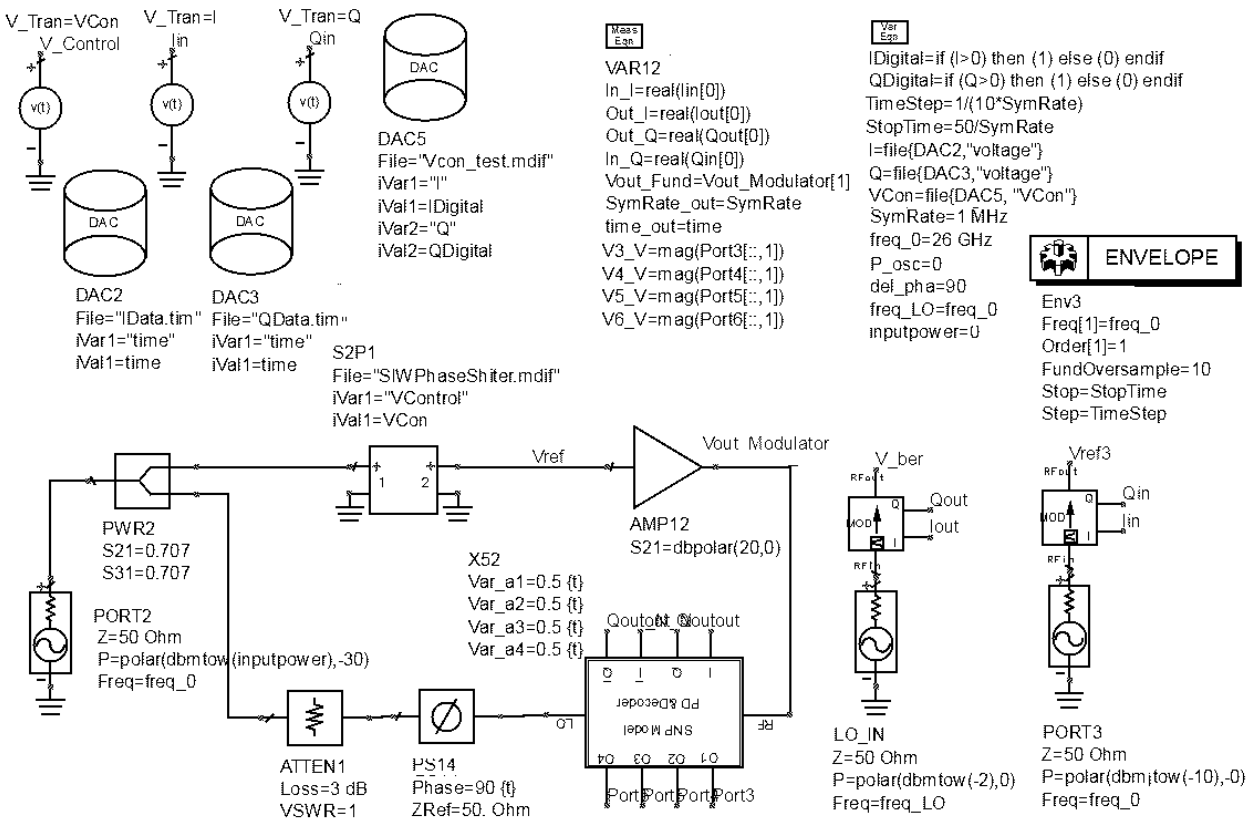


Figure 6.22 ADS simulation model of an SIW phase shifter modulator and an SIW six-port demodulator.

The constellation of the simulation model is plotted in Figure 6.24(b).

To verify this simulation, an experiment is conducted as shown in Figure 6.25. Figure 6.25(a) illustrates the entire experiment setup. The Rohde & Schwarz I/Q Modulation Generator AMIQ is used for generating the baseband signal. The I/Q signal input into the encoder (Figure 6.25(b)(1)) to generate the voltage sequence for controlling the phase shift of location frequency passing through the 360° phase shifter (Figure 6.25(b)(3)) modulator. A 3 dB power divider splits the RF signal source into two. One is for generating the modulated signal and the other is used as reference signal after a phase offset in a 180° phase shifter (4). Like the topology used in (Tatu *et al.* (2001)), the circuit of the demodulator (Figure 6.25(b)(2)) includes a six-port junction and four RF detectors for directly converting the modulated signal into baseband signal. Each detector is connected with an analogy circuit including low pass filter, operational amplifier and potentiometer circuit for DC offset cancelation. Two of four outputs are compared in a comparator AD8611 and generate the one baseband signal. The output I/Q signals are compared with the inputs in an oscilloscope (Figure 6.25(c)(5)).

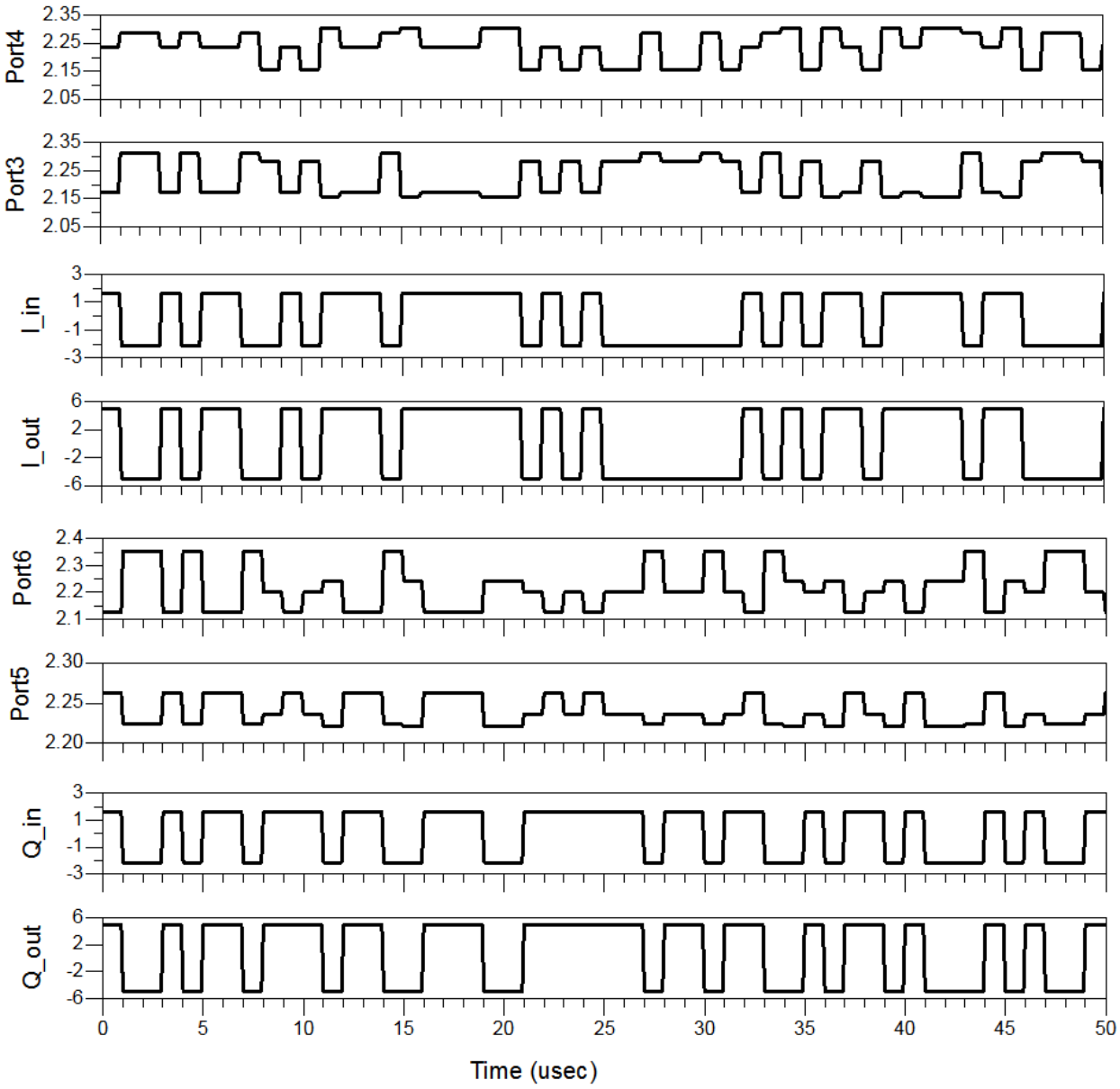


Figure 6.23 Waveform of the ADS simulation model of the SIW phase shifter modulator and the SIW six-port demodulator.

The pictures of some essential parts used in the experiment are shown in Figure 6.25(b). The snapshot of display on the oscilloscope is shown in Figure 6.25(c). The first and third channels are input I and Q signals and the second and forth channels are corresponding output baseband signal. The symbol rate in this experiment is 50 Kbit/sec. When the symbol rate is increased, the error bit obviously increases. We believe that the DC offset in the demodulator might cause the DC leakage from the modulator and degenerate the performance of the DC

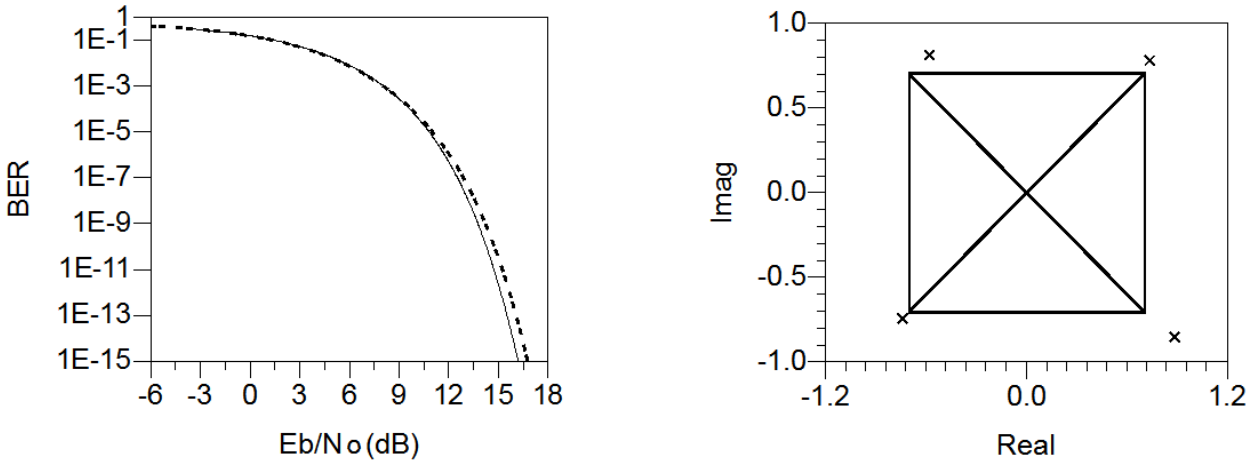


Figure 6.24 BER (a) and constellation (b) of the ADS simulation model of the SIW phase shifter modulator and the SIW six-port demodulator.

cancelation circuit.

6.2.4 ADS simulation of SIW transceiver

In this section, an SIW transceiver is composed of the phase modulator proposed in Chapter 5 and a six-port demodulator. The system diagram and layout of the transceiver are shown in Figure 6.26. Compared with the traditional heterodyne receiver, a low-cost homodyne (or direct conversion) receiver can demodulate high-speed signal by using broadband and less sensitive six-port junction. However, the performance of such a direct conversion receiver depends on the implementation of an efficient carrier recovery. A carrier recovery is a technique to synchronize the frequency and phase of the reference signal (or local oscillation signal) of the receiver with the modulated signal. If their frequencies of the two signals are the same, the phase synchronization can easily be achieved with a tuneable phase shifter. In some studies of the direct conversion receiver, the modulated signal and the LO are generated by the same RF source in which case the carrier recovery is simplified to the phase synchronization only. However, this is a practical problem one needs to face when using a multi-port direct conversion receiver in the design of a transceiver system. There are two solutions used for solving this problem in the previous works. In (Marsan *et al.* (2002); Tatu *et al.* (2003)), second six-port modulator is used to generate the carrier signal using the demodulated baseband signal. Limited by the analog to digital circuit and the digital signal processing algorithm, this is not a low-cost solution which can keep the capability of demodulation for high-speed data rate signal. Another solution proposed in (Mallat *et al.* (2009)) is to transmit the car-

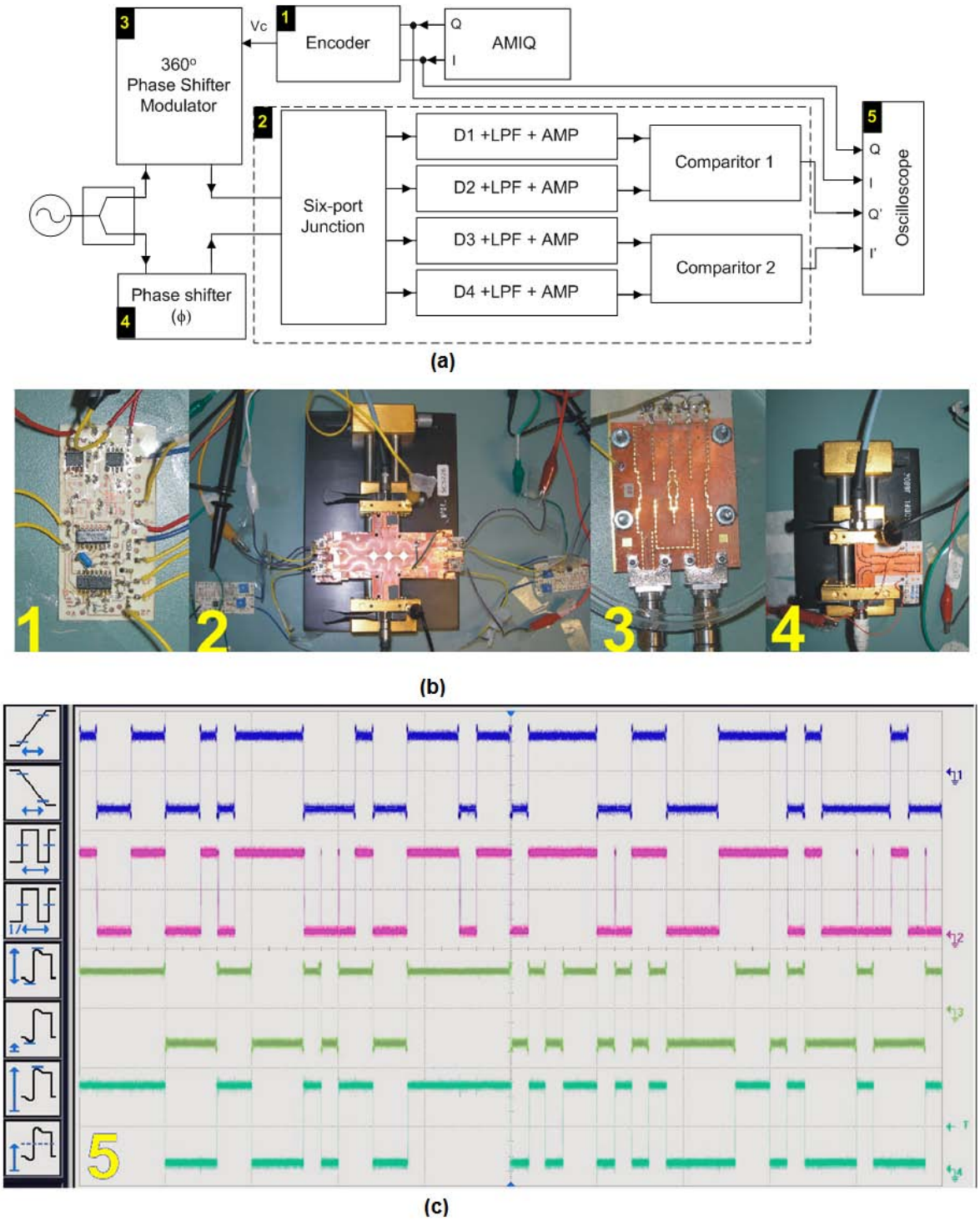
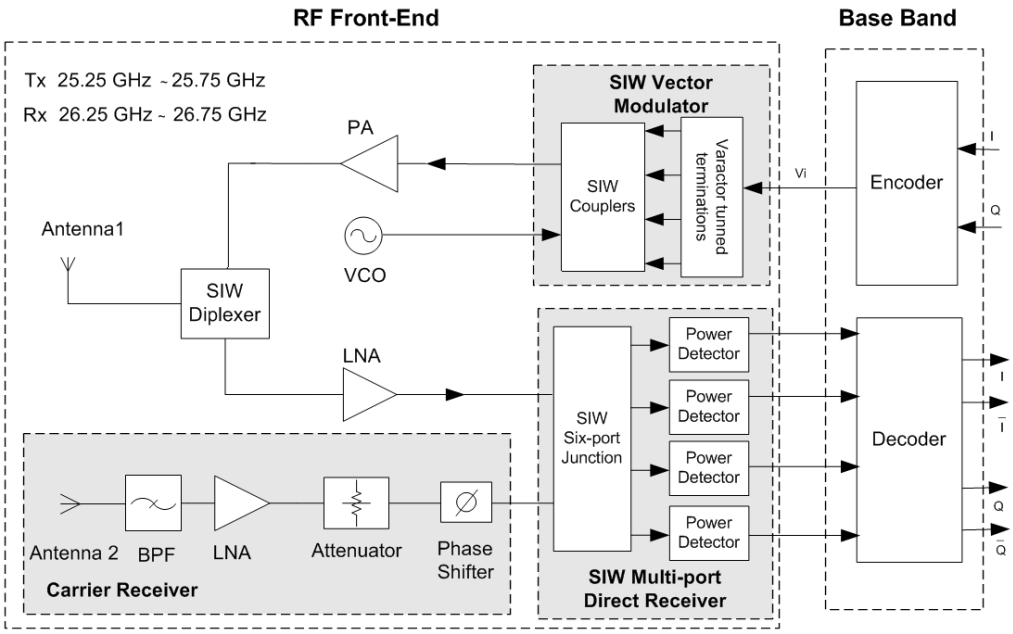
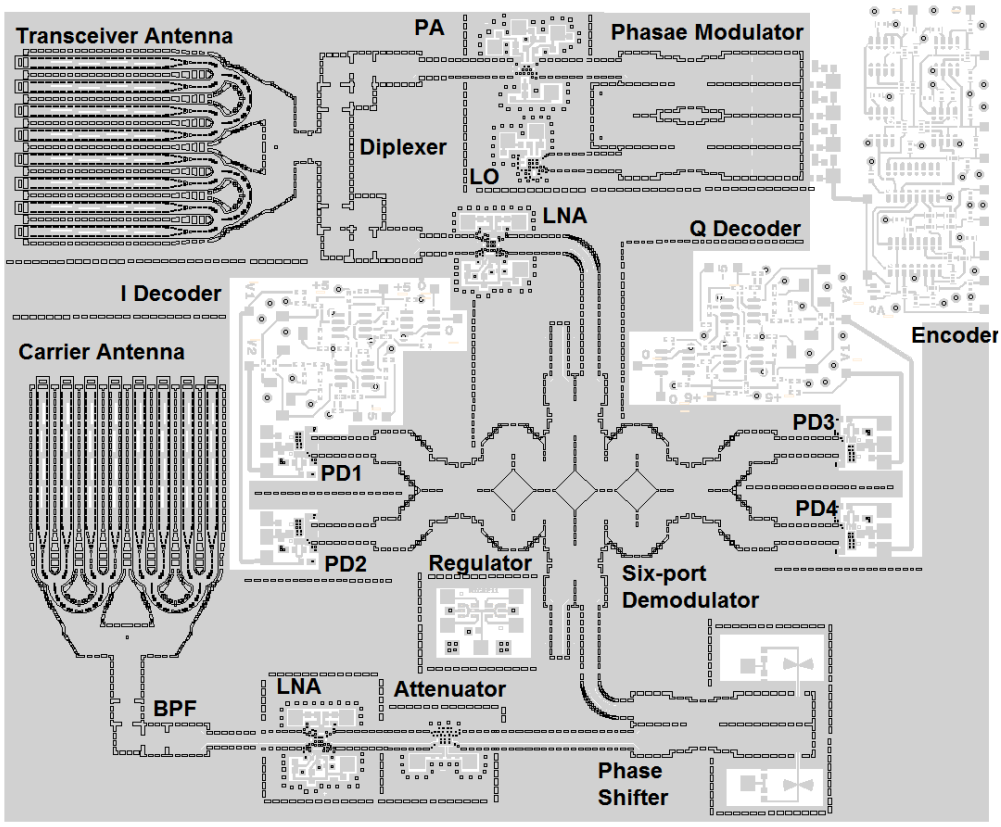


Figure 6.25 Measurement of the SIW phase shifter modulator and the SIW six-port demodulator, (a) the diagram of measurement setup, (b) four essential components and (c) measured input and output waveforms of I/Q signals.



(a)



(b)

Figure 6.26 (a) System diagram and (b) layout of SIW transceiver.

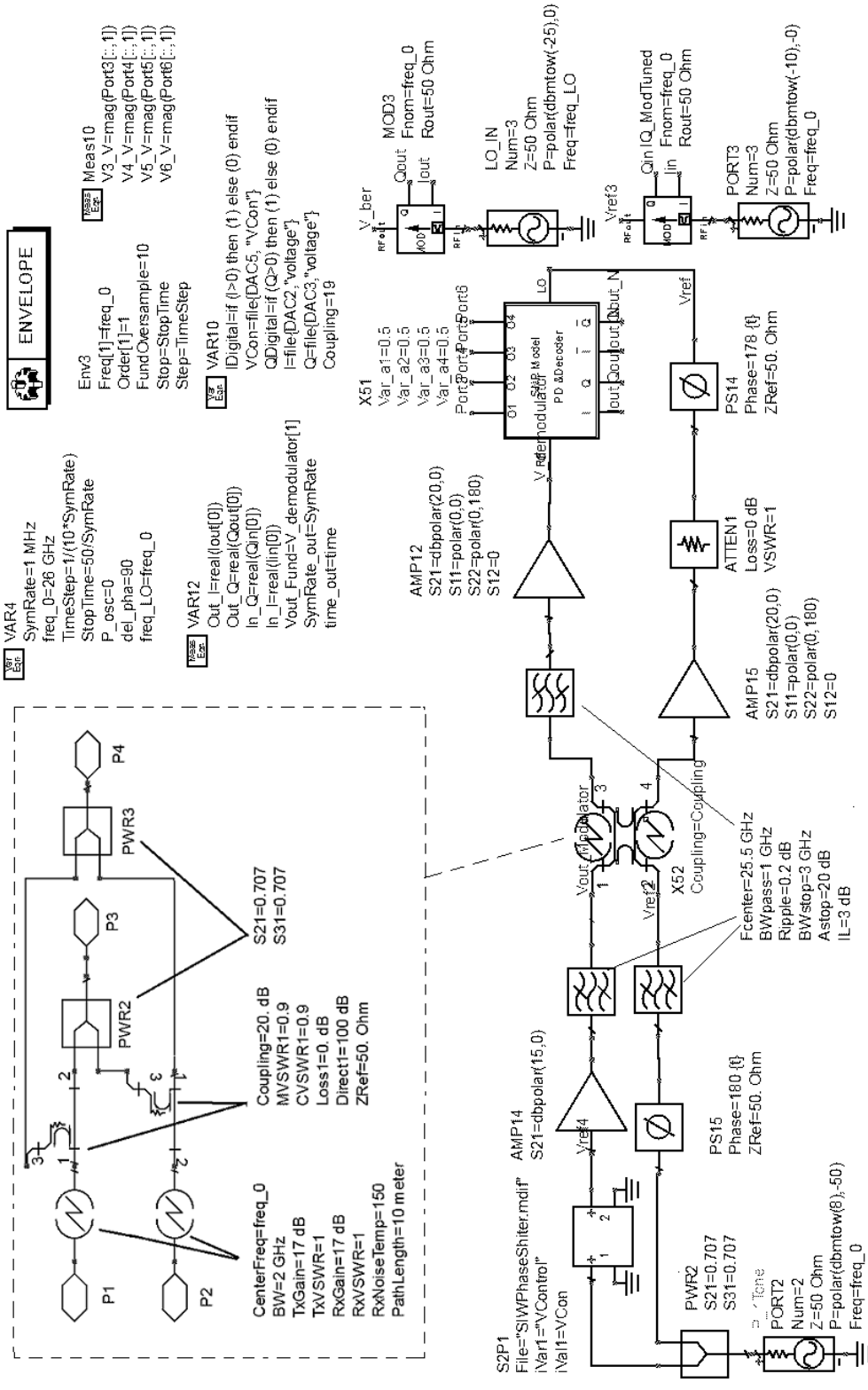


Figure 6.27 ADS simulation model of SIW transceiver.

rier to the receiver using a cross-polarized antenna instead of recovering the carrier from the modulated signal. Although the frequencies of the two signals are overlapped, the isolation between them can be achieved by placing two linear polarized antennas perpendicularly. The second solution is adopted in the proposed transceiver system as shown in Figure 6.26.

A system simulation is performed in ADS, as shown in Figure 6.27. In the same way as the previous one, this simulation is based on the measured S-parameter of the phase shifter and simulated S-parameter of the six-port junction. According to the measurement in Chapter 4, two vertically placed 4 SIW slot array antennas both have 17 dBi gain and a 20 dB polarization loss factor (PLF) at the carrier frequency of 26.5 GHz. In order to model the impact of the polarization mismatch between the two antennas, two couplers and power dividers are used to build the dual air links between the transmitter and receiver, as shown in Figure 6.27. As shown in Figure 6.28(a), a typical 10^{-6} value of the bit error rate (BER) corresponds to 14.7 dB value of the Eb/No ratio when the PLF equals to -20 dB, versus a 10.7 dB value as in the theoretical case. The BER of the transceiver degenerates greatly when the PLF decreases to 10 dB. The constellation of the modulated input into and output from the demodulator are given in Figure 6.28(b).

Except some components we have designed and measured in the previous chapters, such as modulator, demodulator, two antennas, band pass filter (BPF) and diplexers, there are also active components, including power amplifier, low noise amplifier, voltage controlled oscillator. These are all commercial packaged integrated circuits, which are surface mounted on a single layer Rogers substrate and connected with other circuits through GCPW. These active devices are fabricated and their measured values are directly used in the ADS simulation in order to validate the power budget of the proposed architecture. The measured S-parameters of these components are shown in Figure 6.29. The output power of the VCO (HMC739) is about 8 dBm with a resonant frequency of 26.5 GHz, when the control voltage is about 4.2 V. The measured gain of the low noise amplifier (HMC499) in the receiver and the power amplifier (HMC752) in the transmitter are 25 dB and 15 dB, respectively. A tunable attenuator (HMC722) and a 180° phase shifter are used between the BPF and six-port junction for a fine phase and magnitude tuning to the received carrier signal or reference signal. As shown in the Figure 6.28(c), the power of the carrier and modulated signal output from the transmitter are about 5 dBm and -10 dBm respectively. The free space loss at such a frequency can be analytically calculated using the Friis transmission equation below

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 \tag{6.13}$$

where R (10 m in our simulation) is the distance between transmitter and receiver, G_t and G_r

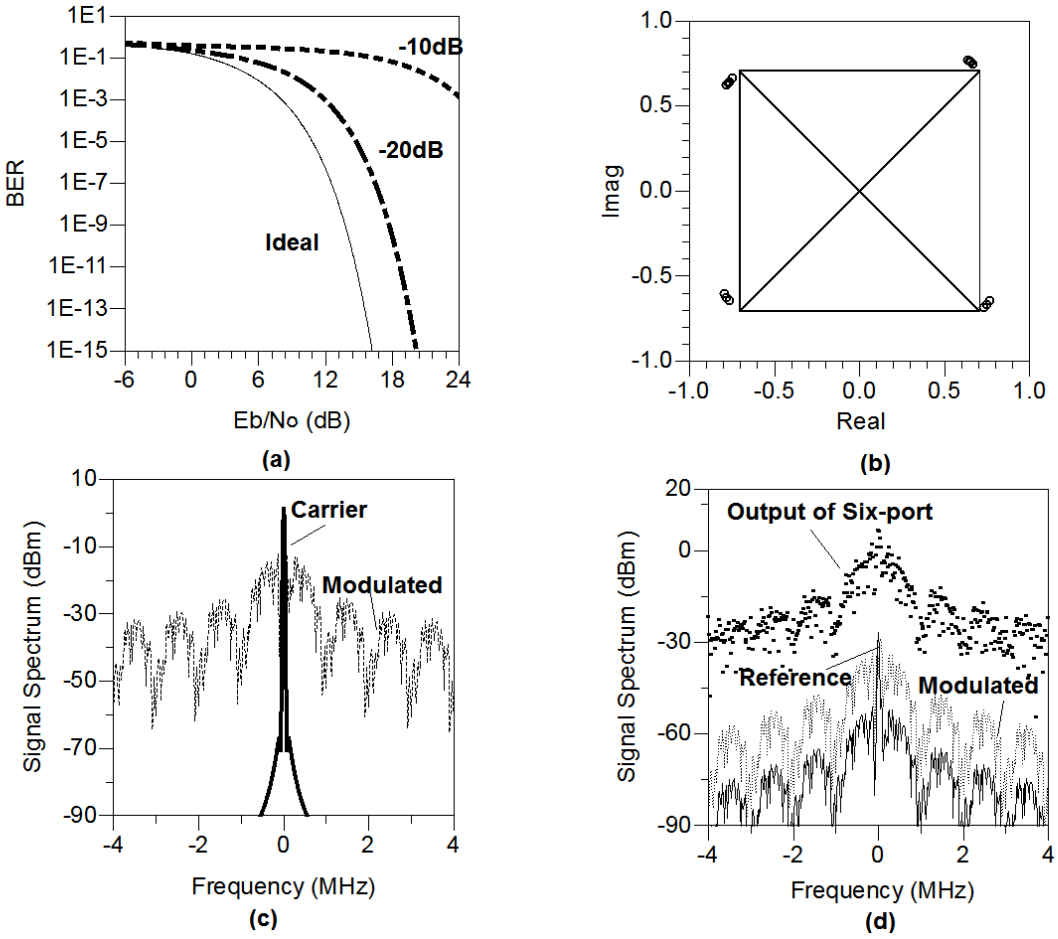


Figure 6.28 (a) BER , (b) constellation and (c) (d) spectrum of ADS simulation of SIW transceiver.

are gains of the transmitting and receiving antennas, P_t and P_r are powers of the transmitted and received signals. The spectrum of the received modulated signal and reference signal are shown in Figure 6.28(d). The calculated path loss of a signal of 26.5 GHz is about 45 GHz, the same as the value abstained in the simulation. The symbol rate used in the simulation is 1 Mbit/sec. The waveforms of the output of four power detectors are given in Figure 6.30, together with the input and output I/Q signals.

6.3 Conclusion

In this chapter, we firstly discuss the impact of nonideal terminations to the phase and magnitude balance in different six-port architectures. Because the isolation between two outputs of a waveguide three-port junction is not as ideal as a Wilkinson power divider, the

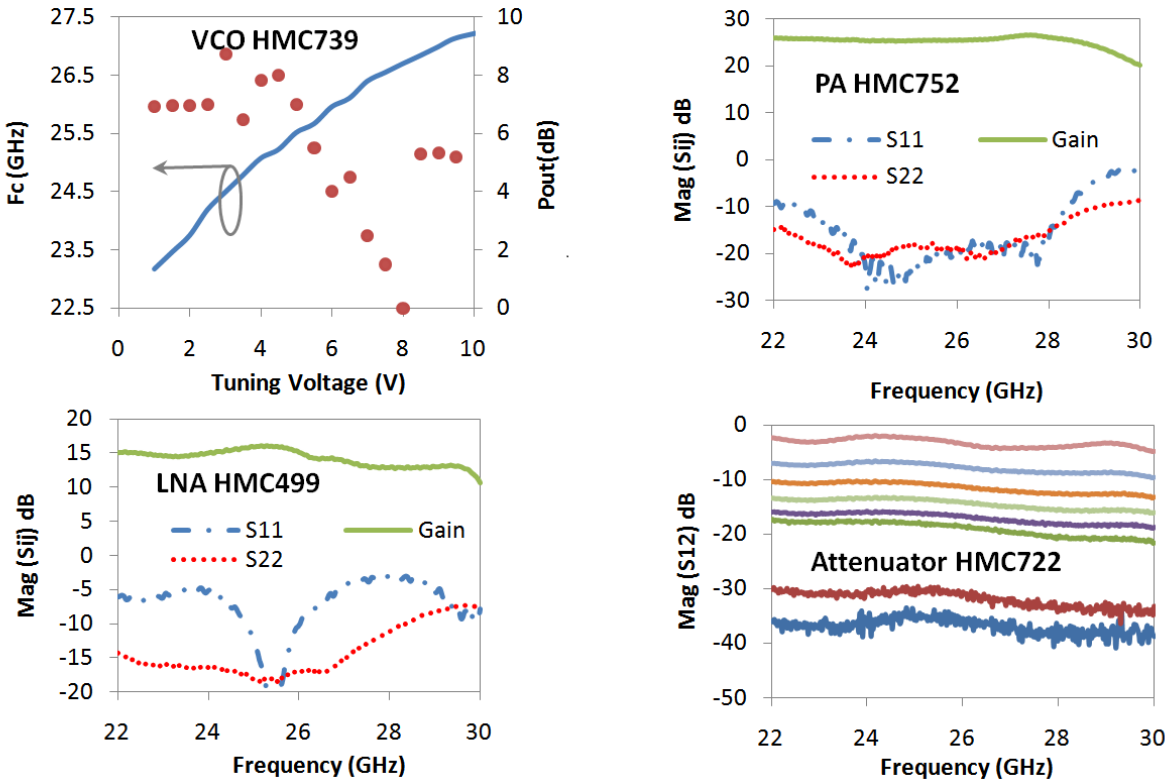


Figure 6.29 Measured S-parameters of active components : (a) VCO HMC739, (b) power amplifier HMC752, (c) low noise amplifier HMC499 and (d) attenuator HMC722.

architecture composed of four couplers has less sensitivity of phase and magnitude balance. An SIW six-port junction is then built in a Rogers substrate and the measurements have a good correlation with the simulations. In the second part of this chapter, an SIW transceiver is introduced by integrating the proposed six-port junction and the phase modulator and frond-end designed in the previous chapters. A serials simulations of the proposed transceiver system are carried out in ADS. The simulations start with ideal models of all devices. Then we replace the ideal models of key devices with the customized models built with the measured data, and the simulation results become more realistic. The concept of the proposed transceiver is verified in an experiment with low data rate data. In this experiment, a modulated signal is generated by the proposed phase modulator and then demodulated by the six-port direct conversion receiver. The recovered base band signal is compared with the original I/Q in an oscilloscope.

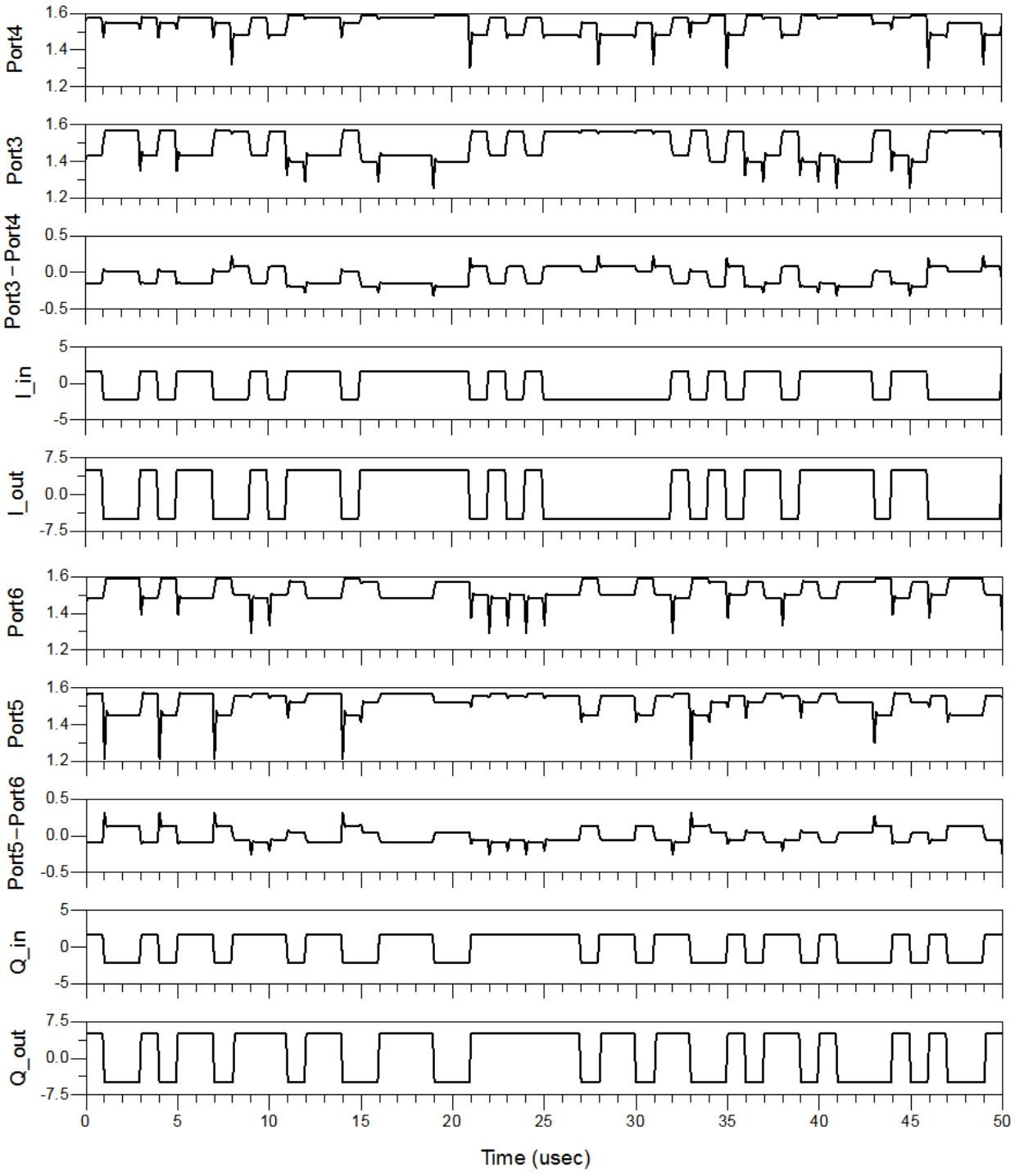


Figure 6.30 Waveform of ADS simulation of SIW transceiver.

CHAPITRE 7

Conclusions and Future Work

The principal scientific and technical contributions of this dissertation are as following :

– Several miniaturization techniques of SIW circuits, such as RSIW, TFSIW and HMSIW, are discussed in order to achieve a high compression ratio. A group of SIW transmission lines based on these miniaturization techniques are analyzed and their propagation constants and quality factors are compared. Various passive devices are designed, fabricated and tested. All measurements are compared with the simulations. The passive designs include :

  * Two six-port junction circuits based on HMSIW technique and integrated on the basis of the developed basic building components.
  * A hybrid ring (rat race coupler) based on TFSIW technique.
  * Two five-port junctions based on TFSIW technique.

– A novel transition between microstrip line and SIW in a multilayer substrate design environment is presented. In order to achieve a broadband response, a transition, consisting of a tapered ridged SIW and a tapered microstrip line, is modeled and designed by considering both impedance matching and field matching. A design guideline is also proposed.

– Several transitions between various miniaturized SIW structures and SIWs in multilayered PCBs are designed and tested.

– A series of waveguide slot antenna arrays are developed and investigated.

  * A 4×4 slot array antenna based on ridge SIW and T-type folded SIW techniques is proposed and an 8.8% bandwidth is achieved. The proposed antenna structure is then fabricated. Measured results are well consistent with simulated ones.
  * A 2×4 T-type folded substrate integrated waveguide (TFSIW) slot array antenna is developed and manufactured. Each linear array is fed through a microstrip line and a TFSIW Y-junction. The size of the proposed antenna is reduced by 40% and the impedance bandwidth (-10 dB) is 5.6%. The dimensions of the structure are presented and the proposed array antenna is fabricated in a two-layer substrate. Simulation and measurement of the proposed antenna are compared.

    * Several feeding networks for a 8×4 ridge SIW slot array antenna is compared. The polarization loss factors of two 8×4 ridge SIW slot array antennas, connected with a SIW diplexer and a low pass filter, respectively, are measured.

– Two design platforms of SIW phase shifter at 26 GHz, namely inline phase shifter and reflection-type phase shifter, are presented, fabricated and tested. Measured results are in good agreement with responses calculated from equivalent models and EM models. An inline phase shifter tuned by a single varactor has a phase shift larger than 25° over a 30% bandwidth. Two phase shifters, which have a maximum phase shift of 180° and 360° respectively, are designed and tested. The 360° phase shifter is performed as a phase modulator with the control voltage generated by the baseband I/Q signals through an analog encoder circuit.

– An SIW six-port is designed for direct conversion receiver. Four-coupler architecture is utilized, considering the impact of the non-ideal terminations to the phase imbalance.

– A series of ADS envelop simulations are performed for an SIW transceiver system which is composed of the proposed SIW phase modulator and six-port direct conversion receiver. A preliminary experiment is conducted.

Based on the conclusions and designs reported in this dissertation, there is some future work can be anticipated for completing the study. Several active devices, such as PA, LNA, power detector and VCO integrated in Figure 6.26, are now implemented with commercial integrated circuits which are surface mounted on the top of other SICs in the system through GCPW. We believe some of them can be implemented within SIW structure and take the advantage of the high Q of SIW resonators. For example, there are already some publications on the design of SIW VCO. Some preliminary investigation of SIW power detector has already been conducted during this dissertation. However the obtained results are not good enough to report here. It is believed that a more dedicated integration approach of SIW and semiconductor devices needs to be developed. Secondly, the architecture of the transceiver system proposed in Figure 6.26 needs to be further improved. Instead of using phase shifter connected in serial as a phase modulator, a parallelly connected six-port junction can probably provide a better performance on DC-offset.

All work in this dissertation is developed based on two aspects, **multilayer** and **miniaturization**. However, limited by the fabrication capability, the number of PCBs used in this work could not go beyond two. With the increasing technical and performance requirement on wireless systems for communication and sensor applications, high-density microwave and millimeter-wave system integration techniques have been under intensive development. Ge-

nerally, a high-performance system involves high-quality analog passive components, active devices and even digital parts. A number of hybrid integrated circuit design concepts have been proposed to enhance the integration at system level, such as system on chip (SoC) solution and system in package (SiP) solution. Compared with the individual-packaged ICs, both SoC solution and SiP solution have prominent advantages, such as small circuit size and volume, excellent system performance, and low fabrication cost. SiP has more flexibility in connection with mixing different fabrication technologies, which has a lower risk for design or redesign ; while SoC provides even a smaller circuit size, a less potential overall cost and a better system performance, especially when the operating frequency goes high into mmW band.

Except exploiting advanced design concepts, in order to reduce the volume and overall cost of an optimized system design, researchers and designers have been looking for more suitable approaches and technologies for the design and fabrication, especially the system requirements become more stringent in mmW applications. Multilayer technology is an attractive approach judging from its high integration density. A number of multilayer technologies have experienced a fast growth in the past decade such as low temperature co-fired ceramic (LTCC), multilayered thin-film, multilayered printed circuit board (PCB), micro-electro-mechanical systems (MEMS) and various silicon-based semiconductor technologies. Among various technologies, complementary metal-oxide-semiconductor (CMOS) technology is one of the most popular technologies in industry because of its prominent compatibility with base-band portion-related logic CMOS and also attractive cost of manufacturing. The scaling of CMOS results in a significant improvement for the RF performance of CMOS devices. The speed of analog CMOS circuits climbs by roughly one order of magnitude every ten years and the time frame for the process node spans by roughly two years per generation. Currently, with 130 nm and 90 nm nodes, it is normal for the operating frequencies of RF and mmW CMOS devices and circuits, such as carrier for transceivers, oscillating frequency of voltage controlled oscillators (VCOs) and operating frequency of amplifiers, approaching at one hundred GHz and above. Especially, after 7 GHz continuous bandwidth was opened for unlicensed use at mmW frequencies around 60 GHz in the U.S. (57 GHz $\sim$ 64GHz) and Japan (59 GHz $\sim$ 66 GHz), mmW CMOS is believed to be a very promising technology in the near future for a variety of applications such as gigabit/s point-to-point links, wireless local area networks (WLANs) with extraordinary capacity, short-range high resolution radars and automotive sensors.

The disadvantages of circuits based on CMOS technology are the interior noise performance, passive component integration, and electrostatic discharge (ESD). When CMOS scales down for RF and mmW applications, these problems will be more pronounced as the ope-

rating frequency goes higher. Since long-time, high-density integrations of high-Q and large-value passive elements have been a bottleneck for the optimized SoC designs for mmW using CMOS technology. There are two solutions for passive integration in IC designs. One is to use on-chip inductors, capacitors and varactors. Quality factors (Q) for both inductors and capacitors are critical parameters in term of the total system loss. To certain extent, the growing number of interconnect layers allows the realization of these passives with higher Q and larger component values. However, with a low-resistivity semiconductor material and the traditional structures for passive components used in CMOS circuits, such as spiral inductor, metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors, more chip space is needed to achieve large component values with a satisfactory Q. Meanwhile, the layout of microstrip-type passive components embedded in semiconductor dies need a careful design to minimize the parasitic resistance and capacitance. Another solution to passive integration in SiP is to place the passive devices in the packaging board. A packaging board, either organic or ceramic, provides interconnections between multiple chips and interface between chip and peripheral devices. Because of the larger form factor as well as material's better RF performance, a higher Q passive at packaging level is a common solution in SiP. However, more interconnections are required between the chip and the passives. New approaches for passive integration are urgently required.

SIW technology can be one of the promising approaches for high-density and high-performance passive integrations. Some special techniques are required for achieving a successful SIW circuit design based on CMOS technique. A high resistivity silicon substrate is to be used in order to decrease the dielectric loss. High density through silicon/wafer via (TSV/TWV) technique provides ideal post-walls for SIW circuits at mmW frequency. Except the requirements to the fabrication process to be investigated, because the SIW circuits have much bigger size compared with conventional planar transmission line circuits and this can greatly increase the cost of mass productions, the SIW miniaturization techniques might be very helpful on reducing the cost of mass productions. SIW passives integrated at chip level can not only provide a higher Q factor but also less interconnection. The integration density is a trade off between SiP and SoC. However, wafer cost is the biggest portion in a RF product. The growth and success of this SIW based passive integration technique is primarily driven by its cost in massive production. 3-dimension (3D) IC is expected to have more than 7% market share in the coming 10 years. As the key technique of 3D IC, TSV technique has already become a research hotspot in both industry and academy. Passive integration based on TSV technique and SIW structure can be a very important topic at that time and all studies of SIWs and SICs based on PCBs nowadays provide a good start point at the emergence of this new technology.

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