View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by PolyPublie

UNIVERSITÉ DE MONTRÉAL

High-Efficiency Low-Voltage Rectifiers for Power Scavenging Systems

SEYED SAEID HASHEMI AGHCHEH BODY

DÉPARTEMENT DE GÉNIE ÉLECTRIQUE

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

THÉSE PRÉSENTÉE EN VUE DE L'OBTENTION

DU DIPLÔME DE PHILOSOPHIAE DOCTOR (PH.D.)

(GÉNIE ÉLECTRIQUE)

AOÛT 2011

© Seyed Saeid Hashemi Aghcheh Body, 2011.

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Cette Thèse intitulée:

High-Efficiency Low-Voltage Rectifiers for Power Scavenging Systems

Présentée par : HASHEMI AGHCHEH BODY Seyed Saeid

en vue de l'obtention du diplôme de : Philosophiae Doctor

a été dûment accepté par le jury d'examen constitué de :

M. AUDET Yves, Ph. D., président

M. SAWAN Mohamad, Ph. D., membre et directeur de recherche

M. SAVARIA Yvon, Ph. D., membre et codirecteur de recherche

M. BRAULT Jean-Jules, Ph. D., membre

M. SHAMS Maitham, Ph. D., membre externe

DEDICATION

Dedicated to my parents

And

To my wife and sons

ACKNOWLEDGEMENTS

My thanks are due, first and foremost, to my supervisor, Professor Mohamad Sawan, for his patient guidance and support during my long journey at École Polytechnique de Montréal. It was both an honor and a privilege to work with him. His many years of circuit design experience in biomedical applications have allowed me to focus on the critical and interesting issues.

I would like to also thank Professor Yvon Savaria, whom I enjoyed the hours of friendly and stimulating technical discussions. His insightful comments, support, and timely advice was instrumental throughout the course of this work. He has been an invaluable source of help for my thesis and all the other submitted papers for publication.

I owe much gratitude to my wife, Mahboubeh, not only for taking care of our children, but also for her love, devotion, support, and patience during these many years, and for believing me every time I said I would graduate the "next year".

My special thanks go to my departed parents, whom I miss so much. They offered me their unconditional love, and encouraged me throughout my studies. I wish they could see this day. May the Great God bless their souls.

I would also like to thank my sons, Hossein, Hamid and Mahdi for not complaining about my absence in many of their life events because to my studies. I specially appreciate Hossein, for listening to my ideas and providing valuable feedback and help.

Last but not least, my special gratitude goes to all fellow students, technicians, and staff of Polystim and GRM, in the past and present, for constructive discussions, friendship, and all the help they offered me over the years. I cannot list their names as they are many but I enjoyed the pleasant atmosphere they created in our research group. I would like to specifically thank Sami Hached, Amine Miled and Mohamed Zgaren for their valuable time helping me in French translation of the summary section of this thesis.

I would like to thank the Natural Science and Engineering Research Council of Canada (NSERC), Canada Research Chair in Smart Medical Devices, and the Canada Research Chair in

Advanced Microelectronics Design for their financial support. I would also like to thank CMC Microsystems for providing access to design tools, technologies, and chip fabrication facilities.

ABSTRACT

Rectifiers are commonly used in electrical energy conversion chains to transform the energy obtained from an AC signal source to a DC level. Conventional bridge and gate cross-coupled rectifier topologies are not sufficiently power efficient, particularly when input amplitudes are low. Depending on their rectifying element, their power efficiency is constrained by either the forward-bias voltage drop of a diode or the threshold voltage of a diode-connected MOS transistor. Advanced passive rectifiers use threshold cancellation techniques to effectively reduce the threshold voltage of MOS diodes. Active rectifiers use active circuits to control the conduction angle of low-loss MOS switches.

In this thesis, an active rectifier with a gate cross-coupled topology is proposed, which replaces the diode-connected MOS transistors of a conventional rectifier with low-loss MOS switches. Using the inherent characteristics of MOS transistors as comparators, dynamic biasing of the bulks of main switches and small pull-up transistors, the proposed self-supplied active rectifier exhibits smaller voltage drop across the main switches leading to a higher power efficiency compared to conventional rectifier structures for a wide range of operating frequencies in the MHz range. Delivery of high load currents is another feature of the proposed rectifier.

Using the bootstrapping technique, single- and double-reservoir based rectifiers are proposed. They present higher power and voltage conversion efficiencies compared to conventional rectifier structures. With a source amplitude of 3.3 V, when compared to the gate cross-coupled topology, the proposed active rectifier offers power and voltage conversion efficiencies improved by up to 10% and 16% respectively. The proposed rectifiers, using the boot strap technique in double- and single-reservoir schemes, are well suited for very low input amplitudes. They present power and voltage conversion efficiencies of 75% and 76% at input amplitude of 1.0V and maintain their high efficiencies over input amplitudes greater than 1.0V. Single-reservoir boot strap rectifier also reduces die area by 70% compared to its double-reservoir counterpart.

Different bulk biasing techniques for the various transistors are proposed. Short auxiliary

paths use the parasitic diffusion-bulk junction of the main pass switches in place of diode-connected pMOS transistors in the auxiliary paths. A flow-back current free scheme is also introduced in which, a smart control circuit selectively regulates the conduction angle of main pass transistors and prevents reverse currents. A close-track scheme using the parasitic diffusion-bulk junction diode of the charging transistor is also proposed. The resulting configuration has a relatively simple structure and produces the best performance among all double-reservoir structures for a wide range of input peak voltages. All the proposed rectifiers were fabricated in a 0.18 μm 6-Metal/2-Poly TSMC 3.3 V standard CMOS process.

RESUMÉ

Les redresseurs sont couramment utilisés dans de nombreux systèmes afin de transformer l'énergie électrique obtenue à partir d'une source alternative en une alimentation continue. Les topologies traditionnelles telles que les ponts de diodes et les redresseurs se servant de transistors à grilles croisées-couplées ne sont pas suffisamment efficaces en terme d'énergie, en particulier pour des signaux à faibles amplitudes. Dépendamment de leur élément de redressement, leur efficacité en termes de consommation d'énergie est limitée soit par la chute de tension de polarisation directe d'une diode, soit par la tension de seuil du transistor MOS. Les redresseurs passifs avancés utilisent une technique de conception pour réduire la tension de seuil des diodes MOS. Les redresseurs actifs utilisent des circuits actifs pour contrôler l'angle de conduction des commutateurs MOS à faible perte.

Dans cette thèse, nous avons proposé un redresseur actif avec une topologie en grille croisée-couplée. Elle utilise des commutateurs MOS à faible perte à la place des transistors MOS connectés en diode comme redresseurs. Le circuit proposé utilise: des caractéristiques intrinsèques des transistors MOS pour les montages comparateurs et une polarisation dynamique des substrats des commutateurs principaux supportés par de petits transistors de rappel. Le redresseur proposé présente de faibles chutes de tension à travers le commutateur principal menant à une efficacité de puissance plus élevée par rapport aux structures d'un redresseur conventionnel pour une large gamme de fréquences de fonctionnement de l'ordre des MHz. La conduction des courants de charge élevée est une autre caractéristique du redresseur proposé.

En utilisant la méthode de *bootstrap*, des redresseurs à simple et à double réservoir sont proposés. Ils présentent une efficacité de puissance et un rapport de conversion de tension élevés en comparaison avec les structures des redresseurs conventionnels. Avec une amplitude de source de 3,3 V, le redresseur proposé offre des efficacités de puissance et de conversion de tension améliorées par rapport au circuit à transistors croisés couplés. Ces améliorations atteignent 10% et 16% respectivement. Les redresseurs proposés utilisent la technique de *bootstrap*. Ils sont bien adaptés pour des amplitudes d'entrée très basses. À une amplitude

d'entrée de 1,0 V, ces derniers redresseurs présentent des rendements de conversion de puissance et de tension de 75% et 76%. Le redresseur à simple réservoir réduit également l'aire de silicium requise de 70% par rapport à la version à double-réservoir.

Ajoutons que différentes techniques de polarisation du substrat pour les divers transistors sont également suggérées. Des chemins auxiliaires courts utilisent la diffusion parasite au niveau des jonctions des deux transistors commutateurs de passage principaux à la place des transistors pMOS connectés en diode dans ces chemins. Un chemin de retour du courant est également introduit. Ce chemin exploite un circuit de commande intelligent qui régule de manière sélective l'angle de conduction des transistors de passage principaux et qui bloque les courants inverses. Aussi, un circuit réalisé à l'aide d'une diode de diffusion à jonction parasite du transistor de charge est également proposé. La configuration qui en résulte a une structure relativement simple et elle affiche la meilleure performance parmi toutes les structures à réservoir double pour une large gamme de signaux de tension d'entrée. Tous les redresseurs proposés ont été simulés, implémentés et fabriqués avec la technologie CMOS 0.18 µm 3.3V CMOS de Taiwan Semiconductor Manufacturing Company (TSMC).

CONDENSÉ EN FRANÇAIS

1. Introduction

Les avancées technologiques dans le domaine des communications sans fil ont mené au développement des circuits intégrés à faible voltage et à basse consommation de puissance. Ces derniers sont nécessaires au bon fonctionnement et à l'atteinte des performances désirées dans les systèmes embarqués. Parmi les classes de systèmes qui nous intéressent, on peut citer les réseaux de capteurs [4,30,37], les étiquettes d'identification par radio fréquence (RFID) [11,134] et les dispositifs biomédicaux intelligents [57,81]. Plusieurs techniques d'alimentation incluant les batteries embarquées et les transmissions transcutanées sont relativement limitées en densité d'énergie, durée de vie, risque potentiel, intégration et en dimensions physiques.

D'un autre coté, les techniques de récupération d'énergie sont des procédés qui permettent de récupérer l'énergie disponible dans l'environnement (incluant le corps humain) et de la convertir en énergie électrique exploitable. Plusieurs travaux dédiés au développement de ces techniques montrent qu'elles peuvent être peu coûteuses, hautement intégrable et capables d'afficher des niveaux de puissance élevés. Néanmoins, ces techniques ne sont pas encore considérées fiables et réalisables, bien que la recherche est en constante progression [41,155]. Ainsi, fournir l'énergie nécessaire et suffisante pour alimenter les implants électroniques demeure un défi.

La plupart des sources d'énergie, y compris les circuits à alimentation par induction et les systèmes autoalimentés grâce aux techniques de récupérations d'énergie sont de sources alternatives (AC) et doivent être converties en sources continues (DC). On a aussi rapporté que les liens à couplage inductif souffrent d'une faible efficacité de transfert de puissance due au mauvais couplage et à une bande passante étroite. Il est donc crucial d'utiliser un redresseur à haute efficacité à l'interface du système de transmission de puissance.

Dans une structure de redresseur alimenté par liaison inductive, les transistors MOS qui partagent le même substrat et dont les sources sont connectées à la bobine secondaire, sont sujets

à de grandes variations de tension. Par conséquent, cela peut induire d'importants courants de fuite au niveau du substrat, ce qui mène à une situation qui peut provoquer de *latch-up* dans un circuit intégré alimenté par un lien inductif. Ce phénomène pourrait entraver l'efficacité de puissance du circuit et compromettre sa fiabilité. Par conséquent, la tension de seuil des transistors principaux MOS doit être contrôlée avec précision et les polarisations fixes [54,119] ou les techniques de commutation dynamique du substrat (DBS) [16-20] sont à considérer. Ces dernières (DBS) réduisent aussi l'effet du substrat sur les transistors MOS de rectification.

1.1 Implémentation des diodes

Une des parties essentielles d'un redresseur de puissance est l'élément de redressement, appelé aussi diode qui fournit un chemin unidirectionnel pour le courant circulant de la source vers la charge. Toutefois, dans certains procédés CMOS standard, il est impossible d'intégrer des diodes avec d'autres composants. Par conséquent, les diodes sont couramment implémentées en utilisant soit des diodes parasites d'une jonction P-N, ou des transistors connectés en diode. Ils sont tous deux limités par la chute de tension intrinsèque d'une diode ou par la chute de tension directe du transistor (0.4-0.6 V). Les transistors MOS connectés en diode (grâce à la courte connexion entre leur grille et leur drain) opèrent dans la région de saturation, ce qui entraîne une consommation d'énergie élevée.

Par ailleurs, dans les redresseurs à base de transistors connectés en diode, V_{GS} est modulée par V_{DS}. Pour les tensions autour de la tension de seuil (V_{Th}), ce paramètre change légèrement d'une conduction directe en conduction inverse. Par conséquent, les commutateurs sont lents et ne peuvent être activés et désactivés complètement. Ceci assujetti la structure à de fuites importantes, ce qui conduit à une faible efficacité de rectification.

La chute de tension dans un MOS connecté en diode dépend de la tension de seuil et de la surtension sur la grille nécessaire pour la circulation du courant. La chute de tension provoque une importante perte de puissance au sein du redresseur, qui affecte l'efficacité globale de puissance et diminue la tension délivrée aux modules précédents. D'autre part, l'usage des diodes Schottky à chute de tension faible (0.3 V) est possible [92,108,174] mais leur

implémentation est coûteuse, en raison des étapes de fabrication supplémentaires nécessaires et qui ne sont pas disponibles dans les procédés CMOS standard.

1.2 Performances et classification des redresseurs

Il y a de nombreux paramètres, tels que : l'efficacité de conversion de puissance (PCE), le rapport de conversion de tension (VCR), la tension moyenne de sortie (DC), la tension d'entrée minimale, et le courant moyen de charge qui peuvent être utilisés pour la caractérisation des redresseurs. Le PCE est défini comme le rapport de la puissance moyenne de sortie sur la puissance RF d'entrée. Le VCR est défini comme étant le rapport de la tension moyenne (DC) de sortie sur l'amplitude crête à l'entrée. La tension d'entrée minimale est la tension minimale qui pourrait être détectée par le redresseur. Ces tensions maximales et minimales déterminent la plage dynamique du redresseur.

Les redresseurs de puissance sont classés selon la méthode avec laquelle la diode est implémentée. Les circuits redresseurs utilisant des composants passifs comme diode ou les transistors MOS connectés en diode sont appelés redresseurs passifs. Les redresseurs actifs sont une autre catégorie de redresseurs dans lesquels la diode est implémentée en utilisant des diodes actives, principalement composée de commutateurs MOS, de comparateurs et de circuits périphériques. Récemment, les redresseurs passif-actif ont également été introduits où le redresseur utilise une configuration à multi-étage, combinée de phases actives et passives.

2. Les redresseurs passifs à structures conventionnels

Les redresseurs demie-onde ne sont pas assez efficaces et leurs performances en termes de PCE et VCR sont limitées par une chute de tension dans les diodes. Les redresseurs en pont sont la version populaire des redresseurs pleine onde, où l'arrangement est constitué de quatre diodes (Figure 2.2). Une paire de diodes est responsable de la rectification dans chaque cycle du signal. Lorsque la tension d'entrée est supérieure à la tension de sortie, une diode est conductrice, ce qui permet de délivrer de la puissance à la charge. Dans ce cas l'autre diode régit le chemin du courant de la charge à la masse. Bien que la structure, par rapport à un pont

de demie-onde, bénéficie d'une efficacité de puissance plus élevée, de plus petites ondulations de sortie et d'une tension de claquage inverse plus élevée [1,83]. Elle souffre cependant d'une chute de tension de deux diodes en cascade à chaque cycle du signal.

2.1 Les rectificateurs passifs à grille partiellement croisée-couplée

Les rectificateurs passifs à grille partiellement croisée-couplée (PGCCR) utilisent dans leur configuration une seule paire de transistors MOS à couplage croisé (Figure 2.4) [60,126]. Dans chaque cycle du signal de ce circuit, le V_{Th} d'un transistor MOS connecté en diode, est remplacé par la chute de tension efficace à travers un interrupteur MOS. Par rapport à un transistor connecté en diode, la chute de tension d'un interrupteur MOS dans la région triode, est négligeable. Cela réduit effectivement la chute de tension dans le redresseur à un seul V_{Th} par opposition aux configurations basées sur la chute de tension de deux transistors connectés en diode. L'autre avantage de ce redresseur est de commander la grille du transistor MOS avec une plage de tension plus élevée que celle des structures des transistors montés en diodes, ce qui réduit les fuites provoquées par les commutateurs et améliore leur conductivité. Le redresseur résultant affiche une plus grande efficacité de puissance comparée aux structures conventionnelles (FWDR), cependant, à chaque cycle de la source, il utilise les transistors MOS connectés en diode pour les connexions de charge et souffre donc de chutes de tension associées.

Comme les sources de tous les transistors MOS de rectification dans la structure PGCCR sont connectés aux bornes d'entrée, ils subissent de grandes variations de tension se produisant à haute fréquence. La protection de ce circuit contre le *latch-up* et les courants de fuite au niveau du substrat est cruciale. La technique de commutation dynamique du substrat (DBS) est utilisée avantageusement pour polariser dynamiquement les substrats des transistors [16-20].

2.2 La topologie à grille complètement croisé-couplée

Le problème associé à la tension de seuil de n' importe quel transistor MOS connecté en

diode suivant une configuration PGCCR est surmonté avec l'utilisation de l'architecture à grille complètement croisé-couplée (FGCCR), où chaque paire de commutateurs MOS dans la topologie de type pont est connectée en croisé (Figure 4.1b) [13,44,111]. En topologie FGCCR, les transistors MOS agissent comme des commutateurs et le circuit n'est donc plus limité par la tension de seuil des transistors MOS connectés en diode, mais plutôt par la chute de tension drain source des interrupteurs.

Cependant, à chaque cycle, il existe une période où le potentiel du nœud de sortie est supérieur à celui du nœud d'entrée pour une durée considérable. Lorsque cela arrive, les paires croisées couplées ne peuvent pas être complètement désactivées, provoquant ainsi une fuite de charge du condensateur de sortie du à la source d'entrée. La fuite de charge dégrade alors l'efficacité de puissance. En outre, le circuit redresseur n'a pas une tension d'alimentation stable qui peut garantir le plus haut potentiel dans le système. Par conséquent, si les substrats du pMOS sont statiquement liés à des potentiels fixes, la diode entre la source et le substrat (ou drain et substrat) du transistor peut être polarisée directement.

2.3 Les redresseurs à base de pompe à charge

Les circuits typiques de pompe de charge AC-DC utilisés dans les systèmes de collecte de puissance et dans les circuits RFID se composent de plusieurs cellules de redresseur dans une configuration en cascade [40,83,163,177]. La pompe de charge de Greinacher (Figure 2.6) est souvent utilisée comme cellule de redresseur, qui se compose de diodes et de condensateurs afin de transférer des quantités de charge à travers les commutateurs cadencés de la source vers le condensateur de réservoir à la sortie. Cependant, la puissance de sortie de cette famille de redresseurs est souvent limitée à de faibles niveaux en raison des contraintes imposées pour la quantité des charges transférées et la taille du condensateur de sortie [173-174]. Aussi, ces redresseurs souffrent généralement de grandes ondulations à la sortie. Cela les rend incompatibles avec les applications où un courant élevé de charge et/ou une tension de sortie stable est nécessaire.

Les redresseurs de pompes de charges à multi-étages (Figure 2.8) sont souvent utilisés pour générer des tensions DC assez élevées à partir des faibles amplitudes d'entrée [39,86,108,173]. Dans cette configuration, les entrées RF sont alimentées en parallèle dans chaque étage grâce à des condensateurs de pompage. Les tensions de sorties sont additionnées en série, afin de produire la tension de sortie finale. Cependant, comparé aux structures à un seul étage, l'efficacité globale de puissance et l'impédance d'entrée de l'étage subit une réduction.

Le problème commun associé aux redresseurs basés sur les multiplicateurs de tension est qu'ils fournissent du courant au nœud de sortie pendant le demi-cycle positif de l'entrée (phase de transfert de charge). Au cours du demi-cycle négatif (phase de *clamping*), la diode en parallèle aide à la pré-décharge de la capacité de stockage vers la masse. Ce phénomène réduit l'efficacité globale de conversion de puissance (PCE) de ces types de redresseurs [137].

Les redresseurs à pompe de charge avancée basés sur des commutateurs MOS à seuil dynamiques (DTMOS) [166], ou sur des diodes de puissance ultra-faible (ULPD) (Figure 2.12b) [58,142] sont mises en œuvre à travers le processus Silicium-sur-Isolant (SOI). Le redresseur de type commutateur seulement [137] et ses versions avancées, à polarisation inversée (*bias-flip*) [137-138], et à résonnance [22,64,110,141,159] sont également introduites**.** Ils se composent d'un commutateur et d'une bobine qui sont connectés à travers la source d'entrée pilotant un redresseur en pont. On a rapporté que ces nouvelles configurations présentent une efficacité de puissance nettement supérieure à celle des redresseurs en pont conventionnel ou au doubleur de tension. Cependant, leur application est limitée par la disponibilité du procédé SOI, par une fréquence d'opération très basse et par la nécessité d'utiliser de grandes inductances.

3. Les techniques d'annulation de seuil

La tension de seuil est un paramètre dépendant du processus, qui dépend du choix de l'oxyde et de son épaisseur. La tension de seuil des principaux commutateurs MOS entraîne une dissipation de puissance constante au sein du redresseur et diminue la tension moyenne de sortie (DC). L'effet du substrat aggrave la situation en imposant son effet délétère sur la tension de

seuil. L'utilisation de transistors à faible seuil, disponibles dans certains procédés CMOS avancés, peut sembler être une solution prometteuse au problème. Cependant, leur disponibilité n'est pas encore généralisée et les dispositifs implémentés sont soumis à des fuites significatives à cause du grand dopage du canal menant à une consommation de puissance excessive et à des problèmes de fiabilité.

Il existe d'autres solutions qui emploient différentes techniques de circuits pour atténuer l'impact de la tension de seuil des transistors MOS.

3.1 La technique de la grille flottante

La technique de la grille flottante (FG) a été suggérée pour réduire de façon passive la tension de seuil des transistors MOS en injectant quelques charges dans la couche d'oxyde de la grille du transistor [23,100]. La charge programmée est emprisonnée pour des années sur la grille flottante et complètement isolée (environ 0.1% en 10 ans @ 100C °). Cette technique a été appliquée aux commutateurs MOS à grille crroisée partiellement et entièrement couplée [111,128] et aux topologies de redresseurs à base de pompe de charge [100].

En général, les compromis des redresseurs à grille flottante compromettent la tension de seuil du transistor avec une augmentation de la capacité d'entrée. La grille flottante doit être programmée au moins une fois, pour tenir compte de charges résiduelles inconnues accumulées aux grilles flottantes de transistors après la fabrication de circuit intégré (effet d'antenne) [16,100]. Par ailleurs, le processus de programmation est lent, requiert souvent des tensions élevées fournies hors-puce, et présente un impact potentiel sur la fiabilité des circuits [42,111]. D'autre part, la performance du circuit redresseur peut diminuer légèrement avec la fuite de charges de la grille flottante et avec le changement de la température et du temps [16,100].

3.2 Techniques d'annulation statique du seuil

Avec ces techniques, une tension DC statique est générée durant une phase de repos du circuit pour être utilisée comme tension de polarisation à tout moment, indépendamment

de l'amplitude instantanée du signal d'entrée RF et a fin d'éliminer ou de réduire l'effet de la tension de seuil des dispositifs MOS sur la phase de travail. La tension DC statique peut être générée à partir des sources internes ou externes. Par conséquent, les différentes techniques, y compris l'élimination externe de V_{Th} (EVC) (Figure 2.9) [161] et l'élimination interne de V_{Th} (IVC) (Figure 2.10 et 2.11) [121,169,175,178] sont introduits. D'autre part, ces techniques de polarisation peuvent être appliquées sur les connexions grille et drain [161] ou substrat et source (effet du substrat) des transistors connectés en diode. Malheureusement, toutes les techniques citées consomment beaucoup d'énergie. Néanmoins, la réalisation d'une réduction simultanée de la résistance du canal (R_{ON}) et du courant de fuite inverse pour les commutateurs MOS n'est pas possible [92].

3.3 Technique de courant commandé par le substrat

La technique de courant commandé par le substrat utilise un courant constant forcé de la connexion au substrat du transistor MOS, afin d'abaisser sa tension de seuil [103]. En utilisant cette technique, la contrainte de tension possible, la consommation de puissance accrue et le couplage du bruit associé à une pompe de charge sont à éviter. De plus, la mise en œuvre de cette technique exige de grands efforts au niveau de l'élaboration du circuit et du dessin des masques.

3.4 Technique de condensateur de *bootstrap*

Une autre technique permet la réduction du seuil en utilisant des condensateurs *bootstrap* [79-80,118]. Avec cette technique, la tension de seuil effective d'un transistor MOS connectée en diode est réduite à la différence entre deux tensions de seuil (Figure 2.14) [99]. Parmi les techniques actuellement connues, c'est la mieux adaptée aux procédés standards CMOS avancés, dans lesquels l'implémentation des condensateurs intégrés est faisable.

Avec une tension de seuil du transistor MOS classique, l'utilisation de cette technique pourrait entraîner une augmentation de la plage de tension de sortie pour une source de tension d'entrée donnée. Cette technique a été appliquée à une configuration classique de

redresseur demi-onde construite en utilisant une structure doubleur de tension [99]; cependant, la structure n'a pas affiché les améliorations de performance attendues.

4. Redresseurs de puissance actifs (synchrones)

Les redresseurs de puissance actifs (synchrones) se basent sur la diode active, à la place de diodes ou transistors connectés en diode, pour atteindre des performances élevées (Figures 2.15 ou 4.1). Les diodes activent fonctionne presque comme une diode idéale, avec une chute de tension négligeable (généralement aux alentours de 20 mV) en conduction directe et un blocage de courant inverse presque parfait. La diode active se compose généralement de commutateurs, des comparateurs, et dans certains cas de rétroactions**.** Lorsque la tension d'entrée du redresseur est supérieure à sa tension de sortie, la sortie du comparateur passe au rail d'alimentation positive et active le commutateur pour permettre la recharge du condensateur de sortie. Inversement, lorsque la tension d'entrée du redresseur synchrone est inférieure à la tension de sortie, la sortie du comparateur passe au niveau bas, le commutateur est désactivé et le circuit de la conduction directe est déconnecté. En comparaison avec les structures de redresseurs passifs, le fait d'appliquer une tension d'entraînement de grille plus élevée sur la base du transistor permet d'améliorer la conductivité du commutateur et l'efficacité de puissance en conséquence.

Généralement, les redresseurs actifs, comparativement aux redresseurs passifs, offrent une commutation ON/OFF plus rapide, utilisent une tension d'entraînement de grille plus élevée améliorant la conductivité des commutateurs, et permettent de réduire les fuites. Par conséquent, ils sont considérablement plus efficaces que leur homologue, en termes de tension de sortie et d'efficacité énergétique [21,97,104,130] pour des fréquences d'utilisation faibles et moyennes. Cependant, cet avantage est obtenu au prix de pertes statiques et de commutation. Les pertes statiques sont dues à l'état statique des circuits actifs, tandis que les pertes de commutation sont principalement associées aux grandes capacités parasites du commutateur.

Le nombre, la structure et les caractéristiques (retard intrinsèque, la consommation de puissance, vitesse, tension d'alimentation) des comparateurs pourraient affecter considérablement les performances du redresseur en termes de courant de fuite inverse, la consommation de

puissance, la génération du courant de charge, la fréquence d'opération, l'ondulation de sortie, et l'efficacité de puissance. Généralement, un comparateur rapide dont la courbe d'hystérésis à faible consommation d'énergie est utilisée et d'autres caractéristiques telles que le gain unitaire de la bande passante, le gain en boucle ouverte et le temps de montée sont adaptés dépendamment de l'application. L'utilisation des boucles de rétroactions avec le comparateur sont également utilisées afin d'améliorer les performances (stabilité), ou introduire une tension arbitraire de décalage à leurs entrées [97]. Néanmoins, si ces pertes sont excessives, la réduction de la chute de tension de la diode devient obsolète. Ainsi, les redresseurs actifs sont principalement mis en œuvre pour les applications dont les fréquences de fonctionnement sont relativement faibles et les plages de tension d'entrée sont supérieures à 1.5 V [128-129].

D'autres inconvénients associés aux redresseurs actifs sont le nombre élevé de composants et la complexité de conception. En général, des conceptions plus complexes comprenant plusieurs composants ont une consommation élevée de puissance et de grande surface.

Les redresseurs actifs utilisent soit l'alimentation d'appoint ou de la tension non régulée et déformée due au condensateur de sortie, pour alimenter leurs circuits actifs. Les redresseurs actifs autoalimentés utilisent soit un circuit de démarrage ou un chemin auxiliaire de chargement pour leur démarrage. Dans ce dernier cas, un transistor MOS connecté en diode permet de charger le condensateur de sortie à partir de la source.

4.1 Architectures actives classiques

Le concept d'utilisation des diodes actives, pour remplacer les diodes classiques dans les redresseurs passifs, pourrait être appliqué à toutes les structures passives. Il comprend un pont classique [149-150], des structures qui utilisent partiellement ou entièrement la grille croisée-couplée (Figures 2.16, 2.17 et 2.18) [47,56,63,97,104,144], ainsi que des architectures basées sur des pompes de charges (Figure 2.19) [80,113,152].

4.2 Redresseurs actifs avancés

Les redresseurs actifs avancés utilisent des comparateurs *phase-lead* [16-19] ou prédictifs

[87] pour améliorer les performances du comparateur et compenser son délai intrinsèque. Bien que ces techniques sont destinées à améliorer significativement la PCE du redresseur, les deux approches sont limitées par la complexité du circuit de temporisation et celle du système de surveillance de tension de sortie, ainsi que par leur sensibilité aux paramètres de conception.

Les redresseurs actifs basés sur une résonnance pulsée sont introduits pour être utilisés avec des générateurs d'alimentation, ce qui rend leurs performances considérablement limitées par l'impédance capacitive interne [123,171-172]. Dans cette topologie, la commutation se produit à très basses fréquences (10 Hz à 1 kHz), afin de réduire les pertes de commutation. L'efficacité de puissance du redresseur est signalée être significativement plus élevée que celle de circuits classiques actifs, mais au prix d'utiliser une inductance élevée.

5. Les structures de redresseurs de puissance actif-passif

Il y a des topologies de redresseurs où les étages actifs et passifs sont utilisées [105,127,130-133]. Le redresseur se compose de deux étages (Figure 2.20). Le premier étage est un circuit complètement passif et utilisé pour convertir la moitié négative de l'onde sinusoïdale, reçue à l'entrée, en une onde positive avec presque pas de chute de tension. Cette conversion est faite avec seulement quatre transistors CMOS standard et sans consommation importante de courant. La chute de tension dans cet étage est également limitée à la chute de tension drain-source des deux commutateurs MOS. Le deuxième étage est une diode active, y compris le commutateur MOS commandé par un comparateur qui utilise la connexion de substrat comme entrée, un biais de bêta-multiplicateur et un chemin auxiliaire pour le démarrage. Le redresseur expose une efficacité de tension et de puissance significativement plus élevé, par rapport aux solutions passives.

6. Contributions

6.1 Un redresseur actif

Pour améliorer l'efficacité de la conversion de puissance (PCE) et augmenter la tension de

sortie, nous proposons un nouveau redresseur actif pleine-onde (FWAR) dans lequel les commutateurs MOS remplacent toutes les diodes ou les MOS connectées en diode dans un redresseur de type pont conventionnel (FWBR) ou un redresseur en croisé-couplé (GCCR) structures (Figure 3.4) [71]. Le redresseur utilise des transistors de pMOS en forme de la grille croisée-couplée avec des transistors nMOS jouant le rôle de commutateurs à faible perte dans leur région triode, où ils peuvent présenter une chute de tension très faible à travers leur terminaux drain-source. Les tensions les plus élevées disponibles dans le circuit sont appliquées de manière dynamique aux commutateurs à transistors afin de maximiser leur transconductance et minimiser, par conséquent, leur résistance de canal. Ainsi, ils n'introduisent pas de chute de tension à cause de V_{Th} dans le chemin direct de la source à charge. Les fuites à travers le substrat sont également minimisées par la polarisation dynamique de N-puits de pMOS avec la tension la plus élevée possible. Le design ne nécessite ni une source d'énergie interne, ni un chemin de signal auxiliaire pour la livraison de puissance au démarrage.

Le circuit proposé utilise un système à schéma double de contrôle symétrique pour les cycles positifs et négatifs. Il fonctionne de sorte que, pour chaque cycle d'entrée et sous des conditions adéquates de source et de charge (Tableau 3.1), une paire de transistors en chemin principal conduit. La conduction simultanée des commutateurs ferme le chemin du courant, de la source vers la charge, et charge le condensateur de sortie. Les transistors pMOS de *pull-up* sont également utilisés pour aider à prévenir les grilles flottantes. Les courants de fuite et court-circuits sont également évités. En choisissant des transistors relativement plus larges que le minimum, on a, en partie, pu fournir un bon «timing» et optimiser des performances.

Le projet de redresseur actif pleine-onde a été soigneusement aménagé pour avoir une structure symétrique minimisant un déséquilibre potentiel dans les capacités parasites entre les connexions d'entrée. Il a été fabriqué en technologie 0.18 µm 6-Métal/2-Poly TSMC 3.3V CMOS (Figure 3.11). La puce mesure une superficie de 1594×1080 μm^2.

Basé sur les résultats de simulations, le redresseur actif à pleine-onde **(**FWAR) produit des tensions de sortie, des efficacités de puissance et des VCR sensiblement plus élevés en comparaison avec un redresseur en diode de type pont et redresseur à grille croisée-couplée

(GCCR) (Figures 3.8, 3.9 et 3.10). Les résultats de simulation confirment que la nouvelle structure est capable de générer des courants de charge élevés avec une petite dégradation de l'efficacité de puissance.

Pour mesurer les performances du redresseur, une plateforme a été développée (Figure 3.12) se servant d'un transformateur d'isolement (1:1) qui est utilisé pour découpler l'oscilloscope de la masse commune. Cette isolation permet d'éviter les boucles de terre dans l'installation et permet de référencer le signal de sortie à des tensions autre que la terre. Les tensions d'entrée et de sortie ainsi que le courant ont été mesurés pour calculer le PCE et le VCR. A partir des mesures, en accord étroit avec les résultats de la simulation, le redresseur proposé offre des tensions de sortie, une efficacité de tension et de puissance, remarquablement élevés par rapport à des structures FWBR et GCCR lorsqu'ils sont utilisés dans des applications à basse tension et courant élevé.

6.2 Redresseur de *bootstrap* à double-réservoir

Nous proposons aussi un redresseur intégré pleine-onde (FWNR), ce qui est approprié pour de nombreuses applications y compris les implants intelligents biomédicaux et des étiquettes RFID (Figure 4.3a). La structure ne nécessite pas des techniques complexes de conception de circuits. Il bénéficie des avantages de la structure à la grille croisée-couplée utilisée sur des transistors MOS sélectionnés.

Il intègre également une paire d'interrupteurs pMOS avec une tension efficace de seuil très basse pour remplacer les diodes ou transistors pMOS connectés en diode dans les structures précédemment citées. Une combinaison de transistors pMOS connectés en diode avec le petit condensateur de *bootstrap* fournit la polarisation qui réduit la tension effective de seuil du transistor principal. Par conséquent, le redresseur est constitué de deux circuits pour la réduction du seuil, chacun contrôle l'un des interrupteurs principaux. Un autre avantage de la nouvelle architecture est sa compatibilité avec les procédés CMOS standard, qui permet l'intégration des gros condensateurs sur la puce. L'architecture utilise la technique de commutation dynamique de substrat (DBS) pour polariser les substrats des transistors sélectionnés (Figure 4.3b), afin de réduire les fuites de courant à travers le substrat et d'éliminer l'effet de substrat.

Il a été constaté que l'application de la technique DBS aux substrats de transistors principaux réduit de manière significative l'efficacité globale de puissance du redresseur. Par conséquent, les substrats de transistors principaux étaient reliés à V_{Out} ainsi que la plus haute tension disponible pendant la majorité du temps de fonctionnement du redresseur en raison de la présence du réservoir de sortie.

Le redresseur modifié fonctionne comme un redresseur à la grille croisée-couplée. Pendant chaque cycle d'entrée, une branche du circuit (chemin auxiliaire) qui comprend le transistor pMOS connectés en diode est insérée pour fournir un chemin entre l'entrée et la sortie pour charger le condensateur *bootstrap*. Cependant, la conduction simultanée des transistors pMOS dans les chemins principaux et auxiliaires contribue au courant de sortie.

Les résultats obtenus à partir des simulations (Figures 4.4 et 4.5) montrent que le PCE et le VCR pour la structure proposée (FWNR) permettent d'atteindre rapidement des valeurs élevées pour des amplitudes de source très faible, et reste nettement plus élevé pour les tensions d'entrée plus large, par rapport aux structures de redresseur en pont classique (FWBR) et de la gille croisée-couplée (FWGR). Il a également été montré dans [70] que la tension de sortie moyenne de FWNR est significativement plus élevée que celle des autres topologies. Par conséquent, on peut s'attendre à ce que le nouveau circuit puisse être applicable à la mise en œuvre de redresseurs à l'aide de nouvelles technologies CMOS submicroniques où la tension d'alimentation nominale est inférieure à 1 V. Il a été noté que, comme prévu, les fréquences élevées de la source produisent de plus grandes PCE et de tension moyenne de sortie, dont il en résulte des grandes VCR (Figure 4.9). Diverses simulations montrent que la nouvelle topologie du redresseur peut fonctionner sur une large gamme de fréquences jusqu'à 60 MHz à condition de faire les optimisations adéquates.

Le PCE et le VCR pour la structure FWNR varient avec la taille du condensateur d'amorçage (Figure 4.6). Toutefois, sur une large gamme de capacité, la performance du redresseur n'est pas très dépendante de la taille des condensateurs intégrés. Les résultats confirment que le nouveau redresseur fonctionne très bien avec un condensateur de 50 pF qui sont réalisables avec les procédés CMOS standard.

Le projet de redresseur pleine-onde (FWNR) a été soigneusement aménagé pour avoir une structure symétrique minimisant le déséquilibre du potentiel dans les capacités parasites entre les connexions de source et fabriqué en utilisant la procédé CMOS standard 0.18 µm 6-Métal/2-Poly TSMC 3.3V (Figure 4.7). Cette puce mesure 780 µm×780 µm et elle possède 40 broches à double rangée. Les substrats locaux, nécessaires pour utiliser la technique DBS, ont été mis en œuvre en utilisant la couche «d*eep n-well*. Tous les commutateurs principaux sont entourés par des anneaux de protection pour les isoler des cellules adjacentes.

Basé sur des observations distinctes, les mesures confirment que l'efficacité de puissance diminue avec le courant de charge. Le redresseur proposé génère une meilleure tension de sortie et une meilleure efficacité de puissance par rapport aux résultats rapportés par d'autres travaux en particulier lors du fonctionnement à partir de tensions de sources faibles. Le redresseur proposé, même avec des éléments mis en œuvre en utilisant la technologie d' intégration CMOS sous-micronique, est capable de supporter des courants de charge importants allant jusqu'à quelques mA.

6.3. Redresseurs de *bootstrap* à double-réservoir améliorées

Des améliorations s'appliquant à un redresseur intégré de pleine onde à double-réservoir (DRR-1) sont présentées [75]. Elles améliorent considérablement ses performances en termes d'efficacité de conversion de puissance et de tension en réduisant le courant de retour de fuite tout en éliminant les chemins auxiliaires.

6.3.1 Court chemin auxiliaire

Un court chemin auxiliaire, proposé pour la structure de la DRR-1 où les parasites de la jonction P-N de diffusion-substrat des commutateurs du chemin principal, est utilisé pour remplacer les transistors pMOS connectés en diode dans les chemins auxiliaires (DRR-2). La configuration proposée sert simultanément à polariser le substrat des commutateurs du passage principal, tout en fournissant des pistes auxiliaires de l'entrée au condensateur *bootstrap* (Figure 5.1c). Il est réalisé par la connexion du terminal du substrat des transistors du passage principal à V_{Out}. Il est à noter que le substrat du transistor pMOS dans les chemins de la charge est

toujours polarisé en utilisant la technique DBS.

Basé sur les résultats des simulations du schématique avec des conditions sur la charge appliquée, le redresseur proposé (DRR-2) présente une PCE et VCR significativement plus élevés que le DRR-1 (Figures 5.2 et 5.3). Les améliorations augmentent significativement pour les sources ayant des amplitudes plus élevées. On a également observé que le temps d'établissement du circuit de DRR-2 est plus courte que celle de la DRR-1.

6.3.2 Les redresseurs sans courant de retour

Pendant le fonctionnement normal d'une structure de la DRR, la tension d'entrée à la chaîne de conversion de puissance et la tension de sortie varient dans le temps. Par conséquent, il existe des intervalles de temps, durant lesquels le flux de courant s'inverse dans les transistors pMOS principaux. Dans la structure utilisée avec des conditions variables sur la source et la charge, ce courant de retour peut considérablement dégrader les performances du redresseur d'un point de vue efficacité de puissance.

6.3.3. Système de contrôle pour limiter le flux de courant de retour

Pour résoudre le problème ci-dessus, nous proposons d'utiliser soit un système de contrôle (Figure 5.4) ou bien polariser les substrats des transistors de charge (Figure 5.6b). Dans le cas de la première solution, chaque transistor du passage principal est équipé du circuit de commande proposé (DRR-3). Dans une structure DRR-3, lors de chaque cycle d'entrée, ce circuit de commande compare en permanence les tensions d'entrées et sortie, et connecte la plaque supérieure des condensateurs *bootstrap* à la grille des commutateurs du passage principal, lorsque les conditions appropriées sont réunies. Ainsi, il conduit finalement à un transfert de charge de la source d'entrée vers la charge que lorsque la tension d'entrée est supérieure à la tension de sortie, et elle bloque le courant de fuite inverse qui pourraient autrement passer via des interrupteurs principaux dans d'autres conditions. Des circuits de contrôle double doivent donc être utilisés de la même manière entre chaque condensateur *bootstrap* et la grille du transistor passage principal correspondant, pour annuler le courant d'écoulement de retour dans les cycles de source à la fois positifs et négatifs.

Nous proposons également d'utiliser les diodes parasites de la diffusion-substrat de la jonction P-N des transistors de charge pour limiter les fuites de courant inverse à travers les transistors du passage principal. En utilisant cette technique, la tension sur la plaque supérieure des condensateurs *bootstrap* étroitement liée à la tension de sortie et la différence entre ces tensions est limitée à la chute de tension d'une diode polarisée en direct. Cette technique, appelée aussi "*close-track*" (Figure 5.6c), est mise en œuvre en connectant les substrats des transistors de charge à la tension de sortie (DRR-4). Cela réduit la complexité du circuit, et l'espace perdue de silicium sur la puce.

Les résultats des simulations (Figure 5.5) montrent que la structure DRR-3 proposée présente un PCE significativement plus élevé que les deux autres structures de la DRR sur une large plage de résistance de sortie. L'amélioration de l'efficacité est plus évidente avec des résistances de charge plus grandes. Le redresseur DRR-3, en accord avec nos attentes, offre un rendement énergétique plus élevé que la topologie de la DRR-2 avec des amplitudes crêtes à la source inférieures à 1.0 V (Figure 5.7). Cependant, pour des amplitudes d'entrée plus grandes que 1.0 V, le rendement énergétique global est légèrement dégradé. La configuration de la DRR-4 a une structure relativement simple et produit la meilleure performance parmi toutes les structures à double-réservoir pour une large gamme d'amplitudes crêtes d'entrée.

6.4. Redresseur *bootstrap* à faible surface

L'utilisation de deux condensateurs de valeur relativement grande avec un grand transistor MOS de charge connecté en diode, qui est le cas pour les structures de DRR, peut limiter leur utilisation lorsque l'espace de silicium est limité. Afin d'économiser la surface de silicium, tout en bénéficiant des avantages offerts par la technique *bootstrap*, nous proposons une nouvelle structure de redresseur mono-réservoir pleine-onde (SRR). La structure (Figure 5.8a) a une grille à couplage croisé-couplé en plus d'un système de contrôle de polarité sélectif. Un système de contrôle amélioré conduisant les transistors du passage principal avec les plus hautes tensions disponibles dans le circuit est utilisé pour connecter un seul condensateur *bootstrap* aux commutateurs du passage principal.

Le réservoir *bootstrap* peut être nettement plus petit que la taille totale des condensateurs dans les diverses structures de DRR. Les petits condensateurs *bootstrap*, par rapport aux structures de DRR différents, impliquent de plus petits transistors de charge que les composants correspondant dans les structures de la DRR. La symétrie dans le circuit proposé assure qu'il peut traiter la distorsion du signal d'entrée. Ainsi, le redresseur proposé maintient sa haute efficacité de puissance, si les amplitudes crêtes positives et négatives sont différentes.

Le substrat du transistor de charge est connecté au nœud de sortie pour réduire le courant de retour de fuite de la charge à la source. Cependant, les substrats des transistors des chemins principaux et auxiliaires sont connectés au nœud de sortie, car il correspond au nœud où est la tension plus élevée pendant la plupart de la période d'utilisation du redresseur.

Différentes simulations des circuits en schématique montrent que la nouvelle topologie des redresseurs peut fonctionner sur une large plage de fréquences jusqu'à 50 MHz Figure 5.9). Les résultats (Figure 5.10) montrent également que sur une plage spécifique de capacité, la performance de la structure en termes de PCE et VCR ne dépendent pas de la taille des condensateurs intégrés. On note aussi que la structure de SRR offre un rendement proche de sa valeur maximale avec un condensateur de 4 pF lorsqu'il est intégré à un processus CMOS standard. L'utilisation d'un condensateur *bootstrap* plus petit implique aussi de temps plus court pour le chargement proche de la tension de crête. La configuration de SRR permet d'obtenir des efficacités de puissance aussi élevées que la structure DRR-4 pour une large plage d'amplitudes l'entrée du circuit.

La SRR proposé a été étudiée et fabriquée en utilisant un processus CMOS standard 0.18 µm 6-Métal/2-Poly TSMC 3,3V. La puce mesure $180\times600\,\mu m^2$. En comparant la surface de silicium utilisée par les circuits SRR et DRR-1, quand l'intégration de transistors de dimensions comparables, montre une économie de près de 70% dans la zone perdue de la puce.

7. Conclusions

Les redresseurs sont des circuits qui sont utilisés pour transformer l'énergie obtenue à partir de la plupart des sources d'énergie en une alimentation DC. Basé sur le type d' élément de

rectification, les circuits de redresseur sont classés comme actifs et passifs. La topologie grille croisée-couplée passive peut remplacer une ou deux diodes de redresseur en pont conventionnels par des commutateurs MOS et donc elle présente une plus grande efficacité de puissance. Les redresseurs actifs utilisent des circuits actifs pour contrôler les commutateurs MOS. Ils présentent généralement une efficacité énergétique plus élevée que le redresseur passif pour les fréquences de fonctionnement faibles ou moyennes. Ils sont cependant limités par les pertes de commutation, la complexité et les difficultés de conception. Nous avons proposé une nouvelle structure de redresseur pleine-onde intégrée qui utilise les qualités intrinsèques des transistors MOS sélectionnés comme comparateurs fonctionnant dans la région triode, pour atteindre une efficacité de puissance accrue et une chute de tension réduite. Le design ne nécessite ni une source d'énergie interne, ni un chemin de signal auxiliaire pour produire de la puissance au démarrage.

Il a également été montré qu'avec un transistor MOS classique qui a une tension de seuil régulière, l'application simultanée de la structure croisée-couplée et les techniques de réduction du seuil permettent d'obtenir une chute de tension très faible dans les commutateurs de passage principal. Cela engendre des efficacités de puissance et de tension significativement plus élevée comparée aux redresseurs avec les structures conventionnel en pont et à grille croisée-couplée.

Différents redresseurs passifs basés sur la technique *bootstrap* ont également été proposés. Ils utilisent des condensateurs simple ou double amorçage pour réduire les seuil effectif des commutateurs du passage principal. La structure mono-réservoir économise la surface requise sur la puce par rapport à la topologie à double réservoir.

L'utilisation de diodes parasites des jonctions, disponibles dans le procédé CMOS standard ainsi que d'une technique de polarisation à courts chemins auxiliaires et de circuit "*close-track*" ont été introduits. Ils simplifient le redresseur, tout en maintenant son efficacité de puissance à un niveau élevé.

Avec une amplitude de source de 3,3 V et par rapport à la porte croisée couplée topologie, le redresseur proposé offre une puissance améliorée et une efficacité de conversion de tension

allant jusqu'à 10% et 16 % de plus respectivement. Le redresseur proposé utilise la technique bootstrap, y compris les doubles et simples réservoirs. Ils sont bien adaptés pour des amplitudes d'entrée très basses. Ils présentent des rendements de conversion de puissance et de tension de 75% et 76% à l'amplitude d'entrée de 1,0 V et ils permettent de maintenir des rendements élevés sur les amplitudes d'entrée supérieure à 1.0V. Le redresseur à simple réservoir permet également d'économiser 70% de l'aire requise pour intégrer un redresseur double-réservoir. Tous les redresseurs ont été mis en œuvre en utilisant la technologie CMOS 0,18 µm et ils sont conçus pour produire un courant de charge de plus de 2 mA lorsqu'ils opèrent dans la bande ISM jusqu'à 50 MHz.

TABLE OF CONTENTS

DEDICATION III

ACKNOWLEDGEMENTS IV

ABSTRACT VI

RESUMÉ VIII

CONDENSÉ EN FRANÇAIS X

TABLE OF CONTENTS XXX

LIST OF TABLES XXXV

LIST OF FIGURES XXXVI

LIST OF ABBREVIATIONS XL

LIST OF SYMBOLS XLII

CHAPTER 1 : INTRODUCTION 1

1.1 Motivation 1

1.2 Research Problems 1

1.3 Research Objectives 2

1.4 Research Contributions 3

1.5 Thesis Organization 6

CHAPTER 2 : INTEGRATED HIGH-EFFICIENCY LOW-VOLTAGE CMOS RECTIFIERS FOR WIRELESSLY POWERED APPLICATIONS: PAST AND PRESENT 8

2.1 Introduction 8

2.2 Design and Implementation Challenges for Passive Rectifiers 10

2.2.1 Size of Main Switches 10

2.2.2 Operating Frequency 11

2.2.3 Output Ripples 11

2.2.4 Threshold Voltage 11

2.2.5 Load Current 13

2.2.6 Bulk Biasing 14

2.3 Performance Metrics and Classification of Power Rectifiers 15

2.3.1 Diode Implementations 16

2.3.1.1 P-N Junction Diode 16

2.3.1.2 Schottky Diode 16

2.3.1.3 Diode-Connected MOS 17

2.3.2 Conventional Topologies for Passive Rectifiers 18

2.3.2.1 Half-Wave Topology 18

2.3.2.2 Full-Wave Bridge Topology 19

2.3.3 Advanced Passive Bridge Rectifiers 20

2.3.3.1 Partially Gate Cross-Coupled Topology 20

2.3.3.2 Fully Gate Cross-Coupled Topology 22

2.3.3.3 Charge-Pump Based Rectifiers 24

2.4 Rectifiers with Threshold Cancellation Techniques 27

2.4.1 Rectifiers Based on the Floating-Gate Technique 28

2.4.2 Static V_{Th} Cancellation Techniques 30

2.4.2.1 External V_{Th} Cancellation Technique 30

2.4.2.2 Internal V_{Th} Cancellation Technique 31
2.4.2.3 Self-V_{Th}-Cancellation Technique 34
2.4.3 Differential V_{Th} Cancellation Technique 35
2.4.4 Bulk-Drive Technique 36
2.4.5 Bootstrapped Capacitor Technique 37

2.5 Analysis and Modeling of Passive Rectifiers 37

2.6 Active (Synchronous) Power Rectifiers 40
2.6.1 Active Diode Concept 41
2.6.2 Main Challenges in Design of Active Rectifiers 41
2.6.3 Active Rectifiers with Conventional Topology 43
2.6.4 Active Rectifiers with a Charge-Pump Structure 47

2.7 Active-Passive Power Rectifier Structures 49

CHAPTER 3 : A NOVEL LOW-DROP CMOS ACTIVE RECTIFIER 52

A NOVEL LOW-DROP CMOS ACTIVE RECTIFIER FOR RF-POWERED DEVICES: EXPERIMENTAL RESULTS 53

3.1 Introduction 53

3.2 Power Conversion Chain 54
3.2.1 Rectifier Implementation 55
3.2.2 CMOS Bridge Rectifiers 55

3.3 New Proposed Active Rectifier 59

3.4 Performance Metrics and Simulation Results 65

3.5 Measurement Results 67

3.6 Conclusion 71

3.7 References **71**

CHAPTER 4 : A DOUBLE-RESERVOIR BOOTSTRAP RECTIFIER 75

A HIGH-EFFICIENCY LOW-VOLTAGE CMOS RECTIFIER FOR HARVESTING ENERGY IN IMPLANTABLE DEVICES

4.1 Introduction **76**

4.2 Rectifier Topologies and Threshold Cancellation Techniques **78**

4.2.1 CMOS Rectifier Implementation 78

4.2.2 Threshold Cancellation Techniques 80

4.3 The Proposed Rectifier **83**

4.4 Simulation and Measurement Results **85**

4.4.1 Simulation results 86

4.4.2 Measurement Results 88

4.4.3 Measurement Setup and Test Protocol 89

4.5 Conclusions **96**

4.6 References **96**

CHAPITRE 5 : LOW-AREA BOOTSTRAP RECTIFIERS 100

LOW-AREA AND F LOW-BACK CU RRENT F REE CM OS INTEGRATED RE CTIFIERS FOR POWER SCAVENGING DEVICES

5.1 Introduction **102**

5.2 Bootstrapped-Capacitor Based Rectifiers **103**

5.2.1 Short Auxiliary Paths 105

5.3 Flow-Back Current Free Rectifiers **108**

5.3.1 Control Scheme to Limit Flow-Back Current 109

5.3.2 Close-Track Scheme for Flow-Back Current Reduction 111

5.4 Low-Area Bootstrapped Rectifier..... 113

5.4.1 Control Circuit.....114

5.5 Conclusions..... 123

5.6 References..... 123

CHAPTER 6 : GENERAL DISCUSSION 127

6.1 Active Rectifier 128

6.2 Bootstrap Passive Rectifiers..... 128

6.2.1 Double-Reservoir Bootstrapped Rectifier 128

6.2.2 Improvements in Double-Reservoir Bootstrapped Rectifier 129

6.2.2.1 Short-Auxiliary Paths.....129

6.2.2.2 Flow-back Free Scheme 130

6.3 Single-Reservoir Bootstrapped Rectifier 130

6.4 Test and measurement setup 131

CHAPTER 7 : CONCLUSIONS AND RECOMMENDATIONS 132

7.1 Contributions of This Research 132

7.2 Directions/Recommendations for Future Work..... 134

7.2.1 Single-Reservoir Bootstrapped Rectifier with Asymmetrical Input Cycles 134

7.2.2 Circuit Reliability Test 135

7.2.3 Input Matching Network Analysis 135

7.2.4 Modified Passive-Active Rectifier 135

7.2.5 Active Rectifier with Low Effective Switching Frequency.....136

BIBLIOGRAPHIE..... 137

LIST OF TABLES

Table 3.1. Rectifier switching states for positive cycle..... 63

Table 3.2. Summary of measured power efficiency for cited rectifiers. 71

Table 4.1. Post-layout and measurement results. 94

Table 4.2. Comparison with most advanced rectifier characteristics..... 94

Table 5.1. Circuit parameters for rectifier topologies. 106

Table 5.2. Comparison with most advanced rectifier characteristics..... 122

LIST OF FIGURES

Figure 2.1. Dynamic bulk switching scheme: (a) for nMOS transistors, (b) for pMOS transistors. 14

Figure 2.2. Circuit diagram for a full-wave rectifier: (a) bridge, (b) center-tapped. 19

Figure 2.3. Circuit diagram for a full-wave nMOS-based bridge rectifier. 20

Figure 2.4. Circuit diagram for a gate cross-coupled rectifier. 21

Figure 2.5. Circuit diagram for a fully gate cross-coupled rectifier in [43]. 23

Figure 2.6. Circuit diagram for a fully gate cross-coupled rectifier in [160]. 23

Figure 2.7. Schematic of a Greinacher charge pump. 24

Figure 2.8. Schematic of a N-stage charge pump rectifier. 25

Figure 2.9. Circuit diagram for an external V_{Th} cancellation technique in [161]. 30

Figure 2.10. Circuit diagram for an internal V_{Th} cancellation technique in [121]. 31

Figure 2.11. Circuit diagram for an internal V_{Th} cancellation technique in [169]. 33

Figure 2.12. Circuit diagram for a Villard rectifier: (a) conventional diode-connected MOS, (b) ULPD-connected MOS in [94]. 35

Figure 2.13. Circuit diagram for a rectifier cell using differential V_{Th} cancellation technique. .. 36

Figure 2.14. Circuit diagram for a Villard charge-pump based rectifier using the bootstrapping capacitor technique [99]. 38

Figure 2.15. Block diagram of typical active (synchronous) rectifier. 40

Figure 2.16. Circuit diagram for active rectifier in [97]. 44

Figure 2.17. Circuit diagram for active rectifier in [104]. 45

Figure 2.18. Circuit diagram for active rectifier in [63]. 46

Figure 2.19. Circuit diagram for active rectifier in [113]. 48

Figure 2.20. Circuit diagram for active-passive rectifier in [133]. 50

Figure 3-1. Block diagram of a typical PCC..... 54

Figure 3.2. Schematic of a full-wave bridge rectifier: (a) diode implementation, (b) MOS diode-connected implementation..... 56

Figure 3.3. Gate cross-coupled rectifier [12]. 57

Figure 3.4. Schematic of the proposed full-wave rectifier..... 60

Figure 3.5. Schematic of the active parts during the positive half cycle 60

Figure 3.6. Simulated result of the FWAR over one period. 62

Figure 3.7. Schematic of dynamic bulk biasing for main switches: (a) M_1 and (b) M_3..... 64

Figure 3.8. Simulated output voltage of FWDR, GCCR and FWAR..... 66

Figure 3.9. Simulated VCRs for various rectifier structures..... 66

Figure 3.10. Simulated power efficiency versus input amplitude..... 67

Figure 3.11. Photomicrograph of the prototype chip. 68

Figure 3.12. Voltage and power measurement setup. 69

Figure 3.13. Input/output waveforms of FWAR operating at: (a) f=1 MHz, (b) f=10 MHz. 69

Figure 3.14. Measured power conversion efficiency of FWAR operating at 10 MHz..... 70

Figure 4.1. Schematics of full-wave rectifiers: a) gate cross-coupled, b) fully cross-coupled. ... 79

Figure 4.2. Block diagram of active rectifier typical configuration.**Error! Bookmark not defined.**

Figure 4.3. Schematics of: a) the proposed full-wave rectifier, b) its dynamic bulk biasing circuit for diode-tied transistors of $M_{5\text{-}6}$..... 82

Figure 4.4. Simulated power conversion efficiency versus input peak amplitude. 86

Figure 4.5. Simulated voltage conversion ratio versus input peak amplitude. 87

Figure 4.6. Simulated power efficiency and voltage conversion ratio versus boot strapped capacitor size. 88

Figure 4.7. Photomicrograph of the prototype chip; A and B highlight bootstrapped capacitors (C_{B1-2}), C and D address main pass transistors (M_{1-4}), and E marks the bootstrapping (M_{5-8}) and dynamic bulk biasing circuitry. 89

Figure 4.8. Voltage and power measurement setup. 89

Figure 4.9. Simulated frequency response of the proposed rectifier. 91

Figure 4.10. Measured voltage conversion ratio of the proposed full-wave rectifier versus input amplitude operating at f=10 MHz. 91

Figure 4.11. Measured power conversion efficiency of the proposed full-wave rectifier operating at f=10 MHz. 92

Figure 5.1. Schematics of: a) the double-reservoir rectifier: b) its original bootstrapped pMOS setup (DRR-1) [17], c) its revised boot strapped pMOS setup with short-auxiliary paths (DRR-2). 104

Figure 5.2. Simulated power efficiency versus input peak amplitude for the DRR-1 and DRR-2 structures. 104

Figure 5.3. Simulated voltage conversion ratio versus input peak amplitude for the DRR-1 and DRR-2 structures 107

Figure 5.4. Schematic of control scheme for positive cycles. 109

Figure 5.5. Simulated power efficiency versus load resistance for three considered DRR structures. 110

Figure 5.6. Schematics of the charging path for bootstrapping capacitor in positive input cycles: a) typical DRR, b) DRR with the basic close-track biasing, c) proposed implementation of DRR with simplified close-track biasing (called DRR-4).. **Error! Bookmark not defined.**

Figure 5.7. Simulated power efficiency for DRR structures with and without the parallel diode. 113

Figure 5.8. Schematic of the proposed single-reservoir topology: a) Rectifier architecture (SRR), b) Control circuit. 113

Figure 5.9. Performance of the proposed rectifier over different input source frequencies. 117

Figure 5.10. Simulated power efficiency and voltage conversion ratio versus boot strapped capacitor size. 118

Figure 5.11. Simulated power conversion efficiency versus input peak amplitude for double- and single-reservoir rectifier structures 117

Figure 5.12. Photomicrograph of chips for different rectifier structures: a) double-reservoir, b) single-reservoir. 119

Figure 5.13. Measured voltage conversion ratio of the proposed SRR as a function of input peak amplitude when operating at f=10 MHz. 119

Figure 5.14. Measured power conversion efficiency of the SRR full-wave rectifier versus input peak amplitude operating at f =10 MHz. 121

LIST OF ABBREVIATIONS

AC	Alternative current
BERT	Berkeley reliability test
BiCMOS	Bipolar-CMOS
BJT	Bipolar-junction transistor
CMOS	Complementary metal-oxide semiconductor
DC	Direct current
DBS	Dynamic bulk witching
DRR	Double-reservoir rectifier
DTMOS	Dynamic-threshold MOS
ESD	Electrostatic discharge
EVC	External-V_{Th}-cancellation
FG	Floating-gate
FGCCR	Fully gate cross-coupled rectifier
FSL	Fast-switching limit
FWAR	Full-wave active rectifier
FWBR	Full-wave bridge rectifier
FWDR	Full-wave diode rectifier
FWGR	Full-wave gate cross-coupled rectifier
FWFR	Full-wave fully gate cross-coupled rectifier
FWNR	Full-wave new rectifier
F-N	Fowler-Nordheim

GCCR	Gate cross-coupled rectifier
HF	High frequency
IVC	Internal-V_{Th}-cancellation
MEMS	Micro electro-mechanical systems
OP-AMP	Operational amplifier
PCE	Power conversion efficiency
PGCCR	Partially gate cross-coupled rectifier
RF	Radio frequency
RFID	Radio frequency identification
RMS	Route mean square
SRR	Single-reservoir rectifier
SSH	Synchronized switch harvesting
SSL	Slow-switching limit
STS	Silicon-Titanium-schottky
SVC	Self-V_{Th}-cancellation
UHF	Ultra high frequency
ULPD	Ultra-low-power device
VHF	Very high frequency
VCR	Voltage conversion ratio

LIST OF SYMBOLS

C_L	Load capacitance
C_{OX}	Gate capacitance per unit area
f	Frequency
g_m	Transconductance
G_{ds}	Drain-source conductance
I_D	Drain current
L	Length of transistor
R_L	Load resistance
R_{ON}	Channel resistance
V_{BS}	Bulk-source voltage
V_{CAP}	Capacitor voltage
V_{DD}	Supply voltage
V_{eff}	Effective voltage
V_G	Ground voltage
V_{GD}	Gate-drain voltage
V_{GS}	Gate-Source voltage
V_{IN}	Input voltage
V_{In+}	Input voltage (positive terminal)
V_{In-}	Input voltage (Negative terminal)
V_{Out}	Output voltage
V_{SG}	Source-gate voltage

V_{SS}	Supply voltage
V_{Th}	Threshold voltage
W	Width of transistor
μ	Mobility of carrier
μ_P	Mobility of holes

Chapter 1 : INTRODUCTION

1.1 Motivation

Nowadays, inductive RF links are a preferred solution to power up a wide range of wireless devices including, but not limited to, smart implantable medical devices, low-cost passive radio frequency identification (RFID) tags, and wireless sensor networks. In such systems, the same link is typically used both for power and data transmission. However, this method suffers from poor electromagnetic coupling, and the strong dependence of received power to the distance, orientation and displacement of the remote transmitter can result in a low power efficiency. Power scavenging techniques are shown to be able to harvest significant amount of power from the environment including the human body. All these techniques require transforming the energy from an AC signal to an unregulated DC voltage, in order to supply power to the various blocks in their power conversion chain.

Previously developed power systems generally use rectifiers in their front-end to accomplish the AC to DC conversion. The power efficiency of the rectifiers therefore significantly affects the performance and the characteristics of the power conversions chain.

The need for configurations with higher power efficiencies and greater output voltage has attracted many researchers to improve the performance of the power conversion chain in wirelessly powered systems. For an inductively coupled power chain, it is important to mention that a more efficient rectifier can deliver a given amount of power for a lesser voltage induced across the secondary coil. Thus, it requires a smaller coupling coefficient and allows for a greater relative distance between the coils.

1.2 Research Problems

Conventional integrated passive rectifiers use inefficient parasitic junction diodes or diode-connected MOS transistors. Their performance is significantly degraded by the forward-bias voltage drop of diodes or the threshold voltage of MOS transistors. Such threshold voltage results in a significant power loss within the rectifier, which affects the overall power efficiency and

decreases the delivered voltage to the following blocks. This negative impact becomes increasingly significant in the design of low-voltage power supplies. Such low-voltage supplies are common with sub-micron CMOS technologies. Moreover, in diode-connected rectifiers, V_{GS} of the transistors is modulated by V_{DS}. Therefore, for voltages around the threshold voltage (V_{Th}), the latter parameter changes slightly from forward to reverse conduction. This subjects the structure to significant leakages and leads to inefficient rectification.

Furthermore, transistors implemented with CMOS processes commonly share a global substrate. Depending on the biasing of the bulk terminals, there exist time intervals in which a significant amount of leakage current may flow from the bulk of pMOS transistors into the substrate. For rectifier circuits where input and output voltages vary significantly over time, this scenario is very likely. Note that the leakage current through the main pass MOS transistors which carry high load currents may drastically affect the overall power efficiency of a rectifier and potentially trigger a latch-up condition. Therefore, one should take extensive care to ensure proper bulk biasing for the main switches.

Active rectifier configurations have been reported to have higher power efficiency compared to their passive counterparts. They use active circuitry such as comparators to control the main pass MOS switches, replacing the diode-connected transistors. They offer faster switching between the ON and OFF states and allow reducing leakages. However, they generally require an independent power source to operate and the associated extra circuitry adds to design complexity and power consumption. These drawbacks typically outweigh the benefits they offer and limit their application to systems where an auxiliary power source is present. The auxiliary power source may come from a secondary low efficiency parallel rectifier, or a large capacitor. The design of high-speed high-resolution low-power comparators, which are a core block in an active rectifier, can be very challenging. This is particularly true when the power source to be rectified is recovered from a signal whose frequency can exceed 10 MHz.

1.3 Research Objectives

The main objective of this thesis is to introduce an integrated high-efficiency CMOS rectifier for low-voltage and high current applications. Based on the research problems and requirements, the detailed objectives of this thesis are as follows:

- To develop a rectifier that can be integrated in standard sub-micron CMOS processes to achieve high performance, with low area and cost.
- To maintain high performance with asymmetric inputs. Asymmetric inputs may be result from sudden changes in the distance and orientation of the primary and the secondary coils in an inductively powered system.
- To reduce reverse currents from the output load back to the input source.
- To be functional over a wide range of frequencies in the MHz range. This frequency range is suited for many industrial, scientific, medical (ISM) and RFID applications operating in HF, VHF and UHF bands.
- To be robust and reliable against leakages into the substrate and reduce risks of latch-up.
- To be able to provide a load current in the mA range. High current capability is required for many applications including biomedical stimulation.
- To be sufficiently sensitive to low input amplitudes. This is especially challenging with advanced sub-micron processes, where the threshold voltage does not scale with the nominal supply voltage.

1.4 Research Contributions

In this thesis, we have achieved three main contributions with respect to the development of full-wave high-efficiency low-voltage integrated rectifiers capable of handling high load currents. It includes the design and implementation of active and passive rectifiers reported in:

- S. Hashemi, M. Sawan, and Y. Savaria, "A novel low-drop CMOS active rectifier for RF-powered devices: Experimental results, Elsevier Microelectronics Journal, no. 40, pp. 1547-1554, Jan. 2009.
- S. Hashemi, M. Sawan, and Y. Savaria, "A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices," IEEE Transactions on Biomedical Circuits and Systems (April 2011, Paper to appear).

- S. Hashemi, M. Sawan, and Y. Savaria, "Low-area and flow-back current free CMOS integrated rectifiers for power scavenging devices," IEEE Trans. Circuits and Systems: Regular Papers-I (June 2011, Submitted).

Before coming up with the new rectifier architectures, we proposed an new high-level modeling technique for power conversion chains [69]. This model is based on analytical expressions, behavioral and/or empirical considerations in the design of power chains to quickly predict the dissipated power and estimate the power efficiency. Using this model, the impact of power efficiency degradation due to non-ideal characteristics of various blocks in a typical power conversion chain was studied in detail as reported in.

- S. Hashemi, M. Sawan, Y. Savaria, "A Power Planning Model for Implantable Stimulators", IEEE International Symposium on Circuits and Systems (ISCAS), Greece, May 2006.

Following is a detailed list of contributions in the proposed architectures for active rectifiers:

- Configuring the rectifier based on a partially gate cross-coupled structure which implies positive feedback and maintains maximum input voltage swing for the main switches.
- Replacing diode-connected transistors with low-loss MOS switches acting in the triode region, where they present a very low voltage drop.
- Using inherent characteristics of MOS transistors as comparators in place of an explicit comparator, which results in circuit simplicity, power savings, and area reduction.
- Applying the dynamic biasing technique to the bulk of the main pass switches, which results in less leakage through the substrate and reduced risk of latch-up.
- Employing small pull-up transistors in the control circuit of the main switches which helps preventing floating gates and associated drawbacks during inactive periods.
- Using low-threshold MOS transistors within the control scheme to reduce the dead zone for the comparators. This results in increasing the sensitivity of the rectifier circuit to low amplitude inputs.

- Driving the gate of all transistors in the control path with the highest voltages available in the circuit to increase their speed and transconductance and reduce their channel resistance.
- Considering adequate timing for the rectifier by proper sizing the transistors, to maintain high-efficiency over a wide range of operating frequency in the MHz range.
- Developing a test setup with an isolating transformer to generate a floating source.
- Implementing the proposed passive rectifier in the TSMC 0.18 µm CMOS process.
- Evaluating the effect of a local (isolated) substrate to implement the dynamic bulk biasing technique on nMOS native transistors.
- Implementing a precise measurement technique for evaluating the input and output voltages and currents to calculate the power efficiency.

Two rectifiers topologies based on the bootstrapping technique were also proposed to reduce the effective threshold voltage of the main pass transistors. The proposed double-reservoir rectifier is the result of the following contributions:

- Implementing the bootstrapping technique using small integrated capacitors to reduce the effective threshold of main pass switches.
- Configuring the rectifier based on partially gate cross-coupled structure which implies positive feedback and maintains maximum input voltage swing for the main switches.
- Using auxiliary paths for circuit startup using diode-connected MOS transistors in parallel with the main pass pMOS switches.
- Applying the dynamic bulk biasing technique to the charging transistors and fixing the bulk voltage of main pass switches to the output voltage in order to minimize leakage into the substrate.
- Implementing the proposed passive rectifier in the TSMC 0.18 µm CMOS process.

The proposed single-reservoir rectifier is an improved version of the double-reservoir rectifier with the following contributions:

- Introducing a short auxiliary path using the parasitic diffusion-bulk junction diode of main pass pMOS switches to create a path between the source and the boot strapping

capacitor particularly at startup. This path replaces the explicit diode connections and simplifies the rectifier circuit.

- Introducing a control scheme to reduce the flow-back current by regulating the conduction angle of main pass transistors.
- Introducing a close-track scheme using the parasitic diffusion-bulk junction diode of charging transistors to force the bootstrapping capacitor voltage closely track the output voltage. Close-tracking limits the voltage difference between the bootstrapping node and the output to the voltage drop across a diode. This simple structure significantly reduces the flow-back current through the main pass transistors.
- Introducing a smart polarity selective control scheme for asymmetrical inputs to share the bootstrapping capacitor between the positive and negative cycles. Using a single bootstrapping capacitor results in considerable area savings.
- Implementing the proposed passive rectifier in the TSMC 0.18 μm CMOS process.

1.5 Thesis Organization

This thesis is written in a paper-based format and contains copies of the published journal article in chapter 3, the accepted journal article in chapter 4, and the submitted journal article in chapters 5.

Chapter 2 reviews the principles and classification of power rectifiers. It highlights key issues and major challenges in their design and implementation in CMOS processes both at device and architecture levels. It also introduces important metrics to evaluate the performance of rectifiers and discusses several approaches to optimize them. Various analysis methods and modeling techniques for rectifier circuits are also presented. It covers all the significant related work in the power rectifier domain and briefly describes the suggested topologies along with their achievements. This review will be submitted for publication shortly.

The design and implementation of a new rectifier is discussed in chapter 3, where an active rectifier with a gate cross-coupled topology in place of the diode-connected transistors in conventional rectifiers is introduced. Using the inherent characteristics of MOS transistors as comparators, dynamic bulk biasing of main pass switches is proposed, and pull-up transistors are

used to avoid floating gates in that proposed rectifier. Results obtained from simulations and measurements reveal that the proposed rectifier exhibits significantly higher power efficiency compared to conventional rectifier structures for a wide range of operating frequencies in the MHz range. This work was published in Elsevier Microelectronic Journal in January 2009.

Using the bootstrapping technique to reduce the effective threshold voltage of MOS switches, an integrated full-wave high-efficiency rectifier with a gate cross-coupled topology is proposed in chapter 4. The rectifier uses two bootstrapping circuits attached to main pass MOS switches along with auxiliary paths to activate the bootstrapping circuit at startup. The voltage drop across the rectifier is significantly reduced, making it suitable for low-voltage applications. This work was submitted to IEEE transactions on Biomedical Circuits and Systems in April 2011 and was accepted with minor corrections on July 11th, 2011.

A single-reservoir rectifier is proposed in chapter 5, in which a single bootstrapping circuit serves for both of input cycles. The rectifier presents a performance as high as a double-reservoir structure in terms of power efficiency and voltage conversion ratio, while saving almost 70% of the die area. Several bulk biasing approaches for the main and charging transistors including the short auxiliary paths and the close-track scheme are suggested. The new biasing techniques use parasitic diffusion-bulk junction diode of the main and charging transistors, which results in considerable simplifications in the design. The former serves for circuit startup and the latter eliminated the reverse leakage current. The resulting configuration produces the best performance among all double-reservoir structures. This work was submitted to IEEE Transaction on Circuits and Systems: Regular Papers-I in June 2011.

Chapter 6 covers the general discussions about the thesis and finally, the conclusions of this thesis, along with few recommendations for the future works are presented in chapter 7.

Chapter 2 : INTEGRATED HIGH-EFFICIENCY LOW-VOLTAGE CMOS RECTIFIERS FOR WIRELESSLY POWERED APPLICATIONS: PAST AND PRESENT

2.1 Introduction

Advances in wireless communications have led to the development of low-voltage and low-power integrated circuits. They are necessary for supporting the functionality and meeting the desired performances of embedded electronic systems, such as wireless sensors networks [4,30,37], radio frequency identification (RFID) tags [11,34], smart biomedical devices [57,81], and general wirelessly powered devices. These applications require high-efficiency, high-sensitivity, long operating time, and low-power rectifiers as one of their most critical circuit elements.

Various powering techniques including embedded batteries and transcutaneous transmission are relatively constrained in terms of energy density, device lifetime, potential hazards to human safety, integration, and required space. On the other hand, energy harvesting techniques are processes by which energy readily available from the environment (including the human body) is harvested and converted into usable electrical energy. Remarkable efforts dedicated to developing these techniques reveal that they can be inexpensive, highly compatible with electronics, and capable of procuring high power levels. However, despite the significant progress in the recent years [8-9], these techniques are not considered reliable yet [41,155].

Several types of wireless systems benefit from inductive links to extract power from the signal received by an antenna [45,167]. In this case, a radio frequency (RF) signal is commonly used to simultaneously transmit data and transfer the energy required for carrying the intended functions. This technique is more convenient and advantageous compared to wired [81] and battery-based architectures [101]. This is particularly true for biomedical implants where human safety and convenience are involved and system autonomy is a requirement. In such applications, a highly efficient rectifier can reduce the total required power and consequently reduces the risk of potential tissue damage caused by overheating. Overheating may be the result of absorption of

RF power in t issues surrounding t he i mplanted de vice w hich i ncreases w ith t ransmission frequency and a mplitude. P assive R FID t ags a nd s ensor node s often us e i nductive l inks to wirelessly pr ocure t he r equired pow er. A part f rom t echnology l imits, s haring a c ommon r adio field f or da ta a nd po wer t ransmission makes t he i nductively pow ered s ystem s usceptible t o significant i nput a verage pow er v ariations due t o pos sible c hange i n ope rating di stance and orientation of t he pr imary coil w ith r espect t o t he s econdary on e. A ny amplitude m odulation scheme in data transmission will also directly influence power transmission. T hese changes in input pow er a nd pr esence of a mplitude m odulation i nevitably l ead t o l arge f luctuations i n t he input s ignal l evels w hich c an be de trimental t o t he f unctionality of s upply s ensitive a nalog circuits. In extreme cases, excessive drop in supply voltage could trigger a power-on-reset and interrupt normal functionality, and excessive supply voltage may subject the device to reliability issues.

Most of the energy transmission systems sources, including inductively-powered circuits and self-powered s ystems b ased o n p ower s cavenging t echniques, employ alternating cu rrent (AC) sources to deliver power. This AC signal must be transformed into a DC supply using a rectifier to power electronic devices. An essential part of a power rectifier is its rectifying element, very often a di ode, which provides a uni directional path f or t he current f lowing from t he s ource toward t he l oad. In general, rectifiers m ay be fabricated us ing s olid-state di odes, t hyristors, vacuum tubes, mercury arc valves, and other components.

Power efficiency of the rectifier significantly affects the performance and characteristics of the power conversion chain. It is therefore crucial to use a high-efficiency rectifier in the front-end of the power conversion system. There is no recent comprehensive survey on the structure, performance, and applications of power rectifies. Authors in [153] presented some survey on the contributions to the field; however while emphasizing on high power rectifiers, they do not cover low-voltage a nd hi gh-efficiency pow er r ectifiers. A uthors ha ve r eported d ifferent r ectifiers structures and implementations for various applications, which will be addressed throughout this paper along with discussions on their operation, features (advantages and/or disadvantages), and applications.

The r ectifiers may u se d evices imp lemented b y s ilicon-on-isolator (SOI) [34,77,164], b y bipolar-metal o xide s emi-conductor (BiCMOS) [47], or b y m icro-electro-mechanical s ystems

(MEMS) [120] processes. These rectifiers are not covered as they are not supported by standard CMOS processes.

This chapter focuses on rectifiers used for power conversion, which excludes the so called precision rectifiers. This other class of rectifiers used for signal processing purposes is beyond the scope of this thesis.

2.2 Design and Implementation Challenges for Passive Rectifiers

In low power devices, it is imperative for the rectifier to be highly efficient when converting small amplitude AC input signals to DC supply with minimum power dissipation. For an inductively coupled power conversion chain, a more efficient rectifier can deliver more output DC power from the same AC signal induced across the secondary coil. Thus, a power conversion chain embedding a more efficient rectifier may allow operation with a smaller coupling coefficient or a larger distance between the primary and secondary coils. Many design parameters such as input impedance matching network, size and type of main switches, operating frequency, output ripples, threshold voltage, load current and bulk biasing may affect the performance of an integrated rectifier in a power conversion chain. The rest of this section reviews the importance of these factors.

2.2.1 Size of Main Switches

A rectifier circuit can be implemented using MOS switches connected and used as diodes. These transistors have a certain threshold voltage, and they operate at up to some frequency. As for the size of MOS switches, larger *W/L* will result in lower impedance that may produce larger output voltage and shorter switching time. This mainly results from the fact that larger W/L produces a larger saturation current and a smaller channel resistance. However, power efficiency does not necessarily increase as the reverse current within the switches is also increased and parasitic capacitances associated with them is also incremented. It was shown that substrate losses, which is omnipresent in bulk CMOS, has a simple dependency on the substrate parasitic resistance, and a quadratic dependency on substrate parasitic capacitance as well as on the RF signal voltage and frequency [86]. Larger devices with higher parasitic capacitances are also shown to lower the output voltage of a charge pump based rectifier [108]. It is therefore required

that the size of diode-connected MOS transistors be optimized to maximize power efficiency [33,108-109,173-174]. Authors in [31] presented various issues and trade-offs that lead to the development of a pure CMOS rectifier.

2.2.2 Operating Frequency

For inductively powered systems, where the data and power are transmitted simultaneously, the RF transmission frequency is partly determined by the required data transmission rate. Therefore, the transmission frequency should be high enough to allow a large bandwidth for duplex communication between transmitter and receiver. The data transmission rate also depends on data modulation and encoding techniques [3,59,165]. Implementing circuits operating at high frequencies implies a complex design which is generally more power hungry. In biomedical implants however, power losses due to tissue absorption increase with frequency resulting in overheating the surrounding tissues. The operating frequency is then bound by the maximum electromagnetic radiation limits. Therefore there exists a clear trade-off in selecting the frequency of operation. Previous studies have shown that for carrier frequencies between 1 and 10 MHz, RF energy penetrates the body with minimum loss [165] and high frequencies (>20 MHz) should be avoided to minimize tissue damage.

2.2.3 Output Ripples

The output waveform of a rectifier typically shows ripples due to charging and discharging of the output capacitor. On the other hand, many analog circuits require a constant supply voltage to maintain their functionality and performance. Thus, it is often desirable to reduce the amount of output ripples. The magnitude of the rectifier output ripples can be substantially reduced by increasing the source operating frequency, or by using larger output capacitances. Using a large output capacitor however increases the settling time of the output voltage degrading its high frequency performance [109].

2.2.4 Threshold Voltage

The MOS threshold voltage is a process dependent parameter. It is a voltage barrier that hinders AC-to-DC conversion. It has profound impacts on rectifier performance consisting of

diode-connected MOS diodes. First, the product of the threshold voltage by the diode forward current represents a power dissipation that degrades rectifier power conversion efficiency. Secondly, it decreases the rectifier average (DC) output voltage, increasing the required minimum amplitude of the AC input voltage. Third, with fixed supply, a small increment of threshold voltage demands a similar increase in input source voltage while keeping a negligible disturbance to its diode current, hence input resistance of the rectifier increases in proportional to threshold voltage. Similar to the transistor sizing problem, any increase in input resistance creates a current divider by shunting more current through input parasitic capacitance, hence subjecting the rectifier to further losses [31].

The threshold voltage of a MOS transistor is related to its size (*W*/L) and bulk biasing. These effects are captured in the so-called body-effect that can increase the effective transistor threshold and its negative impact. This effect can be alleviated by the transistor configuration (use of pMOS transistors as main switches), and/or by increasing the aspect ratio of the MOS transistors, and/or by properly biasing the transistor bulks. However, trying to influence the threshold may be challenging as it may: 1) increase area; 2) cause latch-up hazards due to the lack of a well-defined supply voltage and due to the presence of multiple parasitic transistors; 3) degrade high frequency performance due to parasitics associated with large transistors and to the presence of extra well parasitic junction capacitances at the RF driving point [31].

Process foundries offers several options for the threshold voltage of transistors. Some advanced CMOS processes provide transistors with different (low, medium and high) threshold voltages. Intrinsic devices, sometimes referred to as native devices, are created by blocking the channel implantation process steps to create a channel with very low doping, which generates devices with near zero threshold voltages (50-100 mV) [160]. In twin-well CMOS and silicon-on-insulator (SOI) processes, both pMOS and nMOS intrinsic devices can be fabricated, which is not the case for single-well processes.

Use of low- or medium-threshold devices [29,34,38,43-44,55-56,90,106,108-111,160-161,173-174,176-177] appears to be a promising solution to the problems associated with the threshold voltage of MOS transistors connected as diodes. However, using threshold voltage less than 100 mV is not recommended because all transistors can turn on simultaneously and lead to severe reverse leakage current [33].

In general, very low input amplitudes fail to turn on diode-connected MOS transistors and hence cannot generate a forward current to charge the storage capacitor. On the other hand, low-threshold transistors tend to induce high leakage currents that can have significant detrimental effects. Therefore, for a rectifier implemented using native transistors, the power consumption can increase remarkably, especially at low input amplitudes, which deteriorates its performance. Many authors [38,111,160, 169,175] have reported such poor performance when low-threshold MOS transistors are used as diodes in the main path of the rectifiers. This effect can, in part, be countered by increasing the operating frequency or the value of the storage capacitor. However, when very high values of either frequency or capacitance are needed, this option becomes unfeasible [38]. The possibility of using Schottky devices, which offer a forward drop lower than regular diodes instead of low-threshold MOS devices, depends on their availability, their cost and the threshold voltage variations.

2.2.5 Load Current

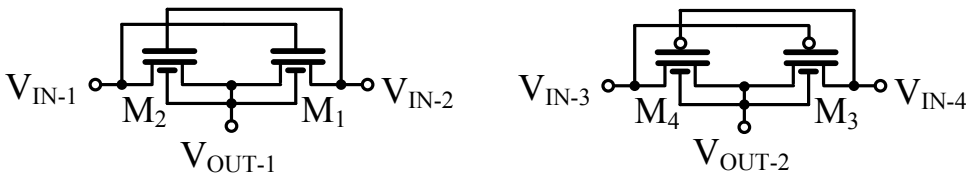
Low-current integrated full-wave rectifiers are used in remote sensing [54] and radio-frequency identification (RFID) [114] applications. However, there are also applications, such as in biomedical implants target stimulation large number of sites, which require high current values [48-51]. Effective power delivery for such applications typically requires an output current of around 20 mA. This current when combined with a megahertz input source induces major challenges in the design and implementation of a power conversion chain.

In order for the rectifier to source a large output current, large transistors should be used to minimize the conduction power loss. However, compared to a hundred-kHz input, a megahertz input signal can lead to higher losses in the rectifier associated with the leakage current due to more frequent improper switching of large-size power transistors. The design of several high-current wideband integrated rectifiers in CMOS and BiCMOS processes are presented in [52]. A variety of on-chip conventional BJT bridge rectifiers with different topologies, frequency response, size, breakdown voltage, and current handling capabilities were tested.

2.2.6 Bulk Biasing

In a rectifier structure supplied by an inductive link, MOS transistors share the same substrate. Their sources are connected to the secondary coil. The terminals of this coil are subject to large variations in the source-bulk voltage. They go above the output voltage, and below the ground. Therefore, the transistors that experience such large fluctuations may be subject to significant substrate leakage currents leading to latch-up. This phenomenon could constrain the power efficiency of the circuit and compromise its reliability. It is crucial then to reduce this risk by preventing the vertical parasitic transistors from turning on. Therefore, the body potential of main pass MOS transistors should be precisely controlled. Use of fixed [54,119] or dynamic [2,8,16-20,28-29,47-48,52,56,89,114,127,154,169] biasing schemes have been introduced for such purpose. Authors have also made additional efforts to reduce the risk of latch-up by following strict layout guidelines. Some of these guidelines include attention to large current handling capability, observing a minimum distance between large devices, and insertions of guard rings around potential injectors. Separating the wells of large transistors from the rest of circuit is also suggested in processes where deep n-wells are available [47,52,76].

The Dynamic Bulk Switching (DBS) technique is implemented using an auxiliary pair of transistors to selectively bias the bulk of the targeted transistors, as shown in Figure 2.1. The output of the circuits should be connected to the bulk of the targeted MOS transistor. Depending on the type of transistor, adequate nMOS or pMOS auxiliary pairs should be employed. For an nMOS transistor, for which the bulk should be connected to the lowest voltage in the circuit, the nMOS only circuit is used. The pMOS only circuit is used for dynamic bulk biasing of the pMOS transistor, for which the bulk should be connected to highest available voltage. These bulk biasing circuits do not let the parasitic vertical BJT transistors to turn on and leave little chance



(a) (b)

Figure 2.1. Dynamic bulk switching scheme: (a) for nMOS transistors, (b) for pMOS transistors.

for leakage current or latch-up. Another advantage of this configuration is the elimination of the body effect on the rectifying MOS transistors [76]. Although the DBS technique is reported to effectively reduce the substrate leakage current and body effect, however, it subjects the design to further power consumption which is against the objectives for many designs. The DBS circuit does not properly work when the input amplitudes are below the threshold of the transistors, leading to a high impedance output. Lack of a proper bias voltage at the bulk during low input intervals can significantly increase leakage currents through the bulk.

2.3 Performance Metrics and Classification of Power Rectifiers

For a power rectifier, there are different parameters such its power conversion efficiency (PCE), voltage conversion ratio (VCR), average (DC) output voltage, minimum input voltage and average load current which may be characterized. PCE is defined as the ratio of the power dissipated by the load compared to total power consumed by the rectifier circuitry. This parameter is commonly used to compare different rectifier. The PCE of a rectifier is affected by its circuit topology, diode-device parameters, amplitude and frequency of input RF signal, and output loading conditions. VCR is defined as the ratio of the average (DC) output voltage to the input peak amplitude. The minimum input voltage is the minimum voltage that could activate the rectifier. The maximum input voltage is determined by the maximum voltage that the devices can sustain. It may be associated with gate breakdown or activation of reverse biased junctions or parasitic devices. These maximum and minimum voltages determine the dynamic range of the rectifier. Rectifiers may have also been categorized by their load current handling capabilities. Authors have presented approximate formulas for the calculation of the output voltage, ripple voltage, and the RMS/peak values of the source current of different rectifier circuits.

Power rectifiers are also classified based on the method by which their diodes are implemented. Rectifier circuits using passive components, such as diodes or diode-connected MOS transistors are called passive rectifiers. Active rectifiers are those in which the diode is implemented using active elements that typically consist of MOS switches, comparators and their peripheral circuitry. Recently, some passive-active rectifiers with multi-stage configuration have been introduced. These configurations combine stages of different classes (either active or passive).

2.3.1 Diode Implementations

Depending on the features and characteristics of the process in use, diodes could be implemented in different ways. In the processes where integrating diodes along with other components is not possible, either discrete (off-chip) or hybrid diode bridge [6,15,59,107] are used. This approach increases the number of off-chip components and the size of the system. Implementing an on-chip rectifier with CMOS technology offers several advantages. Integrated rectifiers a) can be fast enough to operate in the MHz range due to the elimination of off-chip interconnect and parasitic components, b) are compatible with other circuitry that can be realized using IC fabrication processes, c) are miniaturized, and d) can be manufactured at low cost. Many authors proposed different methods to implement diodes in standard CMOS processes as discussed in the sequel.

2.3.1.1 P-N Junction Diode

In the standard CMOS processes floating power diodes are not available. Instead, inefficient parasitic diodes formed at different P-N junctions are mainly used [82]. Forward biasing some of the said diodes can result in forward biasing of the parasitic BJTs with significant power loss and potential risk of latch-up. To alleviate this constrain, some designs make use of BiCMOS or discrete diodes. The junction diodes sharing diffusion regions also suffer from low reverse breakdown voltage due to high level of doping in diffusion regions. Ignoring the leakage currents, diode losses are mainly due to resistive losses when current flows through them. Therefore, in order to realize a high efficiency rectifier, diodes with small turn-on voltage are necessary. The typical forward-bias voltage threshold of a P-N diode (typically 500-600 mV) significantly degrades the PCE of power conversion chains operating at low voltages. Nevertheless, simple P-N junctions are usually avoided in CMOS technologies because of above mentioned challenges.

2.3.1.2 Schottky Diode

Owing to their low series resistance and small forward bias voltage drop, large saturation current, and small junction capacitance, Silicon-Titanium Schottky (STS) diodes are widely employed in rectifier. They were cited as allowing to reduce substrate losses, to shorten settling

time, and to enhance conversion efficiency [86,108]. The effective turn-on voltage of a Schottky diode is lower than that of a regular P-N junction (200-300 mV). However, these diodes are often unavailable in standard CMOS technologies due to the extra manufacturing steps required and higher costs. They also suffer from large temperature dependencies [92-93,108-109,174] and high reverse currents [158].

2.3.1.3 Diode-Connected MOS

In integrated circuits, implemented with standard CMOS processes, diodes are commonly replaced with diode-connected MOS transistors. These diodes, compared to their BJT counterparts, exhibit less substrate leakage currents [144]. They could be easily integrated with standard CMOS processes which make them more popular and cost effective than BiCMOS. However, due to short connection between their gate and drain terminals, all MOS transistors mainly work in saturation region, which implies high power consumption. While the voltage drop in P-N junction diodes follows a logarithmic trend, in diode-connected MOS transistors, the voltage drop changes with a square root behavior.

The voltage drop across a diode-connected MOS depends on the threshold voltage, and the overdrive voltage needed for the current flow. MOS threshold voltage strongly depends on the process used and operating temperature. Typical value is 500-800 mV and it is comparable with the forward-bias voltage of a P-N junction diode [127]. By selecting MOS transistors of given sizes in the diode-connected arrangement, an inevitable trade-off between parasitic capacitance, substrate leakage and on-state resistance results in some compromise between operating speed, power efficiency, and load current handling ability of the rectifier [178].

The substrate leakage is not significant in MOS diodes except when the reverse diode voltage is close to the gate oxide or junction breakdown voltages [47]. However, these diodes are not suited for high frequency applications as they have a wide depletion region [91]. Authors in [78] conducted comparative studies over various rectifier structures evaluating their associated parasitics, I-V curves, leakage current and output voltage. They compared P-N junction diodes, Schottky diodes, diode-connected nMOSs, body-controlled diode-connected pMOSs, pMOS diode-connected transistor with its source and body connected together (V_{SB}=0), and high voltage nMOSs.

nMOS transistors connected as diodes may be preferred over their pMOS counterparts due to their higher g_m resulting in higher current handling. However, the body-effect further increases the threshold voltage of nMOS transistors during their operation. Authors in [99] proposed an alternative method to reduce this effect using an additional diode-connected pMOS transistor with a source body connection in parallel with the nMOS transistor. The output power of this rectifier is reported to be improved.

2.3.2 Conventional Topologies for Passive Rectifiers

2.3.2.1 Half-Wave Topology

A half-wave rectifier permits half of input AC signal, either the positive or the negative cycle, to pass toward the output node, while the other half is blocked. The conduction phase depends on the polarity of the rectification element. In many recent biomedical implant designs, the rectifier block uses a half-wave topology implemented using substrate or off-chip diodes [15,85,117,156-157,168]. When implemented using nMOS transistors, a half-wave rectifier is subject to increase in the threshold voltage of the diode due to its body effect.

Depending on the application, some other topologies are introduced for half-wave rectifiers, which lead to significant improvements in power efficiency. For example, authors in [168] suggested using a dual diode based topology for the rectifier in a biphasic stimulation application to generate dual supply voltages. Here, only one of the stimulators is active at any time and therefore, only half of the total power is wasted. This type of scheduling reduces some unnecessary power consumption that would be induced in shunt regulators located right after each diode. Therefore power consumption can be optimized by changing the arrangement of rectifiers depending on the load requirements. It is shown that for the same load power, the equivalent resistance in dual-diode topology is one fourth of the single diode case and the equivalent AC load current is twice larger. This approach is reported to significantly reduce the power dissipated in the regulator in a single diode based topology. However, the improvement in the overall power efficiency has been obtained at the price of an extra diode and capacitor. It is noted that the proposed design exhibits less voltage conversion ratio compared to its conventional single diode rectifier.

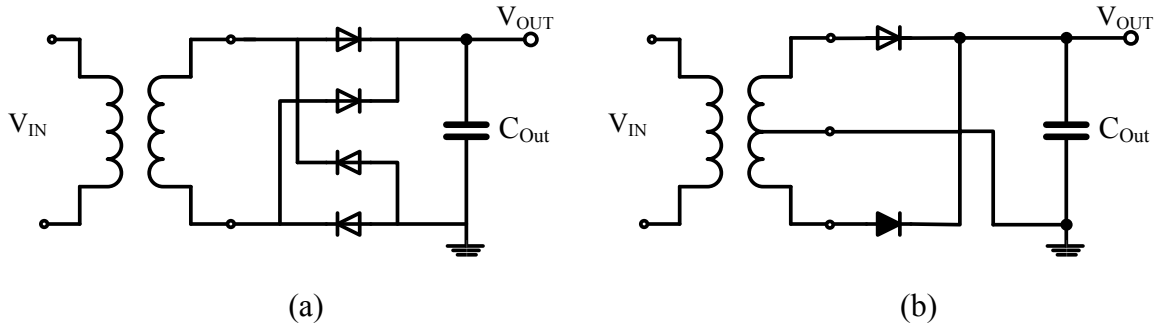


Figure 2.2. Circuit diagram for a full-wave rectifier: (a) bridge, (b) center-tapped.

Nevertheless, since half-wave rectifiers are used every half of input cycle, they are not the most power efficient and their PCE and VCR is limited by the voltage drop across the diodes.

2.3.2.2 Full-Wave Bridge Topology

A full-wave rectifier converts whole input waveform to a fixed polarity (positive or negative) at its output. For a center tapped transformer (Figure 2.2b), two back-to-back diodes form a full-wave rectifier. Here, during each half cycle, one of the diodes will be forward biased, and the input voltage will be delivered to the load. In a circuit with a non-center tapped transformer (Figure 2.2a), four diodes are required. This arrangement is called a diode bridge rectifier. In the bridge topology, when the input amplitude is higher than the output voltage, a diode conducts to deliver power to the load and another diode provides a return path to ground. The bridge structure, when compared to a conventional half-wave topology, benefits from a higher power efficiency, smaller output ripples, and higher reverse breakdown voltage. It can also provide a larger average (DC) output voltage than its half-wave counterpart [1,83]. Full-wave topology however suffers from having forward-bias voltage drop of two cascaded diodes in each signal cycle. This causes considerable losses in AC-to-DC conversion when the input voltage is small).

Authors in [27] and [54] have built a bridge rectifier using nMOS diode-connected transistors with a p-well CMOS process (Figure 2.3). The former design is reported to properly work up to 50 MHz source frequency while providing large (2 mA) load current. The bulk of the MOS transistors for both designs are connected to the rectifier output. This bulk biasing subjects some drain/source to p-well diodes to be intermittently forward biased in the operation of the rectifier, and therefore, the obvious latch-up hazard and leakages into substrate is reported.

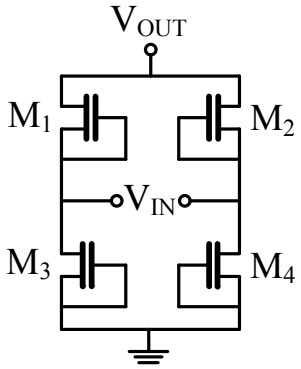


Figure 2.3. Circuit diagram for a full-wave nMOS-based bridge rectifier.

To solve the problem associated with the bulk biasing of the diode-tied MOS transistors, a full-wave rectifier circuit using pMOS transistors is introduced in [124]. Here, the bulks of MOS transistors are dynamically biased to higher available voltages in the circuit. The rectifier was reported to be successfully tested with sources of up to 350 MHz frequency.

The full-wave bridge topology however suffers from the forward-bias voltage drop of two diodes in each signal cycle. This causes an inherent voltage drop at the output of the rectifier which will degrade PCE and VCR especially in low-voltage applications.

2.3.3 Advanced Passive Bridge Rectifiers

As we saw in the previous section, conventional integrated topologies use two pairs of MOS transistors, connected as diodes, to implement a bridge rectifier. In such structure, for each input source cycle and depending to its polarity, a pair of diodes turns on in series with the input RF signal. A popular circuit topology for bridge rectifier employs the use of one or two pairs of diodes in a gate cross-coupled configuration. Depending on the representation of gate cross-coupling scheme, these rectifiers are categorized in different groups. Authors in [178] have studied different bridge and gate cross-coupled structures.

2.3.3.1 Partially Gate Cross-Coupled Topology

In a partially gate cross-coupled rectifier (PGCCR) topology, two diodes of the conventional bridge rectifier are replaced by two gate cross-coupled MOS transistors (Figure 2.4). Here, the

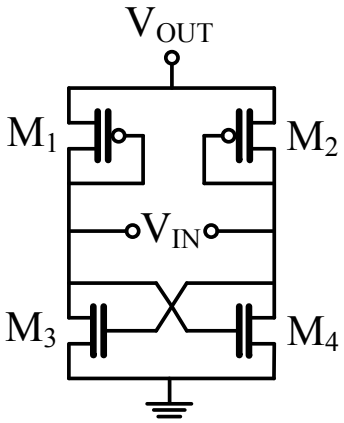


Figure 2.4. Circuit diagram for a gate cross-coupled rectifier.

positive feedback from the cross-coupled nMOS pair ensures that the positive side of the input AC signal will be connected to the load, while the negative side will be connected to ground. The cross-coupled transistors are directly driven by the input presenting a higher voltage swing at the input. Using the cross-coupled configuration the voltage drop across the cross-coupled MOS pair depends on the flowing current level, and if it is sufficient and the transistors are properly sized, this drop voltage can be lower than the threshold voltage.

Authors have suggested different versions of this topology using all pMOS [126,136,144], and complementary arrangements with cross-coupled nMOS [2,8,47-48,53,60-61,114,154] switches. It is however reported in [121] that CMOS rectifier circuits can reduce parasitic capacitance at the input node compared to nMOS and pMOS only rectifier circuits leading to lower leakage. However, the GCCR topology suffers from at least one threshold voltage drop across the diode-connected MOS transistors.

The overdrive voltage of pMOS in the bridge topology is much lower than nMOS in the gate cross-coupled topology. Moreover, nMOS devices have higher electron mobility than the pMOS counterparts. With these reasons, the gate cross-coupled circuit is smaller in size, has a lower turn-on voltage and a smaller voltage drop over the standard bridge structure. However, due to operation of lower nMOS switches in the linear region, the nMOS cross-coupled topology experiences higher switching losses, which become significant at high frequencies. Nevertheless,

the bridge topology is better suited for high voltage and low current applications while the PGCC structure is useful in low voltage and high current applications [178].

On the other hand, since the source nodes of all rectifying MOS transistors in PGCCR structure are connected to the input terminals, it is crucial to protect this circuit against substrate leakage and possible latch-up. This can be achieved by preventing the vertical parasitic P-N junctions from turning on. Therefore, the body potential of cross-coupled transistors should be dynamically controlled. Authors in [2,47-48,52-53] suggested to apply the DBS technique to reduce leakage through substrate and eliminate the body effect.

The authors in [48,52,8,53] have suggested an enhanced version of the PGCCR employing diodes placed in parallel with diode-connected transistors to improve the return current form the load to the source. The diodes were implemented using parasitic diodes available in the targeted process.

2.3.3.2 Fully Gate Cross-Coupled Topology

The problem associated with threshold voltage of any diode-connected MOS transistors in PGCCR is overcome with the use of a fully gate cross-coupled rectifier architecture (FGCCR), where each pair of MOS switches in the bridge-like topology is cross-connected. Various authors have called this arrangement the differential driver rectifier [92-93,143], the self-driven synchronous rectifier [111], and the differential bridge rectifier [43-44,46].

In FGCCR topology, as shown in Figure 2.5, all of MOS transistors act as switches and consequently the circuit is no longer constrained by the voltage drop across the diode-connected MOS transistors, but only by the drain-to-source voltage drop of switches. The design also benefits from the highest available swing at the switches to provide lowest channel resistance. Therefore, the FGCCR topology can deliver significantly higher output voltages compared to the PGCCR topology. Furthermore, for very low input power levels the adopted FGCCR circuit maintains superior power efficiency compared to the PGCCR. It is important to note that the RF input amplitude should be greater than the threshold voltage of MOS transistors to activate the rectifier.

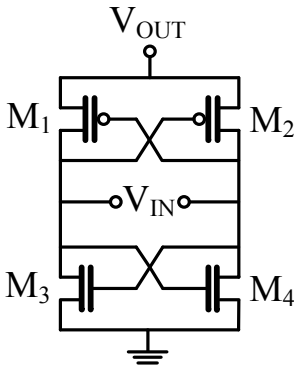


Figure 2.5. Circuit diagram for a fully gate cross-coupled rectifier in [43].

However, there exists a significant period of time in every cycle, where the output node potential is higher than that of the input node. When this happens, the cross-coupled pairs cannot be turned off completely, thereby causing charge leakage from store-charge capacitor back to the input source. In addition, the rectifier circuit does not have a stable supply voltage that can guarantee the highest potential in the system. Therefore, if pMOS body terminals are tied to a fixed potential, the source-body (or drain-body) diodes of pMOS transistors may be forward-biased. Authors in [89,160] have thoroughly investigated such reverse currents.

To suppress this leakage current while retaining the low turn-on levels, the circuit topology

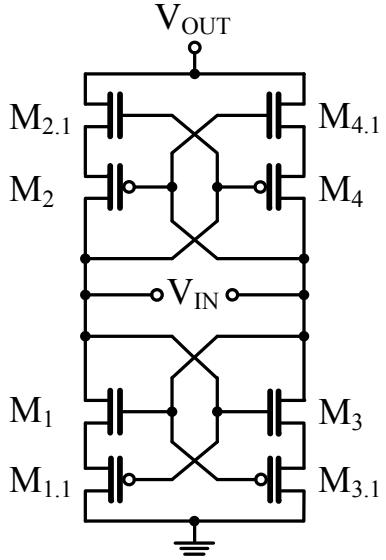


Figure 2.6. Circuit diagram for a fully gate cross-coupled rectifier in [160].

has been modified by the addition of four more low-threshold transistors, as shown in Figure 2.6 [160]. However, as the additional transistors are inserted along the main current path, they should be of the same size as the main switches. This implies doubling the number of main transistors which leads to doubling the conduction and switching losses and the area consumption. As the main switches conduct, the auxiliary switches form diode-connected transistors, which result in a voltage drop equal to their threshold voltage. This voltage drop is added to the drain-source voltage of the main switches and increases the voltage drop at the output, even higher than the conventional FGCCR structure.

Authors in [116] presented a comparison between different rectifier topologies including a diode bridge, partially and fully gate cross-coupled rectifiers and a voltage doubler in terms of power efficiencies and voltage conversion ratios for different input amplitude and load conditions.

2.3.3.3 Charge-Pump Based Rectifiers

A charge-pump, also called a voltage multiplier, converts some received AC or DC input voltage to a stable DC output voltage. Depending on the type of input, charge pumps can be classified as AC-to-DC or DC-to-DC converters. A typical AC-to-DC charge pump circuits used in power harvesting systems and RFID circuits consist of multiple rectifier cells in a stacked configuration. Here, packets of charge are transferred through clocked switches from the source towards the output storage capacitor. The output powers of this family of rectifiers are often limited due to constraints on the quantity of charges that can be transferred per unit of time, and on the size of the storage capacitor [173-174].

Single stage rectifiers based on the Villard charge-pump that is composed of a capacitor and diode combination was suggested for various applications in [40,83,163,177]. This structure has

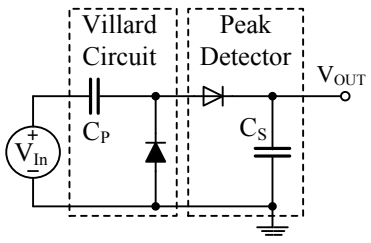


Figure 2.7. Schematic of a Greinacher charge pump.

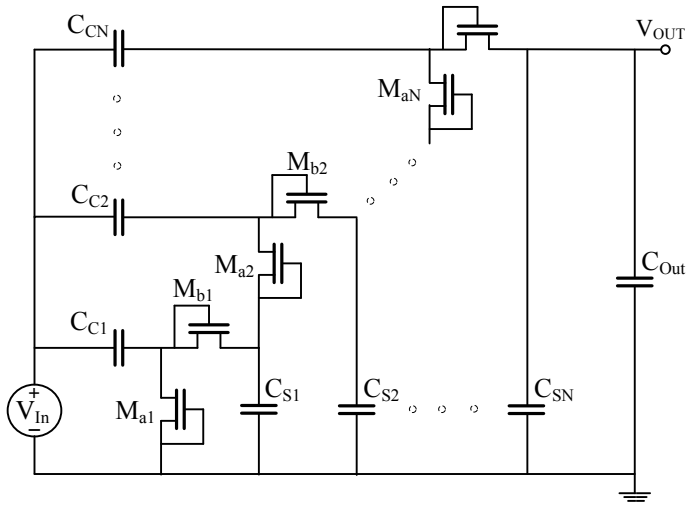


Figure 2.8. Schematic of a N-stage charge pump rectifier.

very poor ripple characteristics. Greinacher charge-pump (Figure 2.7) works by following a Villard cell stage with a peak (envelope) detector stage. The ripple for this structure is much reduced.

However, when the input amplitudes are low, a single rectifier stage does not usually produce an output voltage that is sufficiently high. In that case, a number of charge-pump stages can be cascaded in a rectifier topology to increase the output voltage (Figure 2.8). Here, the AC or RF inputs are fed in parallel into every stage through pump capacitors and the outputs add up in series, to produce the final output voltage [7,39,86,108-109,173,]. However, since the inputs of individual stages appear in parallel, the equivalent input impedance is divided by the number of stages. On the other hand, the number of stages should be kept to a minimum to avoid excessive leakage through the parasitic junctions and capacitors [40]. Hence, a suitable trade-off between the output voltage level and the overall power efficiency of the charge pump must be made when determining the number of stages.

Some charge-pump rectifiers use Schottky diodes [12,86]. Reference [86] presents an example of some optimizations made on the number of stages, the size of diodes, and the size of coupling capacitors.

There are rectifier circuits consisting of charge-pump stages that make use of low-threshold MOS transistors as switches [34,38,90,106,109,170,173-174]. Many charge pump designs [28,42,99,121-122,169,175] have been suggested where the threshold voltage of the main switches are compensated using V_{Th} cancellation techniques. Detailed discussions about this family of rectifiers will be presented in the next section.

The frequency response of a rectifier is typically a bandpass. The low-frequency cutoff occurs when the impedance of the pump capacitor becomes comparable to that of the load and the high-frequency cutoff is determined by the impedance of the package and by the input capacitance [111] of the rectifier. Authors in [38,40,163-164,176] have reported rectifiers operating in the gigahertz frequency range.

The power efficiency of a rectifier also depends on the amplitude of the input RF signal. Larger voltage amplitudes often enhance the power efficiency of rectifiers. However, when exceeding a certain input amplitude, the power efficiency of the rectifier may decrease due to the increase in leakage currents [7]. There is also a tradeoff between the output current and PCE of charge-pump based rectifiers. Furthermore, based on the derived equation for the transconductance of a MOS switch, there is an optimal size (W/L) for transistor based rectifiers that produces maximum PCE. Size of switches may also affect the output voltage and the settling time of a rectifier [173-174].

Power efficiency can be improved by a careful selection of the number of charge-pump stages and the size of switches and capacitors [33,86,177]. The voltage drop across the charge pump switches is determined by the drain current, reverse bias leakage current, parasitic components, and body-effect of the transistors [33].

Charge-pump based structures generally suffer from large output ripples. This makes them incompatible with applications where a stable output voltage is required unless a regulator stage is used [173-174].

For a rectifier implemented using nMOS switches subject to high input amplitudes, the body-effect may not be neglected as it significantly reduces the output voltage and power efficiency. For those applications, source-body connected pMOS transistors with some threshold cancellation techniques may be used [108-109].

Authors in [78] have studied six different charge pump structures: diode connected nMOS, high voltage nMOS, body controlled diode-connected pMOS, P-N junction, Schottky diode, and pMOS diode-connected transistor with a source to body connection. They compared them in terms of associated parasitics, I-V characteristics, leakage currents, and output voltages.

A common problem associated with voltage multiplier based rectifiers is that they provide current to the output node only during the positive half-cycle of the input (charge transfer phase). During the negative half-cycle (clamping phase), the parallel diode helps pre-discharging the clamping capacitors to ground. This phenomenon reduces the overall PCE of these types of rectifiers [137].

There are also several other charge-pump based topologies such as switch-only [64,96,137], bias-flip [137-138] and resonance [22,64,110,141,159] for passive rectifiers developed for special applications, Some of these topologies significantly improve the power efficiency. They are typically constrained by large inductors in the 10's μH range to be efficient. Such inductors are of course not implementable in standard CMOS processes.

2.4 Rectifiers with Threshold Cancellation Techniques

The MOS threshold voltage, V_{Th}, is defined as the gate voltage for which an inversion layer forms at the interface between the oxide layer and the substrate of the MOS transistor. It is then a process dependent parameter which depends on the choice of oxide and its thickness. The threshold voltage of a transistor can be minimized by eliminating the body effect. To minimize this effect, the *W/L* ratio of the transistor must be increased as much as possible.

The rectifier must be highly sensitive to maintain its performance with low input amplitudes. For a rectifier implemented using high threshold voltages, the MOS transistors do not fully turn on with low input amplitudes. This leads to a high rectifier output resistance and a low output voltage [111]. The PCE of a rectifier circuit is mainly determined by the effective on-resistance of the MOS switches. The lower the threshold voltage of the MOS transistor, the lower its effective on-resistance becomes with the same input overdrive. Therefore, the large PCE and average (DC) output voltage are obtained if the threshold voltage can be minimized. On the other hand, when the threshold voltage of a MOS is too small, reverse leakage currents from the load

cannot be ignored. If some noticeable reverse current exists, it results in direct energy loss since charges flowing in a reverse direction are simply wasted. In addition, forward current must be increased so as to compensate the reverse current. As a result, excessive reduction in the threshold voltage spoils the advantage obtained by the reduction in the on-resistance and causes severe decrease in PCE. Thus, an optimal threshold voltage exists for which PCE of the rectifier is maximized. This threshold voltage is found to be in the range of 100-300mV [92-93,111,128].

Several standard CMOS processes offer so-called native transistors that have low threshold voltages [90]. Native transistors can be used to realize low-threshold designs, however these devices are subject to significant leakage due to their high channel doping. Moreover, their effective channel resistance for a weak input signal is still significantly high [16]. Thus, low-threshold devices are generally not very good candidates to be used as switches in the main path of the rectifier.

Therefore, it is essential to come up with design techniques at the circuit and system levels that can increase the voltage available for rectification or reduce the effective threshold voltage of the main switches. Various circuit techniques are available to alleviate the impact of high V_{Th} in standard CMOS processes.

2.4.1 Rectifiers Based on the Floating-Gate Technique

This technique was suggested to reduce the threshold voltage of MOS transistors by injecting charges into the floating gate (FG) of the transistor [23,100,111]. This can be done by applying a high voltage to the gate of the transistor to create a tunneling effect to trap the electrons in the oxide. The trapped charges act as a gate-source bias to reduce the effective threshold voltage of the transistor. The programmed charge is trapped for years on the completely insulated floating gate (about 0.1% leakage in 10 years @ 100 C°) [100,128-129]. The FG devices require a programming and erasing procedure, either by Fowler-Nordheim (F-N) tunneling, or hot electron injection supplied by a high amplitude sinusoidal signal source [100]. These devices are less area efficient compared to standard CMOS devices and they present a larger input capacitance [111].

For a floating-gate MOS device, the associated programming and erasing voltage varies depending on the required threshold adjustment speed and the allowable damage to the gate

oxide. The required programming voltages are reported to be as low as 6 V for large transistor sizes [128-129]. Therefore, depending on the technology in use, on-chip reprogramming may be possible at high input voltages. However, on-chip programming/erasing requires very large drain-source connected transistors. Furthermore, whether an on-chip programming and control circuit leads to a higher overall power efficiency needs to be investigated further.

Authors in [111] and [128-129] applied the FG technique to adjust the threshold of the MOS switches in partial- and full-gate-cross-coupled topologies. They have used single-poly standard CMOS processes for the fabrication of MOS switches. The first design presented in [111] reported voltages as low as 6.2V for programming and erasing the floating gates. It also measured no decrease in the output voltage at frequencies up to 13.56 MHz. The latter design reported in [128-129] uses cascaded FGCCR stages to increase the output DC voltage. In this topology, the first stage is directly connected to input alternative source and succeeding stages are capacitively coupled to input source, allowing the output DC voltage to build up at the output storage capacitor.

Authors in [100] have used FGMOS transistors to implement a multi-stage charge pump based rectifier operating at 916 MHz which can rectify input voltages as low as 50 mV. The high voltage range achieved at low load current makes it ideal for passively powered sensor networks. The design is capable of simultaneous programming of all FG nodes using both the F-N tunneling and hot-electron injection techniques. The output power of this circuit is reported to be significantly higher than other designs.

Floating-gate based rectifiers generally tradeoff lower transistor threshold voltage with increased device size and input capacitance. The programming process is slow and it can impact circuit reliability [42,111]. Moreover, the performance of the rectifier circuit may degrade with charges leaking from the floating gate over time and with temperature variations [16,100]. This is particularly true for deep sub-micron technologies where oxide layers are very thin and do not provide high isolation. During fabrication, the residual charges trapped in the floating gate (antenna effect) may also affect the threshold voltage of the rectifier circuit. Therefore, the floating gate must be programmed off-chip at least once to account for these unknown residual charges [16,100].

2.4.2 Static V_{Th} Cancellation Techniques

In this scheme, a static DC voltage is generated in an idle phase of the circuit to be used as a constant bias voltage to eliminate or reduce the effect of threshold voltage of MOS devices in the working phase. The fixed voltage source can be included either between the drain and gate of the diode-connected transistors [28,94,121,143] or the bulk and source [103]. The static voltage source may be supplied by an internal or external source.

2.4.2.1 External V_{Th} Cancellation Technique

Using capacitors between drain and gate terminals of the MOS transistors to alleviate the V_{Th} was originally introduced in [84] in the form of a varactor.

A high-sensitivity rectifier for semi-passive RFID tags was suggested in [161-162]. The rectifier includes a bias voltage connected between the gate and the source terminals of each nMOS transistor in a conventional Villard configuration. The voltage source for this circuit is supplied by an external pre-charged capacitor. The unit cell of the rectifier using the external V_{Th} cancellation (EVC) technique is shown in Figure 2.9. Using this scheme, the effective threshold voltage of each nMOS switch is decreased by the applied voltage (V_{bth}), allowing the rectifier output voltage to increase. The proposed rectifier is reported to be especially efficient at low input powers.

The scheme is however constrained by power consumptions of the internal circuit. For this configuration, it is measured that the rectification current increases with the bias voltage up to

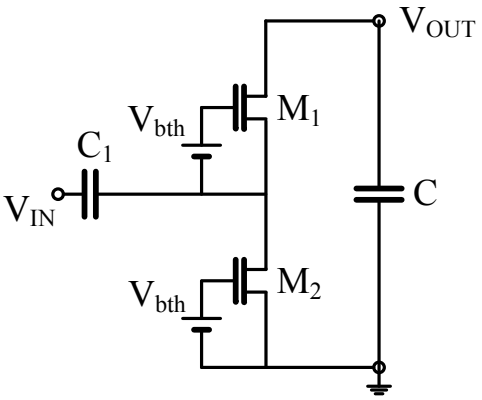


Figure 2.9. Circuit diagram for an external V_{Th} cancellation technique in [161].

certain value. Beyond this voltage level, the rectified current rapidly decreases due to significant leakage during the off-state of the rectifier. The scheme is not suitable for multi-stage configurations where each stacked transistor operates with a different potential. In such structures, individual voltage sources should be supplied which further complicates the implementation of the distribution circuitry.

2.4.2.2 Internal V_{Th} Cancellation Technique

Authors in [121-122] have studied the major factors contributing to power losses within a rectifier. They conclude that improving PCE requires that the input parasitic capacitance and threshold voltages associated with the MOS diodes are minimized. This is due to the fact that input parasitic capacitances form a leakage path for the incoming signal, and that the V_{Th} reduces the output DC voltage. In the same reference, they also present a technique, called the internal V_{Th} cancellation (IVC) technique, where an internally generated bias voltage is applied on the gate of MOS switches in the rectifier circuit. The IVC technique removes the effect of extra parasitics at the input terminals which are associated with the V_{Th} cancellation transistors. Figure 2.10 shows the circuit diagram for a half-wave rectifier using the IVC technique. Here, transistors M_p and M_n selectively decouple the parasitic capacitances of the IVC circuit from the input terminals. The gate-drain bias not only lowers the voltage drop across the MOS switches, but also shortens the turn-on time of the pMOS transistor, which leads to improvements in the high frequency performance of the rectifier [178]. The use of large bias resistors (R_b) forces the leakage currents of all diodes in this configuration to be negligible. This technique is able to also compensate for the impact of process and temperature variations in V_{Th}, if transistors M_{pb}-M_p and

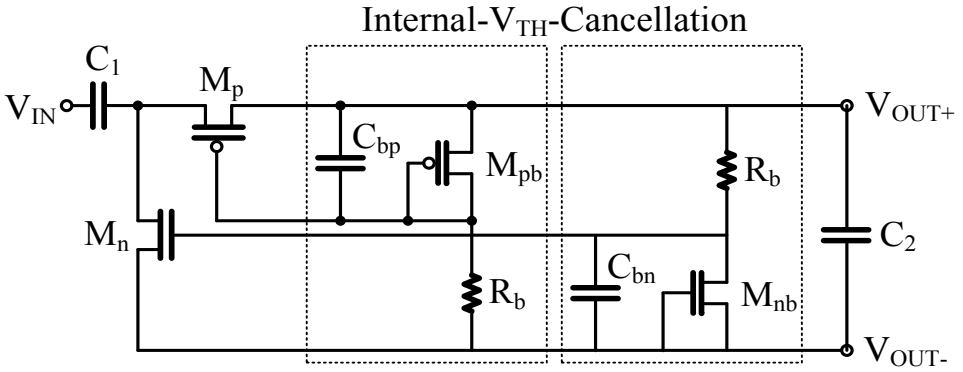


Figure 2.10. Circuit diagram for an internal V_{Th} cancellation technique in [121].

M_{nb}-M_n are matched. The proposed rectifier is reported to achieve almost twice the power efficiency of the EVC structure for large input power conditions. However, it suffers from poor PCE for small input power conditions [94].

Use of large bias resistors (few MΩ) implies a large die area and a decrease in the input power when the bias voltage drops rapidly [169]. Nevertheless, this technique is found to be less effective in reducing the threshold voltage, compared to the EVC technique [98].

Authors in [175] introduced a two stage rectifier based on the IVC technique, where a matching network is inserted. As a result, high power efficiency even at low power levels is achieved. Authors in [178] suggested a rectifier with PGCCR structure that achieved both high speed and high current handling capabilities. In this rectifier, by connecting gate and drain of the diode-connected pMOS transistors with a V_{Th} auto-generation circuit, the R_{ON} of the switches is decreased, and the switching time is reduced.

A rectifier circuit is proposed in [169], which uses a modified multi-stage charge-pump structure. A Self-bias (internal) feedback and the threshold cancellation technique are combined to reduce the voltage drop, increase the PCE, and reduce the effect of process variations. The diode-connected MOS transistors in a conventional rectifier are replaced by a new structure as shown in Figure 2.11. The structure includes transistors responsible for charge transfer (M_i), two auxiliary switches ($M_{1\text{-}2}$) to update the body voltage of M_i (DBS circuit), and a diode-connected pMOS (M_{pi}) to provide the bias voltage. C_P is used to filter the high frequency components and conserve charges to generate V_{Bias}. The multi-stage charge-pump also uses bias and switch blocks to generate the required bias voltages for odd and even stages. It is reported that using this architecture and properly adjusting the circuit, the threshold voltage is effectively eliminated, and an output voltage 2.5 times higher than the conventional charge-pump topology is obtained. The circuit does not need any extra power supply. However, it is also reported that the performance of the circuit is affected by the load, input magnitude, process and temperature variations. The bias voltage determines the opening time of charge-transfer transistor and has a great effect of the output voltage and power efficiency. Therefore, it should also be optimized according to the input power and the output load. The performance of the rectifier is significantly load dependent.

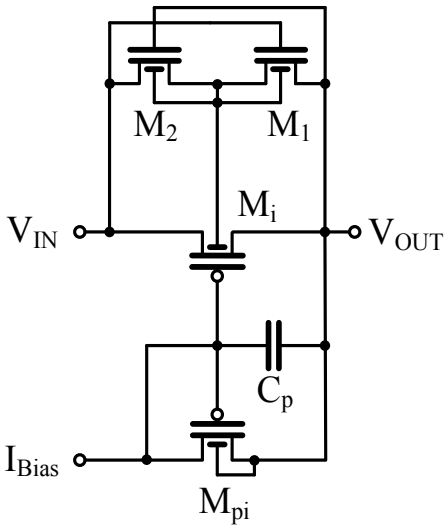


Figure 2.11. Circuit diagram for an internal V_{Th} cancellation technique in [169].

Based on the above design, a UHF (860-960 MHz) band multi-stage charge-pump rectifier for semi-passive RFID applications is introduced in [28], where each stage uses threshold cancellation and DBS techniques simultaneously. The rectifier includes a low power startup circuit which controls the system power supply by detecting the input power level. Bias voltage is applied using diode-connected transistors. The rectifier operates such that the main pass device turns on only if the input amplitude is greater than the output voltage. The generated bias voltage is used to compensate the threshold voltage of the main switch. The circuit, however, is constrained by the complex biasing distribution circuitry which is also power hungry. Similar to previous designs, the value of voltage drop across the main pass transistors should be set carefully to prevent any reverse leakage current. In optimizing the value of such voltage drop, process and temperature variations should be taken into account.

Authors in [42] introduced a multi-stage full-wave rectifier for RFID applications with a complementary architecture. The proposed converter replaces the diode-connected transistors with transistors operating in the triode region. Therefore, the output voltage is no longer constrained by the threshold voltage of MOS transistors, but the drain-to-source voltage across the channel which is significantly smaller. Capacitors are used between the gate and drain of the switches to overcome their threshold voltage, and DBS technique is also used to actively bias the bulk of level shifting transistors. Despite extensive care in sizing the charge transfer MOS

switches and the application of the DBS techniques, the design is reported to suffer from significant reverse leakage currents. Moreover, using complementary structures for positive and negative input cycles makes the circuit more complex.

Authors in [10] proposed a passive CMOS rectifier, called the driven-gate scheme, for RFID tags with improved sensitivity compared to the conventional diode rectifier. The design is similar to a FGCCR structure with a DC voltage source connected in series with the gate of the transistors to control their effective threshold voltage. It also uses a simple auxiliary driver, which drives the gates of the rectifier transistors with the same amplitude as the input with an adjusted DC level. The design benefits from a self-sufficient biasing scheme which is internally powered except at start-up. In this circuit, the on-resistance of the transistors is decreased by increasing the gate-source voltage of the switches. The power efficiency profile of the driven-gate rectifier is similar to that of a conventional FGCCR cell, except that its high efficiency region has shifted towards the lower input amplitudes. The value of this shift is proportional to the bias voltages applied by the biasing circuit. Despite its advantages, this rectifier suffers from reverse leakage current, extra power consumption by the large biasing circuitry, and larger die area.

2.4.2.3 Self-V_{Th}-Cancellation Technique

Authors in [94] have presented a self-V_{Th}-cancellation (SVC) scheme, based on the ULPD configuration for UHF RFID applications. This configuration is similar to a diode-connected CMOS rectifier (Villard), except that the gate-source voltages of the nMOS and pMOS transistors are biased using the output DC voltage and ground, respectively. This connection boosts gate-source voltages of the nMOS and pMOS transistors as much as possible. In other words, threshold voltages of the MOS transistors are decreased by the value of the output DC voltage. Figure 2.12b shows the circuit diagram of the conventional SVC-based rectifier.

Compared to the EVC and the IVC schemes, the SVC scheme is much simpler and requires no additional power. In addition, the SVC scheme can achieve the best V_{Th} cancellation efficiency at lower DC output voltage conditions. However, since gate bias voltage is directly supplied by the output DC voltage, PCE decreases under conditions of large DC output voltage. This is due to the increase in leakage currents resulting from reducing the effective threshold voltage of MOS switches. Therefore, PCE of the SVC-based rectifier first improves with any

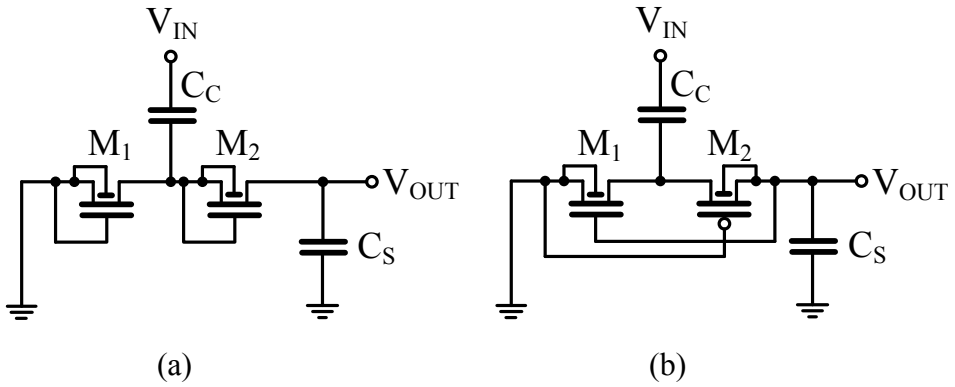


Figure 2.12. Circuit diagram for a Villard rectifier: (a) conventional diode-connected MOS, (b) ULPD-connected MOS in [94].

increase of the input power, and then decreases with further increases, reaching a maximum in between. Nevertheless, the PCE for a conventional diode-connected nMOS Villard rectifier is reported to be superior to the SVC-based CMOS rectifier when operating from very low input powers. This is because under extremely small input power conditions, the SVC mechanism cannot work well and the rectifier operates just like a conventional CMOS rectifier.

2.4.3 Differential V_{Th} Cancellation Technique

In a diode-connected MOS with V_{Th} cancellation, excess gate bias voltage results in the effective V_{Th} to be very small. In this condition, reverse leakage current cannot be avoided. It is therefore not possible to achieve a small on-resistance and a small reverse leakage current using a static V_{Th} cancellation scheme [92].

Authors in [92-93] introduced a multi-stage structure called the differential-drive CMOS rectifier which uses the FGCCR structure in each stage. Figure 2.13 illustrates the circuit diagram of the rectifier cell. Using a differential drive scheme in this topology, a dynamic gate bias mechanism is realized. The author claims to be able to automatically minimize the effective V_{Th} of diode-connected MOS transistors in a forward bias condition, and that this circuit automatically increase the V_{Th} in a reverse bias condition using a cross-coupled differential circuit configuration. This design is reported to have a higher output voltage compared to a single-stage topology, however its power efficiency is lower.

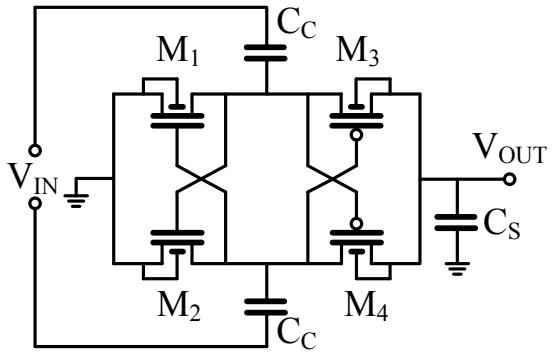


Figure 2.13. Circuit diagram for a rectifier cell using differential V_{Th} cancellation technique [92].

2.4.4 Bulk-Drive Technique

The threshold voltage of a MOS transistor is also a function of the bulk-source voltage (V_{BS}) as a result of the body effect. This voltage is normally greater than zero therefore increases the threshold voltage. To reduce the threshold voltage as much as possible, V_{BS} should be as high as possible.

The impact of bulk-driving technique was studied in [25]. It was found that this technique permits the implementation of analog circuits at supply voltages as low as the MOS threshold voltage plus approximately 200mV. It was also shown that this technique is constrained by its input capacitance and the noise.

Authors in [103] have suggested using a constant current forced out of the bulk terminal of the MOS transistor, called the current-driven bulk technique, to lower its threshold voltage. It is reported that the drain-bulk capacitance which initially subjects these circuits to poor high-frequency performance can be compensated by using additional circuitry. Using this technique, the possible voltage overstress, excessive power consumption, and noise coupling associated with a charge pump are avoided. The gain and input impedance reduction due to higher input capacitance associated with a bulk-driven technique are also prevented. This real time technique does not require special processing and calibration steps, however, implementing this technique requires additional circuitry to implement the current source and burns more power.

2.4.5 Bootstrapped Capacitor Technique

This technique is widely used in switched-capacitor (SC) circuits. It involves using the charges stored in a capacitor to reduce the effective threshold voltage of a MOS switch. This technique is well adapted in CMOS integrated circuits design, where implementing capacitors are feasible. Authors in [79-80] proposed the use of an nMOS gate cross-coupled bridge rectifier structure where the bootstrapping capacitors are connected to the gate of the main pass switches. Under the same load and source conditions, the proposed rectifier can achieve higher power efficiency and higher output voltage, compared to the conventional gate cross-coupled rectifier structure. However, the design suffers from charge sharing between the bootstrapping capacitor and the gate parasitic capacitor of the main pass switches. As a result, the power efficiency of the rectifier is degraded.

Authors in [118] presented a dual frequency band (UHF/HF) rectifier. It uses a bridge structure with a gate cross-coupled pair along with boot strapped switches. As a result, the minimum input peak voltage can be reduced to as low as 0.7V. However, the circuit has a complex structure and needs additional circuitry for start-up.

Authors in [99] have presented a low-frequency rectifier based on a voltage-doubler structure and the bootstrapping technique, as shown in Figure 2.14. Here, the effective threshold voltage of the main switches is replaced by the difference of two threshold voltages. This results in improving the power efficiency and increasing the output voltage level. However, this structure requires large off-chip capacitors in the µF range and generates load currents in µA range.

2.5 Analysis and Modeling of Passive Rectifiers

Rectifiers are nonlinear circuits with a complex startup process and a nonlinear behavior in the steady state, which is difficult to analyze. However, in early calculations an approximate linear model was used to analyze them for simplicity. In that simple model, the source resistance was neglected and the fall in output voltage due to the load was attributed to the finite reservoir capacitance. Authors in [145] considered the source resistance for thermionic rectifiers. Authors in [26] also took into account the source resistance and the finite reservoir capacitance. They were able to produce accurate results for output voltage, ripple content, and the peak and RMS

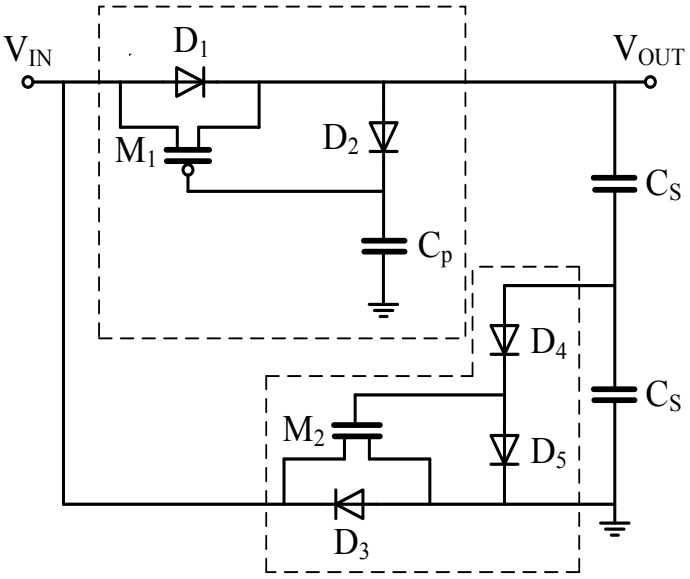


Figure 2.14. Circuit diagram for a Villard charge-pump based rectifier using the bootstrapping capacitor technique [99].

values of the source current. They assumed a constant source resistance and a constant load current for their analysis. In [65], the capacitor series resistance was also taken into account.

Therefore, analytical formulae have been derived for the common half-wave and bridge rectifier configurations, which enable us to evaluate the effect of their key parameters such as the source voltage and resistance, rectifier voltage drop, load impedance, and load current.

The Dickson equation appears most often in the published literature even though it is not enough. Authors in [174] considered MOS transistor sizes for a charge pump structure with ideal switches in their analysis. In this work, transistor currents were assumed to be equal to the DC loading current. In fact, transistor currents consist of pulses [88], and [174] gives an overestimation of the output voltage. In [39], an analysis of the P–N-junction diode rectifier was presented using special functions and an analytic expression was derived, but the effect of transistor sizing was not considered. In [33], a numerical time-domain analysis based on the MOS diode DC I-V characteristics is given. Calculations were found to be well-matched with the results extracted from simulations and measurements. However, little design insight could be gained from this numerical solution, and no design procedure was suggested. Authors used Ritz-Galerkin theory to develop a nonlinear analysis for the rectifier which incorporates the effect of

nonlinear forward voltage drop across the rectifier. This theory was first applied to predict the AC to DC conversion for single-diode rectifiers [66], and was later expanded to multi-stage rectifiers [39]. However, major design tradeoffs, such as number of diodes and their sizing and coupling capacitors are not apparent as the Dickson equation.

Authors in [13-14] analyzed the input impedance, input capacitance, and output resistance for diode voltage doubler and multi-stage rectifiers. Tradeoffs between device sizes and number of stages are presented with emphasis on low cost impedance matching.

Recently, an analytical expression of the DC output voltage of multistage UHF band rectifiers with appropriate approximations and incorporating the effect of the non linear forward voltage drop in diodes is derived [177]. It primarily concentrates on analysis of multistage rectifiers with diodes as rectifying devices and takes into account non-ideal issues associated with diode-connected CMOS devices such as: conduction angle, leakage current, body effect, and transistor sizes. However, this work does not consider the impact of impedance matching between the antenna and the rectifier circuit, which is very important in achieving a high PCE in the whole chain.

In [34,39,86], the inter-dependency of the input network and the AC-to-DC conversion equation are ignored. A complete model for multi-stage rectifiers is presented in [86] and a AC to DC conversion equation was derived. It also separates the fixed losses from the losses that scale with the number of rectification stages. The derived equation includes important effects of nonlinear forward voltage drop in diodes, and impedance matching between the antenna and the multi-stage rectifier.

In [177], a design strategy and power efficiency optimization method using diode-connected MOS transistors with very low threshold voltage is presented. The analysis takes into account the conduction angle, leakage current, and body effect in degrading the output voltage. Appropriate approximations allow analytical expressions for the output voltage, power consumption, and efficiency to be derived. Authors in [88], have discussed the charge redistribution loss of capacitors and its impact on the PCE of a charge-pump based design and have clearly defined the average output voltage.

Authors in [147-148] have presented an analysis method to determine the performance of any switched-capacitor power converter using easily-determined charge multiplier vectors. They considered the most commonly used converter topologies for their effectiveness in utilizing capacitors and switches. It covers the ladder, Cockcroft-Walton multiplier, Fibonacci, series-parallel, and doubler architectures for the rectifier. They noted that based on the performance of the investigated topologies in terms of slow-switching limit (SSL) and fast switching limit (FSL), some converters use capacitors efficiently and others use switches efficiently, but none of them are efficient in both. It was also reported that for converters designed using a capacitor-limited process, a series-parallel topology would work best, while switch-limited designs should use a topology such as the Cockcroft-Walton multiplier or the ladder topology. The exponential converters, such as the Fibonacci and Doubler topologies exhibit mediocre performance.

2.6 Active (Synchronous) Power Rectifiers

Unlike passive rectifiers, active (synchronous) rectifiers use active devices including switches, comparators, and possibly feedback to control the conduction in the forward path without a significant voltage drop and power loss. Figure 2.15 shows a typical structure for an active rectifier.

When the input voltage to the rectifier is higher than its output voltage, the comparator output goes to the positive supply rail and turns on the main switch to allow the charging of the output load. Conversely, when the input voltage of the synchronous rectifier is lower than the output

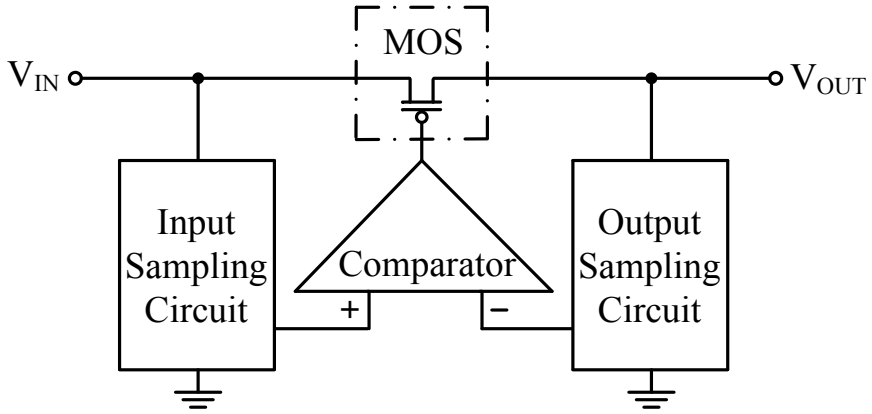


Figure 2.15. Block diagram of typical active (synchronous) rectifier.

voltage, the comparator output goes low, the switch is turned off and the forward conduction path is disconnected. Generally, active rectifiers are considerably more efficient compared to passive rectifiers in terms of output voltage and power efficiency [21,97,104,130] for low and medium operating frequencies. Medium to high output currents are very suitable for active rectifier because the current consumption of the comparator can then be almost neglected compared to the output current. However, implementing high efficiency comparators operating at very high operating frequencies, which is the case for many wirelessly powered devices working at Industrial, Scientific and Medical (ISM) band, is challenging. Bias generation for the internal circuitry is not trivial either since there is no DC supply at start-up. Active rectifiers mainly use regular MOS transistors as their main switch as they offer a linear characteristic for passing current, and a low voltage drop resulting in lower power loss.

2.6.1 Active Diode Concept

Active rectifiers rely on active diodes as their main building block to achieve high performance. The active diode works nearly as an ideal diode with almost zero reverse current and negligible voltage drop (typically about 20 mV) in forward operation. However, this advantage comes at the cost of static power losses associated with its quiescent current. If this power is excessive, it can outweigh its benefits in reducing the diode voltage drop. An active diode typically consists of a MOS switch and a control circuit to determine its conduction angle. The core of the controlling scheme is always a comparator. pMOS transistors are used as the main switch for active rectification as they do not require an additional start-up circuit.

The concept replacing conventional diodes with active diodes can be extended to all passive rectifier structures. This includes the classical bridge and the partially- and fully-gate cross-coupled structures. Active diodes are also reported to be used in charge-pump based architectures.

2.6.2 Main Challenges in Design of Active Rectifiers

Active rectifiers are constrained by the switching losses due to parasitics associated with the main pass switches and the comparator power consumption. Switches are often implemented using very large transistors to achieve low conduction losses (R_{ON}) and deliver high output

currents. Large parasitic capacitors are then inevitable, leading to losses along the main path that increase with the operating frequency of the circuit. The switching losses may even dominate conduction losses in the main pass switch. Moreover, large MOS switches are also subject to significant leakage currents through the substrate. Large parasitic and gate capacitances of the main switch affect the slew rate of the comparator making it less responsive to varying input signals. Thus, to obtain the best performance at a given operating frequency, the rectifier size and the comparator drive capability should be scaled appropriately.

Comparators used within the active rectifier circuit are subject to an intrinsic delay. This parameter makes it difficult to instantly switch the state of main pass switches. During such time intervals, reverse leakage current may flow, resulting in power deficiency. Increasing the comparators speed comes at the cost of increased power consumption which harms the overall PCE. Output ripples are determined by the gain of the comparator, the value of the load capacitor, and the carrier frequency. These parameters set another boundary in performance optimization for the active rectifiers.

The power supply voltage of the comparator directly affects its performance. Increasing the supply voltage of the comparator reduces the on-resistance of the controlled MOS switch, and increases slew rate while also increasing the losses through its circuitry. Some active architectures use the voltage stored in the output capacitor to supply the comparators. In this case, any change in the input amplitude and load conditions, may cause changes in the comparator performance and affect the overall PCE.

The maximum input frequency of the active rectifier is limited by the characteristics of the comparator used within its structure. The speed of the comparator is a function of its quiescent current, which depends on the supply voltage. As a result, the design of the comparator is the most critical part in designing an efficient active rectifier. Generally, a fast comparator with low power consumption is selected, and other characteristics such as unity-gain bandwidth, open loop gain, slew rate, and static power consumption are adapted to the application.

The number of comparators used in the rectifier structure also affects the performance of the rectifier. Various designs with different number of comparators have been introduced which will be presented in the following sections. As a result of the above challenges, active rectifiers are

mainly implemented for relatively low frequency applications with minimum input amplitude of 1.5 V [128-129].

2.6.3 Active Rectifiers with Conventional Topology

Authors in [29] suggested using two active diodes with very low forward voltage drop to replace the pMOS transistors in the PGCCR structures presented in [47,144]. As a result, the dropout voltage is reduced compared to a conventional bridge rectifier and the overall power efficiency and output voltage is increased. Nevertheless, two diode-connected transistors still exist in the main path of the rectifier, limiting the performance improvement. This circuit is also constrained at start-up when there is no voltage to turn on the main switches. Moreover, increased internal losses at high output voltage and load currents will make the power efficiency sensitive to the input amplitude levels.

Motivated by previous work, [56] suggested using two symmetrical parts, same as in [29], with the exception of additional nMOS transistors to provide a conduction path to ground. Auxiliary transistors are inserted to control the bulk voltage of the main pass transistors (DBS). The rectifier, compared to previous structures, presents higher PCE and VCR, and maintains its performance over load and carrier frequency variations. However, it produces relatively high ripples due to longer turn-off time.

An alternative design proposed in [97] where the diode-connected MOS transistors of conventional PGCCR topology are replaced with active diodes (Figure 2.16). Each active diode is realized by an nMOS transistor controlled by a 4-input comparator. These comparators are designed to be self-powered and biased by the unsteady and distorted voltages appearing at the input source terminals. The supply voltage is provided by charging a small capacitor through a diode-connected MOS transistor (auxiliary path) which improves the rectifier performance at startup. A feedback scheme, introducing an arbitrary offset current to the comparator is also suggested. The offset current helps in effectively reducing the delay of the comparator which in turn results in significant decrease in the amount of reverse leakage current. As a result, the design exhibits smaller ripples, less dropout voltage, higher DC output voltage, and higher PCE compared to a conventional PGCCR structure. The minimum input voltage is as low as the sum of the drain-source voltage of nMOS and pMOS transistors in their linear region. The total drop-

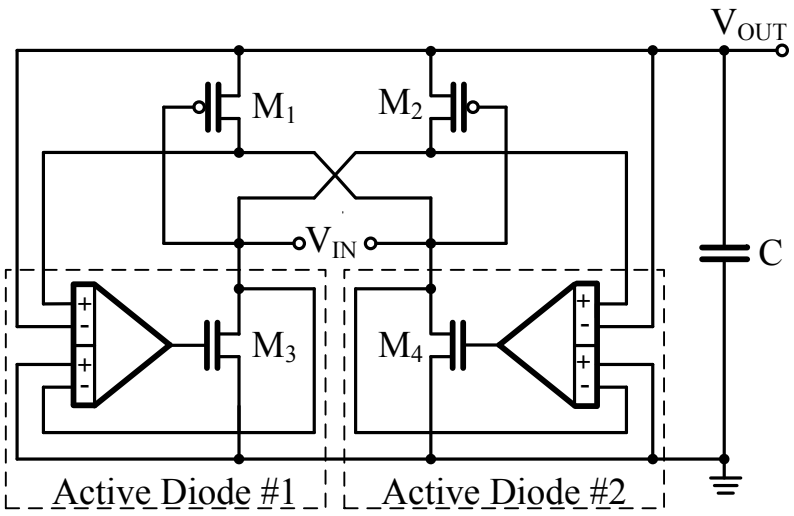


Figure 2.16. Circuit diagram for active rectifier in [97].

out voltage of the rectifier is equal to the sum of the threshold voltage of nMOS and pMOS transistors (almost 1.5 V). However, the power consumption of the proposed design is very high (260 μW) even for a working frequency of 1 MHz.

Since the comparators do not use an external supply and they are connected to nMOS transistors, and considering the variations in the input amplitude over time, there are time intervals in which, the main pass nMOS switches cannot be turned on completely leading to a significant reverse leakage current. To solve the problem, a semi-active rectifier with cross-coupled comparators is introduced in [89]. The cross-coupled comparator structure helps procuring a larger input voltage swing compared to the former design. This topology was used for a multi-stage rectifier.

Authors in [104], proposed an active diode which utilizes a MOS switch, fast comparators, and a conduction angle regulating circuit (one-shot). The conduction angle regulator can generate pulses with varying widths corresponding to given load and source conditions. The design uses passive diodes located in an auxiliary path to generate enough voltage for startup, when there is no power supply for the comparators. Figure 2.17 shows the structure of the active diode with its automatic angle control. The voltage comparator detects if the on-chip diode is starting to become forward biased to trigger the pulse width regulator, which closes a switch in parallel with the diode. The contribution of the new path in the load current dominates the diode path due to its

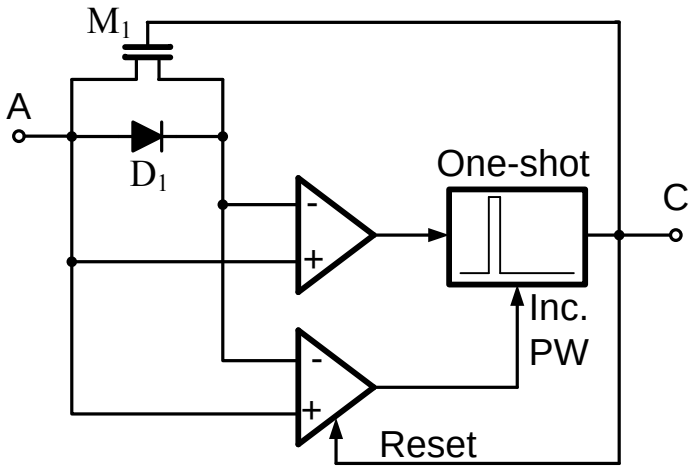


Figure 2.17. Circuit diagram for active rectifier in [104].

very low channel resistance. The proposed active diode was then used to replace the conventional diodes in charge-pump and bridge configurations. In the later configuration, 4 comparators are needed. The rectifier likely needs to employ a complex pulse width regulation circuit. This is due to the fact that pulse length depends on the voltage difference between the input and the output and it must be carefully changed accordingly. The proposed topology, when used in a bridge structure, also requires four additional 100kΩ resistors in the power stage to tackle the synchronization problem which makes its implementation area consuming.

Another active rectifier for three-phase micro generators is suggested in [135]. It is arranged based on a multi-phase bridge structure where the conventional diodes are replaced with active ones. The rectifier requires 6 comparators, two for each phase, which are supplied by the output voltage. An additional circuit is also used to provide power at startup. The operating frequency of the rectifier is reported to be in 10-100 kHz range.

Authors in [60-61] introduced a new synchronous rectifier using the PGCCR structure. It uses an integrated peak selection circuitry which selects the peak voltage generated from a multi-electrode transducer. This dual input rectifier consists of two CMOS controlled rectifiers with their outputs connected together. In this design, the gates of main MOS switches are effectively controlled by the voltage at their sources. Therefore, the phase relationship between input terminals can be arbitrary. This is unlike the conventional gate cross-coupled rectifier where

input terminal voltages must be equal in amplitude and in opposite in phase. For low operating frequencies and a wide range of load conditions, the proposed rectifier has a substantially higher power and voltage conversion efficiencies compared to the conventional PGCCR topology. However, its power efficiency is degraded with very low and very high load resistances and its output ripples are larger.

Authors in [149-150] proposed an active rectifier to harvest energy from an electromagnetic shaker. It uses a bridge topology with three comparators. The lower two transistors of the bridge are gated complementarily by a hysteretic comparator. The upper transistors of the bridge run independently and are controlled by comparators continuously sampling the voltage across each of the switches. Comparators are powered by an internal battery specially at start up. The rectifier was tested in the 100-1000 Hz range and it delivers a peak power efficiency of 88% at an input amplitude of 2.7V.

Authors in [62-63] suggested an efficiency-enhanced CMOS rectifier for the transcutaneous power transmission in high-current biomedical applications. The design uses the PGCCR structure, where pMOS switches are cross-coupled and nMOS transistors are controlled by comparators (Figure 2. 18). The comparators are implemented using an unbalanced-biasing scheme, resulting in the nMOS switches to be turned off earlier, compared to that in typical active designs. Although the shorter conducting time can increase the input current of the rectifier and lead to an increased dropout voltage, the increase in the input current is offset by decrease in the leakage current of the rectifier. The proposed rectifier is self-supplied and can source a large

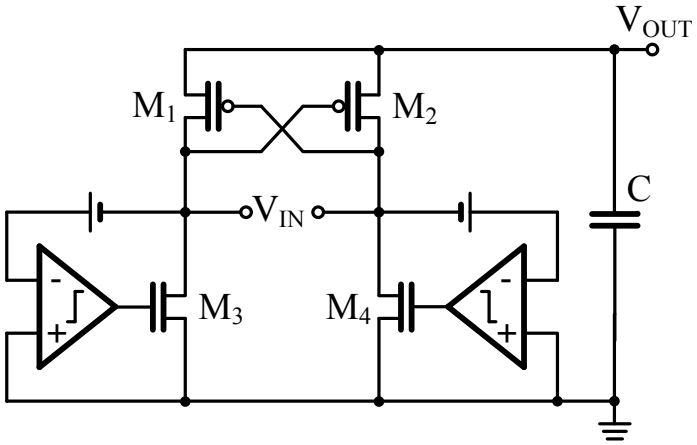


Figure 2.18. Circuit diagram for active rectifier in [63].

output current (up to 20 mA). It operates with low input amplitudes (1.2 V) and achieves very high voltage conversion ratios and power efficiencies. However, the structure requires large resistors to realize unbalanced biasing for the comparators, which their implementation takes significant die area. These resistors should be accurately laid out, as their ratio affects the performance of the comparators. This structure requires special attention in layout and subjects the performance of the design to process variations. Moreover, the lowest input amplitude that the rectifier can process is determined by its output voltage, making its performance dependent on load conditions. The rectifier has a relatively long settling time which limits the range of input frequencies to a few MHz.

2.6.4 Active Rectifiers with a Charge-Pump Structure

Active rectifiers have also used charge-pump structures especially for RFID, biomedical stimulation and energy harvesting systems. The use of such structures helps to improve their startup performance by detecting lower amplitude sources. Authors in [80,152] introduced a half-wave active rectifier which employs a pMOS transistor as the main switch along with a switched capacitor voltage doubler. They also presented a synchronous full-wave rectifier which benefits from two conduction paths, including nMOS transistors controlled by active rectifiers. When the input voltage to the rectifier is higher than the output voltage, the upper active diode is activated, and when it goes negative, the lower dual circuit provides a conduction path between the input and ground. Two comparators, operating in sub-threshold region, with telescopic configuration are used which consume less static power. Each of the comparators requires a separate power supply of 2.5 V which is supplied by external sources.

Authors in [113] modified the rectifier in [99] by inserting an auxiliary diode-connected MOS in parallel with the main switch. The design uses the output voltage directly as the power supply for the active elements. Figure 2.19 depicts the circuit diagram for the proposed rectifier. During startup, the auxiliary diode-connected MOS transistor, M_3, provides charge transfer to the output. As the voltage rises, the active rectifier begins to operate with low performance. The active diode performance gradually improves with charging output voltage. A trigger circuit with hysteresis (not shown in the figure) is used to turn on the active part of the system once there enough energy is collected at the output. This circuit controls the conduction of a series MOS transistor placed

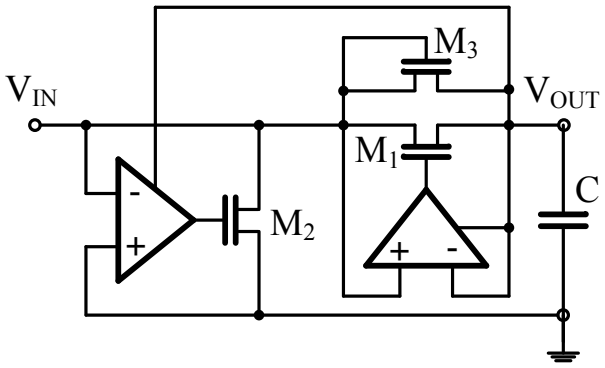


Figure 2.19. Circuit diagram for the active rectifier in [113].

between the input and output. In order to obtain the desired switching threshold voltage, the dimensions of the circuit elements for the trigger circuit should be carefully selected.

In many rectifier designs, similar to the above, active power is provided by charges stored in the output capacitor. This capacitor is normally charged through an auxiliary path, in parallel with the active diodes, to provide power at circuit startup. Passive diodes or diode-connected MOS transistors are widely used to implement such auxiliary paths. However, under certain conditions, the voltage across the storing capacitor is not enough to drive the MOS transistors in the comparator circuit. Moreover, the comparator performance may strongly affected by the process characteristics such as threshold voltage, offset voltage, and mismatch which could cause oscillation and/or waste of charges. To reduce these effects, authors have used the comparators with hysteresis transfer characteristics [16-20,35].

There are other active topologies other than conventional and charge-pump based rectifiers, mainly adapted for specific processes and applications and/or operating frequencies, and/or input source characteristics. For instance, DC-to-DC converter with adaptive dead-time control [112], dual-mode back telemetry using multiplexers [8,16,53], rectifiers with a predictive front-end [87], pulsed resonant [123,171-172] and rectifiers with a pair of comparators using a capacitive voltage divider to create phase-lead in the input of comparators [16-19].

Many applications, including biomedical stimulators [24,115,125] require high voltages. This voltage is preferably obtained from the input directly after rectification without using any additional DC-to-DC converters. To fulfill the high voltage requirements, IC processes with high

voltage capabilities are often required [119]. Two-chip (hybrid) solution with one high voltage IC for stimulation and one low voltage IC for other circuit functions is also suggested [115]. However, this solution may increase the complexity in assembling the implantable device and increase its form factor. While IC processes with both high and low voltage options can be used, the choices for such processes are limited and the performance may be compromised compared to advanced CMOS processes. Therefore, it will be advantageous if the high voltage circuits can be implemented using conventional CMOS processes.

In [102], a high-voltage voltage doubler employing a conventional PGCCR structure is introduced, where MOS transistors are controlled by active circuitry. High voltage operation is achieved by stacking a number of pMOS and nMOS transistors with their source and drain terminals connected in series. Diodes are implemented using n-well/p-substrate junctions which has a large breakdown voltage. The proposed technique allows the integration of a high-voltage rectifier with other low voltage circuits in a conventional CMOS process. This topology, combined with the use of deep n-well layer available in the advanced standard CMOS processes, serve for minimizing risk of potential latch-up. Nevertheless, the minimum input voltage is constrained by the threshold voltage of a diode and multiple drain-source voltage drops of the main and stacked transistors.

2.7 Active-Passive Power Rectifier Structures

There are rectifier topologies based on the multi-stage architecture where active and passive stages are used. Authors in [105,127,130-133] have introduced an ultra-low-voltage highly efficient integrated rectifier with only one threshold voltage drop for micro energy harvesters (Figure 2.20). The ability to convert nearly the entire voltage applied at the input to the output is the main advantage of this circuit. The proposed rectifier consists of two stages. The first stage is completely passive and is used to convert the negative half waves of the input sinusoidal wave into positive ones with nearly no voltage drop. This conversion is done with only four standard CMOS transistors, where no significant current consumption except for negligible leakages exists. In contrast to MOS diodes, no threshold voltage drop is seen between the input and the output of the first stage, but the drain-to-source voltage drop of the two MOS switches. An active diode second stage is inserted to control the current direction by blocking the reverse current

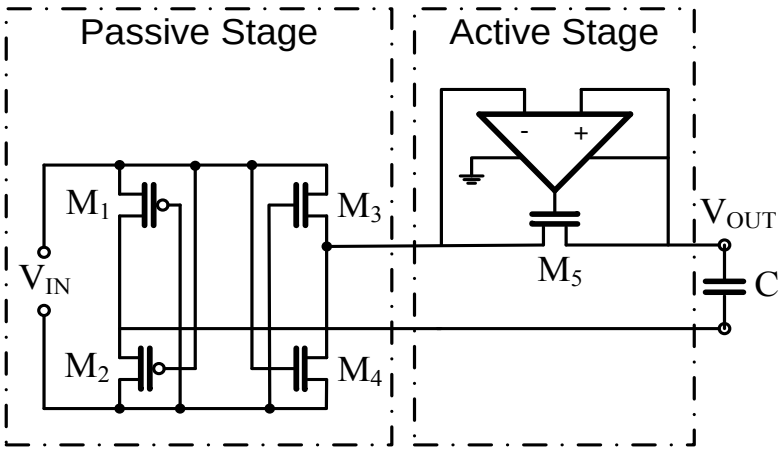


Figure 2.20. Circuit diagram for the active-passive rectifier in [133].

flow. It is implemented using a single multi-stage comparator consisting of a bias circuit and a bulk-input and output stage controlling a regular MOS switch. The biasing voltage is created using a common beta-multiplier bias circuit with start-up which is nearly independent form the supply voltage. The bulk-input comparator has very low power consumption and is well suited for low-voltage applications. The design employs low-threshold MOS transistors in the passive stage, and a dynamically bulk biased MOS transistor in the active stage. In the bulk-input stage, the bulk of MOS device is used as the input terminal while bias is provided at its gate. In order to ensure proper startup of the active diode over all process and temperature corners, an additional bypass pMOS diode (auxiliary path), is used in parallel. This bypass diode conducts only during circuit startup to charge the storage capacitor and remains in a high impedance state in other times. The active diode works nearly as an ideal diode, with current flowing in only one direction with nearly no voltage drop. However, this structure suffers from some current consumption.

It is reported that the maximum output power of the rectifier is 10 times larger than passive solutions and its voltage and power efficiencies are over 90% for operating frequency around 5 kHz. It also exhibits efficient rectification for very low input voltages down to 350mV [131-133].

Using a similar concept, a full-wave integrated rectifier was introduced in [105], where a simple low-voltage active diode is developed. The comparator uses an unbalanced transistor

scale, which makes the rectifier work with small input voltages. The bulk of the main pass switch is dynamically biased to avoid latch-up and to reduce the body-effect associated with it. This results in reduction of the dropout voltage across the active diode and the power consumption. The rectifier is reported to exhibits a peak in PCE and VCR of 87% and 93% at a very low minimum input voltage of 0.7V. The design is tested for operating frequencies between 100 kHz and 1.5 MHz.

Authors in [7,56,61,63,105,131] tabulated the major performance elements for different active and passive rectifier structures.

Conventional passive rectifiers, depending on their topology, are constrained by voltage drop across diode. However, they are capable of sourcing significant load current in mA range operating at very high frequencies with relatively low ripples. They do not need to power supply and do not consume static power. Charge pump passive rectifiers can generate high output voltages out of weak input amplitudes due to their stacked architectures. However, their PCE is deteriated with further increase in the number of stages and they fail to handle large load currents. Active rectifiers are the merit of choice for low and medium operating frequencies. They often need supply for their internal circuitry. Use of threshold conacellation technique significantly improves the PCE of passive rectifier if excessive care is paid is paid to control the reverse leakage current thought the main path switches. They are well-adapted with CMOS processes and can provide significant load charges operating in ISM band.

To summarize, conventional passive rectifiers, depending on their topology, are constrained by voltage drop across one or more diode. However, they are capable of sourcing significant load current in the mA range operating at very high frequencies with relatively low ripples. They do not need separate power supplies and do not consume static power. Charge pump passive rectifiers can generate high output voltages out of weak input amplitudes due to their stacked architectures. However, their PCE is deteriorated with further increase in the number of stages, and they fail to handle large load currents. Active rectifiers are often preferred for low and medium operating frequencies. They usually need an external supply for their operation. Use of threshold cancellation techniques significantly improves the PCE of passive rectifiers if extensive care is paid to control the reverse leakage current through the main path switches. They are well-adapted with CMOS processes and can provide significant load charges operating in ISM band.

Chapter 3 : A NOVEL LOW-DROP CMOS ACTIVE RECTIFIER

As explained in the previous chapters, the partially gate cross-coupled full-wave passive rectifiers use positive feedback to improve the conductance of cross-coupled MOS switches. However, they were constrained with the threshold voltage of diode-connected MOS transistors. This significantly impacts their overall power efficiency and reduces their output voltage.

It was also discussed that active rectifiers with relatively complex circuitry can be more efficient than their passive counterparts using low-loss MOS switches controlled by comparators to implement active diodes. However, it is found that the switching losses in the main pass MOS switches outweigh their advantages if operating at high frequencies. Quiescent current of comparators and the delay associated with them are also considered for further power deficiency. Furthermore, active rectifiers often need to provide supply voltages to the comparators which limits their application and increases their circuit complexity.

This chapter concerns the design and implementation of a new full-wave rectifier that uses active circuitry to control the conduction angle of low-loss MOS switches. The simple structure of the control scheme along with the use of a partially gate cross-coupled structure effectively reduces the losses and significantly improves the performance of the proposed active rectifier, accordingly. Use of inherent characteristics of MOS transistors as comparators in place of explicit comparators in conventional active structures is an advantage of the proposed rectifier. Thus, all main pass transistors behave as switches that offer very low voltage drops when used to perform AC to DC conversion. The proposed structure is self-supplied and therefore, no other supply mechanism is necessary. The quiescent current of comparators is also avoided even though there are some negligible leakage currents through the channel and junctions of MOS devices. Dynamic bulk biasing techniques are applied to the bulk of main pass devices to reduce their leakages in to the substrate. Using the TSMC 0.18 µm CMOS standard process, the consistency of the schematics- and post-layout-simulation results of the proposed active rectifier are demonstrated. Experimental results are also presented and they show good agreement with simulations. This work was published in Elsevier Microelectronics Journal and is reproduced as follows.

A NOVEL LOW-DROP CMOS ACTIVE RECTIFIER FOR RF-POWERED DEVICES: EXPERIMENTAL RESULTS

Saeid Hashemi, Mohamad Sawan, Yvon Savaria
Polystim Neurotechnologies Laboratory
Electrical Engineering Department
Ecole Polytechnique de Montreal, Montreal, Canada

Abstract *-We present, in this paper, a new full-wave rectifier topology. It uses MOS transistors as low-loss switches to achieve a significant increase in overall power efficiency and reduced voltage drop. The design does neither require an internal power source nor an auxiliary signal path for power delivery at startup. The highest voltages available in the circuit are used to drive the gates of selected transistors to reduce the leakages and to lower their channel on-resistance, while having high transconductance. The proposed rectifier was characterized with the SpectreS simulator under the Cadence environment and then fabricated using the standard TSMC 0.18 µm CMOS process. The proposed full-wave rectifier is particularly relevant for wirelessly powered applications, such as implantable microelectronic devices (IMD), wireless sensors, and radio frequency identification (RFID) tags. When connected to a sinusoidal source of 3.3 VAC nominal amplitude, it allows improving the power efficiency by 10% and the average output voltage by 16% when compared to other published results.*

Keywords **-** CMOS, F ull-wave r ectifier, P ower efficiency, S mart m edical d evices, R adio frequency identification (RFID), Wireless power transfer

3.1 Introduction

Many classes o f electronic d evices ar e subject to s tringent s ize constraints. A mong th em, smart imp lantable me dical d evices, lo w-cost pa ssive r adio f requency i dentification (RFID) t ags and w ireless s ensors h ave at tracted attention o f m any researchers [1–5]. In m any applications from t hese cl asses, a n i nternal pow er s ource s uch a s a n e mbedded ba ttery – in a ny form (disposable o r r echargeable) – cannot be a ccommodated. T his m ay b e due t o t heir l ow-energy

density, their limited lifetime, related hazards to human safety or degradation of their comfort. Powering such devices possess significant implementation challenges. Moreover, despite remarkable efforts dedicated to developing power scavenging techniques to harvest power either from environment or human body, these techniques are not yet considered as a reliable and feasible power source [6–9]. Nowadays, inductive RF links are a preferred solution to power up the considered class of devices. Typically, the same link is used both for power and data transmission [1–3]. Here, the lifetime of the system is no longer limited by the insufficient energy density of batteries. On the medical side, the infection risk is strongly reduced when there is no wire going through the skin. It is also of interest that there is no known negative aspects associated with telemetric exposure at moderate frequencies (< 20 MHz) [5]. However, this method of power transmission suffers from poor electromagnetic coupling, which results in a low power efficiency. Moreover, the value of the received power in the application is strongly affected by the distance and the relative orientation and displacement of the remote transmitter with respect to the implantable transponder.

3.2 Power Conversion Chain

Figure 3.1 shows a typical block diagram of a power conversion chain (PCC) for biomedical implantable devices (sensors and stimulators) [10]. The externally generated RF signal is captured by the secondary coil. This coil, combined with an integrated capacitor, form a parallel resonant tank, where the associated electromagnetic power induces voltage waveforms. The following wideband rectifier, along with the voltage regulator, converts these waveforms, which are typically sinusoidal, to a DC supply voltage. This supply is used to power up the core as well as output stages (signal processing and stimuli generation) circuitries located downstream. The

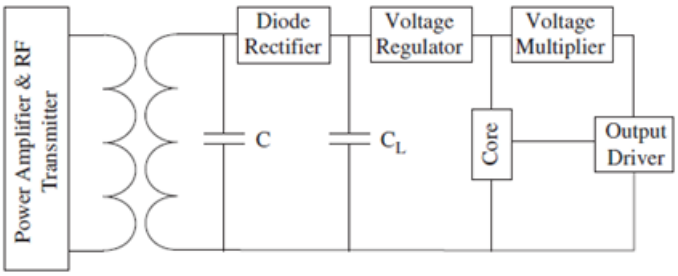


Figure 3.1. Block diagram of a typical PCC.

core of the stimulator, which is responsible for biasing, testing and various control structures is often implemented using digital circuitry. It is therefore powered from a nominal supply voltage for the given technology. However, as some functional electrical stimulation applications require voltages higher than those available by the digital core, a multistage voltage multiplier may be needed to boost the output voltage to the desirable levels.

3.2.1 Rectifier Implementation

Diodes or diode-connected MOS transistors are commonly used to implement rectifiers. Full-wave bridge structures are often used as they offer higher power efficiency, smaller output ripples and greater reverse breakdown voltage compared with their counterpart, the half-wave rectifiers. However, they are both constrained by the inherent diode/transistor forward-bias voltage drop (0.4–0.6 V). Such threshold voltage results in a significant power loss within the rectifier, which affects the overall power efficiency and decreases the delivered voltage to the following modules. This negative impact becomes increasingly significant in the design of low-voltage power supplies, which is the case for new sub-micron CMOS technologies.

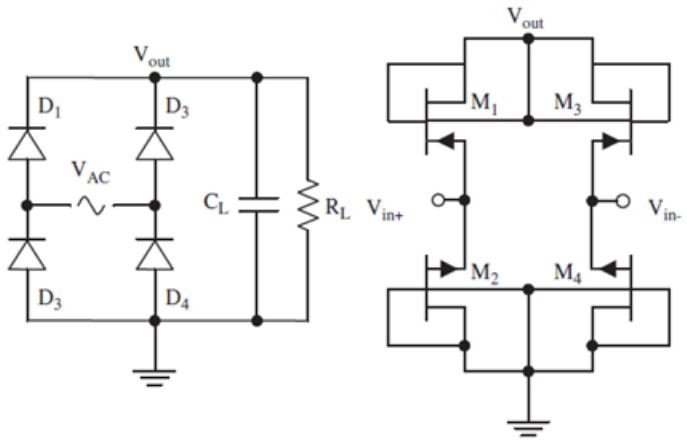
It is important to mention that a more efficient rectifier can deliver a given amount of power for a lesser voltage induced across the secondary coil. Thus, for a certain PCC, it requires a smaller coupling coefficient and allows for a greater relative distance between the coils.

On the other hand, Schottky diodes with a low forward drop (0.3 V) are possible but their implementation is expensive, due to the extra fabrication steps they imply as they are not available in standard CMOS processes [11].

3.2.2 CMOS Bridge Rectifiers

A conventional full-wave bridge rectifier along with a capacitor (Figure 3.2) converts both polarities of the input signal to DC.

The arrangement requires four diodes, where a pair of diodes is responsible for rectification in each signal cycle. When the input voltage is higher than the output one, a diode conducts to deliver power to the load and the other regulates the current path from the load to the ground. Although the structure, when compared to a half-wave bridge, benefits from a higher power



(a) (b)

Figure 3.2. Schematic of a full-wave bridge rectifier: (a) diode implementation, (b) MOS diode-connected implementation.

efficiency, smaller output ripples and higher reverse breakdown voltage, it suffers from having voltage drop of two cascaded diodes in each signal cycle.

In integrated circuits implemented with standard CMOS processes, the diodes are commonly replaced with diode-connected MOS transistors. A variety of conventional full-wave integrated rectifiers is addressed in [12] and their characteristics in terms of topology, size, breakdown voltage and current handling capabilities were reported. Here, the structures are still affected by the threshold voltage (V_{Th}) and instantaneous voltage drop across the transistor-based switches (due to their channel resistances), which degrades the overall power efficiency and reduces the output voltage. This drawback also makes the structure increasingly inefficient in advanced low-voltage submicron processes, where the ratio of the normal supply voltage to the threshold voltage of MOS transistors decreases.

Moreover, in diode-connected transistor-based active rectifiers (FWDR), V_{GS} is modulated by V_{DS}. For voltages around the threshold voltage (V_{Th}), the latter parameter changes slightly from forward to reverse conduction. Therefore, the switches are slow and cannot be turned ON and OFF completely. This subjects the structure to significant leakages, which leads to inefficient rectification.

Threshold voltage is a process-dependent parameter. Various circuit techniques are introduced to suppress the impact of V_{Th} when turning-on transistors using additional biasing circuitries in a standard CMOS process. They benefit from the use of bootstrap [13] or dynamic techniques for gate-drain [14] or bulk-source (body effect) biasing [15]. Here, a DC voltage is generated in an idle phase to eliminate or reduce the effect of V_{Th} in the working phase. Unfortunately, all cited techniques are power hungry. Alternatively, advanced CMOS processes offer low-threshold voltage (native) transistors [1] which could be employed to realize low-voltage designs.

Recently, a gate cross-coupled rectifier (GCCR) shown in Figure 3.3 was introduced [12]. In each signal cycle of this circuit, the V_{Th} of one diode-connected MOS transistor is replaced with the effective voltage drop across a MOS switch ($V_{GS} = V_{eff}$) as formulated in Eq. (3.1).

$$V_{eff} = \sqrt{\frac{2I_D}{\mu COX\left(\frac{W}{L}\right)}} \qquad (3.1)$$

where W and L are the width and length of the transistors, I_D is the current flowing and μC_{OX} is a process related product. This drop could be negligible when the MOS transistor is in its triode region. The other advantage of such rectifier is to drive the gate of the said MOS transistor with a

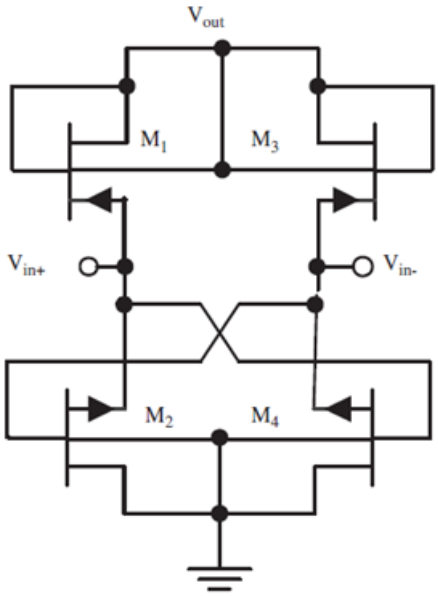


Figure 3.3. Gate cross-coupled rectifier [12].

voltage swing higher than that of the diode-connected structures, which reduces the switch leakages and improves the switch conductivity, as expressed in Eq. (3.2).

$$g_{ds} = \sqrt{\mu_P C_{OX} \left(\frac{W}{L}\right)_P (V_{SG} - |V_{Th}|)} \qquad (3.2)$$

The resulting rectifier produces higher power efficiency than conventional FWDR structures; however, it uses diode-connected MOS transistors for load connections and thus suffers from the associated drawbacks.

Fully cross-coupled structures have also been introduced where both upper and lower main branch transistors are cross-coupled [16]. It was shown that such a structure does not present good power efficiency due to existing parasitics [17].

Previously reported structures – except the fully cross-coupled configuration – exploit at least one diode or diode-connected MOS transistor to regulate the direction of the current flow toward the load.

Active rectifier configurations have been reported to have higher power efficiency [18–22] and to generate less heat [23]. They use active circuitries (comparators) to provide adequate control signals for each MOS transistor, replacing the diode-connected transistors in each signal cycle. In this way, the conduction angles of the MOS switches with respect to the sinusoidal source are managed based on the source characteristics and load requirements. They offer faster switching between ON and OFF states and allow reducing the leakages. In comparison with the passive rectifier structures, they benefit from higher gate-drive voltages improving the switch conductivity and the power efficiency accordingly. However, most approaches based on active devices require additional static power to operate. Recall that there is no power available especially at the starting point of the rectifier. This outweighs the benefits they offer, and it limits their application to the circuits leveraging some alternate solution such as: an auxiliary power source, a second parallel lower efficiency rectifier for bootstrap, or a large capacitor to power up active devices and peripherals. The last two solutions can be combined, such that the reservoir can be charged by an extra signal path active at least temporarily at startup [24].

Several active rectifiers rely on high-speed high-resolution low-offset comparators that actively control switches in the main power conversion path. Their design can be very challenging, and their characteristics can have a strong influence on the performance of an active rectifier. This is particularly true when the sinusoidal power source to be rectified is recovered through a RF signal whose frequency can exceed 10 MHz. Indeed, when the AC source frequency is high the comparator delay and response time could lead to flow of current from the output reservoir back to the source coil. Such a reverse current can cause coil voltage distortions, increased power dissipation in the switches and decrease of V_{Out} due to loss of charge from the capacitor reservoir. Other drawbacks associated with active rectifiers are the higher component count and the design complexity. In general, more complex designs comprising more components have higher power consumption and larger area.

The need for configurations with higher efficiencies and greater output voltages attracted many researchers trying to improve the overall characteristics of the power conversion chain in wirelessly powered devices. The remainder of this paper includes in Section 2 the presentation of the new full-wave active rectifier along with its circuit description. It uses MOS transistors as low-loss switches to achieve a significant increase in overall power efficiency and reduced voltage drop. The design does neither require an internal power source nor an auxiliary signal path for power delivery at startup. Section 3 reports simulation and measurement results for the new structure as well as a comparison between different structures followed by concluding remarks in Section 4.

3.3 New Proposed Active Rectifier

To improve the power conversion efficiency (PCE) and increase the output voltage, we propose a new full-wave active rectifier (FWAR). It employs MOS switches with very low forward drop to replace all diodes or diode-connected MOS in previous structures. Figure 3.4 provides the schematic of the proposed structure.

The design benefits from driving the gate voltages with the highest available voltage in the circuit and it does not introduce a V_{Th} drop in the direct current loop from source to load. To help understand how the circuit in Figure 3.4 operates, its half part active during the positive input cycle for simplicity is redrawn in Figure 3.5.

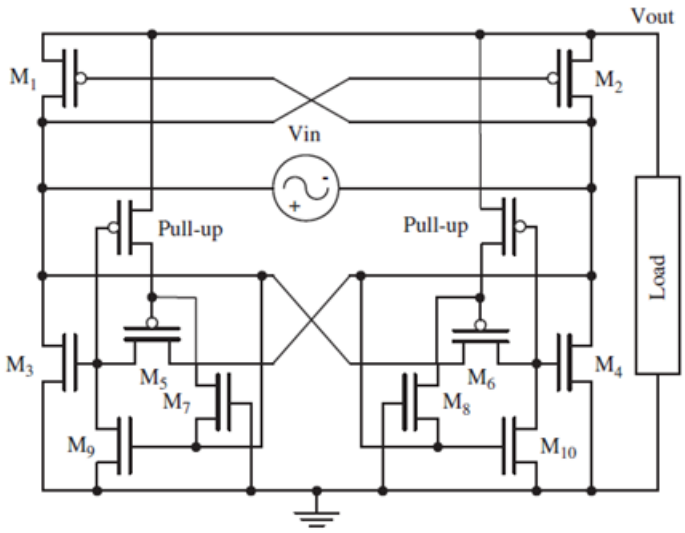


Figure 3.4. Schematic of the proposed full-wave rectifier.

Here, M_1 and M_4 replace a pair of diodes in a conventional bridge rectifier. Ignoring for simplicity the impact of MOS threshold voltages, M_1 operates during positive cycles ($V_{In+} > V_{In-}$) while the combination of M_4, M_6 and M_8 checks for valid load charging condition ($V_{In} > V_{Out}$). M_{10} provides the condition for complete cut-off of M_4 in its stop mode of operation.

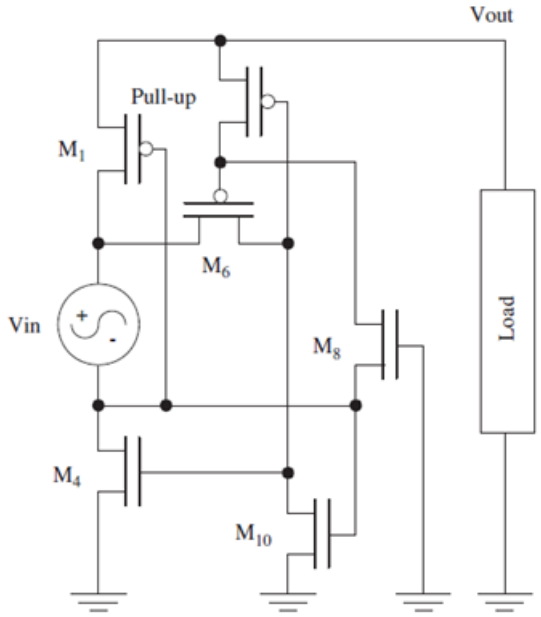


Figure 3.5. Schematic of the active parts during the positive half cycle.

During positive cycles, M_1 conducts and connects the output terminal to the floating input source. Therefore, neglecting possible resistive drops (as would be correct if there is no current flowing) the lower terminal of the signal source is set at a voltage equal to (V_{Out} - V_{In}) with respect to the ground. If the second crucial condition for rectification becomes true ($V_{In} > V_{Out}$), the lower terminal of the signal source has a voltage lower than the ground. Therefore, M_8 conducts and that applies a low voltage to the gate of M_6. This forces M_6 to conduct, which puts M_4 in conduction too. The combinations of gate and source voltages that are selected are such that the switches have high conductance and low leakages.

Simultaneous conduction of M_1 and M_4 closes the current path from the source to the load and charges the output capacitor reservoir. Otherwise, M_{10} forces M_4 in deep cut-off region preventing floating gates and reducing leakage and short circuit currents to flow. Note that the circuit functionality and performance are influenced by the need to respect proper timing between various switching conditions.

Pull-up pMOS transistors are also used to attach the gate of M_5/M_6 to V_{Out}, while M_7/M_8 are idle. The gates of such transistors are driven by the same voltage as the gates of M_3/M_4. These extra transistors help preventing floating gates. In negative cycles, the dual circuit will rectify the input voltage in the same manner. Considering the dead zone due to the threshold voltage of the main switches ($M_{1\text{-}4}$), the design operates in a way that is somewhat analogous to a class AB amplifier [25].

The proposed rectifier was implemented at the circuit level using the standard TSMC 0.18 µm CMOS process with 3.3 V nominal voltage and then characterized with the SpectreS simulator under the Cadence environment. An AC sinusoidal floating voltage source was used to model RF power being fed into the rectifier stage. The source peak-to-peak amplitude is 5V and its frequency is set to 10 MHz, which fits the requirements for an intracortical stimulator implant application developed in our laboratory.

It is of interest that some gate oxides and junctions may be subject to voltage stress that could decrease reliability. This issue was left for future research.

The main branch transistors ($M_{1\text{-}4}$) sizes are 20/0.35 µm with multiply factor of 50. M_5/M_6 sizes are 0.525/ 0.35 µm while M_7/M_8 and M_9/M_{10} are implemented with native transistors

(typical V_{Th} = -120 m V) a re, r espectively, 1. 2–1.35/1.52 µ m w ith multiply f actor of 100. Minimum size pull-up pMOS transistors are also employed. Figure 3.6 illustrates the behavior of the proposed FWAR showing $|V_{In}|$, V_{In+}, V_{In-} and V_{Out} over a full period. Considering the main switches (M_{1-4}) acting in deep triode region, the output resistance contributed by the rectifier in each s ource c ycle i s a co mbination o f R_{ON} for nMOS (M_3 or M_4) a nd pMOS (M_1 or M_2) transistors. A s t he si zes o f n - and p -type M OS tr ansistors lo cated in main p aths (M_{1-4}) ar e identical and due to higher mobility for majority carriers in nMOS (electrons) compared to holes in pMOS, for a given load and source conditions, one may expect the R_{ON} of the pMOS (M_{1-2}) to dominate.

From Figure 3.6, we observe that the waveforms V_{In+} and V_{In-} with respect to V_{Gnd} look more like skewed and distorted sinusoids. The switching dynamics is described as follows. At the start of t he pos itive c ycle, when $t = T_0(S_0)$ and $V_{In} = 0$, as M_1 behaves as a r eversed-bias di ode-connected and therefore is OFF. M_6 is OFF due to its gate connected to V_{Out} via pull-up. M_8 and M_{10} are a lso O FF due t o t heir c onnections t o t he f loating s ignal s ource a nd t he g round w hich results in M_4 staying OFF.

At $t = T_1(S_1)$, when $V_{In} = |V_{TP}|$, M_1 is gradually turned on, s horting V_{In+} to V_{Out}. Thus, t he change i n V_{In} is r eflected b y t he dr op i n V_{In-}. T his imp lies V_{In-} to be m ore pos itive t han t he ground w hich l eads M_6 and M_8 to stay OFF a nd M_{10} to t urn ON, respectively. As a result, t he condition for complete cut-off of M_4 is provided and no c urrent flows in M_1. The conduction of M_{10} also helps pull-up to hold M_6 in stop mode.

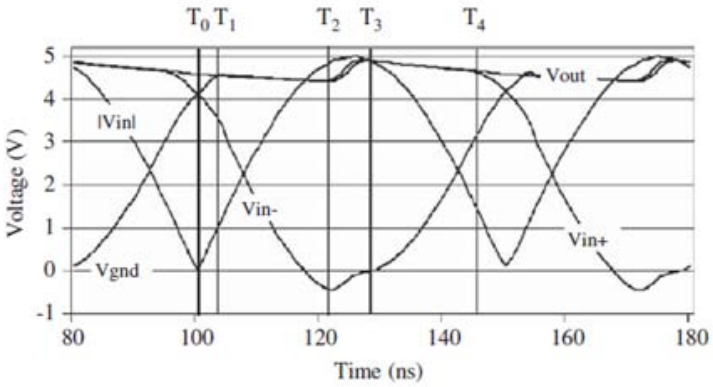


Figure 3.6. Simulated result of the FWAR over one period.

At $t = T_2(S_2)$, when V_{In} is higher than (V_{Out}+$V_{DS\text{-}M6}$) such that $V_{In\text{-}}$ drops below V_{Gnd}, and therefore, M_8 gets ON which puts M_6 in conduction, too. As such, M_{10} turns OFF as well which leads the gate of M_4 no longer to be fixed to the ground. Therefore, M_4 starts conduction with a very low forward drop and V_{Out} is charged up via the path consisted of M_4 along with M_1. The difference between V_{In+} and V_{Out} represents the conduction drop due to the finite resistance of the charging path elements. Obviously, the overall power efficiency of the FWAR is affected by the effective voltage drop of the pass switches.

After V_{In} reaches the peak, it starts to decrease and at $t = T_3(S_3)$, $V_{In\text{-}}$ rises above V_{Gnd}. This results in turning off M_6 and M_8 and putting on M_{10}, respectively. Finally, as V_{In} drops to $|V_{TP}|$, $t = T_4(S_4)$, the gate-drive of M_1 is no longer sufficient to short V_{In+} to V_{Out}, and V_{In+} starts to drop.

Table 3.1 tabulates all the switching states of the various transistors for the proposed active rectifier in a positive cycle of the signal. The source terminals of the transistors connected to the floating signal source terminals are varying over time significantly. They go above V_{Out} and below the ground voltages and therefore, subject the exposed transistors to possible latch-up and/or substrate leakage currents. Therefore, proper bulk biasing is essential. This is accomplished using the dynamic bulk switching technique [26]. This technique is applied for biasing the bulk of $M_{1\text{-}4}$ as shown in Figure 3.7. Using the said technique, the bulk of the main pMOS transistor (M_1) is selectively connected to the highest available voltage (either V_{Out} or V_{In+}). A symmetrical reverse configuration is applied for bulk biasing of other main nMOS transistors (such as M_4) which are selectively connected to the lowest available voltage (V_{Gnd} or

Table 3.1. Rectifier switching states for positive cycle.

	M_1	M_4	M_6	M_8	M_{10}
S_0	OFF	OFF	OFF	OFF	OFF
S_1	ON	OFF	OFF	OFF	ON
S_2	ON	ON	ON	ON	OFF
S_3	ON	OFF	OFF	OFF	ON
S_4	OFF	OFF	OFF	OFF	ON

S ≡ State, M ≡ MOS Transistor

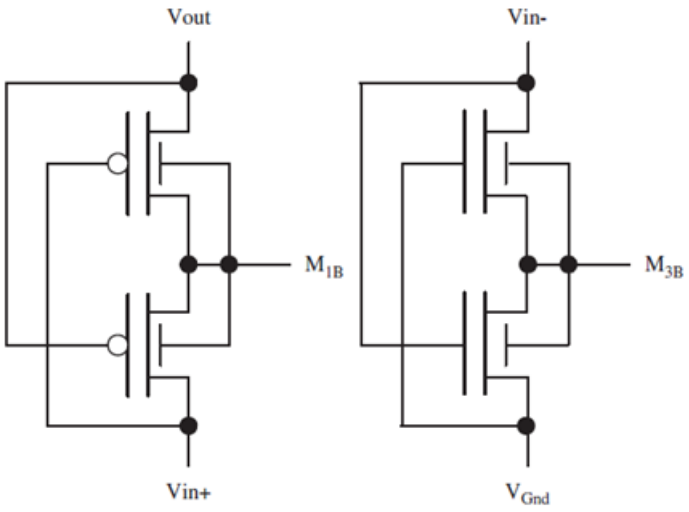


Figure 3.7. Schematic of dynamic bulk biasing for main switches: (a) M_1 and (b) M_3.

V_{In-}). Note that implementing such bulk biasing technique requires locally isolated wells or substrate. In the proposed configuration, this is realized by using separate n-well for pMOS devices and deep n-well around nMOS transistors.

It is worthy to notice that due to the nature of the design, using inherent characteristics of MOS switches for having a voltage at least equal to V_{Th} to form the channel and conduct, the use of low-threshold transistors can contribute to improving power efficiency. However, the maximum output voltage of the rectifier remains almost the same as the peak-to-peak input amplitude irrespective of the transistor's threshold.

The following discussion relates to a design optimized for a shunt *RC* load of $C = 200$ pF and $R_L = 2\text{k}\Omega$. This load condition when combined with applying a sinusoidal source amplitude of 5 V leads to a load current of up to 2.5 mA. The size of the main pass transistors (M_1/M_4 and M_2/M_3) was traded-off with associated parasitics to handle large load currents with low enough channel resistances. As other switching-based circuits, the performance of the design and its function strongly depends on timing and operating frequency. Providing proper timing and optimizing the performance can be accomplished in part by choosing transistors of the eight times larger than minimum. This is necessary for quick pulling down of the gate of M_3/M_4 and forcing them to cut-off region while in stop mode. M_5/M_6 are minimum size transistors. The

choice of these sizes along with those of M_9/M_{10} provides proper timing for M_3/M_4 to switch. M_7/M_8 are also designed with transistors seven times larger than minimum to handle gate parasitic capacitance discharging associated with the gate of M_5/M_6 and their quick switching. Minimum size pull-up pMOS transistors are also used.

Although the resistance of a diode may be decreased by increasing its area, the junction capacitance will become dominant and deteriorate the PCE. Increasing the size of the main pass transistors increases the g_m of the transistor, which leads to quicker reaction in response to small changes in input signal. It also reduces the R_{ON} of the channel in MOS pass device, which leads to lower voltage drop across the channel. However, switches with larger area also introduce higher parasitic capacitances which degrade their performance in high frequency applications.

3.4 Performance Metrics and Simulation Results

Power conversion efficiency is an index of the power dissipated by the load compared to total energy consumed by whole circuit. It is commonly used to compare different rectifier structures and is defined as the ratio of the output DC power to the input RF power.

$$\text{PCE}=\frac{P_{Out}}{P_{In}}\times 100 \qquad (3.3)$$

There are other important parameters such as the output DC (average) voltage and the minimum input voltages which may be characterized. Parameter PCE includes all drops across the series components located in the power chain. The minimum input voltage is the minimum voltage that could be detected by the rectifier. These maximum and minimum voltages determine the dynamic range of the rectifier. The simulation result in Figure 3.6 shows that the rectifier gives an output maximum voltage of 4.86 V for R_L = 2kΩ and C_L = 200 pf, and the conduction time is approximately 7 ns per phase. This is the time interval when the rectifier charges the load reservoir.

We have compared the simulation results of FWDR and GCCR structures with our new proposed FWAR circuit. Figure 3.8 shows the output voltage variations over time for these different structures for the same transistor sizes and load as already stated. The FWAR produces significantly higher output voltages in comparison with other structures. This is due to the use of

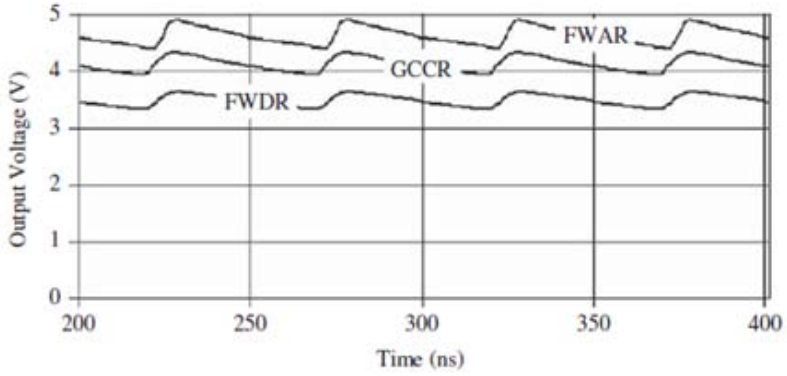


Figure 3.8. Simulated output voltage of FWDR, GCCR and FWAR.

MOS transistors as switches in their triode region, where they can present very low voltage drops across their drain-source terminals. Use of high V_{GS} for such transistors has also resulted in higher g_m and lower channel on-resistance accordingly.

The voltage conversion ratio (VCR) is defined as the ratio of the average output voltage to the peak magnitude of the AC input voltage Eq. (3.4). It indicates the portion of input voltage which is available at the output. Figure 3.9 illustrates the VCRs for the different structures.

$$M = \frac{V_{Out-av}}{|V_{In}|} \tag{3.4}$$

The new proposed structure has the highest voltage conversion efficiency among the considered structures. The average output voltage with a source amplitude 3.3 V is 54% and 16% greater than those produced by the FWDR and the GCCR topologies, respectively. This is due to

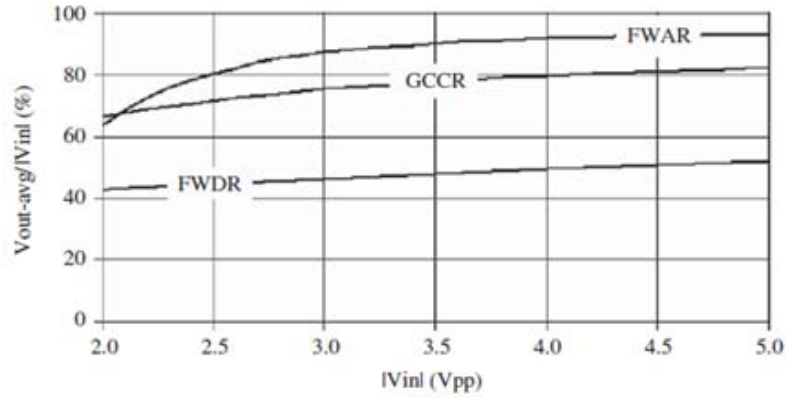


Figure 3.9. Simulated VCRs for various rectifier structures.

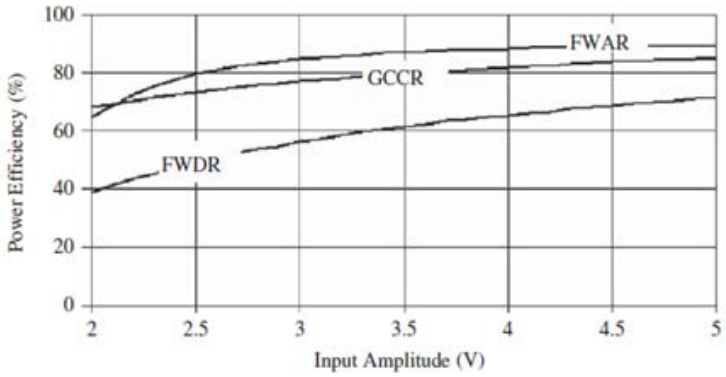


Figure 3.10. Simulated power efficiency versus input amplitude.

the smaller voltage drop across the pass devices observed at each cycle.

Figure 3.10 shows the simulation results characterizing the power efficiency versus input amplitude for FWDR, GCCR and FWAR structures. The FWAR presents significantly higher power efficiency when compared to other structures.

With a 3.3V AC source amplitude, the new rectifier offers improved power efficiency by up to 46% and 10% compared to the FWDR and GCCR topologies, respectively. This is due to use of MOS transistors in their triode region as switches, where they can have very low voltage drop across their drain-source terminals. Simulations confirm that the new structure is capable of handling high load currents with small power efficiency degradation.

3.5 Measurement Results

The proposed full-wave active rectifier was fabricated in a 0.18 µm 6-Metal/2-Poly TSMC 3.3V standard CMOS process. The die photomicrograph provided in Figure 3.11. This chip measures an area of 1594×1080 μm^2 and it is mounted in 40 pin dual-in-line package. The chip consists of two versions of the proposed design. In one version, the native transistors are laid out such that their bulk is connected to the general substrate.

In a second version, some DRC violations were done on purpose, to allow implementing a local substrate for the native transistors, which is normally not permitted by existing design rules. The local substrate is then implemented using the deep n-well layer. Having local substrate makes it possible to apply dynamic bulk biasing technique to the native transistor, which may

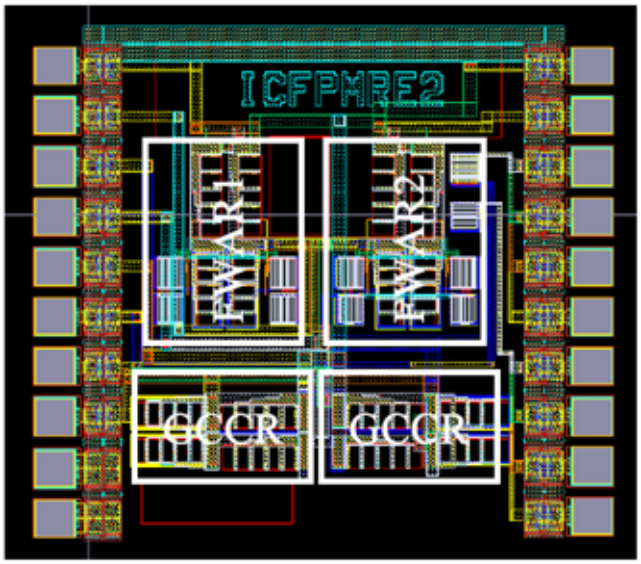


Figure 3.11. Photomicrograph of the prototype chip.

result in reducing body effect, leakages through bulk and latch-up. A conventional diode-connected rectifier as well as a gate cross-coupled topology is also fabricated for comparison in our experiments.

All the main switches are surrounded by guard rings to isolate them from adjacent cells. All transistors have short channel lengths (0.35 μm for normal devices and 1.52 μm for native devices) to maximize the speed of operation. The chip was carefully laid out to have a symmetrical structure minimizing potential imbalance in parasitic capacitances between input rails (V_{In+} and V_{In-}).

To measure the performance of the fabricated rectifiers, the measurement setup shown in Figure 3.12 was used. The rectifiers implemented in this design require a truly floating input signal to act as a full-wave rectifier. Given the fact that signal generators normally produce outputs with reference to their outlet ground, an isolating transformer (1:1) was used to decouple the source output from the common ground of the outlet. Experiments confirmed that this is a necessity.

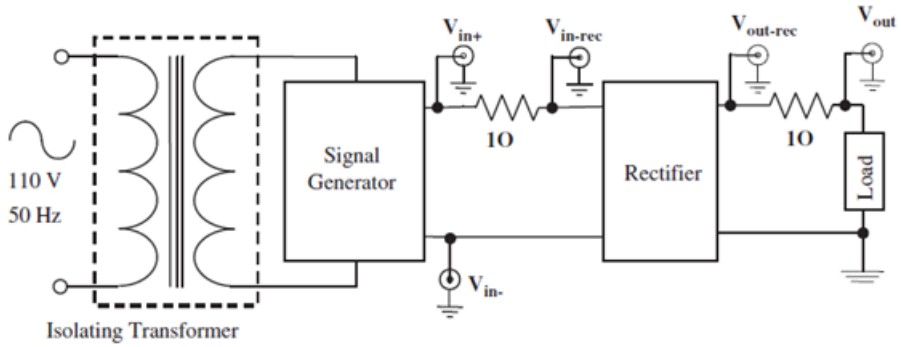
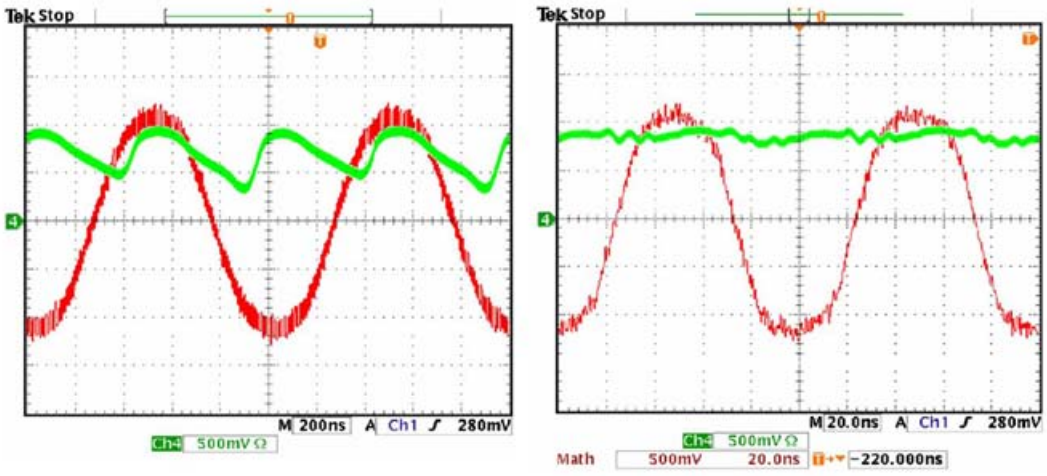


Figure 3.12. Voltage and power measurement setup.

Due to significant loading impact of using a regular AC ammeter placed in series with the source and the load of the rectifier, the current, flowing into the rectifier and out of it, was differentially measured across 1 Ω resistors connected in series with input and output terminals.

A signal generator (Agilent 32350A) was used to drive the primary coil of the isolating transformer with a sinusoidal signal. This transformer is responsible to transfer energy to the rectifier inputs. The output load consists of a 200 pF capacitor combined with a 2 kΩ resistor in parallel.

Figure 3.13 shows the measured transient waveforms of input and output when the FWAR is operated at 1 and 10 MHz, respectively. Here, the input peak-to-peak voltage is adjusted at 2.5 V,



(a) (b)

Figure 3.13. Input/output waveforms of FWAR operating at: (a) *f*=1 MHz, (b) *f*=10 MHz.

which resulted in output average voltages of 0.82 and 0.96 V and power efficiency of 87.6% and 92.5% at 1 and 10 MHz, respectively. It can be seen, from V_{Out} that C_L exponentially recharges during the normal rectifier operation and discharges in R_L at other times. Under the same test conditions, other existing rectifiers produce output voltages and power efficiencies significantly lower than the FWAR. Measurement shows that at source frequency of 10 MHz, the output voltage for the FWDR is 0.55 V while 0.81 V is measured at the output of the GCCR topology. Therefore, the other circuits become much less efficient at lower source amplitudes.

However, the proposed design is still effective in reducing the dropout voltage, even when the AC input is lower than the value for driving one or two (depending on FWDR or GCCR structures) diode-connected MOS transistors. The case for lower output voltage and power efficiency would get even worse if one considered using conventional full-wave diode bridge rectifiers constrained by two cascaded diodes drop (V_γ = 0.7 V) in each source signal phase. The performance of the proposed rectifier is found to be close to the simulated results, particularly at the high end of the AC input source range considered (5 V peak-to-peak).

To summarize, the proposed active rectifier is feasible and was successfully implemented. It offers remarkably higher output voltages and power efficiency compared to other proposed rectifier configurations when used in low voltage and high current applications.

Figure 3.14 shows the measured PCE of FWAR for different source voltages operating at f = 10 MHz. We obtained a peak PCE = 79% with a 2.2V input peak-to-peak sinusoidal input voltage. Table 3.2 summarizes the measured power and voltage conversion efficiency values for

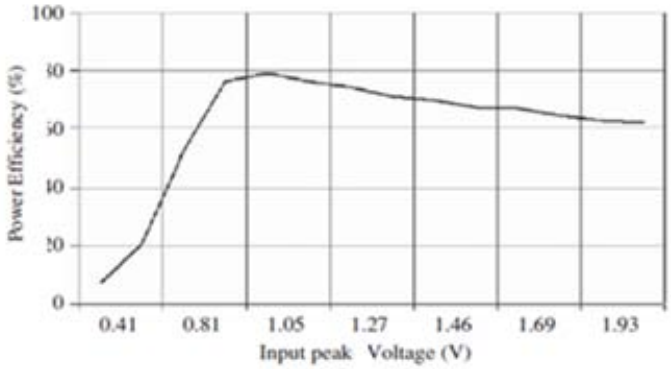


Figure 3.14. Measured power conversion efficiency of FWAR operating at 10 MHz.

Table 3.2. Summary of measured power efficiency for cited rectifiers.

Parameters	Topology		
	FWDR (%)	GCCR (%)	FWAR (%)
Power efficiency	31	38	76
Voltage conversion efficiency	28	73	92.5

FWDR and GCCR compared with the proposed topology at $f = 1$ MHz and $V_{pp} = 2.5$ V. It is obvious that FWAR has a significantly higher power and voltage conversion efficiencies among the compared rectifier structures.

3.6 Conclusion

A full-wave active rectifier was presented. It is suitable for many applications including smart biomedical implants and RFID tags. The structure does not require in efficient rectification techniques or complex circuit design. The new design employs MOS-based switches that can offer very low voltage drop to achieve AC to DC conversion. The rectifier also uses dynamic body biasing and native transistors. It is advantageous compared to conventional diodes, fully or partially diode-connected MOS-based structures. The highest available voltage differences in the structure are used to control its embedded switches, which results in lower channel resistance and less leakage currents. This design has been implemented in a 0.18 µm 3.3 V TSMC CMOS process and successfully tested. Measurements confirm significantly higher power and voltage efficiencies compared with other rectifier topologies, particularly when the source voltage is low.

3.7 References

[1] M. Sawan, Y. Hu, J. Coulombe, Wireless smart implants dedicated to multichannel monitoring and microstimulation, IEEE Circuits Syst. Mag. 5 (1) (2005) 21–39.

[2] J. Coulombe, M. Sawan, J.-F. Gervais, A highly flexible system for Microstimulation of the visual cortex: design and implementation, IEEE Trans. Biomed. Circuits Syst. 1 (4) (2007) 270–277.

[3] M. Ghovanloo, K. Najafi, A wireless implantable multichannel microstimulating system-on-a-chip with modular architecture, IEEE Trans. Neural syst. Rehabil. Eng. 15 (3) (2007) 449–457.

[4] C. Sauer, M. Stanacevic, G. Cauwenberghs, N. Thakor, Power harvesting and telemetry in cmos for implanted devices, IEEE Trans. Circuits Syst. I 52 (12) (2005) 1605–2613.

[5] K. Finkenzeller, RFID-Handbook, Second ed., Wiley, Hoboken, NJ, ISBN 0470844027, 2003.

[6] B. Jiang, J.R. Smith, M. Philipose, S. Rou, K. Sundara-Rajan, A.V. Mamishev, Energy scavenging for inductively passive RFID systems, IEEE Trans. Instrum. Meas. 56 (1) (2007) 118–125.

[7] S. Roundy, P.K. Wright, J. Rabaey, A Study of Low Level Vibration as a Power Source for Wireless Sensor Nodes, Computer Communications, vol. 26, Elsevier Science, 2003, pp. 1131–1144.

[8] R. Paradiso, G. Loriga, N. Taccini, A wearable health care system based on knitted integrated sensors, IEEE Trans. Inf. Technol. Biomedicine 9 (3) (2005) 337–344.

[9] M. Ferrari, V. Ferrari, D. Marioli, A. Taroni, Modeling, fabrication and performance measurements of a pirezoelectric energy converter for power harvesting in autonomous microsystems, IEEE Trans. Instrum. Meas. 55 (6) (2006) 2096–2101.

[10] S. Hashemi, M. Sawan, Y. Savaria, A power planning model for implantable stimulators, IEEE Int. Symp. Circuits Syst. ISCAS (2006).

[11] U. Karthaus, M. Gischer, Fully integrated passive UHF RFID transponder IC With 16.7-mW minimum RF input power, IEEE J. Solid-State Circuits 38 (10) (2003) 1602–1608.

[12] M. Ghovanloo, Kh. Najafi, Fully integrated wideband high-current rectifiers for inductively powered devices, IEEE J. Solid-State Circuits 39 (11) (2004) 1976–1984.

[13] T.T. Le, A. Von Jouanne, K. Mayaram, T.S. Fiez, Piezoelectric micro-power generation interface circuits, IEEE J. Solid-State Circuits 41 (6) (2006) 1411–1420.

[14] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, S. Otaka, A 950MHz rectifier circuit for sensor networks with 10 m-distance, IEEE J. Solid-State Circuits 41 (1) (2006) 35–41.

[15] T. Lehmann, M. Cassia, 1-V power supply CMOS cascode amplifier, IEEE J. Solid-State Circuits 36 (7) (2001).

[16] A. Facen, A. Boni, Power Supply Generation in CMOS Passive UHF RFID Tags, Research in Microelectronics and Electronics 2006, Ph.D. dissertation, pp. 33–36, June 2006.

[17] Zh. Zhu, B. Jamali, P.H. Cole, "Brief comparison of different rectifier structures for RFID transponders," /http://www.mlab.ch/autoid/SwissReWorkshop/papers/BriefComparisonOfRectifierStructuresForRFIDtransponders.pdf.

[18] T. Lehmann, Y. Moghe, ''On-Chip Active Power Rectifiers for Biomedical Applications,'' Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Vol. 1, pp. 732–735, Japan, May 2005.

[19] Y-H. Lam, W-H. Ki, C-Y. Tsui, Integrated low-loss CMOS active rectifier for wirelessly powered devices, IEEE Trans. Circuits Syst. II 53 (12) (2006) 1378–1382.

[20] C. Peters, O. Kessling, F. Henrici, M. Ortmanns, Y. Manoli, CMOS integrated highly efficient full wave rectifier, IEEE Int. Symp. Circuits Syst. (2007) 2415–2418.

[21] C.L. Chen, K.H. Chen, S.I. Liu, Efficiency enhanced CMOS rectifier for wireless telemetry, Electron. Lett. 43 (18) (2007).

[22] S. Atluri, M. Ghovanloo, Incorporating back telemetry in a full-wave CMOS rectifier for RFID and biomedical applications, Proc. IEEE Int. Symp. Circuits Syst. (2007) 801–804.

[23] G. Lazzi, Thermal effects of bioimplants, IEEE Eng. Med. Biol. Mag. 24 (5) (2005) 75–81.

[24] Bawa G, Ghovanloo M., A High Efficiency Full-Wave Rectifier in Standard CMOS technology, Proc. 50th MWSCAS conference, pp. 81–84, Montreal, Canada, Aug. 2007.

[25] A. Sedra, M. Smith, Microelectronic Circuits, Oxford University Press, 2004.

[26] P. Favrat, Ph. Deval, M.J. Declercq, A high-efficiency CMOS voltage doubler, IEEE J. Solid-State Circuits 33 (3) (1998) 410–416.

Chapter 4: A DOUBLE-RESERVOIR BOOTSTRAP RECTIFIER

In the previous chapter, we proposed an active full-wave high-efficiency rectifier with a partially gate cross-coupled structure. It uses inherent characteristics of the MOS switches to replace explicit comparators. The cited active rectifier offers significantly higher power and voltage conversion ratios compared to conventional bridge and partially gate cross-coupled passive structures. It does not require any supply voltage for its normal operation. The proposed rectifier however is constrained in operating frequency and by the reverse leakage current through the channels of the main pass transistors.

Passive rectifiers are an alternative to active rectifiers when operating at high frequencies and when complexity is a concern. They use passive elements and circuit techniques to implement rectification. They consume no quiescent current and have simpler circuitry. Similar to the previously presented active rectifier, they do not require any extra supply voltage for their internal circuit biasing specially. However, they are constrained with threshold voltage of diode-connected MOS switches and power consumptions due to leakages in controlling circuitry and reverse current in main pass switched.

In this chapter, we present a new passive rectifier based on a partially gate cross-coupled structure where the effective threshold voltage of the rectifier is effectively reduced when it turns on. The bootstrapped capacitor technique which is well suited with standard CMOS processes is used with this structure. The proposed rectifier uses dual circuitry, including two diode-connected MOS transistors forming dual auxiliary and charging paths, along with two bootstrapped capacitors. It achieves a significant increase in its overall power efficiency and low voltage-drop. Therefore, the rectifier is good for applications with low-voltage power supplies and large load currents. The rectifier topology does not require complex circuit design. The highest voltages available in the circuit are used to drive the gates of selected transistors in order to reduce leakage current and to lower their channel on-resistance, while having high transconductance. The rectifier also uses dynamic body biasing in auxiliary paths. The rectifier was implemented using the TSMC 0.18 μm CMOS standard process. The schematics- and post-layout-simulation results of the proposed bootstrap rectifier show consistent results. Measurements are also provided and they show good agreement with simulations. This work will appear in IEEE transactions on

biomedical circuits and systems and is reproduced as follows.

A High-Efficiency Low-Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices

Saeid Hashemi, Mohamad Sawan, *Fellow, IEEE*, and Yvon Savaria, *Fellow, IEEE*

Abstract *– We present, in this paper, a new full-wave CMOS rectifier dedicated for wirelessly-powered low-voltage biomedical implants. It uses bootstrapped capacitors to reduce the effective threshold voltage of selected MOS switches. It achieves a significant increase in its overall power efficiency and low voltage-drop. Therefore, the rectifier is good for applications with low-voltage power supplies and large load current. The rectifier topology does not require complex circuit design. The highest voltages available in the circuit are used to drive the gates of selected transistors in order to reduce leakage current and to lower their channel on-resistance, while having high transconductance. The proposed rectifier was fabricated using the standard TSMC 0.18 µm CMOS process. When connected to a sinusoidal source of 3.3 V peak amplitude, it allows improving the overall power efficiency by 11% compared to the best recently published results given by a gate cross-coupled-based structure. In addition, the proposed rectifier presents an average output voltage up to 210% higher than the best previously reported circuits when the peak amplitude of the sine source drops down to 0.8 V AC.*

Index Terms—Bootstrapping technique, Low-voltage devices, Power efficiency, Rectifiers, Bioelectronics, Implantable devices.

4.1 Introduction

Progresses in microelectronics have resulted in miniaturized smart medical devices [1]-[2], advances of radio frequency identification (RFID) tags [3]-[4], as well as several types of sensors and body sensor networks [5]-[7]. These devices require energy sources for carrying out their intended functions.

Medical implantable devices dedicated to either sensing and treatment purposes are widely used to monitor and record targeted biological activities [1]-[2], [8]-[12], and/or stimulate certain sites of neural or muscle tissues [13]-[14]. In order to improve the efficiency of sensing and treatment by electrical stimulation, various forms of implantable devices are employed. These devices often use multi-channel sensing and stimulation through electrode arrays [13]. To support their operation, sufficient energy must be provided. As energy or power available to implanted devices is generally limited, efficient power conversion chains capable of handling sufficient power are strongly required.

Classical powering techniques, including embedded batteries [15] and transcutaneous power harvesting methods [1] are relatively constrained in terms of energy density, device lifetime, potential hazards to human safety, integration, and physical size. Moreover, despite remarkable efforts dedicated to developing power harvesting techniques to scavenge power either from the environment or from the human body, these techniques are not yet considered reliable and feasible, but research is steadily progressing [16]-[17]. Thus, procuring adequate energy to power electronic implants remains challenging.

Recently reported experimental systems commonly use inductively coupled links to wirelessly deliver needed energy over short distances. This technique suffers from extremely low power transfer efficiency due to poor electromagnetic coupling, skin absorption, and narrow band-pass.

Gate cross-coupled rectifiers have been proposed by [18]. In this topology, two diodes of the classical diode rectifier are replaced by two cross-coupled MOS transistors. They introduce a full-wave rectifier constrained with a single threshold voltage (V_{Th}) instead of two, which is the case for conventional bridge full-wave rectifiers.

Another rectifier topology proposed by [19] is the use of the boot strapped capacitor technique that allowed reducing the effective threshold voltage of a diode-connected transistor to the difference between two threshold voltages. In this paper, we propose a new rectifier configuration for medical implantable devices. It combines the gate cross-coupled configuration with the boot strapped technique to build a new rectifier architecture that has a voltage drop smaller than the other configurations and that is capable of handling large load currents.

The remainder of this paper includes, in Section II, the architecture and characteristics of passive- and active-rectifier topologies. Section III introduces a short review on different threshold cancellation techniques. Section IV presents a new topology for a full-wave rectifier along with its circuit description. Section V presents simulation and measurement results of the proposed device, as well as a comparison between different topologies followed by concluding remarks in Section VI.

4.2 Rectifier Topologies and Threshold Cancellation Techniques

Wideband power rectifiers are commonly used within the power conversion chains to convert an input AC signal to an unregulated DC supply using diodes.

4.2.1 CMOS Rectifier Implementation

In standard CMOS processes, the diodes are commonly replaced with diode-tied MOS transistors that are easier to implement. Here, the structure is still affected by the threshold voltage (V_{Th}) and instantaneous voltage drop across the transistor-based switches due to their channel resistances results in degrading the overall power efficiency and reducing the output voltage. On the other hand, Schottky diodes with a low forward drop are possible, but their implementation is expensive, due to the extra fabrication steps that they imply as they are not available in standard CMOS processes [20]. It is worthy to note that with technology evolution, the required power to operate multi-function devices tends to grow with the application needs and sophistication of their modes of operation. This makes the structure increasingly inefficient in advanced low-voltage sub-micron processes, where the ratio of the normal supply voltage to the threshold voltage of MOS transistors decreases.

Bridge full-wave rectifiers (FWBR) are popular version of full-wave rectifiers. They offer higher power efficiencies, smaller output ripples and greater reverse breakdown voltages compared with their counterpart, the half-wave rectifiers [18].

The full-wave gate cross-coupled rectifier (FWGR) shown in Figure 4.1a was introduced in [18]. The rectifier works such that, in each signal cycle of the circuit, the threshold voltage of one diode-connected MOS transistor is replaced with the effective voltage drop across a MOS switch. The other advantage of such rectifier is to drive the gate of the said MOS transistor with a voltage

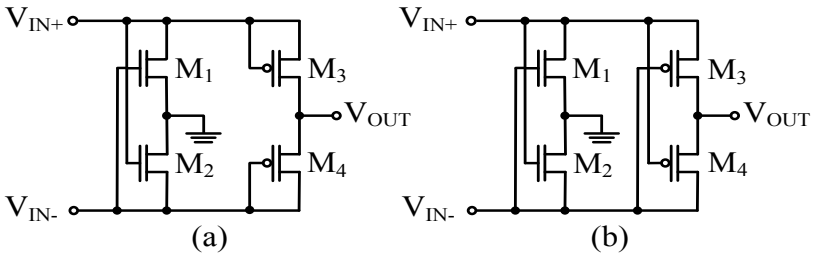


Figure 4.1. Schematics of full-wave rectifiers: a) gate cross-coupled, b) fully cross-coupled.

swing higher than those commonly used with diode-connected structures, which reduces the switches' leakage and improves their conductivity. The resulting rectifier produces higher power efficiency than conventional FWBR structures; however, in each source cycle, it uses a single diode-connected MOS transistor for load connections and thus suffers from the associated (threshold) voltage drop.

Full-wave fully gate cross-coupled rectifiers (FWFR) are also introduced, where the transistors in the two main branches are cross-coupled [21]. Here, unlike the previous rectifier, all the main pass MOS transistors are cross-coupled as illustrated in Figure 4.1b. This circuit solves the problem of threshold voltage drop by diode-tied MOS transistors. However, it was shown that such a structure does not present good power efficiency due to flow-back current from the storage capacitor to the antenna, and other parasitics [22].

Another approach for improving power efficiency of rectifiers relies on active circuit to control pass transistors in place of diodes or diode-connected transistors. Figure 4.2 depicts the typical conceptual structure of so-called active rectifiers. As the source is nominally a sine wave, one circuit of this kind is often needed for each phase (positive and negative).

At each source cycle, a comparator regulates the conduction angle of the relevant pass device based on simultaneous comparison between the information obtained from input and output. In this way, the conduction angles of the MOS switches with respect to the sinusoidal source are managed based on the source characteristics and load requirements. These designs are reported to have higher power efficiencies compared to passive topologies [23]-[26] and to generate less heat [27]. There are new active designs where a combination of the classical approach (as above) and the gate cross-coupled structure is employed [28]. Recently, a new version of this class of

rectifier was introduced, which is using the inherent characteristics of selected MOS transistors as comparators working in the triode region, where they present very low voltage drops [29].

In spite of the advantages that the active configuration brings, the internal structure of those circuits consumes some additional static power to operate. This can be very challenging as there is no regulated power available at the starting point of the rectifier. This often outweighs expected benefits of active rectifiers when compared to the passive structures, and it limits their application mostly to the circuits leveraging some alternate solution such as: an auxiliary power source, a large capacitor to power up active devices and peripherals [28] or a second parallel lower efficiency rectifier for bootstrap [30]. Another major drawback of many active rectifiers occurs at higher frequencies. The pass transistors are usually very large in order to reduce the voltage drop and handle enough load current, and thus have significant parasitics which must be driven by the active circuitry. This requires more current at higher frequencies and reduces the power efficiency accordingly.

4.2.2 Threshold Cancellation Techniques

Threshold voltage is a process-dependent parameter which depends on the choice of oxide and on oxide thickness. Some standard CMOS procesess offer low- and medium-threshold devices which could be employed to realize low-threshold designs. However, their availability is not generalized yet, and the implemented devices are subject to significant leakage due to higher channel doping leading to excessive power consumption and reliability problems. Thus, low-threshold devices are generally not good candidates to put in the main flow of current towards the load.

Various circuit techniques are available to alleviate the impact of V_{Th} when turning-on transistors using additional biasing circuitries in a standard CMOS process. They often benefit from using additional biasing circuitry in a standard CMOS process in the form of either a bootstrap capacitor [19] or some dynamic techniques for gate-drain [31] or bulk-source (body-effect) biasing [32]. With these techniques, a DC voltage is generated in an idle phase to eliminate or reduce the effect of V_{Th} in the working phase.

Another approach involves using a floating gate technique to regulate the threshold voltage of given MOS transistors [33]. This technique requires high voltage to program the threshold voltage during set up and erase phases which implies new implementation constraints. They are also restricted to low operating frequencies.

Among the above cited techniques, the boot strapping approach is the most adapted with standard CMOS integrated circuit design. This method is outlined in the upper part of Figure 4.3a. Here, the diode-connected transistor (DCT), M_5, forms an auxiliary path which provides the required current to charge up the bootstrapping capacitor at start up via another DCT (M_7). The charges stored on C_{B1} are then simultaneously applied to the gate of M_3, the main pass pMOS transistor.

When the input voltage (V_{IN}) is higher than the output voltage (V_{OUT}) by at least the diode forward-bias voltage drop (V_{Th5}), current flows through the diode-tied transistor M_5 and charges the output capacitor. As the output node is being charged, the voltage across the capacitor, V_{CAP}, is also charged through M_7. Recall that, for a given process, ignoring body-effect due to different bulk biasing and process variations, the threshold voltage of the same type transistors are nominally the same, that is, V_{Th5}=V_{Th7}. Therefore, the voltage held on the capacitor is twice as high as the pMOS threshold voltage below the input voltage. Considering these facts, it can be shown [19] that the output voltage reaches:

$$V_{OUT} = V_{IN} - (|V_{Th3}| - |V_{Th7}|) \qquad (4.1)$$

where V_{Th3} and V_{Th7} are the threshold voltages of the main pass pMOS switch and M_7, respectively.

From (4.1), the effective V_{Th} of the circuit is reduced compared to that of the conventional diode-connected pMOS structure. Therefore, with a typical MOS transistor threshold voltage, the use of this technique could result in increasing the output voltage range for a given input source voltage. This becomes increasingly significant with new deep sub-micron technologies where the nominal supply voltage of the integrated circuits is less than 1 V.

This technique was applied to a This technique was applied to a conventional half-wave rectifier built using a voltage-doubler based structure [19]; however, the structure failed to present improved characteristics as expected. The rectifier required very large holding capacitors to procure miliampere-range current. This is due to its nature, which relies on pumping charges from source towards the load. The structure was also slow compared to other structures, as it needs frequent charging and discharging of the involving capacitors. For rectifier using very large capacitors, even with large switches, it results in relatively long settling times. Moreover, the need for remarkably large charge holding capacitors, in the micro-Farad range, is against the objective of implementing the rectifier using standard integrated circuits. The design was also reported as being subject to significant leakage through bulk of transistors, which deteriorate the power efficiency.

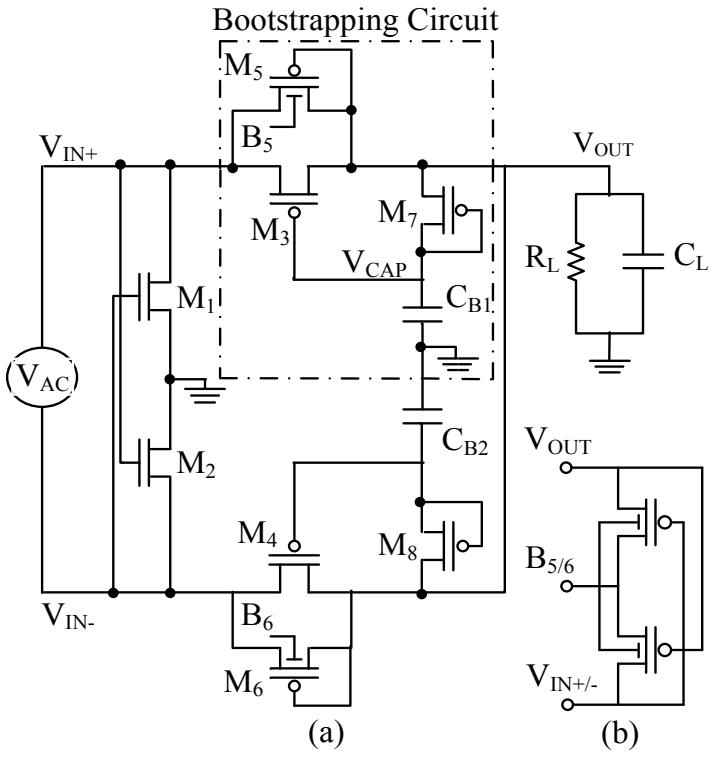


Figure 4.3. Schematics of: a) the proposed full-wave rectifier, b) its dynamic bulk biasing circuit for diode-tied transistors of $M_{5\text{-}6}$.

4.3 The Proposed Rectifier

In order to improve the power conversion efficiency (PCE) and increase the output voltage for a given input source amplitude, we propose a new full-wave rectifier (FWNR). It employs a pair of pMOS switches with very low effective threshold voltage to replace the diodes or diode-connected pMOS transistors found in previously reported structures.

The design also benefits from the advantages of gate cross-coupled structures applied on selected MOS transistors. This allows driving the gates of the nMOS transistors with a voltage swing larger than what would be found in conventional structures exploiting diode-connected nMOS transistors. Hence, a higher ON/OFF current ratio can be achieved. Figure 4.3a provides the schematics of the proposed full-wave rectifier.

The design uses the Dynamic Bulk Switching (DBS) technique to bias the bulk of selected transistors, in order to reduce the leakage current through bulk. Small bootstrapping capacitors were used to reduce the effective threshold voltage of the main pass transistors and to ensure the rectifier holds its functionality along with significant power and voltage efficiencies over a wide range of source voltages. $C_{B1\text{-}2}$ can be built using a standard CMOS process.

The modified rectifier operates very much like the gate cross-coupled rectifier [18]. In the input positive cycle, M_3 provides the main conduction path from the source to the load and charges the output reservoir, C_{B1}. The gate cross-coupled nMOS transistor (M_2) provides a low impedance return path for the current charging C_L.

Although the circuit branch (auxiliary path) that includes the diode-connected M_5 is mainly inserted to provide a path between the input and the output nodes to charge the holding capacitor (C_{B1}), simultaneous conduction of M_3 and M_5 contributes to the output current. Such diode-connected MOS transistor (M_5) does not significantly compromise the overall power efficiency, due to its remarkably small size (large channel resistance) compared to the main path transistor (M_3), which has a much larger size (to produce the desired small channel resistance).

Thus, the bulk of the load current flows through M_3, the transistor for which the effective threshold voltage is significantly reduced by the bootstrapping capacitor connected to its gate. In fact, as only a small part of the load current passes through M_5 in steady state regime, its

contribution to power losses of the rectifier remains small. The combination of M_5, M_7, and C_{B1} provides the biasing that reduces the effective threshold voltage of M_3. In negative cycles, the dual circuit (consisting of M_2, M_4, M_6, M_8, and C_{B2}) will rectify the input voltage in the same manner.

The design should be optimized by adjusting the sizes of the transistors to operate at different source frequencies. This is necessary to attain adequate time constants for the charging paths of the bootstrapping capacitors. Various simulations demonstrate that the new rectifier topology can operate over a wide range of operating frequencies up to 60 MHz provided adequate optimizations are performed.

The new design is simple and does not require complex circuit design techniques. Another advantage of the new design is its compatibility with standard CMOS processes, which allows implementing sufficiently large embedded capacitors. Obviously, a rectifier designed with a fixed size constraint must trade off the size of the main switch and the area dedicated to the bootstrapping capacitors.

The source of the pMOS transistors that are connected to the floating signal source terminals ($M_{5\text{-}6}$) see their voltage vary greatly over time. They go above V_{OUT} and below the ground voltage and, therefore, the exposed transistors could inject (leakage) currents in the substrate and induce latch-up. Therefore, DBS, as illustrated in Figure 4.3b, is essential [34]. Using this technique, the bulk of the auxiliary path transistors, $M_{5\text{-}6}$, are selectively connected to the highest available voltage (either V_{OUT} or input source). Note that implementing such bulk biasing requires locally isolated wells or substrate. In the proposed configuration, this is realized by using separate n-well for the pMOS devices used for biasing.

Another advantage of this DBS configuration is eliminating the body effect on the rectifying pMOS transistors, where this technique is applied, thus reducing the rectifier dropout voltage and power dissipation at start up. Since no sustained current passes through DBS transistors when they turn on, their drain-source voltage is close to zero [35]. The dynamic bulk biasing circuits are not shown in the schematics of Figure 4.3a for simplicity. It was observed that dynamic biasing of the bulk terminals of the main pass transistors ($M_{3\text{-}4}$) may significantly reduce the overall power efficiency. Indeed, they remained off when the voltage difference between their

source and gate was too low to allow conduction. Therefore, the bulk of the main pass transistors ($M_{3\text{-}4}$) was connected to V_{OUT} as it is the highest voltage available during the majority of the rectifier operating time due to the presence of an output charge reservoir.

The size of the main pass transistors ($M_{1\text{-}4}$) was optimized with respect to the associated parasitic in order to handle specified load currents with a sufficiently small channel resistance. Considering the time constant associated with the charging path of the bootstrapping capacitor and in order to get the best performance, it is necessary to inject enough charges into the bootstrapping capacitor (C_{B1} or C_{B2}). Thus, the sizes of transistors $M_{5\text{-}8}$ should be selected carefully. Similarly, transistors $M_{7\text{-}8}$ need to be sufficiently large.

It is of interest that some gate oxides and junctions may be subject to instantaneous voltage stress. Significant design efforts were invested to limit the current passing through the junctions and to ensure that all transistors remain in safe operating regions. A detailed study of possible instantaneous voltage stress was left for future research.

4.4 Simulation and Measurement Results

Power Conversion Efficiency (PCE), output average voltage, and Voltage Conversion Ratio (VCR) are the performance metrics commonly used to compare different rectifier structures [29].

The proposed rectifier was implemented at the circuit level using the standard TSMC 0.18 µm CMOS process with 3.3 V nominal supply voltage, and then characterized with the SpectreS simulator in the Cadence environment. A shunt load of C_L=200 pF and R_L=2 kΩ is considered. This load condition, when combined with applying a sinusoidal voltage source peak amplitude of 5 V and frequency of 10 MHz, leads to a load current up to 2.3 mA. This load condition fits the requirements of an intracortical stimulator implant application developed in our laboratory.

The main paths transistors ($M_{1\text{-}4}$) sizes are 20/0.35 µm with multiply factor of 50. Diode-tied transistors of M_5/M_6, which form the auxiliary paths are 1/0.35 µm, while the diode-connected transistors M_7/M_8 are implemented using 6/0.35 µm size transistors with multiply factor of 50. Small size pMOS transistors (0.50/0.35 µm) are employed to form DBS structures for dynamic bulk biasing of auxiliary path transistors. The size of bootstrapping capacitors ($C_{B1\text{-}2}$) is selected as 50 pF.

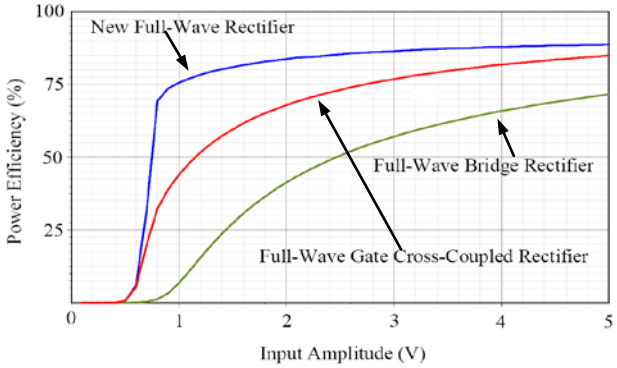


Figure 4.4. Simulated power conversion efficiency versus input peak amplitude.

4.4.1 Simulation results

In this section, we compare the simulation results of the FWBR and the FWGR [18] structures discussed earlier with our new proposed FWNR. Figure 4.4 shows the simulation results characterizing the PCE variation versus the peak input amplitude for these different structures using the same sizes for the main pass transistors ($M_{1\text{-}4}$) and load as already stated.

The FWNR presents significantly higher power conversion efficiency over a wide range of input peak amplitude greater than 0.8 V. Its power efficiency is remarkably higher than that of the other structures. With a 3.3 V AC source peak amplitude, the new rectifier offers a power efficiency up to 87%, which corresponds to an improvement by up to 11% and 47% compared to the FWGR and FWBR topologies respectively. These improvements result from the reduced effective threshold voltage, which leads to lower voltage drop across drain–source terminals of the pMOS main switches ($M_{3\text{-}4}$) and, from the large V_{GS} in cross-coupled nMOS transistors, $M_{1\text{-}2}$, which results in higher *gm* and lower channel on-resistance.

Simulated VCRs for different topologies are also illustrated in Figure 4.5. The results confirm that the circuit maintains its functionality as a rectifier even for a very low source voltage. It presents voltage conversion ratio larger than 70% for an AC input source with 0.8 V peak amplitude. This is significantly higher compared to other topologies.

Figure 4.5 also reveals that for the FWNR structure, the voltage conversion ratio rapidly reaches high values at low input source voltages, and remains the best for larger input voltages.

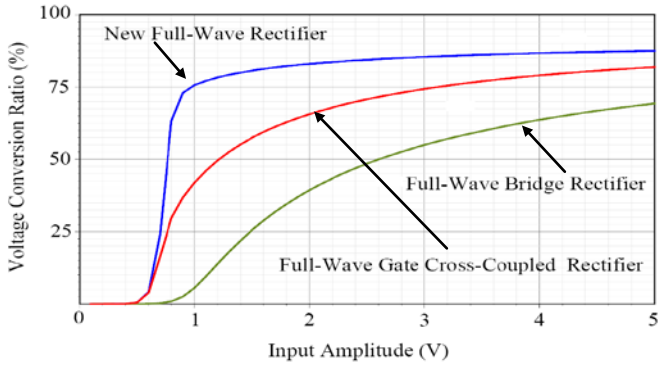


Figure 4.5. Simulated voltage conversion ratio versus input peak amplitude.

The significance of the new design with respect to VCR could be better visualized from a graph, in which the ratio of average output voltages for the FWNR and the FWGR structures is plotted. It was shown in [36] that the average output voltage for the FWNR is significantly higher than that of the FWGR, particularly for peak input voltages between 0.6 V to 2.2 V. For example, at 0.8 V input amplitude, the proposed FWNR produces an output voltage almost 2.1 times larger than the FWGR. Therefore, one may expect that the new design could be applicable to implement integrated rectifiers using new advanced sub-micron CMOS technologies where the nominal supply voltage is below 1 V. Based on separate simulation results, at 0.8 V input amplitude, the VCR is much larger when comparing FWNR and FWBR structures.

An important design concern could be the size of boot strapping capacitor. Integrated capacitors consume considerable area on the die when implemented using standard CMOS processes. Figure 4.6 shows how the PCE and VCR vary with the bootstrapping capacitor size. It shows that over a wide range of capacitance, the design performance in terms of PCE and VCR is not very dependent on the size of the embedded capacitors. The decrease in the PCE and VCR for bootstrapping capacitors larger than 100 pF could be explained by the impact of significant changes in the time constants of charging paths of the said capacitors as already addressed in Section III.

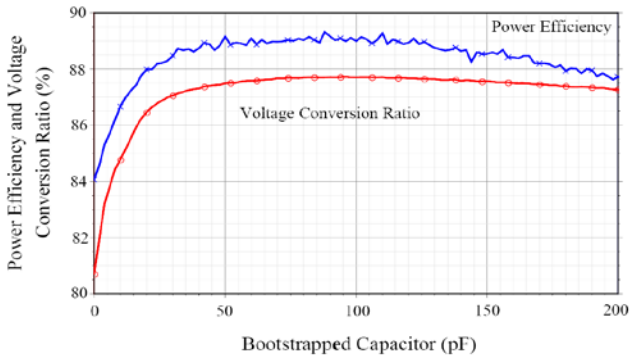


Figure 4.6. Simulated power efficiency and voltage conversion ratio versus bootstrapped capacitor size.

Considering the same input source amplitude, the rectifier with larger bootstrapping capacitors requires longer time to attain the adequate voltage. Therefore, for a given time frame, depending on the period of the input source, the gate-to-source voltage of the main pass transistors will be reduced, which causes them to represent smaller conductance. The results confirm that the new rectifier works very well with 50 pF capacitors which are feasible with standard CMOS processes.

4.4.2 Measurement Results

The proposed full-wave rectifier was fabricated using a 0.18 µm 6-Metal/2-Poly TSMC 3.3V standard CMOS process. The die photomicrograph is provided in Figure 4.7. This chip measures 780 µm x 780 µm and it is mounted in 40 pin dual-in-line package. Local substrates, needed for applying the DBS technique, were implemented using the deep n-well layer. All the main switches are surrounded by guard rings to isolate them from adjacent cells. In agreement with 3.3 V design rules, all transistors have channel lengths of 0.35 µm to maximize the speed of operation. The chip was carefully laid out to have a symmetrical structure minimizing potential imbalance in parasitic capacitances between the source rails (V_{IN+} and V_{IN-}). Pads with electro-static discharge (ESD) protection are used to feed the input source signal into the chip. The ESD supply voltages ($V_{DD\text{-}ESD}$ and $V_{SS\text{-}ESD}$) are directly accessible.

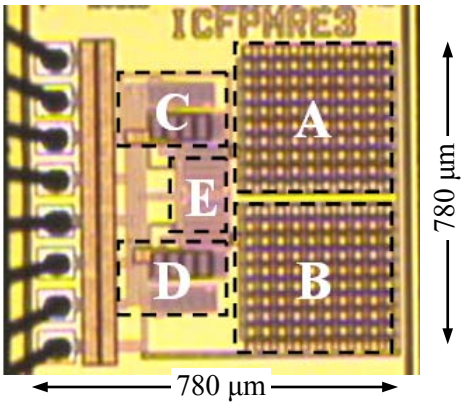


Figure 4.7. Photomicrograph of the prototype chip; A and B highlight boot strapped capacitors (C_{B1-2}), C and D address main pass transistors (M_{1-4}), and E marks the bootstrapping (M_{5-8}) and dynamic bulk biasing circuitry.

4.4.3 Measurement Setup and Test Protocol

To measure the performance of the fabricated rectifier, the measurement setup shown in Figure 4.8 was used. The rectifier implemented in this design requires a truly floating input signal to act as a full-wave rectifier. A wideband RF transformer with small insertion and return losses was used as an interface between the signal generator and the rectifier. Note that no terminal of the RF transformer secondary is at ground potential. This transformer is responsible to transfer energy to the rectifier inputs.

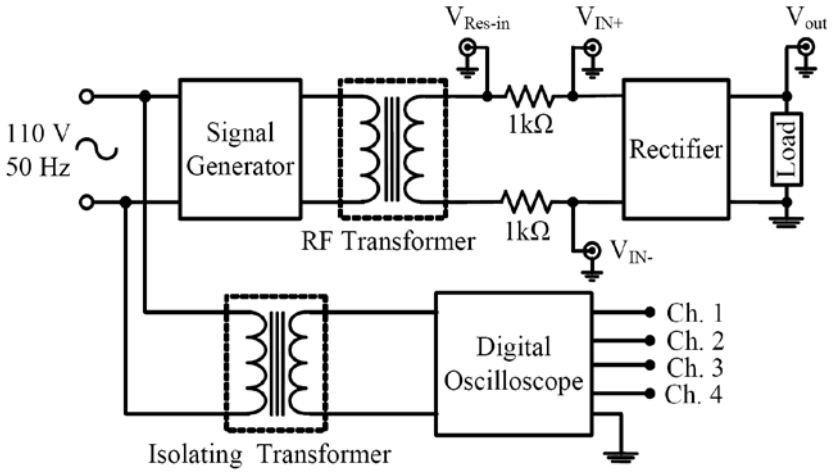


Figure 4.8. Voltage and power measurement setup.

The input voltage to the rectifier is not referenced to ground. Therefore, the oscilloscope cannot be used to view both the input and the load voltages of the rectifier at the same time. On the other hand, simultaneous measurements are required to increase reading accuracy. A solution to this problem is to use an isolating transformer (1:1) to decouple the oscilloscope from the common ground. This isolation helps avoiding ground loops (especially at operating frequencies in the mega hertz range) in the setup; it also allows referencing the output signal to voltages other than ground. Experiments confirmed that the use of these transformers is a necessity for proper operation.

The input power to the rectifier was measured as the integral of the instantaneous product of the input voltage by the input current over one period of the source. The output power was calculated as the integral of the squared measured output voltage divided by the load resistance over a period. The VCR was calculated as the ratio of the average output voltage to the input peak amplitude.

The input current was calculated using the measured drop voltage across a resistor in series with the RF transformer. The charge holding elements present at the output comprise a 200 pF explicit capacitor in addition to the capacitance of the output pad, of the package parasitics and of the probe of the test equipment. With an input sine wave peak voltage of 3.3 V operating at 10 MHz, the average output voltage was measured to be 2.89 V. This measured voltage represents a VCR of 87% at the given frequency.

A number of different source frequencies were applied to the laid-out rectifier that its results are shown in Figure 4.9. Here, the same rectifier which its elements were optimized such that the rectifier presents the maximum power at 10 MHz operating frequency, was used. It is of interest that the parameters producing maximum power efficiency may not be the same as those that produce maximum voltage efficiency. It was noted that, as expected, higher source frequencies produce larger power efficiency and average output voltages, which the later results in larger VCRs. Figure 4.10 illustrates the measured and the post-layout simulated VCRs for the same no-load condition (except parasitics associated with probe and pads) at 10 MHz source frequency. At 1.0 V, 1.8 V, and 3.3 V AC peak input amplitudes, voltage conversion ratios of 70%, 80%, and 87% are obtained.

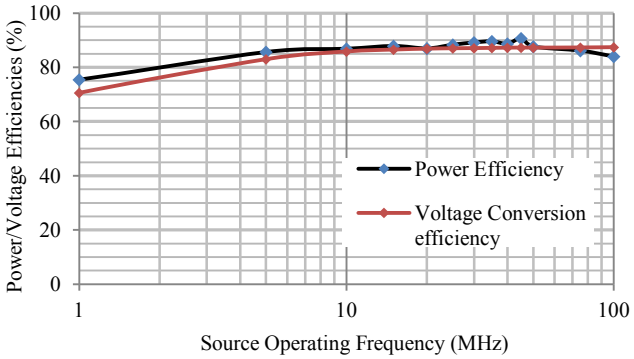


Figure 4.9. Simulated frequency response of the proposed rectifier.

The deviation of the measured results compared to post-layout simulations can be explained by the impacts of two phenomena; 1) the charge sharing between the bootstrapping capacitors and the parasitic capacitances, and 2) the leakage to the bulk of the main pass transistors. For applications with high operating frequency, as encountered in biomedical implants, parasitic capacitors associated with MOS terminals and interconnections should be considered. Many parasitics in the proposed circuit cannot be modeled as capacitors in parallel with the bootstrapping capacitors. Depending on their representations, they might contribute in further charge accumulation producing more efficient bootstrapping or in charge sharing degrading the efficiency of the said technique.

Nevertheless, from the observation of the results presented in Figure 4.6, one may consider

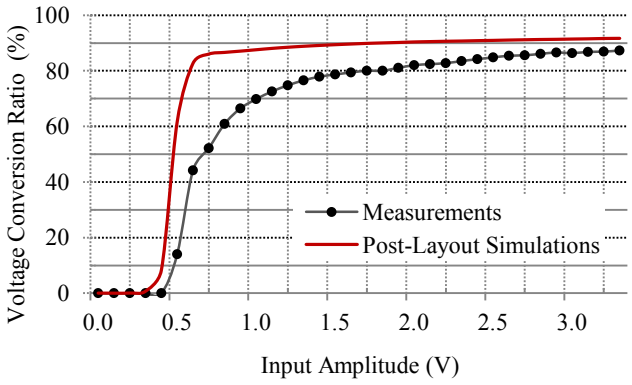


Figure 4.10. Measured voltage conversion ratio of the proposed full-wave rectifier versus input amplitude operating at f=10 MHz.

the charge sharing effect to be less affecting the VCR of the circuit than the leakages current, and hence ignore it. This is not particularly true due to lack of accurate simulation models to emulate the representation of the parasitics and to predict their impact on the performance of the rectifier. It is of interest that leakage through bulk to the rectifier output contributes in load current. Depending on the portion of the load current passing through the source-to-n well junction, which is connected to output node, the rectifier efficiency varies.

In the measurements, parasitic capacitances consist of the parasitics associated with the gate of the extremely large main pass pMOS transistors ($M_{1\text{-}4}$), the large interconnection metal strips, and the significant parasitics capacitances associated with the output pads and oscilloscope probe. In fact, the occurred charge sharing may result in wasted charges, which reduces the output voltage. The results are more affected at low voltages, where the threshold reduction technique is less effective due to slow switching. However, the measured results are significantly better than that of the other topologies.

Figure 4.11 depicts the measured power efficiency versus input amplitude for the rectifier with a 2 kΩ load resistance shunting a 200pF capacitance, at source frequency of 10 MHz. The overall power efficiency is measured to be 37%, 71%, and 80% at 0.8 V, 1.8 V, and 2.7 V peak input source amplitudes.

Here, the difference between the results obtained from simulations and measurements could be explained by the fact that significant leakage currents flow through the bulk of the main pass pMOS transistors ($M_{1\text{-}4}$) considering the fixed biasing of the bulk when the source is floating. In

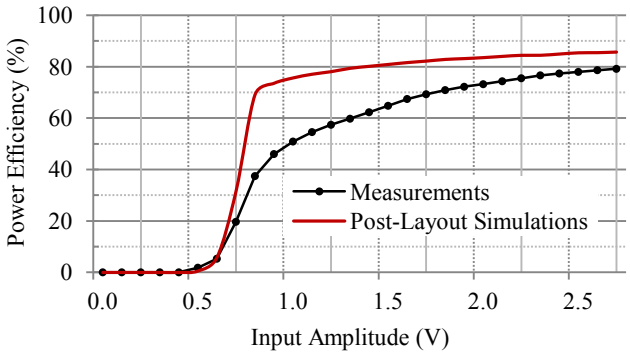


Figure 4.11. Measured power conversion efficiency of the proposed full-wave rectifier operating at f=10 MHz.

the proposed rectifier, the bulk of $M_{1\text{-}2}$ is connected to the ground while the bulk of $M_{3\text{-}4}$ is connected to V_{Out}. Therefore, depending on the load and floating source conditions, there will be time intervals when the parasitic vertical diodes, formed between n-well and substrate of the said pMOS transistors, become forward biased, which leads to significant leakage current to their substrate. Thus, protecting the main pMOS transistors against the bulk-to-substrate leakage is crucial. This could be done using the DBS technique as explained for auxiliary paths transistors, $M_{6\text{-}7}$. However, it was found that applying the said technique does not improve the efficiencies due to very short time intervals when the gate-to-source voltage of DBS transistors is not sufficient to form their channels, a necessary condition for the main pass transistors to operate.

Moreover, the circuit employs pads with ESD protection implemented using the vertical parasitic diodes formed between diffusion, n-well and substrate. Here, p-diodes are used for directing the input spikes towards the $V_{DD\text{-}ESD}$ ring and n-diodes are used for suppressing them using the $V_{SS\text{-}ESD}$ ring. In our implementation, there are two parallel p-diodes and two parallel n-diodes used for such protection. The p-diode, n-diode, and n-well diode are respectively subject to a 200 nA, 400 nA, and 650 nA reverse bias current.

Considering the fact that there are 6 pads used for accessing the rectifier, the leakage current through these diodes can be calculated to be 2.4 µA, 4.8 µA and 7.8 µA respectively. Assuming that normal operation of the rectifier involves all those parasitic diodes to be reversely biased, there are cases where all this leakage occurs simultaneously, leading to a leakage of 15 µA. At a low input voltage, and considering the charge sharing phenomenon as explained in the analysis of the results in Figure 4.10, this leakage may constitute more than 10 % of the total power consumption of the rectifier. Thus, using proper biasing for the bulk of the main pMOS transistors and using probe connections on die instead of pads, may make measurements and post-layout simulation results more consistent.

Based on a separate observation, measurements confirm that the power efficiency decreases with the load current. This may be due to an increase of the power consumption within the channel of the main pass and auxiliary paths transistors, as well as the leakage current from the source to the bulk of the main pass transistors. Recall that these leakages contribute to the load current when V_{IN} is higher than V_{OUT}. Table 4.1 summarizes the results obtained from the post-layout simulation and the measurements for a load of 2 kΩ in shunt with a 200 pF capacitance.

Table 4.1. Post-layout and measurement results.

Metrics	Post-Layout Simulations			Measurements		
Source peak Amplitude (V)	0.8	1.8	2.7	0.8	1.8	2.7
Power Efficiency (%)	69	83	86	37	71	80
Average Output Voltage (V)	0.5	1.5	2.3	0.3	1.2	2.0

Unfortunately, the existing differences in terms of process and feature sizes, prevents us to be able to compare all reported characteristics of the state-of-the-art rectifiers. However, among the designs using standard CMOS processes with given feature size, for the same source amplitudes as reported in Table 4.1, the result of the comparison, as stated in Table 4.2, confirms that, the proposed rectifier topology generates the best output voltage and power efficiency compared to other reported results particularly when operating from low source voltages.

The advanced rectifiers rarely provide large load currents, which is the case for most biomedical implantable devices. The proposed rectifier and the gate cross-coupled rectifier, even with elements implemented using sub-micron CMOS integrated circuits, are capable of handling significant load currents, as large as a few mA. However, the gate cross-coupled topology uses a

Table 4.2. Comparison with most advanced rectifier characteristics

Rectifier Topology	Process	Source Amplitude (V)	Output Voltage (V)	Power Efficiency (%)	Load (kΩ)
Gate Cross-Coupled [18]	BiCMOS 1.50 μm	9.0	6.54	-	1
V_{TH} Reduction [19]	CMOS 0.25 μm	2.5	0.9	55	20
Self V_{TH} Cancelation [37]	CMOS 0.18 μm	1.8	-	32	10
This Work	CMOS 0.18 μm	0.8	0.3	37	2
		1.8	1.2	71	
		2.7	2.0	80	

BiCMOS process, with significantly longer feature size compared to the standard deep sub-micron CMOS process used in fabricating the proposed rectifier.

Remember that charge-pump-based (voltage doubler) rectifiers realized using small charge reservoirs do not maintain large charges and, therefore, fail to provide significant current. Simulation-based results of implementing the gate cross-coupled structure in deep sub-micron technologies confirm that the resulting rectifier is not power and voltage efficient at low source voltages. Other advanced rectifiers implemented in smaller feature sizes (except the rectifier in [37]) provide neither large load currents, nor present high power efficiencies. Some of them [19] require large off-chip capacitors in the micro-Farad range which makes their implementation unfeasible in advanced integrated circuit processes. Measurements reported in [37] also confirm that the said rectifier is not a good candidate for implementing rectifiers with high voltage and power efficiencies when using low source voltages.

The stated results for voltage conversion ratios could be explained as the result of leakage through bulk terminals of the main pass transistors and of the flow-back current from output node toward the source when the output voltage is larger than the inputs. Charge sharing between the bootstrapping capacitor and the parasitic capacitances associated with the gate of the main pMOS pass devices may caused result derivation. The leakage currents due to use of large ESD protection diodes and the parasitics associated with the interconnections could also be considered as other potential reasons for the drift in simulation and measurements.

As a general design practice, the reported implementation uses ESD (electrostatic discharge) protected pads. The full impact of this design choice was fully appreciated when the prototype circuit was experimentally tested. Even though dedicated V_{SS} and V_{DD} pads that can be tied to suitable voltage allow mitigating this effect in our prototype, we noticed that leakage paths to the substrate can be activated. ESD protection with this class of circuit can become a challenging issue that was left for future research.

From power efficiency standpoint, the measured results are in agreement with simulations if the proper bulk biasing technique is employed to bias the bulk of the pMOS main transistors and the leakage through large ESD protection diodes is mitigated.

It was also noted that for peak voltages higher than 1.8V, the power efficiency is significantly reduced. It is conjectured that the main pass transistors have significant leakage currents resulting from voltage stress. Table 4.2 presents the comparison between the measured characteristics obtained from the proposed rectifier and the most advanced full-wave rectifiers described in the literature. Note that the performance of respective circuits is quoted for different load conditions and processes.

4.5 Conclusions

A full-wave integrated rectifier was presented. It is suitable for many applications including smart biomedical implants and RFID tags. The structure does not require complex circuit design. The new design employs MOS-based gate cross-coupled nMOS switches along with pMOS switches equipped with reduced effective threshold voltage technique to achieve AC to DC conversion. The simultaneous application of a cross-coupled structure and threshold reduction techniques can result in very low voltage drop across the MOS switches. The rectifier also uses dynamic body biasing in auxiliary paths. This design has been fabricated using the standard 0.18 µm 3.3 V TSMC CMOS process. The schematic and post-layout simulations confirm significantly higher power and voltage efficiencies of the proposed rectifier compared to other advanced rectifier structures. The measurements also confirm that the proposed rectifier provides a higher voltage conversion ratio than previously reported designs. It also confirms that the use of the proposed rectifier is advantageous, particularly when the power supply source voltage is low.

4.6 References

[1] R.F. Weir, et al, "Implantable myoelectric sensors (IMESs) for intramuscular electromyogram recording," IEEE Trans. Biomedical Engineering, vol. 56, no. 1, pp. 159-171, Jan. 2009.

[2] B. Gosselin, et al., "A mixed-signal multichip neural recording Interface with bandwidth reduction," IEEE Trans. Biomedical Circuits and Systems, vol. 3, no. 3, pp. 129-141, June 2009.

[3] H. Nakamoto, et al., "A passive UHF RF identification CMOS tag IC using ferroelectric

RAM in 0.35-um technology," IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 101-110, Jan. 2007.

[4] J. Liu, et al., "Wireless RF identification system based on SAW," IEEE. Trans. Industrial Electronics," vol. 55, no. 2, pp. 958-961, Feb. 2008.

[5] D.J. Yeager, et al., "NeuralWISP: A wirelessly powered neural interface with 1-m range," IEEE Trans. Biomedical Circuits and Systems, vol. 3, no. 6, pp. 379-387, Dec. 2009.

[6] Y.-K. Song, et al., "Active microelectronic neurosensor arrays for implantable brain communication interfaces," IEEE Trans. Neural Systems and Rehabilitation Engineering, vol. 17, no. 4, pp. 339-345, Aug. 2009.

[7] A.D. DeHennis, et al., "A wireless microsystem for the remote sensing of pressure, temperature, and relative humidity," IEEE J. Microelectromechanical Systems, vol. 14, no. 1, pp. 12-22, Feb. 2005.

[8] F. Shahrokhi, et al., " The 128-Channel Fully Differential Digital Integrated Neural Recording and Stimulation Interface," IEEE Trans. Biomedical Circuits and Systems, vol. 4, no. 3, pp. 149-161, June 2010.

[9] S.K. Kelly, et al., "A Power-Efficient Neural Tissue Stimulator with Energy Recovery," IEEE Trans. Biomedical Circuits and Systems, vol. 5, no. 1, pp. 20-29, Feb. 2011.

[10] M.M. Ahmadi, et al., "A Wireless-Implantable Microsystem for Continuous Blood Glucose Monitoring," IEEE Trans. Biomedical Circuits and Systems, vol. 3, no. 3, pp. 169-180, June 2009.

[11] S. Ethier, et al., "Exponential Current Pulse Generator for Efficient Very High-Impedance Multisite Stimulation," IEEE Tran. Biomedical circuits and systems, vol. 5, no. 1, pp. 30-38, Feb. 2011.

[12] G. Simard, et al., "High-Speed OQPSK and Efficient Power Transfer Through Inductive Link for Biomedical Implants," IEEE Trans. Biomedical Circuits and Systems, vol. 4, no. 3, pp.192-200, June 2010.

[13] J. Coulombe, et al., " A Highly Flexible System for Microstimulation of the Visual Cortex: Design and Implementation," IEEE Trans. Biomedical Circuits and Systems, vol. 1, no. 4, pp. 258-269, Dec. 2007.

[14] H.P. Rayait, et al., "Interpretations of Wrist/Grip Operations From SEMG Signals at Different Locations on Arm," IEEE Tran. Biomedical Circuits and Systems, vol. 4, no. 2, pp. 101-111, Apr. 2010.

[15] H.-Ch. Liu, et al., "A novel battery-assisted class-1 genreation-2 RFid entification tag design," IEEE Trans. Microwave theory and Techniques, vol. 57, no. 5, pp. 1388-1397, May 2009.

[16] H.-L. Jung, et al. "Feasibility study on a new energy harvesting electromagnetic device using aerodynamic instability," IEEE Trans. Magnetics, vol. 45, no. 10, pp. 4376 -4379, Oct. 2009.

[17] D. Guyomar, et al., "Energy harvesting based on FE-FE transition in ferroelectric single crystals," IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control, vol. 55, no. 2, pp. 279-285, Feb. 2008.

[18] P. Rakers, et al., " "Secure Contactless Smartcard ASIC with DPA Protection," IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 559-565, Mar. 2001.

[19] T. Le, et al., "Piezoelectric micro-power generation interface circuits," IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1411–1420, June 2006.

[20] U. Karthaus, et al., "Fully integrated passive UHF RFID transponder IC with 16.7-mW minimum RF input power," IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[21] A. Facen, et al ., " Power supply generation in CMOS passive UHF RFID tags," Research in Microelectronics and Electronics 2006, Ph.D. dissertation, pp. 33 –36, June 2006.

[22] J. Hu, et al., "A low power and high performance analog front end for passive RFID transponder," IEEE workshop Automatic Identification Advanced Technologies, pp. 199-204, Oct. 2005.

[23] T. Lehmann, et al., ''On-chip active power rectifiers for biomedical applications,'' Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), vol. 1, pp. 732–735, Japan, May 2005.

[24] C. Peters, et al., "CMOS integrated highly efficient full wave rectifier," IEEE Int. Symp. Circuits and Syst., pp. 2415–2418, 2007.

[25] C.L. Chen, et al., "Efficiency enhanced CMOS rectifier for wireless telemetry," Electron Letters, vol. 43, no. 18, 2007.

[26] S. Atluri, et al., "Incorporating back telemetry in a full-wave CMOS rectifier for RFID and biomedical applications," Proc. IEEE Int. Symp. Circuits Syst., pp. 801–804, 2007.

[27] G. Lazzi, "Thermal effects of bioimplants," IEEE Eng. Med. Bio. Mag., vol. 24, no. 5, pp. 75–81, 2005.

[28] Y-H. Lam, et al., "Integrated low-loss CMOS active rectifier for wirelessly powered devices," IEEE Trans. Circuits Systems II, vol. 53, no. 12, pp. 1378–1382, 2006.

[29] S. Hashemi, et al., "A novel low-drop active rectifier for RF-powered devices: Experimental results," Elsevier Microelectronics Journal, 2009.

[30] G. Bawa, et al., "Active high power conversion efficiency rectifier with built-In dual-mode back telemetry in standard CMOS technology," IEEE Trans. Biomedical Circuits and Systems, vol. 2, no. 3, pp. 184-192, Sept. 2008.

[31] T. Umeda, et al., "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 35–41, Jan. 2006.

[32] T. Lehmann, et al., "1-v power supply CMOS cascode amplifier," IEEE J. Solid-State Circuits, vol. 36, no. 7, pp. 1082–1086, July 2001.

[33] C. Peters, et al., "Experimental Results on Power Efficient single-Poly Floating Gate Rectifier," IEEE Int'l Symp. Circuits and Systems, Taiwan, 2009.

[34] P. Favrat, et al., "A high-efficiency CMOS voltage doubler," IEEE J. Solid-State Circuits, vol. 33, no. 3, pp. 410-416, Mar. 1998.

[35] M. Ghovanloo, et al., "Fully integrated wideband high-current rectifiers for inductively powered devices," IEEE Trans. Solid-State Circuits, vol. 39, no. 11, pp. 1976–1984, Nov. 2004.

[36] S. Hashemi, et al., "Fully-integrated low-voltage high-efficiency CMOS rectifier for wirelessly powered devices," IEEE Int'l New Circuits and Systems Conf., France, 2009.

[37] K. Kotani, et al., "High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation techniques," IEEE 8th Conf. ASIC (ASICON'09), pp. 20-23, Oct. 2009, Changsha, China.

Chapter 5 : **LOW-AREA BOOTSTRAP RECTIFIERS**

The boot strap pa ssive r ectifiers us e t he boot strapped c apacitor t echnique t o alleviate th e effective t hreshold vol tage of m ain pa ss M OS t ransistors w hen t hey conduct. U sing t his technique, t he effective threshold vot lage of t he m ain pM OS t ransitors a re replaced w ith t he difference between two threshold voltages of the MOS transitors used in the main and charging path. The previously presented boostrap rectifier used dual circuity forming auxiliary charging paths and bootstrapped capacitors.

An improved version of the double-reservoir bootstrap rectifier with short auxiliary paths is presented in this chapter, where the auxiliary paths are implemented using parasitic P-N junction diodes of main pass pMOS transistors. The design still suffers from the flow-back current from load towards the source. This can occur in some particular source and load conditions and if not mitigated, it degrades power efficiency.

Different ve rsions of f low-back current f ree d ouble-reservoir b ootstrap re ctifiers are also proposed. In a f irst ve rsion, a dua l c ontrol s cheme i s us ed t o d ynamically c onnect t he bootstrapped capaciotrs to the gate of each pMOS main pass transisotr. A second version of the flow-back free double-reservoir bootstrap rectifier uses a diode with reverse polarity in parallel with the charging diode-connected transistors to force the voltages of the bootstrapped capacitors to c losely t rack th e o utput v oltage. T he d iode w as imp lemented u sing p arasitic b ulk-substrate junction diode of charging paths transistors. The simulation results show that the proposed bulk biasing techniques significanlty increase the power efficiency of the rectifiers.

This chapter also covers the desinng and implementation of a new full-wave rectifier based on bootstrapped capacitor technique which uses a single small bootstrapped capacitor along its charging paths to reducing the effective threshold of main path MOS transisotrs in each source cycles. Yet, it uses the partially gate cross-coupled structure to have faster settling time and lower switch r esistances. T he proposed s ingle-reservoir b ootstrap re ctifier functions v ery w ell w ith asymettrical inputs. The proposed r ectifiers w ere i mplemented an d l aid-out us ing the TSMC 0.18 μm CMOS standard process. The s ingle-reservoir r ectifier a lso s aves a lmost 7 0% s ilicon area saving compared to previusly proposed double-reservoir structures. The experimental results

show g ood a greement w ith s imulationss. T his w ork w as s ubmitted t o IEEE t ransactions on Circuits and Systems: Regular Papers-I and is reproduced as follows.

Low-Area and Flow-Back Current Free CMOS Integrated Rectifiers for Power Scavenging Devices

Saeid Hashemi, Mohamad Sawan, *Fellow, IEEE*, and Yvon Savaria, *Fellow, IEEE*

Abstract- *This paper presents advanced topologies for full-wave CMOS rectifiers. They use bootstrapped capacitors to reduce the effective threshold voltage of selected MOS switches in the positive and negative input source cycles. The new double-reservoir rectifier (DRR) employs separate charge reservoirs, while the single-reservoir rectifier (SRR) also proposed in this paper uses a single capacitor. The DRR uses new control schemes to reduce the flow-back current from the load to the source. It also presents an efficient solution to the problem associated with bulk biasing of transistors exposed to varying voltages. The proposed topology also removes the need for auxiliary paths to charge bootstrapped capacitors at start-up. The SRR topology uses a simple control. Both topologies present significant increases in power efficiency and reduction in voltage drops. The proposed rectifiers were implemented and laid-out using a standard TSMC 0.18 μm CMOS process and then characterized with the SpectreS simulator. The post-layout-based simulation results were found to be in good agreement with measurements on the implemented devices. The improved DRR presents 14% and 20% increase in power efficiency for input peak voltage of 0.8 V and 1 V, respectively. The SRR saves almost 70% area compared to a previously reported DRR structure. For a source peak amplitude of 1.8 V, the SRR presents 8% and 18% increase in power and voltage conversion efficiencies respectively, compared to the previous version. The measurements show that the new rectifier presents significantly higher performance with AC source amplitudes of less than 1 V peak.*

Index Terms— Rectifiers, B ootstrapping t echnique, T hreshold c ancellation, B iomedical implants, Power harvesting.

5.1 Introduction

Advances in wireless communications have led to the development of low-voltage and low-power integrated circuits. They are necessary for supporting the functionality and meeting the desired performances of embedded electronic systems, such as wireless sensors networks [1-3], radio frequency identification (RFID) tags [4-5], and smart biomedical devices [6-7]. Various powering techniques including embedded batteries and transcutaneous transmission are relatively constrained in terms of energy density, device lifetime, potential hazards to human safety, integration, and required space. Thus, providing adequate energy to power up electronic implants remains challenging.

On the other hand, energy harvesting techniques are processes by which energy readily available from the environment (including the human body) is harvested and converted into usable electrical energy. Remarkable efforts dedicated to developing these techniques reveal that they can be inexpensive, highly compatible with electronics, and capable of procuring fairly high power levels. On the other hand, these techniques are not yet considered reliable and feasible, although research is steadily progressing [8-9].

Several types of wireless systems benefit from inductive links to extract power from the signal received by an antenna [10-11]. In this case, a radio frequency (RF) signal is commonly used to transmit data and transfer the energy required for carrying the intended functions. This technique is more convenient and advantageous compared to wired [6] and battery-based architectures [12]. This is particularly true for biomedical implants where human safety and convenience are involved and system autonomy is a bottleneck.

In a wirelessly-powered structure, a rectifier is required to convert an input AC signal to an unregulated DC voltage. Therefore, its power efficiency significantly affects the performance and characteristics of the power conversion chain. Conventional full-wave rectifiers such as bridges and gate cross-coupled structures [13-14] fail to present high efficiencies when operating from low voltage alternating current (AC) sources, typically used with advanced sub-micron processes. Indeed, their output voltage is constrained by the forward-bias drop of one or two diodes in each input cycle. Some rectifier configurations allow replacing diodes with MOS transistors acting in

their triode region, where they present voltage drops lower than a diode [15]. Their power efficiency can be greatly improved at the expense of extra layout efforts and/or use of complex control schemes.

Recently, the authors proposed a circuit using the bootstrapped capacitors technique to reduce the effective threshold voltage of a diode-tied MOS transistor to the difference between two threshold voltages [16-17]. It significantly improves the output voltage and the power efficiency.

In this paper, circuit techniques are proposed to overcome the flow-back current from load to source during time intervals when the input voltage gets smaller than the voltage on the output node. A new rectifier structure that removes the need for auxiliary paths responsible for charging the bootstrapped capacitors is then proposed. We also propose a new rectifier configuration that combines the bootstrapped capacitor technique along with an improved control scheme to derive a new high-efficiency low-voltage rectifier, employing a single charge reservoir, which is highly efficient in terms of silicon area.

The remainder of this paper includes, in Section II, a brief description of the characteristics of the bootstrapped capacitor-based rectifiers. Section III includes the analysis of the rectifier auxiliary paths, the conditions that cause flow-back currents, and provides circuit solutions to remove them. Section IV introduces a new topology for low-area rectifiers based on the bootstrapped capacitor technique along with circuit description and characteristics. Section V provides concluding remarks.

5.2 Bootstrapped-Capacitor Based Rectifiers

There are various circuit techniques to alleviate the impact of threshold voltage, V_{Th}, of MOS transistors. They benefit either from dynamic techniques for gate-drain [18] or bulk-source (body-effect) biasing [19]. These techniques commonly benefit from a DC voltage generated in an idle phase to reduce the effect of V_{Th} of MOS transistors in the active phase. Applying the floating gate technique is also reported as a means to program the threshold voltage of the given MOS transistor during setup and erase phases [20]. However, this technique requires high-voltages, which implies additional implementation constraints. The leakage of induced charges

on the floating gate via the oxide layer also subjects the design to long term reliability problems. The latter technique is also restricted to low operating frequencies. Another technique accomplishes threshold cancellation by using bootstrapped capacitors [21]. Using this technique, the effective threshold voltage of a diode-connected MOS transistor is reduced to the difference between two threshold voltages. Among currently known techniques, this is the best suited with advanced standard CMOS processes, where implementing integrated capacitors is feasible. This technique was employed to implement a high efficiency full-wave rectifier as illustrated in Figure 5.1a [17] that presents the schematics of the double-reservoir rectifier (DRR) with its previously reported bootstrapped pMOS setup (Figure 5.1b) called DRR-1 in this paper. The dual of this bootstrapping circuit is used in the same manner for negative source cycles. This dual circuit links the other input source rail, V_{IN-}, the second bootstrapped capacitor, C_{B2}, and the output node.

It was shown that with a typical MOS transistor, with regular threshold voltage, the

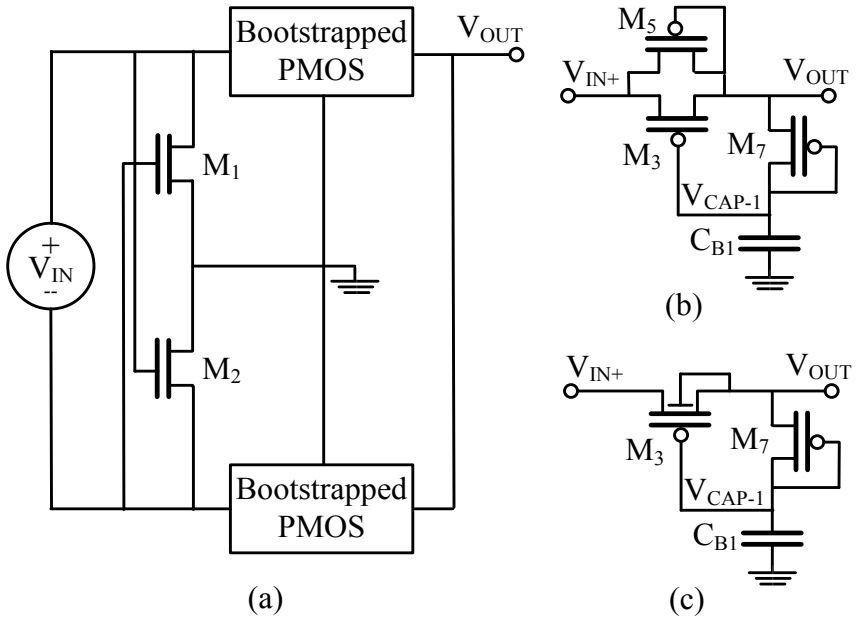


Figure 5.1. Schematics of: a) the double-reservoir rectifier: b) its original bootstrapped pMOS setup (DRR-1) [17], c) its revised bootstrapped pMOS setup with short-auxiliary paths (DRR-2).

simultaneous application of the cross-coupled structure and threshold reduction technique results in a very low voltage drop across the pMOS switches, $M_{3\text{-}4}$. This leads to significantly higher power and voltage efficiencies compared with conventional bridge and gate cross-coupled rectifier topologies. This becomes increasingly significant with current deep sub-micron technologies where the nominal voltage is less than 1 V.

5.2.1 Short Auxiliary Paths

Within the original DRR structure (DRR-1), as shown in Figure 5.1b, there are transistors for which the source and drain terminals are subject to significant voltage variations. For instance, the pMOS transistors located in the main (M_3), the auxiliary (M_5), and charging (M_7) paths are in that situation. Therefore, providing adequate biasing for the bulk of the exposed transistors is essential as these transistors may inject (leakage) current into the substrate and induce latch-up.

The authors have proposed using a dynamic bulk switching (DBS) technique to bias the bulk of the selected transistors [14,22]. Using this technique, the bulk of the exposed pMOS transistors are selectively connected to the highest available voltage that can be observed at their drain and source terminals. This DBS technique also eliminates the body effect on the selected transistors. Implementing such bulk biasing implies an additional effort at the layout level as it requires locally isolated wells or substrate.

This technique was originally applied on all pMOS transistors in the main, auxiliary, and charging paths (DRR-1). These circuits are not shown in Figure 5.1b for simplicity. However, we recently demonstrated that the use of the DBS technique is not beneficial if applied to the bulk of the main pass switches, as they significantly degrade the power efficiency of the rectifier [17].

On the other hand, the DRR-1 includes circuit branches (auxiliary path) for positive input cycles. These paths allow charging the holding capacitors (for instance C_{B1}) and they are essential when there is no other means of harvesting power within the design, especially at startup [14,22].

Here, we propose to employ a so-called short auxiliary path as it employs the parasitic diode formed at the junction of a diffusion island and the bulk of the main pass switches. It acts as an

auxiliary path, providing proper bias to the main switches (see DRR-2 in Figure 5.1c). It is implemented by connecting the bulk terminal of the main pass transistors to V_{OUT}. Therefore, the proposed setup simultaneously serves as bulk biasing of the main pass switches, while providing auxiliary paths from input to the holding capacitor. Note that the output node maintains the highest voltage available in the circuit during the greater part of the rectifier operating time. Note also that the pMOS transistor bulk in the charging paths, M_7, is still biased using the DBS technique [17]. The same is true of M_8, the dual transistor not shown in Figure 5.1c.

The probability of latch-up is also reduced by considering conservative approaches at the layout level. This implies implementing the large transistors far enough from each other, and employing isolated (local) substrates for nMOS transistors for which the bulk is connected to voltages other than the ground.

Transistor sizes of typical designs based on the various considered topologies optimized for a

Table 5.1. Circuit parameters for rectifier topologies.

Circuit Element	Rectifier Topology				
	DRR-1	**DRR-2**	**DRR-3**	**DRR-4**	**SRR**
$M_{1\text{-}4}$ (µm)	1000/0.35	1000/0.35	1000/0.35	1000/0.35	1000/0.35
$M_{5\text{-}6}$ (µm)	1.0/0.35	N/A	N/A	N/A	1.0/0.35
M_7 (µm)	50/035	50/035	50/0.35	50/0.35	50/0.35
M_8 (µm)	50/035	50/035	50/035	50/035	N/A
M_{DBS} (µm)	0.50/0.35	0.50/0.35	0.35/0.35	N/A	N/A
M_a (µm)	N/A	N/A	7.35/0.35	N/A	N/A
M_b (µm)	N/A	N/A	10.35/0.35	N/A	N/A
M_c (µm)	N/A	N/A	7.5/0.35	N/A	N/A
$M_{8\text{-}11}$ (µm)	N/A	N/A	N/A	N/A	0.35/0.35
$M_{12\text{-}13}$ (µm)	N/A	N/A	N/A	N/A	10/1.5
$C_{B\text{-}1/2}$ (pF)	2 × 50	2 × 50	2 × 50	2 × 50	1 × 6
C_L (pF)	200	200	200	200	200
R_L (kΩ)	2	2	2	2	2
$V_{IN\text{-}Peak}$ (V)	3.3	3.3	3.3	3.3	3.3
f_{IN} (MHz)	10	10	10	10	10

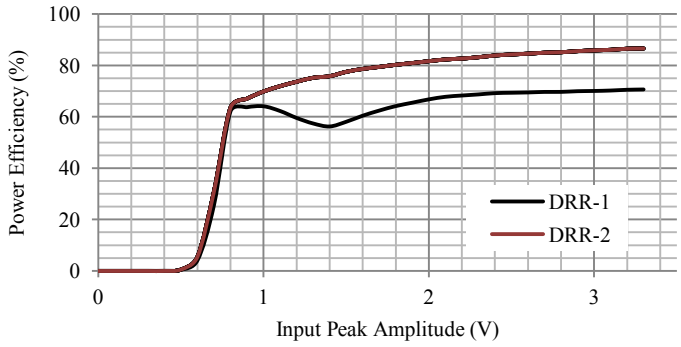


Figure 5.2. Simulated power efficiency versus input peak amplitude for the DRR-1 and DRR-2 structures.

shunt RC load and a sine wave source capable of providing up to 1.5 mA are reported in Table 5.1. Such a current was found to be necessary for driving up to 16 channels of an intra-cortical stimulator being implemented in the Polystim neurotechnologies laboratory [23]. Figure 5.2 plots the results of schematics-based simulations for power conversion efficiency (PCE) versus input peak amplitude of DRR structures. It shows that the proposed DRR-2 presents significantly higher power efficiency than the DRR-1.

For instance, for input peak voltage of 1-V, DRR-2 gives 9% higher power efficiency than the DRR-1, with the same circuit elements. This improvement increases significantly to over 35% for higher input peak amplitudes. Based on other circuit simulation results, very similar to

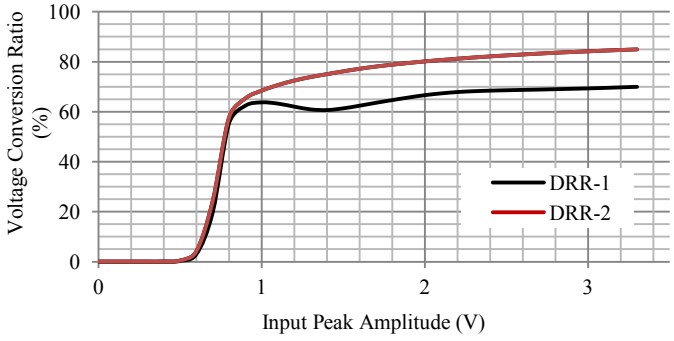


Figure 5.3. Simulated voltage conversion ratio versus input peak amplitude for the DRR-1 and DRR-2 structures.

Figure 5.2 in shape, it is observed that the DRR-2 structure also presents significantly higher voltage conversion ratios (VCR) compared to DRR-1. It was also observed that the settling time of the DRR-2 circuit is shorter than that the DRR-1. This is due to very large size transistors which are used to implement the main switches and therefore, the associated parasitic diodes are larger, which allows larger current. As a result the bootstrapped capacitors are charged faster. Figure 5.3 plots the voltage conversion ratios for the DRR-1 and the DRR-2 structures. It shows that the DDR-2 structure presents significantly higher VCR for different input peak amplitudes. For instance, with a 1-V source peak amplitude, the DRR-2 structure offers VCR improvement of 7%. This ratio also increases significantly up to 25% for higher input source amplitudes.

5.3 Flow-Back Current Free Rectifiers

Different factors may impose the value of input and output voltages. The input sinusoidal voltage varies over time above and below the output voltage periodically. For a wirelessly-powered device using inductive link, apart from the periodic amplitude variations, there are also time intervals, when, for a given input source amplitude, the induced voltage in the secondary coil abruptly changes. This happens notably due to changes in distance and orientation of the primary and secondary coils with respect to each other. These changes result in output voltage variations, which provoke output ripples depending on the output holding capacitor, load condition, and leakage currents.

Therefore, during normal operation of the previously presented DRR circuits, there are time intervals when the input voltage gets smaller than the output voltage. Indeed, when $V_{IN}<V_{OUT}$ and V_{CAP} is at least one threshold voltage below the output voltage, the current flow in the main pass pMOS transistors ($M_{3\text{-}4}$) reverses. The value of this current depends on the voltage difference between the output node and the input source, and on the size and gate-to-source voltage of the main pass transistors. However, for design used in variable source and load conditions, this flow-back current may significantly degrade the performance of the rectifier from a power efficiency stand point. We propose different solutions to this problem in the following sections.

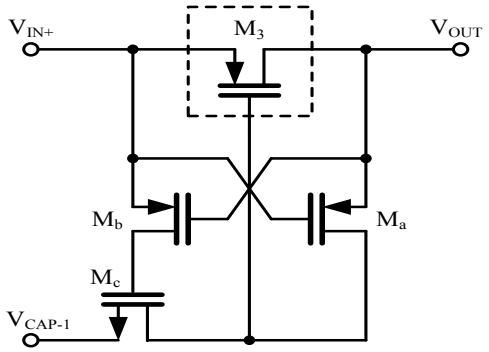


Figure 5.4. Schematic of control scheme for positive cycles.

5.3.1 Control Scheme to Limit Flow-Back Current

Figure 5.4 shows a circuit that we propose to reduce the flow-back current. It employs a dedicated control scheme which is configured within the previously presented DRR-2 structure (DRR-3). In fact, each main pass transistor, for instance M_3, is equipped with the proposed control circuit. During each input cycle, this circuit continuously compares the input and output voltages and connects V_{CAP-1} to the gate of the main pass switch, M_3, when the proper conditions are met. For the source positive cycles, transistors M_a and M_b evaluate the difference between V_{IN+} and V_{OUT} as shown in Figure 5.4. If the voltage of the positive terminal of the input source is larger than V_{OUT}, at least by a threshold voltage, M_b conducts and brings V_{IN+} (neglecting its source-to-drain drop voltage) to the gate of transistor M_c. This transistor then checks if the condition $V_{IN+}>V_{CAP-1}$ is valid. Simultaneous conduction of M_b and M_c provides a path from the bootstrapped capacitor C_{B1} connected to V_{CAP-1}, to the gate of main pass MOS transistor, M_3 (see Figure 5.4). Thus, it eventually leads to a charge transfer from the input source toward the load only when the input voltage is greater than the output voltage, and it blocks the reverse leakage current that could otherwise flow via M_3 in other conditions.

When $V_{IN+}<V_{OUT}$, at least by a threshold voltage, transistor M_a conducts and forces M_3 off. Therefore, no flow-back current, ignoring leakages, could pass through M_3. The dual of this control circuit must be used in the same manner between the other bootstrapped capacitor, C_{B2}, and the gate of the other main pass transistor, M_4, to cancel the flow-back current in negative

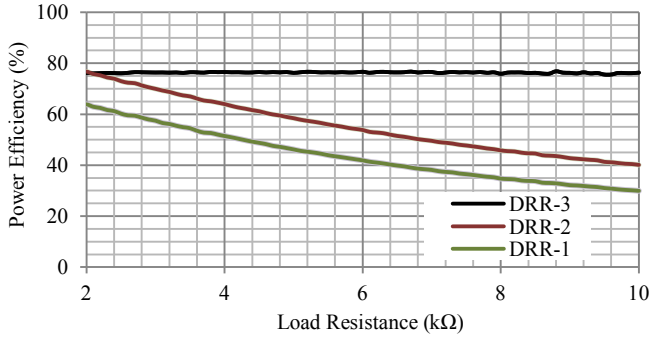


Figure 5.5. Simulated power efficiency versus load resistance for three considered DRR structures.

source cycles. The size of M_b, M_c, and M_a, as reported in Table 5.1, were chosen in order to optimize power efficiency. The efficiency of the proposed technique could be compromised if a reverse leakage current is allowed to flow when the difference between the input rail voltages and the output voltage does not exceed the threshold voltage of either M_a or M_b. This effect could be mitigated if low-threshold transistors are employed. M_c switches are selected from low-threshold transistors.

Figure 5.5 plots the power efficiencies of three DRR circuits in the same chart for different load resistances. It shows that the DRR-3 maintains higher power efficiency over a wide range of output resistance, which is not the case for the other two DRR structures. It also reveals that the proposed rectifier (DRR-3), in which the control scheme for reducing the flow-back current is inserted, has significantly larger power efficiency than the other considered topologies. The improved efficiency is more obvious with larger load resistances. From separate simulations, it was found that the voltage conversion ratio of the DRR-3 circuit also maintains its value over the same load resistance range.

In fact, for a given input peak amplitude and holding capacitor size, as the load resistance is increased, the output voltage variation (ripples) is reduced. Therefore, for larger load resistances, there is more opportunity for flow-back currents to occur. Therefore, the rectifier designed to limit such phenomenon (DRR-3) shows significantly higher power efficiencies, compared to the DRR-1 topology. The DRR-3 rectifier, in agreement with our expectations, maintains a power

efficiency as high as the DRR-2 topology with source peak voltages smaller than 1.0 V.

However, for input peak voltages larger than 1.0 V, compared to a rectifier for which the circuit elements are optimized for the exact source and load parameters, the overall power efficiency is slightly degraded. This is due to an indirect path that is formed between the bootstrapped capacitors and the gate of the main pass switches. Indeed, for different input amplitudes, there are time intervals when source-to-gate voltage of M_c is too small to force it into the conduction region. This makes the applied boot strapping technique less effective, which eventually leads the rectifier to present lower power and voltage efficiencies.

5.3.2 Close-Track Scheme for Flow-Back Current Reduction

In the basic DRR-1 design of Figure 5.1b, the drain and gate of the pMOS charging transistor for boot strapping capacitors, M_7, are tied together to form a diode. This was essential, as explained in [17], to make the boot strapping technique efficient in reducing the effective threshold voltage of the main pass pMOS transistors, M_3. In fact, the DRR-1 circuit works in a way that, except for start up and ignoring the small voltage changes due to leakages, the bootstrapped capacitors, C_{B1}, maintain their induced voltage, $V_{CAP\text{-}1}$. However, the output voltage, V_{OUT}, may vary over time due to change in the input peak voltage or load conditions. This causes the bulk of the charging transistors to leak into the substrate. Indeed the DRR-1 design uses the dynamic bulk switching (DBS) technique to reduce such leakage current. For reference, Figure 5.6a shows the original schematic of the charging path in the DRR structure, where the bulk of the charging transistor is dynamically biased. Although this approach decreases leakages, it increases the risk for flow-back current to occur. This is due to the fact that V_{OUT} and $V_{CAP\text{-}1}$ are not linked together, except for the time intervals when M_7 conduct (startup).

In order to closely link V_{OUT} and $V_{CAP\text{-}1}$, and to limit their voltage differences to the voltage drop of a forward-biased diode, we propose inserting diodes connected with reverse polarity in parallel with the diode-tied charging transistors, M_7. Figure 5.6b shows a basic implementation of a proposed circuit solution called close-track biasing. For positive source cycles, the combination of diode-connected transistor M_7 and the parallel diode D_1 limits the voltage difference between $V_{CAP\text{-}1}$ and V_{OUT} to at most one MOS transistor threshold voltage. This reduces the possibility for

flow-back current to occur. The dual of this circuit must be used in the same manner between the other boot strapped capacitor, C_{B2}, and the output node, to reduce the flow-back current in negative source cycles. The diodes $D_{1/2}$ may be implemented using diode-tied MOS transistors.

In a simplified implementation of close track biasing, we propose to use the existing parasitic diode present between the drain and the bulk of charging transistors, $M_{6\text{-}7}$, to implement the desired parallel back propagating diodes. This reduces the complexity of the circuit, and its die area. Figure 5.6c illustrates the new charging path setup for this DRR structure (called DRR-4).

This new charging path structure is a key component of the rectifier configuration called DRR-4 that produces the best performance among all those proposed or considered as will shown in the rest of this paper. The proposed arrangement is called close-track biasing because it implies $V_{CAP\text{-}1}$ to closely follow V_{OUT} against its variations over time. Here, the diode-connected MOS transistor behaves as a charging element, while the parasitic diode, created between its drain and bulk junctions, operates as a parallel diode to implements the short-track path.

At this stage, based on the knowledge and experience developed so-far, the design of the rectifier based on the DRR-4 configuration is relatively simple as it does not require dynamic bulk biasing and its associated challenges. Figure 5.7 illustrates the impact of the proposed configuration on the power efficiency of the DRR structure, where the circuit elements reported in Table 5.1 are used. It demonstrates that when compared to the DRR-1 and DRR-2 structures, the power efficiency is improved over a wider range of input peak voltages. For instance, comparing DRR-4 and DRR-1 circuits, the increases in power efficiency are 14% and 20% for input peak voltages of 0.8 V and 1 V, respectively. This improvement is mostly explained by the fact that the new rectifier configuration with close track biasing reduces the flow-back current. Thus, the energy efficiency of the bootstrapping technique is not compromised even for short time intervals.

It was also observed that the new proposed configuration does not affect the voltage conversion ratio. The simulations with the same circuit parameters performed to compare DRR-4 and DRR-1 show the remarkably higher VCR of DRR-4. Therefore, using the proposed close-track biasing (DRR-4) to reduce the flow-back current is advantageous from the power and

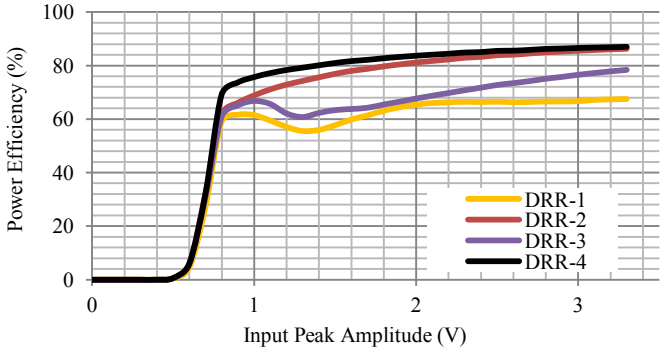


Figure 5.7. Simulated power efficiency for DRR structures with and without the parallel diode.

voltage efficiency standpoints, especially for low-voltage applications where the input peak amplitude is less than 1 V.

5.4 Low-Area Bootstrapped Rectifier

The previously proposed topologies for a full-wave rectifier used two separate large bootstrapped capacitors (C_{B1} and C_{B2}), of 50 pF each, along with large charging diode-connected MOS transistors, $M_{7\text{-}8}$ [17]. This may limit their applicability when silicon area is tight. In order to save silicon area, while benefiting from improved power conversion efficiency, and an

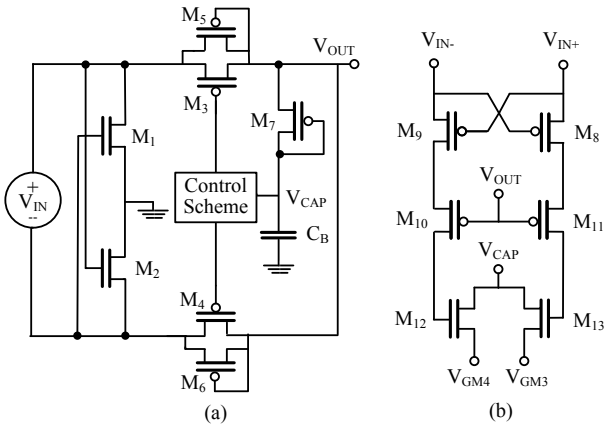


Figure 5.8. Schematic of the proposed single-reservoir topology: a) Rectifier architecture (SRR), b) Control circuit.

increased output voltage for a given input source amplitude, we now propose a new single-reservoir full-wave rectifier (SRR) that exploits bootstrapping techniques. The structure, shown in Figure 5.8a, has a bridge-like configuration augmented by a polarity selective control scheme. The control module consists of circuitry which provides the proper path from the upper plate of the bootstrapped capacitor, C_B, to the gate of the pMOS main pass transistors that is active in each respective conduction cycle, $M_{3\text{-}4}$. With this configuration, a single capacitor, C_B, serves as charge reservoir for reducing the effective threshold voltage of the pass transistors, $M_{3\text{-}4}$, in both positive and negative source cycles. Thus, it leads to significant silicon area savings.

The SRR configuration, as the DRR-1, is formed as a gate cross-coupled configuration for main nMOS pass devices, $M_{1\text{-}2}$, which provide the ground for the dual parts of the circuit in each source cycles. Therefore, it benefits from its associated advantages such as applying to the gates of the selected MOS transistors a voltage swing larger than the one obtained with diode-connected nMOS transistors in the conventional structure. This leads to a higher ON/OFF current ratio.

As will be shown in the sequel, the bootstrapped reservoir, C_B, can be significantly smaller than the total size of the capacitors in the various DRR structures. Indeed, in addition to the obvious gain of replacing 2 capacitors by one, the size of the capacitor can also be reduced further because, during the charge phase, there is only an indirect connection between the reservoir and the gates of the main pass devices, thus charge sharing is reduced. Considering the time constant associated with the charging path of the bootstrapped capacitor (consisting of M_5 or M_6 along with M_7) and to obtain effective threshold reduction, it is necessary to inject enough charges into the bootstrapped capacitor (C_B). Thus, the size of $M_{5\text{-}7}$ must be selected carefully. Nevertheless, due to the smaller bootstrapped capacitor, when compared to the various DRR structures, transistor M_7 could be remarkably smaller than the corresponding device in Figure 5.1b.

5.4.1 Control Circuit

The control circuit is responsible for connecting the bootstrapped capacitor (C_B) to the gate terminal of the given main pass devices ($M_{3\text{-}4}$). It consists of a dual switching circuitry

implemented to act in either positive or negative input cycles. It does not include complex circuit techniques which are commonly power hungry. Figure 5.8b shows the schematic of the control circuit for both input cycles. Ignoring first the impact of MOS threshold voltage for simplicity, M_8 operates during positive cycles ($V_{In+}>V_{In-}$) while M_{11} checks for valid load charging condition ($V_{In}>V_{Out}$). If both conditions are true, M_{13} (connecting the gate of M_3, V_{GM3}, to V_{CAP} in Figure 5.8a) provides the path from the bootstrapped capacitor to the gate of the main pass transistor, M_3. This path can be biased in a way that compensates for the voltage drop that M_3 threshold could induce. Recall that M_3 regulates the current from the input source to the load in positive cycles, but that it could also adversely contribute to reverse current and leakage if not controlled properly.

Wirelessly powered applications may have to operate from distorted RF signals. This may be due to rapid changes in distance and/or orientation of the wirelessly powered device with respect to the source. In such cases, the rectifier should be capable of handling asymmetrical input cycles in an efficient way. The symmetry in the proposed circuit ensures that it can handle distortion of the input signal. Thus, the proposed rectifier maintains its high power efficiency if positive and negative peak amplitudes are different. A detailed analysis of the impact of asymmetrical input cycles and of further circuit simplifications are beyond the scope of this paper and will be presented elsewhere.

This circuit should be optimized by adjusting the size of the transistors to operate at different source frequencies. This is necessary to attain adequate time constants for the charging paths of the bootstrapped capacitor. In the proposed configuration, M_8 and M_{11} are minimum size transistors to reduce loading and to allow switching faster. Transistor M_{13} must be fairly large in order to drive the gate of the wide main pass transistor (M_3) properly. Note that the maximum voltages are applied on the gates of these transistors to reduce R_{ON}, resulting in smaller power dissipation and voltage drop.

The dual part of the control scheme acts in the same manner for negative input cycles. Here, transistors M_9 and M_{10} are activated by the same mechanism as described for M_8 and M_{11} in source positive cycles. It leads M_{12} to conduct and connect the bootstrapped capacitor (C_B) to the gate of the other main pass device (M_4). Depending on the process capabilities, M_{12} and M_{13} are

implemented with low-threshold transistors to improve the performance of the circuit. An advantage of the new design is its compatibility with standard CMOS processes, where implementing integrated capacitors is often feasible.

The bulk of the charging transistor, M_7 is connected to V_{OUT} to benefit from the advantages of the close-track biasing method (first uncovered with DRR-4), in order to reduce the flow-back current from the load to the source.

It was observed, as in the DRR structure, that dynamic biasing of the bulk terminals of the main pass transistors ($M_{3\text{-}4}$) may significantly reduce the overall power efficiency. Indeed, the transistors employed in DBS circuits remain off when the voltage difference between their source and gate is too low to allow conduction. Therefore, the bulk of the main pass transistors ($M_{3\text{-}4}$), as well as the auxiliary path transistors ($M_{5\text{-}6}$) were connected to V_{OUT} because it is the highest voltage available during most of the rectifier operating period due to the presence of an output charge reservoir.

Various schematics-based simulations demonstrate that the new rectifier topology can operate over a wide range of operating frequencies up to 50 MHz. Figure 5.9 plots the power and voltage conversion efficiencies in relation to the input source frequency. As listed in Table 5.1, the same source amplitude and load (3.3 V peak, R_L= 2 kΩ, C_L= 200 pF) were used. Here, the rectifier was optimized such that it presents the maximum power and voltage conversion efficiencies at a 10 MHz operating frequency. Larger bandwidth may be obtained if adequate optimizations are performed.

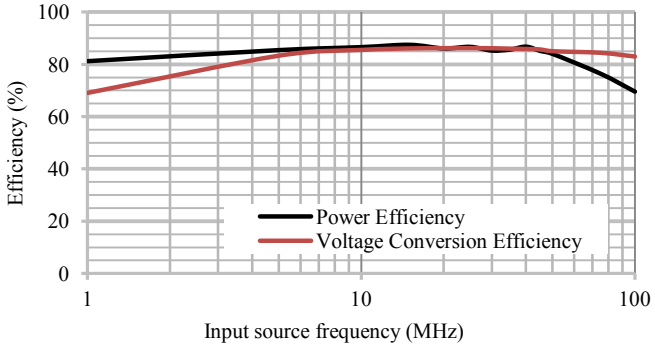


Figure 5.9. Performance of the proposed rectifier over different input source frequencies.

An important design concern is the size of the boot strapped capacitor (C_B). Integrated capacitors consume considerable die area when implemented using standard CMOS processes. Figure 5.10 shows how power efficiency and voltage conversion ratio vary with boot strapped capacitor size. It shows that, over a specific range of capacitance, the design performance in terms of PCE and VCR does not depend strongly on the size of the embedded capacitors. The decrease in PCE and VCR for very small bootstrapped capacitors can be explained by the impact of leakage within the capacitor itself as well as the one associated with the transistor parasitics in the control circuit. From Figure 5.10, the SRR offers an efficiency close to its maximal value with a 4 pF capacitor when integrated with a standard CMOS process.

We have compared the simulation results of SRR and DRR-4. While having comparable

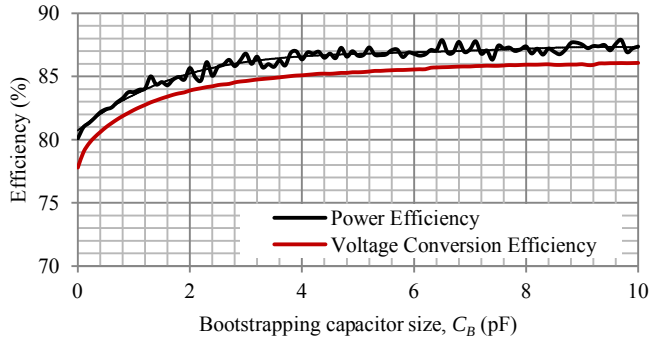


Figure 5.10. Simulated power efficiency and voltage conversion ratio versus bootstrapped capacitor size.

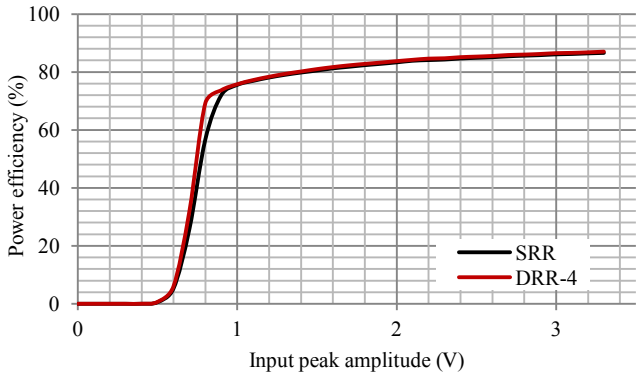


Figure 5.11. Simulated power conversion efficiency versus input peak amplitude for double- and single-reservoir rectifier structures.

power efficiencies, the bootstrapped capacitors are 50 pF each in DRR-4 and 6 pF in SRR. Figure 5.11 shows the power conversion efficiency variation versus input amplitude for these different structures with their elements configured as listed in Table 5.1. With a source voltage higher than 0.90 V, the new rectifier presents power efficiencies as high as that offered by the DRR-4 topology. . In fact, due to the indirect path from the bootstrapped capacitor to the gate of the main pass transistors, charge sharing between the bootstrapped capacitor and the parasitics associated with the gate of very large main pass transistors occurs for only a fraction of the input source period, when M_{11}/M_{12} is ON. The use of a smaller bootstrapped capacitor also implies shorter settling time for charging close to the peak voltage. This results in a more effective threshold compensation.

The proposed SRR was laid out and fabricated using a 0.18 µm 6-Metal/2-Poly TSMC 3.3 V standard CMOS process. It measures 180x600 µm^2. Figure 5.12 depicts the die photomicrographs of the chips comprising these structures. Here, the areas labeled A, B, and F indicate the bootstrapped capacitors ($C_{B1\text{-}2}$ and C_B), C, D, G, and H indicate the main pass transistors ($M_{1\text{-}4}$), E and K indicate the bootstrapping transistors ($M_{5\text{-}8}$) and control circuitry.

Comparing the silicon area consumed by SRR and a previously fabricated DRR-1 circuit (530x670 µm^2) embedding transistors of comparable sizes shows a saving of almost 70% in die area.

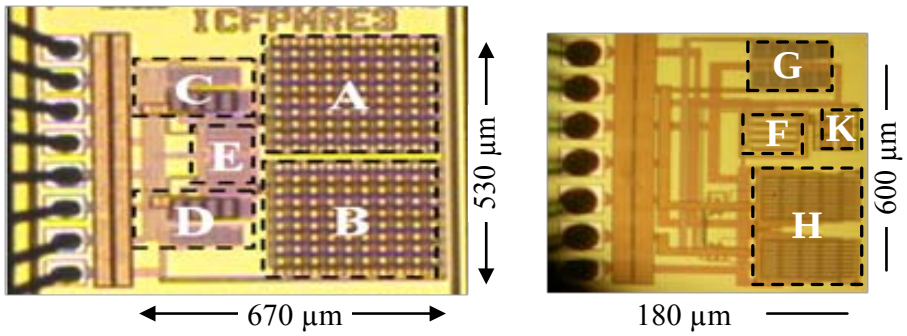


Figure 5.12. Photomicrograph of chips for different rectifier structures: a) double-reservoir, b) single-reservoir.

The measurement setup and protocol explained in [17] was used to measure the input and output voltages and power in order to calculate the voltage and power efficiencies. The simulations were conducted on schematics and layout views of the new design to verify the consistency of the results for the new rectifiers. Based on the waveforms obtained from measurements of SRR, an average output voltage of 2.79 V is obtained. This measured voltage represents a VCR of 85% at the given frequency.

Figure 5.13 plots the measured and the post-layout simulated VCRs of the SRR for the uniformly assumed load condition with a 10 MHz source frequency. At 1.0 V, 1.8 V, and 2.8 V input peak amplitudes, measured voltage conversion ratios of 82%, 79%, and 78% are obtained.

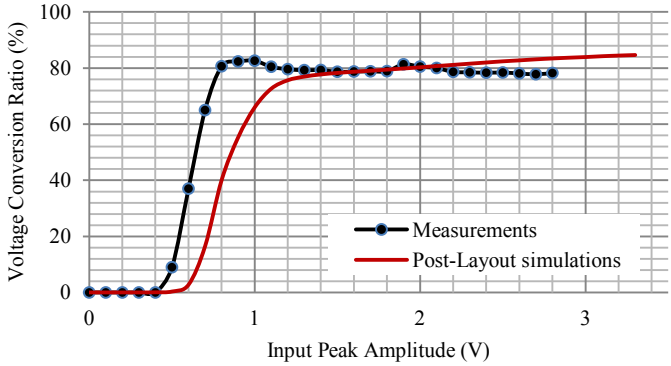


Figure 5.13. Measured voltage conversion ratio of the proposed SRR as a function of input peak amplitude when operating at f=10 MHz.

The plot also shows that the proposed rectifier maintains its high voltage conversion ratio for the wide range of input peak amplitude supported by the CMOS process used.

Some parasitics influence the experimental measurements. For instance, there are parasitics associated with the gate of the large native nMOS transistors ($M_{11\text{-}12}$), the large interconnection metal strips, and the significant parasitic capacitances associated with the output pads and oscilloscope probes. From the measurements, it seems that these parasitics have acted in a way that improves the VCR of the SRR as compared to post-layout simulations, for different source peak amplitudes. Note that the SRR topology uses a relatively small bootstrapped capacitor, compared to the DRR structure. Therefore, such parasitics tend to play a more significant role in the performance of SRR compared to DRR structure.

It was noted that the measured VCR slightly degrades under high input peak amplitudes (more than 1V), while the one predicted with post-layout simulations keeps increasing. We also observed from the measurements that the phenomenon is not destructive and performance is very repeatable over a long test period. Noting that the rectifier is laid-out using 3.3 V design rules, no simple explanation of this observation could be derived. Considering the floating nature of the source signal and establishing the reference ground with respect to the output of the rectifier, some parasitic paths may be activated when the source voltage increases. As part of our investigations in relation with those observations, we considered parasitics associated with the measuring probes and setup transformers, along with series resistive paths made by bonding wires. We measured the current flowing through the global substrate to the ground and observed some significant currents. We could not localize the junctions causing such leakage as our circuit is not sufficiently instrumented for such debugging purposes. As this phenomenon is not dominant and does not preclude effective used of the SRR, we left this issue for future research.

Figure 5.14 depicts the measured power efficiency versus input peak amplitude for the proposed SRR rectifier with the same load conditions, as previously cited, at a source frequency of 10 MHz. The overall power efficiency is measured to be 76%, 77%, and 70% at 0.8 V, 1.8 V, and 2.8 V peak input source amplitude. The results were found to be in good agreement with the simulations in the desired input peak range up to 2 V. The slight difference between the

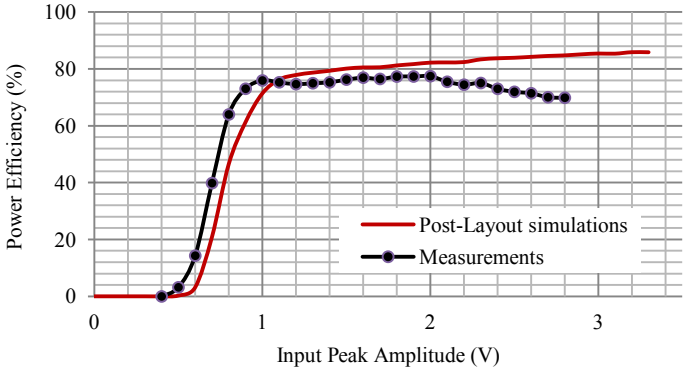


Figure 5.14. Measured power conversion efficiency of the SRR full-wave rectifier versus input peak amplitude operating at f=10 MHz.

measurements and the post-layout simulation can be explained by the power dissipated within the large interconnection metal strips, and the parasitics associated with the measurement probes and large pads. These are not very well modeled within the simulation environment. Thus, one may expect more consistent measurements by using probe connections on die instead of the pads.

From the measurement, for the design laid-out based on 3.3 V design rules, under peak amplitudes larger than 2.0 V, the PCE is degraded somewhat similarly to the VCR. The excessive leakage current flowing under such conditions eventually results in a larger power dissipation within the rectifier. Based on separate measurements, it was also observed that the power efficiency decreases with load current and our best hypothesis is again that some leakage paths that we could not isolate get activated.

Table 5.2 presents the comparison between the measured characteristics obtained from the proposed rectifier and the most advanced full-wave rectifiers, described in the literature. The last three designs use boot strapping techniques. Note that they are quoted for different load conditions, and processes.

Unfortunately, the existing differences in terms of process and feature size make it difficult to compare reported characteristics of state-of-the-art rectifiers. However, for the source amplitude range reported in Table 5.1, the comparison results confirm that the proposed rectifier topology generates the best output voltage and power efficiency compared to other reported results,

Table 5.2. Comparison with most advanced rectifier characteristics

Rectifier Topology	Process	Source Amplitude (V)	Output Voltage (V)	Power Efficiency (%)
V_{TH} Reduction [12]	CMOS 0.25 µm	2.5	1.45	65
Self V_{TH} Cancelation (SVC) [24]	CMOS 0.18 µm	1.8	-	32
Differential-Drive SVC [23]	CMOS 0.18 µm	1.8	-	67
Previous work [17]	CMOS 0.18 µm	1.8	1.20	71
This work (SRR)	CMOS 0.18 µm	1.8	1.42	77

particularly when operating from a low source voltage.

The proposed rectifier is capable of handling significant load currents. This is not the case for some other topologies, for which the load handling capability depends on the size of the capacitors. The design reported in [21] uses large off-chip capacitors in the micro-Farad range, which is against our objective for implementing integrated rectifiers. The proposed design also uses a standard CMOS process with significantly longer feature size in fabricating the rectifier.

Measurements reported in [24] also confirm that the rectifier proposed in that reference is not a good candidate for implementing rectifiers with high voltage and power efficiencies when using a low source voltage.

The SRR proposed in this paper presents significantly larger power and voltage conversion efficiencies compared to all double-reservoir structures. For instance, at 1.8 V input peak amplitude, the SRR achieves 8% and 18% increased in PCE and VCR while it save almost 70% of the die area, compared to DRR-1 topology.

5.5 Conclusions

Improvements applicable to a double-reservoir integrated full-wave rectifier were presented. They significantly improve its performance in terms of power and voltage conversion efficiencies by reducing the flow-back current while removing the need for auxiliary paths. The improved rectifier (DRR-4) presents 14% and 20% respective increases in power efficiency for input peak voltage of 0.8 V and 1 V when compared to basic double-reservoir rectifier (DRR-1) structure. A single-reservoir (SRR) full-wave integrated rectifier was also introduced. It employs MOS-based gate cross-coupled nMOS switches, along with pMOS switches controlled to have reduced effective threshold, thus reducing the forward voltage drops in AC to DC conversion. This results in very low voltage drop across the MOS switches and high power efficiency. An improved control scheme driving the main pass transistors with the highest voltages available in the circuit is used to connect a single bootstrapped capacitor to the main pass switches. This reservoir holds enough charges to reduce the effective threshold voltage of the selected MOS switches in both positive and negative input source cycles. The SRR rectifier uses low-threshold transistors. It achieves a 70% savings in silicon area compared to a previously reported double-reservoir structures. Experimental measurements were found to be in good agreement with post-layout simulations results. For a source peak amplitude of 1.8V, the proposed rectifier presents 8% and 18% increase in power and voltage conversion efficiencies, compared to previously reported double-reservoir topology (DRR-1). The measurements show that the new rectifier presents significantly higher performance when the AC source amplitudes has less than 1 V peak.

5.6 References

[1] C. Alippi, and C. Galperti, "An Adapative System for Optimal Solar Energy Harvesting in Wireless Sensor Network Nodes," IEEE Trans. Circuits and Systems-I: Regualr Papers, vol. 55, no. 6, pp. 1742-1750, July 2008.

[2] P.-Y. Chen, et al., "A Low-Cost VLSI Architecure for Fault-Tolerant Fusion Center in Wireless Sensor Networks," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 4, pp. 803-813, Apr. 2010.

[3] A.D. DeHennis, and K.D. Wise, "A wireless microsystem for the remote sensing of pressure, temprature, and relative humidity," IEEE J. Microelectromechanical Systems, vol. 14, no. 1, pp. 12-22, Feb. 2005.

[4] V. Pillai, et al., "An Ultra-Low-Power Long Range Battery/Passive RFID Tag for UHF and Microwave Bands With a Current Consumtion of 700 nA at 1.5 V," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 54, no. 7, pp. 1500-1512, July 2007.

[5] G.K. Balachandran, and R.E. Barnett, "A Passive UHF RFID Demodulator With RF Overvoltage Protection and Sutomatic Weighted Threshold Adjustment," IEEE. Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 9. Pp. 2291-2300, Sep. 2010.

[6] Y. Hu, and M. Sawan, "A Fully Integrated Low-Power BPSK Demodulator for Implantable Medical Devices," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 52, no. 12, pp. 2552-2562, Dec. 2005.

[7] B. Gosselin, et al., "A mixed-signal multichip neural recording Interface with bandwidth reduction," IEEE Trans. Biomedical Circuits and Systems, vol. 3, no. 3, pp. 129-141, June 2009.

[8] N. Soltani, and F. Yuan, "A High-Gain Power-Matching Technique for Efficient Radio-Frequency Power Harvest of Passive Wireless Microsystems," IEEE. Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 10, pp. 2685-2695, Oct. 2010.

[9] A. Dolgov, R. Zane, and Z. Popovic, "Power Management System for Online Low Power RF Energy Harvesting Optimization," IEEE. Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 7, pp. 1802-1811, July 2010.

[10] G. Wang, et al., "Design and Analysis of an Adapative Transcutaneous Power Telemetry for Biomedical Implants," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 52, no. 10, pp. 2109-2117, Oct. 2005.

[11] K. Finkenzeller, RFID-Hnadbook. John Wiley and Sons Ltd., 2003.

[12] E. Lee, et al., "A Biomedical Implantalbe FES Battery-Powered Micro-Stimulator," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 56, no. 12, pp. 2583-2593, Dec. 2009.

[13] Ch. Sauer, et al., "Power Harvesting and Telemetry in CMOS for Implanted Devices," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 52, No. 12, pp. 2605-2613, Dec. 2005.

[14] M. Ghovanloo and K. Najafi, "Fully integrated wideband high-current rectifiers for inductively powered devices," IEEE J. Solid-State Circuits, vol. 39, no. 11, pp. 1976 – 1984, Nov. 2004.

[15] S. Hashemi, M. Sawan, and Y. Savaria, "A novel fully-integrated dropless voltage cmos rectifier for wirelessly powered devices," Proc. Int'l Conf. on Microelectronics (ICM'2007), pp. 333–336, Egypt, Dec. 2007.

[16] S. Hashemi, M. Sawan, and Y. Savaria, "Fully-Integrated Low-Voltage High-Efficiency CMOS Rectifier for Wirelessly Powered Devices," IEEE Joint Conference NEWCAS-TAISA'09, France, Jul. 2009.

[17] S. Hashemi, M. Sawan, and Y. Savaria, "A High-Efficiency Low-Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices," Paper to appear, TBioCAS.

[18] T. Umeda, et al., "A 950-mhz rectifier circuit for sensor network tags with 10-m distance," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 35–41, Jan. 2006.

[19] T. Lehmann and M. Cassia, "1-v power supply cmos cascode amplifier," IEEE J. Solid-State Circuits, vol. 36, no. 7, pp. 1082–1086, Jul. 2001.

[20] C. Peters, et al., "Experimental Results on Power Efficient single-Poly Floating Gate Rectifier," IEEE Int'l Symp. Circuits and Systems (ISCAS), Taiwan, 2009.

[21] T. Le, J. Han, A. von Jouanne, K. Mayaram, and T. Fiez, "Piezoelectric micro-power generation interface circuits," IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1411–1420, June 2006.

[22] Bawa G., and Ghovanloo M., "Active High Power Conversion Efficiency Rectifier With Built-In Dual-Mode Back Telemetry in Standard CMOS Technolody," IEEE J. Biomedical Circuits and Systems, vol. 2, no. 3, pp. 184-192, Sep. 2008.

[23] J. C oulombe, e t a l., “ A H ighly Flexible S ystem f or M icrostimulation o f th e V isual Cortex: Design and Implementation,” IEEE Trans. Biomedical Circuits and Systems, vol. 1, no. 4, pp. 258-269, Dec. 2007.

[23] K. Kotani and T. Ito, “High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation t echniques,” IEEE 8 th Conf. A SIC (ASICON’09), pp. 20 -23, C hina, O ct. 2009.

Chapter 6 : **GENERAL DISCUSSION**

Conventional bridge and gate cross-coupled rectifier topologies are not sufficiently power efficient, particularly when input amplitudes are low. Depending on their rectifying element, their power efficiency is constrained by either the forward-bias voltage drop of a diode or the threshold voltage of a diode-connected MOS transistor. This negative impact becomes increasingly significant in the design of low-voltage power supplies, which is the case for new sub-micron CMOS technologies.

Furthermore, transistors implemented with CMOS processes commonly share a global substrate. Depending on the biasing of the bulk terminals, there exist time intervals in which a significant amount of leakage current may flow from the bulk of pMOS transistors into the substrate. This leakage current through the main pass MOS transistors which carry high load currents may drastically affect the overall power efficiency of a rectifier and potentially trigger a latch-up condition. For rectifier circuits where input and output voltages vary significantly over time, this scenario is very likely.

Advanced passive rectifiers use circuit techniques to effectively reduce the threshold voltage of MOS diodes. For this purpose, they apply threshold cancellation methods which benefit from a DC voltage generated in an idle phase to reduce the effect of V_{Th} of MOS transistors in the active phase. Applying the floating gate technique is also reported as a means to program the threshold voltage of the given MOS transistor during setup and erase phases. However, this technique requires high-voltages, and subjects the design to long term reliability problems. Another technique uses bootstrapped capacitors to reduce the effective threshold voltage of a diode-connected MOS transistor to the difference between two threshold voltages. Among currently known techniques, this is the best suited with advanced standard CMOS processes, where implementing integrated capacitors is feasible.

Active rectifiers use active circuits to control the conduction angle of low-loss MOS switches. These rectifier configurations have been reported to have higher power efficiency compared to their passive counterparts. They offer faster switching between the ON and OFF states and allow reducing leakages. However, they generally require an independent power source to operate and the associated extra circuitry adds to design complexity and power consumption. These

drawbacks typically outweigh the benefits they offer and limit their application to systems where an auxiliary power source is present.

6.1 Active Rectifier

An active rectifier with a gate cross-coupled topology is proposed in chapter 3, which replaces the diode-connected MOS transistors of a conventional rectifier with low-loss MOS switches. The proposed rectifier structure uses the inherent characteristics of MOS transistors as comparators to replace the explicit comparators, dynamic bulk biasing of main pass switches to reduce leakage currents, and pull-up transistors to avoid floating gates. Results obtained from simulations and measurements reveal that the proposed rectifier exhibits significantly higher power and voltage conversion efficiencies compared to conventional full-wave diode rectifier (FWDR) and gate cross-coupled rectifier (GCCR) structures for a wide range of operating frequencies in the MHz range. Moreover, contrary to the previous designs, the new rectifier does neither require an internal power source nor an auxiliary signal path for power delivery at startup. Delivery of high load currents is another feature of the proposed rectifier. With a source amplitude of 3.3 V, when compared to the gate cross-coupled topology, the proposed active rectifier offers power and voltage conversion efficiencies improved by up to 10% and 16% respectively.

6.2 Bootstrap Passive Rectifiers

6.2.1 Double-Reservoir Bootstrapped Rectifier

A new passive rectifier configuration for wirelessly powered devices is also presented in chapter 4. It uses two bootstrapped capacitors to effectively reduce the threshold voltage of main pass switched when they are conducting. Double-reservoir bootstrapped rectifier combines the gate cross-coupled configuration with the bootstrapped technique to build a new rectifier architecture that has a voltage drop smaller than the other configurations and that is capable of handling large load currents. The rectifier uses dual structure for positive and negative source cycles. The dual structure consists of auxiliary and capacitor charging paths along with dynamic

bulk biasing of charging diode-connected MOS transistors. The bulk of charging diode-connected MOS transistors are dynamically biased to reduce the leakage current from their bulks to the global substrate. It achieves a significant increase in its overall power efficiency and low voltage-drop compared to conventional rectifier passive topologies. Therefore, the rectifier is good for applications with low-voltage power supplies and large load current.

When connected to a sinusoidal source of 3.3 V peak amplitude, it allows improving the overall power efficiency by 11% compared to the best recently published results given by a gate cross-coupled-based structure. In addition, the proposed rectifier presents an average output voltage up to 210% higher than the best previously reported circuits when the peak amplitude of the sine source drops down to 0.8 V AC. Yet, there exists time intervals when the leakage reverse current may flow from output towards the source degrading the overall power efficiency.

6.2.2 Improvements in Double-Reservoir Bootstrapped Rectifier

Improvements applicable to a double-reservoir integrated full-wave rectifier were presented in chapter 5. They significantly improved the performance of the rectifier in terms of power and voltage conversion efficiencies.

6.2.2.1 Short-Auxiliary Paths

Within the original DRR structure, there are circuit branches that allow charging the holding capacitors and they are essential when there is no other means of harvesting power within the design, especially at startup. Moreover, there are transistors which their source terminals are connected to varying voltages providing adequate biasing for the bulk of the exposed transistors is essential as these transistors may inject (leakage) current into the substrate and induce latch-up. An improvement to original DRR structure, so-called short auxiliary path, is proposed which employs the parasitic diode formed at the junction of a diffusion island and the bulk of the main pass switches. It acts as an auxiliary path, providing proper bias to the main switches.

6.2.2.2 Flow-back Free Scheme

Another improvement in the DRR circuit consists of introducing circuit techniques to reduce the reverse leakage current from load to source during time intervals when the input voltage gets smaller than the voltage on the output node. This leakage current may significantly degrade the performance of the rectifier from a power efficiency standpoint. Different solutions to this problem were suggested in chapter 5. It includes control scheme and close-track schemes. The control scheme, eventually leads to a charge transfer from the input source toward the load only when the input voltage is greater than the output voltage, and it blocks the reverse leakage current that could otherwise flow via main pass transistors in other conditions. However, for input peak voltages larger than 1.0 V, compared to a rectifier for which the circuit elements are optimized for the exact source and load parameters, the overall power efficiency is slightly degraded.

In order to closely link the voltages on output node and bootstrapped capacitor, and to limit their voltage differences, we proposed the close-track scheme where diodes connected with reverse polarity are inserted in parallel with the diode-tied charging transistors. In a simplified implementation of close track biasing, the existing parasitic diode presented between the drain and the bulk of charging transistors was used to implement the desired parallel back propagating diodes. This reduced the complexity of the circuit, and its die area. The improved rectifier (DRR-4) presents 14% and 20% respective increases in power efficiency for input peak voltage of 0.8 V and 1 V when compared to basic double-reservoir rectifier structure.

6.3 Single-Reservoir Bootstrapped Rectifier

The need for two separate large bootstrapped capacitors of 50 pF each, along with large charging diode-connected MOS transistors in DRR structures may limit their applicability when silicon area is tight. A single-reservoir rectifier was also introduced in chapter 5, in which a single boot strapping circuit serves for the two consecutive input cycles induced by polarity reversal of the AC source. In this architecture, a smart polarity selective control scheme is developed such that it connects the bootstrapping capacitor to the gate of the relevant main pass transistor in either of input cycles. Indeed, in addition to the obvious gain of replacing two

capacitors by one, the size of the capacitor can also be reduced further. The symmetry in the proposed circuit ensures that it can handle distortion of the input signal. Thus, the proposed rectifier maintains its high power efficiency if positive and negative peak amplitudes are different.

For a source peak amplitude of 1.8V, the proposed rectifier presents 8% and 18% increase in power and voltage conversion efficiencies, compared to previously reported double-reservoir topology (DRR-1). The measurements show that the new rectifier presents significantly higher performance when the AC source amplitudes has less than 1 V peak. The proposed single reservoir rectifier also requires almost 70% less die area. From the measurements, it was noted that the measured VCR slightly degrades under high input peak amplitudes (more than 1 V), while the one predicted with post-layout simulations keeps increasing.

6.4 Test and measurement setup

All of the proposed rectifiers were fabricated in a 0.18 μm 6-Metal/2-Poly TSMC 3.3 V standard CMOS process. Special test setups were also developed to realize floating sources and accomplish precise measurements. From measurements, which are in close agreement with simulation results, the proposed rectifiers offer remarkably higher output voltages and power efficiencies, compared to conventional bridge and gate cross-coupled structures, when used in low-voltage and high-current applications. All of the prototypes were designed to deliver a load current larger than 2 mA when operating in ISM band up to 50 MHz. Some derivations in the results obtained from the simulations and measurements were reported and the parasitics associated with the proposed circuit elements, the test setup and the ESD circuits are considered as main reason for such discrepancies.

Chapter 7 **CONCLUSIONS AND RECOMMENDATIONS**

7.1 Contributions of This Research

A new full-wave integrated active rectifier, and passive rectifiers based on bootstrapping capacitor technique were proposed in this thesis. The proposed active rectifier with a gate cross-coupled topology uses low-loss MOS switches in place of diode-connected MOS transistors of conventional rectifiers. Using the inherent characteristics of MOS transistors as comparators in place of an explicit comparator is another advantage of the proposed circuit. Leakage through the substrate of the main switches is also minimized by dynamically biasing their bulks with the highest available voltage. Small low leakage pull-up transistors are also used to help prevent floating gates during inactive periods. Use of these transistors along with the highest available voltages in the circuit to control them results in reduced channel resistance, increased transconductance, and faster switching.

Owing to these techniques, the proposed active rectifier exhibits smaller voltage drop across the main switches leading to higher power efficiency compared to conventional rectifier structures for a wide range of operating frequencies in the MHz range. Moreover, contrary to previous designs, the new rectifier does neither require an internal power source nor an auxiliary signal path for power delivery at startup. Delivery of high load currents is another feature of the proposed rectifier.

Using the bootstrapping technique, different versions of high-efficiency integrated full-wave rectifiers with gate cross-coupled topology are proposed. Using this technique, the effective threshold voltage of main pass MOS switches are reduced to the difference of two threshold voltages, making the proposed rectifiers suitable for low-voltage operation. Implementation of the proposed rectifiers is also feasible with standard CMOS processes.

The double-reservoir rectifier uses two bootstrapping circuits attached to main pass MOS switches; each threshold reduction circuit active for one input cycle. Auxiliary paths consisted of diode-connected MOS transistors are also inserted to activate the bootstrapping technique at

startup. Dynamic Bulk Switching (DBS) technique is applied to the bulk of diode-connected charging transistors while the bulk of main pass switches is connected to the output voltage.

A single-reservoir rectifier is also proposed in which a single bootstrapping circuit serves for both of input cycles. In this architecture, a smart polarity selective control scheme is developed such that it connects the bootstrapping capacitor to the gate of the relevant main pass transistor in either of input cycles. Due to the indirect path from bootstrapping capacitor to the gate of main switches, the capacitor size is remarkably smaller than the double-reservoir structure leading to smaller charging transistors. The proposed rectifier presents a performance as high as a double-reservoir structure in terms of power efficiency and voltage conversion ratio while saving almost 70% of die area.

Different bulk biasing for the main and charging transistors are also suggested. Short auxiliary paths uses parasitic diffusion-bulk junction of the main pass switches in place of diode-connected pMOS transistors in the auxiliary paths.

During normal operation of a bootstrapping capacitor-based rectifier, time intervals exist, in which the current flow in the main pass pMOS transistors reverses. For a rectifier used in variable source and load conditions, this flow-back current may significantly degrade the performance of the circuit from a power efficiency stand point. To solve this problem, a flow-back current free scheme is proposed, in which a smart control circuit selectively regulates the conduction angle of main pass transistors and prevents reverse current. A close-track scheme using the parasitic diffusion-bulk junction diode of the charging transistor is also introduced. In this scheme, the voltage on bootstrapping capacitor closely tracks the output voltage, and limits the difference between these voltages to the voltage drop of a forward-biased diode. The resulting configuration has a relatively simple structure and produces the best performance among all double-reservoir structures for a wide range of input peak voltages.

All the proposed rectifiers were simulated using the SpectreS simulator in Cadence environment and fabricated with a 0.18 μm 6-Metal/2-Poly TSMC 3.3 V standard CMOS process. Special test setups, including isolating and wideband RF transformers with small insertion and return losses were developed to realize floating sources. Precise measurements on

input and output voltages and currents were carried out to calculate the power efficiency.

From measurements, which are in close agreement with simulation results, the proposed rectifiers offer remarkably higher output voltages, and power efficiencies compared to conventional bridge and gate cross-coupled structures when used in low-voltage and high-current applications.

With a source amplitude of 3.3 V, when compared to the gate cross-coupled topology, the proposed active rectifier offers power and voltage conversion efficiencies improved by up to 10% and 16% respectively. The proposed rectifier using the bootstrap technique, including double- and single-reservoir schemes, are well suited for very low input amplitudes. They present power and voltage conversion efficiencies of 75% and 76% at input amplitude of 1.0 V and maintain their high efficiencies over input amplitudes greater than 1.0V. Single-reservoir bootstrap rectifier also reduces die area by 70% compared to its double-reservoir counterpart. All of the proposed rectifiers are implemented using CMOS 0.18 µm technology and our prototypes were designed to deliver a load current larger than 2 mA when operating in ISM band up to 50 MHz.

7.2 Directions/Recommendations for Future Work

In this section, we address several open avenues for future work along with recommendations based on our experience and findings throughout this study.

7.2.1 Single-Reservoir Bootstrapped Rectifier with Asymmetrical Input Cycles

The proposed single-reservoir bootstrap rectifier uses a close-track scheme with independent controls for positive and negative input cycles. This dual control structure ensures that the rectifier can handle distortion of the input signal in order to maintain its high power efficiency if positive and negative peak amplitudes are different. However, one may imagine other situations in which the input source amplitude is not significantly distorted. An example of an undistorted input signal is in the inductively powered biomedical implants, where the distance and orientation of the transmitter and the receiver are almost fixed and/or an implant drives an almost constant

load. A detailed analysis of the impact of such symmetrical input cycles and of further circuit simplifications may be of interest.

7.2.2 Circuit Reliability Test

An interesting continuation of this work is to test the reliability of the proposed bootstrapped rectifiers. While the principle of operation is sound, a thorough verification would further prove the concept viable. The experimental prototype was tested with input amplitudes up to 5V with no device degradation or failure in the short term. While the prototype survived many attempts of input voltages higher than the allowable 4.6V limit in the 3.3V thick oxide devices, evaluation of long term reliability of circuits was beyond the scope of this research. This study could be carried out with a reliability simulator of the bootstrap circuit, such as the Berkeley Reliability Tool, and with the actual accelerated stressing of a statistically large population of test devices. For applications where a high input amplitude is possible, a protection circuitry is required to limit the overstress to rectifier transistors.

7.2.3 Input Matching Network Analysis

The impact of input matching networks was previously analyzed for the power harvesters with large output capacitance and charge pump based rectifiers with high input capacitance. It was shown that proper matching at the interface of generators and rectifier may result in significant power efficiency improvement. Contrary to previous applications, the input impedance of bootstrapped rectifiers is not significantly capacitive. This fact, when considered along with the diversity of rectifier applications, may encourage further investigations. It is then of high interest to study the impact of an embedded input matching network on the performance of bootstrapped rectifiers.

7.2.4 Modified Passive-Active Rectifier

In a passive-active structure, the first stage of the rectifier is a completely passive block used to convert the negative half waves of the input AC signal into positive ones, with the voltage drop equal to the drain-to-source voltage drop of MOS switches. Use of operational amplifiers in place

of comparators was also reported to be beneficial. Considering these points, one may realize a new active polarity converter stage, implemented using active diodes in place of cross-coupled MOS switches. The active diodes would consist of MOS switches controlled by an operational amplifier with differential outputs. The presence of the OPAMP and the higher voltage at the MOS gates will reduce the voltage drop across the switches and makes the switching faster. It also reduces the chance for short-circuit current flow between the supplies, due to simultaneous conductions of cascode transistors. This undesired current may not be negligible when the input amplitude is about the threshold voltage of the switches.

7.2.5 Active Rectifier with Low Effective Switching Frequency

Active rectifiers are generally more power efficient than their counterpart, the passive rectifiers. However, their application is mainly limited to low and medium operating frequencies. This is because the power efficiency of an active rectifier is mainly constrained by its switching losses. These losses have quadratic dependence on the operating frequency. Therefore, lowering the effective switching frequency for the comparators may result in significant power savings. This could be done by using some learning from source and load conditions over time in specific periods of rectifier operation.

BIBLIOGRAPHIE

[1] Adriaensen S., Flandre D., and Dessard V., "Ultra-Low Power Basic Blocks and Their Uses," Patent EP1217662, 2002.

[2] Ahmadi M.M., and Jullien G., "A Full CMOS Voltage Regulating Circuit for Bioimplantable Applications," Midwest Symp. Circuits and Systems, vol. 2, pp. 988-991, USA, 2005.

[3] Akin T., Najafi K., and Bradley R.M., "A Wireless Implantable Multichannel Digital Neural Recording System for a Micromachined Sieve Electrode," IEEE J. Solid-State Circuits, vol. 33, no. 1, pp. 109-118, Jan. 1998.

[4] Alippi C., and Galperti C., "An Adapative System for Optimal Solar Energy Harvesting in Wireless Sensor Network Nodes," IEEE Trans. Circuits and Systems-I: Regualr Papers, vol. 55, no. 6, pp. 1742-1750, July 2008.

[5] Allstot D.J., "A Precision Variable Supply CMOS Comparator," IEEE J. Solid-State Circuits, vol. 17, no. 6, pp. 1080-1087, Dec. 1982.

[6] Arabi K., and Sawan M., "Electronic Design of a Multi-Channel Programmable Implant for neuromuscular Electrical Stimulation," IEEE Trans. Rehabilitation Engineering, vol. 7, no.2, pp. 204-214, June 1999.

[7] Ashry A., and Sharaf K., "Ultra Low Power UHF RFID Tag in 0.13 µm CMOS," Int'l Conf. Microelectronics (ICM), pp. 283-286, Egypt, 2007.

[8] Atluri S., and Ghovanloo M., "Incorporating Back Telemetry in a Full-Wave CMOS Rectifier for RFID and Biomedical Applications," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 801-804, USA, 2007.

[9] Bahl I.J., "High-Q and Low-Loss Matching Network Elements for RF and Microwave Circuits," IEEE MTT-S Int'l Microwave Symp. Digest, vol. 1, no. 3, pp. 64-73, Sep. 2000.

[10] Bakhtiar A.S., Jalali M.S., and Mirabbasi S., "A High-Efficiency CMOS Rectifier for Low-Power RFID Tags," IEEE Int'l Conf. RFID, pp. 83-88, USA, 2010.

[11] Balachandran G.K., and Barnett R.E., "A Passive UHF RFID Demodulator With RF Overvoltage Protection and Sutomatic Weighted Threshold Adjustment," IEEE. Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 9. Pp. 2291-2300, Sep. 2010.

[12] Balachandran G.K., and Barnett R.E., "A 110 nA Voltage Regulator System with Dynamic Bandwidth Boosting for RFID Systems," IEEE J. Solid-Stage Circuits, vol. 41, no. 9, pp. 2019-2028, Sep. 2006.

[13] Barnett R.E., Liu J., and Lazar S., "A RF to DC Voltage Conversion Model for Multi-Stage Rectifiers in UHF RFID Transponders," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 254-370, Feb. 2009.

[14] Barnett R.E., Lazar S., and Liu J., "Design of Multistage Rectifiers with Low-Cost Impedance Matching for Passive RFID Tags," IEEE Symp. Radio Frequency Integrated Circuits (RFIC), USA, 2006.

[15] Bashirullah R., *et al.*, "A Smart Bi-Directional Telemetry Unit for Retinal Prosthetic Device," Proc. Int'l Symp. Circuits and Systems (ISCAS), vol. 5, pp. V-5-V-8, 2003.

[16] Bawa G., Huang A.Q., and Ghovanloo M., "An Efficient 13.56 MHz Active Back-Telemetry Rectifier in Standard CMOS Technology," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 1201-1204, France, 2010.

[17] Bawa G., and Ghovanloo M., "A Back Telemetry-Capable Active High Efficiency Rectifier in Standard CMOS Process," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 2514-2517, USA, 2008.

[18] Bawa G., and Ghovanloo M., "Analysis, design, and implementation of a high-efficiency full-wave rectifier in standard CMOS technology," Analog Integrated Circuits and Signal Processing, vol. 60, no. 1-2, pp. 71-81, 2009.

[19] Bawa G., and Ghovanloo M., "Active High Power Conversion Efficiency Rectifier with Built-In Dual-Mode Back telemetry in Standard CMOS Technology," IEEE Trans. Biomedical Circuits and Systems, vol. 2, no. 3, pp. 184-192, Sep. 2008.

[20] Bawa G., Jow U.-M., and Ghovanloo M., "A High Efficiency Full-Wave Rectifier in Standard CMOS Technology," MWSCAS 2007 Symp. Circuits and Systems, pp. 81-84, Canada, 2007.

[21] Bawa G., Jow U.-M., and Ghovanloo M., "A High Efficiency Full-Wave Rectifier in Standard CMOS Technology," IEEE Midwest Symp. Circuits and Systems (MWSCAS), pp. 81-84, Canada, 2007.

[22] Ben-Yaakov S., and Krihely N., "New Resonant Rectifier for Capacitive Sources," in Proc. 23rd IEEE Conv. Elect. Electron. Eng., pp. 48–51, Sep. 2004.

[23] Berg Y., Wisland D.T., and Lande T.S., "Ultra Low-Voltage/Low-Power Digital Floating-Gate Circuits," IEEE Trans. Circuits and Systems-II, vol. 46, pp. 930-936, May 1999.

[24] Bhatti P., Lee S., and Wise K., "A 32-Site 4-Channel Cochlear Electrode Array," ISSCC Dig. Tech. Papers, pp. 50-51, Feb. 2006.

[25] Blalock B.J., Allen P.E., and Rincon-Mora G.A., "Designing 1-V Op Amps Using Standard Digital CMOS Technology," IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 7, pp. 769-780, Jul. 1998.

[26] Bogle A.G., "Rectifier Circuit Performance: Some New Approximate Formulas," Proc. IEE, vol. 124, No. 12, pp. 1127-1134, 1977.

[27] Chaimanonart N., and Young D.J., "Remote RF Powering System for Wireless MEMS Strain Sensors," IEEE J. Sensors, vol. 6, no. 2, pp. 484-489, Apr. 2006.

[28] Che W., *et al.*, "Analysis, Design and Implementation of Semi-Passive Gen2 Tag," IEEE Int'l Conf. RFID, pp. 15-19, USA, 2009.

[29] Chen C.-L., Chen K.-H., and Liu S.-I., "Efficiency-Enhances CMOS Rectifier for Wireless Telemetry," Electron Letters, vol. 43, no. 18, pp. 976-978, Aug. 2007.

[30] Chen P.-Y., *et al.*, "A Low-Cost VLSI Architecure for Fault-Tolerant Fusion Center in Wireless Sensor Networks," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 4, pp. 803-813, Apr. 2010.

[31] Choi Y.B., and Yeoh W.G., "Air-Interfacing Microwave Passive RFID Tag in Bulk CMOS," IEEE Int'l Workshop Radio-Frequency Integration Technology (RFIT): Integrated Circuits for Wideband Communication and Wireless Sensor Networks, pp. 65-69, 2005.

[32] Cole P., Ng M.L., and Leong K.S., "Some Notes on Antenna Matching and Measurement for Small RFFID Tags [online], Available: http/autoidlab.adelaide.edu.au.

[33] Curty J.-P., *et al.*, "A Model For µ-Power Rectifier Analysis and Design," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 52, no. 12, pp. 2771-2779, Dec. 2005.

[34] Curty J.-P., *et al.*, "Remotely Powered Addressable UHF RFID Integrated Systems," IEEE J. Solid-State Circuits, vol. 40, no. 11, pp. 2193-2202, Nov. 2005.

[35] Dallago E., *et al.*, "Self-Supplied Integrable Active High-Efficiency AC-DC Converter for Piezoelectric Energy Scavenging Systems," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 1633-1636, USA, 2007.

[36] Dallago E., *et al.*, "Active Self Supplied AC-DC Converter for Piezoelectric Energy Scavenging Systems with Supply Independent Bias," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 1448-1451, USA, 2008.

[37] De Hennis A.D., and Wise K.D., "A wireless microsystem for the remote sensing of pressure, temprature, and relative humidity," IEEE J. Microelectromechanical Systems, vol. 14, no. 1, pp. 12-22, Feb. 2005.

[38] De Roover C., and Steyaert M., "A Fully Integrated Wireless Power Supply for Pinless Active RFID-devices in 130nm CMOS," IEEE Asian Conf. Solid-State Circuits (ASSCC), pp. 123-126, 2007.

[39] De Vita G., and Iannaccone G., "Design Criteria for the RF Section of UHF and Microwave Passive RFID Transponsers," IEEE Trans. Microwave Theory Tech., vol. 53, no. 9, pp. 2978-2980, 2005.

[40] De Vita G., and Iannaccone G., "Ultra Low Power RF Section of a Passive Microwave RFID Transponder in 0.35 μm BiCMOS," IEEE Int'l Symp. Circuits and Systems (ISCAS), vol. 5, pp. 5075-5078, 2005.

[41] Dolgov A., Zane R., and Popovic Z., "Power Management System for Online Low Power RF Energy Harvesting Optimization," IEEE. Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 7, pp. 1802-1811, July 2010.

[42] Ebrahimian M., El-Sankary K., and El-Masry E., "Enhanced RF to DC CMOS Rectifier with Capacitor Bootstrapped Transistor," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 1655-1658, France, 2010.

[43] Facen A., and Boni A., "Power Supply Generation in CMOS Passive UHF RFID Tags," PhD Research in Microelectronics and Electronics, 2006.

[44] Facen A., and Boni A., "A CMOS Analog Frontend for a Passive UHF RFID Tag," Int'l Symp. Low Power Electronics and Design (ISLPED), pp. 280-285, 2006.

[45] Finkenzeller K., RFID-Hnadbook. John Wiley and Sons Ltd., 2003.

[46] Fu Q., *et al.*, "Optimization for the NMOS and PMOS Gate Cross-Connected Rectifier for RF Power Extraction in RFID Applications," Asia-Pacific Microwave Conf. (APMC), pp. 1-4, China, 2008.

[47] Ghovanloo M., and Najafi K., "Fully Integrated Power Supply Design for Wireless Biomedical Implants," IEEE-EMB Int'l Special Topic Conf. Microtechnologies in Medicine and Biology, pp. 414-419, USA, 2002.

[48] Ghovanloo M., and Najafi K., "A Modular 32-Site Wireless Neural Stimulator Microsystem," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2457-2466, Dec. 2004.

[49] Ghovanloo M., *et al.*, "A BiCMOS Wireless Interface Chip for Micromachined Stimulating Microprobes," Int'l IEEE-EMBS Special Topic Conf. Microtechnologies in Medicine and Biology, pp. 277-282, USA, 2002.

[50] Ghovanloo M., and Najafi K., "A BiCMOS Wireless Stimulator Chip for Micromachined Stimulating Microprobes," Proc. IEEE 2nd EMBS BMES Conf., pp. 2113-2114, Oct. 2002.

[51] Ghovanloo M., Wise K.D., and Najafi K., "Toward a Button-Sized 1024-Site Wireless Cortical Stimulating Array," Proc. 1st Int'l IEEE/EMBS Conf., Neural Eng., pp. 138-141, Mar. 2003.

[52] Ghovanloo M., and Najafi K., "Fully Integrated Wideband High-Current Rectifiers for Inductively Powered Devices," IEEE J. Solid-State Circuits, vol. 39, no. 11, pp. 1976-1984, Nov. 2004.

[53] Ghovanloo M., and Atluri S., "An Integrated Full-Wave Rectifier with Built-In Back Telemetry for RFID and Implantable Biomedical Applications," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 55, no. 10, pp. 3328-3334, Nov. 2008.

[54] Glasser L.A., Malamy A.C., and Selvidge C.W., "A Magnetic Power and Communication Interface for a CMOS Integrated Circuit," IEEE J. Solid-Sate Circuits, vol. 24, no. 4, pp. 1146-1149, Aug. 1989.

[55] Glidden R., *et al.*, "Design of Ultra-Low-Cost UHF RFID Tags for Supply Chain Applications," IEEE Commun. Mag., vol. 42, pp. 140-151, Aug. 2004.

[56] Gong C.-C.A., *et al.*, "Efficient CMOS Rectifier for Inductively Power-Harvested Implants," IEEE Int'l Conf. Electron Devices and Solid-State Circuits (EDSSC), pp. 1-4, 2008.

[57] Gosselin B., *et al.*, "A mixed-signal multichip neural recording Interface with bandwidth reduction," IEEE Trans. Biomedical Circuits and Systems, vol. 3, no. 3, pp. 129-141, June 2009.

[58] Gosset G., Rue B., and Flandre D., "Very High Efficiency 13.56 MHz RFID Input Stage Voltage Multipliers Based On Ultra Low Power MOS Diodes," IEEE Int'l RFID Conf., pp. 134-140, USA, 2008.

[59] Gudnason G., Bruun E., and Haugland M., "A Chip for an Implantable Neural Stimulator," Kluwer Academic Publications, Analog Integrated Circuits and Signal Processing, no. 22, pp. 81-89, 1999.

[60] Guilar N.J., Amirtharajah R., and Hurst P.J., "A Full-Wave Rectifier for Interfacing with Multi-Phase Piezoelectric Energy Harvesters," IEEE Int'l Solid-State Circuits Conf.(ISSCC), Digest of Technical Papers, pp. 302-615, USA, 2008.

[61] Guilar N.J., Amirtharajah R., and Hurst P.J., "A Full-Wave Rectifier with Integrated Peak Selection for Multiple Electrode Piezoelectric Energy Harvesters," IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 240-246, Jan. 2009.

[62] Guo S., and Lee H., "An Efficiency-Enhanced Integrated CMOS Rectifier with Comparator-Controlled Switches for Transcutaneous Powered Implants," IEEE Custom Integrated Circuits Conf. (CICC), pp. 385-388, USA, 2007.

[63] Guo S., and Lee H., "An Efficiency-Enhanced CMOS Rectifier with Unbalanced-Biased Comparators for Transcutaneous-powered High-Current Implants," IEEE J. Solid-State Circuits, vol. 44, no. 6, pp. 1796-1804, Jun. 2009.

[64] Guyomar D., *et al.*, "Toward Energy Harvesting Using Active Materials and Conversion Improvement by Nonlinear Processing," IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control, vol. 52, no. 4, pp. 584–595, Apr. 2005.

[65] Hall K.S., "Calculation of Rectifier-Circuit Performance," IEE Physical Science, Measurement and Instrumentation, Management and Education – Reviews, vol. 127, no. 1, pp. 54-60, Jan. 1980.

[66] Harison R.G., "Full Nonlinear Analysis for Detector Circuits Using Ritz-Galerkin Theory," IEEE MTT-S Int'l Microwave Symp. Dig., pp.267-270, Jun. 1992.

[67] Hashemi S., Sawan M., and Savaria Y., "Modeling Power Budget Requirements of Implantable Electronic devices", 12th IEEE Int'l Conf. Electronics, Circuits and Systems (ICECS'05), Tunisia, Dec. 2005.

[68] Hashemi S., Sawan M., and Savaria Y., "A Novel Fully-Integrated Low-Drop Voltage CMOS Rectifier for Wirelessly Powered Devices", 19th Int'l Conf. Microelectronics (ICM'07), Egypt, Dec. 2007.

[69] Hashemi S., Sawan M., and Savaria Y., "A Power Planning Model for Implantable Stimulators", IEEE Int'l Symp. Circuits and Systems (ISCAS'06), Greece, May 2006.

[70] Hashemi S., Sawan M., and Savaria Y., "Fully-integrated low-voltage high-efficiency CMOS rectifier for wirelessly powered devices", 7th IEEE Int'l North Eastern Workshop on Circuits and Systems (NEWCAS-TAISA'09), France, June 2009.

[71] Hashemi S., Sawan M., and Savaria Y., "A low-area power-efficient CMOS active rectifier for wirelessly powered medical devices", 16th IEEE Int'l Conf. Electronics, Circuits and Systems (ICECS'09), Tunisia, Dec. 2009.

[72] Hashemi S., Sawan M., and Savaria Y., "Multi-coils-based inductive links dedicated to power up implantable medical devices: Modeling, design and experimental results", Springer Journal of Biomedical Microdevices, pp. 1059-1070, vol. 11, no. 5, October 2009.

[73] Hashemi S., Sawan M., and Savaria Y., "A novel low-drop CMOS active rectifier for RF-powered devices: Experimental results", Elsevier Microelectronics Journal, vol. 40, no. 11, pp. 1547-1554, November 2009.

[74] Hashemi S., Sawan M., and Savaria Y., "A High-Efficiency Low-Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices", Paper to appear, IEEE Trans. On Biomedical Circuits and Systems, June 2011.

[75] Hashemi S., Sawan M., and Savaria Y., "Low-Area and Flow-Back Current Free CMOS Integrated Rectifiers for Power Scavenging Devices," submitted to IEEE Transactions on Circuits and Systems: Regular Papers –I, June 2011.

[76] Hasting A., The Art of Analog Layout, Upper Saddle River, NJ: Prentice-Hall, 2001.

[77] Hirano Y., *et al.*, "Impact of 0.10 μm SOI CMOS with Body-Tied Hybrid Trench Isolation Structure to Break Through the Scaling Crisis of Silicon Technology," IEEE Electron Device Meeting (IEDM) Tech. Dig., pp. 467-470, Dec. 2000.

[78] Hooper M., Kucic M., and Hasler P., "Characterization of Charge-Pump Rectifiers for Standard Submicron CMOS Processes," IEEE Int'l Symp. Circuits and Systems (ISCAS), vol. 5, pp. 964-967, 2004.

[79] Hu J., and Min H., "A Low Power and High Performance Analog Front End for Passive RFID Transponder," IEEE Workshop Automatic Identification Advanced Technologies (AutoID), USA, 2005.

[80] Hu J., He Y., and Man H., "High Efficient Rectifier Circuit Eliminating Threshold Voltage Drop for RFID Transponders," Int'l Conf. ASIC (ASICON), pp. 607-610, China, 2005.

[81] Hu Y., and Sawan M., "A Fully Integrated Low-Power BPSK Demodulator for Implantable Medical Devices," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 52, no. 12, pp. 2552-2562, Dec. 2005.

[82] Hu Y., Sawan M., and El-Gamal M.N., "A Power Recovery Strategy Dedicated to Implantable Applications," Proc. IEEE Int'l Conf. Electronics, Circuits and Systems (ICECS), vol. 3, pp. 1212-1215, 2003.

[83] Huang Q., and Oberle M., "A 0.5-mW Passive Telemetry IC for Biomedical Applications," IEEE J. Solid-State Circuits, vol. 33, no. 7, pp. 937-946, Jul. 1998.

[84] Joynson R.E., *et al.*, "Eliminating Threshold Losses in MOS Circuits by Bootstrapping Using Varactor Coupling," IEEE J. Solid-State Circuits, vol. 7, no. 3, pp. 217-224, Jun. 1972.

[85] Kaiser U., and Steinhaugen W., "A Low-Power Transponder IC for High-Performance Identification Systems", IEEE J. Solid-State Circuits, vo1.30, pp. 306-310, Mar. 1995.

[86] Karthaus U., and Fischer M., "Fully Integrated Passive UHF IFID Transponder IC with 16.7-μW Minimum RF Input Power," IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1602-1608, Oct. 2003.

[87] Kelly S.K., and Wyatt J., "A Power-Efficient Voltage-Based Neural Tissue Stimulator with Energy Recovery," IEEE Int'l Solid-State Circuits Conf. (ISSCC), vol. 1, pp. 228 - 230, 2004.

[88] Ki W.-H., Su F., and Tsui C.-Y., "Charge Redistribution Loss Consideration in Optimal Charge Pump Design," IEEE Int'l Symp. Circuits and Systems (ISCAS), vol. 2, pp. 1895-1898, 2005.

[89] Kim S.T., *et al.*, "Semi-Active High-Efficient CMOS Rectifier for Wireless Power Transmission," IEEE Radio Frequency Integrated Circuits Symp. (RFIC), pp. 97 -100, USA, 2010.

[90] Kocer F., and Flynn M.P., "A New Transponder Architecture with On-Chip ADC for Long-Range Telemetry Application," IEEE J. Solid-Stage Circuits, vol. 41, no. 5, pp. 1142-1148, May 2006.

[91] Kolnsberg S., "Drahtlose Signal-und Energieubertragung mit Hilfe von Hochfrequenztechnik in CMOS-Sensor Systems," PhD Thesis, Duisburg University, 2001.

[92] Kotani K., Sasaki A., and Ito T., "High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs," IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3011-3018, Nov. 2009.

[93] Kotani K., and Ito T., "High Efficiency CMOS Rectifier Circuits for UHF RFIDs Using Vth Cancellation Techniques," IEEE Int'l Conf. ASIC (ASICON), pp. 549-552, 2009.

[94] Kotani K., and Ito T., "High Efficiency CMOS Rectifier Circuit with Self-Vth-Cancellation And Power Regulation Functions for UHF RFIDs," IEEE Asian Solid-State Circuits Conf. (ASSCC), pp. 119-122, 2007.

[95] Krihely N., Ben-Yaakov S., "Self-Contained Resonant Rectifier for Piezoelectric Sources Under Variable Mechanical Excitation," IEEE Trans. Power Electronics, vol. 26, no. 2, pp. 612-621, Feb. 2011.

[96] Lallart M., and Guyomar D., "An Optimized Self-Powered Switching Circuit for Non-Linear Energy Harvesting with Low-Voltage Output," Smart Materials and Structures, vol. 17, no. 3, pp. 1–8, 2008.

[97] Lam Y.-H., Ki W.-H., and Tsui C.-Y., "Integrated Low-Loss CMOS Active Rectifier for Wirelessly Powered Devices," IEEE Trans. Circuits and Systems II: Express Briefs, vol. 53, no. 12, pp. 1378-1382, Dec. 2006.

[98] Le T., Mayaram K., and Fiez T., "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Networks," IEEE J. Solid-State Circuits, vol. 43, no. 5, pp. 1287 - 1302, May 2008.

[99] Le T.T., *et al.*, "Piezoelectric Micro-Power Generation Interface Circuits," IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1411-1420, Jun. 2006.

[100] Le T.T., Maryaram K., and Fiez T.F., "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," IEEE J. Solid-State Circuits, vol. 43, no. 5, pp. 1287-1302, May 2008.

[101] Lee E., *et al.*, "A Biomedical Implantalbe FES Battery-Powered Micro-Stimulator," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 56, no. 12, pp. 2583-2593, Dec. 2009.

[102] Lee E.K.F., "High-Voltage Rectifier and Voltage Doubler in Conventional 0.18μm Process," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 605-608, France, 2010.

[103] Lehmann T., and Cassia M., "1-V Power Supply CMOS Cascode Amplifier," IEEE J. Solid-State Circuits, vol. 36, no. 7, pp. 1082-1086, Jul. 2001.

[104] Lehmann T., and Moghe Y., "On-Chip Active Power Rectifiers for Biomedical Applications," IEEE Int'l Symp. Circuits and Systems (ISCAS), vol. 1, pp. 732 -735, 2005.

[105] Li Q., *et al.*, "A Low Power CMOS Rectifier for Wirelessly Powered Devices," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 873-876, France, 2010.

[106] Lim J., *et al.*, "High Sensitive RF-DC Rectifier and Ultra Low-Power DC Sensing Circuit for Waking Up Wireless Systems," Asia Pacific Microwave Conf. (APMC), pp. 237-240, Singapore, 2009.

[107] Liu W., *et al.*, "A Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthesis Device," IEEE J. Solid-State Circuits, vol. 35, pp. 1487-1496, Oct. 2000.

[108] Ma C., Zhang C., and Wang Z., "Power Analysis for the MOS AC/DC Rectifier of Passive RFID Transponders," IEEE Circuit and Systems Asia Pacific Conf., pp. 1350 - 1353, Singapore, 2006.

[109] Ma C., Zhang C., and Wang Z., "A Low-Power AC/DC Rectifier for Passive UHF RFID Transponder," Int'l Symp. Microwave, Antenna, Propagation and EMC Technologies for Wireless Communication, pp. 309-314, China, 2007.

[110] Makihara K., Onoda J., and Miyakawa T., "Low-Energy Dissipation Electric Circuit for Energy Harvesting," Smart Mater. Struct., vol. 14, pp. 1493-1498, 2006.

[111] Mandal S., and Sarpeshkar R., "Low-Power CMOS Rectifier Design for RFID Applications," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 54, no. 6, pp. 1177-1188, Jun. 2007.

[112] Man T.Y., Mok P.K.T., and Chan M., "A CMOS-Control Rectifier for Discontinuous Conduction Mode Switching DC-DC Converters," IEEE Int'l Solid-State Circuits Conf. (ISSCC), Digest of Technical Papers, pp. 1408-1417, USA, 2006.

[113] Marinkovic D., *et al.*, "A New Rectifier and Trigger for a Piezoelectric Microgenerator," Proc. Eurosensors XXII Conf., Elsevier, vol. 1, no. 1, pp. 1447-1450, 2009.

[114] Masui S., *et al.*, "A 13.56 MHz CMOS RF Identification Transponder Integrated Circuit with a Dedicated CPU," IEEE Int'l Solid-State Circuits Conf. (ISSCC), Digest of Papers, pp. 162-163, USA, 1999.

[115] Matei E., *et al.*, "A Biomedical Implantable FES Battery-Powered Micro-Stimulator," Proc. IEEE 2008 CICC, pp. 317-324, Sep. 2008.

[116] Mazzilli F., *et al.*, "Design Methodology and Comparison of Rectifiers for UHF-band RFIDs," IEEE Radio Frequency Integrated Circuits Symp. (RFIC), pp. 505-508, USA, 2010.

[117] McDermott H., "A Custom-Designed Receiver-Stimulator Chip for an Advanced Multiple-Channel Hearing Prosthesis," IEEE J. Solid-State Circuits, vol.26, pp. 1161 - 1164, Aug. 1991.

[118] Missoni A., *et al.*, "A Triple-Band Passive RFID Tag," IEEE Int'l Solid-State Circuits Conf. (ISSCC), Digest of Technical Papers, pp. 288-614, USA, 2008.

[119] Mounaim F., and Sawan M., "Integrated high-voltage inductive power and data recovery front-end dedicated to implantable devices," IEEE Trans. Biomed. Circuit and Systems, vol. 5, no. 3, pp. 283-291, Feb. 2011.

[120] Nagasawa S., *et al.*, "Mechanical Rectifier for Micro Electric Generators," IEEE Int'l Conf. Micro Electro Mechanical Systems (MEMS), pp. 992-995, USA, 2008.

[121] Nakamoto H., *et al.*, "A Passive UHF RF Identification CMOS Tag IC Using Ferroelectric RAM in 0.35-μm Technology," IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 101-110, Jan. 2007.

[122] Nakamoto H., *et al.*, "A Passive UHF RFID Tag LSI with 36.6% Efficiency CMOS-Only Rectifier and Current-Mode Demodulator in 0.35 μm FeRAM Technology," IEEE Int'l Solid-State Circuits Conf. (ISSCC), Digest of Technical Papers, pp. 1201-1210, USA, 2006.

[123] Ngo K.D.T., *et al.*, "Power Converters for Piezoelectric Energy Extraction," 2006 ASME Int'l Mechanical Engineering Congress and Exposition (IMECE2006), vol. 1, pp. 597 - 602, USA, Nov. 2006.

[124] Onizuka K., *et al.*, "Chip-to-Chip Inductive Wireless Power Transmission System for SiP Applications, IEEE Custom Integrated Circuits Conf. (CICC), pp. 575-578, USA, 2006.

[125] Ortmanns M., *et al.*, "A 232-channel epiretinal stimulator ASIC," IEEE J. Solid-State Circ., vol. 42, pp. 2946-2959, Dec. 2007.

[126] Panitantum N., *et al.*, "A CMOS RFID Transponder," http://www.geocities.ws/kitalo17/Papers/ISCIT3_CMOS_RFID.pdf.

[127] Peters C., *et al.*, "A CMOS Integrated Voltage and Power Efficient AC/DC Converter for Energy Harvesting Applications," J. Microelectronics and Microengineering, vol. 18, no. 10, 2008.

[128] Peters C., *et al.*, "Experimental Results on Power Efficient Single-Poly Floating Gate Rectifies," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 1097-1100, Taiwan, 2009.

[129] Peters C., *et al.*, "High-Bandwidth Floating Gate CMOS Rectifiers with Reduced Voltage Drop," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 2598-2601, USA, 2008.

[130] Peters C., et al., "CMOS Integrated Highly Efficient Full Wave Rectifier," IEEE Int'l Symp. Circuits and Systems (ISCAS), pp. 2415-2418, USA, 2007.

[131] Peters C., Ortmanns M., and Manoli Y., "CMOS Integrated Active Rectifier with Temperature Independent Efficiency," IEEE NORCHIP Conf., Estonia, 2008.

[132] Peters C., Ortmanns M., and Manoli Y., "Fully CMOS Integrated Active Rectifier without Voltage Drop," Midwest Symp. Circuits and Systems (MWCAS), pp. 185-188, USA, 2008.

[133] Peters C., *et al.*, "An Ultra-Low-Voltage Active Rectifier for Energy Harvesting Applications," IEEE Symp. Circuits and Systems (ISCAS), pp. 889-892, France, 2010.

[134] Pillai V., *et al.*, "An Ultra-Low-Power Long Range Battery/Passive RFID Tag for UHF and Microwave Bands With a Current Consumtion of 700 nA at 1.5 V," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 54, no. 7, pp. 1500-1512, July 2007.

[135] Raisigel H., *et al.*, "Autonomous, low voltage, high efficiency, CMOS rectifier for three-phase micro generators, IEEE Solid-Stage Sensors, Actuators and Microsystems Conf., pp. 883-886, France, 2007.

[136] Rakers P., *et al.*, "Secure Contactless Smartcard ASIC with DPA Protection," IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 559-565, Mar. 2001.

[137] Ramadass Y.K., and Chandrakasan A.P., "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," IEEE J. Solid-State Circuits, vol. 45, no. 1, pp. 189-204, Jan. 2010.

[138] Ramadass Y.K., and Chandrakasan A.P., "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," IEEE Int'l Solid-State Circuits Conf. (ISSCC), Digest of Technical Papers, pp. 296-297, 2009.

[139] Rao K.V.S., Nikitin P.V., and Lam S.F., " Impedance Matching Concepts in RFID Transponder Design," IEEE Workshop Advanced Automatic Identification Technologies, vol. 10, pp. 39, 2005.

[140] Razavi B., Design of Analog CMOS Integrated Circuits, New York: McGraw Hill, 2001.

[141] Richard C., *et al.*, "Enhanced Semi-Passive Damping Using Continuous Switching of a Piezoelectric Device on an Inductor," in Proc. SPIE Smart Struct. Mater. Conf., Passive Damping Isolation, pp. 288–299, 2000.

[142] Rue B., Levacq D., and Flandre D., "Low-Voltage Low-Power High-Temperature SOI CMOS Rectifiers," IEEE Int'l SOI Conf., pp. 65-66, USA, 2006.

[143] Sasaki A., Kotani K., and Ito T., "Differential-Drive CMOS Rectifier for UHF RFIDs with 6% PCE at -12 dBm Input," IEEE Asian Solid-State Circuits Conf. (A-SSCC), pp. 105-108, Japan, 2008.

[144] Sauer C., *et al.*, "Power Harvesting and Telemetry in CMOS for Implanted Devices," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 52, no. 12, pp. 2605-2613, Dec. 2005.

[145] Schade O.H., "Analysis of Rectifier Operation," Proc. IRE, vol. 31, pp. 341-347, 1943.

[146] Sedra A.S., and Smith K.C., Microelectronic Circuits, 5th ed., Oxford U.K.: Oxford Univ. Press, 2004.

[147] Seeman M.D., and Sanders S.R., "Analysis and Optimization of Switched-Capacitor DC-DC Converters," IEEE Trans. Power Electronics, vol. 23, no. 2, pp. 841-8851, Mar. 2008.

[148] Seeman M.D., and Sanders S.R., "Analysis and Optimization of Switched-Capacitor DC-DC Converters," IEEE COMPEL Workshop, pp. 216-224, USA, 2006.

[149] Seeman M.D., Sanders S.R., and Rabaey J.M., "An Ultra-Low-Power Power Management IC for Wireless Sensor Nodes," IEEE Custom Integrated Circuits Conf. (CICC), pp. 567-570, USA, 2007.

[150] Seeman M.D., Sanders S.R., and Rabaey J.M., "An Ultra-Low-Power Power Management IC for Energy-Scavenging Wireless Sensor Nodes," IEEE Power Electronics Specialists Conf. (PESC), pp. 925-931, 2008.

[151] Shameli A., *et al.*, "Power Harvester Design for Passive UHF RFID Tag Using a Voltage Boosting Technique," IEEE Trans. Microwave Theory Tech., vol. 55, no. 6, pp. 1089 - 1097, 2007.

[152] Shin J., *et al.*, "A New Charge Pump Without Degradation in Threshold Voltage due to Body Effect," IEEE J. Solid-State Circuits, vol. 35, pp. 1227-1230, Aug. 2000.

[153] Siebert A., Troedson A., and Ebner S., "AC to DC Power Conversion Now and in the Future," IEEE Trans. Industry Applications, vol. 38, no. 4, pp. 934-940, Jul./Aug. 2002.

[154] Sodagar A.M., *et al.*, "Fully-Integrated CMOS Power Regulator for Telemetry-Powered Implantable Biomedical Microsystems," IEEE Custom Integrated Circuits Conf. (CICC), pp. 659-662, USA, 2006.

[155] Soltani N., and Yuan F., "A High-Gain Power-Matching Technique for Efficient Radio-Frequency Power Harvest of Passive Wireless Microsystems," IEEE. Trans. Circuits and Systems-I: Regular Papers, vol. 57, no. 10, pp. 2685-2695, Oct. 2010.

[156] Stangel K., *et al.*, "A Programmable Introcular CMOS Pressure Sensor System Implant," IEEE J. Solid-State Circuits, vol. 36, pp. 1094-1100,July 2001.

[157] Suaning G .J., a nd Lovell N .H., " CMOS N eurostimulation A SIC w ith 100 C hannels, Scalable Output, and Bidirectional Radio-Frequency Telemetry," IEEE Trans. Biomedical Engineering, vol. 48, no. 2, pp. 248-460, Feb. 2001.

[158] Sze S.M., Physics of Semiconductor Devices, New York: Wiley, pp. 250, 1981.

[159] Taylor G. W., *et al.*, "The Energy Harvesting eel: A Small Subsurface Ocean/River Power Generator," IEEE J. Ocean. Eng., vol. 26, no. 4, pp. 539–547, Oct. 2001.

[160] Theilmann P.T., *et al.*, "Near Zero Turn-on Voltage High-Efficiency UHF RFID Rectifier in S ilicon-on-Sapphire C MOS," IEEE R adio F requency Integrated Circuits S ymp. (RFIC), pp. 105-108, USA, 2010.

[161] Umeda T ., *et al.*, "A 9 50-MHz R ectifier C ircuit f or S ensor Network Tags w ith 1 0-m Distance," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 35-41, Jan. 2006.

[162] Umeda T., *et al.*, "A 950 MHz Rectifier Circuit for Sensor Networks with 10m-Distance," IEEE Int'l S olid-State C ircuits C onf. (ISSCC), D igest of P apers, vol . 1, pp. 256 -597, USA, 2005.

[163] Usami M ., *et al.*, " P owder LSI: A n U ltra S mall R F Identification C hip f or Individual Recognition A pplications," IEEE Int'l S olid-State C ircuits C onf. (ISSCC), D igest of Tech. Papers, vol. 1, pp. 398-501, USA, 2003.

[164] Usami M., *et al.*, "A 0.05x0.05 mm^2 RFID Chip with Easily Scaled-Down ID-Memory," IEEE Int'l Solid-State Circuits Conf., Digest of Tech. Papers, pp. 482-483, USA, 2007.

[165] Vaillancourt P ., *et al.*, "EM R adiation B ehavior upon B iological T issues i n a R adio-Frequency Power Transfer Link for a Cortical Visual Implant." Proc. IEEE EMBC Conf., vol. 6. pp. 2499-2502, 1997.

[166] Villard P ., *et al.*, "A Low-Voltage Mixed-Mode CMOS/SOI Integrated Circuit for 13.56 MHz RFID Applications," IEEE Int'l SOI Conf., pp. 163-164, 2002.

[167] Wang G., *et al.*, "Design and Analysis of an Adapative Transcutaneous Power Telemetry for Biomedical Implants," IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 52, no. 10, pp. 2109-2117, Oct. 2005.

[168] Wang G., *et al.*, "Power Supply Topologies for Biphasic Stimulation in Inductively Powered Implants," IEEE Int'l Symp. Circuits and Systems (ISCAS), vol. 3, pp. 2743 - 2746, 2005.

[169] Wang X., *et al.*, "A High Efficiency AC-DC Charge Pump Using Feedback Compensation Technique," IEEE Asian Solid-State Circuits Conf. (ASSCC), pp. 252 - 255, 2007.

[170] Wu S.-M., Lin C.-Y., and Pai L.-C., "Analysis and Design of an Efficient RF/DC Rectifier for UHF Power Harvester," IEEE Int'l Conf. Wireless Information Technology and Systems (ICWITS), pp. 1-4, 2010.

[171] Xu S., *et al.*, "Converter and Controller for Micro-Power Energy Harvesting," IEEE Applied Power Electronics Conf. (APEC), vol. 1, pp. 226-230, USA, 2005.

[172] Xu S., *et al.*, "Low Frequency Pulsed Resonant Converter for Energy Harvesting," IEEE Trans. Power Electronics, vol. 22, no. 1, pp. 63-68, Jan. 2007.

[173] Yao Y., *et al.*, "A Fully Integrated 900 MHz Passive RFID Transponder Front-End with Novel Zero-Threshold RF-DC Rectifier," IEEE Trans. Industrial Electronics, vol. 56, no. 7, pp. 2317-2325, Jul. 2009.

[174] Yao Y., Shi Y., and Dai F.F., "A Novel Low-Power Input-Independent MOS AC/DC Charge Pump," IEEE Int'l Symp. Circuits and Systems (ISCAS), vol. 1, pp. 380 -383, 2005.

[175] Ye S., and Fan J., "A High Efficiency CMOS Rectifier for 900 MHz Passive RFID Tags," Pacific-Asia conf. Circuits, Communications and System (PACCS), pp. 450-452, China, 2010.

[176] Yeoh W.G., *et al.*, "A CMOS 2.45-GHz Radio Frequency Identification Tag IC with Read/Write Memory," IEEE Symp. Radio Frequency Integrated Circuits (RFIC), USA, 2005.

[177] Yi J., Ki W.-H., and Tsui C.-Y., "Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications, IEEE Trans. Circuits and Systems-I: Regular Papers, vol. 54, no. 1, pp. 153-166, Jan. 2007.

[178] Yuxiang Y., Yoshida Y., and Kuroda T., "Non-Contact 10% Efficient 36 mW Power Delivery Using On-Chip Inductor in 0.18-μm CMOS,"IEEE Asian Solid-State Circuits Conf. (ASSCC), pp. 115-118, 2007.