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Design Methodology of Tightly Regulated Dual-Output LLC Resonant Converter Using PFM-APWM Hybrid Control Method †

HwaPyeong Park, Mina Kim, HakSun Kim and JeeHoon Jung *

Ulsan National Institute of Science and Technology (UNIST), Ulsan KS017, Korea;
darkrla6@unist.ac.kr (H.P.); kmaop44@unist.ac.kr (M.K.); hszic@unist.ac.kr (H.K.)

* Correspondence: jhjung@unist.ac.kr or jung.jeehoon@gmail.com; Tel.: +82-052-217-2140

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Abstract: A dual-output LLC resonant converter using pulse frequency modulation (PFM) and asymmetrical pulse width modulation (APWM) can achieve tight output voltage regulation, high power density, and high cost-effectiveness. However, an improper resonant tank design cannot achieve tight cross regulation of the dual-output channels at the worst-case load conditions. In addition, proper magnetizing inductance is required to achieve zero voltage switching (ZVS) of the power MOSFETs in the LLC resonant converter. In this paper, voltage gain of modulation methods and steady state operations are analyzed to implement the hybrid control method. In addition, the operation of the hybrid control algorithm is analyzed to achieve tight cross regulation performance. From this analysis, the design methodology of the resonant tank and the magnetizing inductance are proposed to compensate the output error of both outputs and to achieve ZVS over the entire load range. The cross regulation performance is verified with simulation and experimental results using a 190 W prototype converter.

Keywords: resonant converter; dual output converter; pulse frequency modulation (PFM); asymmetric pulse width modulation (APWM)

1. Introduction

Nowadays, many industry fields require well-regulated multiple output voltages to guarantee the stable operation of products, such as ultra-high-definition (UHD) TVs, computers, and other home appliances. To satisfy this requirement, point-of-use power supplies (PUPS) have been used for multiple output applications. However, this method has disadvantages of bulky size and low cost-effectiveness with many power converter modules [1]. Therefore, tightly regulated multiple output converters have been developed to improve the power density and the cost-effectiveness.

In previous research for multiple output converters, cross regulation methods have been popular, since they require output voltage sensors to obtain the output voltage regulation. However, wide load variations between the multiple output channels induce large output voltage error [2–7]. The secondary side post regulators (SSPR) have been proposed to tightly regulate the output voltage with small output voltage error. They can regulate each output voltage independently, however, additional switches, gate driving circuits, and voltage controllers are required [8–20].

In terms of topology, the LLC resonant converter is attractive for several applications, because it has soft switching capability and a small number of resonant components [21–24]. In previous research of the multiple output LLC resonant converter, the cross regulation technique has been used

to regulate multiple output voltages [25,26]. In addition, the SSPR has been used to achieve tight output voltage regulation for the LLC resonant converter [27–30]. The LLC resonant converter using conventional control methods has the tradeoff between the cost effectiveness and regulation performance.

To obtain the high cost-effectiveness and tight output voltage regulation, the concept of a hybrid control method employing PFM and APWM was introduced for the dual-output LLC resonant converter in [31]. It does not require any additional components to implement the hybrid control algorithm, which shows the same cost-effectiveness as the conventional cross regulation method. However, it can only be applied to the dual-output converter. This previous research shows the preliminary operational principle and the decoupling algorithm to regulate the output voltages using the hybrid algorithm [32]. However, the previous research only shows the preliminary concept of the hybrid control algorithm. Therefore, the available voltage gain design, resonant tank design, and magnetizing inductance design are necessary to implement the hybrid control algorithm for the entire load condition with high power conversion efficiency.

In this paper, the design methodology of the dual-output LLC resonant converter with a hybrid control algorithm are proposed to regulate the output voltage with zero output voltage error and to obtain the ZVS capability for the entire load condition. The available voltage gain range is analyzed to implement the hybrid control algorithm. The design methodology of proper magnetizing inductance is proposed to achieve ZVS on the primary MOSFETs for the entire load range. The proper resonant tank design is proposed to compensate output voltage error for the worst-case load condition. In Section 4, the regulation performance of the dual-output LLC resonant converter with the hybrid control algorithm is verified through simulation and experimental results using a 190 W prototype converter.

2. Analysis of Dual-Output LLC Resonant Converter

The dual-output LLC resonant converter has the half-bridge structure of a primary inverting stage, a single transformer, and two output channels with diode rectifiers, as shown in Figure 1.

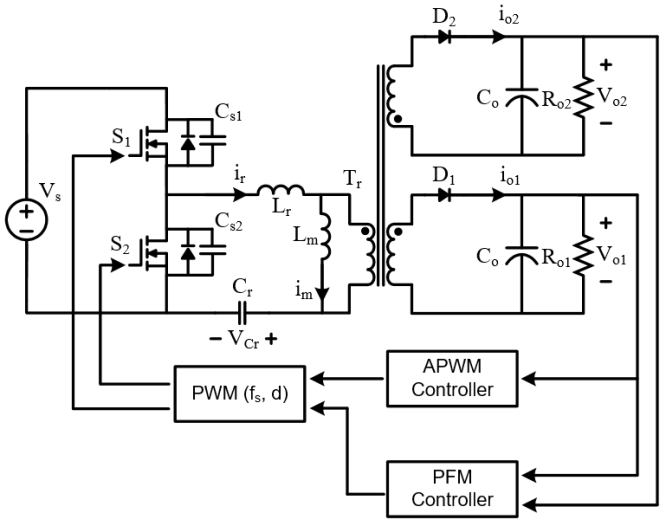


Figure 1. Schematic of the dual-output LLC resonant converter.

2.1. Operational Principle

Figure 2 shows the operation modes of the dual-output LLC resonant converter, which is divided into six modes during a single switching period. Mode 4 to Mode 6 are repeated from the previous half switching cycle. Figure 3 shows the operational waveforms of the dual-output converter. Mode 1 and 4 are a series resonant mode between the resonant inductance and the resonant

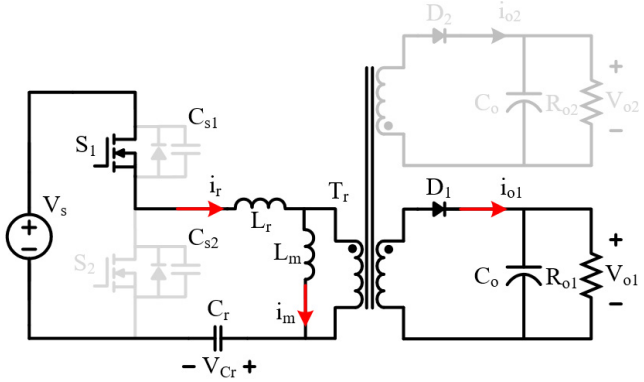
capacitance. During Mode 1, the proposed converter transfers electric power in the primary side to V_{o1} in the secondary side. The primary and magnetizing current for Mode 1 can be derived as follows:

$$\begin{aligned} i_r(t) &= I_{ini}\cos(\omega_r t) + C_r\omega_r\left(V_{in} - nV_{o1} - V_{cr,ini}\right)\sin(\omega_r t) \\ i_m(t) &= I_{ini} + \frac{nV_{o1}}{L_m}t \end{aligned} \quad (1)$$

where I_{ini} is the initial magnetizing current, C_r is the resonant capacitance, L_m is the magnetizing inductance, ω_r is the resonant angular frequency, V_{in} is the input voltage, n is the primary to secondary transformer turn ratio, V_{o1} is the one output voltage, and V_{cr} is the initial resonant capacitor voltage. During Mode 4, the converter transfers electric power to the V_{o2} side. The primary and magnetizing current for Mode 4 can be derived as follows:

$$\begin{aligned} i_r(t) &= I_{ini}'\cos(\omega_r t) + C_r\omega_r\left(V_{cr,ini}' - nV_{o2}\right)\sin(\omega_r t) \\ i_m(t) &= I_{ini}' - \frac{nV_{o2}}{L_m}t \end{aligned} \quad (2)$$

where I_{ini}' is the initial magnetizing current, and $V_{cr,ini}'$ is the initial resonant capacitor voltage.



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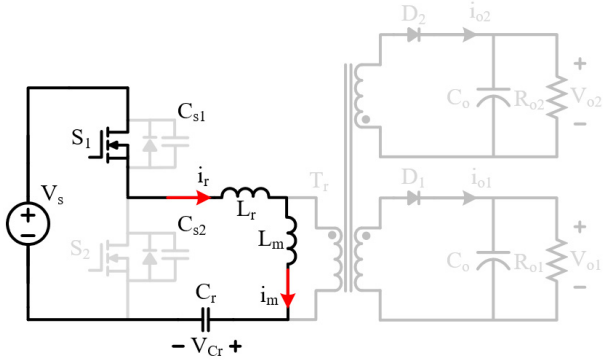

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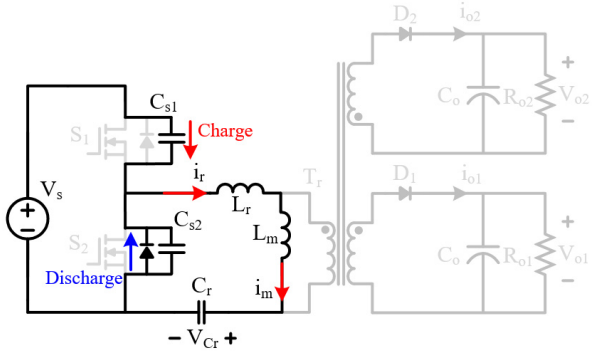
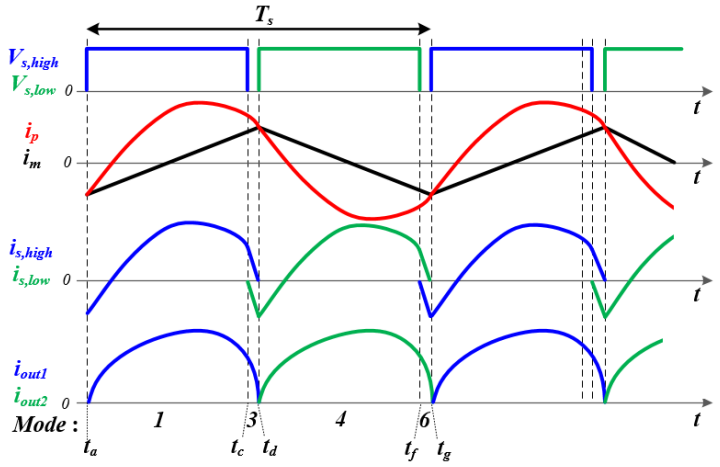


(**c**)

Figure 2. Operation mode of the dual-output LLC resonant converter: (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3.



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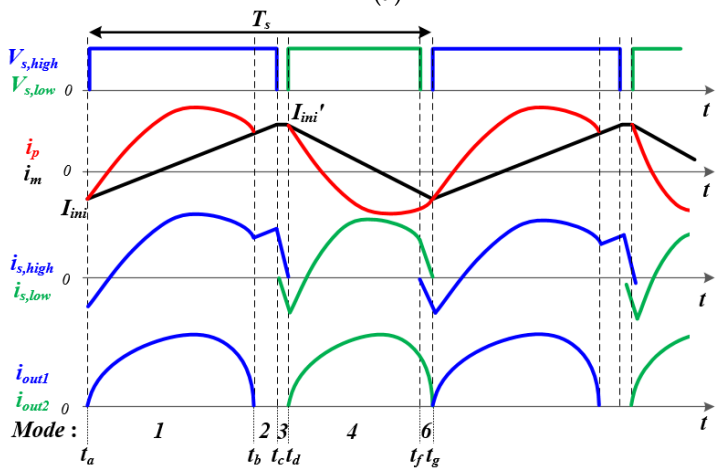

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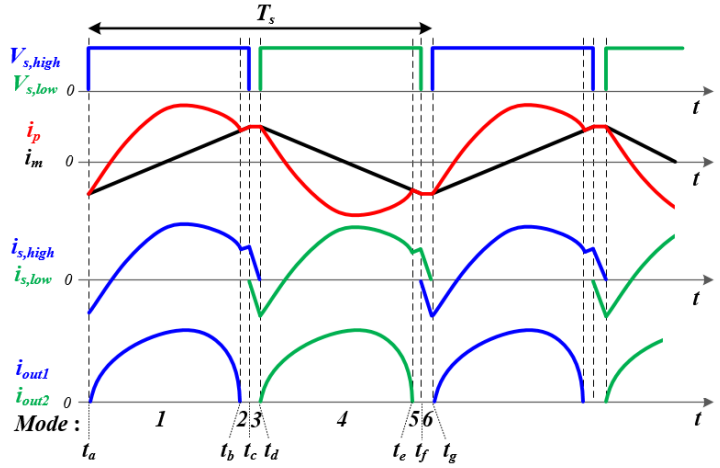


(**c**)

Figure 3. Operation mode of the dual-output LLC resonant converter: (**a**) Case A, (**b**) Case B, (**c**) Case C.

Mode 2 and 5 are parallel resonant modes among the resonant inductance, the magnetizing inductance, and the resonant capacitance. Those modes guarantee soft commutation on the secondary side diode rectifiers. Mode 3 and 6 are the dead time durations of the primary switch. During Mode 3 and 6, the output capacitance of the power switches is charged and discharged to obtain the ZVS. In steady state, the dual-output converter using the hybrid control algorithm can operate under a four operation mode (Case A), a five operation mode (Case B), and a six operation mode (Case C) according to output power conditions.

The light load condition makes the Case A operation, which induces no soft commutation on all output rectifiers during Mode 3 and 6. From middle to full load condition the converter operates according to Case B, which induces soft commutation on the diode of the V_{o1} channel during Mode 2 and 3. However, Mode 6 induces no soft commutation on the diode of the V_{o2} channel. When the same amount of power is transmitted to both output channels and the switching frequency is lower than the resonant frequency, the converter operates according to Case C, which induces soft commutation on all output rectifiers during Mode 2, 3, 5, and 6. Case C can show higher power conversion efficiency than that of Case A and B, because Case C has soft commutation capability on both the output rectifiers of V_{o1} and V_{o2} channels.

2.2. Gain Analysis According to Modulation Methods

The input-output voltage gain can be derived with the first harmonic approximation (FHA) as follows [29]:

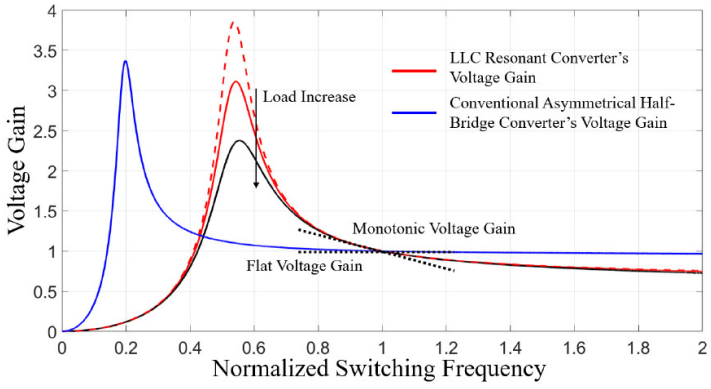
$$H_r(f_n) = \left[\left(1 + k - \frac{k}{f_n^2} \right)^2 + Q^2 \left(f_n - \frac{1}{f_n} \right)^2 \right]^{-\frac{1}{2}} \tag{3}$$

where f_n is the normalized switching frequency, k is L_r/L_m inductance ratio, and Q is the quality factor as follows:

$$R_{o,e} = \frac{V_{o,FHA}}{I_{o,FHA}} = \frac{8n^2}{\pi^2} R_o,\ f_n = \frac{f_s}{f_r},\ Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{o,e}},\ k = \frac{L_r}{L_m} \tag{4}$$

where R_o is the output resistance, f_s is the switching frequency, and f_r is the resonant frequency.

The conventional asymmetric half-bridge converter, only controlled by the APWM, uses small resonant inductance to obtain the linear voltage gain by the APWM [30]. However, it induces a flat voltage gain by the PFM, which cannot regulate the output voltage with PFM. Therefore, the resonant inductance is high enough to obtain the monotonic voltage gain by the PFM, as shown in Figure 4a. The large resonant inductance has limited monotonic voltage gain by the asymmetric duty variation.



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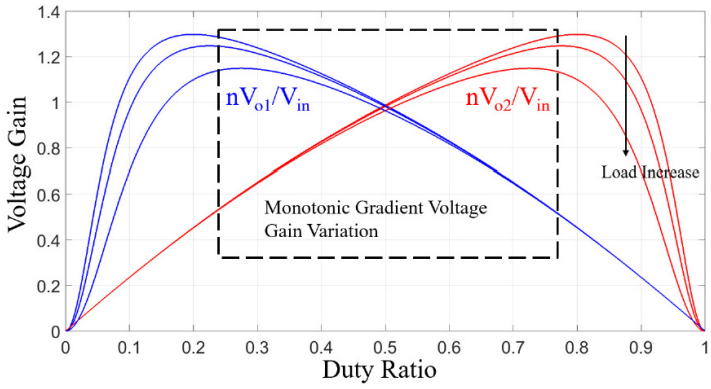


(**b**)

Figure 4. Voltage gain curves: (**a**) According to normalized switching frequency, (**b**) according to asymmetric duty ratio and load variation.

The conventional voltage gain of the APWM can be derived as follows [33]:

$$\frac{V_o}{V_{in}} \cong \frac{L_m D}{n\left(L_m + L_r\right)} \tag{5}$$

where D is the duty ratio. It has validity only for small resonant inductance conditions. Therefore, the voltage gain with enough resonant inductance is required to implement the hybrid control algorithm for the entire load conditions.

In steady state, the offset current on the magnetizing inductance can be derived as follows:

$$I_{offset} = \frac{I_{o1}}{n_1} - \frac{I_{o2}}{n_2} = \frac{1}{T_s}\int_0^{T_S}\left(i_r(t) - i_m(t)\right)dt \tag{6}$$

Assuming that V_{cr} is constant in Mode 1, $V_{cr,ini}$ can be derived as follows:

$$\begin{aligned} \frac{nV_{o1}DT_s}{L_m} &= \frac{V_{cr,ini}(1-D)T_s}{L_m} \\ V_{cr,ini} &= \frac{1-D}{D}nV_{o1} \end{aligned} \tag{7}$$

From (1)–(2) and (6)–(7), the proposed input to output voltage gains ($H_{o1}(D) = n_1V_{o2}/V_{in}$, $H_{o2}(D) = n_2V_{o2}/V_{in}$) according to the asymmetric duty ratio can be derived as follows:

$$\begin{aligned} \frac{nV_{o1}}{V_{in}} &= \frac{D'\dfrac{1-\cos(A)}{Z_1\omega_1}}{\dfrac{D'}{\omega_r}\left(R' + \dfrac{DT_s}{2L_m}\right)\sin(A) + D'^2T_s\left(\dfrac{1}{n_1^2R_{o1}} - \dfrac{1}{n_2^2R_{o2}}\right) + \dfrac{1-\cos(A)}{Z_1\omega_r}} \\ \frac{nV_{o2}}{V_{in}} &= \frac{D\dfrac{1-\cos(A')}{Z_1\omega_1}}{\dfrac{D}{\omega_r}\left(R' + \dfrac{(1-D)T_s}{2L_m}\right)\sin(A') + D^2T_sR' + \dfrac{1-\cos(A')}{Z_1\omega_r}} \end{aligned} \tag{8}$$

where $D' = 1 - D$, $Z_1 = L_r/C_r$, $R' = 1/(n_1^2R_{o1}) - 1/(n_2^2R_{o2})$, $A = \omega_rDT_s$, and $A' = \omega_rD'T_s$.

Figure 4b shows the voltage gain of the APWM according to load variations. It shows a complementary voltage gain relationship between V_{o1} and V_{o2} in the monotonic gradient voltage gain region. From (8), the design of APWM operational range is necessary to obtain the monotonic gradient voltage gain at the designed APWM range.

2.3. Magnetizing Inductance Design for Soft Switching Capability

The ZVS capability of the primary MOSFETs is achieved by discharging and charging their output capacitance during the dead time. Therefore, the LLC resonant converter requires enough magnetizing current and dead time duration to guarantee ZVS condition which can be expressed as follows:

$$i_p\left(t_{dt}\right) \geq i_{req}\left(t_{dt}\right) \tag{9}$$

where i_{req} (=$2V_{in}C_s/t_{dt}$) is the required minimum primary current to obtain the ZVS condition on the primary MOSFETs, C_s is the equivalent output capacitance of the primary MOSFETs, and t_{dt} is the dead time duration.

From (6), the dual-output LLC resonant converter makes an unbalanced magnetizing current during the dead time based on each load condition of the dual-output. The unbalanced magnetizing current has to satisfy (9) to achieve ZVS operation. Therefore, the design of the magnetizing inductance and the dead time duration should take unbalanced magnetizing currents into consideration. Assuming the primary current is constant during the dead time, the proposed ZVS condition in the dual-output converter can be derived as follows:

$$\begin{aligned} t_{dt1} &\geq \frac{\left(C_{s1}+C_{s2}\right)V_{in}}{\left|i_p\left(t_c\right)\right|} = \frac{\left(C_{s1}+C_{s2}\right)V_{in}}{\left|I_{off}+\frac{n_1V_{o1}}{2L_m}DT_s\right|} \\ t_{dt2} &\geq \frac{\left(C_{s1}+C_{s2}\right)V_{in}}{\left|i_p\left(t_c\right)\right|} = \frac{\left(C_{s1}+C_{s2}\right)V_{in}}{\left|I_{off}-\frac{n_2V_{o2}}{2L_m}\left(1-D\right)T_s\right|} \end{aligned} \tag{10}$$

where C_{s1} and C_{s2} are the output capacitance of $S1$ and $S2$, respectively, and $f_{s,max}$ is the maximum switching frequency, $t_{dt1} = t_d - t_c$ and $t_{dt2} = t_g - t_f$ are the first and second dead time of the primary MOSFETs, respectively. From (10), t_{dt} can be reformulated as follows:

$$t_{dt} \geq \frac{2C_sV_{in}}{\min\left\{\left|i_p\left(t_c\right)\right|,\left|i_p\left(t_f\right)\right|\right\}} \tag{11}$$

From (10) to (11), the proposed magnetizing inductance for the ZVS capability can be derived as follows:

$$\begin{aligned} L_m &\leq \frac{t_{dt1}D_{\min}T_sn_1V_{o1}}{2\left(C_sV_{in}-I_{off,\max}t_{dt1}\right)} \\ L_m &\leq \frac{t_{dt2}\left(1-D_{\max}\right)T_sn_2V_{o2}}{2\left(C_sV_{in}-I_{off,\max}t_{dt2}\right)} \end{aligned} \tag{12}$$

From (11) and (12), the proposed magnetizing inductance and dead time duration can be designed for the dual-output LLC resonant converter to obtain ZVS capability of the primary MOSFETs over the entire load condition. These equations consider both the unbalanced magnetizing current and the switching frequency variation to achieve ZVS. Figure 5 shows the comparison of the required magnetizing inductance between the conventional LLC resonant converter and the dual-output converter to achieve ZVS. The dual-output converter requires lower magnetizing inductance for ZVS capability compared to the conventional LLC resonant converter.

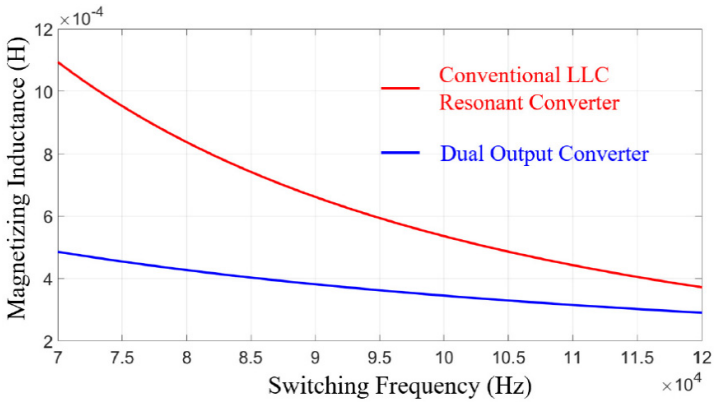


Figure 5. Magnetizing inductance according to the switching frequency for zero voltage switching (ZVS) capability.

3. Analysis of PFM and APWM Hybrid Control Algorithm and Resonant Tank Design

In this section, the operational principle of the hybrid control algorithm is analyzed to regulate output voltages. Through this analysis, the resonant tank is designed to achieve output voltage error compensation.

3.1. Analysis of the Hybrid Control Algorithm

The hybrid control algorithm has two control freedoms using two independent modulation methods. The PFM is adapted to regulate the output voltages using the conventional cross regulation method. In steady state, the conventional multiple output feedback can be derived as follows:

$$k_{w1}V_{o1} + k_{w2}V_{o2} = V_{ref} \tag{13}$$

where k_{w1} and k_{w2} are weight factors and V_{ref} is the reference output voltage. From (13), the output voltage errors using the weight factor can be derived as follows:

$$\begin{aligned} k_{w1}\Delta V_{o1} + k_{w2}\Delta V_{o2} &= 0 \\ V_{o1} &= V_{o1,ref} + k_{w1}\Delta V_{o1} \\ V_{o2} &= V_{o2,ref} + k_{w2}\Delta V_{o2} \end{aligned} \tag{14}$$

where $V_{o1,ref}$ and $V_{o2,ref}$ are the reference voltages of V_{o1} and V_{o2}, and ΔV_{o1} and ΔV_{o2} are output voltage errors of V_{o1} and V_{o2}, respectively. The feedback method for the multiple outputs affects the performance of the cross regulation using the weight factors. As a result, (14) cannot eliminate the output voltage errors which are divided into each output voltage according to the weight factor.

The APWM control method is adopted to regulate V_{o1}, which makes zero steady state voltage errors of the V_{o1} channel. The complementary voltage gain relationship between each output channel also reduces the output voltage error of V_{o2}, as shown in Figure 4b. The decrement of the V_{o1} and V_{o2} error using the APWM can be derived as follows:

$$\begin{aligned} \Delta V_{o1}{}' &= H_{o1}(D)\cdot V_{o1} - V_{o1,ref} \cong 0 \\ \Delta V_{o2}{}' &= H_{o2}(D)\cdot V_{o2} - V_{o2,ref} \end{aligned} \tag{15}$$

where $\Delta V_{o1}'$ and $\Delta V_{o2}'$ are the output voltage errors which are compensated with the APWM control method. The V_{o1} error is almost zero after the APWM control, however, the APWM cannot completely compensate the V_{o2} error. From (15), the output voltages after the APWM regulation can be derived as follows:

$$V_{o1}{}' = V_{o1,ref},\ V_{o2,ref} = V_{o2,ref} - \Delta V_{o2}{}' \tag{16}$$

where V_{o1}' and V_{o2}' are the output voltages of each output channel, which are compensated by the APWM. The flow chart of the hybrid control algorithm is shown in Figure 6 which shows the control sequence of the output voltage regulation to reduce the output voltage errors.

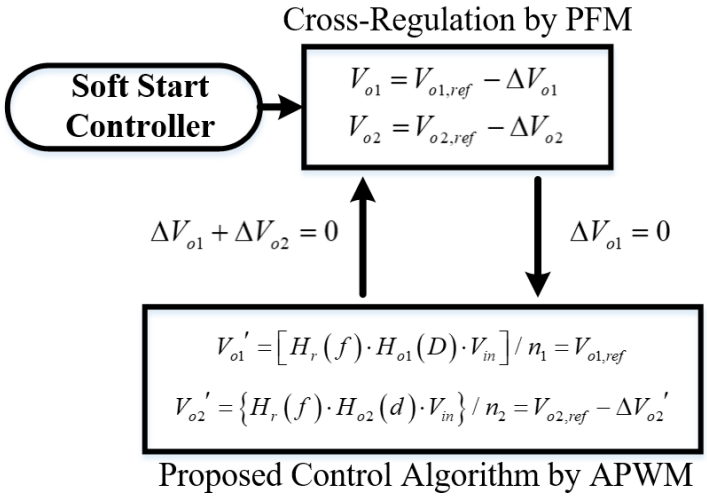


Figure 6. Block diagram of the PFM-APWM hybrid control algorithm.

After the APWM regulation, the cross regulation using the PFM with the feedback for the multiple outputs divides the output voltage error of V_{o2} with respect to the weight factors as follows:

$$\begin{aligned} V_{o1,ref} - \left[H_{o1}(d) H_r(f_{s,c}) V_{in} \right] / n_1 &\cong -k_{w2} \Delta V_{o2}' \\ V_{o2,ref} - \left[H_{o2}(d) H_r(f_{s,c}) V_{in} \right] / n_2 &\cong -k_{w1} \Delta V_{o2}' \end{aligned} \tag{17}$$

where $f_{s,c}$ is the switching frequency which divides the output voltage error according to the weight factor, and $H_r(f_{s,c})$ is the voltage gain of the PFM at the $f_{s,c}$. The voltage gain according to the switching frequency satisfies (13) to divide the output voltage error with respect to the weight factor. From (17), the output voltages regulated by the PFM can be derived as follows:

$$V_{o1}' = V_{o1,ref} - k_{w2} \Delta V_{o2}', \; V_{o2,ref} = V_{o2,ref} + k_{w1} \Delta V_{o2}' \tag{18}$$

where V_{o1}'' and V_{o2}'' are the output voltages of each output channel, which are compensated by the PFM at the next control step. The control iterations of the PFM and the APWM can reduce the output voltage errors of V_{o1} and V_{o2}.

From (15) to (18), the voltage gain variation by the PFM and the APWM can decrease the output voltage error. However, the dual-output converter has limited voltage gain variation caused by the switching frequency and the duty ratio ranges. The proper operating ranges to obtain tightly regulated output voltages can be calculated as follows:

$$\begin{aligned} H_{o1}(d) H_r(f_s) V_1 &= V_{o1,ref} \\ H_{o2}(d) H_r(f_s) V_2 &= V_{o2,ref} \end{aligned} \tag{19}$$

where $V_1 = V_{in}/n_1 - I_{o1}R_{eff}$, $V_2 = V_{in}/n_2 - I_{o2}R_{eff}$, and R_{eff} is the effective series resistance. The voltage gain variation according to the PFM and the APWM has to satisfy (19) for the tight output voltage regulations. Using (19), the required voltage gain of the APWM can be calculated as follows:

$$H_{o1}(d) = \frac{V_{o1,ref} V_2}{V_{o2,ref} V_1} H_{o2}(d) \tag{20}$$

From (20), the APWM control method requires a voltage gain difference between $H_{o1}(d)$ and $H_{o2}(d)$ to reduce the output voltage error. The maximum voltage gain difference range of the APWM can be derived at the worst load condition as follows:

$$\frac{H_{o1}(d)}{H_{o2}(d)} = \max\left(\frac{V_{o1,ref}V_{2,\min}}{V_{o2,ref}V_{1,\max}}, \frac{V_{o1,ref}V_{2,\max}}{V_{o2,ref}V_{1,\min}}\right) \tag{21}$$

where $V_{1,max}$ and $V_{1,min}$ are minimum and maximum output voltages of V_{o1}, respectively, $V_{2,max}$ and $V_{2,min}$ are minimum and maximum output voltages of V_{o2}, respectively. These consider the voltage drop according to the forward bias and conduction loss. Figure 7a shows the maximum voltage gain difference between $H_{o1}(d)$ and $H_{o2}(d)$.

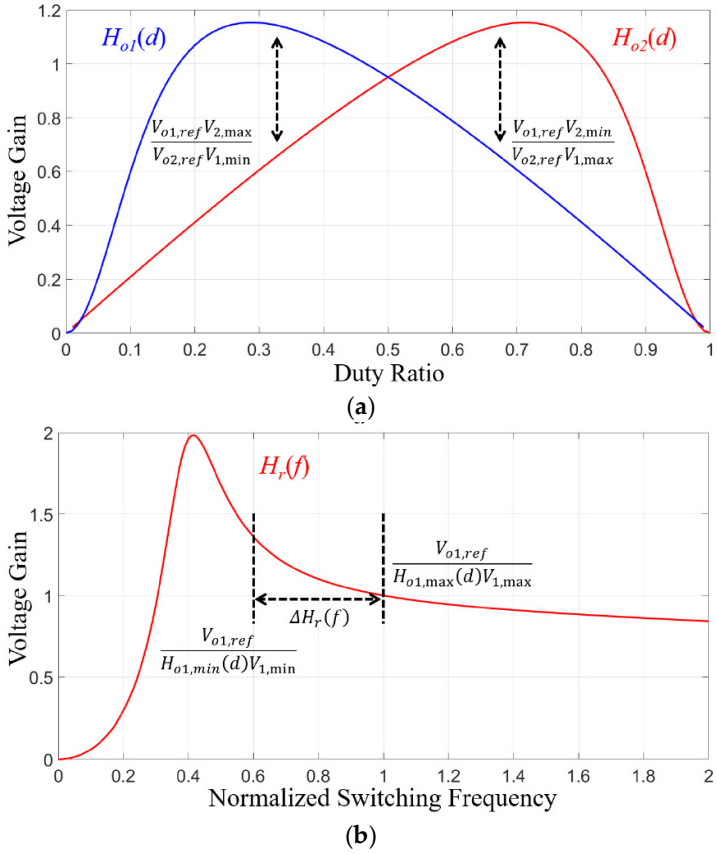


Figure 7. Required minimum and maximum voltage gains: (**a**) APWM case, (**b**) PFM case.

The required voltage gain of the PFM can be obtained for the cross regulation as follows:

$$H_r(f_s) = \frac{V_{o1,ref}}{H_{o1}(d)V_1} \tag{22}$$

From (22), the maximum and minimum voltage gains for the cross regulation can be derived as follows:

$$\begin{aligned} H_{r,\max}(f_s) &= \frac{V_{o1,ref}}{H_{o1,\min}(d)V_{1,\min}} \\ H_{r,\min}(f_s) &= \frac{V_{o1,ref}}{H_{o1,\max}(d)V_{1,\min}} \end{aligned} \tag{23}$$

where $H_{o1,min}(d)$ and $H_{o1,max}(d)$ are the minimum and maximum voltage gains of the APWM, respectively. Figure 7b describes the maximum and the minimum voltage gains to implement the cross regulation method. The resonant tank should be designed to compensate the maximum output voltage difference of the dual-output converter. The voltage gain according to the duty cycle and the switching frequency should satisfy (21) and (23) to compensate the maximum power difference. The

power converter does not require any additional circuits to implement the hybrid control algorithm. Therefore, the power converter size is not affected by the control algorithm.

3.2. Resonant Tank Design for Minimizing Output Voltage Error

The voltage gain using APWM and PFM has to satisfy (21) and (23) for compensation of output voltage error over the entire load range. Figure 8 shows the voltage gain variation according to the resonant inductance and the modulation methods. Large resonant inductance makes monotonic voltage gain variation as switching frequency varies around the resonant frequency. However, the large resonant inductance reduces the compensation range according to the APWM by (8). On the other hand, small resonant inductance can compensate the large output voltage error using the APWM according to (5). However, it induces flat voltage gain variation according to the PFM, which makes large switching frequency variation to obtain the proper voltage gain for minimizing the output voltage error. Therefore, the maximum resonant inductance design is required to achieve small switching frequency variation and output voltage error compensation.

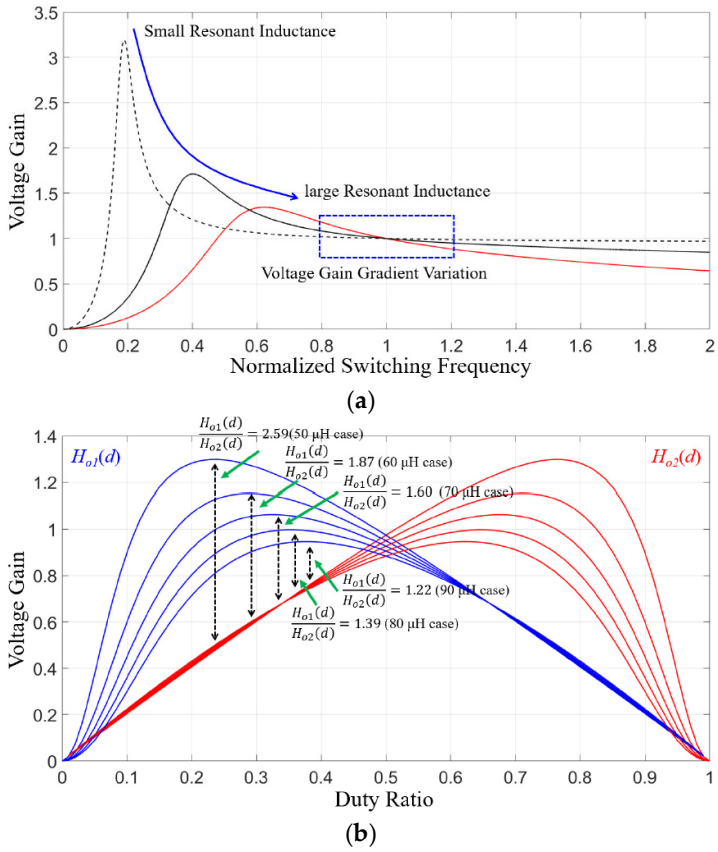


Figure 8. Voltage gain variation according to the resonant inductance: (**a**) PFM case, (**b**) APWM case.

The maximum and minimum output voltages can be calculated with loss analysis. The primary side voltage drop can be calculated as follows:

$$V_{tr} = V_{in} - I_p \left(R_{ds} + R_{tr1} + R_c \right) \tag{24}$$

where V_{tr} is the transfer voltage from the primary to the secondary side, I_p is the primary current, R_{ds} is the on resistance of MOSFET, R_{tr1} is the primary resistance of the transformer, and R_c is the resistance of the resonant capacitor. In addition, the output voltage can be calculated as follows:

$$\begin{aligned} V_{o1} &= V_{tr} / n - V_{D1} - I_{o1} R_{tr2} \\ V_{o2} &= V_{tr} / n - V_{D2} - I_{o2} R_{tr2} \end{aligned} \tag{25}$$

where V_{D1} and V_{D2} are the on-drop voltage of secondary diodes, I_{o1} and I_{o2} are the secondary rms currents of each output channel, and R_{tr2} is the series resistance of the transformer. Table 1 shows the specification of the proposed dual-output LLC resonant converter and its parasitic components.

Table 1. Power stage specifications and design parameters of the dual-output LLC resonant converter.

Parameter	Value	Parameter	Value	Parameter	Value
V_{in}	400 V	Load 1	20 V, 6 A	Load 2	10 V, 7 A
n_{mod}	12	L_m	380 μH	L_r	70 μH
C_r	30 nF	f_r	109 kHz	R_{ds}	330 mΩ
R_{tr1}	300 mΩ	R_{tr2}	130 mΩ	R_c	40 mΩ
$V_{D1,2}$	0.4 V				

From (8), (21) and (25), the resonant impedance (Z_1) can be designed to compensate the output voltage errors for the entire load range. Within the designed duty variation range, the resonant impedance can be derived as follows:

$$\sqrt{\frac{L_r}{C_r}} = \frac{x(D'B)\frac{B}{\omega_r} - (DB')\frac{B'}{\omega_r}}{(DB')C' - x(D'B)C} \tag{26}$$

where x is the maximum voltage gain ratio by (21), $B = 1 - \cos(A)$, $B' = 1 - \cos(A')$, $C = (D/\omega_r)[R' + (D'T_s)/2L_m]\sin(A') + D^2T_sR'$, and $C' = (D'/\omega_r)[R' + (DT_s)/2L_m]\sin(A) + D'^2T_sR'$. From (26), the resonant inductance and capacitance can be calculated to obtain the tight output voltage regulation.

The design methodology of the resonant tank can be described as follows. First, the specifications, such as input voltage range, resonant frequency, and output voltages, are required to design the power stage. Second, the magnetizing inductance is designed by considering the resonant frequency, the input voltage, and the parasitic capacitance of the MOSFETs, which was derived in (12). Third, the resonant inductance and capacitance ratio can be designed using (26). From the loss analysis, the required maximum voltage gain ratio can be calculated using (21), and (25). Through the proposed design methodology, the dual-output LLC resonant converter can achieve tight output voltage regulation and ZVS capability for the entire load conditions.

The example of the power stage design can be described as follows.

Step 1: The design specifications are shown in Table 1.

Step 2: The magnetizing inductance can be calculated with (12). The proper magnetizing inductance is 280 μH to achieve ZVS for the entire load range as shown in Figure 9.

Step 3: The required maximum voltage gain ratio is 1.31 and 0.64, which can be calculated with (21), and (25). The resonant inductance and capacitance can be calculated with (26), which are 70 μH and 30 nF. Therefore, the design example shows resonant impedance and magnetizing inductance to achieve ZVS for the entire load range, which can compensate all voltage errors of all the outputs using the hybrid control algorithm.

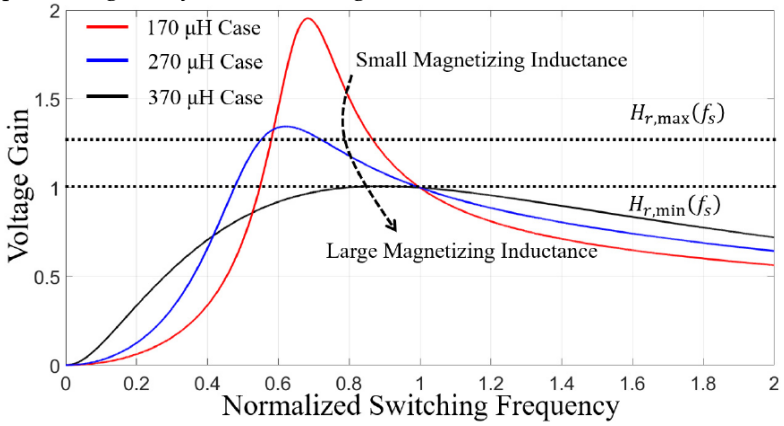


Figure 9. Compensation range of the output voltage error according to the resonant inductance.

4. Experimental Results

Figure 10 shows the simulation result of the PFM-APWM hybrid control method which has the minimum output voltage error, almost zero, according to the load variation. The simulation results verify the performance enhancement of tightly regulated output voltage of the hybrid control algorithm compared to the conventional cross regulation method. Figure 11 shows the prototype converter and diagram of the experimental setup to verify the performance of the proposed hybrid control algorithm. Figure 11a shows a photograph of the prototype converter which has two outputs and a single primary side. Two separated electronic loads are connected to the converter to verify the output voltage regulation performance as shown in Figure 11b.

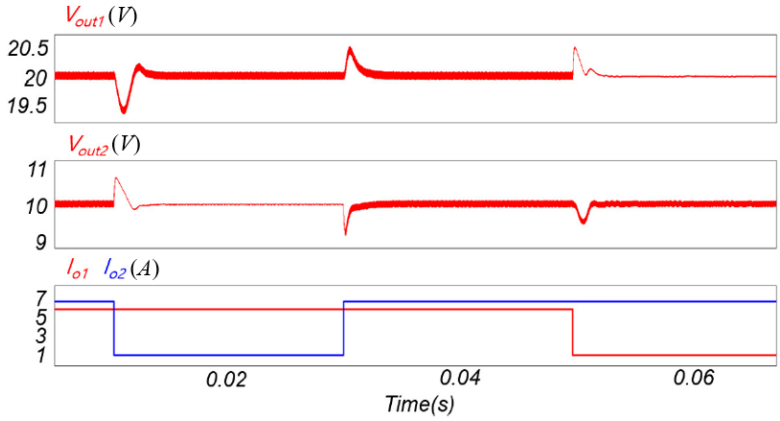
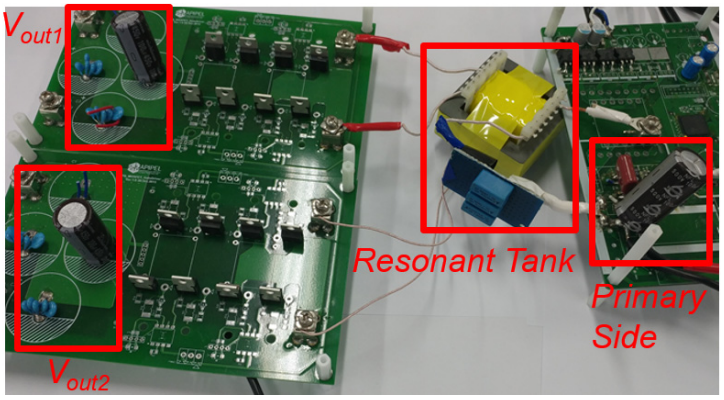
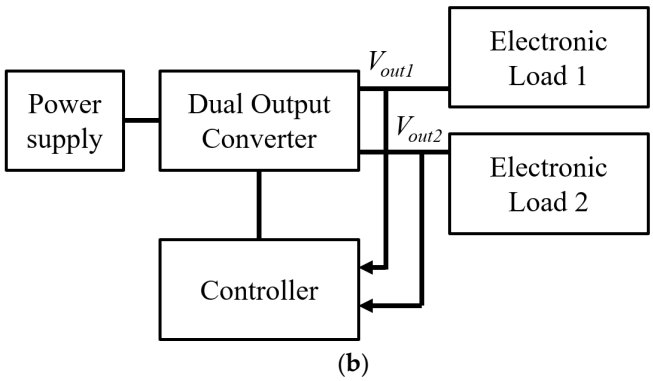


Figure 10. Simulation result using dual-output LLC converter with hybrid control algorithm.



(**a**)



(**b**)

Figure 11. Experimental condition: (**a**) Prototype converter, (**b**) diagram of experimental setup.

The conventional cross regulation method has high output voltage error (6.1% for V_{o1} and 9% for V_{o2}) since its performance is not enough to compensate the output voltage error at the worst load condition. Figure 12 shows experimental waveforms of a prototype dual-output LLC resonant converter using the PFM-APWM hybrid control method at the worst load condition. The proposed control method shows much smaller output voltage error (0.25% for V_{o1} and 0.3% for V_{o2}) than that of the conventional method. It verifies the validity of the proposed design methodology with tight output voltage regulation at the worst load condition. The small voltage error of the hybrid control method might be composed of analog-to-digital conversion (ADC) and measurement errors.

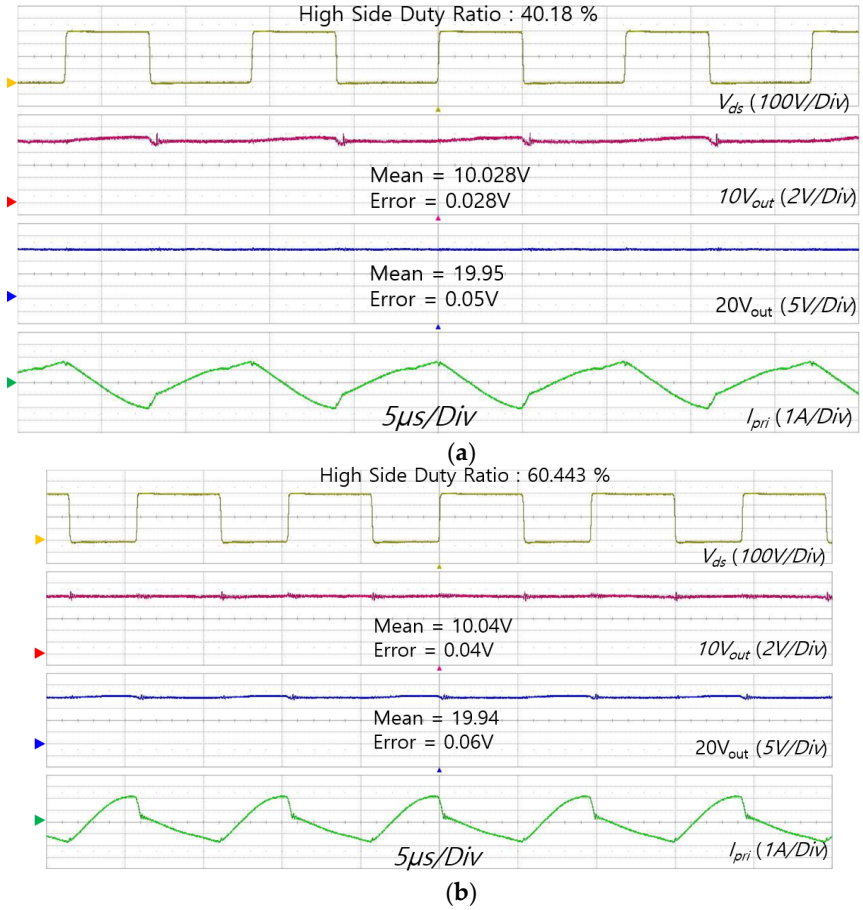


Figure 12. Experimental waveforms of the output voltage regulation with hybrid control algorithm: (**a**) I_{out1} = 1 A and I_{out2} = 7 A, (**b**) I_{out1} = 6 A and I_{out2} = 1 A.

Figure 13 shows the voltage error in cross regulation according to the load variation. In Figure 12, large load difference causes bigger errors of the output voltages. All the detail measured values of the simulation and experimental results are shown in Table 2 which shows the performance comparison of the cross regulation in the output voltages according to the control method. When two output powers are similar, the conventional and hybrid control algorithm has good output voltage regulation performance. When two output powers are significantly different, the conventional control algorithm has poor output voltage regulation. However, the hybrid control algorithm with the proposed design methodology can tightly regulate the output voltage for the entire load difference. The hybrid method shows more than 20 times less voltage regulation errors than those of the conventional simple cross regulation method at the worst condition.

Table 2. Performance comparison by experimental verifications.

	Conventional Cross Regulation	**Proposed Cross Regulation**

k_w Duty	$k_{w1} = 1$ and $k_{w2} = 1$ $D = 1$	$k_{w1} = 1$ and $k_{w2} = 1$ $0.35 < D < 0.65$
Case 1 Error	$I_{out1} = 1$ A and $I_{out2} = 7$ A $V_{out1} = 5\%$ and $V_{out2} = 9\%$	$V_{out1} = 0.25\%$ and $V_{out2} = 0.3\%$
Case 2 Error	$I_{out1} = 6$ A and $I_{out2} = 1$ A $V_{out1} = 6.1\%$ and $V_{out2} = 8.8\%$	$V_{out1} = 0.3\%$ and $V_{out2} = 0.3\%$
Case 3 Error	$I_{out1} = 1$ A and $I_{out2} = 1$ A $V_{out1} = 0.25\%$ and $V_{out2} = 0.34\%$	$V_{out1} = 0.12\%$ and $V_{out2} = 0.18\%$
Case 4 Error	$I_{out1} = 6$ A and $I_{out2} = 7$ A $V_{out1} = 0.41\%$ and $V_{out2} = 0.63\%$	$V_{out1} = 0.1\%$ and $V_{out2} = 0.12\%$

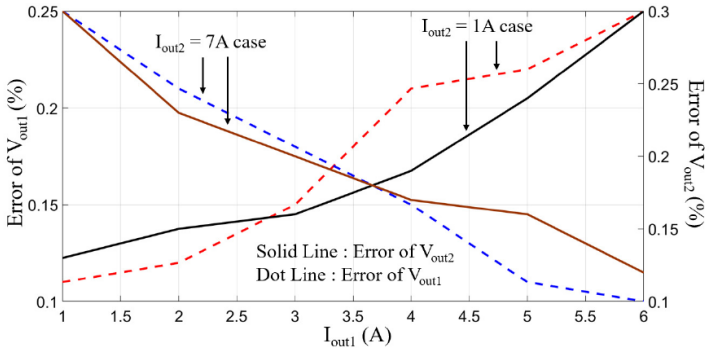
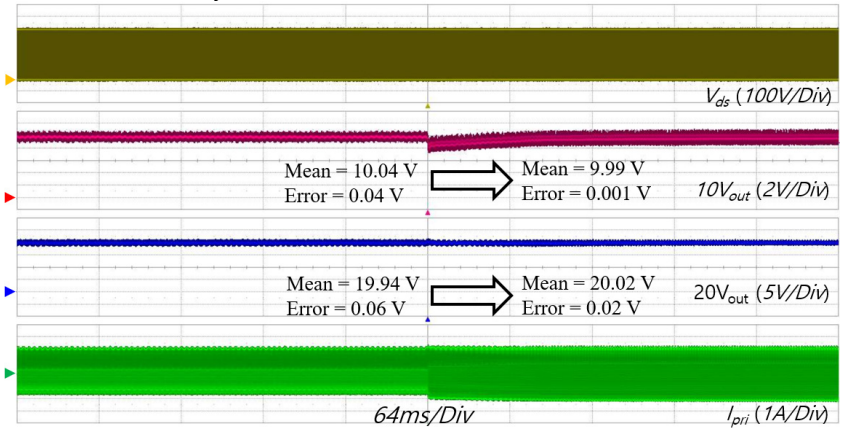
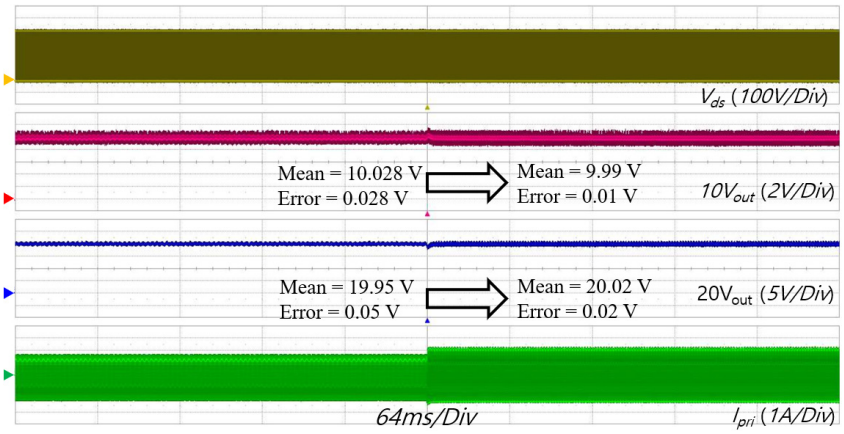


Figure 13. Error of output voltages according to the load variation.

Figure 14 shows the step load response of the prototype dual-output LLC resonant converter using the PFM-APWM hybrid control method which regulates the output voltages under load variations. There are no oscillations and disturbances in the converter operating waveforms. The results indirectly verify operating stability of the dual-output converter controlled by the hybrid control algorithm. Figure 15 shows the step load response of the conventional cross regulation method. The conventional regulation method has poor output voltage regulation according to the load condition. At the worst condition, the output voltage regulation performance is 24 times poorer compared with the hybrid control algorithm. The poor output voltage regulation is shown in Table 2. Figure 16 shows the power conversion efficiency of the prototype converter according to the load variations which show the load change in one output channel when the other is set to a fixed value. The proposed algorithm reduces the offset current on the magnetizing inductance compared with the case of the conventional method. However, the APWM operation induces a higher turn-off loss than that of the conventional method. Figure 16b shows the loss analysis according to the control method. Figure 16a shows the power conversion efficiency between the conventional and proposed methods. The power conversion efficiency is similar between the two control methods.

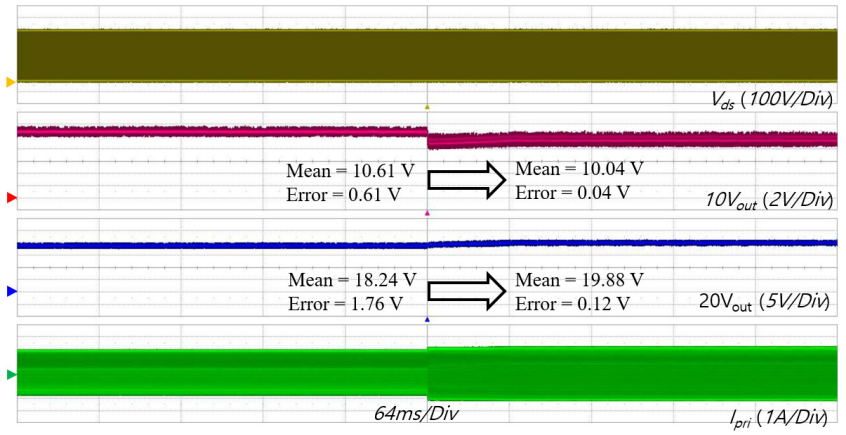


(**a**)

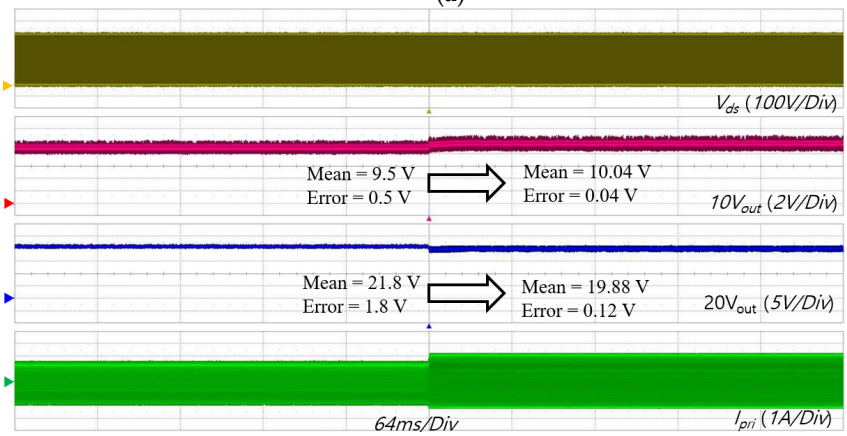


(**b**)

Figure 14. Step load responses of the dual-output converter with hybrid control algorithm: (**a**) I_{out1} = 6 A and I_{out2} changed from 1 A to 7 A, (**b**) I_{out1} changed from 1 A to 6 A and I_{out2} = 7 A.



(**a**)



(**b**)

Figure 15. Step load responses of the dual-output converter with conventional cross regulation method: (**a**) I_{out1} = 6 A and I_{out2} changed from 1 A to 7 A, (**b**) I_{out1} changed from 1 A to 6 A and I_{out2} = 7 A.

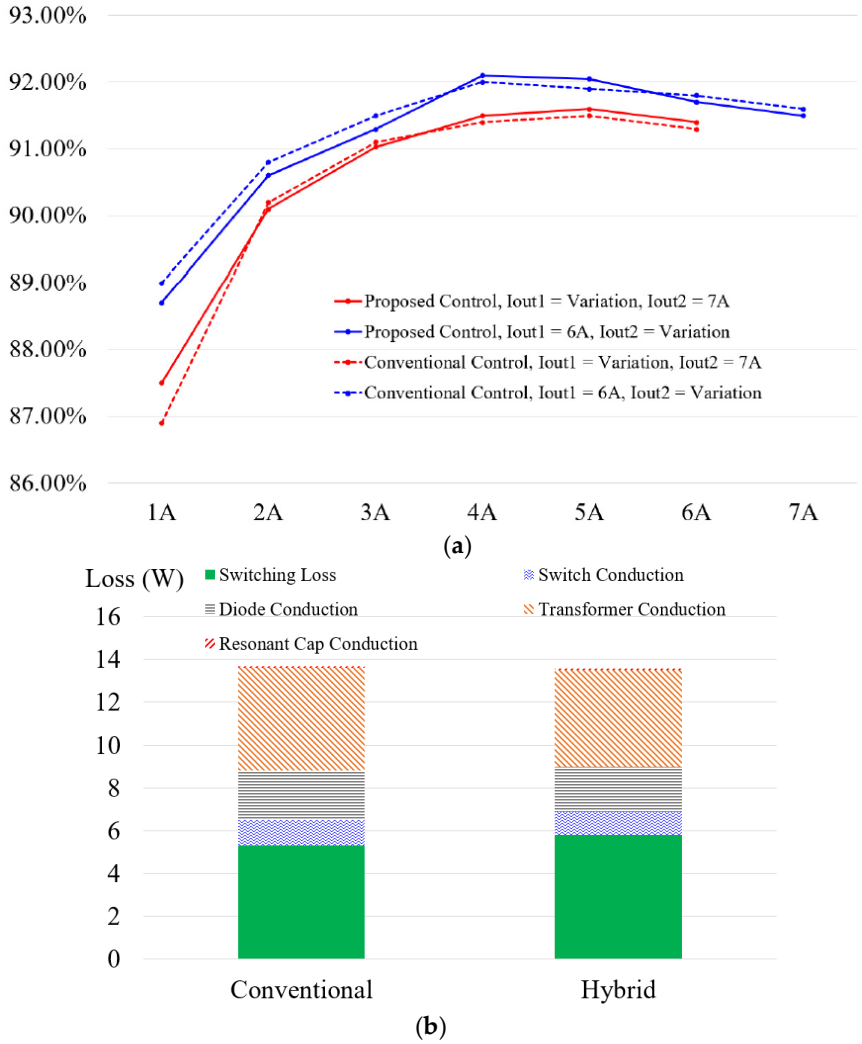


Figure 16. Comparison of power conversion efficiency and loss according to the control algorithm: (**a**) Power conversion efficiency, (**b**) loss analysis.

5. Conclusions

In this paper, the design methodology of a dual-output LLC resonant converter using the PFM-APWM hybrid control method is proposed to obtain tight output voltage regulation and ZVS capability for the entire load conditions. Through the analysis of the operational principle, the magnetizing inductance is designed to obtain ZVS capability. The resonant impedance is designed to implement the tight output voltage regulation for the entire load condition. The simulation and experimental results using the 190 W prototype converter verify the validity of the proposed design methodology, and the hybrid control algorithm. Without any power conversion efficiency degradation, the PFM-APWM hybrid control algorithm reduces the output voltage error to 24.4 times and 30 times smaller than those of the conventional cross regulation method at the worst load condition.

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