Doctoral Thesis

Carrier Transport of Graphene Quantum Device and its Application for Ferroelectric Memory

Sungchul Jung

Department of Physics

Graduate School of UNIST

2019

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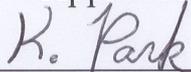
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Carrier Transport of Graphene Quantum Device

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Doctor of Philosophy

Sungchul Jung

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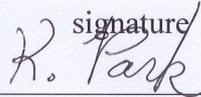
K. Park

Advisor

Kibog Park

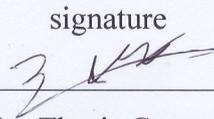# Carrier Transport of Graphene Quantum Device and its Application for Ferroelectric Memory

Sungchul Jung

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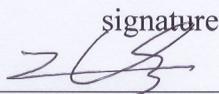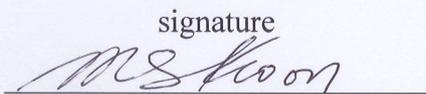
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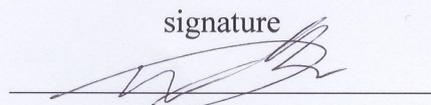
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Abstract

Carrier transport in lateral tunnel junction was studied to apply it for ferroelectric memory devices in theoretical calculations and experimental methods. The edge metal-insulator-metal (EMIM) lateral tunnel junction on ferroelectric layer structure was proven to be a large resistive switching memory device theoretical calculation. The lateral tunnel junction in 2-dimensional material was fabricated with graphene and selectively functionalized graphene. The quantum mechanical tunneling of both 3D and 2D lateral tunnel junction was investigated to apply ferroelectric memory device. Not only the resistive switching memory device, the ferroelectric memory device by using graphene field effect transistor with novel read-out mechanism was studied.

Recently, new memory devices substituting currently used DRAM and flash memory are more actively studied because the memory cell size reaches the physical limits less than 10 nanometer scale. Extreme ultraviolet (EUV) photolithography has been adapted to one of the way for overcoming the scaling issue of memory device. Otherwise, the 3D XPoint nonvolatile memory device has been made by Intel Corp. with higher speed than current NAND flash memory. Based on the electrostatic potential change by ferroelectric layer, we studied the new memory device without selection devices by read-out using two crossing lines.

Theoretical calculation of tunnel current density at EMIM structure on ferroelectric layer shows the ~10^{13} switching ratio between polarization up and down state. The read-out mechanism is applying the half of turn on voltage on word and bit line which is connected to the drain and source electrode in lateral tunnel junction. The writing memory cell can be performed with applying voltages on word, bit, and writing line connected to the bottom of ferroelectric layer. This structure is the basic idea for nonvolatile memory device without selection devices. Based on this research, the lateral tunnel junction in two dimensional materials was studied for memory application. We fabricated graphene/fluorinated-graphene/graphene tunnel junction by using selective insulation of graphene layer after E-beam lithography process. Small gap formed in lateral direction between two graphene electrodes works as a tunnel barrier. The theoretical calculation of thermionic emission current and tunneling current were compared with the current-voltage measurement of fabricated tunnel junction. We confirmed that the graphene lateral tunnel junction can be a good candidate for ferroelectric memory devices. Moreover, we studied that read-out of transconductance of graphene field effect transistor on ferroelectric material can be a new way for defining the memory cell state. Using this method, the series resistance of word and bit line cells connected to read-out cell has no effect during read-out. In case of graphene, the transconductance can be switched from negative to positive depending on the polarization direction of ferroelectric layer due to the energy band structure of graphene. We can also apply this read-out mechanism to 3D tunnel junction even though it has no

dramatic effect than the graphene field effect transistor. However, considering the commercialization of this kind of memory device, the 3D tunnel junction can be more adaptable than the graphene transistor.

Contents

List of Figures

List of Tables

Nomenclature

1T-1C	1 Transistor - 1 Capacitor
AgNW	Silver Nanowire
ALD	Atomic Layer Deposition
BEEM	Ballistic Electron Emission Microscopy
BEES	Ballistic Electron Emission Spectroscopy
BHES	Ballistic Hole Emission Spectroscopy
BST	Barium Strontium Titanate
CNPF	Charge Neutrality Point at Forward Sweeping
CNPR	Charge Neutrality Point at Reverse Sweeping
CSD	Chemical Solution Deposition
CVD	Chemical Vapor Deposition
CW	Continuous Wave
DC	Direct Current
DRAM	Dynamic Random Access Memory
EMIM	Edge Metal-Insulator-Metal
FeRAM	Ferroelectric Random Access Memory
FET	Field Effect Transistor

FG   Fluorinated Graphene

FN Tunneling   Fowler-Nordheim Tunneling

FWHM   Full Width at Half Maximum

GFET   Graphene Field Effect Transistor

GQHE   Graphene Quantum Hall Effect

h-BN   Hexagonal Boron Nitride

HOPG   Highly Oriented Pyrolytic Graphite

IPA   Isopropyl Alcohol

IPE   Internal Photo-Emission

ITO   Indium Tin Oxide

I-V   Current-Voltage

MEMS   Microelectromechanical System

MOCVD   Metal Organic Chemical Vapor Deposition

MOSFET   Metal-Oxide-Semiconductor Field Effect Transistor

MRAM   Magnetoresistive Random Access Memory

NEP   Noise Equivalent Power

OAP   Off-Axis Parabolic

PCM   Phase Change Material

PDMS	Polydimethylsiloxane
PE Hysteresis	Polarization-Electric Field Hysteresis
PECVD	Plasma Enhanced Chemical Vapor Deposition
PLD	Pulsed Laser Deposition
PMMA	Polymethylmethacrylate
PZT	Lead Zirconate Titanate
RF	Radio Frequency
RIE	Reactive Ion Etching
SCCM	Standard Cubic Centimeter per Minute
SEM	Scanning Electron Microscopy
STM	Scanning Tunneling Microscopy
THz	Terahertz
TMA	Trimethylaluminum
TSP	Touch Screen Panel

I. Overview

In this research, the carrier transport characteristics of lateral tunnel junction on a ferroelectric layer was studied for next generation memory device applications. The novel method for forming a lateral tunnel junction by using thin film processes was demonstrated as an application for a ferroelectric memory cell. Based on the study of 3D lateral junction, the 2D lateral tunnel junction formation was also studied by using graphene. The fabricated graphene lateral tunnel junction was investigated by comparing the theoretical model we derived from basic equations. Finally, a possible way for making ferroelectric memory devices utilizing the transconductance of the conventional FET was demonstrated. This method can be applicable to other types of lateral junction or transistor structure.

A brief introduction to graphene and ferroelectric material is described in chapter 2. In this chapter, the principles of nonvolatile memory devices such as magnetoresistive random access memory, phase change material memory, and ferroelectric random access memory are also explained.

In the chapter 3, graphene lateral tunnel junction fabrication processes and its current-voltage characteristics are represented. Instead of conventional wet transfer method, we developed a dry transfer method by using the Kapton tape as a flexible supporting layer to minimize the effect of trapped water molecules during a transfer process. The selective functionalization of graphene as an insulating material was achieved by fluorination process. The lateral graphene/fluorinated-graphene/graphene tunnel junction was fabricated on SiO_2/Si substrate. The current-voltage characteristics of this lateral 2-dimensional tunnel junction was compared with the theoretical value obtained by the thermionic emission current model and tunneling current equation. Resultantly, the energy barrier and the effective thickness of tunnel barrier was estimated.

Chapter 4 demonstrates the edge-metal-insulator-metal (EMIM) tunnel junction on a ferroelectric layer can be a memory cell with two different states depending on the spontaneous polarization direction of the underlying ferroelectric material. The EMIM structure has advantages of forming the tunnel junction in lateral direction and a controllable junction area by film thickness. Therefore, the EMIM junction itself can be applicable to the THz detector by using the nonlinear current-voltage characteristic. The EMIM junction on ferroelectric layer has significantly large switching ratio between two different polarization of ferroelectric.

Finally, in the chapter 5, we tried to fabricate a graphene device on ferroelectric layer as a memory device application. The graphene field effect transistor (GFET) was fabricated on lead zirconate titanate (PZT) substrate for ferroelectric memory device by using the transconductance of GFET. Based on the operating principle of the graphene/ferroelectric memory device, the applications for memory can be realized with various device structures and materials.

II. Introduction

2.1 Characteristics of Graphene

Graphene is a single layer of carbon sheet which can be exfoliated from the graphite. Because of its Dirac cone shape band structure, outstanding carrier mobility and electric field tunable carrier density could be measured in many research results. Moreover, graphene nanoribbon and graphene quantum Hall effect (GQHE) has been studied for quantum mechanical phenomena of two-dimensional electron system. In this chapter, the characteristics of graphene are discussed based on the energy band structure of graphene and the examples of excellent electrical properties are introduced.

2.1.1 Crystal Structure and Energy Band of Graphene

Graphene is atomically thin carbon sheet that has been noticed by K. S. Novoselov and A. K. Geim from 2004 [1]. In their experiment, monolayer graphene is prepared by the repeated peeling of the highly oriented pyrolytic graphite (HOPG). Graphene has a hexagonal honeycomb lattice structure composed of carbon. As shown in Fig. 2.1a, the lattice constant (a_0) which is the length of carbon-carbon (C-C) bonding of graphene is 0.14 nm [2]. Since the arrangement of carbon atoms doesn't have perfect periodicity, a unit cell should be defined like red parallelogram in Fig. 2.1a. The unit cell contains two adjacent carbon atoms as a basis and is repeated with unit vector $\vec{a_1}$ and $\vec{a_2}$.

$$\vec{a_1} = \frac{a_0}{2}\left(3, \sqrt{3}\right), \ \vec{a_2} = \frac{a_0}{2}\left(3, -\sqrt{3}\right) \tag{2.1}$$

Starting from the crystal structure, we can convert the real space to k-space represented by the reciprocal lattice vectors. The reciprocal lattice vector should satisfy the relation like below.

$$\vec{a_i} \cdot \vec{b_j} = 2\pi\delta_{ij} \ (i, j = 1 \text{ or } 2) \tag{2.2}$$

Here, δ_{ij} is the Kronecker delta and b_j is the reciprocal lattice vector. The reciprocal lattice vector of graphene is calculated with the Eq. 2.2.

$$\vec{b_1} = \frac{2\pi}{3a_0}\left(1, \sqrt{3}\right), \ \vec{b_2} = \frac{2\pi}{3a_0}\left(1, -\sqrt{3}\right) \tag{2.3}$$

The reciprocal lattice can be drawn with lattice constant $b_0 = 4\pi/3a_0$. The reciprocal lattice is shown in Fig. 2.1b. The first Brillouin zone is the Wigner-Seitz primitive cell of reciprocal lattice [3]. The green parallelogram in Fig. 1b represents the first Brillouin zone bisecting the lines connecting to the nearest neighbors.

After defining the reciprocal lattice, the energy band structure of graphene can be derived by using

tight binding method. The tight binding model considers only the nearest neighbors because the wave functions are assumed to be well localized in each lattice points. The number of nearest neighbors in graphene lattice structure is 3 as shown in Fig. 2.2a. The translation vectors for nearest neighbors are $\vec{\delta_1}$, $\vec{\delta_2}$, and $\vec{\delta_3}$. The energy equation for a tight binding model is expressed by the Eq. 2.4 [3].

$$E = E_0 - \beta - \gamma \sum_{\vec{R}} \exp\left(i\vec{k} \cdot \vec{R}\right) \tag{2.4}$$

The E_0 represents the bound energy for an atom, β the correction for periodic potential, γ the correction for nearest neighbors, $\vec{k}$ the wave vector, and $\vec{R}$ the translation vectors. The calculated energy dispersion relation of graphene is,

$$
\begin{aligned}
E &= E_0 - \beta - \gamma \left[\exp\left(-ik_x a_0\right) + \exp\left(i\frac{k_x a_0}{2} + i\frac{\sqrt{3}k_y a_0}{2} \right) + \exp\left(i\frac{k_x a_0}{2} - i\frac{\sqrt{3}k_y a_0}{2} \right) \right] \\
&= E_0 - \beta - \gamma \cdot \exp\left(-ik_x a_0\right) \cdot \left[1 + 2\cos\left(\frac{\sqrt{3}k_y a_0}{2} \right) \cdot \exp\left(i\frac{3k_x a_0}{2} \right) \right]
\end{aligned}
\tag{2.5}
$$

Based on the Eq. 2.5, the energy gap (ΔE) is calculated with the magnitude of the last term.

$$
\begin{aligned}
\Delta E &= \pm\gamma \sqrt{ \left(1 + 2\cos\left(\frac{\sqrt{3}k_y a_0}{2} \right) \cdot \exp\left(i\frac{3k_x a_0}{2} \right) \right) \cdot \left(1 + 2\cos\left(\frac{\sqrt{3}k_y a_0}{2} \right) \cdot \exp\left(-i\frac{3k_x a_0}{2} \right) \right) } \\
&= \pm\gamma \sqrt{ 1 + 4\cos^2\left(\frac{\sqrt{3}k_y a_0}{2} \right) + 4\cos\left(\frac{\sqrt{3}k_y a_0}{2} \right)\cos\left(\frac{3k_x a_0}{2} \right) }
\end{aligned}
\tag{2.6}
$$

Here, the zero energy gap ($\Delta E = 0$) occurs when $\cos\left(\frac{3k_x a_0}{2} \right) = 1$ and $\cos\left(\frac{\sqrt{3}k_y a_0}{2} \right) = -\frac{1}{2}$ or

$\cos\left(\frac{3k_x a_0}{2} \right) = -1$ and $\cos\left(\frac{\sqrt{3}k_y a_0}{2} \right) = \frac{1}{2}$. For both cases, the wave vector $\vec{k}$ lying on the first

Brillouin zone should be located on the vertices. The red circles in Fig. 2.2b satisfy the first condition and the blue circles are the positions of the second case. Based on the energy dispersion relation, the energy band diagram of monolayer graphene was derived and expressed as in Fig. 2.3 [4].

a
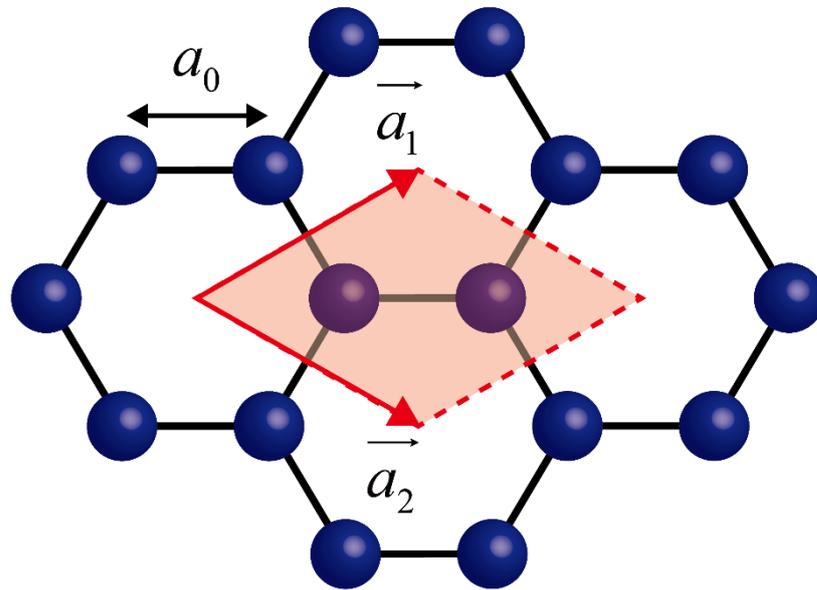
b
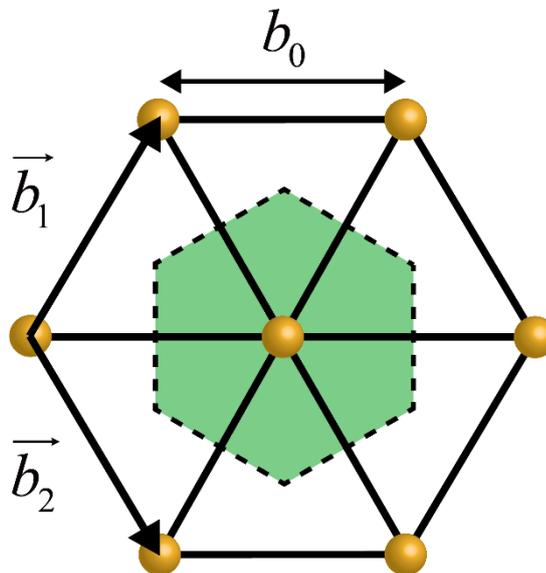
Figure 2.1 (a) Graphene crystal lattice structure with lattice constant a_0. Red parallelogram represents basis, blue circles are carbon atoms, and unit vectors are $\vec{a_1}$ and $\vec{a_2}$. (b) Reciprocal lattice structure with lattice constant b_0. Green parallelogram is first Brillouin zone and the reciprocal lattice vectors are $\vec{b_1}$ and $\vec{b_2}$.
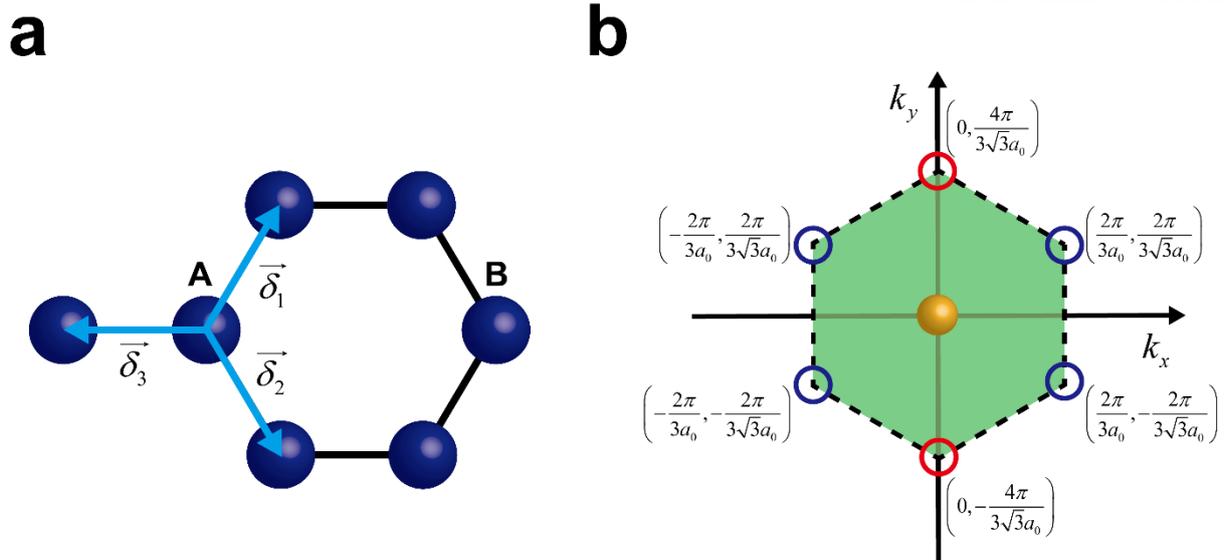
Figure 2.2 (a) Lattice vectors for nearest neighbor. A and B sites have different nearest neighbor lattice vectors. (b) The coordinates of the first Brillouin zone vertices in k-space.
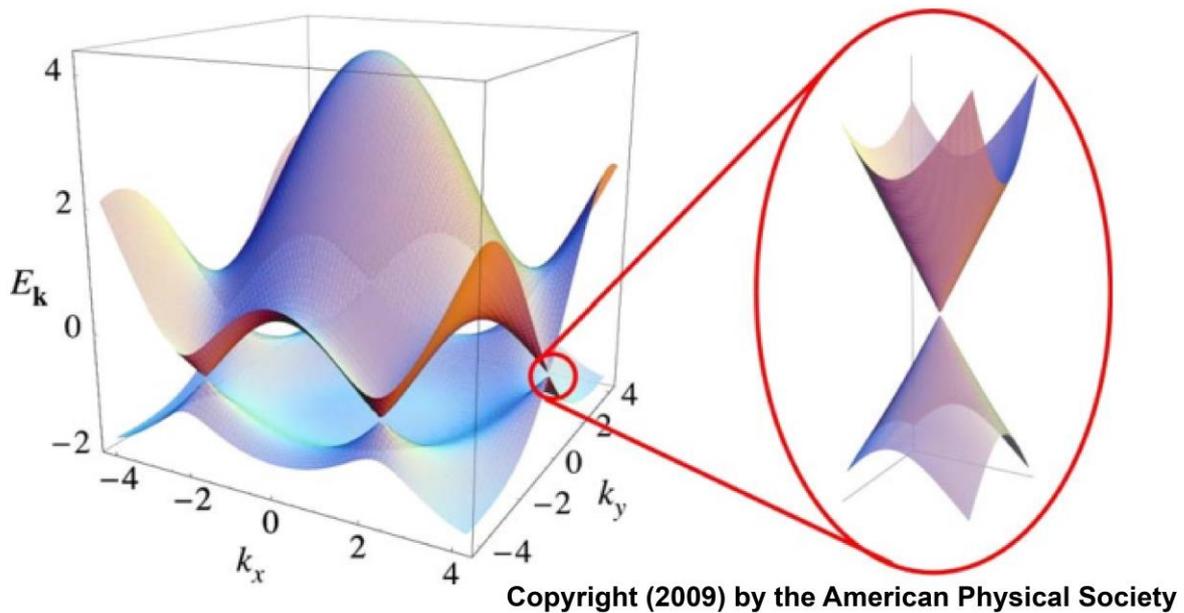
Figure 2.3 Energy dispersion relation of graphene and zoom-in at Dirac point [4].

2.1.2 Electrical Properties of Graphene

As described in the previous chapter, graphene has Dirac cone shape energy band structure. The electrical properties of graphene are much influenced by its energy band structure. Since the curvature of the energy band is related to the effective mass of the particle, graphene has theoretically zero effective mass [4] and an extremely high carrier mobility ($\sim 100,000\ cm^2/V \cdot s$) [5, 6] at room temperature. Moreover, due to the gapless semimetal band structure, the Fermi level and its carrier type can be tunable by an external electric field [7, 8]. Lastly, graphene is two-dimensional material possible to measure the quantum Hall effect [9-11].

Much of researches have been conducted for a graphene field effect transistor (FET) as a substitution of silicon-based FETs because of its extremely high mobility [8, 12, 13]. However, due to the gapless band structure, graphene FET (GFET) is not fully off, which means that the leakage current at off state is very large. Although the limitation of GFET as a candidate for substituting the Si-FET, its structure can be also applied to THz detectors [14-16]. Furthermore, graphene p-n junction can be formed electrostatically utilizing the tunable graphene Fermi level [17, 18]. As follows, the superior graphene's electrical properties have been applied in many research areas and could be applicable to new fields in the future.

2.2 Characteristics of Ferroelectric Material

Ferroelectricity was first found in Rochelle salt ($NaKC_4H_4O_6$) with very low Curie point, weak ferroelectricity, and poor stability [19, 20]. After this first discovery of ferroelectricity, the perovskite structure was found as a ferroelectric material by its spontaneous polarization from the displacement of atom. The ferroelectric materials such as $BaTiO_3$, $PbTiO_3$, lead zirconate tintanate (PZT), and barium strontium titanate (BST) have been studied for using dielectric material in capacitor, microelectromechanical system (MEMS), or memory devices [20]. Chapter 2 describes the ferroelectric material and its application for memory devices. In the end of chapter, other types of new memory devices and their working principles are explained to compare the ferroelectric memory device.

2.2.1 Spontaneous Polarization of Ferroelectric Material

Ferroelectric material has its spontaneous electric polarization without any external electric field. Generally, a perovskite structure is representative structure for ferroelectric material. The spontaneous polarization of ferroelectric comes from the displacement of center atoms in perovskite structure as depicted in Fig. 2.4 [21]. In this figure, the double well potential is shown in the energy-displacement curve and the energy minima are formed at points slightly displaced from the center. Therefore, the ferroelectric material is more stable when the center atom is deviated upward or downward having lowest energy [21, 22].

The basic material properties of ferroelectric film can be measured by using polarization-electric field hysteresis (PE hysteresis) curve. Generally, the ferroelectric material has hysteresis on electric field because it has the two stable polarized states as described in previous paragraph. The PE hysteresis curve provides remnant polarization (P_r), saturation polarization (P_s), and coercive field (E_c) as shown in Fig. 2.5. Initially, the polarization direction of each cell may be randomly arranged, and the overall polarization direction of ferroelectric material can be 0. When an external electric field larger than E_c is applied, the polarization directions of ferroelectric cells are aligned in the same direction as the applied field. Here, the minimum electric field required to align the polarization of ferroelectric material is defined to be coercive field (E_c). As the electric field becomes stronger, the polarization value is saturated at P_s. After applying an external electric field bigger than E_c, the ferroelectric film has a polarization of P_r since the polarization direction of each cells are already aligned in one direction. In short, the ferroelectric materials have remnant polarization (P_r) after applying the external electric field larger than the coercive field (E_c).
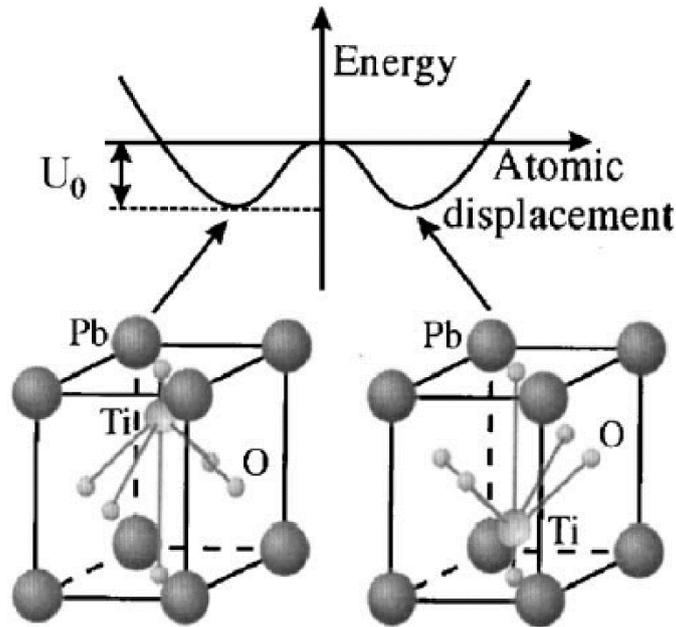
Figure 2.4 Schematic crystal structure of $Pb(Zr_{0.2}Ti_{0.8}O_3)$ with two degenerate ground states and its energy-atomic displacement diagram [21].
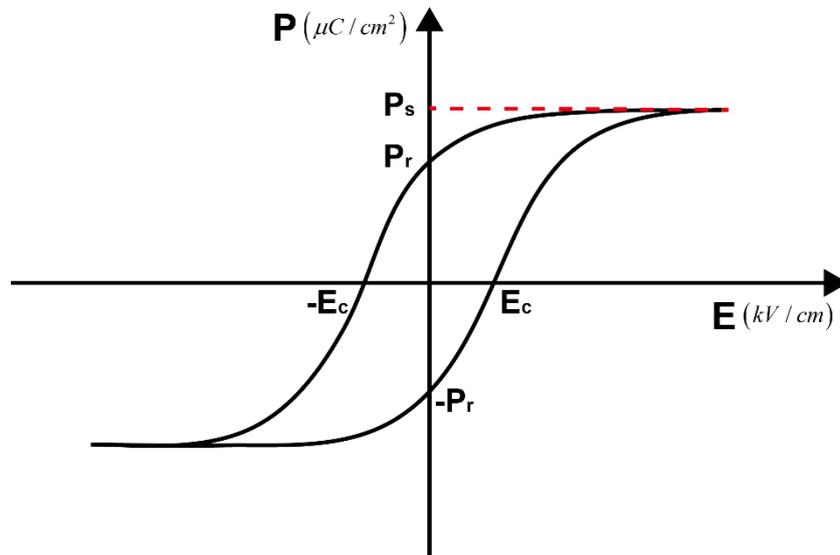
Figure 2.5 PE hysteresis curve of ferroelectric material. P_r represents remnant polarization, P_s the saturation polarization, and E_c the coercive field.

2.2.2 Formation of Ferroelectric Film

Ferroelectric films can be grown by using various methods such as CSD (Chemical Solution Deposition), MOCVD (Metal Organic Chemical Vapor Deposition), ALD (Atomic Layered Deposition), Sputtering, and PLD (Pulsed Laser Deposition) [23]. Depending on the synthesis method, the properties of films are determined as shown in the Table 2.1 [23]. In the CSD method, so called sol-gel method, the ferroelectric solution is spin-coated on the substrate and heated to crystallize. Much of ferroelectric films with perovskite structure, particularly PZT, have been grown by the sol-gel method because of its simplicity in the experiments [23-25]. The MOCVD method is another chemical synthesis of ferroelectric material using the liquid source [26, 27]. The ALD also has been used for depositing ferroelectric films with high uniformity and surface morphology [28, 29]. The film growth using sputtering or PLD is the physical deposition method by depositing the solid source target [30-33].

Table 2.1 Comparison of synthesis methods for ferroelectric films [23]

Characterization	Synthesis methods				
	CSD (sol-gel)	MOCVD	Sputtering	PLD	ALD
Stoichiometric ratio	better	better	ordinary	good	better
Doping difficulties	easy	easy	hard	hard	easy
Precursor obtained	easy	easy	easier	easier	ordinary
Adhesion to substrates	good	good	better	good	better
Growth rate	low	high	high	high	lower
Epitaxial ability	strong	weak	strong	stronger	strongest
Uniformity	better	better	good	good	best
Thickness control	hard	easy	easy	easy	best
Surface morphology	ordinary	better	good	good	best
Repeatability	better	better	ordinary	good	better
Suitable for large-scare preparation	ordinarily	better	good	no	better
Compatibility for heterostructures/ superlattices formation	ordinary	good	good	better	best
Applicability in ferroelectric film preparation	Almost suitable for all of the perovskite compounds	Not suitable for films containing elements with high atomic number such as Ba,Sr, Bi, Pb, etc.	Restrict to compounds containing volatile heavy elements like PZT	Almost suitable for all of the perovskite compounds besides those cannot be fabricated into PLD targets	Suitable precursors and substrates with appropriate chemical properties are needed for surface chemisorptions

2.3 Nonvolatile Memory

2.3.1 Ferroelectric Random Access Memory (FeRAM)

Ferroelectric material is attractive for application to memory devices due to its spontaneous polarization [34-37]. Since the polarization of ferroelectric film forms electric field in a specific direction, the electric field tunable devices near the ferroelectric can have two stable states with different electrical characteristics. Moreover, the ferroelectric memory device is nonvolatile meaning that the memory state is remained without electrical power supply. Furthermore, the programming and reading time of FeRAM is few tens of nanoseconds which is much faster than the NAND or NOR flash memories [38]. Therefore, FeRAM has been studied as a future nonvolatile memory because of its low power consumption and fast operation speed [38-42].

The structure of the FeRAM can be divided into a 1T-1C (1 Transistor-1 Capacitor) structure used in DRAM (Dynamic Random Access Memory) and a 1T structure like a floating gate transistor as shown in Fig. 2.6. In the 1T-1C structure, the dielectric material in conventional DRAM is substituted by the ferroelectric material. Thus, the memory cell should be rewritten after the reading mechanism due to the destructive read-out. Meanwhile, the 1T FeRAM is floating gate transistor structure just replacing the floating gate and oxide film with a ferroelectric film. Programming the memory cell can be achieved by applying coercive voltage across the ferroelectric film using word and bit lines. The ferroelectric of programmed cell has spontaneous polarization in specific direction and generates the electric field on the channel of transistor. In result, the transistor has different turn-on voltage depending on the polarization direction of ferroelectric layer. With this structure, the FeRAM can perform non-destructive read-out unless the operating voltage across the ferroelectric layer during read-out need to be exceed the coercive voltage. However, it has limitation for low integration density and high cost compared to the currently widely used flash memories.

(a)

(b)
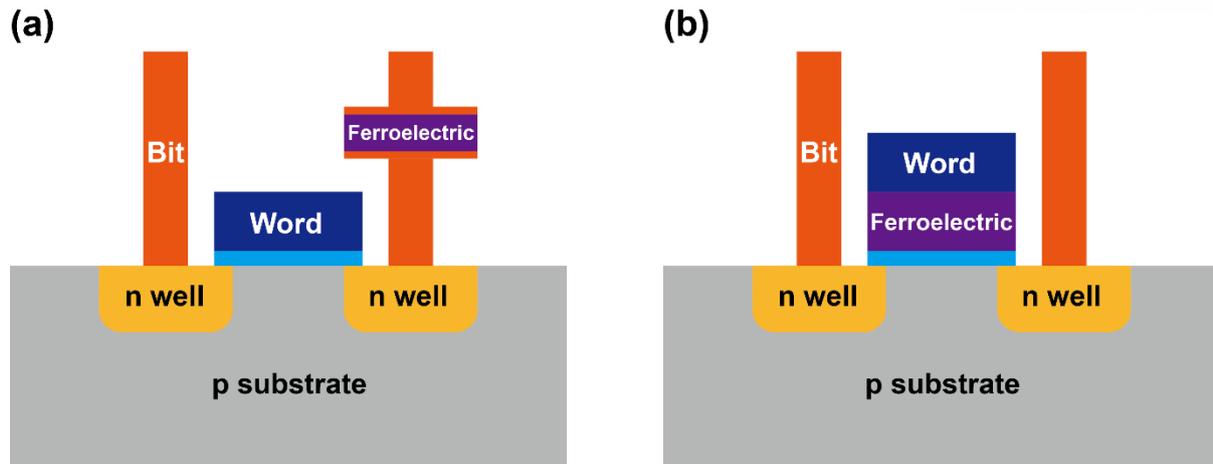
Figure 2.6 FeRAM with (a) 1T-1C (1 Transistor, 1 Capacitor) structure and (b) 1T (1 Transistor) structure.

2.3.2 Other Types of Memory

In addition to the FeRAM described in the previous section, researches for nonvolatile memory have been studied with a variety of materials and structures [38, 40, 43-45]. Magnetoresistive random access memory (MRAM) is one of the promising candidates for new memory devices. Similar to FeRAM using ferroelectric materials, MRAM is a memory device utilizing ferromagnetic materials [46, 47]. The ferromagnetic material changes its magnetization by an external magnetic field and preserve the state until an opposite magnetic coercive field is applied. In order to operate the MRAM, a magnetic field should be applied, which can be realized by the magnetic field inducing electric circuits. In case of MRAM, the read-out can be performed by measuring the tunnel current through the tunnel barrier between two ferromagnetic layers. One of the ferromagnetic layers adjacent to the antiferromagnetic material has fixed magnetization direction and the other layer changes its magnetization direction by the external magnetic field. Thus, the spin-polarized electron has different tunneling probability depending on the combination of two polarization directions of ferromagnetic. However, there is a limitation for scaling because the induced magnetic field during programming the specific memory cell can change the magnetization direction of neighboring memory cells [38]. As shown in Fig. 2.7, spin transfer torque (STT) MRAM was proposed to overcome this scaling issue [48, 49]. Using this technique, the magnetization direction can be switched by the current through the ferromagnetic layer. Therefore, the STT MRAM is one of the leading technologies for a new type of memory device.

The phase change material (PCM) has been studied as a nonvolatile memory using its two states, amorphous and crystalline [50]. As shown in Fig. 2.8, the PCM is initially crystalline structure in PCM memory [50]. When PCM is dissolved by strong heat, it becomes an amorphous state and its electrical conductivity drops sharply compared to the crystalline state. The amorphous state is commonly reset state. Here, the heating mechanism is just flowing the current through the PCM and utilizing the joule heating. On the other hand, the crystalline state can be achieved by heating the PCM with mediate heat for a longer time than programming the reset state as depicted in Fig. 2.8 and 2.9 [50]. The required voltages for read-out, set state, and reset state are different each other considering the phase change. In short, PCM memory also have two stable states with fast read/write speed and is being studied for next generation memory devices [51-54].

a

b
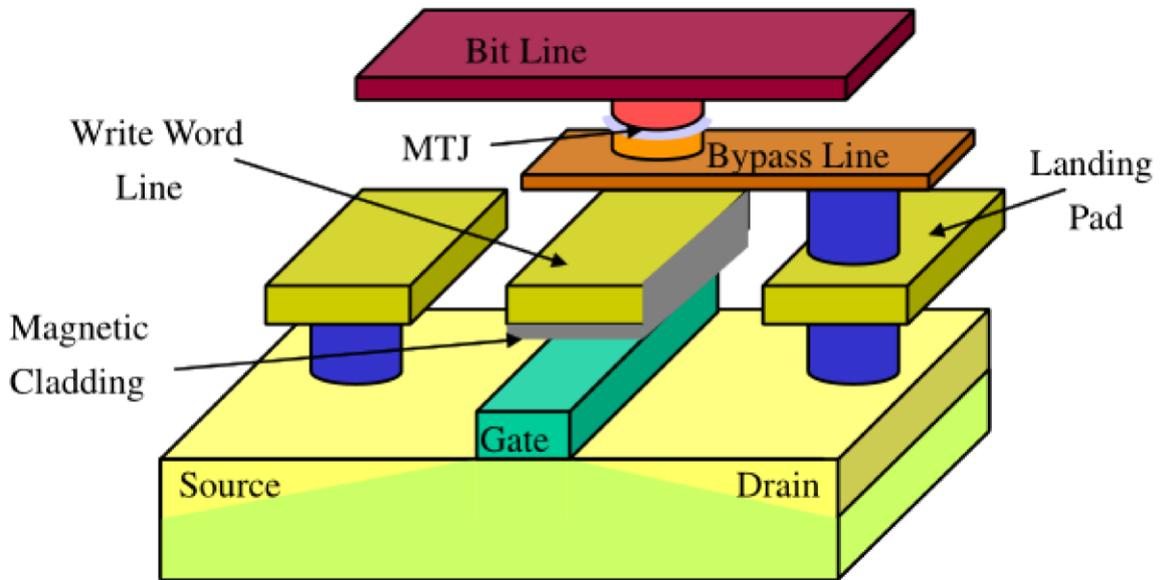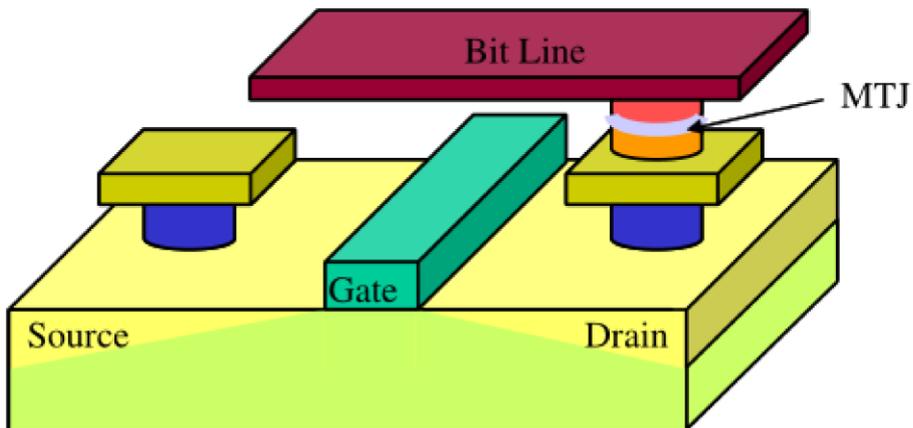
Figure 2.7 Memory architecture of (a) conventional toggle field-switched MRAM and (b) spin transfer torque (STT) MRAM [49].

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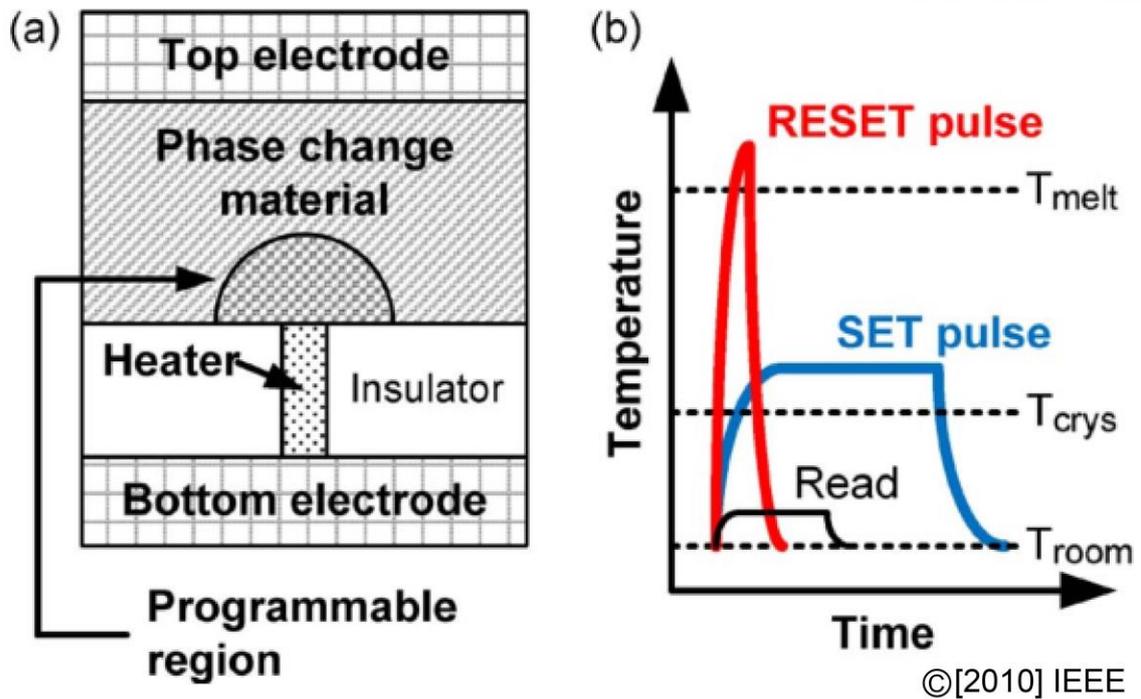
Figure 2.8 (a) PCM memory cell structure (b) Operating voltage pulse time and temperature for reading and writing (RESET pulse and SET pulse) [50].
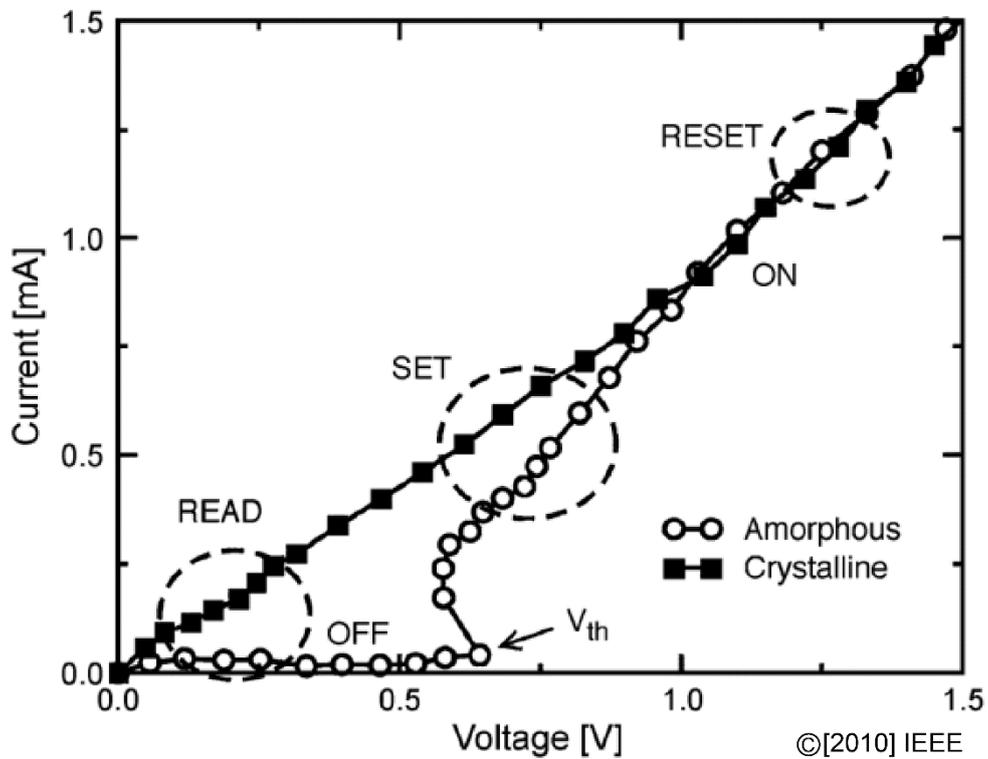
Figure 2.9 Current-voltage characteristics of PCM. The read, set, and reset region has different voltage range [50].

III.   Graphene Lateral Tunnel Junction

3.1 CVD Graphene Dry Transfer

3.1.1 Graphene Dry Transfer

The mechanically exfoliated graphene has much better electrical properties than CVD (Chemical Vapor Deposition) or epitaxially grown graphene [5-8, 55]. However, CVD graphene has advantage of transferring on the wanted position in large scale. Thus, considering the mass production of graphene devices, CVD graphene is more competitive in fabrication processes.

Generally, CVD-grown graphene on Cu foil is transferred on the substrate by using PMMA (Polymethyl methacrylate)-assisted wet transfer method. The spin-coated PMMA on graphene can supports the graphene layer even after the Cu foil is etched. The PMMA/graphene stack should be floated on a liquid (etchant or distilled water) because it is very thin and prone to tearing. This is the main reason for transferring CVD graphene into a wet process. However, in the wet transfer process, water molecules can be inevitably trapped under the graphene layer and a water-sensitive substrate cannot be used. Because the trapped water molecules can interfere measuring the pristine graphene properties [56, 57], dry transfer method has been studied to overcome the limitation of wet transfer method by reducing water molecules attached under the graphene layer [58-61].

Dry transfer of graphene should have stronger supporting layer to be controllable in the air. Several studies for dry transfer method to minimize the trapped water molecules have been performed using the PDMS (polydimethylsiloxane) or metal frame sample holders [58-61].

3.1.2 Dry Transfer with Flexible Supporting Layer

In our experiment, keeping the whole processes of PMMA-assisted wet transfer method, flexible supporting layer is additionally attached to the PMMA/graphene stack. As shown in Fig. 3.1, the transfer processes of wet and dry transfer method are depicted. In the first step, graphene on Cu foil is spin coated with PMMA (495 A2, MicroChem) at 5000 rpm for 60 seconds. Next, the graphene forming on the opposite side of the PMMA-coated graphene is etched in the reactive ion etching system (TTL Korea) with oxygen plasma (20 W, 60 seconds). After etching the backside graphene, there is an additional step in the dry transfer method. The Kapton tape is attached to top of the PMMA/graphene/Cu foil stack as a flexible supporting layer. Then, the Cu foil is etched by using ammonium persulfate (Sigma Aldrich). Several studies have proven that the ammonium persulfate provide cleaner graphene layer after etching Cu than using the $FeCl_3$ [62, 63]. After chemical etching process, the graphene is rinsed by using

distilled water several times to remove chemicals. In case of the wet transfer method, the floated PMMA/graphene stack should be handled with the glass to transfer it from one bath to other one. However, in case of the dry transfer method, Katpon tape/PMMA/graphene stack can be dealt with the tweezer in the air. With this advantage, before transferring the graphene on the substrate, the N_2 blowing and heating process (70 °C for 15 minutes) are preceded to eliminate the water molecules. However,

differently from the conventional wet transfer method, the Kapton tape/PMMA/graphene stack doesn't settle down to the substrate naturally due to the rigidity of Kapton tape. In this experiment, we found one of the way to transfer the graphene evenly on the substrate. After locating the Katpon tape/PMMA/graphene stack on the substrate, the N_2 is blown to the center of the sample for the uniform attachment without generation of bubbles. Although the wet transferred sample is tilted to drain off the water molecules captured between the substrate and graphene layer, much of them are still remained.

Then, both wet and dry transferred samples are heated on the hot plate (150 °C for 15 minutes) for

better adhesion of graphene and substrate. Next, they are dipped into the acetone to remove PMMA. The Kapton tape is also automatically detached from the substrate because the PMMA acting as an interlayer is vanished. Finally, they are rinsed with IPA (isopropyl alcohol) and heated on the hot plate (200 °C for 15 minutes) to evaporate any residual solvents on the graphene.
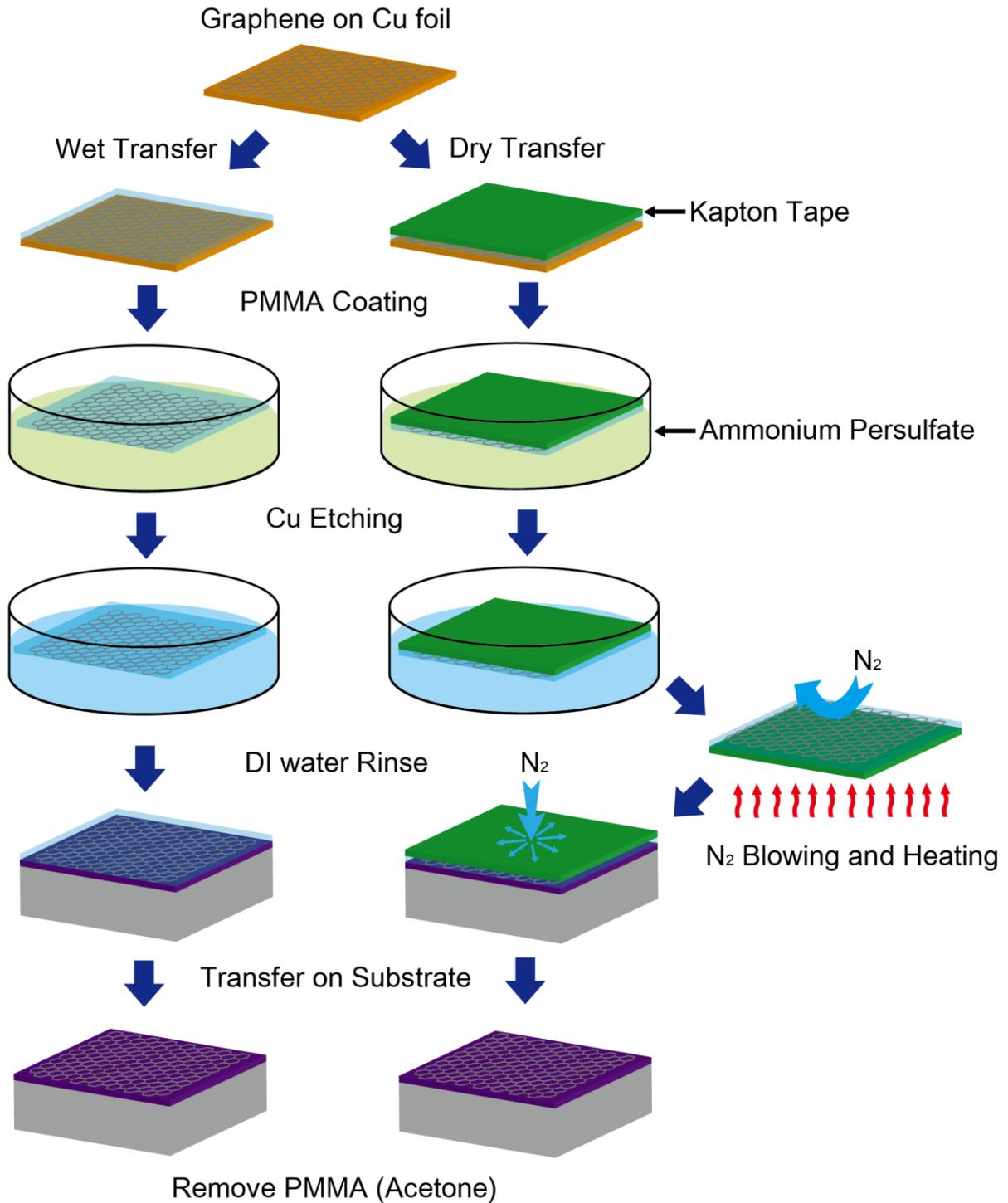
Figure 3.1 Transfer process of wet and dry method. The N_2 blowing and heating process is included to vaporize the water molecules before transferring graphene. During dry transfer process, N_2 is blown to the center of Kapton tape/PMMA/graphene stack for uniform transfer of graphene on the substrate without wrinkles. [*Submitted*]

Figure 3.2 is the Raman spectra (alpha 300R, WITec, Germany) of wet and dry transferred graphene on SiO_2/Si substrate. The inset graph in Fig. 3.2 magnifies the 2D peaks for both wet and dry transferred graphene. Typically, monolayer graphene has 2D/G peak ratio greater than 2 and the FWHM (Full Width at Half Maximum) about 30 cm^{-1} [64, 65]. The Raman spectrum of wet transferred graphene (black spectrum) shows about 2.5 of 2D/G ratio and 31 cm^{-1} of FWHM. The relative intensity of D peak is very small compared to the 2D peak indicating that the defect density of graphene is very low, and the grain size is relatively large. In case of the dry transferred graphene, 2D/G ratio is ~4.1, FWHM is ~32 cm^{-1}, and D peak is very little. Therefore, both wet and dry transferred graphene are confirmed to be high quality monolayer graphene.
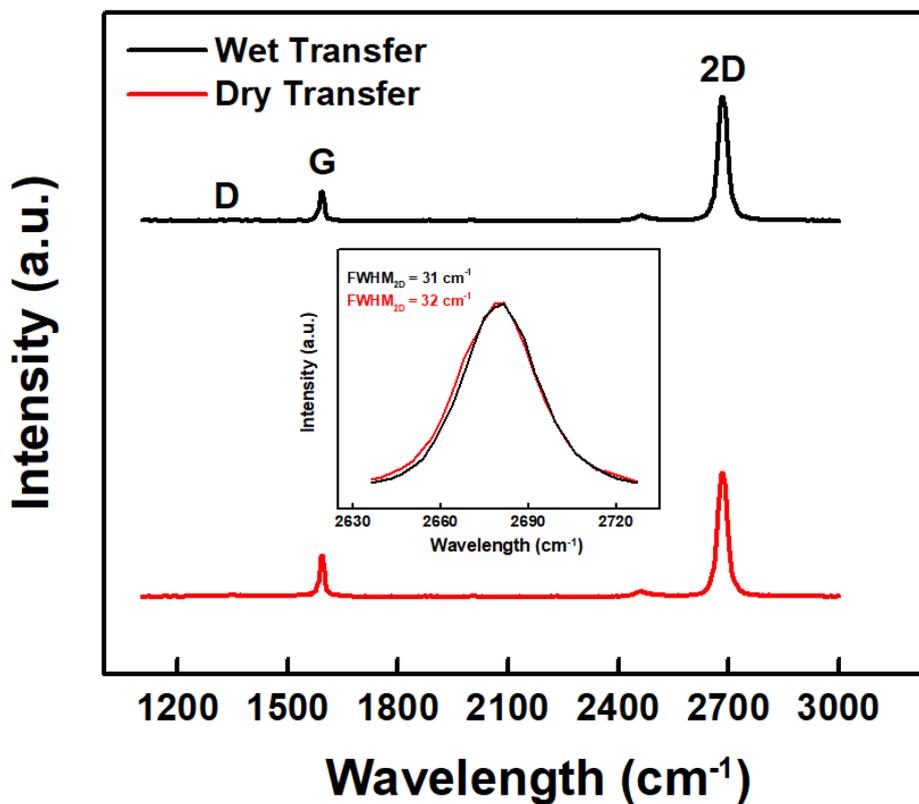
Figure 3.2 Raman single spectra of wet and dry transferred graphene. The zoom-in of 2D peaks are depicted in the inset graph. [*Submitted*]

3.1.3 Effect of Trapped Water Molecules under Graphene Layer

In the previous studies, graphene or carbon nanotube field effect transistors have current-voltage hysteresis due to the charge trapping by water molecules or ions [66-69]. As shown in Fig. 3.3, the origins of hysteric behavior can be from the substrate or ambient condition because both hydrophobic substrate and vacuum condition contribute to the reduction of the hysteresis of GFET [57]. In this experiment, we expected that a smaller amount of water molecules between graphene and the substrate can reduce the trapping of charge carrier in graphene channel.
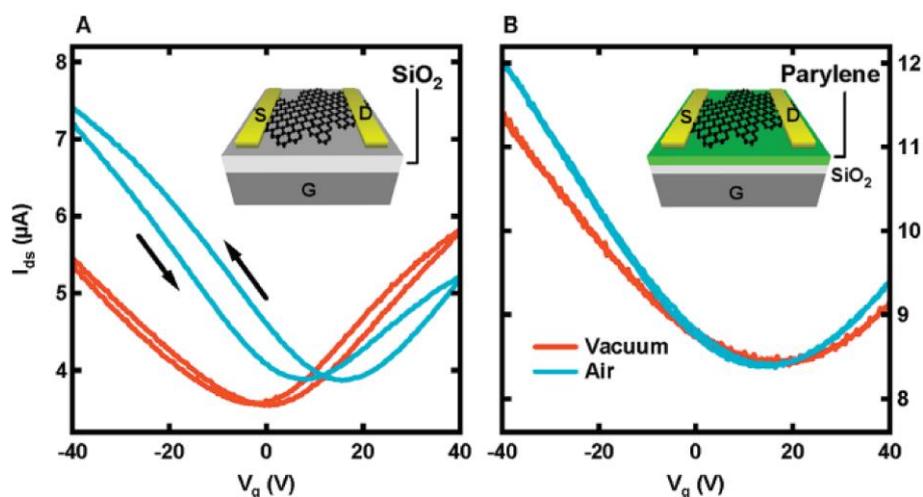
Figure 3.3 Source-drain current vs. gate voltage hysteresis of GFET on hydrophilic (SiO$_2$) and hydrophobic (Parylene) substrate. The red curve represents the measurement in vacuum and the blue curve is in air [57].

The schematic of GFET structure and its optical microscope image are depicted in Fig. 3.4. As shown in Fig. 3.4a, graphene channel is formed on the SiO$_2$/Si substrate so that the SiO$_2$ works as a gate oxide and heavily doped silicon as a gate electrode. The fabrication processes of GFET are as follows. First, clean the SiO$_2$/Si substrate by ultra-sonic agitation using acetone and methanol for 5 minutes each. Next, transfer the graphene on the substrate as described in the previous section. After transferring the graphene, patterning the graphene channel by using conventional photolithography process (AZ 5214E, 3000 rpm, 100 J more detail). The O$_2$ plasma etching process is followed with the reactive ion etching (RIE) system. As shown in Fig. 3.5, the etched area has no peaks from 1000 cm^{-1} to 3000 cm^{-1} and the only graphene channel has sharp 2D and G peaks. After removal of the photoresist, the source and drain contacts are formed by using photolithography, e-beam evaporation, and lift-off process.

Figure 3.4 The fabricated GFET structure and its optical microscope image. The source and drain electrodes are Ti/Au (10/50 nm) and the channel width and length are both 10 μm. [*Submitted*]
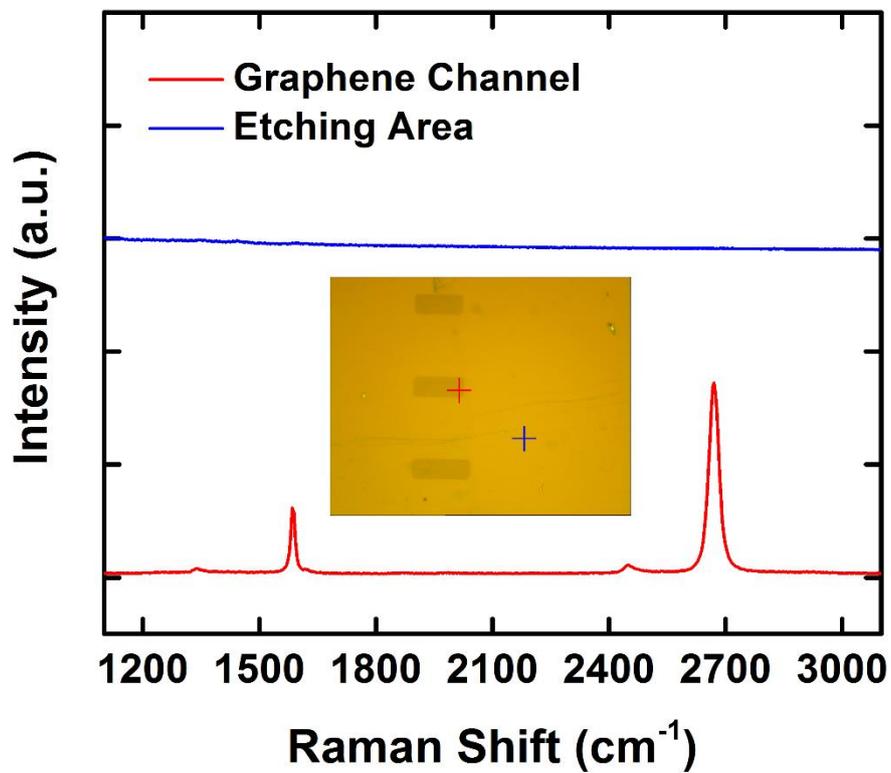
Figure 3.5 The Raman spectrum after etching the graphene remaining the channel area. The inset optical microscope image shows the position of spectrum. The red cross represents the position of red single spectrum (Graphene channel) and the blue one is for etched area. [*Submitted*]
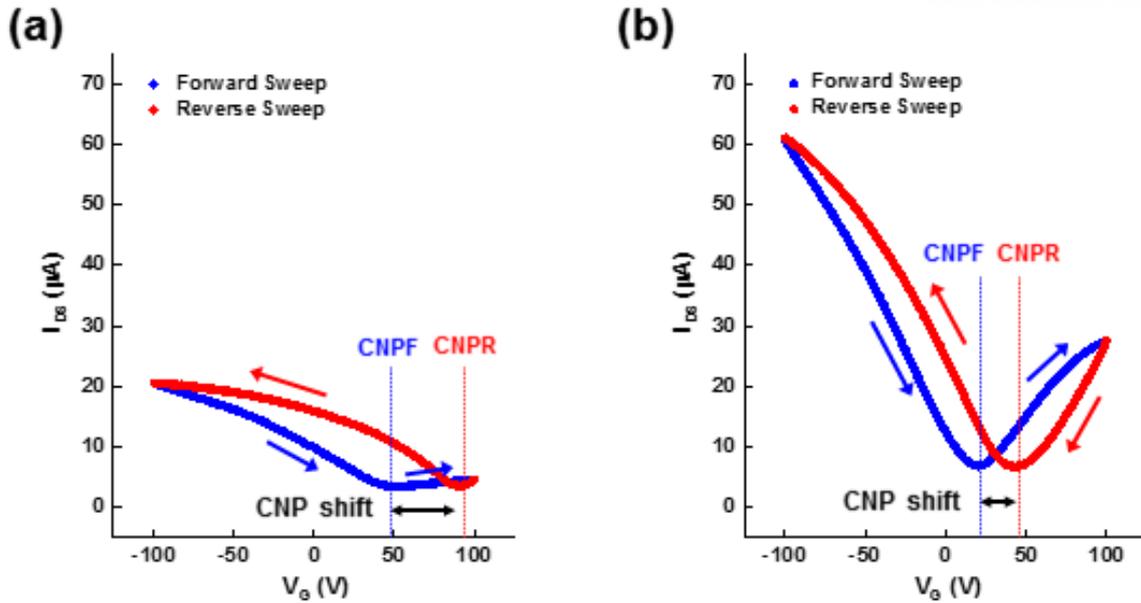
Figure 3.6 Source-drain current vs. gate voltage for (a) wet and (b) dry transferred GFET. The blue curves show the I-V curves for the forward sweep and the red curves represent the reverse sweep. [*Submitted*]

In Fig. 3.6, the source-drain current (I_{DS}) vs. gate voltage (V_G) curves of wet and dry transferred GFETs are shown. Since we focused on the effect of trapped water molecules on current-voltage hysteresis, the measurements were performed with two different gate voltage sweep directions. The blue curve corresponds to the sweeping from -100 V to 100 V (Forward sweeping) and the red one is from 100 V to -100 V (Reverse sweeping). The charge neutrality points for the forward gate sweeping (CNPF) and for reverse sweeping (CNPR) are different in both wet and dry transferred GFET. The CNPF and CNPR are ~21 V and ~43 V for dry sample. Similarly, the CNPF of wet sample lies at ~51 V and CNPR at ~90 V. Both wet and dry samples have larger CNPR values rather than the CNPF. However, the wet sample has the larger value of CNPF (51 V > 21 V) and CNPR (90 V > 43 V) and seems more p-doped. Moreover, the difference between CNPF and CNPR is also larger than the dry sample (39 V > 22 V). Lastly, the source-drain current of the dry sample is much larger than the wet one.

Because we fabricated the dry and wet GFET with same processes, the only difference between them is the amount of water molecules trapped at graphene/SiO_2 interface. Therefore, based on the difference in I_{DS}-V_G characteristics, the charge trapping by water molecules underneath the graphene layer can be a candidate for reasonable explanation.

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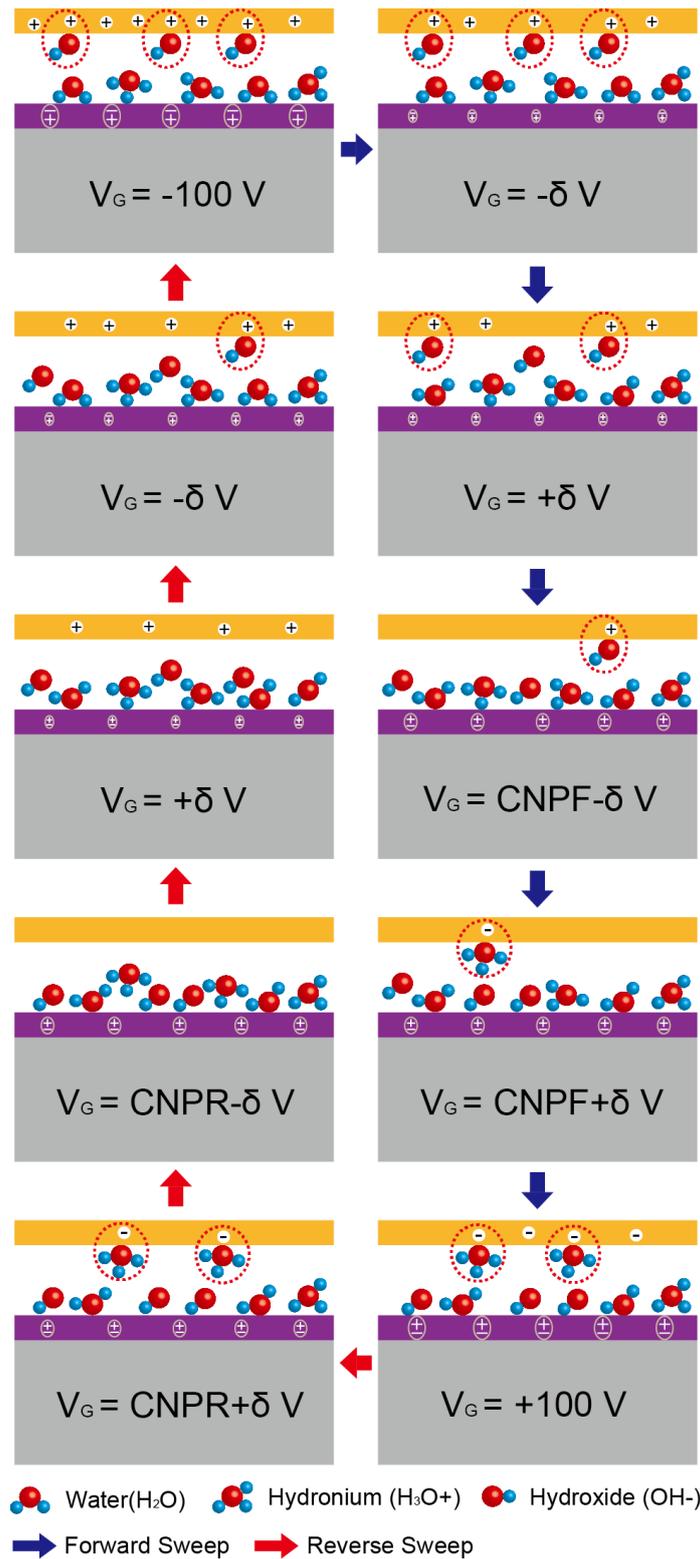
Figure 3.7 The schematic diagram of charge trapping mechanism on graphene channel for two different sweeping direction. CNPF is defined to be a charge neutrality point (CNP) for forward sweeping and CNPR is CNP for reverse sweeping. δ is a very small value approaching 0. The red dotted circles mean that the free carrier in graphene channel is trapped by the hydronium or hydroxide ions. [*Submitted*]

In Fig. 3.7, the free carriers of the graphene channel and the dynamics of trapped water molecules are depicted for forward and reverse gate sweeping. Without any gate bias voltage, the graphene channel is naturally p-doped because of the surface charge or defects of SiO_2 surface. The trapped water molecules can be also ionized into hydronium (H_3O^+) and hydroxide (OH^-) ions with the aid of SiO_2 surfaces [70-73]. Thus, the hydronium and hydroxide ions can be attached to either graphene or SiO_2 sides.

At -100 V gate voltage, the starting point of forward sweep, hydroxide ions are attached to the graphene layer owing to the repulsive force by gate field effect. On the other hand, the hydronium ions are attached to the SiO_2 surface. Here, the holes which are free carriers of the graphene channel can be trapped by the hydroxide ions. The attached ions on both graphene layer and SiO_2 surface have no applied repulsive force until the gate voltage reaches to $-\delta$ V (δ is significantly small value close to 0). When the polarity of gate voltage changes from negative to positive ($-\delta$ V to $+\delta$ V) the hydroxide and hydronium ions start to be detached from the graphene and SiO_2 surfaces. The ions are detached continuously, and the trapped holes becomes free carriers as the gate voltage reaches to CNPF-δ V. Considering the gate field effect on graphene, the number of electrons should be increased, and holes decreased in positive gate voltage. However, the number of holes decreases more slowly than the in the absence of hydroxide ions due to the generation of freely moving holes. After passing the CNPF (CNPF+δ V), the carrier type of graphene channel becomes electron. Now, the attached hydroxide ions are expected to be completely detached from the graphene layer by repulsive force from the electrons in the channel. Because the graphene channel becomes n-type, the hydronium ions starts to be attached to graphene layer and the hydroxide accumulate to the SiO_2 surface. Therefore, the hydronium ions bind the free electrons in graphene channel resulting the slower increment of carrier concentration with gate voltage increase to 100 V. As shown in Fig. 3.6, the current-voltage curve of forward sweep is retarded at the region of CNPF to 100 V compared to the reverse sweeping curve. When the gate voltage reaches to 100 V, the number of hydronium-electron pairs is maximized.

At the beginning of the reverse sweep, graphene channel has both free and trapped electrons as described in above. The number of free electrons decreases as the gate voltage approaches to the CNPR, but the trapped electrons are not detached from the hydronium ions because there is no repulsive force applied to them. Thus, the change of the electron density follows the gate electric field with no additional effects from the water molecules or ions. The hydronium ions start to be detached from the graphene layer after the gate voltage passes the CNPR similarly to the mechanism of hydroxide detachment at CNPF. The hole dominant graphene channel drives the hydronium ions to get away from it. Until the gate voltage passes 0 V, the hole is continuously increased by decreasing gate electric field. When the gate voltage becomes negative ($-\delta$ V to -100 V), holes are induced in graphene channel and the hydroxide ions are also attached to the graphene. This region corresponds to the CNPF to 100 V in forward sweeping case. The free holes increase slower than in the absence of the water molecules owing

to the free carrier trapping by hydroxide ions. Therefore, in this region, the current-voltage curve is retarded compared to the forward sweeping case as shown in Fig. 3.6. This picture can explain the actual measurement of current-voltage characteristics very well.
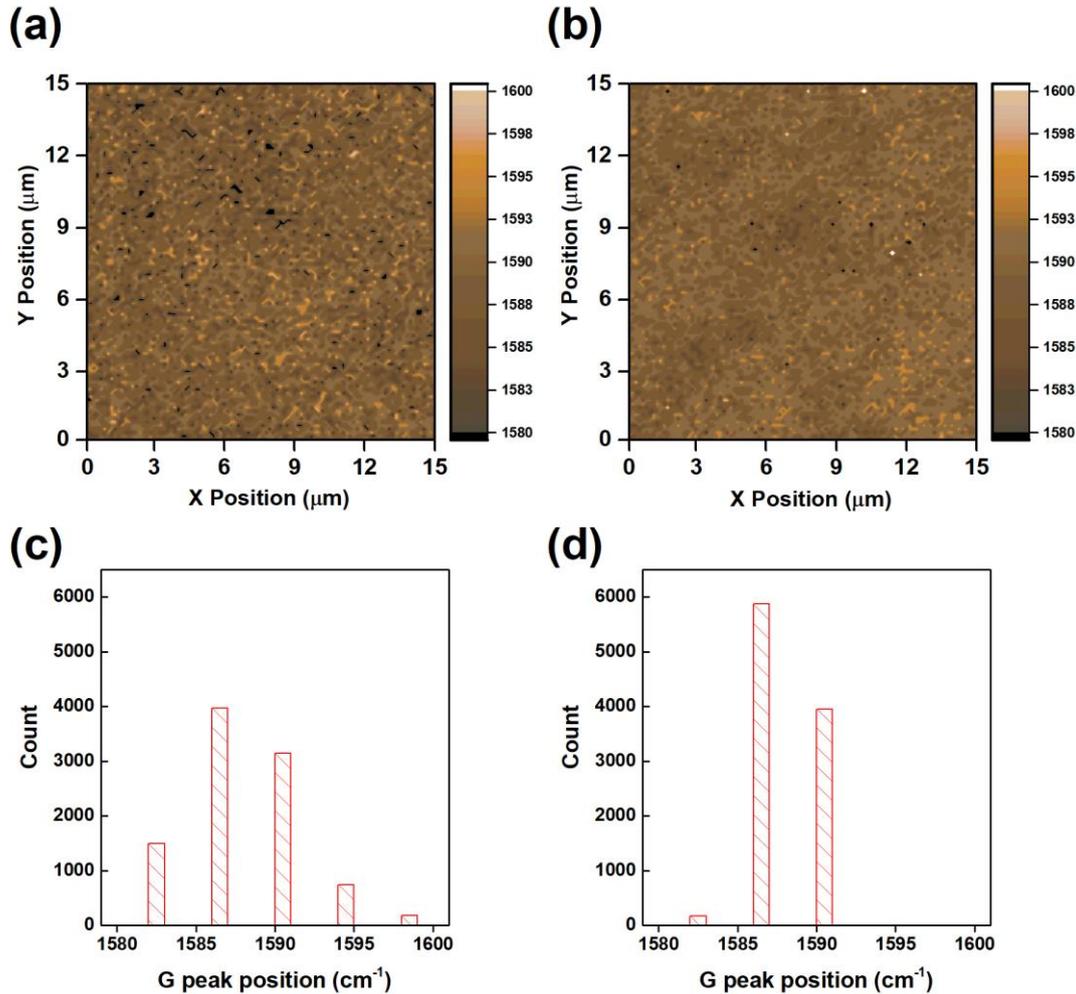
Figure 3.8 The Raman mapping for G peak position in case of (a) wet transferred graphene and (b) dry one. Corresponding histogram for (a) wet and (b) dry transferred graphene. [*Submitted*]

After the measurement of Raman single spectra, we performed Raman mapping to investigate the uniformity of the graphene. Figure 3.8 represents the Raman mapping images for G peak position and their histograms. The G peak position corresponding to the in-plane phonon vibration mode [74, 75] is ~1580 cm^{-1} in case of intrinsic graphene. The G peak shift from it can be explained by the extrinsic doping effect [76, 77]. Based on the histogram, the average value of G peak position for dry transferred graphene is 1587.8 cm^{-1} and for wet sample is 1587.7 cm^{-1}. While the average values are similar to each other, the standard deviation of G peak position is quite different depending on the transfer method. The wet transferred graphene has 4.1 cm^{-1} of standard deviation and the dry one has 2.1 cm^{-1}. The reason for broader G peak distribution of wet transferred graphene can be a non-uniform presence of

hydronium and hydroxide ions under the graphene layer as shown in Fig. 3.7 because the ions can make spatial variation of local charge density resulting the G peak position shift [78, 79]. A little spatial variation of G peak position in dry transferred graphene can be from the impurities and defects on SiO$_2$ substrate and a small amount of trapped water molecules and ions.

Based on the GFET measurements, the on-off ratio and field effect mobility can be derived. The on-off ratio in GFET $I_{DS} - V_G$ curve is dividing the saturation current from the minimum current. In this experiment, we found that the on-off ratio of dry transferred graphene is 9 and wet one is 6. The minimum current is similar to each case, but the saturation current of dry transferred GFET is bigger than the wet one. Next, the field effect mobility was calculated using the below equation.

$$\mu = L_{ch}|g_m|/W_{ch}C_G V_{DS} \tag{3.1}$$

Here, L_{ch} is the channel length, W_{ch} the channel width, g_m the transconductance (dI_{DS}/dV_G), C_G the capacitance of gate oxide, and V_{DS} the source-drain voltage. Since the transconductance value varies in gate voltage, a proper value should be inserted in the Eq. 3.1. Considering the charge trapping and retardation of the current-voltage curve, we chose the reverse sweeping curve to extract the transconductance rather than the forward case. In case of electron channel, the field effect mobilities of wet and dry transferred graphene are ~415 cm^2/Vs and ~1118 cm^2/Vs respectively. The corresponding transconductances of them are extracted from the slope of $I_{DS} - V_G$ curve in the range of CNPR to 100 V. The hole mobilities of wet and dry transferred graphene are ~399 cm^2/Vs and ~967 cm^2/Vs. Both electron and hole mobilities are much better for dry transferred graphene. The different electrical performance can be due to the scattering from the uneven Coulomb potential landscape originated from the water molecules, hydronium ions, and hydroxide ions. In other words, the non-uniform potential states in graphene layer can be enhanced by the adsorbates at the interface between SiO$_2$ and graphene.

Based on the $I_{DS} - V_G$ curve, we tried to estimate the reduction of trapped water molecules at graphene/SiO$_2$ interface between wet and dry transfer method. Both wet and dry transferred graphene channel seem to be p-doped because the CNPs are positioned in the positive gate voltage. The free hole density in the graphene channel can be expressed as

$$p_{channel} = p_0 - Q_{dielectric} \tag{3.2}$$

where p_0 is free hole density at zero gate voltage and $Q_{dielectric}$ is the induced charge on SiO$_2$ adjacent to the graphene layer. The $Q_{dielectric}$ is also calculated as

$$Q_{dielectric} = \varepsilon_r \varepsilon_0 \frac{V_G}{d} \tag{3.3}$$

where ε_r is the dielectric constant of SiO$_2$, ε_0 the vacuum permittivity, V_G the gate voltage, and d the thickness of SiO$_2$. When the gate voltage reaches to the CNP, the free hole density in channel becomes nearly 0. Substituting this condition into Eq. 3.2, free hole density at zero gate voltage (p_0) can be calculated to be $p_0 \approx \varepsilon_r \varepsilon_0 V_G^{CNP}/d$ where V_G^{CNP} is the CNP gate voltage. Since the possible reason for a larger shift of CNPR than CNPF is the electron holding by hydronium ions, the number of hydronium ions can be estimated from the difference between two CNPs. The number of electrons held by hydronium ions is considered to be

$$n_{hold} = p_0^r - p_0^f = \varepsilon_r \varepsilon_0 \Delta V_G^{CNP}/ed \qquad (3.4)$$

where n_{hold} is the electron density held by hydronium ions, p_0^r and p_0^f the free hole densities at zero gate voltages for reverse and forward sweeping, ΔV_G^{CNP} the CNP difference between reverse and forward sweeping, and e the electron charge. Considering the trapped water molecules might not be fully ionized into hydronium and hydroxide, the n_{hold} is a lower bound of trapped water molecule density. Thus, the density of trapped water molecules can be estimated as

$$N^{water} = n_{hold} + N_{non-ionized}^{water} + N_{free}^{hydronium} \qquad (3.5)$$

where N^{water} is the total density of trapped water molecules, $N_{non-ionized}^{water}$ the density of non-ionized water molecules, and $N_{free}^{hydronium}$ the density of hydronium ions not attached to graphene channel. Since the number of non-ionized water molecules and free hydronium ions will be larger in wet transferred graphene than the dry one, the reduced number of trapped water molecules can be estimated at least by the amount of

$$\Delta n_{hold} = \left(\varepsilon_r \varepsilon_0/ed\right)\left(\Delta V_{G,wet}^{CNP} - \Delta V_{G,dry}^{CNP}\right). \qquad (3.6)$$

Using the final equation (Eq. 3.6), we can derive Δn_{hold} as $\sim 1.2 \times 10^{12}$ cm^{-2} based on the $I_{DS} - V_G$ curves in Fig. 3.5.

In summary, we proposed a simple dry transfer method using a Kapton tape as a flexible supporting layer to hold PMMA/graphene stack. Raman single spectrum shows the dry transferred graphene shows the small D peak with larger than 2 of 2D/G peak ratio. Comparing the Raman mapping data of dry transferred graphene with wet sample, the variation of G peak position is much less indicating that the local doping density of graphene is more uniform. This phenomenon can be explained by the reduction of trapped water molecules which may cause the charge trapping of graphene layer. The transferred graphene was fabricated to GFET and $I_{DS} - V_G$ measurement was performed. Depending on the gate voltage sweeping direction, the GFET has different CNPs and curvatures. This current-voltage hysteresis is also reduced in dry transferred GFET than wet sample because the number of ions

dissociated from the trapped water molecules at the graphene/SiO$_2$ interface is decreased. Moreover, the field effect mobility is enhanced due to the more uniform Coulomb potential established with the reduced adsorbates such as water molecules, hydroxide, and hydronium ions. Our dry transfer method is not much different from the conventional wet transfer method excepting the attachment of Katpon tape on PMMA/graphene stack. However, this makes it possible to evaporate the water molecules using N$_2$ blowing and heating processes before the transferring on the substrate. In result, our dry transfer method can be applicable to the currently used graphene transfer method and enable to transfer the graphene on the water-sensitive substrates.

3.1.4 Graphene Hall Measurements (Wet vs. Dry)

Hall effect was first discovered by E. H. Hall [80] and have been used for estimating the carrier type and density by investigating the Hall voltage. In Fig. 3.9, the principle of Hall effect is depicted for both electrons and holes at a specific magnetic field direction. The magnetic field direction is upward, and the current density direction is left to right. In case of the free carrier charge is positive, the Lorentz force is applied in the amount of

$$\vec{F}_E = q\vec{v} \times \vec{B} \tag{3.7}$$

where q is the amount of charge, $\vec{v}$ the velocity of free carrier, and $\vec{B}$ the magnetic field. Here, considering only the direction of Lorentz force,

$$\vec{F}_E = q\vec{v} \times \vec{B} = qvB(\hat{x} \times \hat{z}) = -qvB\hat{y} \tag{3.8}$$

since the positive charge has the same velocity direction with the current density $\vec{j}_x$. The positive free carrier is accumulated to the down-side of the sample as shown in Fig. 3.9b. Once the free carriers move to bottom of the sample, the top-side is automatically negative. Then, the electric field is formed from bottom to top. This electric field enforces the free carriers to move to the top-side which is opposite to the Lorentz force. When the Lorentz force and the electric force is balanced, the free carriers stop moving in y-direction and the Hall voltage (V_H) can be measured.

In case of negatively charged free carriers, the Lorentz force direction is same for the positive case because the charge q has a negative sign and $\vec{v}$ is also negative in the Eq. 3.7.

$$\vec{F}_E = q\vec{v} \times \vec{B} = -|q|vB(-\hat{x} \times \hat{z}) = -qvB\hat{y} \tag{3.9}$$

Therefore, the accumulation direction of negatively charged free carrier is also downward. Similar to the positive case, the electric field is formed from the top- to bottom-side. However, the electric force direction applied to the free carrier is same because the free carrier charge is now negative. In short, the electric force direction is just the opposite direction to the Lorentz force direction. The charge distribution and applied force directions are shown in Fig. 3.9c. In result, we can safely decide the free carrier charge by using the Hall voltage sign.

In the Hall measurement, the carrier density can be derived from the Hall voltage vs. Magnetic field curve. The current density can be expressed as like the below equation.

$$\vec{I} = \vec{j}_x A = qn\vec{v}A = qn\vec{v}wt \tag{3.10}$$

Here, n is the carrier density, A the cross section area of the sample, w the width of the sample, and t the thickness of the sample. As described in the above, the free carriers move until the Lorentz force and electric force is balanced. Thus, the force equation should be

$$qvB = qE \tag{3.11}$$

because the two forces are same in magnitude but opposite in direction. The induced Hall voltage can be expressed as the product of the electric filed and width of the sample.

$$V_H = wE \tag{3.12}$$

By substituting the Eq. 3.10 and 3.11 into 3.12, Eq. 3.12 becomes

$$V_H = wvB = \frac{BI}{qnt}. \tag{3.13}$$

Rearrange the Eq. 3.13 in terms of carrier density n,

$$n = \frac{BI}{V_H qt}. \tag{3.14}$$

Since the Hall voltage is varied with the magnetic field, dividing terms can be expressed as derivative term.

$$n = \frac{I}{qt} \cdot \frac{dB}{dV_H} \tag{3.15}$$

This equation gives the carrier density of 3D bulk sample and the equation for 2D case is little different from it. In the current equation (Eq. 3.10), the thickness of the sample is 0 so that the current is the product of the current density and width. Here, the current density has a unit of A/m instead of A/m².

$$\vec{I}_{2D} = \vec{j}_x w = qn\vec{v}w \tag{3.16}$$

Corresponding carrier density equation becomes

$$n = \frac{I}{q} \cdot \frac{dB}{dV_H}. \tag{3.17}$$

(a)

(b)

(c)
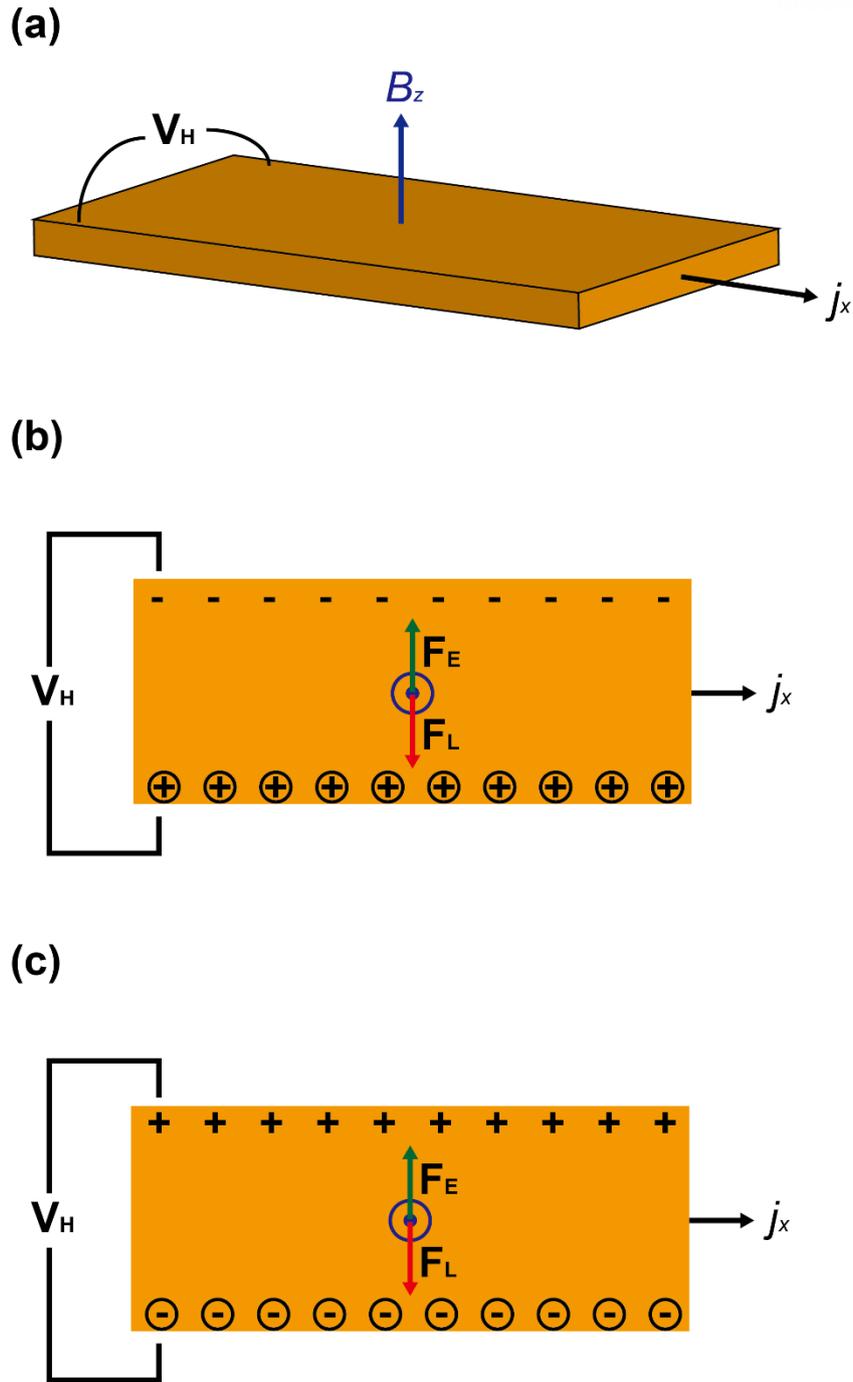
Figure 3.9 The schematic of Hall measurement. (a) The directions of current density and magnetic field. The charge distribution depending on the free carrier type (b) positive and (c) negative. F_L means the Lorentz force and F_E represents the electric force by electric field induced by the charge accumulation.

Since the electric conductivity is the product of the electric charge, carrier density, and mobility, the carrier mobility can be extracted in Hall measurement. As described in the above equations (Eq. 3.14 and 3.17), the carrier density can be obtained by the Hall measurement. The conductivity can be precisely measured by 4-point probe measurement. As shown in Fig. 3.10, the Hall bar geometry enables us to measure the Hall voltage and magnetoresistance at once. The Hall voltage can be measured by selecting upper and lower electrodes in the same x-coordinate position when the current flows from electrode 1 to 4. For example, the electrode pair of 2 and 6 or pair of 3 and 5 gives the Hall voltage when the magnetic field is applied. Since the Hall voltage is the voltage in y-direction with x-directional current, another expression in Hall bar geometry is V_{xy} and corresponding resistance can be expressed as R_{xy}. Otherwise, the conductivity or resistivity of channel can be measured by choosing two electrodes in the same y-coordinate position. For instance, the voltage across the electrode 2 and 3 or 5 and 6 divided by the current from electrode 1 to 4 is the pure channel resistance diminishing the contact resistance. Similar to the Hall voltage expression, the channel resistance can be expressed as a R_{xx} and the corresponding voltage is V_{xx}. Therefore, the carrier density and mobility can be calculated by the simultaneous measurements of Hall voltage and channel resistance with this pattern.

The resistivity can be expressed as

$$\frac{1}{\rho} = qn\mu \tag{3.18}$$

where ρ is the resistivity, q the electric charge, n the carrier density, and μ the carrier mobility. The resistivity can be also expressed as

$$R_{xx} = \frac{V_{xx}}{I} = \rho \frac{L}{W}. \tag{3.19}$$

Combining the Eq. 3.18 and 3.19, the carrier mobility equation is

$$\mu = \frac{1}{qn\rho} = \frac{1}{qnR_{xx}}\frac{L}{W}. \tag{3.20}$$

Here, the carrier density can be substituted by Eq. 3.17 and the mobility equation becomes

$$\mu = \frac{1}{qnR_{xx}}\frac{L}{W} = \frac{1}{q}\frac{q}{I}\cdot\frac{dV_H}{dB}\frac{I}{V_{xx}}\frac{L}{W} = \frac{dV_H}{dB}\frac{1}{V_{xx}}\frac{L}{W}. \tag{3.21}$$

Thus, the mobility can be calculated by the slope of Hall voltage with the magnetic field curve (dV_H/dB), the V_{xx}, and the geometric factor (L/W).
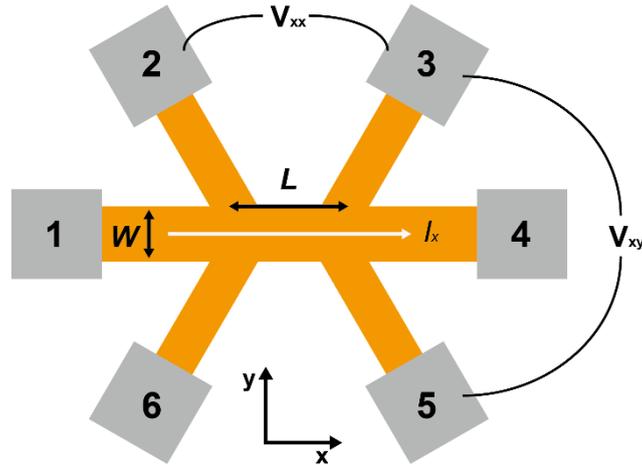
Figure 3.10 Hall bar geometry with 6 electrodes. The width (W) and length (L) of the channel is shown.
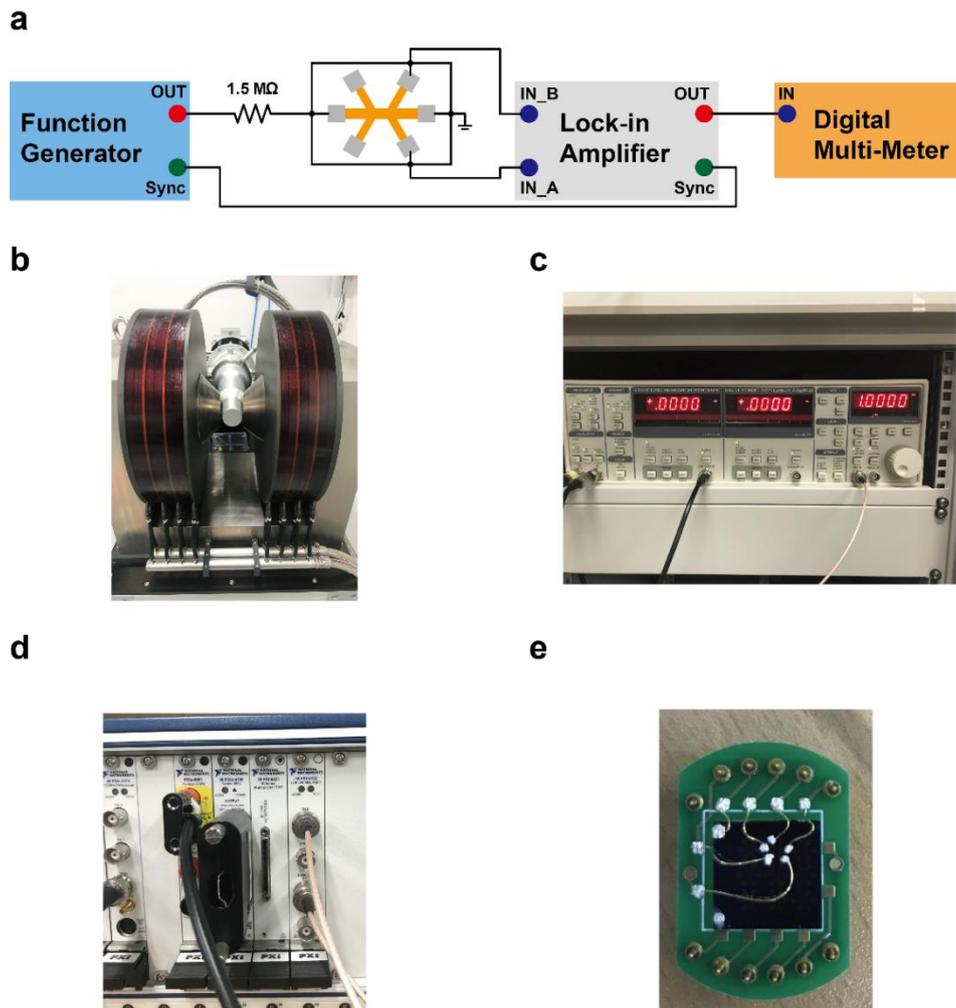
Figure 3.11 (a) The schematic diagram for Hall measurement system circuit. The optical images of (b) magnetic coil, (c) lock-in amplifier, (d) function generator and digital multi-meter, and (e) sample mounted on sample holder.

In the previous section, we found that the trapped water molecules and their ions (hydronium and hydroxide) can be adsorbates holding the free carriers in the graphene channel. Since the charge trapping can affect to the carrier density in the graphene channel, Hall measurement is needed to confirm our explanation.

First, graphene is transferred on the SiO_2/Si substrate with two different transfer methods (wet and dry). Then, the Hall bar patterned shadow mask is aligned to the sample and aluminum (30 nm) is deposited by using E-beam evaporator to form metal etch mask. Here, we performed the patterning of the graphene by using metal etch mask instead of polymers such as photoresist or PMMA because they can be remained as a residue on graphene after removing them. After depositing the metal mask, O_2 plasma etching process is followed and only the graphene under the metal mask survives. Next, the aluminum layer is removed by using the aluminum etchant type-A (Transene, USA). Finally, the contact metal evaporation (Ti/Au, 10/50 nm) is performed with the shadow mask method. There are no lithography processes and use of polymers during the fabrication of Hall measurement sample. Thus, we can expect that there are a very few extrinsic factors to affect the Hall measurement result.

As shown in Fig. 3.11, the Hall measurement was performed by using function generator, lock-in amplifier, digital multi-meter, and magnetic coils. The Fig. 3.11a is the schematic diagram of the measurement circuit, Fig. 3.11b, c, and d the optical images of magnetic coil, lock-in amplifier, and the digital multi-meter and function generator, Fig. 3.11e the sample mounted on sample holder connected with gold wire and indium ball. The magnetic coil generates the coil current of 63 A resulting 1 tesla of magnetic field across the two different coils.

After set-up the measurement system, the sample is equipped to the cryostat and rotary pump is turned-on to pumping down the system. Next, the helium compressor is turned-on to reach at low temperature. Then, the cryostat is rotated with 90 degrees and moved into the gap between two magnetic coils. The function generator is now turned-on with sinusoidal waveform to provide the current on the sample. Finally, the coil current is driven to make a magnetic field and the Hall voltage is simultaneously measured by the lock-in amplifier and the digital multi-meter.

a

b

c

d
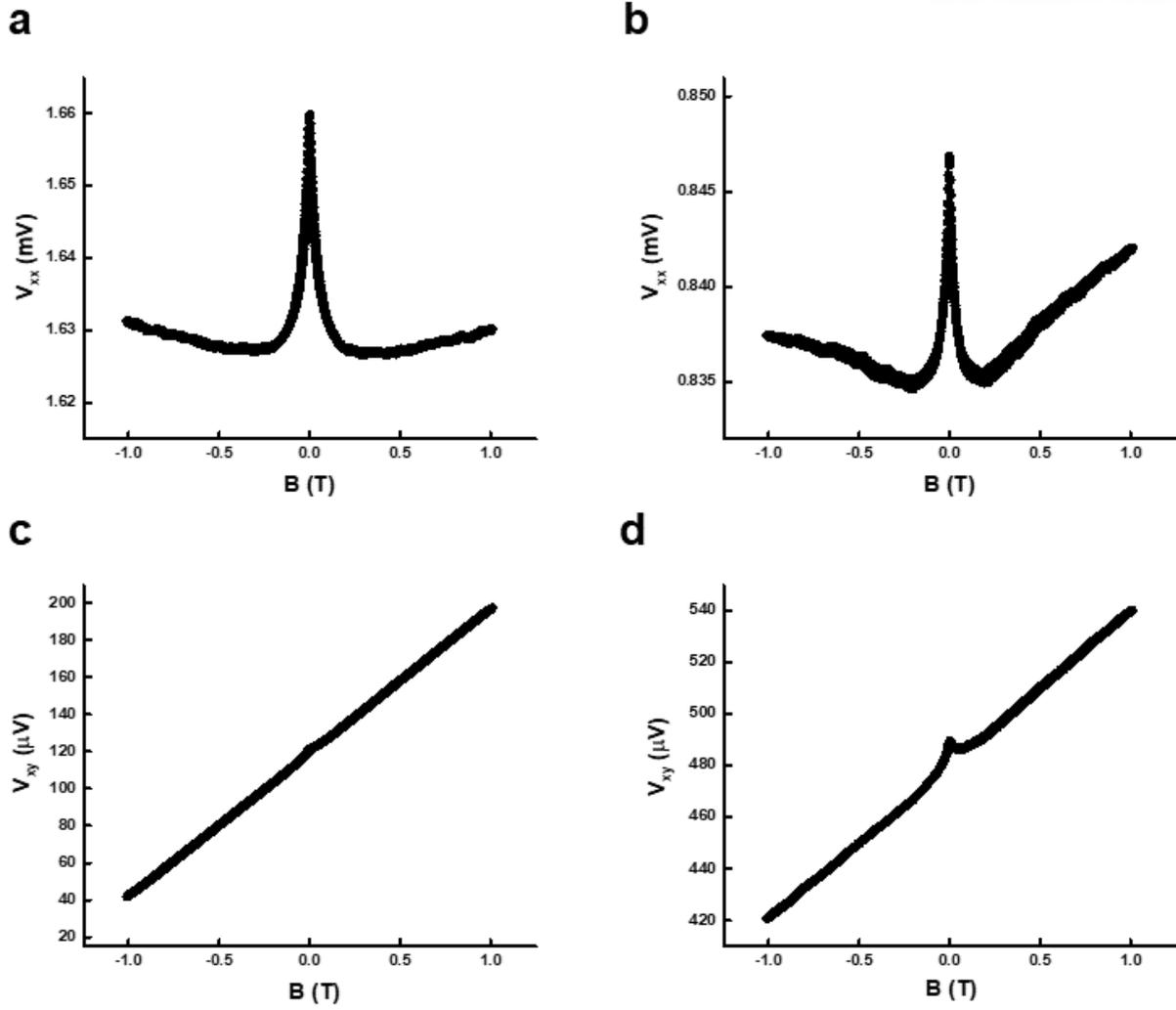
Figure 3.12 The V_{xx} for (a) wet and (b) dry transferred graphene in Hall bar geometry. The V_{xy} for (c) wet and (d) dry case.

The Hall measurement results for wet and dry transferred graphene are shown in Fig. 3.12. Figure 3.12a and b show the V_{xx} of the Hall bar geometry of wet and dry transferred graphene. The shapes of graphs are very similar to each other with different lowest value. Generally, the magnetoresistance of graphene should be increased with the magnetic field without any defects because the carrier is accumulated to one side or rotated in the channel so that the number of carriers contributed to the electric current is decreased. However, the resistance can be decreased by the scattering assisted current flow which is called weak localization [81, 82]. As the magnetic field increases, the resistance is increased after this phenomenon. In our case, the magnetic field is very small so that the weak localization is mainly shown in the graphs. The V_{xx} of wet transferred graphene is not increased much even after the decrease of V_{xx}. Compared to the wet case, the V_{xx} of dry transferred graphene has a larger increase rate after decrease. This can be an evidence for that the larger number of scattering sources exist in wet transferred graphene due to the trapped water molecules.

In Fig. 3.12c and d, the Hall voltage (V_{xy}) of wet and dry transferred graphene are shown. The shape of Hall voltage vs. magnetic field is linear with a small peak around zero magnetic field. This small peak can be expected to be from the existence of a small amount of V_{xx} component in Hall bar geometry such as the electrode contact on graphene or gold wire connection on the contact pad. Therefore, we ignored the small peak around zero magnetic field and calculated the carrier density with the overall slope of the curve. As described in the Eq. 3.17, the carrier density can be estimated from Hall voltage vs. magnetic field curve. The carrier densities of wet and dry transferred graphene are calculated to be 5.31×10^{13} cm^{-2} and 6.90×10^{13} cm^{-2}. Considering the free carrier charge trapping by hydroxide ions, the results are well matched with the previous explanation because the carrier density is larger in dry transferred graphene. Moreover, the Hall mobility can be calculated by Eq. 3.21 and its value is 1911 cm^2/Vs for wet transferred graphene and 2866 cm^2/Vs for dry sample. Here, we can conclude again that the dry transferred graphene has better mobility due to reduced scattering sources.

3.2 Graphene Fluorination

3.2.1 Synthesizing Method of Fluorinated Graphene (FG)

Functionalization of graphene has been studied with various methods to modify the electronic properties of graphene [83-85]. In this experiment, we performed the fluorination process on graphene to convert it from a semi-metal to an insulator [86-88]. Generally, fluorinated graphene has been synthesized by using fluorine exposure with or without plasma [87]. The fluorine gas used in these processes are XeF_2, F_2, SF_6, and CF_4. As shown in Fig. 3.13 [89], the fluorination process can be performed in the RIE system with fluorine gas. Since the plasma fluorination process has a shorter reaction time than the direct gas exposure method, fluorination with plasma has been studied much recently.
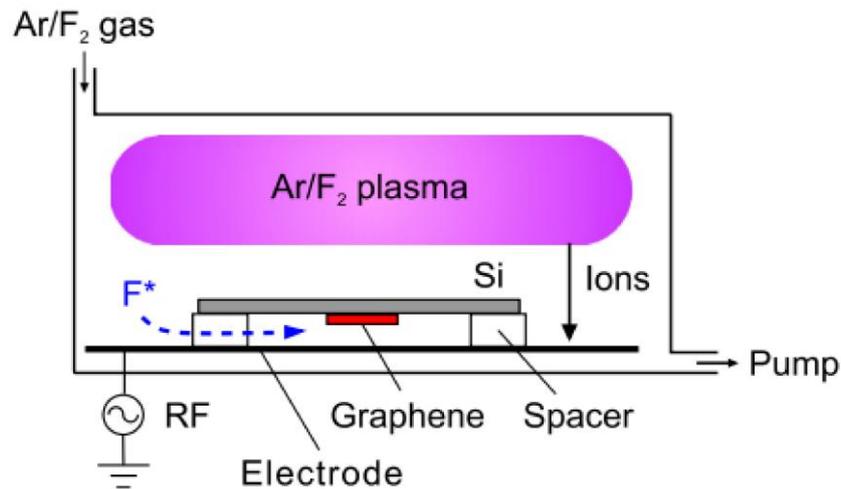
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Figure 3.13 The schematic of the plasma fluorination process in the RIE system [89].

3.2.2 Characteristics of FG

The fluorinated graphene (FG) has very different electrical and optical properties compared to the pristine graphene [86-90]. First, the optical property of FG on SiO_2/Si substrate was studied by J. T. Robinson *et al* [90]. In Fig. 3.14, the images for graphene and FG on SiO_2 surface are shown. The cross bar patterned graphene is shown in Fig. 3.14a which is clearly distinguishable from the SiO_2 substrate. However, it is hard to find the area of FG as depicted in Fig. 3.14b except the bilayer regions indicated by small arrows. Direct comparison for optical properties of graphene and FG on SiO_2 surface is shown in Fig. 3.14d. The patterned region is graphene and the other area is FG which seems to be much transparent on SiO_2 surface.

The electrical properties of FG have been proven to be relying on the fluorination process time [88, 90]. As shown in Fig. 3.15 [90], the energy band gap of FG becomes larger as increase of fluorine coverage on graphene. When the ratio of carbon atoms and fluorine is 4, the graphene can be fully fluorinated. The fully fluorinated graphene is an insulator and the moderately fluorinated graphene is a semiconducting material [91].
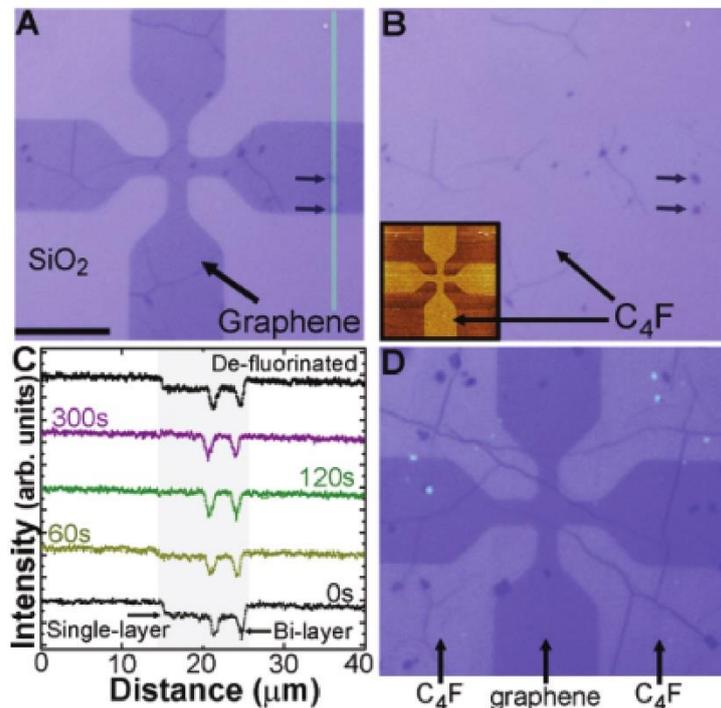
Figure 3.14 The optical properties of FG on SiO_2 surface. Images for patterned (a) graphene and (b) FG on SiO_2 surface. (c) RGB signal recorded by CCD camera. (d) Images for patterned graphene and FG on the rest of area [90].

37
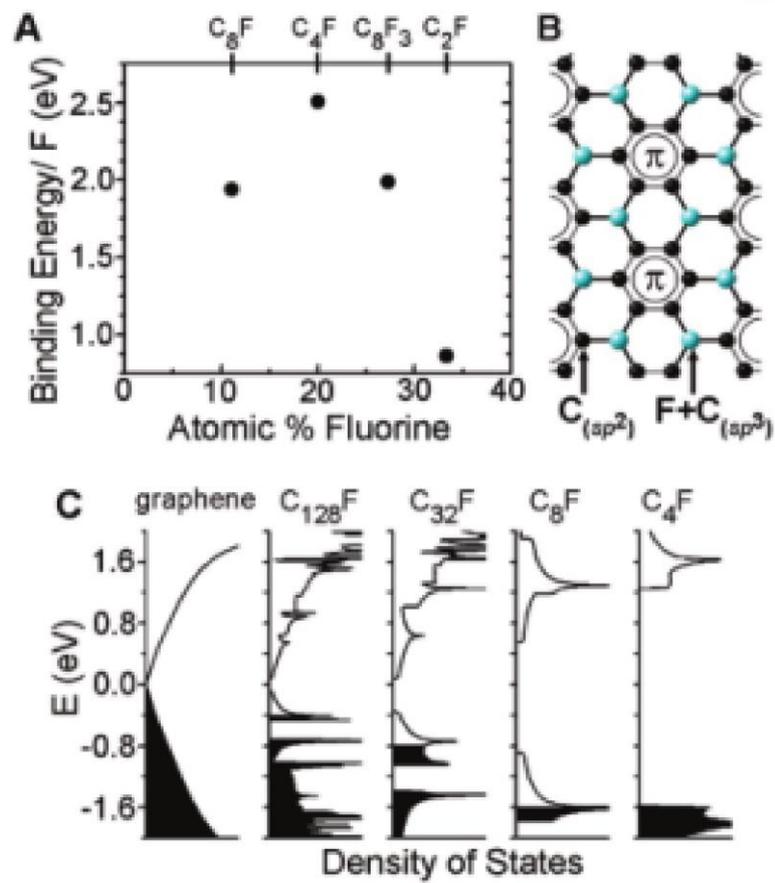
Figure 3.15 (a) Calculated binding energy with an atomic percentage of fluorine atoms. (b) The schematic of C_4F (Fully fluorinated graphene). (c) Density of states of FG with various fluorine coverage [90].

3.3.3 Device Applications

As described in the previous section, the FG has semiconducting and insulating characteristics depending on the fluorine coverage. Therefore, studies for FG have been conducted by using the semiconducting channel or insulating layer [88, 91-93].

The FG semiconducting channel can be formed with moderate fluorination by adjusting the process time [90]. The semiconducting characteristics of FG can be used as a channel material for a field effect transistor (FET) [91, 92]. As shown in Fig. 3.16 [91], the FG channel on the SiC substrate has diode characteristics between graphene electrodes. The semiconducting channel characteristics can be tuned by the top gate voltage as shown in the graph. The FG channel by using CVD graphene was also studied as depicted in Fig. 3.17 [92]. The source-drain current vs. source-drain voltage curve (Fig. 3.17a) shows nonlinear characteristics. The channel resistance is also tunable by the back gate voltage as shown in Fig. 3.17b.
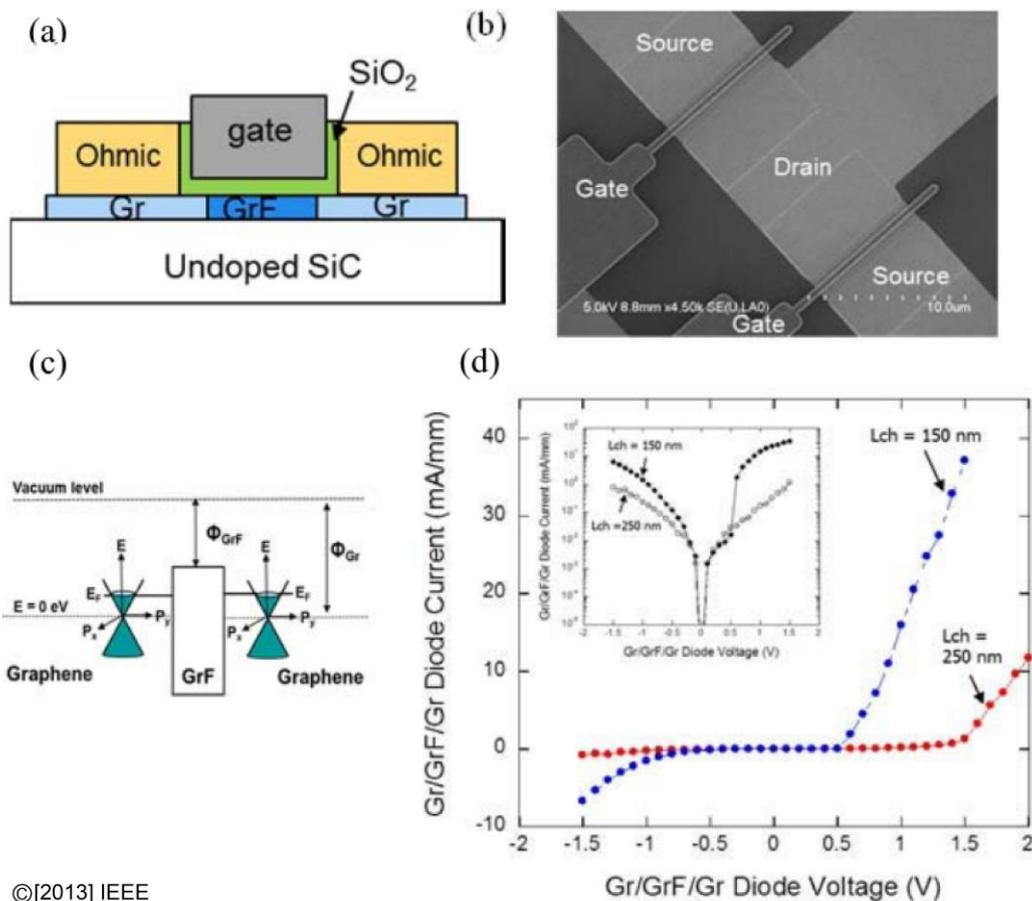
©[2013] IEEE

Figure 3.16 (a) Graphene/FG/Graphene lateral heterojunction with top gate. Graphene layer is epitaxially grown on SiC substrate. (b) Device image. (c) Energy band diagram of G/FG/G heterostructure. (d) Current-voltage curve with different channel length [91].
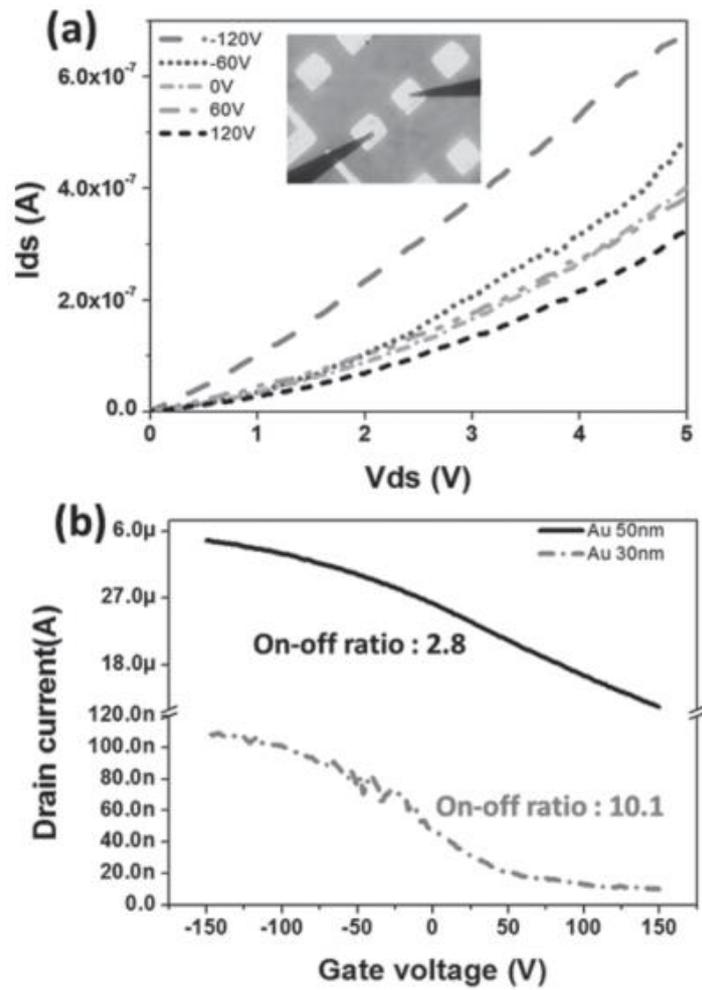
Figure 3.17 Field effect transistor using FG as a channel material. (a) Source-drain current vs. source-drain voltage characteristics. Inset image is the device image. (b) Source-drain current vs. gate voltage characteristics [92].

In case of using FG as an insulating layer, the graphene should be fully fluorinated. The FG was used as a dielectric material by K. I. Ho *et al* [88]. As shown in Fig. 3.18, the graphene channel is covered by the FG layers that are acting as a gate insulator. The transfer characteristics of GFET is also measured well using multilayer FG as a top gate insulator (Fig. 3.18b). With a monolayer FG, vertical tunnel junction was studied for a spin and charge transport by A. L. Friedman *et al* [93]. Figure 3.19 shows the vertical tunnel device with graphene and FG. As described in this section, the FG have been utilized as a semiconducting channel or insulator in various purposes.
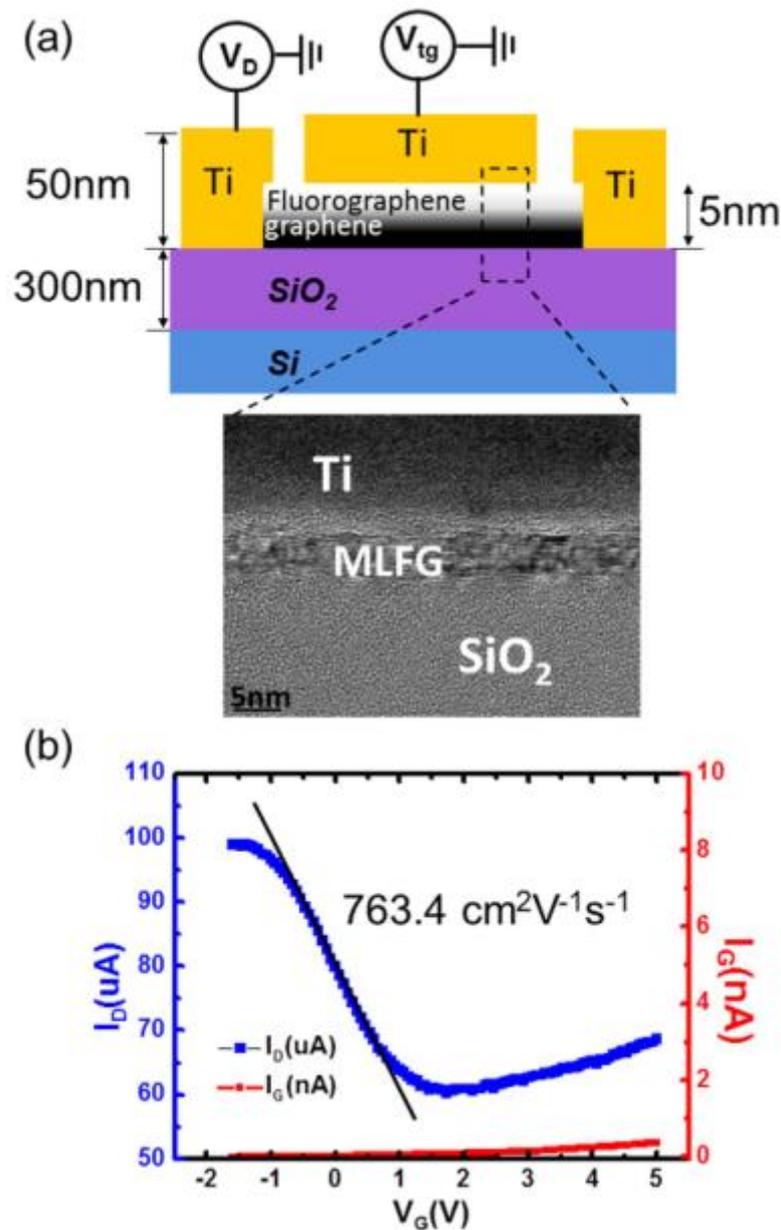
Figure 3.18 (a) GFET structure with FG top gate insulator. (b) Transfer characteristics of GFET [88].

Figure 3.19 (a) Schematic and (b) optical image of Graphene/FG/Graphene vertical tunnel junction [93].
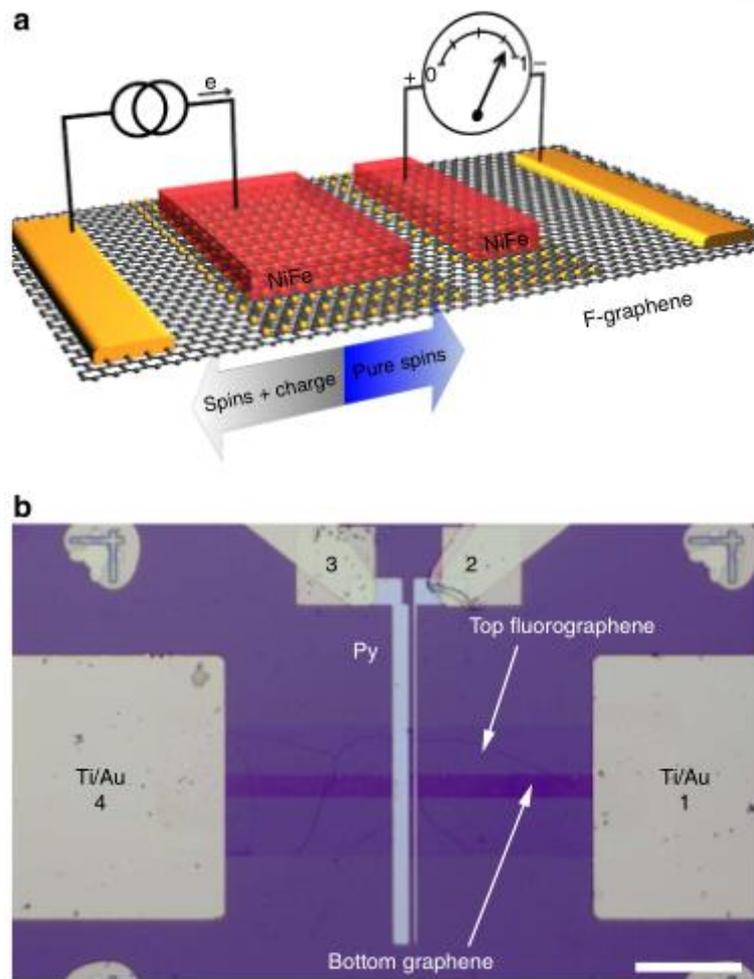
3.3 Characteristics of Graphene Lateral Tunnel Junction

3.3.1 Experimental Method of Forming Lateral Tunnel Junction

Researches for graphene vertical tunnel junction with FG as a tunnel insulator have been studied as described in the previous section [93]. Also, the graphene lateral junction with the semiconducting FG channel was fabricated both using epitaxial and CVD grown graphene [90, 91]. However, there is no research for lateral tunnel junction using FG tunnel barrier. In this experiment, we fabricated Graphene/FG/Graphene lateral tunnel junction using selective fluorination.

Figure 3.20 shows the first fabrication method of Graphene/FG/Graphene lateral tunnel junction device (Method 1). First, we transferred the graphene on SiO$_2$/Si substrate using the dry transfer method (described in section 3.1). Second, the contact pad pattern is formed by using E-beam lithography and contact metal (Ti/Au 10/50 nm) is deposited with E-beam evaporator. Here, two different contact pads are apart from each other with very small distance (50 nm) becoming the thickness of the tunnel barrier. After the lift-off process, the remaining area is fluorinated using the dielectric RIE system. The fluorination process condition for fully FG is flowing 50 SCCM (Standard Cubic Centimeter per Minute) of CF$_4$ gas with 20 W plasma state for 30 minutes in 50 mTorr pressure. This is a very simple method to form Graphene/FG/Graphene tunnel junction because the contact pads act as shadow mask to prevent the underlying graphene becomes FG. After fluorination, Raman spectroscopy was measured to confirm whether the graphene is fully fluorinated or not. The single spectrum of Raman spectroscopies for both graphene and fluorinated graphene are shown in Fig. 3.21. Before fluorination, the graphene has larger than 2 of 2D/G peak ratio and small D peak. However, after the fluorination process, the FG has no G, D, and 2D peaks. This result coincides with the previous studies of Raman spectroscopy of FG [86, 87].

Another fabrication method of forming Graphene/FG/Graphene tunnel junction was also performed (Method 2) as shown in Fig. 3.22. The reasons for developing the second method is to form a wider width and to eliminate the underlying graphene on contact pads. In this method, the graphene channel is patterned with the metal shadow mask and etching process. Here, the evaporated metal shadow mask was used to prevent the polymer residue on graphene when we use the lithography process. Then, the evaporated metal on graphene is removed by metal etchant. After the graphene channel is defined, the contact metal is evaporated on the two sides of the graphene channel by using the shadow mask method. This shadow mask is made of stainless steel and attached to the sample temporarily. Next, the E-beam lithography process is followed to expose only the region where the tunnel barrier should be formed (50 nm width). Finally, the fluorination process is performed on the sample resulting only the exposed area becomes FG. This process is more complex than the "Method 1". However, we can define the channel and tunnel barrier more precisely compared to the metal pattern with the lift-off process in "Method 1"
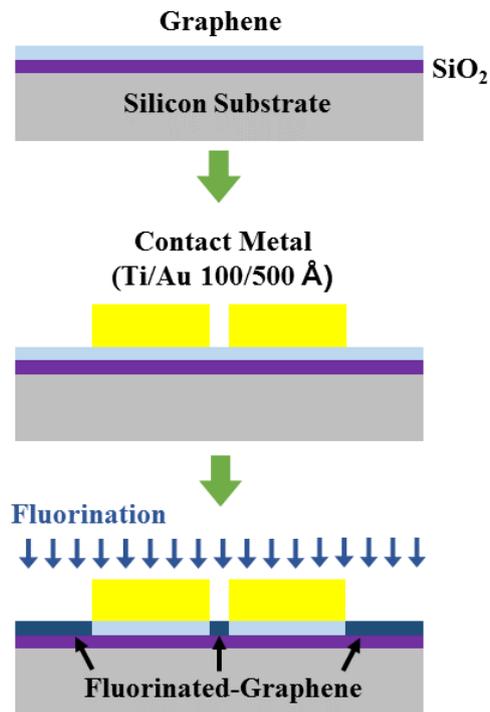
Figure 3.20 Fabrication process of graphene/FG/graphene tunnel junction on SiO_2/Si substrate (Method 1).
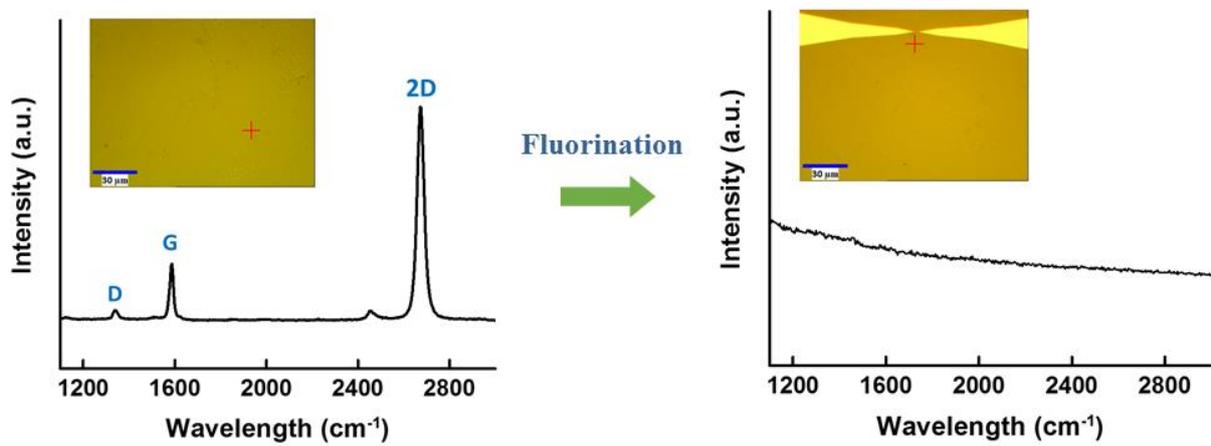
Figure 3.21 The single spectra of Raman spectroscopies of graphene and FG.

Graphene

SiO$_2$

Silicon Substrate

O$_2$ Plasma Etching

↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓

Metal Mask

**Contact Metal
(Ti/Au 100/500 Å)**

Fluorination

↓↓↓↓↓↓

PMMA

Fluorinated-Graphene
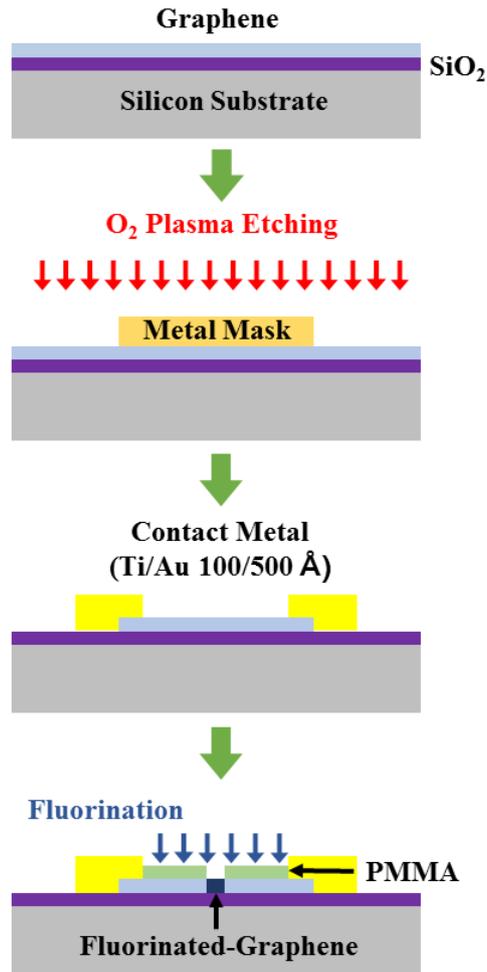
Figure 3.22 Fabrication process of graphene/FG/graphene tunnel junction on SiO$_2$/Si substrate (Method 2).
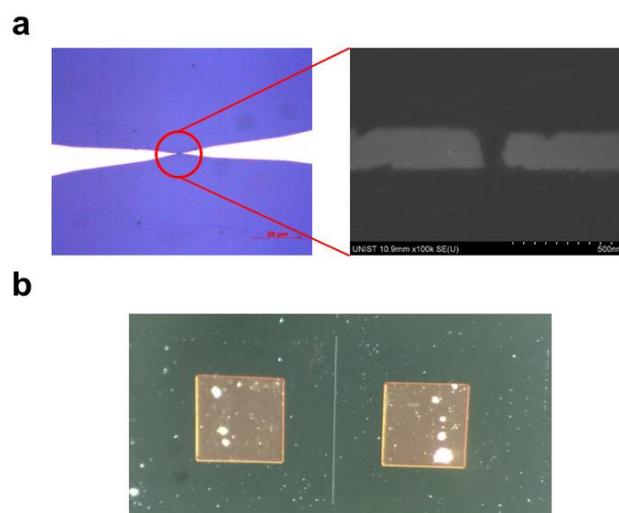
Figure 3.23 (a) The optical microscope and scanning electron microscope (SEM) images of Graphene/FG/Graphene tunnel device using "Method 1". (b) The optical microscope image of Graphene/FG/Graphene tunnel device using "Method 2".

3.3.2 Current-Voltage (I-V) Characteristics

The current-voltage (I-V) measurement of fabricated Graphene/FG/Graphene lateral tunnel junction was performed to investigate the junction characteristics. In Fig. 3.24, the I-V curves of graphene lateral tunnel junction with "Method 1" and "Method 2" are represented. With the first fabrication method, the tunnel junction has the asymmetric I-V curve as shown in Fig. 3.24a. Considering the slope of both positive and negative bias voltage in the increasing regions, it has similar tunneling mechanisms. However, the turn-on voltage can be slightly different in positive and negative bias cases. This phenomenon can be explained by the local charge density of graphene. In Fig. 3.8 (Section 3.1.3), the Raman mapping data shows the local charge density can be varied in space even in the dry transferred graphene. In the "Method 1", the tunnel junction width is very narrow as shown in Fig. 3.23. Thus, the initial doping concentration of graphene under the two electrodes can be different from each other. In that case, the energy barrier can be changed by the polarity of bias voltage as depicted in Fig. 3.25. When the left graphene is more p-doped compared to the right graphene, the energy barrier at a positive bias voltage on the right electrode (ϕ_{BP}) is smaller than the negative bias case (ϕ_{BN}). Therefore, the turn-on voltages of positive and negative bias cases are different as shown in the I-V curve. However, we can consider that the graphene/FG interface characteristics of both sides are similar because the slopes of the increasing region are almost same.

On the other hand, the I-V curve of "Method 2" is symmetric with the polarity of bias voltage. This characteristic also supports the effect of the local charge density effect in the previous case. In this method, the width of the tunnel barrier is quite long enough to ignore the local charge density since the overall doping is similar in space. Moreover, the tunneling current is much higher than the "Method 1" due to the wider tunnel barrier. In result, we can estimate the tunnel barrier and energy band alignment using this clear I-V curve in the following section.
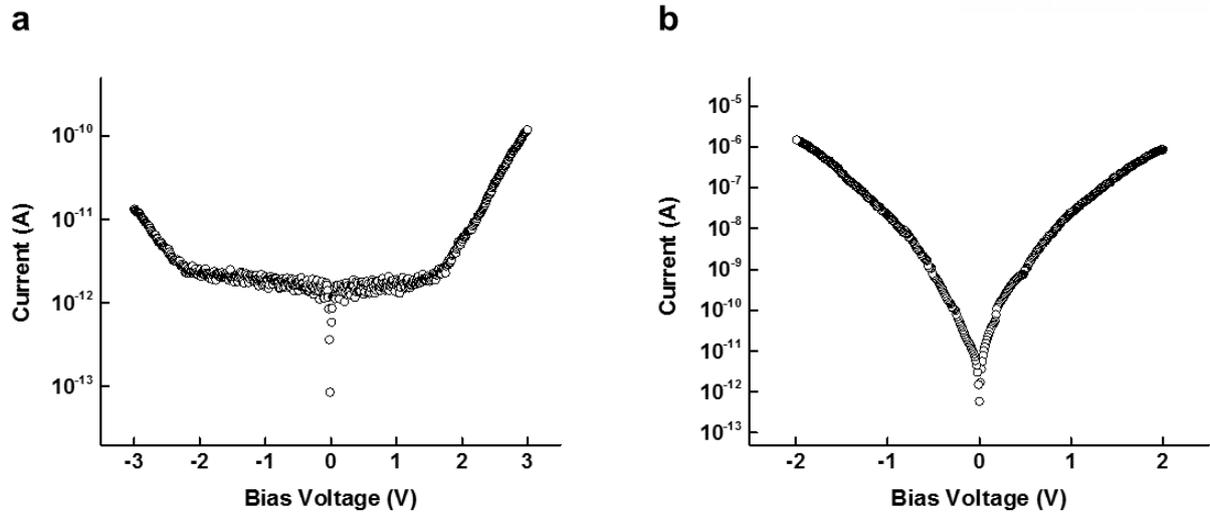
Figure 3.24 Current-voltage characteristics of lateral Graphene/FG/Graphene tunnel junction with (a) "Method 1" and (b) "Method 2".
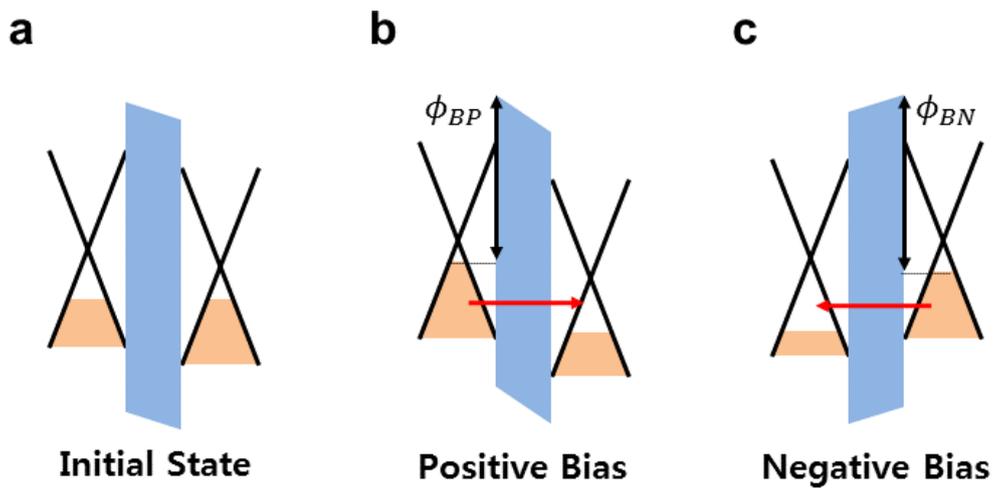
Figure 3.25 The energy band diagrams of graphene lateral tunnel junction with "Method 1" at (a) Initial state without any bias voltage, (b) positive bias voltage applied, and (c) negative voltage applied.

3.3.3 Energy Band Extraction by Thermionic Emission and Tunneling Model

Based on the current-voltage characteristic of Graphene/FG/Graphene tunnel junction, the energy band alignment was extracted by both thermionic emission and tunneling model. Since we have two-dimensional lateral junction, the thermionic emission current was derived from the current density equation [94].

$$J_{therm} = \int q n(E) v_x(E) dE \tag{3.22}$$

Here, q is the electron charge, $n(E)$ the electron density, and $v_x(E)$ the electron velocity. The electron density can be expressed as the product of Fermi-Dirac distribution ($f(E)$) function and density of states ($g(E)$).

$$n(E) = g(E) f(E) \tag{3.23}$$

Generally, the density of states in two-dimension can be expressed as

$$g(E) = \frac{m}{\pi \hbar^2} \sigma(E - E_c) \tag{3.24}$$

where m is the effective mass of the electron, $\hbar$ the reduced Planck's constant, σ the step function, and E_c the conduction band energy. Considering only the electron can contribute to the current, the electron energy should be larger than the conduction band energy (E_c). The Fermi-Dirac distribution function is

$$f(E) = \frac{1}{1 + \exp\left(\dfrac{E - E_F}{k_B T}\right)} . \tag{3.25}$$

Here, E_F is the fermi energy, k_B the Boltzmann's constant, and T the temperature. In thermionic emission, the electron should have the energy larger than the energy barrier so that the electron energy (E) is much larger than the fermi energy (E_F). Therefore, the Fermi-Dirac distribution function can be approximated by a simple exponential function like below.

$$f(E) = \exp\left(-\frac{E - E_F}{k_B T}\right) \tag{3.26}$$

Now, substituting Eq. 3.24 and 3.26 into 3.23, the Eq. 3.23 becomes

$$n(E) = \frac{m}{\pi \hbar^2} \exp\left(-\frac{E - E_F}{k_B T}\right) . \tag{3.27}$$

Then, the current density equation (Eq. 3.22) can be expressed as

$$J_{therm} = \frac{qm}{\pi\hbar^2}\int v_x(E)\exp\left(-\frac{E-E_F}{k_BT}\right)dE . \tag{3.28}$$

Here, we can change the variable E as velocity of the electron (v) to simplify the Eq. 3.28.

$$E = \frac{1}{2}mv^2 \iff dE = mvdv \tag{3.29}$$

Substituting Eq. 3.29 into Eq. 3.28,

$$\begin{aligned}
J_{therm} &= \frac{qm}{\pi\hbar^2}\int v_x(E)\exp\left(-\frac{E-E_F}{k_BT}\right)mvdv \\
&= \frac{qm^2}{2\pi^2\hbar^2}\exp\left(\frac{E_F}{k_BT}\right)\int v_x(E)\exp\left(-\frac{E}{k_BT}\right)2\pi vdv \\
&= \frac{qm^2}{2\pi^2\hbar^2}\exp\left(\frac{E_F}{k_BT}\right)\int v_x(E)\exp\left(-\frac{mv_x^2}{2k_BT}\right)\exp\left(-\frac{mv_y^2}{2k_BT}\right)dv_xdv_y \\
&= \frac{qm^2}{2\pi^2\hbar^2}\exp\left(\frac{E_F}{k_BT}\right)\int_{v_{min}}^{\infty} v_x(E)\exp\left(-\frac{mv_x^2}{2k_BT}\right)dv_x\int_{-\infty}^{\infty}\exp\left(-\frac{mv_y^2}{2k_BT}\right)dv_y
\end{aligned} \tag{3.30}$$

Here, v_{min} is the minimum electron energy corresponding to the minimum electron energy which is same as the sum of fermi energy and energy barrier (ϕ_B).

$$\phi_B + E_F = \Phi_m - \chi_{ins} + E_F = \frac{1}{2}mv_{min}^2 \tag{3.31}$$

The energy barrier (ϕ_B) is the difference between metal workfunction (Φ_m) and electron affinity of the insulator (χ_{ins}). The first integral becomes

$$\begin{aligned}
\int_{v_{min}}^{\infty} v_x(E)\exp\left(-\frac{mv_x^2}{2k_BT}\right)dv_x &= \left[-\frac{k_BT}{m}\exp\left(-\frac{mv_x^2}{2k_BT}\right)\right]_{v_{min}}^{\infty} \\
&= \frac{k_BT}{m}\exp\left(-\frac{mv_{min}^2}{2k_BT}\right) \\
&= \frac{k_BT}{m}\exp\left(-\frac{E_F+\phi_B}{k_BT}\right)
\end{aligned} \tag{3.32}$$

The second integral is the general form of Gaussian integral,

$$\int_{-\infty}^{\infty}\exp\left(-Ax^2\right)dx = \sqrt{\frac{\pi}{A}} . \tag{3.33}$$

Then, it becomes

$$\int_{-\infty}^{\infty}\exp\left(-\frac{mv_y^2}{2k_BT}\right)dv_y = \sqrt{\frac{2k_BT\pi}{m}} . \tag{3.34}$$

49

Finally, substituting Eq. 3.32 and 3.34 into Eq. 3.30

$$
\begin{aligned}
J_{therm} &= \frac{qm^2}{2\pi^2\hbar^2}\exp\left(\frac{E_F}{k_BT}\right)\frac{k_BT}{m}\exp\left(-\frac{E_F+\phi_B}{k_BT}\right)\sqrt{\frac{2k_BT\pi}{m}} \\
&= \frac{2q}{h^2}\left(k_BT\right)^{3/2}\left(2m\pi\right)^{1/2}\exp\left(-\frac{\phi_B}{k_BT}\right)
\end{aligned}
\tag{3.35}
$$

This is the final equation of thermionic emission current density in 2-dimensional lateral junction. Considering the image force lowering, the ϕ_B can be rewritten as the maximum value of the energy barrier of the insulator (ϕ_B'). The image potential can be expressed as

$$
V_{image} = -\frac{0.288d}{\varepsilon_{ins}x(d-x)}
\tag{3.36}
$$

where d is the insulating layer thickness in nanometer scale, and ε_{ins} the dielectric constant of insulating layer [95]. Then, the total potential energy of the insulating layer is

$$
\phi_B' = \phi - eV_b\frac{x}{d} - \frac{0.288d}{\varepsilon_{ins}x(d-x)}
\tag{3.37}
$$

where V_b is the bias voltage between two electrodes. With this potential barrier, the maximum value of ϕ_B' was chosen to be our energy barrier (ϕ_B) in the Eq. 3.35. Finally, we can get the thermionic emission current density in 2-dimensional lateral junction.

The 2-dimensional tunnel current density was calculated by Simmons tunneling equation [96] and WKB method. The number of electron tunnel through the insulating barrier (N) can be expressed as

$$
N = \int_0^{v_m} v_x n(v_x) D(E_x) dv_x
\tag{3.38}
$$

where v_m is the maximum velocity of the electron in x-direction, $n(v_x)$ the electron number density, $D(E_x)$ the tunneling probability obtained by WKB method. Here, the maximum velocity is same as the minimum velocity at thermionic emission electron because the tunneling should be happened only when the electron energy is lower than the energy barrier.

$$
\phi_B + E_F = \Phi_m - \chi_{ins} + E_F = \frac{1}{2}mv_{max}^2
\tag{3.39}
$$

The electron number density can be derived from the number of states in k-space.

$$
\#\text{ of states } = 2\times\frac{\left(\dfrac{dk_x}{2}\right)\left(\dfrac{dk_y}{2}\right)}{\left(\dfrac{\pi}{L}\right)^2}\times\frac{1}{L^2} = \frac{1}{2\pi^2}\times\left(\frac{m}{\hbar}\right)^2\times dv_x dv_y
\tag{3.40}
$$

$$n(v)dv_x dv_y = \frac{1}{2\pi^2}\left(\frac{m}{\hbar}\right)^2 dv_x dv_y \times f(E) \qquad (3.41)$$

$$n(v_x) = \int_{-\infty}^{\infty} n(v)dv_y = \frac{1}{2\pi^2}\left(\frac{m}{\hbar}\right)^2 \int_{-\infty}^{\infty} f(E)dv_y$$

$$= \frac{1}{2\pi^2}\left(\frac{m}{\hbar}\right)^2 \int_{-\infty}^{\infty} \frac{1}{1+\exp\left(\dfrac{E_F - E_x - mv_y^2/2}{k_B T}\right)} dv_y \qquad (3.42)$$

Here, we integrate the Fermi-Dirac distribution function as dv_y because the change of variable by E_y makes divergence near $E_y \approx 0$.

Lastly, the tunneling probability can be expressed as

$$D(E_x) = \exp\left\{-\frac{4\pi}{h}\int_0^d \sqrt{2m(V(x)-E_x)}dx\right\}. \qquad (3.43)$$

Finally, the number of electrons tunnel through from the source to drain side (N_1) can be expressed as

$$N_1 = \int_0^{v_m} v_x n(v_x) D(E_x) dv_x$$

$$= \frac{m}{2\pi^2 \hbar^2} \int_0^{E_m} \exp\left\{-\frac{4\pi}{h}\int_0^d \sqrt{2m(V(x)-E_x)}dx\right\} \int_{-\infty}^{\infty} \frac{1}{1+\exp\left(\dfrac{E_F - E_x - mv_y^2/2}{k_B T}\right)} dv_y dE_x. \qquad (3.44)$$

Similarly, the number of electrons from the drain to source side is

$$N_2 = \frac{m}{2\pi^2 \hbar^2} \int_0^{E_m} \exp\left\{-\frac{4\pi}{h}\int_0^d \sqrt{2m(V(x)-E_x)}dx\right\} \int_{-\infty}^{\infty} \frac{1}{1+\exp\left(\dfrac{E_F - E_x - mv_y^2/2 + eV_b}{k_B T}\right)} dv_y dE_x \qquad (3.45)$$

Then, the final tunnel current density can be written as

$$J_{tunnel} = e(N_1 - N_2). \qquad (3.46)$$

The integrals in the Eq. 3.44 and 3.45 were solved by mensuration by parts with the aid of MATLAB. In result, we can calculate both thermionic emission current and tunnel current for specific energy barrier and thickness. By comparing our measurement result with these calculated current, the energy barrier of Graphene/FG/Graphene junction was estimated.

51
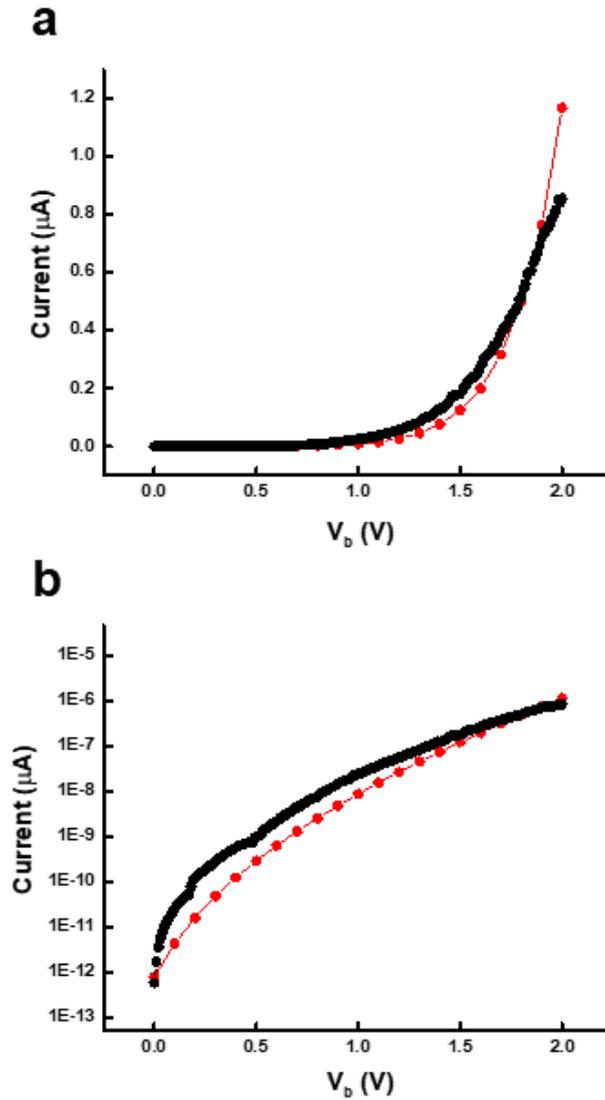
Figure 3.26 Current-voltage characteristics of graphene/FG/graphene tunnel junction in (a) linear and (b) log scale. The black curve indicates the measurement result and the red line represents the theoretically calculated current which is the sum of thermionic emission and quantum mechanical tunneling current.

As shown in Fig. 3.26, the measured current (black line) and the calculated total current (red line) are plotted. Since we fabricated the tunnel junction with several tens of nanometer scale, the thickness of the tunnel barrier can be varied in that scale. Therefore, the tunneling and thermionic emission currents were calculated with the several thickness and energy barrier of the tunnel insulator. We found that the total current with 10 nanometer thickness and 0.8 eV energy barrier of FG is well matched with the measured current. In result, we can estimate the thickness and the energy barrier of tunnel insulator by comparing the current-voltage characteristics.

IV. Ferroelectric Memory Device

4.1 Edge-Metal-Insulator-Metal (EMIM) Tunnel Junction

4.1.1 Device Structure

The Edge-Metal-Insulator-Metal (EMIM) tunnel junction is a lateral metal-insulator-metal tunnel junction by using thin film processes. Figure 4.1a and 1b shows the 3-D schematic of EMIM structure and cross sectional view [97]. The materials for EMIM junction are Ni (Metal 1, 60 nm), SiO_2 (Insulator 1 and 2, 300 and 30 nm each), Ni/Au (Metal 2, 30/80 nm), and SiC (Tunnel Insulator, 10 nm). Here, the "Insulator 2" is the blocking insulator which is to enforce the current flow from "Metal 2" to "Metal 1" only in lateral direction not in vertical direction. The yellow dashed rectangles represent the EMIM junctions where most current flows. The intrinsic SiC was chosen by the tunnel insulator because the amorphous SiC has wide bandgap.

4.1.2 Fabrication Process

The SiO_2/Si substrate is clean with acetone and methanol by using ultra-sonic agitation. First, metal pattern is formed by using photolithography. HMDS (AZ AD Promoter-K) and photoresist (AZ5214E) are sequentially spin-coated at the speed of 3000 rpm for 30 seconds and baked on the hot plate at 105° C for 90 seconds. The photolithography process is performed with a mask aligner (MA6, SUSS MicroTec, Germany) and the sample is developed in MIF 300. After rinsing the sample with distilled water, the "Metal 1" is deposited by using e-beam evaporator (FC-200, Temescal, USA). Next, the "Insulator 2" is deposited with RF magnetron sputtering (SRN-120D, SORONA, Korea). Then, the sample is dipped into the acetone for a lift-off process. Competing the "Metal 1" and "Insulator 2" stacked pattern, a SiC film is deposited on the whole area of the sample with PECVD (Plasma Enhanced Chemical Vapor Deposition) system. Next, the "Metal 2" pattern is formed in the same manner of the previous photolithography process except for the deposition of "Insulator 2" layer. Finally, the "Metal 1" contact pad is exposed by using photolithography and etching process by using the dielectric reactive ion etching system (Labstar, Top Technology Ltd, Korea). The fabrication processes are depicted in Fig. 4.2.
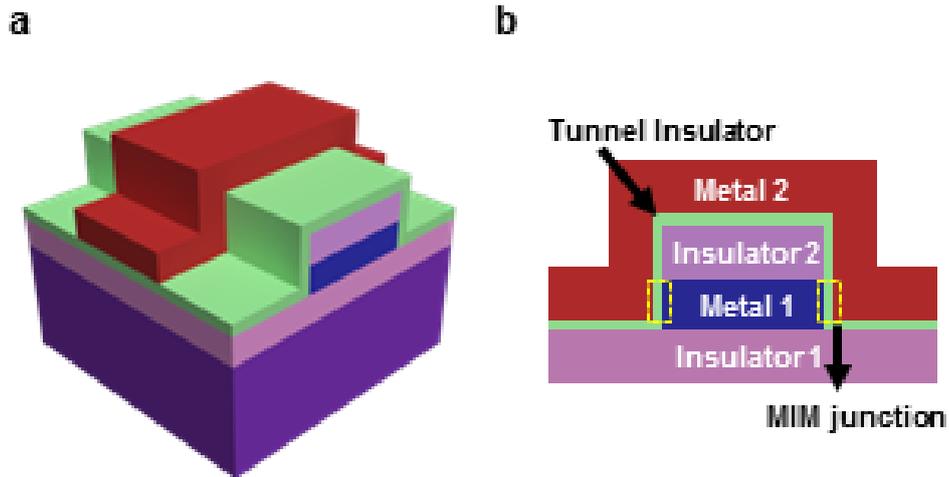
Figure 4.1 The schematic of EMIM junction in (a) 3D view and (b) cross-sectional view [97].
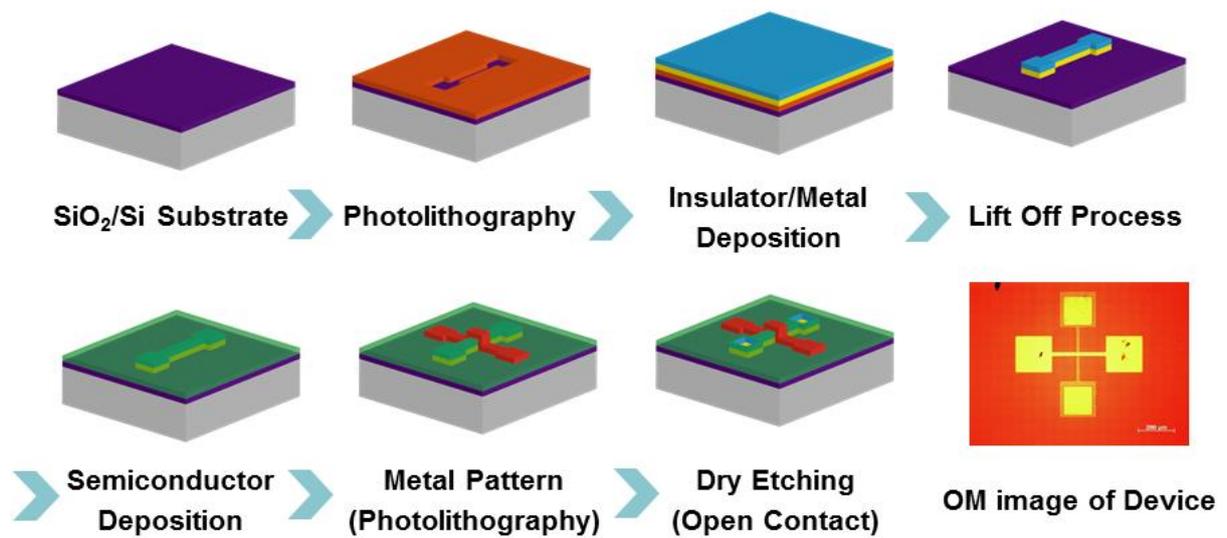
Figure 4.2 Fabrication processes of EMIM junction on SiO$_2$/Si substrate. The last image is the optical microscope (OM) image of the fabricated EMIM device.

4.1.3 Current-Voltage (I-V) Characteristic

Since the amorphous SiC is inserted between two metal electrodes, the current-voltage (I-V) characteristics of EMIM junction is expected to be similar to the conventional metal-insulator-metal junction. In Fig. 4.3a, I-V characteristics of EMIM junction on SiO_2/Si substrate is shown. The I-V curve increases with nonlinearity. The first and second derivatives of I-V curves are also depicted in Fig. 4.3b and 3c. The derivatives were calculated by using Savitzky-Golay smooth in Origin. Here, we can confirm again that the EMIM junction is a nonlinear device.

4.1.4 THz Detector Application

One of the special characteristics of EMIM junction is that the junction area can be controlled by the film thickness. In other words, the junction area can be significantly reduced by the few or tens of nanometer. Metal-insulator-metal junction with a small junction area have been utilized for THz detector because it has small RC delay and high cut-off frequency [98]. Therefore, we decided to measure the terahertz (THz) response of our EMIM device.

THz detectors are now being used in a security system in the airport, imaging for medical purpose, and non-destructive inspection in the various area [99-104]. The THz wireless communication is also a significant research area because of its fast speed of data transmission [105-107]. Thus, not only the THz transmitter, THz detector should be studied for developing THz wireless communication. However, the limitation of the THz communication is that the THz wave is attenuated by water molecules in the atmosphere [105, 108]. Nevertheless, the THz with specific frequencies have been revealed to be propagated long distances in atmosphere condition [109-112]. Up to now, the THz detector studies have been performed with using FET structure or diode type [98, 113-118]. Among the FET type THz detector, GFET THz detector is recently studied much due to the short response time because a graphene has higher carrier mobility than silicon or other semiconductors [14-16]. Besides, the diode type THz detectors are based on the Schottky diode or metal-insulator-metal tunnel diode [119-122]. The diode type THz detectors usually utilize the nonlinearity of I-V characteristics as described in Fig. 4.4. As shown in Fig. 4.4, the voltage can oscillate with THz beam and the induced current is also fluctuated. Even if the voltage change is same for the decrease and increase from the V_b, the induced current at each side is different due to the nonlinear I-V characteristic. The difference of induced current generates the rectified voltage across the junction [123, 124]. The rectified DC voltage of EMIM junction at an external oscillating field can be derived like below.
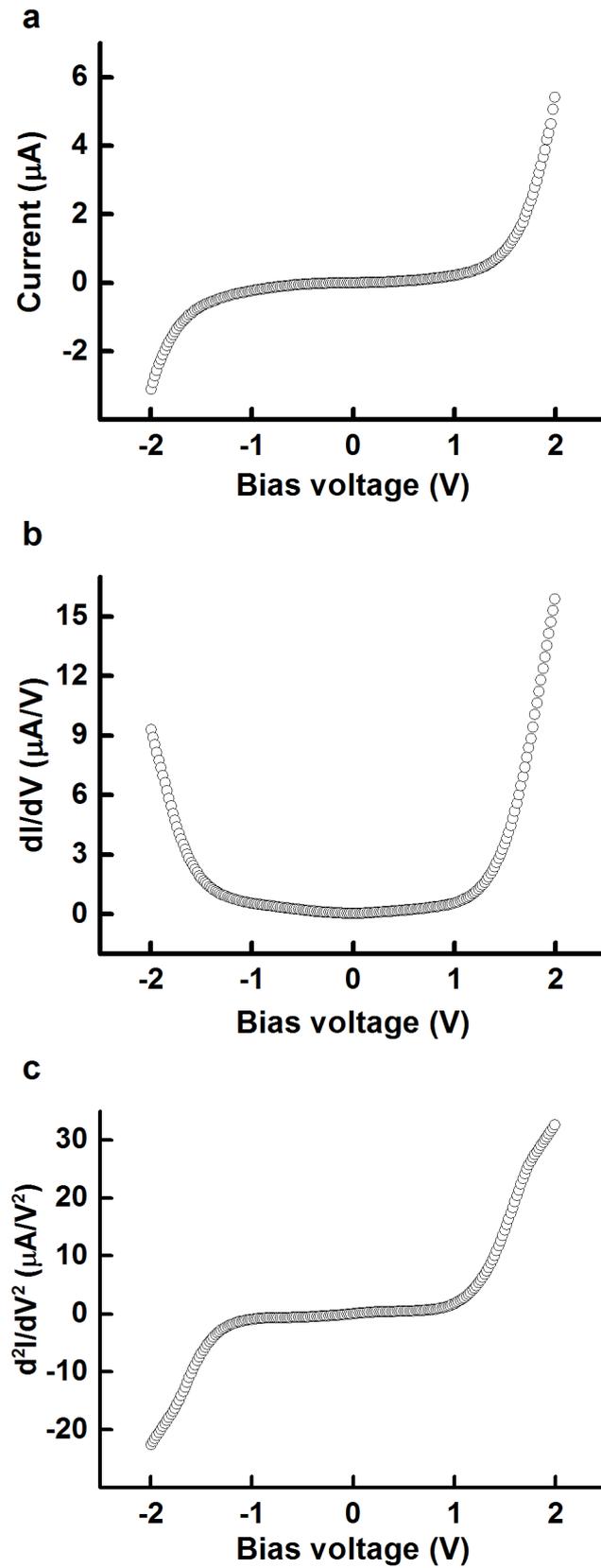
Figure 4.3 (a) I-V curve of EMIM junction. (b) The first derivative and (c) second derivative of I-V curve [97].
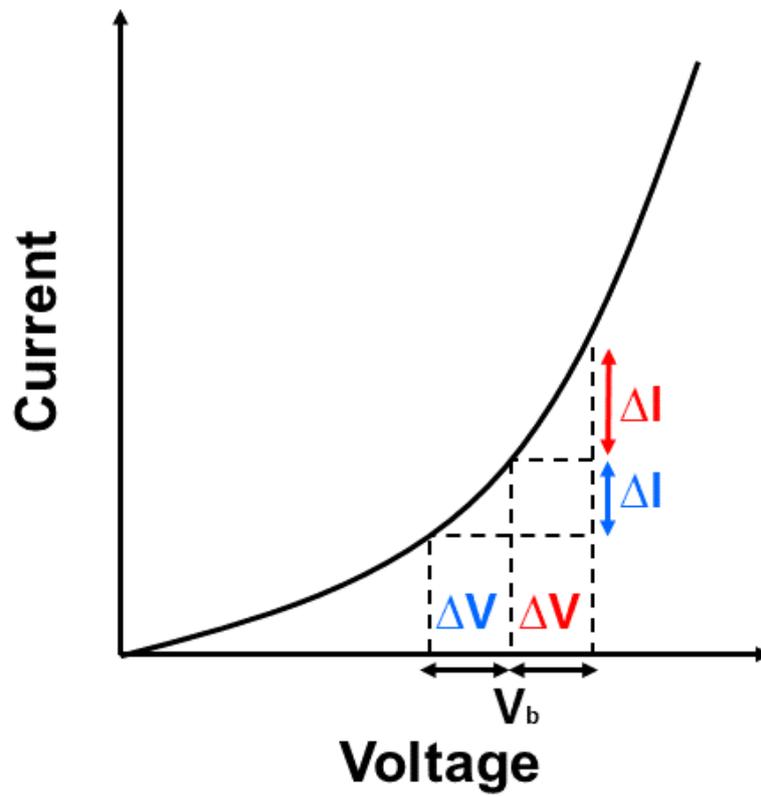
Figure 4.4 Nonlinear current-voltage characteristics for application in THz detector. The voltage oscillation around V_b is depicted and corresponding current change is expressed.

Considering the applied DC voltage (V_b) and the oscillating voltage due to the THz beam, the total amount of voltage can be expressed as

$$V = V_b + V(t) = V_b + V_0 \cos(\omega t) \qquad (4.1)$$

where V_b is the applied voltage, V_0 the magnitude of oscillating voltage, and ω the angular frequency. Using Taylor expansion,

$$I(V) = I(V_b) + \left.\frac{dI}{dV}\right|_{V=V_b} V(t) + \frac{1}{2}\left.\frac{d^2 I}{dV^2}\right|_{V=V_b} V^2(t) + \cdots \qquad (4.2)$$

The time average of current can be calculated with the second order term because the magnitude of oscillating voltage (V_0) is small enough for neglecting the first order term.

$$\begin{aligned}
I_{avg} &\approx \frac{1}{2\pi} \int_{-\pi}^{\pi} \left[I(V_b) + \left.\frac{dI}{dV}\right|_{V=V_b} V(t) + \frac{1}{2}\left.\frac{d^2 I}{dV^2}\right|_{V=V_b} V^2(t) \right] d(\omega t) \\
&\approx I(V_b) + \frac{1}{4}\left.\frac{d^2 I}{dV^2}\right|_{V=V_b} V_0^2
\end{aligned} \qquad (4.3)$$

Here, the second term is the additional term due to the oscillating field induced by the THz beam. Therefore, the second term means the rectified current (I_{rec}).

$$I_{rec} = \frac{1}{4}\left.\frac{d^2 I}{dV^2}\right|_{V=V_b} V_0^2 \qquad (4.4)$$

Then, the rectified voltage (V_{rec}) can be just dividing the rectified current by the resistance.

$$V_{rec} = \frac{I_{rec}}{dI/dV} = \frac{1}{4}\frac{I''}{I'} V_0^2 \qquad (4.5)$$

As described in the Eq. 4.5, the rectified voltage is proportional to the second derivative, inverse of the first derivative and square of oscillating voltage magnitude. The junction characteristics are the first and second derivatives and the THz beam properties are also included in the magnitude of the oscillating field.

The experimental set-up for THz detecting system using the EMIM junction is shown in Fig. 4.5. The THz beam source was a continuous wave (CW) sub-THz gyrotron and the generated THz beam was focused on the sample by using off-axis parabolic (OAP) mirrors. Here, the THz beam frequency was selected to 0.4 THz because it is one of the frequencies propagating a long distance in the air with less attenuation [105, 106]. The reflected THz beam transmitted through the chopper before reaching to the sample. This chopper frequency is 200 Hz which is much lower than the THz beam. The sample is also connected to the read-out circuit as shown in Fig. 4.5. In the read-out circuit, the lock-in amplifier is connected to the sample output node and the chopper. The detailed explanation about the principle of measurement is as follow.

First, we used the lock-in technique to minimize the noise signal. The rotating chopper makes THz beam has 200 Hz frequency and its frequency information is transmitted to the lock-in amplifier. Then, the output signal from the read-out circuit is the sum of the rectified voltage induced by the THz beam and other noise signals. However, the rectified voltage has a frequency of 200 Hz because the THz beam also has chopper frequency. The lock-in amplifier amplifies only the signal having reference frequency (f_{ref}). Mathematically, the sinusoidal function with reference frequency is multiplied by the input signal and integrated with time. Therefore, the actual response voltage ($V_{response}$) can be expressed with the output voltage (V_{out}) of the read-out circuit as

$$V_{response} = \frac{1}{T} \int_{t-T}^{t} \sin\left[2\pi f_{ref} \cdot s + \varphi \right] \cdot V_{out}(s) ds \tag{4.6}$$

where t is an arbitrary time and T is the period time corresponding the reference frequency ($T = 1/f_{ref}$). Unless the frequency is as same as the reference frequency, any sinusoidal functions must be eliminated in the Eq. 4.6. Therefore, the only surviving term is the rectified voltage induced by the THz beam.

Next, we used the resistor and capacitor in the read-out circuit. The reason for the necessity of the additional electric component is described. The EMIM junction can exist in two forms, one is a just resistor and the other is a parallel connection of capacitor and resistor as shown in Fig. 4.5b and 5c. When the THz beam is not irradiated to the EMIM junction, there is no induced current or charge across the junction. Thus, the EMIM junction acts as a resistor in the equivalent circuit without any external THz beam. In this case, there is no induced charge on the Node-A and results no voltage generation on the output capacitor (C_{out}). However, during the THz beam irradiation on EMIM junction, the rectified voltage is generated and the corresponding charge (Q) is accumulated across the junction. In this case, we can deal with the EMIM junction as a capacitor (C_j) and resistor (R_j) connected in parallel because it still has DC resistance and also the induced

across the junction.
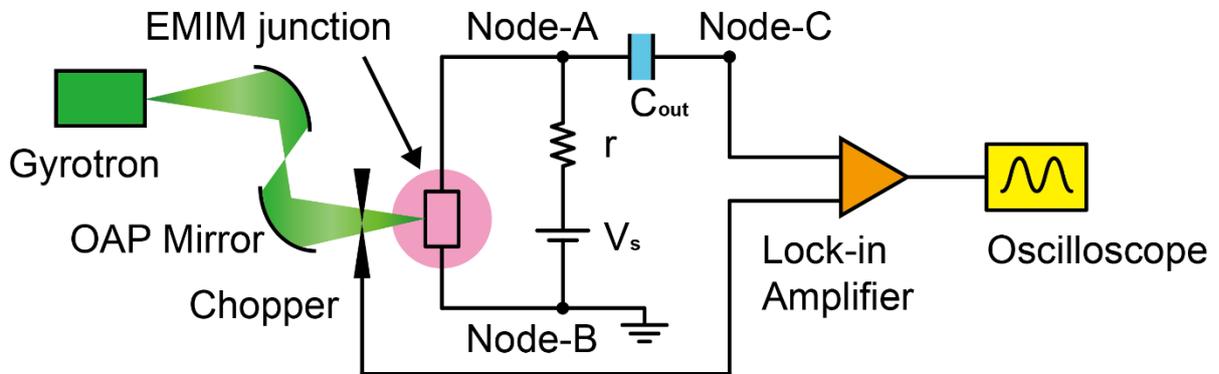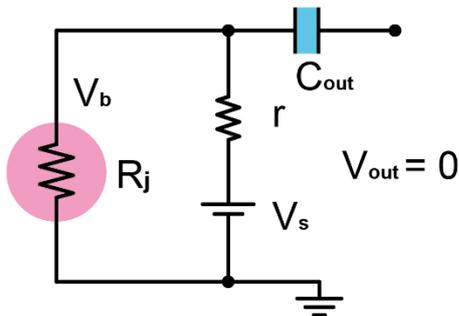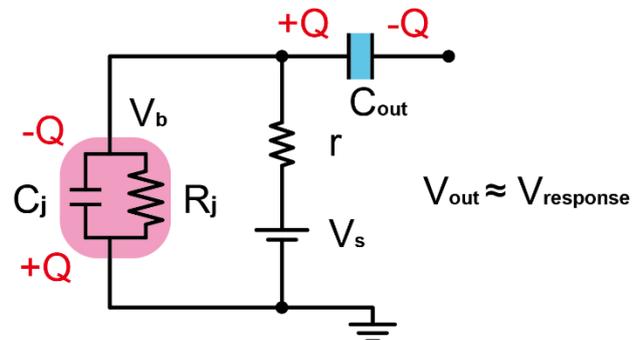
Figure 4.5 (a) THz detecting measurement set-up using lock-in technique. Equivalent read-out circuit (b) without and (c) with irradiated THz beam on EMIM junction. EMIM junction is expressed as a simple resistor in (b) and parallel connection of resistor and capacitor in (c) [97].

With an incoming THz beam, the EMIM junction has net negative charge ($-Q$) on the upper side and the positive charge ($+Q$) is induced on the lower side. At this moment, the same amount charge should be induced on the output capacitor (C_{out}) due to the charge neutrality. Therefore, the positive charge ($+Q$) is accumulated on the left side of output capacitor and the opposite charge ($-Q$) is induced on the right side. Now, the output voltage (V_{out}) is calculated by sum of the voltage of C_j and C_{out} because they are connected in series.

$$V_{out} = \frac{Q}{C_j} + \frac{Q}{C_{out}}$$ (4.7)

Here, comparing the magnitude of capacitance C_j (~8.14 fF) and C_{out} (~100 nF), C_j is much smaller. Thus, the voltage across the junction capacitance is dominant factor for determining the output voltage (V_{out}). Resultantly, V_{out} is almost same value as the voltage response (V_{rec}) of EMIM junction. This signal is amplified in the lock-in amplifier as described in the above.

In Fig. 4.6, the voltage response (V_{rec}) of EMIM junction with various beam power, polarization, and bias voltage are depicted. Since the square of oscillating voltage is proportional to the rectified voltage (V_{rec}), described in the Eq. 4.3, the voltage response increases as the THz beam power increases (Fig. 4.6a). Considering the dependence on junction characteristic, the larger bias voltage gives the bigger response as expected in the second derivative of I-V curve in Fig. 4.3c. The last variable of voltage response is the polarization direction of THz beam which is significant factor for THz detecting system. When the polarization direction of THz beam is perpendicular to the EMIM junction direction (parallel to the current flow direction), the induced charge is maximized (Fig. 4.6d). However, the polarization direction is parallel to the EMIM junction (perpendicular to the current flow direction), there is little rectified voltage because the electric field oscillation across the junction is hard to be happened. Therefore, the voltage response as a function of polarization direction degree has W-shaped curve. Noticing that the voltage responses at 0 and 180 degrees are different, there might be some misalignment of rotational axis of sample and THz beam. The THz beam from gyrotron is not perfectly symmetric as shown in Fig. 4.7. The simulation result profile and the measured profiles are depicted in Fig. 4.7 and the black circles are the boundaries of used in this experiment. The 0 degree was adjusted to the position where the voltage response is maximized. Thus, there can be a misalignment with THz beam and the EMIM junction because its size is very small (20 μm by 20 μm). Moreover, the asymmetry of THz beam power profile contributes to the misalignment.

a

b

c

d
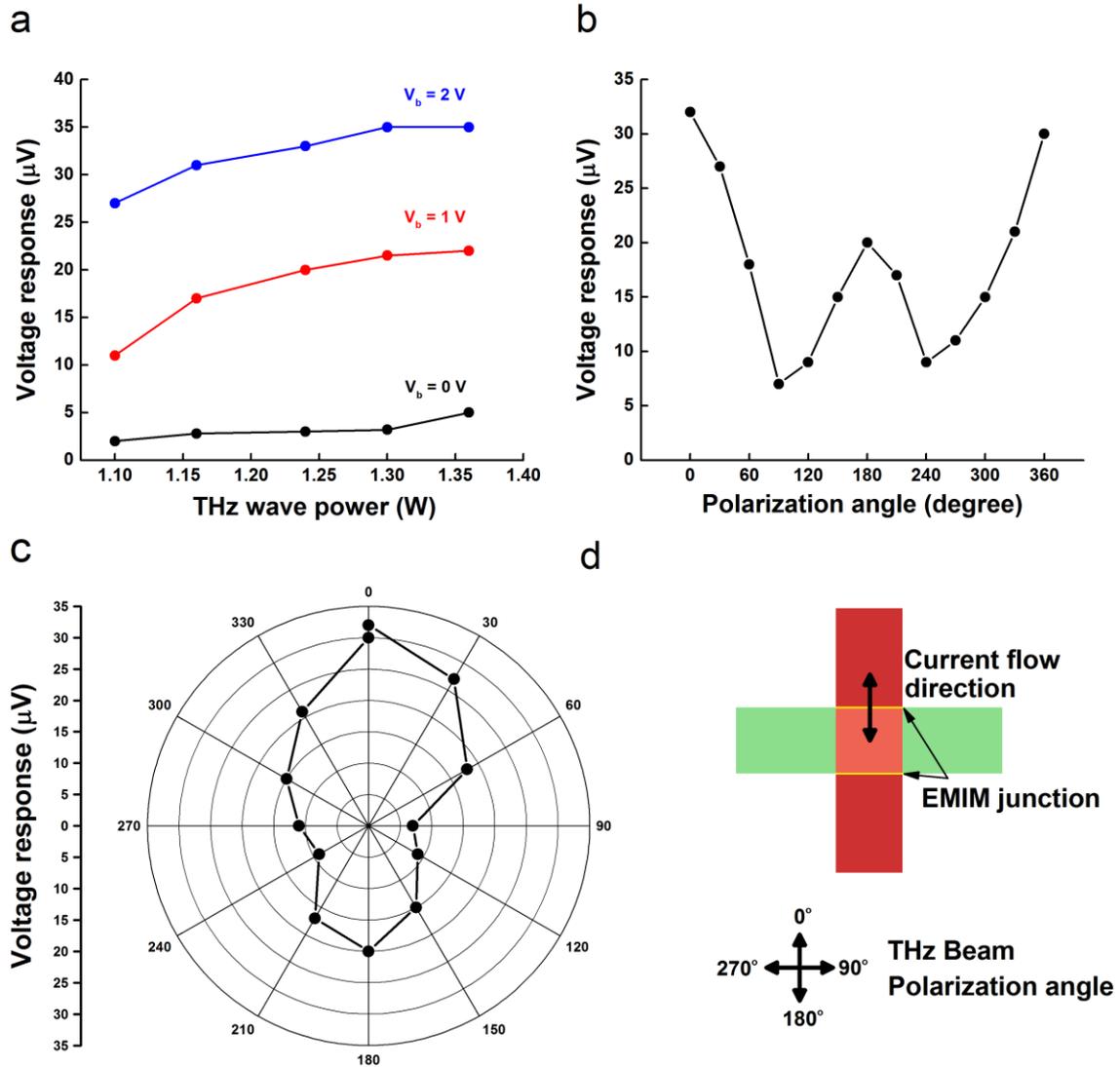
Figure 4.6 (a) The voltage response with various THz beam power and applied bias voltage. The voltage response depending on the THz beam polarization direction with (b) line plot and (c) contour plot. (d) Definition of the polarization angle of the THz beam with respect to the EMIM junction [97].
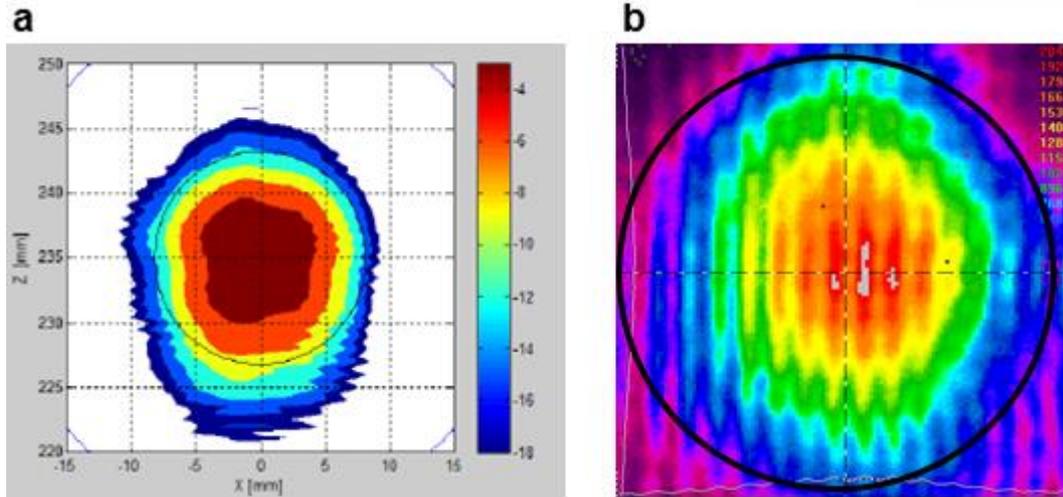
Figure 4.7 THz beam power profile in (a) simulation and (b) measurement result. The black circles represent the THz beam used in this experiment [97].

Based on the measurement of voltage response of EMIM junction, the responsivity and NEP (Noise Equivalent Power) was derived. The responsivity can be calculated by

$$\text{Responsivity } (R) = \frac{V_{response}}{P_{incident}} \qquad (4.8)$$

where $P_{incident}$ is the incident power on THz detector. In this experiment, we measured the power of THz detector with diameter of 15 mm (black circles in Fig. 4.7) and its value is about 1.1 W. The beam power per unit area is then 6,225 W/m^2. Therefore, the incident power on EMIM junction is approximately 1.25×10^{-8} W. The responsivity is derived from the measured voltage response and the estimated incident power. At 2 V bias voltage, the responsivity is about 2,169 V/W. Given that there is no antenna structure and signal amplifier in EMIM device, the responsivity is quite high compared to the other diode type THz detectors. For comparison, typically the Schottky diode THz detector with antenna has 500 V/W responsivity and tunnel diode detector has 1,150 V/W with antenna structure as shown in the Table 4.1 [125, 126]. The FET type THz detectors have 5000 V/W and 74 V/W for MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) and GFET with antenna structures [115, 127].

Lastly, the NEP is calculated by using the calculated responsivity. The meaning for NEP is the minimum detectable power per square root of frequency.

$$\text{NEP} = \frac{\text{Noise Spectral Density } (V / \sqrt{Hz})}{\text{Responsivity } (V / W)} \qquad (4.9)$$

The noise spectral density was obtained by the equation for Johnson noise [128]. The Johnson noise can be expressed as $\sqrt{4 k_B T R}$ where k_B is Boltzmann's constant, T temperature, and R the resistance of junction [129]. Since the resistance is varied in our EMIM junction, the differential resistance was adopted to calculate the noise spectral density. At 2 V bias voltage, the differential resistance is about 63.7 kΩ and the noise spectral density is 32.4 $nV / \sqrt{Hz}$ at 300 K. Corresponding NEP can be obtained as 14.9 $pW / \sqrt{Hz}$ by using Eq. 4.9. This is quite comparable to the other types of THz detectors as shown in the Table 4.1.

Table 4.1 Comparison of responsivity and NEP with other types of THz detectors [97]

	Schottky	Tunnel Diode	MOSFET	GFET	This Work
Responsivity (V/W)	500	1,150	5,000	74	2,169
	(@ 0.4 THz)	(@ 0.2 THz)	(@ 0.3 THz)	(@ 0.4 THz)	(@ 0.4 THz)
NEP $(pW / \sqrt{Hz})$	5	7	10	130	14.9
	(@ 0.4 THz)	(@ 0.2 THz)	(@ 0.3 THz)	(@ 0.4 THz)	(@ 0.4 THz)

4.2 EMIM Tunnel Junction on Ferroelectric Layer

4.2.1 Energy Band Profile of Tunnel Junction

The EMIM junction on SiO_2/Si substrate was applied to the THz detector as described in the previous section. In this part, we studied the theoretical modeling of EMIM junction on ferroelectric layer for memory device application.

Ferroelectric memory devices have been studied extensively using the spontaneous polarization of ferroelectric material as described in section 2.3.1. In case of metal/ferroelectric/metal tunnel junction, the energy band profile is expected to be changed abruptly relying on the polarization direction of ferroelectric and have large switching ratio of tunnel current [130-132]. Moreover, the ferroelectric FET structure has been studied for memory device [133-138]. However, the high-quality ferroelectric thin film is hard to grow with reliable operation.

In this study, theoretical modeling for calculating the current density of EMIM junction on ferroelectric layer was performed by using the finite element electrostatic modeling. The EMIM/Ferroelectric memory array is depicted in Fig. 4.8. The only difference between the THz detecting EMIM device and EMIM/Ferroelectric memory device is that the substrate is changed from SiO_2/Si to SiO_2/Ferroelectric. The materials we used in our EMIM/Ferroelectric memory device modeling are $Pb_{1.1}Zr_{0.35}Ti_{0.65}O_3$ (Ferroelectric layer, 400 nm, 25μC/cm^2 remnant polarization [139, 140]), SiO_2 (Insulator 1, 8 nm, Insulator 2, 20 nm), SiC (Tunnel insulator, 10 nm), and Pt (Source, 30 nm, Drain, 30 nm, Writing electrode, 30 nm, 5.1 eV workfunction [141, 142]). The specifications of materials such as thickness, dielectric constant, and electron affinity are described in Table 4.2 [94, 140, 143-145].

Table. 4.2 Thickness, dielectric constant, and electron affinity used in EMIM/Ferroelectric memory structure [146]

	Thickness (nm)	Dielectric Constant	Electron Affinity (eV)
Ferroelectric layer ($Pb_{1.1}Zr_{0.35}Ti_{0.65}O_3$)	400	350	3.5
Insulator 1 (SiO_2)	8	3.9	0.9
Insulator 2 (SiO_2)	20	3.9	0.9
Tunnel Insulator (SiC)	10	4.6	3.85

With these parameters, the energy band profile of tunnel insulator is calculated by using FlexPDE [147]. In Fig. 4.9, the FlelxPDE modeling result with mesh size is represented. Here, Poisson's equation [148] is applied with dielectric constant of tunnel insulator (ε_i).

$$\nabla^2 \left(\frac{\phi}{-q} \right) = -\frac{\rho}{\varepsilon_i \varepsilon_0} \tag{4.10}$$

After solving the Poisson's equation (Eq. 4.10), the electrostatic potential energy for electrons (ϕ) is obtained and the total electrostatic potential (ϕ_{tot}) is calculated with Eq. 4.11

$$\phi_{tot} = \phi + \left(W_m - \chi_i \right) \tag{4.11}$$

In this equation, the metal workfunction (W_m) and electron affinity of tunnel insulator (χ_i) are included to adjust the reference of electrostatic potential.
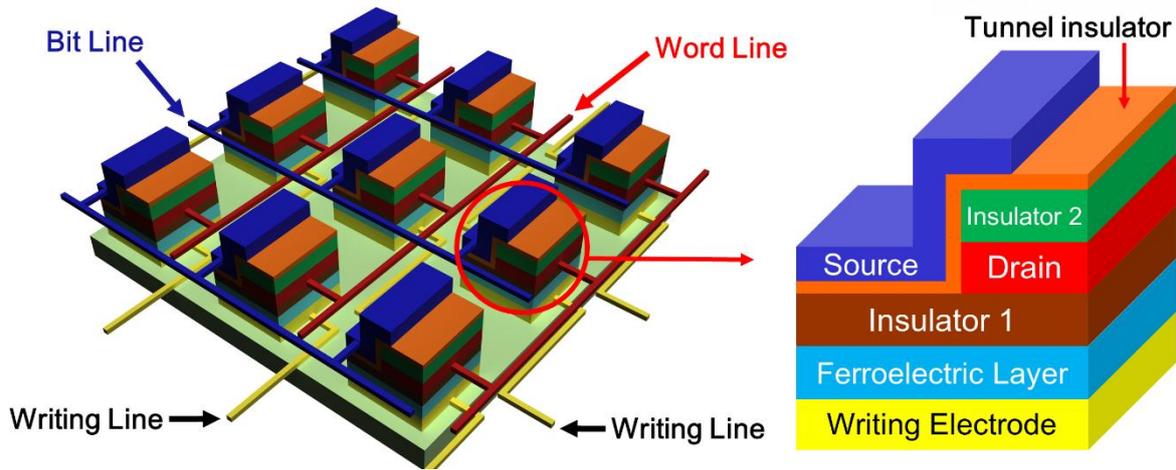
Figure 4.8 EMIM/Ferroelectric memory cell array and zoom-in of one memory cell. Word lines and bit lines are positioned in perpendicular to each other. The writing lines are the diagonal direction to the memory cell array [146].
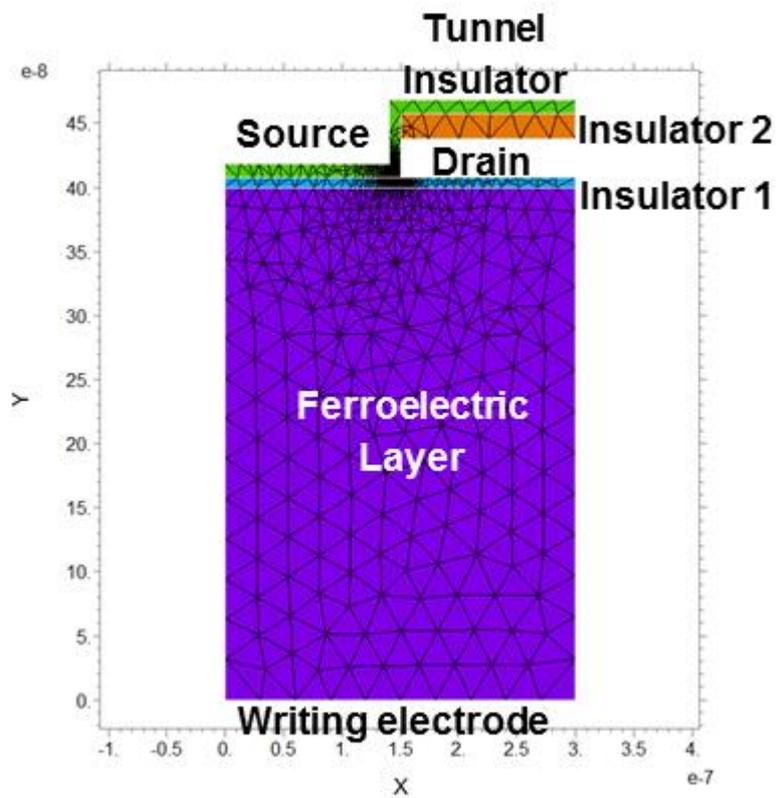
Figure 4.9 Finite element electrostatic modeling by using FlexPDE solution package. The triangles with black lines are the mesh for calculation.

In Fig. 4.10, the calculated energy band diagram shows the significant change by the polarization direction of underlying ferroelectric layer. At zero source-drain bias, the energy band of tunnel insulator shows valley shape in case of upward polarization (Fig. 4.10b) and ridge shape in opposite case (Fig. 4.10c). However, we can also notice that the energy band far away from the ferroelectric layer is almost flat because the induced surface charges on ferroelectric layer cannot affect much on that region. One more thing we should notice is the role of "Insulator 1" which is blocking the leakage current from the ferroelectric layer to source and drain electrodes and adjusting the screening effect. Considering the fringe field effect abruptly decreases with distance, the thickness and dielectric constant of "Insulator 1" is very important factor for energy band change in tunnel insulator.
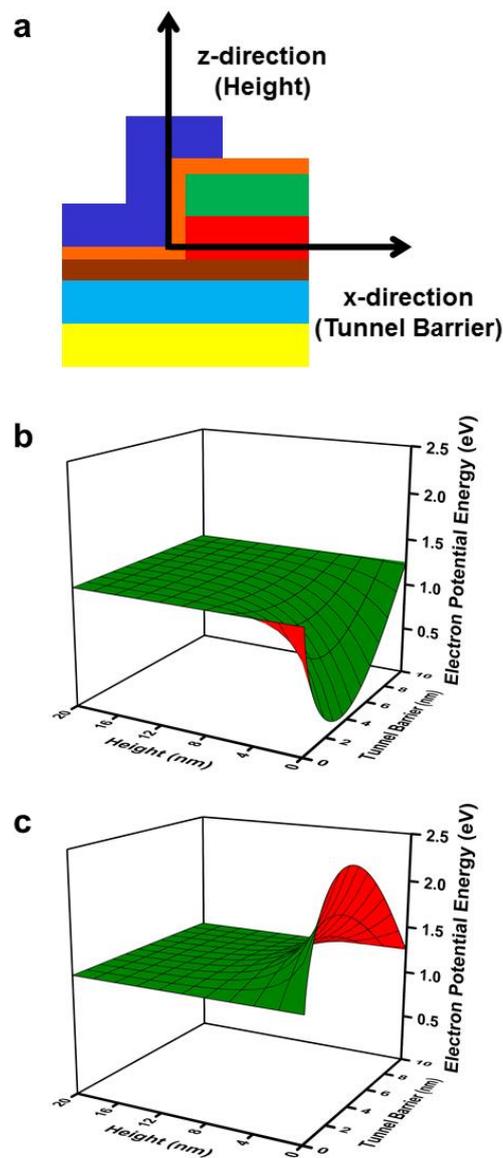
Figure 4.10 (a) Coordination of EMIM junction. Energy band profile of tunnel insulator with polarization (b) up-state and (c) down-state [146].

4.2.2 Tunnel Current Density Calculation with Transfer Matrix Method

After obtaining the energy band profile of tunnel insulator, the tunnel current density was calculated. In this calculation, the transfer matrix method [149-151] is used for calculating the tunneling probability. First, we started from the Schrödinger equation [152] as below.

$$\left[-\left(\hbar^2/2\right)\partial_x\left(1/m^*\right)\partial_x +V(x)-E_x\right]\psi(x)=0 \tag{4.12}$$

In the above equation, $\hbar$ is the reduced Plank's constant, m^* the effective mass of electron, $V(x)$ the potential energy, and E_x the x-directional electron energy. The x-direction is the perpendicular direction of EMIM junction as described in Fig. 4.10a. We divide the energy band profile of tunnel insulator in "N" segments with having the width of dx. Figure 4.11 shows the demonstration of divided energy band profile. Since each segments should follow the Eq. 4.12, the Schrödinger equation for j-th segment is

$$\left[-\left(\hbar^2/2m_j^*\right)\partial_x^2 +V_j -E_x\right]\psi_j(x)=0 \tag{4.13}$$

where m_j^* is the effective mass and V_j is the potential energy for j-th segment. Next, we calculated the tunneling probability using the general solution of Schrödinger equation.

$$\psi_j(x)=A_j\exp\left[ik_j\left(x-x_j\right)\right]+B_j\exp\left[-ik_j\left(x-x_j\right)\right] \tag{4.14}$$

Here, the A_j and B_j are constant for rightward and leftward moving solution and x_j is the position of left edge in j-th segment. The momentum k_j is

$$k_j=\sqrt{2m_j^*(E_x-V_j)}\Big/\hbar. \tag{4.15}$$

The wave functions for adjacent segments should be continuous and its first derivatives is also continuous. With this boundary condition, we can get the relation between two neighboring segments like below.

$$\begin{pmatrix} A_j \\ B_j \end{pmatrix}=T_{j+1,j}\begin{pmatrix} A_{j+1} \\ B_{j+1} \end{pmatrix} \tag{4.16}$$

Here, the $T_{j+1,j}$ is the transfer matrix for j+1-th and j-th segments as described in the Eq. 4.17

$$T_{j+1,j}=\begin{pmatrix} \dfrac{\beta_j+\beta_{j+1}}{2\beta_j}e^{-ik_jdx} & \dfrac{\beta_j-\beta_{j+1}}{2\beta_j}e^{-ik_jdx} \\ \dfrac{\beta_j-\beta_{j+1}}{2\beta_j}e^{ik_jdx} & \dfrac{\beta_j+\beta_{j+1}}{2\beta_j}e^{ik_jdx} \end{pmatrix} \tag{4.17}$$

where $\beta_j=k_j\big/m_j^*$.

N rectangular potential barriers

$\Phi_{source} - \chi_{tunnel}$

$E_{x,m}$

Source

$E_{F,source}$

Tunnel Barrier

Drain

← Calculated electron potential energy

j=1   j=2 j=3 j=4 · · · j=N-1 j=N j=N+1 j=N+2
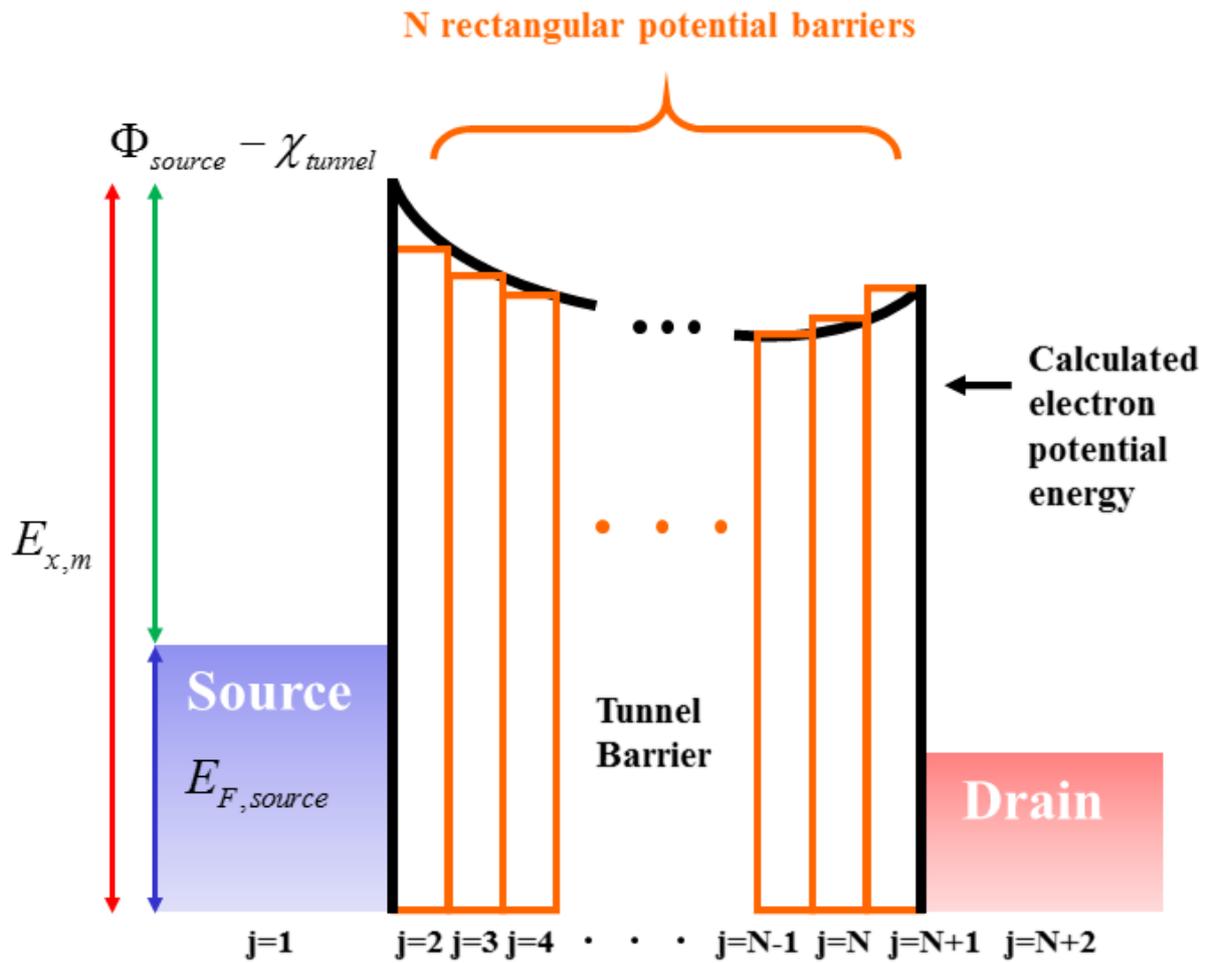
Figure 4.11 Demonstration of dividing tunnel insulator potential profile. Potential barrier is estimated by N rectangular potential barriers [146].

As depicted in Fig. 4.11, the wave functions for source and drain electrodes are also needed (j=1, j=N+2). Thus, we have N+2 wave functions and N+1 transfer matrices to calculate the tunneling probability from source to drain electrode. By multiplying transfer matrices from $T_{2,1}$ to $T_{N+2,N+1}$, the final transfer matrix which represents the relation between the constants of wave function in the source electrode (A_1, B_1) to the constants in the drain side (A_{N+2}, B_{N+2}) is obtained.

$$\begin{pmatrix} A_1 \\ B_1 \end{pmatrix} = T_{2,1}T_{3,2}\cdots T_{N+1,N}T_{N+2,N+1}\begin{pmatrix} A_{N+2} \\ B_{N+2} \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix}\begin{pmatrix} A_{N+2} \\ B_{N+2} \end{pmatrix} \tag{4.18}$$

Assuming that the electrons are only comes from the source electrode, there is no solution for electrons moving leftward in the drain electrode ($B_{N+2}=0$). The tunneling probability can be expressed as the ratio of moving rightward electrons in source side to drain side.

$$T = \left|\frac{A_{N+2}}{A_1}\right|^2 = |T_{11}|^2 \tag{4.19}$$

After calculating the tunneling probability of EMIM junction, we combined the Eq. 4.19 to the generalized tunneling formula by Simmons [96]. The tunnel current density is

$$J = \left(4\pi me/h^3\right)\int_0^{E_{x,m}} T(E_x)\left[\int_0^\infty f(E) - f(E+eV)dE_r\right]dE_x \tag{4.20}$$

where m is the free electron mass, e the electron charge, h Planck's constant, $E_{x,m}$ the upper limit of energy in x-direction, $T(E_x)$ the tunneling probability, and $f(E)$ the Fermi-Dirac distribution function with respect to the electron energy. The electron energy is composed of the x-directional energy (E_x) and the radial directional energy (E_r) which is perpendicular to each other. The sum of E_x and E_r gives the total electron energy ($E = E_x + E_r$). In this experiment, we used the mensuration by parts to calculate the integration in tunnel current density equation. Then, the current density equation becomes

$$J = \left(4\pi me/h^3\right)\int_0^{E_{x,m}} T(E_x)\left[\int_0^{E_{r,m}} f(E) - f(E+eV)dE_r\right]dE_x$$
$$= \left(4\pi me/h^3\right)\sum_{n=1}^{N_x} T\left(\frac{E_{x,m}}{N_x}\cdot n\right)\cdot\frac{E_{x,m}}{N_x} \tag{4.21}$$
$$\times\sum_{l=1}^{N_r}\left[f\left(\frac{E_{r,m}}{N_r}\cdot l + \frac{E_{x,m}}{N_x}\cdot n\right) - f\left(\frac{E_{r,m}}{N_r}\cdot l + \frac{E_{x,m}}{N_x}\cdot n + eV\right)\right]\cdot\frac{E_{r,m}}{N_r}$$

where N_x and N_r are the dividing number of E_x and E_r. We also determine the upper limit of integral for E_r ($E_{r,m}$) because the upper limit of integral was infinity. The upper limits of E_x

71

and E_r were chosen properly with physical consideration. First, the upper limit of E_x should not be exceed the energy barrier height of tunnel insulator because the tunneling is only occurred when the energy is less than the tunnel barrier. In other words, we didn't include the ballistic moving electrons in tunneling equation. In case of polarization up state, the largest barrier height is the difference between the workfunction of source metal (Φ_{source}) and the electron affinity of tunnel insulator (χ_{tunnel}) because it has valley shaped energy band profile. Then, the upper limit of E_x can be expressed as

$$E_{x,m} = E_{F,source} + \left(\Phi_{source} - \chi_{tunnel}\right). \tag{4.22}$$

However, the energy band profile in polarization down state is ridge shape so that the maximum of energy barrier is quite larger than the polarization up case. Though they have different energy barrier maximum, we chose the same upper limit because the Fermi-Dirac distribution function decays very quickly [153]. Numerically, the Fermi-Dirac distribution function has value of 0.001 when the electron energy is 0.3 eV higher than the Fermi level at room temperature (300 K). Considering the energy barrier in our device ($\Phi_{source} - \chi_{tunnel}$) is about 1.24 eV, the larger upper limit of integral has no meaning in the actual calculation result. In the same manner, the upper limit of E_r was selected to be 0.3 eV higher than the Fermi level of source electrode.

$$E_{r,m} = E_{F,source} + 0.3 \ eV \tag{4.23}$$

The number of electrons having energy larger than this value is almost zero as mentioned above. Therefore, we chose the upper limits of E_x and E_r as shown in the Eq. 4.22 and 4.23.

Now, the tunnel current density can be calculated using the Eq. 4.21. However, the energy band profile changes with the height of EMIM junction as shown in Fig. 4.10. Thus, we need to divide the junction height with several sections and calculate the tunnel current density in each section. The unit of current density obtained in the Eq. 4.21 is A/m^2 and the total current density is A/m because we should add the current density and multiply the height of each section.

The calculated tunnel current density for polarization up and down states are shown in Fig. 4.12. The tunnel current density difference between two polarization states is significantly large as shown in both graphs with log scale (Fig. 4.12a) and linear scale (Fig. 4.12b). Since the energy band profile of polarization up state is valley shape, the effective tunnel barrier thickness at Fermi level of source metal is thinner than the polarization down case. Here, the effective tunnel barrier thickness is the width of electric potential larger than the electron energy. As depicted in Fig. 4.12b, the turn-on voltage of polarization up state is nearly 1.2 V because the difference between metal workfunction and the electron affinity of tunnel insulator is 1.24 eV. At this source-drain bias voltage, the switching ratio between the polarization up and down state is almost 10^{13} which is

very large value.

One more thing we can notice in this current density curve is the oscillation of tunnel current density in polarization up state. In Fig. 4.12a, the tunnel current density fluctuation occurs at low bias region. Moreover, we can also find the current density oscillation at high bias voltage region in the linear scale plot (Fig. 4.12b). This phenomenon can be happened due to the resonant tunneling [154, 155] by valley shaped energy band profile. Generally, the resonant tunneling occurs at double tunnel barrier. The valley shaped energy band can be considered as a double tunnel barrier in which a first tunnel barrier is formed at the source side and a second barrier at the drain side. The magnitude of oscillation decrease as the source-drain voltage becomes bigger because the Fowler-Nordheim tunneling starts around 1.2 V [94].

As described in the previous paragraph, the tunnel current density characteristics of polarization up state is mainly contributed from the valley shaped potential profile. However, the tunnel current density curve of polarization down state is monotonically increased in the log scale plot. This can be explained by the potential profiles shown in Fig. 4.10. Both energy bands of polarization up and down state are almost same at the large height region which is far from the underlying ferroelectric layer. Considering the effective tunnel barrier, the tunnel current density is much larger in low height region in case of polarization up state. Therefore, the overall tunnel current density follows the tunneling probability at the valley shaped potential profile. However, in case of polarization down state, the tunnel current density is larger in the large height region. Thus, the tunnel current density at the low height region cannot contribute much on the total tunnel current density. In result, the tunnel current characteristics of polarization down state is similar to the conventional metal-insulator-metal tunnel junction.
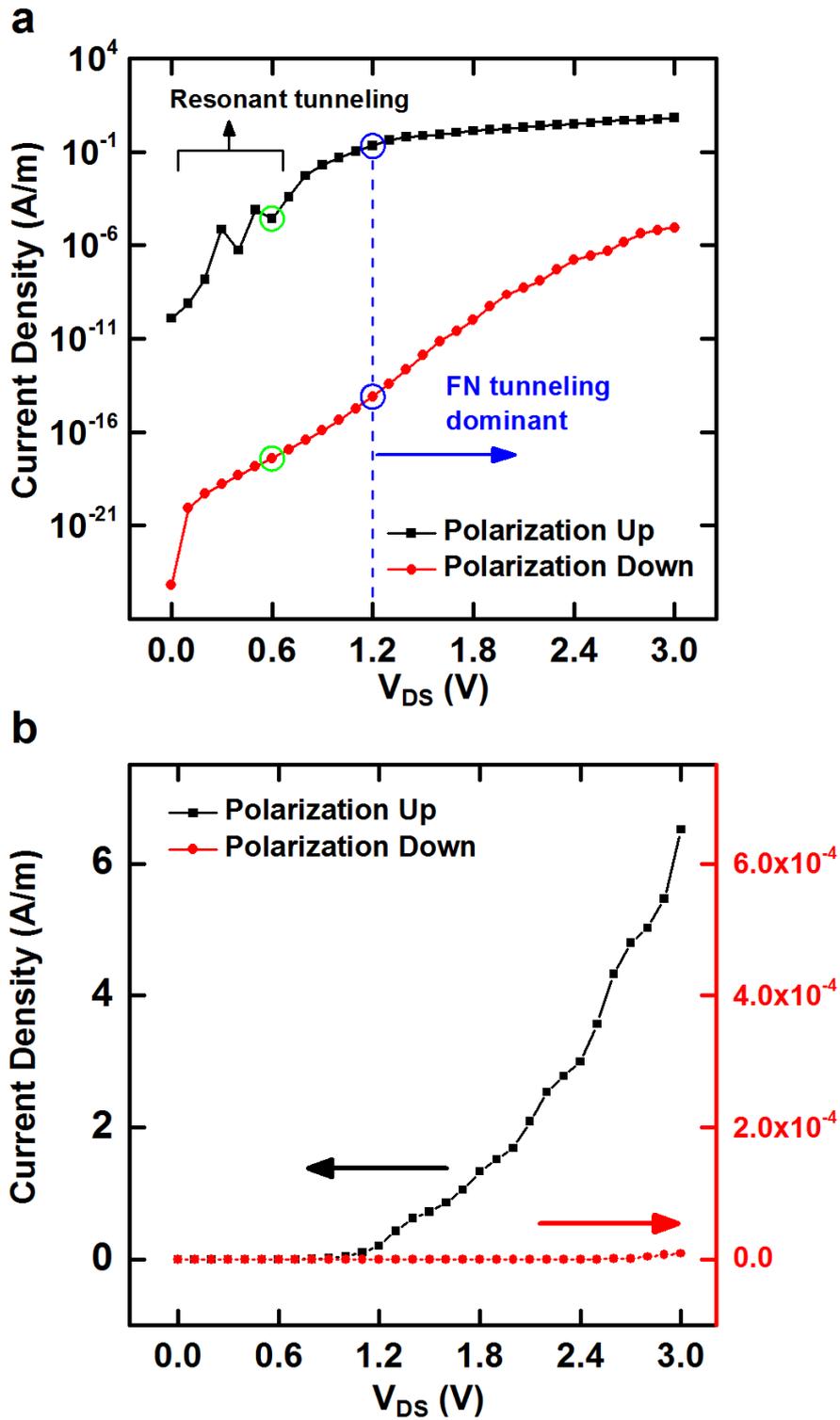
Figure 4.12 The calculated tunnel current density of EMIM/Ferroelectric memory device depending on the polarization up and down states in (a) log scale and (b) linear scale [146].

4.2.3 Read and Write Method

Based on the tunnel current density calculation, the read/write method for EMIM/ferroelectric cell array is established. First, the reading mechanism can be explained by using the Fig. 4.13. In the figure, the energy band profiles of memory cell at word line, bit line, and cross cell for both polarization up and down states.

As described in previous section, the turn-on voltage is around 1.2 V where the Fowler-Nordheim (FN) tunneling starts. After the turn-on voltage, the current density of polarization up state increases slower than before. Therefore, we selected the applying voltage for word and bit line as 0.6 V and -0.6 V as shown in Fig. 4.13. The source electrodes of memory cells are connected to the bit line and the drain electrodes are connected to word line. The energy band profiles of word and bit lines are actually same considering the difference of source-drain voltage. However, the total voltage difference at the cross cell is 1.2 V which is the turn-on voltage of EMIM junction. Here, we defined the polarization up state as a written state and the polarization down state as erased state. Then, the calculated current density of written state (Blue circle on black curve) is 10^{13} times larger than the erased state (Blue circle on red curve) at turn on voltage. In addition, the current density of written state memory cell at turn on voltage (Blue circle on black curve) is 10^3 times bigger than at the half of turn on voltage (Green circle on black curve).

When the read-out cell is written state, the read-out current is very large because the cross cell has very low resistance. In case of the read-out cell is erased, the current density of cross cell is very low. However, there might be some memory cells in written state connected to the word and bit lines. Their current densities (Green circle on black curve) are much bigger than the current density of cross cell at erased state (Blue circle on red curve). Even though the current densities of word and bit lines with written state contribute to the read-out current, they still smaller than the read-out current of cross cell at written state. Therefore, at any circumstances, the current density is much larger when the cross cell is written than the erased case.
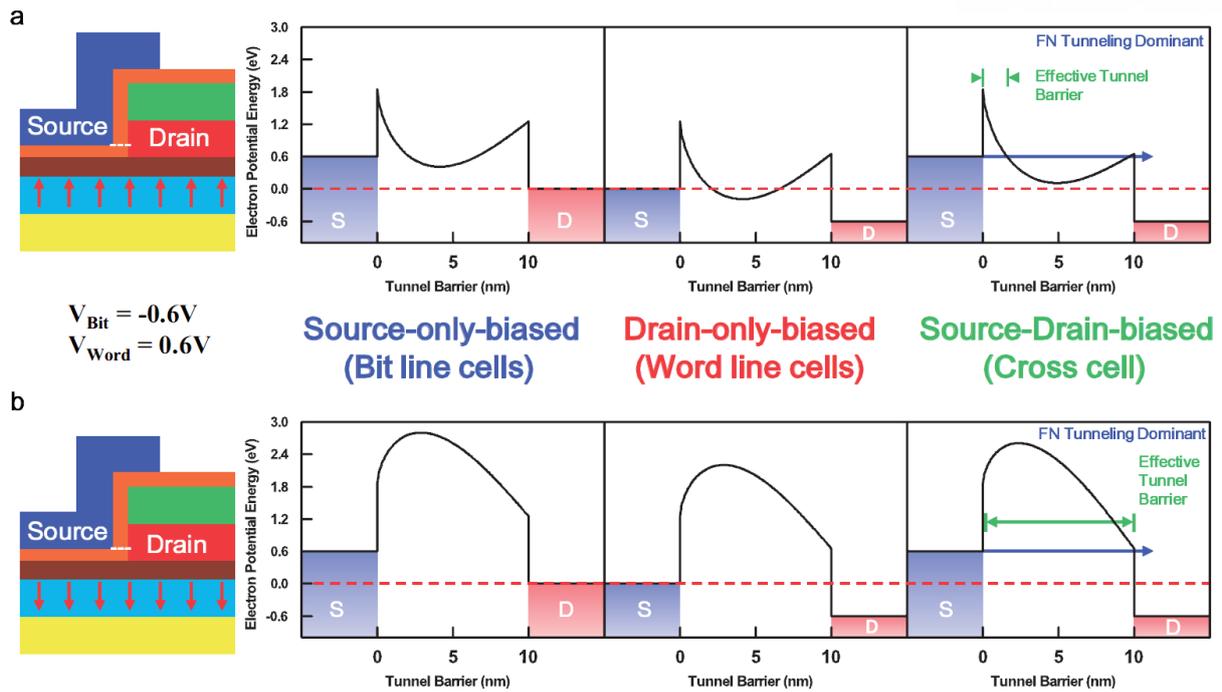
Figure 4.13 The electron potential profiles of tunnel insulator at polarization (a) up and (b) down states. The applied voltage at bit line is -0.6 V and word line is 0.6 V. The energy band profiles at bit line, word line, and cross cell are represented for both polarizations [146].
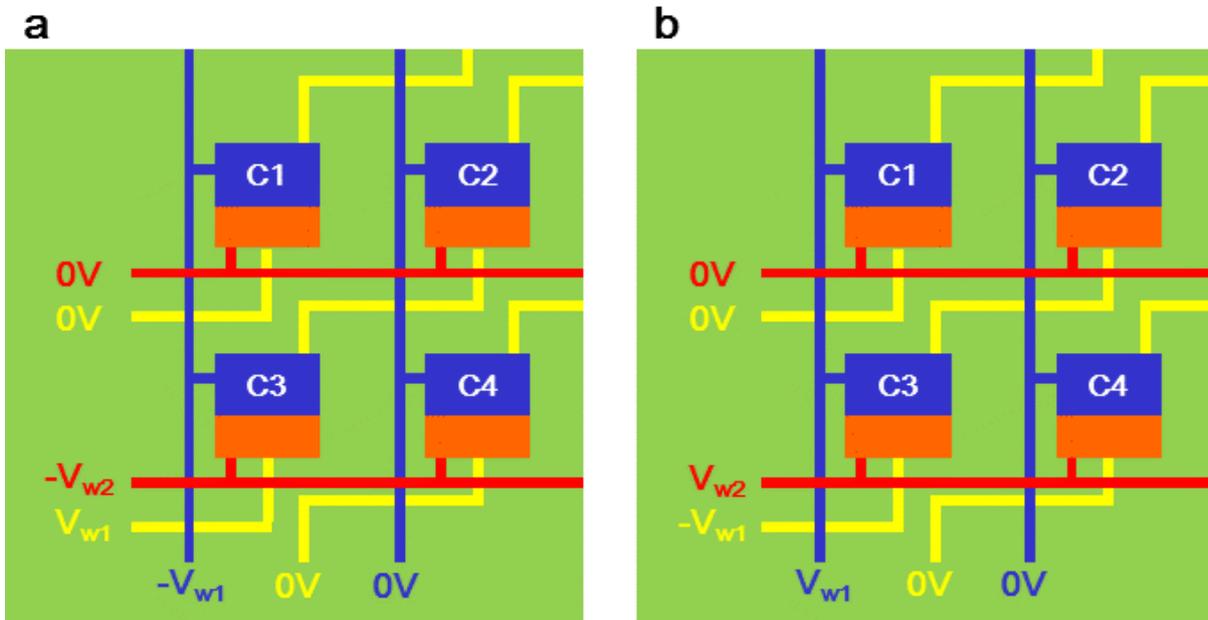
Figure 4.14 (a) The writing and (b) erasing mechanism of C3. Other memory cells (C1, C2, C4) has no changed with these applied voltages [146].

The writing mechanism of EMIM/Ferroelectric memory cell array is just applying electric field larger than the coercive field across the ferroelectric layer. The schematics of writing mechanism is shown in Fig. 4.14. The memory cell can be written by applying V_{w1} on writing line, $-V_{w1}$ on bit line, and $-V_{w2}$ on word line. At this moment, the only cell that three lines are crossed each other becomes written state. Here, V_{w1} and V_{w2} should be lower than the voltage which can produce the coercive field. However, $V_{w1}+V_{w2}$ and $2V_{w1}$ can make electric field larger than the coercive field across the ferroelectric layer. Considering the structure of EMIM/Ferroelectric memory cell, the voltage across the ferroelectric should be calculated differently at source electrode side and drain electrode side. When the voltage V_{appl} is applied between the drain and writing electrode, the voltage across the ferroelectric layer (V_1) and "Insulator 1" layer (V_2) can be approximately calculated like

$$V_1 = \frac{C_2}{C_1 + C_2}V_{appl}, \qquad V_2 = \frac{C_1}{C_1 + C_2}V_{appl} \qquad (4.24)$$

where C_1 is the capacitance of ferroelectric layer and C_2 the capacitance of "Insulator 1" layer. In case of the source side, the applied voltage (V_{appl}) can be divided into three layers.

$$V_1 = \frac{C_2 C_3}{C_1 C_2 + C_2 C_3 + C_3 C_1}V_{appl}, \quad V_2 = \frac{C_1 C_3}{C_1 C_2 + C_2 C_3 + C_3 C_1}V_{appl}$$
$$V_3 = \frac{C_1 C_2}{C_1 C_2 + C_2 C_3 + C_3 C_1}V_{appl}$$

$$(4.25)$$

Here, V_1 and C_1 is the voltage and capacitance across the ferroelectric layer, V_2 and C_2 for "Insulator 1", and V_3 and C_3 for "Tunnel insulator". The Eq. 4.24 and 4.25 are the results considering only the series connection of several simple parallel capacitors between two electrodes. Even in the simple calculation, the voltage across the ferroelectric layer has different voltage when the same voltage is applied to source and drain electrode with respect to the writing electrode. Therefore, we determined V_{w1} to be slightly larger than V_{w2} to produce uniform electric field during writing and erasing process.

As shown in Fig. 4.14a, C1 and C4 cell has only negative bias voltage ($-V_{w1}$ and $-V_{w2}$) on the source and drain side. The C2 cell has no voltage on the source and drain electrode but V_{w1} is applied in writing electrode. However, these cells have no change in their polarization direction of ferroelectric layer. The only C3 can be written because the source and drain electrodes have negative bias voltage and the writing electrode also has positive voltage resulting the electric field across the ferroelectric layer larger than the coercive field of ferroelectric.

In Fig. 4.14b, the only difference with previous case is the polarity of applied voltage. This means that the induced electric field across the ferroelectric layer is opposite direction with respect

77

to the writing case. Therefore, only C3 can be erased and the memory states of other cells (C1, C2, C4) are remained. Figure 4.15 shows the schematic 3D memory cell array during writing and erasing. Here, the lighted lines represent that the appropriate voltages are applied. At a glance, the only the center memory cell can be written or erased.

In the EMIM/Ferroelectric memory device study, the tunnel current density relying on the polarization direction of ferroelectric layer can be drastically changed. This type of memory device can be stackable and have no need of selection devices due to its giant electroresistance switching. Moreover, the fabrication methods are all thin film based processes and the high speed with low power consumption nonvolatile memory device can be realized with this structure.
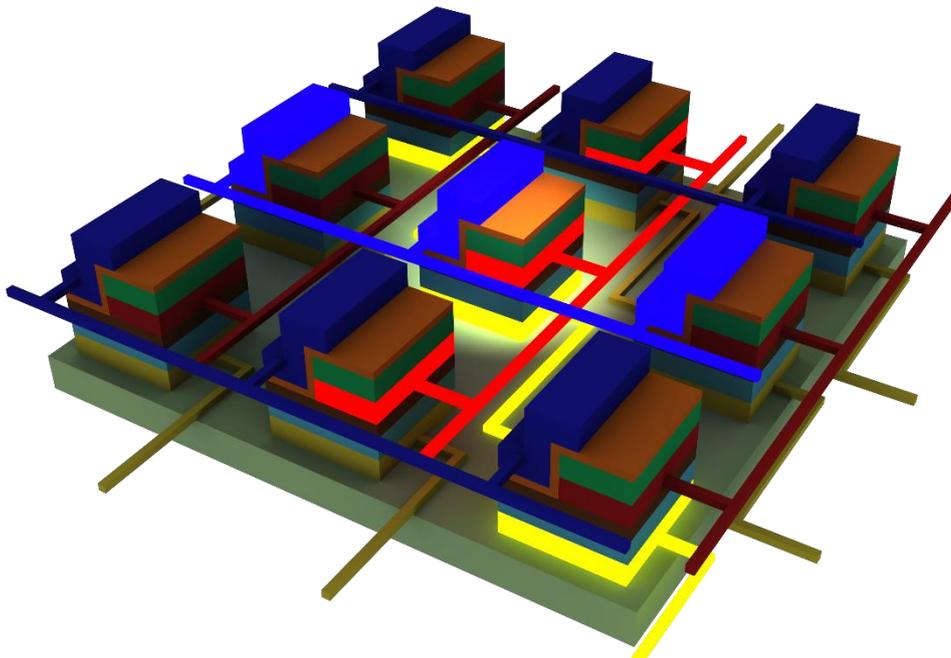
Figure. 4.15 Visualization of writing and erasing memory cell. Lighted lines are applied bias voltages on them.

V.   Ferroelectric Memory Application with Graphene Devices

5.1 Memory Effect of Graphene Field Effect Transistor (FET) on Ferroelectric Layer

Researches for ferroelectric memory combining the graphene have been studied in various ways by utilizing electronic properties of graphene [136, 156, 157]. Usually, the working principle is mainly depending on the resistance of graphene changed by spontaneous polarization of ferroelectric. Thus, the graphene field effect transistor (FET) on ferroelectric material is already studied as memory device. However, the graphene FET has no fully off state due to the conductance minimum experimentally. In our study, we utilize the transconductance of graphene FET as a memory unit for unambiguous read-out using just two crossing lines. This read-out principle can be a milestone for developing new memory devices in future.

5.1.1 Atomic Layer Deposition (ALD) Process on PZT

In chapter 4.2, the energy band of EMIM structure on ferroelectric layer was calculated and the tunnel current density was also obtained. Since the leakage current from the metal electrode to ferroelectric film can affect to the operation of memory device, the insulating layer on ferroelectric layer is necessary for blocking leakage current. In our experiment, the first step for fabricating graphene/ferroelectric memory device is depositing thin insulating layer on ferroelectric. A PZT ($Pb_{1.1}Zr_{0.35}Ti_{0.65}O_3$) and aluminum oxide ($Al_2O_3$) were chosen for ferroelectric layer and blocking insulator. The PZT substrate is stack of PZT/Pt/Ti/SiO$_2$/Si so that the bottom electrode of ferroelectric layer is already formed. Before the deposition of Al_2O_3 film, the PZT substrate was cleaned with acetone and methanol with ultra-sonic agitation.

After cleaning process, the aluminum (2 nm) was deposited as a seed layer on the PZT substrate by using E-beam evaporator. The deposited aluminum layer was oxidized and formed thin aluminum oxide layer on PZT substrate. Then the sample was mounted on ALD system as shown in Fig. 5.1. TMA (trimethylaluminum) and H_2O were used as precursors in deposition cycle. The TMA is first attached to the aluminum oxide seed layer and the remained molecules are purged. Next, the H_2O reacts with the attached TMA and form aluminum oxide layer. Finally, the H_2O molecules which is not react with TMA are also purged. These steps consist of one cycle of ALD process. The 154 cycles were performed to deposit 30 nm of Al_2O_3 layer on the sample.

Since the memory effect depends on the spontaneous polarization of ferroelectric layer, the coercive voltage should be measured to operate the memory device. Thus, we measured the polarization-electric field hysteresis (PE hysteresis) curve for a bare PZT sample and Al_2O_3/PZT sample. Figure 5.2 shows the PE hysteresis curve and represents the coercive voltage for both

samples. In the table 5.1, the P_s, P_r, and E_c extracted from the PE hysteresis curves are described.

Figure 5.1 Atomic Layer Deposition (ALD) system in nanofabrication clean room in UNIST.
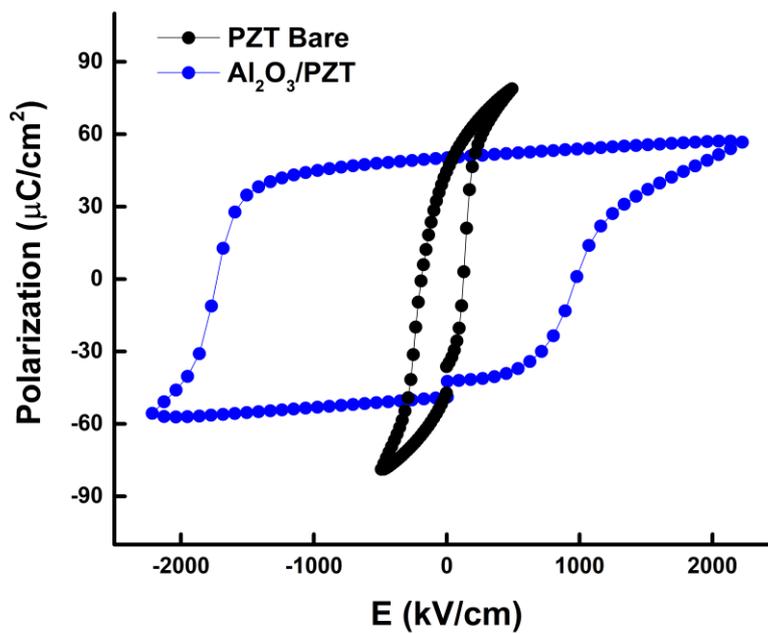
Figure 5.2 PE hysteresis curve of bare PZT film (black curve) and Al_2O_3 (30 nm) deposited film (blue curve).

Table 5.1 P_s, P_r, and E_c of bare PZT and Al_2O_3/PZT film.

	Bare PZT	**Al_2O_3/PZT**
P_s ($\mu C / cm^2$)	79	57
P_r ($\mu C / cm^2$)	45	50
E_c (kV / cm)	127	975

As shown in the Table 5.1, the coercive field increases much in case of the aluminum oxide film is deposited on the PZT film. The Al_2O_3 layer can prohibit the applied electric field across the ferroelectric layer so that the required voltage to change polarization direction of ferroelectric becomes larger.

5.1.2 FET Fabrication Process

The graphene FET was fabricated with conventional photolithography process. First, the align mark was patterned by photolithography and the metal (Ti/Au 10/50 nm) was deposited by E-beam evaporator. Lift off process was subsequently followed to leave only align mark pattern. Secondly, the channel pattern was fabricated by using the photolithography and oxygen plasma etching. After etching process, the photoresist was removed by acetone. Finally, the source and drain electrodes were also patterned as same as first step (photolithography and metal deposition). The schematic device structure is shown in Fig. 5.3.
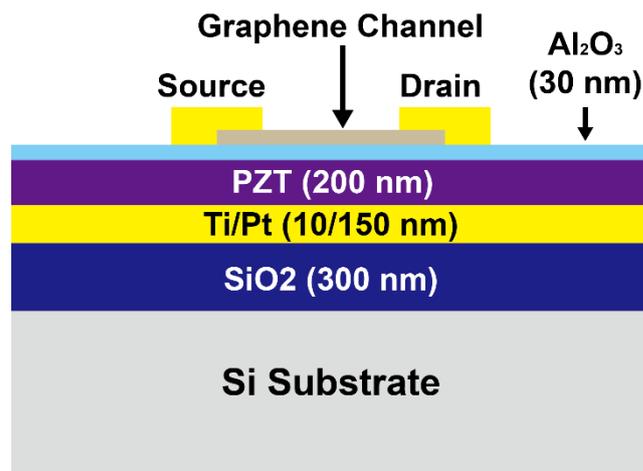
Figure 5.3 Schematic diagram for graphene FET/ferroelectric memory device structure. [*In preparation*]

5.1.3 Transconductance Measurement Depending on Spontaneous Polarization

Graphene FET on PZT was tested to confirm that the transconductance change depending on the polarization direction of ferroelectric. As depicted in Fig. 5.3, the gate electrode is the bottom Pt layer below the PZT. The voltage pulse diagram for programming and reading two memory states of our memory device is shown in Fig. 5.4. First, the positive gate voltage pulse is applied with a grounded source electrode to make polarization direction of PZT upward. After this programming, the read-out process is followed by applying a small source-drain voltage with the sweeping gate voltage from -0.1 V to 0.1 V which is much smaller than the programming voltage. At this measurement, the transconductance can be measured by the slope of source-drain current with gate voltage curve. Next, the negative programming voltage is applied to the gate electrode to convert the polarization direction as downward. Then, the transconductance is measured with the same method as before. This cycle was repeated to confirm the reliability of memory states. The measurement results are shown in Fig. 5.5.
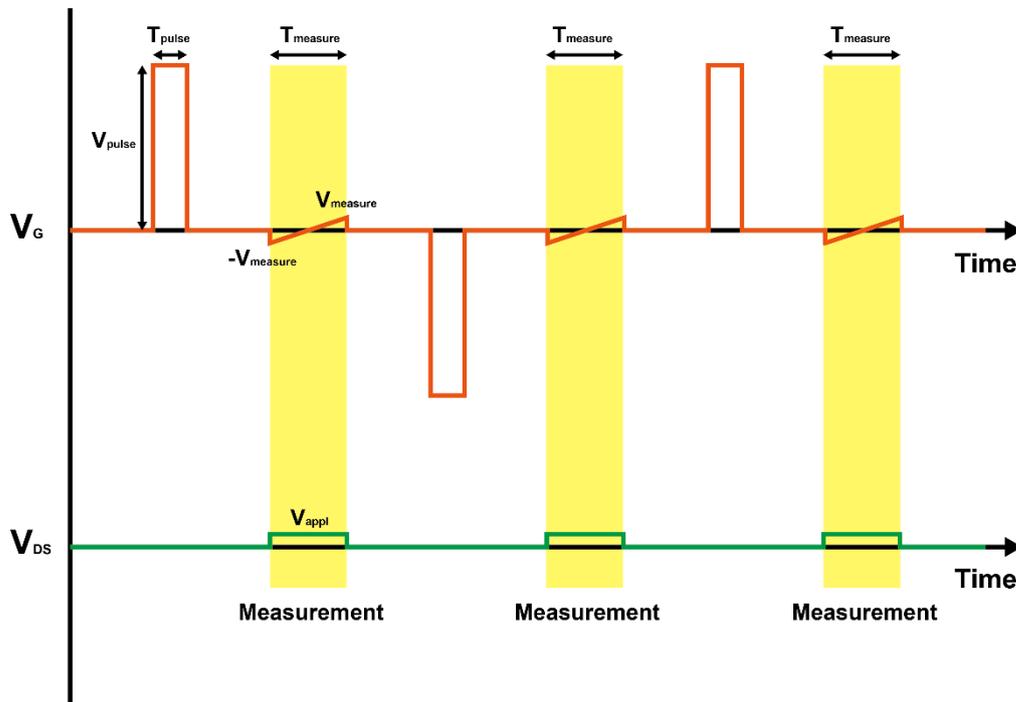
Figure. 5.4 Voltage pulse diagram for gate and source-drain voltage. Measurement is performed with constant source-drain voltage with varying gate voltage. [*In preparation*]

a

b
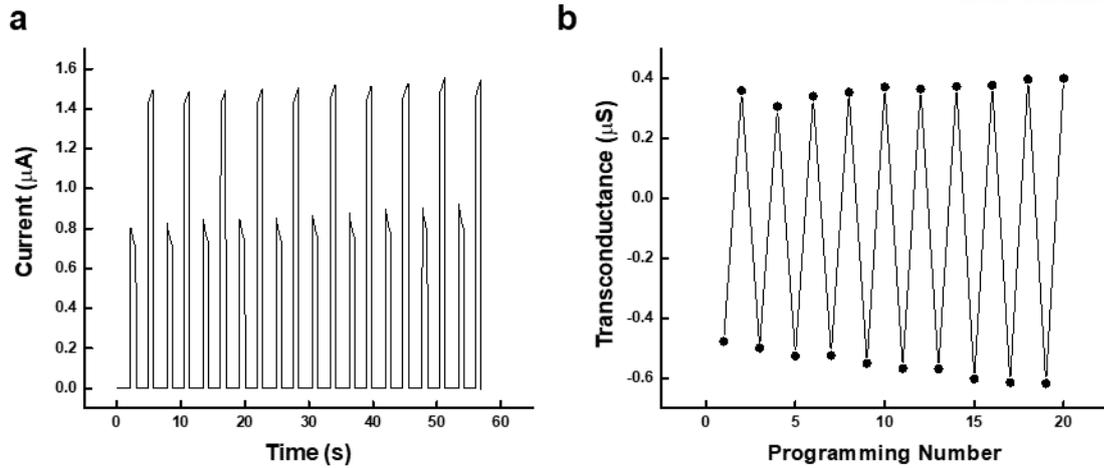
Figure 5.5 (a) Source-drain current with voltage pulse as shown in Fig. 5.4. (b) Corresponding transconductance change. [*In preparation*]

As depicted in Fig. 5.5, the source-drain current change by gate voltage sweep is significantly different from one to the other programmed state. Here, we applied 7 V and -5 V of V_{pulse} for 40 ms (T_{pulse}), -0.1 V (-$V_{measure}$) to 0.1 V ($V_{measure}$) for 0.8 s ($T_{measure}$), and 0.1 V of V_{appl} for 0.8 s ($T_{measure}$). The calculated transconductance which is the slope of source-drain current vs. gate voltage is also shown in Fig. 5.5b. In this graph, we can clearly distinguish the two different states. Therefore, this device structure can be a candidate for next generation memory device based on the measuring transconductance.

VI. Conclusions

In this study, we focused on the carrier transport including quantum mechanical tunneling of lateral junction on ferroelectric layer. The main idea for our study was the energy band of laterally formed tunnel junction can be significantly affected by the electric fringe field of underlying ferroelectric material. In 3-dimensional structure, the EMIM structure was proposed to realize the lateral junction without E-beam lithography process. This structure is just simple cross bar structure with blocking vertical junction at crossing area by insulating layer. Therefore, the fabrication method is compatible with conventional silicon process. The theoretical modeling for EMIM junction on ferroelectric layer shows that the significantly large resistive switching ratio ($\sim 10^{13}$) depending on the polarization direction of ferroelectric. The memory cell can be written by applying appropriate voltages on source, drain, and writing electrodes to form coercive field across the ferroelectric layer only for cross cell. The read-out of memory cell can be achieved by applying voltages with opposite sign on source and drain electrode. Thus, the writing speed is very fast because the time for converting the polarization direction of ferroelectric layer is extremely short. Moreover, the read-out speed is also fast since it only measures the resistance of cross cell. Based on the energy band change by underlying ferroelectric layer, we performed theoretical and experimental studies of 2D lateral tunnel junction on ferroelectric layer. The graphene/FG/graphene tunnel junction was formed by selective fluorination of graphene. The junction characteristic was confirmed by the I-V measurement and analyzed with theoretical calculation. Comparing theoretical value and experimental data, the energy barrier of FG was estimated as ~0.8 eV. This 2D lateral tunnel junction can be applicable to the ferroelectric memory device as similar as the EMIM/ferroelectric memory. Lastly, we demonstrated the graphene FET structure on ferroelectric material can be acted as a memory device by measuring transconductance of FET. With two different gate voltage pulse, the transconductance was changed clearly.

At the first stage, the EMIM/ferroelectric memory device was invented to make resistive switching memory device considering the fabrication process. Even though the lateral tunnel junction was hard to achieved with nice side wall due to the limitation of etching system, it can be realized by current etching technologies used in companies. Since the theoretical calculation was very precisely performed, this device can inspire the new memory device structure.

Secondly, the graphene/FG/graphene lateral tunnel junction can provide another way for fabricating lateral tunnel junction. Thus, the junction itself has meaning of studying the exact value of energy band alignment between FG and graphene. Moreover, it can be applicable to the ferroelectric memory device as similar as the EMIM/ferroelectric memory.

Lastly, the transconductance measurement method was proposed as a reading mechanism of memory device because the transconductance is not affected by the series resistance owing to the

connected memory cells. Therefore, it can be easy to determine the memory states more clearly than the resistive switching memory devices. As a demonstration of transconductance memory device, graphene FET on ferroelectric layer shows the clear change in transconductance. Still more sophisticated conditions for depositing insulating layer on PZT and operating voltages are needed. However, it shows two different transconductance states depending on the sign of programming voltage so that this device concept can be a good model for inventing new memory devices.

In conclusions, new types of memory device were demonstrated based on the studies for carrier transport mechanism in quantum mechanical system. Since the size of memory device becomes smaller, the interpretation of carrier transport in quantum mechanical regime should be supported to invent the new memory devices. Therefore, this kind of research is important for both studying for quantum mechanical system and applying actual memory devices.

APPENDICES

A. Ballistic Electron Emission Spectroscopy (BEES)

A.1 Principle of BEES

Researches for probing the energy barrier at the interface of two different materials forming a junction have been performed with various methods such as current-voltage characteristics, internal photoemission (IPE), and ballistic electron emission microscopy (BEEM). The BEEM technique can investigate the energy barrier of junction precisely with high resolution in space by using a scanning tunneling microscope (STM) system [158]. As shown in Fig. A.1, the STM tip emits the hot electron to the metal/semiconductor junction which is departed from the STM tip with a small vacuum gap. The vacuum gap is the tunnel barrier between tip and metal. When the negative bias voltage is applied to the STM tip, the hot electron injection from the tip to the metal. At this moment, the metal is grounded so that the electrons with lower energy than the Schottky barrier flow into the grounded metal. However, when the electron energy becomes larger than the Schottky barrier, the hot electrons can travel through the metal and reach to the semiconductor. Here, the thickness of the metal should be thin enough to a hot electron can move ballistically without scattering. The STM tip work as an emitter, the metal as a base, and the semiconductor as a collector. Then, the collector current with tip bias voltage curve shows a sharp increase at the Schottky barrier as shown in Fig. A.2 [159]. The turn on voltages are varied with the type of metal because of the Schottky barrier height change.

Based on the principle of BEEM, ballistic electron emission spectroscopy (BEES) can be measured without STM by using the tunnel junction on Schottky junction [160]. W. Yi and V. Narayanamurti fabricated $Al/Al_2O_3/Al$ tunnel junction on GaAs substrate and showed the BEES and BHES (ballistic hole emission spectroscopy) simultaneously using its band alignment [160]. Figure A.3 shows the device structure and its band alignment [160]. With this method, the Schottky barrier between Al/GaAs can be measured in the same manner with BEEM configuration. As shown in Fig. A.4, the BEES and BHES was measured very close to the theoretical expectation value.
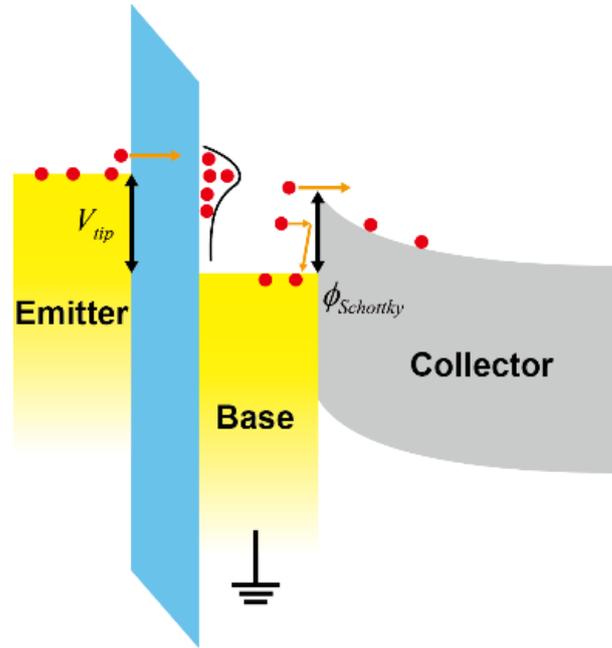
Figure A.1 The schematic of BEEM measurement. Red circles represent the electrons.
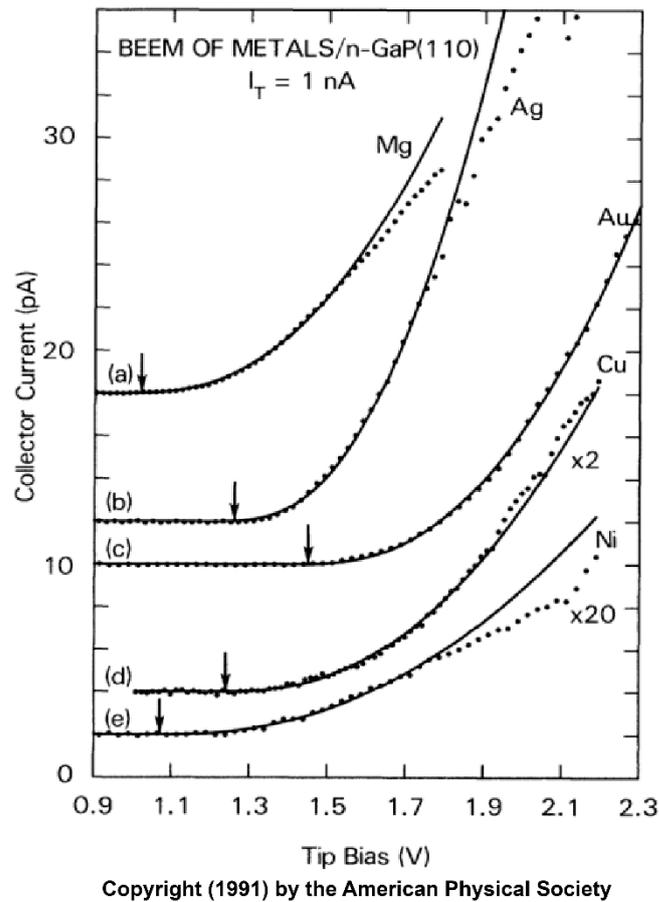
Figure A.2 The collector current with tip bias voltage for various metals [159].
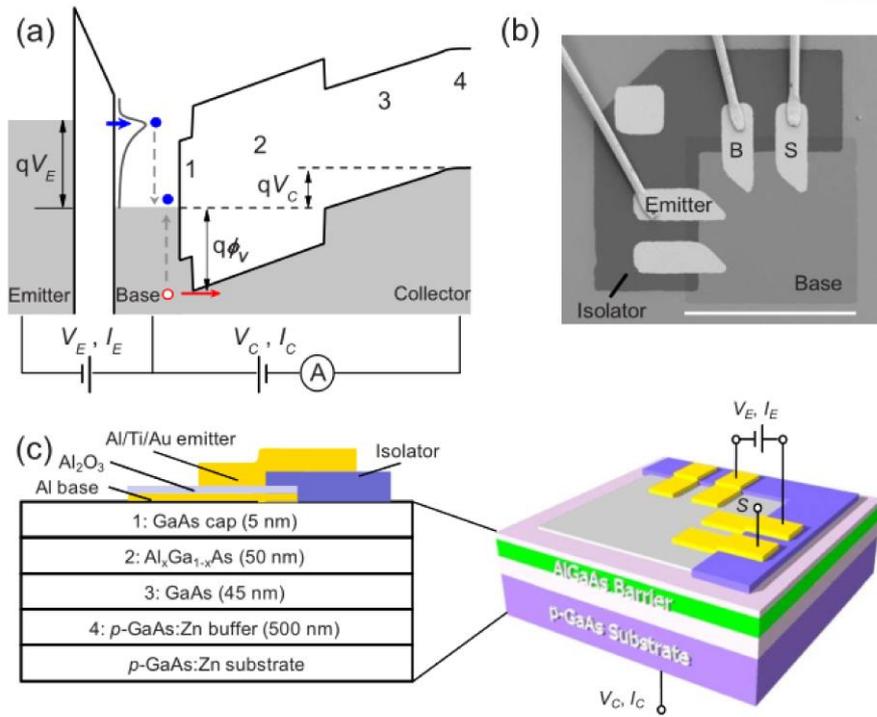
Figure A.3 (a) Energy band diagram, (b) optical image, and (c) schematic of BEES device [160].
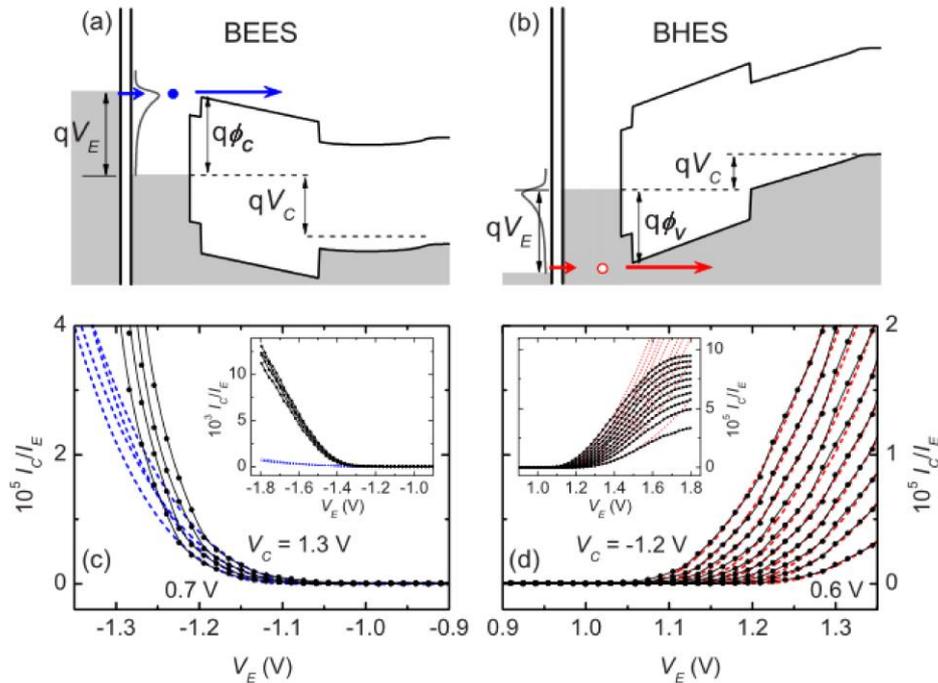
Figure A.4 Energy band diagram of (a) BEES and (b) BHES. Collector current of (c) BEES and (d) BHES with emitter voltage [160].

A.2 BEES Measurement

A.2.1 Experimental Method

In this experiment, the device for BEES measurement was fabricated and the collector current was measured. The device structure is shown in Fig. A.5a and its optical microscope image is represented in Fig. A.5b. Silicon carbide substrate with a buffer layer and two different epitaxially grown layers on top was cleaned by using Acetone/Methanol with ultra-sonic agitation and HF dipping. Then, the platinum (Pt, 8 nm) is deposited on the SiC substrate with the shadow mask method. After forming the Schottky junction (Pt/SiC), several layers of hexagonal boron nitride (h-BN) is mechanically exfoliated from the monocrystalline bulk h-BN by using the scotch tape method and transferred on the Pt. Finally, the emitter metal (Pt/Au, 10/50 nm) was deposited on the transferred h-BN on the Pt metal with the shadow mask method. The shadow mask was aligned with the use of the optical microscope.

(a)

(b)
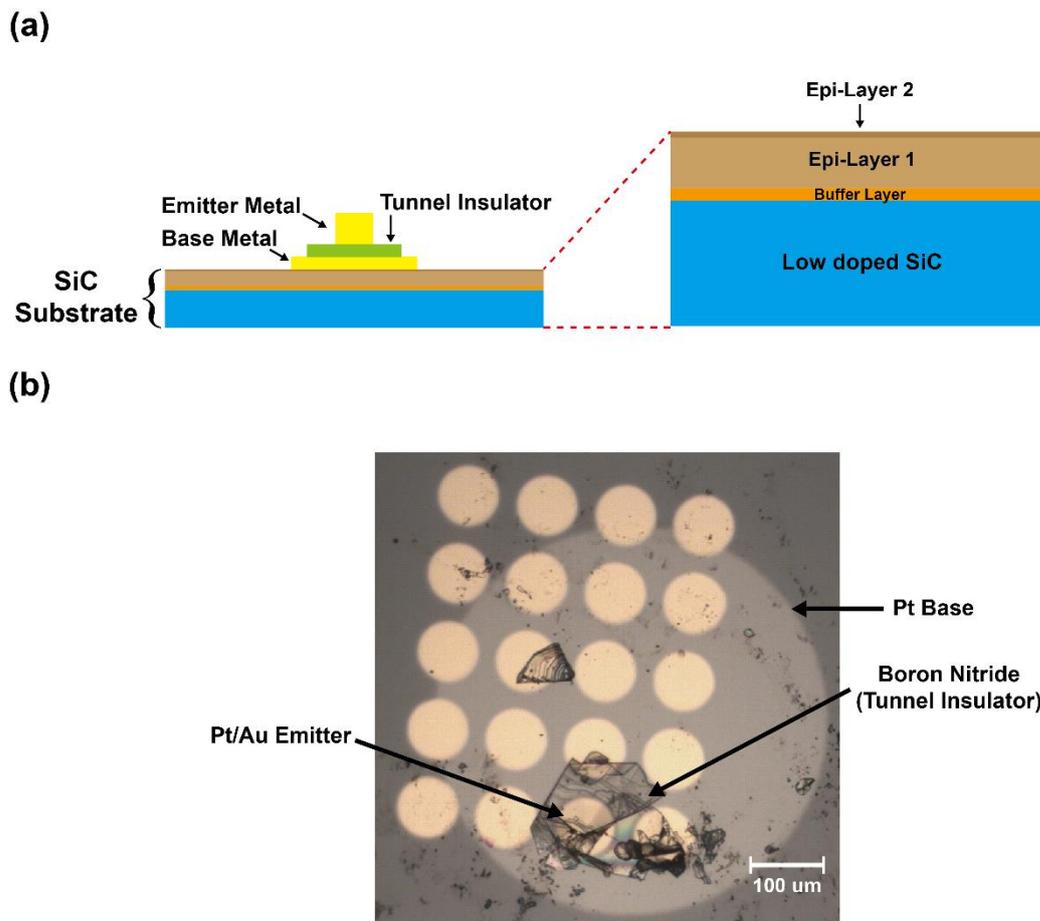
Figure A.5 (a) The schematic of device structure and (b) the optical microscope image of device.

A.2.2 BEES Measurement Results

Figure A.6 shows the electrical measurement results of the fabricated BEES device. As shown in Fig. A.6a, the Schottky barrier was formed well with rectifying characteristic. The tunnel current between emitter and the base metal is depicted in Fig. A.6b. The tunnel current-emitter voltage shows the slightly nonlinear characteristic. Confirming the Schottky and tunnel junction is well formed, the BEES measurement was followed. We measured the emitter tunnel current and the collector current simultaneously. As depicted in Fig. A.6c, the collector current abruptly increases at emitter-base voltage is near 1.5 V. Theoretically, the energy barrier between Pt and SiC is known as ~1.7 eV which is very similar to our BEES measurement result.
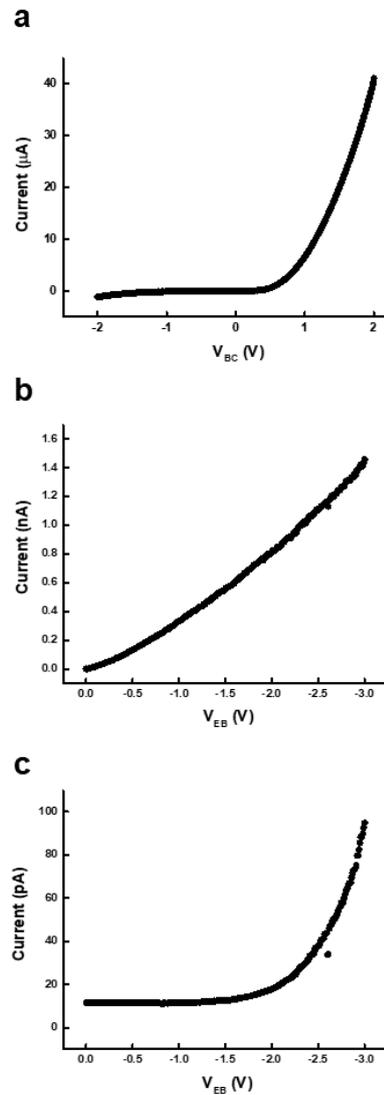
Figure A.6 (a) Current-voltage characteristic of base and collector Schottky junction. (b) Tunnel current-voltage characteristic of emitter and base. (c) Collector current with emitter bias voltage (ballistic electron emission current).

B.   Multi-functional Stretchable Touch Screen Panel (TSP)

In this section, the researches for TSP cooperate with Samsung Display corporation. First, we proposed the force-touch sensing TSP by using a soft bridge insulator. Second, the finger moisture sensing TSP was demonstrated with interdigit patterned electrodes.

B.1 On-Pixel Force-Touch Sensing TSP by Using Soft Bridge Insulator

The touch screen panel (TSP) have been used extensively in tablet PC, smartphone, and security [161]. Since the demands for TSPs has been increasing, researches for TSP with high performance and functionalities are actively studied [162-164]. TSPs can be classified into resistive [165, 166], capacitive [167, 168], surface acoustic wave [169], and infrared [170] TSPs. Among these various types of TSPs, the resistive and capacitive TSPs are widely used in the market.

In case of resistive TSP, the lower and upper electrodes are separated by the small spacer between them. The touched position can be detected by the resistance change through the spacer [171]. The resistive TSPs can be operated regardless of surface contamination and types of touching object. Furthermore, the manufacturing cost and power consumption of resistive TSPs are very low. However, they cannot sense multi-touch and the sensitivity is lower than the other mode TSPs.

The capacitive TSPs are composed of transmission (T_x) and receiving (R_x) electrodes separated with a dielectric material. Initially, the mutual capacitance between T_x and R_x electrodes is formed through the dielectric material and the air. When the grounded conductive thing is touched on TSP, this mutual capacitance is reduced by losing their fringe electric field to grounded material [164, 172]. The advantages of capacitive TSPs are high sensitivity, resolution, and transmission with supporting multi-touch. However, only conductive things can be sensed.

Recently, the pressure sensing or various touching action sensing such as tapping, dragging, and multi-touch are developed and applied to TSPs [173, 174]. The "3D touch" or "Force touch" concept is applied in touch interface by Apple Inc. The 3D touch can sense the applied pressure perpendicular to the TSP as well as the touched position on TSP enabling to detect more various touch motions.

In this experiment, we fabricated three types of pressure sensible TSPs with rigid, flexible, and stretchable substrates. Our TSPs can detect the touch motion, pressure, and force touch on each pixel. This multi-functional TSP is expected to be applicable to future wearable device such as electronic skin.

B.1.1 Device Structure and Fabrication Processes with Various Substrates

The fabrication process of pressure sensing TSP is depicted in Fig. B.1. The first step is forming R_x and T_x electrodes on the substrate. Here, the connected electrodes are R_x electrodes and the disconnected diamond patterned electrodes are T_x. Depending on the substrate type, the first step is different each other.

Step 1 : Rx , Tx Electrodes

Step 2 : Bridge Insulator

Step 3 : Bridge Electrodes

Step 4 : Protective Layer
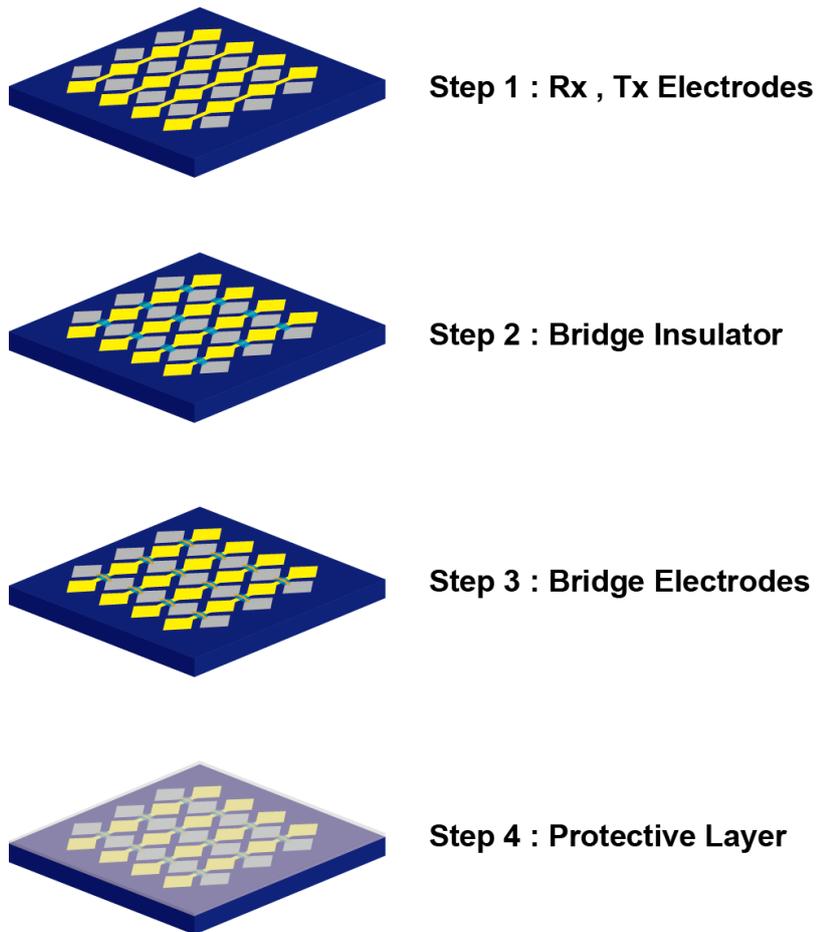
Figure B.1 Fabrication process of on-pixel pressure sensible TSP. Yellow and gray lines represent R_x and T_x. [*In preparation*]

In case of rigid TSP, the quartz substrate cleaned with acetone and methanol by using ultrasonic agitation is prepared as a backplane of TSP. Then, the ITO (Indium Tin Oxide) film is deposited on the whole area of quartz substrate with RF sputtering system (SRN-120, SORONA, Korea). After deposition, the sample is heated in the furnace to make a ITO film transparent (400 °C, 1 hour). Lastly, the conventional photolithography process with AZ5214E photoresist and wet etching process with ITO etchant (LCE-12K) are followed to form the bottom electrode pattern.

For flexible TSP, PC (polycarbonate) film with the pre-deposited AgNW (silver nanowire) is used in this experiment. First, the PC film is cut into pieces of appropriate size and attached to a bare silicon wafer for ease of handle. Next, the AgNW is patterned with conventional photolithography similar to the rigid TSP process and etched with aluminum etchant (Aluminum etchant type A, Transene, USA).

Differently from the other types of TSPs, the substrate of stretchable TSP was made by ourselves. First, the PDMS (Polydimethylsiloxane) is prepared by mixing the silicon elastomer and curing agent with a ratio of 10:1 (SYLGARD, Dow Corning, USA). Then, the PDMS is spin-coated onto a bare silicon wafer and baked in the oven at 100 °C for 20 minutes. Here, the bare silicon wafer just supports the PDMS substrate during the fabrication process and is eventually detached from the PDMS substrate. Next, the sample is treated with the oxygen plasma condition in RIE (Reactive ion etching) system to convert the surface from hydrophobic to hydrophilic. After plasma process, the AgNW solution (dispersed in distilled water) is coated on the PDMS substrate. Then, the sample is baked on a hot plate to evaporate water molecules and only AgNWs are remained on the PDMS surface. Finally, the conventional photolithography and etching process are followed as same as the flexible TSP fabrication process.

The first step of three different types of TSPs are different each other as described in above. However, the fabrication processes from the second step to last step are same for every type of TSPs. In the second step, the soft bridge insulators are formed on the crossing points of R_x and T_x electrodes. As shown in Fig. B.2, the side-wall of bridge insulator has low slope because the bridge electrodes should be connected without any disconnection at the side-wall of bridge insulator. In order to prevent the damages on the R_x and T_x electrodes, the shadow mask method was used in this step. The shadow mask was attached to the sample and PDMS is subsequently spin-coated over the shadow mask. After detaching the shadow mask, we waited for a while to make a shape of the bridge insulator from rectangular parallelepiped to hemisphere. Completing the spread of PDMS, the baking process is followed to cure the bridge insulator. The cross-section profile of bridge insulator was measured by using the surface profiler (KLA Tencor, P6, USA) as shown in Fig. B.2b. Since the cross-sectional profile is the semi-elliptical shape with a low side-wall slope, the bridge electrode can be formed without any damage on the sides of the bridge insulator. Without this structure, the bridge electrode connection can be very poor or have high resistance [175].
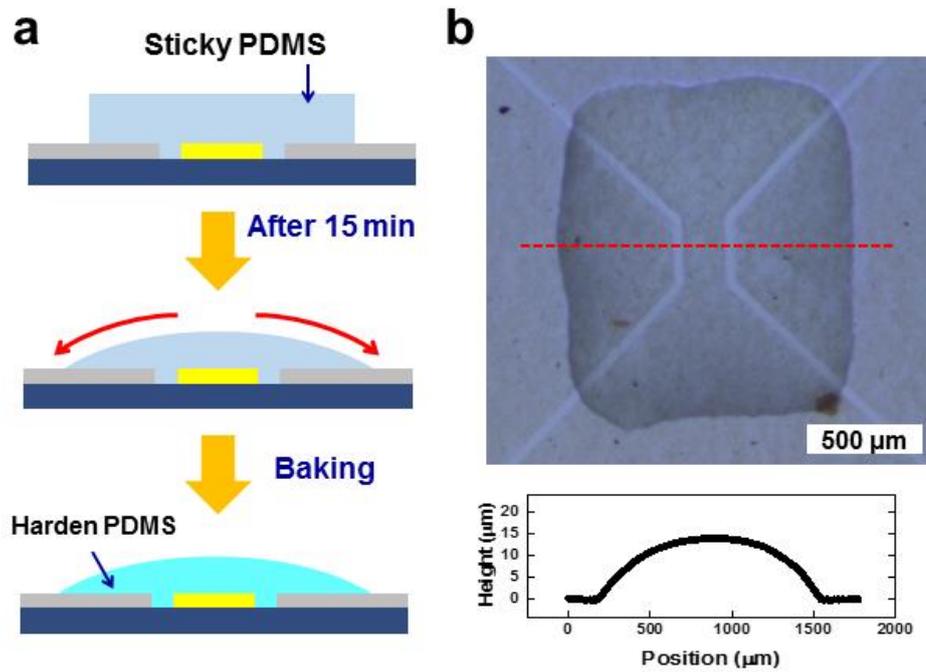
Figure B.2 (a) Detailed fabrication process of forming bridge insulator. (b) The optical microscope image and the cross-sectional profile of the bridge insulator. [*In preparation*]

The third step is forming a bridge electrode on the soft bridge insulator. The AgNW was used for a bridge electrode because the AgNW random network can maintain the conductivity on stretchable substrate [176, 177]. The shadow mask was attached to the sample aligned with bridge insulator. Then, the exposed area is treated with oxygen plasma for better adhesion of AgNWs. Next, the AgNW solution is spin-coated over the shadow mask and the sample is baked on the hot plate. After evaporating the water molecules, the shadow mask is detached from the sample.

The last step is forming the protective layer on whole are of the sample. The PDMS is spin-coated on the sample at 5000 rpm for 60 seconds. Finally, the PDMS protective layer is cured in the oven at 100 °C for 10 minutes. Silicon bare wafers attached as a backplane of flexible and stretchable TSP are detached from the sample at the end of the fabrication process.

B.1.2 Touch/Pressure/Force Touch Sensing

In Fig. B.3, the capacitance changes by touch or pressure for three different types of TSPs are shown. The y-coordinates represent the ratio of capacitance change with respect to the initial capacitance ($\Delta C / C_0$). All TSPs has reduced capacitance value when the finger is touched to the surface of TSPs. The capacitance change ratio is -17.5 % for rigid TSP (Fig. B.3a), -7 % for flexible TSP (Fig. B.3c), and -5 % for stretchable TSP (Fig. B.3e). The reason for the decrease of capacitance is shown in Fig. B.3g. Some amount of electric fringe field from T_x to T_x electrodes can be absorbed by the touched finger. Then, the incoming electric field lines to T_x electrode is reduced so that the measured capacitance decreases. When the touched finger is detached from the TSP, the capacitance instantaneously goes back to initial value as shown in our measurement results.

In case of pressure sensing, we applied pressure with insulating material on the bridge electrode. The capacitance change ratio of rigid TSP, flexible TSP, and stretchable TSP are 13.1 % (Fig. B.3b), 7.1 % (Fig. B.3d), and 4.5 % (Fig. B.3f) at 28 kPa pressure. The capacitance change ratio vs. pressure curves of three different types of TSPs have similar shape. At the small pressure (less than 10 kPa), the capacitance increases drastically. However, as the applied pressure increases the capacitance change ratio increases slowly.

The capacitance change by applied pressure can be explained by using a simple parallel capacitor model. The capacitance of simple parallel capacitor is determined by the dielectric constant of insulating material, area of electrodes, and distance of two electrodes.

$$C = \varepsilon_0 \varepsilon_r \left(A/d \right) \tag{B. 1}$$

Here, ε_0 is the vacuum permittivity, ε_r the relative dielectric constant of insulating layer, A the area of parallel capacitor, and d the distance between two electrodes. The bridge electrode and the R_x electrode can be considered as two electrodes of a parallel capacitor and the bridge insulator as an insulating layer. When the pressure is applied to the bridge insulator, the distance between the bridge electrode and the R_x electrode is closer than the initial state because the bridge insulator is soft material so that it deforms its shape by external pressure. Then, the capacitance between the bridge electrode and R_x electrode can be reduced. One more thing we can notice in pressure sensing measurement results is that the capacitance change ratio of stretchable TSP is smaller than the other two types of TSPs. This can be explained by the deformation of substrate by external pressure since the substrate is also soft material. Therefore, the applied pressure is not fully contributed to the deformation of the bridge insulator.
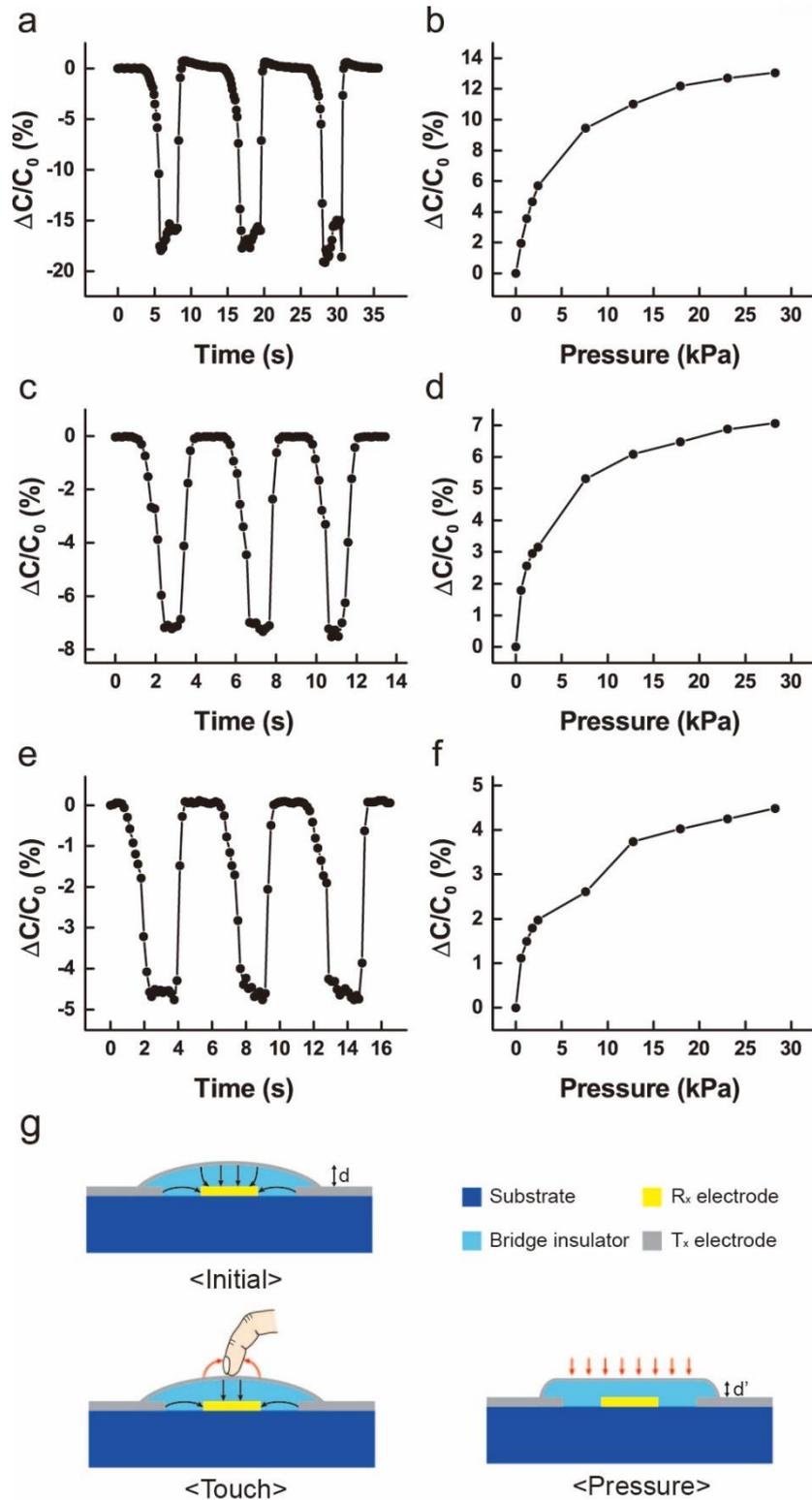
Figure B.3 The capacitance change ratio at touch for (a) rigid TSP, (c) flexible TSP, and (e) stretchable TSP. The ratio at external pressure for (b) rigid TSP, (d) flexible TSP, and (f) stretchable TSP. (g) The schematic of the principle of touch and pressure sensing. [*In preparation*]
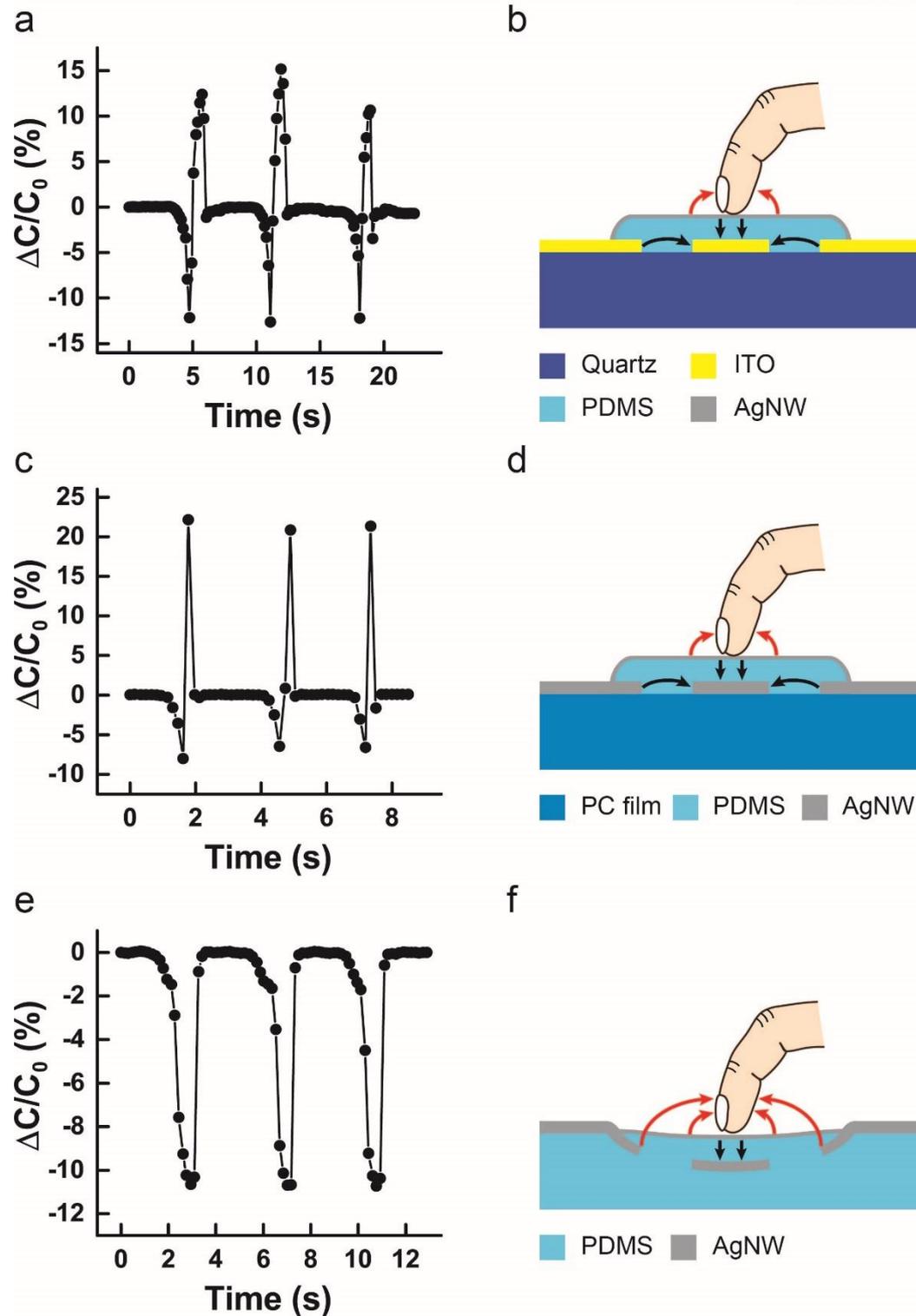
Figure B.4 The capacitance change ratio at force touch for (a) rigid TSP, (c) flexible TSP, and (e) stretchable TSP. The schematic diagram of a deformation of the bridge insulator and the corresponding electric field lines at force touch for (b) rigid TSP, (d) flexible TSP, and (f) stretchable TSP. Red arrows represent the electric field loss by the touched finger and black arrows mean the electric field from T_x to R_x electrodes. [*In preparation*]

Based on the touch and pressure sensing measurement, we tried to measure the capacitance change at force touch which is the combination of touch and pressure. The force touch measurement results are shown in Fig. B.4. In case of rigid TSP, the capacitance is decreased very quickly (-10 %) at first and increased again (10 %) as shown in Fig. B.4a. Similarly, the capacitance of flexible TSP is also decreased momentarily at first (-7 %) and abruptly increased (20 %) depicted in Fig. B.4c. These results can be expectable because the force touch is the combination of touch and pressure so that the capacitance is decreased at touching moment and increased by the reduction of thickness of the bridge insulator. Therefore, the capacitance change by external pressure is more dominant than the electric field loss by touching in these two types of TSPs.

However, the capacitance is not increased again in case of stretchable TSP. As shown in Fig. B.4e, the capacitance is just decreased by force touch. Considering the capacitance change ratio at normal touch case for stretchable TSP (Fig. B.3e) is -5 %, the reduction of capacitance is much larger in case of force touch (-11 %). This can be happened by deformation of substrate by force touch. As measured before, the rigid and flexible TSPs have a sharp increase after the momentary decrease due to the reduced thickness of the bridge insulator. However, in pressure sensing measurement, the stretchable TSP has lower capacitance change by external pressure because of the deformation of substrate. Therefore, we can expect that the bridge insulator is not decreased much in force touch case. Instead, the number of electric field lines captured by touched finger can be increased by deformation of substrate as shown in Fig. B.4f. Thus, we cannot distinguish the force touch and normal touch in this stretchable TSP. In order to overcome this problem, the substrate should be changed with higher Young's modulus or smaller thickness to reduce the deformation of substrate.

Since the capacitance is increased with the applied pressure, we measured the capacitance change by force touch with various pressure. As shown in Fig. B.5, the more pressure is applied during force touch, the larger increase of capacitance is measured.
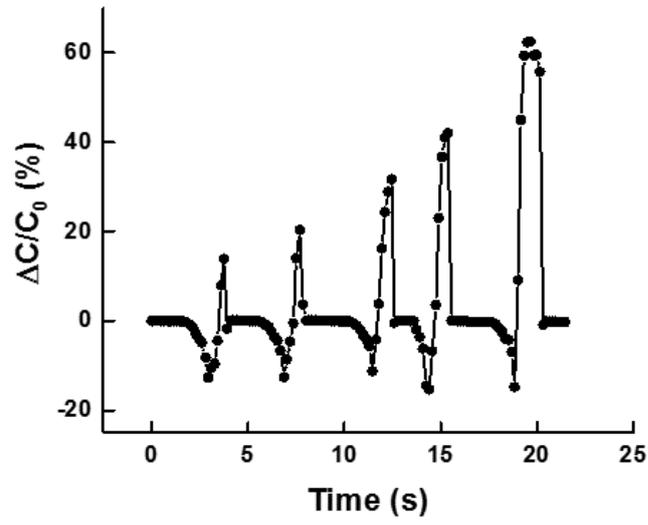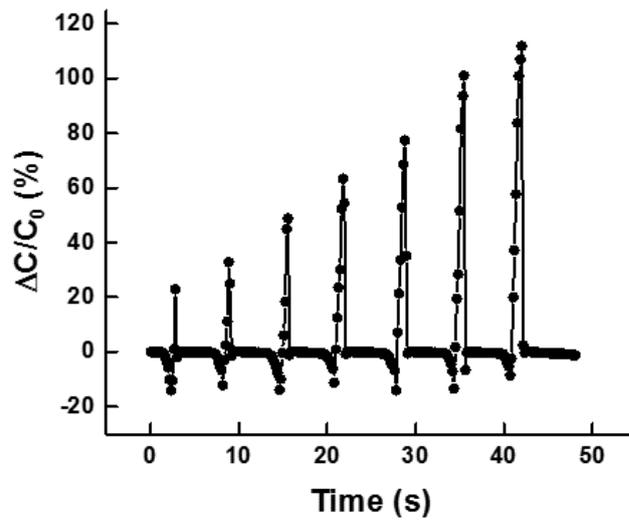
Figure B.5 The capacitance change by force touch with different strength in (a) rigid TSP and (b) flexible TSP. [*In preparation*]

Lastly, we measured the transmittance of rigid, flexible, and stretchable TSPs in the visible light region as depicted in Fig. B.6. The transmittance value at 550 nm is 77 % for rigid TSP, 88 % for flexible TSP, and 81 % for stretchable TSP. The inset images are optical images of fabricated TSPs showing their transparency.
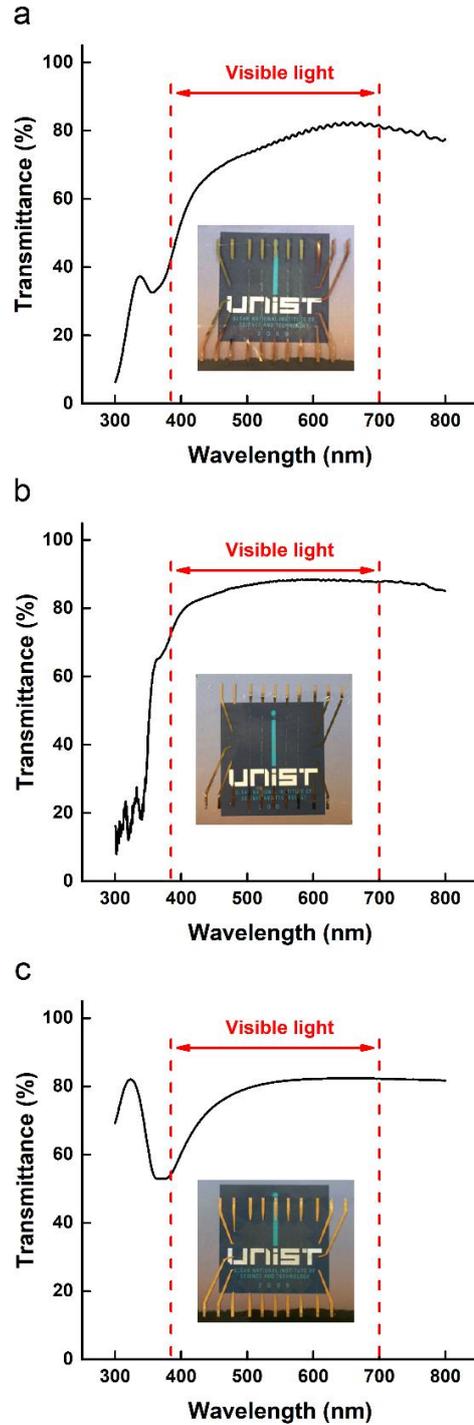
Figure B.6 Transmittance and the optical images of (a) rigid TSP, (b) flexible TSP, and (c) stretchable TSP. [*In preparation*]

100

In summary, we fabricated pressure sensible TSPs by using rigid, flexible, and stretchable substrates. The soft bridge insulator enables to sense the external pressure by the capacitance changed due to the reduced thickness. Our fabricated TSPs have high sensitivity in touch, pressure, and force touch. However, the stretchable TSP has limitation of force touch owing to the deformation of substrate. This problem can be solved by reducing the deformation of substrate during force touch. Moreover, the force touch varying strength was also distinguishable in rigid and flexible TSPs. With this structure, the pressure can be sensed in each pixel with high resolution and applicable to current commercialized TSPs.

B.2 Moisture Sensible TSP with Interdigit Pattern

B.2.1 Interdigit Pattern for Moisture Sensing

The commercialized interdigit patterned moisture sensors are using the capacitance change by skin moisture. As shown in Fig. B.7, the interdigit patterned electrode forms an electric field with penetration depth [178, 179]. The stratum corneum is the outermost part of skin and contains the moisture [180]. When the skin is touched to the interdigit electrodes (Fig. B.7c), the electric fringe field can go through the stratum corneum. Then, the moisture in stratum corneum can be contributed to the capacitance between interdigit electrodes. Since the dielectric constant of water is much larger than the air [181], the capacitance can be significantly increased by skin moisture [182].
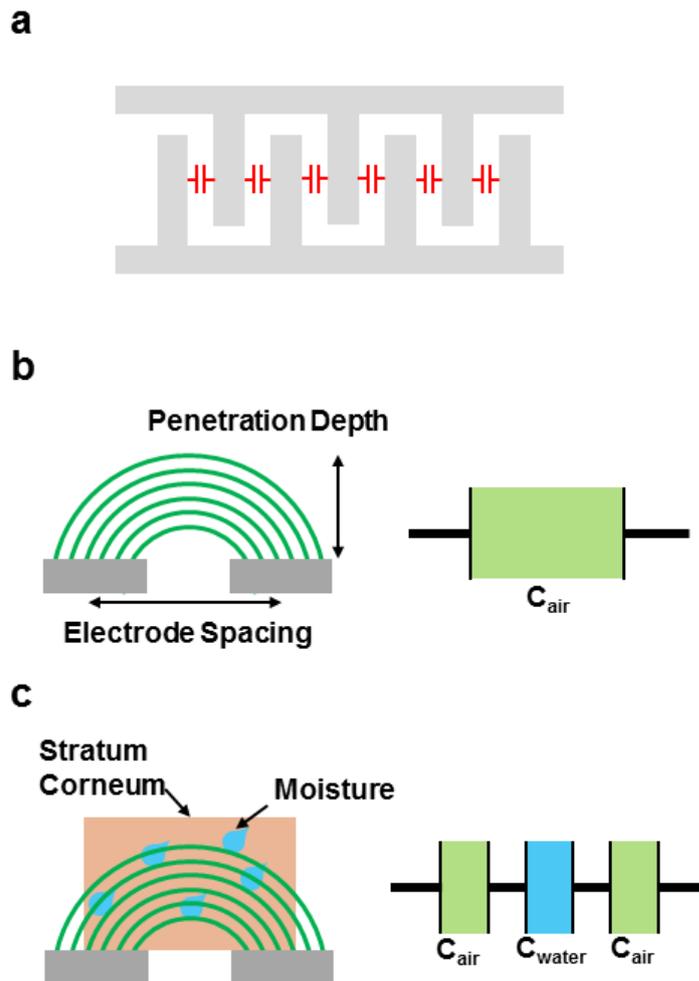
Figure B.7 (a) Interdigit patterned electrodes with mutual capacitance. The electric field line (green) and capacitor model for (b) interdigit electrodes and (c) electrodes with skin moisture. [*In preparation*]

B.2.2 Fabrication Processes of Multilayer Structure TSP

The fabrication process of moisture sensible TSP is shown in Fig. B.8. First, the bottom electrode is formed on a substrate. Then, the whole area of sample is covered by an insulating layer. Finally, the interdigit patterned top electrode is formed on insulting layer.

In this experiment, we only used the AgNWs as our electrode material and PDMS as a substrate and an insulting layer. The fabrication processes are very similar to the method for making stretchable force touch sensing TSP. The PDMS substrate was made by using spin coating on barer silicon wafer and curing process in the oven. Before the patterning electrodes, the oxygen plasma treatment was preceded to make the surface hydrophilic. The insulating layer was also spin-coated by using PDMS.

Bottom Electrode   **Insulating Layer**   **Top Electrode**
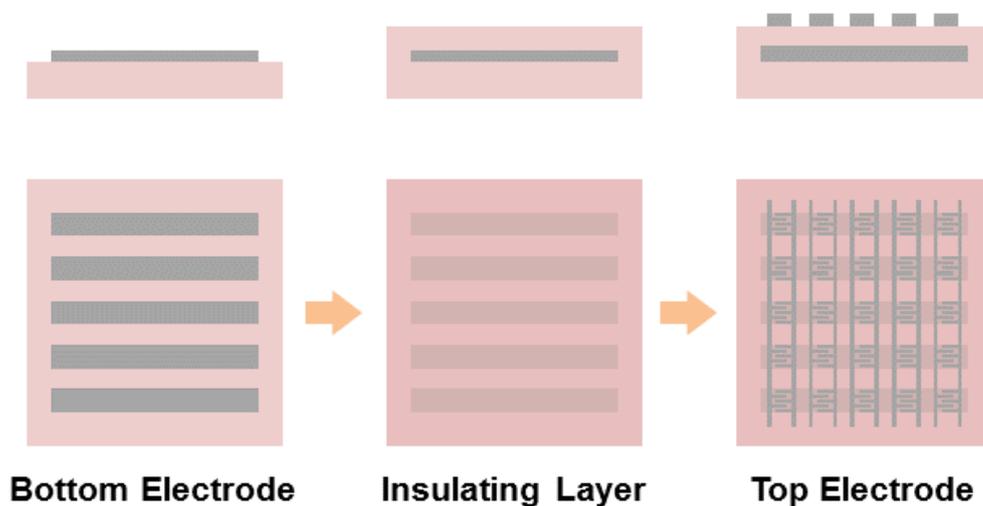
Figure B.8 The fabrication process of moisture sensible TSP. [*In preparation*]

B.2.3 Touch/Pressure/Moisture Sensing Measurement Results

As described in fabrication process, the insulating layer between top and bottom electrodes is PDMS so that the thickness can be changed by the external pressure. Therefore, moisture sensible TSP can also measure the applied pressure with the same principle of force touch sensing TSP. In other words, the moisture sensible TSP is a combination of moisture sensor and the force touch sensing TSP. One very important difference is that the moisture sensible TSP uses the different R_x lines during the moisture sensing mode. The touch and pressure sensing are performed with the bottom electrode and top electrode. However, the moisture should be sensed by two interdigit patterned top electrodes. The schematic diagram for three different sensing modes are depicted in Fig. B.9.
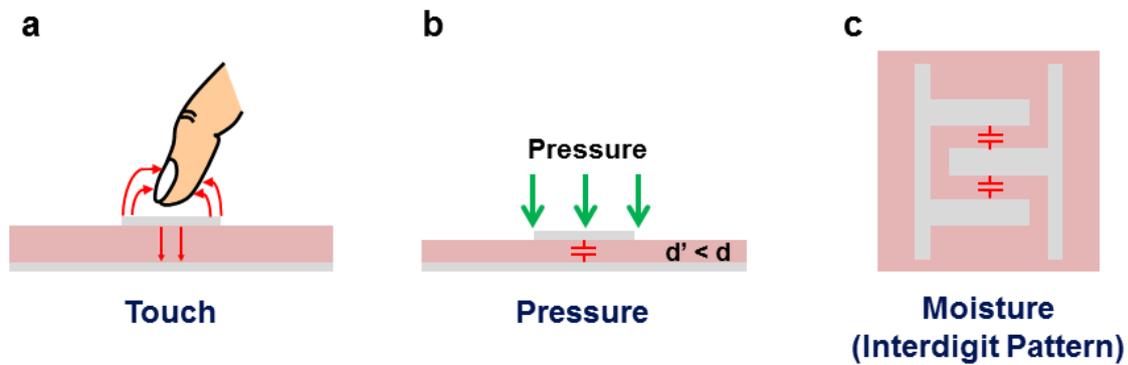
Figure B.9 The schematic diagram for (a) touch, (b) pressure, and (c) moisture sensing modes. [*In preparation*]

Since we have two paired top electrodes in one line, we can choose any one of them as a T_x electrode line and bottom electrode as R_x line in case of touch and pressure sensing. The capacitance measurement results for touch and pressure sensing are shown in Fig. B.10. As shown in Fig. B.10, the sensitivity of touch is very high (-80 % change). This high sensitivity can be explained by the interdigit pattern of top electrodes. During touching, the electric field loss is mainly from the fringe field as shown in Fig. B.9a. Since the interdigit pattern has quite long boundary line, the electric fringe field can be formed much compared to the simple straight line. Therefore, much of the electric fringe field can be captured by the grounded finger resulting the large capacitance reduction in touching mode. In pressure sensing, the capacitance change curve is similar to the previous research of force touch sensing TSP. The capacitance increases as the applied pressure becomes larger.
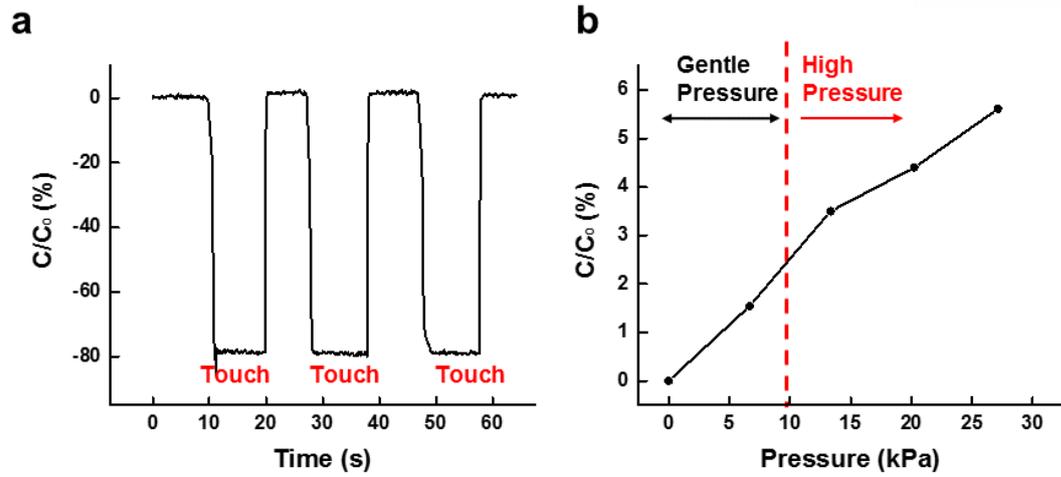
Figure B.10 The capacitance change ratio for (a) touch and (b) pressure. [*In preparation*]
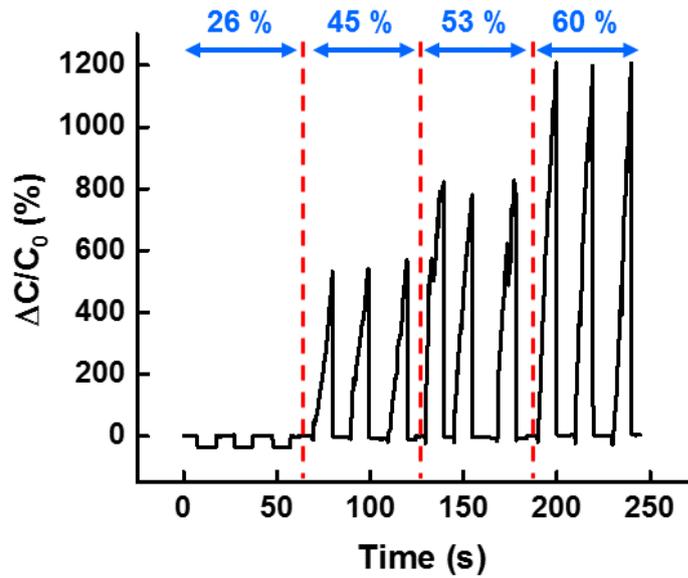
Figure B.11 Capacitance change ratio for moisture sensing at 26 %, 45 %, 53 %, and 60 % of skin moisture measured by commercialized sensor. The interdigit pattern spacing is 100 μm and the measurement frequency is 10 kHz. [*In preparation*]

In Fig. B.11, the capacitance change ratio for moisture sensing is shown. Before touching the finger to our fabricated TSP, the skin moisture content was measured by commercialized sensor. At 26 % of moisture content, the capacitance was decreased as opposite to expectation. However, as moisture content increases, the capacitance change ratio becomes positive and increases up to 1200 %. Here, we can notice that the skin moisture can induce the larger capacitance value, but there is electric field loss during touch. These two effects are competitive to determine the final capacitance value. However, the moisture contents measured by commercialized sensor is proportional to the capacitance change of our moisture sensible TSP. Therefore, the skin moisture content can be precisely measured after quantification of our measurement results.

Next, we performed the moisture sensing measurement depending on the operating frequency. Figure B.12a shows the capacitance change ratio with various frequencies by using 60 % of moisture content finger. Figure B.12b is the other research results for the capacitance change by water contents depending on the frequency [182].

a

b

Copyright (2001), with permission from Elsevier
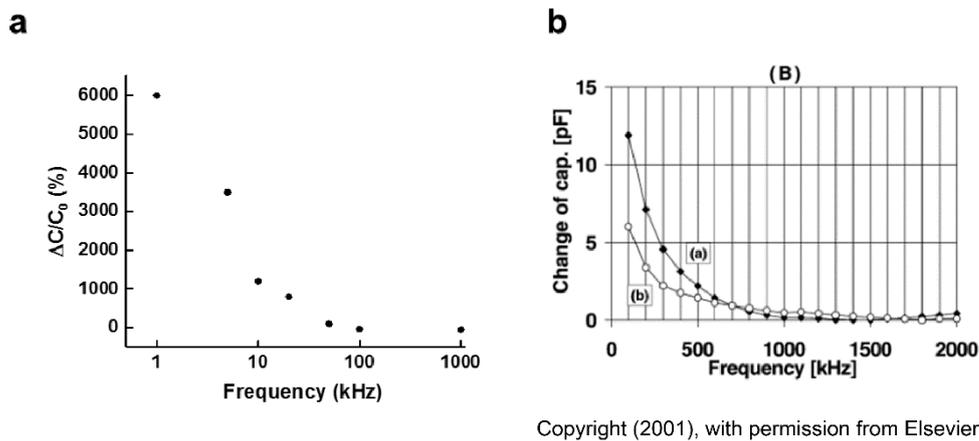
Figure B.12 (a) The capacitance change ratio by 60 % moisture content finger at various frequencies. (b) The capacitance change by water content in frequency domain results by N. Sekiguchi *et al* [182].

In the measurement of our fabricated TSP, the capacitance change ratio is 6000 % for 1 kHz, 3500 % for 5 kHz, 1200 % for 10 kHz, 800 % for 20 kHz, 100 % for 50 kHz, -40 % for 100 kHz, and -50 % for 1MHz. Here, two important characteristics are shown depending on the operating frequency. First, as similar to the previous research by N. Sekiguchi *et al*, the capacitance change decreases with the increase of frequency. Considering the capacitance measurement mechanism, we can explain this phenomenon with impedance equation.

$$Z = \frac{1}{2\pi f \times C} \qquad (B.2)$$

Here, Z is the impedance of the capacitor, f the frequency, and C the capacitance. As described in the Eq. B.2, the impedance of the capacitor can be expressed by the frequency and the capacitance. In the actual measurement, the induced charge is measured for oscillating voltage with specific frequency. In other words, the capacitance measurement can be determined by the impedance of the circuit. During sensing the moisture, the capacitance is increased by skin moisture and the impedance becomes smaller. At a lower frequency, the $1/2\pi f$ becomes larger so that the impedance change is much greater compared to the high frequency at the same amount of capacitance change by skin moisture. Therefore, the capacitance change ratio is decreasing function of frequency. Second, the capacitance is decreased at very high frequencies such as 100 kHz and 1 MHz. At a high frequency, the capacitance change by the skin moisture has very little effect on impedance change because the $1/2\pi f$ is too small. Meanwhile, the electric field loss by touched finger is still remained so that the total capacitance change becomes negative.

Although our fabricated moisture sensible TSP can detect the touch, pressure, and skin moisture, the driving frequency of moisture sensing mode (10 to 50 kHz) is much lower than the operating frequency of commercialized TSPs (200 kHz). Therefore, we fabricated moisture sensible TSP that can be operated in high frequency. The solution for an increase of operating frequency was also from the impedance equation (Eq. B.2). Experimentally, we found the range of impedance that can be measured in our system. Since the impedance was determined by the product of frequency and the capacitance, we have the same initial impedance when the product of them is not changed even though we have different frequency and capacitance value. Therefore, we decided to reduce the initial capacitance to achieve the high operating frequency. In previous experiment, 50 kHz was the limit for operating frequency with 100 μm electrode spacing. In order to operate the moisture sensing TSP at 200 kHz, the electrode spacing should be larger than 400 μm. Thus, we fabricated moisture sensible TSP with electrode spacing of 500 μm. Then, the capacitance was measured at 200 kHz frequency for moisture sensing. Figure B.13 shows the capacitance change ratio at 50 %, 60 %, and 90 % of moisture content. The change ratio is 2,000 % for 50 % moisture, 5,000 % for 60 % moisture, and 11,000 % for 90 % moisture. Compared to the moisture sensing at 100 μm electrode spacing TSP, the capacitance change ratio becomes significantly larger. The possible explanation for this result is that the initial capacitance is smaller than before so that the capacitance increase or impedance decrease by skin moisture becomes much bigger.
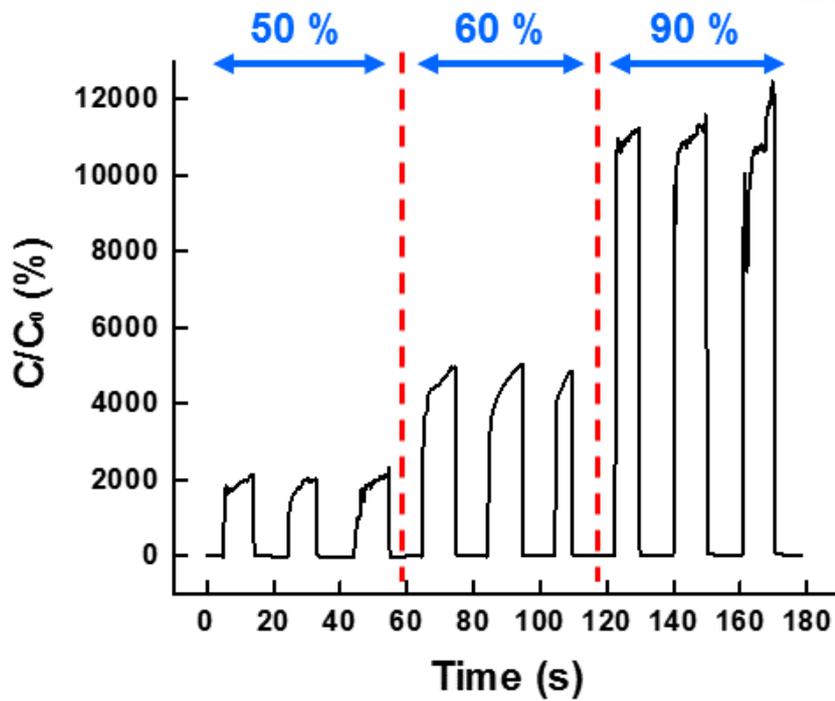
Figure B.13 The capacitance change ratio for moisture sensing at 50 %, 60 %, and 90 % of skin moisture measured by commercialized sensor. The interdigit pattern spacing is 500 μm and the measurement frequency is 200 kHz. [*In preparation*]
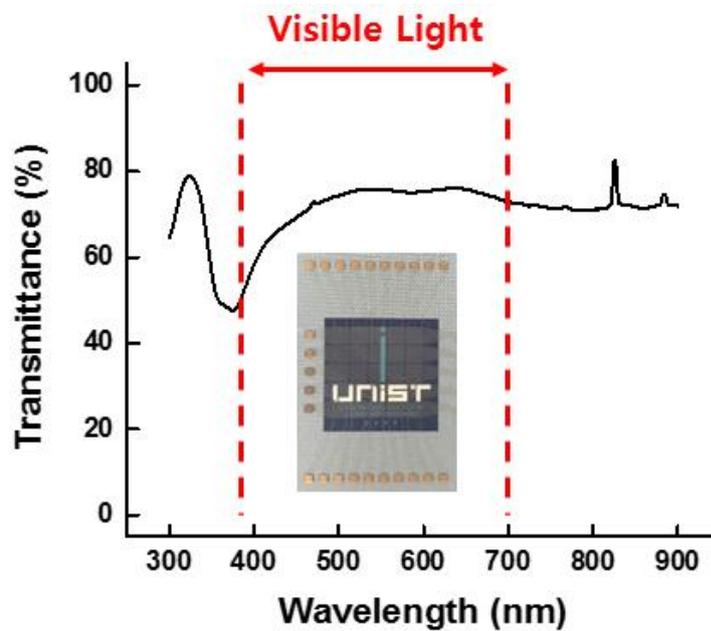
Figure B.14 Transmittance and the optical images of moisture sensible TSP. [*In preparation*]

In Fig. B.14, the transmittance measurement result and optical images of fabricated moisture sensible TSP. The transmittance value at 550 nm wavelength is about 75 %.

In conclusion, the moisture sensible TSP was fabricated by using AgNWs and PDMS. Our fabricated TSP can detect the touch, pressure, and skin moisture content. Interdigit patterned top electrode designed to moisture sensing was helpful to sensitivity of touch sensing because it has much of the electric fringe field than a simple straight line pattern. In case of moisture sensing, the frequency and electrode spacing were the significant factor. As the frequency becomes smaller, the capacitance change by moisture becomes larger. The electrode spacing was determining factor for an initial capacitance of interdigit pattern so that the larger spacing gives high operating frequency limit considering the Eq. B.2. In this study, we confirmed that the moisture sensing function can be equipped to TSP by using simple interdigit patterned electrodes.

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